Compal Confidential

CML-H MB Schematic Document

LA-J561P

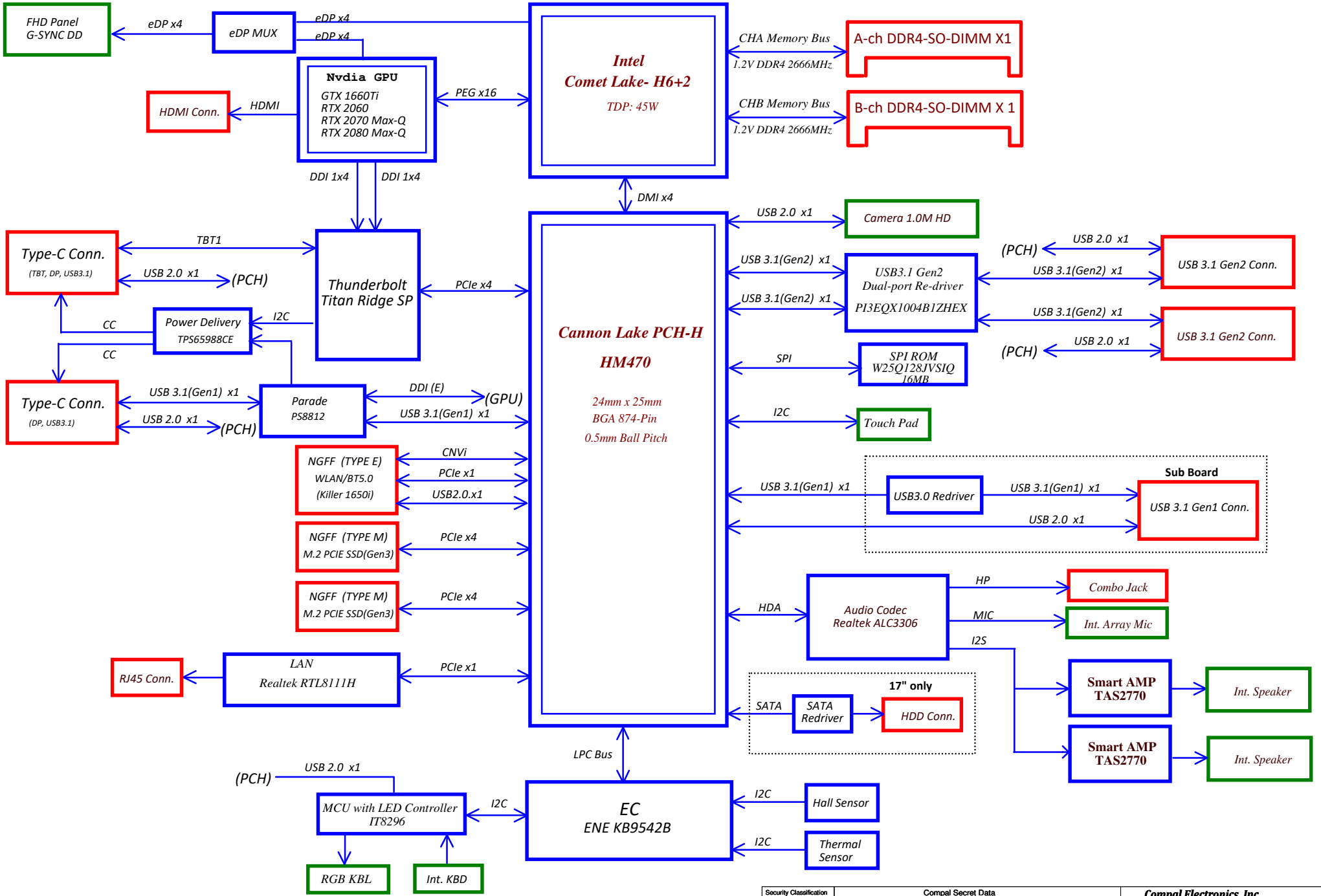
Rev: 1.0

2020.02.26

Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.		
Title: Cover Sheet		
Size: Custom	Document Number: LA-J561P	Rev: 0.2
Date: Wednesday, February 26, 2020	Sheet 1 of 100	

Comet Lake H Block Diagram



Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.			
Title	CFL-H 6+2 Block Diagram		
Size	Document Number		Rev
Custom	LA-J561P		1.0
Date:	Wednesday, February 26, 2020	Sheet	2 of 100

Board ID Table for AD channel

Vcc	3.3V +/- 1%
Ra	100K +/- 1%

Board ID /PCB Revision	Rb	V_{AD_BID} min	V_{AD_BID} TYP	V_{AD_BID} Max	EC AD3
0 --> 0.1	0		0 V	0.300 V	0x00 - 0x13
1 --> 0.2	12K +/- 1%	0.347 V	0.354 V	0.36 V	0x14 - 0x1E
2 --> 0.3	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25
3 --> 0.4	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30
4 --> 0.5	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A
5 --> 0.6	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45
6 --> 0.7	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54
7 --> 0.8	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64
8 --> 0.9	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65 - 0x76
9 --> 1.0	100K +/- 1%	1.634 V	1.650 V	1.667 V	0x77 - 0x87
10 --> 1.1	130K +/- 1%	1.849 V	1.865 V	1.881V	0x88 - 0x96
11 --> 1.2	160K +/- 1%	2.015 V	2.031 V	2.046 V	0x97 - 0xA4
12 --> 1.3	200K +/- 1%	2.185 V	2.200 V	2.215 V	0xA5 - 0xAF
13 --> 1.4	240K +/- 1%	2.316V	2.329V	2.343V	0xB0 - 0xB7
14 --> 1.5	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xBF
15 --> 1.6	330K +/- 1%	2.521 V	2.533V	2.544 V	0xC0 - 0xC9
16 --> 1.7	430K +/- 1%	2.667 V	2.677 V	2.687 V	0xCA - 0xD4
17 --> 1.8	560K +/- 1%	2.791 V	2.800 V	2.808 V	0xD5 - 0xDD
18 --> 1.9	750K +/- 1%	2.905 V	2.912 V	2.919 V	0xDE - 0xF0
19 --> 2.0	NC	3.000 V	3.000 V		0xF1 - 0xFF

HSIO Port Table(CPU)

HSIO Port	Device	PCIE CLK&CLKREQ	HPD
PEG	DGPU (DIS)	CLK4 & & CLKREQ#4	
DDI1	NA		NA
DDI2	NA		NA
DDI3	NA		NA
eDP	Embedded Display		EDP_HPD

Power State

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

PCH SMBUS Address Table

PCH_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
PCH_SMBCLK PCH_SMBDATA	+3V_PCH_PRIM	JDIMM1	0X50	0XA0	0XA1
		JDIMM3	0X52	0XA4	0XA3
PCH_SML0CLK PCH_SML0DATA	+3VS	NA			
PCH_SML1CLK PCH_SML1DATA	+3VS	EC	TBC	TBC	TBC

EC SMBUS Address Table

EC_SMBUS Port	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
SMBUS Port1 EC_SMB_CK1 EC_SMB_DA1	+3VLP_EC	BAT	0x16	TBC	TBC
		CHGR	0x09	0x12	0x13
		TBT	Reserved	TBC	TBC
SMBUS Port2 EC_SMB_CK2 EC_SMB_DA2	+3VS				
		PCH	TBC		
		GPU	0x9E/0x9F	TBC	TBC
		Type-C PS8812			
		THERMAL	0x4D	0x9A	0x9B
		USB3.1 re-driver	0x29	0x52	0x53
SMBUS Port4 EC_SMB_CK4 EC_SMB_DA4	+3VS	KB/LED Controller	0x1F	0x3E	0X3F
			TBC		

I2C Address Table

I2C Port	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
I2C_0_SCL I2C_0_SDA	+3VS				
		EC KB9542	TBC	TBC	TBC
I2C_1_SCL I2C_1_SDA	+3VS	Touch Pad	0x15	TBC	TBC

Voltage Rails

Power Plane	Description	S0	S0ix	S3	S4/S5	DS3
VIN	Adapter power supply	N/A	N/A	N/A	N/A	N/A
BATT+	Battery power supply	N/A	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A	N/A
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF	OFF
+VCC_SA	System Agent voltage Supply	ON	OFF	OFF	OFF	OFF
+VCC_GT/+VCC_GTX	Sliced graphics power rail	ON	OFF	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF	OFF	OFF
+VCC_EOPIO/+VCC_EDRAM	Processor EOPIO/EDRAM supply	ON	OFF	OFF	OFF	OFF
+1.05VALW	System +1.0V power rail	ON	ON	ON	ON*	OFF
+0.95VS_VCCIO	+1.0VS IO power rail	ON	ON	OFF	OFF	OFF
+1.05V_VCCMPHY	+1.0V power for PCH MODPHY rails	ON/OFF	ON/OFF	ON/OFF	ON/OFF	OFF
+0.95VS_DGPU	+0.95VS power rail for GPU	ON	OFF	OFF	OFF	OFF
+1.2V_VDDQ	DDR4 +1.2V power rail	ON	ON	ON	OFF	ON
+1.5VS_MEM_GFX	+1.5VS power rail for GPU/VRAM	ON	OFF	OFF	OFF	OFF
+1.8VALW	System +1.8V power rail	ON	ON	ON	ON*	OFF
+1.8VS	System +1.8VS power rail	ON	ON	OFF	OFF	OFF
+1.8VGS	+1.8VS power rail for GPU	ON	OFF	OFF	OFF	OFF
+2.5V	DDR4 +2.5Vpp power rail	ON	ON	ON	OFF	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*	ON
+3VALW	+3VALW power for PCH suspend rails	ON	ON	ON	ON*	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON*	ON
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON	ON
+3VS	System +3VS power rail	ON	ON	OFF	OFF	OFF
+3VGS	+3VS power rail for GPU	ON	OFF	OFF	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON	ON*	ON
+5VS	System +5VS power rail	ON	ON	OFF	OFF	OFF
+3VL_RTC	RTC power	ON	ON	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

BOM Structure Table (1/2)

Function	Stuff	Note
Unit SKU	UMA@	
	DIS@	
Project SKU	15@	
	17@	
CFL-H SKU	CPU1@	i5-9400H-R1
	CPU2@	i9-9880H-R1
	CPU3@	i9-9980HK-R1
DGPU SKU	N18G0@	
	N18G1@	
	N18G2@	
	N18G3@	
PCH SKU HM370	PCH1@	HM370 QNYF
N18 x SKU	GPU1@	1660Ti-G0-R1
	GPU2@	2060-G1-R1
	GPU3@	2070-G2-R1
	GPU4@	2080-G3-R1
VRAM 6G	M6G@	X7685138L01
	S6G@	X7685138L02
VRAM 8G	M8G@	X7685138L03
	S8G@	X7685138L04
Intel RTD3	RTD3@	
	NORTD3@	
eSPI I/F	ESPI@	
	LPC@	
Debug	CMC@	
Panel SKU	GSYNC@	
	NOGSYNC@	
Intel TBT TR	TBT@	
Intel CNVi	CNVI@	
LAN Mode	8111H_SW@	
	8111H_LDO@	
FIN FPC	FIN1@	IT8296 Control
	FIN2@	
OVRM	ON@	NCP45491
	UPI@	US5650PQKI
ME Connector	ME@	
EMI Components	EMI@	@EMI@
ESD Components	ESD@	@ESD@
RF Components	RF@	@RF@

HSIO Port Table(PCH) HM470

HSIO Port	Capable	USB3.0	PCIE	SATA	Device	PCIE CLK&CLKREQ	NOTE
0	USB3.1_1(OTG)	1			USB3.1 PORT 2		Left Back
1	USB3.1_2	2			USB3.1 PORT 1		Right Back
2	USB3.1_3	3			USB3.1 PORT 3		Right Fornt
3	USB3.1_4	4			USB3.1 PORT 4		Left Fornt
4	USB3.0_5	5					
5	USB3.0_6	6					
6	USB3.0_7	7					
7	USB3.0_8	8					
8							
9							
10							
11							
12							
13							
14	PCIE_9 / GbE		9		NGFF SSD2	CLK5 & & CLKREQ#5	
15	PCIE_10		10				
16	PCIE_11 / SATA_0A		11	0			
17	PCIE_12 / GbE / SATA_1A		12	1			
18	PCIE_13 / GbE / SATA_0B		13	0	HDD		
19	PCIE_14 / SATA_1B		14	1	LAN	CLK2 & & CLKREQ#2	
20	PCIE_15		15	2	WLAN+BT NGFF	CLK3 & & CLKREQ#3	
21	PCIE_16		16	3			
22	PCIE_17 / SATA_4		17	4	Thunderbolt Intel Titan Ridge SP	CLK0 & & CLKREQ#0	
23	PCIE_18 / SATA_5		18	5			
24	PCIE_19		19				
25	PCIE_20		20				
26	PCIE_21		21		NGFF SSD1	CLK1 & & CLKREQ#1	
27	PCIE_22		22				
28	PCIE_23		23				
29	PCIE_24		24				

USB2.0 Port Table

USB2	Function
1	USB3.1 PORT 2
2	USB3.1 PORT 1
3	USB3.1 PORT 3
4	LED Controller IT8296
5	TBT TYPE-C
6	Camera
7	DP TYPE-C
8	
9	
10	
11	
12	
13	
14	WLAN+BT NGFF

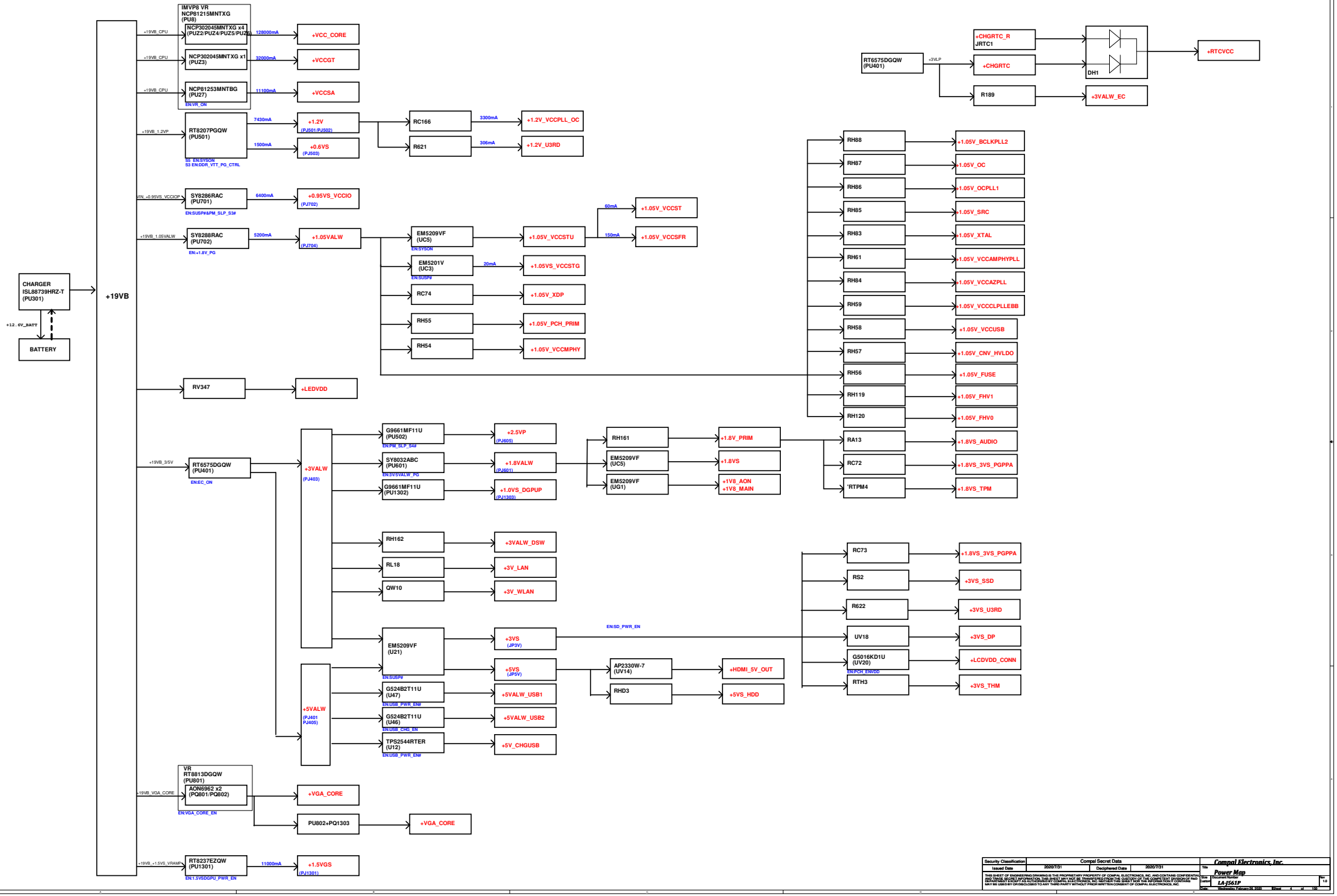
Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

Title: Notes List

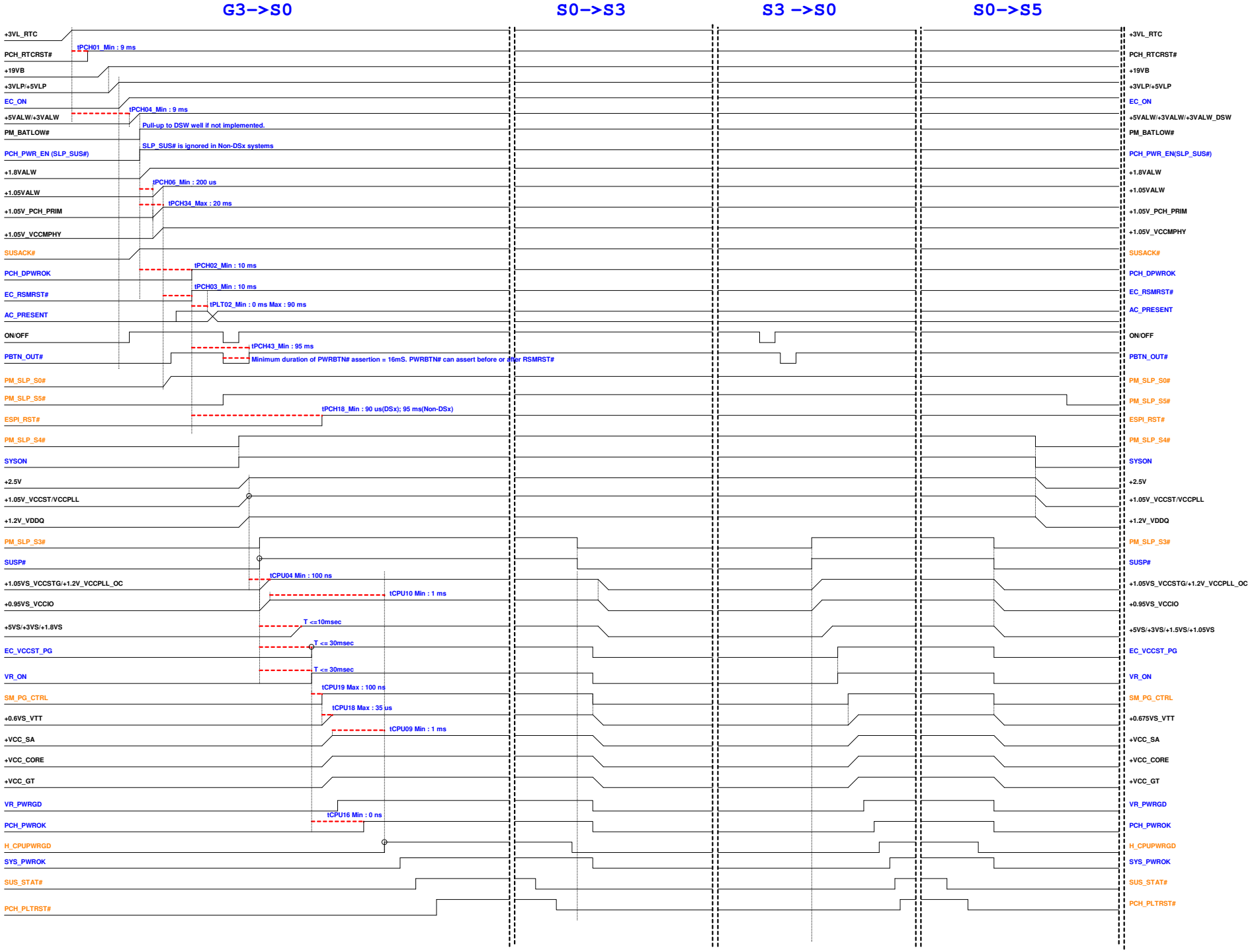
Size: Custom | Document Number: LA-J561P | Rev: 1.0

Date: Wednesday, February 26, 2020 | Sheet 3 of 100



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/7/31	Deciphered Date 2020/7/31	Title: Power Map
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size: Document Number: LA-J561P Rev: 1.0
			Date: Wednesday, February 26, 2020 Sheet 4 of 100

[DDX03 PWR Sequence_CFL-H 6+2_DDR4]



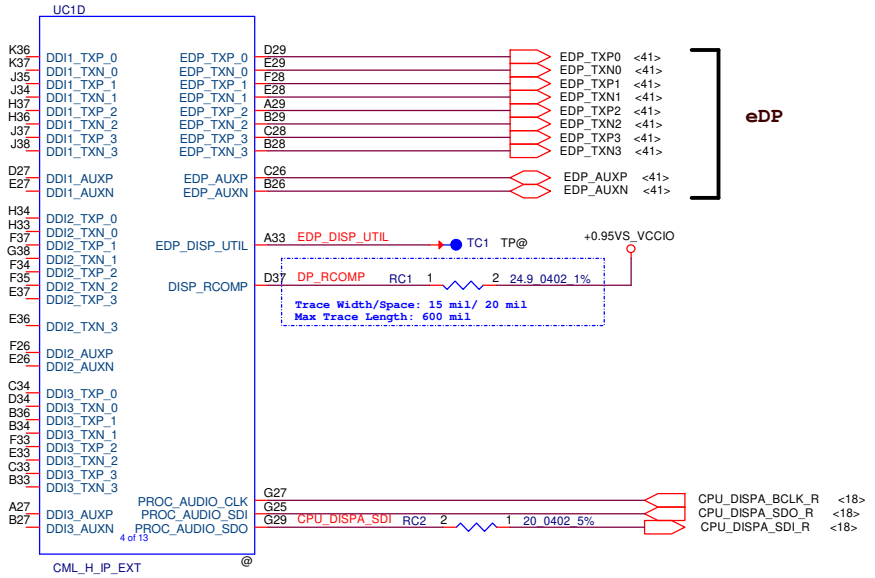
Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

Title: Power Sequence

Size	Document Number	Rev
Custom	LA-J561P	1.0

Date: Wednesday, February 26, 2020 Sheet 5 of 100



Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

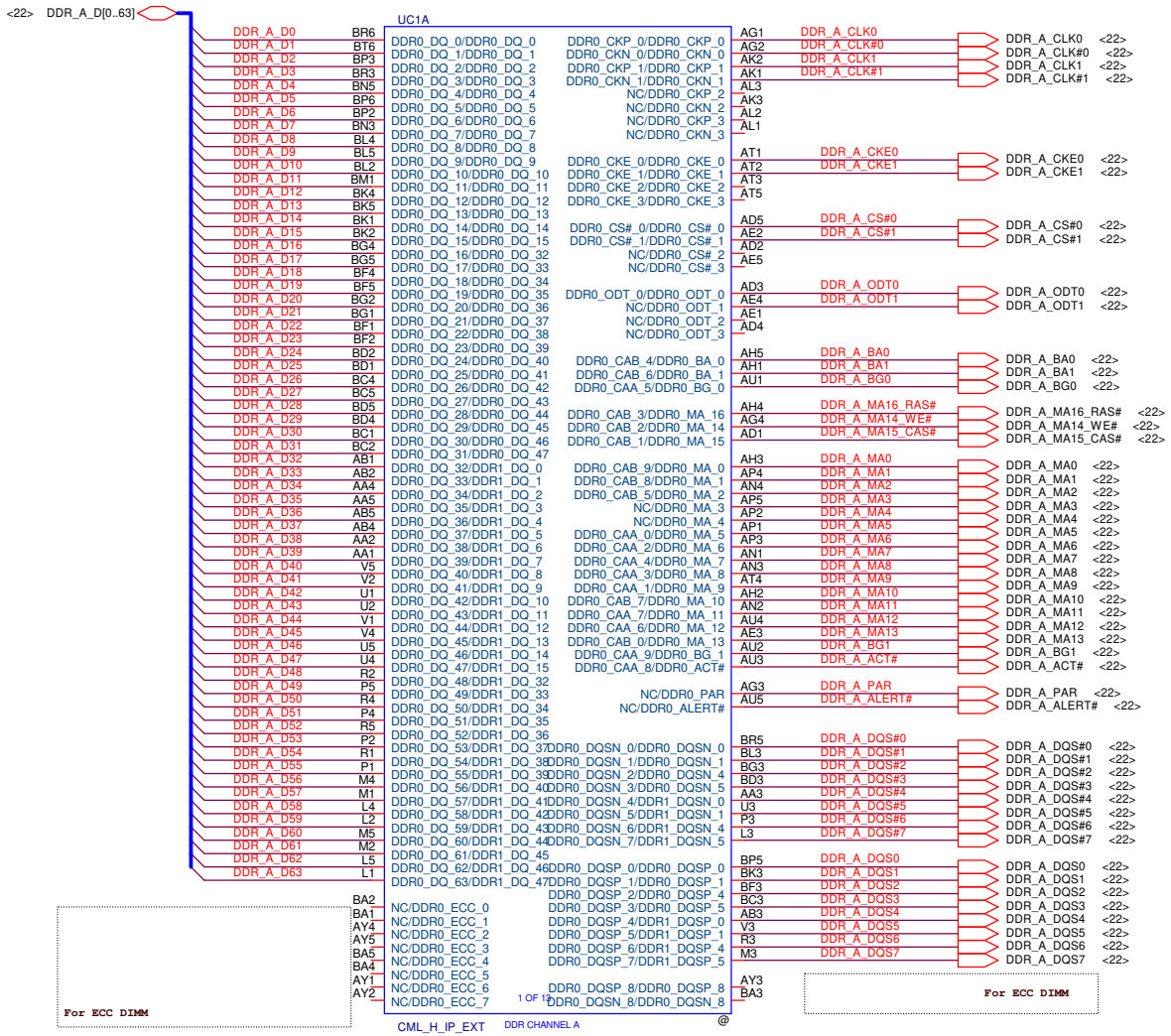
Title: CFL-H(1/8)DDI/eDP

Size: Custom | Document Number: LA-J561P | Rev: 1.0

Date: Wednesday, February 26, 2020 | Sheet 6 of 100

CHANNEL–A

Interleaved Memory

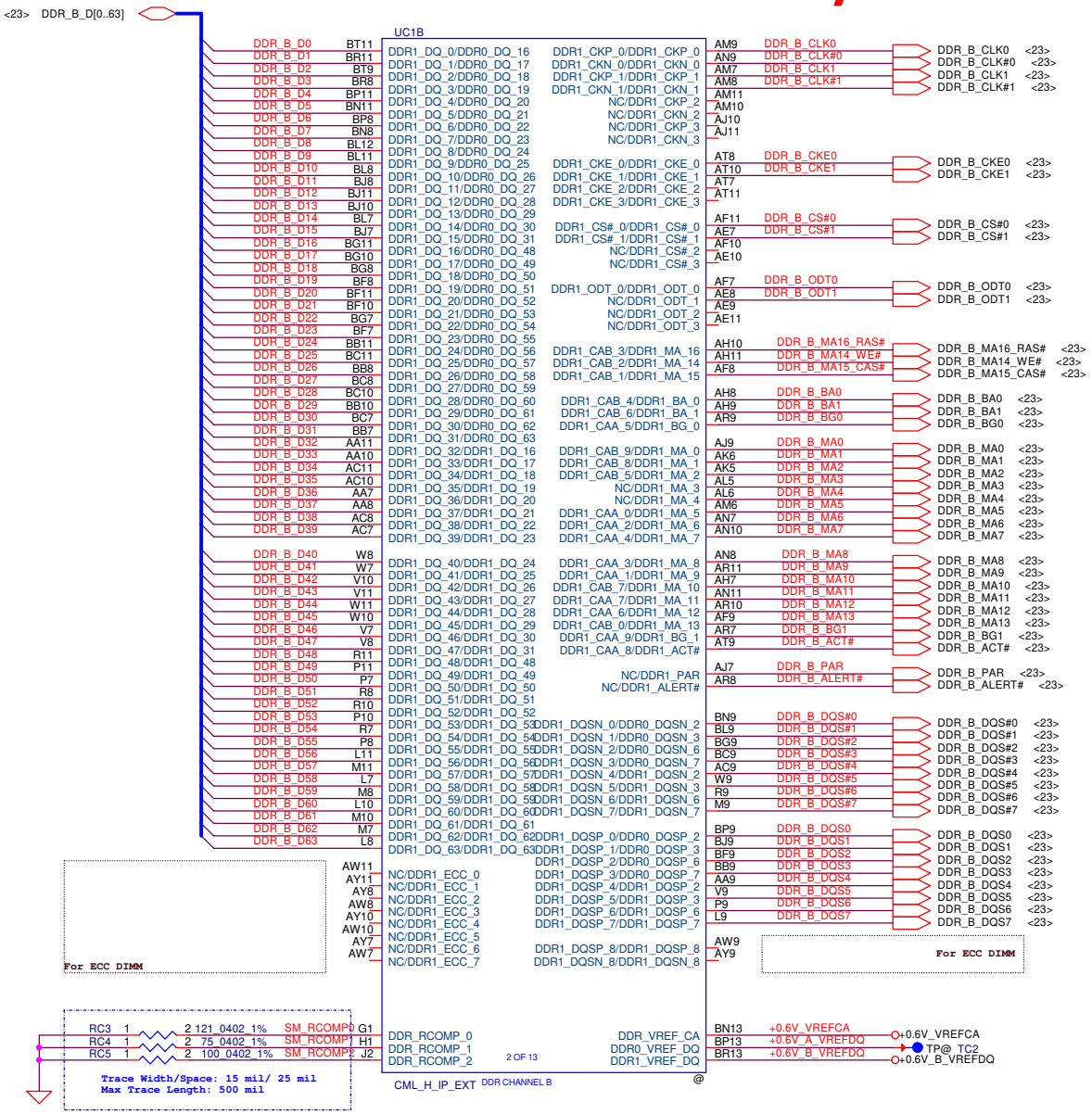


Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.			
Title: CFL-H(2/8)DIMMA			
Size: Custom	Document Number: LA-J561P		Rev: 1.0
Date: Wednesday, February 26, 2020	Sheet 7 of 100		

CHANNEL–B

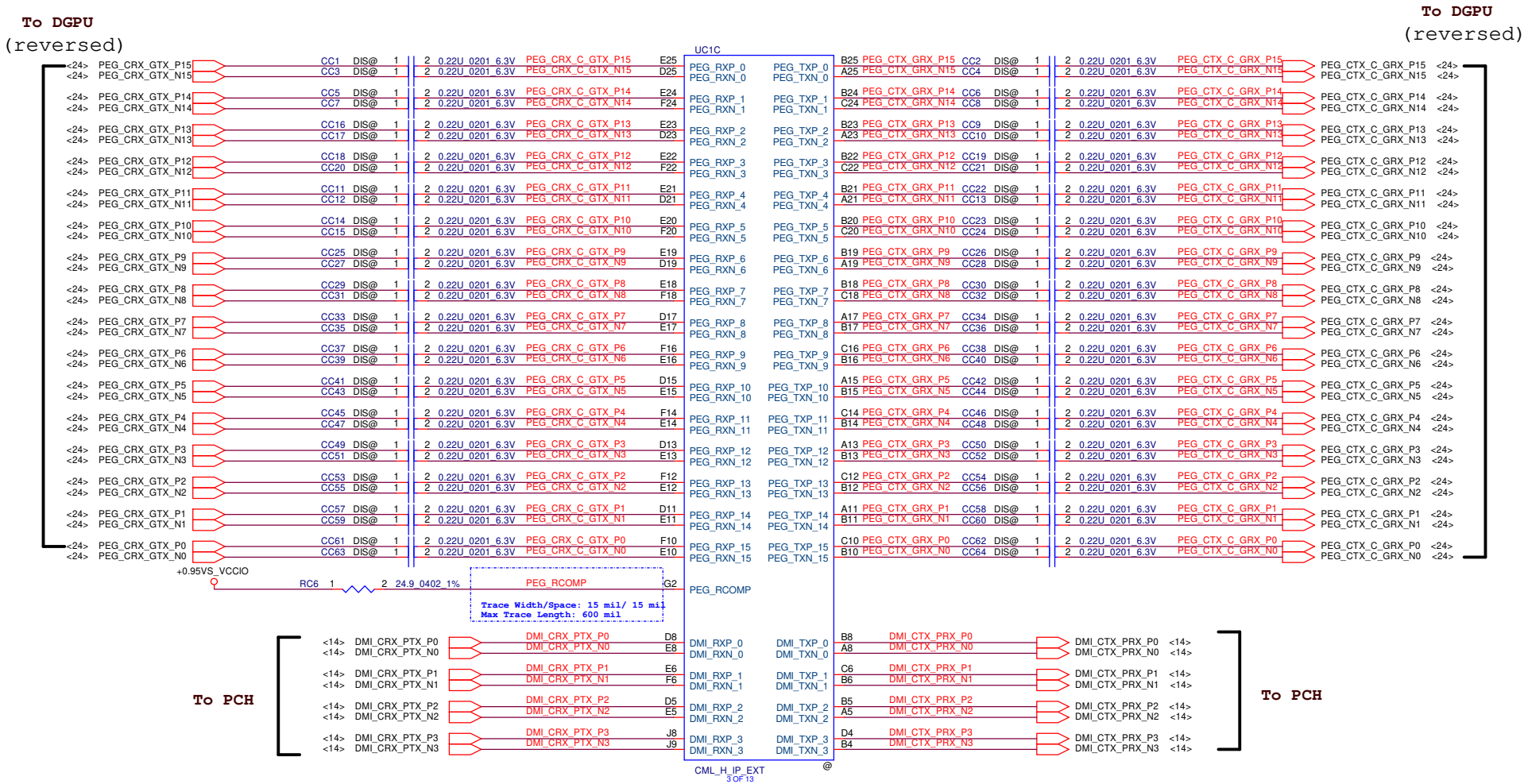
Interleaved Memory



Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.			
Title: CFL-H(3/8)DIMMB			
Size: Custom	Document Number: LA-J561P		Rev: 1.0
Date: Wednesday, February 26, 2020	Sheet 8 of 100		

PEG&DMI



Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.			
Title: PEG/DMI			
Size: Custom	Document Number: LA-J561P		Rev: 1.0
Date: Wednesday, February 26, 2020	Sheet 9 of 100		

Table 2-13. PCI Express* Bifurcation and Lane Reversal Mapping

Bifurcation	Link Width			CFG Signals			Lanes													
	0:1:0	0:1:1	0:1:2	CFG [6]	CFG [5]	CFG [2]	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16	x16	N/A	N/A	1	1	1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16 Reversed	x16	N/A	N/A	1	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2x8	x8	x8	N/A	1	0	1	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
2x8 Reversed	x8	x8	N/A	1	0	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
1x8+2x4	x8	x4	x4	0	0	1	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
1x8+2x4 Reversed	x8	x4	x4	0	0	0	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

The CFG signals have a default value of '1' if not terminated on the board.

CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted
1 = (Default) Normal Operation;
0 = Stall.

CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.
1 = Normal operation
0 = Lane numbers reversed.

CFG[4]: eDP enable:
1 = Disabled.
0 = Enabled.

CFG[6:5]: PCI Express* Bifurcation:
00 = 1 x8, 2 x4 PCI Express*
01 = reserved
10 = 2 x8 PCI Express*
11 = 1 x16 PCI Express*

CFG[7]: PEG Training:
1 = (default) PEG Train immediately following RESET# de assertion.
0 = PEG Wait for BIOS for training.

*CFG Pin Use CMC debug on DDX03 R02 Schematic.

UC1E

<15> PCH_CPU_BCLK_P — PCH_CPU_BCLK_P B31 — BCLKP
<15> PCH_CPU_BCLK_N — PCH_CPU_BCLK_N A32 — BCLKN
<15> PCH_CPU_PCIBCLK_P — PCH_CPU_PCIBCLK_P D35 — PCI_BCLKP
<15> PCH_CPU_PCIBCLK_N — PCH_CPU_PCIBCLK_N C36 — PCI_BCLKN
<15> PCH_CPU_24M_CLK_P — PCH_CPU_24M_CLK_P E31 — CLK24P
<15> PCH_CPU_24M_CLK_N — PCH_CPU_24M_CLK_N D31 — CLK24N

CFG_0 BN25 CFG0
CFG_1 BN27
CFG_2 BN26 CFG2
CFG_3 BN28
CFG_4 BR20 CFG4
CFG_5 BM20 CFG5
CFG_6 BT20 CFG6
CFG_7 BP20 CFG7
CFG_8 BR23
CFG_9 BR22
CFG_10 BT23
CFG_11 BT22
CFG_12 BM19
CFG_13 BR19
CFG_14 BP19
CFG_15 BT19
CFG_17 BN23
CFG_16 BP23
CFG_19 BP22
CFG_18 BN22

@RF@ 10P_0402_50V8J 2 — 1 CC65 — CPU_SVID_CLK
03/14 From RF Team Request

ESD@ 100P_0402_50V8J 1 — 2 CC66 — VCCST_PWRGD
ESD@ 100P_0402_50V8J 1 — 2 CC67 — H_CPUPWRGD
Near CPU side
From ESD Team Request

Sensitive
CPU_SVID_ALERT# BH31 — VIDALERT#
CPU_SVID_CLK BH32 — VIDSCK
CPU_SVID_DAT BH29 — VIDSOUT
H_PROCHOT#_R BR30 — PROCHOT#
DDR_PG_CTRL BT13 — DDR_VTT_CNTL

Sensitive
EC_VCCST_PG H13 — VCCST_PWRGD

BPM#_0 BR27 XDP_BPM#0 — TC3 TP@
BPM#_1 BT27 XDP_BPM#1 — TC4 TP@
BPM#_2 BM31 XDP_BPM#2 — TC5 TP@
BPM#_3 BT30 XDP_BPM#3 — TC6 TP@

<18> H_CPUPWRGD — H_CPUPWRGD BT31 — PROCPWRGD
<17> H_PLTRST_CPU# — H_PLTRST_CPU# BP35 — RESET#
<17> H_PM_SYNC_R — H_PM_SYNC_R BM34 — PM_SYNC
<17> H_PM_DOWN_R — H_PM_DOWN_R — RC7 1 — 2 20_0402_5% — H_PM_DOWN BP31 — PM_DOWN
<17,48> H_PECI — H_PECI BT34 — PECI
<17> PCH_THERMTRIP#_R — RC8 1 @ 2 0_0402_5% — H_THERMTRIP# J31 — THERMTRIP#
pulled high in PCH side

TP@ TC7 — SKTOCC# BR33 — SKTOCC#
TP@ TC8 — PROC_SELECT BN1 — PROC_SELECT#
TP@ TC9 — CATERR# BM30 — CATERR#
AT13 — ZVM#
AW13 — MSM#
TP@ TC10 — AU13 — RSVD1
TP@ TC11 — AY13 — RSVD2

5 OF 13
CML_H_IP_EXT

PROC_TDO BT28 CPU_XDP_TDO — CPU_XDP_TDO <18>
PROC_TDI BL32 CPU_XDP_TDI — CPU_XDP_TDI <18>
PROC_TMS BP28 CPU_XDP_TMS — CPU_XDP_TMS <18>
PROC_TCK BR28 CPU_XDP_TCK0 — CPU_XDP_TCK0 <18>
PROC_TRST# BP30 CPU_XDP_TRST#
BL30 XDP_PREQ#
PROC_PREQ# BP27 XDP_PRDY# — XDP_PREQ# <21>
PROC_PRDY# — XDP_PRDY# <21>
CFG_RCOMP BT25 CFG_RCOMP — RC9 1 — 2 49.9_0402_1%
Trace Width/Space: 4 mil/ 12 mil
Max Trace Length: 600 mil

XDP_PREQ# — T1 @
XDP_PRDY# — T2 @

+1.05V_VCCST — RC10 1K_0402_5% — VCCST_PWRGD — RC11 1 — 2 60.4_0402_1% — EC_VCCST_PG
<48> VCCST_PWRGD

+1.05VS_VCCSTG — RC16 1K_0402_5% — H_PROCHOT# — RC21 2 — 1 499_0402_1% — H_PROCHOT#_R
<48> H_PROCHOT#

TMS/TDI pin CPU on-die termination
Place to PCH side
+1.05VS_VCCSTG — CPU_XDP_TDO — 51_0402_5% 1 — 2 RC65
Place to CPU side
CPU_XDP_TCK0 — 51_0402_5% 1 — 2 RC22
If need debug with INTEL. this cmc@ need pop
CPU_XDP_TRST# — R1 1 @ 2 0_0402_5% — PCH_XDP_TRST# <21>

CFG0 — RC12 1 @ 2 1K_0402_5%
CFG2 — RC13 1 @ 2 1K_0402_5%
CFG4 — RC17 1 @ 2 1K_0402_5%
CFG5 — RC19 1 @ 2 1K_0402_5%
CFG6 — RC20 1 @ 2 1K_0402_5%
CFG7 — RC23 1 @ 2 1K_0402_5%

SVID ALERT
+1.05V_VCCST — RC24 56_0402_1% — VR_SVID_ALERT# — RC25 1 — 2 220_0402_5% — CPU_SVID_ALERT#
<88> VR_SVID_ALERT#

SVID DATA
+1.05V_VCCST — RC27 100_0402_5% — VR_SVID_SDIO — RC28 1 @ 2 0_0402_5% — CPU_SVID_DAT
<88> VR_SVID_SDIO

SVID CLK
VR_SVID_SCLK — RC29 1 @ 2 0_0402_5% — CPU_SVID_CLK
<88> VR_SVID_SCLK

571391_CFL_H_PDG_Rev0p5
1. The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
2. Route the Alert signal between the Clock and the Data signals.
3. Place those resistors close CPU side.

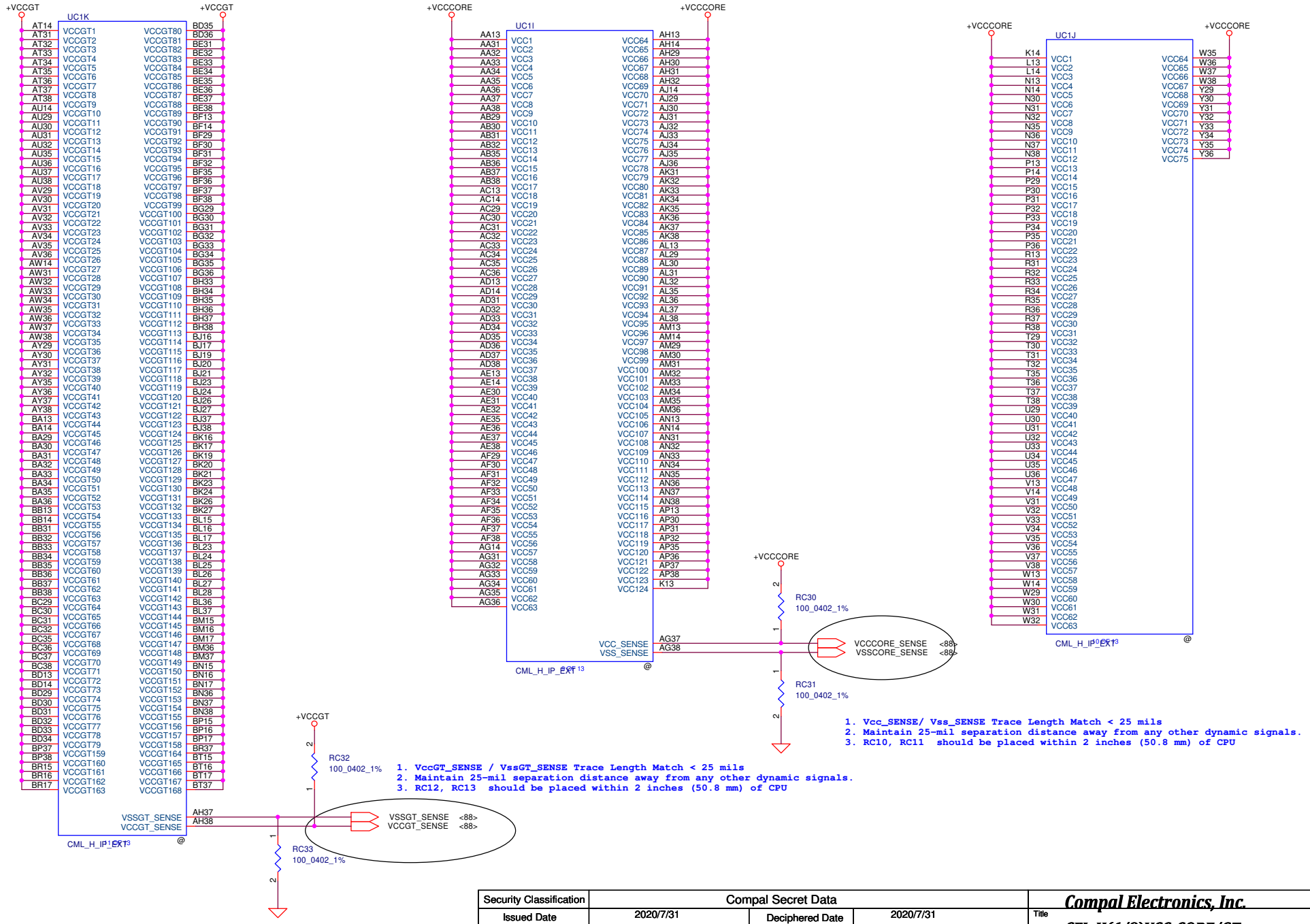
+1.2V — CC68 @ — 0.1U_0201_10V6K — UC2 NC VCC A GND Y — 74AUP1G07GW_TSSOP5
DDR_PG_CTRL — DDR_VTT_PG_CTRL_R — 0_0402_5% — RC61 @
+3VS — RC26 100K_0402_5% @
DDR_VTT_PG_CTRL <85>
<18,48,86> PM_SLP_S3# — 0_0402_5% — RC62 @

Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.
Title: CFL-H(5/8)CFG,SVID
Size: Custom | Document Number: LA-J561P | Rev: 1.0
Date: Wednesday, February 26, 2020 | Sheet 10 of 100

GT
32000mA(Hexa Core GT2)

128000mA(Hexa Core GT2)



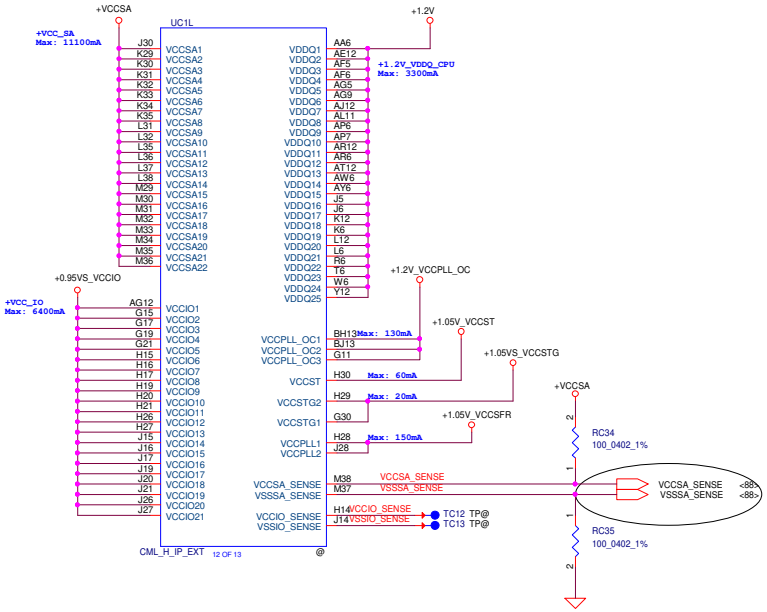
Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

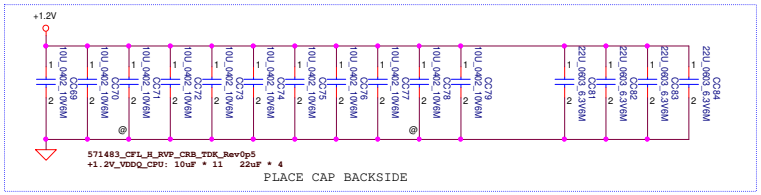
Compal Electronics, Inc.

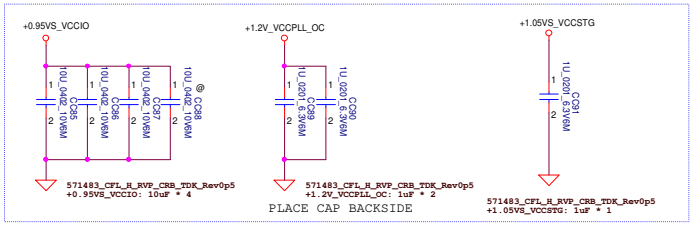
Title: CFL-H(6/8)VCC CORE/GT

Size	Document Number	Rev
Custom	LA-J561P	1.0

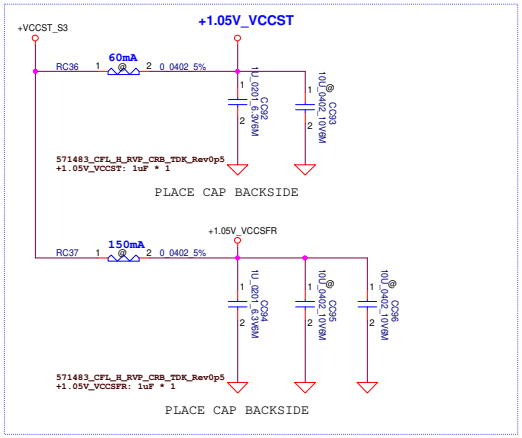
Date: Wednesday, February 26, 2020 Sheet 11 of 100

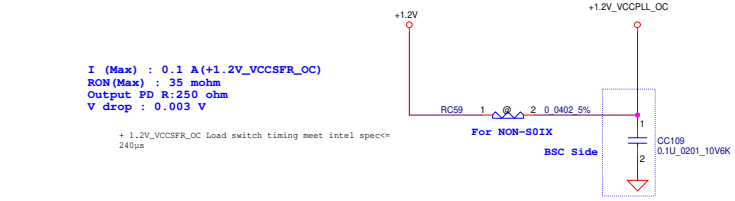




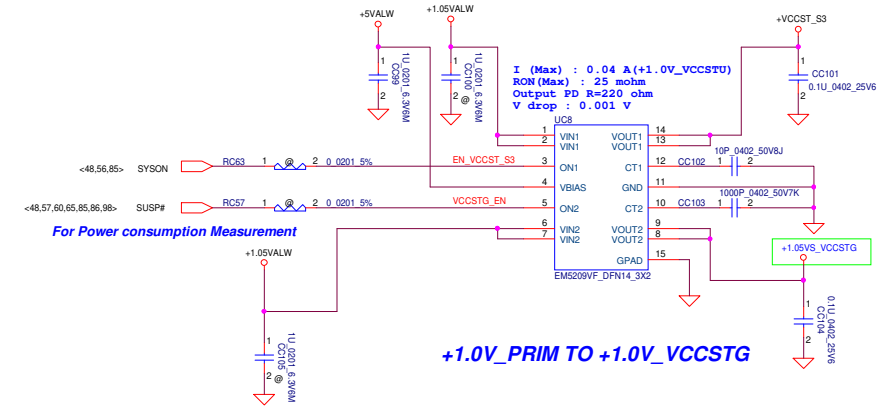


1. VccGT_SENSE / VssGT_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC15, RC16 should be placed within 2 inches (50.8 mm) of CPU





+1.0V_PRIM to +VCCST_S3



+1.0V_PRIM TO +1.0V_VCCSTG

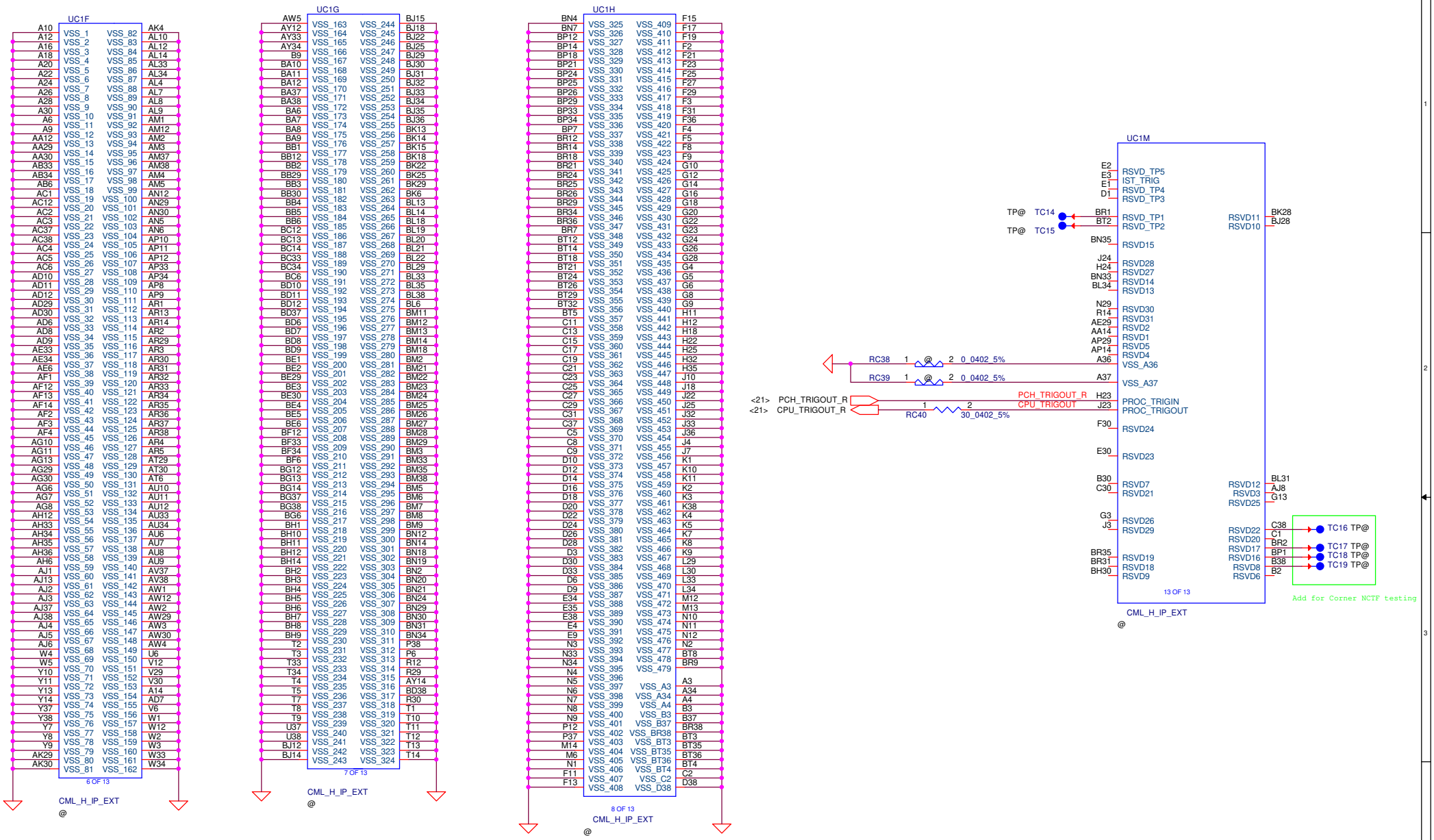
Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

Title: CFL-H(7/8)VCCSA/VCCIO/VDDQ

Size	Document Number	Rev
C	LA-J561P	1.0

Date: Wednesday, February 26, 2020 Sheet 12 of 100



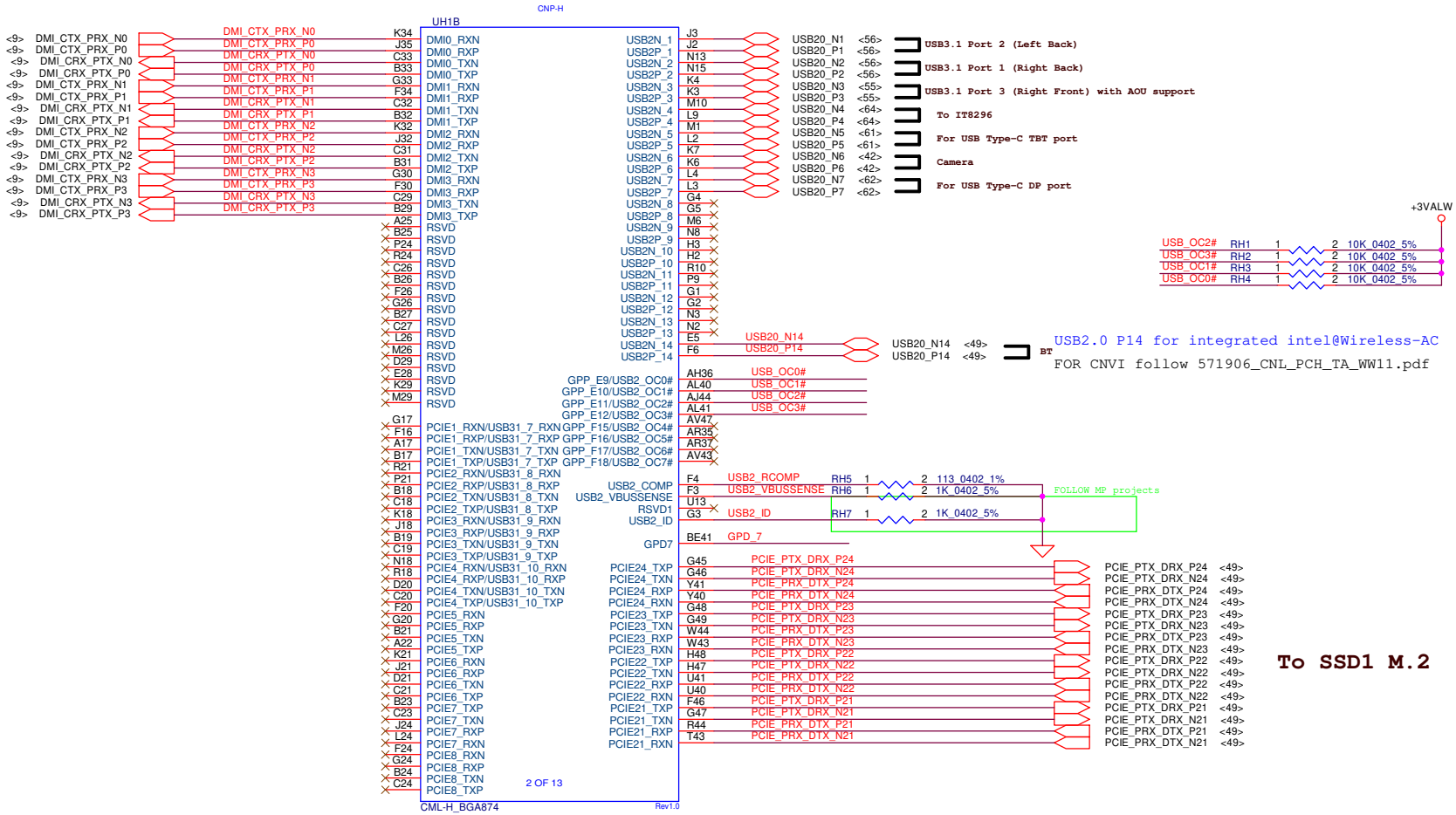
Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

Title: CFL-H(8/8)GND/RSVD

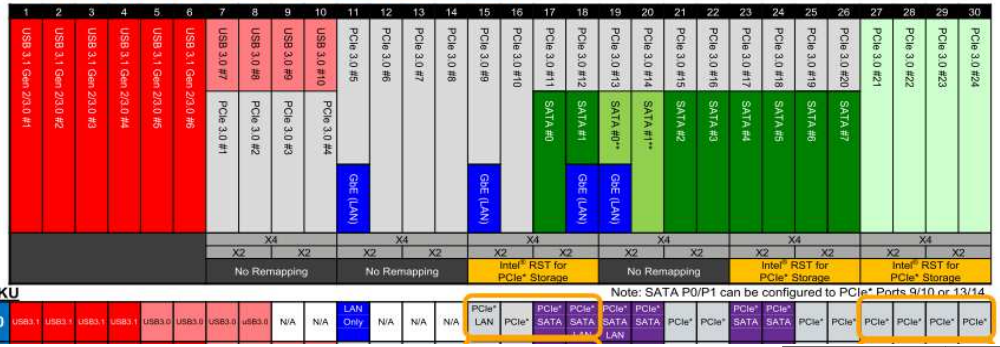
Size	Document Number	Rev
Custom	LA-J561P	1.0

Date: Wednesday, February 26, 2020 Sheet 13 of 100



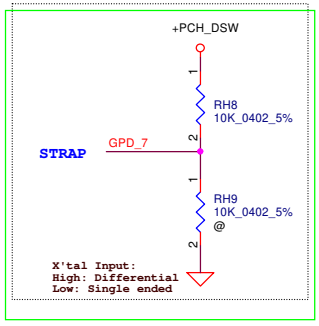
Comet Lake PCH-H HSIO Lane Assignments

- Up to 30 High-Speed I/O Lanes with Port Flexibility.



The 30 HSIO lanes on PCH-H supports the following configurations:
1. Up to 24 PCIe* Lanes
–A maximum of 16 PCIe* Ports (or devices) can be enabled
• When a GbE Port is enabled, the maximum number of PCIe* Ports (or devices) that can be enabled reduces based off the following:
Max PCIe* Ports (or devices) = 16 – GbE (0 or 1)
– PCIe* Lanes 1–4 (PCIe* Controller #1), 5–8 (PCIe* Controller #2), 9–12 (PCIe* Controller #3), 13–16 (PCIe* Controller #4), 17–20 (PCIe* Controller #5), and 21–24 (PCIe* Controller #6) can be individually configured
2. Up to 6 SATA Lanes
– A maximum of 6 SATA Ports (or devices) can be enabled
– SATA Lane 0 has the flexibility to be mapped to Flex I/O Lane 16 or 18
– SATA Lane 1 has the flexibility to be mapped to Flex I/O Lane 17 or 19
3. Up to 10 USB 3.1 Lanes
– A maximum of 10 USB 3.1 Ports (or devices) can be enabled
4. Up to 4 GbE Lanes
– A maximum of 1 GbE Port (or device) can be enabled
5. Supports up to 3 Remapped (IntelR Rapid Storage Technology) PCIe* storage devices
– x2 and x4 PCIe* NVMe SSD
– x2 IntelR Optane? Memory Device
– See the "PCI Express* (PCIe*)" chapter for the PCH PCIe* Controllers,configurations , and lanes that can be used for IntelR Rapid Storage Technology PCIe* storage support

6. For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA, the lanes must be statically assigned to SATA or PCIe* via the SATA/PCIe Combo Port Soft Straps discussed in the SPI Programming Guide and through the IntelR Flash Image Tool (FIT) tool.



Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.			
Title	PCH(1/8)DMI/PCIE/USB2		
Size: Custom	Document Number: LA-J561P		Rev: 1.0
Date: Wednesday, February 26, 2020	Sheet 14 of 100		

PCH-H XTAL_IN/OUT POR is 24MHz for 571697_CNL_MOW_WW16_2017.pdf

XTAL_24M_PCH_OUT RH10 1 EMI@ 2 33_0402_5% XTAL_24M_PCH_OUT_R
XTAL_24M_PCH_IN RH11 1 EMI@ 2 33_0402_5% XTAL_24M_PCH_IN_R

RH12 1 2 1M_0402_5%
24MHZ_18PF_XRCGB24M000F2P51R0
TXC SJ10000UJ00
Murata SJ10000UJ00
27P_0402_50V8J CH1 27P_0402_50V8J CH2
YH1 SJ10000TP00

PCH_RTCX1
PCH_RTCX2
RH14 1 2 10M_0402_5%
YH2 32.768KHZ_9PF_X1A000141000200
10P_0402_50V8J CH3 10P_0402_50V8J CH4
Trace Space: 15 mil
Max Trace Length: 1000 mil
EPSON SJ10000PW00
TXC SJ10000Q400

RH13 1 2 60.4_0402_1% XCLK_BIASREF
XCLK_BIASREF
Trace Width/Space: 15mil /15 mil
Max Trace Length: 1000 mil

CNP-H
UH1G
TH1 TP@

BE33	GPP_A16/CLKOUT_48		
D7	CLKOUT_CPUNSSC_P	CLKOUT_ITPXDP#	Y3 TP@ TH2
C6	CLKOUT_CPUNSSC#	CLKOUT_ITPXDP_P	Y4 TP@ TH3
B8	CLKOUT_CPUBCLK_P	CLKOUT_CPUPCIBCLK#	B6 PCH_CPU_PCIBCLK_N
C8	CLKOUT_CPUBCLK#	CLKOUT_CPUPCIBCLK_P	A6 PCH_CPU_PCIBCLK_P
U9	XTAL_OUT	CLKOUT_PCIE_N0	AJ6
U10	XTAL_IN	CLKOUT_PCIE_P0	AJ7
T3	XCLK_BIASREF	CLKOUT_PCIE_N1	AH9
		CLKOUT_PCIE_P1	AH10
BA49	RTCX1	CLKOUT_PCIE_N2	AE14
BA48	RTCX2	CLKOUT_PCIE_P2	AE15
BF31	GPP_B5/SRCCLKREQ0#	CLKOUT_PCIE_N3	AE6
BE31	GPP_B6/SRCCLKREQ1#	CLKOUT_PCIE_P3	AE7
AR32	GPP_B7/SRCCLKREQ2#	CLKOUT_PCIE_N4	AC2
BB30	GPP_B8/SRCCLKREQ3#	CLKOUT_PCIE_P4	AC3
BA30	GPP_B9/SRCCLKREQ4#	CLKOUT_PCIE_N5	AB2
AN29	GPP_B10/SRCCLKREQ5#	CLKOUT_PCIE_P5	AB3
AE47	GPP_H0/SRCCLKREQ6#	CLKOUT_PCIE_N6	W4
AC48	GPP_H1/SRCCLKREQ7#	CLKOUT_PCIE_P6	W3
AE41	GPP_H2/SRCCLKREQ8#	CLKOUT_PCIE_N7	W7
AF48	GPP_H3/SRCCLKREQ9#	CLKOUT_PCIE_P7	W6
AC41	GPP_H4/SRCCLKREQ10#	CLKOUT_PCIE_N8	AC14
AC39	GPP_H5/SRCCLKREQ11#	CLKOUT_PCIE_P8	AC15
AE39	GPP_H6/SRCCLKREQ12#	CLKOUT_PCIE_N9	U2
AB48	GPP_H7/SRCCLKREQ13#	CLKOUT_PCIE_P9	U3
AC44	GPP_H8/SRCCLKREQ14#	CLKOUT_PCIE_N10	AC9
AC43	GPP_H9/SRCCLKREQ15#	CLKOUT_PCIE_P10	AC11
V2	CLKOUT_PCIE_N15	CLKOUT_PCIE_N11	AE9
V3	CLKOUT_PCIE_P15	CLKOUT_PCIE_P11	AE11
T2	CLKOUT_PCIE_N14	CLKOUT_PCIE_N12	AC7
T1	CLKOUT_PCIE_P14	CLKOUT_PCIE_P12	AC6
AA1	CLKOUT_PCIE_N13	7 OF 13	
Y2	CLKOUT_PCIE_P13	CLKIN_XTAL	R6

CML-H_BGA874 Rev1.0
@

<57> TBT_CLKREQ0#
<49> SSD_CLKREQ1#
<50> LAN_CLKREQ2#
<49> WLAN_CLKREQ3#
<24> GPU_CLKREQ4#
<49> SSD_CLKREQ5#

Thunderbolt: CLK_PCIE_N0 <57> / CLK_PCIE_P0 <57>
NGFF SSD1: CLK_PCIE_N1 <49> / CLK_PCIE_P1 <49>
LAN: CLK_PCIE_N2 <50> / CLK_PCIE_P2 <50>
WLAN: CLK_PCIE_N3 <49> / CLK_PCIE_P3 <49>
GPU: CLK_PEG_N4 <24> / CLK_PEG_P4 <24>
NGFF SSD2: CLK_PCIE_N5 <49> / CLK_PCIE_P5 <49>

REFCLK_CNV <49> 1V@38.4MHZ
RH17 10K_0402_5%

+3VS
RH16 1 2 10K_0402_5% SSD_CLKREQ1#
RH18 1 2 10K_0402_5% LAN_CLKREQ2#
RH19 1 2 10K_0402_5% WLAN_CLKREQ3#
RH20 2 DIS@ 1 10K_0402_5% GPU_CLKREQ4#
RH143 1 2 10K_0402_5% SSD_CLKREQ5#

For DDX03 R02

+1.8V_PRIM XTAL Frequency Select
RH21 1 2 4.7K_0402_5% CNV_BRI_PTX_DRX STRAP 36
This signal has a weak internal pull-down 20K.
0 = 38.4/19.2MHz XTAL frequency selected.
1 = 24MHz XTAL frequency selected. (DDX03)
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

+1.8V_PRIM VCCPSPI Select
RH27 1 @ 2 4.7K_0402_5% GPP_J9 STRAP
The signal has a weak internal pull-down 20K
0 = VCCPSPI is connected to 3.3V rail
1 = VCCPSPI is connected to 1.8V rail
Note: If VCCPSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os

+1.8V_PRIM M.2 CNV Mode Select
RH30 1 2 20K_0402_1% CNV_RGI_PTX_DRX STRAP 32
RH31 2 @ 1 10K_0402_5%
An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.
Pulled down by CRF CNVi RGI_DT pin

CNP-H
UH1M

AW13	GPP_G0/SD_CMD	CNV_WR_CLKN	BD4 CLK_CNV_PRX_DTX_N
BE9	GPP_G1/SD_DATA0	CNV_WR_CLKP	BE3 CLK_CNV_PRX_DTX_P
BF8	GPP_G2/SD_DATA1	CNV_WR_D0N	BB3 CNV_PRX_DTX_N0
BF9	GPP_G3/SD_DATA2	CNV_WR_D0P	BB4 CNV_PRX_DTX_P0
BG8	GPP_G4/SD_DATA3	CNV_WR_D1N	BA3 CNV_PRX_DTX_N1
BE8	GPP_G5/SD_CD#	CNV_WR_D1P	BA2 CNV_PRX_DTX_P1
BD8	GPP_G6/SD_CLK	CNV_WT_CLKN	BC5 CLK_CNV_PTX_DRX_N
AV13	GPP_G7/SD_WP	CNV_WT_CLKP	BB6 CLK_CNV_PTX_DRX_P
AP3	GPP_I11/M2_SKT2_CFG0	CNV_WT_D0N	BE6 CNV_PTX_DRX_N0
AP2	GPP_I12/M2_SKT2_CFG1	CNV_WT_D0P	BD7 CNV_PTX_DRX_P0
AN4	GPP_I13/M2_SKT2_CFG2	CNV_WT_D1N	BG6 CNV_PTX_DRX_N1
AM7	GPP_I14/M2_SKT2_CFG3	CNV_WT_D1P	BF6 CNV_PTX_DRX_P1
AV6	GPP_J0/CNV_PA_BLANKING	CNV_WT_RCOMP	BA1 CNV_WT_RCOMP RH22 1 2 150_0402_1%
AY3	GPP_J1/CPU_C10_GATE#	PCIE_RCOMPN	B12 PCIE_RCOMPN RH23 1 2 100_0402_1%
AR13	GPP_J11/A4WP_PRESENT	PCIE_RCOMPP	A13 PCIE_RCOMPP
AV7	GPP_J10	SD_1P8_RCOMP	BE5 SD_RCOMP_1P8 RH24 1 2 200_0402_1%
AW3	GPP_J_2	SD_3P3_RCOMP	BE4 SD_RCOMP_3P3 RH25 1 2 200_0402_1%
AT10	GPP_J_3	GPPJ_RCOMP_1P81	BD1
AV4	GPP_J4/CNV_BRI_DT/UART0B_RTS#	GPPJ_RCOMP_1P82	BE1 GPPJ_RCOMP_1P8 RH26 1 2 200_0402_1%
AY2	GPP_J5/CNV_BRI_RSP/UART0B_RXD	GPPJ_RCOMP_1P83	BE2
BA4	GPP_J6/CNV_RGI_DT/UART0B_TXD	RSVD2	Y35
AV3	GPP_J7/CNV_RGI_RSP/UART0B_CTS#	RSVD3	Y36
AW2	GPP_J8/CNV_MFUART2_RXD	RSVD1	BC1
AU9	GPP_J9/CNV_MFUART2_TXD	TP	AL35

3.3V
1.8V
13 OF 13
CML-H_BGA874 Rev1.0
@

TP@ TH4
#571483_CFL_H_RVP_CRB_TDK_Rev0p5
Recommend external test point

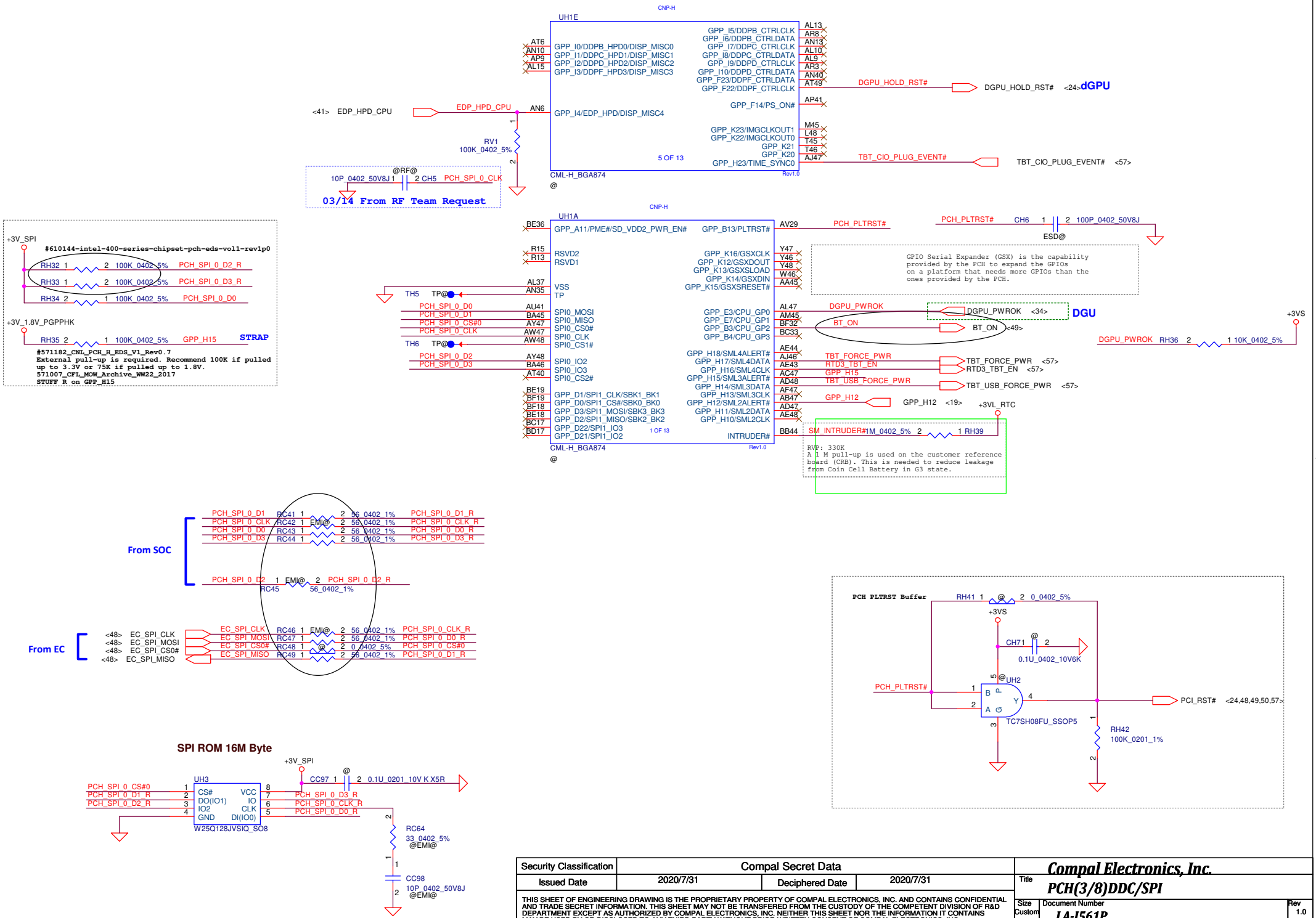
<49> CNV_BRI_PTX_R_DRX
<49> CNV_BRI_PRX_DTX
<49> CNV_RGI_PTX_R_DRX
<49> CNV_RGI_PRX_DTX
RH206 1 CNVI@ 2 22_0201_5% CNV_BRI_PTX_DRX
RH205 1 CNVI@ 2 22_0201_5% CNV_RGI_PTX_DRX
CNV_BRI_PRX_DTX
CNV_RGI_PRX_DTX
VCCPSPI Select GPP_J9

+1.8V_PRIM
RH28 1 @ 2 20K_0402_1% CNV_BRI_PRX_DTX 22
RH29 1 @ 2 20K_0402_1% CNV_RGI_PRX_DTX 34

571391_CFL_H_PDG_Rev0p71
To avoid floating input at the I/O pin BRI_RSP and RGI_RSP it is recommended to add a weak pull up resistor to the SoC pin with a recommended value of 20K ohm.

Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.
Title: PCH(2/8)CLK/CNVI/SD
Size: Custom
Document Number: LA-J561P
Rev: 1.0
Date: Wednesday, February 26, 2020
Sheet 15 of 100



Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.			
Title: PCH(3/8)DDC/SPI			
Size: Custom	Document Number: LA-J561P		Rev: 1.0
Date: Wednesday, February 26, 2020	Sheet 16 of 100		

Rear Side
USB3.1 Gen2 x 2

IO board USB3.1 Gen1

Type-C DP MUX USB3.1 Gen1

CNP-H

UH1F

USB3_PTX_DRX_N1 F9
USB3_PTX_DRX_P1 F7
USB3_PRX_DTX_N1 D11
USB3_PRX_DTX_P1 C11
USB3_PTX_DRX_N2 C3
USB3_PTX_DRX_P2 D4
USB3_PRX_DTX_N2 B9
USB3_PRX_DTX_P2 C9
USB3_PTX_DRX_P3 G12
USB3_PTX_DRX_N3 F11
USB3_PRX_DTX_P3 C10
USB3_PRX_DTX_N3 B10
USB3_PTX_DRX_P4 C14
USB3_PTX_DRX_N4 B14
USB3_PRX_DTX_P4 J15
USB3_PRX_DTX_N4 K16

USB31_1_TXN
USB31_1_TXP
USB31_1_RXN
USB31_1_RXP
USB31_2_TXN
USB31_2_TXP
USB31_2_RXN
USB31_2_RXP
USB31_6_TXN
USB31_6_TXP
USB31_6_RXN
USB31_6_RXP
USB31_5_TXN
USB31_5_TXP
USB31_5_RXN
USB31_5_RXP
USB31_3_TXP
USB31_3_TXN
USB31_3_RXP
USB31_3_RXN
USB31_4_TXP
USB31_4_TXN
USB31_4_RXP
USB31_4_RXN

1.8V (eSPI)

GPP_A1/LAD0/ESPI_IO0 BB39
GPP_A2/LAD1/ESPI_IO1 AW37
GPP_A3/LAD2/ESPI_IO2 AV37
GPP_A4/LAD3/ESPI_IO3 BA38
GPP_A5/LFRAME#/ESPI_CS0# BE38
GPP_A6/SERIRQ/ESPI_CS1# AW35
GPP_A7/PIRQA#/ESPI_ALERT0# BA36
GPP_A0/RCIN#/ESPI_ALERT1# BE39
GPP_A14/SUS_STAT#/ESPI_RESET# BF38
GPP_A9/CLKOUT_LPC0/ESPI_CLK BB36
GPP_A10/CLKOUT_LPC1 BB34
GPP_K19/SMI# T48
GPP_K18/NMI# T47
GPP_E6/SATA_DEVSLP2 AH40
GPP_E5/SATA_DEVSLP1 AH35
GPP_E4/SATA_DEVSLP0 AL48
GPP_F9/SATA_DEVSLP7 AP47
GPP_F8/SATA_DEVSLP6 AN37
GPP_F7/SATA_DEVSLP5 AN46
GPP_F6/SATA_DEVSLP4 AR47
GPP_F5/SATA_DEVSLP3 AP48

6 OF 13

CML-H_BGA874 Rev1.0

@

LPC_AD0 <48>
LPC_AD1 <48>
LPC_AD2 <48>
LPC_AD3 <48>
LPC_FRAME# <48>
PCH_SERIRQ RH195 1 @ 2 0_0402_5% SERIRQ <48>
PIRQA#
KB_RST#

+1.8VS_3VS_PGPPA

PIRQA# RH43 1 2 10K_0402_5%
KB_RST# RH44 1 2 10K_0402_5%
SERIRQ RH45 1 2 10K_0402_5%

CLK_LPC RH46 1 EMI@ 2 22_0402_5% CLK_LPC_EC <48>

HDMI_HPD_PCH_K19 RH198 1 @ 2 0_0402_5% HDMI_HPD_PCH <19,43>
RTD3_TBT_WAKE# <57>

10P_0402_50V8J 1 CH55 @RF@ 2

For Intel CLINK

TH8 TP@
TH10 TP@
TH9 TP@

CL_CLK AR2
CL_DATA AT5
CL_RST# AU4

CL_CLK
CL_DATA
CL_RST#

GPP_K8 P48
GPP_K9 V47
GPP_K10 V48
GPP_K11 W47
GPP_K0 L47
GPP_K1 L46
GPP_K2 U48
GPP_K3 U47
GPP_K4 N48
GPP_K5 N47
GPP_K6 P47
GPP_K7 R46

To SSD2 M.2

<49> PCIE_PTX_DRX_P11
<49> PCIE_PTX_DRX_N11
<49> PCIE_PRX_DTX_P11
<49> PCIE_PRX_DTX_N11

PCIE_PTX_DRX_P11 C36
PCIE_PTX_DRX_N11 B36
PCIE_PRX_DTX_P11 F39
PCIE_PRX_DTX_N11 G38

PCIE11_TXP/SATA0A_TXP
PCIE11_TXN/SATA0A_TXN
PCIE11_RXP/SATA0A_RXP
PCIE11_RXN/SATA0A_RXN

GPP_F10/SATA_SCLOCK AR42
GPP_F11/SATA_SLOAD AR48
GPP_F13/SATA_SDATAOUT0 AU47
GPP_F12/SATA_SDATAOUT1 AU46

LAN

<50> PCIE_PTX_C_DRX_N14
<50> PCIE_PTX_C_DRX_P14
<50> PCIE_PRX_DTX_N14
<50> PCIE_PRX_DTX_P14

CH12 1 2 0.1U_0201_10V6K PCIE_PTX_DRX_N14
CH13 1 2 0.1U_0201_10V6K PCIE_PTX_DRX_P14
PCIE_PRX_DTX_N14 C39
PCIE_PRX_DTX_P14 D39
D46
C47

PCIE14_TXN/SATA1B_TXN
PCIE14_TXP/SATA1B_TXP
PCIE14_RXN/SATA1B_RXN
PCIE14_RXP/SATA1B_RXP

HDD

<54> SATA_PTX_DRX_N0
<54> SATA_PTX_DRX_P0
<54> SATA_PRX_DTX_N0
<54> SATA_PRX_DTX_P0

SATA_PTX_DRX_N0 B38
SATA_PTX_DRX_P0 C38
SATA_PRX_DTX_N0 C45
SATA_PRX_DTX_P0 C46

PCIE13_TXN/SATA0B_TXN
PCIE13_TXP/SATA0B_TXP
PCIE13_RXN/SATA0B_RXN
PCIE13_RXP/SATA0B_RXP

To SSD2 M.2

<49> PCIE_PTX_DRX_P12
<49> PCIE_PTX_DRX_N12
<49> PCIE_PRX_DTX_P12
<49> PCIE_PRX_DTX_N12

PCIE_PTX_DRX_P12 E37
PCIE_PTX_DRX_N12 D38
PCIE_PRX_DTX_P12 J41
PCIE_PRX_DTX_N12 H42

PCIE12_TXP/SATA1A_TXP
PCIE12_TXN/SATA1A_TXN
PCIE12_RXP/SATA_1A_RXP
PCIE12_RXN/SATA1A_RXN

<57> PCIE_PTX_TRX_P20
<57> PCIE_PTX_TRX_N20
<57> PCIE_PRX_TTX_P20
<57> PCIE_PRX_TTX_N20
<57> PCIE_PTX_TRX_P19
<57> PCIE_PTX_TRX_N19
<57> PCIE_PRX_TTX_P19
<57> PCIE_PRX_TTX_N19

TBT@ CH14 1 2 0.22U_0201_6.3V PCIE_PTX_C_TRX_P20
TBT@ CH15 1 2 0.22U_0201_6.3V PCIE_PTX_C_TRX_N20
B44
A44
R37
R35
TBT@ CH16 1 2 0.22U_0201_6.3V PCIE_PTX_C_TRX_P19
TBT@ CH17 1 2 0.22U_0201_6.3V PCIE_PTX_C_TRX_N19
D43
C44
N42
M44

PCIE20_TXP/SATA7_TXP
PCIE20_TXN/SATA7_TXN
PCIE20_RXP/SATA7_RXP
PCIE20_RXN/SATA7_RXN
PCIE19_TXP/SATA6_TXP
PCIE19_TXN/SATA6_TXN
PCIE19_RXP/SATA6_RXP
PCIE19_RXN/SATA6_RXN

To Thunderbolt

CNP-H

UH1C

PCIE9_RXN G36
PCIE9_RXP F36
PCIE9_TXN C34
PCIE9_TXP D34
PCIE10_RXN K37
PCIE10_RXP J37
PCIE10_TXN C35
PCIE10_TXP B35
PCIE15_RXN/SATA2_RXN F44
PCIE15_RXP/SATA2_RXP E45
PCIE_15_SATA_2_TXN B40
PCIE15_TXP/SATA2_TXP C40
PCIE16_RXN/SATA3_RXN L41
PCIE16_RXP/SATA3_RXP M40
PCIE16_TXN/SATA3_TXN B41
PCIE16_TXP/SATA3_TXP C41
PCIE17_RXN/SATA4_RXN K43
PCIE17_RXP/SATA4_RXP K44
PCIE17_TXN/SATA4_TXN A42
PCIE17_TXP/SATA4_TXP B42
PCIE18_RXN/SATA5_RXN P41
PCIE18_RXP/SATA5_RXP R40
PCIE18_TXN/SATA5_TXN C42
PCIE18_TXP/SATA5_TXP D42

To SSD2 M.2

PCIE_PRX_DTX_N9
PCIE_PRX_DTX_P9
PCIE_PTX_DRX_N9
PCIE_PTX_DRX_P9
PCIE_PRX_DTX_N10
PCIE_PRX_DTX_P10
PCIE_PTX_DRX_N10
PCIE_PTX_DRX_P10

PCIE_PRX_DTX_N9 <49>
PCIE_PRX_DTX_P9 <49>
PCIE_PTX_DRX_N9 <49>
PCIE_PTX_DRX_P9 <49>
PCIE_PRX_DTX_N10 <49>
PCIE_PRX_DTX_P10 <49>
PCIE_PTX_DRX_N10 <49>
PCIE_PTX_DRX_P10 <49>

WLAN

PCIE_PRX_DTX_N15
PCIE_PRX_DTX_P15
PCIE_PTX_DRX_N15
PCIE_PTX_DRX_P15

PCIE_PRX_DTX_N15 <49>
PCIE_PRX_DTX_P15 <49>
PCIE_PTX_DRX_N15 <49>
PCIE_PTX_DRX_P15 <49>

To Thunderbolt

PCIE_PTX_C_TRX_N17 TBT@ CH8 2 1 0.22U_0201_6.3V
PCIE_PTX_C_TRX_P17 TBT@ CH9 2 1 0.22U_0201_6.3V
PCIE_PTX_C_TRX_N18 TBT@ CH10 2 1 0.22U_0201_6.3V
PCIE_PTX_C_TRX_P18 TBT@ CH11 2 1 0.22U_0201_6.3V

PCIE_PRX_TTX_N17 <57>
PCIE_PRX_TTX_P17 <57>
PCIE_PTX_TRX_N17 <57>
PCIE_PTX_TRX_P17 <57>
PCIE_PRX_TTX_N18 <57>
PCIE_PRX_TTX_P18 <57>
PCIE_PTX_TRX_N18 <57>
PCIE_PTX_TRX_P18 <57>

SATA_LED# RH196 2 1 10K_0402_5% +3VS

GPP_E8/SATA_LED#

GPP_E0/SATAXPCIE0/SATAGP0
GPP_E1/SATAXPCIE1/SATAGP1
GPP_E2/SATAXPCIE2/SATAGP2
GPP_F0/SATAXPCIE3/SATAGP_3
GPP_F1/SATAXPCIE4/SATAGP4
GPP_F2/SATAXPCIE5/SATAGP5
GPP_F3/SATAXPCIE6/SATAGP6
GPP_F4/SATAXPCIE7/SATAGP7

AK48
AH41
AJ43
AK47
AN47
AM46
AM43
AM47
AM48

RTD3_TBT_PERST# <57>

GPP_F21/EDP_BKLTCTL AU48
GPP_F20/EDP_BKLTEN AV46
GPP_F19/EDP_VDDEN AV44

PCH_BKL_PWM
PCH_ENBKL
PCH_ENVDD

PCH_BKL_PWM <41>
PCH_ENBKL <25,41>
PCH_ENVDD <41>

THRMTRIP# AD3
PECI AF2
PM_SYNC AF3
PLTRST_CPU# AG5
PM_DOWN AE2

PCH_THERMTRIP# RH48 1 2 620_0402_5%
PCH_PECI RH49 1 2 13_0402_5%
H_PM_SYNC RH50 1 2 30_0402_5%
H_PM_DOWN_R

#571391_CFL_H_PDG_Rev0p5.pdf

PCH_THERMTRIP#_R <10>
H_PECI <10,48>
H_PM_SYNC_R <10>
H_PLTRST_CPU# <10>
H_PM_DOWN_R <10>

3 OF 13

CML-H_BGA874 Rev1.0

@

@ RH51 13_0402_5%

#571391_CFL_H_PDG_Rev0p5
12.2.10 PM_DOWN Topology

+1.05V_VCCST

PCH_THERMTRIP#_R 2 1K_0402_5% 1 RH47

RH166 close to PCH

PCH_ENBKL

RH192 10K_0201_5%

Change Net Name and
Add Pull Down for vendor suggest
20190812

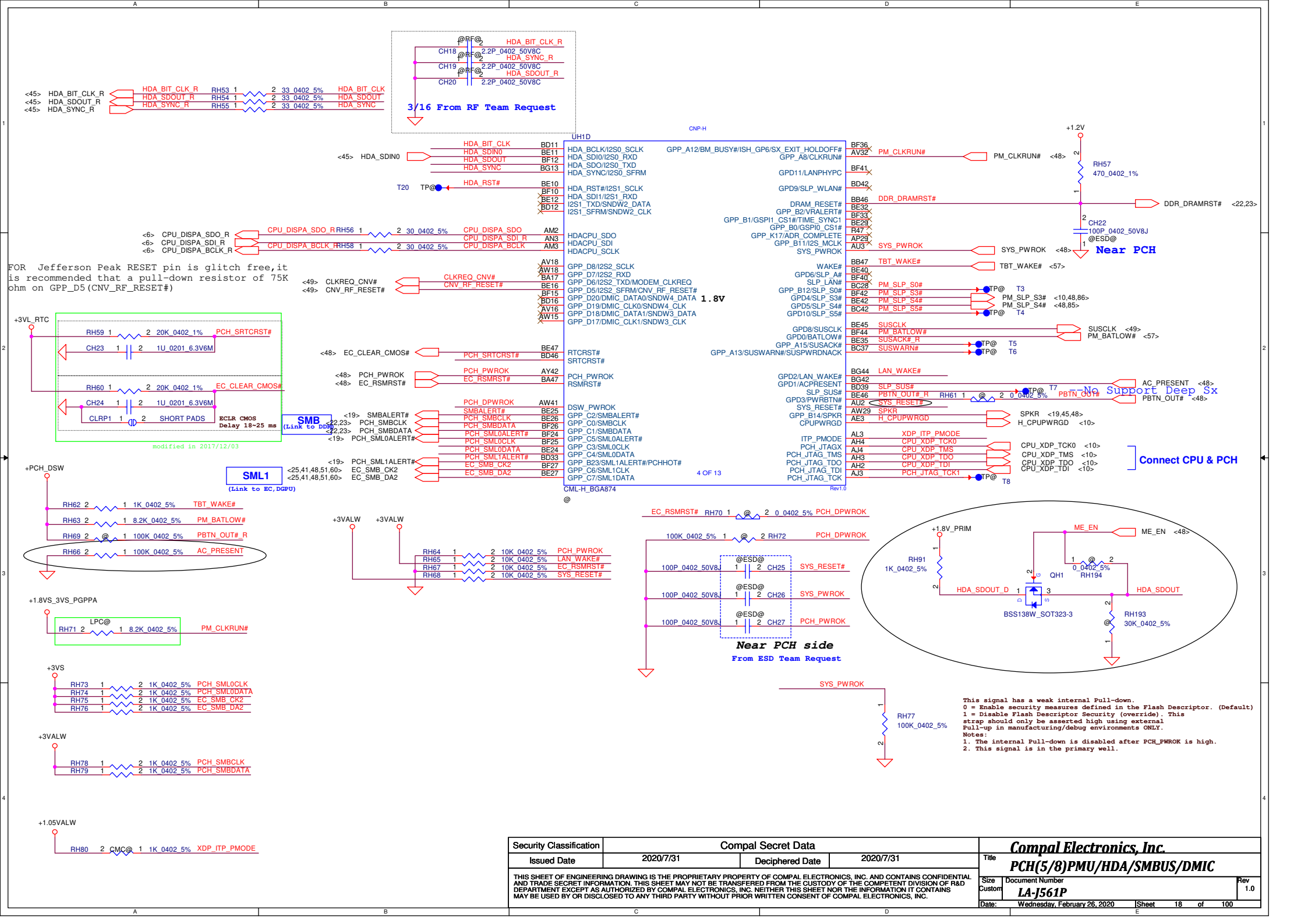
Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

Title: PCIE/SATA/USB3/eSPI

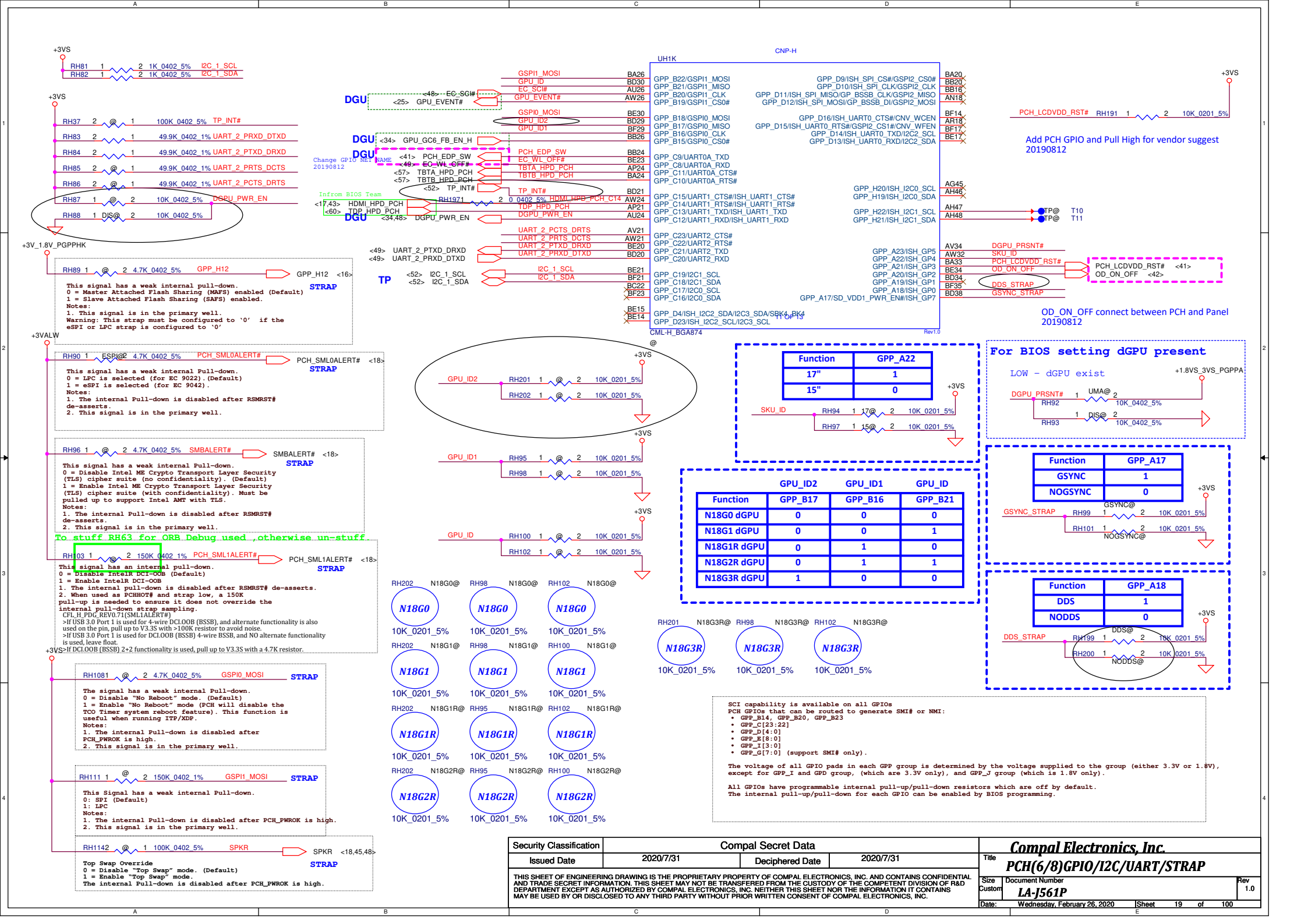
Size: Custom | Document Number: LA-J561P | Rev: 1.0

Date: Wednesday, February 26, 2020 | Sheet 17 of 100



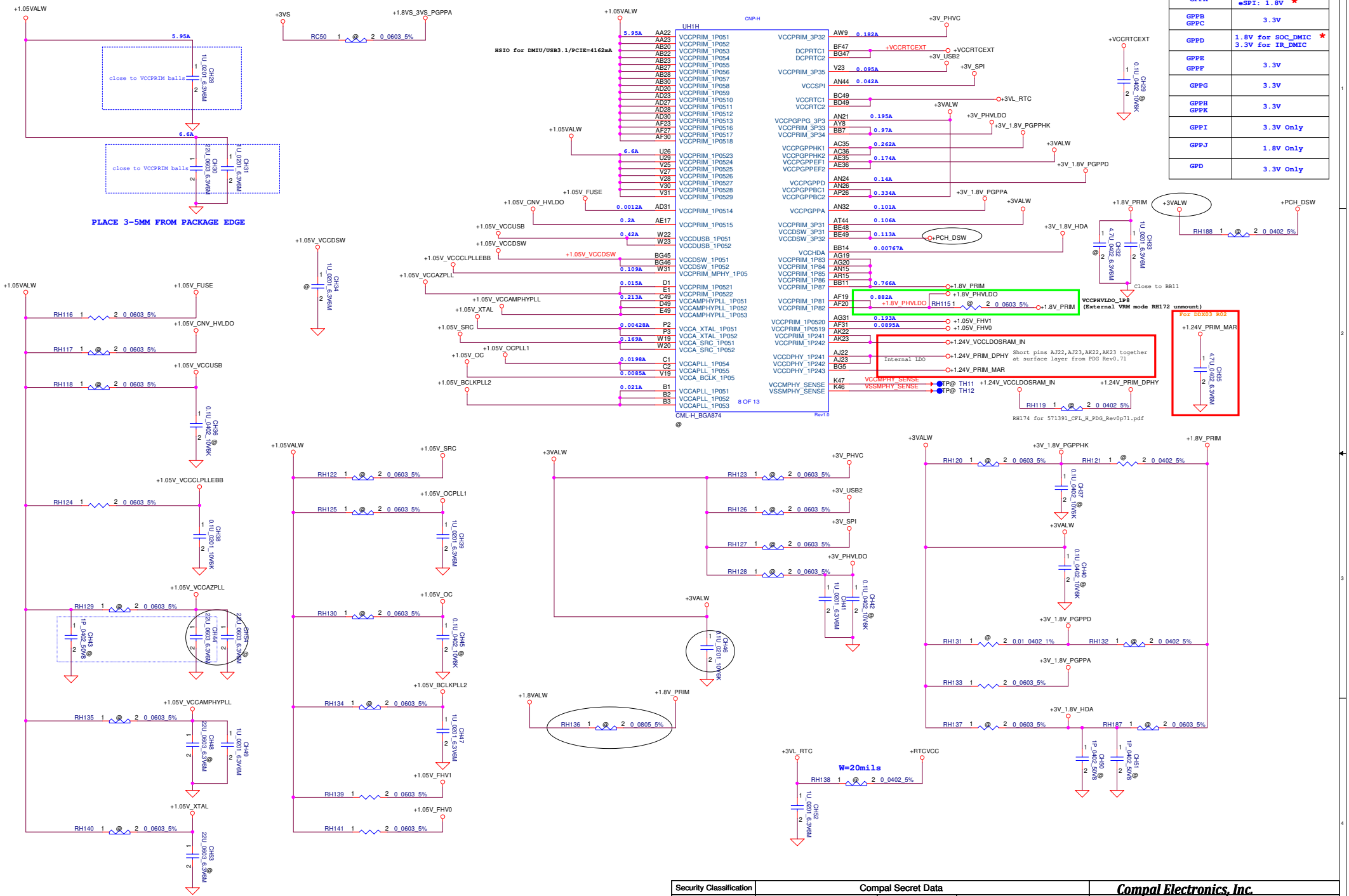
Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

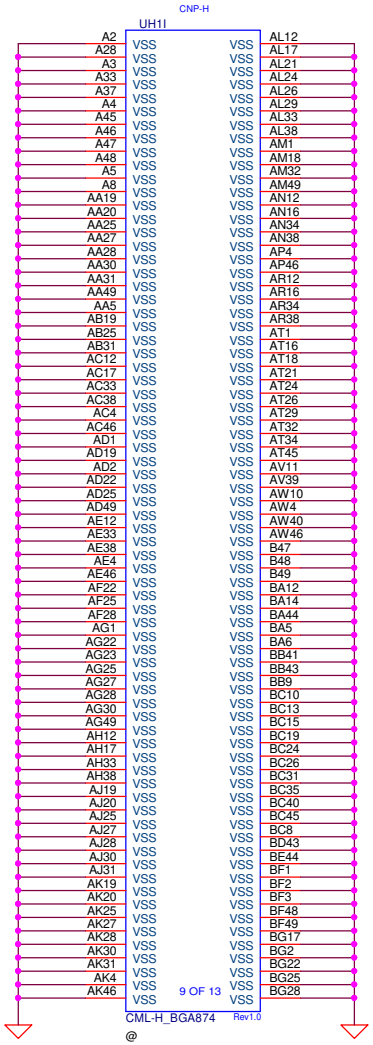
Compal Electronics, Inc.			
Title	PCH(5/8)PMU/HDA/SMBUS/DMIC		
Size: Custom	Document Number: LA-J561P		Rev: 1.0
Date: Wednesday, February 26, 2020	Sheet 18 of 100		

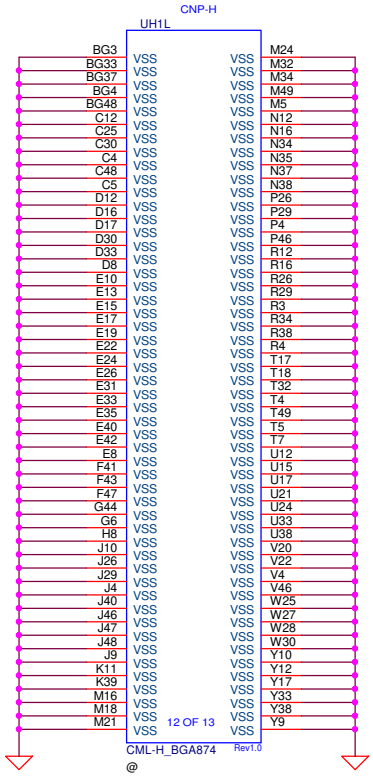


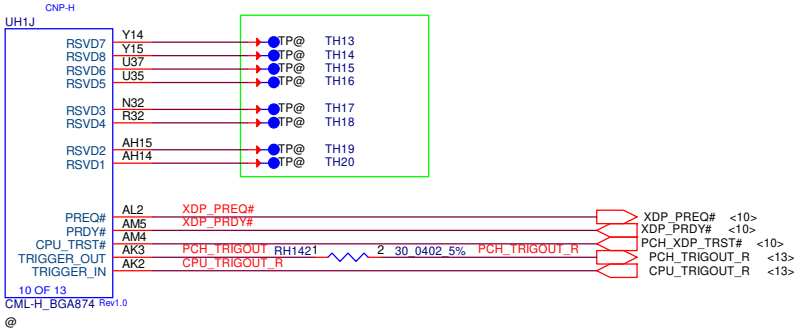
Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.			
Title	PCH(6/8)GPIO/I2C/UART/STRAP		
Size Custom	Document Number LA-J561P		Rev 1.0
Date: Wednesday, February 26, 2020	Sheet 19 of 100		


GPIO Group
Voltage
GPPA
LPC: 3.3V
eSPI: 1.8V
GPPB
GPPC
3.3V
GPPD
1.8V for SOC_DMIC
3.3V for IR_DMIC
GPPE
GPPF
3.3V
GPPG
3.3V
GPPH
GPPK
3.3V
GPPI
3.3V Only
GPPJ
1.8V Only
GPD
3.3V Only
PLACE 3-5MM FROM PACKAGE EDGE
HSIO for DMIO/USB3.1/PCIE=4162mA
UH1H
CML-H_BGA874
8 OF 13
Rev1.0
VCCPHVLDO_1P8
(External VRM mode RH172 unmount)
Close to BB11
Internal LDO
Short pins AJ22,AJ23,AK22,AK23 together at surface layer from PDG Rev0.71
RH174 for 571391_CFL_H_PDG_Rev0p71.pdf
W=20mils
Security Classification
Compal Secret Data
Issued Date
2020/7/31
Deciphered Date
2020/7/31
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.
Compal Electronics, Inc.
Title
PCH(7/8)Power
Size
Custom
Document Number
LA-J561P
Rev
1.0
Date:
Wednesday, February 26, 2020
Sheet
20
of
100







Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

Title: PCH(8/8)GND/RSVD

Size	Document Number	Rev
Custom	LA-J561P	1.0

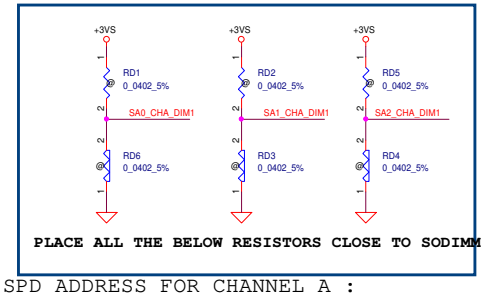
Date: Wednesday, February 26, 2020 Sheet 21 of 100

CHANNEL-A

BOT REVERSE TYPE (4 mm)

Interleaved Memory

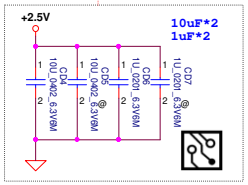
TOP: JDIMM1 CONN Non-ECC DIMM



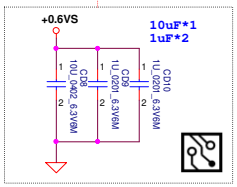
PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

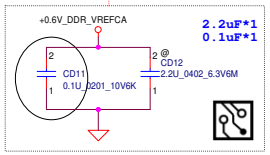
Layout Note:
Place near JDIMM1.257,259



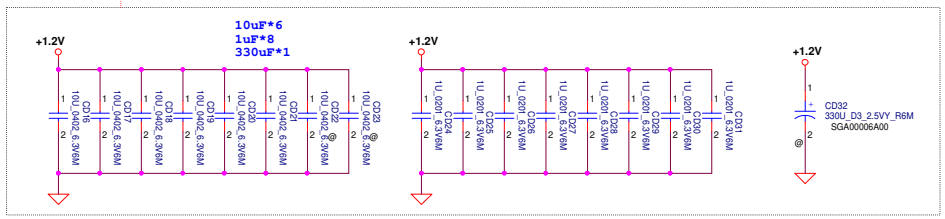
Layout Note:
Place near JDIMM1.258

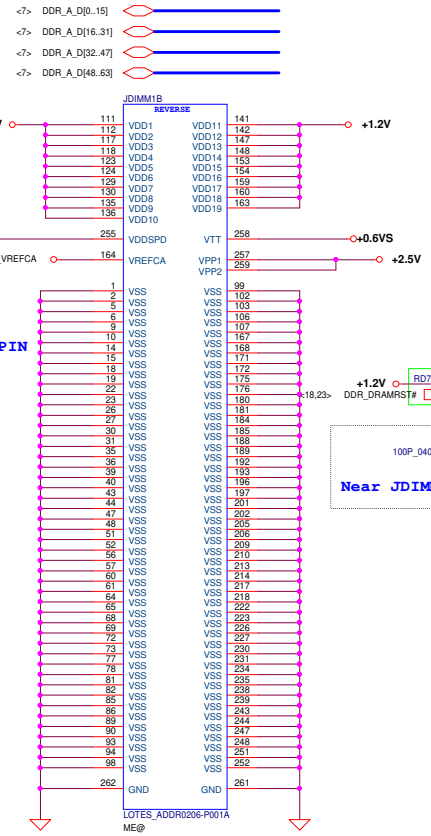


Layout Note:
PLACE THE CAP near JDIMM1. 164

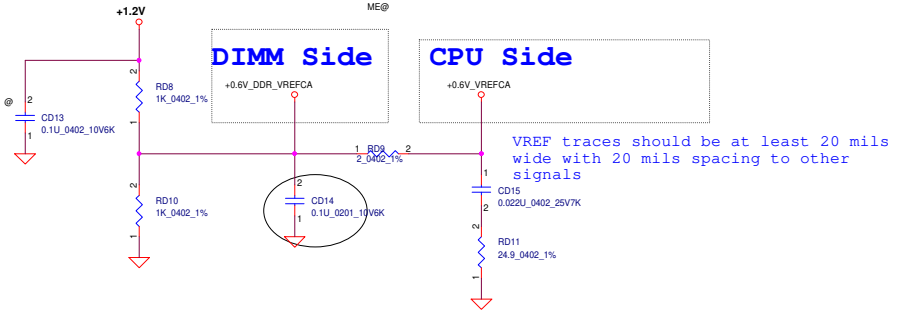


Layout Note:
Place near JDIMM1





Part Number:SP07001FYH0
Part Value:S SOCKET FOX_AS0A826-H4RB-7H 260P DDR4

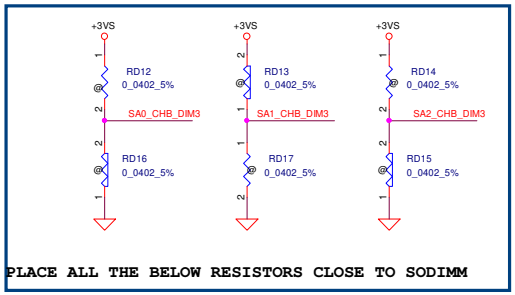


Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.			
Title	DDRIV_CHA: DIMM0		
Size	Document Number		Rev
	LA-J561P		1.0
Date:	Wednesday, February 26, 2020	Sheet	22 of 100

CHANNEL-B

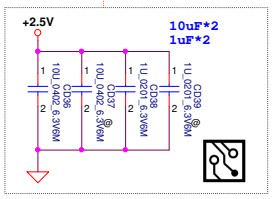
TOP: JDIMM3 CONN Non-ECC DIMM



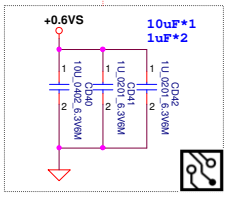
PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

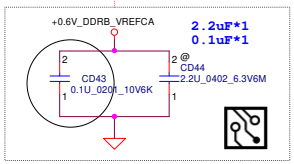
Layout Note:
Place near JDIMM3.257,259



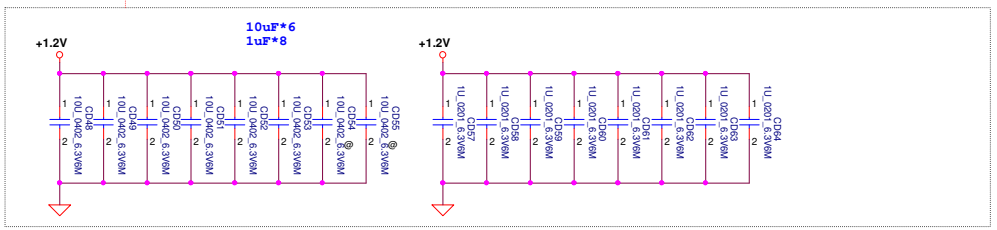
Layout Note:
Place near JDIMM3.258



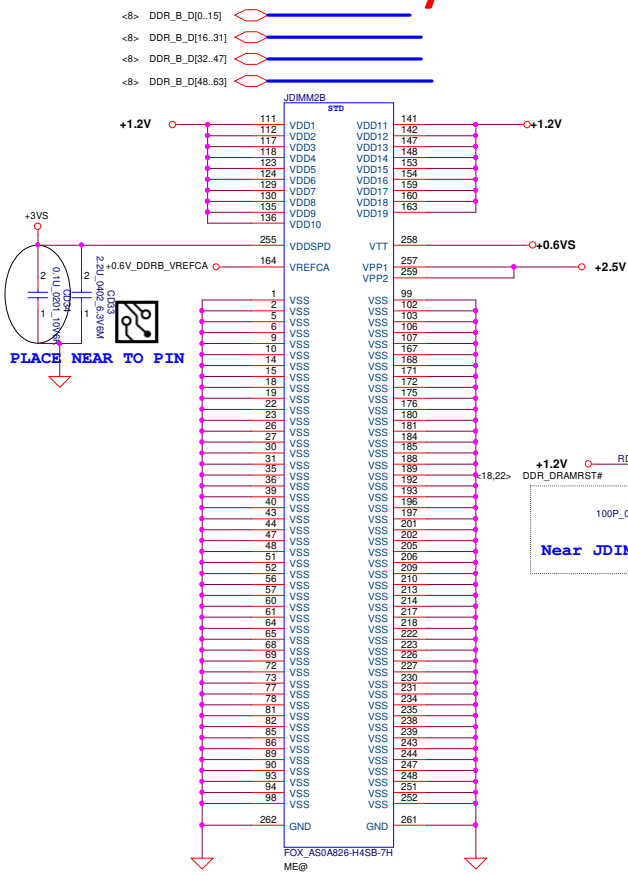
Layout Note:
PLACE THE CAP WITHIN 200 MILS FROM THE JDIMM3

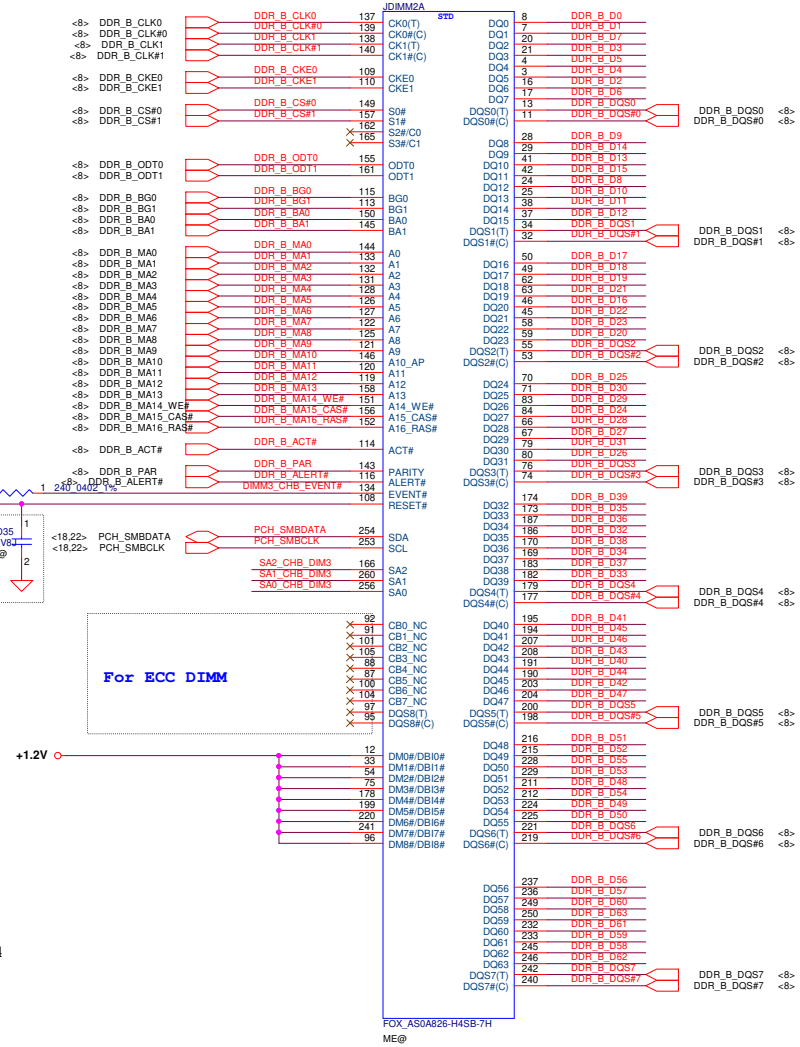


Layout Note:
Place near JDIMM3



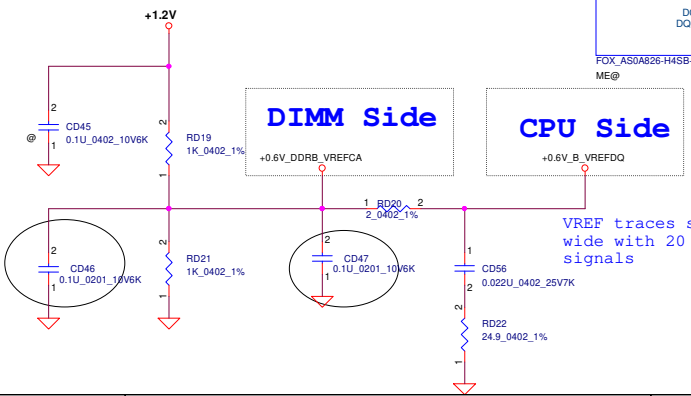
Interleaved Memory





For ECC DIMM

Part Number:SP07001CEA0
Part Value:S SOCKET FOX_AS0A826-H4SB-7H 260P DDR4

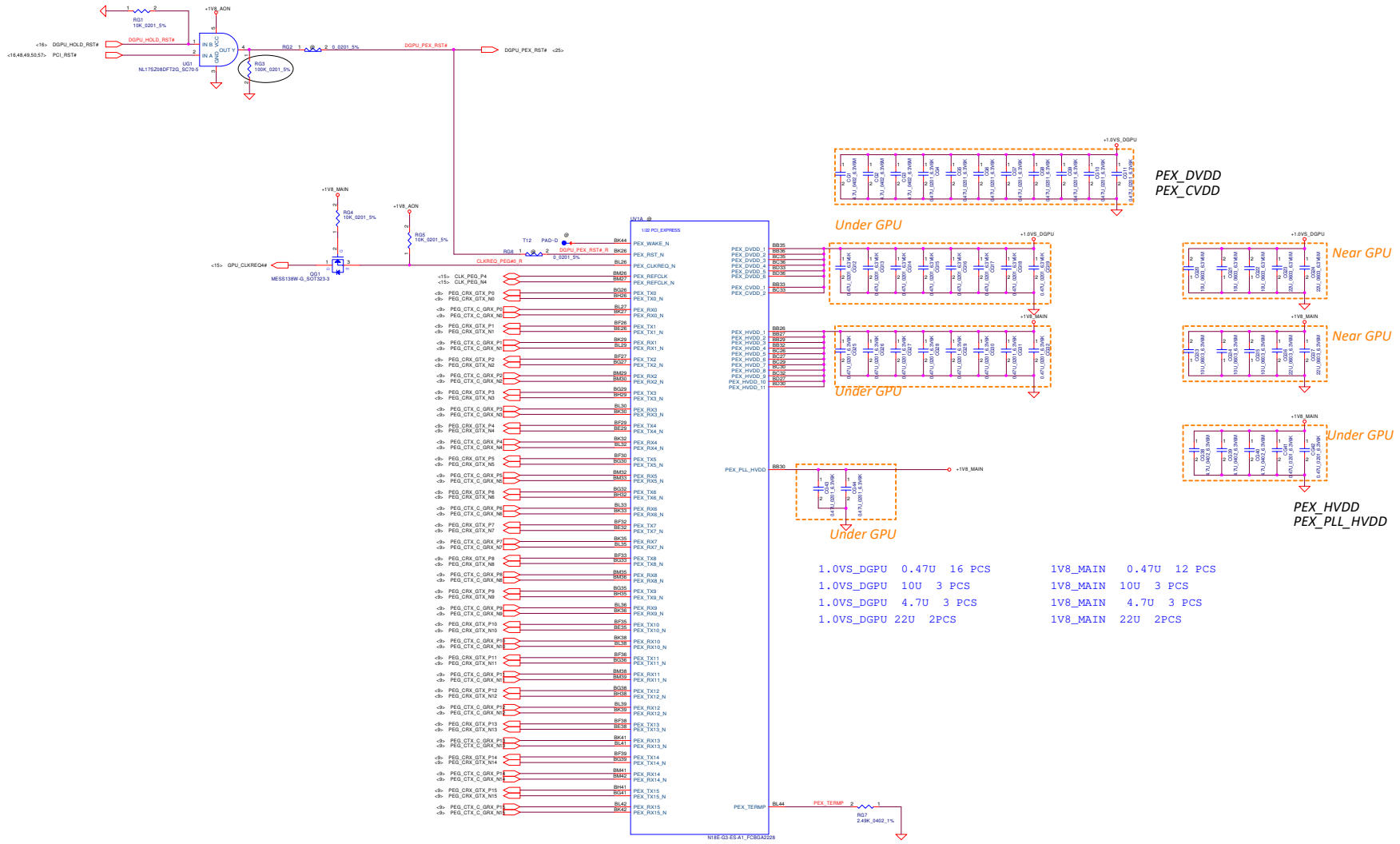


VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.			
Title	DDRIV_CHB: DIMM0		
Size	Document Number		Rev
	LA-J561P		1.0
Date:	Wednesday, February 26, 2020	Sheet	23 of 100

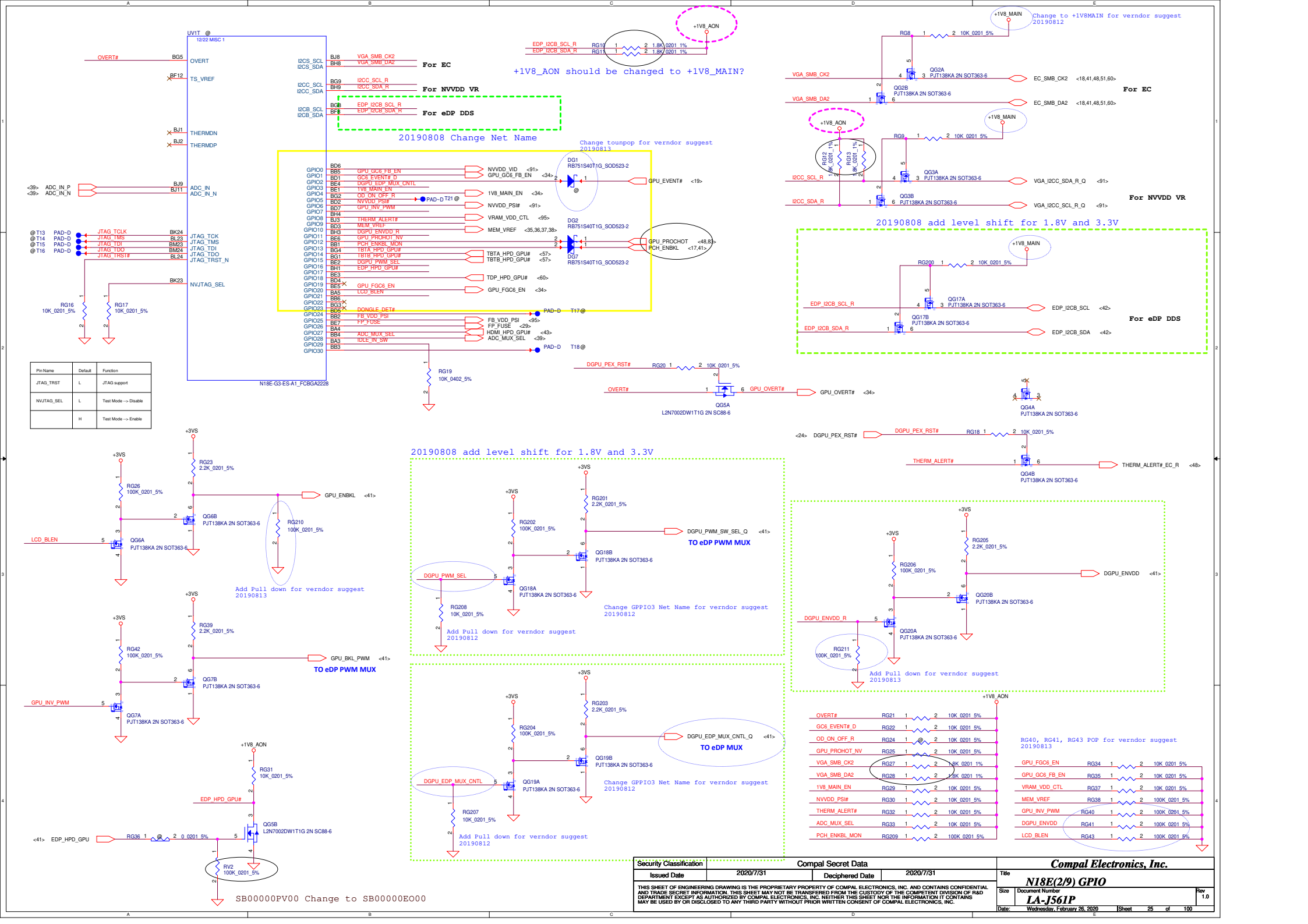
GC OFF 1.0 GPU Power ON/OFF



1.0VS_DGPU	0.47U	16 PCS	
1.0VS_DGPU	10U	3 PCS	
1.0VS_DGPU	4.7U	3 PCS	
1.0VS_DGPU	22U	2PCS	
1V8_MAIN	0.47U	12 PCS	
1V8_MAIN	10U	3 PCS	
1V8_MAIN	4.7U	3 PCS	
1V8_MAIN	22U	2PCS	

Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.	
Title	N18E(1/9) PCIE
Size	Document Number: LA-J561P
Rev	1.0
Date: Wednesday, February 26, 2020	Sheet 24 of 100



Pin Name	Default	Function
JTAG_TRST	L	JTAG support
NVJTAG_SEL	L	Test Mode --> Disable
	H	Test Mode --> Enable

Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

Title: **N18E(2/9) GPIO**

Size	Document Number	Rev
	LA-J561P	1.0

Date: Wednesday, February 26, 2020 | Sheet 25 of 100

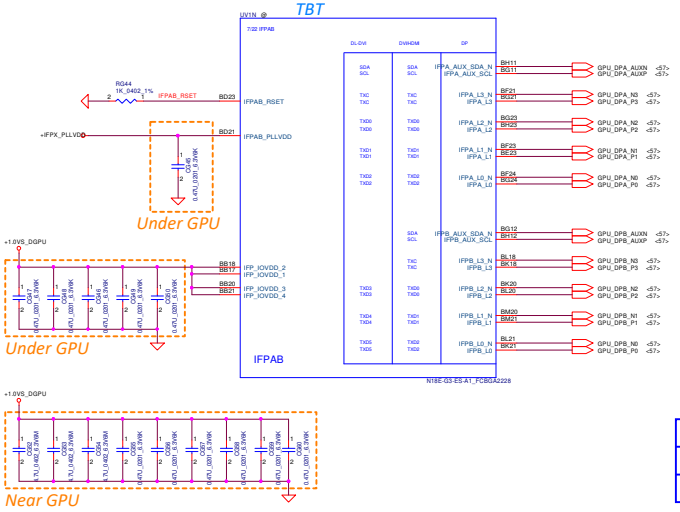
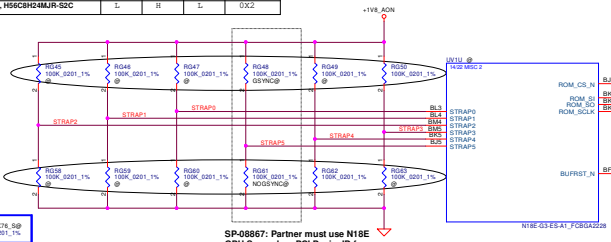


Table 11.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)

GDDR6 VRAM	Strap2	Strap1	Strap0	RAMCFG
Samsung , K4Z80325BC-HC14	L	L	L	0X0
Micron , MT61K256M32JE-14:A	L	L	H	0X1
Hynix , H56C8H24MJR-S2C	L	H	L	0X2

Samsung	RG58 X76_S@ 100K_0201_1%	RG59 X76_S@ 100K_0201_1%	RG60 X76_S@ 100K_0201_1%
Micron	RG58 X76_M@ 100K_0201_1%	RG59 X76_M@ 100K_0201_1%	RG47 X76_M@ 100K_0201_1%

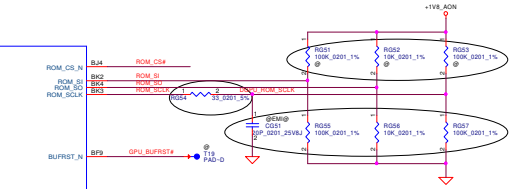


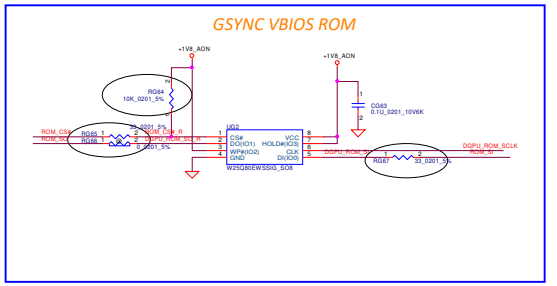
SP-08867: Partner must use N18E GPU Secondary PCI DeviceID for G-SYNC display enablement.

Table 11.4 FS_OVERT* Strap Enablement

Strap Pins see Note			FS_OVERT* Function
ROM_SO	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function ENABLED
L	L	H	FS_OVERT* function DISABLED (Reserved; do not configure)
all other configurations			(Invalid; do not configure)

Note that configurations other than the two listed in Table 11.4 must be avoided, as otherwise damage to strap inputs may result.





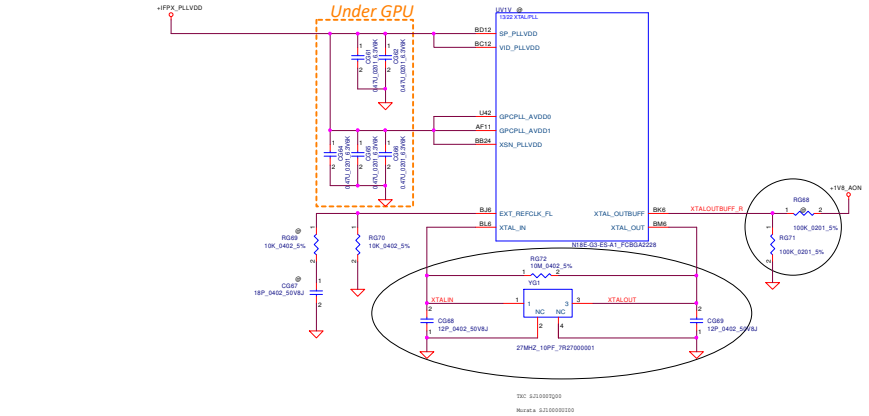
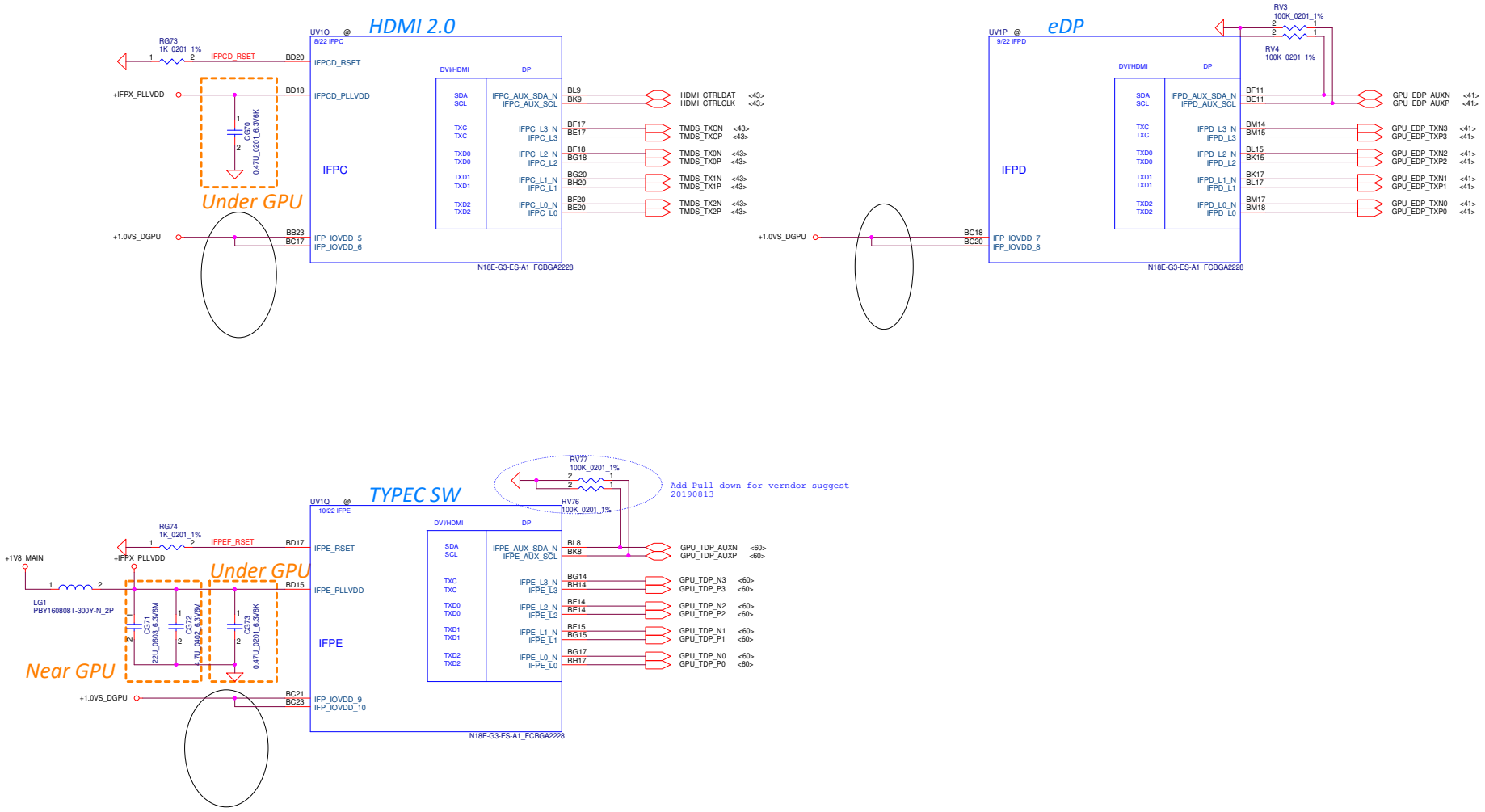


Table 11.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0

- **SMB_ALT_ADDR Enable**: This strap function allows an alternate SMBus address to be configured, so that graphics circuits with multiple GPUs can have separate SMBus connections for each GPU. In dual GPU configurations, use of the alternate address on one GPU (by setting this function to '1') avoids conflicts between the two GPUs on an SMBUS port. The "SMB_ALT_ADDR disabled" setting ('0') is correct for single-GPU graphics circuits.
- **DEVID_SEL**: NVIDIA defines an original and a re-brand Device ID on a per-GPU basis. This Device ID Select strap function allows selection between the original PCIe Device ID defined for the GPU (via a function setting of '0'), and the alternate "re-brand" Device ID defined for the GPU (via a function setting of '1').
- **PCIE_CFG**: This function sets electrical characteristics of PCIe lanes, in particular signal amplitude (swing). A setting of '0' selects normal (full) signal swing. N18x graphics circuits should strap for this setting. (A setting of '1' designates reduced signal amplitude, available if special concerns require. Consult NVIDIA for guidance.)
- **VGA_DEVICE**: This strap function is used to report the graphics circuit either as a 3D device (class code 302, designated by a setting of '0' for this strap) or as a VGA device (class code 300, designated by a setting of '1') to the host system. The 3D Device (class code 302, strap='0') setting is correct for most MS-Hybrid notebook GeForce graphics circuits (consult NVIDIA for details on proper bit setting for MS-Hybrid solutions).

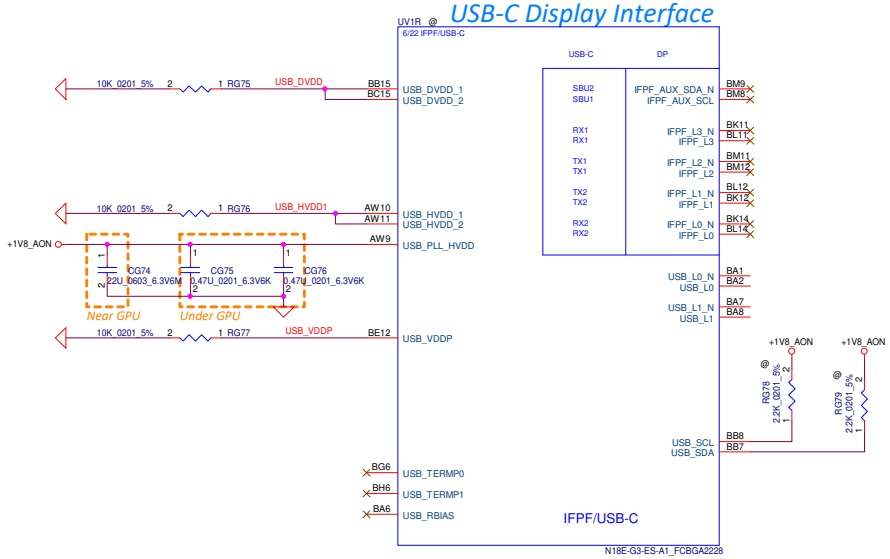
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/7/31	Deciphered Date 2020/7/31	Title: N18E(3/9) Strap, XTAL, IFP
			Size: Document Number: LA-J561P Rev: 1.0
			Date: Wednesday, February 26, 2020 Sheet 26 of 100



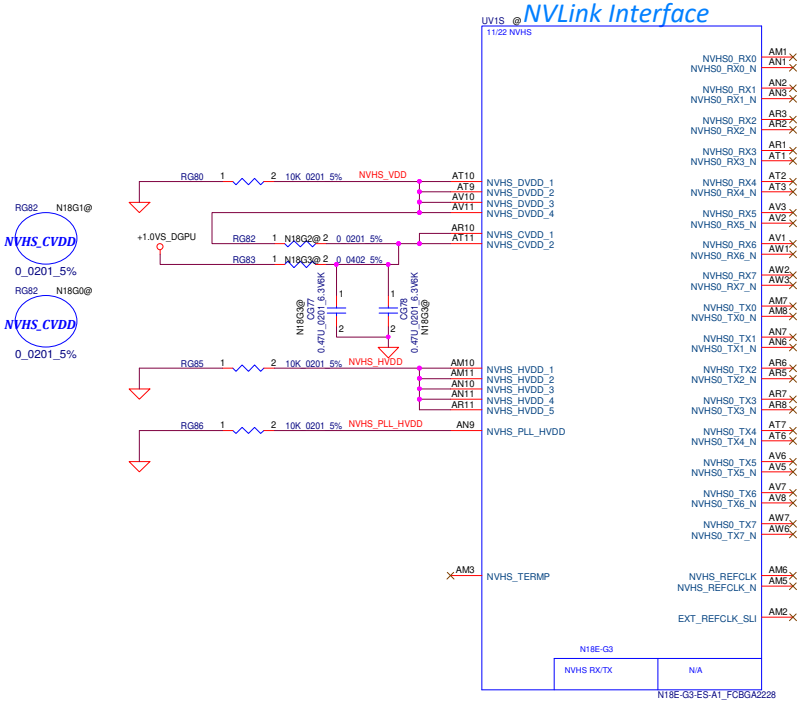
Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.			
Title	N18E(4/9) eDP, HDMI, DP		
Size	Document Number		Rev
	LA-J561P		1.0
Date:	Wednesday, February 26, 2020	Sheet	27 of 100

USB-C Display Interface



NVLink Interface



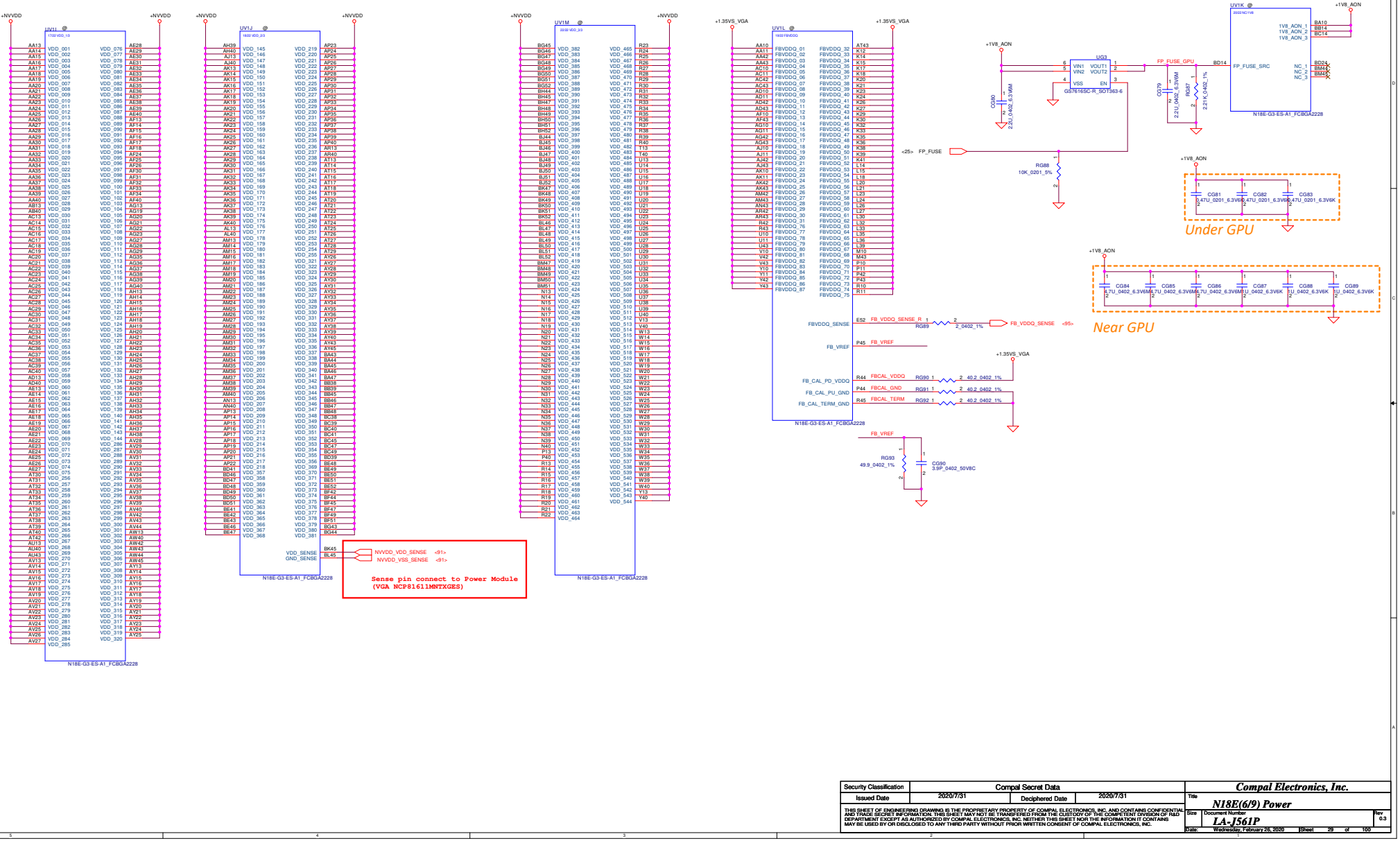
Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

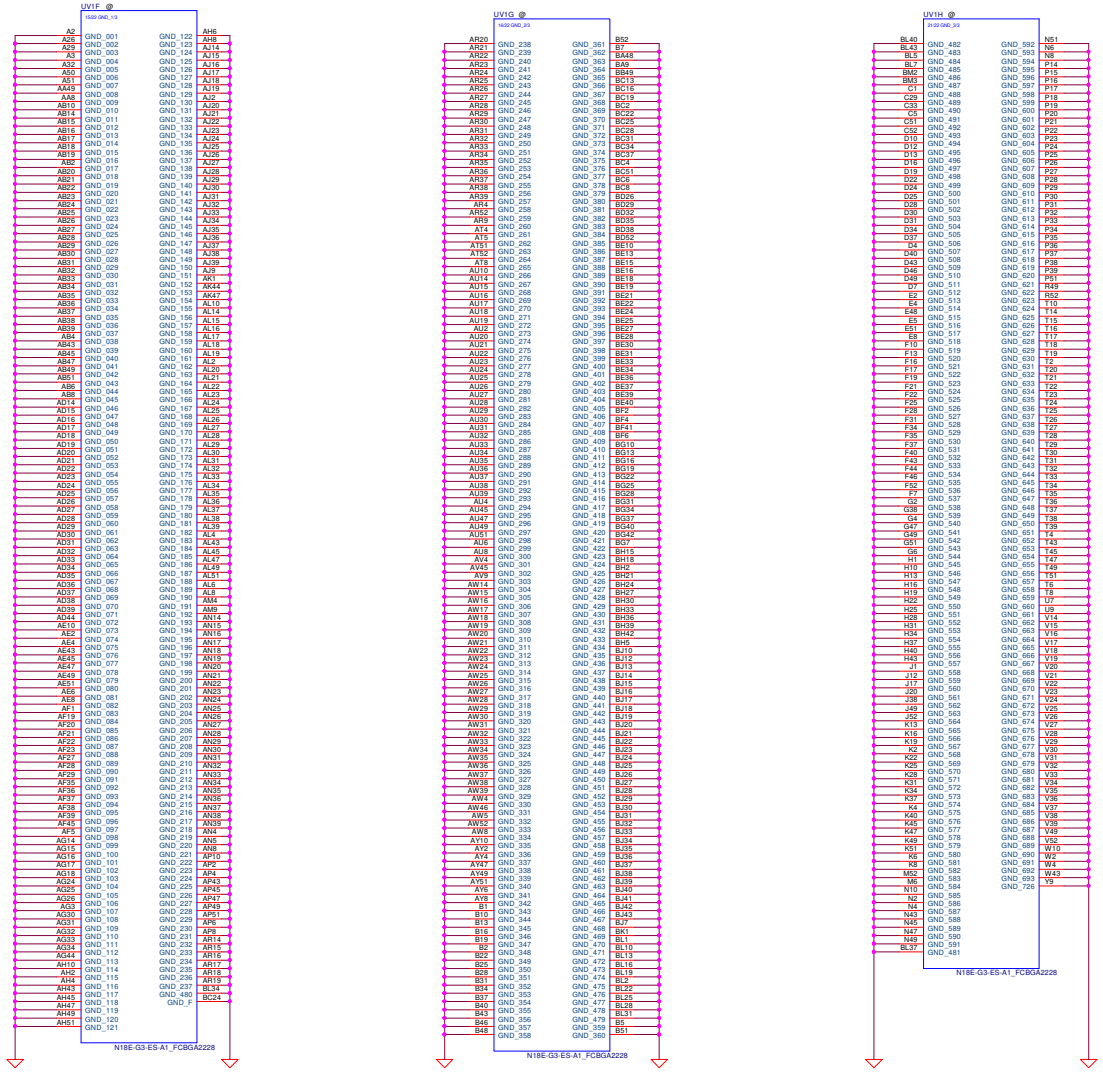
Title: **N18E(5/9) USB-C, NVLink**

Size	Document Number	Rev
	LA-J561P	1.0

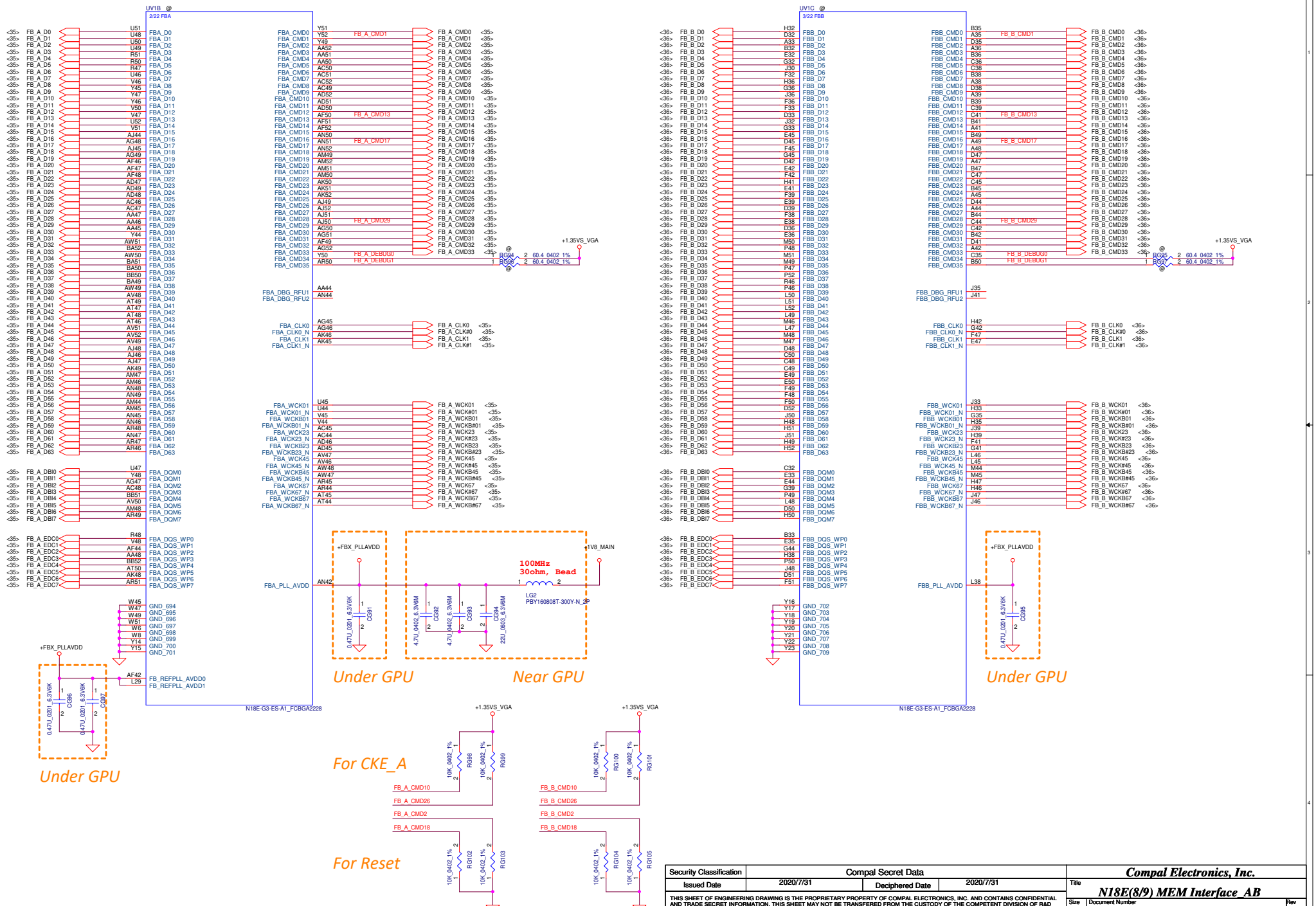
Date: Wednesday, February 26, 2020 Sheet 28 of 100



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/7/31	Deciphered Date 2020/7/31	Title: N18E(6/9) Power
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size: Document Number: LA-J561P Rev: 0.3
			Date: Wednesday, February 26, 2020 Sheet 29 of 100



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/7/31	Deciphered Date 2020/7/31	Title: N18E(7/9) GND
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size: Document Number: LA-J561P Rev: 1.0
			Date: Wednesday, February 26, 2020 Sheet 30 of 100



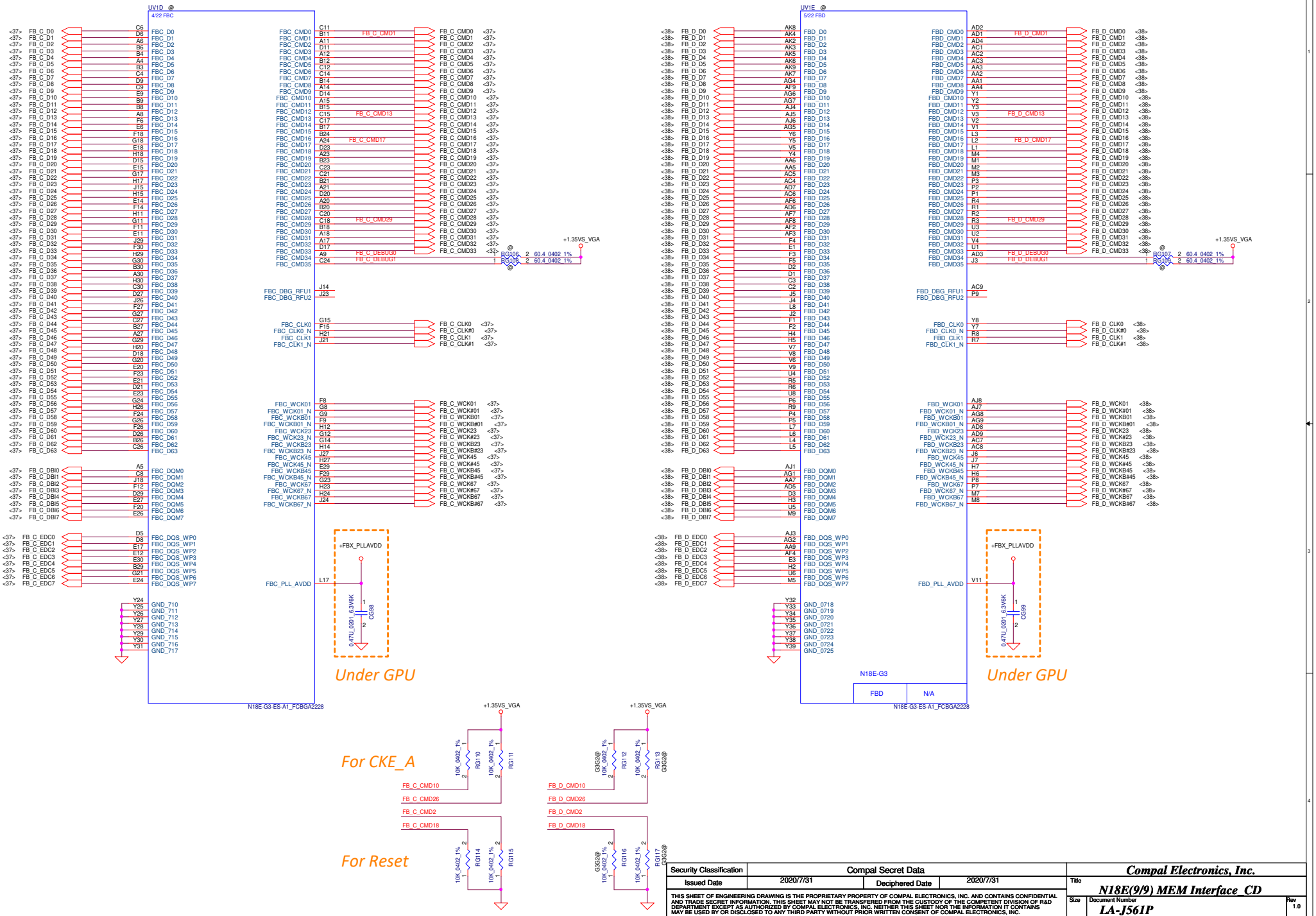
Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

Title: **N18E(8/9) MEM Interface_AB**

Size	Document Number	Rev
	LA-J561P	1.0

Date: Wednesday, February 26, 2020 | Sheet 31 of 100

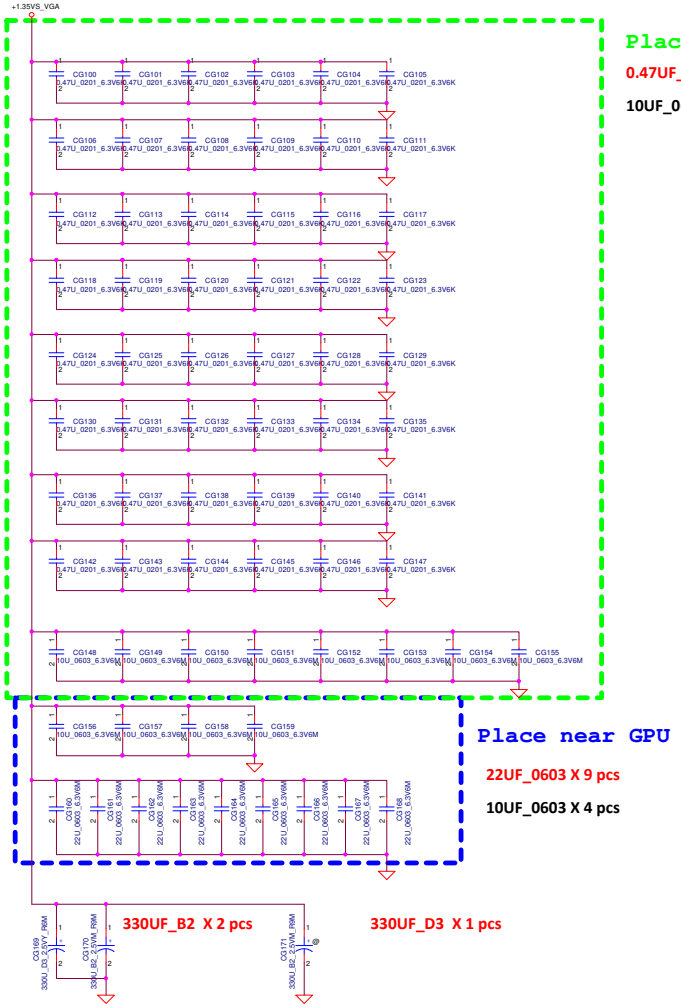


Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.			
Title	N18E(9/9) MEM Interface_CD		
Size	Document Number		Rev
	LA-J561P		1.0
Date:	Wednesday, February 26, 2020	Sheet	32 of 100

GPU Decoupling - NV Spec Recommendation

FBVDDQ_GPU



Place under GPU

0.47UF_0201 X 48 pcs

10UF_0603 X 8 pcs

Place near GPU

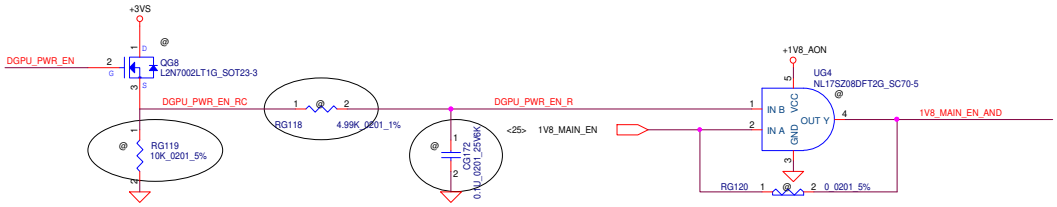
22UF_0603 X 9 pcs

10UF_0603 X 4 pcs

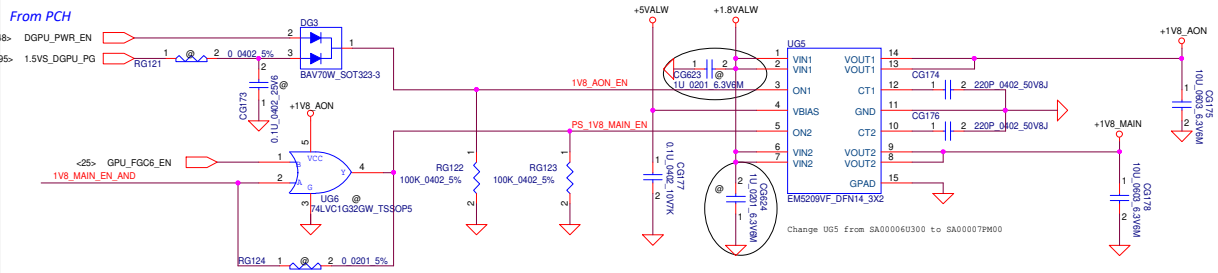
330UF_B2 X 2 pcs

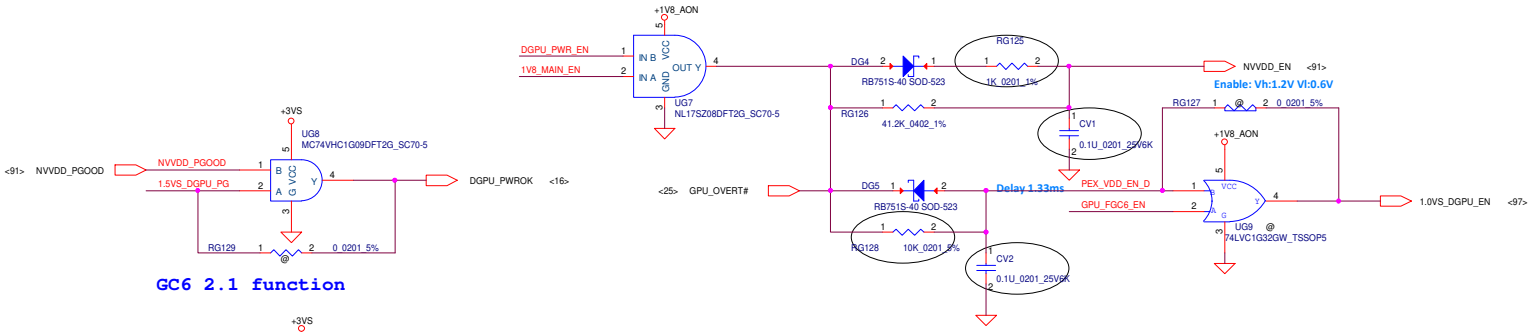
330UF_D3 X 1 pcs

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2020/7/31	Deciphered Date	2020/7/31	Title: GPU Decoupling_1
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size: Document Number: LA-J561P Rev: 1.0
				Date: Wednesday, February 26, 2020 Sheet 33 of 100

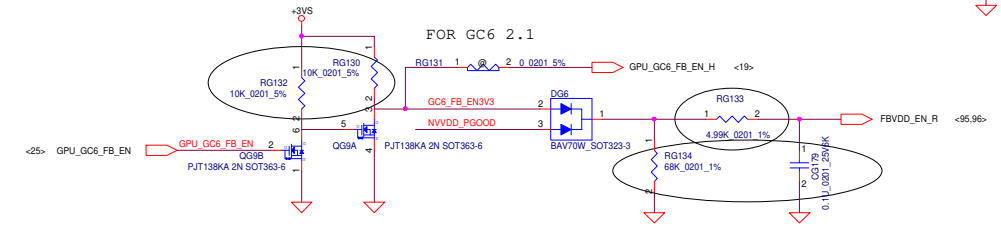


+1V8_AON / +1V8_MAIN





GC6 2.1 function



	1V8_AON	1V8_MAIN	NVVDD	PEXVDD	FBVDD
GC6 2.1	ON	OFF	OFF	OFF	ON
FGC6	ON	ON	OFF	ON	ON

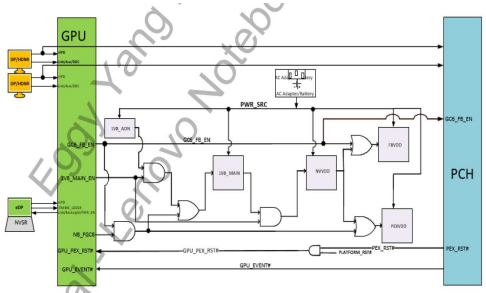
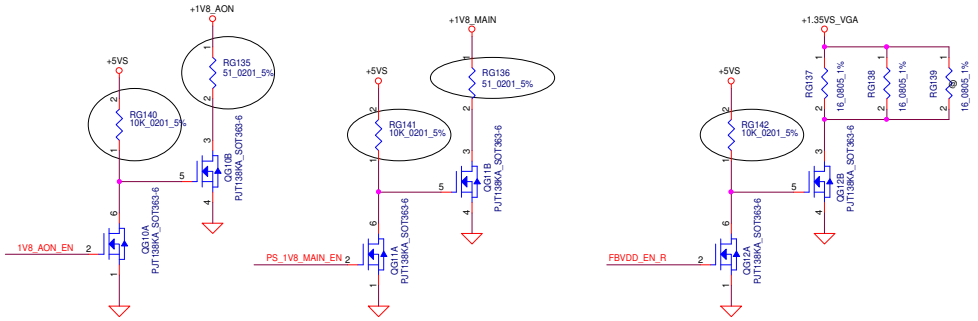


Figure 6.11 FGC6 Block Diagram



SB00001FN00 change to SB000016K00

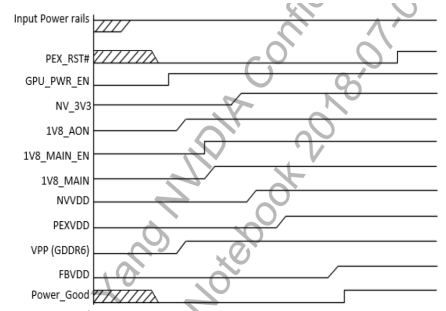


Figure 5.6 Power-Up Sequence

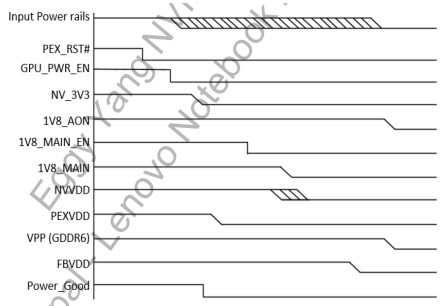
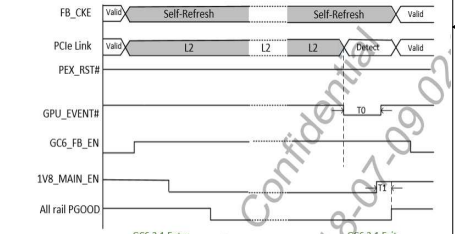


Figure 5.7 Power-Down Sequence



Note 1: GPU_EVENT# assertion and de-assertion event is required for GPU initiated GC6 2.1 Exit only.

Figure 6.12 GC6 2.1 Entry/Exit Sequence Timing Diagram

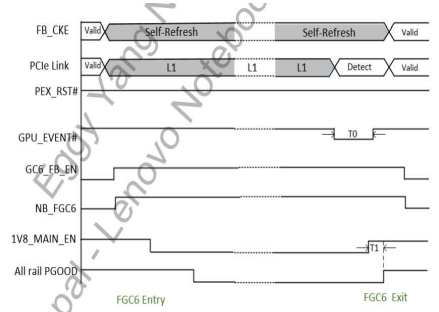
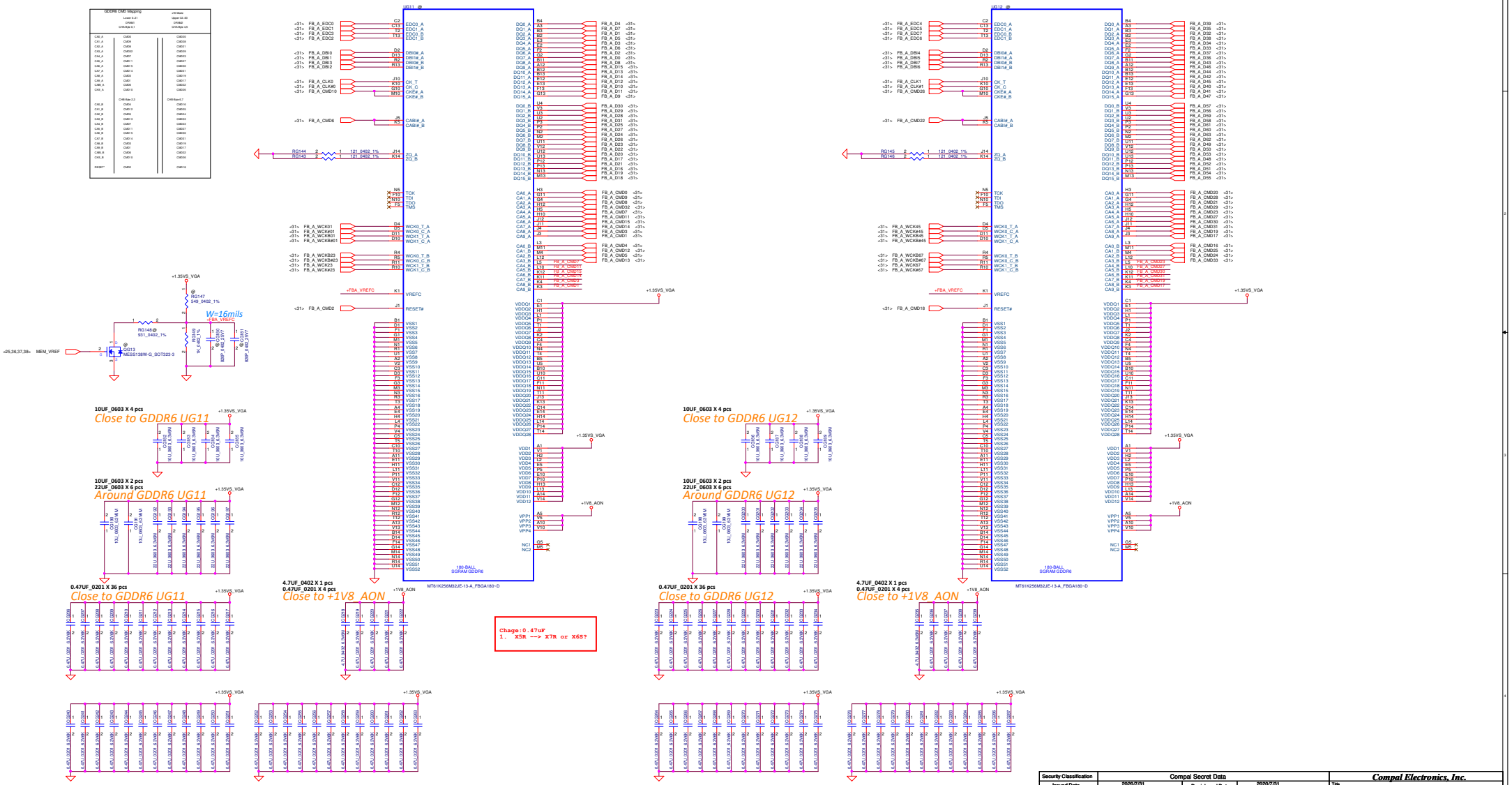


Figure 6.13 FGC6 Entry /Exit Timing Diagram

Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.	
Title	Sequence control
Size	Document Number: LA-J561P
Rev	0.3
Date:	Wednesday, February 26, 2020
Sheet	34 of 100

VRAM A



Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

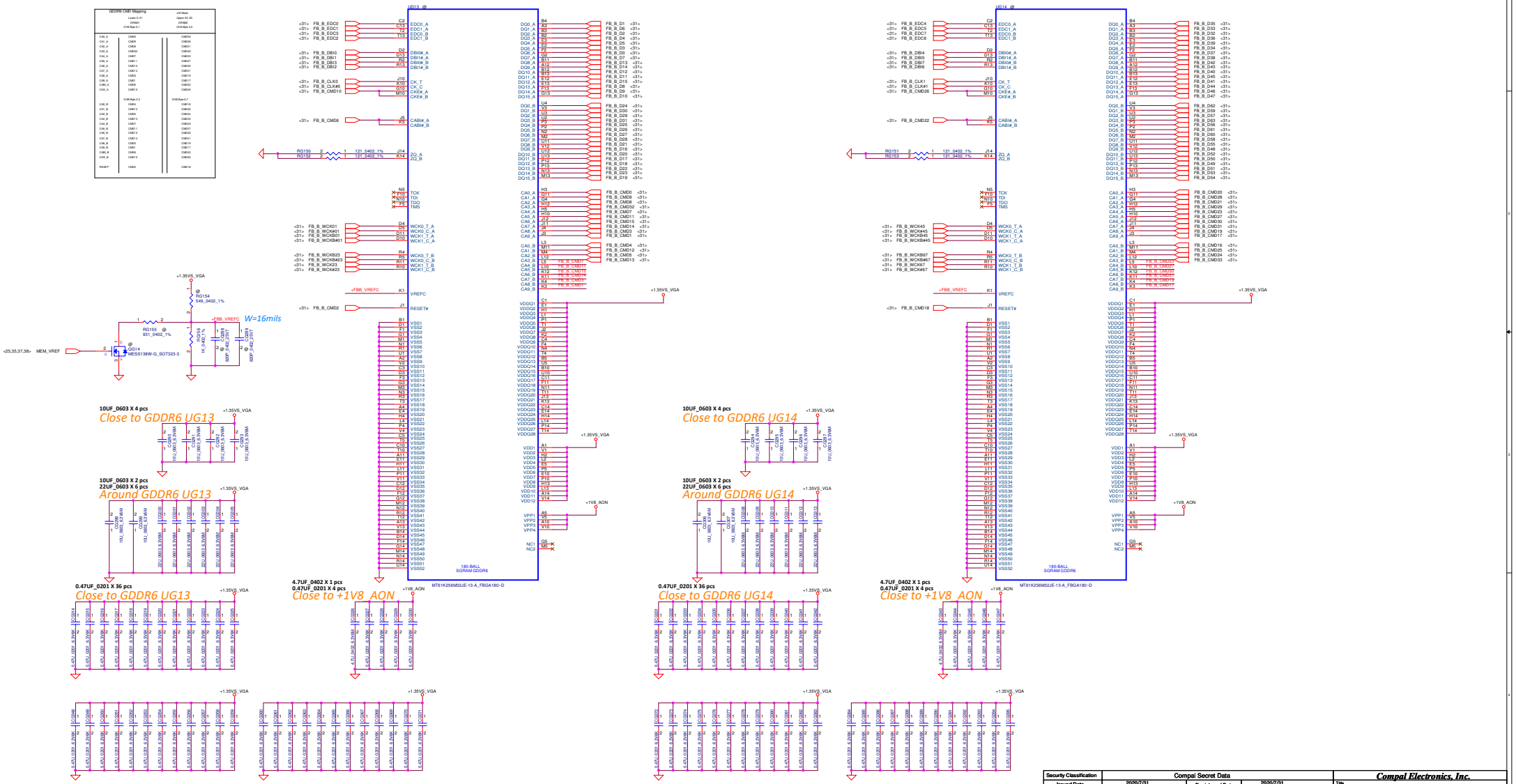
Compal Electronics, Inc.

Title: GDDR6_A_CH2

Size: Document Number: LA-J561P Rev: 1.0

Date: Wednesday, February 26, 2020 Sheet 35 of 100

VRAM B



Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

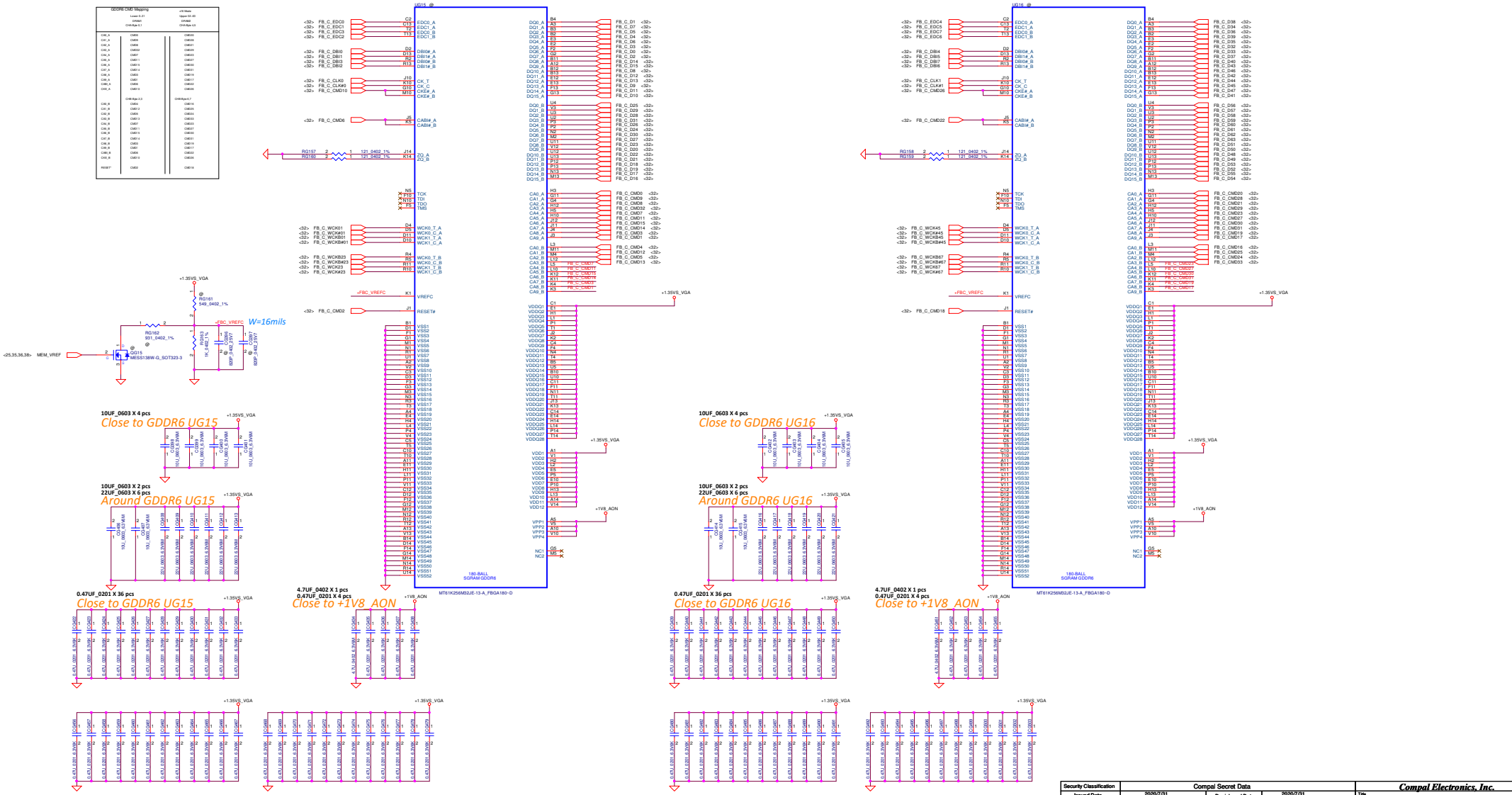
Compal Electronics, Inc.

Title: GDDR6_B_CH2

Size: | Document Number: LA-J561P | Rev: 1.0

Date: Wednesday, February 26, 2020 | Sheet 35 of 100

VRAM C



Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

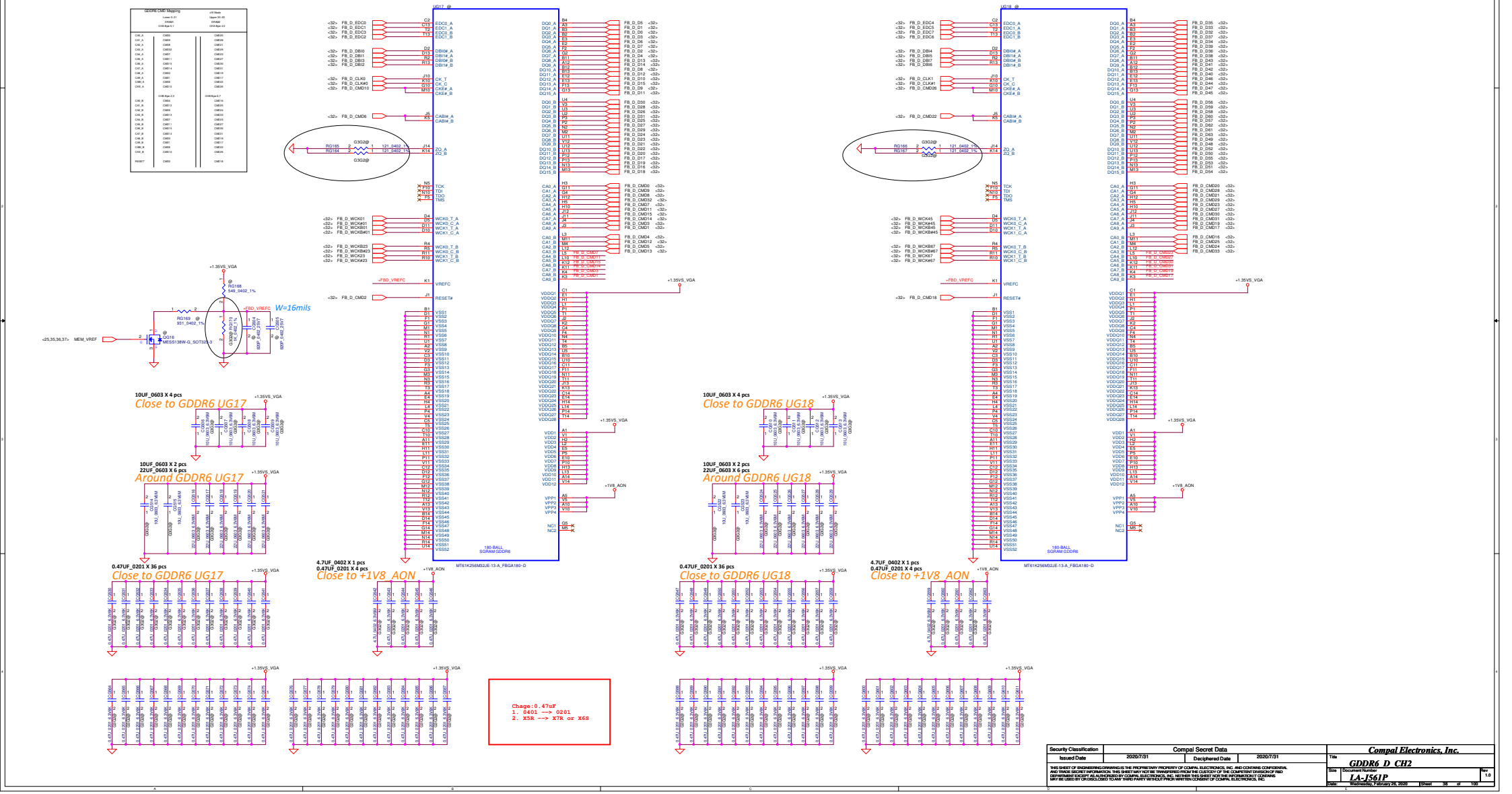
Compal Electronics, Inc.

Title: GDDR6_C_CH2

Size: Document Number: LA-J561P Rev: 1.0

Date: Wednesday, February 26, 2020 Sheet 37 of 100

VRAM D (N18G1,N18G0 No Need)



Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

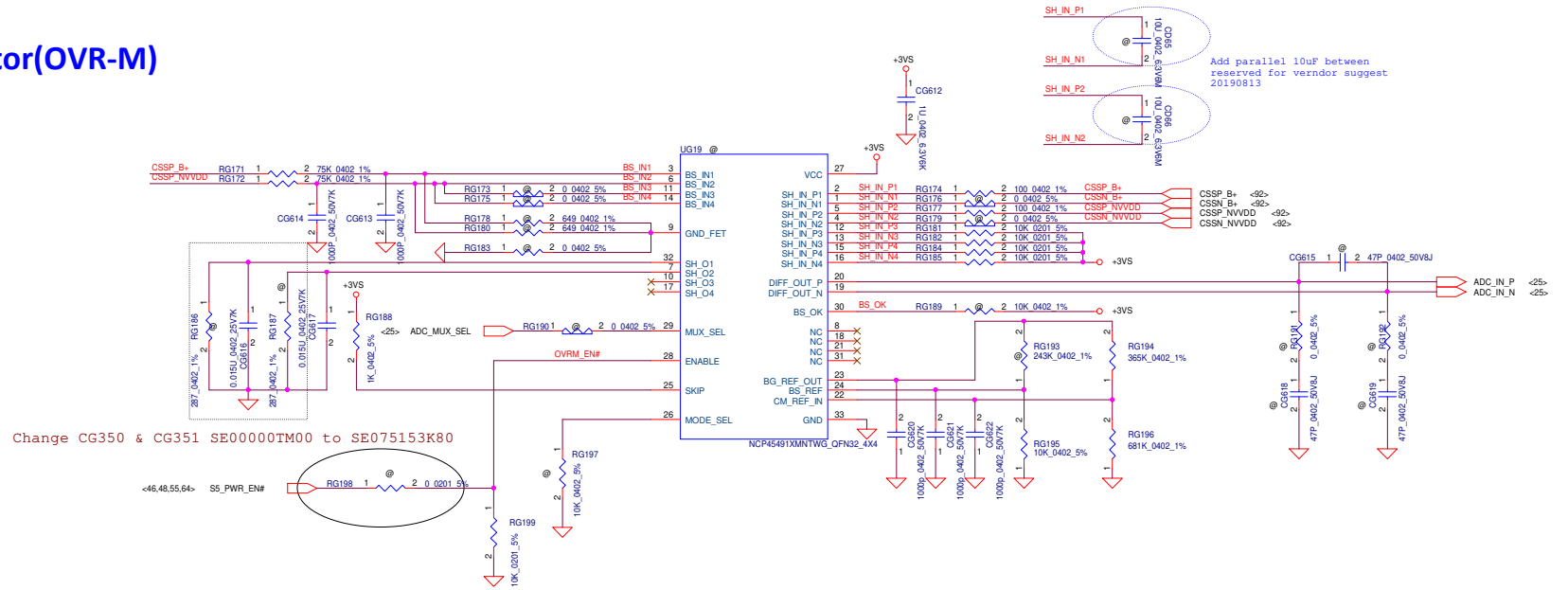
Compal Electronics, Inc.

Title: GDDR6_D_CH2

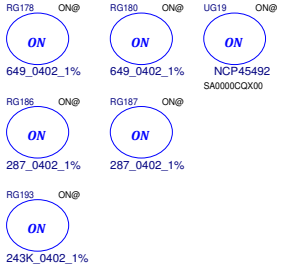
Size: Document Number: LA-J561P Rev: 1.0

Date: Wednesday, February 26, 2020 Sheet 38 of 100

Power Monitor(OVR-M)



OVR-M(OnSemi)



OVR-M(UPI)

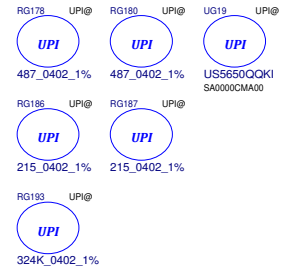


Table 13. Power Monitoring with OnSemi OVR-M

	Component Values				
GPU TGP	R954, 924	R977, R923	R950	R953, R952	C841, C836
150W+	649 Ω	169 Ω	243 kΩ	75 kΩ	1.0 nF
115W to 130W	649 Ω	191 Ω	243 kΩ	75 kΩ	1.0 nF
100W to 110W	649 Ω	221 Ω	243 kΩ	75 kΩ	1.0 nF
75W to 90W	649 Ω	287 Ω	243 kΩ	75 kΩ	1.0 nF
70W or lower	649 Ω	475 Ω	243 kΩ	75 kΩ	1.0 nF

NV location	R954, R924	R977, R923	R950	R953, R952	C841, C836
Y740 location	RG225, RG226	RG222, RG228	RG242	RG259, RG227	CG341, CG342

ON (X7678038L59)		
UG19	SA0000C9Q00	S IC NCP45491XMNTWG QFN 32P MONITOR
RG225, RG226	SD000008O80	S RES 1/16W 649 +-1% 0402
RG222, RG228	SD034287080	S RES 1/16W 287 +-1% 0402
RG242	SD000004200	S RES 1/16W 243K +-1% 0402

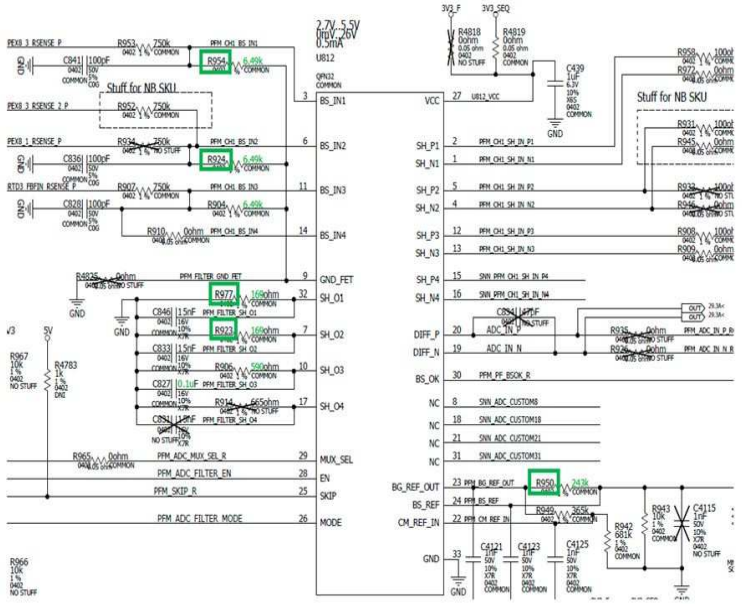
Table 14. Power Monitoring with uPI OVR-M

	Component Values				
GPU TGP	R954, 924	R977, R923	R950	R953, R952	C841, C836
150W+	487 Ω	127 Ω	324 kΩ	75 kΩ	1.0 nF
115W to130W	487 Ω	143 Ω	324 kΩ	75 kΩ	1.0 nF
100W to 110W	487 Ω	165 Ω	324 kΩ	75 kΩ	1.0 nF
75W to 90W	487 Ω	215 Ω	324 kΩ	75 kΩ	1.0 nF
70W or lower	487 Ω	357 Ω	324 kΩ	75 kΩ	1.0 nF

NV location	R954, R924	R977, R923	R950	R953, R952	C841, C836
Y740 location	RG225, RG226	RG222, RG228	RG242	RG259, RG227	CG341, CG342

uPI (X7678038L60)		
UG19	SA0000CEV00	S IC US5650PQKI WQFN 32P POWER MONITOR
RG225, RG226	SD00000EL80	S RES 1/16W 487 +-1% 0402
RG222, RG228	SD000000180	S RES 1/16W 215 +-1% 0402
RG242	SD034324380	S RES 1/16W 324K +-1% 0402

Reference ORB R997 ,R923

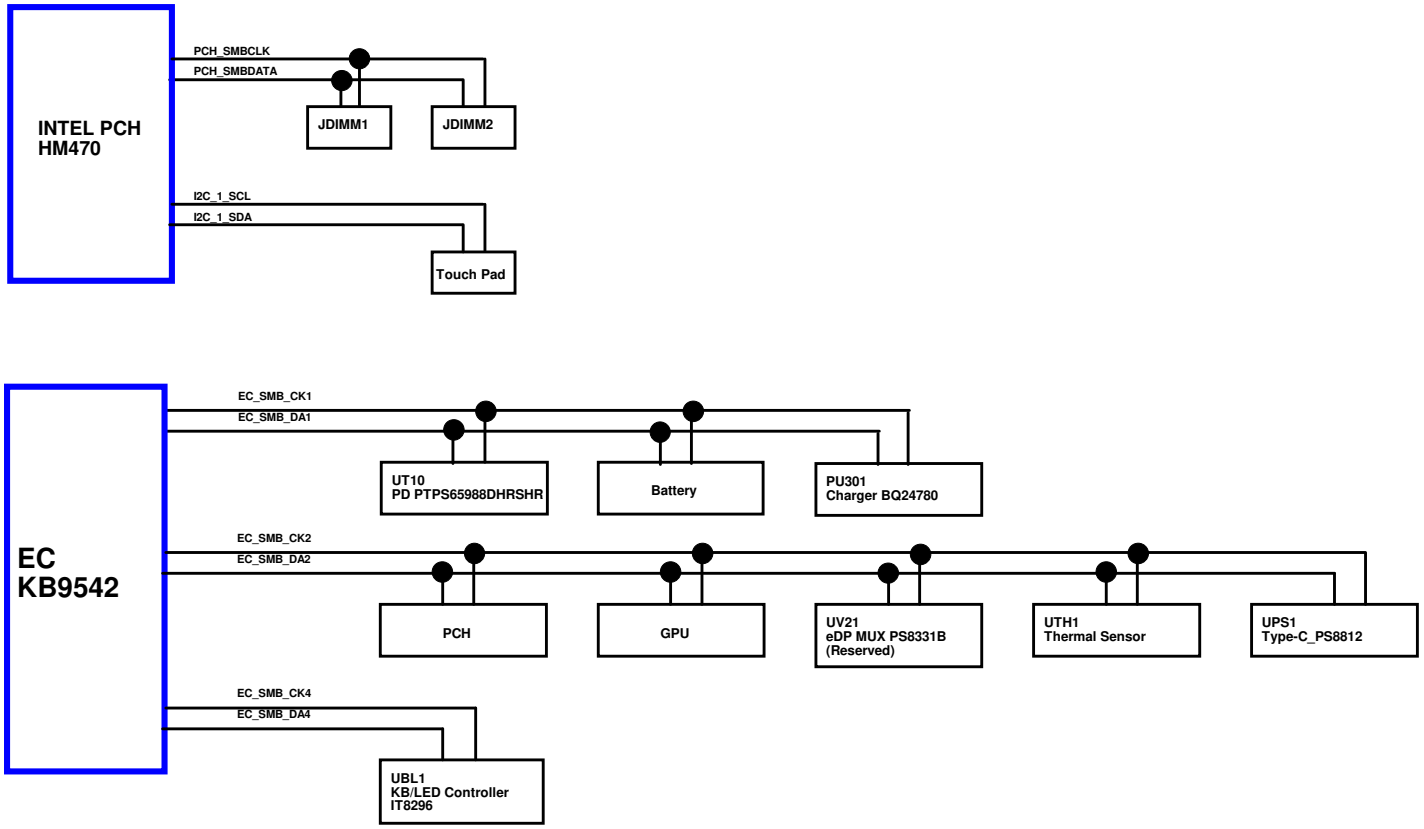


'igure 1. Power Monitoring with OVR-M

Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

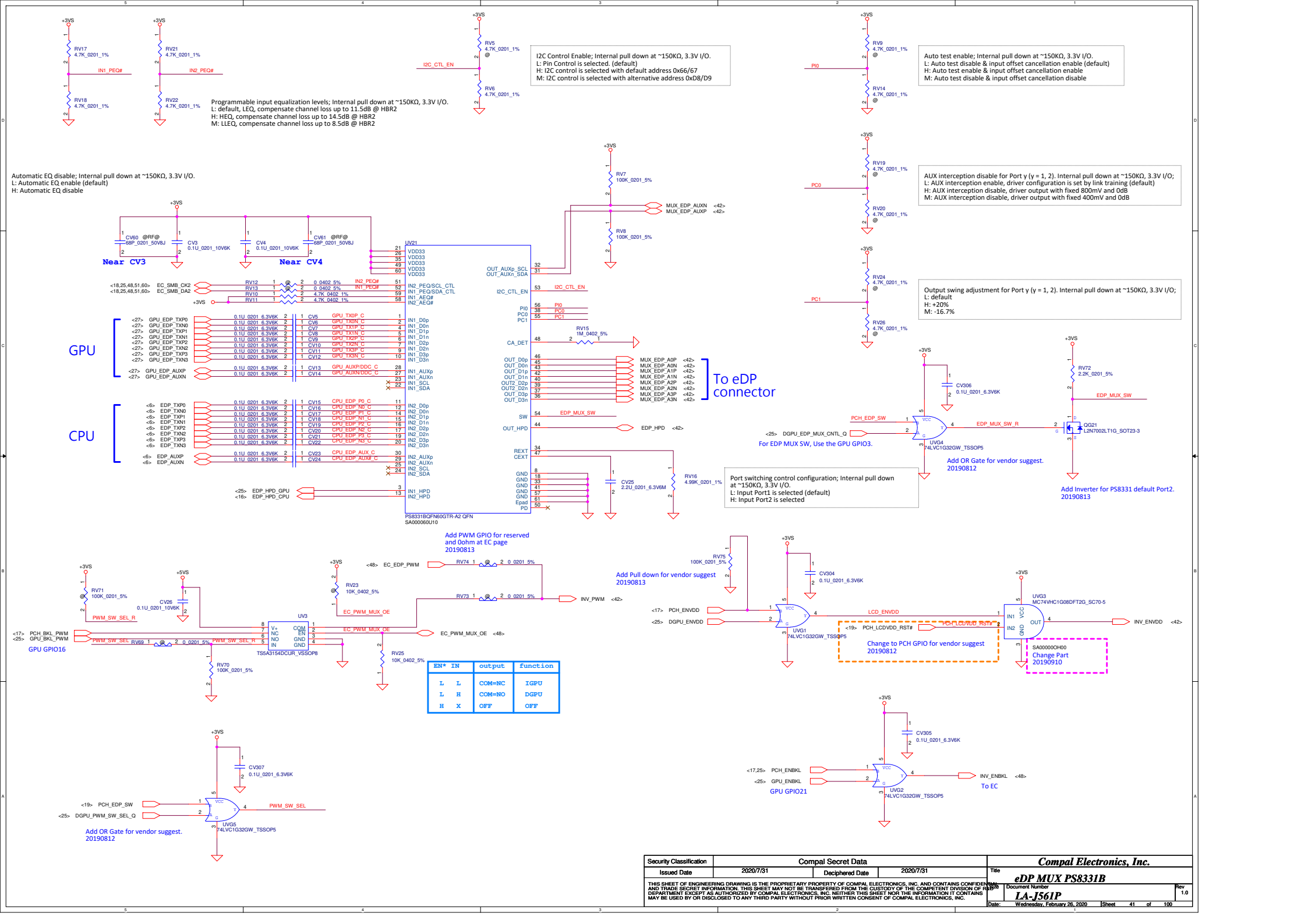
Compal Electronics, Inc.			
Title: OVR-M			
Size	Document Number: LA-J561P		Rev: 1.0
Date: Wednesday, February 26, 2020	Sheet 39 of 100		

SMBus Block Diagram



Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.			
Title: TBD			
Size	Document Number: LA-J561P		Rev: 1.0
Date: Wednesday, February 26, 2020	Sheet 40 of 100		



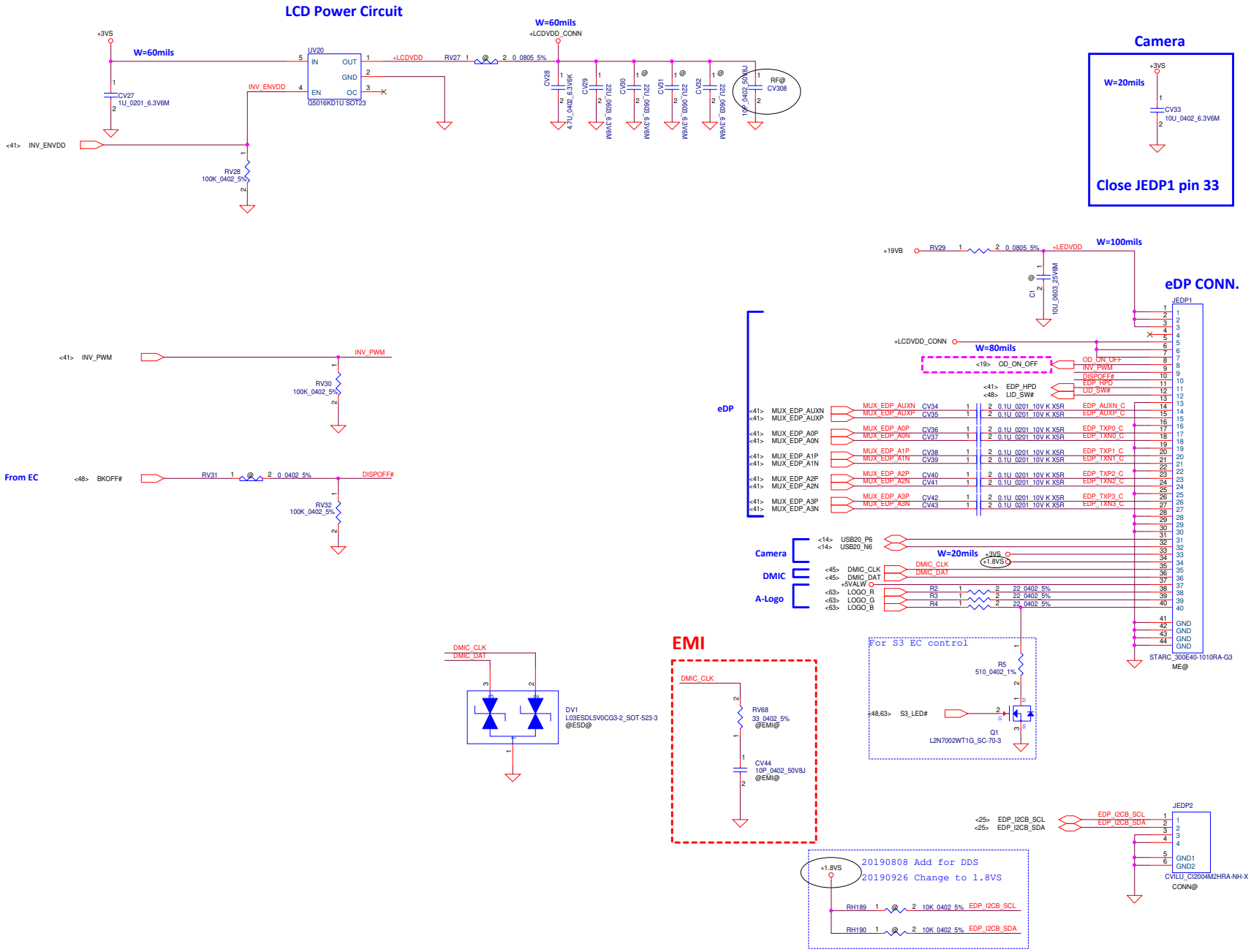
Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

Title: eDP MUX PS8331B

Size: B | Document Number: LA-J561P | Rev: 1.0

Date: Wednesday, February 26, 2020 | Sheet 41 of 100



Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

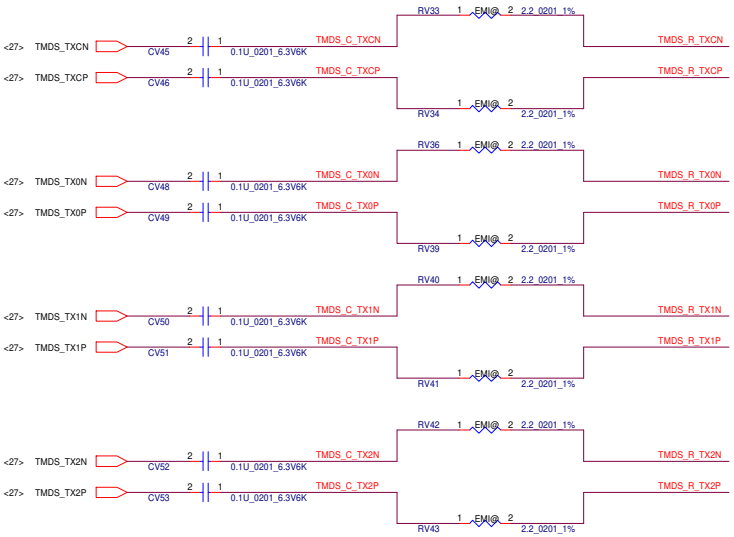
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

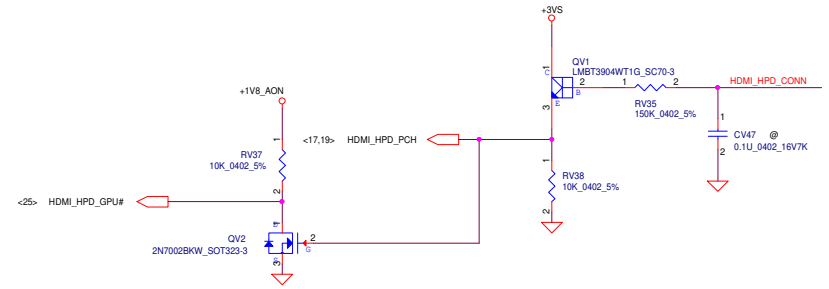
Compal Electronics, Inc.

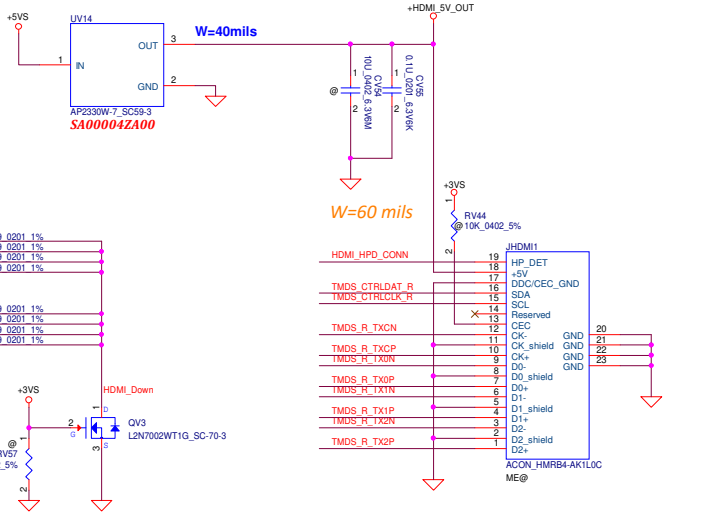
Title: **eDP / Camera**

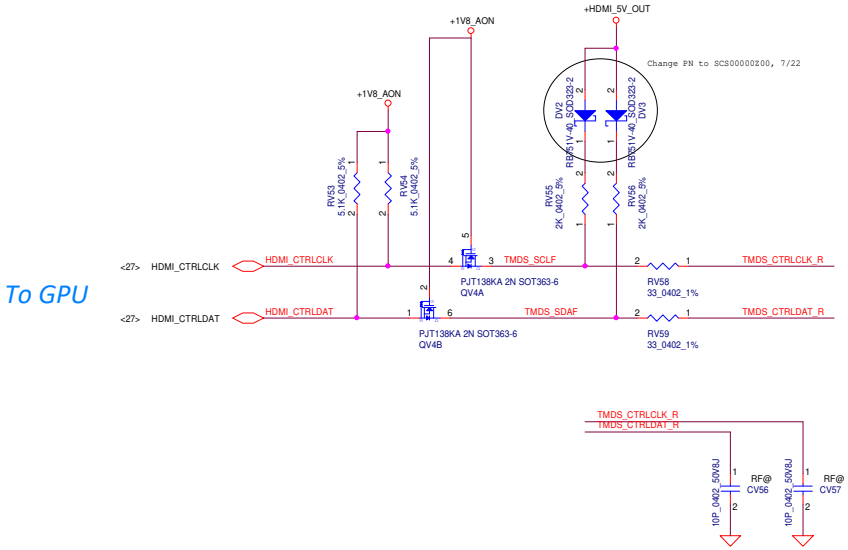
Size	Document Number	Rev
C	LA-J561P	1.0

Date: Wednesday, February 26, 2020 | Sheet 42 of 100









Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.			
Title: HDMI			
Size	Document Number: LA-J561P		Rev: 1.0
Date: Wednesday, February 26, 2020	Sheet 43 of 100		

Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

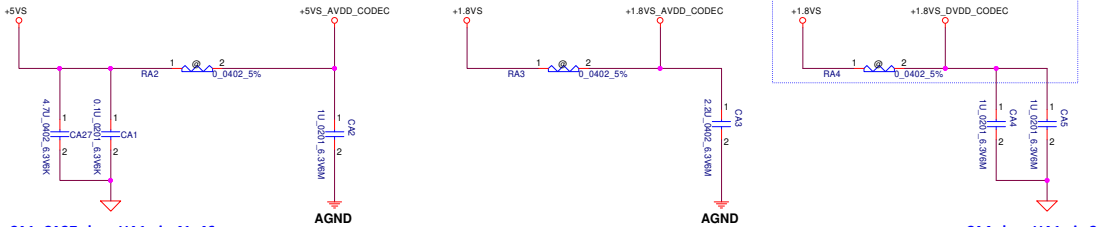
Compal Electronics, Inc.

Title: **Reserved**

Size	Document Number	Rev
	LA-J561P	1.0

Date: Wednesday, February 26, 2020 | Sheet 44 of 100

POWER



CA1, CA27 close UA1 pin 41, 46

CA2 close UA1 pin 40

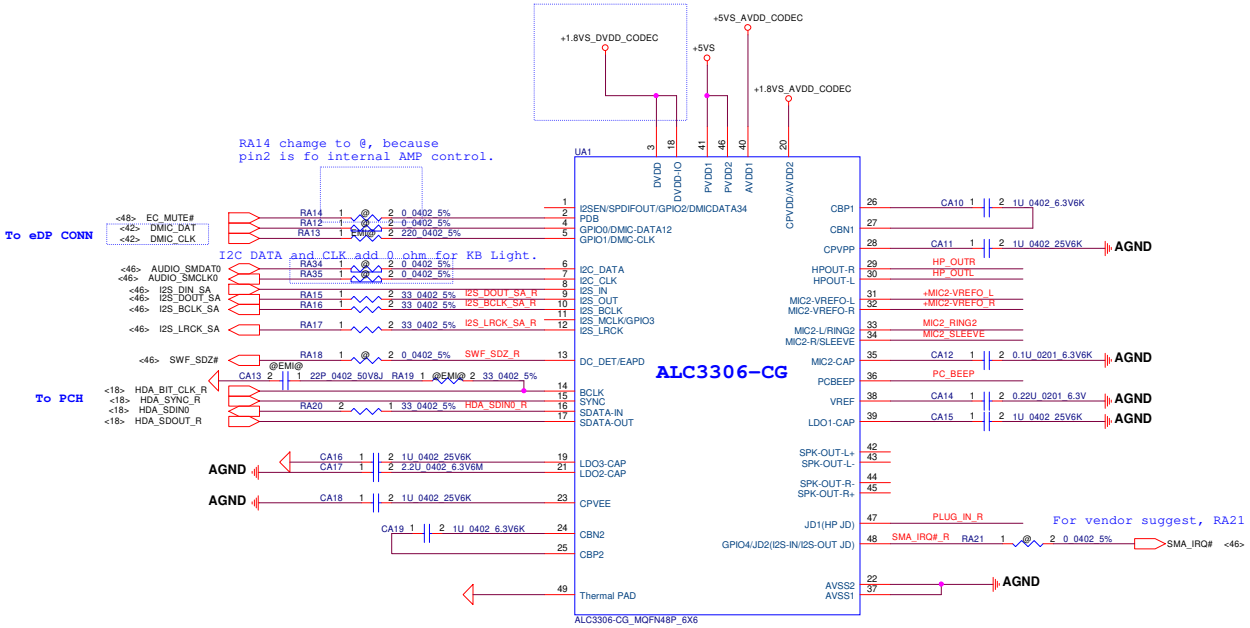
CA3 close UA1 pin 20

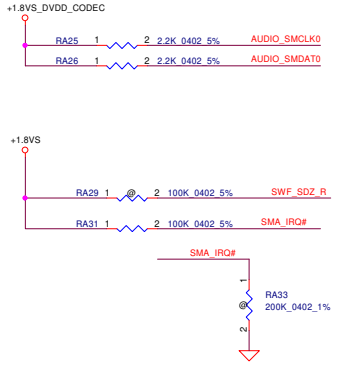
CA4 close UA1 pin 3

CA5 close UA1 pin 18

ALC3306

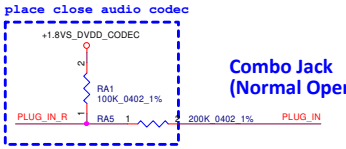
The AMP is 1.8V, so the DVDD should be 1.8V.
DVDD >= DVDDIO



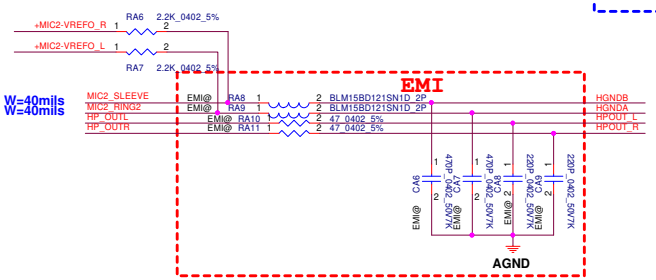


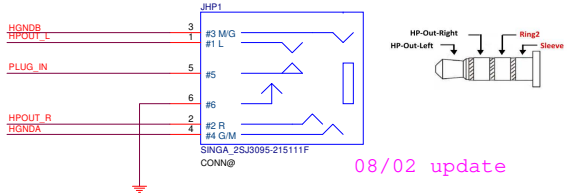
Audio Jack (close Audio codec)

09/18 update to
+1.8VS_DVDD_CODEC

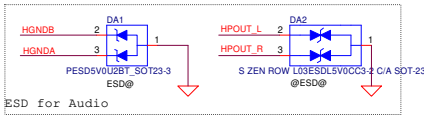


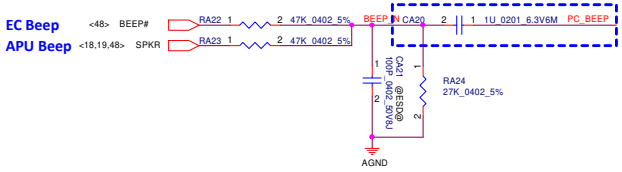
Combo Jack
(Normal Open)

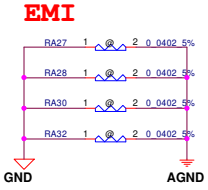


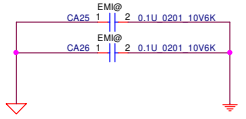


08/02 update



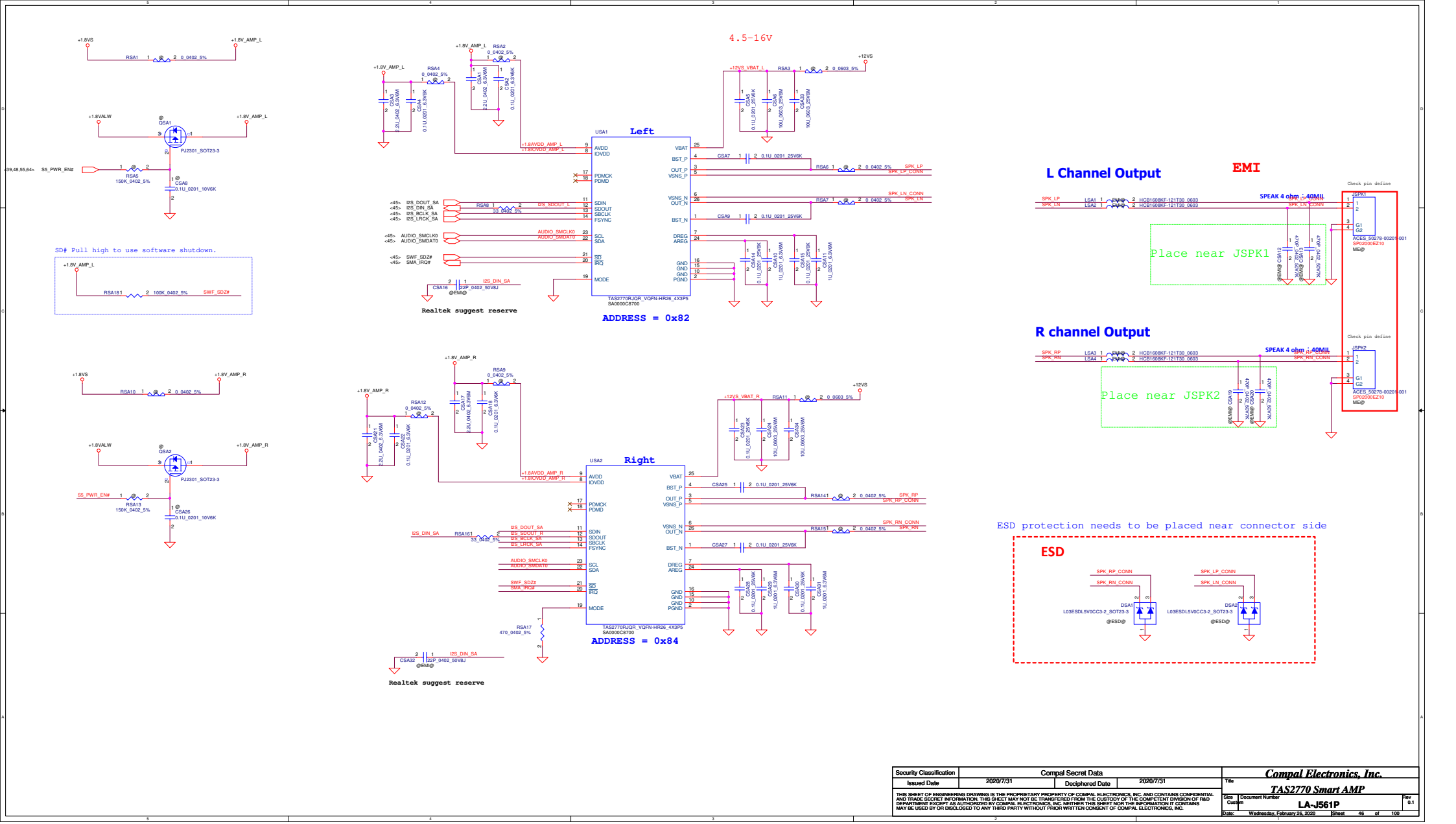






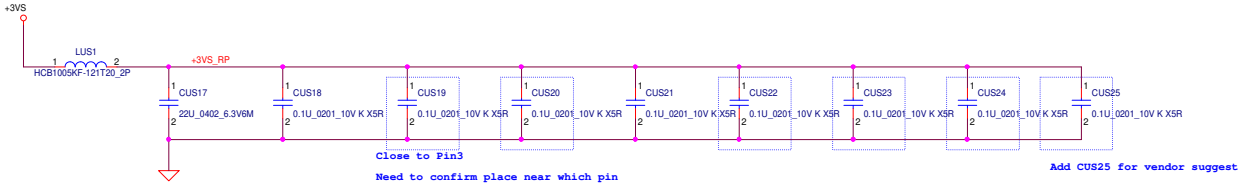
Security Classification	Compal Secret Data	GND	
Issued Date	2020/7/31	Deciphered Date	2020/7/31

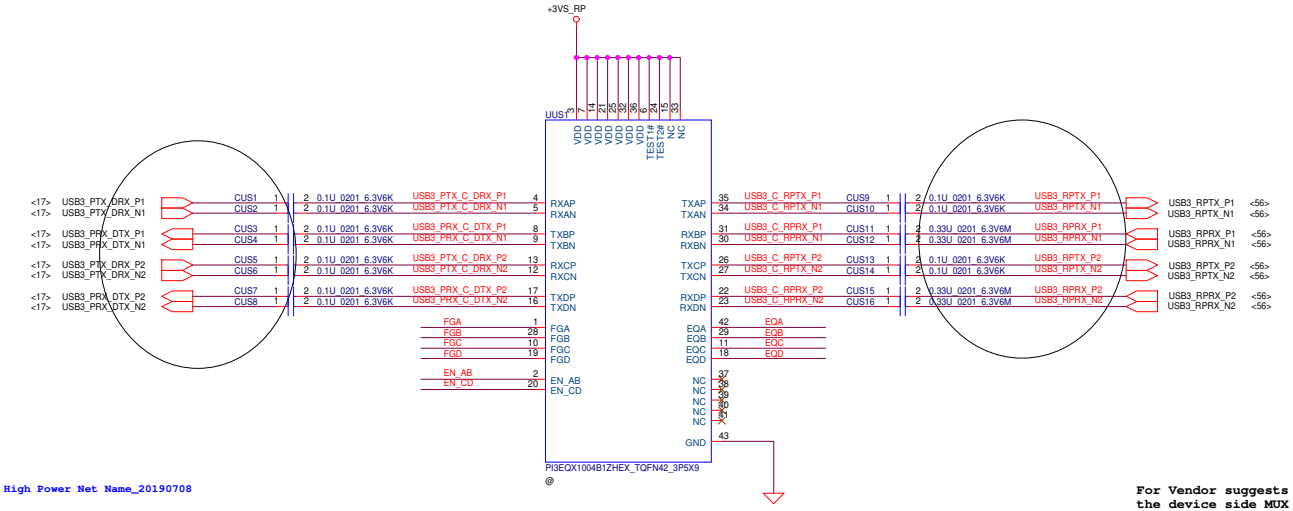
Compal Electronics, Inc.			
Title	HD Audio Codec_ALC3268		
Size	Document Number		Rev
Custom	LA-J561P		0.1
Date:	Wednesday, February 26, 2020	Sheet	45 of 100



Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.			
Title	TAS2770 Smart AMP		
Size	Document Number		Rev
Custom	LA-J561P		0.1
Date:	Wednesday, February 26, 2020	Sheet	46 of 100

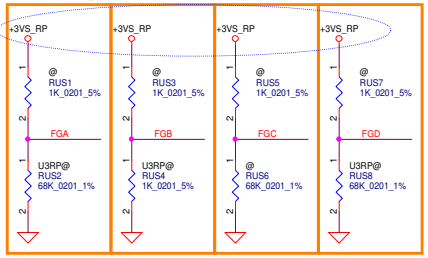




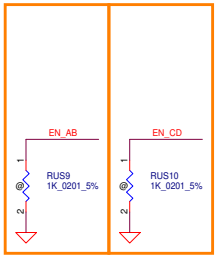
Update Pull High Power Net Name_20190708

For Vendor suggests the RC can provide
the device side MUX tolerance enough to 3.3V DC level or not.
RUS19, RUS20, RUS21 and RUS22 = 200kohm.
CUS11, CUS12, CUS15 and CUS16 = 0.33uF.

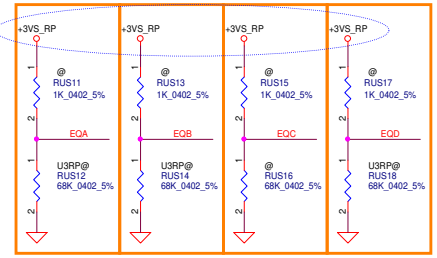
DC flat gain selection

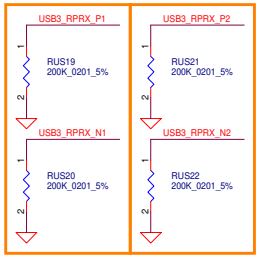


Channel Enable



EQ selection

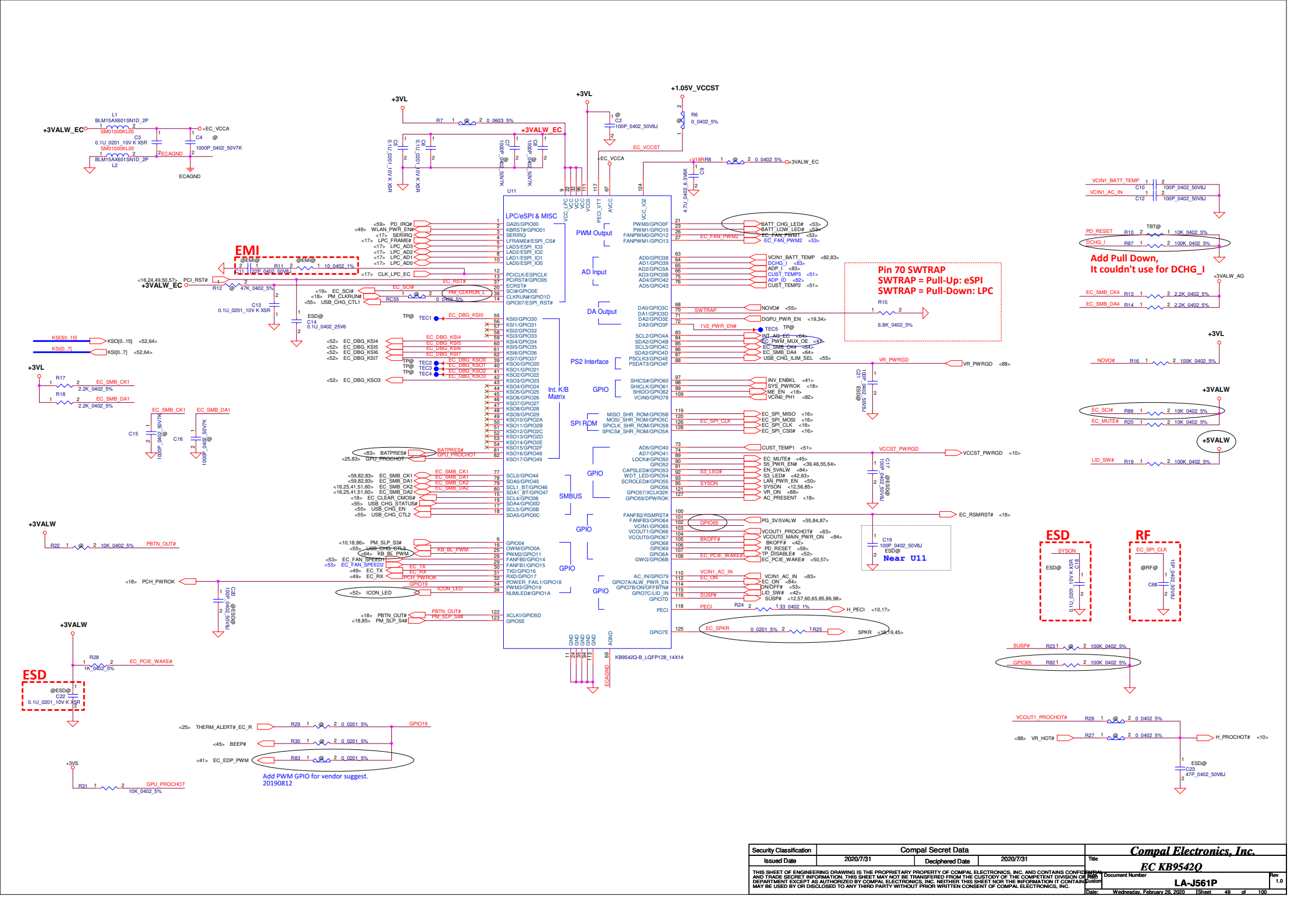




Waiting for Layout TLC to set up EQ anf Gain value.

Post-channel / Pre-channel	less than 2inch		2inch to 4inch		up to 4inch	
For PI3EQX1004/B1	TX	RX	TX	RX	TX	RX
under 7inch	EQA=68kohm to GND FGA=Pull low to 68kohm	EQB=68kohm to GND FGB=Pull low to GND	EQA=68kohm to GND FGA=Pull low to 68kohm	EQB=68kohm to GND FGB=Pull low to GND	EQA=68kohm to GND FGA=Floating	EQB=Floating FGB=Pull low to GND
7inch to 9inch	EQA=Floating FGA=Pull low to 68kohm	EQB=68kohm to GND FGB=Floating	EQA=Floating FGA=Pull low to 68kohm	EQB=68kohm to GND FGB=Floating	EQA=Floating FGA=Floating	EQB=Floating FGB=Floating
up to 12inch	EQA=1kohm to VDD FGA=Pull low to 68kohm	EQB=68kohm to GND FGB=1kohm to VDD	EQA=1kohm to VDD FGA=Pull low to 68kohm	EQB=68kohm to GND FGB=1kohm to VDD	EQA=1kohm to VDD FGA=Floating	EQB=Floating FGB=1kohm to VDD

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/7/31	Deciphered Date 2020/7/31	Title: USB3.1 GEN2 Redriver
Size	Document Number: LA-J561P		Rev: 1.0
Date: Wednesday, February 26, 2020	Sheet 47 of 100		



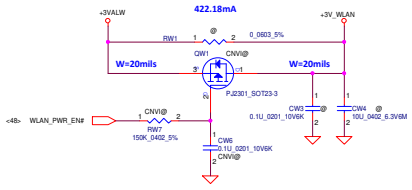
Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

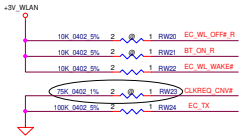
Compal Electronics, Inc.			
Title: EC KB9542Q			
Size: Custom	Document Number: LA-J561P		Rev: 1.0
Date: Wednesday, February 26, 2020	Sheet 48 of 100		

NGFF Wireless LAN / BT (Key E) [PCIE+USB/CNVi]

For Power consumption Measurement

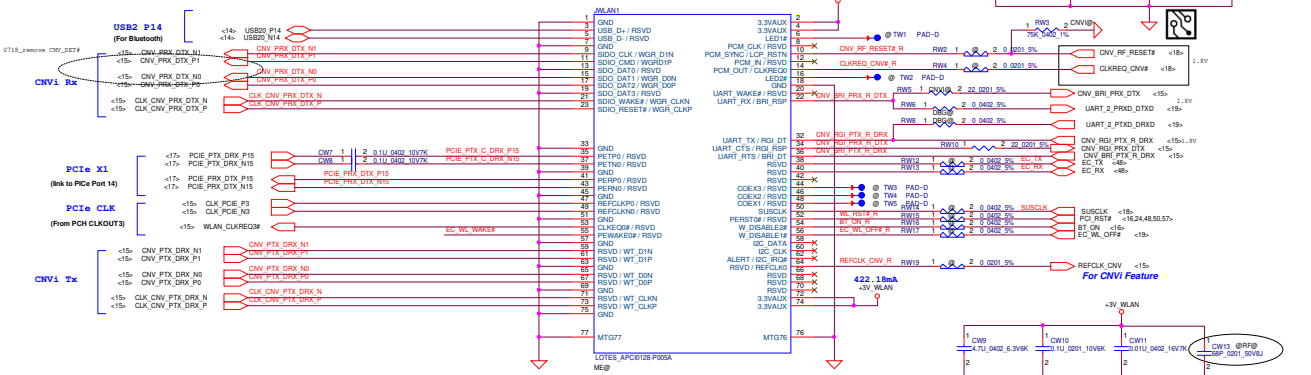


The connectivity module power supply pin shall be connected directly to thr rail DSW.
From
567240_Intel_Wireless_AC_9560_Jefferson_Peak_EPS_Rev1.1



Harrison Peak:800mA@peak current

KEY E



Follow 566468_CNL_UY_PDG_Rev0p73.pdf

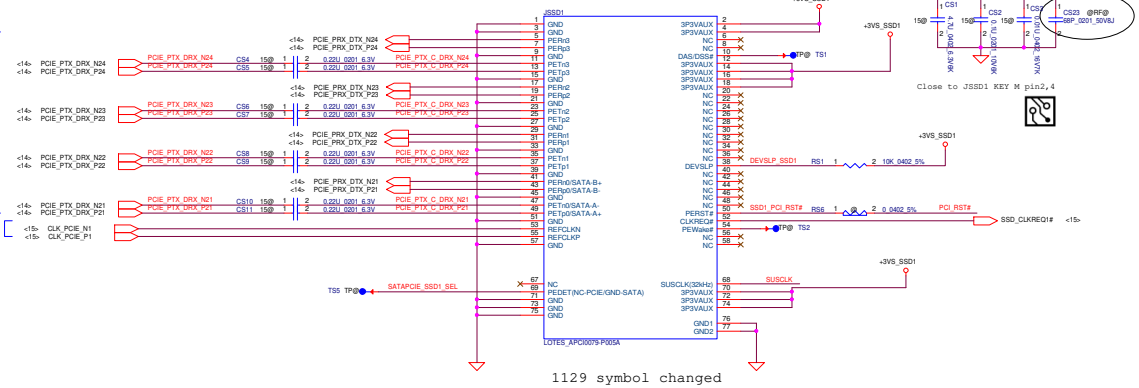
KEY M for 15" only SSD

NGFF SSD1 (KEY M)

PCIE X4
(link to PICE Port 21~24)

PCIE CLK
(From PCH CLKOUT1)

For Power consumption Measurement



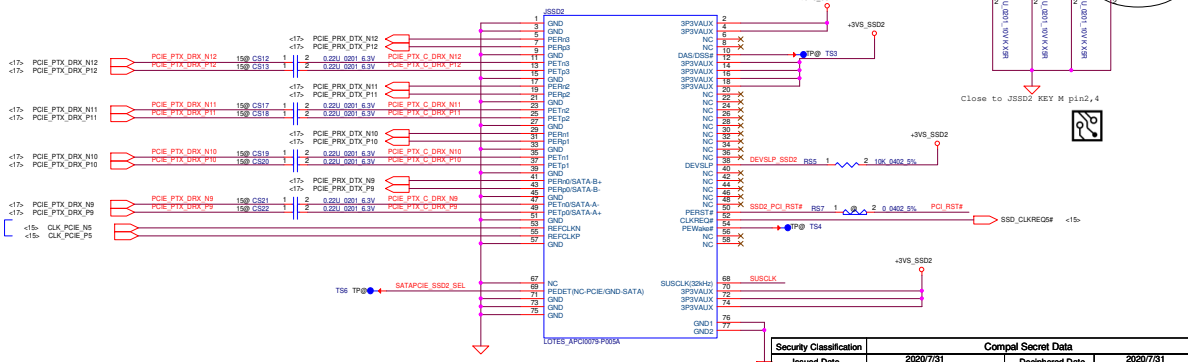
1129 symbol changed

NGFF SSD2 (KEY M)

PCIE X4
(link to PICE Port 9~12)

PCIE CLK
(From PCH CLKOUT5)

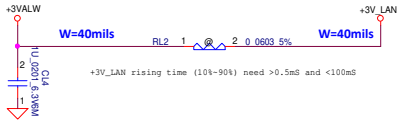
For Power consumption Measurement

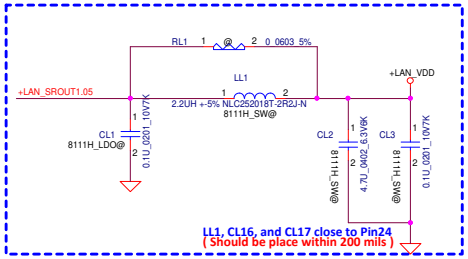


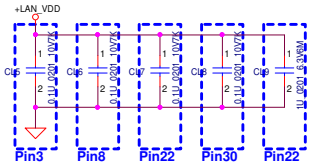
Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

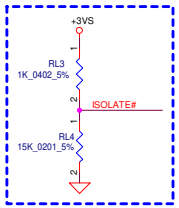
Compal Electronics, Inc.	
Title	WLAN(KEY E)/SSD(KEY M)
Size	Document Number: LA-J561P
Rev	1.0
Date: Wednesday, February 26, 2020	Sheet 49 of 100

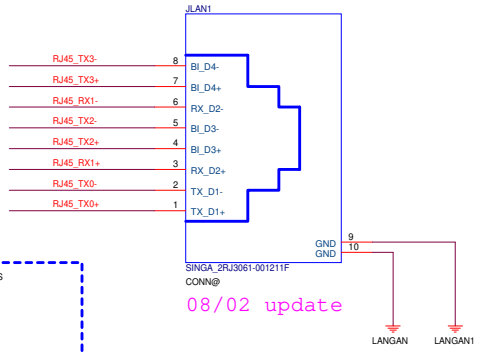
RJ-45 CONN.

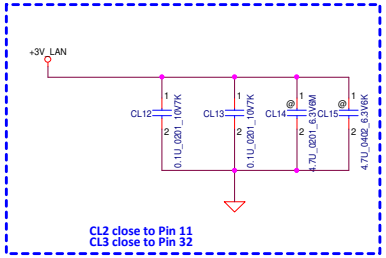


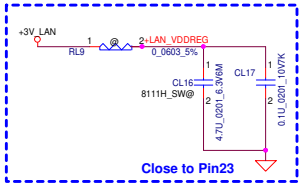


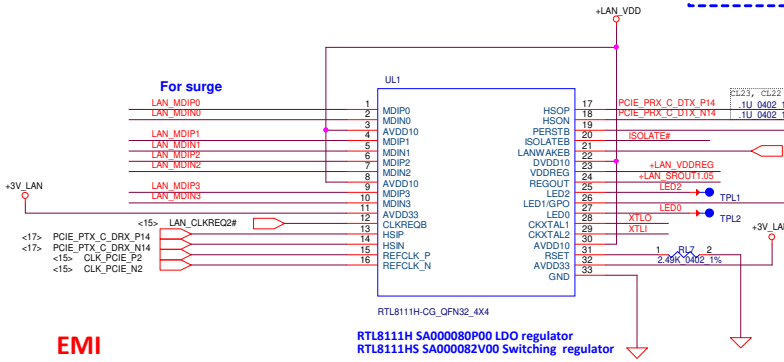


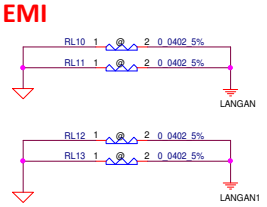


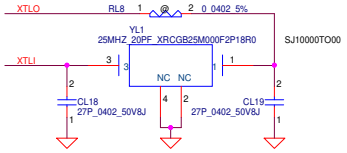


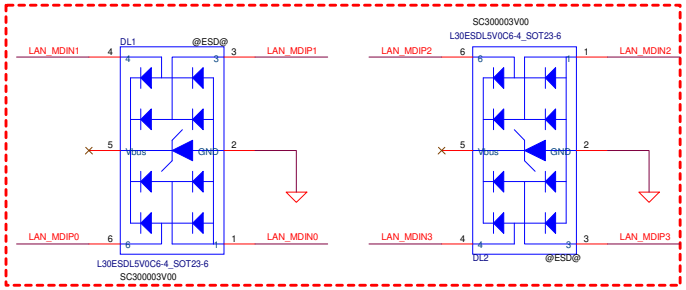


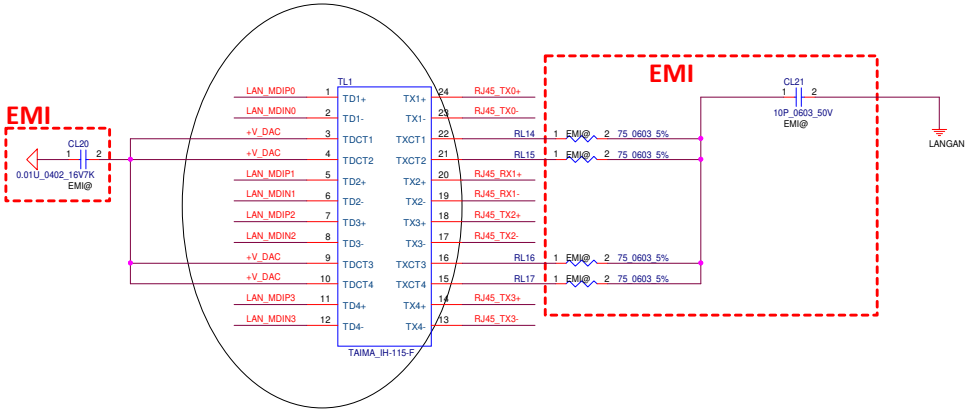






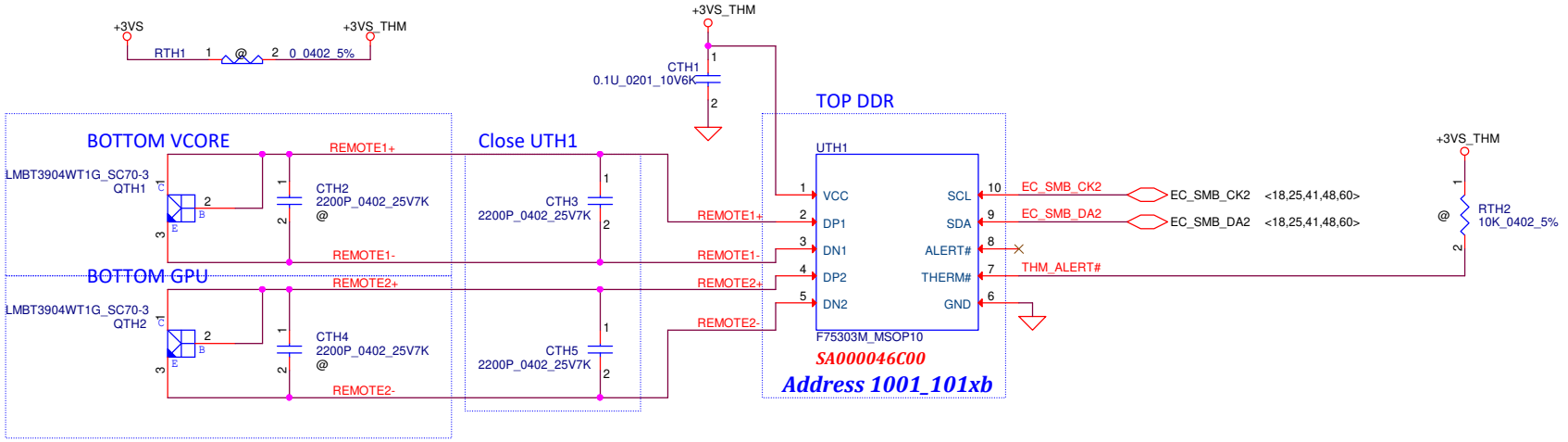






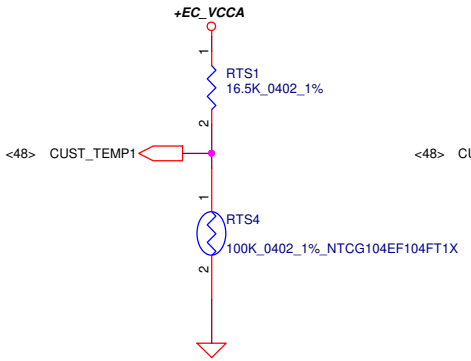
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/7/31	Deciphered Date	2020/7/31
Title	LAN_RTL8111H/RTL8107E		
Size C	Document Number LA-J561P		Rev 1.0
Date: Wednesday, February 26, 2020	Sheet 50 of 100		

THERMAL SENSOR For Smart Performance

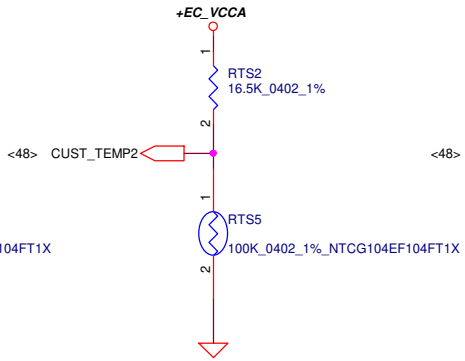


REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"

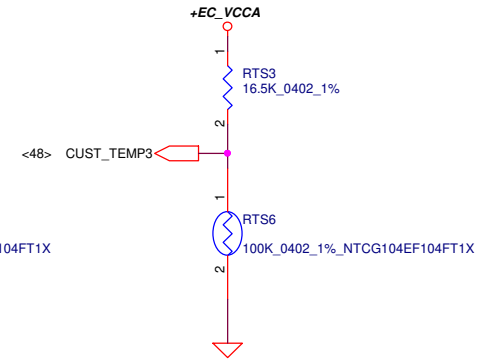
GPU Fan



CPU Fan



SSD



Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

Title: Thermal Sensor

Size: B | Document Number: LA-J561P | Rev: 1.0

Date: Wednesday, February 26, 2020 | Sheet 51 of 100

Bom Structure

Coffee Lake-H CPU SKU

UC1 CPU1@ — CML-H — CML-H ES 65W QTJ0 — SA0000D3G10

UC1 CPU2@ — CML-H — CML-H ES 45W QTJ1 — SA0000D3I10

UC1 CPU3@ — CML-H — CML-H ES 45W QTJ2 — SA0000D3N10

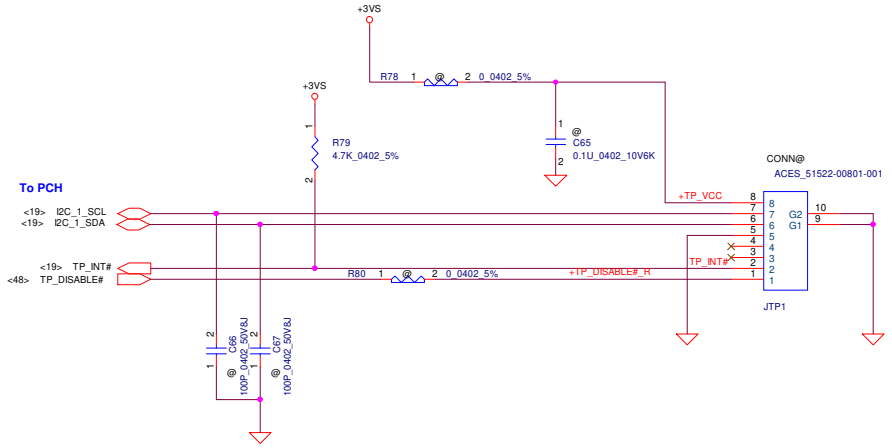
Cannn Lake PCH HM370

UH1 PCH1@ — Pre-QS — HM470 QUCJ — SA0000DDP20

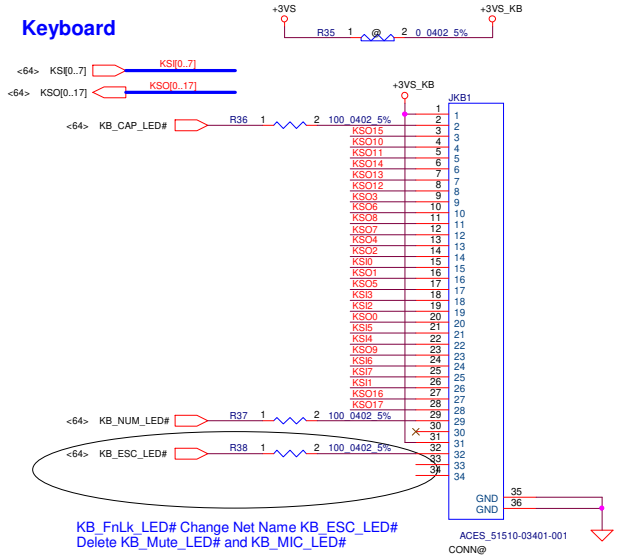
PCB

ZZZ2 PCB@ — PCB FLY00 LA-J561P LS-J561P — DAZ2VH00201

Touch Pad



Keyboard



KB_FnLk_LED# Change Net Name KB_ESC_LED#
Delete KB_Mute_LED# and KB_MIC_LED#

VRAM 6G

ZZZ M6G@ — MT61K256M32JE-14:A — X7685138L01

ZZZ S6G@ — K4Z80325BC-HC14 — X7685138L02

ZZZ MICR_6@ — VRAM — MT61K256M32JE-14:A — SA0000BND60

ZZZ SAM_6@ — VRAM — K4Z80325BC-HC14 — SA0000C6260

VRAM 8G

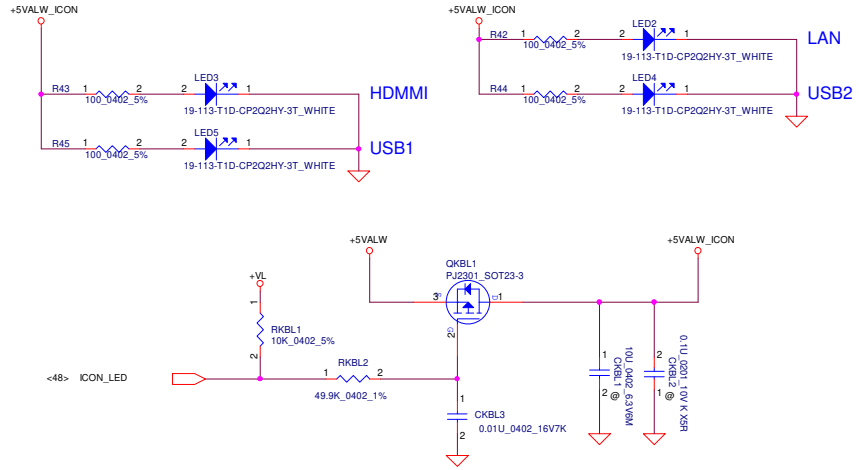
ZZZ M8G@ — MT61K256M32JE-14:A — X7685138L03

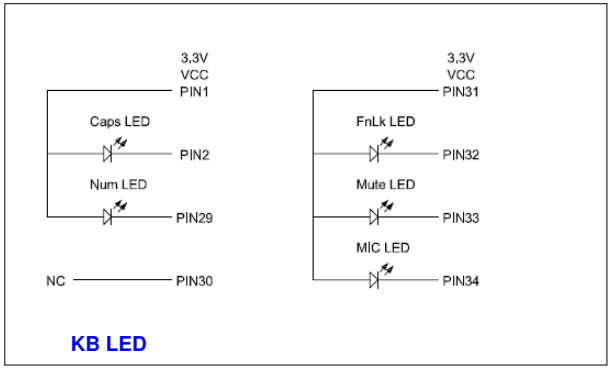
ZZZ S8G@ — K4Z80325BC-HC14 — X7685138L04

ZZZ MICR_8@ — VRAM — MT61K256M32JE-14:A — SA0000BND60

ZZZ SAM_8@ — VRAM — K4Z80325BC-HC14 — SA0000C6260

Icon LED





KB LED

X4E_15

ZZZ X4E_15@ — EMC EE AJ561 FLY00 — X4EAKK38L01

U3 GEN2 re-driver

ZZZ PERICOM@ — PI3EQX1004B1ZHEX — X7685138L07

ZZZ1 GENESYS@ — GL9950-OLY10 — X7685138L08

UUS1 U3RP@ — PI3EQX1004B1ZHEX — SA0000CEM00

UUS1 U3RG@ — GL9950-OLY10 — SA0000D5Q00

Nvidia GPU SKU

UV1 GPU1@ — 1660Ti-G0-R1 — N18E-G0-A1 — SA0000CK420

UV1 GPU2@ — 2060-G1-R1 — N18E-G1-B-KD-A1 — SA0000DDK10

UV1 GPU3@ — 2070-G2-R1 — N18E-G2-A1 — SA0000CCX30

UV1 GPU4@ — 2080-G3-R1 — N18E-G3-A1 — SA0000CD540

UV1 GPU5@ — 2060-G1R-R1 — N18E-G1R-MP-A1 — SA0000D4N50

UV1 GPU6@ — 2070-G2R-R1 — N18E-G2R-A1 — SA0000D4M30

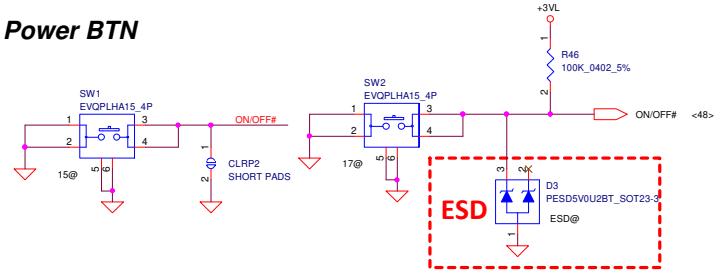
UV1 GPU7@ — 2080-G3R-R1 — N18E-G3R-A1 — SA0000D4L20

0911 update

Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.	
Title	KB/TP/LID/BOM S.
Size	Document Number: LA-J561P — Rev: 1.0
Date: Thursday, February 27, 2020	Sheet 52 of 100

Power BTN

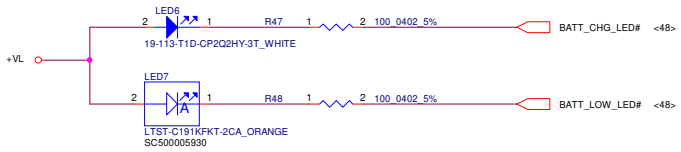


For 15"

For 17"

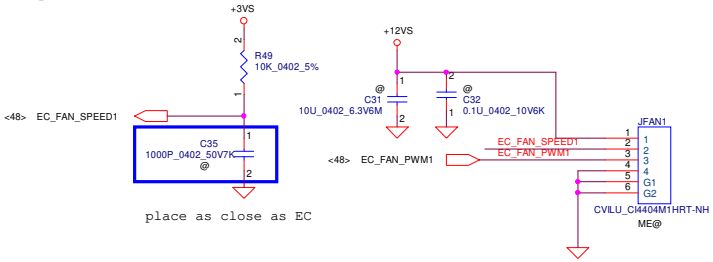
Change SCA00002900 to SCA00000T00

DCIN LED



CPU Fan Control Circuit

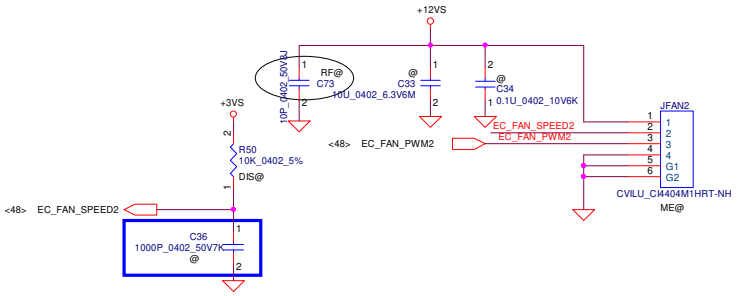
Right Side



place as close as EC

GPU Fan Control Circuit

Left Side



place as close as EC

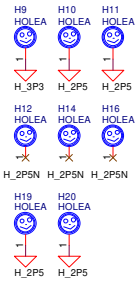
PCB

ZZZ

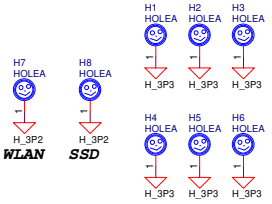
LA-J561P

DAB0005X000

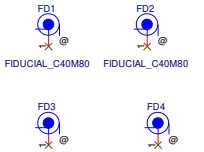
Screw Hole



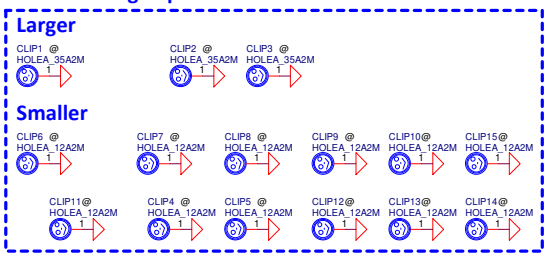
CPU/GPU Thermal Standoff



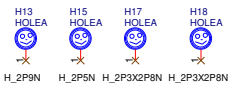
Fiducial Mark



DDR Shielding Clip



Position Hole



Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

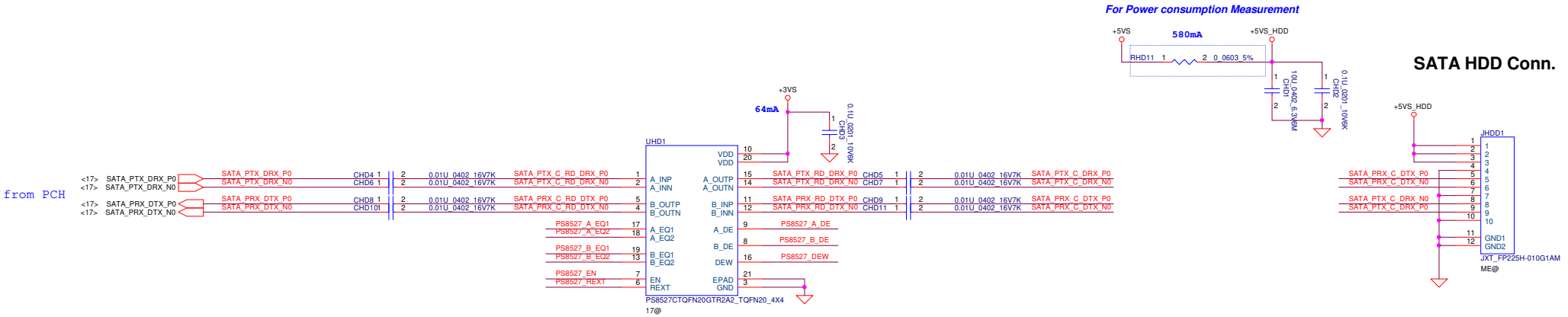
Compal Electronics, Inc.

Title: FAN/LED/PBTN/PCB PN/SCREWS

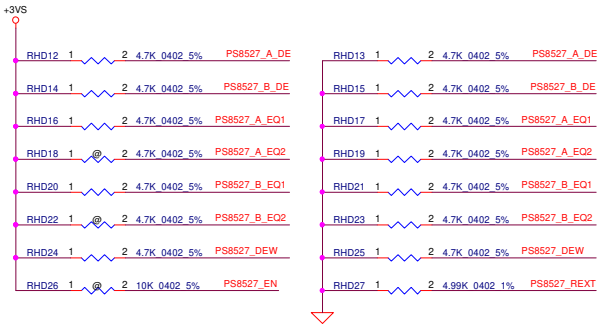
Size | Document Number: LA-J561P | Rev: 0.3

Date: Wednesday, February 26, 2020 | Sheet 53 of 100

SATA HDD



PN:SA00007JU10



Equalizer control and program for channel A.

Internally tied to VDD/2 (M status).

A_EQ2	A_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

Equalizer control and program for channel B.

Internally tied to VDD/2(M status).

B_EQ2	B_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

Programmable output de-emphasis level setting for channel A.

Internally tied to VDD/2(M status).

A_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

Programmable output de-emphasis level setting for channel B.

Internally tied to VDD/2(M status).

B_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

De-emphasis width setting for channel A& B .

Internally tied to VDD/2(M status).

DEW	DE pulse duration optimized for
M	SATA 6Gbp/s(default)
L	SATA 6Gbp/s
H	SATA 3Gbp/s

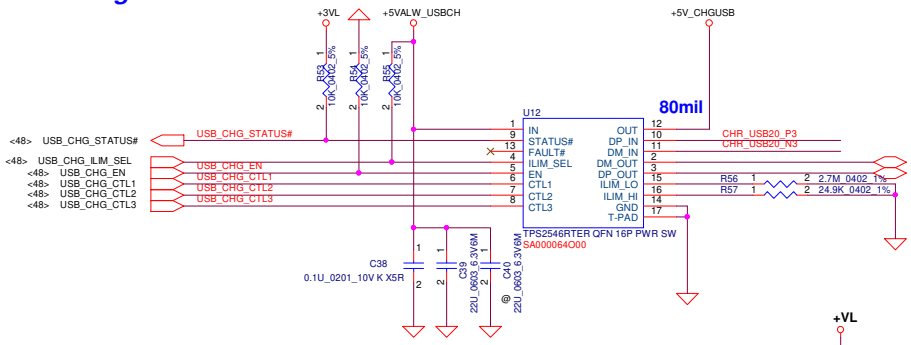
Compal Electronics, Inc.

Title: HDD Connector

Size: | Document Number: LA-J561P | Rev: 1.0

Date: Wednesday, February 26, 2020 | Sheet 54 of 100

USB Charger from YOGA730 15

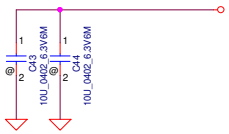


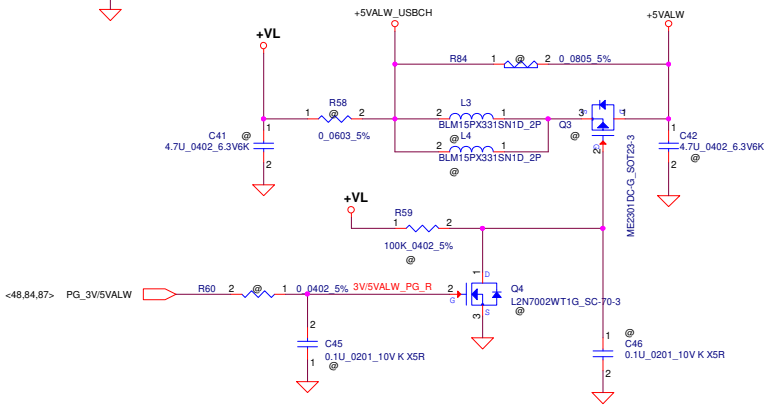
USB3.0 With USB2.0 For Charge

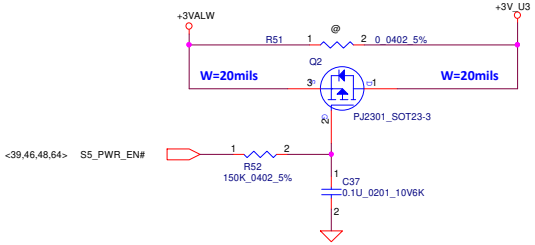
Right Spotlight LED

Right Speaker

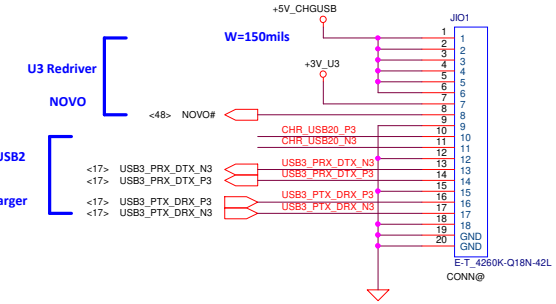
Down USB charger Iout ripple
must under 20mA on DC S5







IO CONN



Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

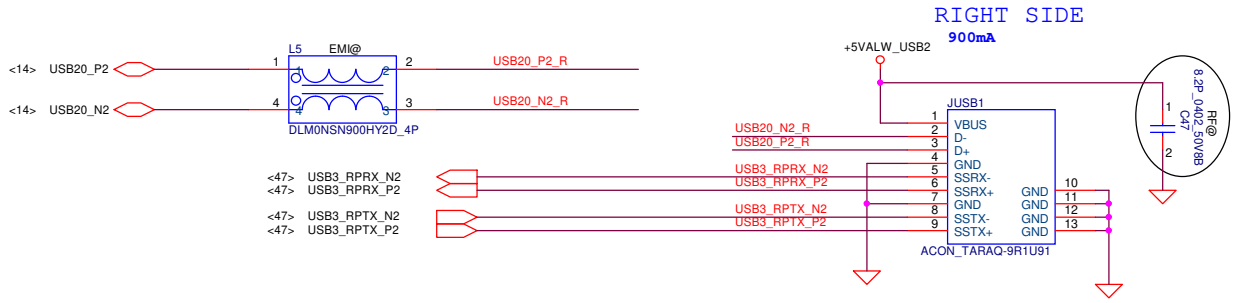
Compal Electronics, Inc.

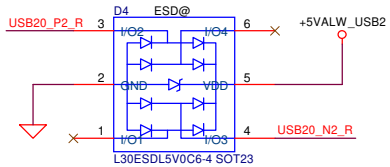
Title: USB3 Port 3 CONN.

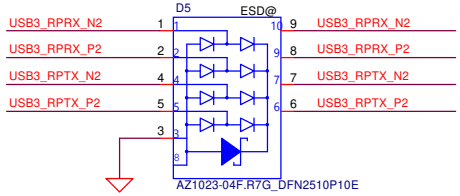
Size: | Document Number: LA-J561P | Rev: 1.0

Date: Wednesday, February 26, 2020 | Sheet 55 of 100

MB_USB3.1 Conn. (Port 1)

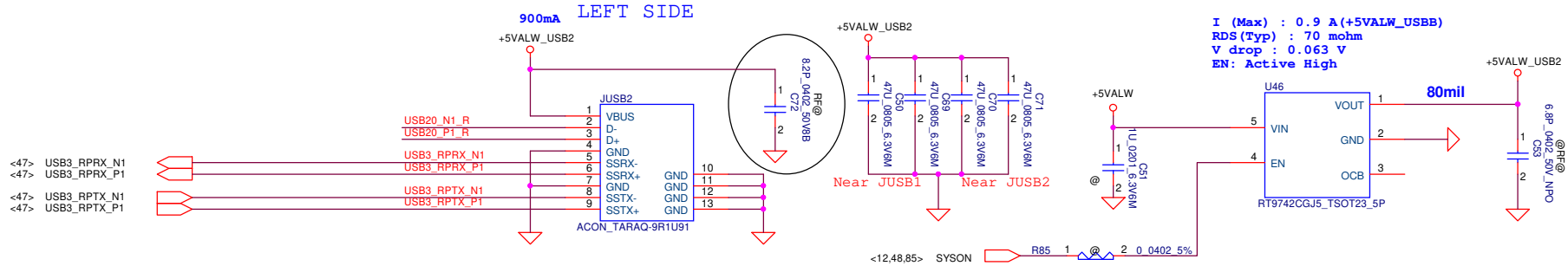


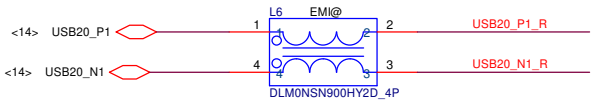


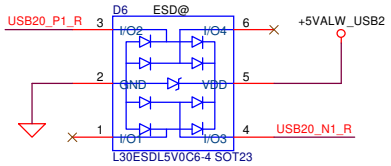


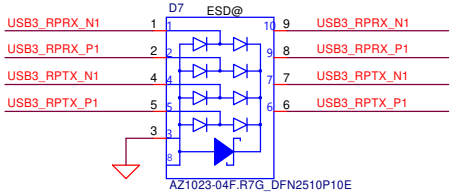
SC300004W00 change to SC300006000

MB_USB3.1 Conn. (Port 2)









SC300004W00 change to SC300006000

Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.			
Title: USB3 Port1/2 Conn.			
Size	Document Number: LA-J561P		Rev: 1.0
Date: Wednesday, February 26, 2020	Sheet 56 of 100		

Titan Ridge SP - High Speed (CIO, USB and PCIe) Parts

Polarity Reversal is allowed on CIO/USB/DP domains.
Need to be configured on NVM.

In case of unused high speed interface,
please leave pins open. No need for termination.

TR DP Configuration:
CIO x2 ports may be used
PCIe x4 lanes may be used
DPSNK x8 lanes may be used
USB 3.1 may be used (for debug only)
DPSRC may be used

From PCH PCIe TX

To SoC PCIe RX

From GPU DDI

Follow TR_DP_TI_PD_HOST_REF_DESIGN_R0V95
PE isn't POR -
Please don't use

PCIE RBIAS
Place as close as possible to pins

TBT Wake function select

TR NORTD3 Desidn	To PCH Wake pin
AR NORTD3 Design	To EC Wake pin
TR RTD3 Design	To PCH GPIO pin for INTEL SPEC

TBT_GPIO_8
'0' - Unsecure mode
'1' - Secure mode

DG_FORCE_PWR:
'0' - Regular Mode, Force Power is disabled (Default)
'1' - Force Power Mode is enabled

DG_USB_FORCE_PWR:
Might be use for seperatly force USB domain - connect to EC/PCH
'0' - by default

DG_FORCE_PWR:
Connect to EC/PCH for FW update
'0' - by default
'1' - for debug only

DG_CIO_PLUG_EVENT# should be conncted to PCH SCI GPIO

Place as close as possible to pins

USB2 Rbias Place as close as possible to pins

JTAG

SPI ROM

TBT RTD3

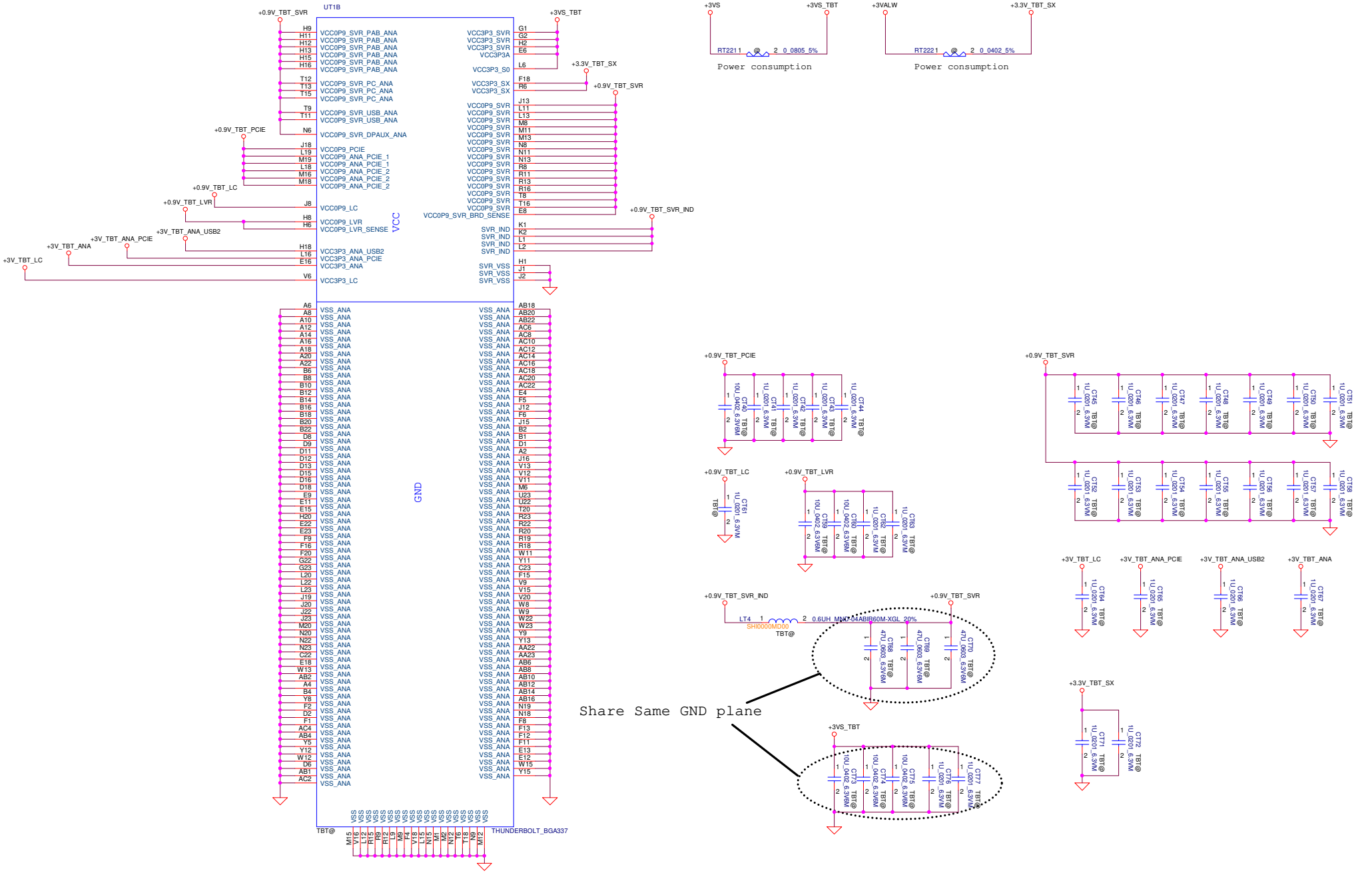
RTD3 Support:
In order to support RTD3, DG_PERST# and DG_PEWAKE# signals should reserve connections to dedicated PCH GPIOs per TBT Controllers.
In order to support RTD3, the following signals should be routed from PCH to TBT Controller:
DG_PERST#
DG_CLKREQ#
DG_PEWAKE#
DG_RTD3_PWR_EN

25M XTAL

Must use Metal shielded crystal for better noise immunity.
(Recommended: FL2500123Z by Pericom)

Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.			
Title: Thunderbolt Titanrid (1/2)			
Size: Custom	Document Number: LA-I561P		Rev: 1.0
Date: Wednesday, February 26, 2020	Sheet: 57	of: 100	



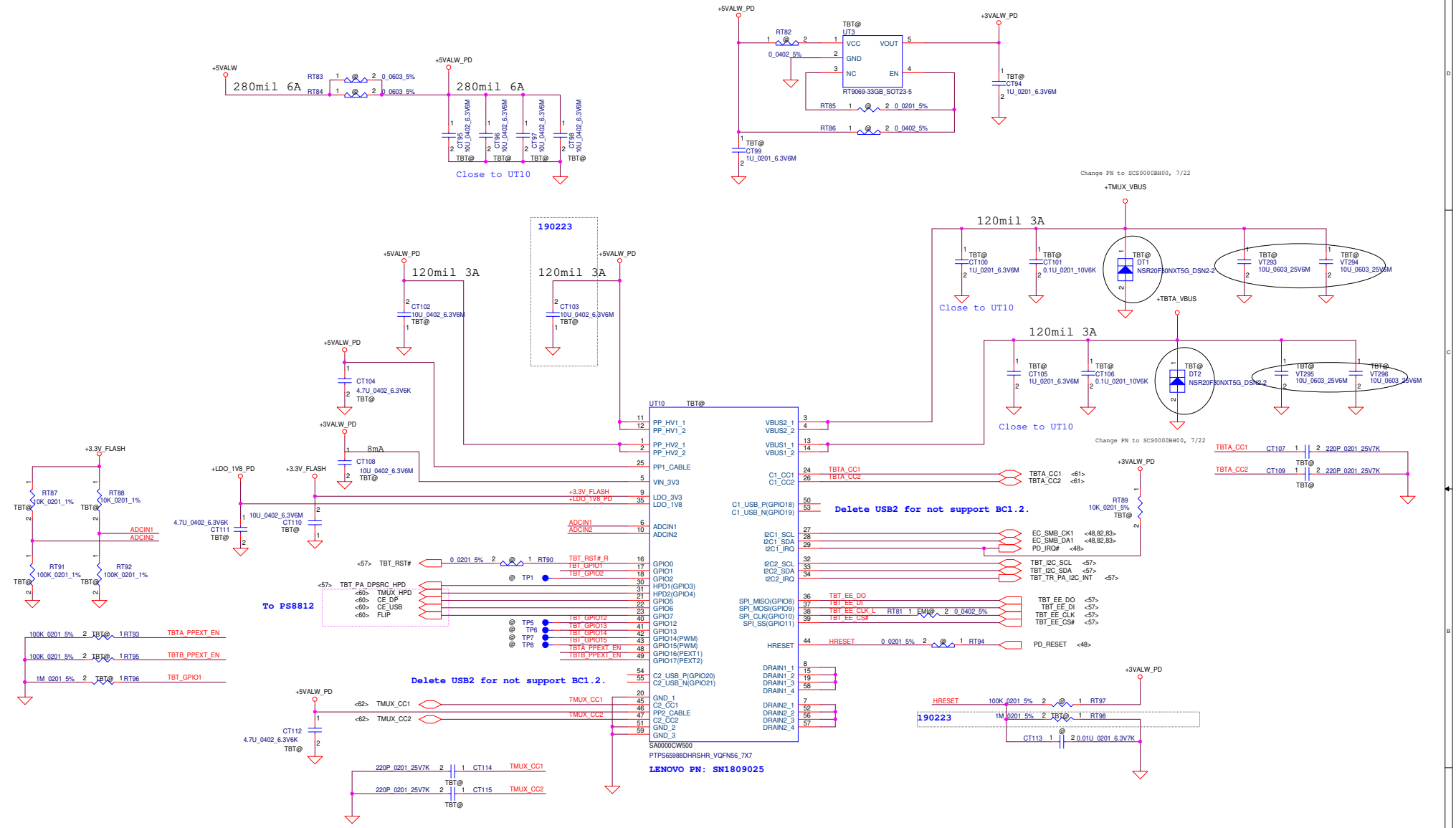
Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

Title: Thunderbolt Titanrid (2/2)

Size	Document Number	Rev
Custom	LA-J561P	1.0

Date: Wednesday, February 26, 2020 Sheet 58 of 100



Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: CC_TPS65988

Size | Document Number: LA-J561P | Rev: 0.1

Date: Wednesday, February 26, 2020 | Sheet 59 of 100

Near UBL1's 1.2VDD PIN

Near UBL1's PIN27,52

DCI Mode isn't used, so the 1.8V changes to 3.3V.

Near UBL1's PIN49

W=40mils

W=40mils

IMAX(per channel)=6A

TPS22965DSGR_SON8_2X2~D

20191007 modify

1st source : APL3526 (SA00006R100)
2nd source : TPS22965 (SA00005X50L)

SYMBOL MUX

PS8812 QFN52FTR-A3

From USB3

From SOC

For vendor suggest, Delete RX CAP.

For vendor suggest, connect to EC.

Use the GPIO4~7 for 65988DH

For vendor suggest, add 0 ohm.

Change to Pull High for vendor suggest

Strapping Pins

I2C Address

EQ Select

Add Pull High for vendor suggest

Add Pull Down for vendor suggest

TO PCH

TO GPU

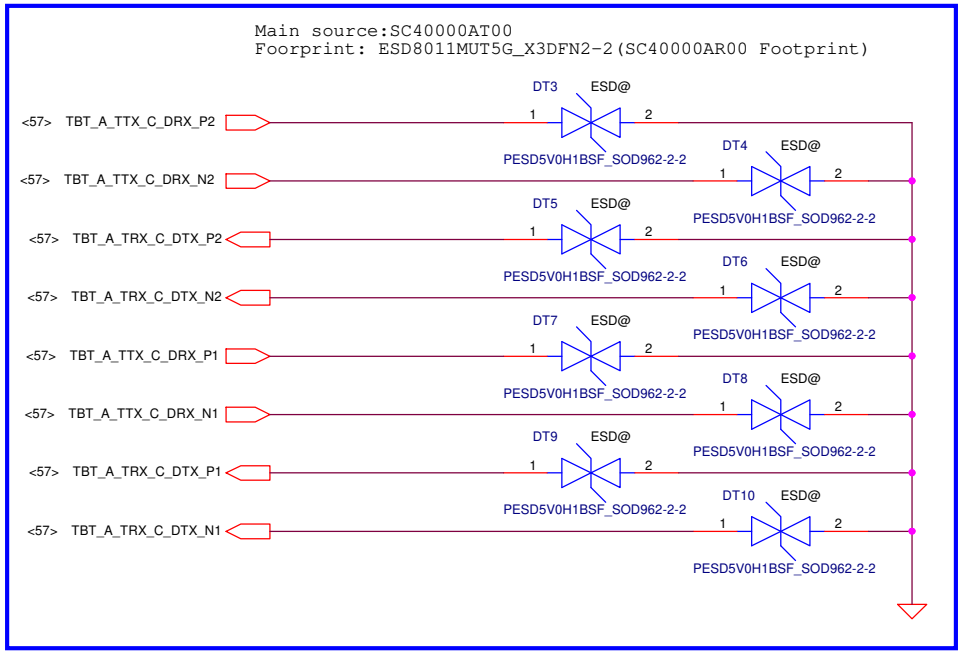
Security Classification	Compal Secret Data		
Issued Date	2017/08/02	Deciphered Date	2018/08/02

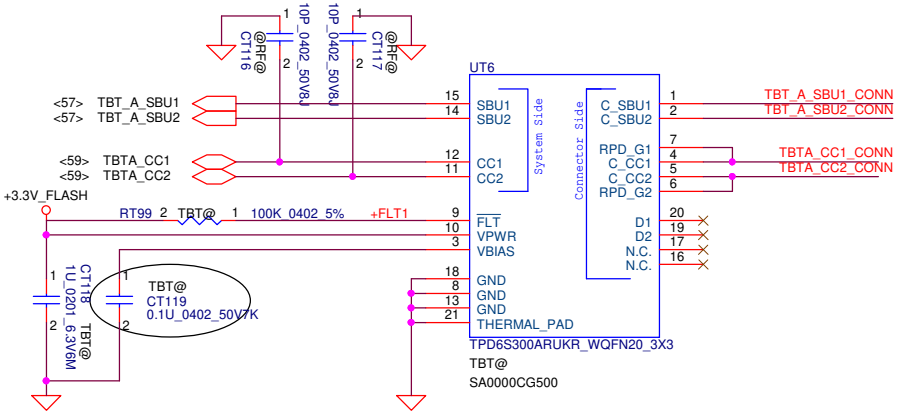
Compal Electronics, Inc.

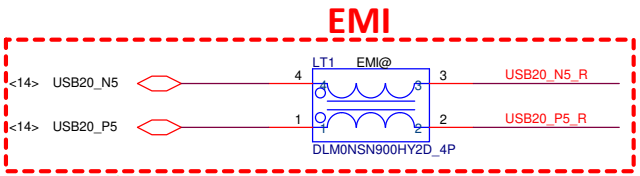
Title: Type-C PS8812

Size: Custom | Document Number: LA-H151P | Rev: 0.3

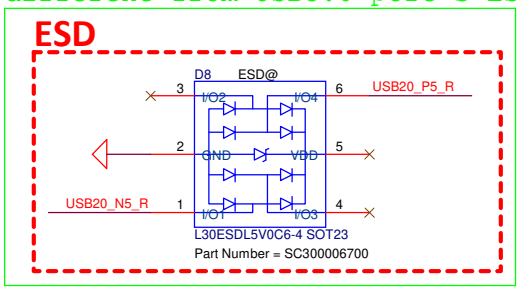
Date: Wednesday, February 26, 2020 | Sheet 60 of 100

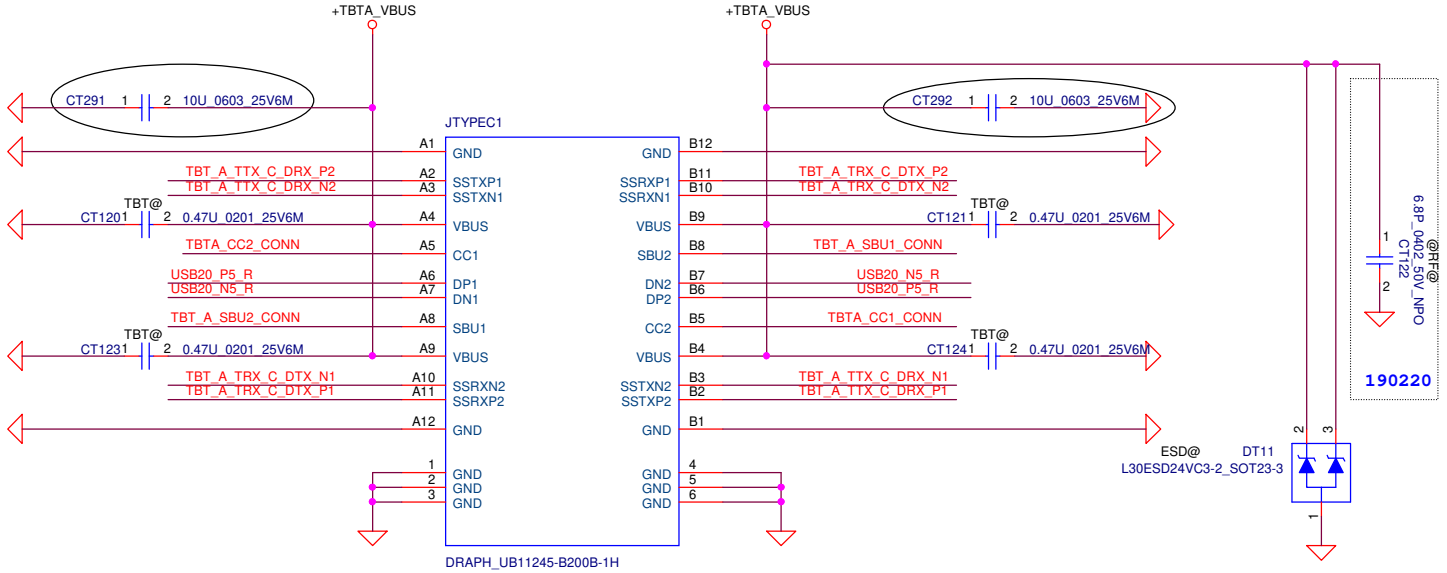


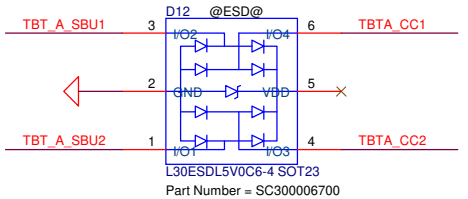




different from USB3.0 port's ESD







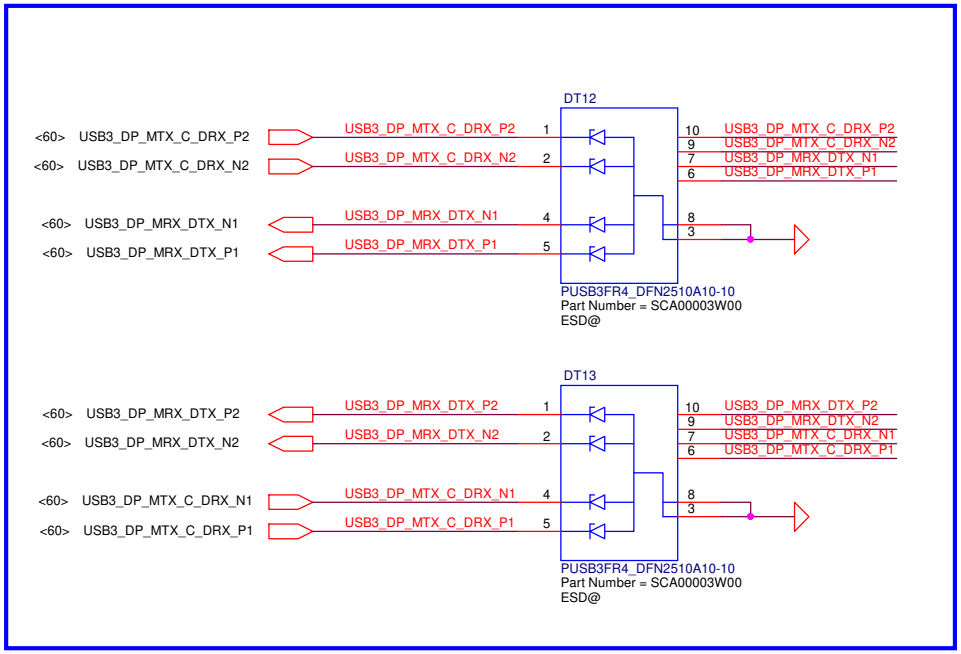
Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

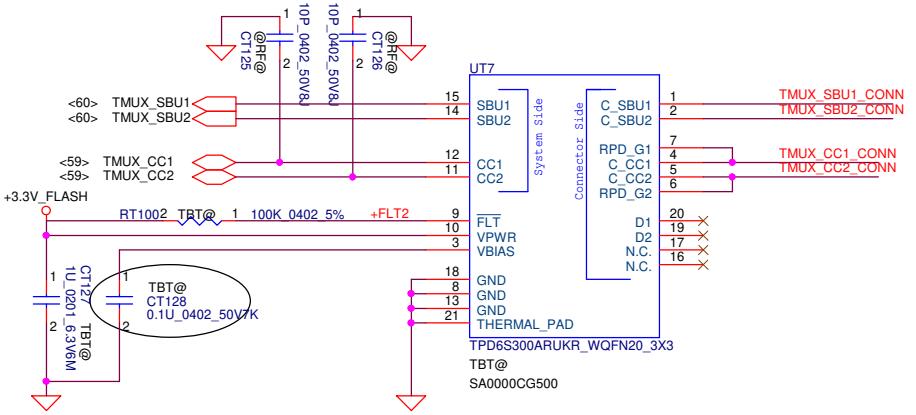
Compal Electronics, Inc.

Title: **USB3.1 TypeC Conn**

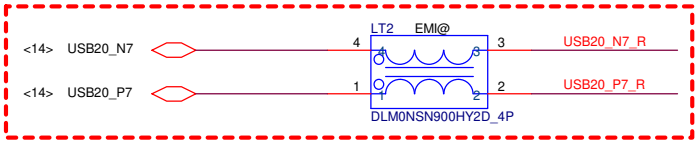
Size | Document Number: **LA-J561P** | Rev: 0.1

Date: Wednesday, February 26, 2020 | Sheet 61 of 100



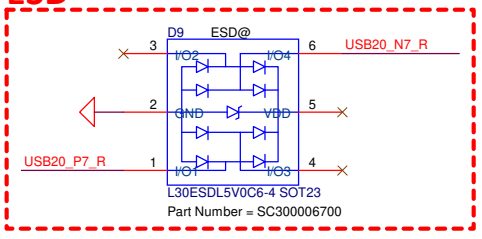


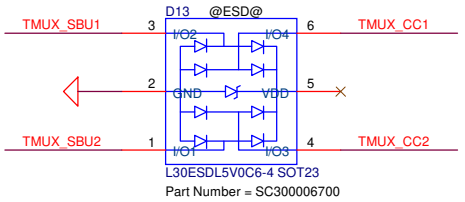
EMI

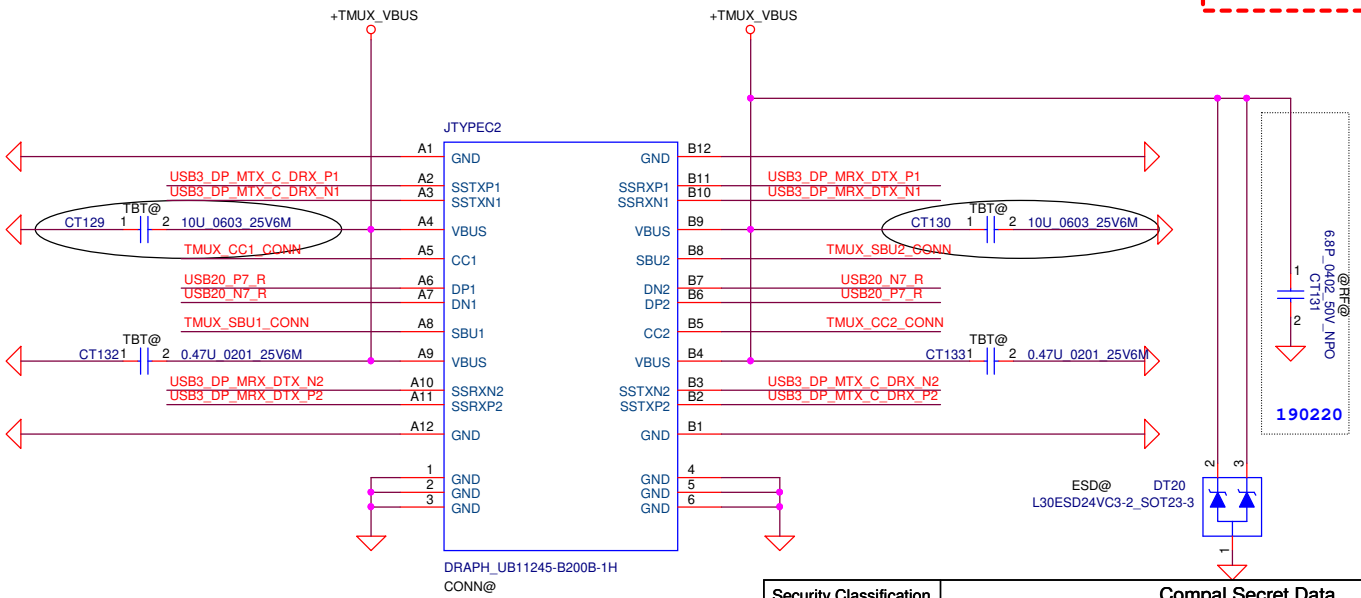


different from USB3.0 port's ESD

ESD







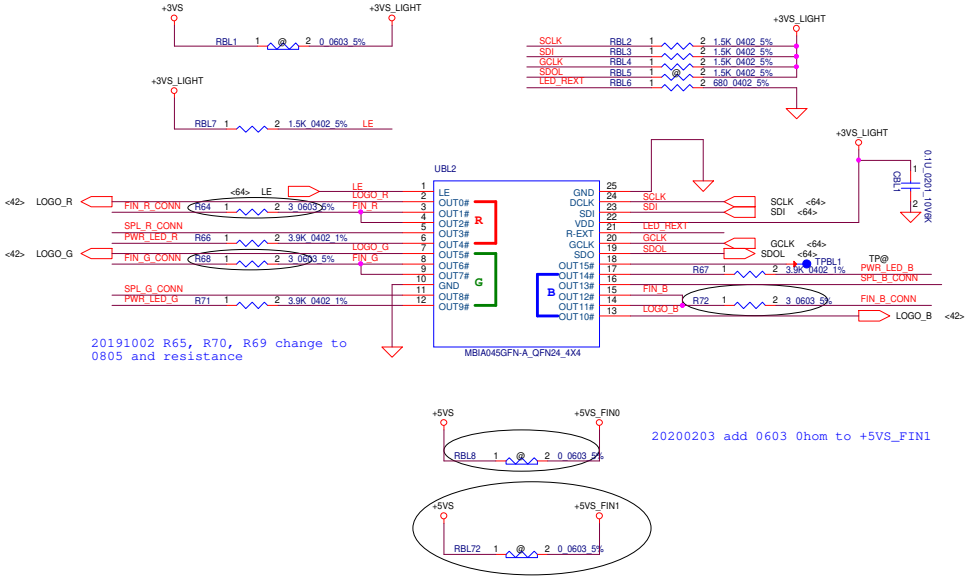
Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

Title: USB3.1 TypeC Conn

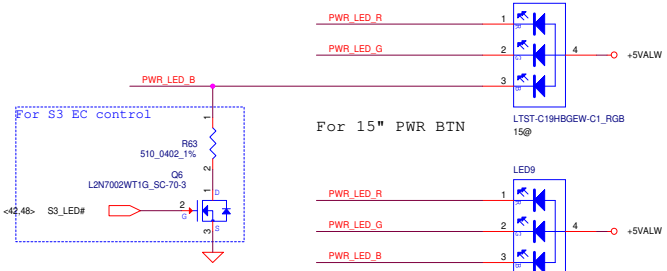
Size | Document Number: LA-J561P | Rev: 0.1

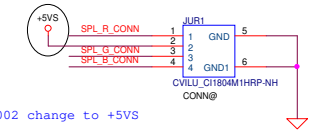
Date: Wednesday, February 26, 2020 | Sheet 62 of 100



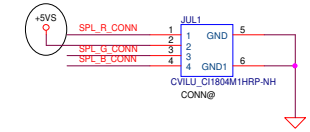
20191002 R65, R70, R69 change to 0805 and resistance

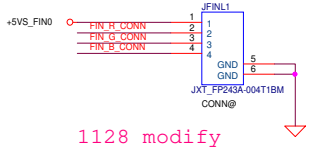
20200203 add 0603 0hm to +5VS_FIN1



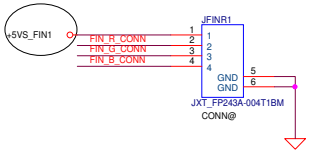


20191002 change to +5VS





1128 modify



Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

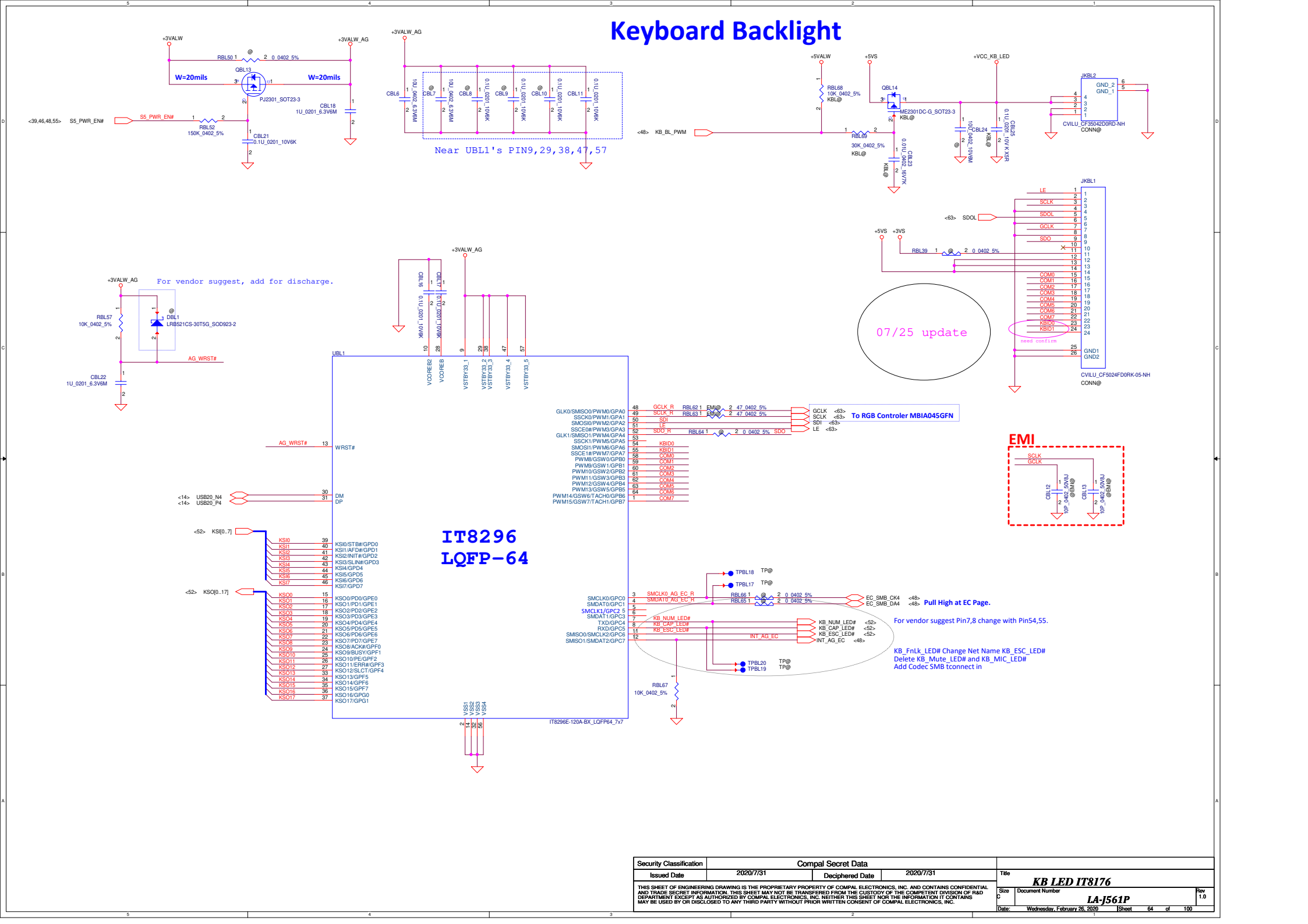
Compal Electronics, Inc.

Title: FIN LED

Size	Document Number	Rev
C	LA-J561P	1.0

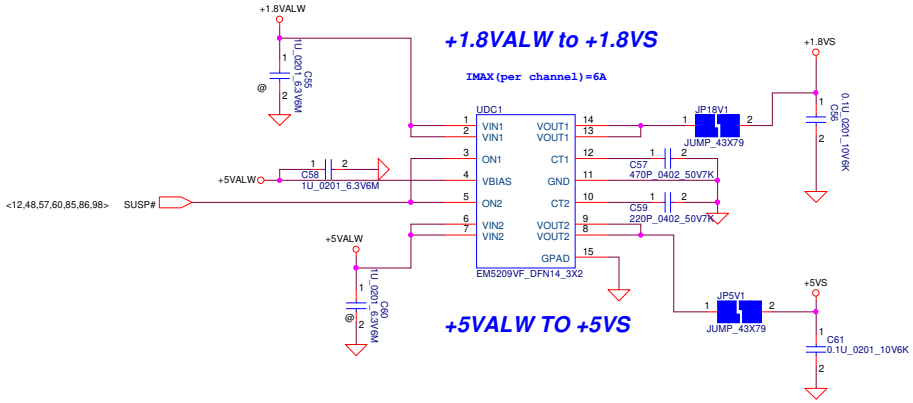
Date: Wednesday, February 26, 2020 Sheet 63 of 100

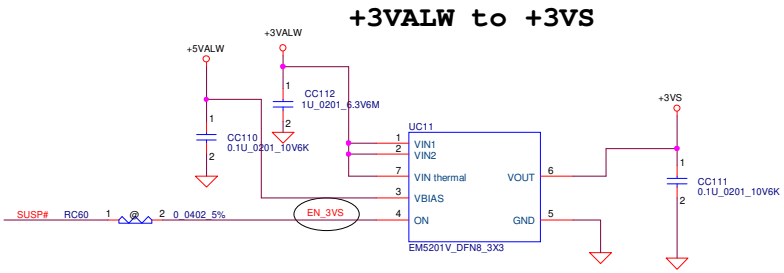
Keyboard Backlight



Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Title	KB LED IT8176		
Size C	Document Number LA-J561P		Rev 1.0
Date: Wednesday, February 26, 2020	Sheet 64 of 100		





Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

Title: DC INTERFACE

Size: | Document Number: LA-J561P | Rev: 1.0

Date: Wednesday, February 26, 2020 | Sheet 65 of 100

Note Color

Version change list (P.I.R. List)

FVT for HW

Item	Page	Modify List	Reason for change	Date
1	18	Add QH1 for ME_EN to HDA_SDOUT level shift	Add level shift for PCH and EC different power plan to solve audio device conldn't recognize	2019/09/06
2	57	Change RT15 and RT16 to 2.2K	Follow INTEL TBT SPEC	2019/09/06
3	41	UGV3 change part to SA00000OH00	Follow GPU DDS function design	2019/09/10
4	47	RUS2, RUS4, RUS6, RUS8, RUS12, RUS14, RUS16, RUS18 change to 68K ohm	Follow vendor recommend to modify DC flat gain and EQ	2019/09/11
5	52	Change JDBG1 CONN to TWVM_FPC0510-06RP-TAGHA	For NPI test only	2019/09/11
6	42	Change EDP_I2CB_SCL and EDP_I2CB_SDA pull-up power from +3VS to +1V8_MAIN for reserved	For DDS panel design update from GPU vendor	2019/09/12
7	58	LT4 (SHI0000MD00) change footprint to MAG_MND-04ABIR60M-XGL_2P	Follow DFB request for shift risk	2019/09/17
8	18	Add RH194 for reserved	For ME_EN reserved	2019/09/18
9	45	Change RA1.2 from +3VS to +1.8VS_DVDD_CODEC	Follow vendor recommend to change JHP1 PLUG_IN voltage divider +3VS to +1.8VS_DVDD_CODEC	2019/09/18
10	53	Add CLIP12, CLIP13, CLIP14	For ME and RF request	2019/09/19
11	55	Add R84	For side USB charger PWR reserved	2019/09/23
12	56	Add R85 and change U46 EN signals to SYSON	For upper USB port S3 resume	2019/09/23
13	60	UPS1 pin28 and pin29 swap	For PS8812 SMBUS signals modify	2019/09/23
14	47	Change RUS4 and RUS8 to 1K ohm	Follow vendor recommend to modify DC flat gain and EQ	2019/09/24
15	42	Change EDP_I2CB_SCL and EDP_I2CB_SDA to pull-up +1.8VS	Follow Nvidia vendor recommend to modify	2019/09/26
16	60	Change QPS1A to QPS2	Update location	2019/09/26
17	41,48	Change RV74 and R29 to pop	For DDS PWM function control from EC	2019/09/27
18	63	Add R86 and R87 to BOM control +3VS/+5VS	For Soucer ask to implement new UL module	2019/09/27
19	65	Change JUMP location name from JP3V1 to JP18V1	For naming update	2019/10/02
20	56	Add C72 0402 8.2P capacitor	For RF request	2019/10/02
21	63	Remove R86 and R87	For UL module use +5VS only	2019/10/02
22	63	RBL8 change 0402 to 0603 0 ohm	For LED power source requiremet	2019/10/02
23	63	R65, R70, R69 change to 0805 and resistance update	For vendor recommend to change it	2019/10/02
24	17	Add RH195 0402 0 ohm	For debug reserved	2019/10/04
25	60	Remove QPL1 and change to UPS2 related circuit	For UPS1 1.2V power switch modify	2019/10/04

Note Color

Version change list (P.I.R. List)

SIT for HW

Item	Page	Modify List	Reason for change	Date
1	60	Add RPS32 and change CPS25 to 10uF	For PS8812 debug to modify and reserved	2019/10/21
2	57	Add RT230 pull up to +3.3V_TBT_SX, RT13 change to un-pop, RT15 change to un-pop and RT16 change to TBT@	For TBT RTD3 debug and updated	2019/10/24
3	34	Add CG623 and CG624 for reserved	For GPU 1.8V dual load switch reserved	2019/11/5
4	20	Change RH136 from 0603 to 0805	For PCH +1.8V_PRIM power	2019/11/6
5	18	Change RH66 to Pull down	Follow INTEL CML-H PCH-H design specificaion	2019/11/7
6	18	Change ME_EN related circuit	Follow previous project design	2019/11/7
7	17	Add RH196 PU to +3VS	Add SATA_LED net pull up circuit	2019/11/7
8	50	Change TL1 to SP050006P00	For thermal interference to change transformer type	2019/11/14
9	16,19,49,52	Change PCH GPP_B3 connect to BT_ON & TP_INT connect to GPP_C15	Follow INTEL instruction to modify for BT native error recovery method issue	2019/11/14
10	48	Modify LID_SW# pull up to +5VALW	For MR sensor vendor recommend	2019/11/21
11	16	Change RH32 and RH33 to 100K pull up	Follow INTEL CML-H ESD REV1P0 to modify	2019/11/21
12	17,19	Add RH197 and RH198 for HDMI_HPD_PCH	For BIOS request to reserved that connect to GPP_K19	2019/11/21
13	19	Add RH199 and RH200 for DDS strap	For BIOS request to add the DDS strap	2019/11/21
14	50	TL1 signals swap	For Layout Routing	2019/11/25
15	19	Add RH201 and RH202 for GPU_ID2 strap	For BIOS request to add the GPU_ID2	2019/11/25
16	49	RW23 change to PD	For CNVi check list modify	2019/11/25
17	18	Add QH5, RH203 and RH204 level shift circuit	For SMBUS level shift to separate +3VALW and +3VS	2019/11/26
18	49	RS2 and RS4 change to 0805	For SSD1 and SSD2 power source optimization	2019/11/26
19	20	RH115 change to 0603 reserved	For PCH internal 1.8V modify	2019/11/26
20	16	Change RC41~RC49 from 33 hom to 56 ohm	For INTEL Design Guide update	2019/11/26
21	14-21	Change UH1 footprint to CML-H_BGA_874P-T	Follow COMPAL ORB schematics	2019/11/26
22	15,49	Change RH205, RH206, RW5, RW10 to 22ohm and RH30 to 20Kohm	Follow CNVi check list to update	2019/11/27
23	18	Remove QH5, RH203 and RH204 level shift circuit	Follow COMPAL ORB	2019/11/27
24	18	Change RH71 to 8.2K	Follow INTEL documents	2019/11/28
25	48	Change R24 to 33ohm	Follow INTEL documents	2019/11/28
26	63	Change JFINL1 and JFINR1 CONN to SP01002X400	Follow ME request to modify	2019/11/28
27	42,53	Add C73 and CV308	Follow RF request to add capacitors	2019/11/28
28	42	JEDP1 pin34 modify to +1.8VS	For solve +1.8VALW OVP issue and change DMIC power source	2019/12/3
29	61,62	Add CT291-CT294	For solve TYPEC issue	2019/12/4
30	48	Add R87	For EC Prochot pin issue	2019/12/4
31	50	Change RL14-RL17 from 0402 to 0603	For EMI request	2019/12/5
32	55	Change R65, R69, R70 to 0 ohm	For U lighting design modify	2019/12/5
33	59,61,62	Add C293-C296 and modiy C291, C292, C129, C130 to 0603	For solve TYPEC issue	2019/12/5
34	63	Change RH66, RH67 and RH71 to 3.9K	For customer request	2019/12/20
35	42	Change RH189 and RH190 to un-pop	For NV vendor recommend	2019/12/20

Compal Electronics, Inc.

Title: PIR-HW

Size: Custom | Document Number: LA-J561P | Rev: 1.0

Date: Wednesday, February 26, 2020 | Sheet 66 of 100

Note Color

Version change list (P.I.R. List)

MP for HW

Item	Page	Modify List	Reason for change	Date
1	63	Add RBL72 0603 0ohm	Add 0hom to improve FIN lighting issue	2020/02/03
2	63	Delete QBL1, QBL3, RBL10, RBL12 and RBL14	Remove components for FIN lighting PWR	2020/02/03
3	63	Change R64, R68, R72 from 22ohm to 3ohm 0603 resistors	Fine tune for FIN lighting	2020/02/04
4	63	Remove RBL5	Fine tune for FIN lighting	2020/02/05
5	63	Delete R65,R69 and R70 0ohm to short RGB signals directly	Fine tune for U lighting	2020/02/06
6	64	Change KBID0/KBID1 to UBL1 pin5.pin6	Not support Keyboard Audio Lighting Mode	2020/02/12
7	63,64	Add Q7,Q8,Q9 to control FIN Lighting directly from UBL1 pin53.pin54.pin55	Follow LD request to modify it	2020/02/12
8	63	UBL2 modify the SPL_R_CONN, SPL_G_CONN, SPL_B_CONN to UBL1 SPL_R, SPL_G, SPL_B controlled by 3 pins.	Increase U lighting signals strength	2020/02/12
9	63	Add R88,R89,R90 and net name SPL_R_CONN_R, SPL_G_CONN_R, SPL_B_CONN_R	Increase FIN lighting signals strength	2020/02/20
10	64	Delete RBL70,RBL71 and QBL2	Not support Keyboard Audio Lighting Mode	2020/02/25
11	64	Change KBID0/KBID1 to UBL1 pin54.pin55	For KB function change back	2020/02/25
12	63	Delete Q7,Q8,Q9,R88,R89,R90 and change R64, R68, R72 connect to UBL2	Fine tune for FIN lighting	2020/02/25

Compal Electronics, Inc.

Title: PIR-HW

Size: Custom | Document Number: LA-J561P | Rev: 1.0

Date: Wednesday, February 26, 2020 | Sheet 67 of 100

Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

Title: **miniDP**

Size	Document Number	Rev
	LA-J561P	1.0

Date: Wednesday, February 26, 2020 | Sheet 68 of 100

Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

Title: **miniDP**

Size	Document Number	Rev
	LA-J561P	1.0

Date: Wednesday, February 26, 2020 | Sheet 69 of 100

Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

Title: **miniDP**

Size	Document Number	Rev
	LA-J561P	1.0

Date: Wednesday, February 26, 2020 | Sheet 70 of 100

Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

Title: **miniDP**

Size	Document Number	Rev
	LA-J561P	1.0

Date: Wednesday, February 26, 2020 | Sheet 71 of 100

Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

Title: **miniDP**

Size	Document Number	Rev
	LA-J561P	1.0

Date: Wednesday, February 26, 2020 | Sheet 72 of 100

Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

Title: **miniDP**

Size	Document Number	Rev
	LA-J561P	1.0

Date: Wednesday, February 26, 2020 | Sheet 73 of 100

Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

Title: **miniDP**

Size	Document Number	Rev
	LA-J561P	1.0

Date: Wednesday, February 26, 2020 | Sheet 74 of 100

Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

Title: **miniDP**

Size	Document Number	Rev
	LA-J561P	1.0

Date: Wednesday, February 26, 2020 | Sheet 75 of 100

Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

Title: **miniDP**

Size	Document Number	Rev
	LA-J561P	1.0

Date: Wednesday, February 26, 2020 | Sheet 76 of 100

Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

Title: **miniDP**

Size	Document Number	Rev
	LA-J561P	1.0

Date: Wednesday, February 26, 2020 | Sheet 77 of 100

Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

Title: **miniDP**

Size	Document Number	Rev
	LA-J561P	1.0

Date: Wednesday, February 26, 2020 | Sheet 78 of 100

Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

Title: **miniDP**

Size	Document Number	Rev
	LA-J561P	1.0

Date: Wednesday, February 26, 2020 | Sheet 79 of 100

Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

Title: **miniDP**

Size	Document Number	Rev
	LA-J561P	1.0

Date: Wednesday, February 26, 2020 | Sheet 80 of 100

Y750 Power

Reserve

Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

Title

Size: Custom | Document Number: LA-J561P | Rev: 0.2

Date: Wednesday, February 26, 2020 | Sheet 81 of 100

Fuse rating=(Normal operating current)/(0.75*percent of rating by temperature)
BATT(95c):8A/(0.75*0.8)=13.3A

VMB2

JBAT201 @CONN@
OCTEK_WTB-12GCBWAB-U

PF201 15A_32V_0501015.WR
SP040006F00

VMB

EMI@ PL201 5A_Z80_0805_2P
EMI@ PL202 5A_Z80_0805_2P

+12.6V_BATT+

EC_SMCA
EC_SMDA

PR201 100_0402_1%
PR202 100_0402_1%

PC201 EMI@ 1000P_0402_50V7K
PC202 EMI@ 0.01U_0402_25V7K

EC_SMB_CK1 <48,59,83>
EC_SMB_DA1 <48,59,83>

PR203 200K_0402_1% +3VL

PR204 10K_0402_5% VCIN1_BATT_TEMP <48,83>

PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

+EC_VCCA

PR205 16.5K_0402_1%

<48> VCIN0_PH1

PH201 100K_0402_1%_B25/50 4250K

ECAGND

@CONN@ JDCIN1
DRAPH_PJSS0056-PB21H

PF202 15A_32V_0501015.WR
SP040006F00

APDIN APDIN1

EMI@ PL203 HCB2012KF-221T30_2P
EMI@ PL204 HCB2012KF-221T30_2P
EMI@ PL205 HCB2012KF-221T30_2P
EMI@ PL206 HCB2012KF-221T30_2P

+19V_VIN

PC209 0.01U_0402_50V7K EMI@
EMI@ PC203 1000P_0402_50V7K
EMI@ PC204 100P_0402_50V8J
EMI@ PC205 100P_0402_50V8J
EMI@ PC206 1000P_0402_50V7K
PC210 0.01U_0402_50V7K EMI@

@PR206 0_0402_5%

Fuse rating=(Normal operating current)/(0.75*percent of rating by temperature)

AC(75c):11.5/(0.75*0.85)=18.3A

65W ID:287 ohm->0.913V
90W ID:549 ohm->1.394V
135W ID:1k ohm->1.885V

+3VALW @ PR207 750_0402_1%
+3VL PR211 750_0402_1%

PC207 0.1U_0402_16V7K
PC208 680P_0402_50V7K

ADP_ID <48>
A/D

@ PR209 45.3K_0603_1%

+CHGRTC

PR208 0_0603_5% +3VL

+CHGRTC_R

PD201 S SCH DIO BAS40CW SOT-323
+RTCVCC

PR210 1K_0603_5%

CONN@ JRTC1
ACES_50271-0020N-001

RTC Battery

GC02001DR00
BATT CR2032 3V 210MAH MB 5 W/C 30MM

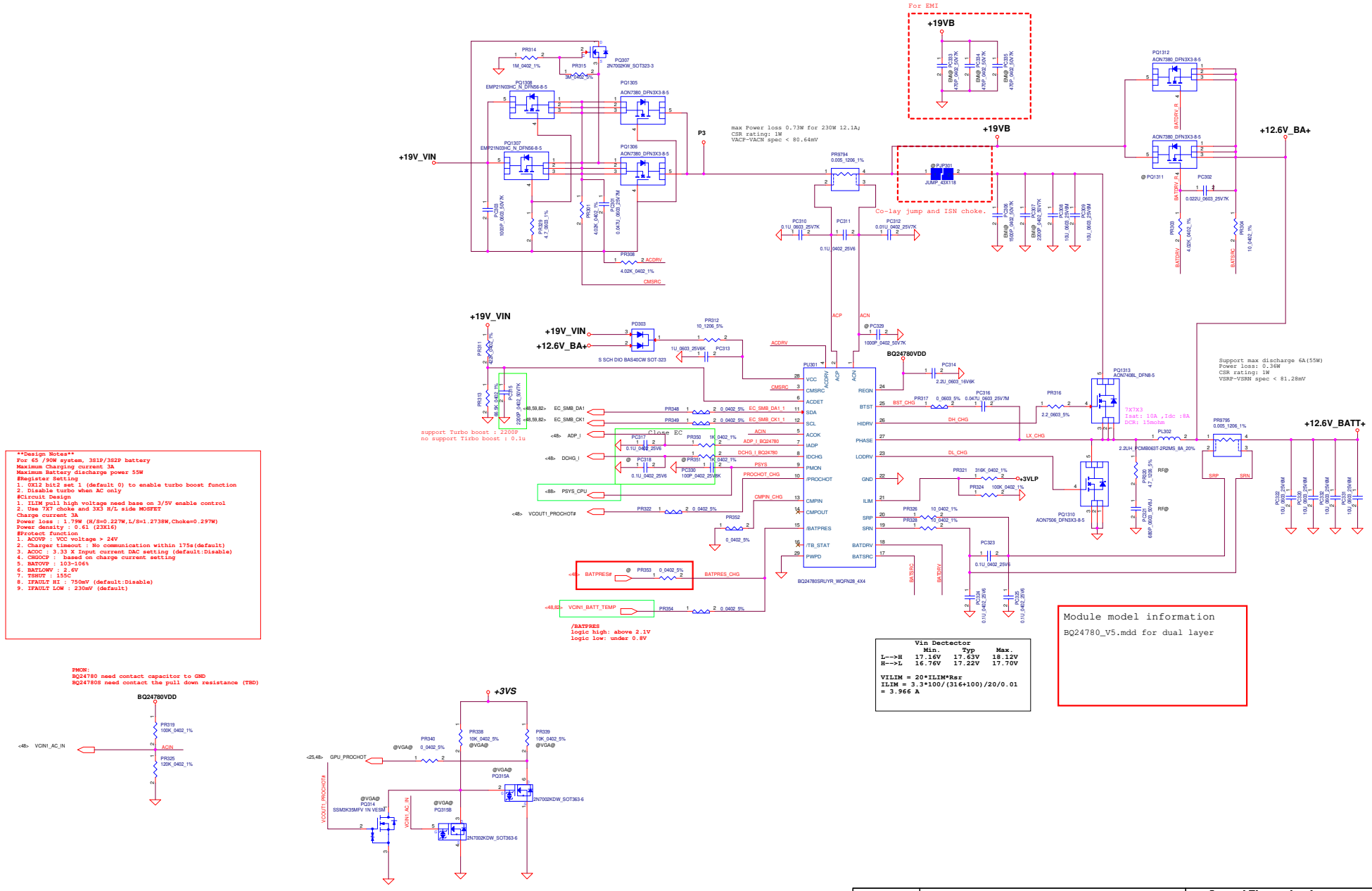
Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

Title: PWR- BATTERY CONN/OTP

Size: Custom | Document Number: Y750 | Rev: 0.2

Date: Wednesday, February 26, 2020 | Sheet 82 of 100



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/7/31	Deciphered Date 2020/7/31	Title BQ24780

Size Custom	Document Number		Rev 0.2
Date: Wednesday, February 26, 2020	Sheet 83 of 100		

Module model information

RT6575D_DMOS_single_V2.mdd
RT6575D_DMOS_dual_V2.mdd

(Common Part)
Choke 4.7uH SH00000YC00

Output capacitor ESR need follow below equation to make sure feed back loop stability
ESR=20mV*L*fsw/2V

RLIMIT = (ILIMIT x RDS(ON)) x 8 / 10µA

POK need pull high, it will pull high on VS transfer circuit

+3VLP
PC402 1U_0603_10V6K
@PC403 100P_0402_50V8J
@PC404 100P_0402_50V8J
PR401 13.7K_0402_1%
PR402 30.9K_0402_1%
VFB=2V
PR403 20K_0402_1%
PR404 20K_0402_1%
PR405 100K_0402_1%
PR406 44.2K_0402_1%
+19VB
EMI@ PL401 5A_Z80_0805_2P
EMI@ PL411 5A_Z80_0805_2P
+12.6VB_3/5V
@EMI@PC401 0.1U_0402_25V6
EMI@ PC406 2200P_0402_50V7K
PC407 10U_0603_25V6M
PC418 10U_0603_25V6M
PC405 10U_0603_25V6M
PC417 10U_0603_25V6M
+3VL
PR617 100K_0402_5%
PG_3V/5VALW <48,55,87>
PU401 RT6575DGQW(2)_WQFN20_3X3
CS2_3V FB_3V FB_5V CS1_5V
CS2 FB2 LDO3 FB1 CS1 GND
EN2 PGOOD PHASE2 BOOT2 UGATE2 LGATE2 VIN LDO5 BYP1 LGATE1 PHASE1 BOOT1 UGATE1 EN1 VCLK
EN_3V EN_5V UG_3V UG_5V LX_3V LX_5V LG_3V LG_5V
PL402 3.3UH_6.3A_20%_7X7X3_M
PC408 0.1U_0402_25V6
PR407 2.2_0603_5%
2BST_3V_R1 2BST_3V
PR408 2.2_0603_5%
PC409 0.1U_0402_25V6
BST_5V 2BST_5V_R1
PQ401 AONH36334_DFN3X3A8-10
PQ402 AONY36352_DFN5X6D-8-7
PL403 3.3UH_TMPA1004S-3R3MN-D__10A_20%
+3VALWP
+5VALWP
+5VLP
PR409 4.7_1206_5%
PC410 220U_6.3V_ESR18M_6.3X4.5
PC412 680P_0402_50V7K
PR410 RF@ 4.7_1206_5%
PC413 RF@ 680P_0402_50V7K
PC411 220U_6.3V_ESR18M_6.3X4.5
PC419 22U_0603_6.3V6M
PC420 @ 22U_0603_6.3V6M
PC421 RF@ 10P_0402_50V8J
PR411 2.2_1206_1%
VIN_3/5V
PC414 @ 1U_0603_25V6K
PC415 1U_0603_10V6K

3.3V
FSW=355kHz
COP: 11.95A
Vout2=2V*(1+13.7k/20k)=3.37V

OVP=Vout*(112.5%~117.5%)

OCP=Vtrip/Rdson+Iripple/2
Vtrip=Ics(min)*Rcs/8+1mV
Vcs=Ics*vcs should be in the range of 0.2~2V

Vout=VFB*(1+Rtop/Rbot)
VFB=2V

Vos=√SQU(Vomax)+L*SQU(I)/C)

5.09V
FSW=300kHz
COP: 23.95A
Vout1=2V*(1+30.9k/20k)=5.09V

EN
Rising=1.6~0.3V
Need inform HW to change NET NAME

<48> VCOUT0_MAIN_PWR_ON
<48> EC_ON
EN_5V3V
EN_5VALW <48>

PR412 0_0402_5%
@PR421 0_0402_5%
PR413 0_0402_5%
PR414 0_0402_5%
PR415 2.2K_0402_5%
PR420 0_0402_5%
@ PR422 100K_0402_5%
PR423 0_0402_5%
PR424 100K_0402_5%
@PR416 402K_0402_1%
PC416 4.7U_0603_25V6K

@PJ401 JUMP_43X118
@PJ405 JUMP_43X118
@PJ403 JUMP_43X118
@PJ402 JUMP_43X39
@PJ404 JUMP_43X39
@PR425 0_0402_5%

Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

Title: +3VALW/+5VALW

Size: Custom | Document Number | Rev: 0.2

Date: Wednesday, February 26, 2020 | Sheet 84 of 100

Module model information

RT8207P_single_V3.mdd For Single layer
RT8207P_dual_V3.mdd For Dual layer

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

Vout=0.75V(1+6.04k/10k) =1.203V
OCP=12.8A

Down size

Down size

Vout=0.8V* (1+Rup/Rdown)

Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

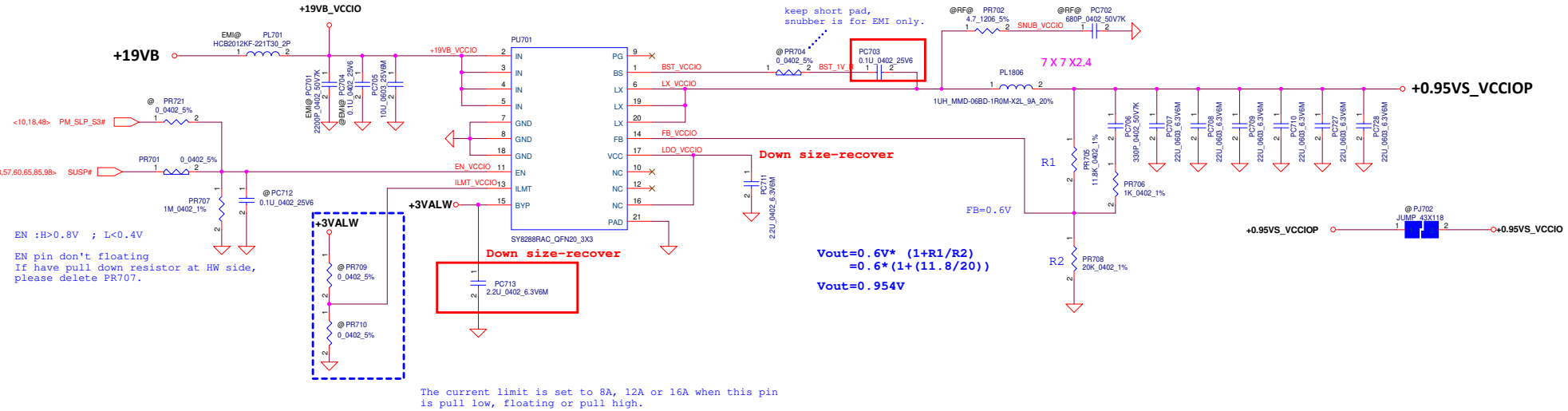
Title: RT8207P

Size: Custom | Document Number | Rev: 0.2

Date: Wednesday, February 26, 2020 | Sheet 85 of 100

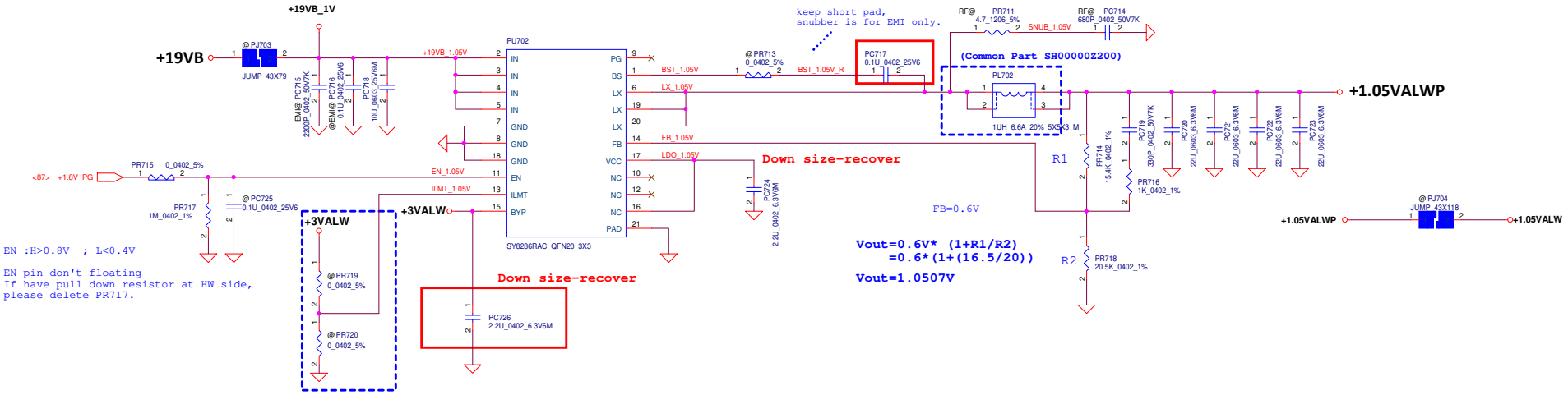
Module model information

SY8286_V2_single.mdd
SY8286_V2_dual.mdd



Module model information

SY8288_V2_single.mdd
SY8288_V2_dual.mdd



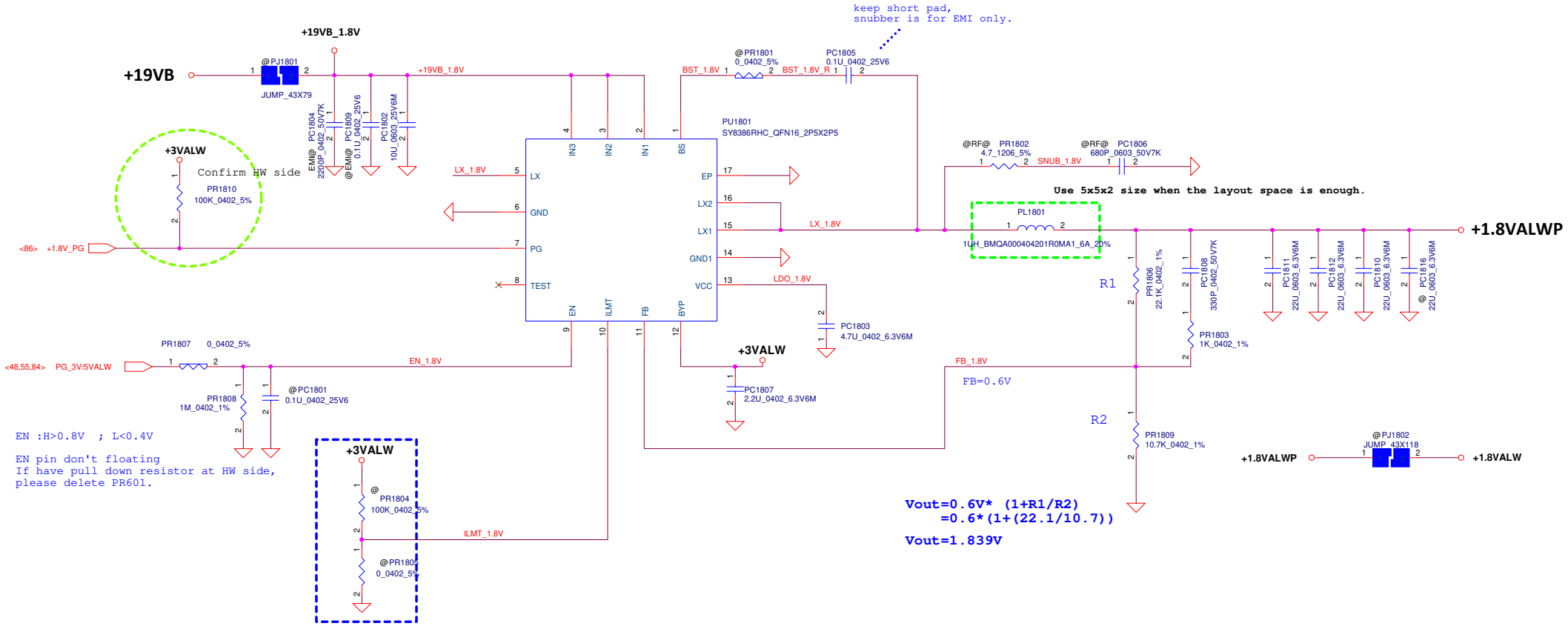
Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

Title: SY8286

Size	Document Number	Rev
C		0.2

Date: Wednesday, February 26, 2020 Sheet 86 of 100



Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

Title: APL5930

Size: Custom | Document Number | Rev: 0.2

Date: Wednesday, February 26, 2020 | Sheet 87 of 100

Module model information

NCP81205_H42_V6A.mdd for IC portion

NCP81205_H42_V6B.mdd for SW portion

SKL Halo	H42(45W)	
TDC@VCORE	56A	
IccMax@VCORE	68A	
OCP@VCORE	75A	
TDC@VGT	39A	
IccMax@VGT	54A	
OCP@VGT	61A	
TDC@VCCSA	10A	
IccMax@VCCSA	11A	
OCP@VCCSA	16.5A	
Fsw	600KHz	
DCR	0.9mohm +/-7%	

VCCSA:

H42: IccMAX@SA= 11A RIccMAX@SA= 34.8K ---> PR109

RIccMAX@SA= IccMAX*2V/10uA/64A

H42: IOUTSP@SA= 11A RIOUTSP@SA=19.6K ---> PR102

RIOUTSP= 2V/(gm*(Rth+RCSSP)*ICCMAX*DCR/(RPHSP+Rth+RCSSP))

H42: OCP@SA= 16.5A RLIMSP@SA=8.45K ---> PR101

RLIMSP= 1.3V/(gm*(Rth+RCSSP)*IoutLIMIT*DCR/(RPHSP+Rth+RCSSP))

Load line@SA= 9.1m

RDRPSP@SA=1.4K ---> PR95

RDRPSP= Load line*(RPHSP+Rth+RCSSP)/(gm * DCR) /(Rth+RCSSP)

CML-H82 (45W) baseline

IA: Max current=140A, loadline=1.1mohm,

GT: 0~1.52V, Max current=32A, loadline=2.7mohm

SA: 0~1.52V, Max current=11A, loadline=10.3mohm

OCP

IA: 168A

GT: 40A

SA: 16.5A

OVP

DAC+370mV

VCCCORE:

H42 OCP@Vcore= 75A RLIM@VCORE=13.7K ---> PR129

RLIM= IoutLIMIT * Load line/10

H42 IccMAX@Vcore= 68A RIccMAX2ph= 52.3K ---> PR154

RIccMAX2ph= (IccMAX2Ph*2V)/ (10uA*256A)

H42 Iout@Vcore= 68A RIOUT@Vcore=22.6K ---> PR120

RIOUT= 2* RLIM /(10 *IOUTICCMAX * Load line)

H42 Load line@VCORE= 1.8m RPH@Vcore=113K ---> PR135,PR137,PR140

Load line= (RCS2+(RCS1*Rth/(RCS1+Rth)))*IOUTTOTAL * DCR/RPH

VCCGT:

H42 OCP@GT= 61A RLIM@GT=16.2K ---> PR130

RLIM= IoutLIMIT * Load line/10

H42 IccMAX@GT= 54A RIccMAX2ph= 42.2K ---> PR150

RIccMAX2ph= (IccMAX2Ph*2V)/ (10uA*256A)

H42 Iout@GT= 54A RIOUT@GT=24.9K ---> PR126

RIOUT= 2* RLIM /(10 *IOUTICCMAX * Load line)

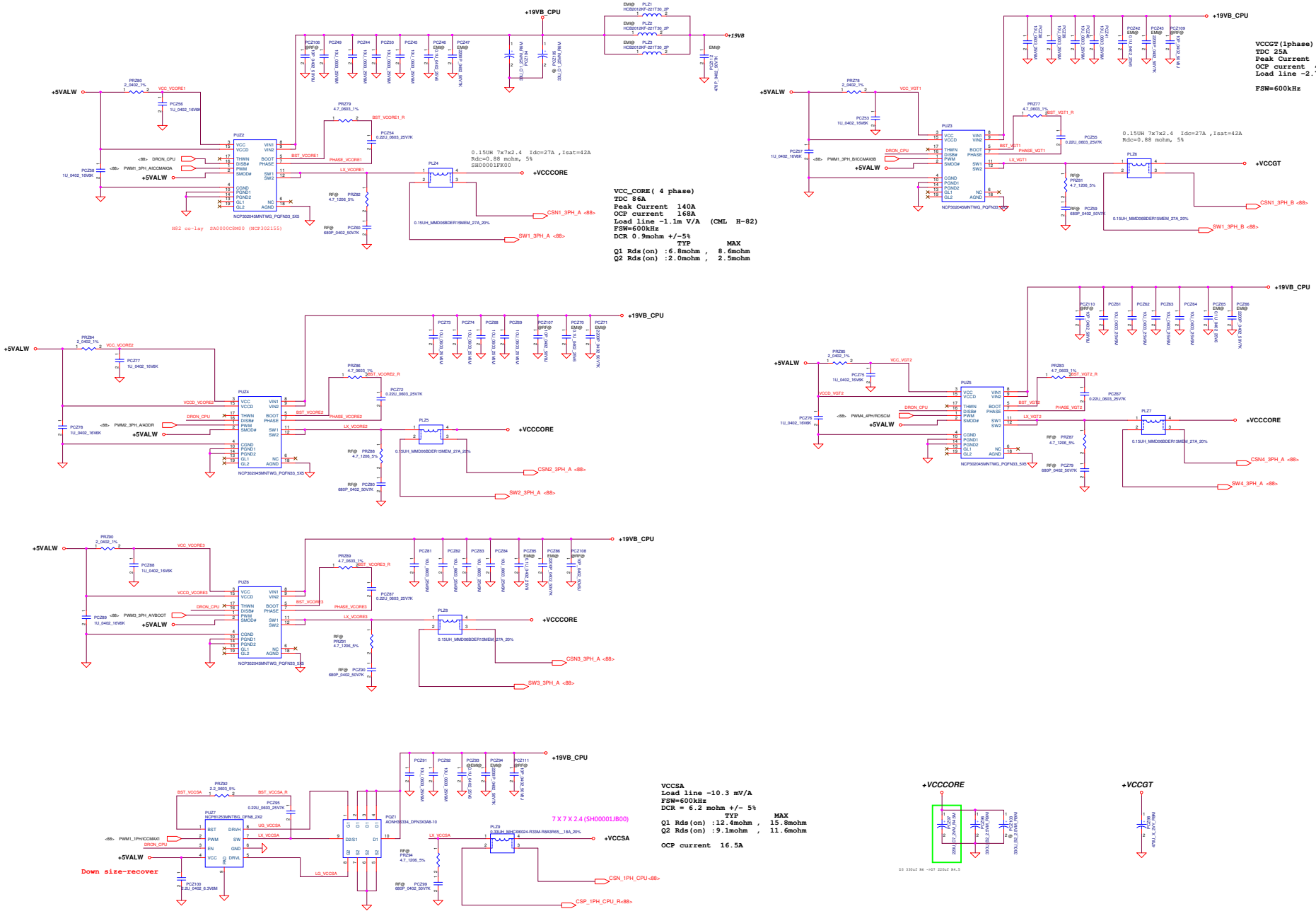
H42 Load line@GT= 2.65m RPH@GT=75K ---> PR139,PR141,PR144

Load line= (RCS2+(RCS1*Rth/(RCS1+Rth)))*IOUTTOTAL * DCR/RPH

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/7/31	Deciphered Date 2020/7/31	Title NCP81215 H62

Size: Document Number: Custom — Rev: 0.2

Date: Wednesday, February 26, 2020 — Sheet 88 of 100



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/7/31	Deciphered Date	2020/7/31
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Title: NCP81215_PowerStage
Size: Custom	Document Number:		Rev: 0.2
Date: Wednesday, February 26, 2020	Sheet 88 of 100		

VCC_CORE Place on CPU Back Side @ V09
22U_0603 *23 pcs+ 1U_0201*30 pcs

SIT(Y730, Y740)
22U_0603 *12 pcs+ 1U_0201*48 pcs

Y750
22U_0603 *19 pcs+ 1U_0201*48 pcs
10U_0402 * 42 pcs

+VCCCORE

VCC_GT Place on CPU Back Side @ V09
22U_0603 * 16 pcs +1U_0201* 20pcs

+VCCGT

VCC_SA Place on CPU Back Side @ V09
22U_0603 *7pcs +1U_0201* 3pcs

+VCCSA

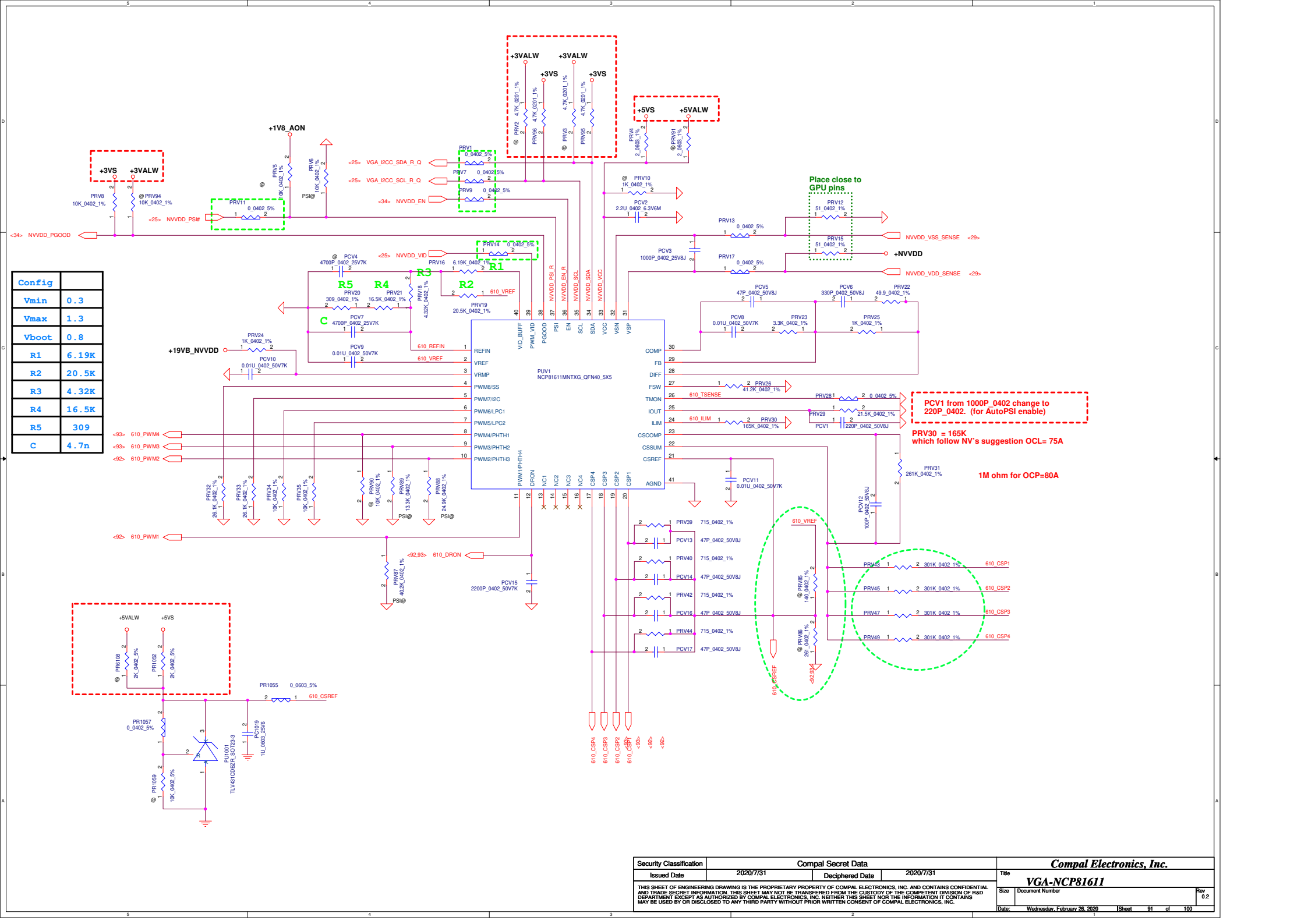
Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

Title: PWR-PROCESSOR_DECOUPLING

Size	Document Number	Rev
C		0.2

Date: Wednesday, February 26, 2020 Sheet 90 of 100



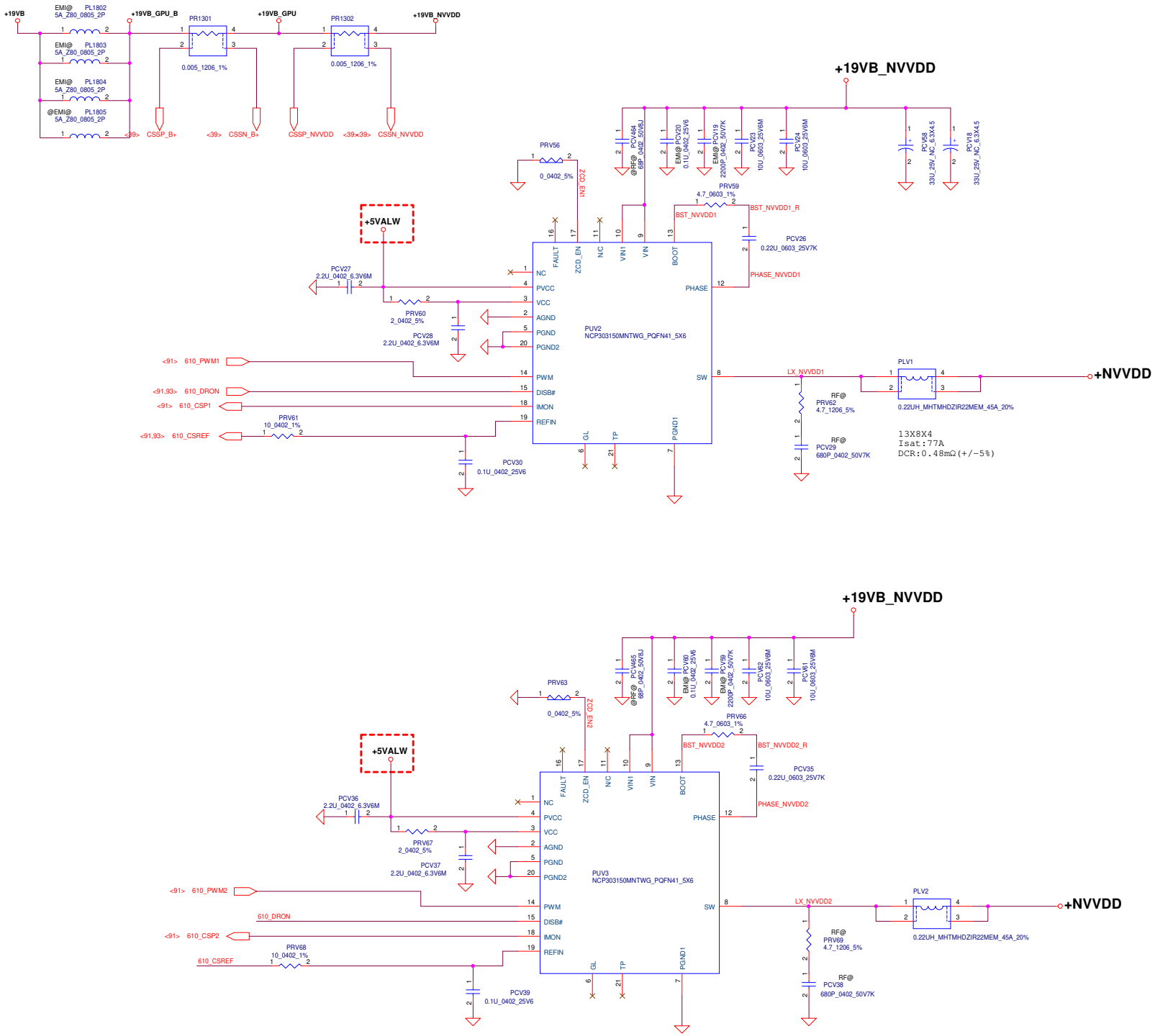
Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

Title: VGA-NCP81611

Size	Document Number	Rev
		0.2

Date: Wednesday, February 26, 2020 | Sheet 91 of 100



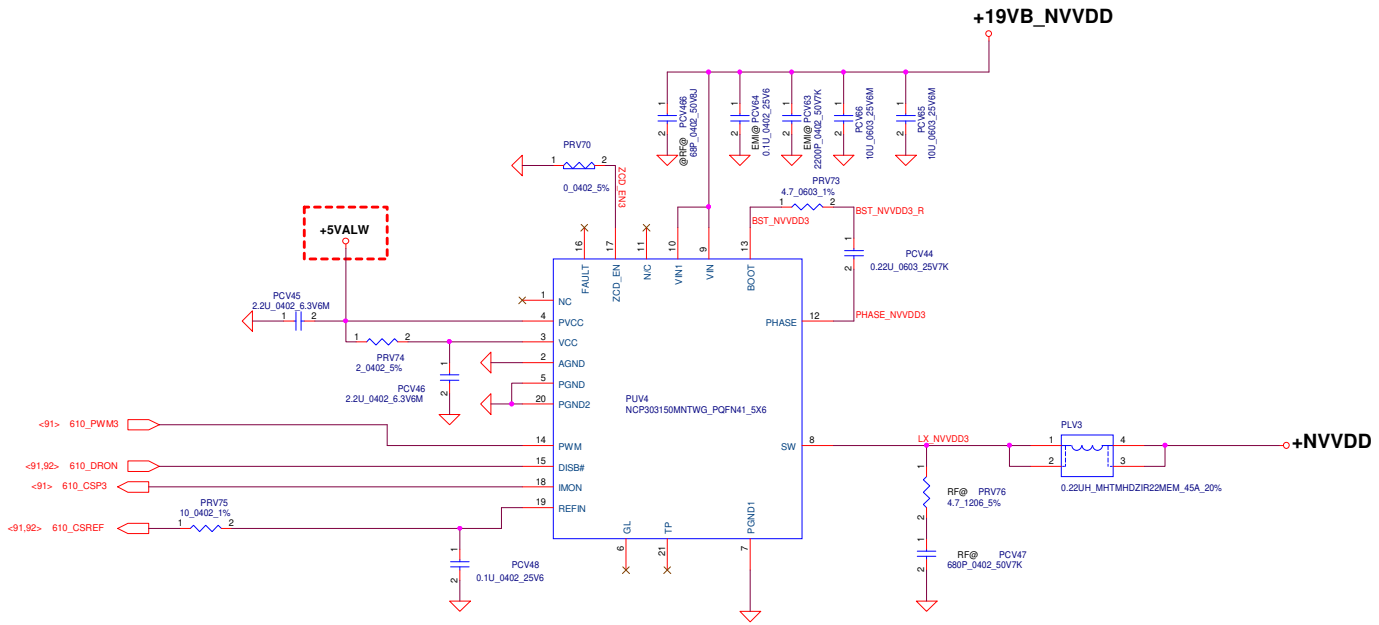
Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

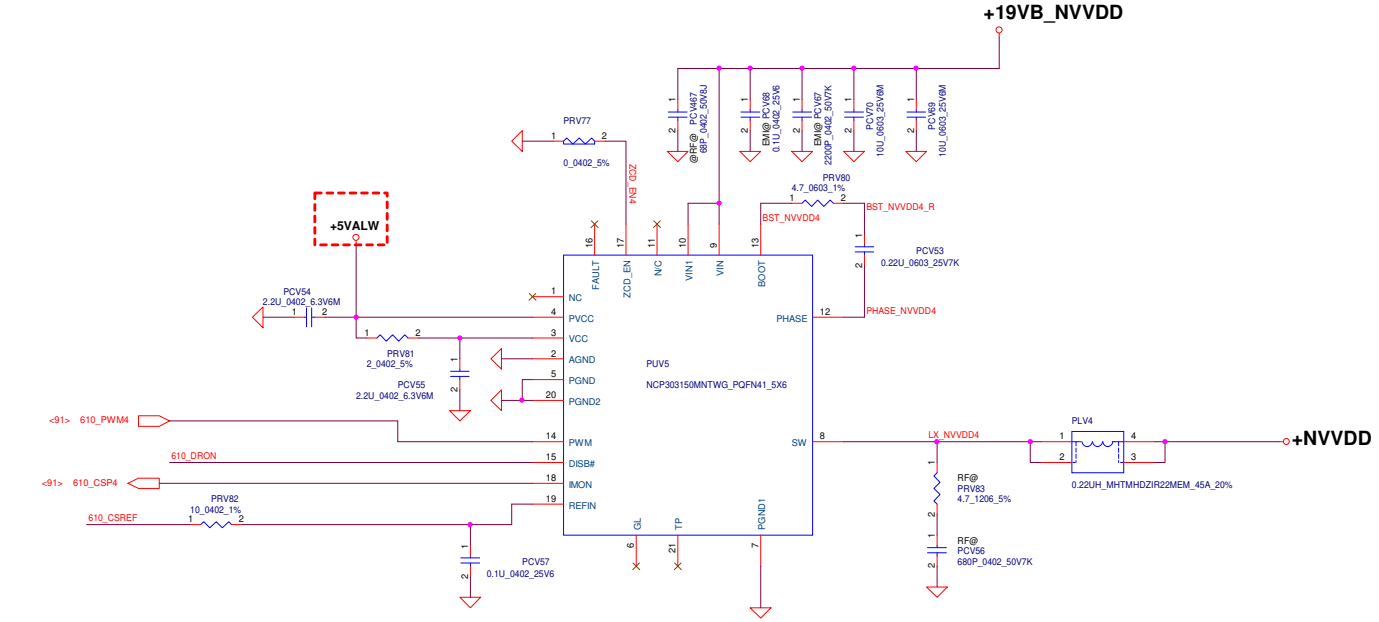
Compal Electronics, Inc.

Title: **PWR-NVVDD1**

Size	Document Number	Rev
		0.2

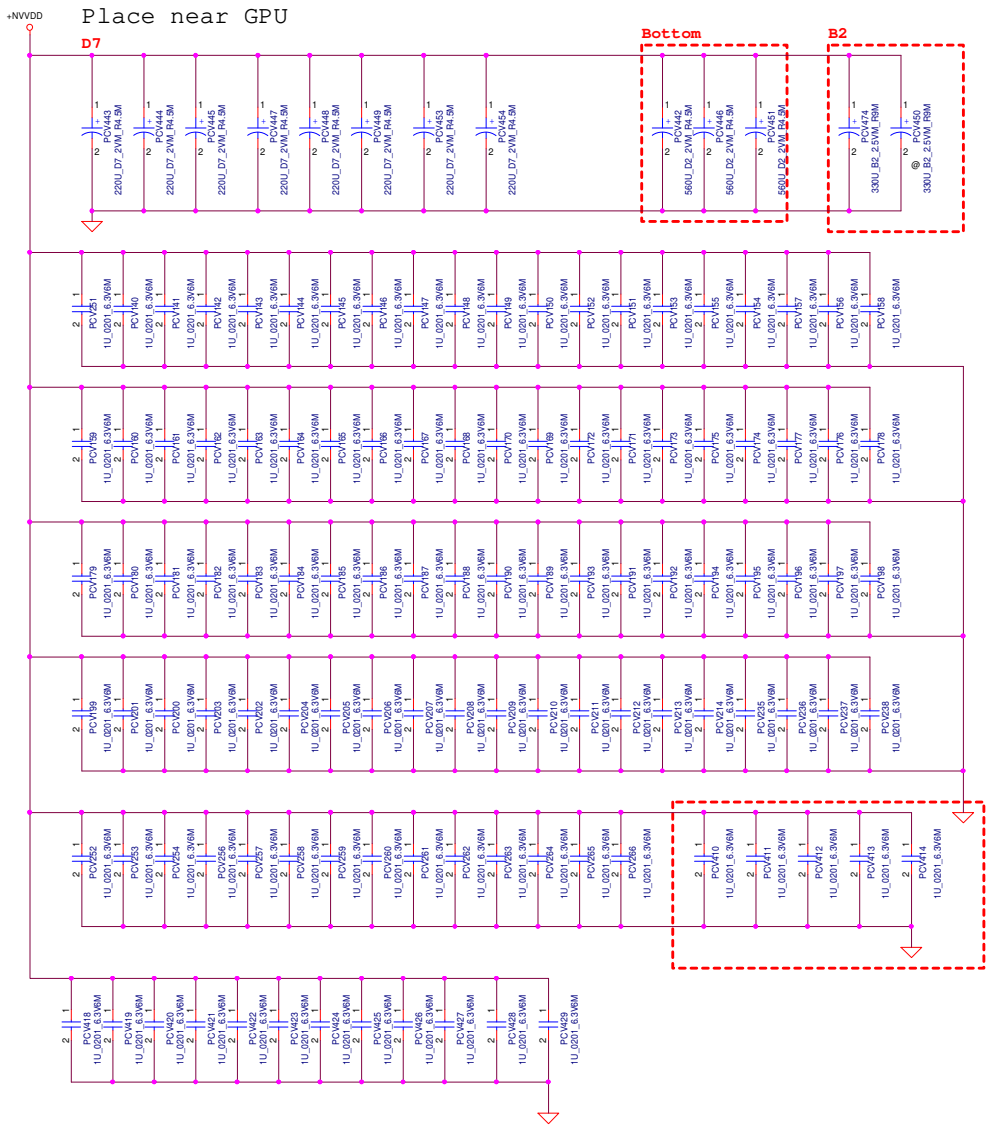
Date: Wednesday, February 26, 2020 | Sheet 92 of 100

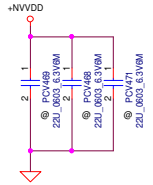




Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.			
Title	PWR-NVVDD2		
Size	Document Number		Rev 0.2
Date: Wednesday, February 26, 2020	Sheet 93 of 100		



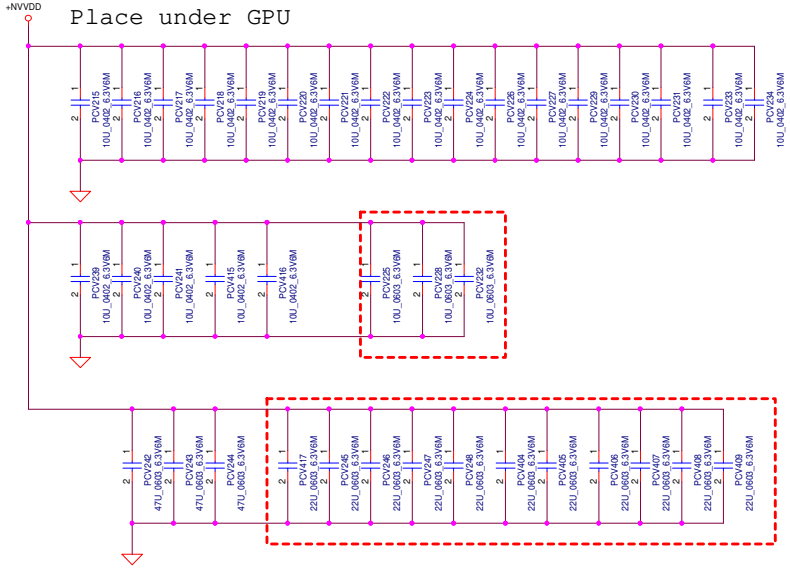


N18E-G3
+NVVDD
220uF X 8
560uF X 3
330uF X 1
47uF_0603 X 3
22uF_0603 X 11
10uF_0402X 22
1uF_0201 X 111
10uF_0603 X 3

N18E-G2
+NVVDD
470uF X 2
330uF X 6
47uF_0603 X 3
22uF_0603 X 4 +7
10uF_0402X 22
1uF_0201 X 94 +17
10uF_0603 X 3

Reserve

N17E-G3
+NVVDD
470uF X 11
47uF_0805 X 3
10uF_0603X 27
4.7uF_0603 X 11
1uF_0402 X 65



Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
GB4B-256 Package				
NVVDD		Varies	185 X 0.47uF (0201W X6S) 23 X 10uF (0603 X6S) 4 X 22uF (0805 X6S) 3 X 47uF (0805 X6S)	2 X 470uF (Poscap)
FBVDDQ (GPU side)[1]		1.25V 1.35V 1.5V 1.55V	48 X 0.47uF (0201 X6S) 5 X 10uF (0603 X6S)	7 X 10uF (0603 X6S) 9 X 22uF (0603 X6S)

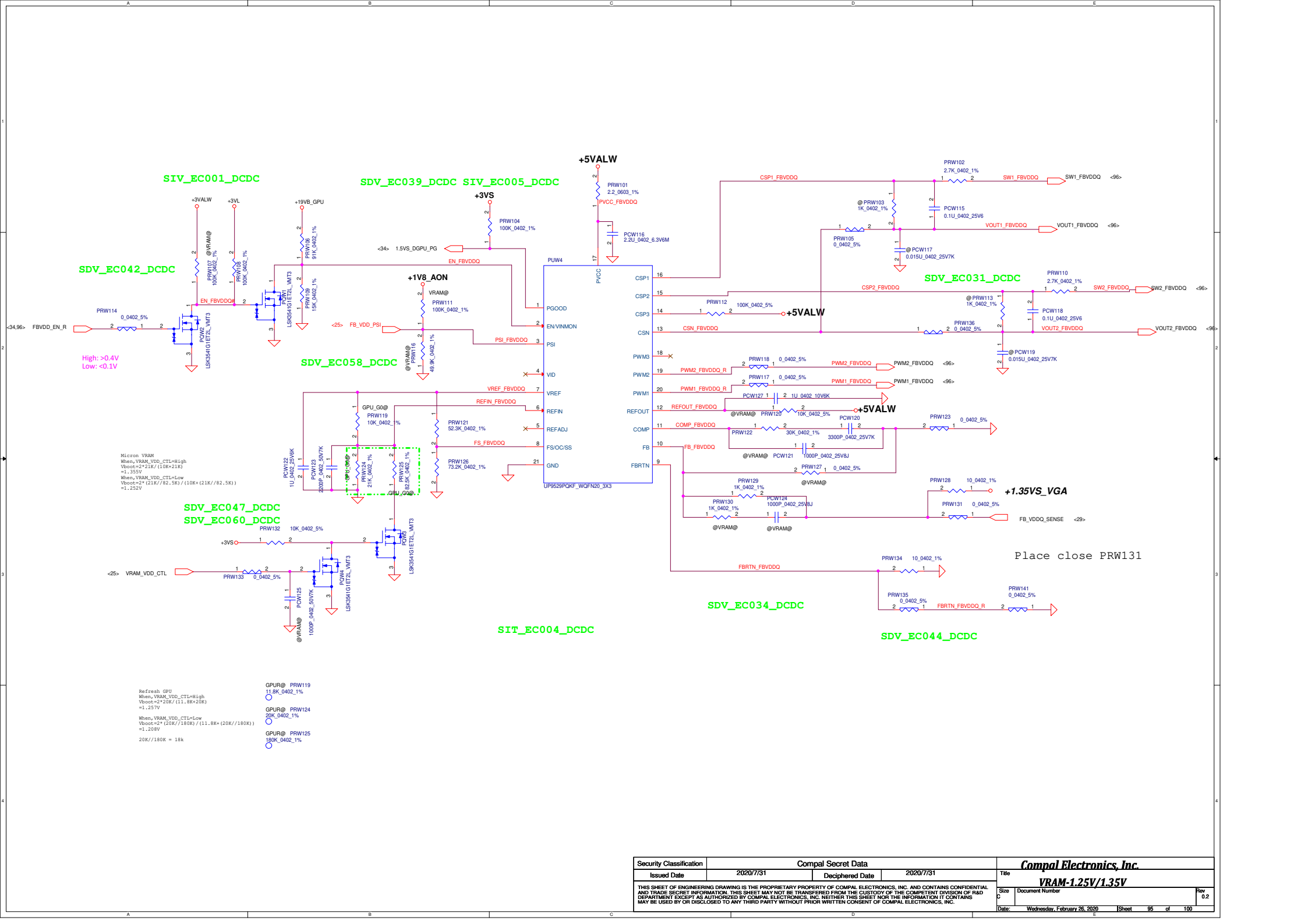
Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

Title: **PWR-VGA_DECOUPLING**

Size	Document Number	Rev
	LA-J561P	0.2

Date: Wednesday, February 26, 2020 Sheet 94 of 100



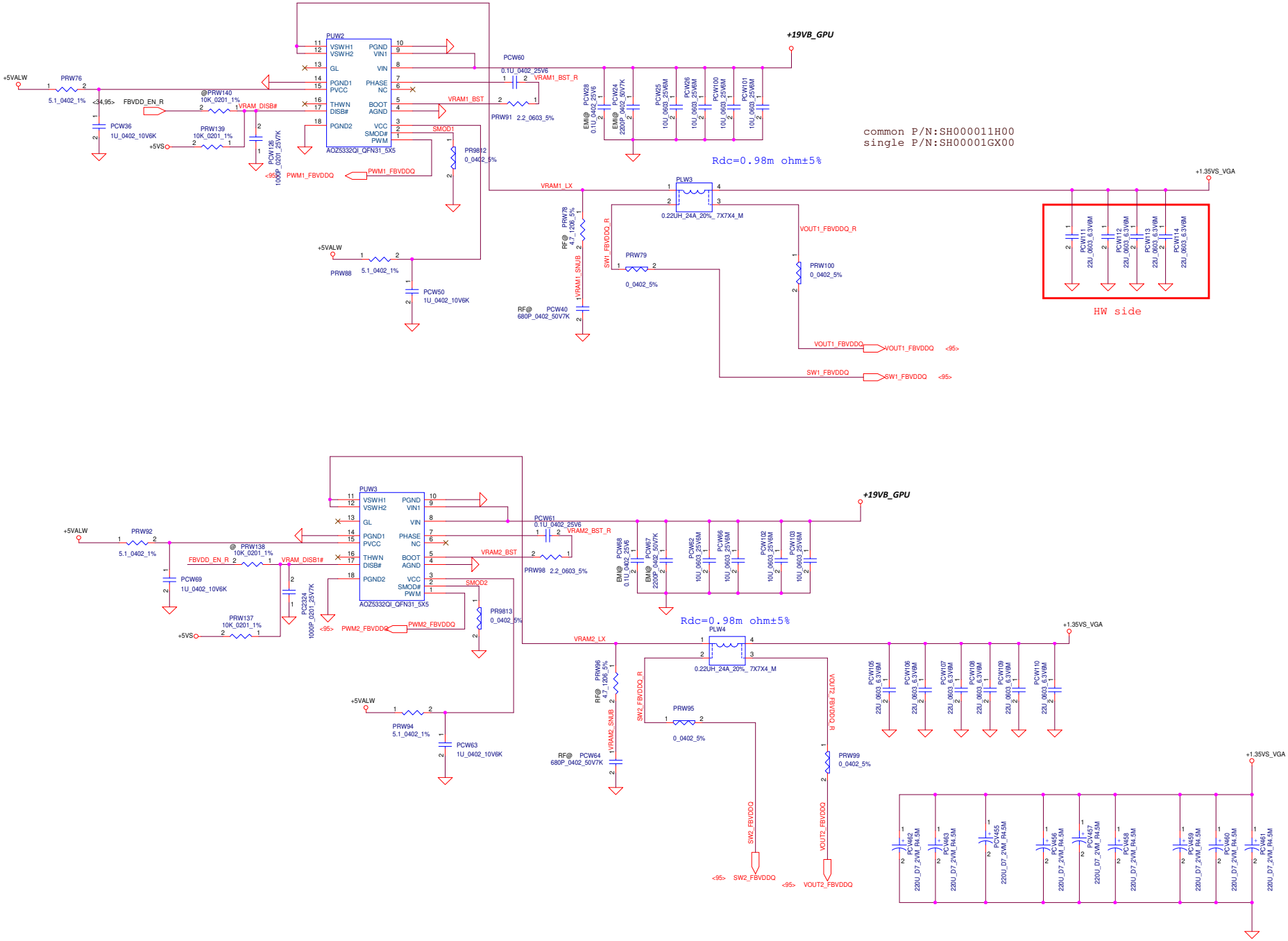
Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

Title: **VRAM-1.25V/1.35V**

Size	Document Number	Rev
C		0.2

Date: Wednesday, February 26, 2020 | Sheet 95 of 100



Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

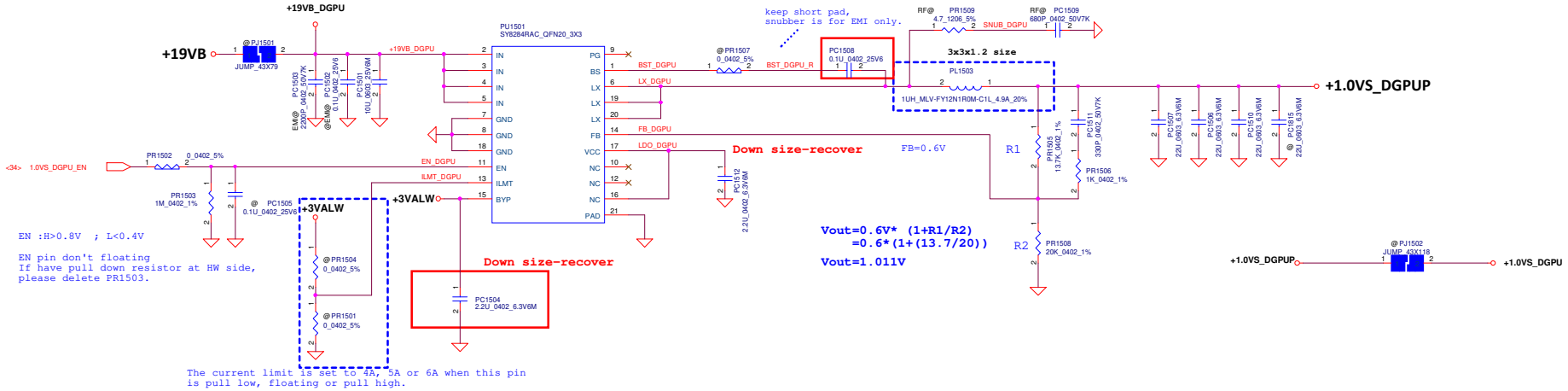
Title: **VRAM_Power**

Size	Document Number	Rev
C		0.2

Date: Wednesday, February 26, 2020 | Sheet 96 of 100

Module model information

SY8288_V2_single.mdd
SY8288_V2_dual.mdd



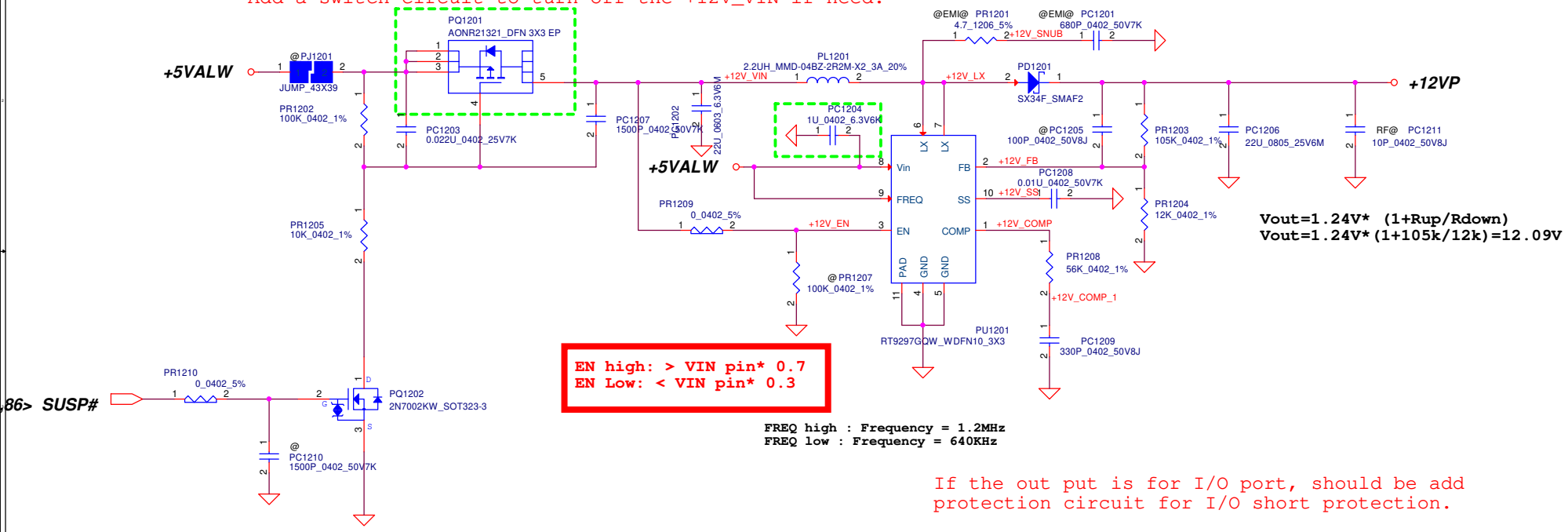
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/7/31	Deciphered Date 2020/7/31	Title: PWR_1.0V_DGPU
			Size: Document Number: Rev: 0.2
			Date: Wednesday, February 26, 2020 Sheet 97 of 100

Module model information

RT9297_V1.mdd

Must check PL501 and PD501 rating
for your application.

Add a switch circuit to turn off the +12V_VIN if need.



Vout=1.24V* (1+Rup/Rdown)
Vout=1.24V*(1+105k/12k)=12.09V

EN high: > VIN pin* 0.7
EN Low: < VIN pin* 0.3

FREQ high : Frequency = 1.2MHz
FREQ low : Frequency = 640KHz

If the out put is for I/O port, should be add
protection circuit for I/O short protection.

Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

Compal Electronics, Inc.

Title: **PWR- 12V**

Size: Custom | Document Number: **LA-J561P** | Rev: 0.2

Date: Wednesday, February 26, 2020 | Sheet 98 of 100

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	2512 size is X1 code	92	PR1301 & PR1302 From 0.005_2512_1% change to 0.005_1206_1%	9/25	SIV
2	Refresh GPU, VRAM Voltage change	95	Add BOM Structure GPUR@ (PRW119 = 11.8k , PRW124 = 20k , PRW125 = 180k)	9/25	SIV
3	Sourcer suggest	91	PCV1 From SE068221J80 (220P 25V J NPO 0402) change to SE082221J80 (220P 50V J NPO 0402) PC303 From SE025102J80 (1000P 50V J X7R 0603) change to SE025102K80 (1000P 50V K X7R 0603)	9/27	SIV
4	EMI suggest		PL501 , PLZ1 , PLZ2 , PL203 & PL204 From SM01000U600 (5A_Z80_0805_2P) change to SM01000EJ00 (HCB2012KF-221T30_2P) Add PLZ3 & PL206 (SM01000EJ00, HCB2012KF-221T30_2P) Add PCZ112 , PC333 , PC334 , PC335(SE074471K80 ,470P_0402_50V7K) Change PR316 from 0 ohm to 2.2_0603_5% Mount PC306,(SE074152K80 1500P_0402_50V7K) PJ701 Change to PL701 (SM01000EJ00, HCB2012KF-221T30_2P) Add PC209 , PC210(0.01U_0402_50V7K)	9/27	SIV
5	RTCVTT change, For CML	82	PR208 change to 0_0603_5% , Unmount PR209	9/27	SIV
6	CPU Test result	88	Change PR136 from 165K_0402 to 143K_0402 , Change PR139 from 78.7K_0402 to 90.9K_0402	10/14	SIV
7	Auto PSI function	91	Change PRV88 from 20K_0402 to 24.9K_0402 , Change PRV89 from 10K_0402 to 13.3K_0402	10/14	SIV
8	DCR sense fine tuning	95	Change PRW102, PRW110 from 2.26K_0402 to 2.7K_0402	10/14	SIV
9	Uniform size	96	Change PR9812,PR9813 from 0_0201 to 0_0402_5%	11/29	SIT
10	RF suggest	84,85,98	Add PC1211 , PC421 & PC527 , (10P_0402_50V8J)	11/29	SIT
11	CPU Test result , Part count reduce	90	Unmount PC900,PC902,PC930	12/03	SIT
12	For CPU PRPCHOT issue	83	Unmount PR351, PC318	12/04	SIT
13	Part count reduce	83,88,90, 95,98	PR90 , PR94 , PR107 , PR111 , PR114 , PR117 , PRV1 , PRV7 , PRV9 , PRV11 , PRV13 , PRV17 PRW114 , PRW135 , PRW131 , PRW135 , PRW141 , PR1209 , PR1210 , PR348 , PR 349 From 0_0402_5% change to R-short.	2020/01/17	SVT
14	Part count reduce	95, 96	PR9812, PR9813, PRW79, PRW100, PRW95, PRW99, PRW117, PRW118, PRW123, PR208, PR412 ,PR413, PR701, PR715, PR1807, PR1502 From 0_0402_5% change to R-short.	2020/01/20	SVT
15	Part count reduce		PR103,PR322,PR352,PR354,PR414,PRV28,PRW105,PRW136,PRW141,PR1055,PR317 From 0_0402_5% change to R-short.	2020/02/25	SVT
16	Cost Down	83	Unmount PQ314 , PQ315 ,PR338	2020/02/25	SVT
16	For ACS5 ID pin issue	82	Unmount PR207 , Mount PR211	2020/02/26	SVT

Compal Electronics, Inc.			
Title: PWR-PIR			
Size: Custom	Document Number: LA-J561P		Rev: 0.2
Date: Wednesday, February 26, 2020	Sheet 99 of 100		

Title	PWR-Reserve
Size: A	Document Number: LA-J561P
Rev: 0.2	
Date: Wednesday, February 26, 2020	Sheet 100 of 100