LYON-External

CPU : Intel PENRYN
Chip Set : Intel CANTIGA PM + ICH9M
Remarks : Montevina Platform (NB9M)

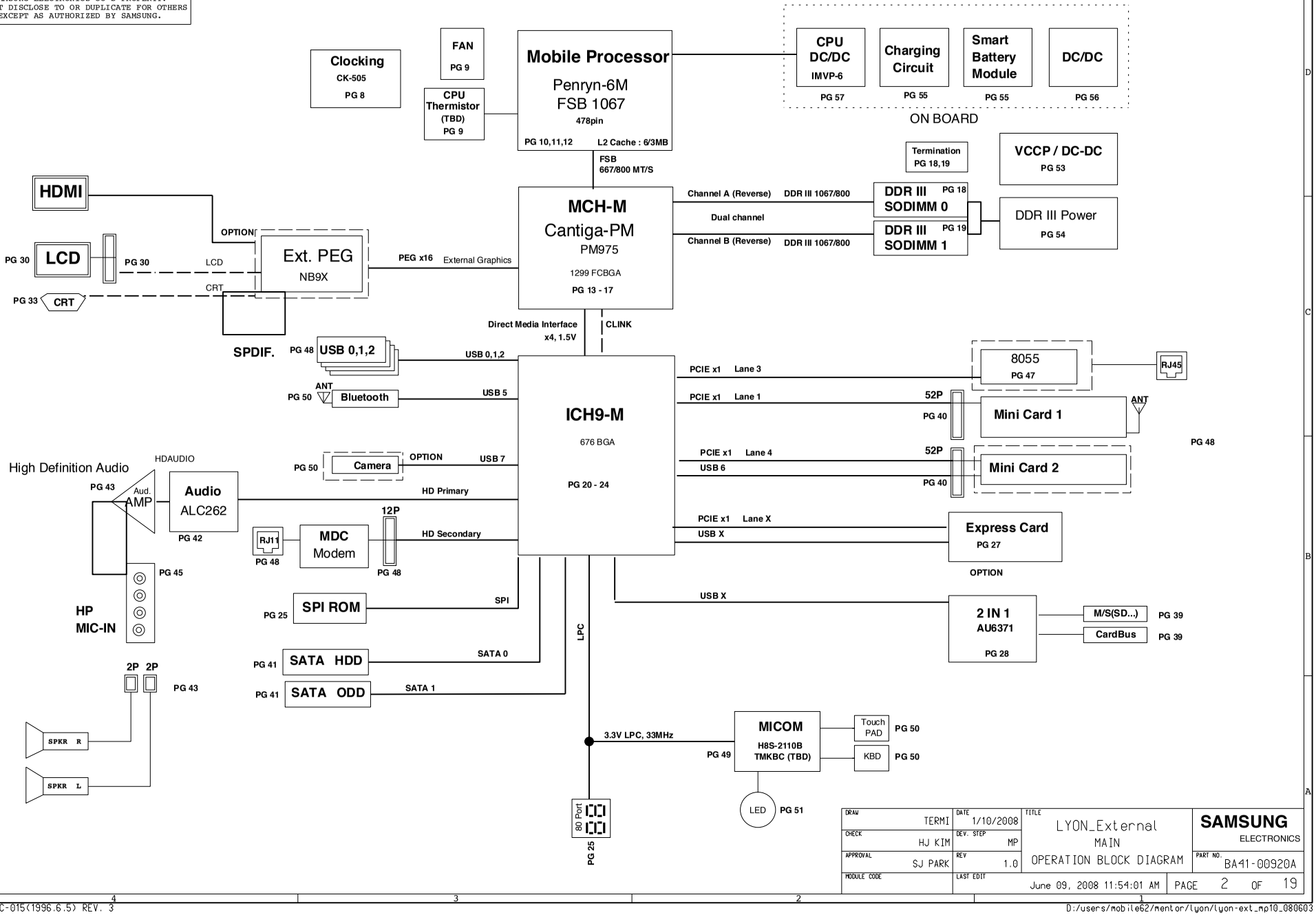
Model Name : LYON-Ext
PBA Name : MAIN
PCB Code : TPT : BA41-00919A
GCE : BA41-00920A
NAN : BA41-00921A

Dev. Step : MP
Revision : 1.0
T.R. Date : 2008.06.09

DRAW	CHECK	APPROVAL

■ *Owner : SEC Mobile R & D* *Signature :* *X*

DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External COVER	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00920A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 1 OF 19	



DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External MAIN OPERATION BLOCK DIAGRAM	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 2 OF 19	

BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	3	A,B,C
USB	AD29(internal)	-	USB2.0 #0 (USB0) : A USB2.0 #1 (USB1) : D USB2.0 #2 (USB4) : C USB2.0 #3 (USB5) : E USB2.0 #4 (EHCI) : H
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B
GLAN	-	-	F

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core Voltage for CPU
GFX_CORE	Core Voltage for GPU
P1.05V (VCCP)	VTT for CPU, Crestline & ICH8-M
P3.3V_MICOM	3.3V always power rail (for Micom)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR (off in S4-S5)
P0.9V	0.9V power rail for DDR (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail (off in S4-S5)
P5.0V	5.0V switched power rail (off in S3-S5)
P5.0V_AUX	5.0V switched on power rail (off in S4-S5)
P5.0V_ALW	5.0V always power rail

USB PORT Assign

PORT #	ASSIGNED TO
	SYSTEM PORT 0
	SYSTEM PORT 1
	SYSTEM PORT 2
	NC
	NC
	Bluetooth
	Mini PCI Express 2
	Camera
	NC
	NC

PCI Express Assign

PORT #	ASSIGNED TO
0	NC
1	Mini Card 1 (WLAN)
2	NC
3	LOM
4	Mini Card 2 (ROBSON or DVB-T)
5	NC

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH8-M	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	Intel LAN

LCD Pannel Detect (TBD)

Devices	Resolution	PANNEL_DETECT_0

I C / SMB Address

Devices	Address	Hex	Bus
ICH8-m	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

REVISION HISTORY

See rev notes for more information.

DESIGN: TERMI	DATE: 1/10/2008	TITLE: LYON_External CHIPSET POWER UNDEFINED	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
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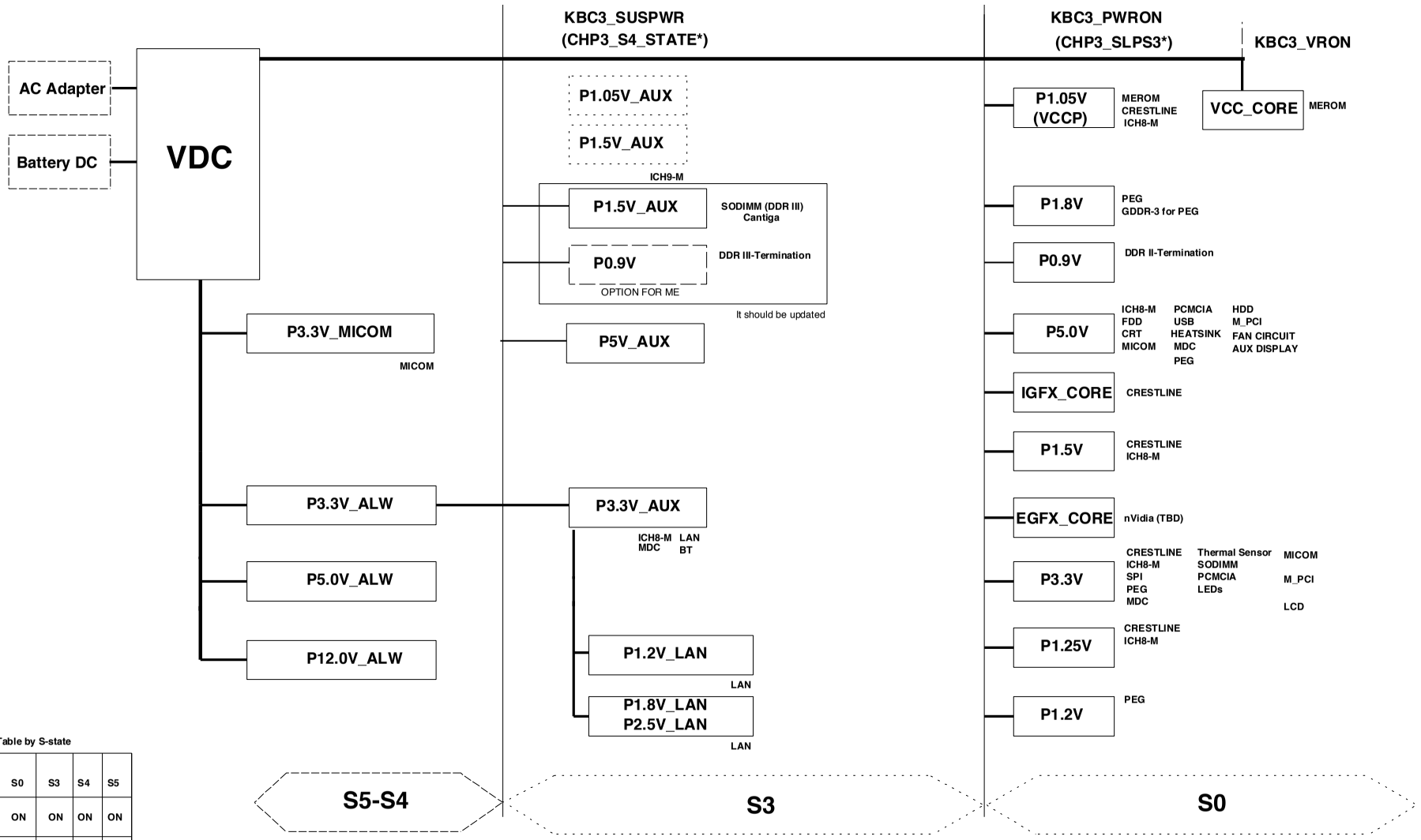
POWER DIAGRAM

Rev 0.1



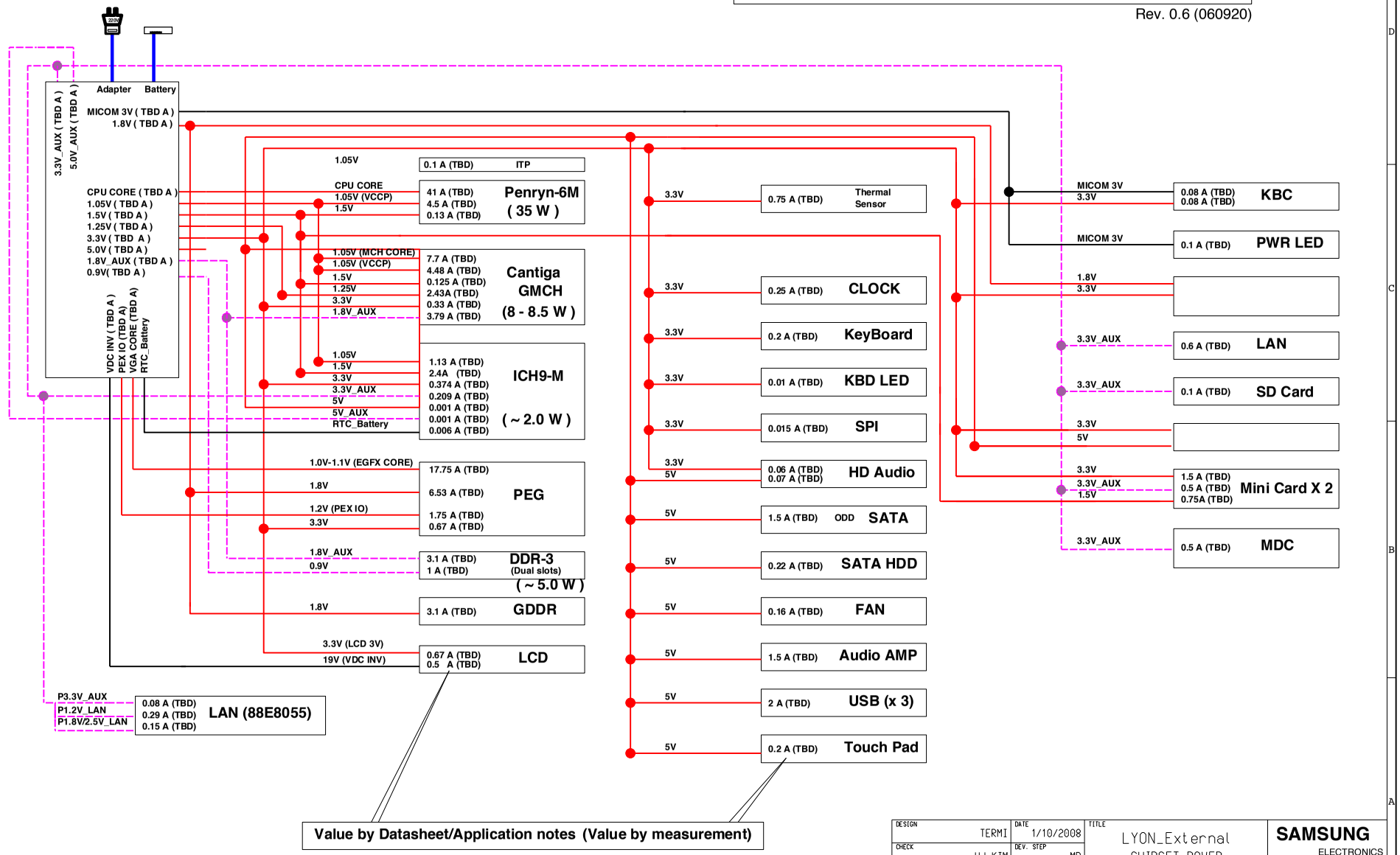
Power On/Off Table by S-state

Rail / State	S0	S3	S4	S5
+V*A(LWS) +V*LAN	ON	ON	ON	ON
+1.8V_AUX +0.9V	ON	ON	—	—
+V*AUX	ON	ON	—	—
+V	ON	—	—	—
+V* (CORE)	ON	—	—	—

DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External MAIN POWER DIAGRAM	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00920A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 4 OF 19	

POWER RAILS ANALYSIS

Rev. 0.6 (060920)



Value by Datasheet/Application notes (Value by measurement)

DESIGN: TERMI	DATE: 1/10/2008	TITLE: LYON_External CHIPSET POWER UNDEFINED	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 5 OF 19	

POWER SEQUENCE

Rev. 0.7

Host Boot / ME Off
(SLPS4* = S4_STATE*) > (SLPM* = SLPS3*)
M-1) KBC3_DDR_PWRON (TBD) = 8) KBC3_SUSPWR
M-2) KBC3_ME_PWRON = 15) KBC3_PWRON

Host / ME Boot
(SLPS4* = S4_STATE*) > SLPM* > SLPS3*

Host S5 / ME Boot
(SLPS4* = SLPM*) > S4_STATE* > SLPS3*

RTC Battery — PRTC_BAT — CHP3_RTCRST# — 1

POWER S/W — 4) POWER_SW*

KBC — 7
110ms Delay
8) CHP3_SLPS5#/4#/3# — 8
7) KBC3_RSMRST#
17) KBC3_PWRGD
15)VRM3_CPU_PWRGD
5) KBC3_SUSPWR
9) KBC3_PWRON
13) KBC3_VRON — 5, 9, 13

ICH8-M — Sheet 22-25
10-1) ICH_CORE (P1.05V)
6) P3.3V_AUX
PRTC PRTC — 16
LAN100_SLP
INTVRMEN
7) P1.05V_AUX
7) P1.5V_AUX
VRMPWRGD
PWROK
CL_PWROK
17) KBC3_PWRGD
15)VRM3_CPU_PWRGD
16) CLK3_PWRGD
18) CPU1_PWRGDCPU
19) PLT3_RST*
19) PCI3_RST*

CK-505 — Sheet 8
16-1) Clock Running
15) VRM3_CPU_PWRGD — 15

CPU VRM — DC/DC B'd
11) VCCP3_PWRGD (GM-model)
12)GCORE3_PWRGD (PM-model)
13) KBC3_VRON (Back-up)
14) VCC_CORE — 14

CPU — Sheet 10-12 — (Test Option) — 18
10-1) P1.5V
10-1) P1.05V
18) CPU1_PWRGDCPU
19) PLT3_RST*
19) PCI3_RST*
20) CPU1_CPURST* — 20

GMCH
17) KBC3_PWRGD
17) KBC3_PWRGD
PWROK
CL_PWROK
19) PLT3_RST*
6) P1.8V_AUX
10-1) P3.3V
10) P1.05V (IGFX_CORE)
PM-model only
Sheet 15-19

DDR2 POWER
SC486 — Sheet 50 — 6
10) P5.0V
2) VDC
5) KBC3_SUSPWR
6) P1.8V_AUX
6) MEM1_VREF
10-2) 0.9V

3) P3.3V_MICOM

Adapter / Battery
AC_DC / Battery
MAX 1909
2) VDC — 2
2-1) P12.0V_ALW

8) KBC3_SUSPWR
9) KBC3_PWRON

SC486 — 10) P1.5V
SC4435 — 10) P5.0V — 10
9-1 — 9-1) KBC3_PWRON_INV#

ISL6227
2) VDC
9) KBC3_PWRON
10) P1.25
10) P1.05V (IGFX_CORE)
11) VCCP3_PWRGD — 11

ADP3209 — 12
11-1) GFX_CORE
12)GCORE_PWRGD

P3.3V_AUX & P5V_AUX
MAX 8734 — 3
P5.0V_ALW
P3.3V_MICOM — 6
6) P5.0V_AUX
6) P3.3V_AUX

9-1
6) P3.3V_AUX
9-1) KBC3_PWRON_INV#
FDS6680A — Sheet 40 — 10-1) P3.3V
6) P1.8V_AUX
FDS6680A — Sheet 40 — 10-1) P1.8V
10-1) P1.25
FDC653N — Sheet 40 — 10-1) P1.2V

6) P1.8V_AUX
10-2) P0.9V
DDR3 Memory — Sheet 20-21

PCIe Devices — 19
10-1) P3.3V
10-1) P1.8V
10) P1.5V

PEG
10-1) P1.2V
2) VDC
10-1) P3.3V

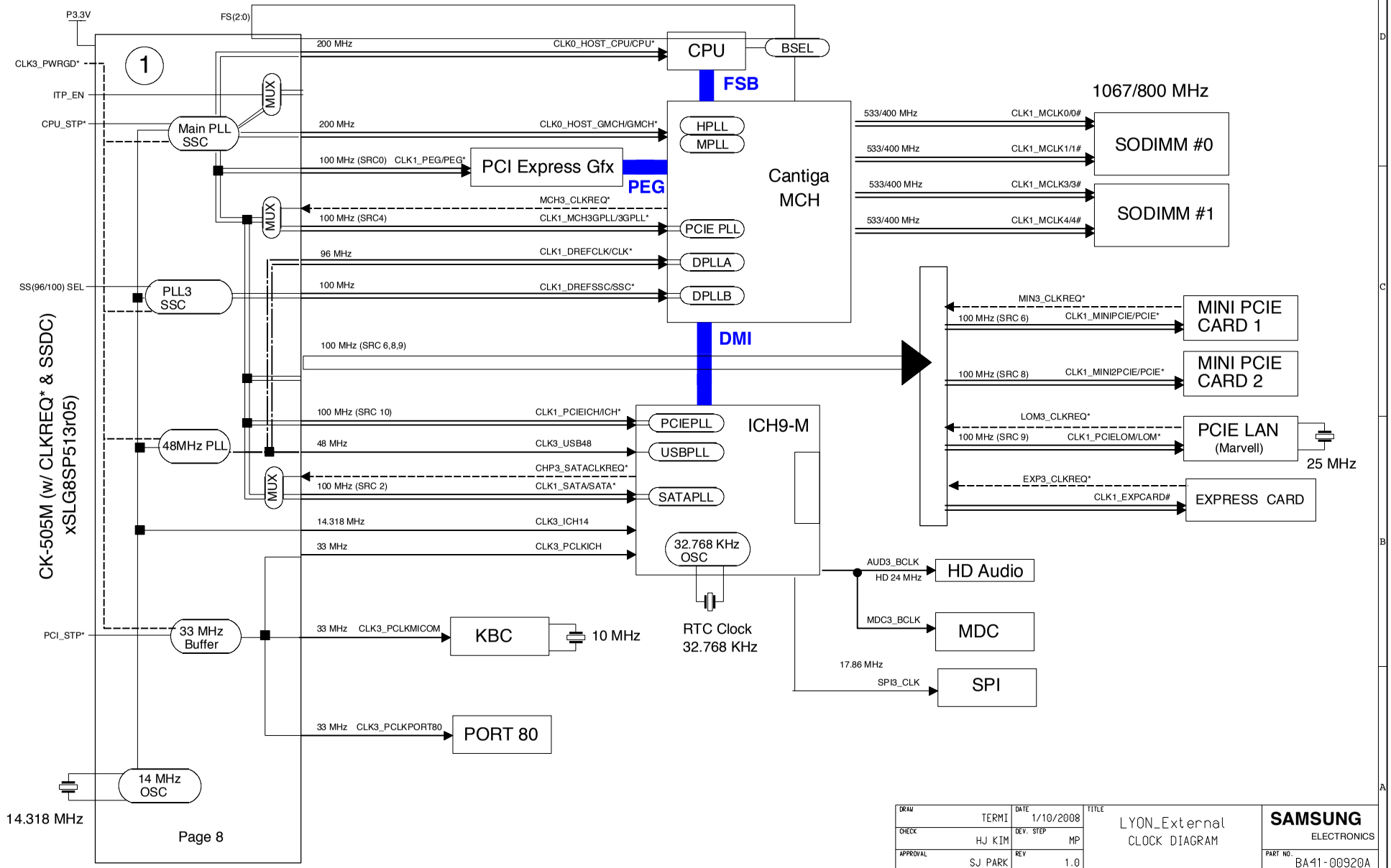
PCI Devices
10-1) P3.3V
10-1) P1.8V
10) P1.5V
19) PCI3_RST*

LOM Marvell — Sheet 46-47
6-1) P1.2V_LAN
6-1) P1.8V/P2.5V_LAN
BCP69 — Sheet 46

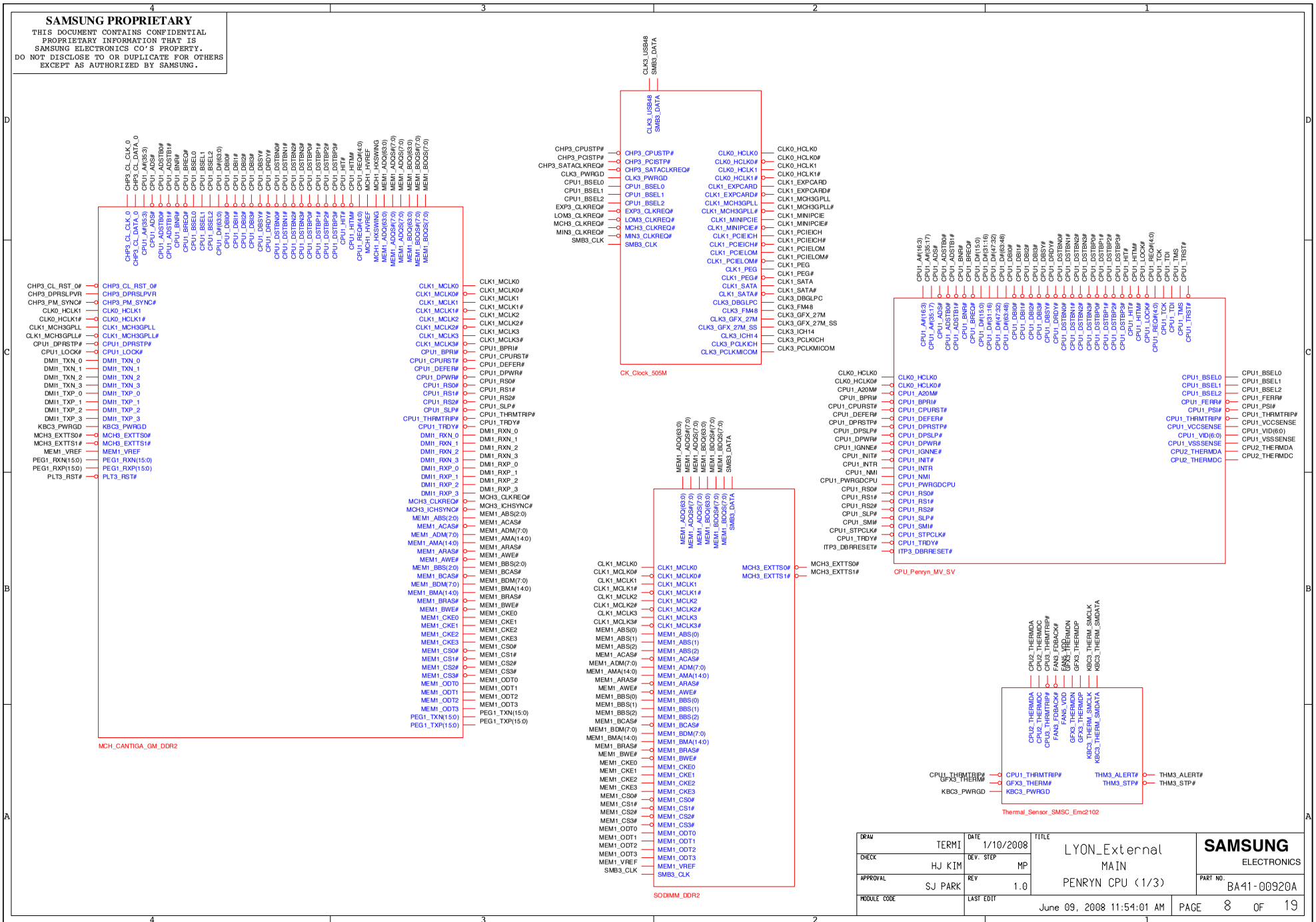
2) VDC
TPS51124
12) P1.05V_M
12) P1.5
11) KBC3_PWRON

DESIGN: TERMI	DATE: 1/10/2008	TITLE: LYON_External CHIPSET POWER UNDEFINED	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00920A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 6 OF 19	

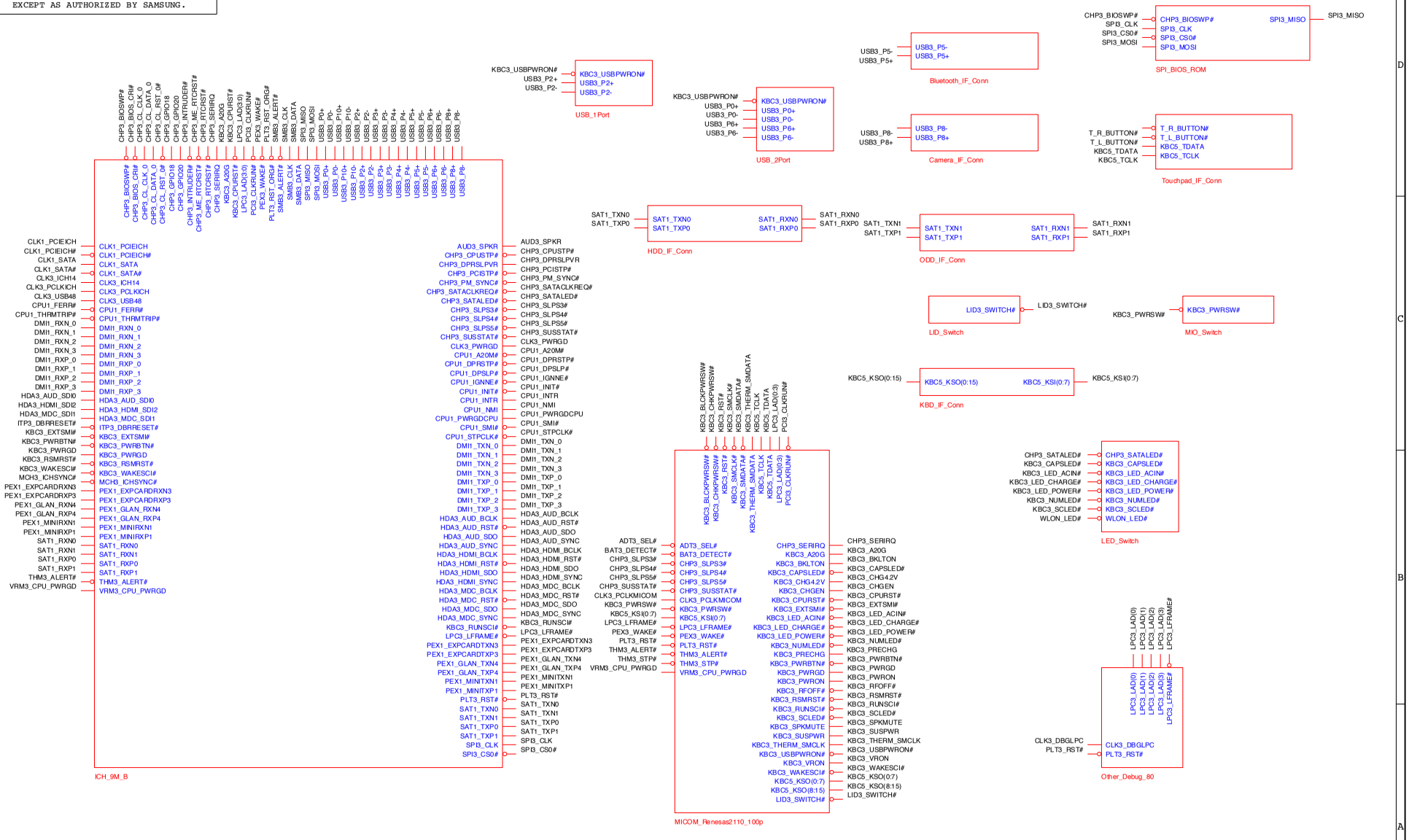
CLOCK DISTRIBUTION Rev. 0.1



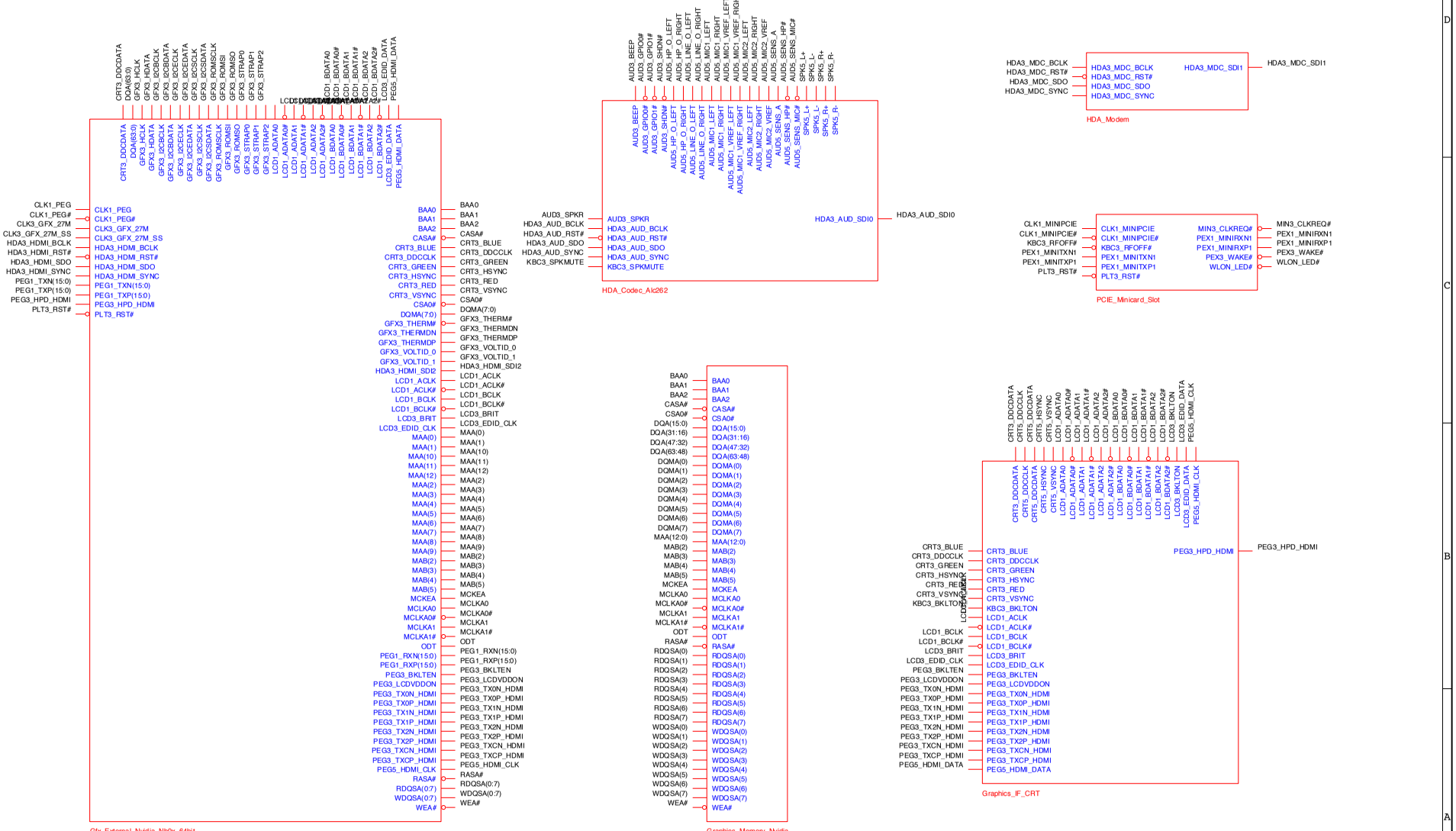
DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External CLOCK DIAGRAM	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 7 OF 19	



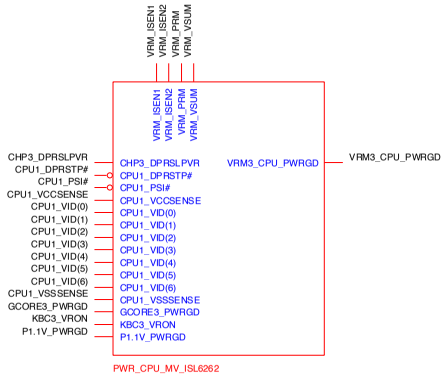
DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External MAIN PENRYN CPU (1/3)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00920A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 8 OF 19	

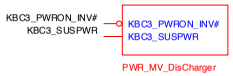


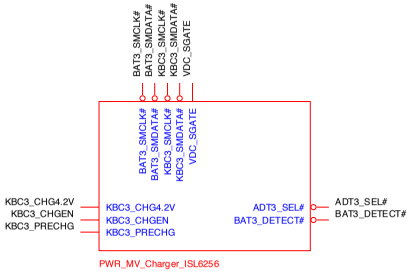
DESIGN: TERMI	DATE: 1/10/2008	TITLE: LYON_External CHIPSET POWER UNDEFINED	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 9 OF 19	



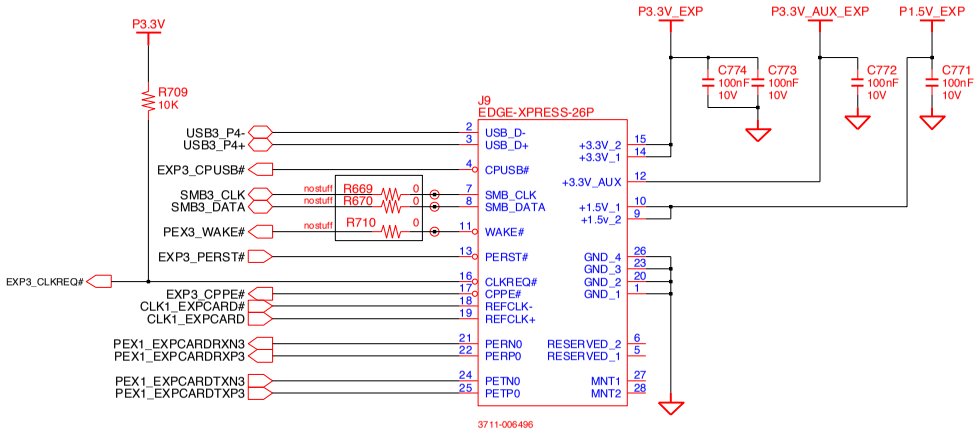
DESIGN: TERMI	DATE: 1/10/2008	TITLE: LYON_External CHIPSET POWER UNDEFINED	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00920A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 10 OF 19	

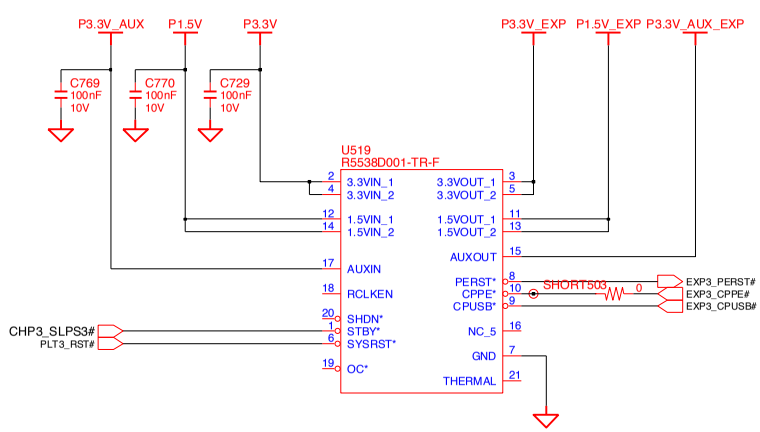


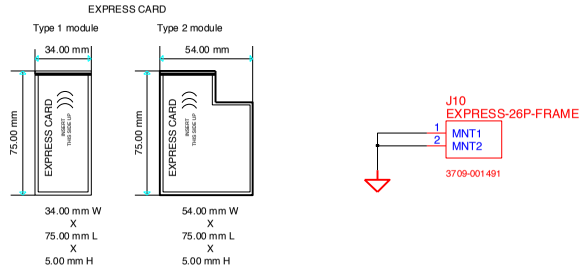




DESIGN: TERMI	DATE: 1/10/2008	TITLE: LYON_External CHIPSET POWER UNDEFINED	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 11 OF 19	







DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0	EXPRESS CARD	PART NO.: BA41-00920A
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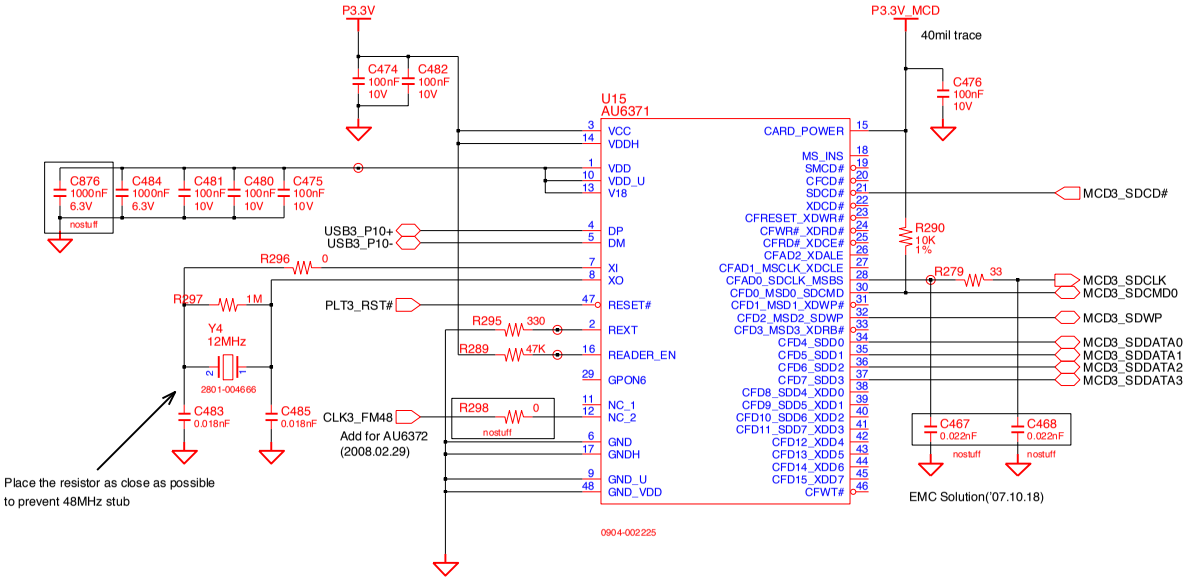
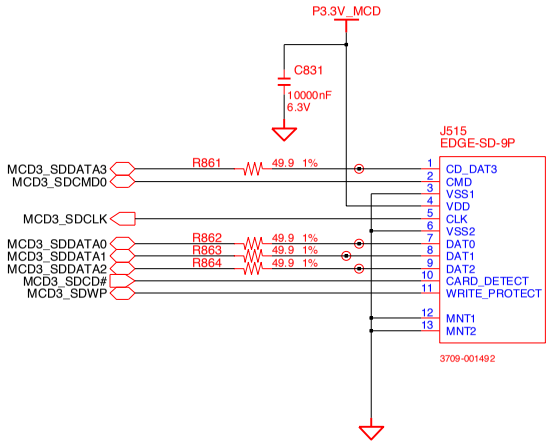
2 IN 1 CARD





2-in-1 Socket

DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP	2 in 1 Socket	
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
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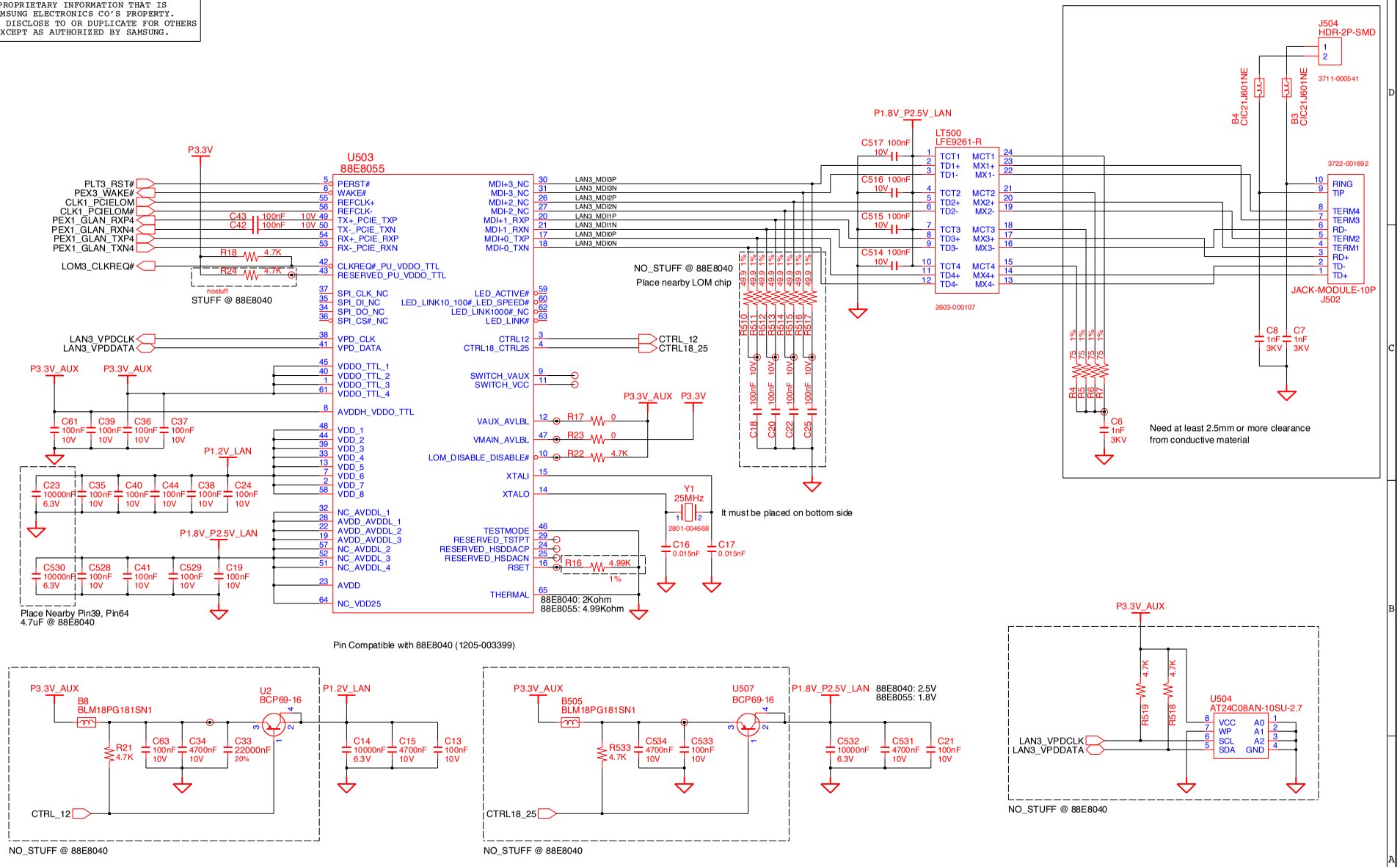

DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External MAIN LAN	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO. BA41-00920A
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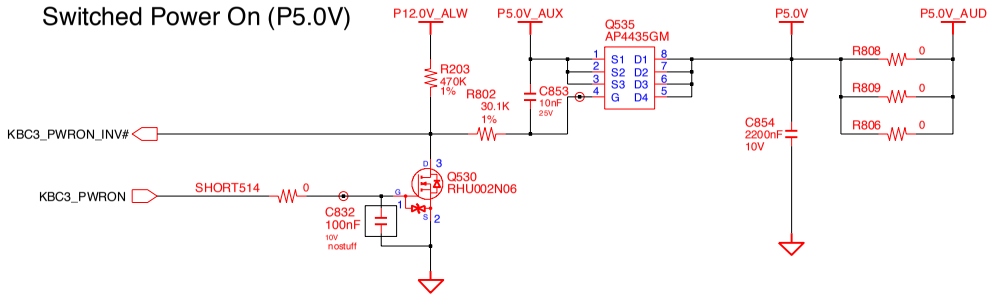
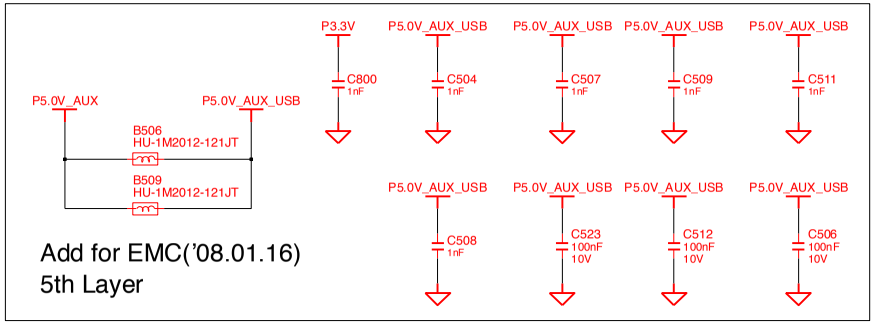
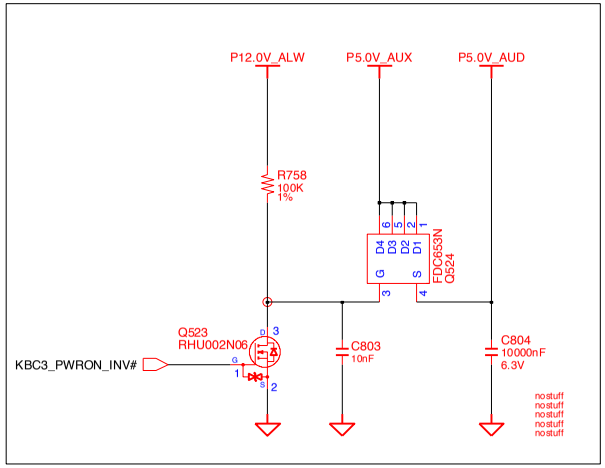
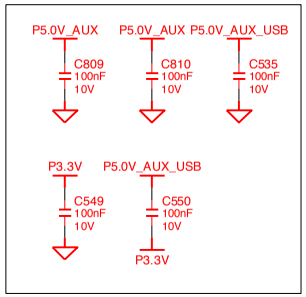
Switched Power On (P5.0V)



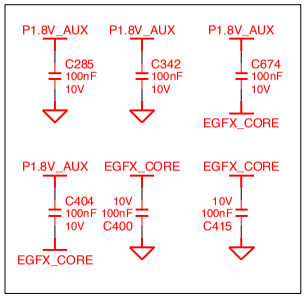


Audio Power (nostuff)

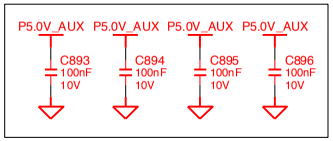




Add for SI(2007.12.6)

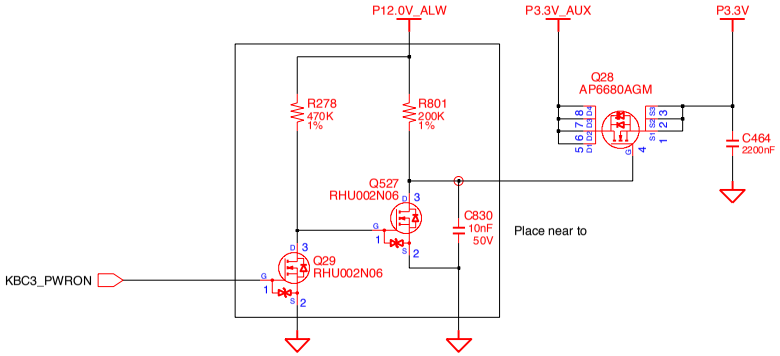


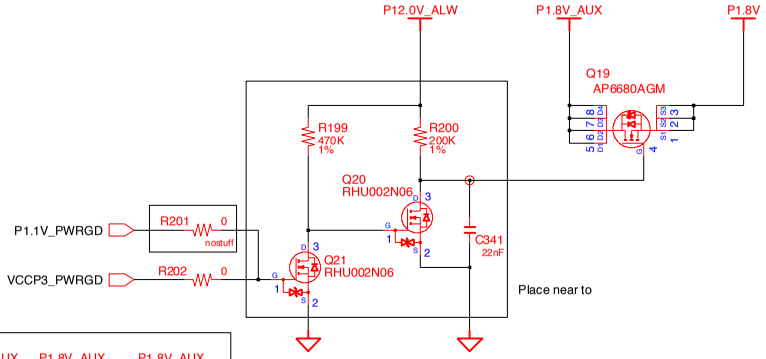
Add for SI(2008.03.07)

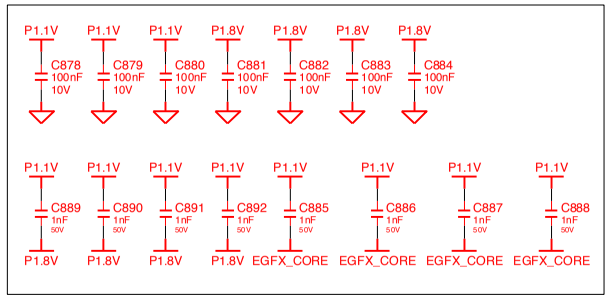


Add for EMI(2008.04.29)

Switched Power On (P3.3V & 1.8V)







Add for EMI(2008.04.26)

DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External MAIN MICOM & SWITCHED POWER	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
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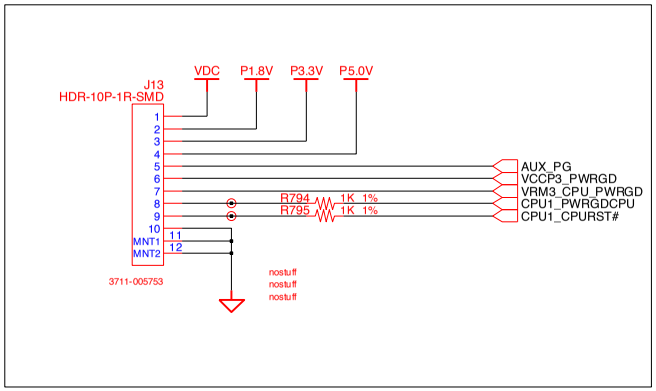
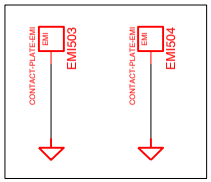
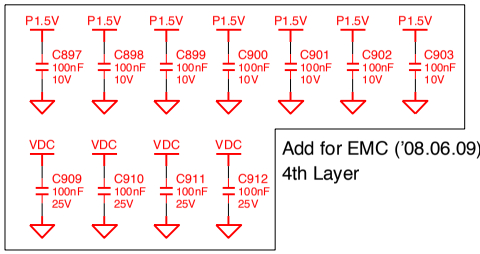
ICT PORT

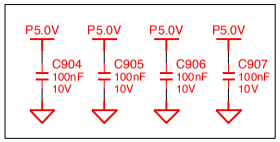




Add for EMC ('08.04.22)

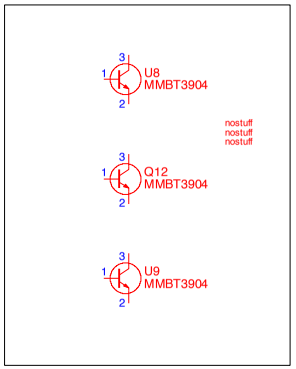


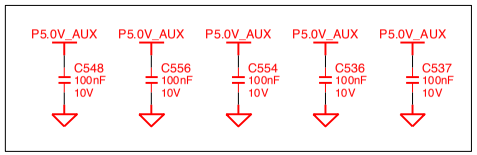
Add for EMC ('08.06.09)
4th Layer



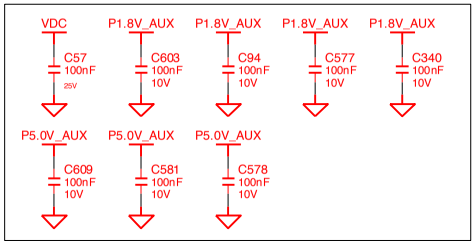
Add for EMC ('08.06.09)
Bottom Side

For Debugging

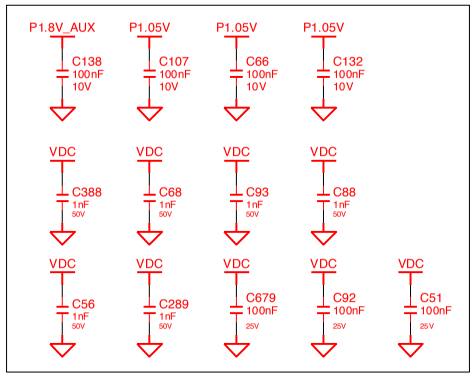




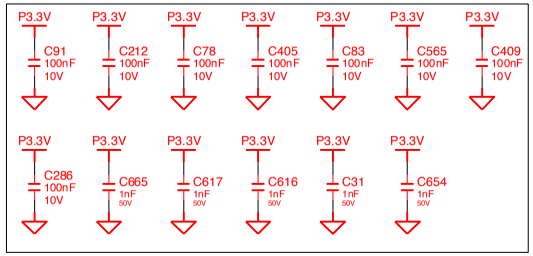
Add for EMC ('08.01.16)
5th Layer



Add for EMC ('08.01.16)
Bottom Side

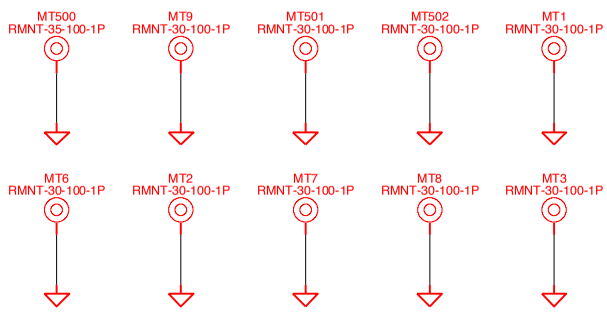


Add for EMC ('08.01.16)
Top Side

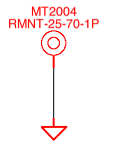


Add for EMC ('08.03.05)

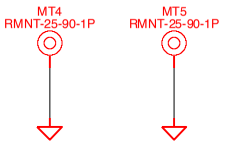
System



Board

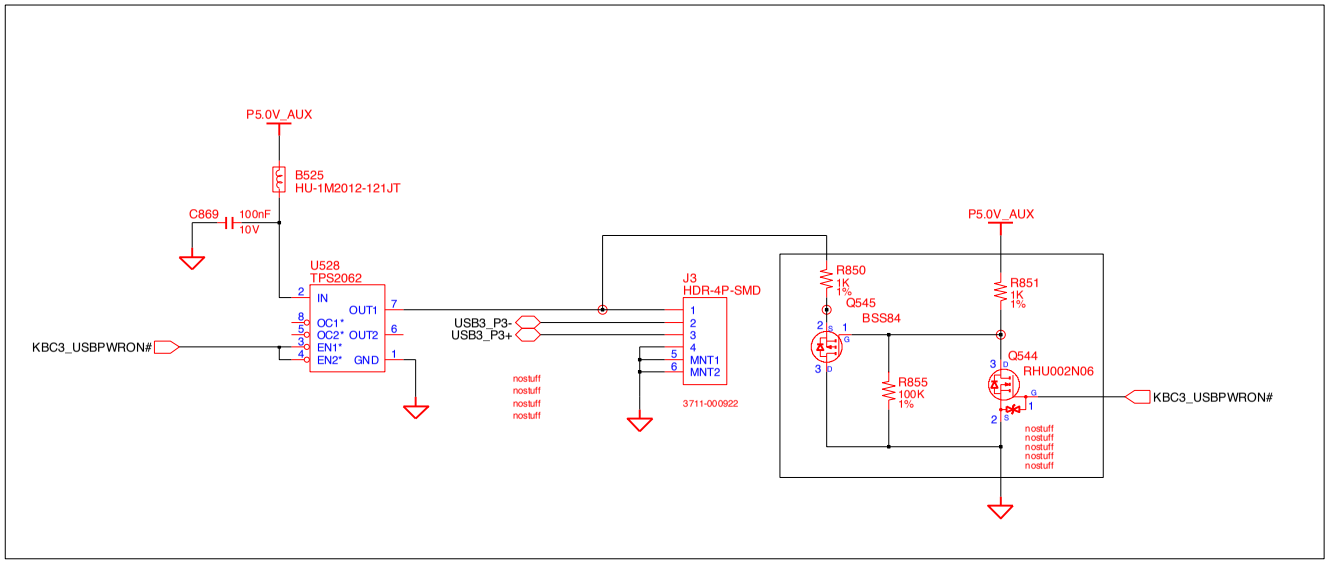


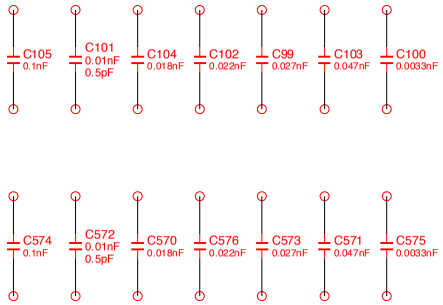
Keyboard



DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP	ICT PORT	
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE: undefined	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 16 OF 19	

Sub Board Connector (Istanbul Only)

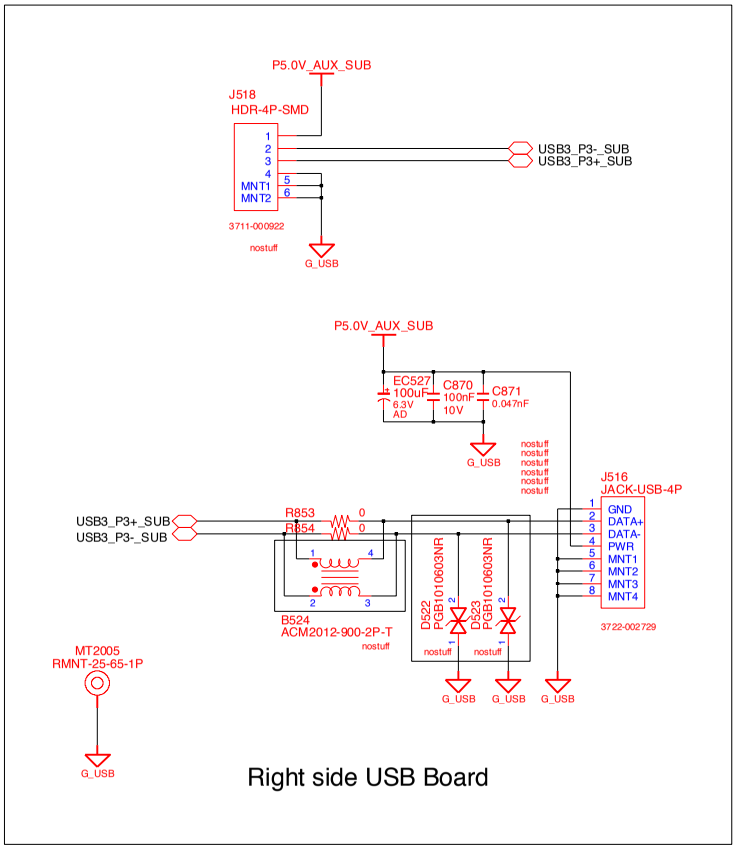


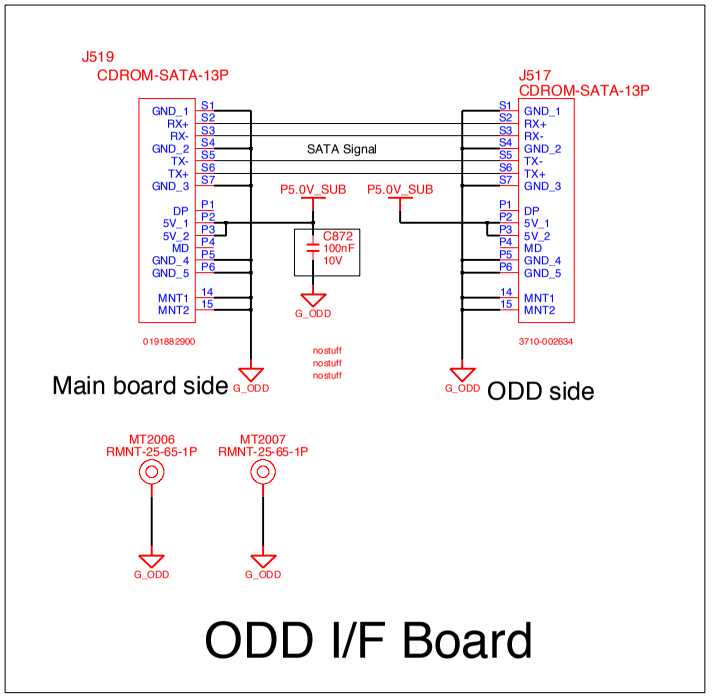


PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(YY/MM/DD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External	SAMSUNG ELECTRONICS	
CHECK: HJ KIM	DEV. STEP: MP	TP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A	
MODULE CODE: undefined	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 17 OF 19		

Sub Board (Istanbul only)





DESIGN: TERMI	DATE: 3/28/2008	TITLE: LYON_External SUB BOARD USB, ODD	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 18 OF 19	

- AUX_PG
- CTRL_12
- SPK5_L+
- SPK5_L-
- SPK5_R+
- SPK5_R-
- VRM_PRM
- CPU1_NMI
- CPU1_TCK
- CPU1_TDI
- CPU1_TMS
- CRT3_RED
- FAN5_VDD
- SMB3_DATA
- SPI3_CS0#
- SPI3_MISO
- SPI3_MOSI
- THM3_STP#
- VRM_ISEN1
- VRM_ISEN2
- WLON_LED#
- AUD3_SHDN#
- EXP3_CPPE#
- KBC3_CHGEN
- KBC3_PWRGD
- KBC3_PWRON
- KBC5_TDATA
- CPU1_TRDY#
- CPU1_TRST#
- CRT3_GREEN
- CRT3_HSYNC
- CRT3_VSYNC
- CRT5_HSYNC
- CRT5_VSYNC
- CPU1_HITM#
- CPU1_INIT#
- CPU1_LOCK#
- SMB3_CLK
- SPI3_CLK
- PEX3_WAKE#
- AUD3_GPIO0#
- AUD3_GPIO1#
- AUD5_SENS_A
- BAT3_SMCLK#
- CHP3_GPIO18
- CHP3_GPIO20
- CHP3_SERIRQ
- CHP3_SLPS3#
- CHP3_SLPS4#
- CHP3_SLPS5#
- CLK3_ICH14
- CLK3_PWRGD
- CLK3_USB48
- VRM_VSUM
- ADT3_SEL#
- AUD3_BEEP
- AUD3_SPKR

- CLK3_FM48
- CPU1_ADS#
- CPU1_BNR#
- CPU1_HIT#
- CPU1_INTR
- CPU1_PSI#
- CPU1_RS0#
- CPU1_RS1#
- CPU1_RS2#
- CPU1_SLP#
- CPU1_SMI#
- CRT3_BLUE
- CTRL18_25
- KBC3_A20G
- KBC3_RST#
- KBC3_VRON
- KBC5_TCLK
- CLK3_DBGLPC
- LCD3_BRIT
- MCD3_SDWP

- CPU1_IGNNE#
- CPU1_VID(0)
- CPU1_VID(1)
- CPU1_VID(2)
- CPU1_VID(3)
- CPU1_VID(4)
- CPU1_VID(5)
- CPU1_VID(6)
- CRT3_DDCCLK
- CRT5_DDCCLK
- EXP3_CPUSB#
- EXP3_PERST#
- MEM1_VREF
- PLT3_RST#
- CPU1_DEFER#
- CPU1_DPSLP#
- KBC3_BKLTON
- KBC3_PRECHG
- KBC3_PWRSW#
- KBC3_RFOFF#
- KBC3_SCLED#
- KBC3_SMCLK#
- KBC3_SUSPWR
- KBC5_KSI(0)
- KBC5_KSI(1)
- KBC5_KSI(2)
- KBC5_KSI(3)
- KBC5_KSI(4)
- KBC5_KSI(5)
- KBC5_KSI(6)
- KBC5_KSI(7)
- KBC5_KSO(0)
- KBC5_KSO(1)
- KBC5_KSO(2)
- KBC5_KSO(3)
- KBC5_KSO(4)
- KBC5_KSO(5)
- KBC5_KSO(6)
- KBC5_KSO(7)
- KBC5_KSO(8)
- KBC5_KSO(9)
- LAN3_VPDCLK
- LCD3_BKLTON
- LPC3_LAD(0)
- LPC3_LAD(1)
- LPC3_LAD(2)
- LPC3_LAD(3)
- MCD3_SDCMD0
- PEG3_BKLTEN
- CPU1_A20M#
- CPU1_BPRI#
- CPU1_BREQ#
- CPU1_BSEL0
- CPU1_BSEL2
- MCD3_SDCD#
- MCD3_SDCLK
- MCH1_HVREF
- CPU1_FERR#
- SMB3_ALERT#
- THM3_ALERT#
- T_L_BUTTON#
- T_R_BUTTON#
- VCCP3_PWRGD
- BAT3_DETECT#
- BAT3_SMDATA#
- CHP3_BIOSWP#
- CHP3_CPUSTP#
- CHP3_PCISTP#
- CHP3_RTCRST#
- CLK3_PCLKICH
- CPU1_CPURST#
- CPU1_DPRSTP#
- CPU1_DBSY#
- CPU1_DPWR#
- CPU1_DRDY#
- KBC5_KSO(14)
- KBC5_KSO(15)
- LAN3_VPDDATA

- CPU1_STPCLK#
- CPU2_THERMDA
- CPU2_THERMDC
- CRT3_DDCDATA
- CRT5_DDCDATA
- EXP3_CLKREQ#
- FAN3_FDBACK#
- HDA3_AUD_SDO
- HDA3_MDC_SDO
- KBC3_CPURST#
- KBC3_EXTSMI#
- KBC3_NUMLED#
- KBC3_PWRBTN#
- KBC3_RSMRST#
- KBC3_RUNSCI#
- KBC3_SMDATA#
- KBC3_SPKMUTE
- KBC5_KSO(10)
- KBC5_KSO(11)
- KBC5_KSO(12)
- KBC5_KSO(13)
- LID3_SWITCH#
- LOM3_CLKREQ#
- LPC3_LFRAME#
- MCD3_SDDATA0
- MCD3_SDDATA1
- MCD3_SDDATA2
- MCD3_SDDATA3
- MCH1_HXSWING
- MCH3_CLKREQ#
- MCH3_EXTTS0#
- MCH3_EXTTS1#
- MIN3_CLKREQ#
- PCI3_CLKRUN#
- AUD5_SENS_HP#
- CHP3_CL_CLK_0
- CHP3_DPRSLPVR
- CHP3_PM_SYNC#
- CHP3_SATALED#
- PEG5_HDMI_CLK
- PLT3_RST_ORG#
- PEG3_HPD_HDMI
- AUD5_HP_O_LEFT
- AUD5_MIC1_LEFT
- AUD5_MIC2_LEFT
- AUD5_MIC2_VREF
- AUD5_SENS_MIC#
- CHP3_BIOS_CRI#
- CHP3_CL_DATA_0
- CHP3_CL_RST_0#
- CHP3_INTRUDER#

- CLK3_PCLKMICOM
- CPU1_THRMTRIP#
- CPU3_THRMTRIP#
- HDA3_HDMI_BCLK
- HDA3_HDMI_RST#
- HDA3_HDMI_SDI2
- HDA3_HDMI_SYNC
- ITP3_DBRRESET#
- KBC3_CHKPWRSW#
- KBC3_LED_ACIN#
- LCD3_EDID_DATA
- CPU1_PWRGDCPU
- CPU1_VCCSENSE
- CPU1_VSSSENSE
- HDA3_AUD_BCLK
- HDA3_AUD_RST#
- HDA3_AUD_SDI0
- HDA3_AUD_SYNC
- HDA3_HDMI_SDO
- HDA3_MDC_BCLK
- HDA3_MDC_RST#
- HDA3_MDC_SDI1
- HDA3_MDC_SYNC
- KBC3_CAPSLED#
- KBC3_WAKESCI#
- LCD3_EDID_CLK

- CHP3_SUSSTAT#
- PEG5_HDMI_CLK
- MCH3_ICHSYNC#
- PEG3_LCDVDDON
- KBC3_BLCKPWRSW#
- KBC3_LED_POWER#
- KBC3_PWRON_INV#
- AUD5_LINE_O_LEFT
- CHP3_SATACLKREQ#
- KBC3_LED_CHARGE#
- KBC3_THERM_SMCLK

- AUD5_LINE_O_RIGHT
- VRM3_CPU_PWRGD
- AUD5_HP_O_RIGHT
- AUD5_MIC1_RIGHT
- AUD5_MIC2_RIGHT
- CHP3_ME_RTCRST#
- PEG5_HDMI_DATA
- KBC3_THERM_SMDATA
- AUD5_MIC1_VREF_LEFT
- AUD5_MIC1_VREF_RIGHT

- P3.3V_AUX
- P3.3V_AUX
- P3.3V_AUX
- P3.3V_AUX

- VCC_CRT

- VDC_CHG

- VDC_INV
- VDC_INV
- VDC_INV
- VDC_INV

- VDC_ADPT

- P3.3V_AUX_EXP

- P1.8V_P2.5V_LAN

- VDC
- VDC
- VDC
- VDC

- VREF
- VREF
- VREF
- VREF

- V5FILT

- P3.3V_MICOM

- P4.75V_AUD

- P5.0V_AUX
- P5.0V_AUX
- P5.0V_AUX
- P5.0V_AUX

- P1.05V_PEG

- P12.0V_ALW

- CPU_CORE
- CPU_CORE
- CPU_CORE
- CPU_CORE

- G_AUD

- G_CHG

- G_CPU

- G_DDR

- G_MIC

- GROUND
- GROUND
- GROUND
- GROUND
- GROUND
- GROUND
- GROUND
- GROUND
- GROUND
- GROUND

- G_P3.3V

- G_P1.05V

- LCD_VDD3V

- P0.9V
- P0.9V
- P0.9V
- P0.9V

TP2518 P1.1V
TP2526 P1.1V
TP2527 P1.1V
TP2514 P1.1V

- P3.3V
- P3.3V
- P3.3V
- P3.3V

- P5.0V
- P5.0V
- P5.0V
- P5.0V

- P1.05V
- P1.05V
- P1.05V
- P1.05V

- PRTC_BAT

- P1.2V_LAN
- P1.2V_LAN
- P1.2V_LAN
- P1.2V_LAN

TP2517 P1.5V
TP2525 P1.5V
TP2515 P1.5V
TP2516 P1.5V

- P1.5V_EXP
- P1.5V_EXP
- P1.5V_EXP
- P1.5V_EXP

- P1.8V_AUX
- P1.8V_AUX
- P1.8V_AUX
- P1.8V_AUX

- P3.3V_EXP

- P3.3V_MCD

- P5.0V_ALW

- P5.0V_AUD

- P5.0V_AMP

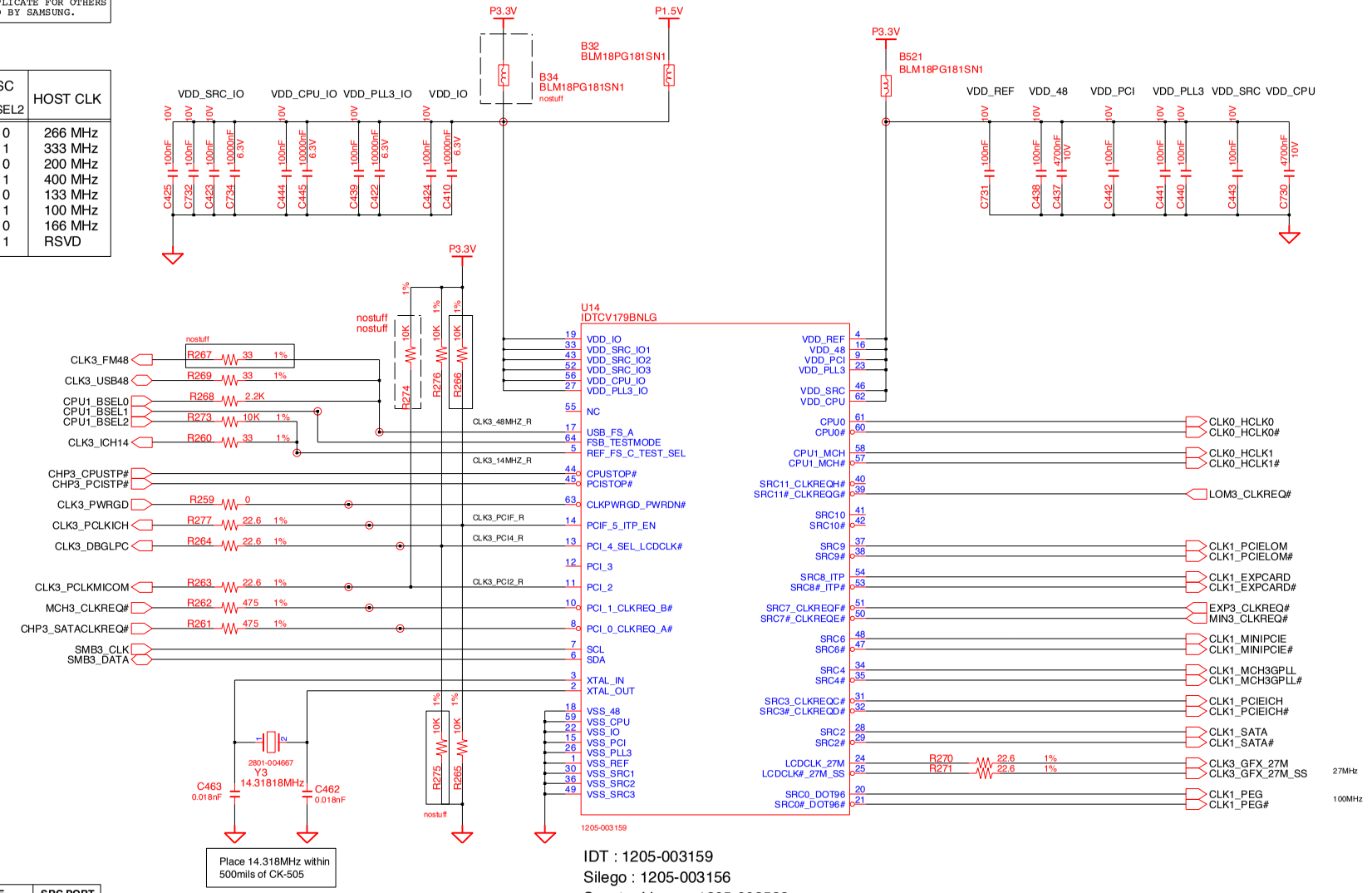
- P5.0V_AUX_USB

TP2506 EGFX_CORE
TP2507 EGFX_CORE
TP2508 EGFX_CORE
TP2504 EGFX_CORE

TP2505 P1.8V
TP2502 P1.8V
TP2503 P1.8V
TP2509 P1.8V

DESIGN: TERMI	DATE: 1/10/2008	TITLE: LYON_External TP UNDEFINED	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 19 OF 19	

FSA BSEL0	FSB BSEL1	FSC BSEL2	HOST CLK
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD



IDT : 1205-003159
Silego : 1205-003156
Spectra Linear : 1205-003533

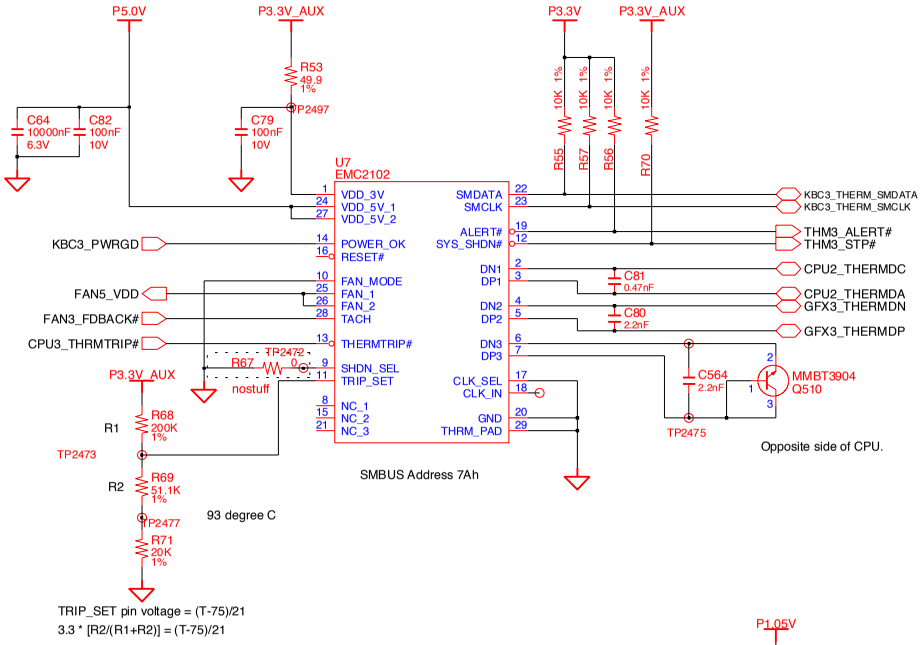
This part is 64pin QFN package.

CLK REQ	DEVICE	SRC PORT
CLK REQ A	SATA	SRC2
CLK REQ B	GMCH	SRC4
CLK REQ E	MINI CARD	SRC6
CLK REQ F	LOM3_CLKREQ#	SRC8

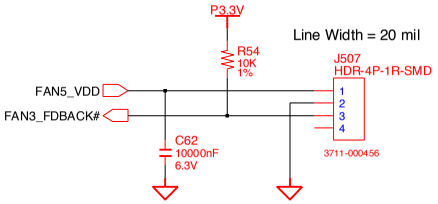
SEL_LCDCLK*	Pin 20/21	Pin 24/25
LOW	DOT_96/DOT_96#	PEG_CLK/PEG_CLK#
HIGH	SRC_0/SRC_0#	27M & 27M_SS

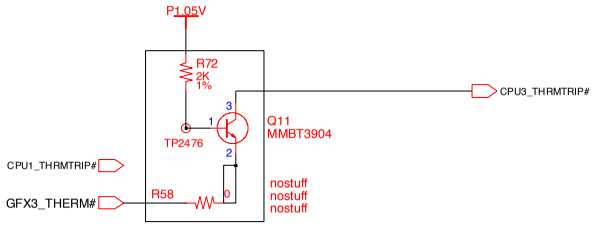
DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External Main_Clock_Circuit CK_Clock_505M	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE: undefined	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 21 OF 64	

THERMAL SENSOR & FAN CONTROL

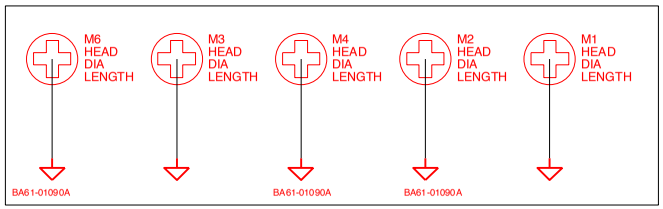


10mil width and 10mil spacing.



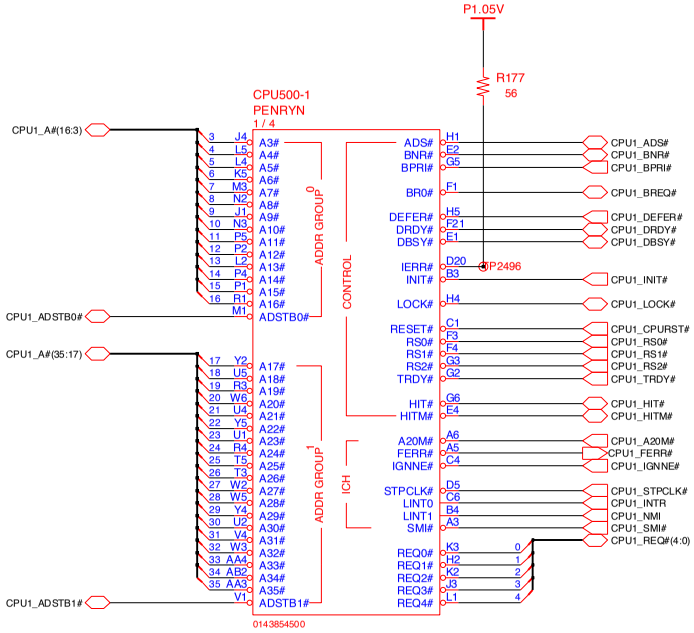


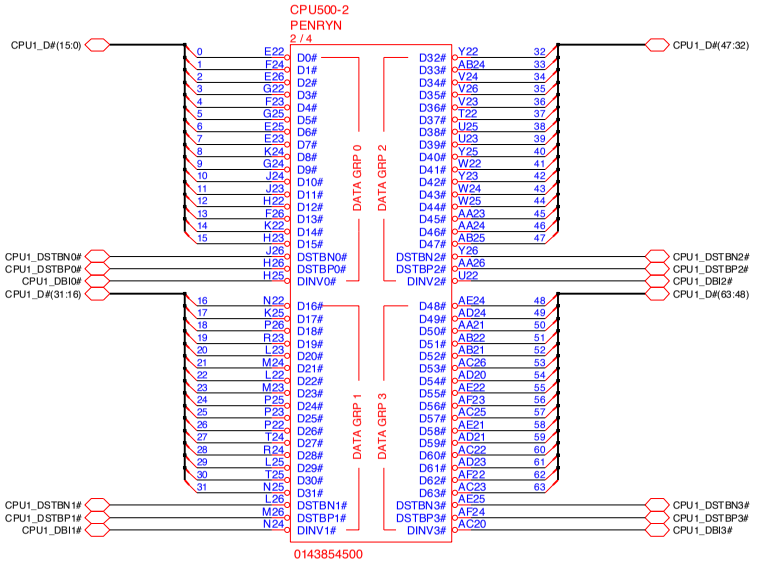
RHE Support (Top)



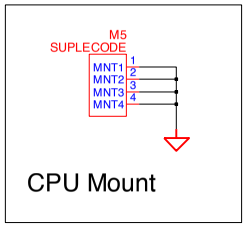
M6
Internal : nostuff
External : stuff

DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP	Thermal_Sensor_SMSC_Emc2102	
APPROVAL: SJ PARK	REV: 1.0	Thermal_Sensor_SMSC_Emc2102	PART NO.: BA41-00920A
MODULE CODE	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 61 OF 64	

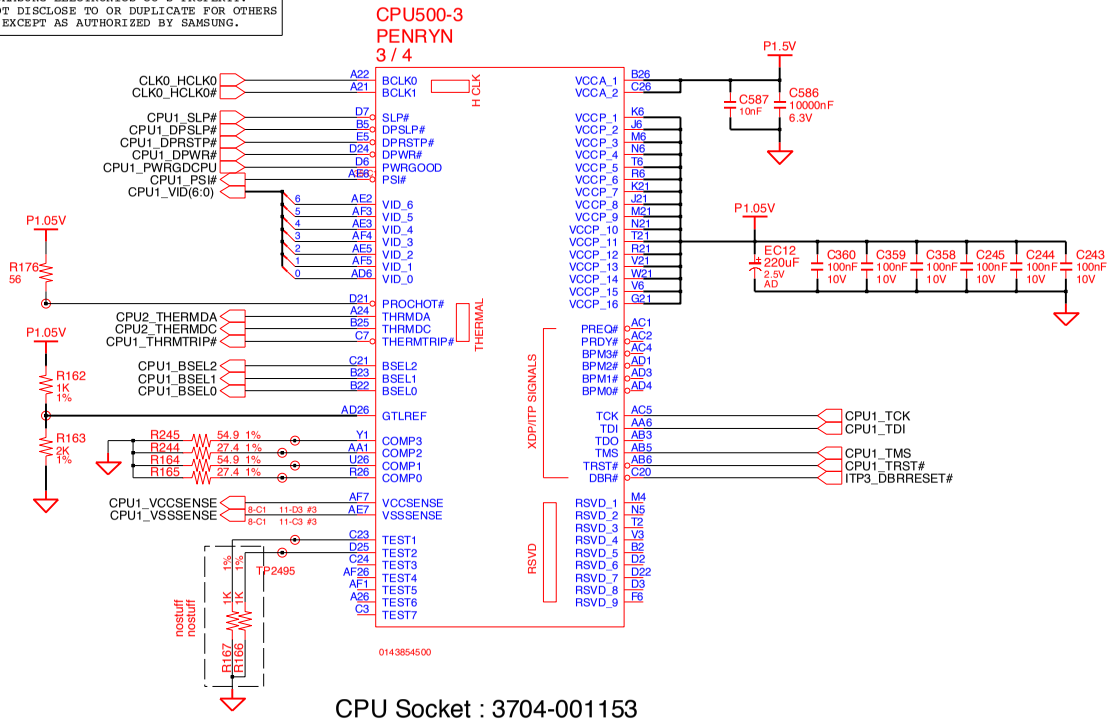




CPU Socket : 3704-001153

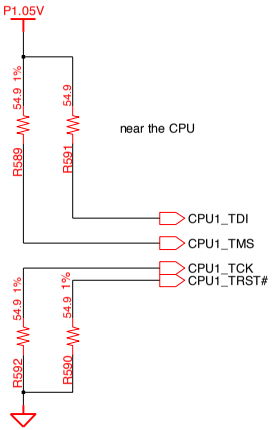


DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External CPU PENRYN (1/3)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00920A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE: undefined	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 22 OF 64	



CPU Socket : 3704-001153

FSC	FSB	FSA	FRQ
0	0	0	266M
0	1	0	200M
0	1	1	166M



CPU Core Voltage Table

IMVP-6

Active Mode VID(6:0)	Voltage	Active/Deeper Sleep Dual Mode Region VID(6:0)	Voltage	Deeper Sleep/Extended Deeper Sleep Dual Mode Region VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 0 1 1 1 1	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 0 1 1 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 0 1 1	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 0	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 0 1 1 1	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 0 1 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 1 1 1 1	0.5125 V	1 1 1 1 0 0 0	0.0000 V
		1 0 1 0 0 0 0	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V

Active

DPRSLPVR 0
DPRSTP* 1
PSI2* 0 or 1

Deeper Slp

DPRSLPVR 1
DPRSTP* 0
PSI2* 0 or 1

*"1111111" : 0V power good asserted.

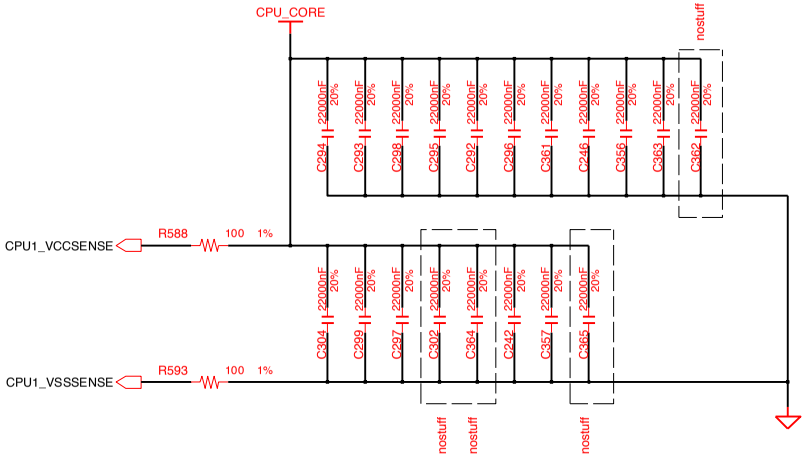
*Yonah Processor (2.33 GHz / 800 MHz : TBD)

GTLREF : Keep the Voltage divider within 0.5" of the first GTLREF0 pin with Zo=55ohm trace. Minimize coupling of any switching signals to this net.

COMP0,2(COMP1,3) should be connected with Zo=27.4ohm(55ohm) trace shorter than 1/2" to their respective Banias socket pins.

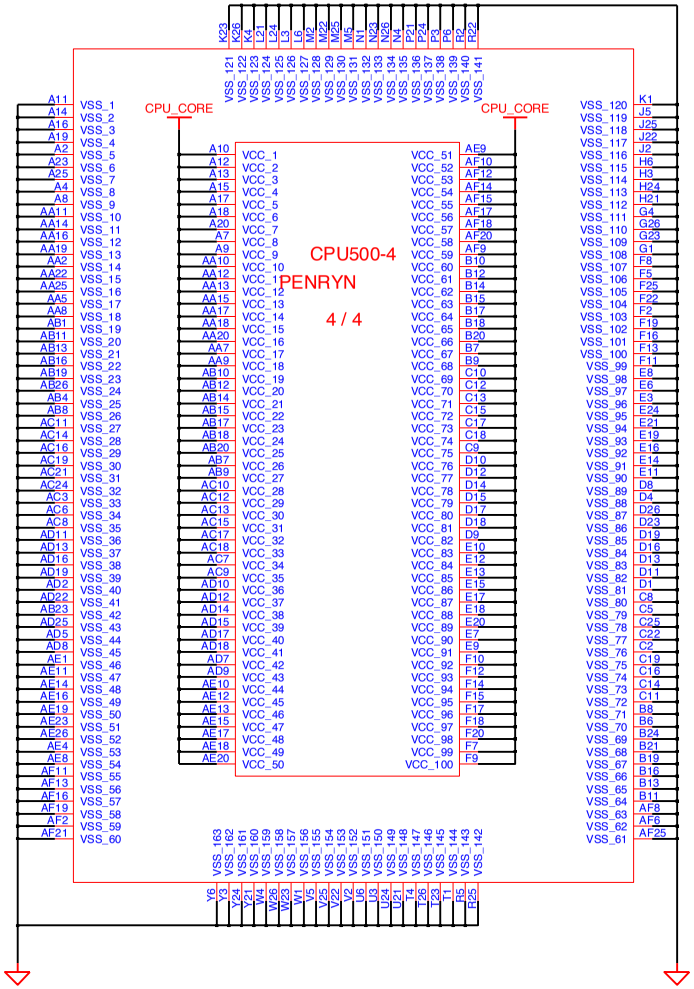
GND test points within 100mil of the VCC/VSSsense at the end of the line. Route the VCC/VSSsense as a Zo=55ohm traces with equal length. Observe 3:1 spacing b/w VCC/VSSsense lines and 25mil away (preferred 50mil) from any other signal. And GND via 100mil away from each of the VCC/VSS test point vias.

DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External CPU PENRYN (2/3)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE: undefined	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 23 OF 64	

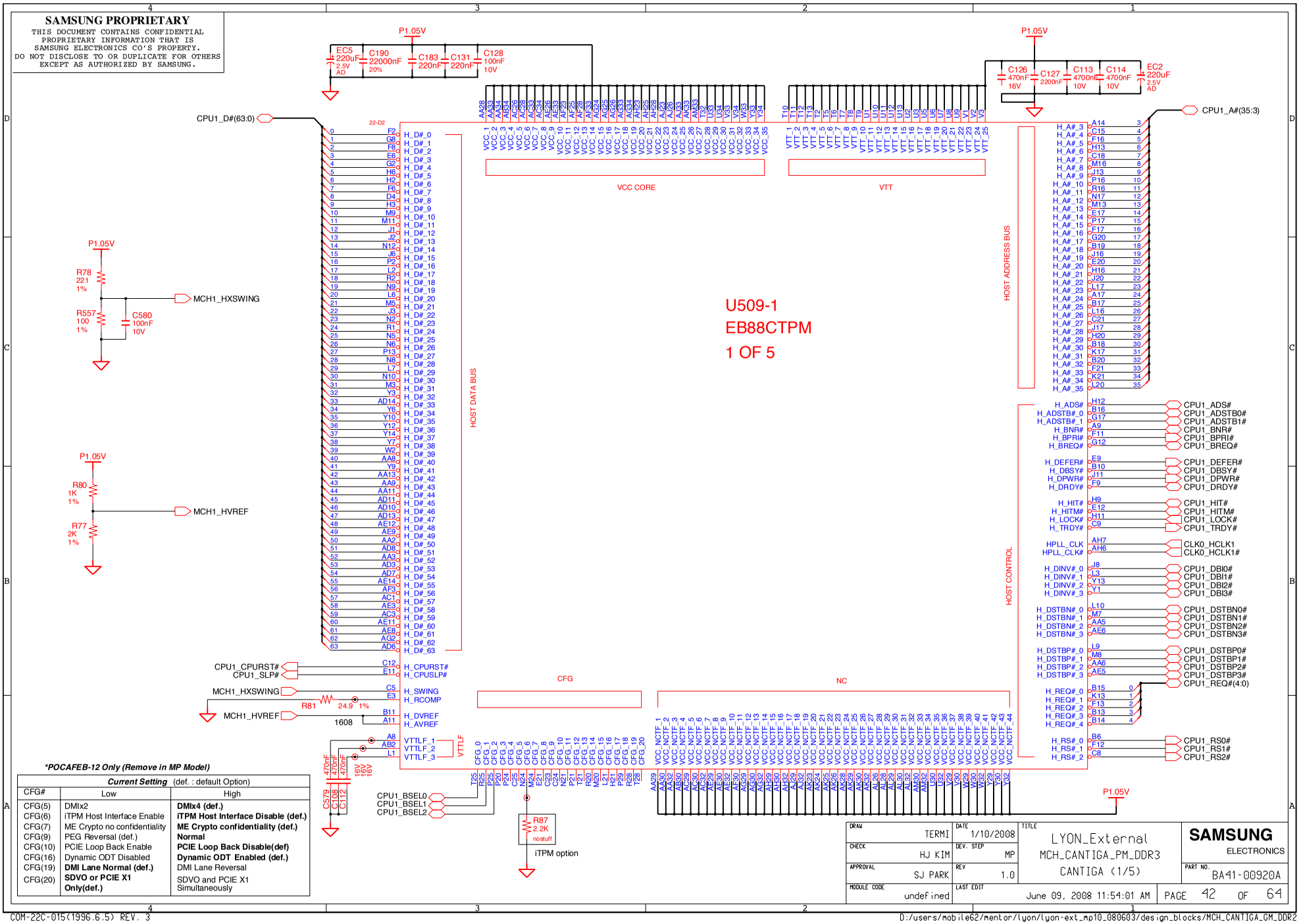


6x 330 uF : CPU VR side

CPU Socket : 3704-001153



DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External CPU PENRYN (3/3)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE: undefined	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 24 OF 64	



POCAFEB-12 Only (Remove in MP Model)

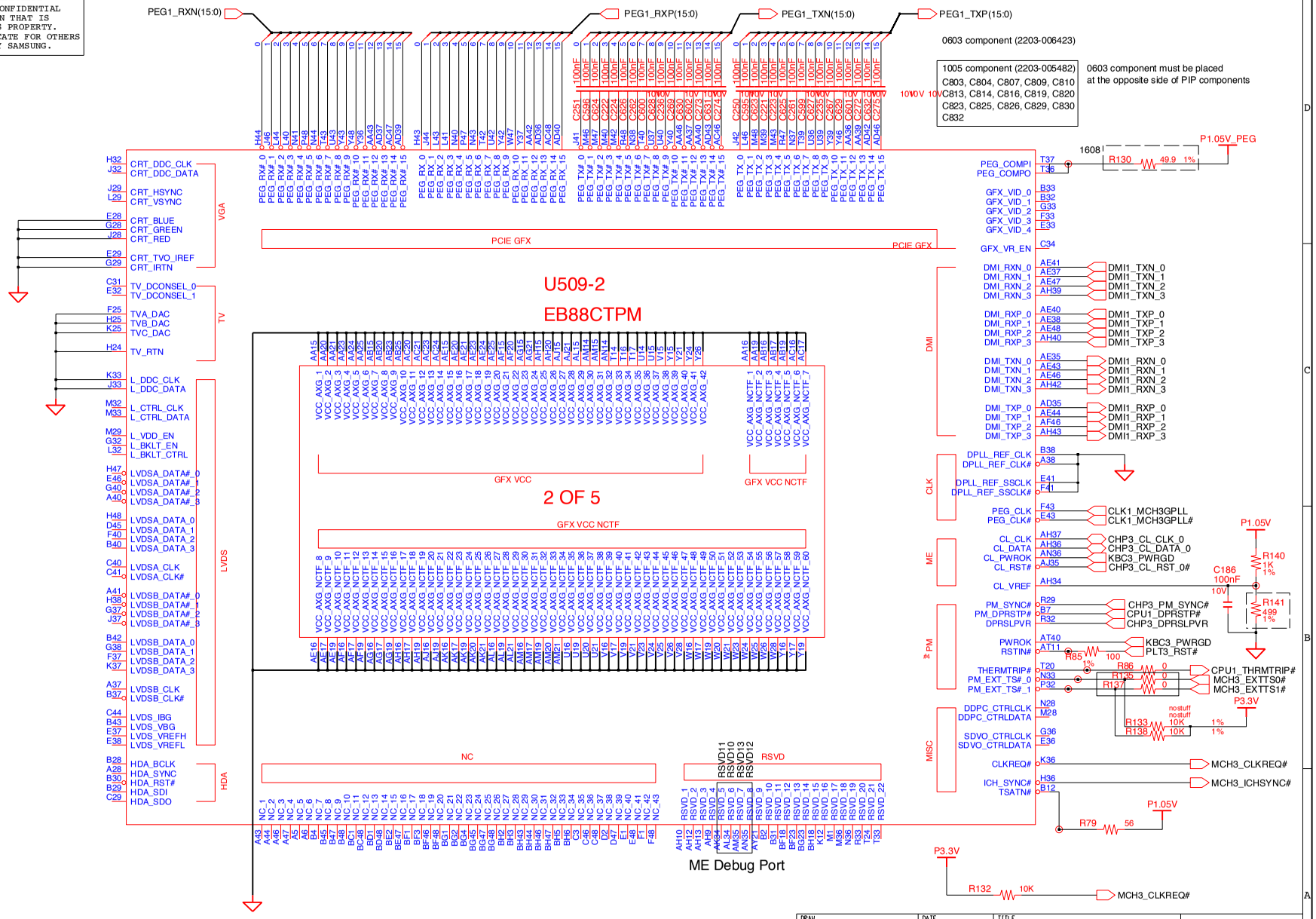
Current Setting (def. : default Option)		
CFG#	Low	High
CFG(5)	DMIx2	**DMIx4 (def.)**
CFG(6)	iTPM Host Interface Enable	**iTPM Host Interface Disable (def.)**
CFG(7)	ME Crypto no confidentiality	**ME Crypto confidentiality (def.)**
CFG(9)	PEG Reversal (def.)	**Normal**
CFG(10)	PCIE Loop Back Enable	**PCIE Loop Back Disable(def)**
CFG(16)	Dynamic ODT Disabled	**Dynamic ODT Enabled (def.)**
CFG(19)	**DMI Lane Normal (def.)**	DMI Lane Reversal
CFG(20)	**SDVO or PCIE X1 Only(def.)**	SDVO and PCIE X1 Simultaneously

DRAW	TERMI	DATE	1/10/2008
CHECK	HJ KIM	DEV. STEP	MP
APPROVAL	SJ PARK	REV	1.0
MODULE CODE	undefined	LAST EDIT	June 09, 2008 11:54:01 AM

TITLE: LYON_External MCH_CANTIGA_PM_DDR3 CANTIGA (1/5)

SAMSUNG ELECTRONICS

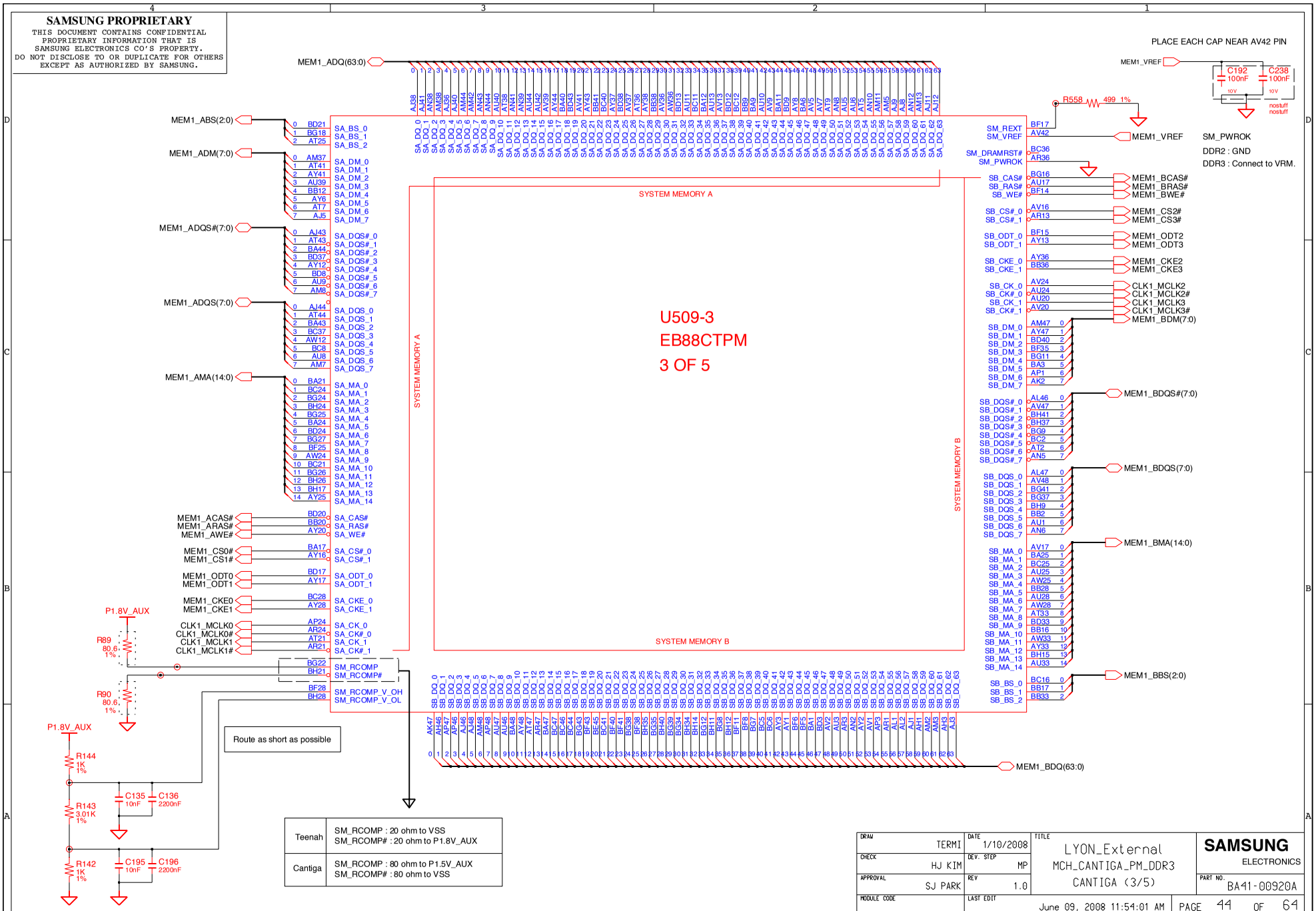
PART NO. BA41-00920A



DRAW	TERMI	DATE	1/10/2008	TITLE	LYON_External MCH_CANTIGA_PM_DDR3 CANTIGA (2/5)
CHECK	HJ KIM	DEV. STEP	MP		
APPROVAL	SJ PARK	REV	1.0		
MODULE CODE	undefined	LAST EDIT	June 09, 2008 11:54:01 AM	PAGE	43 OF 64

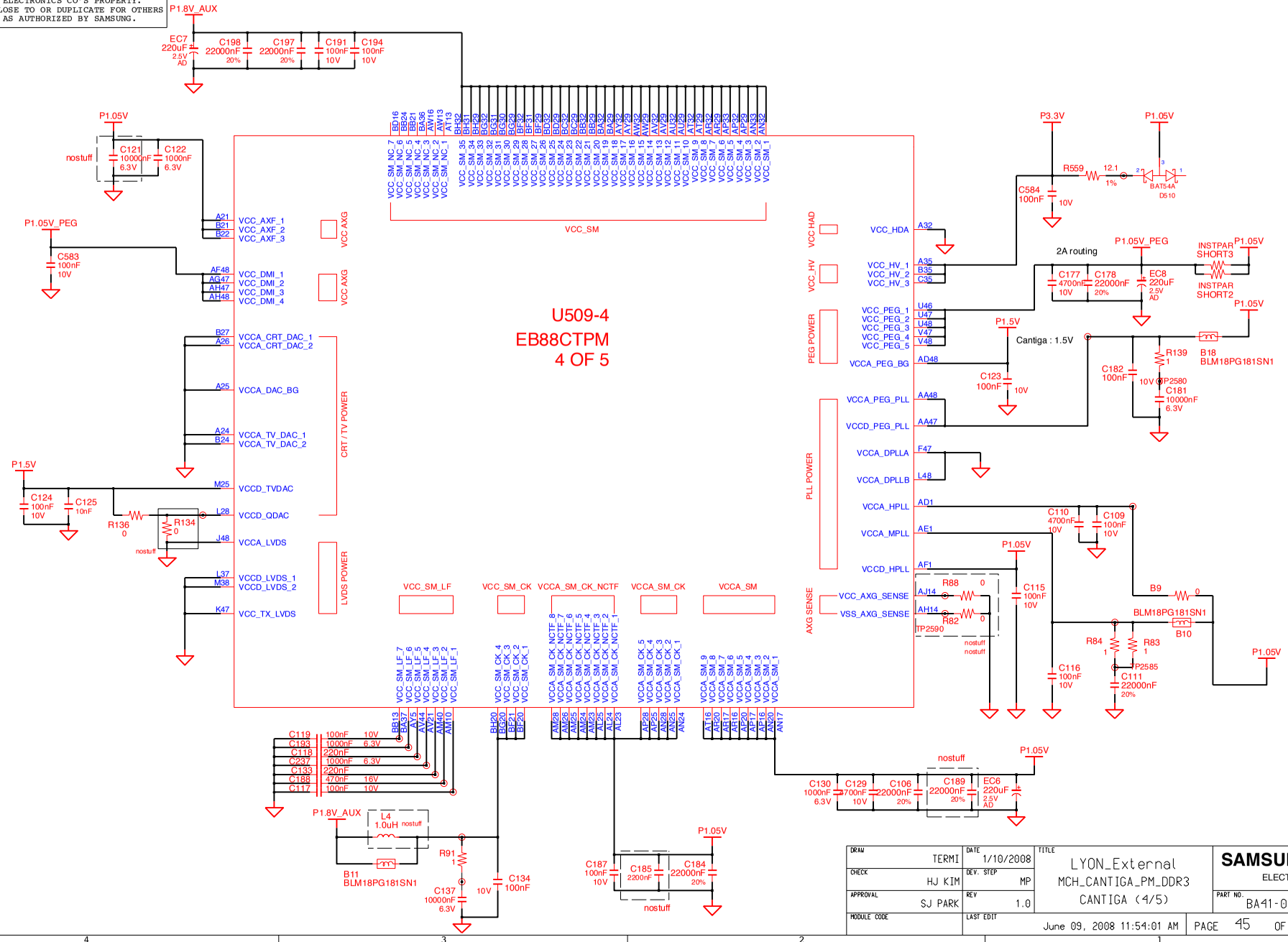
SAMSUNG ELECTRONICS

PART NO. BA41-00920A

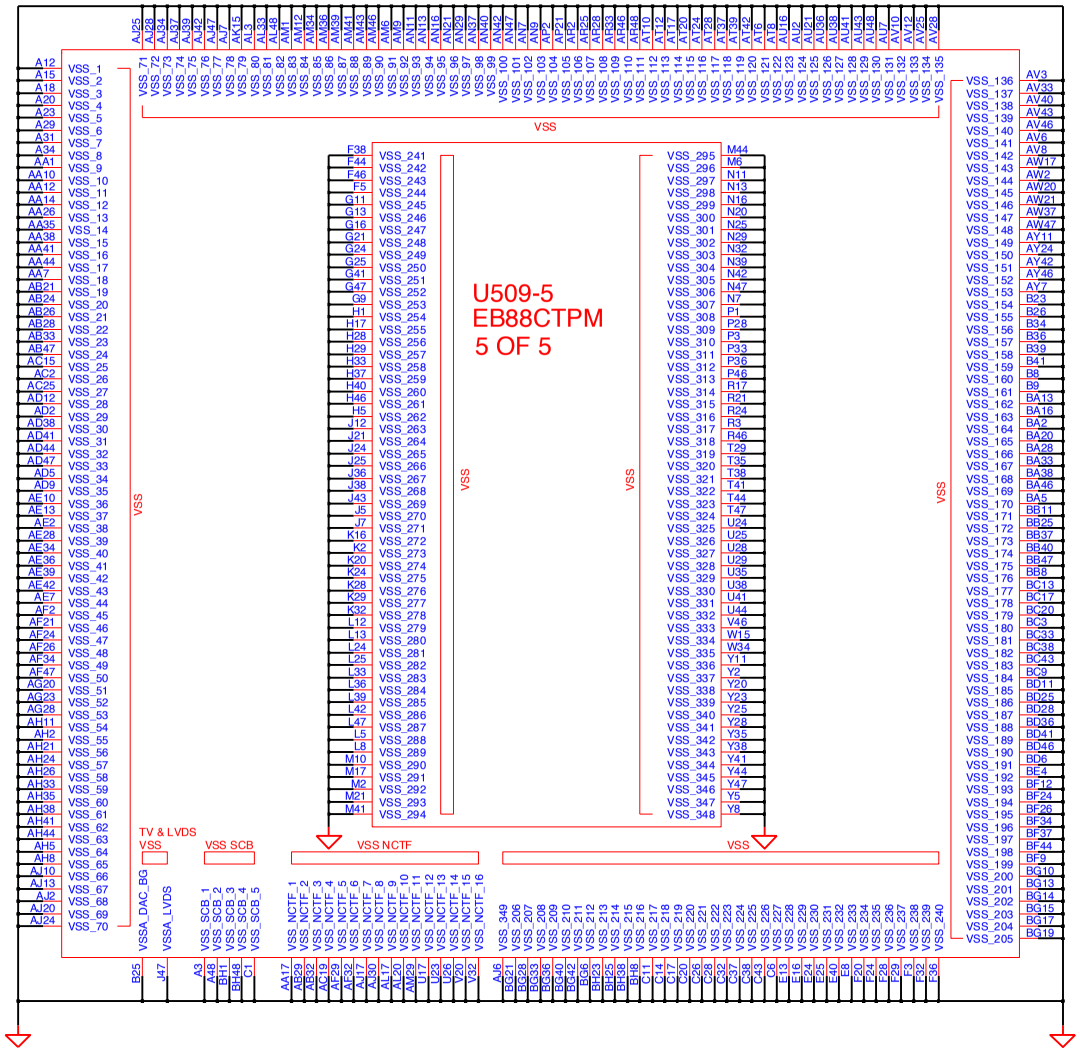


Teenah	SM_RCOMP : 20 ohm to VSS SM_RCOMP# : 20 ohm to P1.8V_AUX
Cantiga	SM_RCOMP : 80 ohm to P1.5V_AUX SM_RCOMP# : 80 ohm to VSS

DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External MCH_CANTIGA_PM_DDR3 CANTIGA (3/5)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00920A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 44 OF 64	



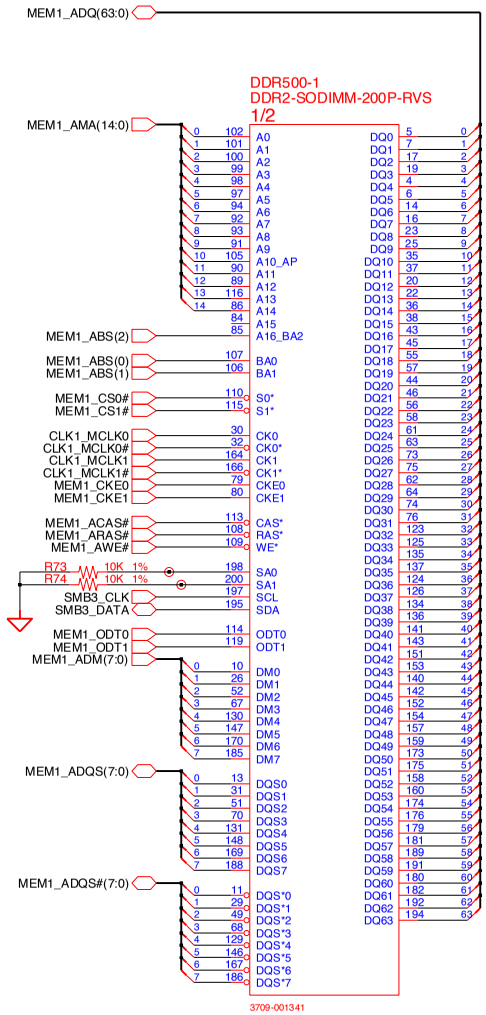
DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External MCH_CANTIGA_PM_DDR3 CANTIGA (4/5)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 45 OF 64	



DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External MCH_CANTIGA_PM_DDR3 CANTIGA (5/5)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 46 OF 64	

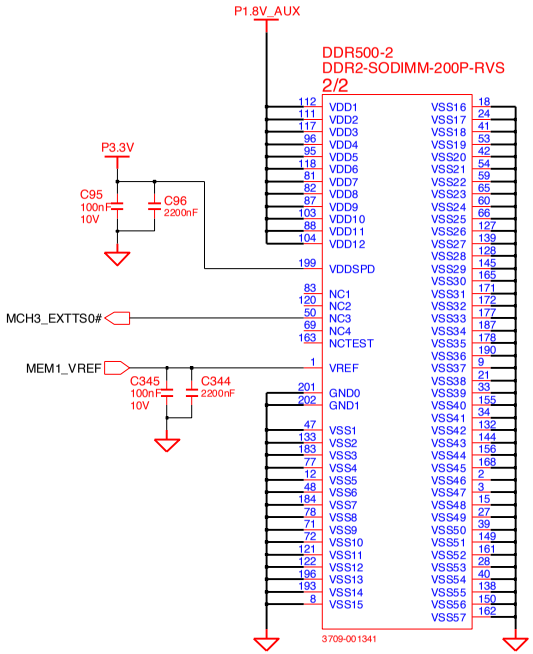
DDR SO-DIMM #0

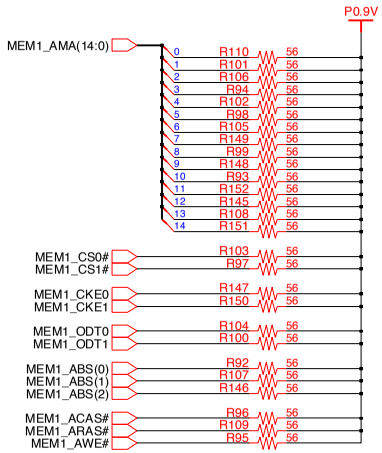
Height : 5.2mm (Reverse)



Tyco/Foxcn : 3709-001341
Suyin : 3709-001502

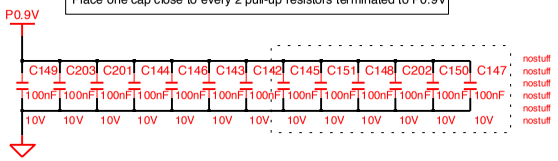
ME POWER RAIL UNDER ME ENABLE



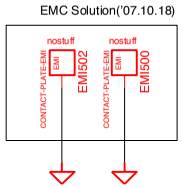


Place one cap close to every 2 pull-up resistors terminated to P0.9V

Place one cap close to every 2 pull-up resistors terminated to P0.9V

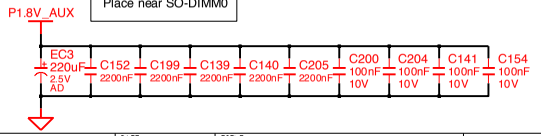


EMC Solution('07.10.18)



ME POWER RAIL UNDER ME ENABLE

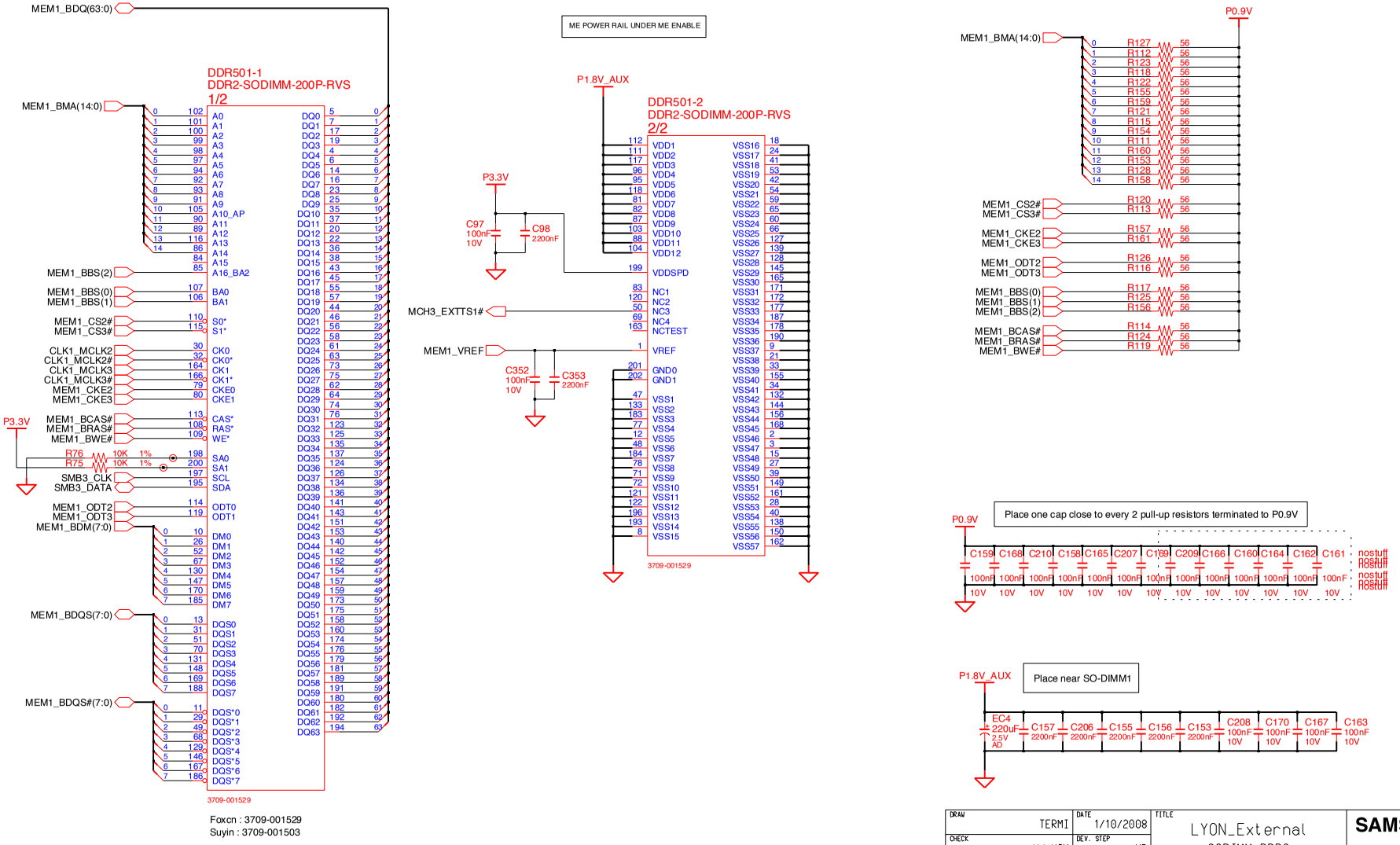
Place near SO-DIMM0



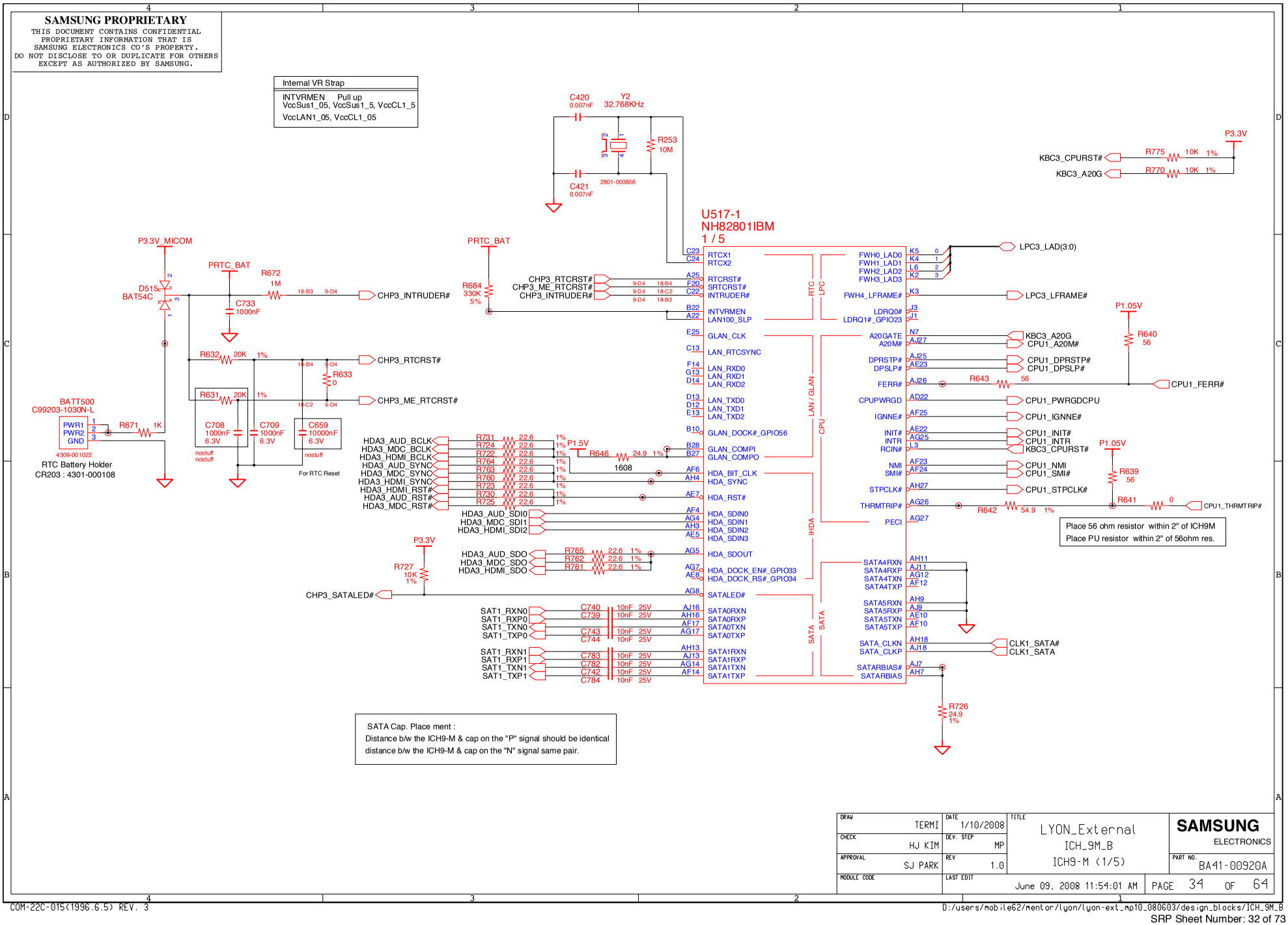
DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External SODIMM_DDR2 SODIMM_DDR2 #1	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 58 OF 64	

DDR SO-DIMM #1

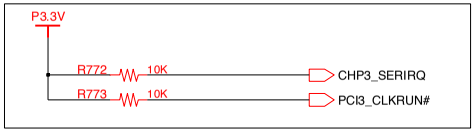
Height : 9.2mm (Reverse)



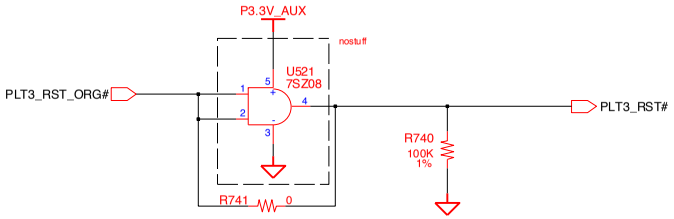
DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External SODIMM_DDR2 SODIMM_DDR2 #2	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00920A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 59 OF 64	

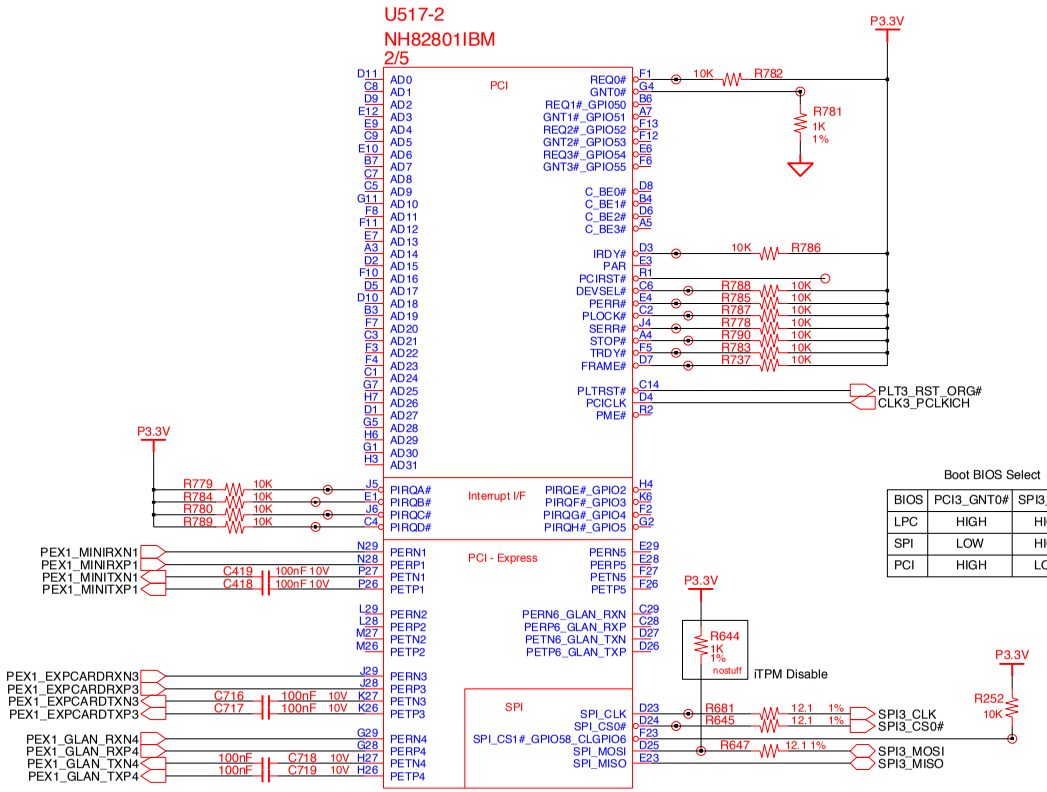


DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External ICH_9M_B ICH9-M (1/5)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 34 OF 64	



LPC option ; These are used with LPC



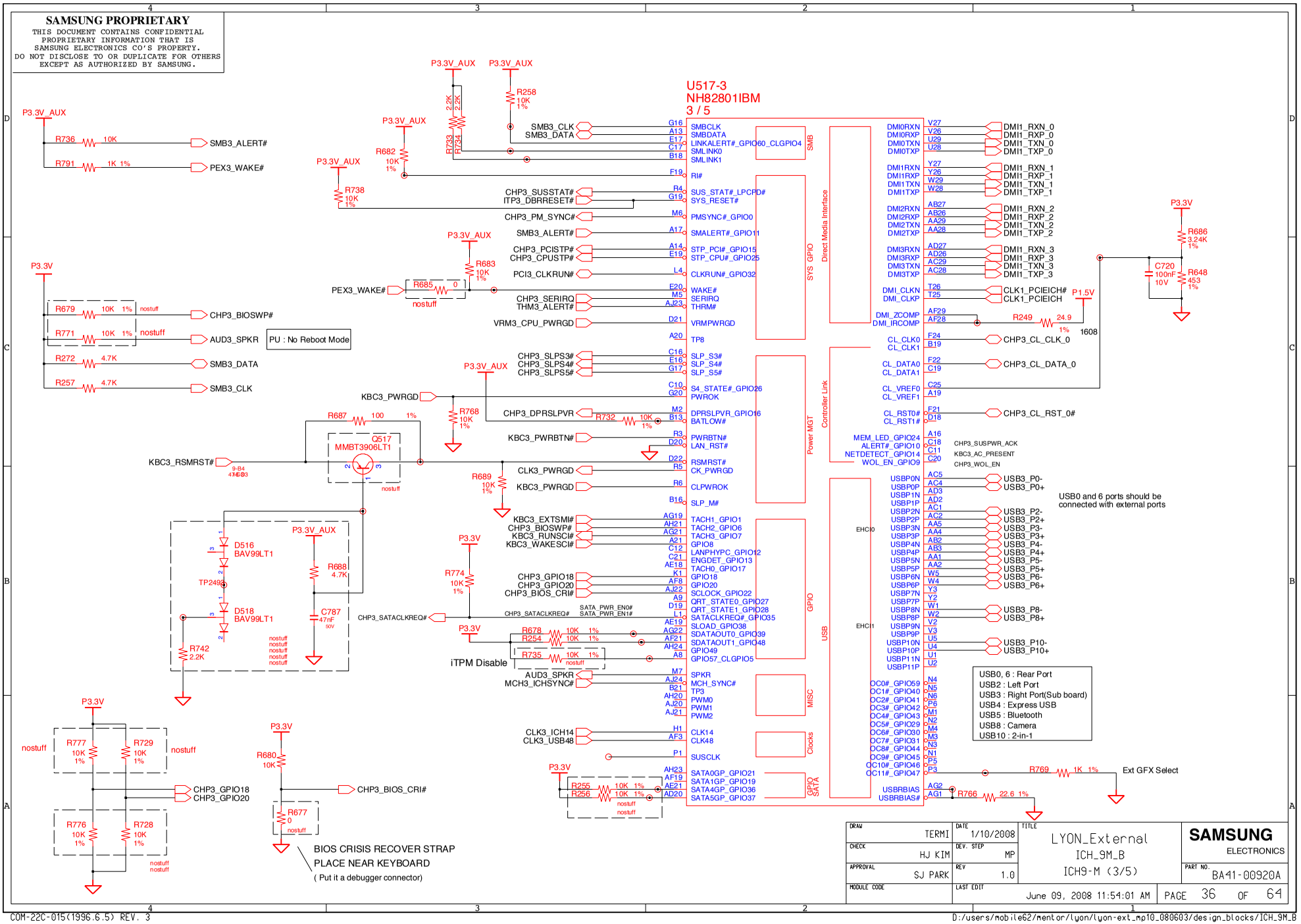


Boot BIOS Select

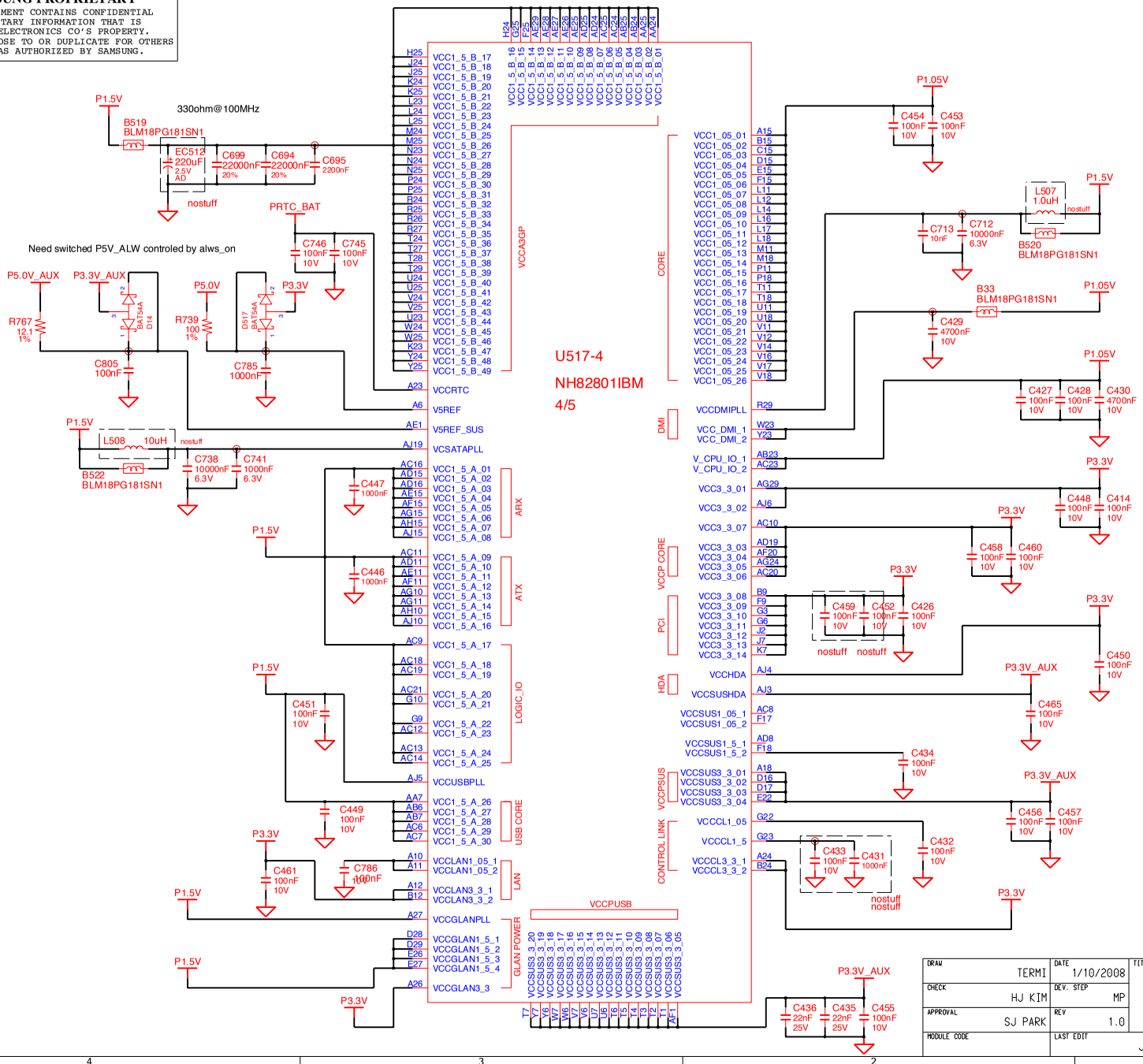
BIOS	PCI3_GNT0#	SPI3_CS1#
LPC	HIGH	HIGH
SPI	LOW	HIGH
PCI	HIGH	LOW

AC caps : PCIE need to be within 250mils of the driver
Resistor for Test : Place Stuffing Option to minimize stubs

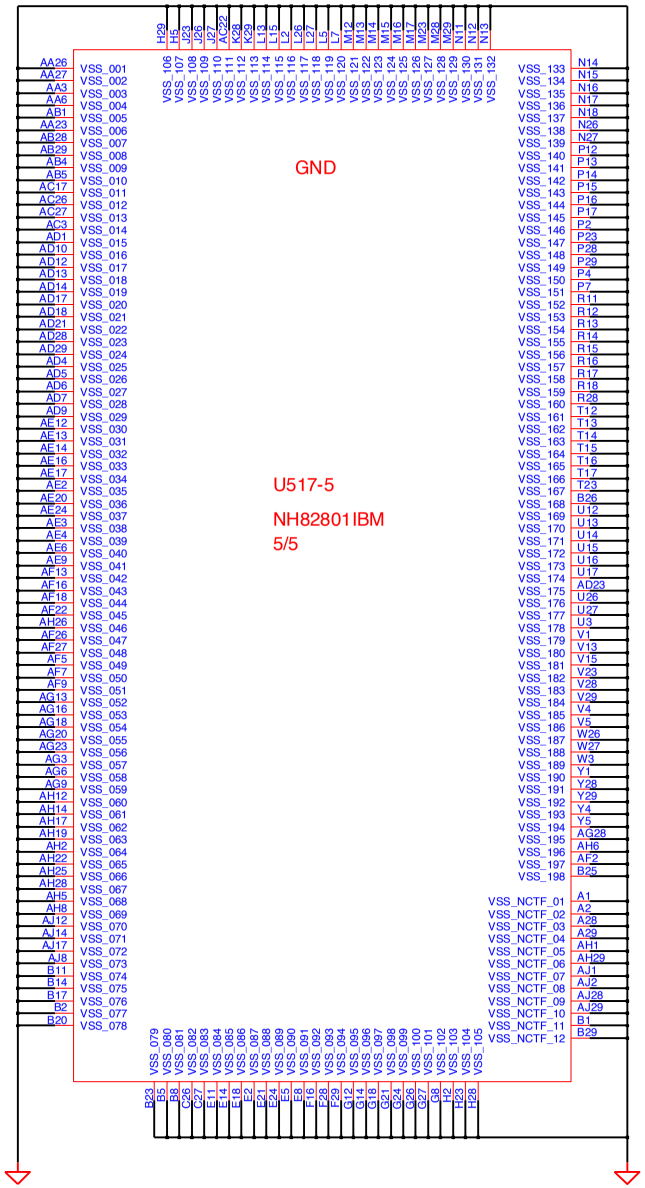
DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External ICH_9M_B ICH9-M (2/5)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE: undefined	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 35 OF 64	



DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External ICH_9M_B ICH9-M (3/5)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 36 OF 64	

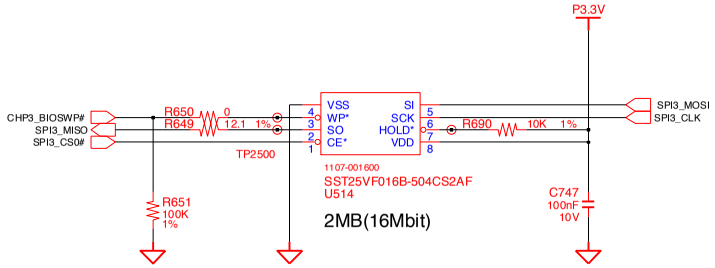


DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External ICH_9M_B ICH9-M (3/5)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00920A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 37 OF 64	



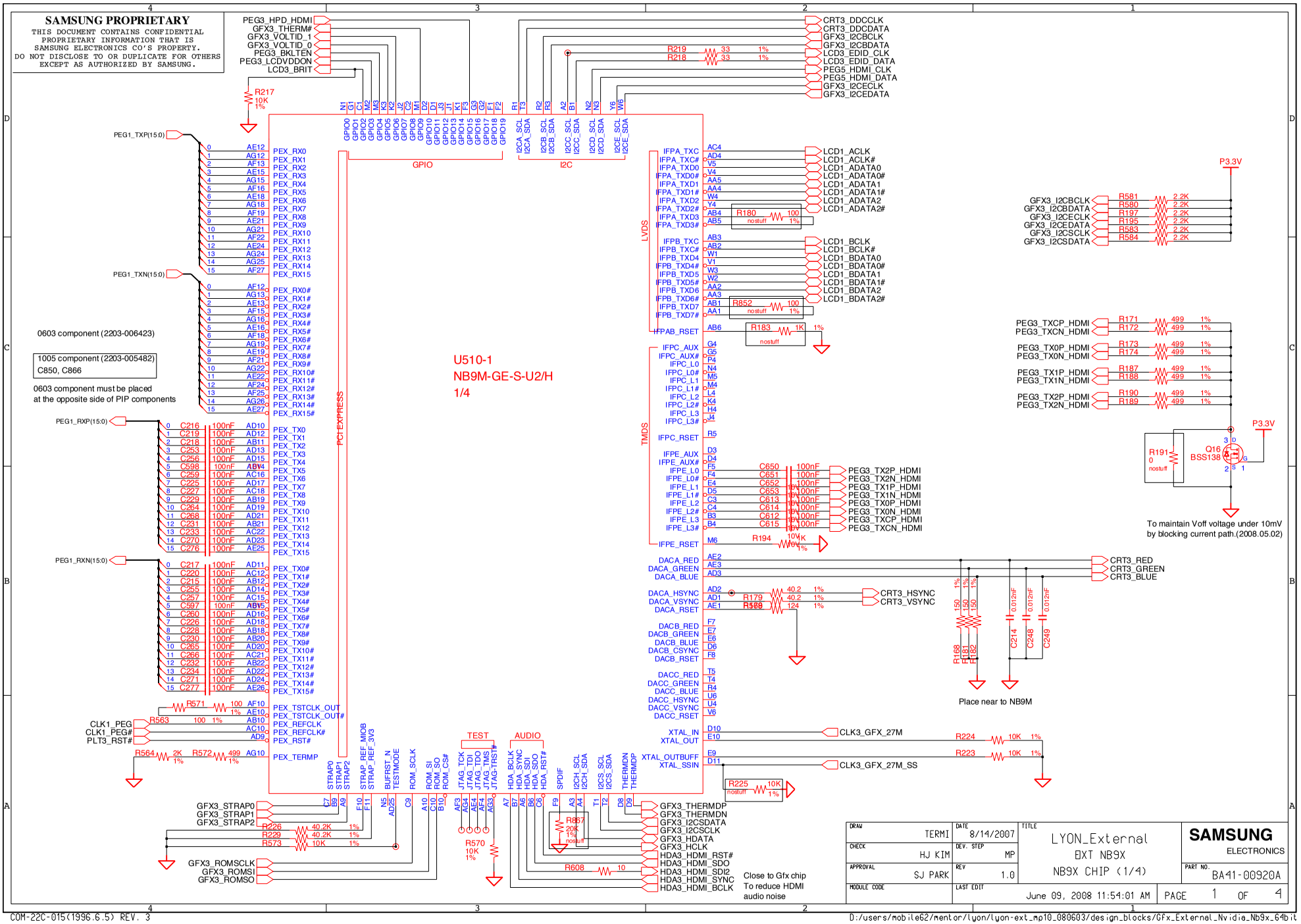
DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External ICH_9M_B ICH9-M (5/5)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00920A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 38 OF 64	

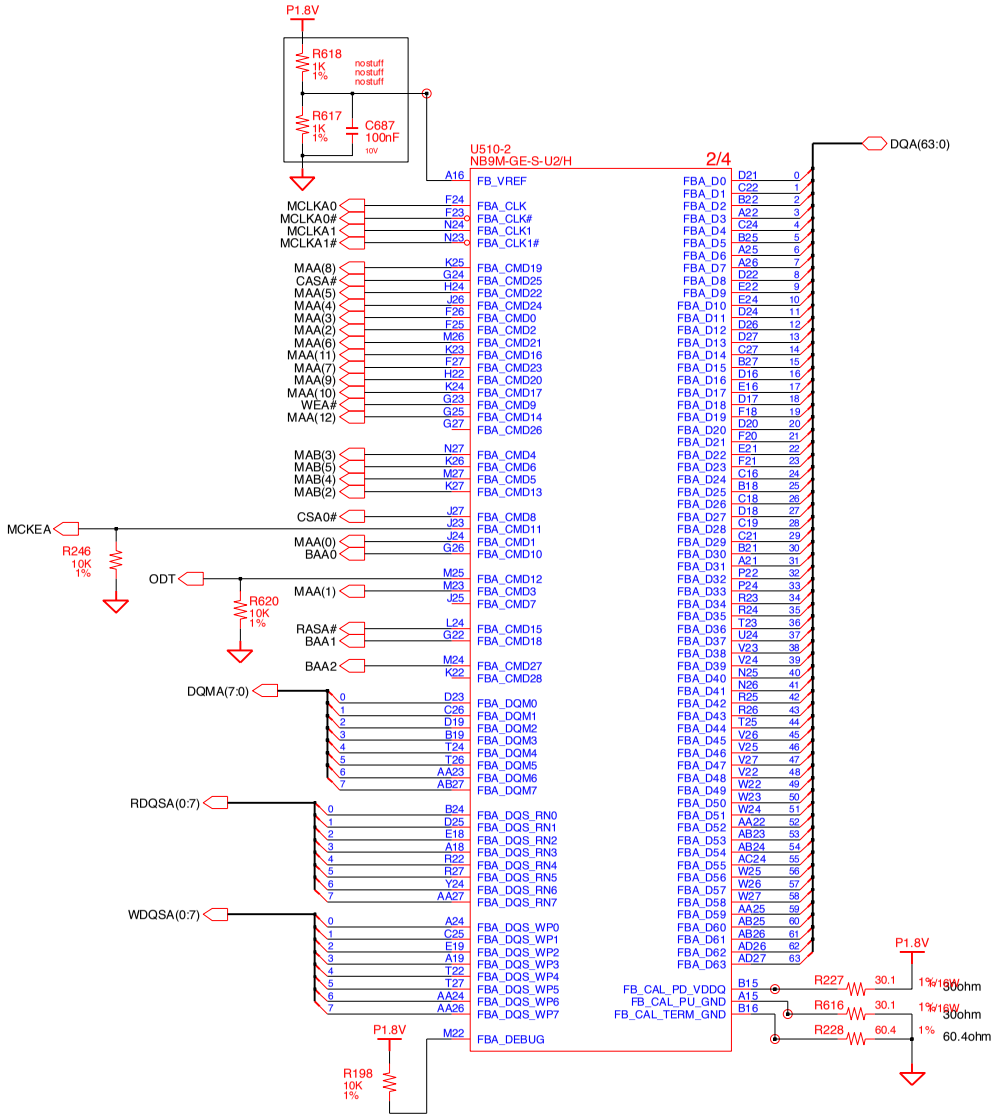
- SPI ROM LIST -



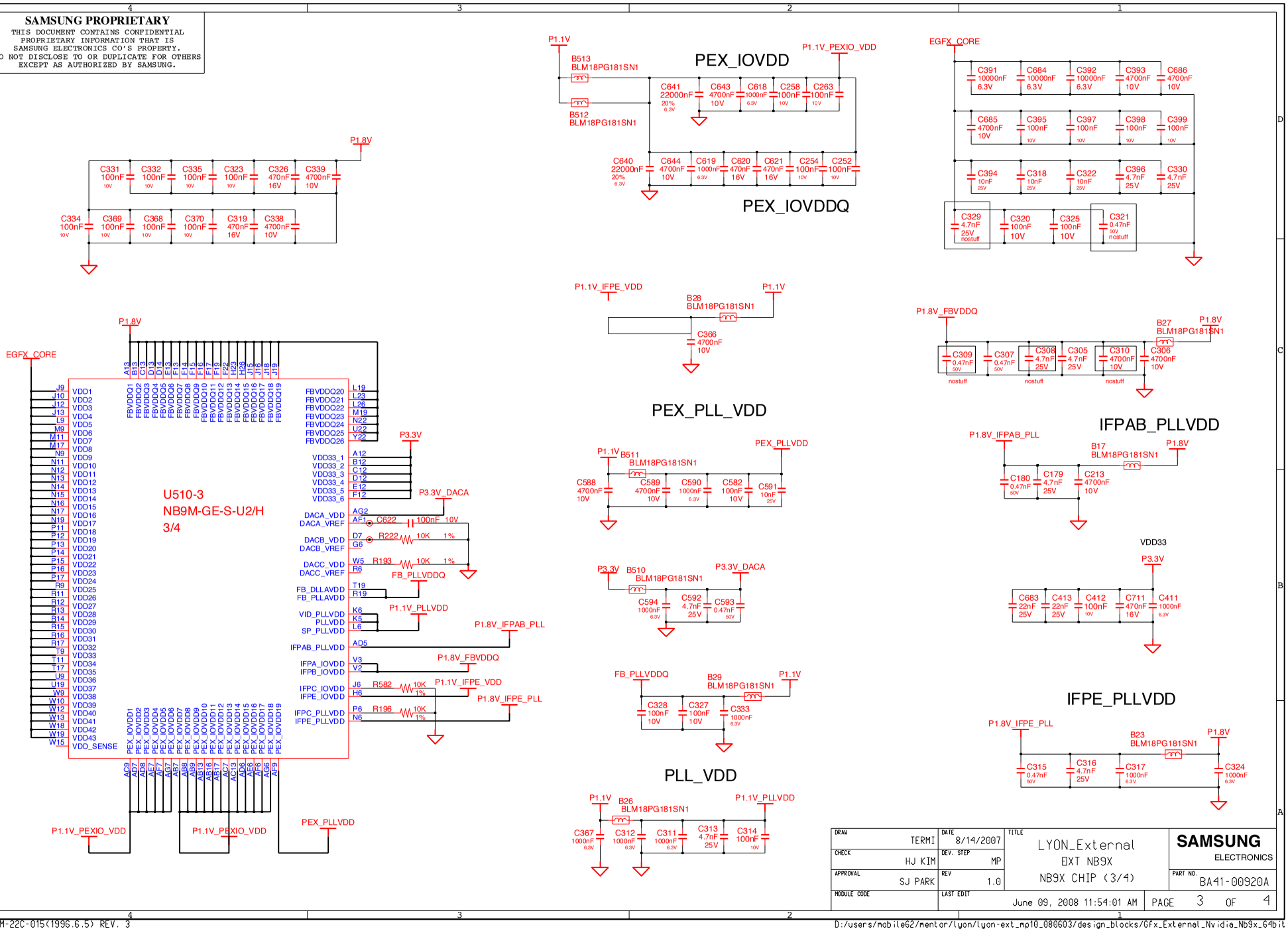
02 VERIFY REAL MODE	66 CONFIGURE ADVANCE CACHE REG.
03 DISABLE NMI	6A DISPLAY EXTERNAL CACHE SIZE
04 GET CPU TYPE	6C DISPLAY SHADOW MESSAGE
06 INIT. SYSTEM H/W	6E DISPLAY NON-DISPOSABLE SEGMENT
08 INIT. CHIPSET REG.	70 DISPLAY ERROR MESSAGE
09 SET IN POST FLAG	72 CHECK FOR CONFIGURATION ERROR
0A INIT CPU.REG	74 TEST REAL-TIME CLOCK
0B CPU CACHE ON	76 CHECK FOR KEYBOARD EERROR
0C INIT.CACHE TO POST	7C SETUP HARDWARE INTERRUPT VECTOR
OE INIT. I/O VALUE	7E TEST COPROCESSER IF PRESENT
0F ENABLE THE L-BUS IDE	80 DISABLE ON-BOARD I/O PORT
10 INIT. POWER MANAGER	82 DETECT AND INSTALL EXT.RS232C
11 LOAD ALTERNATE REG.	84 DETECT AND INSTALL EXT.PARALLEL
13 PCI BUS MASTER RESET WITH INITIAL POST VALUE	86 RE-INIT. ON-BOARD I/O PORT
	88 INIT. BIOS DATA ROM
14 INIT. KEYBOARD CONTROLLER	8A INIT.EXTENDED BIOS DATA AREA
16 CHECK CHECKSUM	8C INIT. FDD CONTROLLER
18 8254 TIMER INIT.	9A SHADOW OPTION ROMS
1A 8237 DMA CONTROLLER INIT.	9C SETUP POWER MANAGEMENT
1C RESET INTERRUP CONTROLLER	9E ENABLE H/W INTERRUPT
20 TEST DRAM REFRESH	A0 SET TIME OF DAY
22 TEST 8742 KEYBOARD CONTROLLER	A4 INIT. TYPEMATIC RATE
24 SET ES SEGMENT REG. TO 4GB	A8 ERASE F2 PROMPT
26 ENABLE A20	AA SCAN FOR F2 KEY STROKE
28 AUTO SIZING DRAM	AC ENTER SETUP
32 COMPUTE THE CPU SPEED	AE CLEAR IN POST FLAG
34 TESET CMOS RAM	B0 CHECK FOR ERRORS
38 SHADOW SYSTEM BIOS ROM	B2 POST DONE-PREPARE TO BOOT O/S
3A AUTO SIZING CACHE	B4 ONE BEEP
3C CONFIGURE ADVANCED CHIPSET REG.	B6 CHECK PASSWORD (OPTION)
3D LOAD ALTER REG. WITH CMOS VALUE	B7 ACPI INIT
42 INIT. INTERRUPT VECTOR	BA DMI INIT
44 INIT. BIOS INTERRUPT	BE CLEAR SCREEN
46 CHECK ROM COPYRIGHT NOTICE	C0 TRY BOOT WITH INT19
47 INIT. I20 SUPPORT IF INSTALLED	D0 INTERRUPT HANDLER ERROR
48 CHECK VIDEO CONFIGURE AGAINST CMOS	D2 UNKNOWN INTERRUPT ERROR
49 INIT. PCI BUS AND DEVICE	D4 PENDING INTERRUPT ERROR
4A INIT. ALL VIDEO BIOS ROM	D6 SHUTDOWN 5
4C SHADOW VIDEO BIOS ROM	D8 SHUTDOWN ERROR
50 DISPLAY CPU TYPE AND SPEED	DA EXTENDED BLOCK MOVE
52 TEST KEYBOARD	DC SHUTDOWN 10
54 SET KEYCLICK IF ENABLED	89 ENABLE NMI
56 ENABLE KEYBOARD	90 INIT. HDD CONTROLLER
58 TEST FOR UNEXPECTED INTERRUPTS	91 INIT. LOCAL BUS HDD CONTROLLER
5A DISPLAY " PRESS ..... SETUP"	92 JUMP TO USER PATCH 2
5C TEST RAM GETWEEN 512K AND 640K	94 DISABLE A20 ADDRESS LINE
60 TEST EXTENDED MEMORY	96 CLEAR HUGE ES SEGMENT REG.
62 TEST EXTENDED MEMORY ADDRESS LINE	98 SEARCH FOR OPTION ROMS
64 JUMP TO USER PATCH 1	

DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External SPI_BIOS_ROM SPI_BIOS_ROM	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 60 OF 64	





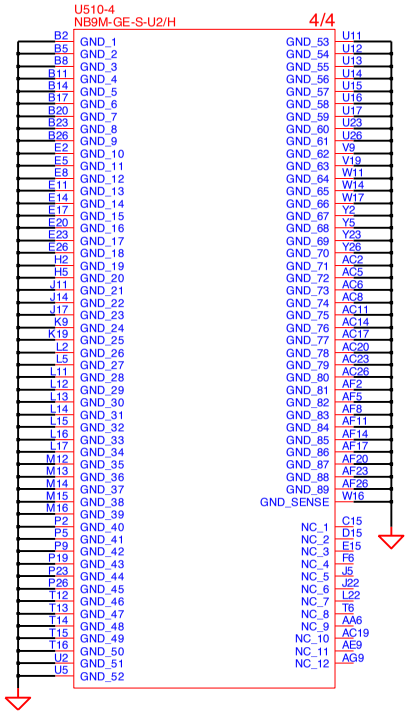
DRAW: TERMI	DATE: 8/14/2007	TITLE: LYON_External EXT NB9X NB9X CHIP (2/4)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 2 OF 4	



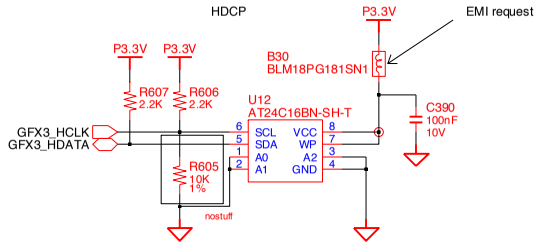
DRAW: TERMI	DATE: 8/14/2007	TITLE: LYON_External EXT NB9X NB9X CHIP (3/4)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 3 OF 4	

Pin	Description	Activate
GPIO(0)	DVI detect	High
GPIO(1)	TV detect	Low
GPIO(2)	PWM Brigtness control	High
GPIO(3)	LCD VDD on enable	High
GPIO(4)	Backlight on/off	High
GPIO(5)	GPU VID0	High = 1.0V, Low = 1.1V
GPIO(6)	GPU VID1	NC
GPIO(7)	GPU VID2 or Mem VID	NC
GPIO(8)	Thermal diode Alert	LOW
GPIO(9)	Fan control	NC
GPIO(10)	Memory VREF switch	NC
GPIO(11)	SLI Rater sync	HIGH
GPIO(12)	AC Power dection input	NC
GPIO(13)	Power supply control	NC
GPIO(14)	Power supply control	NC
GPIO(15)	HDMI Detect	High
GPIO(16)	DP Detect	High

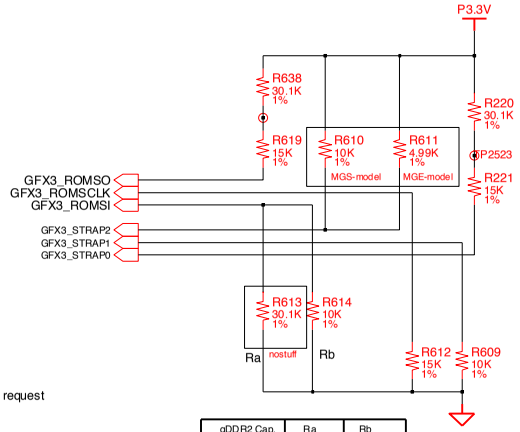
Strap option	Bit 3	Bit 2	Bit 1	Bit 0
ROM_SO	XCLK_27	TVMODE[2]	TVMODE[1]	TVMODE[0]
ROM_SCLK	DEVID[4]	VENID	CLK_CFG	PLL_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	DEVID[3]	DEVID[2]	DEVID[1]	DEVID[0]
STRAP1	PADCFG[3]	PADCFG[2]	PADCFG[1]	PADCFG[0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
Resistor value	PU to VDD	PD to GND	XCLK27 = 1 27MHz	
5K ohm	1000	0000	RAM CFG (SEC)	
10 Kohm	1001	0001	0011 512Mbit 0111 1Gbit	
15K ohm	1010	0010	USER[3:0]=1111 for EDID	
20K ohm	1011	0011	PADCFG[3:0]=0001 of NP	
25K ohm	1100	0100	NB9M-GS:0x06E9 (01001)	
30K ohm	1101	0101	NB9M-GE:0x06E8 (01000)	
35K ohm	1110	0110	NB9P-GS:0x0649 (01001)	
45K ohm	1111	0111	NB9P-GE:0x0406 (00110)	
			NB9P-GE2:0x0??? (0????)	



	Bit3	Bit2	Bit1	Bit0	
ROMSO	1	1	1	1	
SCLK	0	0	1	0	
SI	0	1	0	1	512Mbit (gDDR2)
	0	0	0	1	1Gb (gDDR2)
Strap2	1	0	0	1	9M-GS
	1	0	0	0	9M-GE
Strap1	0	0	0	1	
Strap0	1	1	1	1	



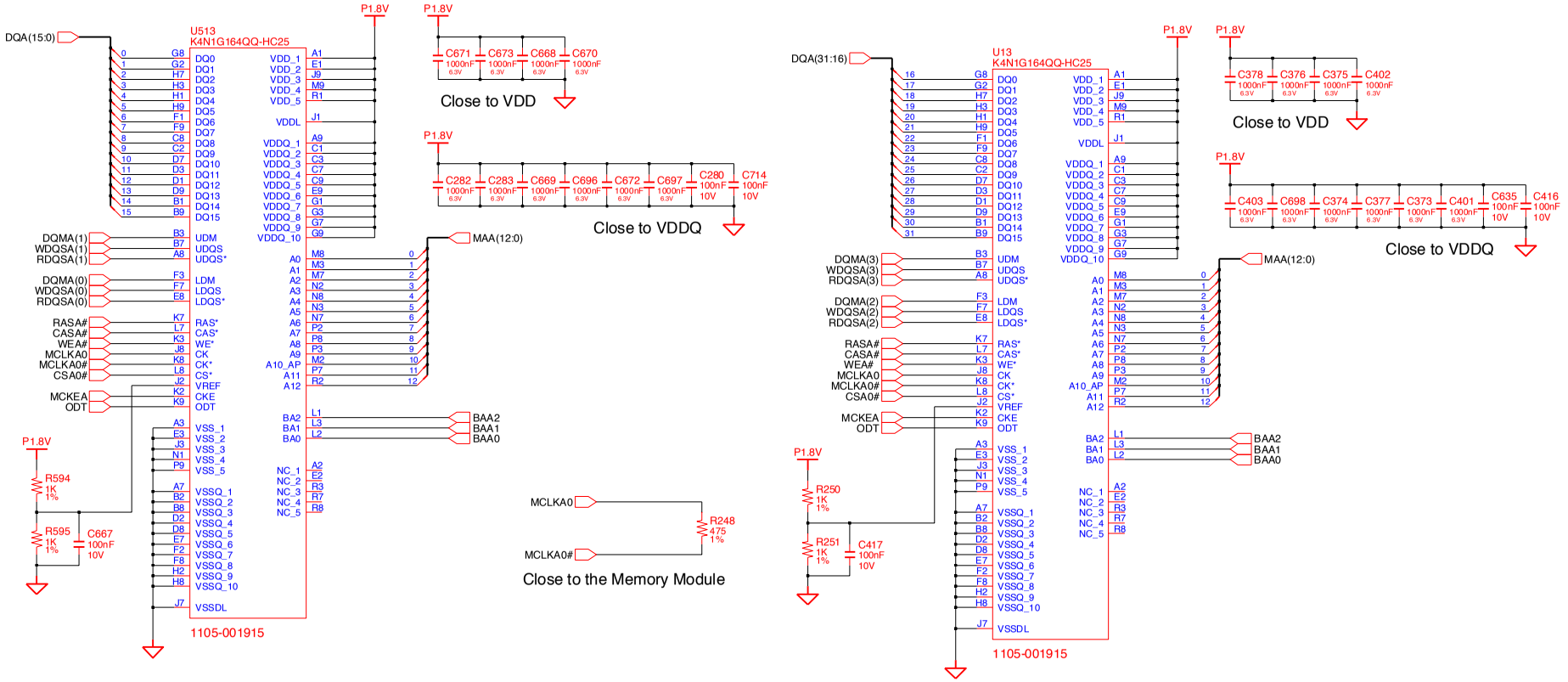
PU is for I2C ROM (AT24C16B, A0~A2 = 000)
PD is for Crypto ROM



gDDR2 Cap.	Ra	Rb
1Gbit	nostuff	stuff
512Mbit	stuff	nostuff

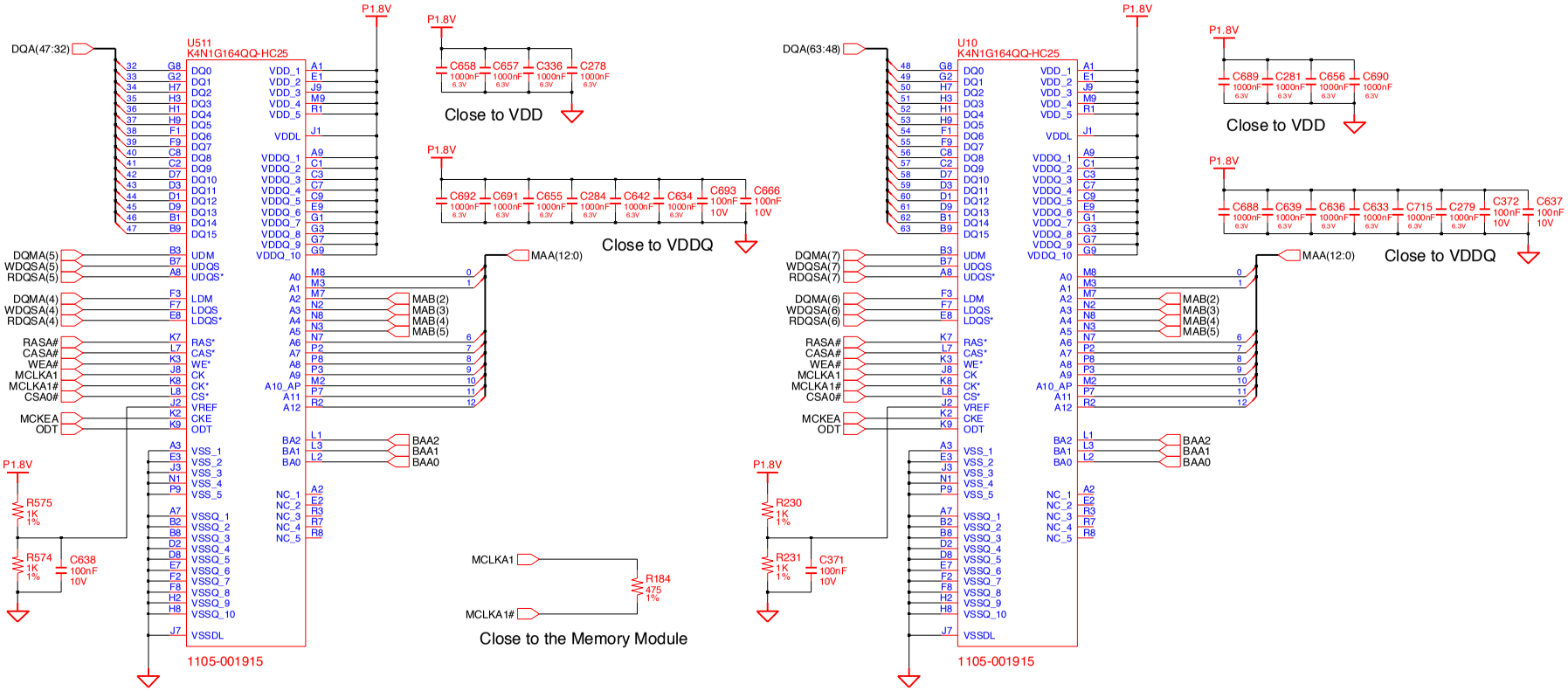
DRAW: TERMI	DATE: 8/14/2007	TITLE: LYON_External EXT NB9X NB9X CHIP (4/4)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 4 OF 4	

LOWER SUB PARTITION

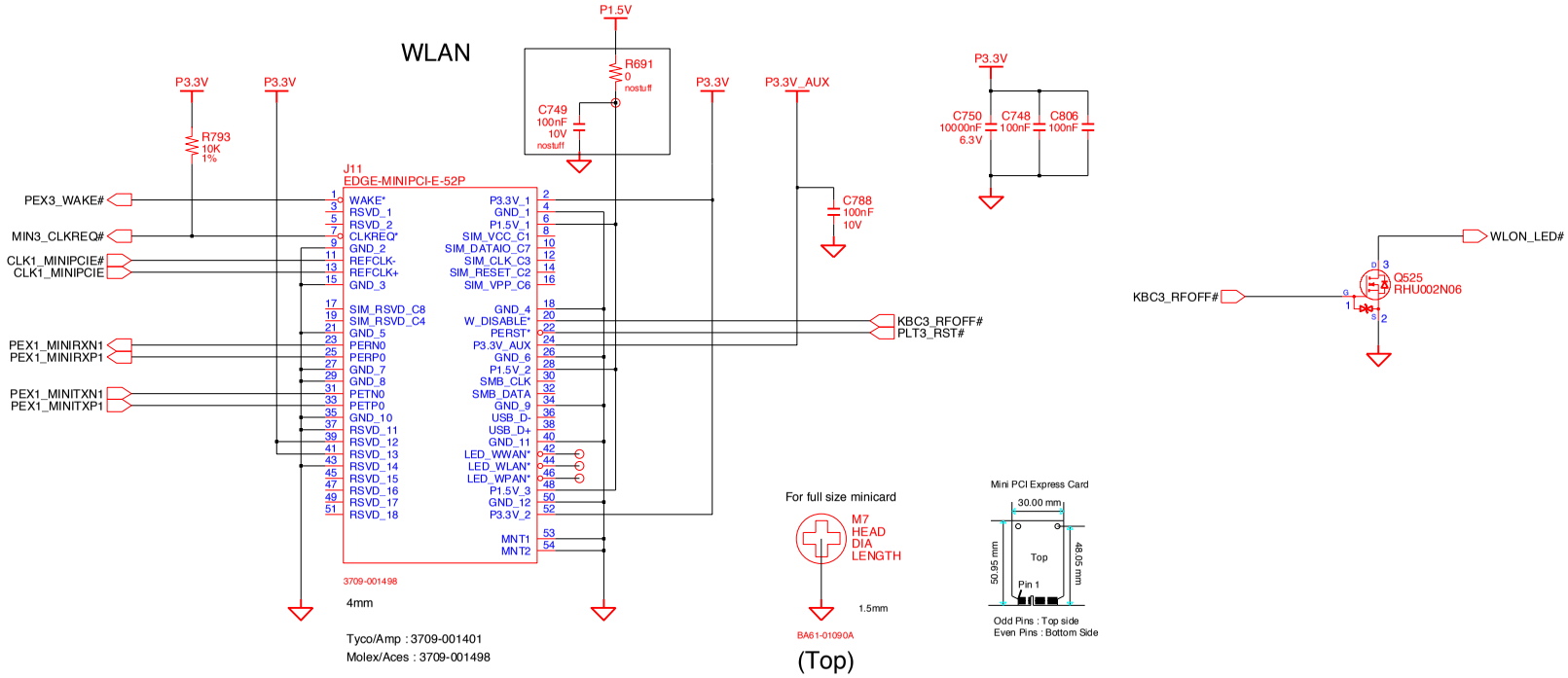


DRAW: TERMI	DATE: 8/12/2006	TITLE: LYON_External Graphics_Memory(GDDR2) Graphics_Memory_Nvidia #1	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 1 OF 2	

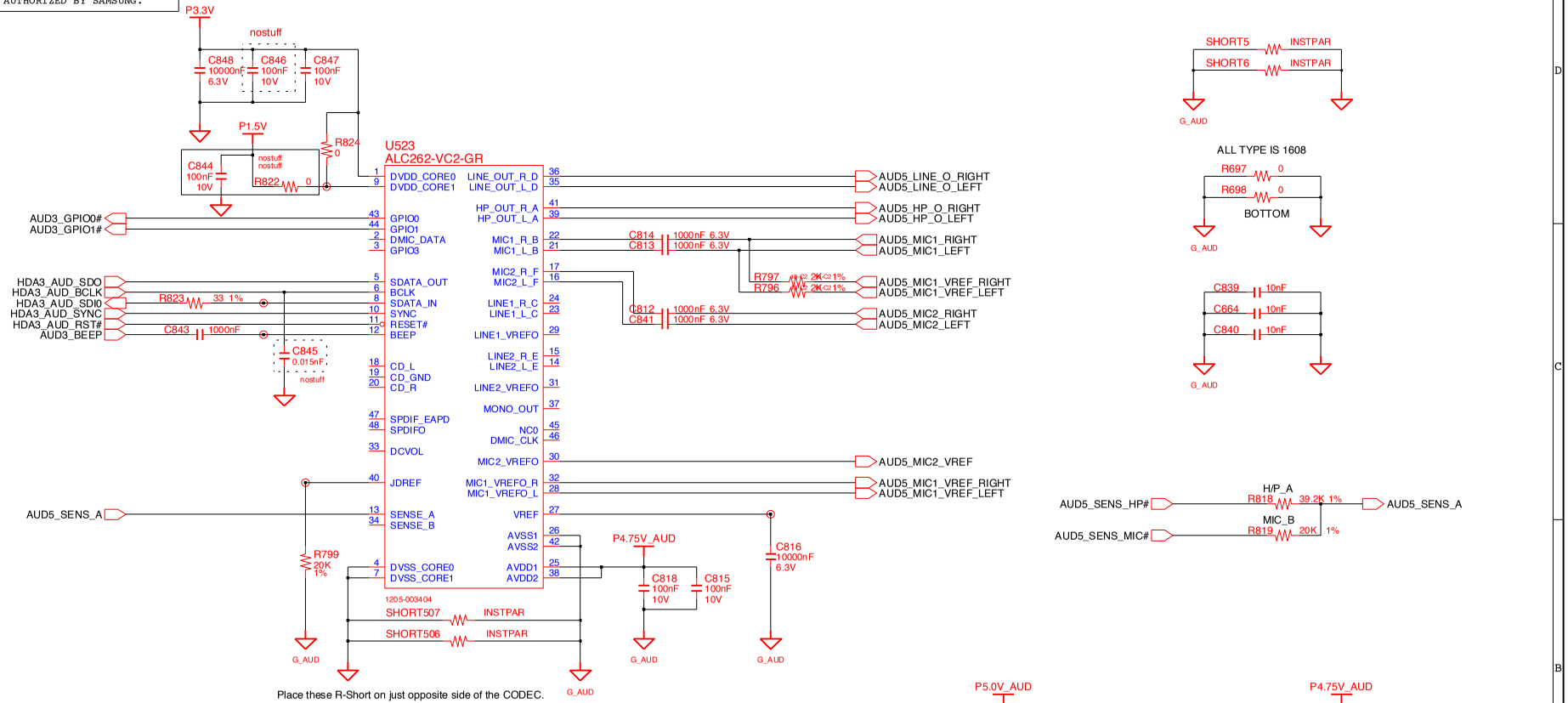
UPPER SUB PARTITION



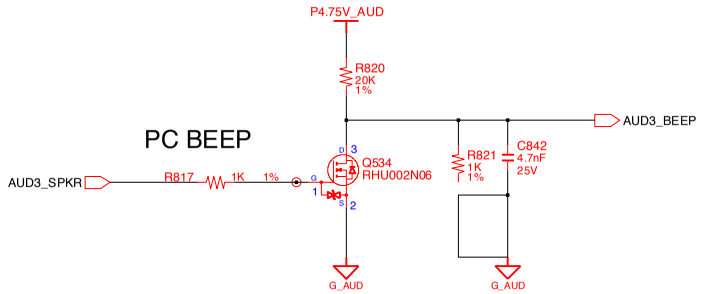
DRAW: TERMI	DATE: 8/12/2006	TITLE: LYON_External Graphics_Memory(GDDR2) Graphics_Memory_Nvidia #2	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 2 OF 2	

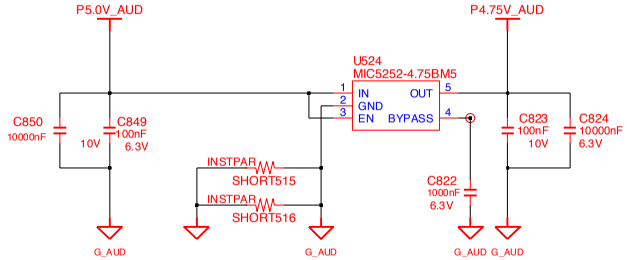


DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External PCIE_Minicard_Slot PCIE_Minicard_Slot	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE: undefined	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 51 OF 64	

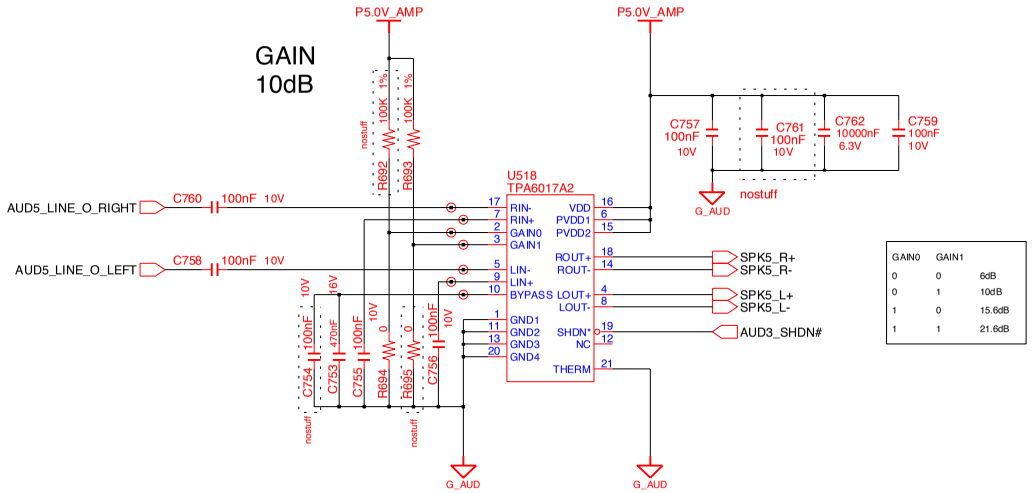


Place these R-Short on just opposite side of the CODEC.

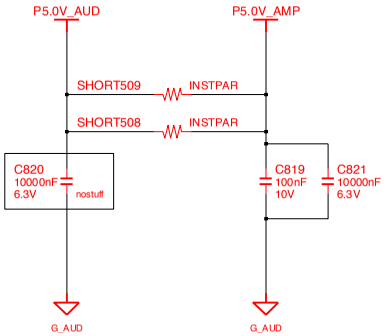


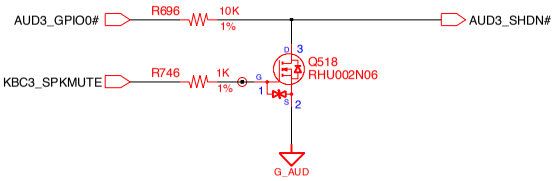


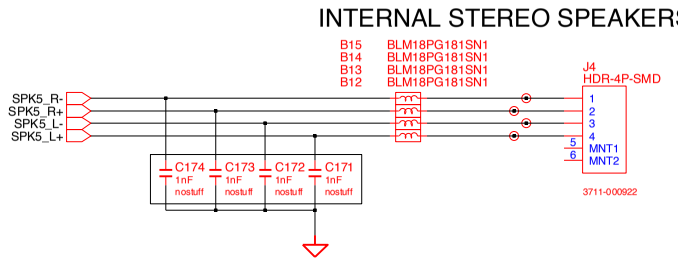
DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External HDA_Codec_Alc262 HDA_Codec_Alc262 #1	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE: undefined	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 28 OF 64	



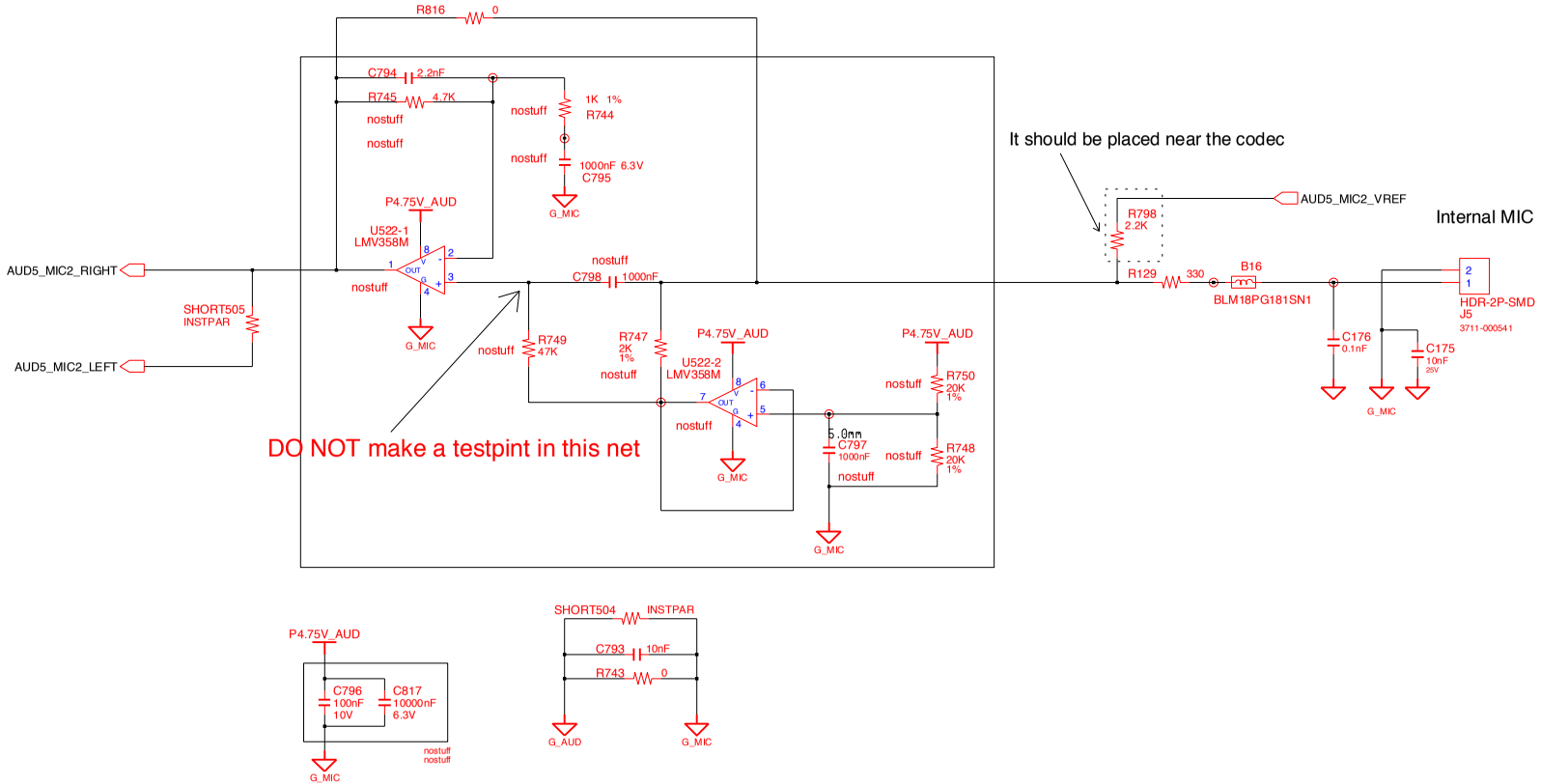
GAIN0	GAIN1	
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB





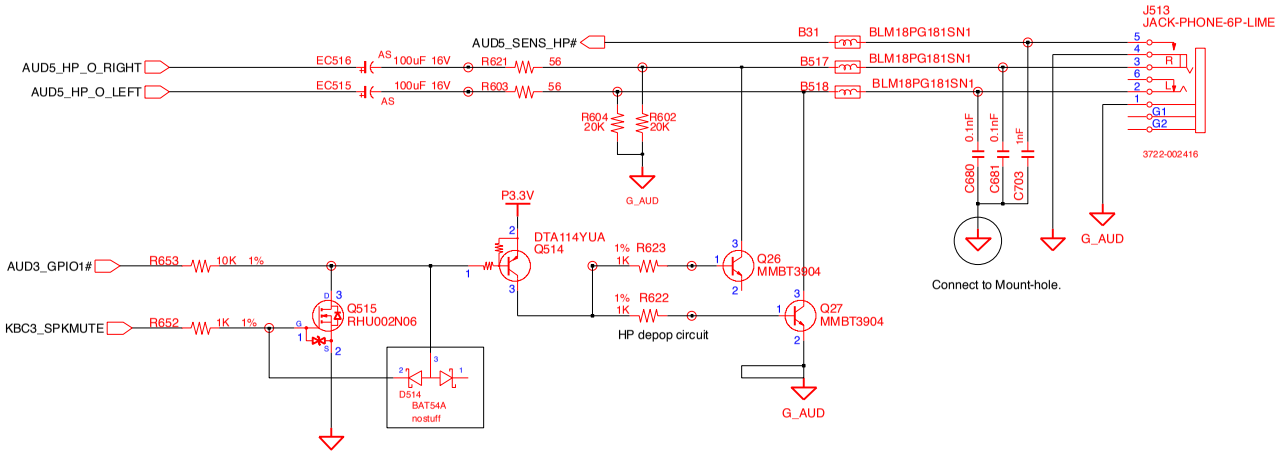


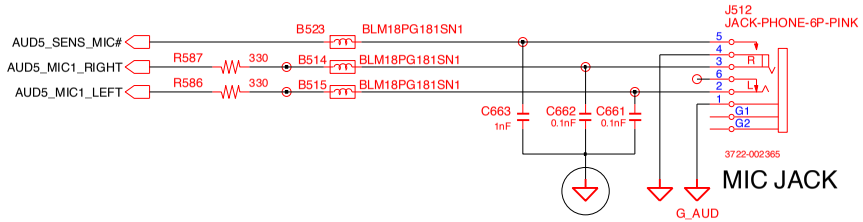
DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP	HDA_Codec_Alc262	
APPROVAL: SJ PARK	REV: 1.0	HDA_Codec_Alc262 #2	PART NO.: BA41-00920A
MODULE CODE	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 29 OF 64	



DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External HDA_Codec_Alc262 HDA_Codec_Alc262 #3	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE: undefined	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 30 OF 64	

HEADPHONE

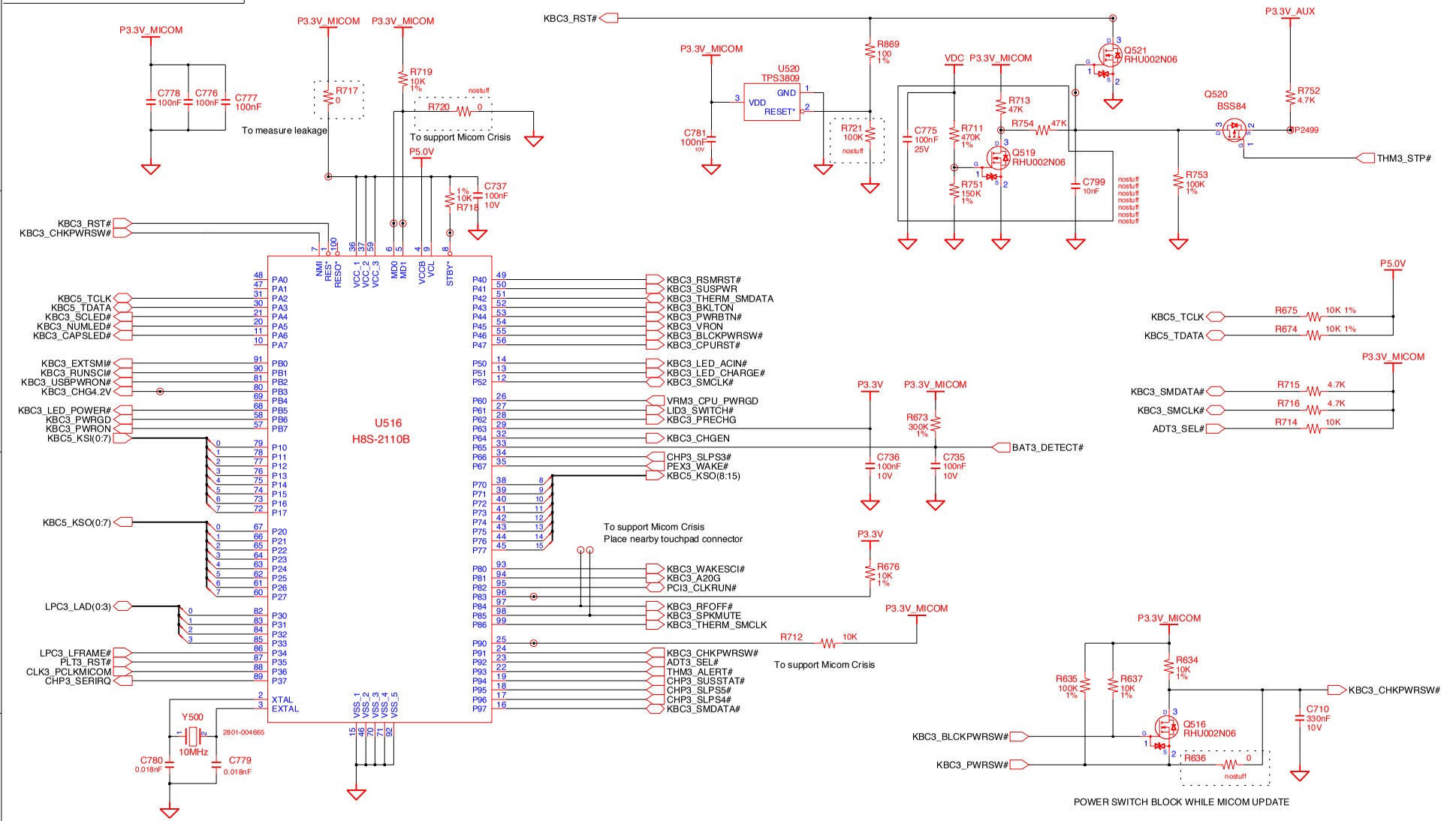




The traces led to Audio Jacks have the width over 10mil

DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP	HDA_Codec_Alc262	
APPROVAL: SJ PARK	REV: 1.0	HDA_Codec_Alc262 #4	PART NO.: BA41-00920A
MODULE CODE	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 31 OF 64	

MICOM RESET

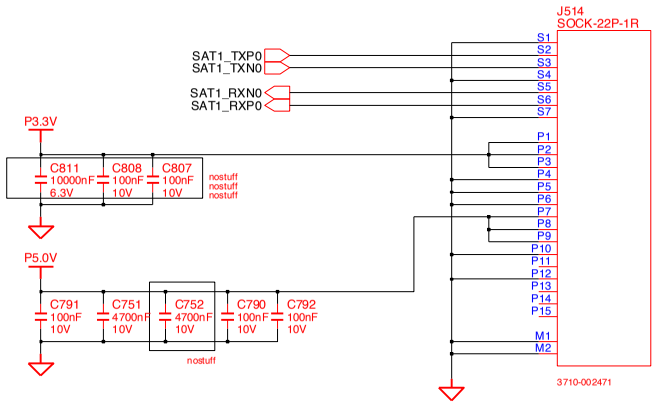


MICOM Crisis Update

Condition: P90=P91=P92=High(MICOM_P3V)
MD0=MD1=Low(0V)
Serial Port: P84 & P85

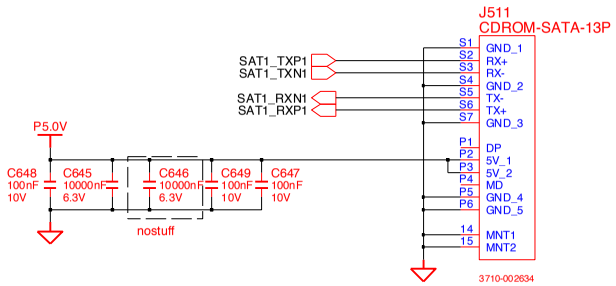
DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP	MICOM_Renesas2110_100p	
APPROVAL: SJ PARK	REV: 1.0	MICOM_Renesas2110_100p	PART NO.: BA41-00920A
MODULE CODE	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 47 OF 64	

Main to HDD



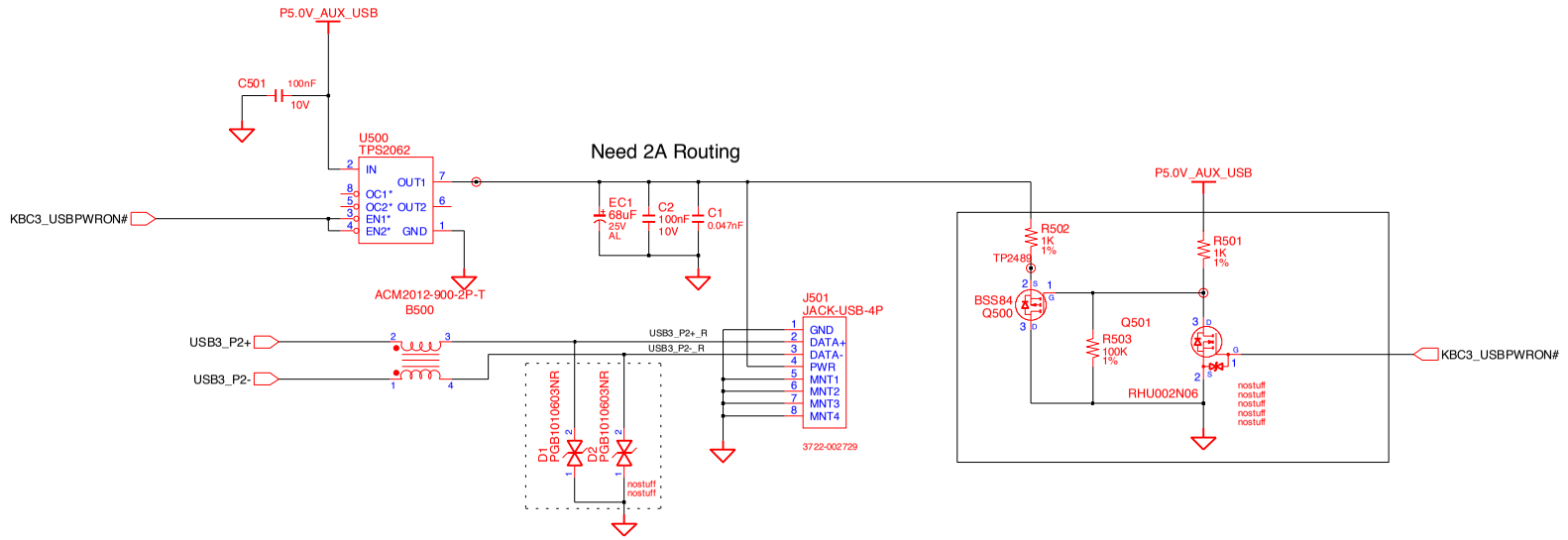
DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External HDD_IF_Conn HDD_IF_Conn	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 33 OF 64	

SATA ODD



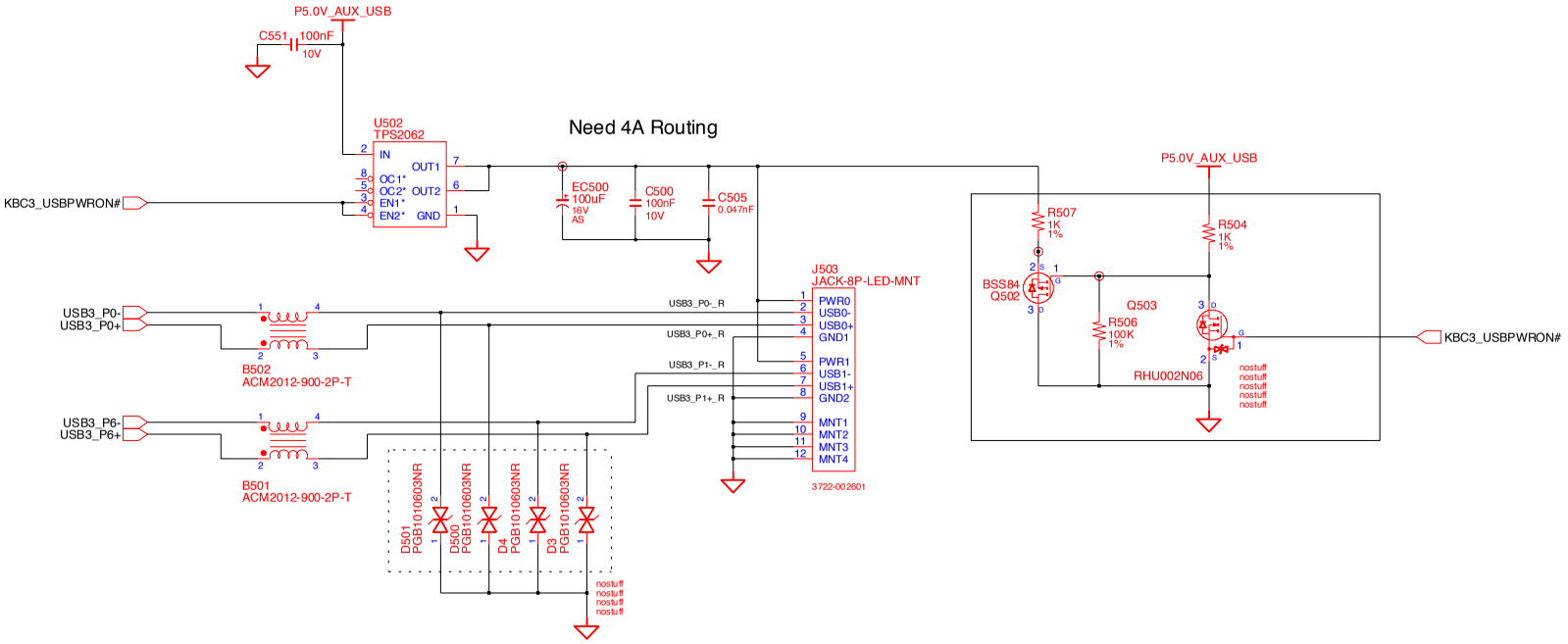
DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External ODD_IF_Conn ODD_IF_Conn	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 49 OF 64	

1 PORT USB CONNECTOR



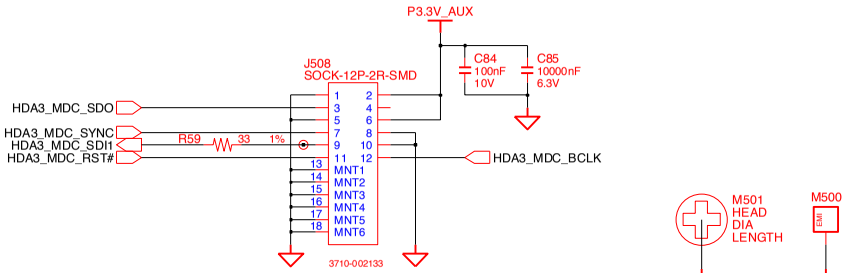
DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External USB_1Port USB_1Port	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 63 OF 64	

2 PORT USB CONNECTOR



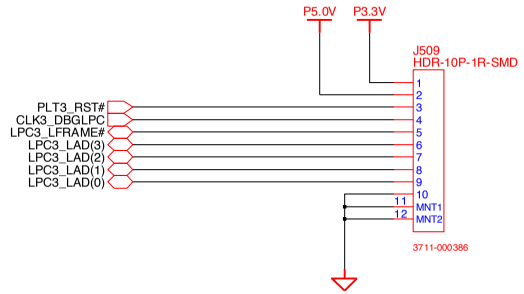
DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External USB_2Port USB_2Port	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 64 OF 64	

MDC Connecter

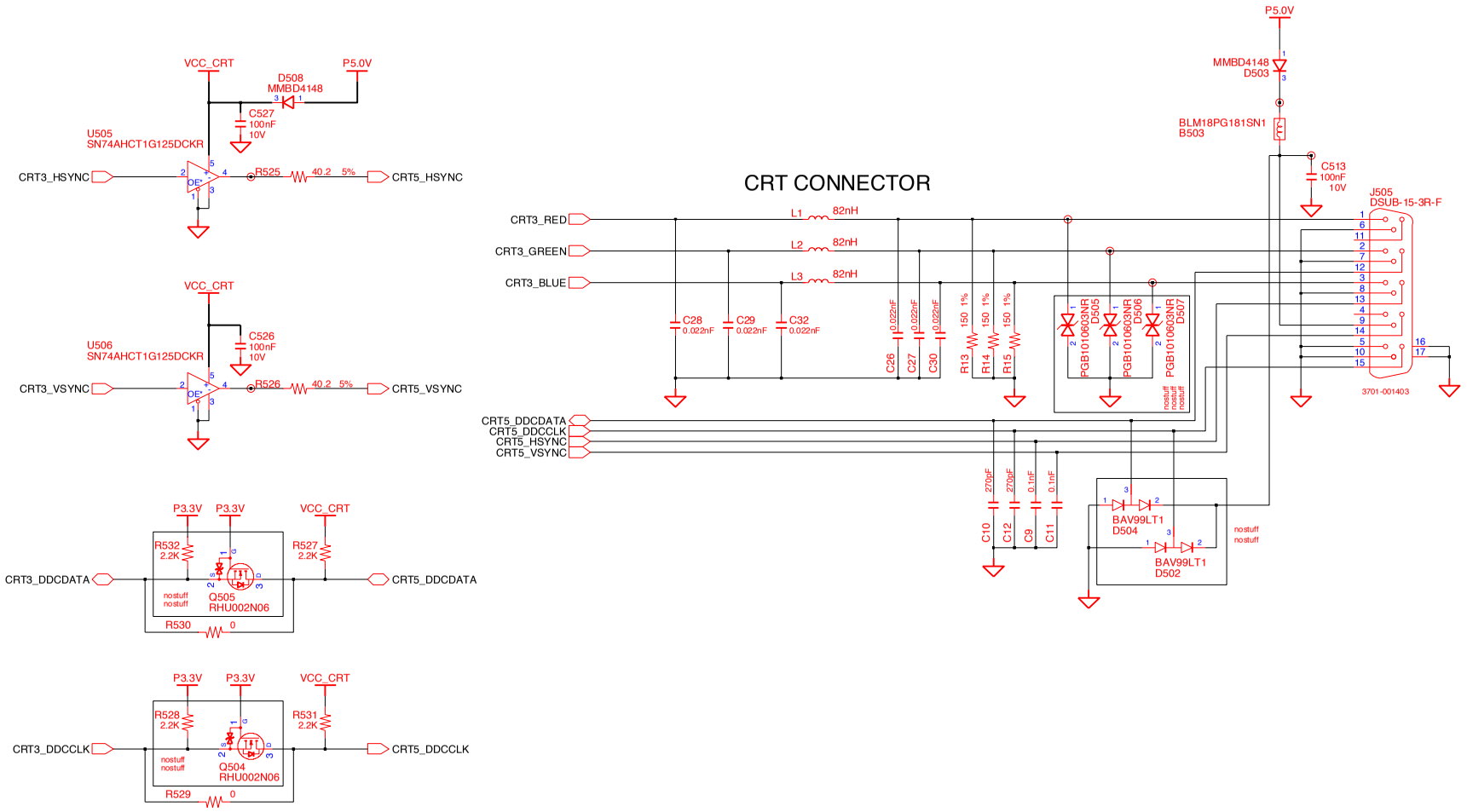


DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External HDA_Modem HDA_Modem	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 32 OF 64	

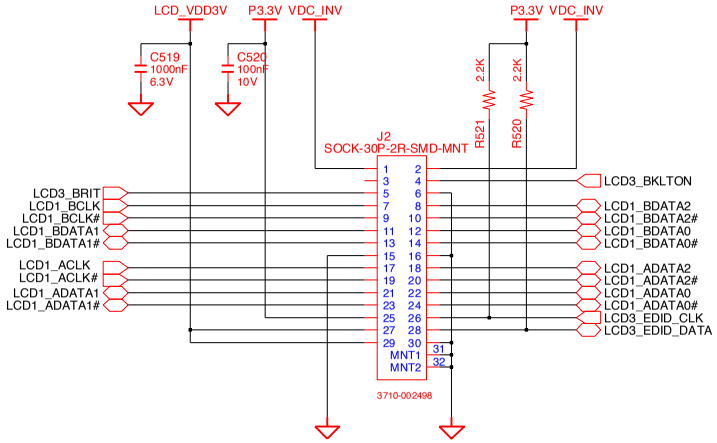
80H DECODER CONNECTOR



DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External Other_Debug_80 Other_Debug_80	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 50 OF 64	

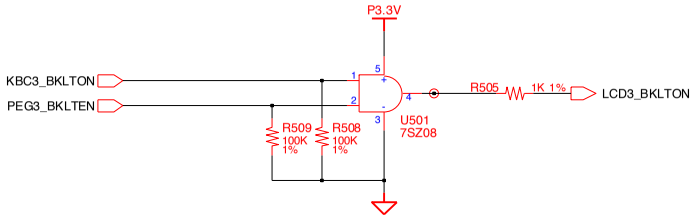


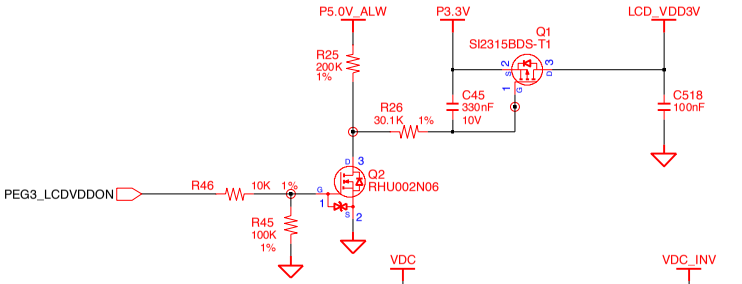
DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External Interface_Circuit Graphics_IF_CRT	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 25 OF 64	

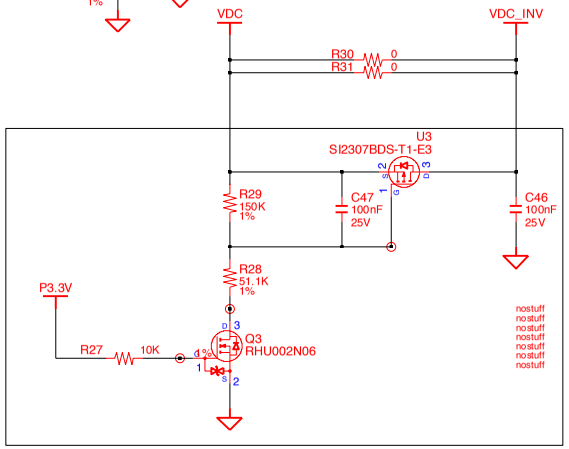


Lyon : 1channel

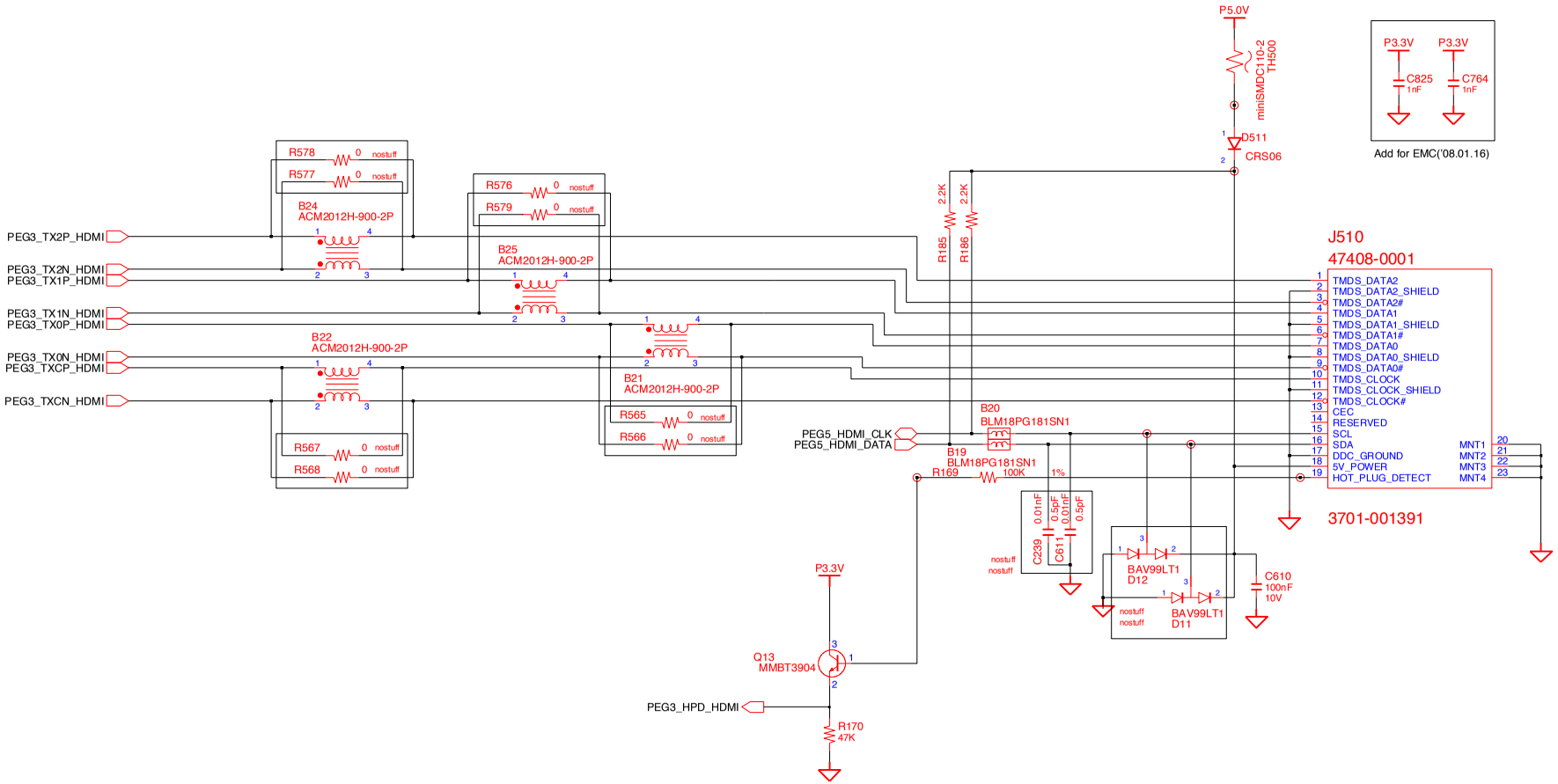
Istanbul : 2channel







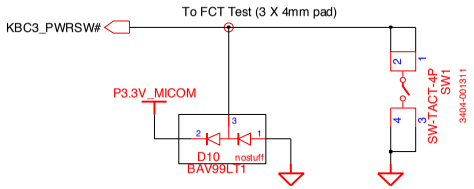
DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External UNDEFINED	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE: 12undefined	



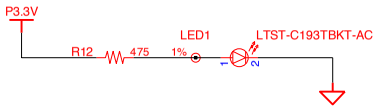
DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External UNDEFINED	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE: 13undefined	

Put this LED located near PWRSW from ME recommedation

Power LED, Blue color

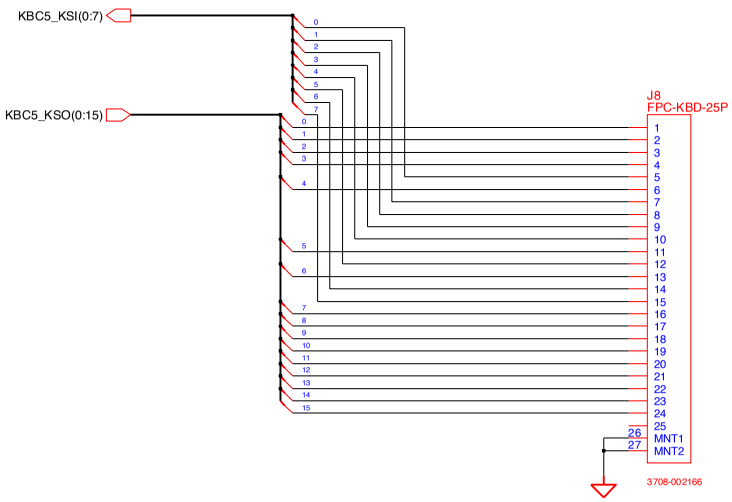


Power On LED



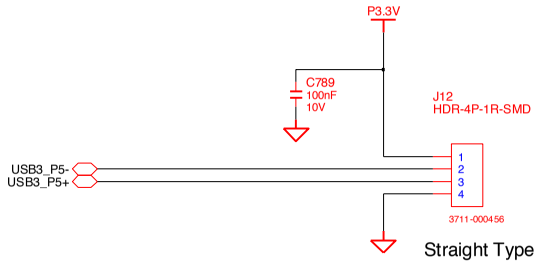
DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External MIO_Switch MIO_Switch	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00920A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 48 OF 64	

KEYBOARD



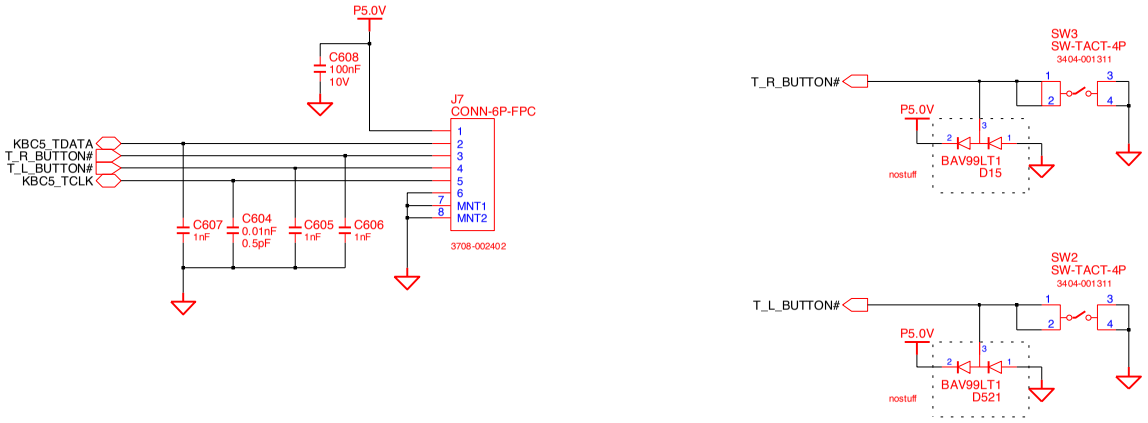
DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External KBD_IF_Conn KBD_IF_Conn	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 39 OF 64	

Bluetooth Interface



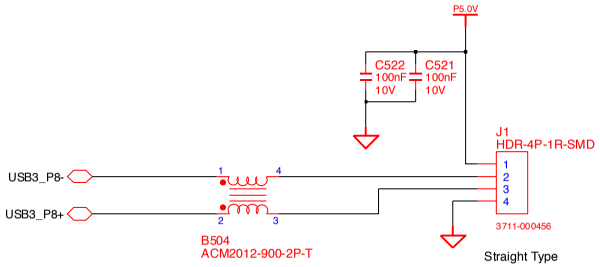
DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External Bluetooth_IF_Conn Bluetooth_IF_Conn	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 19 OF 64	

TOUCHPAD



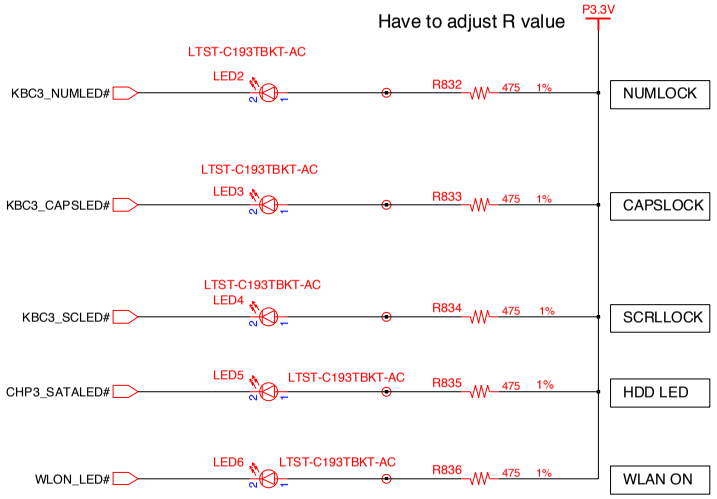
DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External Touchpad_IF_Conn Touchpad_IF_Conn	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 62 OF 64	

CAMERA

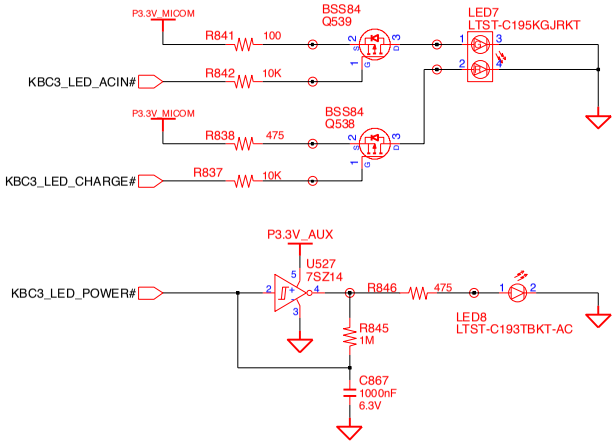


DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External Camera_IF_Conn Camera_IF_Conn	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 20 OF 64	

Have to adjust R value

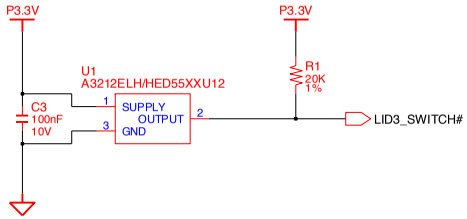


ADAPTERIN/CHARGING LED



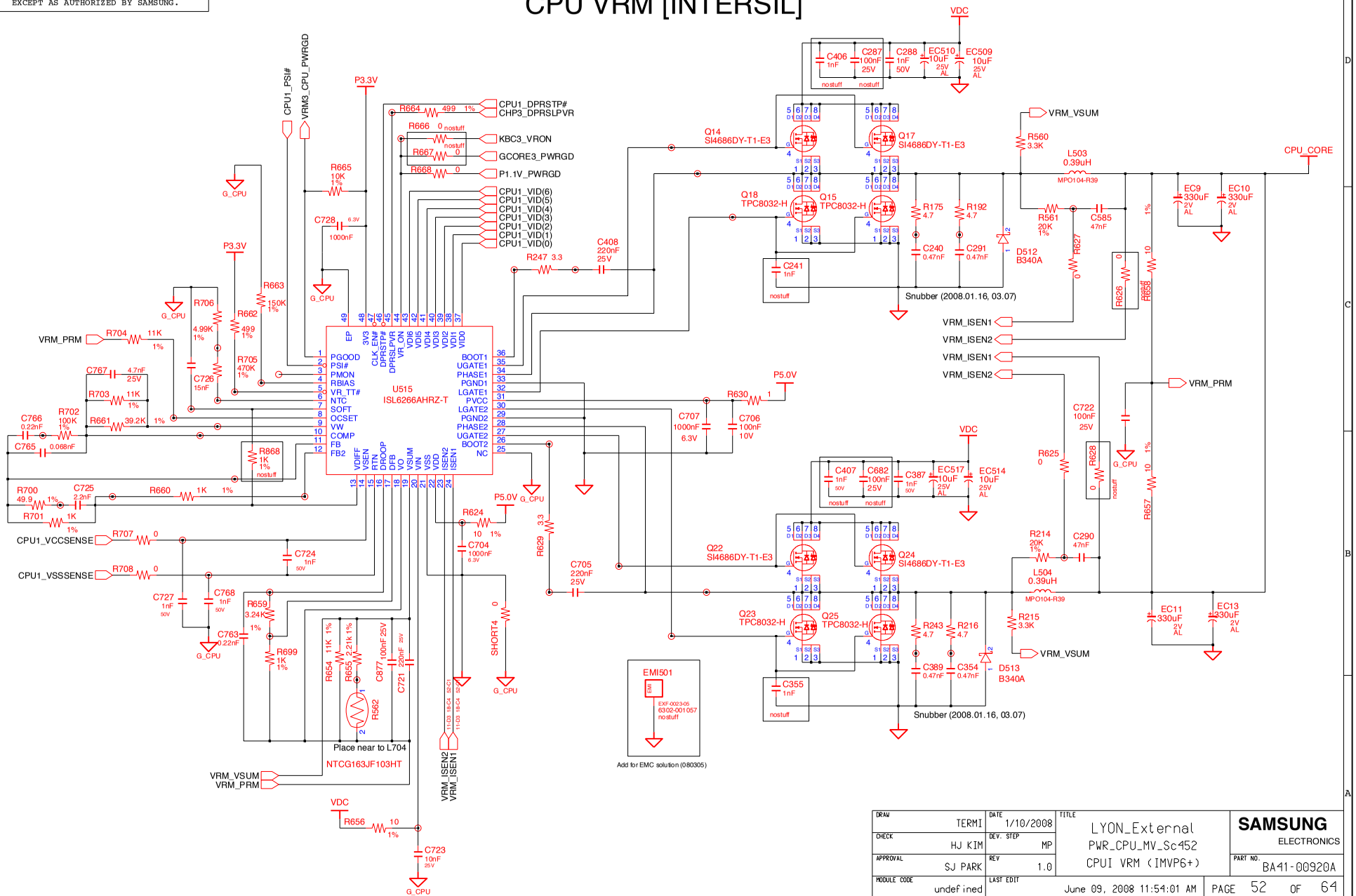
DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External LED_Switch LED_Switch	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 40 OF 64	

LID_SWITCH



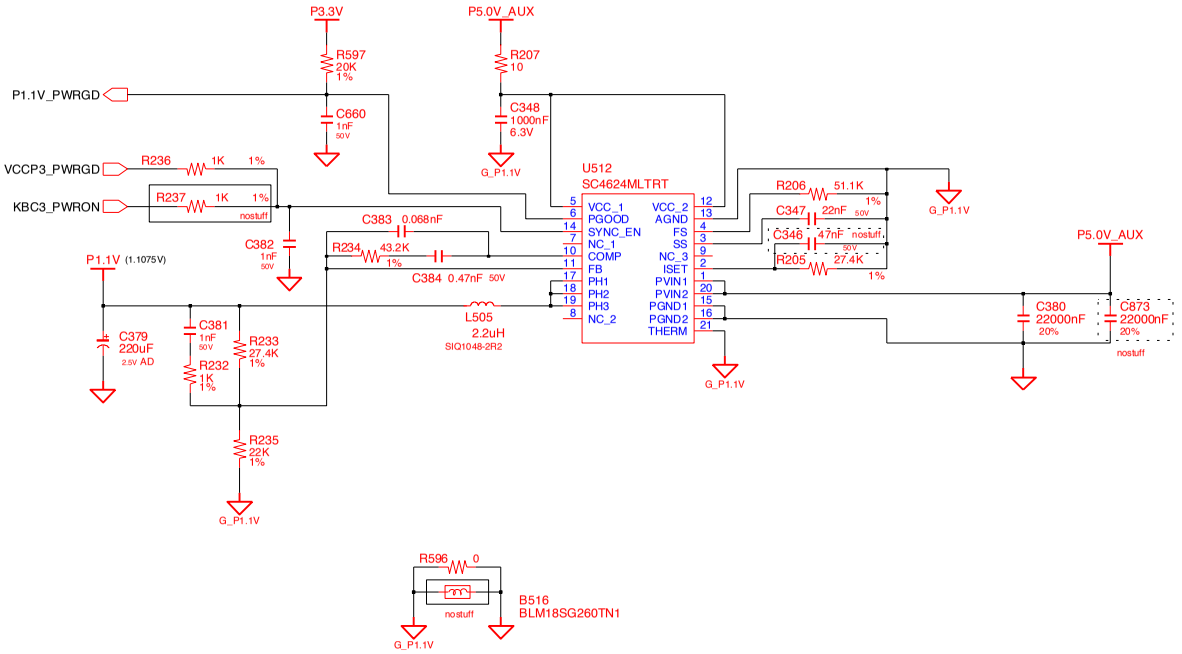
DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External LID_Switch LID_Switch	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00920A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 41 OF 64	

CPU VRM [INTERSIL]



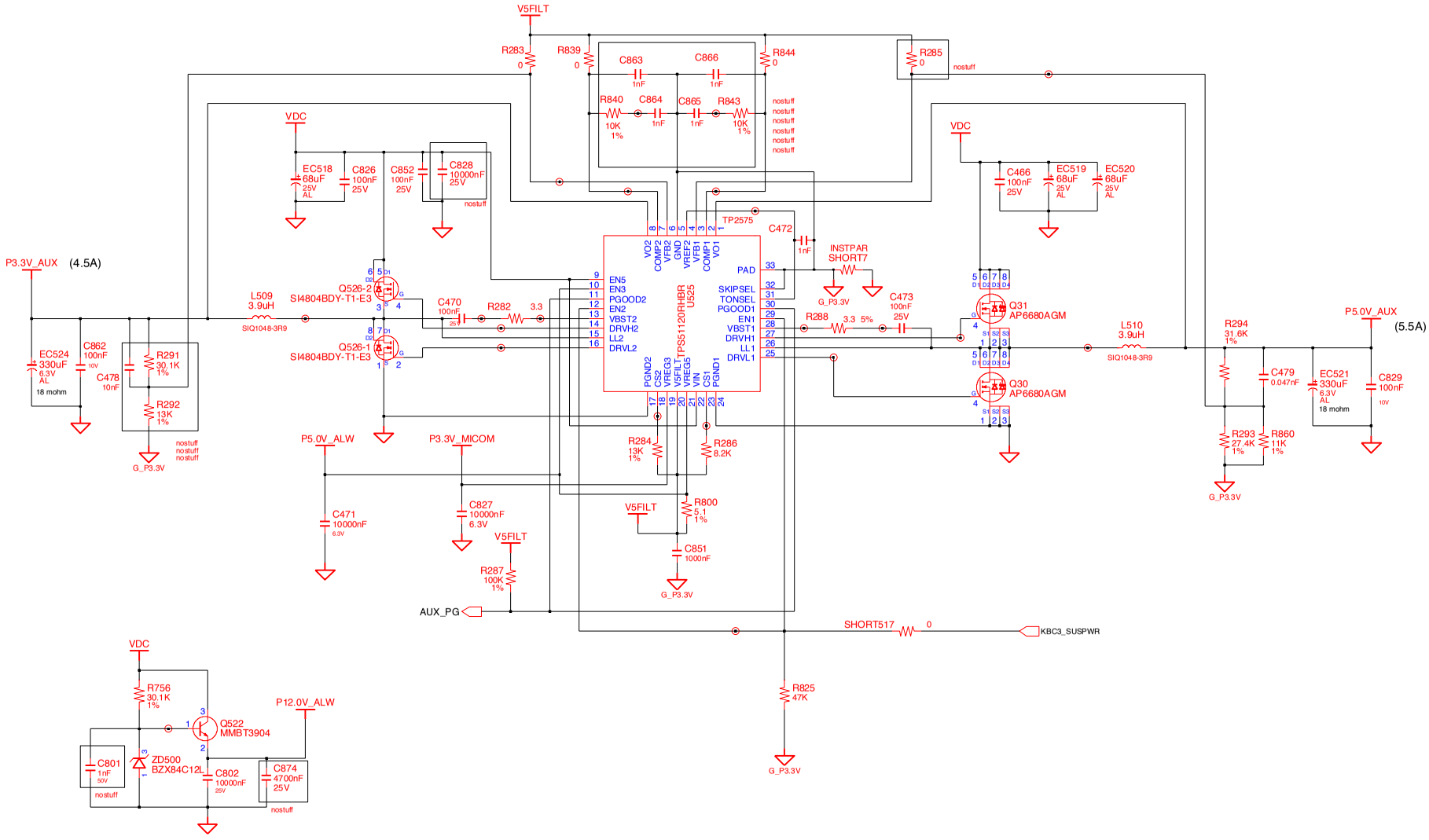
DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External PWR_CPU_MV_Sc452 CPUI VRM (IMVP6+)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE: undefined	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 52 OF 64	

P1.1V



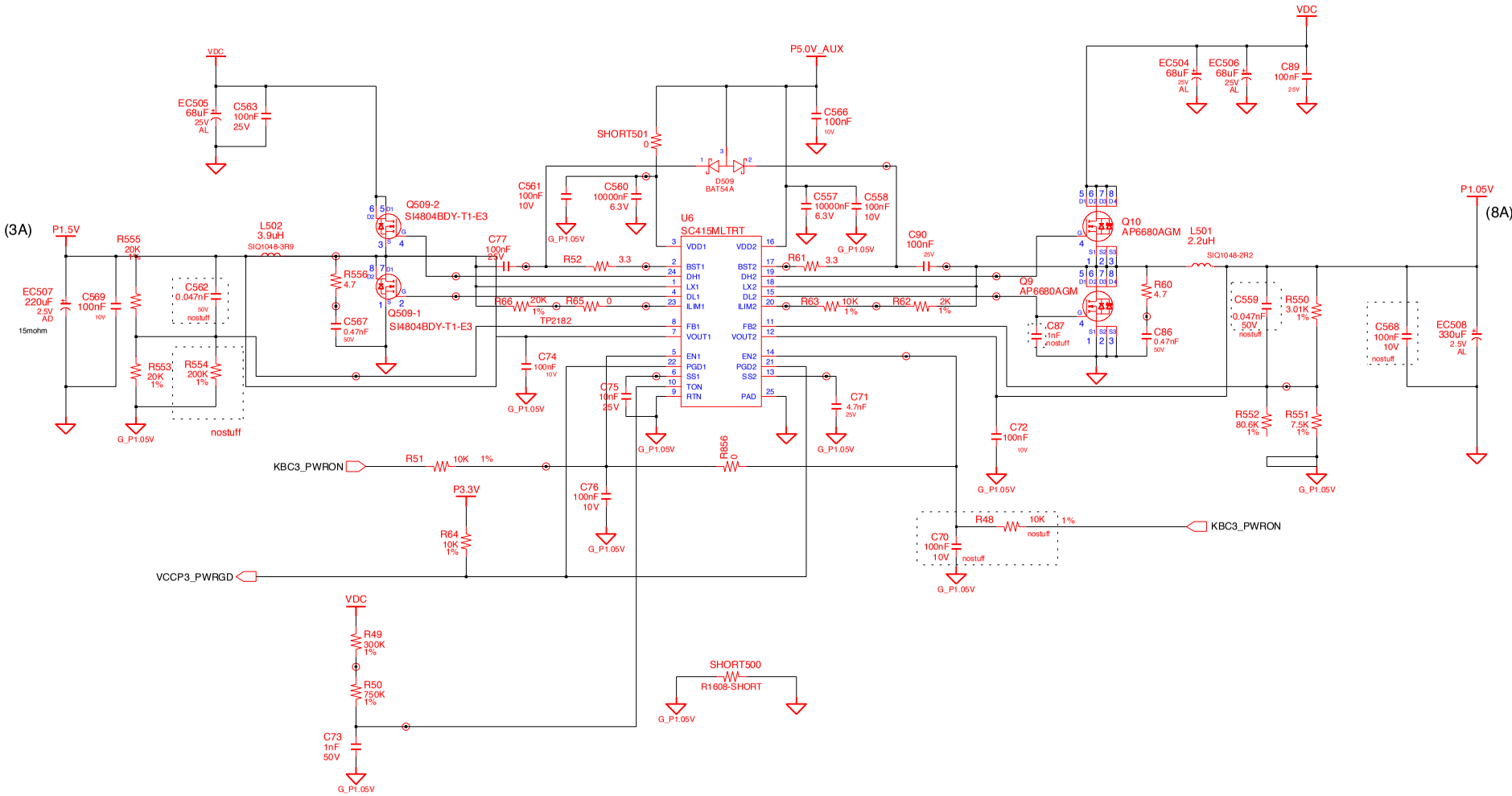
DRAW: TERMI	DATE: 8/14/2007	TITLE: LYON_External PWR_Gfx_MV_Ext Ext Gfx Memory(SC486)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE:	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 1 OF 2	

P3.3V_AUX & P5.0V_AUX



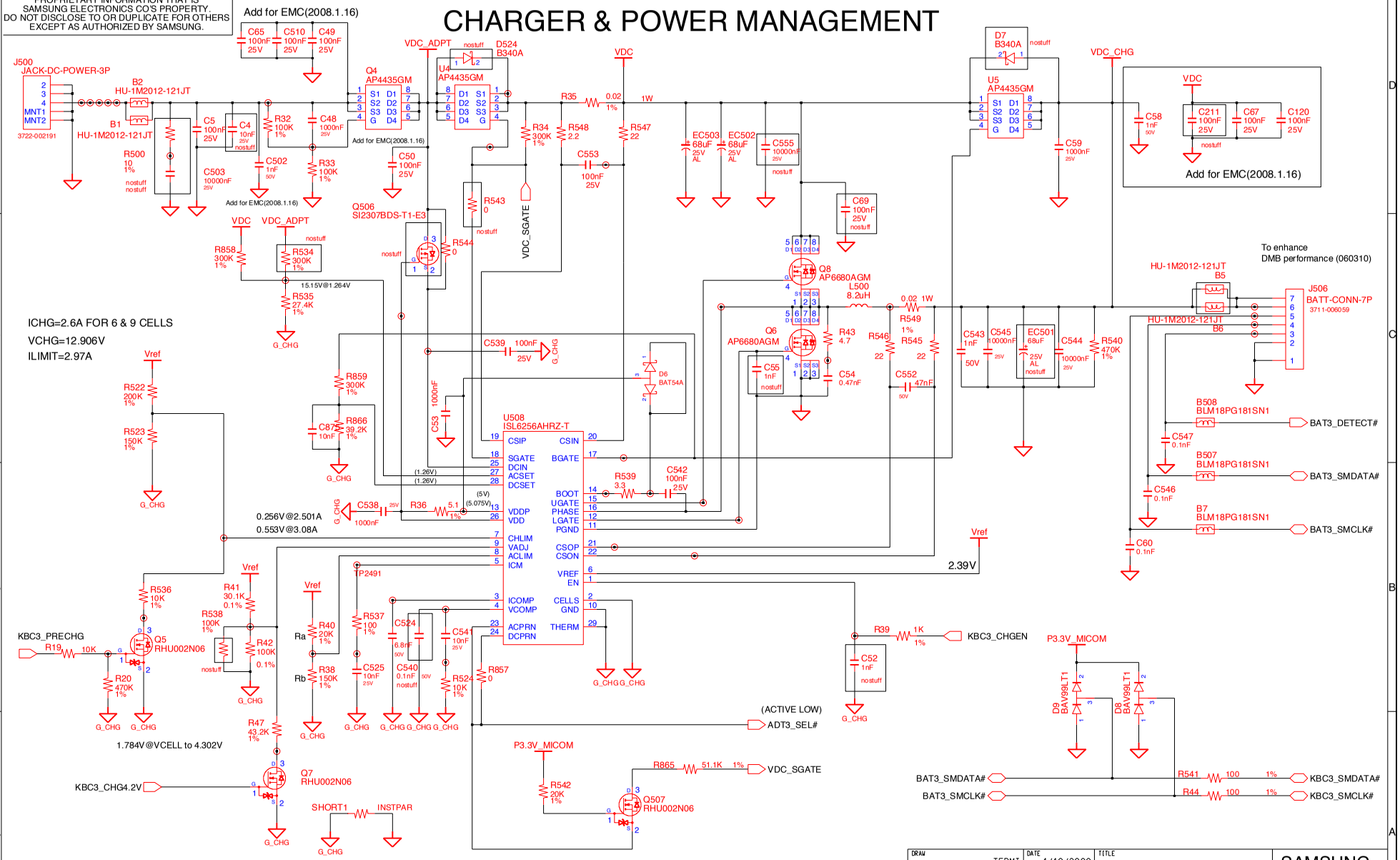
DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External PWR_MV_3V_5V P3.3V_AUX / P5.0V_AUX	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE: undefined	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 53 OF 64	

CHIPSET POWER (P1.05V & P1.5V)



DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External PWR_MV_Cantiga Chipset Power (P1.05V_M,P1.2V)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE: undefined	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 54 OF 64	

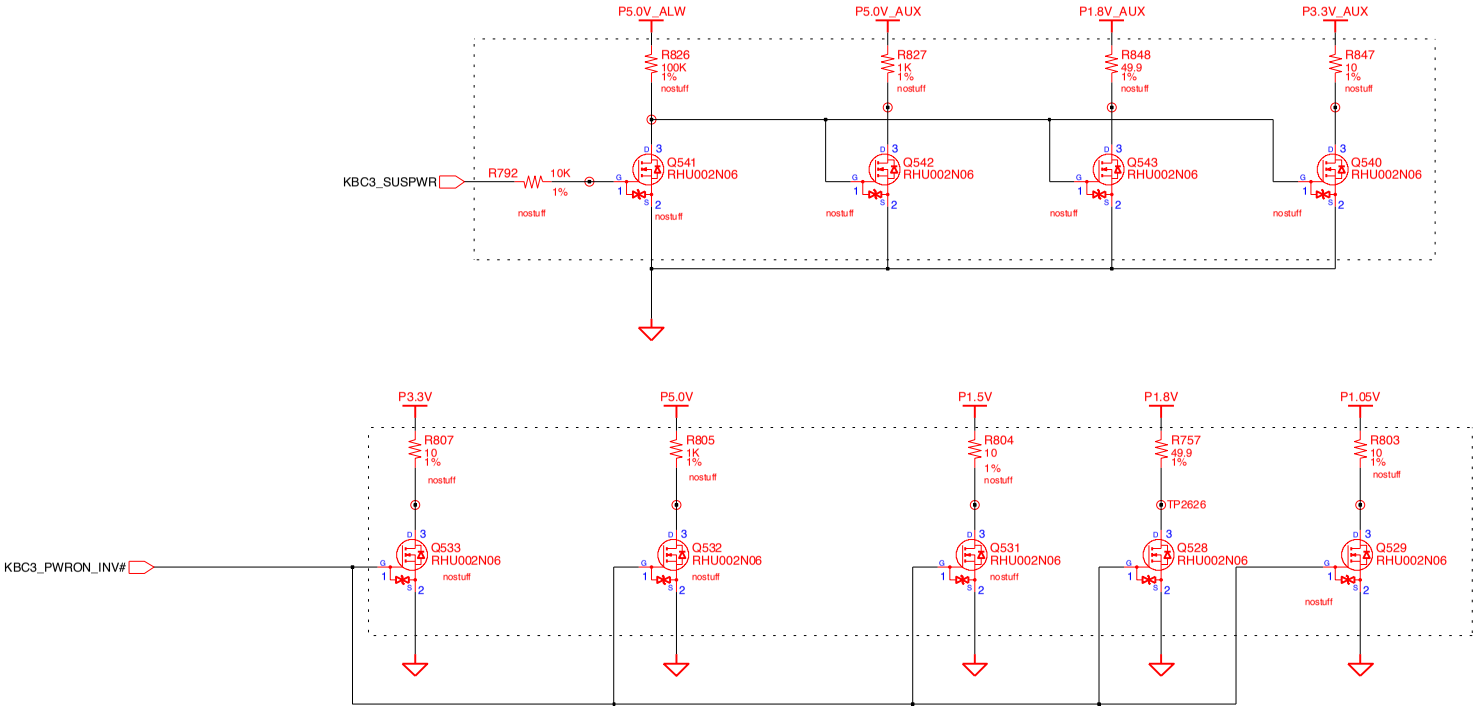
CHARGER & POWER MANAGEMENT



	60W	90W
Ra	150K(2007-007489)	20k(2007-007312)
Rb	20K (2007-007312)	150K(2007-007489)
Iaclim	2.97A	4.526A

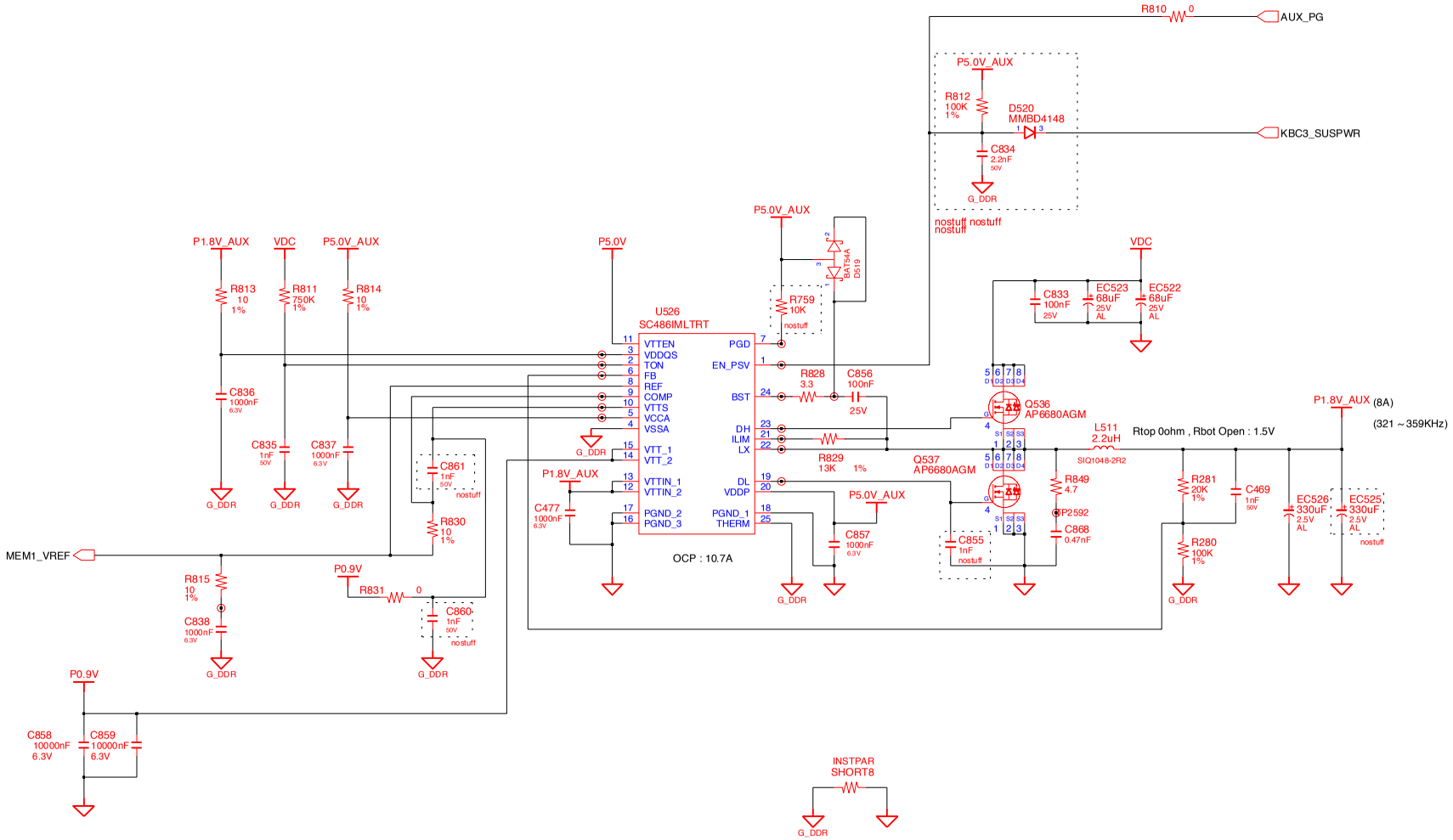
DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External PWR_MV_Charger CHARGER	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE: undefined	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 55 OF 64	

POWER DISCHARGER



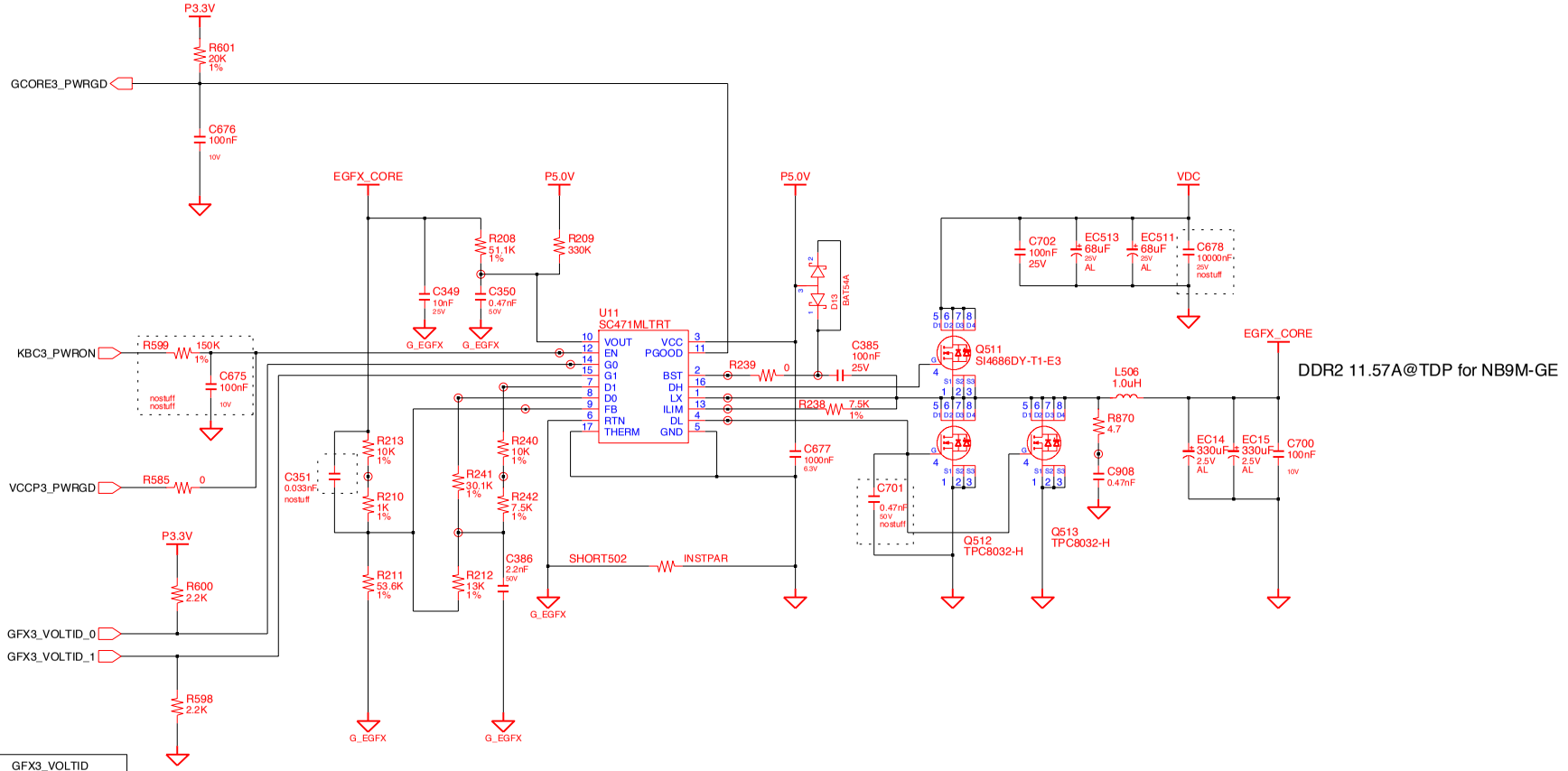
DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External PWR_MV_DisCharger DISCHARGING LOGIC	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE: undefined	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 56 OF 64	

DDR2 Power



DRAW: TERMI	DATE: 1/10/2008	TITLE: LYON_External PWR_MV_MeMory DDR3 POWER (P1.5V_AUX)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE: undefined	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 57 OF 64	

Graphic Core Power



GFX3_VOLTID		
G0	G1	
0	0	0.9V (0.9??V)
1	0	1.09V (1.093V)
0	1	1.17V (1.175V)
1	1	RESERVE

DRAW: TERMI	DATE: 8/14/2007	TITLE: LYON_External PWR_Gfx_MV_Ext Ext Gfx Core(SC471)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00920A
MODULE CODE	LAST EDIT: June 09, 2008 11:54:01 AM	PAGE 2 OF 2	