Rocket BSW 11.6" Schematic

Braswell

2015-11-09
REV : A00

DY : None Installed
0SP/1SP : different config for storage and DRAM
Drax : stuff on Drax

<Core Design>

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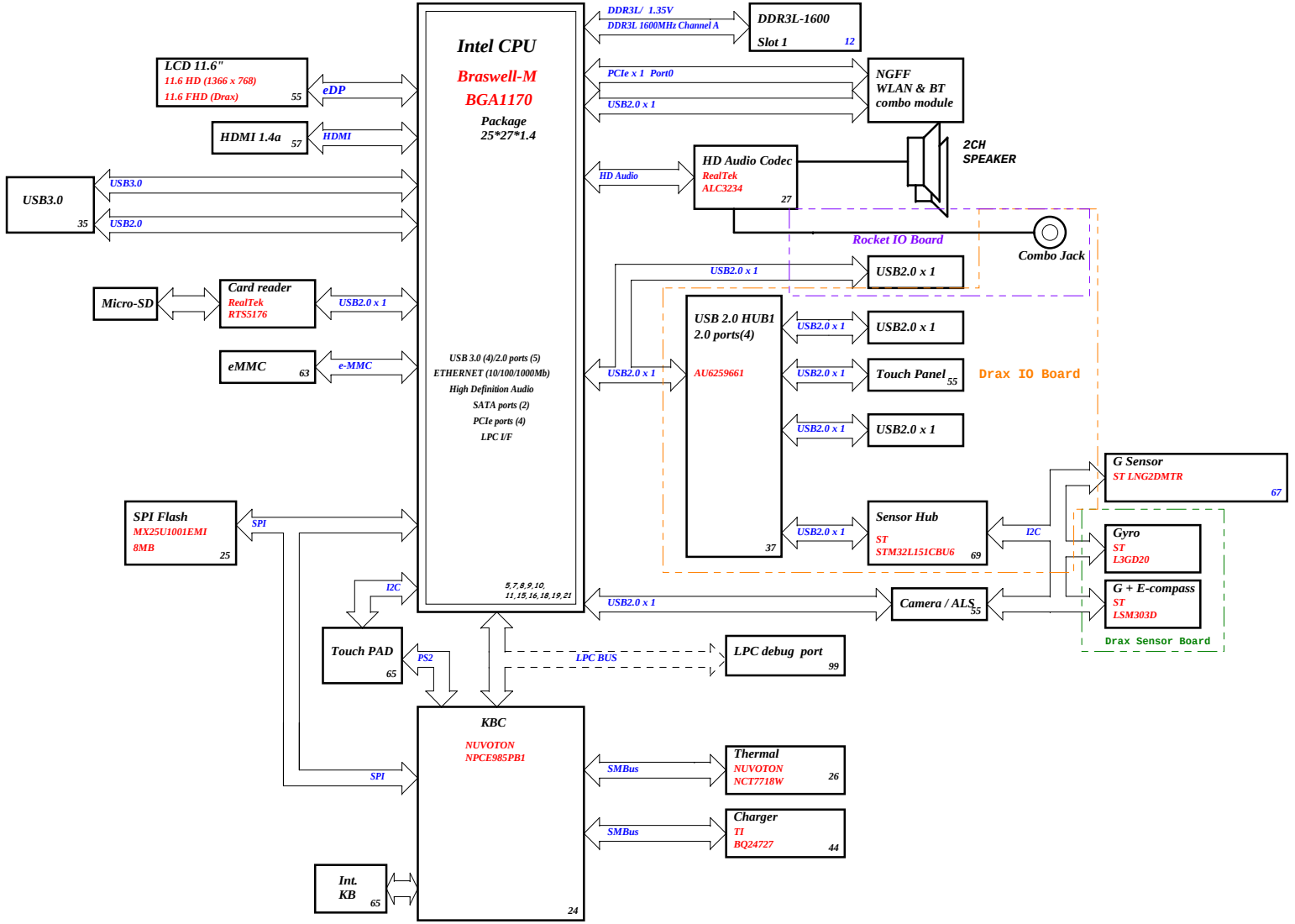
Title: *Cover Page*		
Size: A3	Document Number: *Rocket BSW 11.6"*	Rev: *A00*
Date: Tuesday, November 10, 2015	Sheet 1 of 109	

Project code : 4PD076010001
PCB P/N : 15239
Revision : -1

Rocket 11.6" Block Diagram - 1SP



CHARGER BQ24727RGRR	44
INPUTS	OUTPUTS
19V_AD+	12V_BT+

SYSTEM DC/DC SY8288CRAC SY8286BRAC	45
INPUTS	OUTPUTS
19V_DCBATOUT	3D3V_AUX_S5 3D3V_S5 5V_S5

CPU DC/DC NCP81201MNTXG	46-47
INPUTS	OUTPUTS
19V_DCBATOUT	1V_CPU_CORE

CPU DC/DC NCP81201MNTXG	48
INPUTS	OUTPUTS
19V_DCBATOUT	GFX_CORE

SYSTEM DC/DC SY8286RAC	50
INPUTS	OUTPUTS
19V_DCBATOUT	1D05V_S5

Step Down Regulator SYW232DFC	50
INPUTS	OUTPUTS
3D3V_S5	1D15V_S5

SYSTEM DC/DC SY8286RAC	51
INPUTS	OUTPUTS
19V_DCBATOUT	1D35V_CPU_VDDQ_S3

SYSTEM DC/DC APL5338XAI	51
INPUTS	OUTPUTS
1D35V_CPU_VDDQ_S3	0D675V_VREF_S0

Step Down Regulator SYW232DFC	52
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5

SYSTEM LDO S-1339D15-M5001	53
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0

SYSTEM LDO APL5930KAI	54
INPUTS	OUTPUTS
3D3V_S5	1D24V_S5

PCB LAYER

L1:Top L4:Signal
L2:VCC L5:GND
L3:Signal L6:Bottom

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Title: Block Diagram

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A2	Rocket BSW 11.6"	A00

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SSID = CPU

Blanking

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Title

(Reserved)

Size	Document Number	Rev
A4	*Rocket BSW 11.6"*	*A00*

Date: Monday, November 09, 2015 Sheet 3 of 109

SSID = CPU

Blanking

<Core Design>

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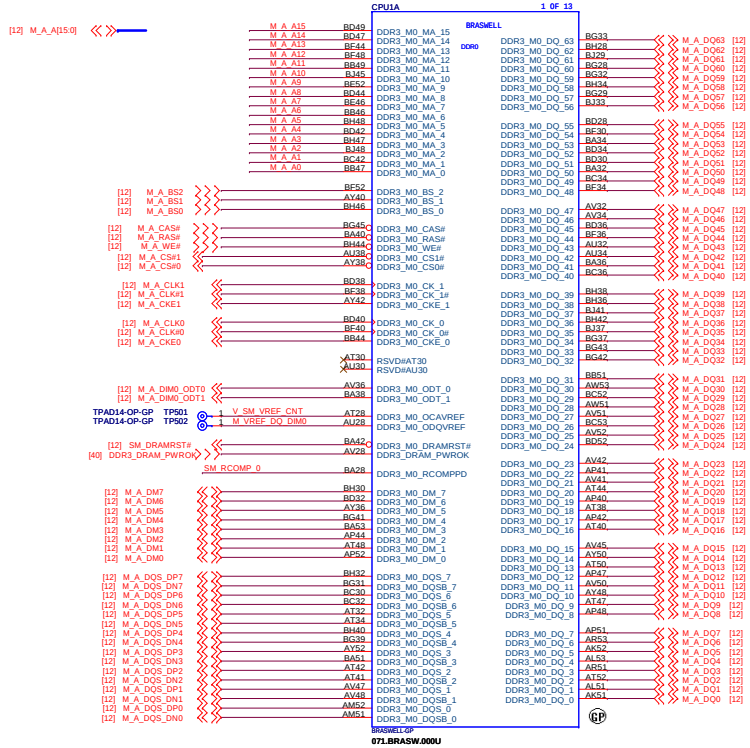
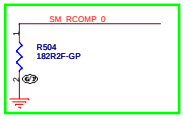
Title: *(Reserved)*

Size	Document Number	Rev
A4	*Rocket BSW 11.6"*	*X00*

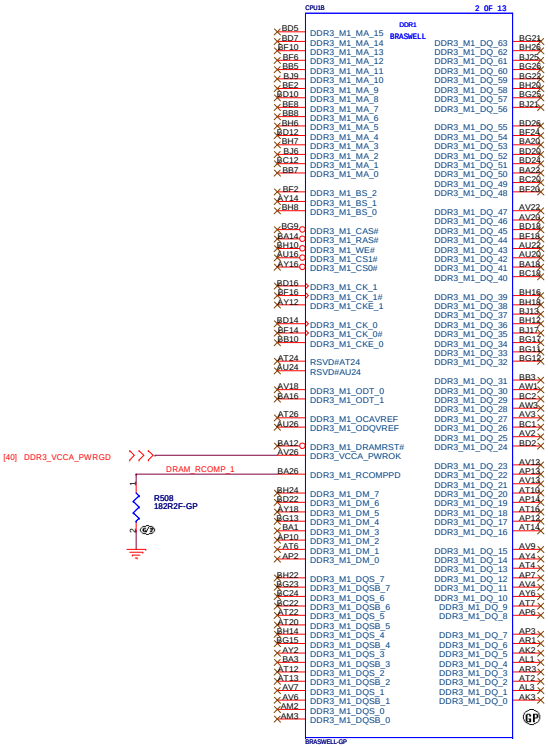
Date: Monday, September 21, 2015 Sheet 4 of 109

SSID = CPU

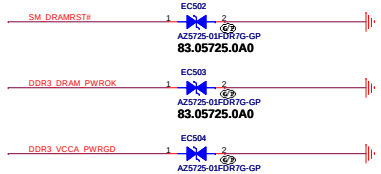




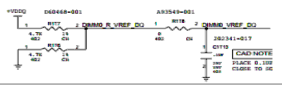
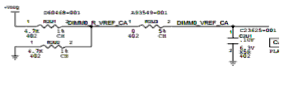
Layout Note: Close CPU



[40] DDR3_VCCA_PWRGD



Follow Intel Check List, Remove Reference Voltage

DDR3_M0_ODQVREF DDR3_M1_ODQVREF	Not applicable to DDR3L implementation. In DDR3L mode, these pins are No Connect on SoC Vref. External Vref circuitry needs to be given on SODIMM side. Example shown as below 0.5*VCCDDR_1P24_1P35. Use 1% resistor. Cannot go higher than 0.6*VCCDDR_1P24_1P35. Example shown as below 	Not use for DDR3L design.
DDR3_M0_OCAVREF DDR3_M1_OCAVREF	Not applicable to DDR3L implementation. In DDR3L mode, these pins are No Connect on SoC Vref. External Vref circuitry needs to be given on SODIMM side. Example shown as below. 0.5*+VCCDDR_1P24_1P35. Use 1% resistor. Cannot go higher than 0.6*VCCDDR_1P24_1P35. Example shown as below 	Not use for DDR3L design.

<Core Design>

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Title: CPU (DDR)

Size: A2 | Document Number: Rocket BSW 11.6" | Rev: X00

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SSID = CPU

Blanking

<Core Design>

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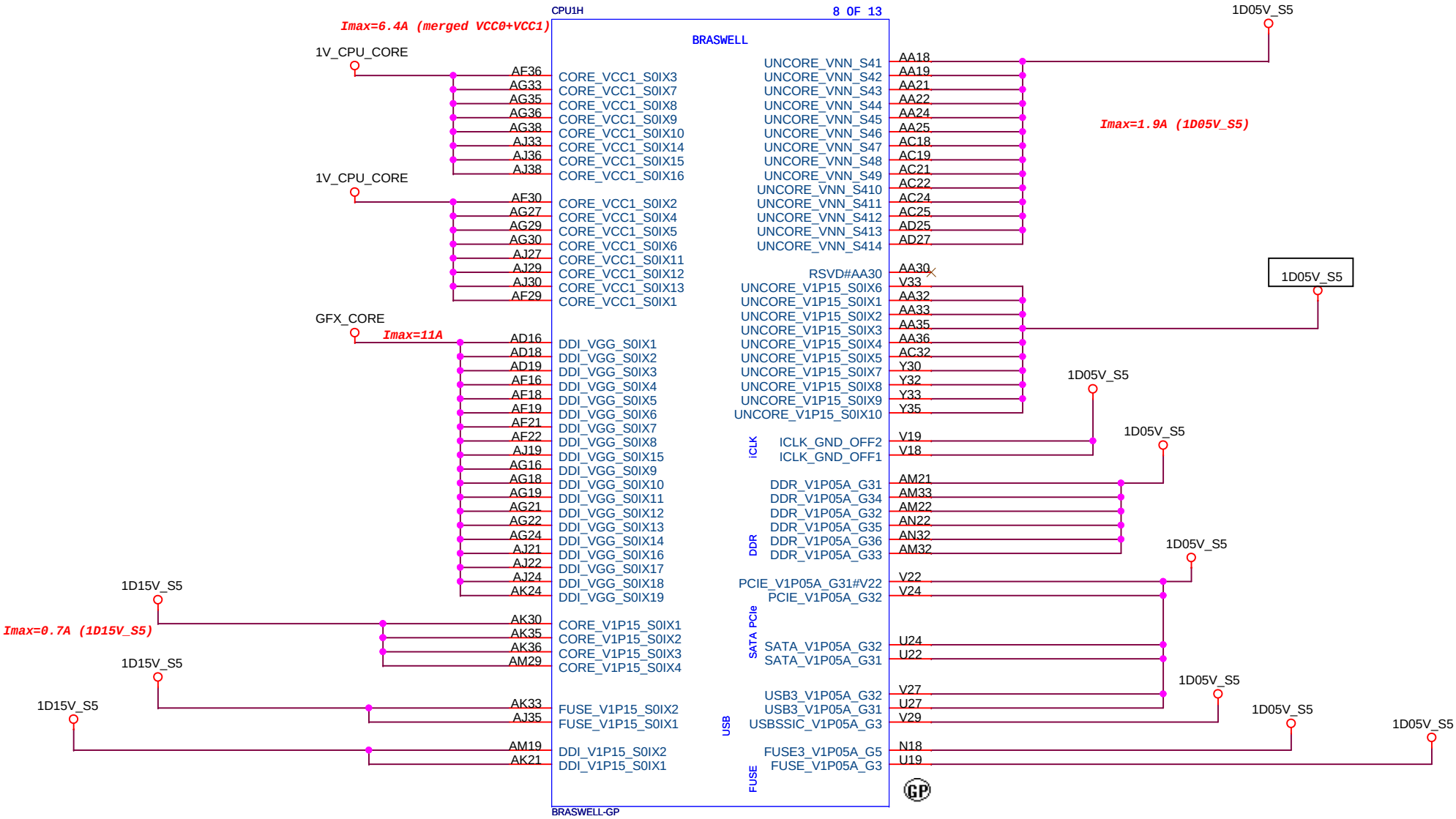
Title: CPU (CFG)

Size: A4 | Document Number: Rocket BSW 11.6" | Rev: X00

Date: Monday, September 21, 2015 | Sheet 6 of 109

SSID = CPU



<Core Design>

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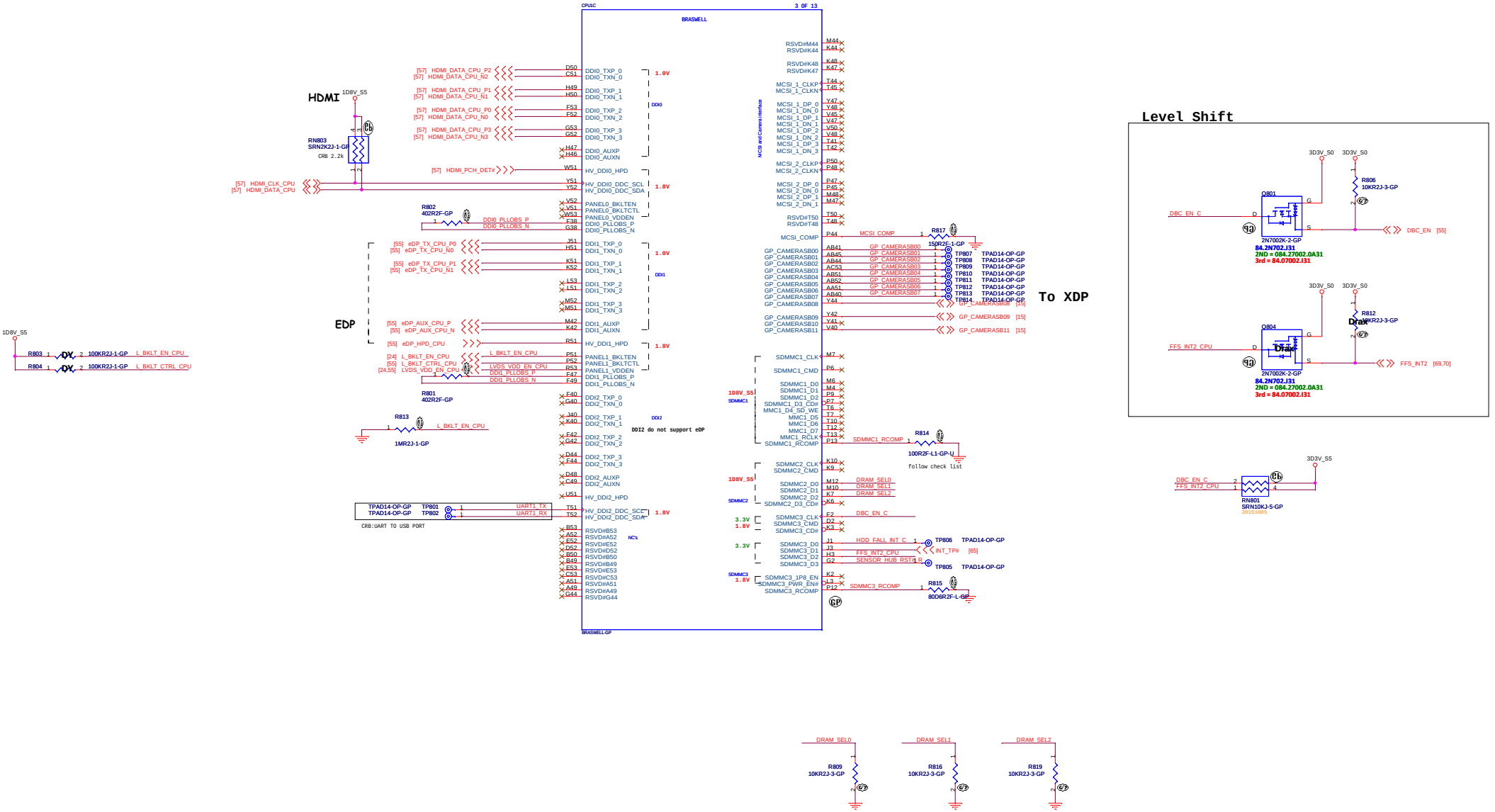
Title
CPU (VCC_CORE)

Size	Document Number	Rev
A4	Rocket BSW 11.6"	X00

Date: Monday, September 21, 2015 Sheet 7 of 109

SSID = CPU



<Core Design>

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Title: CPU (DDI/EDP/GPIO)

Size: A2 | Document Number: Rocket BSW 11.6" | Rev: X00

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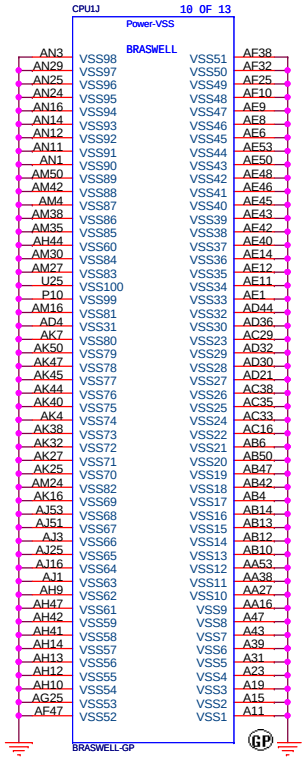
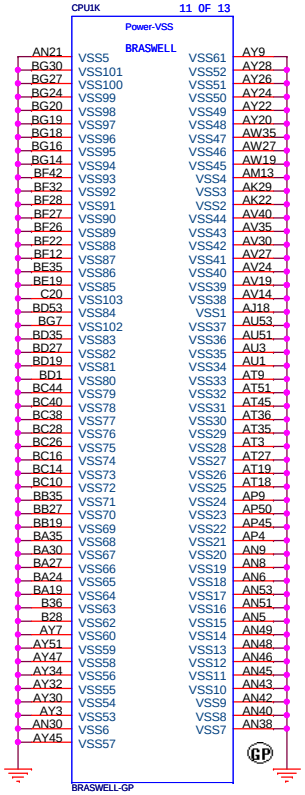
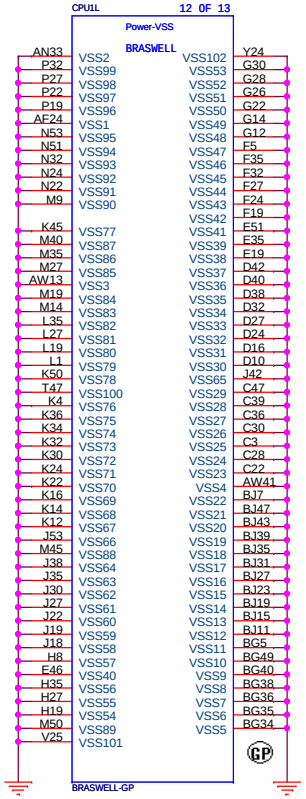
SSID = CPU







2014/04/25
Intel suggest

TP901 1
TPAD14-OP-GP

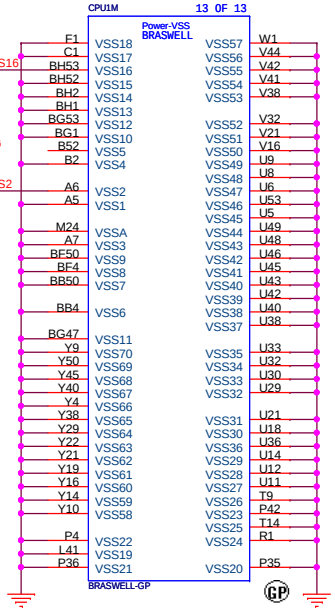
CPU_VSS16

B52 MAY NOT BE ABLE TO BREAK OUT IN ROUTING

TP902 1
TPAD14-OP-GP

CPU_VSS2

2014/04/25
Intel suggest



<Core Design>

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Title: **CPU (VSS)**

Size	Document Number	Rev
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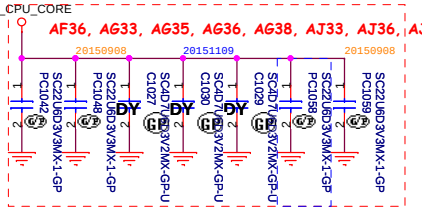
SSID = CPU

PLACE ALL THE CAPS
UNDER THE PKG SHADOW

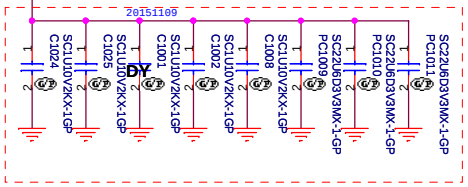
1V_CPU_CORE

AF36, AG33, AG35, AG36, AG38, AJ33, AJ36, AJ38



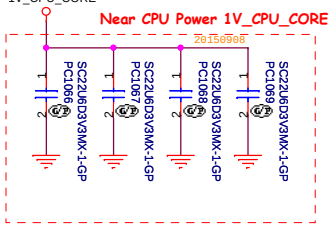
1D05V_S5

AA18, AA19, AA21, AA22, AA24, AA25, AC18, AC19, AC21, AC22, AC24, AC25, AD25, AD27



1V_CPU_CORE

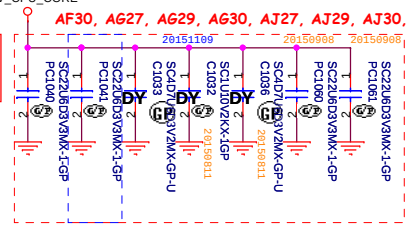
Near CPU Power 1V_CPU_CORE



1V_CPU_CORE

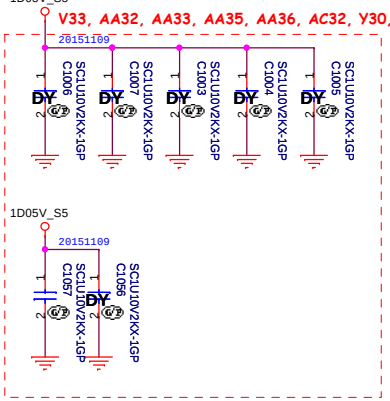
AF30, AG27, AG29, AG30, AJ27, AJ29, AJ30, AF29

PLACE ALL THE CAPS
UNDER THE PKG SHADOW



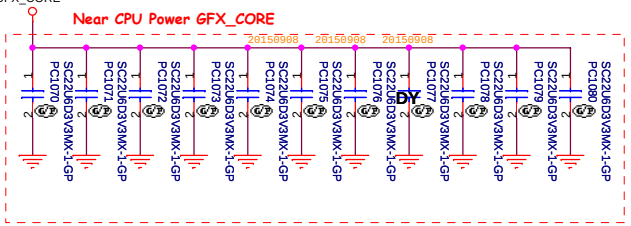
1D05V_S5

V33, AA32, AA33, AA35, AA36, AC32, Y30, Y32, Y33, Y35

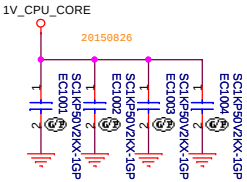


GFX_CORE

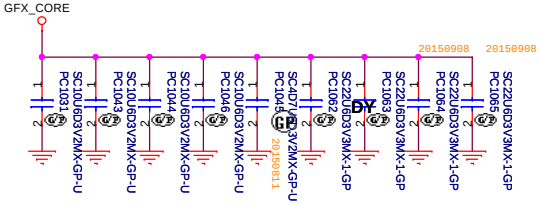
Near CPU Power GFX_CORE



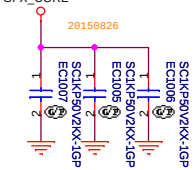
1V_CPU_CORE



GFX_CORE

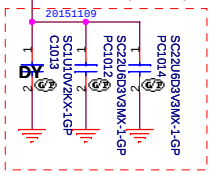


GFX_CORE



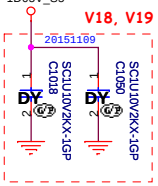
1D05V_S5

AM21, AM33, AM22, AN22, AN32, AM32



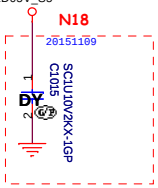
1D05V_S5

V18, V19



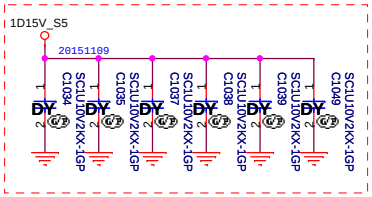
1D05V_S5

N18



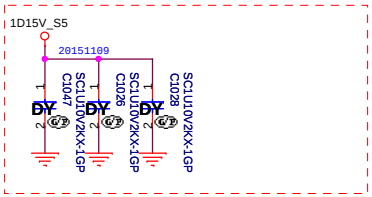
AK30 AK35 AK36 AM29

1D15V_S5



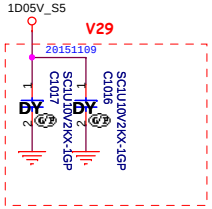
AM19 AK21

1D15V_S5



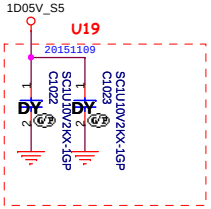
1D05V_S5

V29



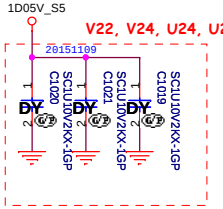
1D05V_S5

U19

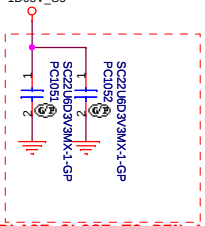


1D05V_S5

V22, V24, U24, U22, V27, U27

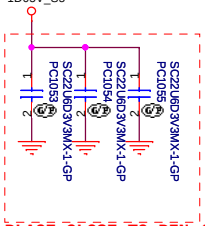


1D05V_S5



PLACE CLOSE TO PIN 1 OF RA

1D05V_S5



PLACE CLOSE TO PIN 1 OF RB

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Title: CPU (Power CAP1)

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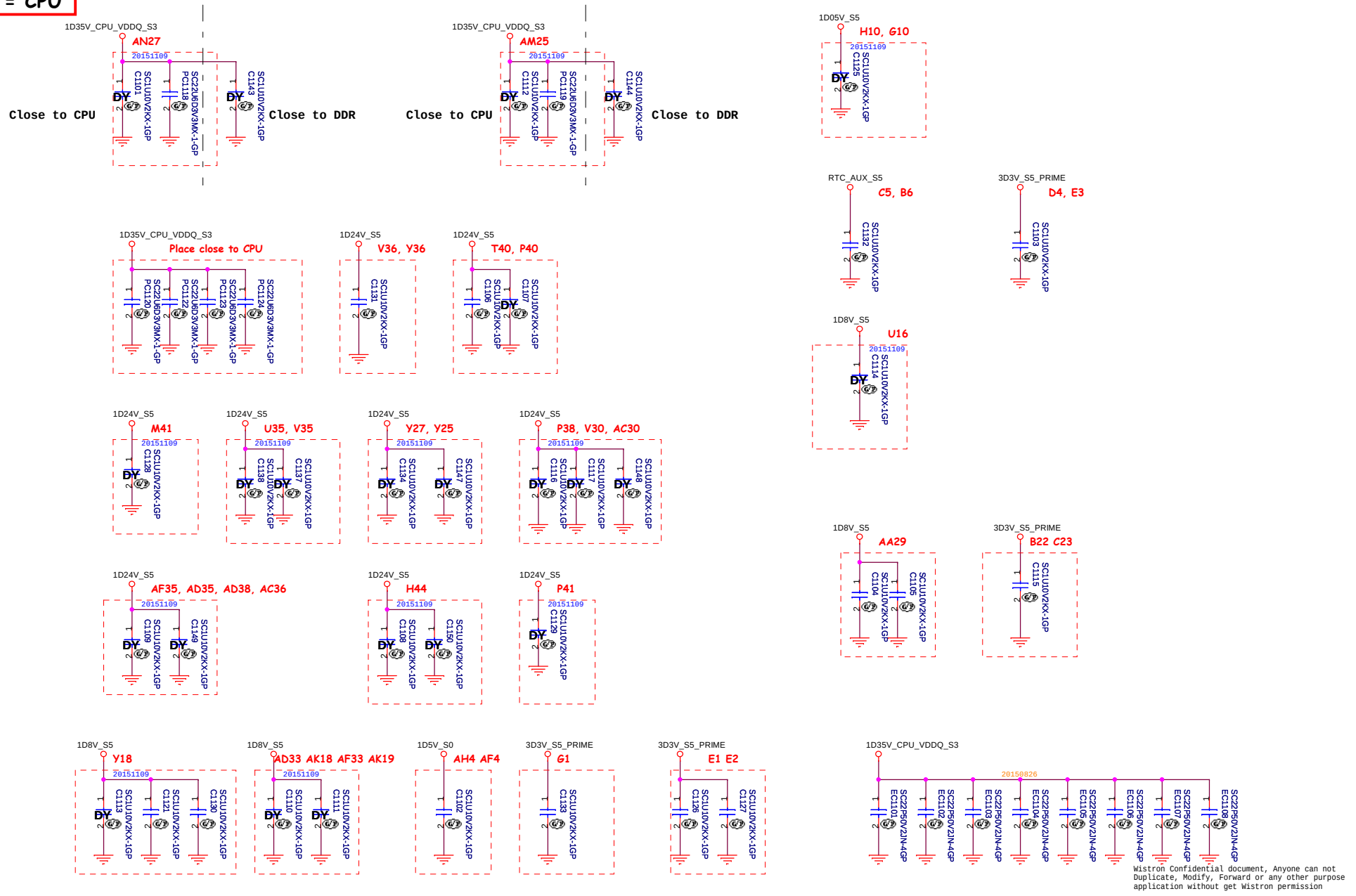
SSID = CPU



<Core Design>

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Title: *CPU (Power CAP2)*

Size	Document Number	Rev
A3	Rocket BSW 11.6"	A00

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SSID = MEMORY

P30

DIMM1

M_A_A[15:0] [5]

M_A_A0 M_A_A1 M_A_A2 M_A_A3 M_A_A4 M_A_A5 M_A_A6 M_A_A7 M_A_A8 M_A_A9 M_A_A10 M_A_A11 M_A_A12 M_A_A13 M_A_A14 M_A_A15

[5] M_A_BS2 [5] M_A_BS0 [5] M_A_BS1

M_A_DQ[63:0] [5]

M_A_DQS_DN[7:0] [5]

M_A_DQS_DP[7:0] [5]

M_A_DIM0_ODT0 [5] M_A_DIM0_ODT1 [5]

VREF_CA VREF_DQ

[5] SM_DRAMRST#

0D675V_VREF_S0

NP1 NP2

RAS# WE# CAS# → M_A_RAS# [5] M_A_WE# [5] M_A_CAS# [5]

CS0# CS1# → M_A_CS#0 [5] M_A_CS#1 [5]

CKE0 CKE1 → M_A_CKE0 [5] M_A_CKE1 [5]

CK0 CK0# → M_A_CLK0 [5] M_A_CLK#0 [5]

CK1 CK1# → M_A_CLK1 [5] M_A_CLK#1 [5]

DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7 → M_A_DM0 [5] M_A_DM1 [5] M_A_DM2 [5] M_A_DM3 [5] M_A_DM4 [5] M_A_DM5 [5] M_A_DM6 [5] M_A_DM7 [5]

SDA SCL → PCU_SMB_DATA [16] PCU_SMB_CLK [16]

EVENT# → TS# DIMM0 1 → TP1201 TPAD14-OP-GP

VDDSPD → 3D3V_S0

SA0 SA1 → SA0 DIM0 = 0, SA1 DIM0 = 0

NC#1 NC#2 NC#/TEST → 1D35V_CPU_VDDQ_S3

VDD1–VDD18 → 1D35V_CPU_VDDQ_S3

VSS

VTT1 VTT2 → 0D675V_VREF_S0

SKT_DDR 204P SMD

DDR3-204P-262-GP-U

62.10024.S21

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

9/10 Remove R1208~1211

9/10 Remove R1201 [Thermal Event]

C1208 SCD1U16V2KX-3GP C1202 SCD1U16V2KX-3GP

Layout Note:
Place these Caps near SO-DIMMA.

1D35V_CPU_VDDQ_S3

20151109

SODIMM A DECOUPLING

C1203 C1204 C1205 C1206 C1207 C1221 C1222 C1223 SCD1U06V2KX-3GP

C1209 C1210 SCD1U10V2KX-1GP C1211 C1212 SCD1U10V2KX-1GP

Layout Note:
Place these capsclose to VTT1 and VTT2.

0D675V_VREF_S0

20158828

C1214 C1215 C1216 C1217 SCD1U10V2KX-1GP C1219 SCD10U6D3V2MX-GP C1220 SCD10U6D3V2MX-GP

1D35V_CPU_VDDQ_S3

C1218 C1224 C1225 C1226 SCD1U16V2KX-1GP C1227 SCD1U16V2KX-1GP

Reseve 0.1uF for ESD

For Intel Recommend Close to DIMM(Braswell)

1D35V_CPU_VDDQ_S3

R1202 4K7R2F-GP

R1203 0R0402-PAD

VREF_DQ VREF_DQ_R1203

R1204 4K7R2F-GP

C1213 SCD1U16V2KX-3GP

For Intel Recommend Close to DIMM(Braswell)

1D35V_CPU_VDDQ_S3

R1205 4K7R2F-GP

R1207 0R0402-PAD

VREF_CA VREF_CA_R1207

R1206 4K7R2F-GP

C1201 SCD1U16V2KX-3GP

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1

Size: A2 | Document Number: Rocket BSW 11.6" | Rev: A00

Date: Tuesday, November 10, 2015 | Sheet 12 of 109

SSID = MEMORY

Blanking

<Core Design>

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Title

(Reserved)

Size	Document Number	Rev
A4	Rocket BSW 11.6"	X00

Date: Monday, September 21, 2015 Sheet 13 of 109

SSID = CPU

Blanking

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

Size	Document Number	Rev
A4	Rocket BSW 11.6"	X00

Date: Monday, September 21, 2015 Sheet 14 of 109

SSID = STRAP

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC
SHOULD BE PLACED OUTSIDE KOZ AREA

All the straps are sampled on the rising edge of the PMC_RSMRST_N signal (check list)

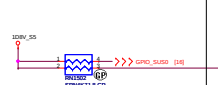
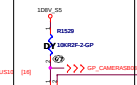
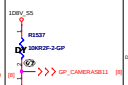
Description	DDI0_Detected	DDI1_Detected	A16 Swap Override	DSI Display Detected	Boot BIOS Strap BBS	Flash Descriptor Security Override	DFX Boot Halt Strap & VISA Early POSM Debug Enable	DFX Sus Debug Strap	ICLK, USB2, DDI SFR Supply Select	ICLK SFR Bypass	POSM Select	ICLK Xtal OSC Bypass	CCU SUS RO Bypass	RTC OSC bypass
GPIO	GPIO_SUS0	GPIO_SUS1	GPIO_SUS2	GPIO_SUS3	GPIO_SUS4	GPIO_SUS5	GPIO_SUS6	GPIO_SUS7	SEC_GPIO_SUS8	SEC_GPIO_SUS9	SEC_GPIO_SUS10	GP_CAMERASB08	GP_CAMERASB09	GP_CAMERASB11
Schematic						Stuff for production 								
High	DDI0 Detect	DDI1 Detect	Normal Operation	DSI Detect	Boot from SPI	Weak internal pull-up Normal Operation	Normal	Weak internal pull-up Normal	1.35V	Weak internal pull-up Bypass with 1.05V	PMC	Bypass	Bypass	Bypass
Low	Disable	Disable	Change Boot Loader address (A16 Override)	Disable Weak internal pull-down	Boot from LPC	Override	Halt boot enable	Sus Debug enable	1.25V	No bypass	Fuse controller Weak internal pull-down	No bypass	No bypass	No bypass

Table 29. Straps (Sheet 1 of 2)

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[0]	DDI0 Detect	Weak internal pull-down	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
GPIO_SUS[1]	DDI1 Detect	Weak internal pull-down	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected
GPIO_SUS[2]	A16 swap overdrive	Weak internal pull-up	Top Swap (A16 Override) 0 = Change Boot Loader address 1 = Normal Operation
GPIO_SUS[4]	Boot BIOS Strap BBS	Weak internal pull-up	BIOS Boot Selection 0 = - 1 = SPI
GPIO_SUS[5]	Flash Descriptor Security Override	Weak internal pull-up	Security Flash Descriptors 0 = Override 1 = Normal Operation

Table 29. Straps (Sheet 2 of 2)

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[8]	ICLK, USB2, DDI SFR Supply Select	Weak internal pull-down	0 = Supply is 1.25V 1 = Supply is 1.35V This strap also contains PLL LDO 0: supply is 1.25V; 1: supply is 1.35V. Selects supply voltage for LDOs used for PLLs, thermal oscillators, USB2, iCLK and DDI
GPIO_SUS[9]	ICLK, USB2, DDI SFR Bypass	Weak internal pull-up	0 = No bypass 1 = Bypass with 1.05V
GPIO_SUS[10]	POSM Select	Weak internal pull-down	Selects which POSM will be observed at time 0 0 = Fuse controller 1 = PMC
GPIO_CAMERASB08	ICLK Xtal OSC Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass
GPIO_CAMERASB09	CCU SUS RO Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass
GPIO_CAMERASB11	RTC OSC Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass

CHV Straps [CRB] -- strap detect @ RSMRST# assertion

Purpose	CHV Pin Name (refer CHV symbol PIN)	PU/PD (internal - Week)	Options	Default State on board?
DDI0 Detected	GPIO_SUS0	PD	1 - DDI0 Detect, 0 - Disable	High
DDI1 Detected	GPIO_SUS1	PD	1 - DDI1 Detect, 0 - Disable	High
A16 swap override	GPIO_SUS2	PU	1- Default, 0- A16 override	High
DSI Display Detected	GPIO_SUS3	PD	1 - DSI detect, 0 - Disable	Low
Boot BIOS Strap BBS	GPIO_SUS4	PU	1 - Boot from SPI, 0 - Boot from LPC	High
Flash Descriptor Security Override	GPIO_SUS5	PU	1- Security enabled, 0 - Security disabled	High
DFX Boot Halt Strap & VISA Early POSM Debug Enable	GPIO_SUS6	PU	1 - normal, 0 - Halt boot enable	High
DFX Sus Debug Strap	GPIO_SUS7	PU	1- Normal, 0 - Sus Debug enable	High
ICLK, USB2, DDI SFR Supply Select-	SEC_GPIO_SUS8	PU	1 - 1.35V, 0 - 1.25V	Low
ICLK SFR Bypass	SEC_GPIO_SUS9	PD	1 - Bypass with 1.05V, 0 - No Bypass	Low
POSM Select	SEC_GPIO_SUS10	PD	1 - PMC, 0 - Fuse controller	Don't care, if GPIO_SUS6 is pulled high.
ICLK Xtal OSC Bypass	GP_CAMERASB08	PD	1 - Bypass, 0 - No bypass	Low
CCU SUS RO Bypass	GP_CAMERASB09	PD	1 - Bypass, 0 - No bypass	Low
RTC OSC Bypass	GP_CAMERASB11	PD	1 - Bypass, 0 - No bypass	Low

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Title: CPU(STRAP)

Size: A1 | Document Number: Rocket BSW 11.6" | Rev: X00

Date: Tuesday, October 08, 2013 | Sheet 15 of 100

SSID = PCH

Level shift

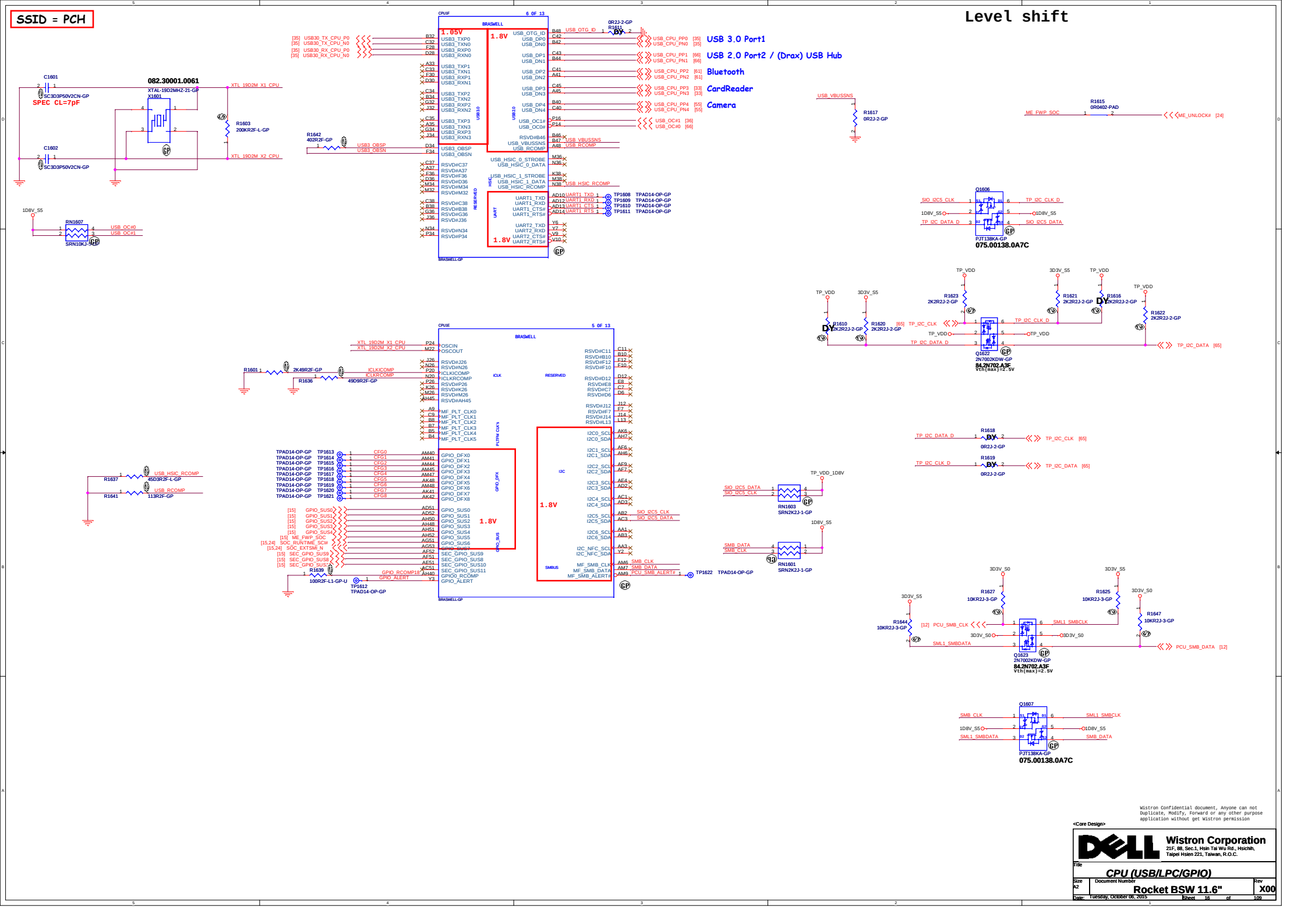
USB 3.0 Port1

USB 2.0 Port2 / (Drax) USB Hub

Bluetooth

CardReader

Camera



<Core Design>

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Title: CPU (USB/LPC/GPIO)

Size: A2 | Document Number: Rocket BSW 11.6" | Rev: X00

Date: Tuesday, October 06, 2015 | Sheet 16 of 109

SSID = CPU

Blanking

<Core Design>

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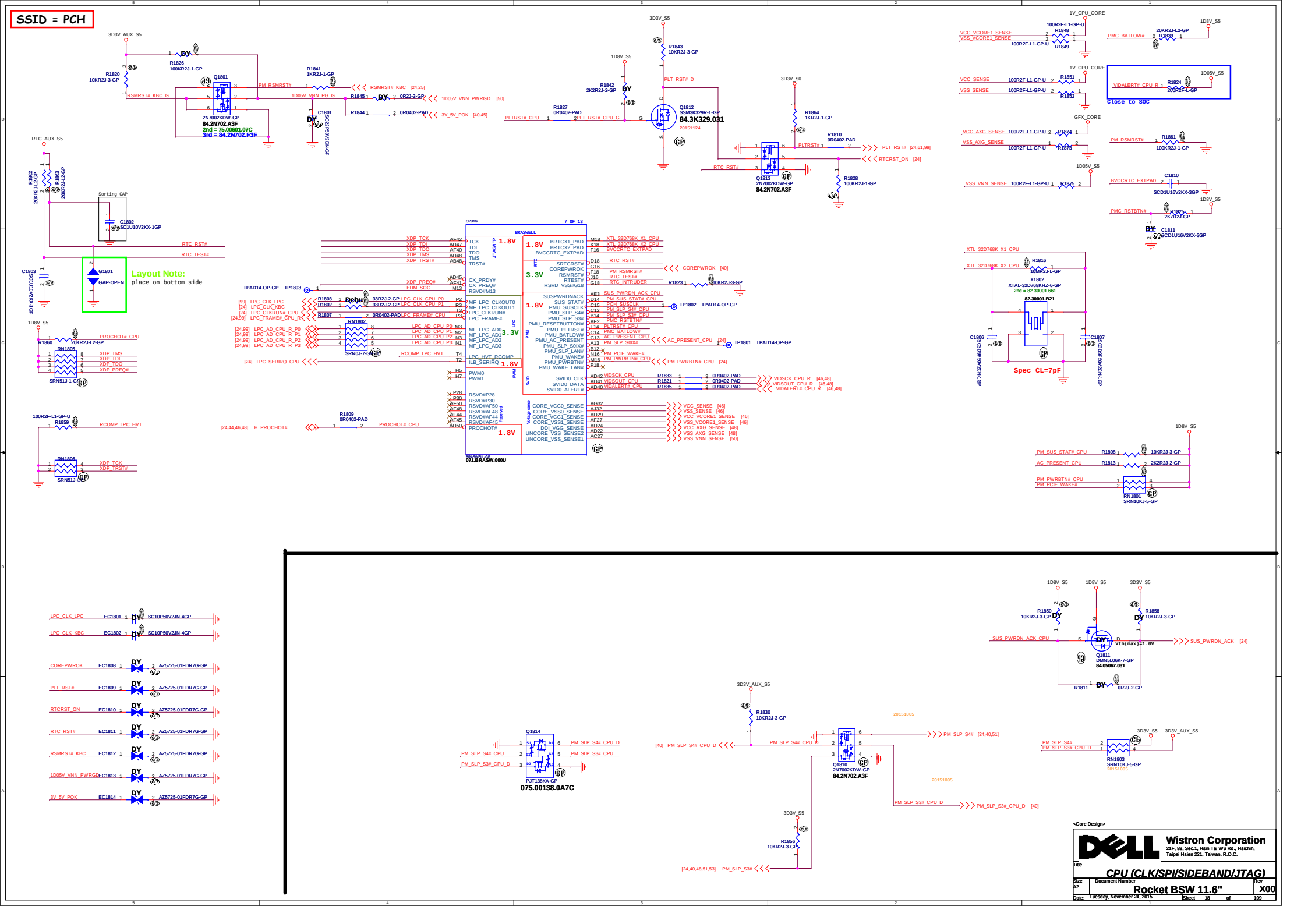
Title
(Reserved)

Size	Document Number	Rev
A4	Rocket BSW 11.6"	X00

Date: Monday, September 21, 2015 Sheet 17 of 109

SSID = PCH

Layout Note:
place on bottom side



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CLK/SPI/SIDEBAND/JTAG)

Size	Document Number	Rev
A2	Rocket BSW 11.6"	X00

Date: Tuesday, November 24, 2015 Sheet 18 of 109

SSID = PCH

WLAN
[61] PCIE_TX_CON_P0
[61] PCIE_TX_CON_N0
[61] PCIE_RX_CPU_P0
[61] PCIE_RX_CPU_N0

C1915 2 1 SCD1U16V2KX-3GP PCIE_TX_CPU_P0
C1916 2 1 SCD1U16V2KX-3GP PCIE_TX_CPU_N0

CPU1D 4 OF 13
BRASWELL
1.0V
PCIe
1.8V
SATA
1.8V
1.8V
FAST SPI
1.5V
AUDIO
1.8V
SPI
1.8V
BRASWELL-GP

HDD
SATA_TX_CPU_P0 [60]
SATA_TX_CPU_N0 [60]
SATA_RX_CPU_P0 [60]
SATA_RX_CPU_N0 [60]
SATA_LED# [24]
SATA_DEVSLP_SOC
SATA_GP3
TP1901 TPAD14-OP-GP
SATA_OBSP
SATA_OBSN
R1931 1 402R2F-GP

1D8V_S0
20150818
R1908
10KR2J-3-GP
DY
SATA_LED#

PEG_CLKREQ0_CPU#
PEG_CLKREQ1_CPU#
PEG_CLKREQ2_CPU#
PEG_CLKREQ3_CPU#

[61] PEG_CLK0_CPU
[61] PEG_CLK0_CPU#

R1930
402R2F-GP
PCIE_OBSP_CPU
PCIE_OBSN_CPU

SPI_CLK_CPU R1911 10R2J-2-GP SPI_CLK_ROM [25]
SPI_CS_CPU_N0 R1909 33R2J-2-GP SPI_CS_ROM_N0 [25]
SPI_SI_CPU R1910 10R2J-2-GP SPI_SI_ROM [25]
SPI_SO_CPU [25]
SPI_WP_CPU [25]
SPI_HOLD_CPU [25]

HDA_RST# CPU
HDA_BITCLK_CPU
HDA_SDIN0_CPU [27]
HDA_SYNC_CPU
HDA_SDOUT_CPU
HDA_SPKR [27]

1D8V_S5
RN1901 SRN10KJ-5-GP
PEG_CLKREQ1_CPU#
PEG_CLKREQ2_CPU#
RN1902 SRN10KJ-5-GP
PEG_CLKREQ0_CPU#
PEG_CLKREQ3_CPU#

HDA_RST# CPU
C1910 SC22P50V2JN-4GP

HDA_RST# CPU R1928 75R2F-2-GP HDA_RST#_CODEC [27,29]
HDA_BITCLK_CPU R1927 75R2F-2-GP HDA_BITCLK_CODEC [27]
HDA_SYNC_CPU R1926 75R2F-2-GP HDA_SYNC_CODEC [27]
HDA_SDOUT_CPU R1929 75R2F-2-GP HDA_SDOUT_CODEC [27]

1D8V_S0
R1906 100KR2J-1-GP
SATA_DEVSLP_SOC
1D8V_S0
3D3V_S0
R1907 10KR2J-3-GP
SATA_DEVSLP [60]
Q1902
SSM3K329R-1-GP
84.3K329.031
20151124

Remove?
VIL=0.35*1.8=0.63 V
3D3V_S5
R1902 10KR2J-3-GP
PEG_CLKREQ0_CPU#
D1901 BAS16-6-GP
PEG_CLKREQ0_D
3D3V_S0
Q1901 2N7002K-2-GP
84.2N702.J31
2ND = 084.27002.0A31
3rd = 84.07002.I31
3D3V_S0
R1904 10KR2J-3-GP
PEG_CLKREQ0_WLAN# [61]
PEG_CLKREQ0_CPU#
R1905 0R2J-2-GP

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (SATA/PCIE/IHDA)
Size: A3
Document Number: Rocket BSW 11.6"
Rev: X00
Date: Tuesday, November 24, 2015
Sheet 19 of 109

SSID = PCH

Blanking

<Core Design>

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Title

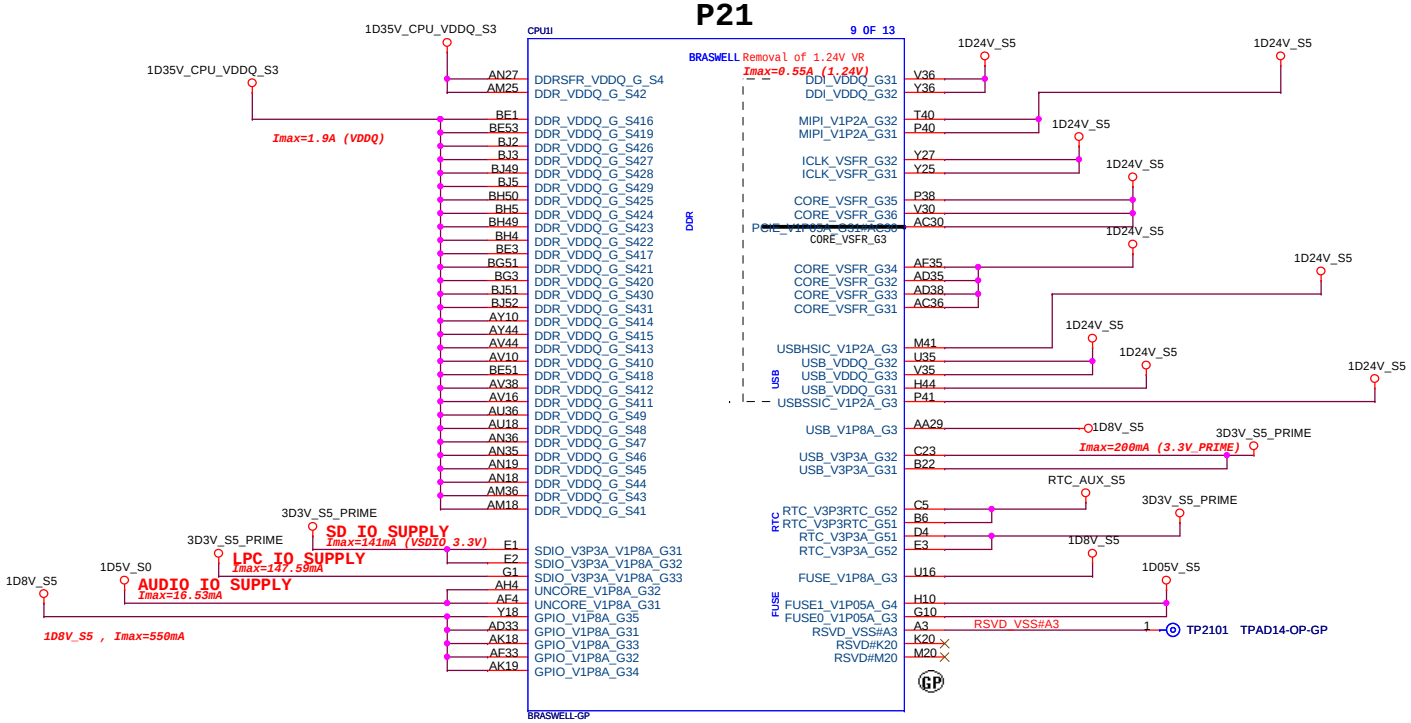
(Reserved)

Size	Document Number	Rev
A4	Rocket BSW 11.6"	X00

Date: Monday, September 21, 2015 Sheet 20 of 109

SSID = CPU

P21



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (POWER1)

Size: A3 | Document Number: Rocket BSW 11.6" | Rev: X00

Date: Monday, September 21, 2015 | Sheet 21 of 109

Blanking

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Title

(Reserved)

Size	Document Number	Rev
A4	Rocket BSW 11.6"	X00

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<Core Design>

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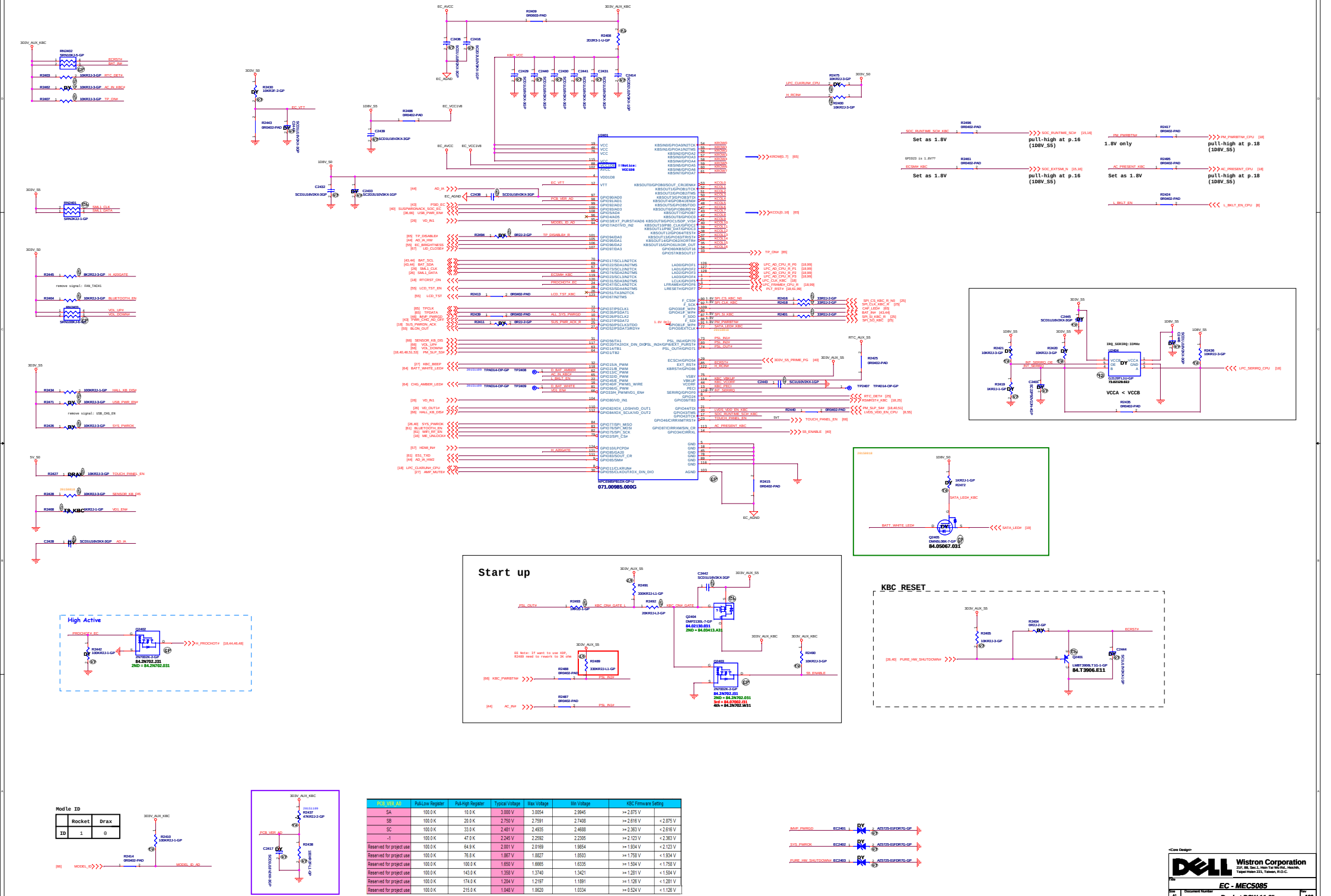
Title
(Reserved)

Size	Document Number	Rev
A4	Rocket BSW 11.6"	X00

Date: Monday, September 21, 2015 Sheet 23 of 109

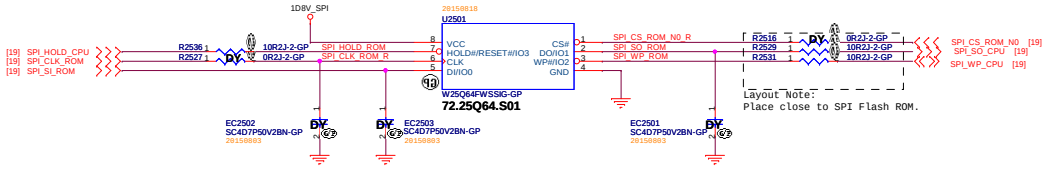
SSID = KBC



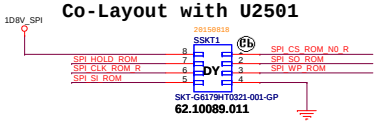
PCB_VER_A0	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	Min Voltage	KBC Firmware Setting	
SA	100.0 K	10.0 K	3.000 V	3.0054	2.9945	>= 2.875 V	
SB	100.0 K	20.0 K	2.750 V	2.7591	2.7408	>= 2.616 V	< 2.875 V
SC	100.0 K	33.0 K	2.481 V	2.4935	2.4688	>= 2.363 V	< 2.616 V
-1	100.0 K	47.0 K	2.245 V	2.2592	2.2305	>= 2.123 V	< 2.363 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.0169	1.9854	>= 1.934 V	< 2.123 V
Reserved for project use	100.0 K	76.8 K	1.867 V	1.8827	1.8503	>= 1.758 V	< 1.934 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.6665	1.6335	>= 1.504 V	< 1.758 V
Reserved for project use	100.0 K	143.0 K	1.358 V	1.3740	1.3421	>= 1.281 V	< 1.504 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.2197	1.1891	>= 1.126 V	< 1.281 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.0620	1.0334	>= 0.524 V	< 1.126 V

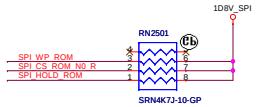
SSID = Flash.ROM

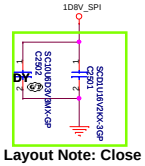
SPI FLASH ROM (8M byte) for CPU



SPI ROM socket Co-Layout with U2501

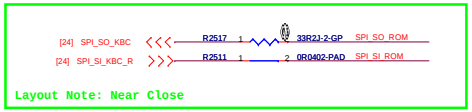




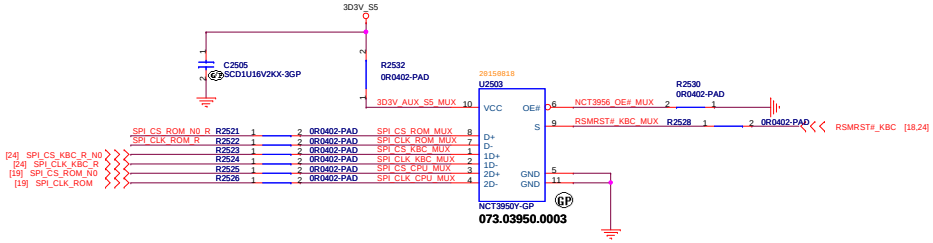


Layout Note: Close to U2501 Pin 8

SPI ROM link to KBC



High Speed Switch for Share ROM

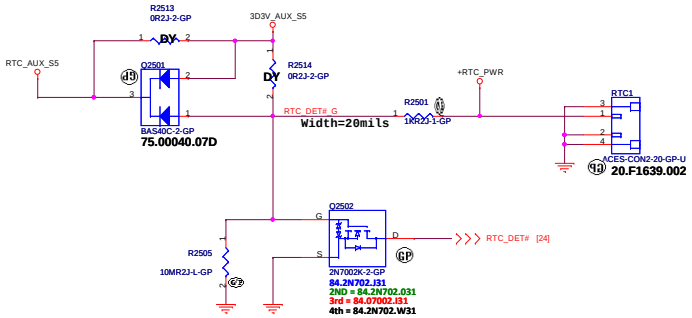


5240626:SPI Signals do not get tri-stated / MUX Sol.

Truth Table

OE#	S	D+	D-	Function
H	X	Hi-Z	Hi-Z	Disable
L	L	1D+	1D-	D=1D
L	H	2D+	2D-	D=2D

SSID = RTC



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Title: Flash/RTC
Size: A2
Document Number: Rocket BSW 11.6"
Rev: X00
Date: Thursday, October 15, 2015
Sheet 25 of 109

SSID = Thermal

EE Note:
1. T8: PURE_HW_SHUTDOWN# through Q2603.
2. THM_SENSOR: Thermal sensor NCT7718W solution.

Layout notice :
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

84.T3904.H11

2.System Sensor, Put on palm rest

1.H/W T8 Shutdown

Thermal sensor NCT 7718W

The default value is trapping after power up 100ms by different pull-up resistors of T_CRIT# and ALERT# pin:

TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

Close to Thermal sensor

EE Note:
R2608 need to fine tune base on thermal test.

Close to KBC
VD_IN1 for system thermal sensor

pull-high at p.24 (3D3V_S5)

Layout Note: Close U2601

<Core Design>

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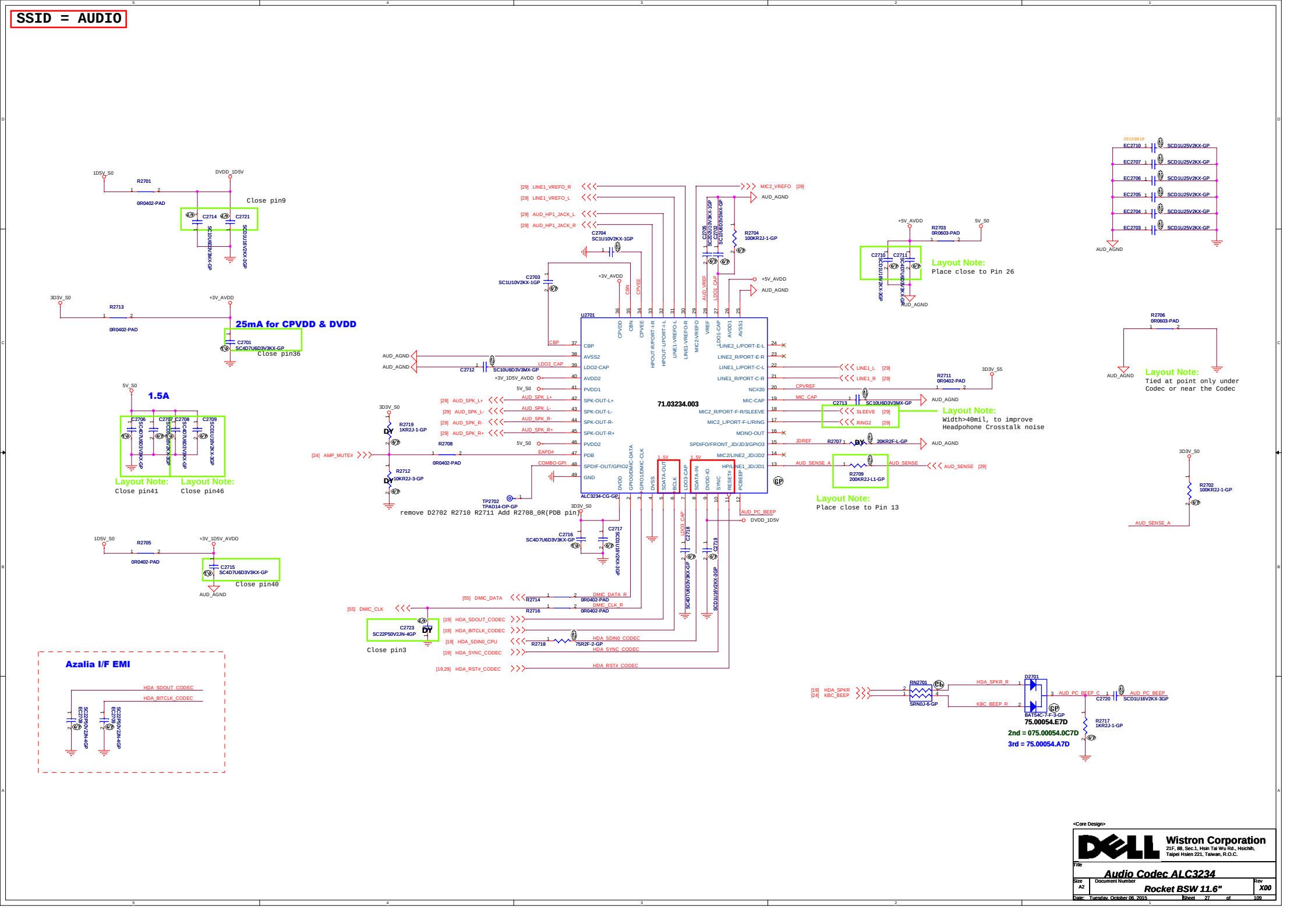
Title: Thermal
Size: A3
Document Number: Rocket BSW 11.6"
Rev: X00
Date: Thursday, October 15, 2015
Sheet 26 of 109

SSID = AUDIO



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec ALC3234

Size	Document Number	Rev
A2	Rocket BSW 11.6"	X00

Date: Tuesday, October 06, 2015 Sheet 27 of 109

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<Core Design>

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Title

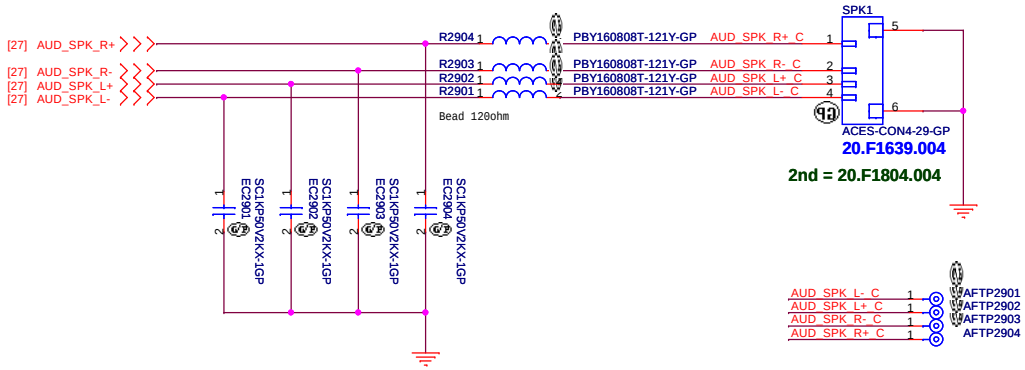
(Reserved)

Size	Document Number	Rev
A4	***Rocket BSW 11.6"***	***X00***

Date: Monday, September 21, 2015 Sheet 28 of 109

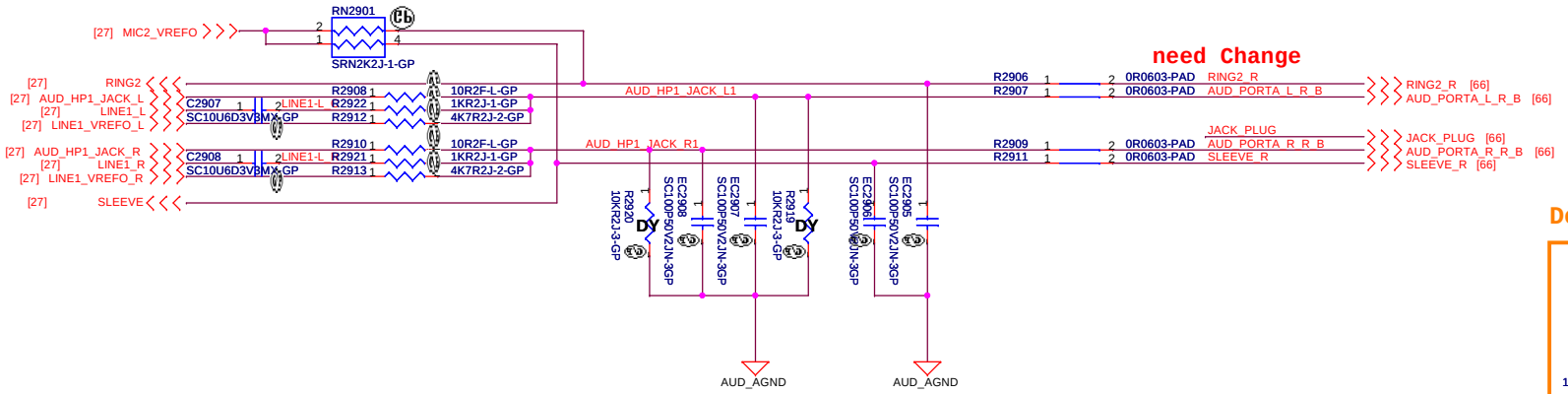
SSID = AUDIO

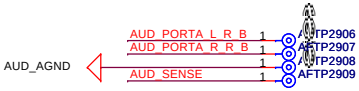
Speaker



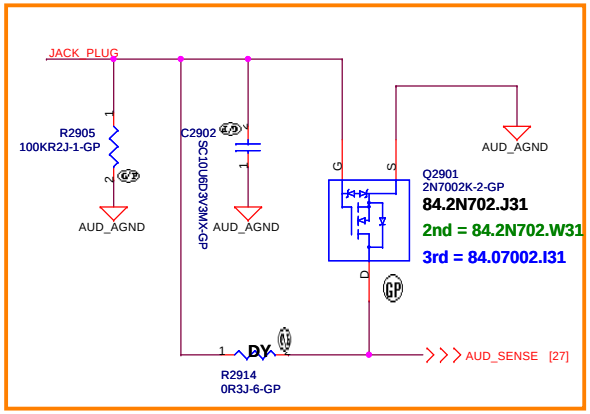
CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L_

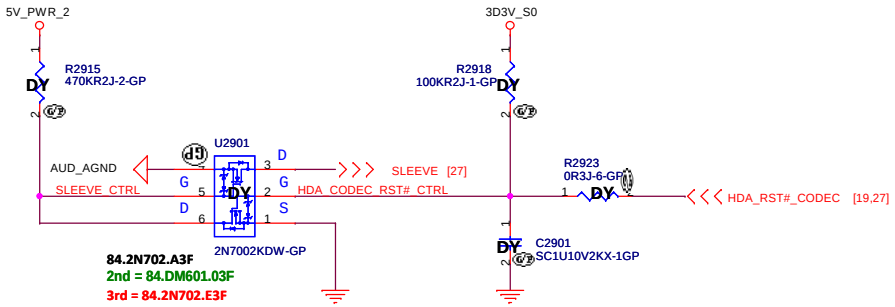
Combo Jack





Delay circuit





<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Speaker/HPMIC CONN

Size	Document Number	Rev
A3	Rocket BSW 11.6"	X00

Date: Thursday, October 15, 2015 Sheet 29 of 109

SSID = LOM

Blanking

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)LOM

Size	Document Number	Rev
A4	*Rocket BSW 11.6"*	*X00*

Date: Monday, September 21, 2015 Sheet 30 of 109

SSID = LAN

Blanking

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)LAN*

Size	Document Number	Rev
A4	Rocket BSW 11.6"	X00

Date: Monday, September 21, 2015 Sheet 31 of 109

SSID = LAN CONN

Blanking

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

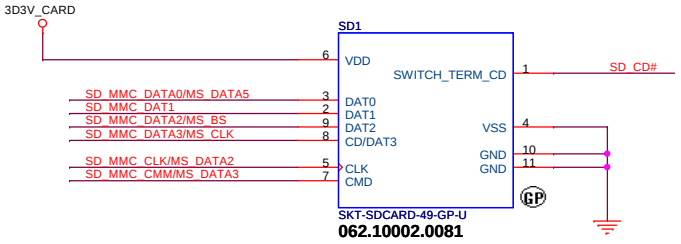
Title: (Reserved)RJ45+Transformer

Size	Document Number	Rev
A4	Rocket BSW 11.6"	X00

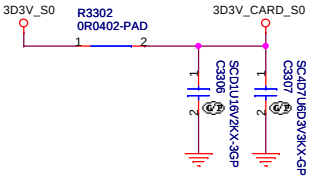
Date: Monday, September 21, 2015 Sheet 32 of 109

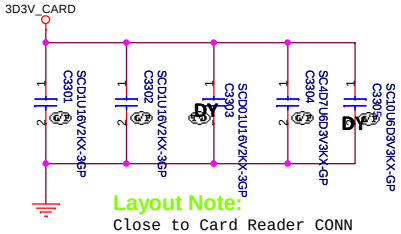
SSID = Card Reader

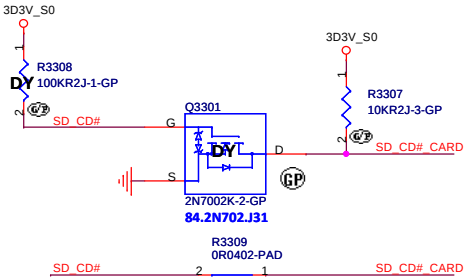
SD Card Connector

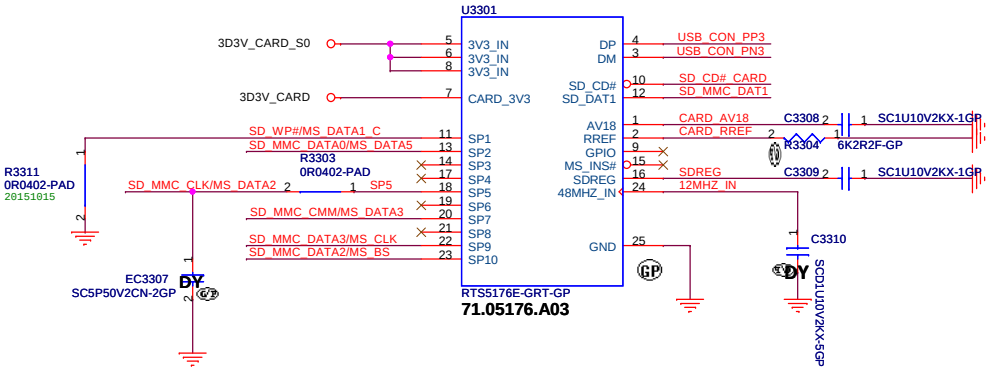


Pin	Define
P1	SWITCH TERM CD
P2	DAT1
P3	DAT0
P4	VSS
P5	CLK
P6	VDD
P7	CMD
P8	CD/DAT3
P9	DAT2
P10	GND
P11	GND

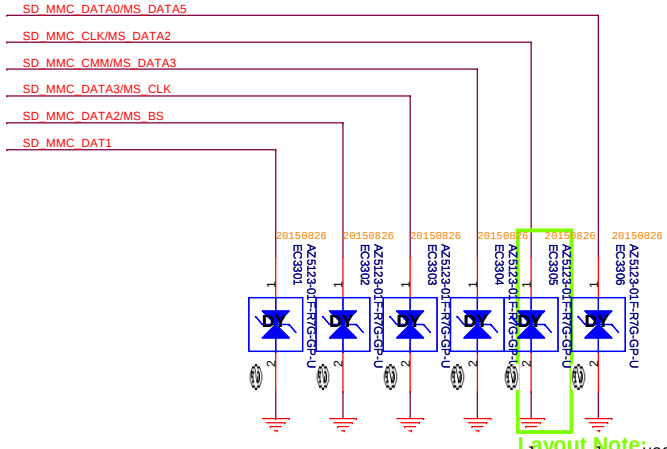




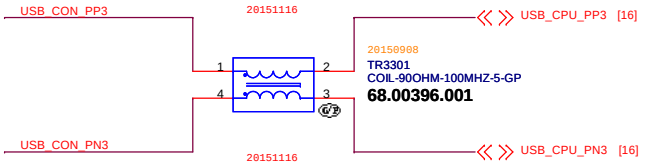




For EMI Reserved



Pin name	Net name
SD_DAT1	SD_MMC_DAT1
SP1	SD_WP/MS_DATA1
SP2	SD_MMC_DATA0/MS_DATA5
SP3	MMC_DATA7/MS_DATA4
SP4	MMC_DATA6/MS_DATA0
SP5	SD_MMC_CLK/MS_DATA2
SP6	MMC_DATA5/MS_DATA6
SP7	SD_MMC Command/MS_DATA3
SP8	MMC_DATA4/MS_DATA7
SP9	SD_MMC_DATA3/MS_CLK
SP10	SD_MMC_DATA2/MS_BS



<Core Design>

Wistron Corporation
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Title	Card Reader + CONN	
Size A3	Document Number Rocket BSW 11.6"	Rev X00
Date: Tuesday, November 17, 2015	Sheet 33 of 109	

SSID = USB

Blanking

<Core Design>

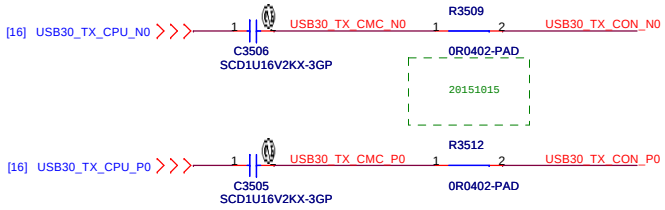
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

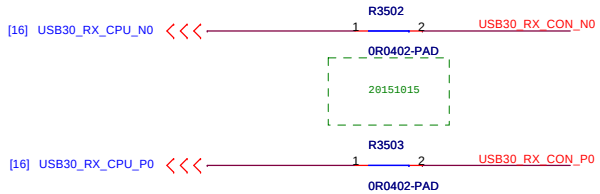
Title: *(Reserved)USB 2.0 Port*

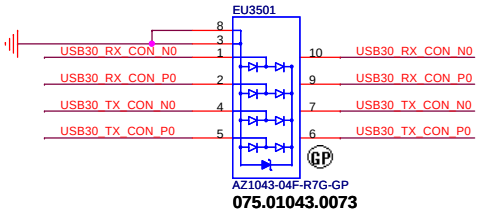
Size	Document Number	Rev
A4	*Rocket BSW 11.6"*	*X00*

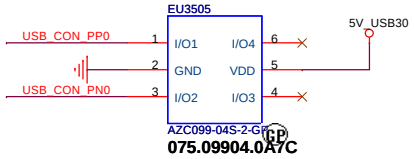
Date: Monday, September 21, 2015 Sheet 34 of 109

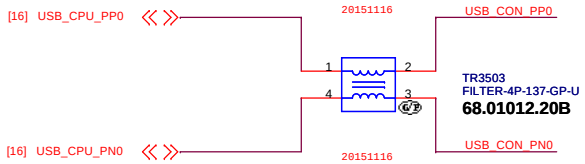
SSID = USB

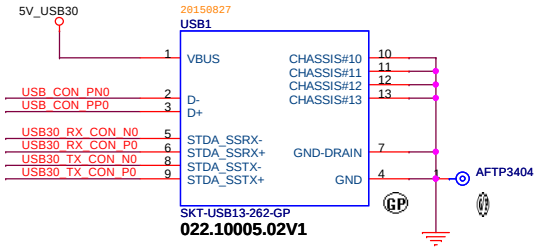


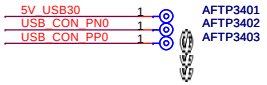






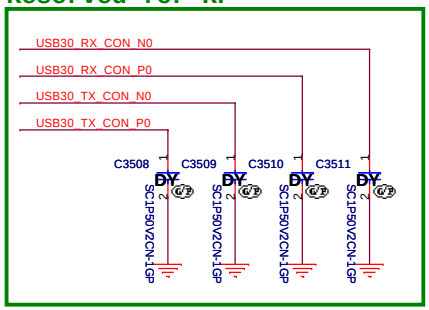






USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

Reserved for RF



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Title: USB3.0 CONN

Size | Document Number: Rocket BSW 11.6" | Rev: A00

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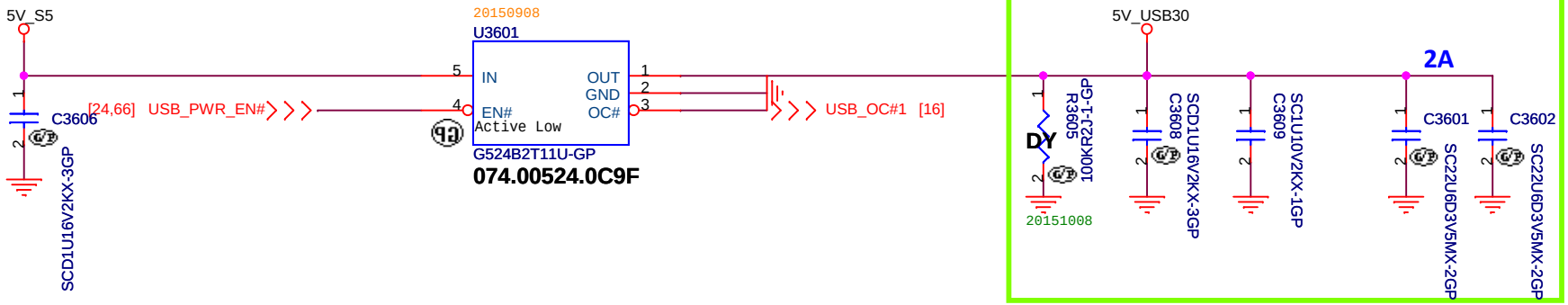
USB3.0 Port1



<Core Design>

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Title	***USB Power SW***	
Size: A4	Document Number: ***Rocket BSW 11.6"***	Rev: ***X00***
Date: Thursday, October 08, 2015	Sheet 36 of 109	

SSID = USB

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<Core Design>

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Title

USB2.0 HUB

Size	Document Number	Rev
A4	Rocket BSW 11.6"	X00

Date: Monday, September 21, 2015 Sheet 37 of 109

Blanking

<Core Design>

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Title

(Reserved)

Size	Document Number	Rev
A4	**Rocket BSW 11.6"**	X00

Date: Monday, September 21, 2015 Sheet 38 of 109

Blanking

<Core Design>

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Title

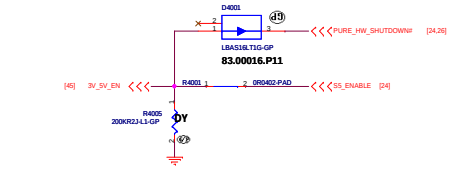
(Reserved)

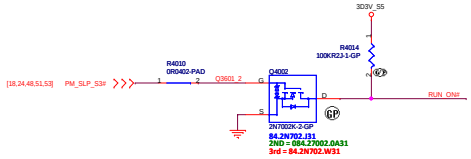
Size	Document Number	Rev
A4	*Rocket BSW 11.6"*	*X00*

Date: Monday, September 21, 2015 Sheet 39 of 109

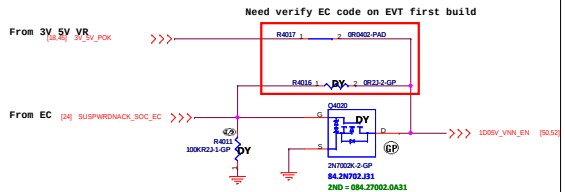
SSID = Reset.Suspend

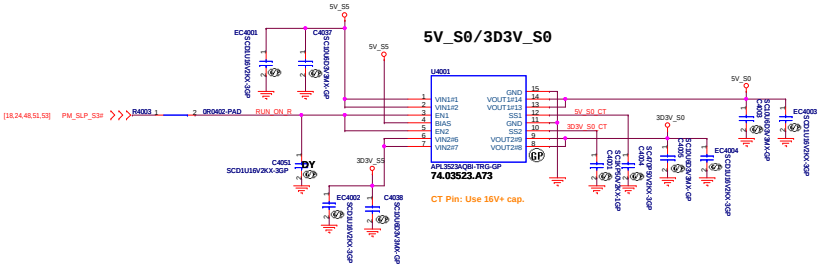
Power Sequence

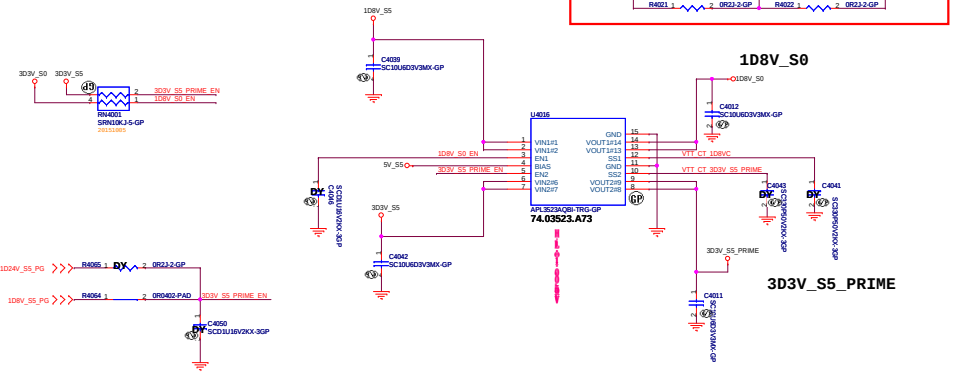




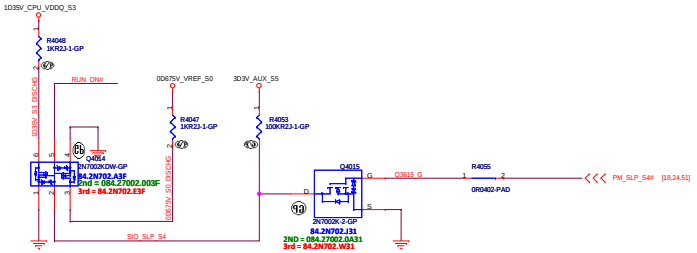
Need verify EC code on EVT first build

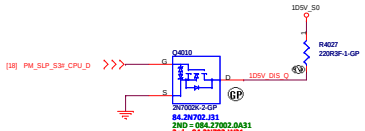


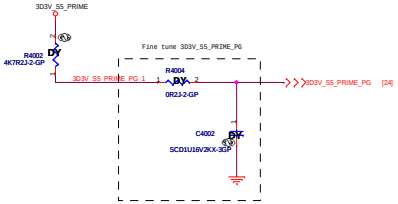




Discharge circuit

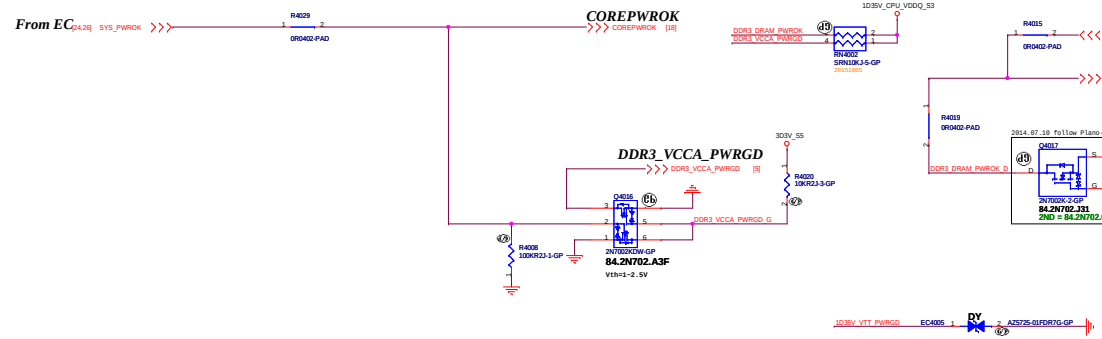






Power Sequence

DDR3_VCCA_PWRGD



DDR3_DRAM_PWROK

<Core Design>

Wistron Corporation
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Title: Power Plane Enable

Size	Document Number	Rev
Custom	Rocket BSW 11.6"	X00

Date: Tuesday, October 06, 2015 Sheet 40 of 109

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<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A4	*Rocket BSW 11.6"*	*X00*

Date: Monday, September 21, 2015 Sheet 41 of 109

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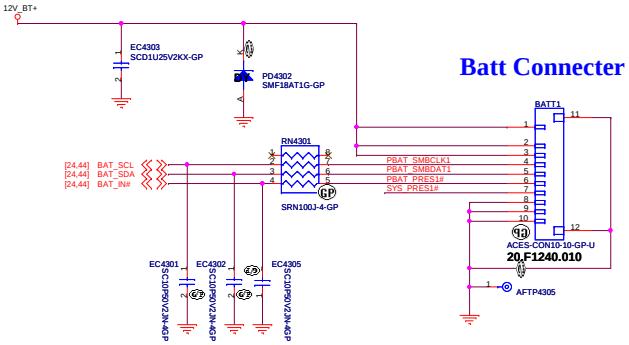
<Core Design>

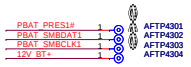
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***(Reserved)***	
Size: A4	Document Number: ***Rocket BSW 11.6"***	Rev: ***X00***
Date: Monday, September 21, 2015	Sheet 42 of 109	

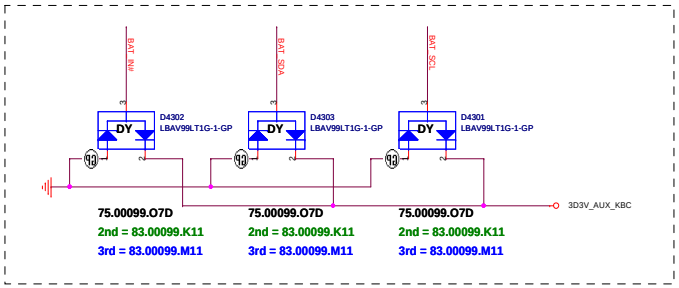
SSID = PWR.Support

Batt Connecter





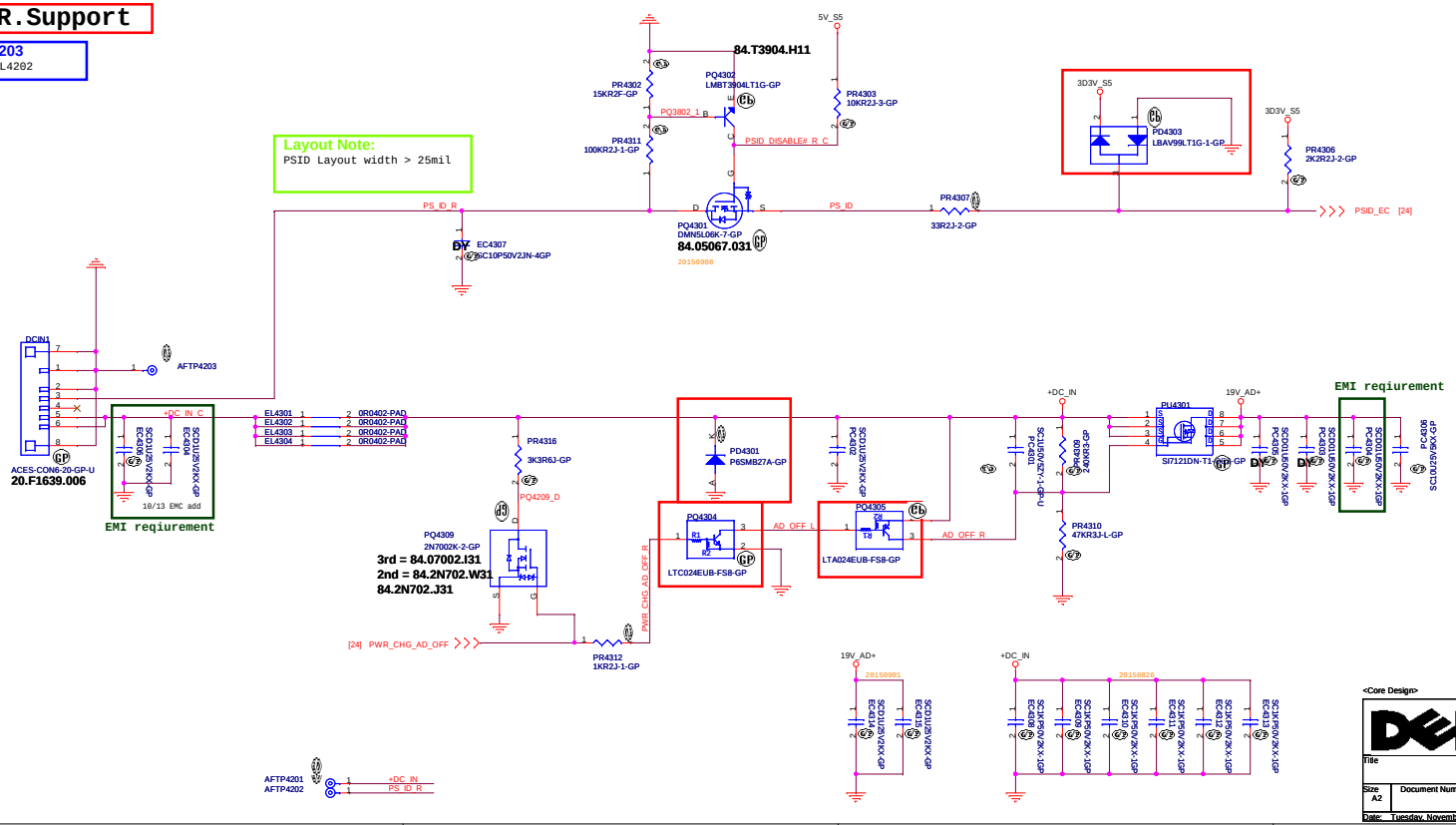
Placement: Close to Batt Connector



SSID = PWR.Support

0103 Add EC4203
ndde close to EL4202

Layout Note:
PSID Layout width > 25mil



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BATTERY CONN

Size	Document Number	Rev
A2	Rocket BSW 11.6"	A00

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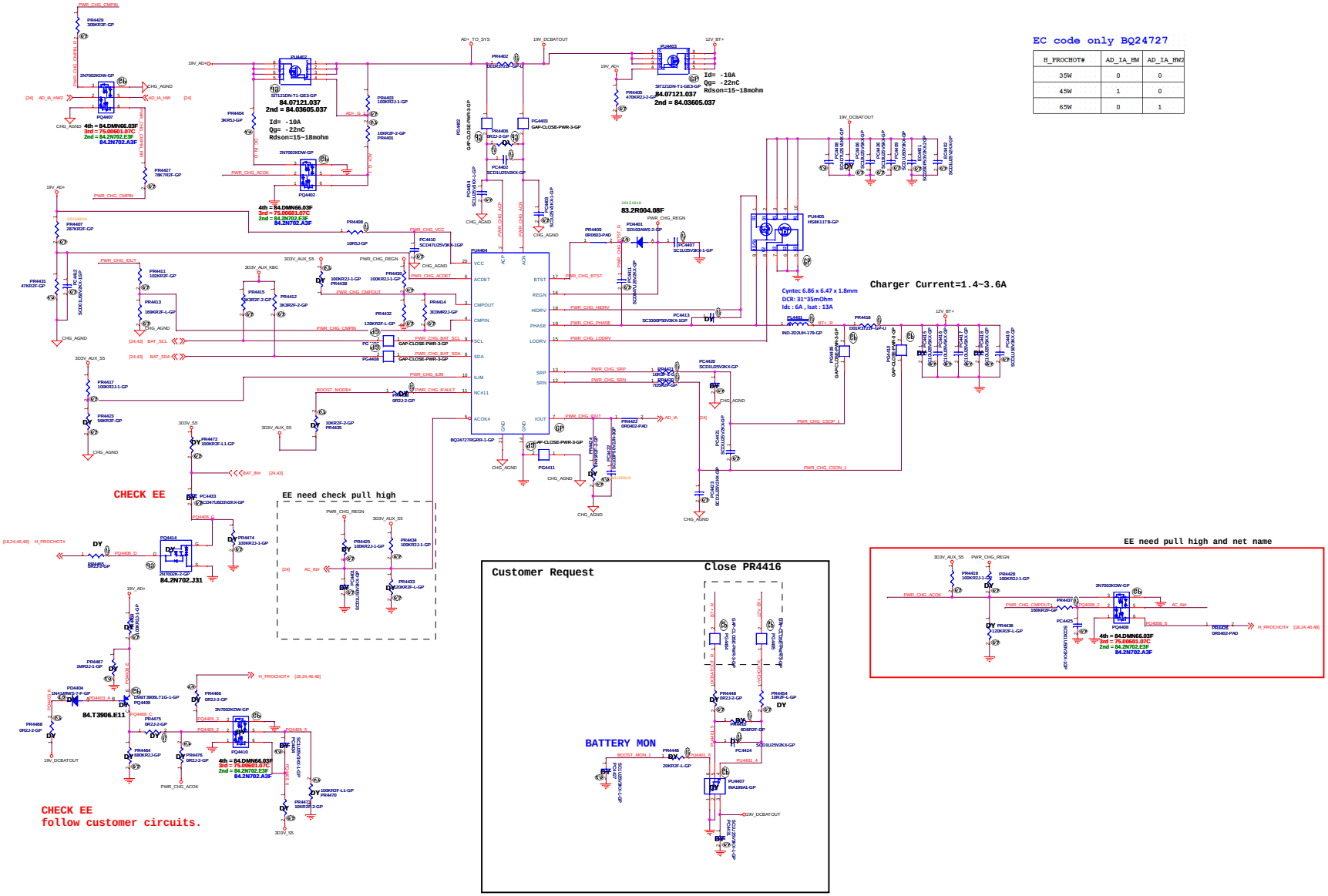
Main Func = Charger



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGE(BQ24727)

Size: A1 | Document Number: Rocket BSW 11.6" | Rev: X00

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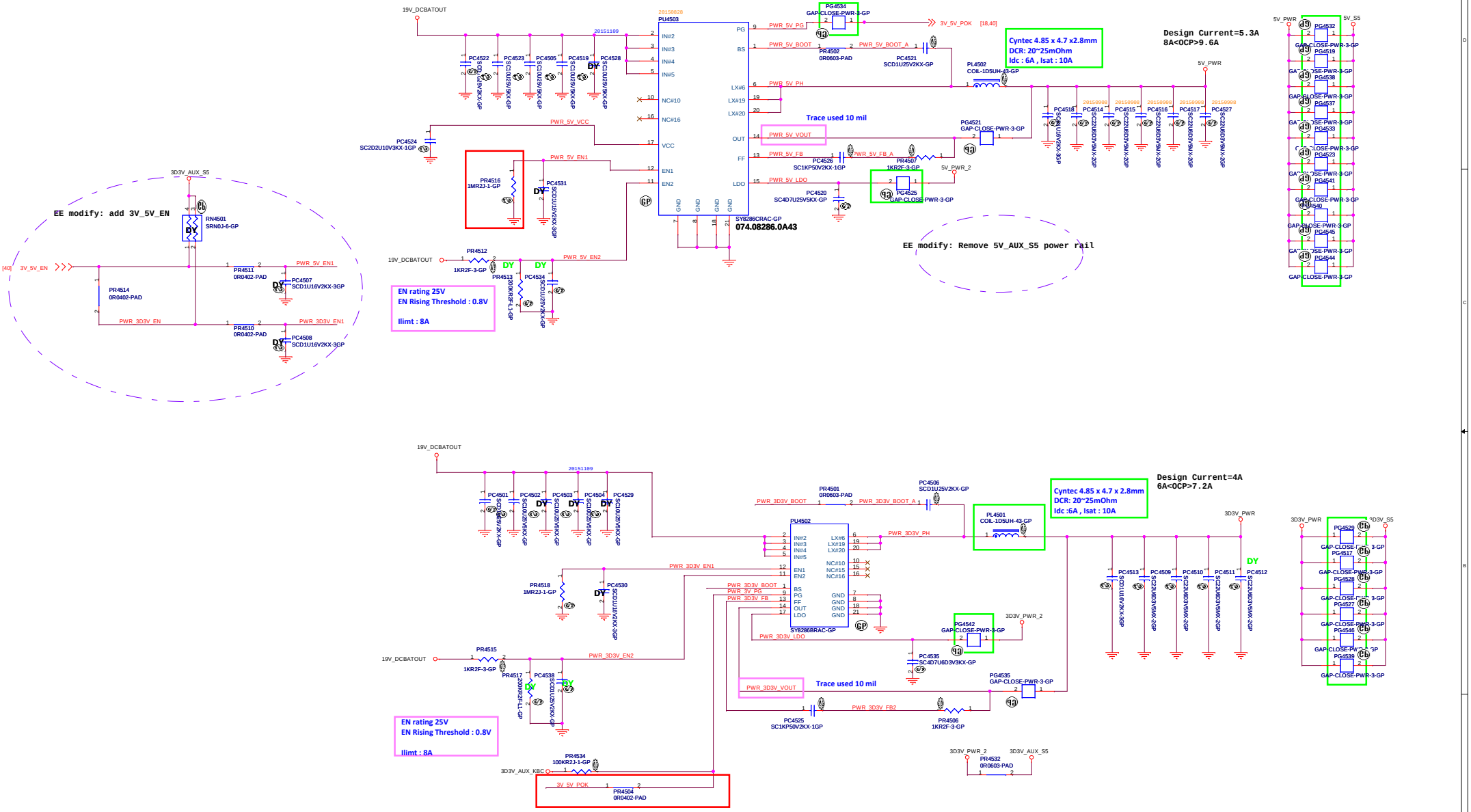


<Core Design>

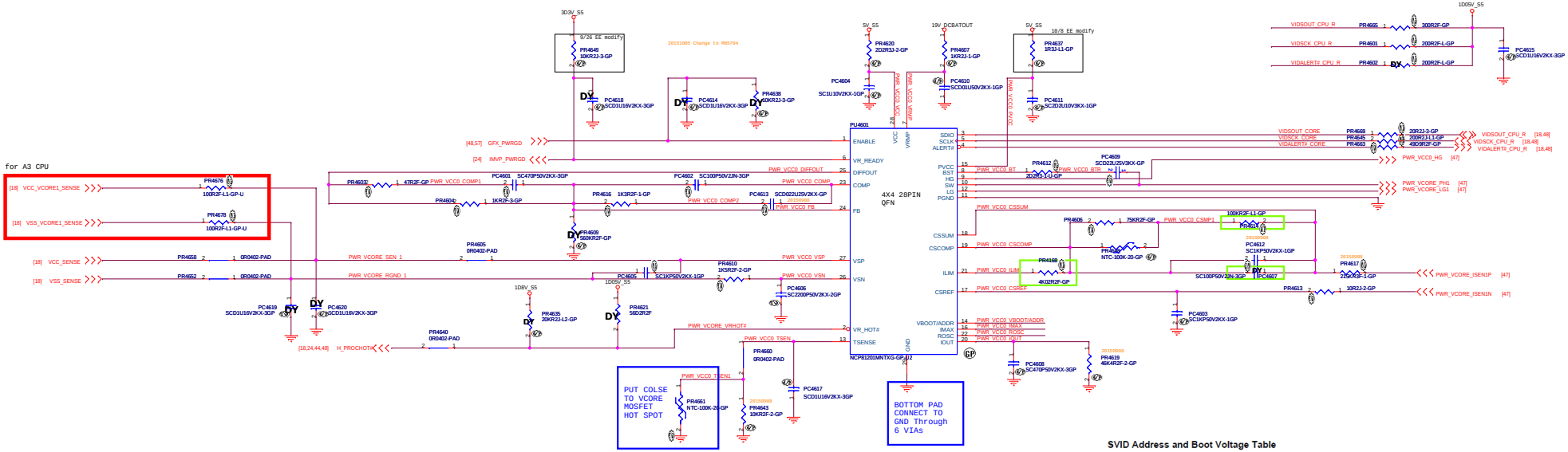
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 5V/3D3V SYN256B/SYN258C

Size: A2 | Document Number: Rocket BSW 11.6" | Rev: A00

Date: Tuesday, November 10, 2015 | Sheet 45 of 109

SSID = CPU Regulator



SVID Address and Boot Voltage Table

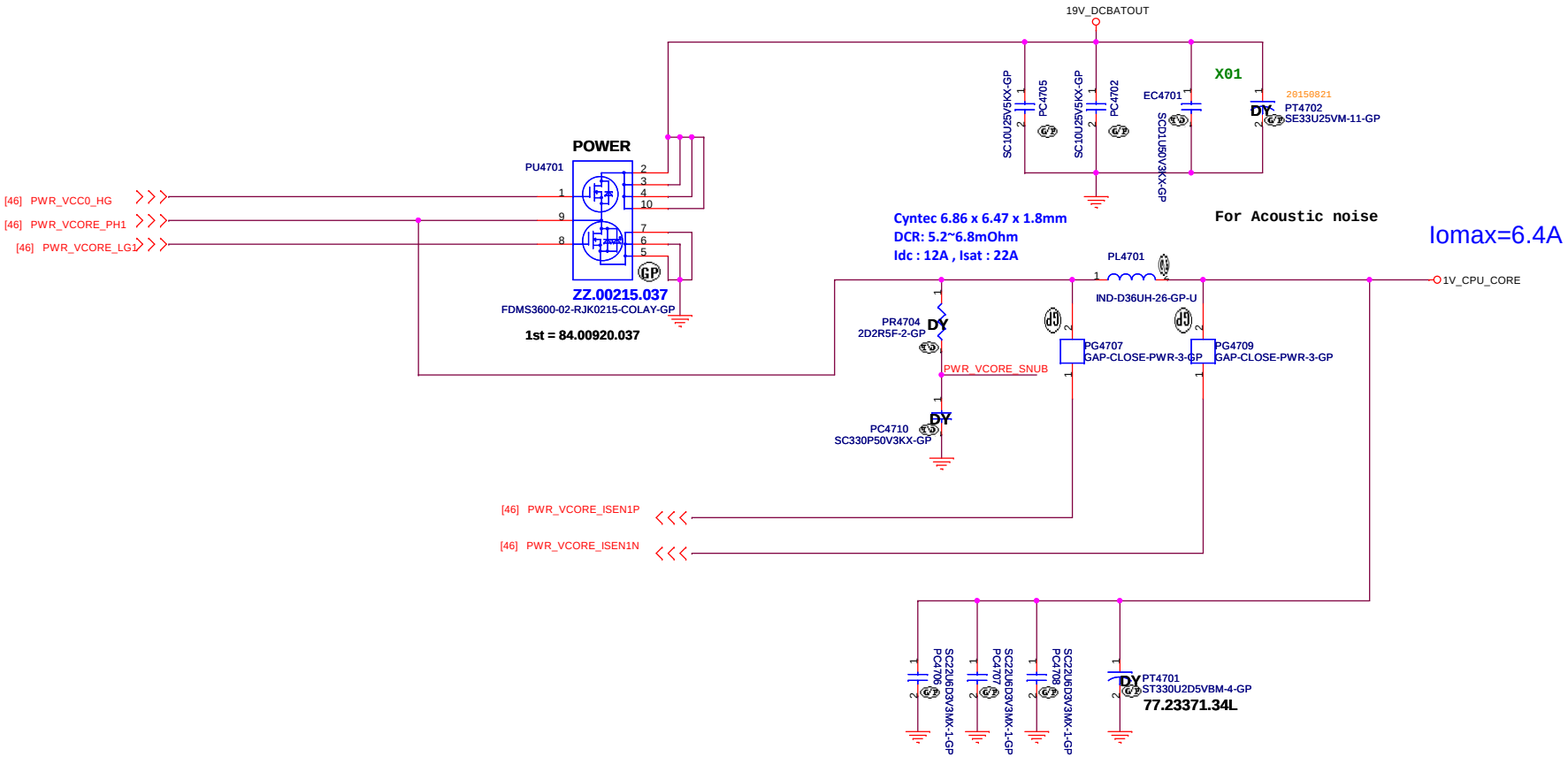
VBOOT/ADDR Resistor (Ohm)	SVID Address	Vboot (V)
0	0x0	1.0
14.0 k	0x1	1.0
22.1 k	0x2	1.0
30.1 k	0x3	1.0
39.2 k	0x4	1.0
48.7 k	0x5	1.0
57.6 k	0x6	1.0
68.1 k	0x7	1.0
78.7 k	0x8	1.1
88.7 k	0x0	1.1
100 k	0x1	1.1
113 k	0x2	1.1
124 k	0x3	1.1
137 k	0x4	1.1
150 k	0x5	1.1
165 k	0x6	1.1
178 k	0x7	1.1
196 k	0x8	1.1

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NCP81201MNTXG_CPUCORE(1/3)
Size: Custom | Document Number: Rocket BSW 11.6" | Rev: X00
Date: Thursday, October 08, 2015 | Sheet 45 of 109

SSID = CPU Regulator

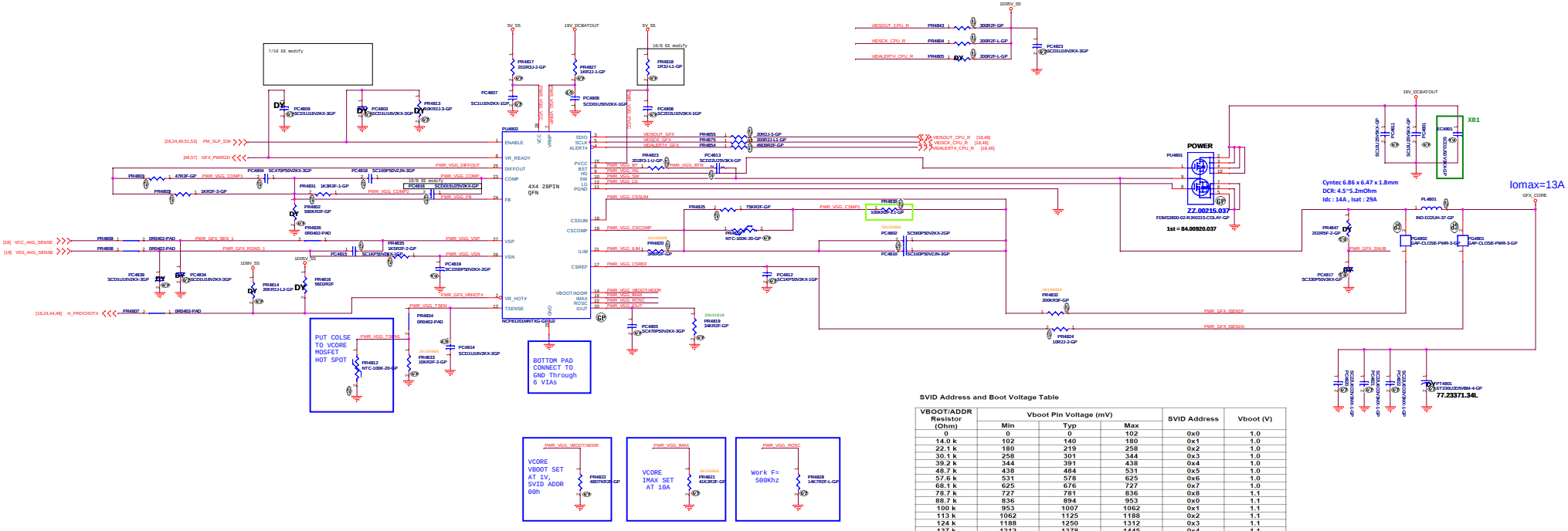


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	NCP81201MNTXG_CPUCORE(2/3)	
Size A3	Document Number: Rocket BSW 11.6"	Rev X00
Date: Tuesday, October 06, 2015	Sheet 47 of 109	

SSID = GFX Regulator



SVID Address and Boot Voltage Table

VBOOT/ADDR Resistor (Ohm)	Vboot Pin Voltage (mV)			SVID Address	Vboot (V)
	Min	Typ	Max		
0	0	0	102	0x0	1.0
14.0 k	102	140	180	0x1	1.0
22.1 k	180	219	258	0x2	1.0
30.1 k	258	301	344	0x3	1.0
39.2 k	344	391	438	0x4	1.0
48.7 k	438	484	531	0x5	1.0
57.6 k	531	578	625	0x6	1.0
68.1 k	625	676	727	0x7	1.0
78.7 k	727	781	836	0x8	1.1
88.7 k	836	894	953	0x0	1.1
100 k	953	1007	1062	0x1	1.1
113 k	1062	1125	1188	0x2	1.1
124 k	1188	1250	1312	0x3	1.1
137 k	1312	1378	1445	0x4	1.1
150 k	1445	1511	1578	0x5	1.1
165 k	1578	1648	1719	0x6	1.1
178 k	1719	1789	1859	0x7	1.1
196 k	1859	1950	-	0x8	1.1

<Core Design>

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Title: NCP81201MNTXG_GFXCORE(3/3)

Size: A3 | Document Number: Rocket BSW 11.6" | Rev: X00

Date: Wednesday, October 05, 2011 | Sheet 48 of 100

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<Core Design>

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Title

(Reserved)

Size	Document Number	Rev
A4	**Rocket BSW 11.6"**	**X00**

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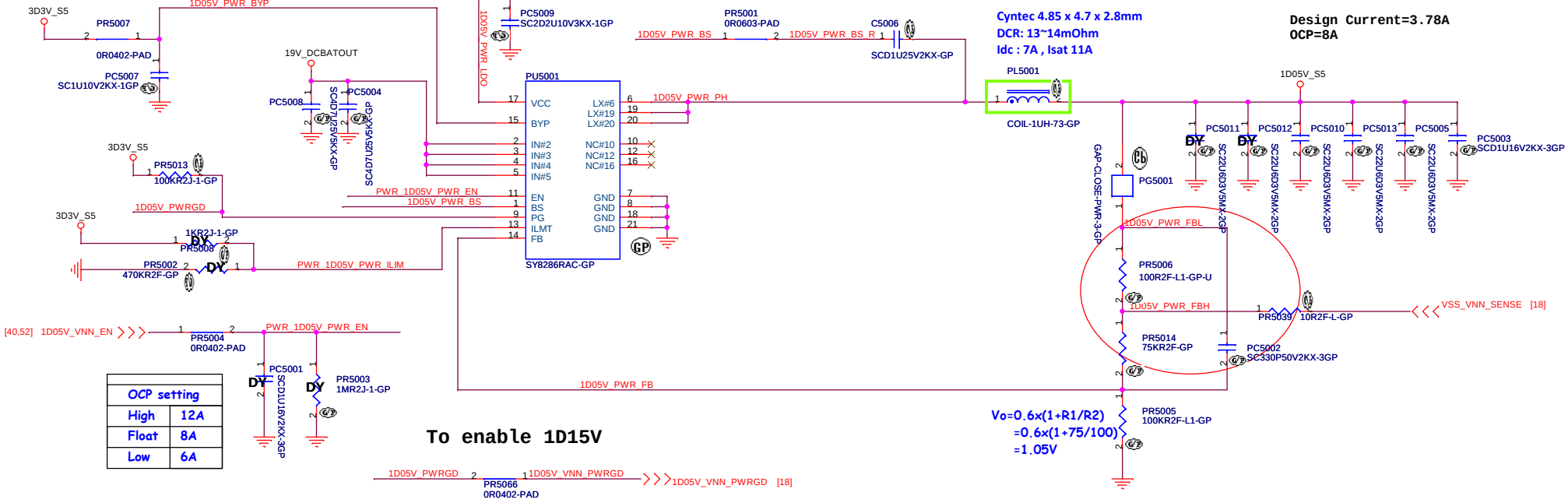
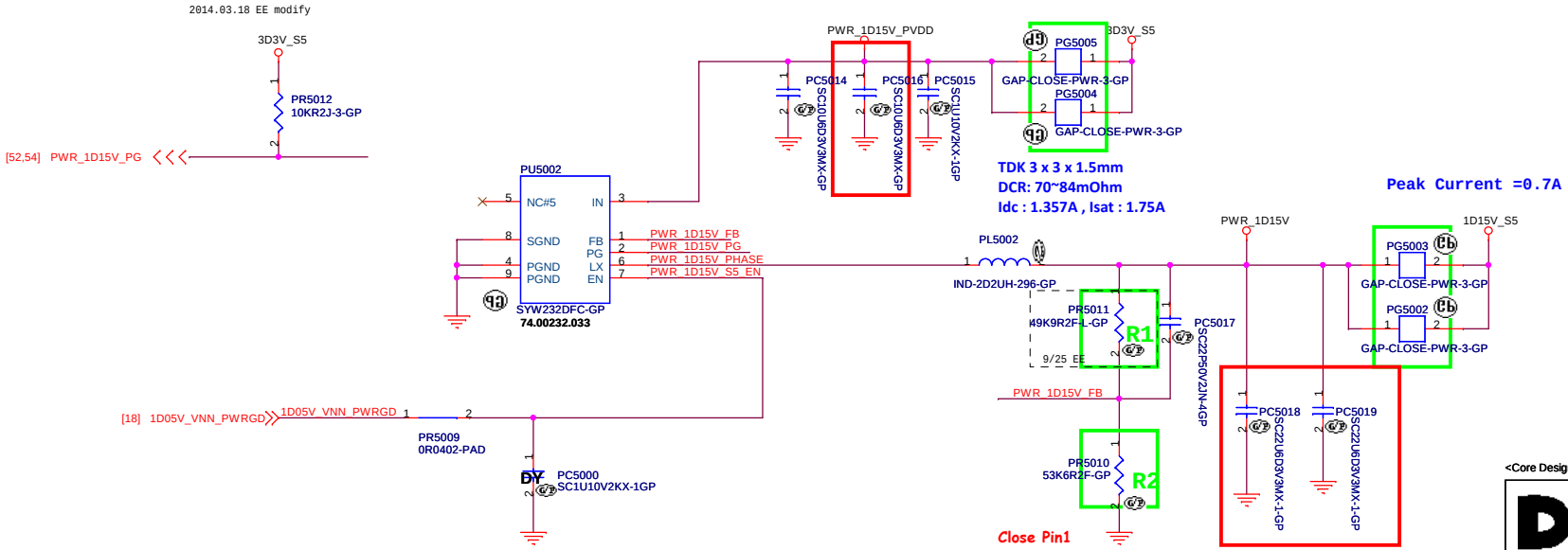
SSID = PWR.Plane.Regulator_1p05v

SY8286D for 1D05V



SSID = PWR.Plane.Regulator_1p8v

SYW232 for 1D15V_S5



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: DCDC_VNN_1D05V_1D15V

Size	Document Number	Rev
A3	Rocket BSW 11.6"	X00

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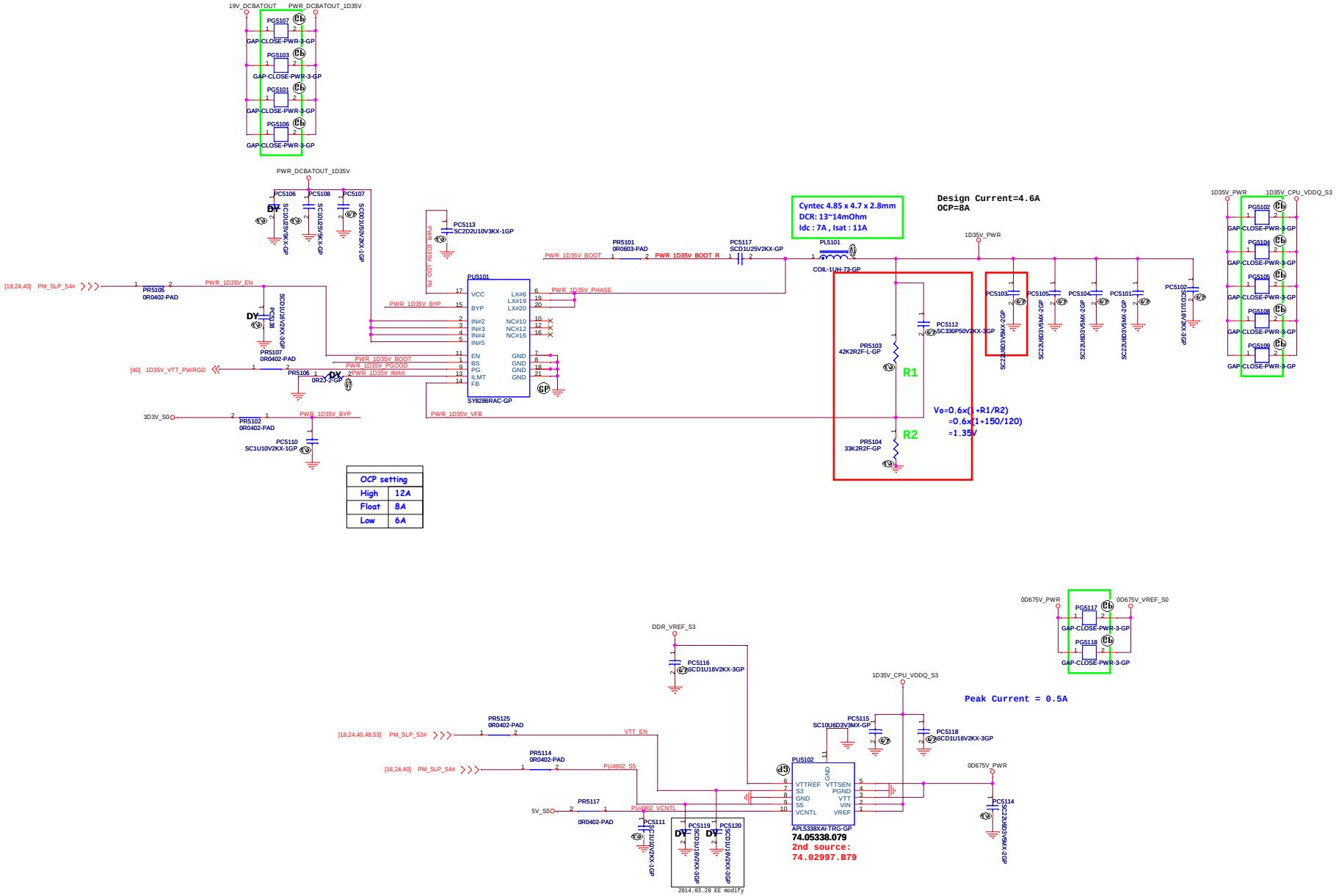
SY8206D for 1D35V



<Core Design>

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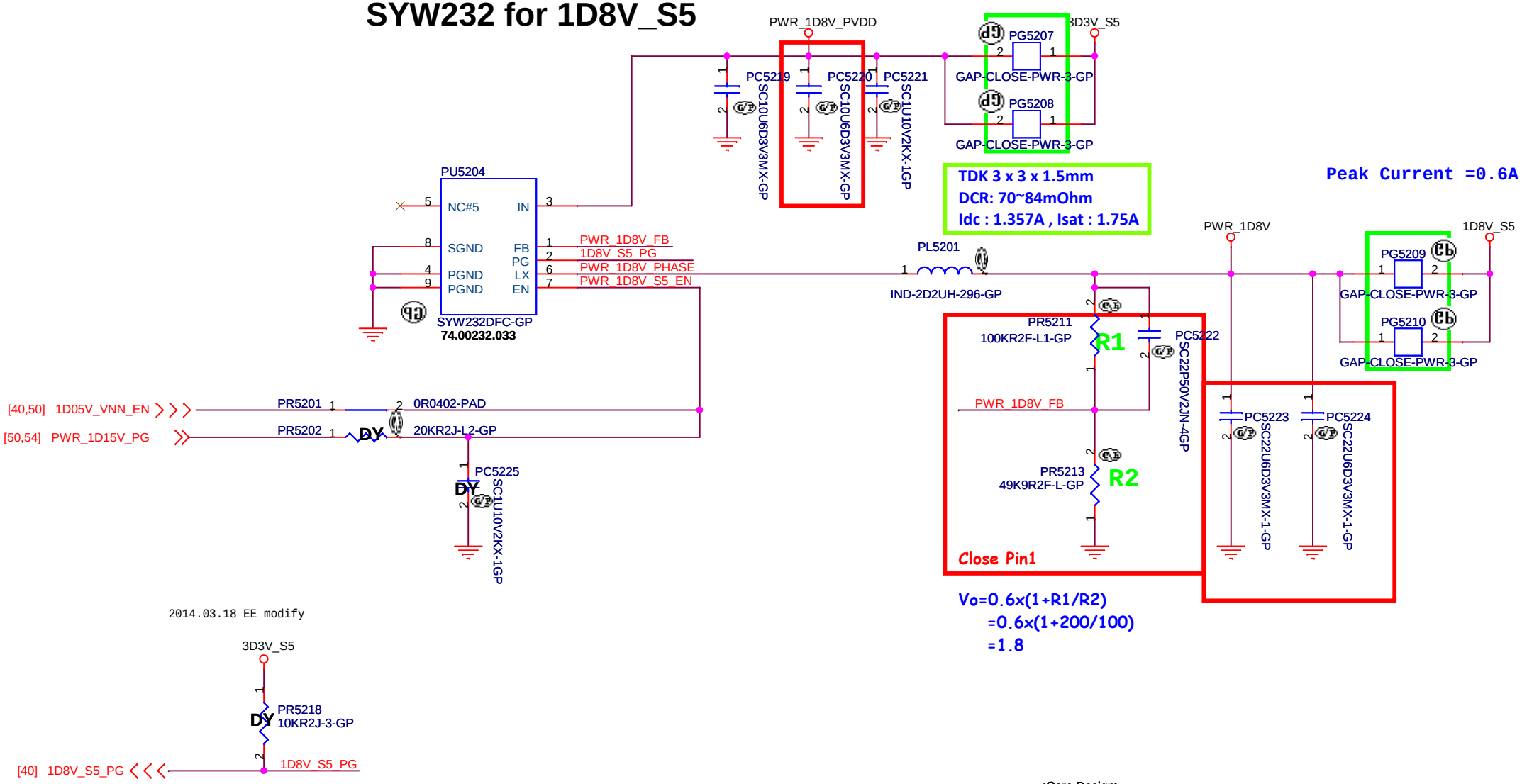
Title: DC to DC 1D35V(SY8206DQNC)

Size: A2 | Document Number: Rocket BSW 11.6" | Rev: X00

Date: Thursday, October 08, 2015 | Sheet 51 of 109

SSID = PWR.Plane.Regulator_1p8v

SYW232 for 1D8V_S5



<Core Design>

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Title	SYW232DFC_1D8V	
Size: A4	Document Number: Rocket BSW 11.6"	Rev: X00
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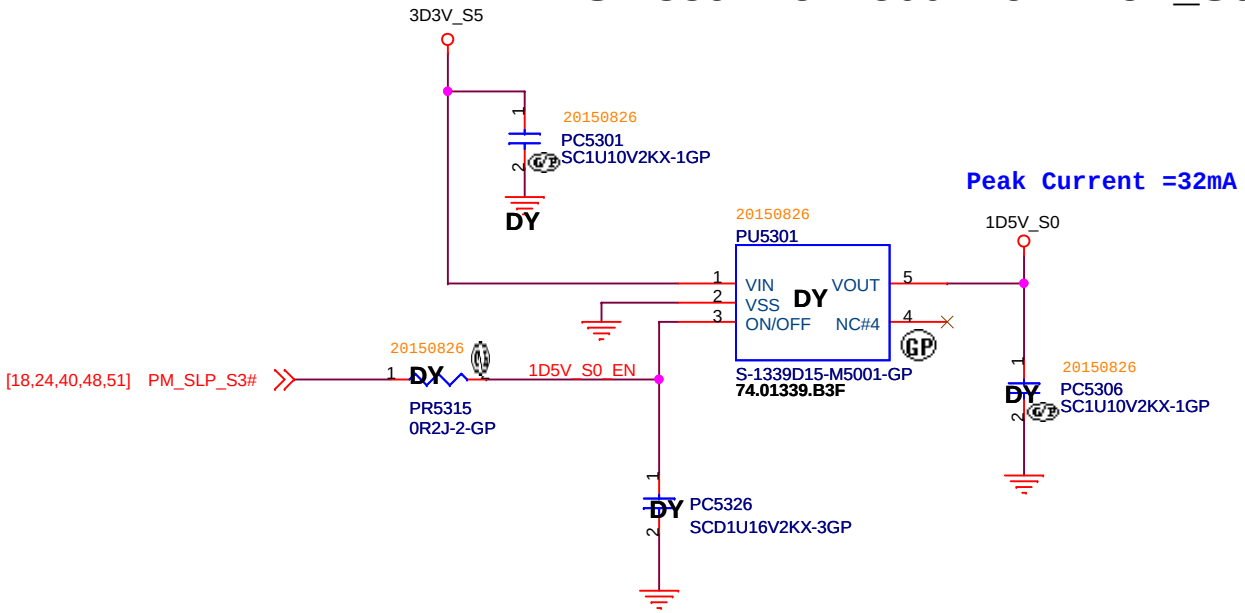
S-1339D15-M5001 for 1D5V_S0



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Title	***S1339D15_1D5V***	
Size: A4	Document Number: ***Rocket BSW 11.6"***	Rev: ***X00***
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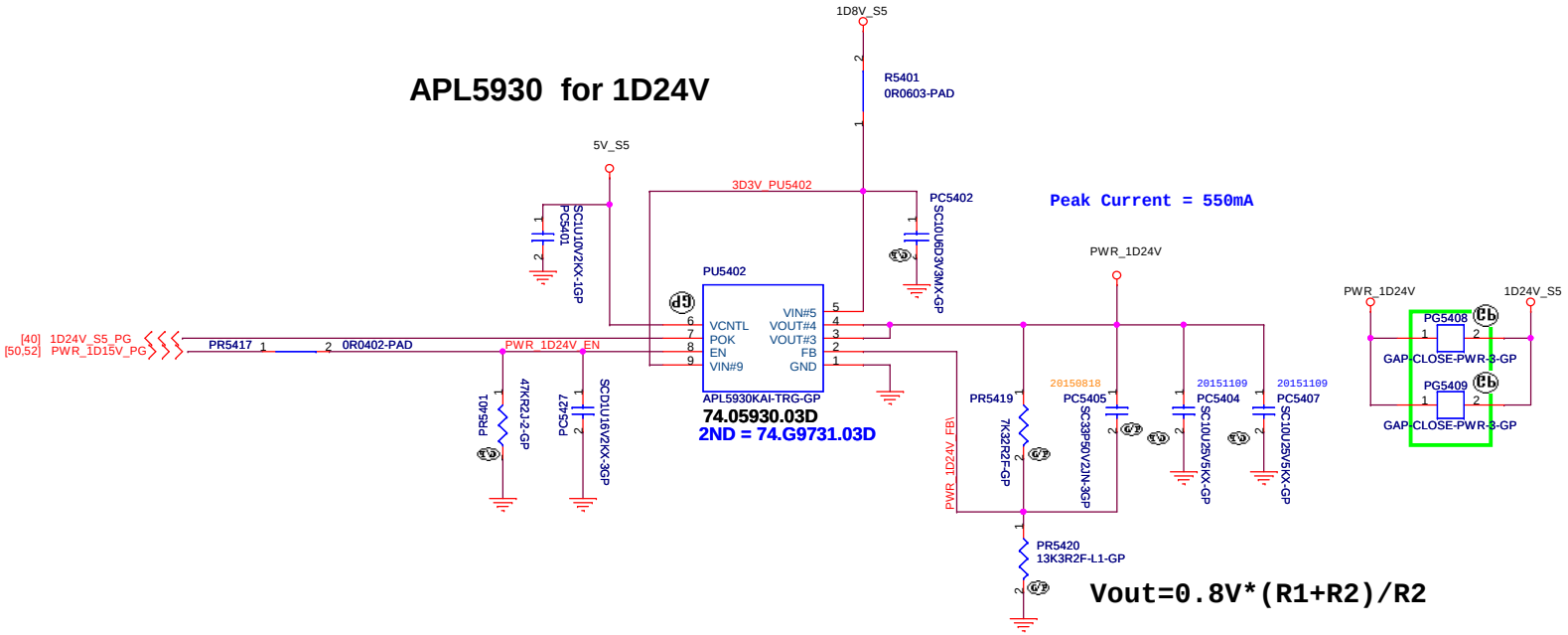
APL5930 for 1D24V



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Title	APL5930_1D24V	
Size: A3	Document Number: Rocket BSW 11.6"	Rev: A00
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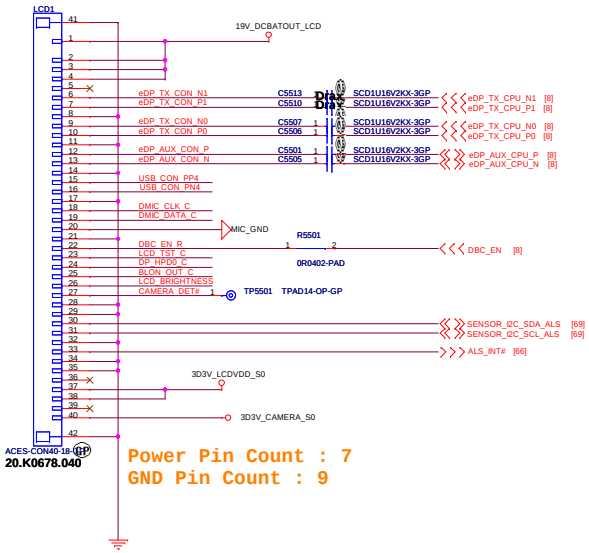
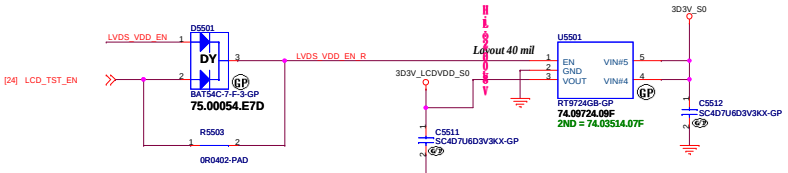
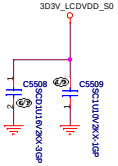
SSID = VIDEO

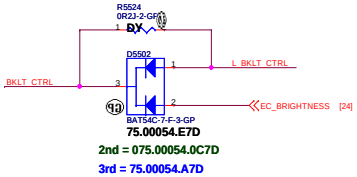
Panel Conn.

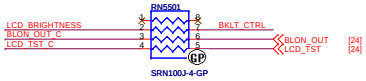


Power Pin Count : 7
GND Pin Count : 9

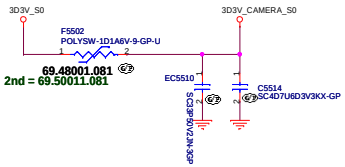




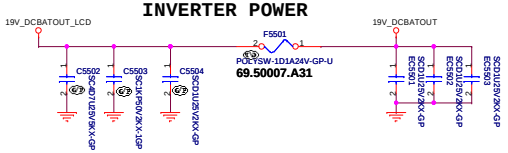




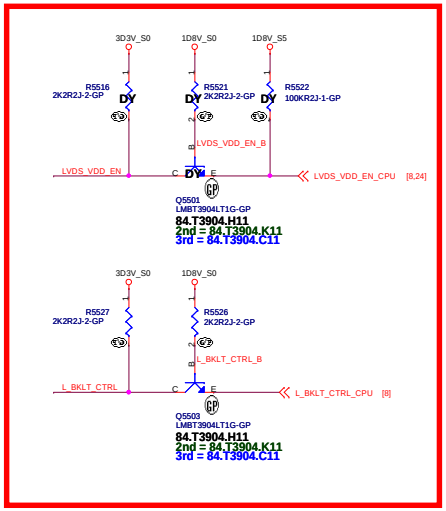
CAMERA POWER

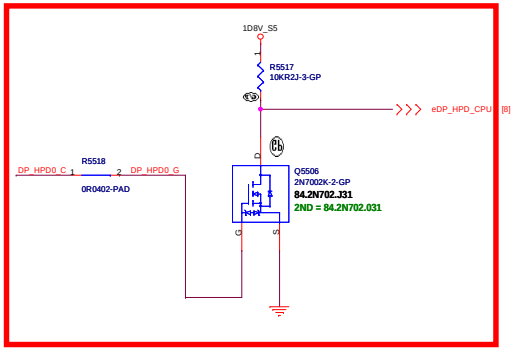


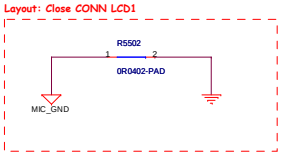
INVERTER POWER

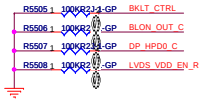


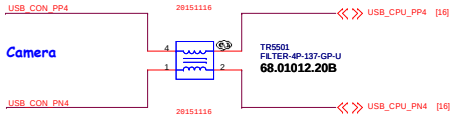
Level shift

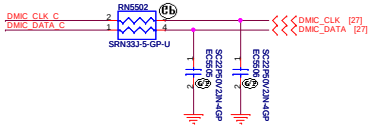












Title	HDMI Level Shifter/Connector	
Size: A2	Document Number: Rocket BSW 11.6"	Rev: X00
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Title

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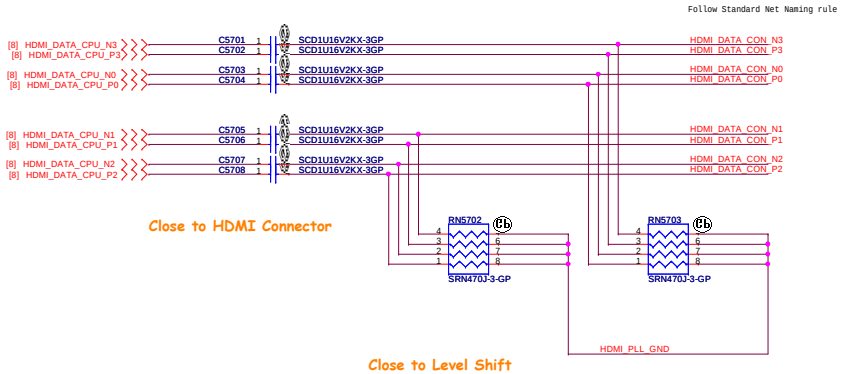
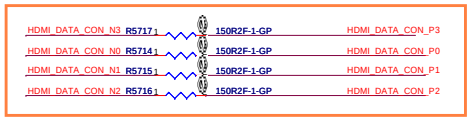
Size	Document Number	Rev
A4	*Rocket BSW 11.6"*	*X00*

Date: Monday, September 21, 2015 Sheet 56 of 109

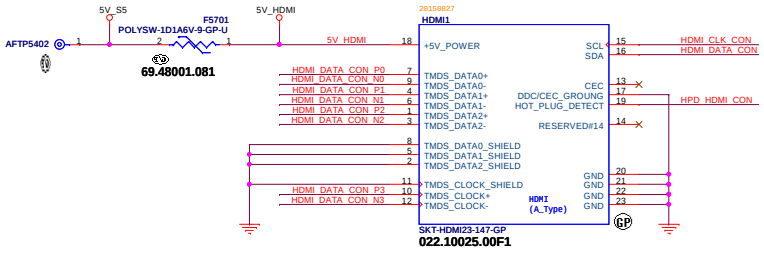
SSID = VIDEO

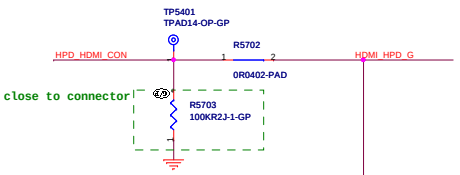
HDMI Level Shifter & CONNECTOR

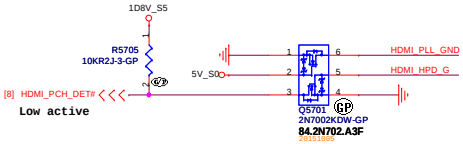


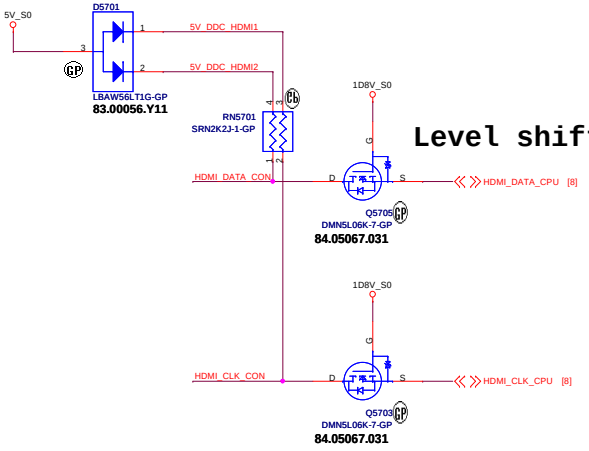


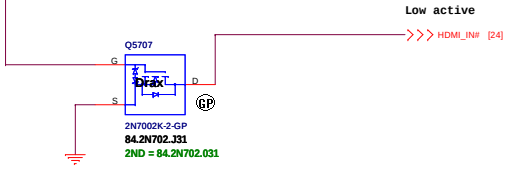
HDMI CONN

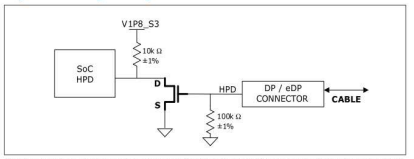












NOTE: It is highly recommended a passgate N-MOSFET device is selected that has Gate Threshold Voltage <=1.5V.
NOTE: The HPD PU resistor tolerance can be relaxed to 5%.

4.2.9 Hot Plug Detect Signal (HPD)

The ground reference for the Hot Plug Detect signal is the DDC/CEC Ground pin.

Table 4-38 Required Output Characteristics of Hot Plug Detect Signal

Item	Value
High voltage level (Sink)	Minimum 2.4 Volts, Maximum 5.3 Volts
Low voltage level (Sink)	Minimum 0 Volts, Maximum 0.4 Volts
Output resistance	1000 ohms ±20%

Table 4-39 Required Detection Levels for Hot Plug Detect Signal

Item	Value
High voltage level (Source)	Minimum 2.0 Volts, Maximum 5.3 Volts
Low voltage level (Source)	Minimum 0 Volts, Maximum 0.8 Volts

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Title: HDMI Level Shifter/Connector

Size	Document Number	Rev
Custom	Rocket BSW 11.6"	X00

Date: Monday, October 12, 2015 Sheet 57 of 109

SSID = Display Port

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Title: *(Reserved) Display Port*

Size	Document Number	Rev
	Rocket BSW 11.6"	*X00*

Date: Monday, September 21, 2015 Sheet 58 of 109

SSID = DVI

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Title: *(Reserved) DVI*

Size	Document Number	Rev
	Rocket BSW 11.6"	*X00*

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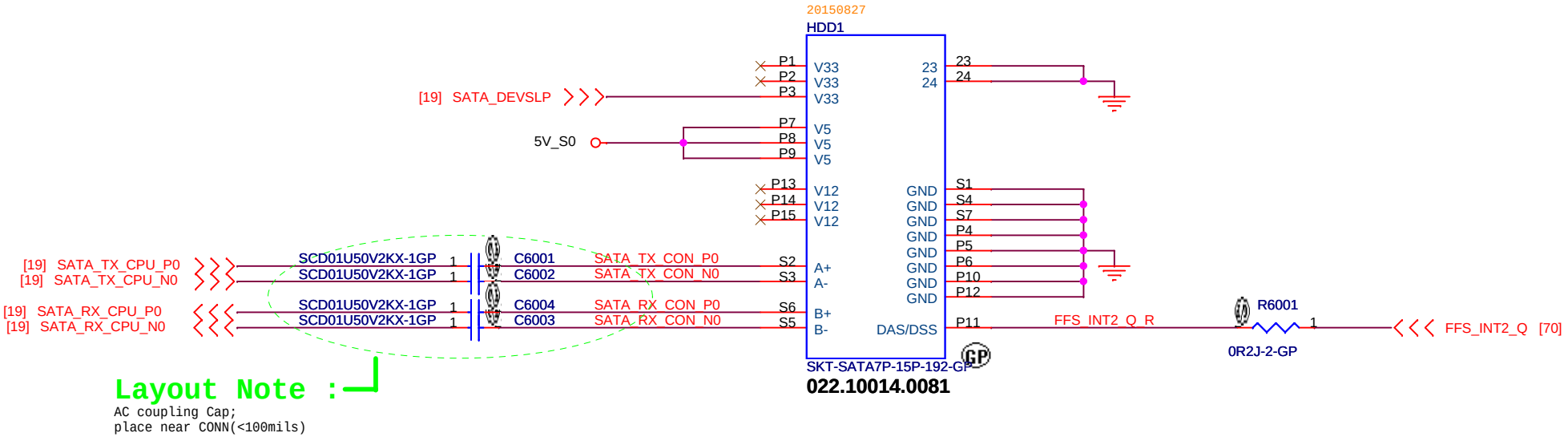
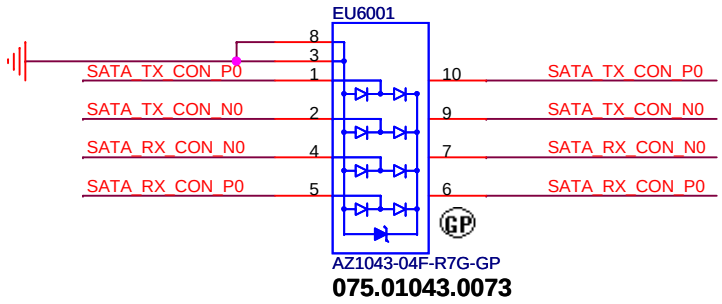
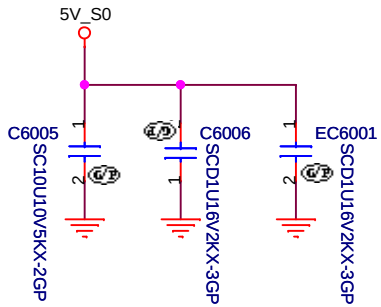
SSID = SATA

SATA HDD Connector



Layout Note :
AC coupling Cap;
place near CONN(<100mils)





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Title: ***HDD***

Size	Document Number	Rev
	Rocket BSW 11.6"	***X00***

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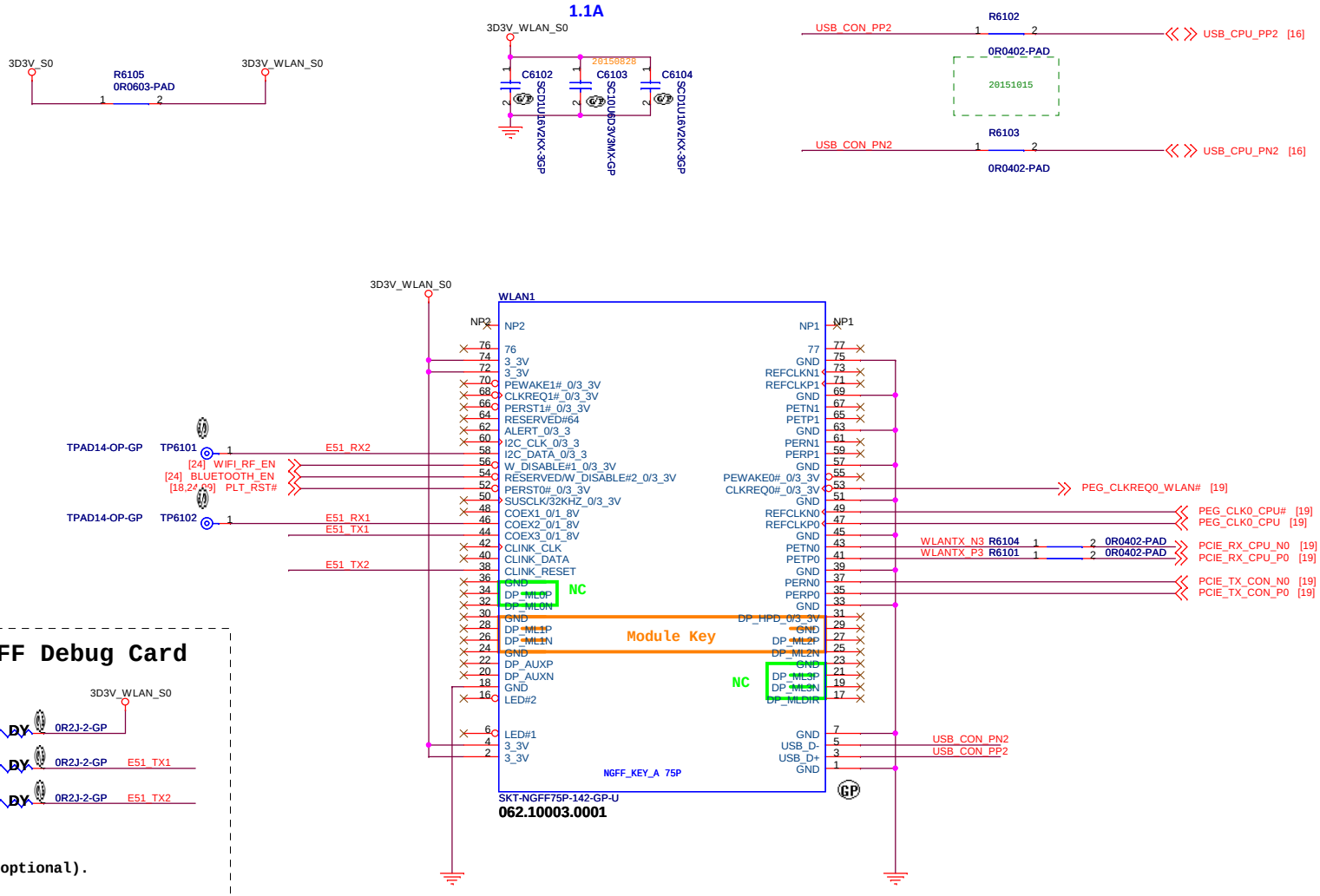
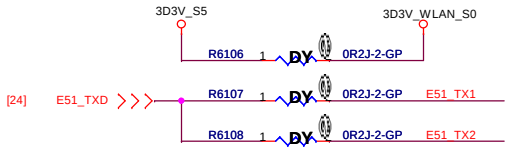
SSID = WLAN

Mini Card Connector(802.11a/b/g)



Reserved for NGFF Debug Card



EE Note:
For NFGG Debug Card:
Stuff R6106,R6107,R6108(optional).
DY R6105

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Title: WLAN		
Size	Document Number: Rocket BSW 11.6"	Rev: X00
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SSID = WWAN

Blanking

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Title
(Reserved) WWAN

Size	Document Number	Rev
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SSID = SSD-NGFF

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Title: *eMMC*

Size: A3 | Document Number: *Rocket BSW 11.6"* | Rev: *X00*

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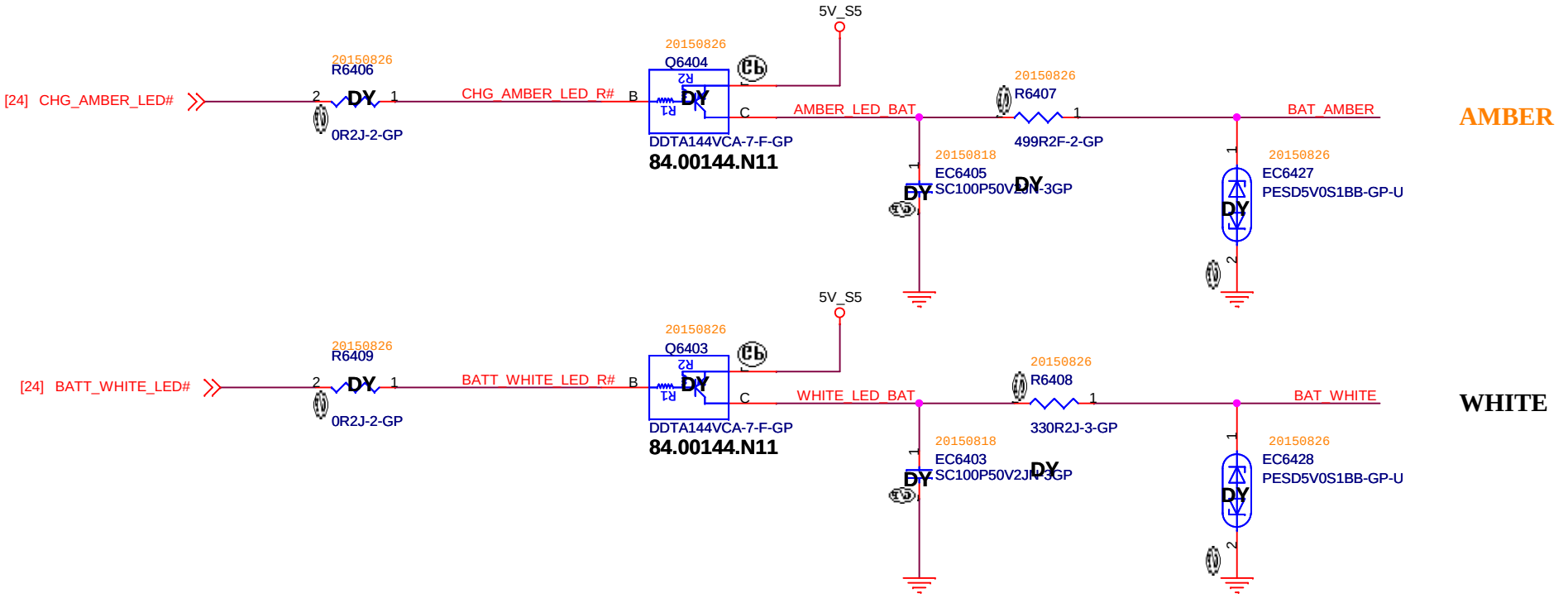
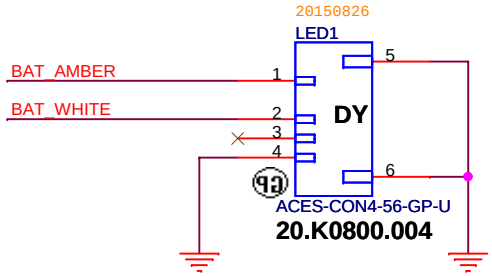
SSID = LED / PWRBTN

Battery LED1 (AMBER_LED)
Low actived from KBC GPIO



Battery LED2 (WHITE_LED)
Low actived from KBC GPIO



<Core Design>

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Title: LED / PWRBTN		
Size: A4	Document Number: Rocket BSW 11.6"	Rev: X00
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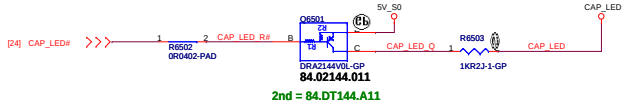
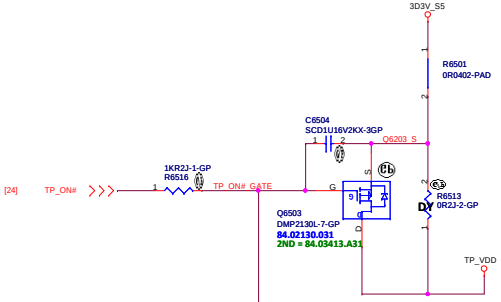
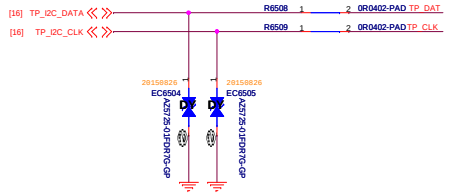
SSID = KB / TOUCH PAD

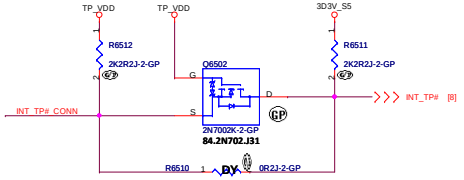
CAP LED Control
LOW actived from KBC GPIO

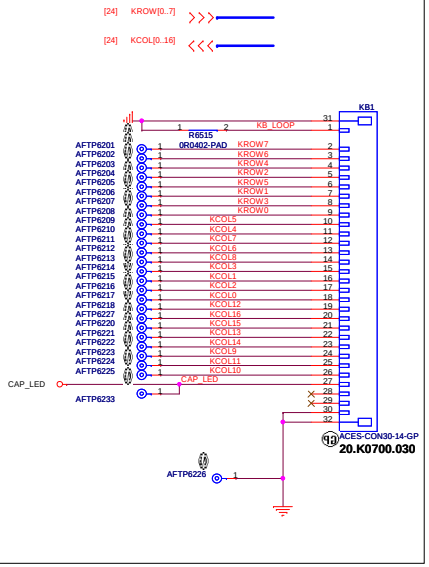


2nd = 84.DT144.A11

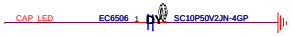


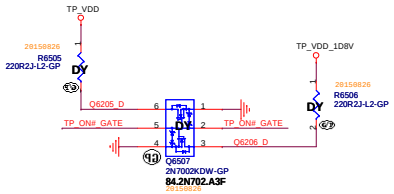


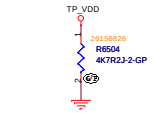




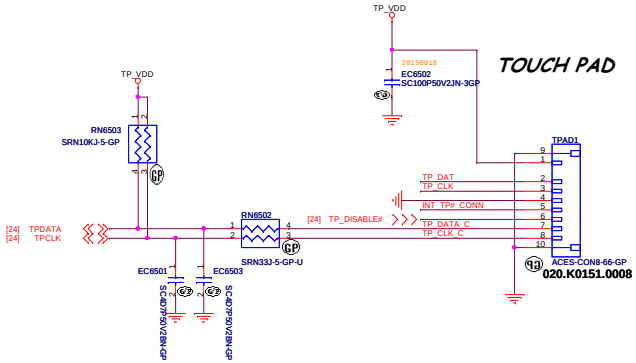
PIN#	SIGNAL
1	Diag_Loop-GPIO_1(TPC)
2	KSI [7] = KBD S8
3	KSI [6] = KBD S7
4	KSI [4] = KBD S5
5	KSI [2] = KBD S3
6	KSI [5] = KBD S6
7	KSI [1] = KBD S2
8	KSI [3] = KBD S4
9	KSI [0] = KBD S1
10	KSO [5] = KBD D6
11	KSO [4] = KBD D5
12	KSO [7] = KBD D8
13	KSO [6] = KBD D7
14	KSO [8] = KBD D9
15	KSO [3] = KBD D4
16	KSO [1] = KBD D2
17	KSO [2] = KBD D3
18	KSO [0] = KBD D1
19	KSO [12] = KBD D13
20	KSO [16] = KBD D17
21	KSO [15] = KBD D16
22	KSO [13] = KBD D14
23	KSO [14] = KBD D15
24	KSO [9] = KBD D10
25	KSO [11] = KBD D12
26	KSO [10] = KBD D11
27	CapsLock LED
28	N/C
29	N/C
30	GND







TOUCH PAD



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Title: Debug connector

Size	Document Number	Rev
	Rocket BSW 11.6"	X00

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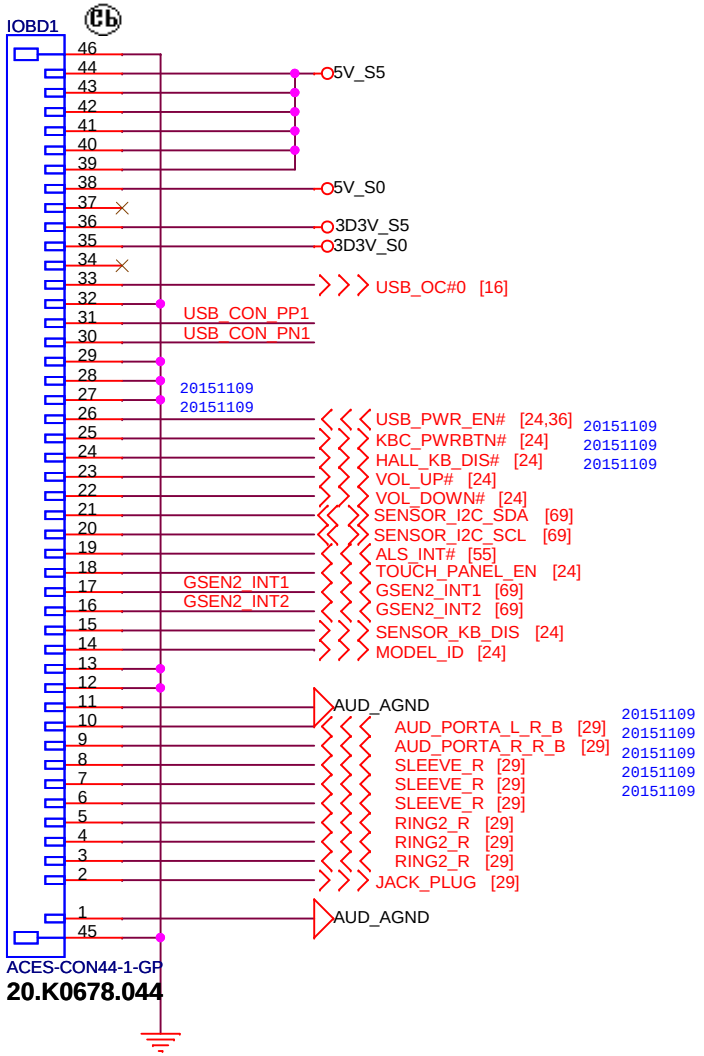

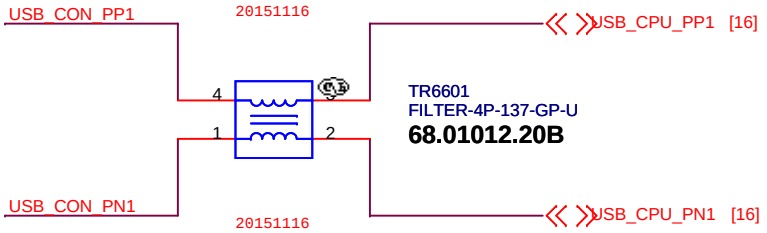

Power Pin Count : 9
GND Pin Count : 8

<Core Design>

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Title: *IO Board CONN*

Size	Document Number	Rev
A4	Rocket BSW 11.6"	A00

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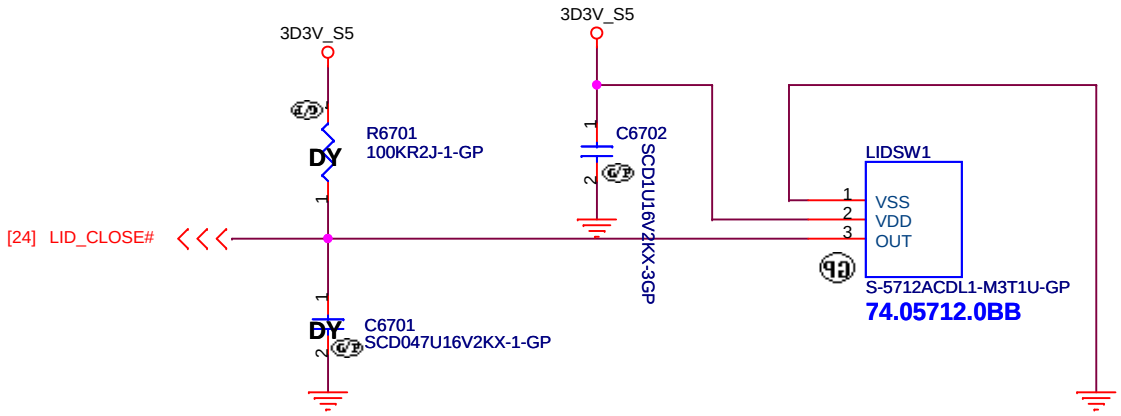

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

Size	Document Number	Rev
A4	***Rocket BSW 11.6"***	***X00***

Date: Tuesday, October 06, 2015 Sheet 67 of 109

SSID = Debug CONN

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

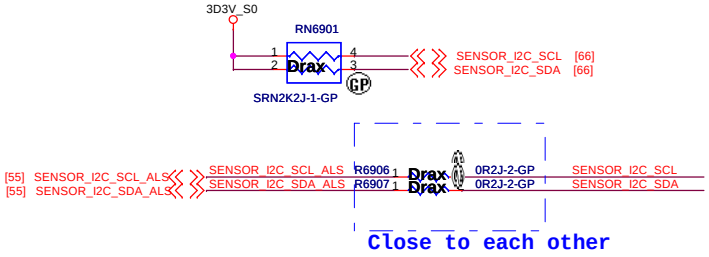
Title

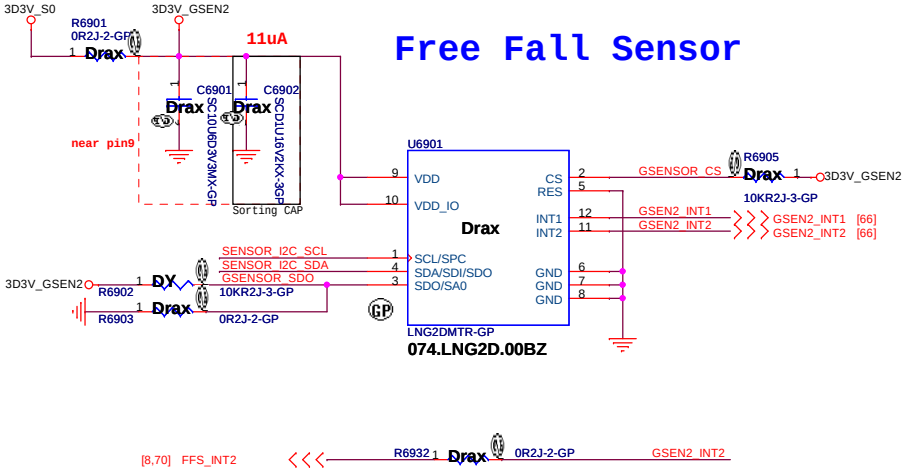
(Reserved) Debug CONN

Size	Document Number	Rev
A4	*Rocket BSW 11.6"*	*X00*

Date: Monday, September 21, 2015 Sheet 68 of 109

SSID = Sensor





<Core Design>

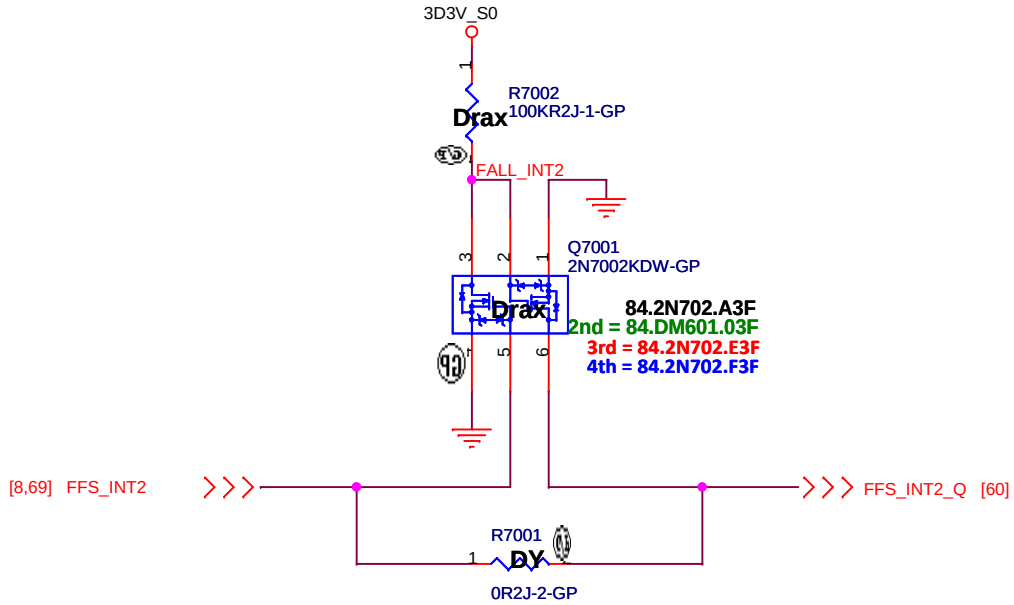
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Sensor

Size	Document Number	Rev
A3	Rocket BSW 11.6"	X00

Date: Tuesday, October 06, 2015 Sheet 69 of 109

SSID = Free Fall Sensor



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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Free Fall Sensor***

Size	Document Number	Rev
A4	***Rocket BSW 11.6"***	*X00*

Date: Tuesday, October 06, 2015 Sheet 70 of 109

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)Thunderbolt (1/5)*

Size	Document Number	Rev
A4	*Rocket BSW 11.6"*	*X00*

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)Thunderbolt (2/5)*

Size	Document Number	Rev
A4	*Rocket BSW 11.6"*	*X00*

Date: Monday, September 21, 2015 Sheet 72 of 109

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)Thunderbolt (3/5)*

Size	Document Number	Rev
A4	*Rocket BSW 11.6"*	*X00*

Date: Monday, September 21, 2015 Sheet 73 of 109

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)Thunderbolt (4/5)*

Size	Document Number	Rev
A4	*Rocket BSW 11.6"*	*X00*

Date: Monday, September 21, 2015 Sheet 74 of 109

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)Thunderbolt (5/5)*

Size	Document Number	Rev
A4	*Rocket BSW 11.6"*	*X00*

Date: Monday, September 21, 2015 Sheet 75 of 109

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)GPU (1/5) PEG

Size	Document Number	Rev
A4	***Rocket BSW 11.6"***	*X00*

Date: Monday, September 21, 2015 Sheet 76 of 109

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)GPU (2/5) DIGITAL*

Size	Document Number	Rev
A4	*Rocket BSW 11.6"*	*X00*

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)GPU (3/5) VRAM*

Size	Document Number	Rev
A4	*Rocket BSW 11.6"*	*X00*

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)GPU (4/5) GPIO*

Size	Document Number	Rev
A4	*Rocket BSW 11.6"*	*X00*

Date: Monday, September 21, 2015 Sheet 79 of 109

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)GPU (5/5) PWR/GND*

Size	Document Number	Rev
A4	*Rocket BSW 11.6"*	*X00*

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)VRAM1,2 (1/4)*

Size	Document Number	Rev
A4	*Rocket BSW 11.6"*	*X00*

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)VRAM3,4 (2/4)*

Size	Document Number	Rev
A4	*Rocket BSW 11.6"*	*X00*

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)VRAM5,6 (3/4)*

Size	Document Number	Rev
A4	*Rocket BSW 11.6"*	*X00*

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)VRAM7,8 (4/4)*

Size	Document Number	Rev
A4	*Rocket BSW 11.6"*	*X00*

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)VGA_CORE*

Size	Document Number	Rev
A4	*Rocket BSW 11.6"*	*X00*

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)DISCRETE VGAPOWER*

Size	Document Number	Rev
	Rocket BSW 11.6"	*X00*

Date: Monday, September 21, 2015 Sheet 86 of 109

Blanking

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A4	**Rocket BSW 11.6"**	**X00**

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)

Size	Document Number	Rev
A4	***Rocket BSW 11.6"***	*X00*

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20151124 20150901 20151008 20151008 20151008 20151008

34.43E24.001
SPRING-13-GP-U
SPR1

34.4YW18.001
SPRING-171-GP
SPR2

34.34S02.002
SPRING-98-GP
SPR4

34.34S02.002
SPRING-98-GP
SPR5

34.34S02.002
SPRING-98-GP
SPR6

34.34S02.002
SPRING-98-GP
SPR7

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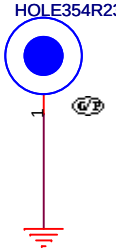

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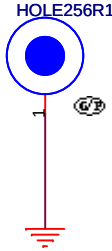
HOLE256R142-OG-1-GP



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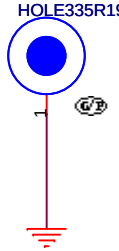

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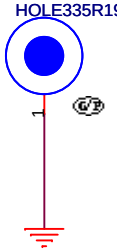
HOLE335R197-GP



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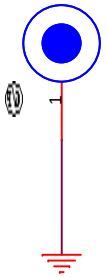
STF237R117H67-3-GP



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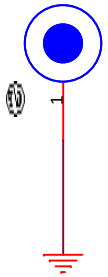
HS2
STF237R117H67-3-GP



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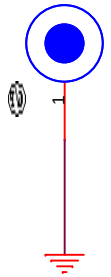
HS3
STF237R117H67-3-GP



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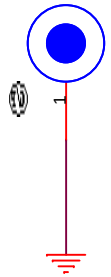
STF237R117H67-3-GP



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***UNUSED PARTS/EMI Capacitors***

Size	Document Number	Rev
A4	***Rocket BSW 11.6"***	***X00***

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)NFC Connector*

Size	Document Number	Rev
A4	*Rocket BSW 11.6"*	*X00*

Date: Monday, September 21, 2015 Sheet 90 of 109

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved) TPM*

Size	Document Number	Rev
A4	*Rocket BSW 11.6"*	*X00*

Date: Monday, September 21, 2015 Sheet 91 of 109

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)Finger Print*

Size	Document Number	Rev
A4	*Rocket BSW 11.6"*	*X00*

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)Express Card

Size	Document Number	Rev
A3	***Rocket BSW 11.6"***	*X00*

Date: Monday, September 21, 2015 Sheet 93 of 109

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<Core Design>

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***(Reserved)Smart Card Socket***		
Size: A4	Document Number: ***Rocket BSW 11.6"***	Rev: ***X00***
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*(Reserved)SW GFX eDP*	
Size: A4	Document Number: *Rocket BSW 11.6"*	Rev: *X00*
Date: Monday, September 21, 2015	Sheet 95 of 109	

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)Bottom Docking*

Size	Document Number	Rev
A4	*Rocket BSW 11.6"*	*X00*

Date: Monday, September 21, 2015 Sheet 96 of 109

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)LAN

Size	Document Number	Rev
A4	***Rocket BSW 11.6"***	***X00***

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)LAN SWITCH*

Size	Document Number	Rev
	Rocket BSW 11.6"	*X00*

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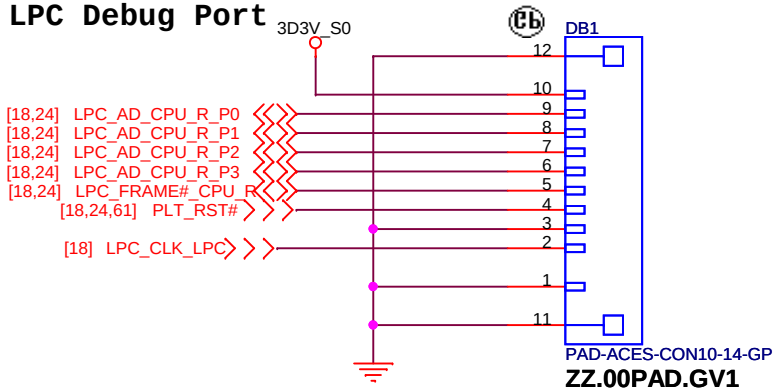
SSID = DEBUG PORT



20.F1180.010: Dummy Pad with solder mask is ZZ.00PAD.GV1

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU_XDP*		
Size: A4	Document Number: *Rocket BSW 11.6"*	Rev: *X00*
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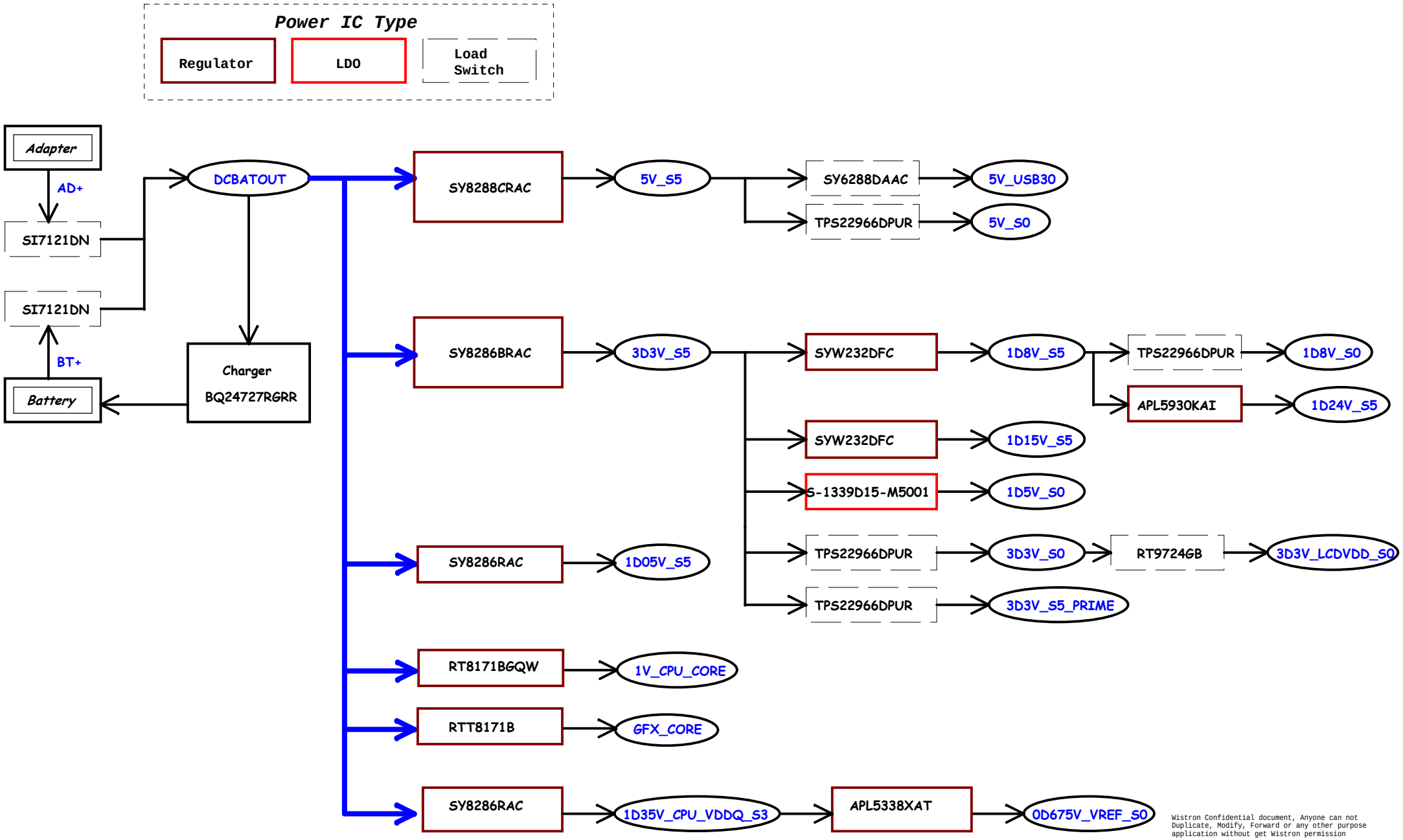

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

Size	Document Number	Rev
A3	Rocket BSW 11.6"	X00

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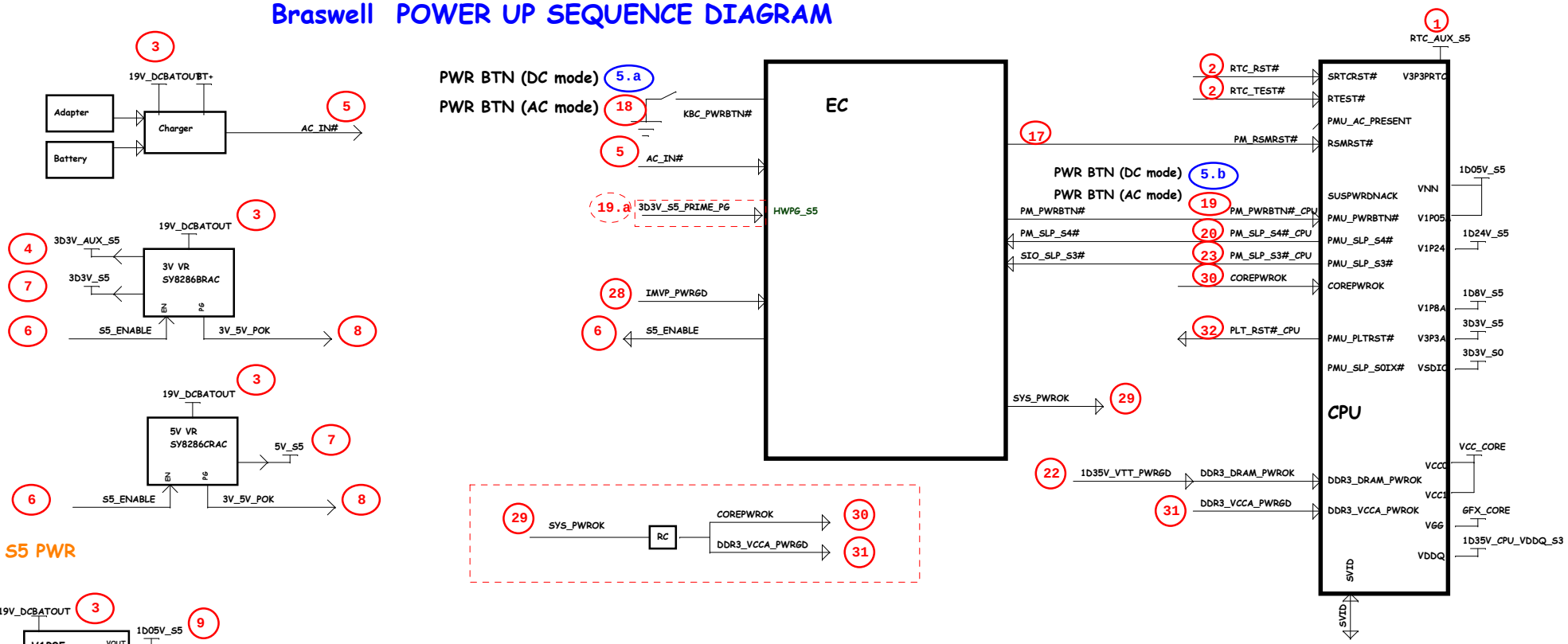
Braswell POWER UP SEQUENCE DIAGRAM



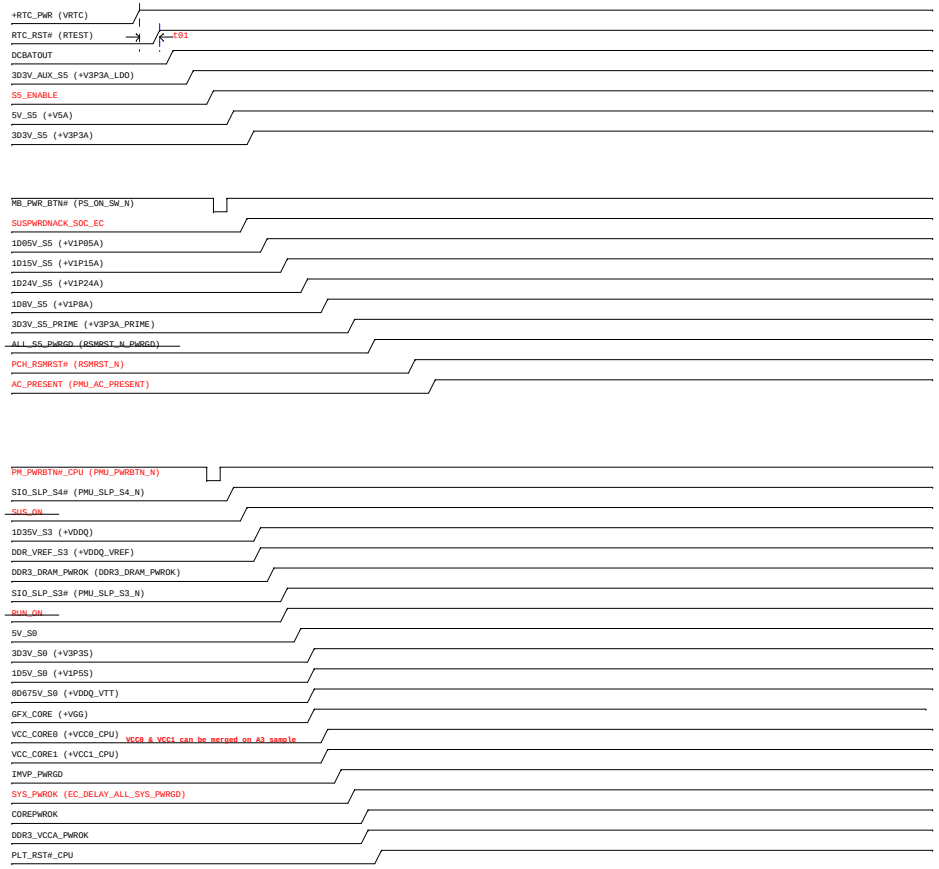
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram
Size: Document Number: Rocket BSW 11.6" Rev: X00
Date: Tuesday, October 06, 2015 Sheet 101 of 109

Intel-Power Up Sequence

(AC mode)

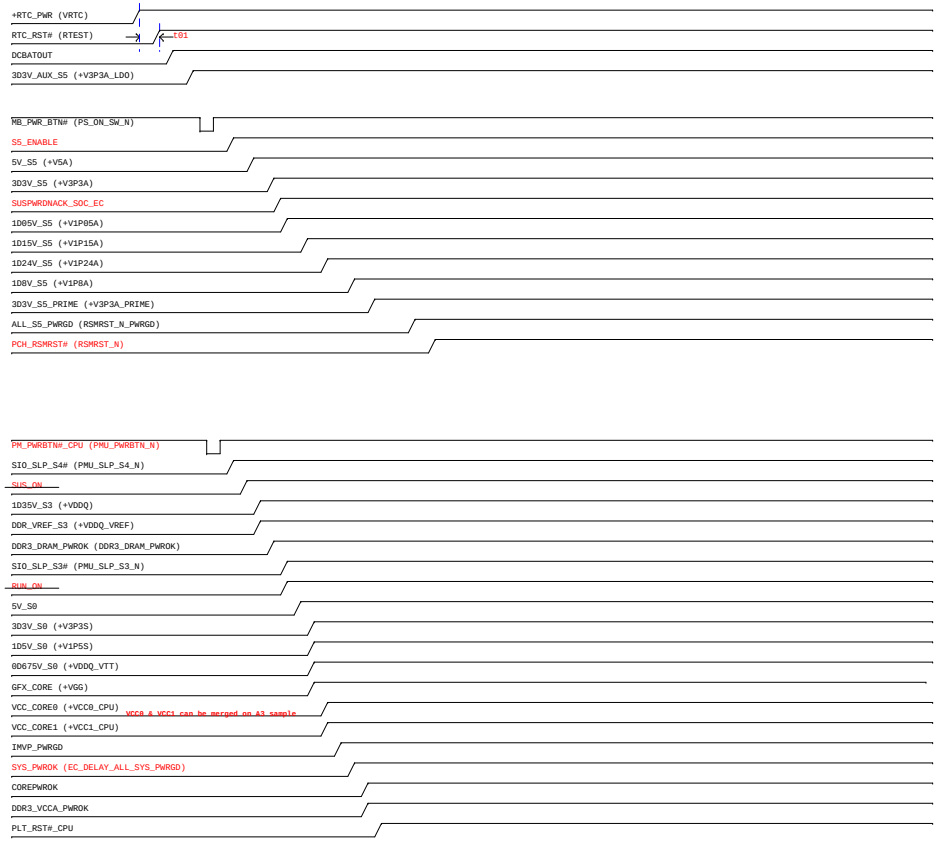
Red word : KBC GPIO



Intel-Power Up Sequence

(DC mode)

Red word : KBC GPIO



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Up Sequence

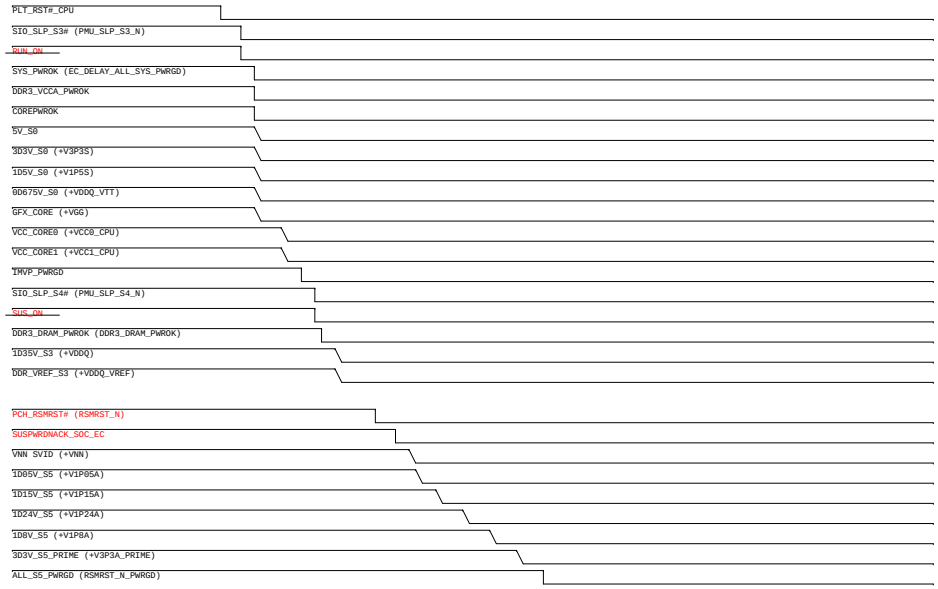
Size: | Document Number: Rocket BSW 11.6" | Rev: X00

Date: Monday, September 21, 2015 | Sheet 102 of 109

Intel-Power Down Sequence

(AC mode)

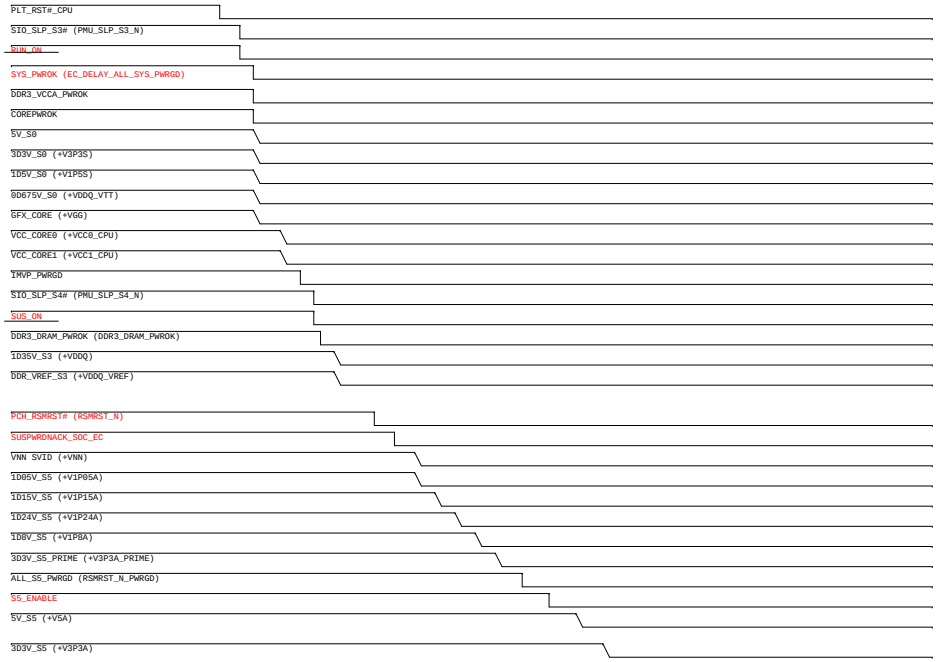
Red word : KBC GPIO



Intel-Power Down Sequence

(DC mode)

Red word : KBC GPIO



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Down Sequence

Size	Document Number	Rev
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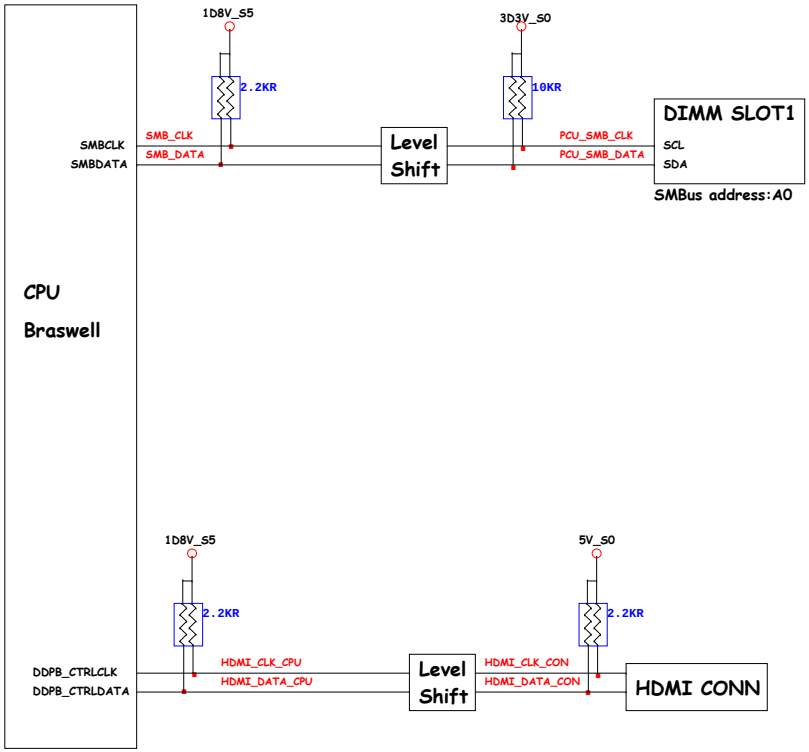
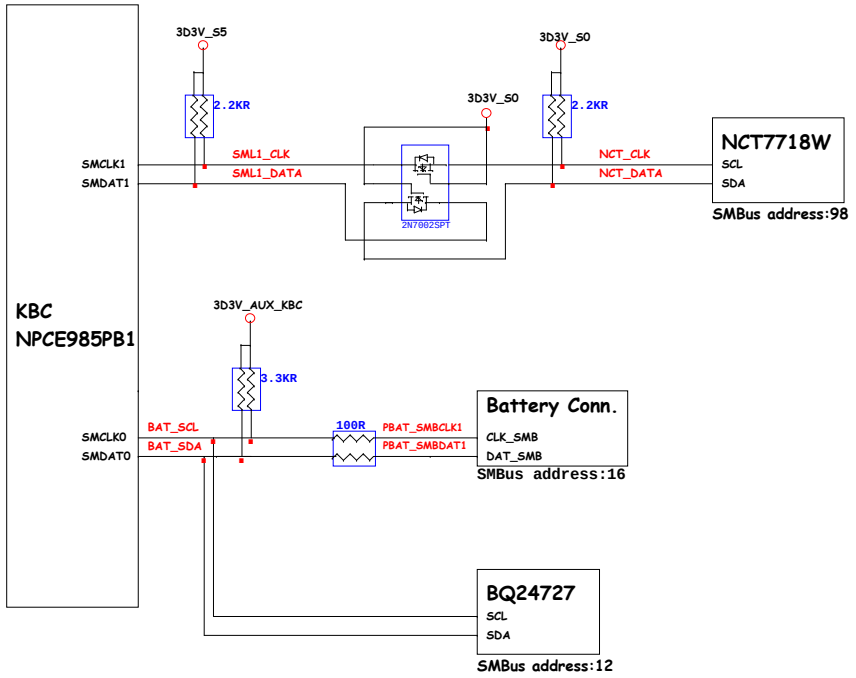
PCH SMBus Block Diagram



KBC SMBus Block Diagram



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS Block Diagram

Size	Document Number	Rev
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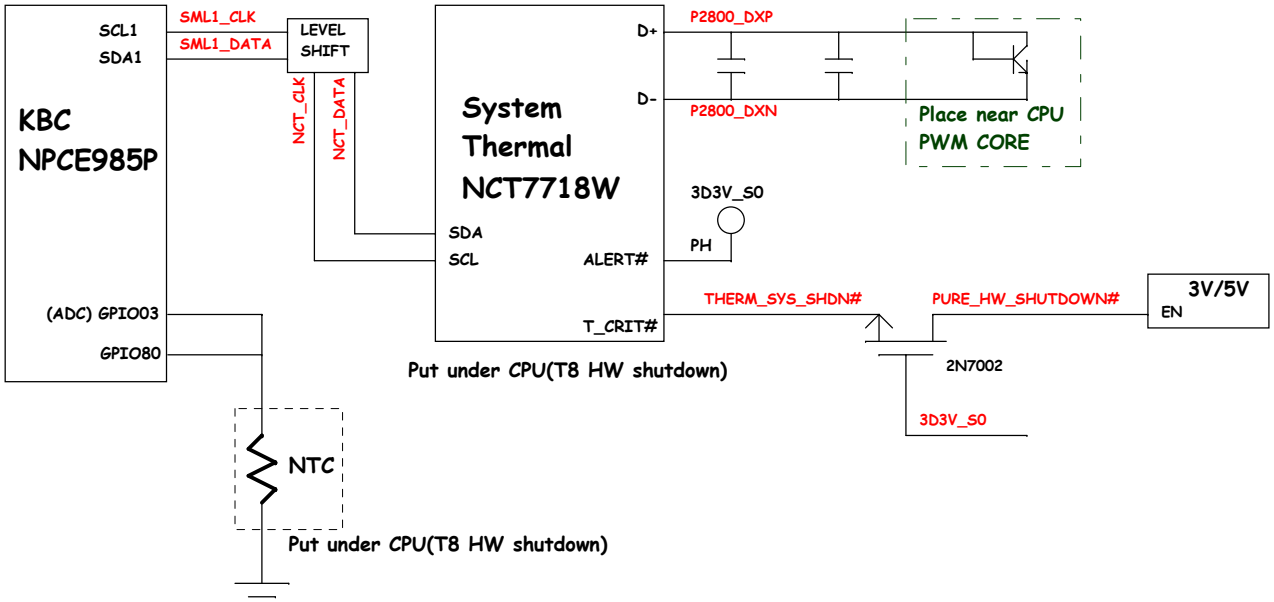
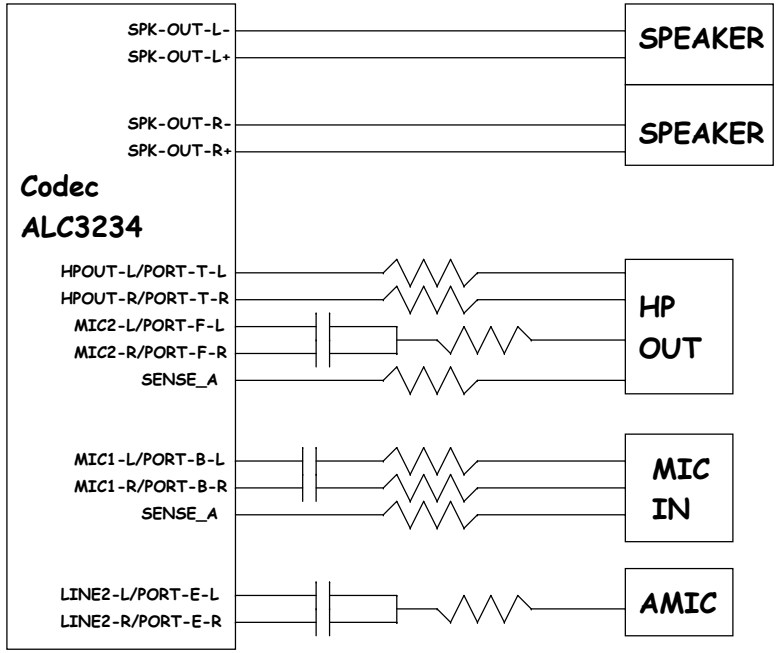
Thermal Block Diagram



Audio Block Diagram



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: Thermal/Audio Block Diagram

Size | Document Number: Rocket BSW 11.6" | Rev: X00

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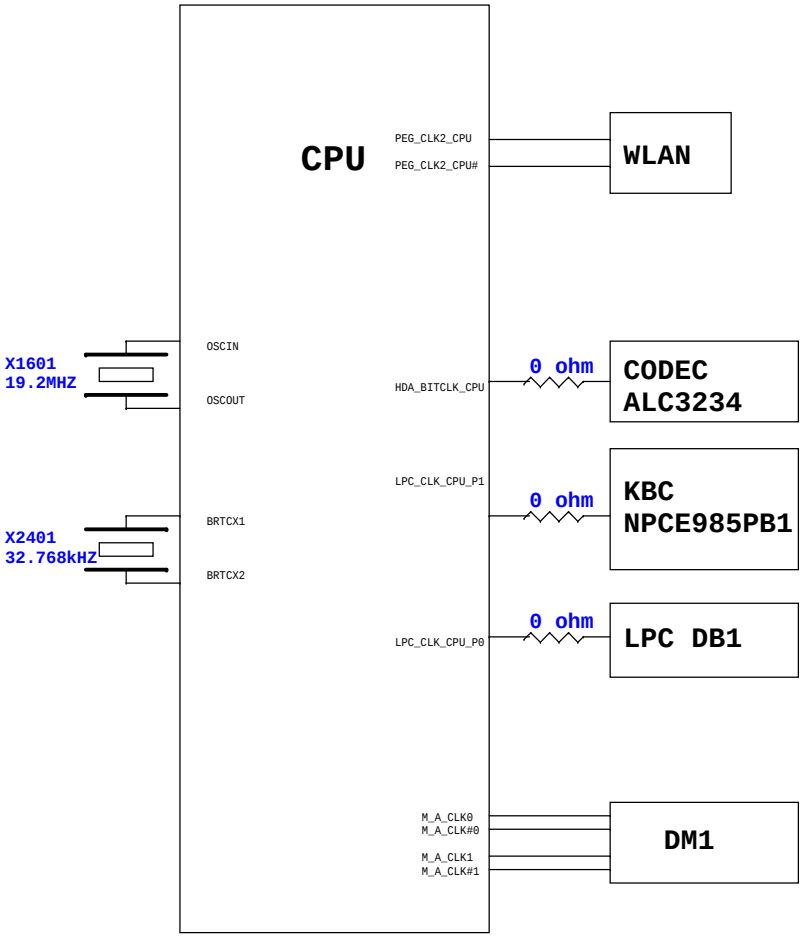
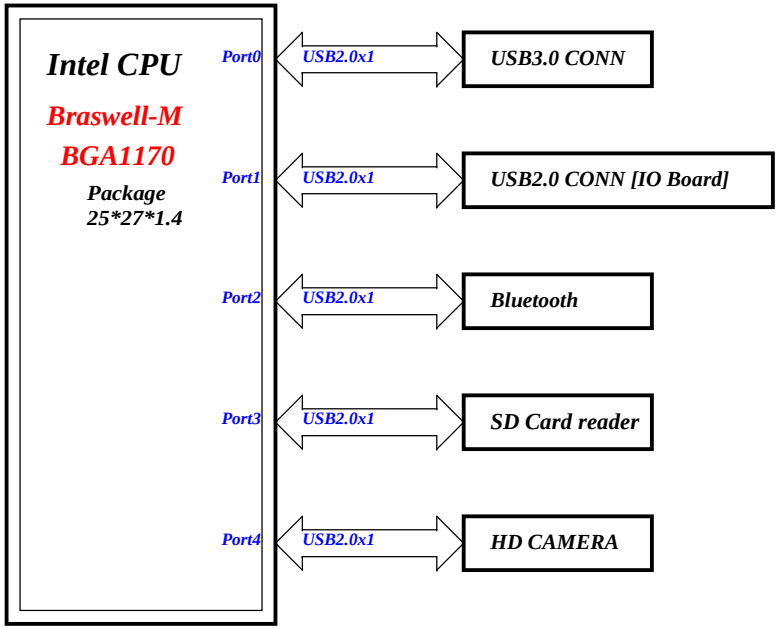
SSID = Block Diagram

CLK Block Diagram



USB2.0 Port Block Diagram



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CLK / USB Block	
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