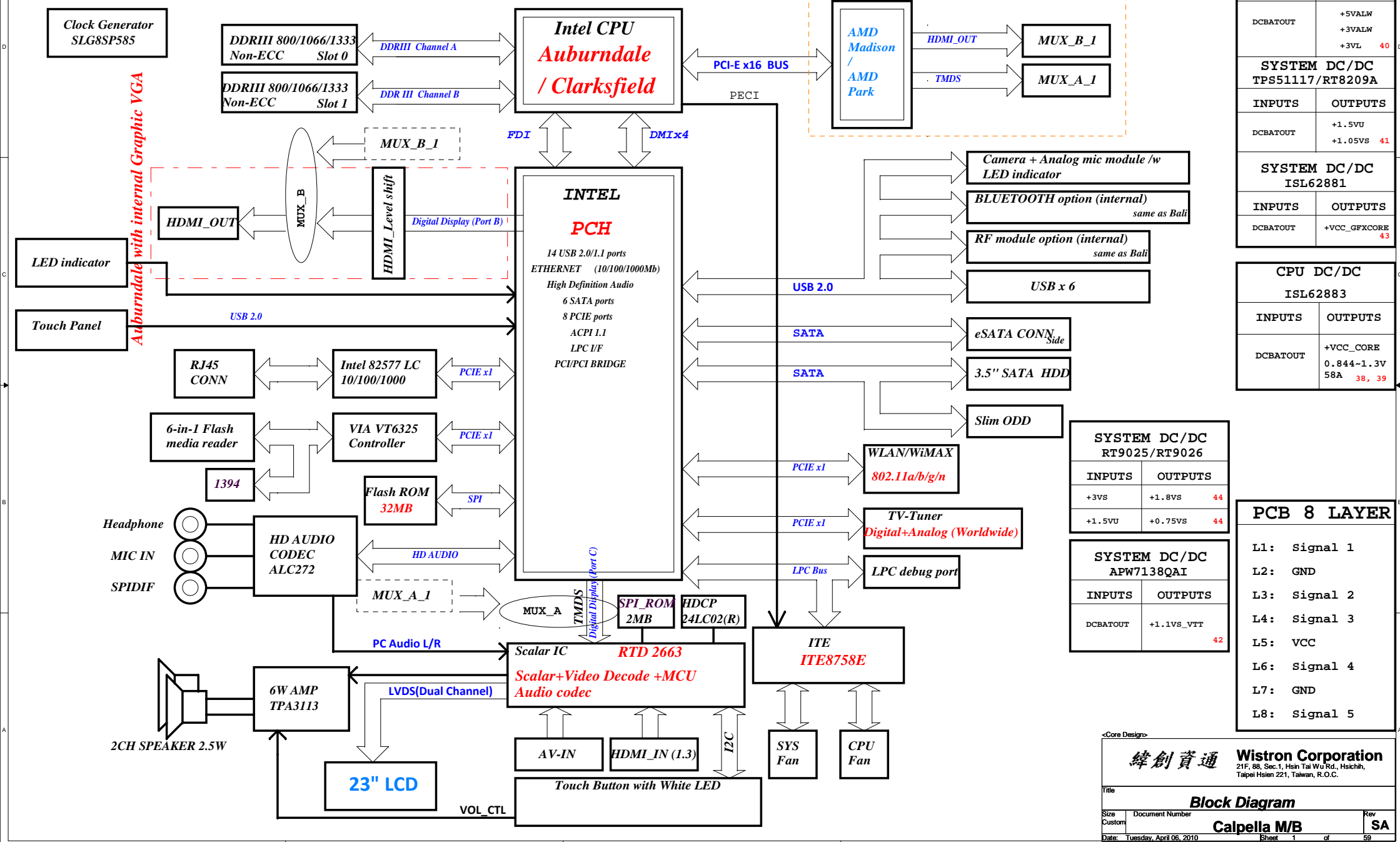


Vinafix Catalina M/B Block Diagram(Calpella)

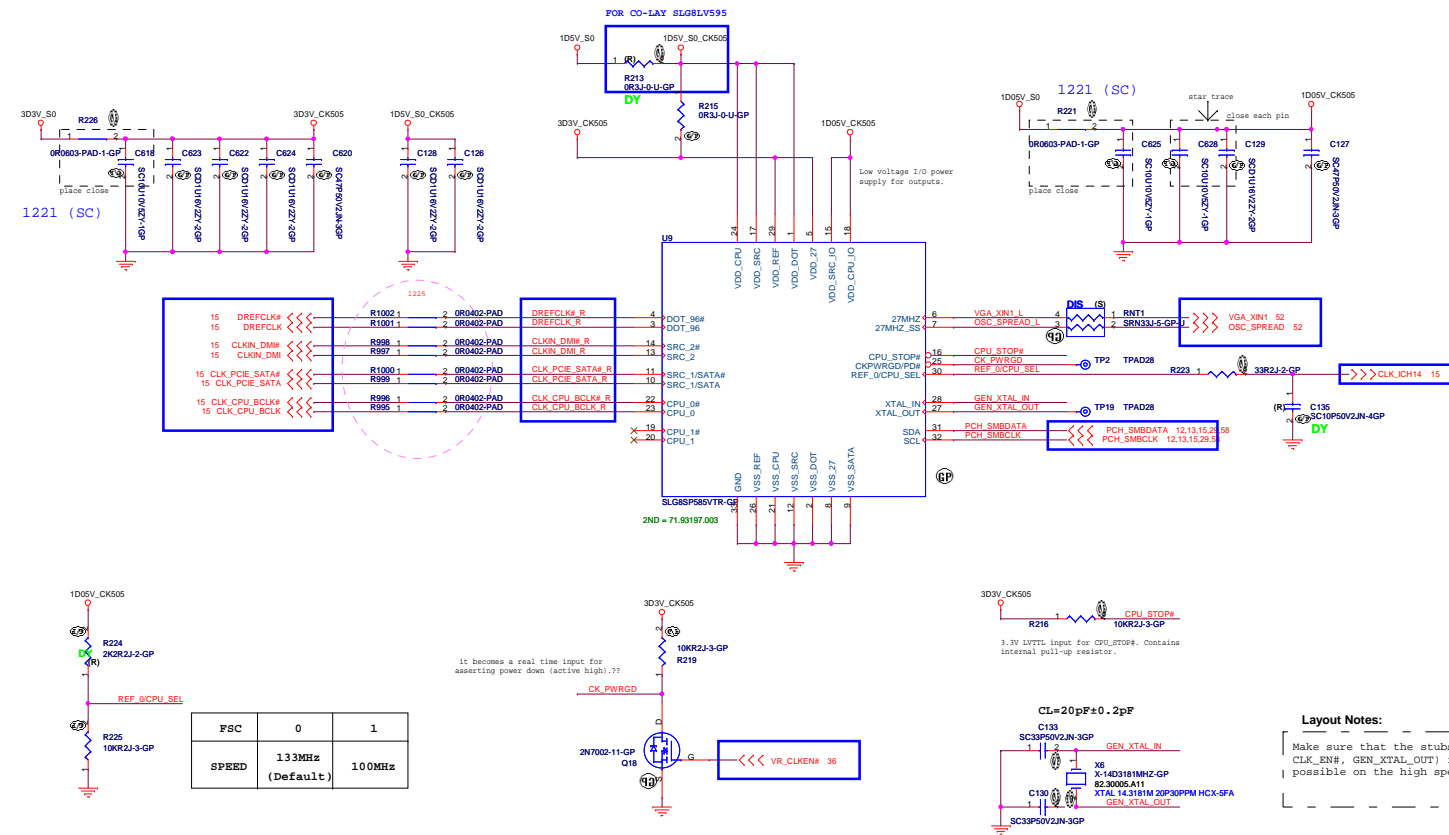


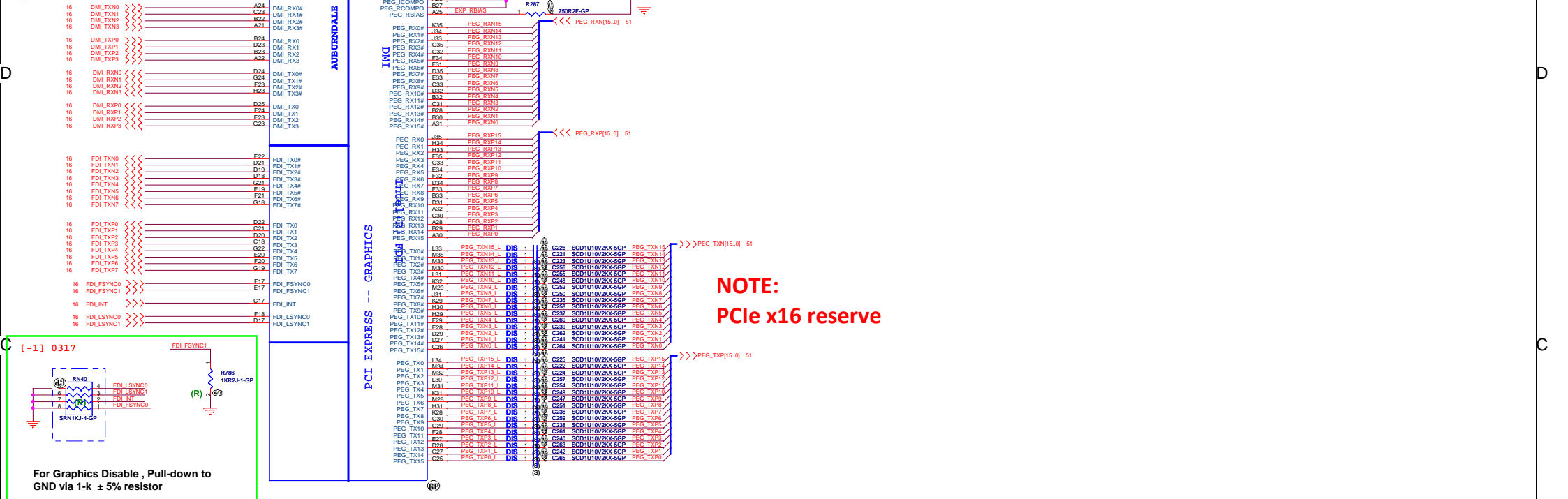
PCH Strapping

N11M-GE Power Sequence

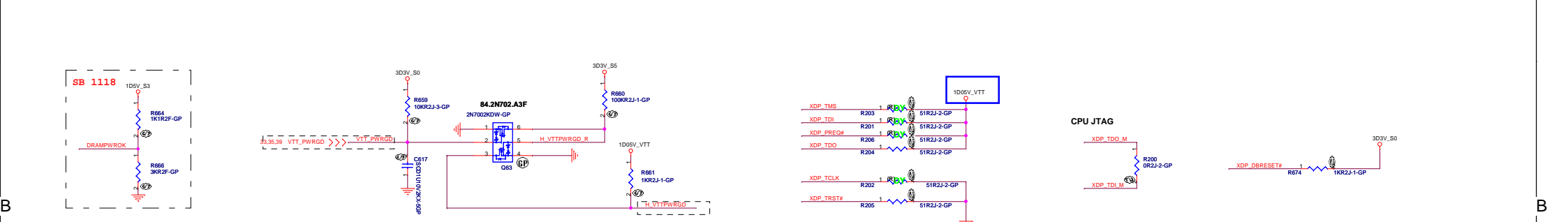
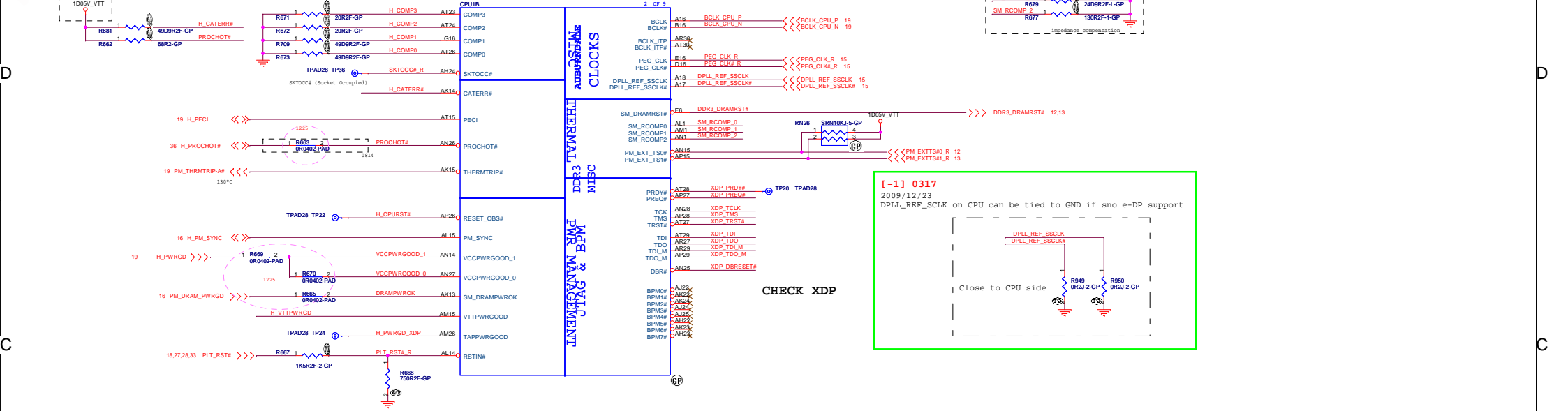


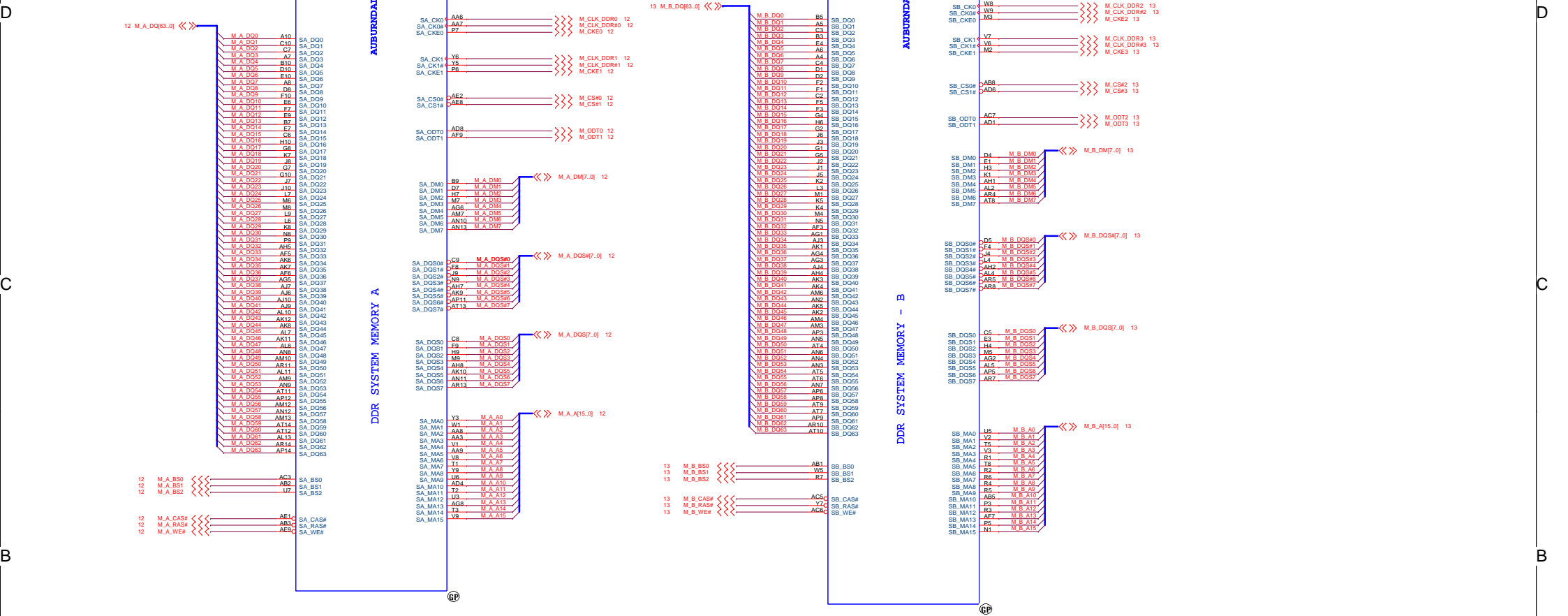
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Size	A2	Document Number			Rev
Date	Tuesday, April 06, 2010	<Doc>			<Rev Code>
		Sheet	2	of	59

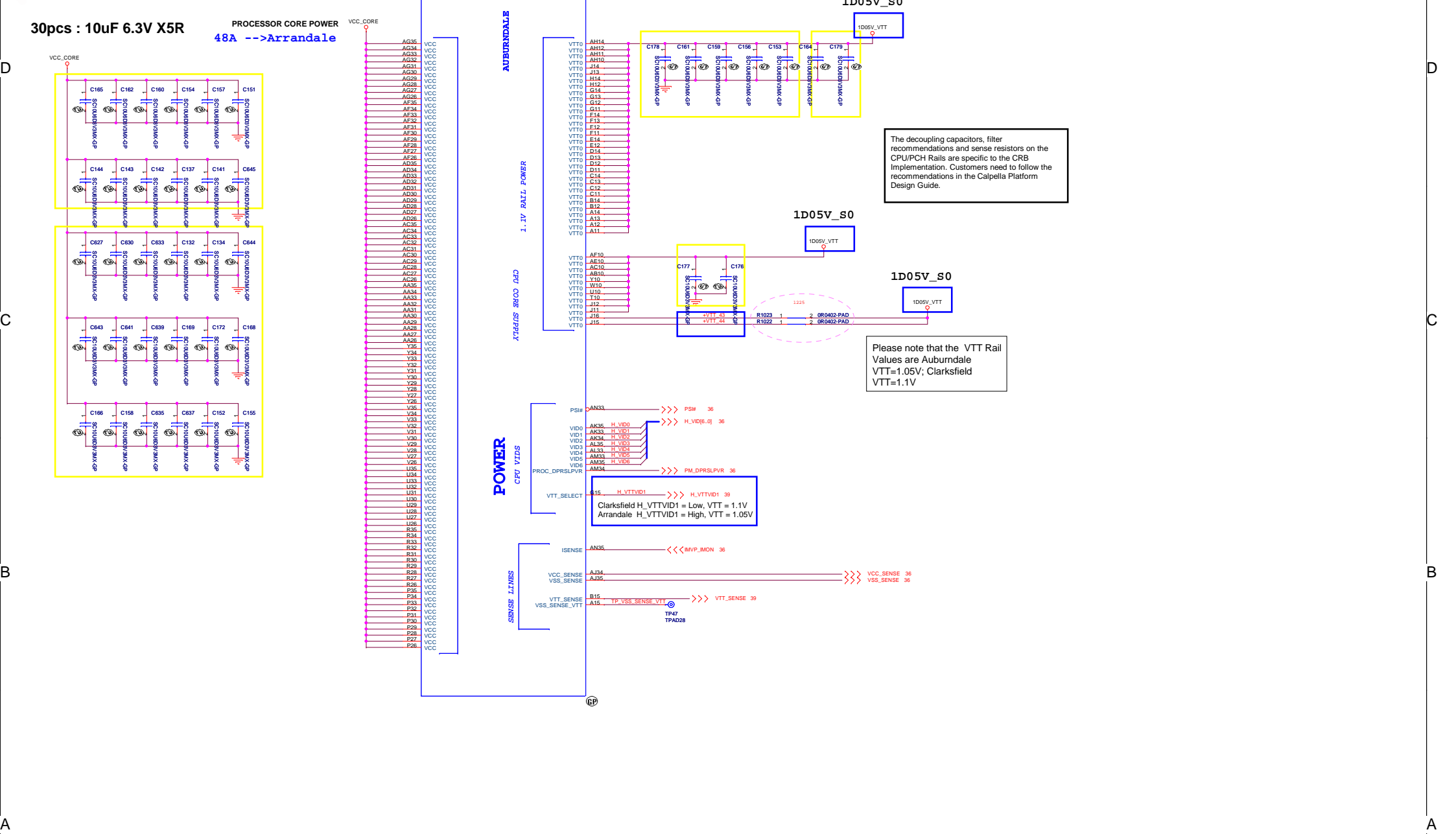


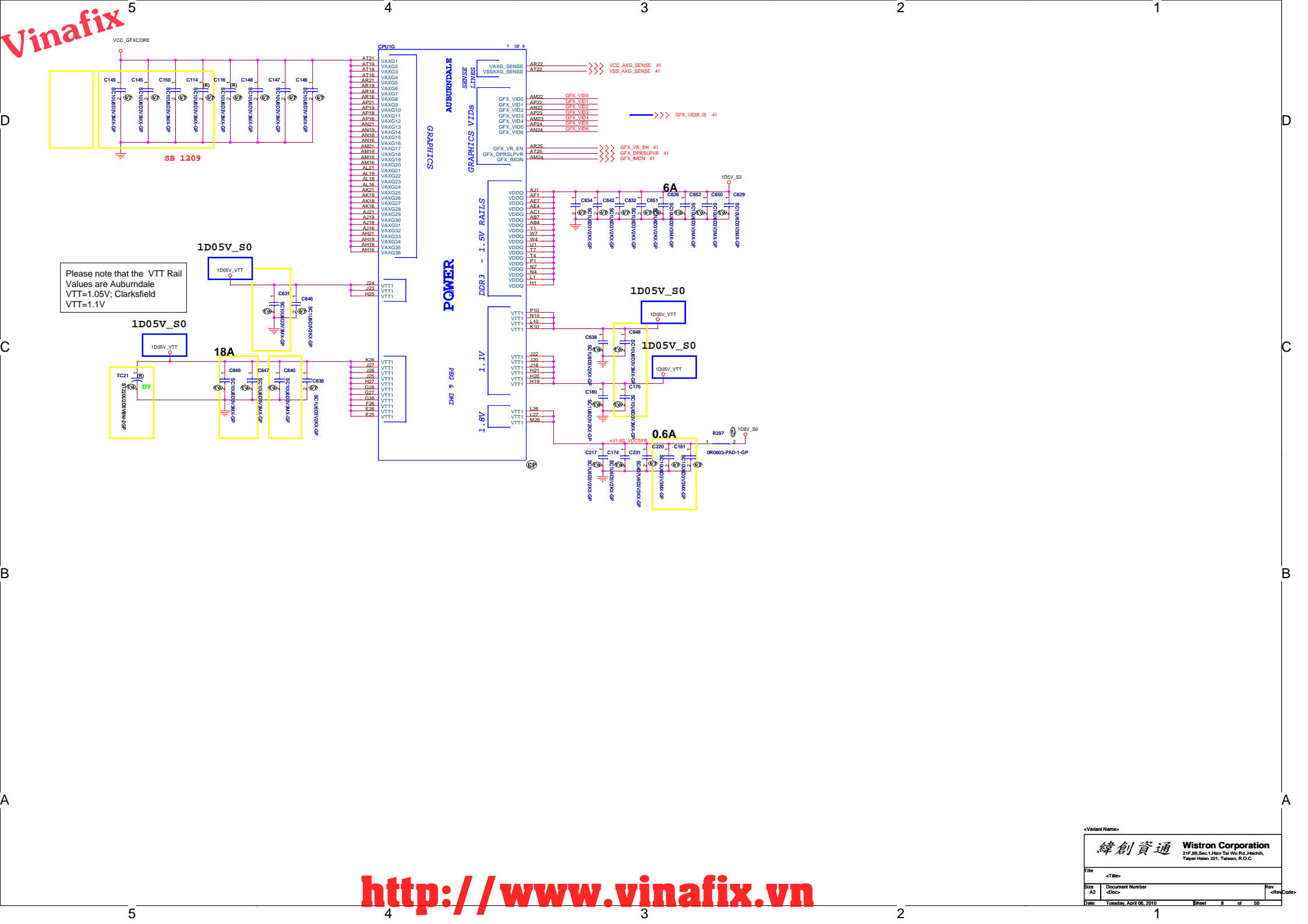


NOTE:
PCIe x16 reserve



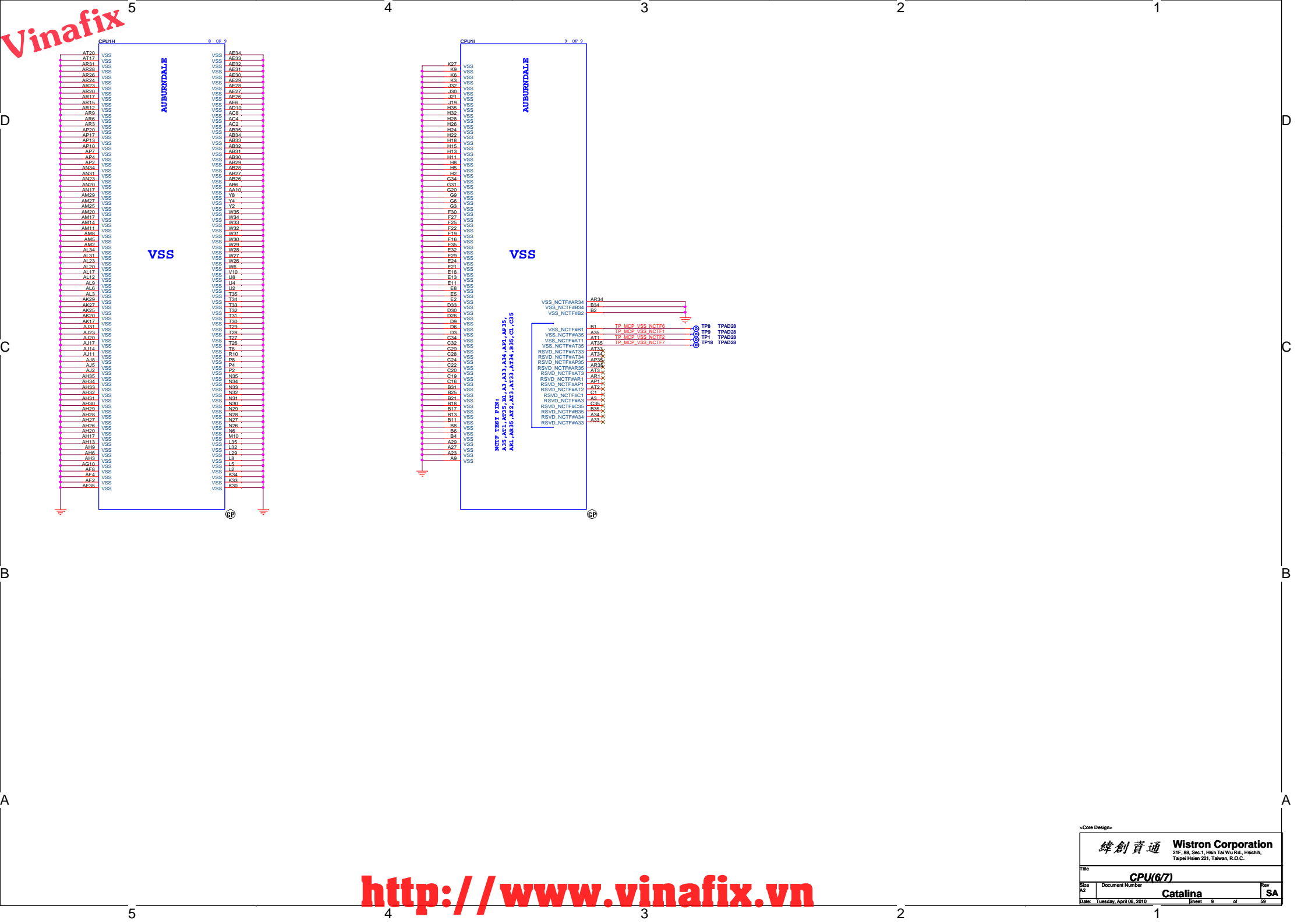




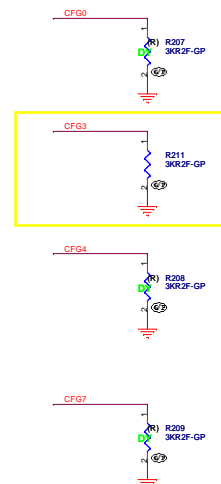
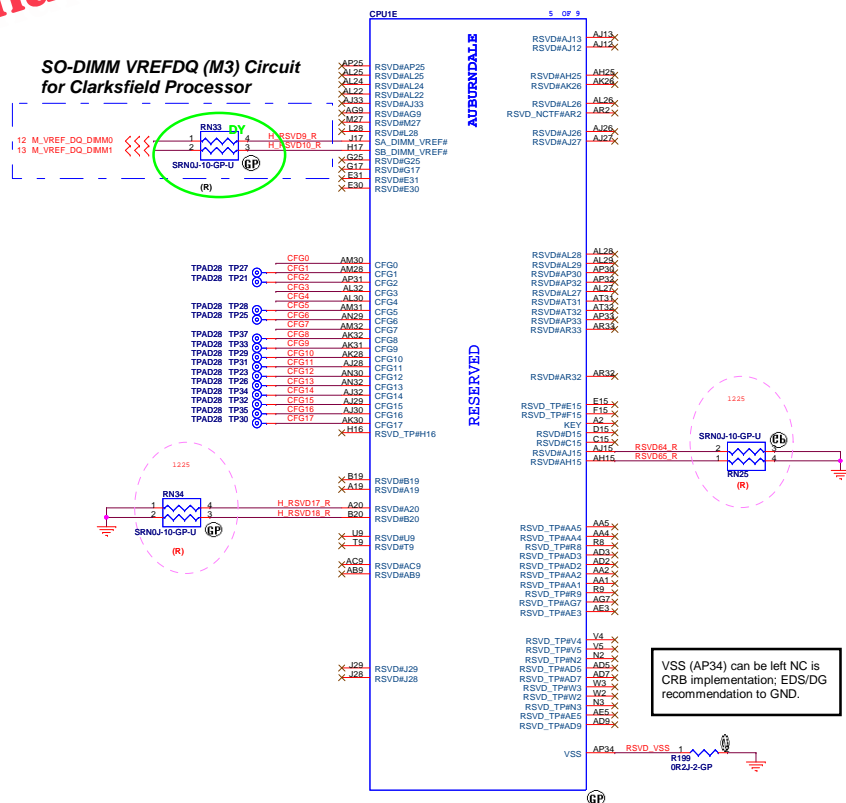


Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

<Variant Name>		<Title>	
Size A2		Document Number <Doc>	
Date: Tuesday, April 06, 2010		Sheet 8 of 59	
Rev <RevCode>			



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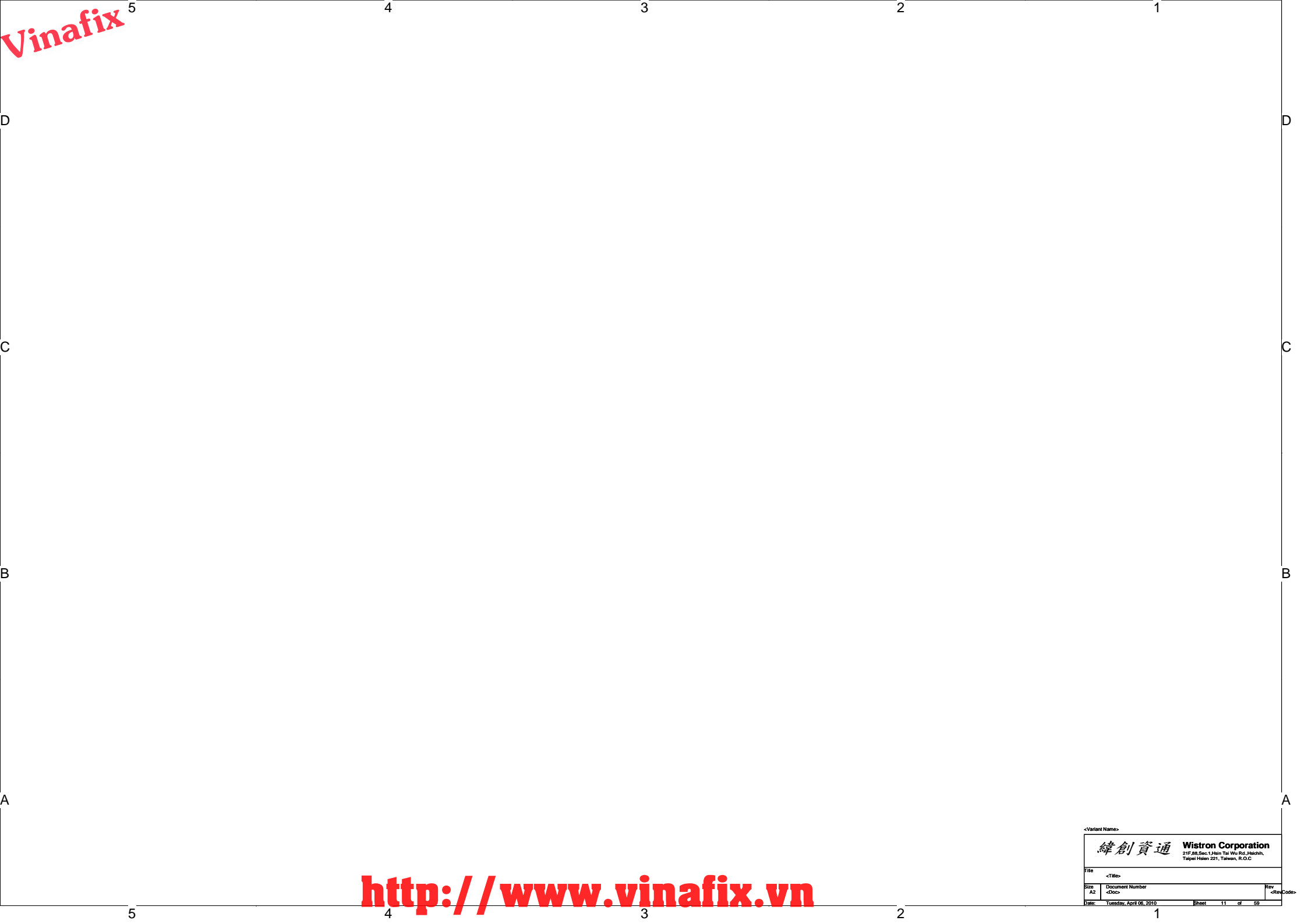
PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 : Normal Operation 0 : Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporally used for early Clarksfield samples.	
CFG7	<p>Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor.</p> <p>Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and signing report].</p> <p>For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.</p>

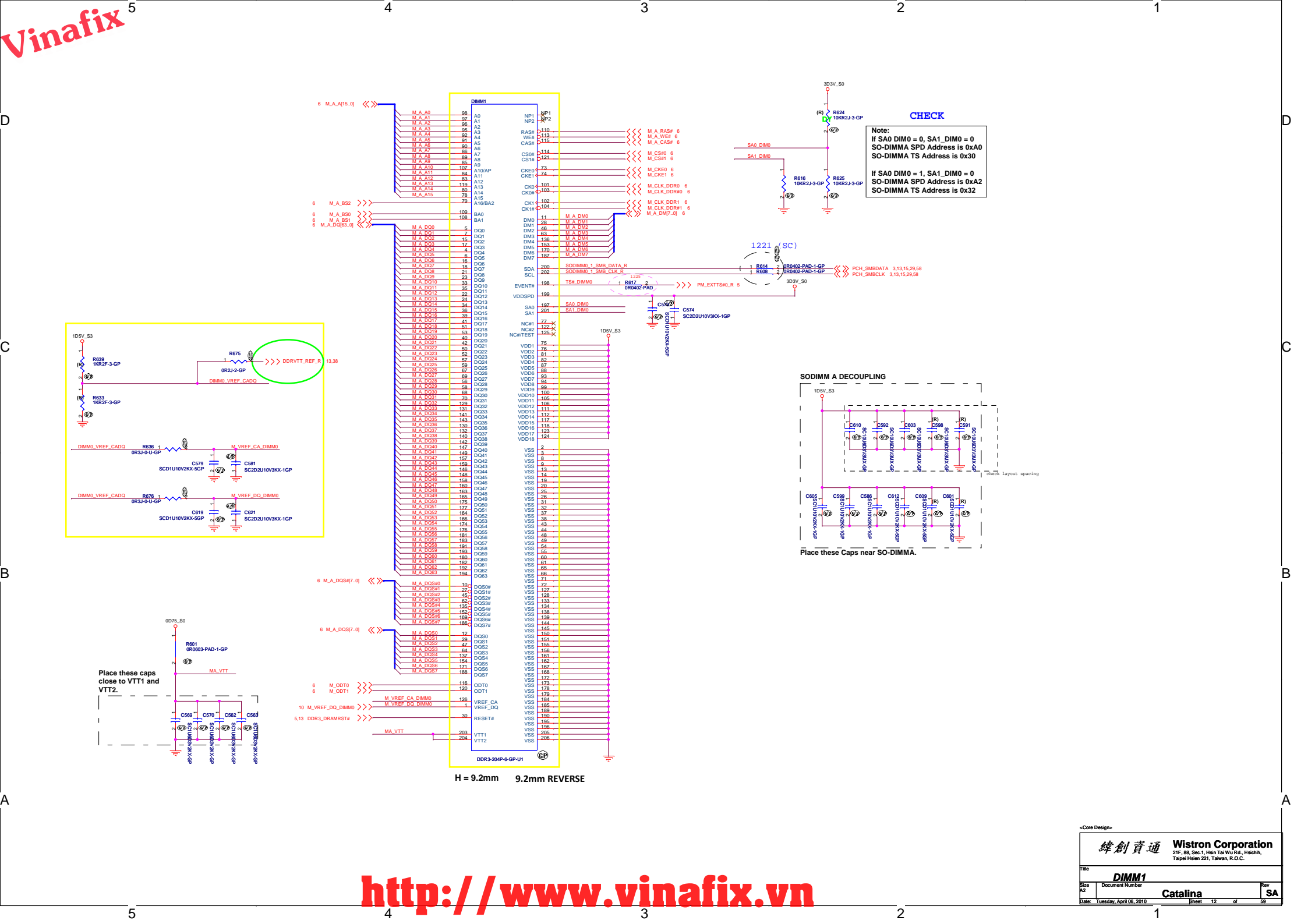
VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.



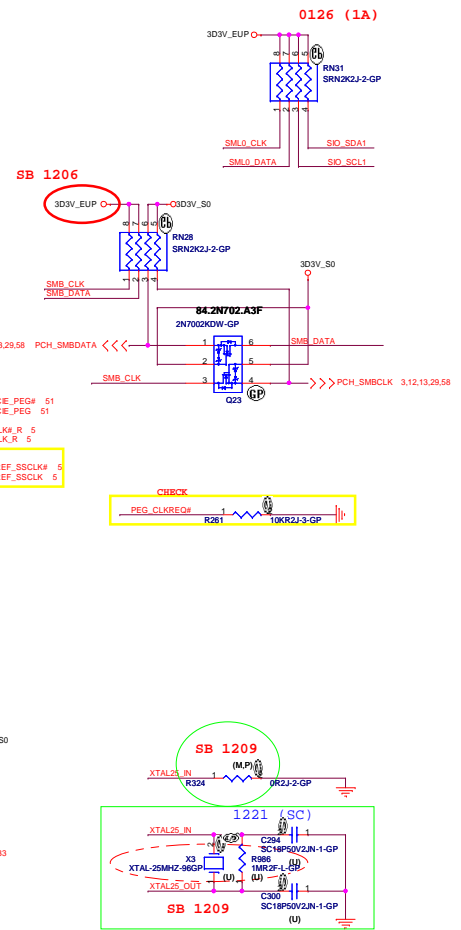
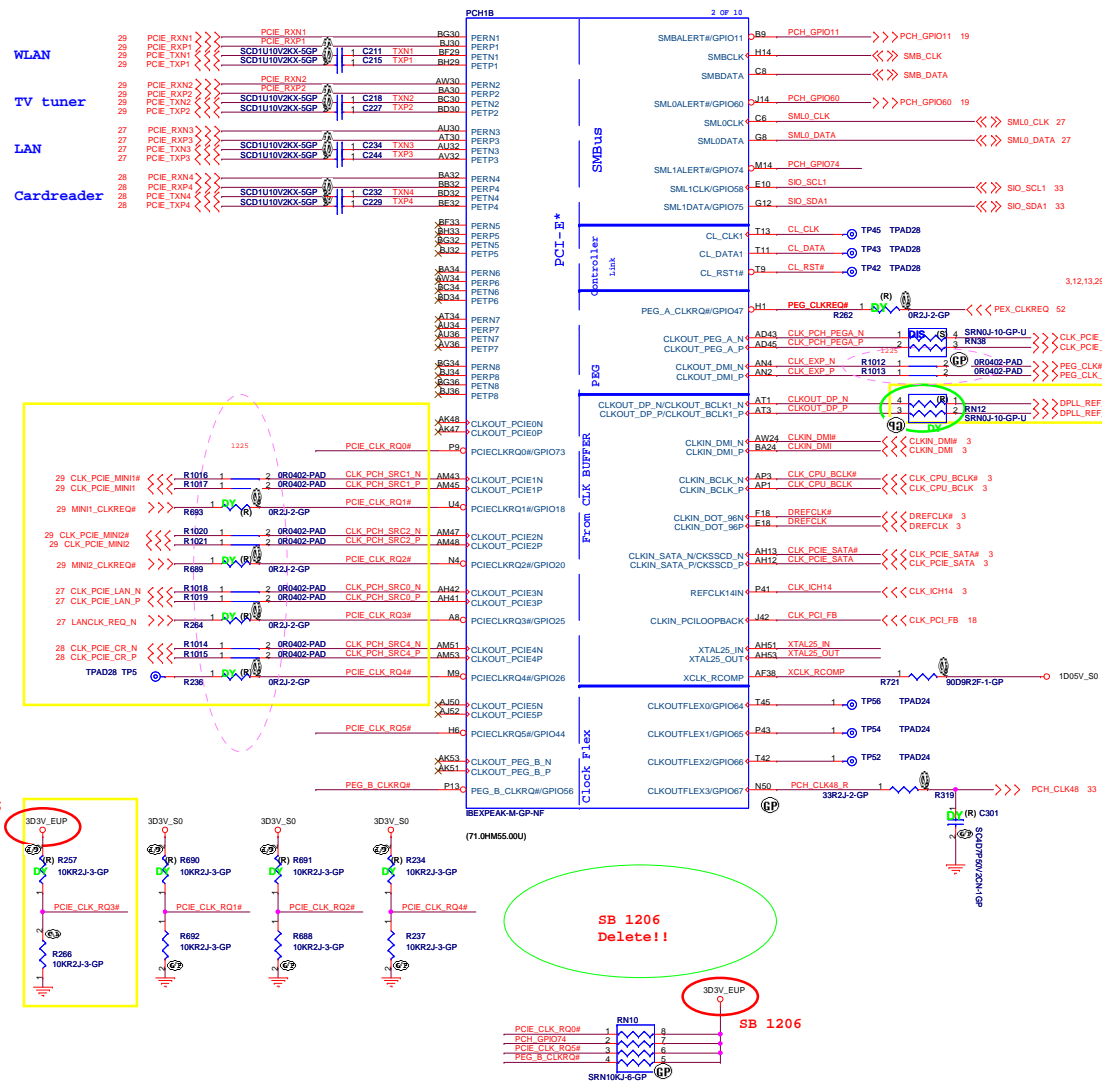
Vinafix

<http://www.vinafix.vn>

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緯創資通 Wistron Corporation		
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C		
Title <Title>		
Size A2	Document Number <Doc>	Rev <Rev>
Date: Tuesday, April 06, 2010	Sheet 11 of 59	





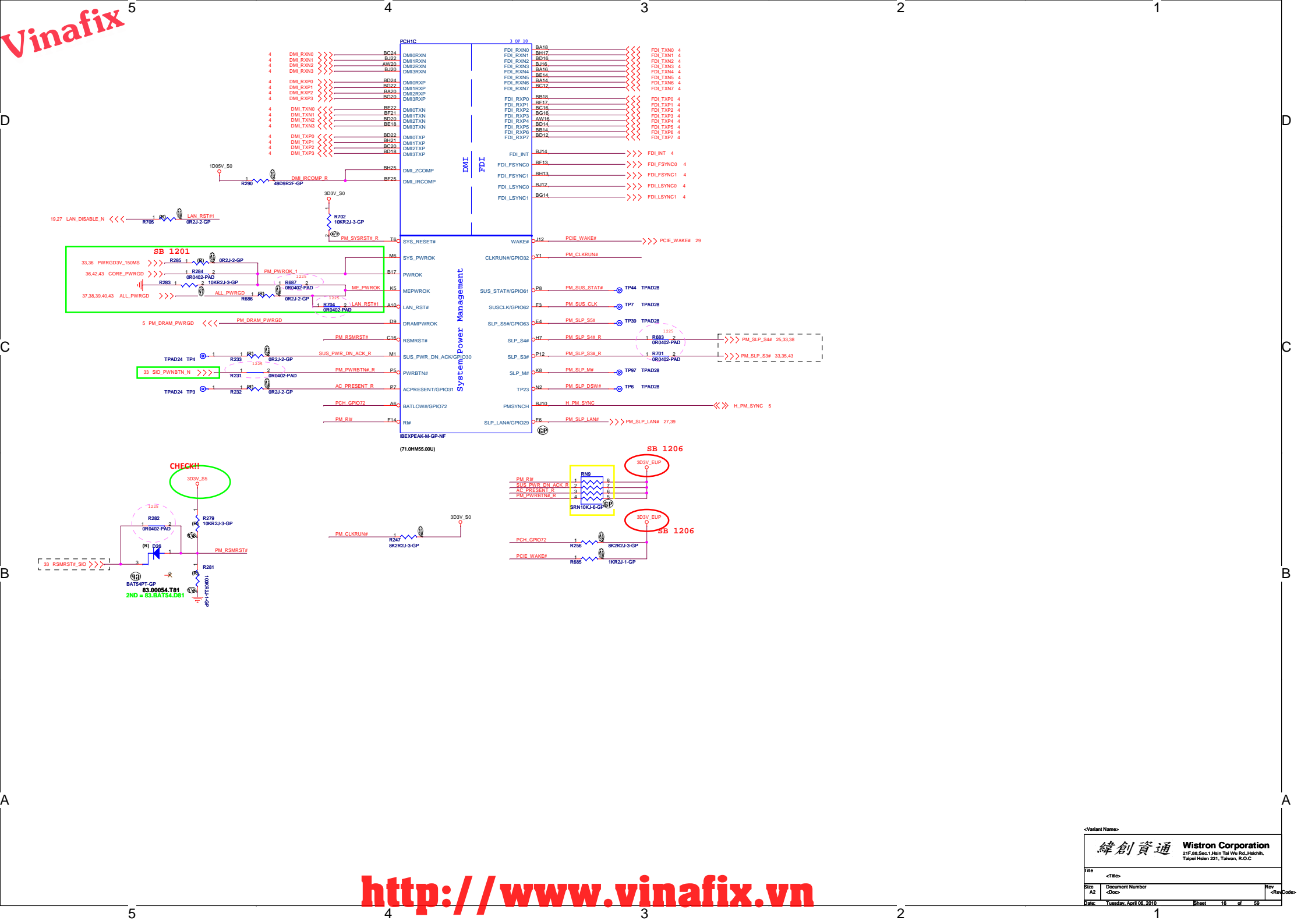


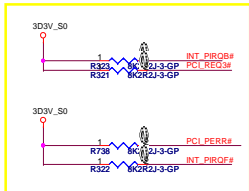
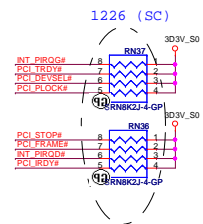
SB 1206
Delete!!

303V_EUP
SB 1

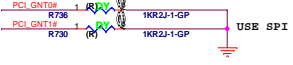
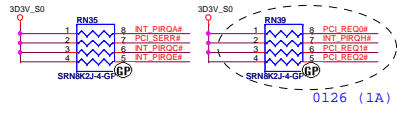
PCIE CLK_R00# 1
PCIE GPIO74 2
PCIE CLK_R05# 3
PEG 8_CLKIN0# 4

RN10
SRN10KJ4-6-CP

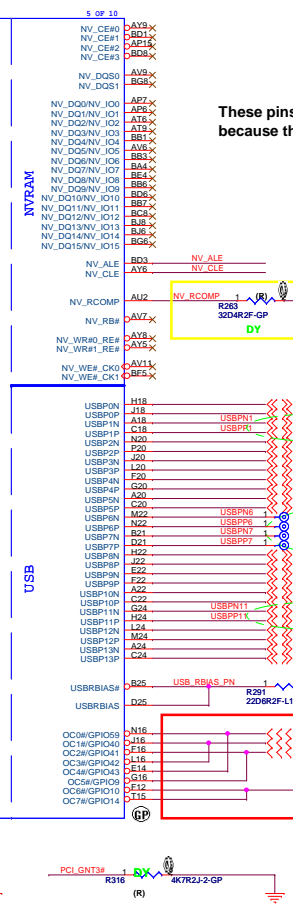
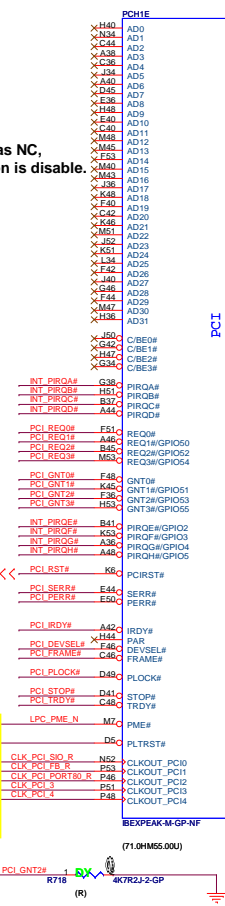
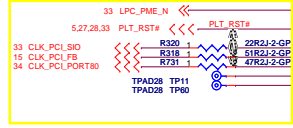




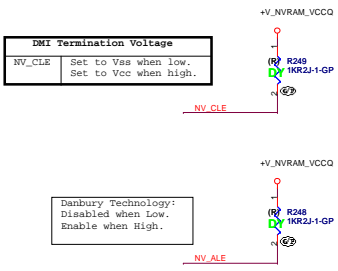
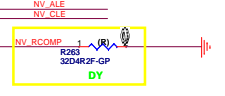
**These pins are left as NC,
because the function is disable.**



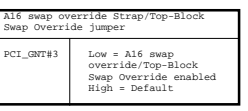
BOOT BIOS Strap		
PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC(Default)
1	0	Reserved
0	1	PCI
1	1	SPI



These pins are left as NC,
because the function is disable.



Pair	Device
0	USB0
1	<i>MINI1</i>
2	USB2
3	USB3
4	USB4
5	Touch panel
6	<i>Reserve</i>
7	<i>Reserve</i>
8	USB8
9	USB9
10	Reserve USB
11	<i>MINI2</i>
12	Bluetooth
13	Camera



Vinafix

GPIOS has a weak(20K) internal pull up.
No need to have external pull down.
GPIO pin set to high at reset.

GPIO15 has a weak(20K) internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak(20K) internal pull up.
To enable on-die PLL Voltage regulator,
should not place external pull down.

SB 1206

0126 (1A)

Placed Within 2" from PCH

Header color: RED

Clear CMOS by GPIO

MB_ID1	MB_ID0	UMA
0	0	MADISON
0	1	PARK
1	0	

1-2 NORMAL (DEFAULT)
2-3 CLR CMOS

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Date: Tuesday, April 06, 2010 Sheet 19 of 59

Vinafix

GPIOS has a weak(20K) internal pull up.
No need to have external pull down/up.
GPIO pin set to high at reset.

GPIO15 has a weak(20K) internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak(20K) internal pull up.
To enable on-die PLL Voltage regulator,
should not place external pull down.

SB 1206

0126 (1A)

Placed Within 2" from PCH

Header color: RED

Clear CMOS by GPIO

MB_ID1	MB_ID0	UMA
0	0	MADISON
1	0	PARK

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Vinafix

GPIOS has a weak(20K) internal pull up.
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High : ME Crypto TLS with confidentiality

GPIO27 has a weak(20K) internal pull up.
To enable on-die PLL Voltage regulator,
should not place external pull down.

SB 1206

0126 (1A)

Placed Within 2" from PCH

Header color: RED

Clear CMOS by GPIO

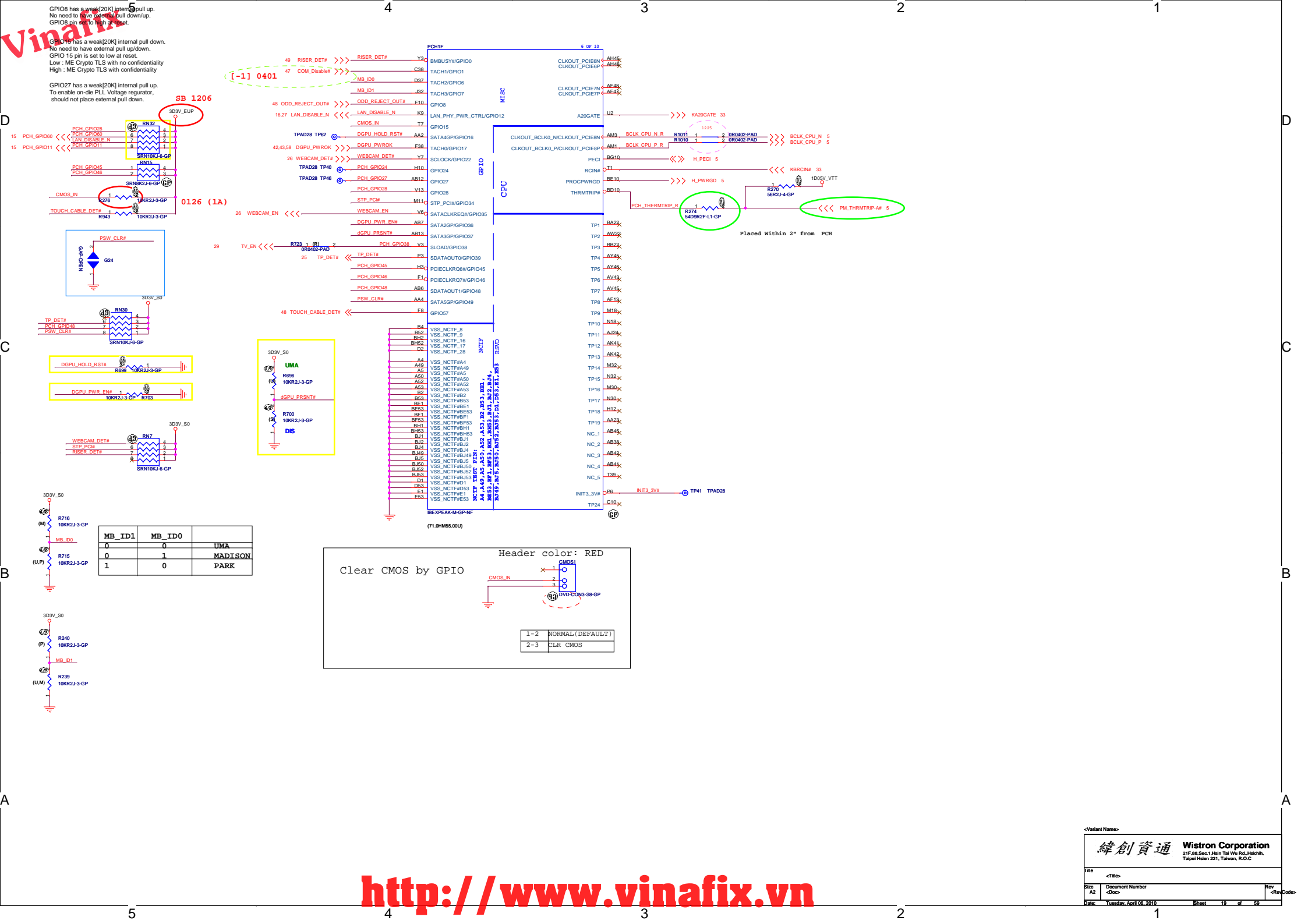
MB_ID1	MB_ID0	UMA
0	0	MADISON
0	1	PARK
1	0	

1-2 NORMAL (DEFAULT)
2-3 CLR CMOS

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[illegible]

Vinafix

GPIOS has a weak(20K) internal pull up.
No need to have external pull down.
GPIO pin set to high at reset.

GPIO15 has a weak(20K) internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak(20K) internal pull up.
To enable on-die PLL Voltage regulator,
should not place external pull down.

SB 1206

0126 (1A)

Placed Within 2" from PCH

Header color: RED

Clear CMOS by GPIO

MB_ID1	MB_ID0	UMA
0	0	MADISON
0	1	PARK
1	0	

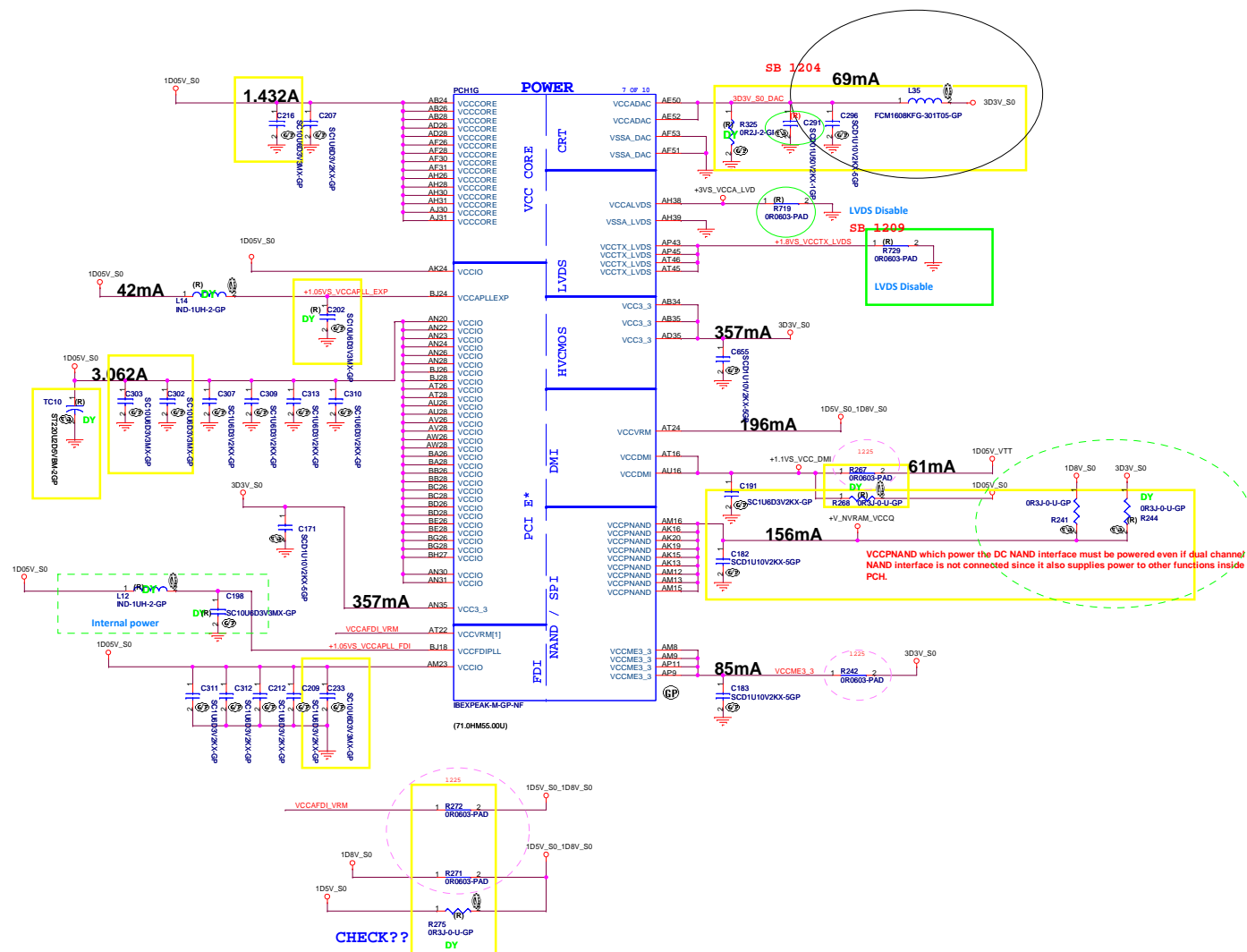
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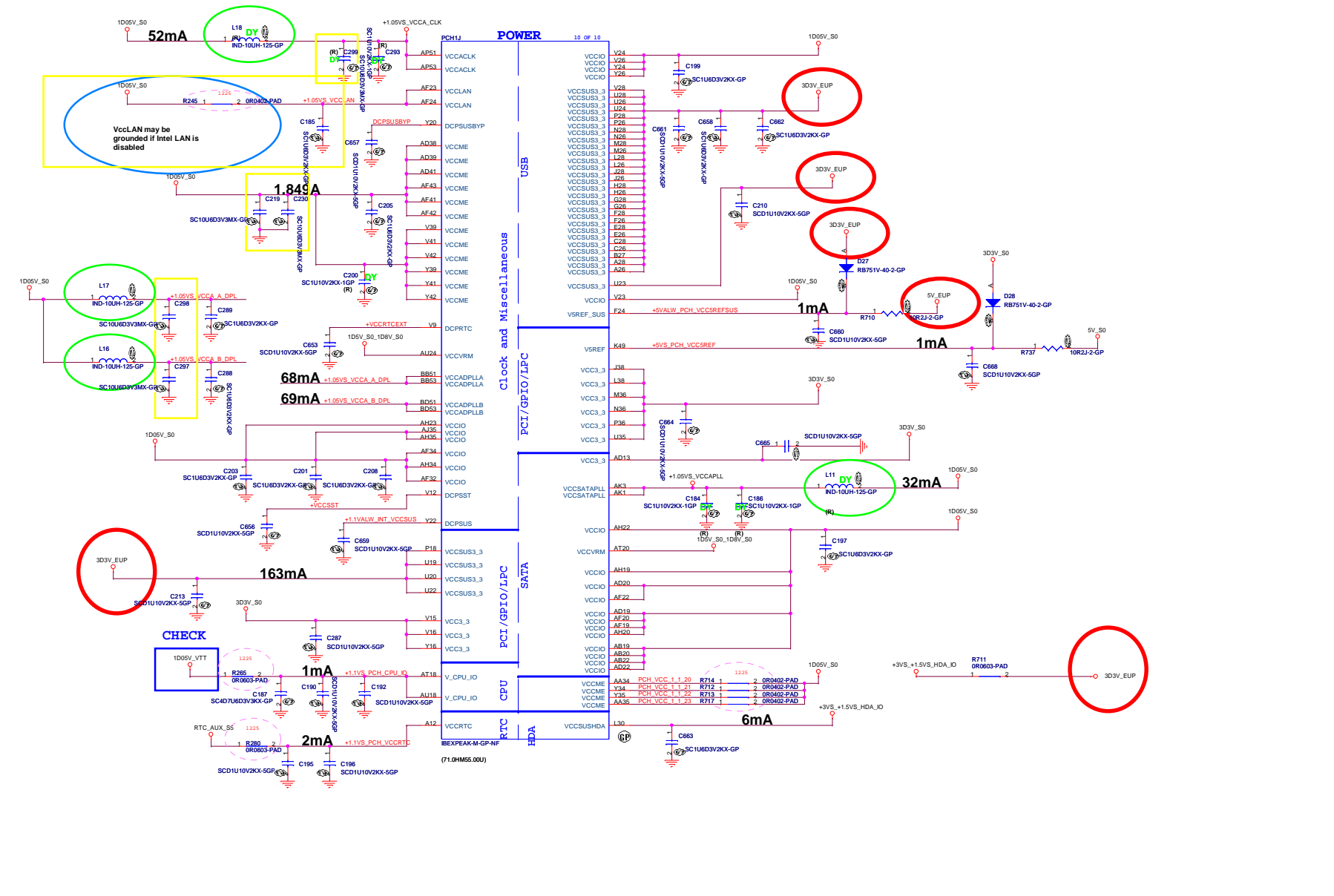
Date: Tuesday, April 06, 2010 Sheet 19 of 58

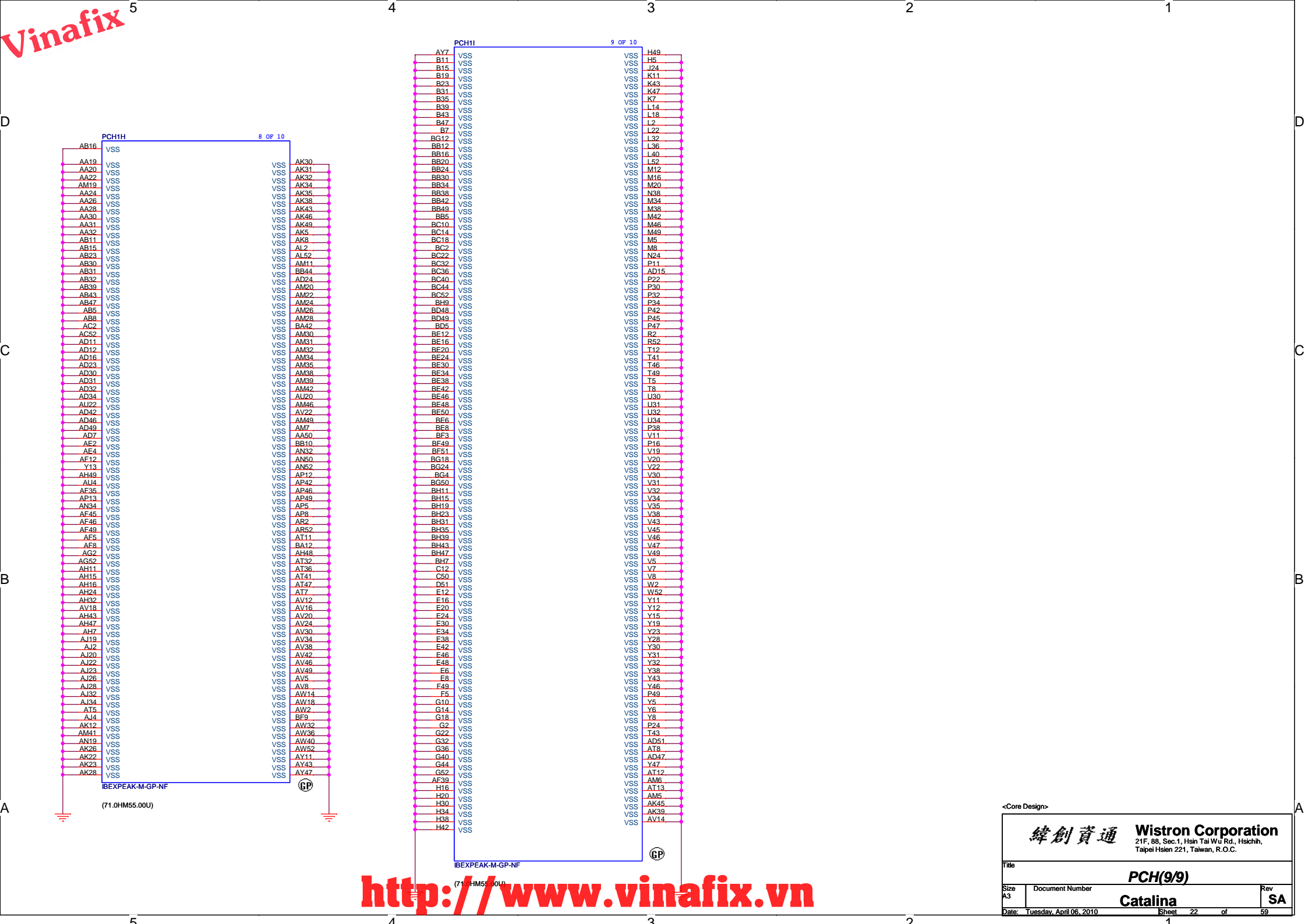
Wistron Corporation
21F, #8, Sec. 1 Main Tai Wu Rd., Hsinchu, Taiwan 301, Taiwan, R.O.C.

<http://www.vinafix.vn>

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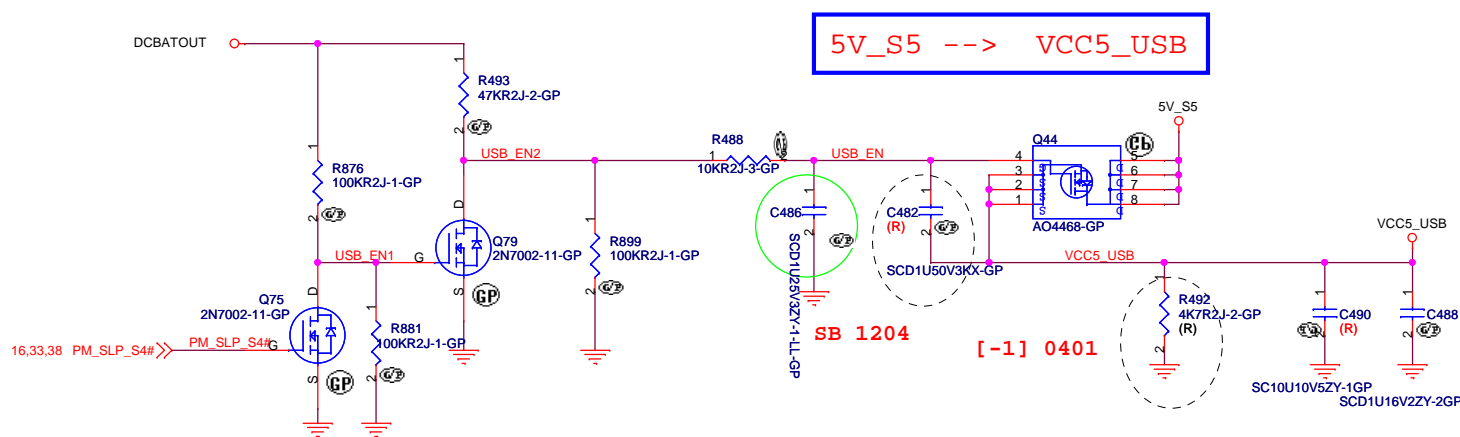




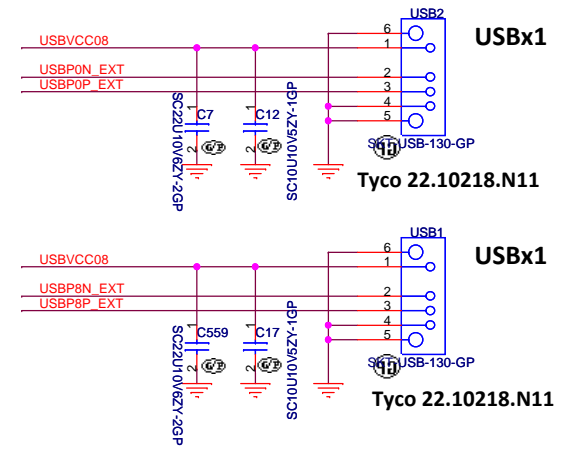
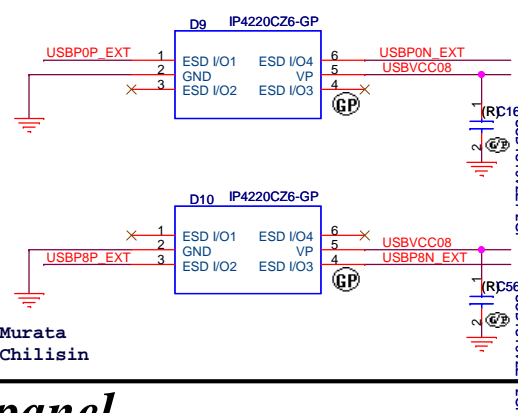
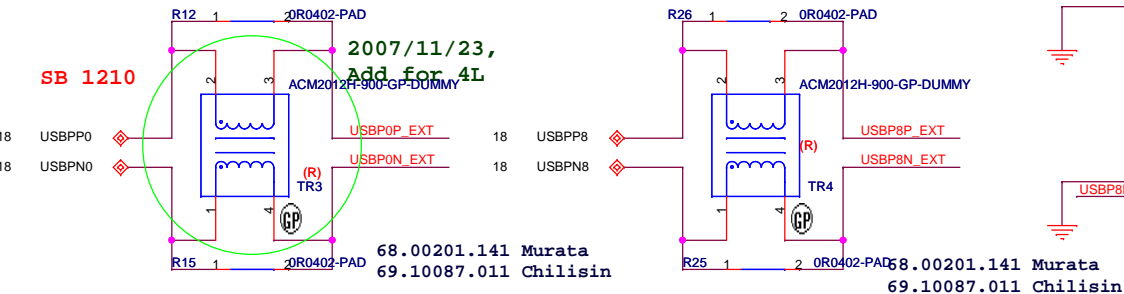
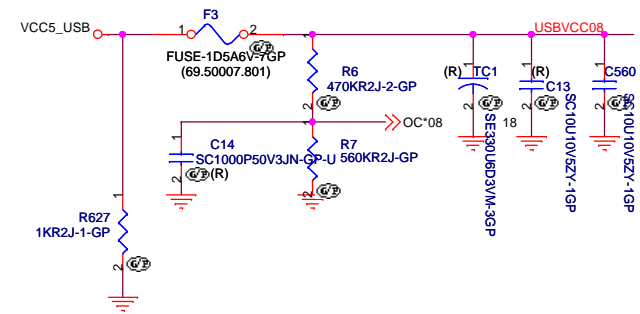




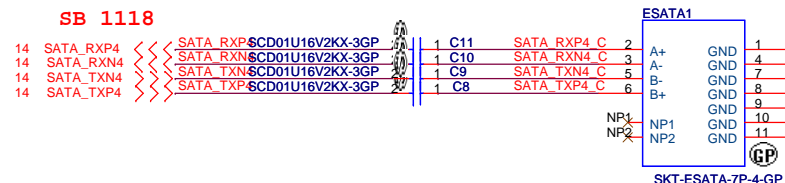
USB PORT Side 2 USB PORT (0/1)



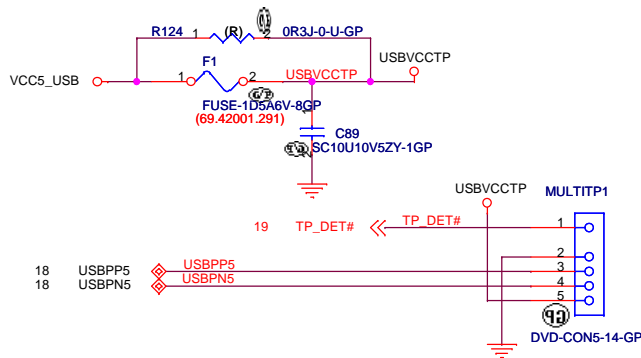
USB Power



eSATA PORT



Touch panel



<Core Design>

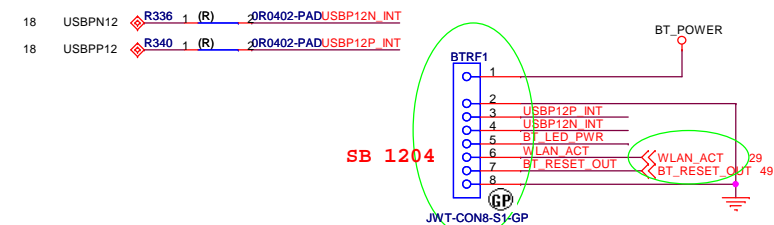
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
USB IO/eSATA/TP		
Size	Document Number	Rev
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Date: Tuesday, April 06, 2010	Sheet 25 of 59	



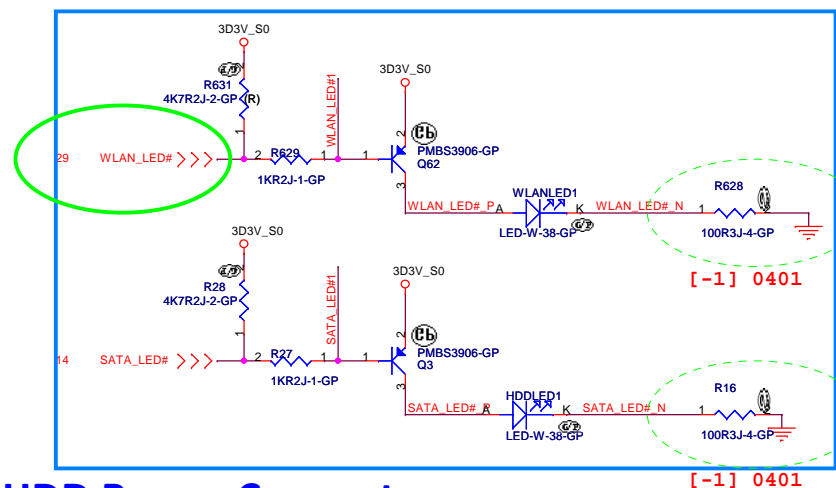
SB 1204

Blue tooth



SB 1204

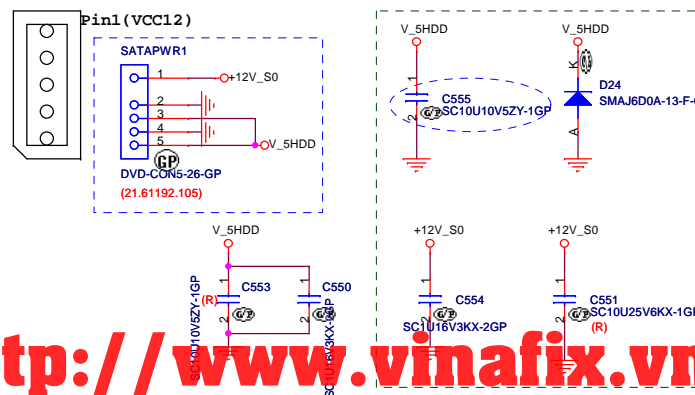
Check connection!!



Check connection!!

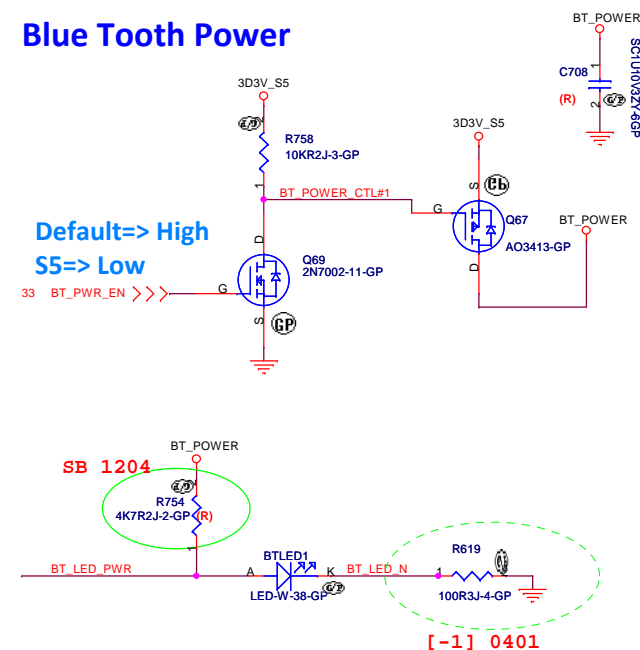


Layout: Please put them together



Blue Tooth Power

Default=> High
S5=> Low



<Core Design>

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

HDD/ODD IF+USB device

Size

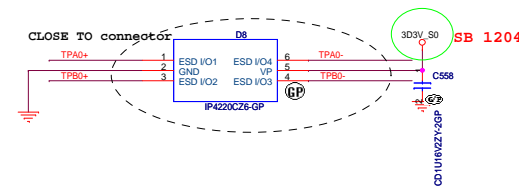
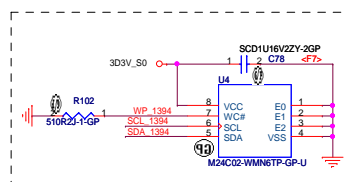
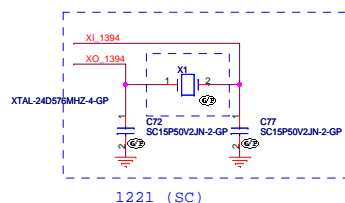
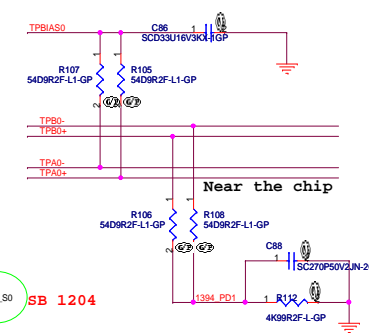
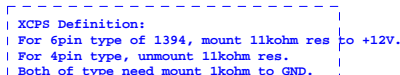
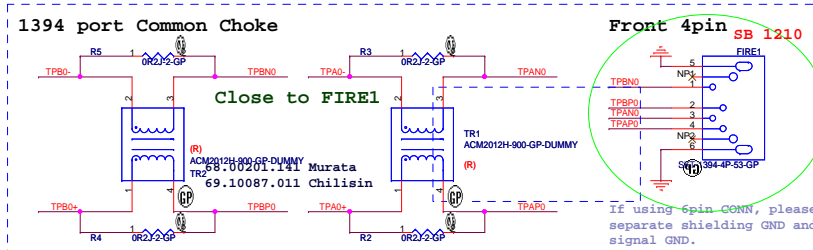
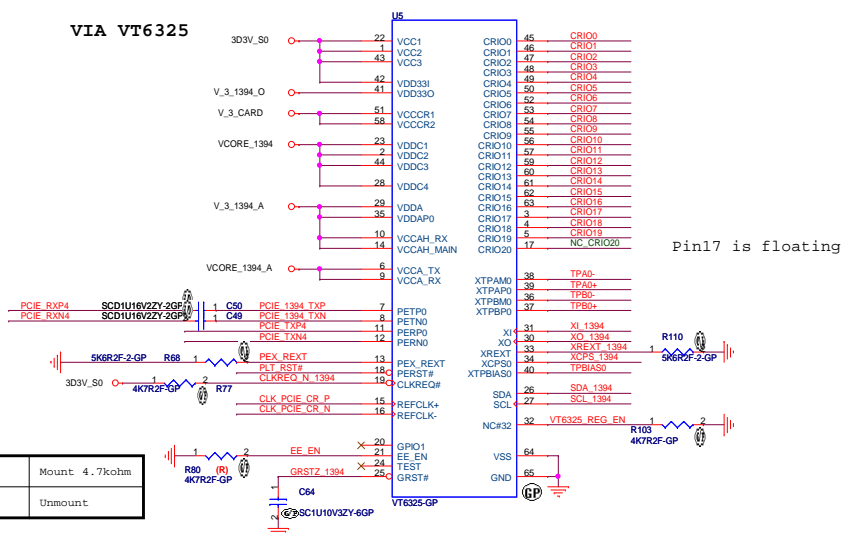
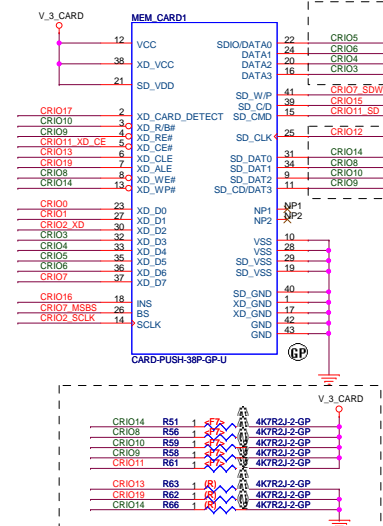
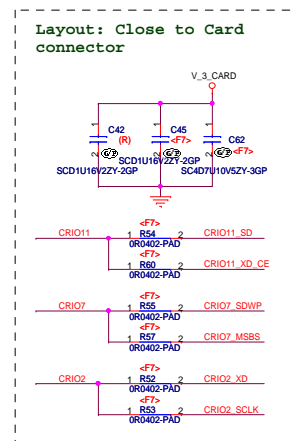
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Catalina

Rev

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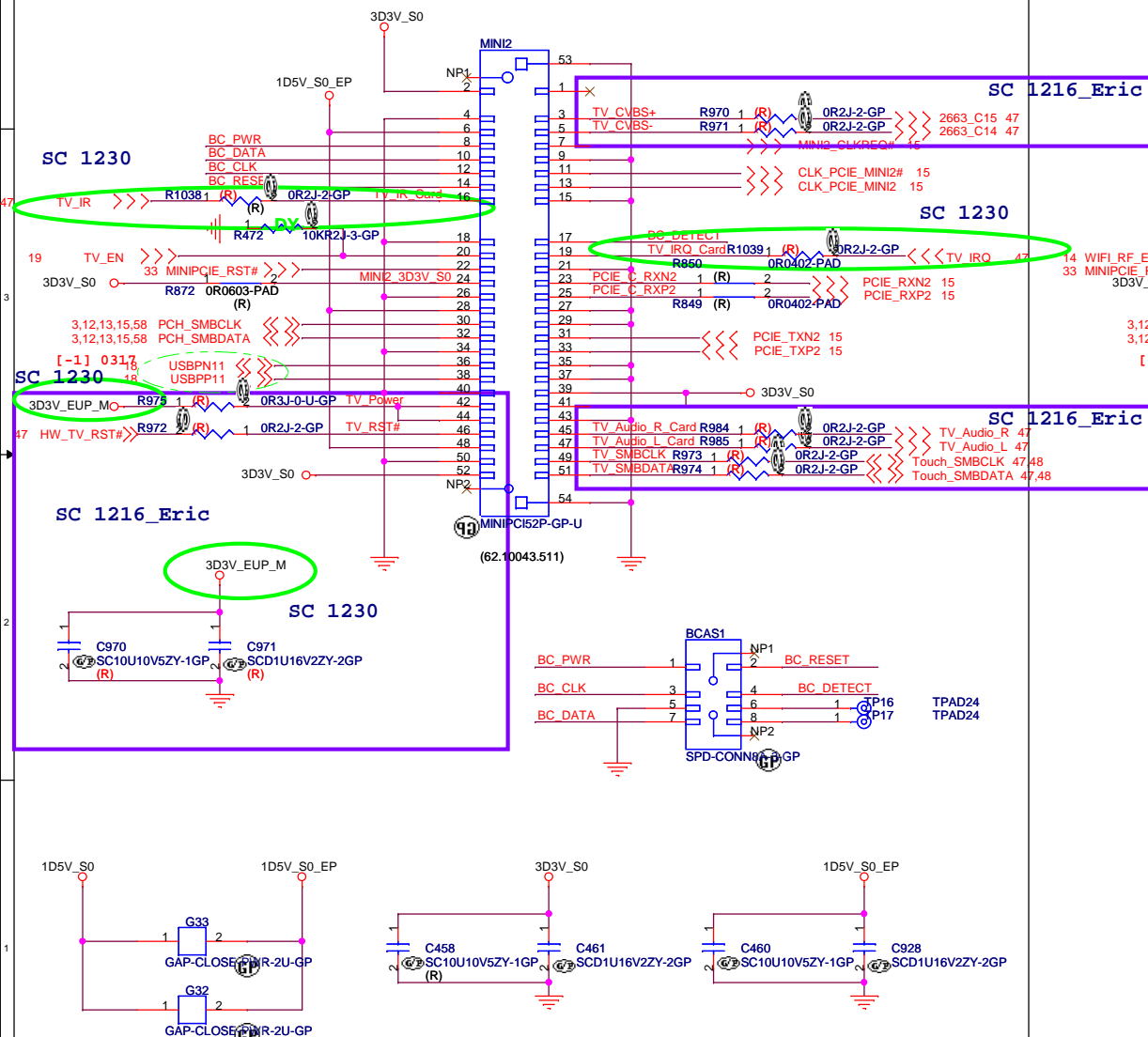


緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

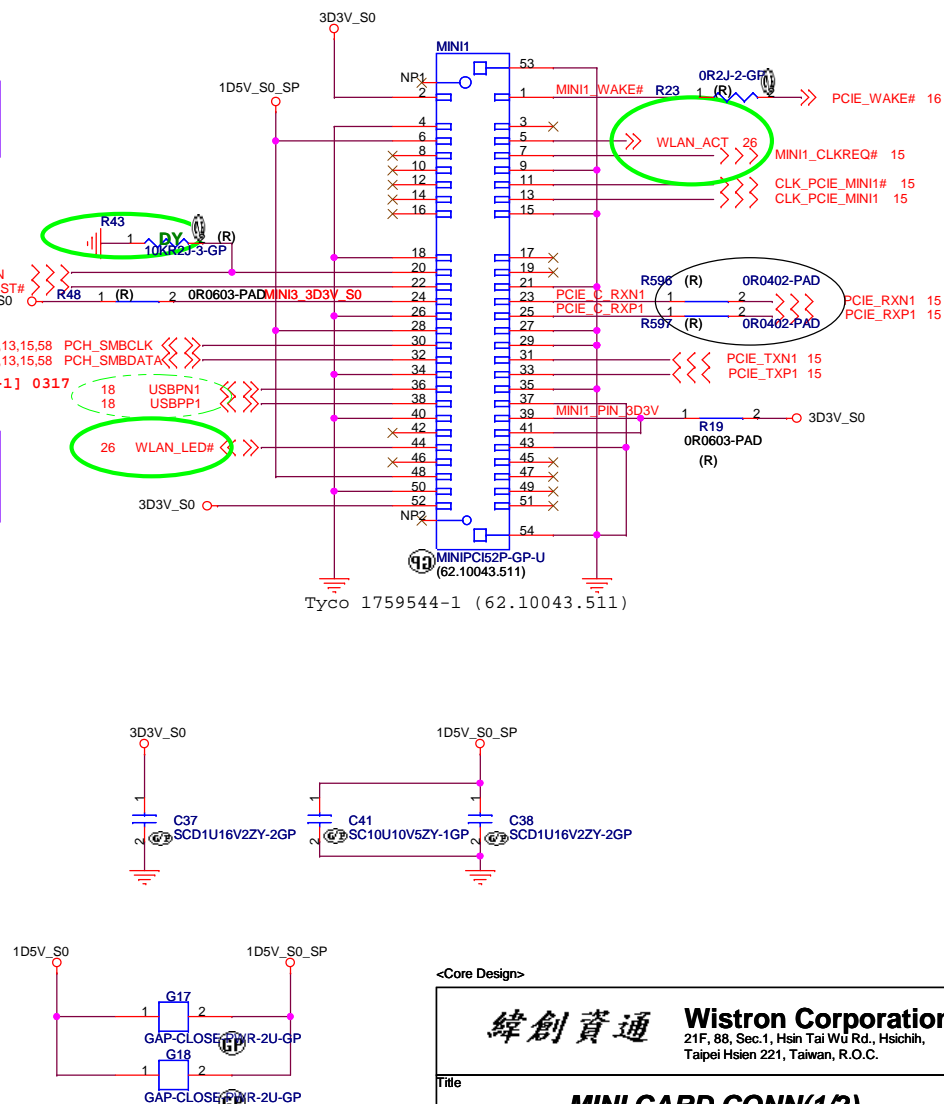
File			
VT6325 1394/CARD READER			
Size	Document Number	Rev	
C	Catalina	S	
Enter	Thursday, April 06, 2010	Sheet	28 of 60

Mini PCI-E Connector

TV-TUNER Card



Wireless Card(Present support EP/SP)



<Core Design>

緯創資通

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

MINI CARD CONN(1/2).

Size

Document Number

Catalina

Rev

Date: Tuesday, April 06, 2010

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	A	B	C	D	E
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3					
2					
1					<div><Core Design></div> <div> <div> <div>緯創資通</div> <div> Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wuj Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. </div> </div> <div> <div>Title</div> <div>Reserve</div> <div> <div>Size B</div> <div>Document Number</div> <div>Rev SA</div> </div> </div> <div> <div>Date: Tuesday, April 06, 2010</div> <div> <div>Sheet E</div> <div>31</div> <div>of</div> <div>59</div> </div> </div> </div>
	A	B	C	D	E

Vinafix

MIC IN

30 MIC_L_JACK >>> MIC_IN_L
30 MIC_R_JACK >>> MIC_IN_R

HP OUT

30 ALC272_HP_OUT_L >>> ALC272_HP_OUT_L
30 ALC272_HP_OUT_R >>> ALC272_HP_OUT_R

JACK DETECT

30 MIC_IN_JD >>> MIC_IN_JD
30 HP_OUT_JD >>> HP_OUT_JD

30 EAPD# >>> EAPD#

47,48 TPA3113_SD# >>> TPA3113_SD#

LINE OUT to Scalar

30 PC_AUDIO_R >>> PC_AUDIO_R
30 PC_AUDIO_L >>> PC_AUDIO_L
47 PC_AUDIO_R_C >>> PC_AUDIO_R_C
47 PC_AUDIO_L_C >>> PC_AUDIO_L_C

HP JACK (14/15)

Chech Jack Spec

HP OUT

SB 1209 DELETE!!

FRONT MIC JACK (21/22)

MIC IN

Speaker Out (35/36) Placement Near Scalar

PC AUDIO R 2 R605 1 PC AUDIO R 1 C572 1 SC22U6D3V5MX-2GP near codec
PC AUDIO L 2 R604 1 PC AUDIO L 1 C571 1 SC22U6D3V5MX-2GP near codec

SB 1209

SB 1209

SC 1226

<http://www.vinafix.vn>

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AUDIO HP JK/ MIC JK

Document Number

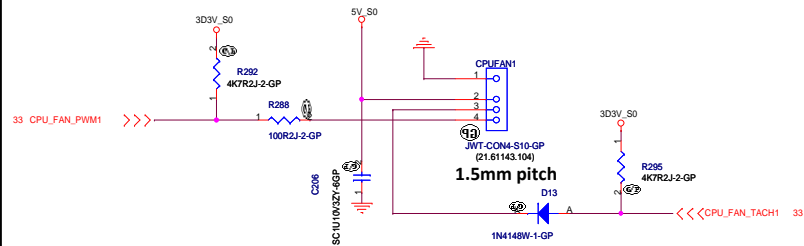
Catalina

Date: Tuesday, April 06, 2010

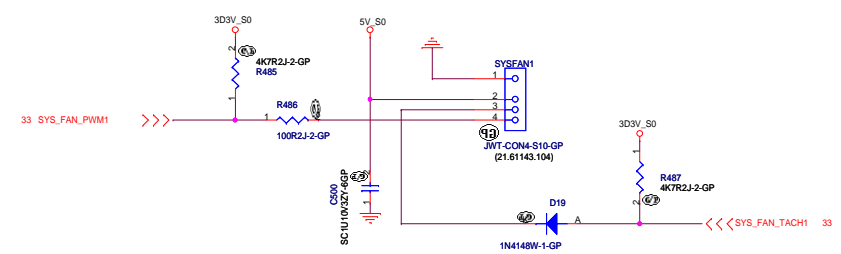
Sheet 32 of 59

Rev SA

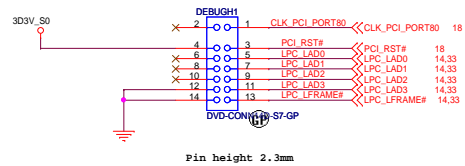
CPU FAN



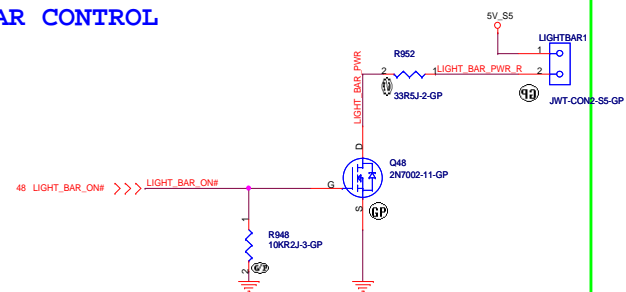
MXM_SYS FAN



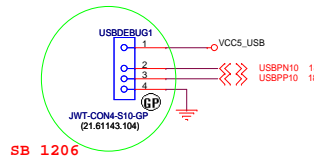
LPC DEBUG PORT



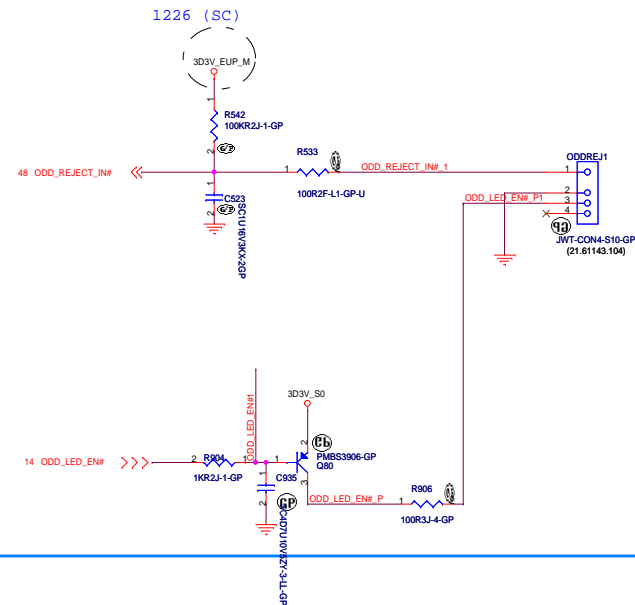
LIGHT BAR CONTROL



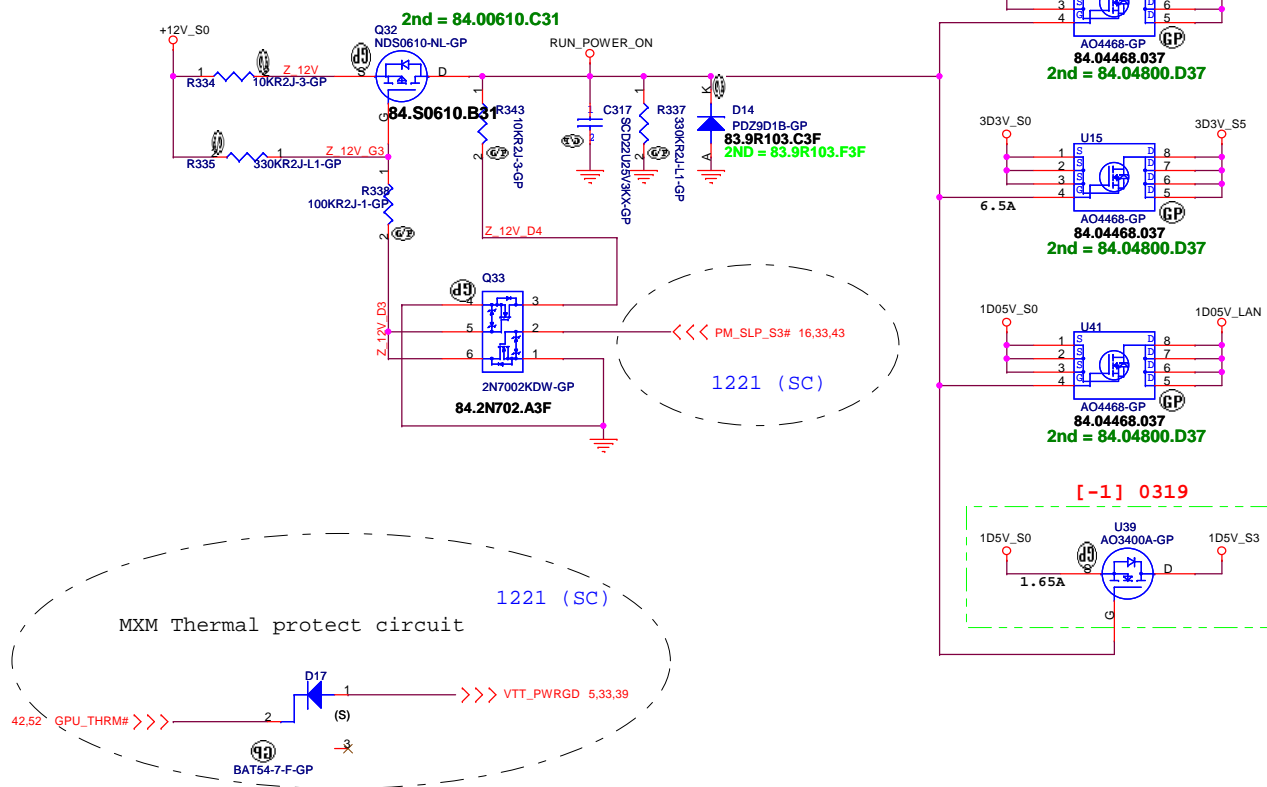
USB RESERVE



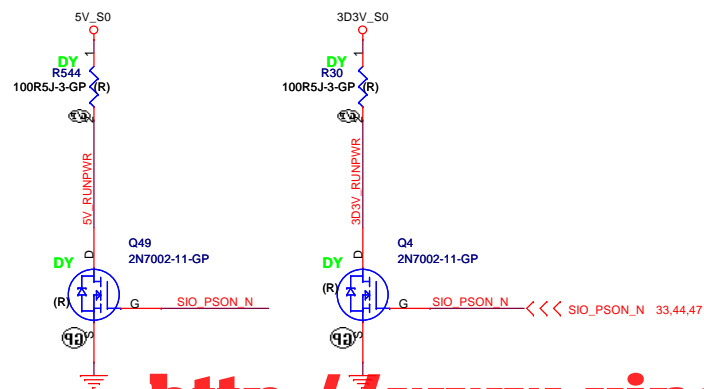
ODD REJECTION



Run Power



Reserved for Discharge



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Title

Run Power

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SA

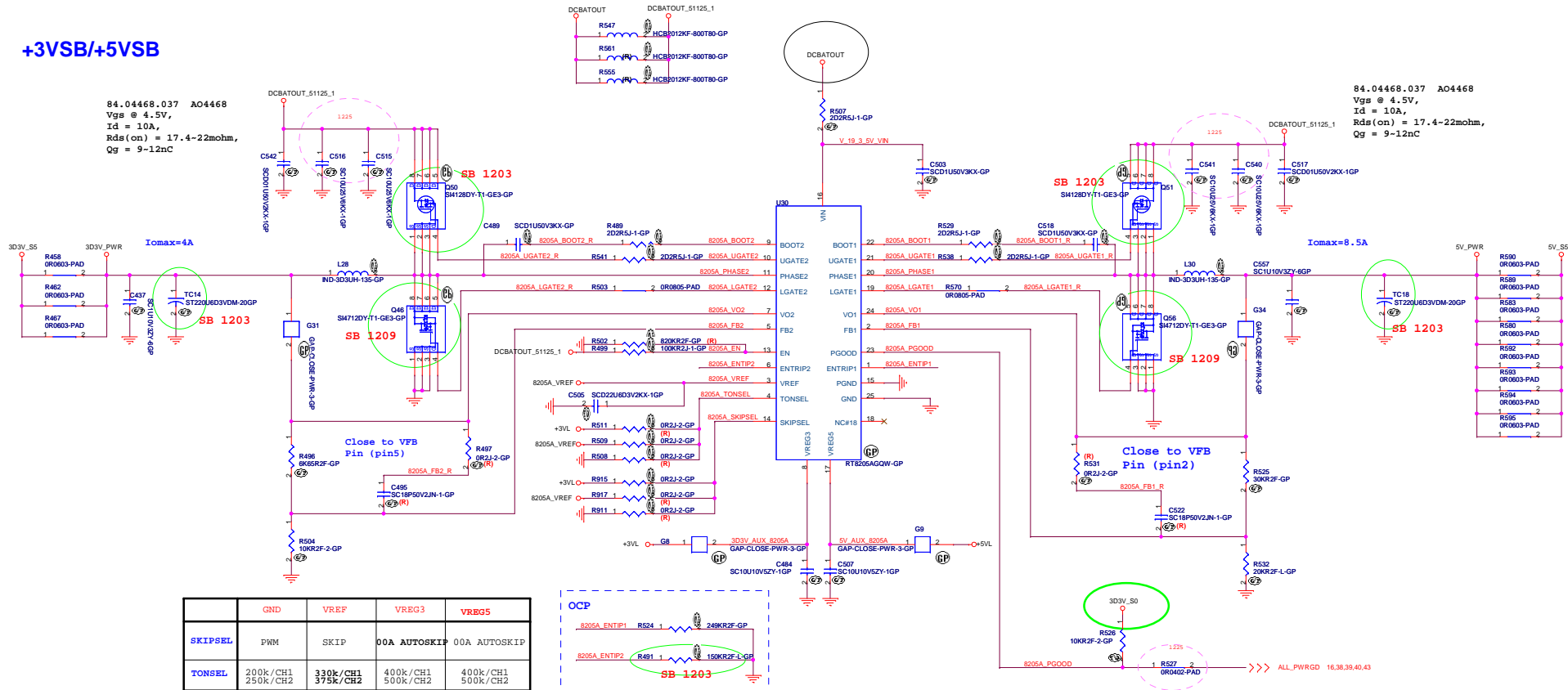
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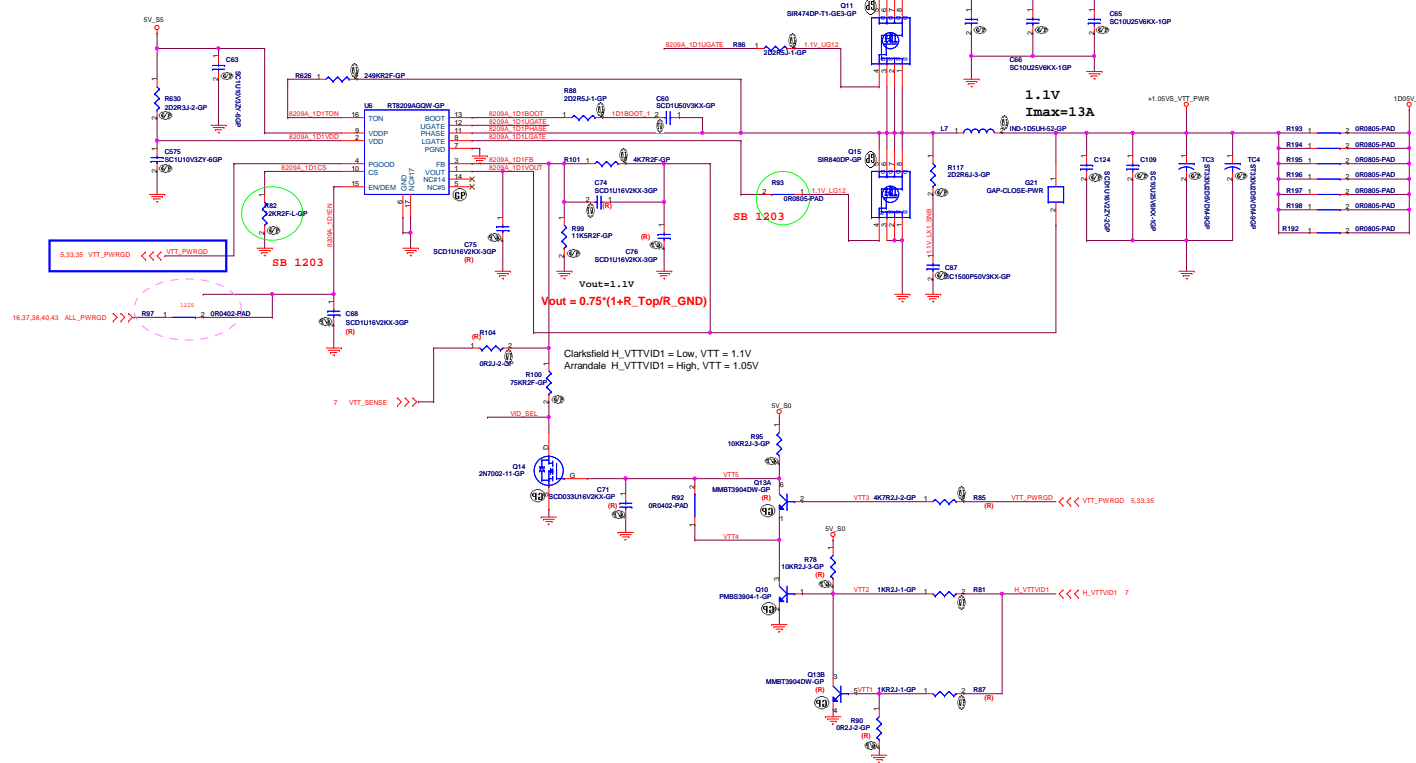
+3VSB/+5VSB

84.04468.037 AO4468
Vgs @ 4.5V,
Id = 10A,
Rds(on) = 17.4-22mohm,
Qg = 9-12nC

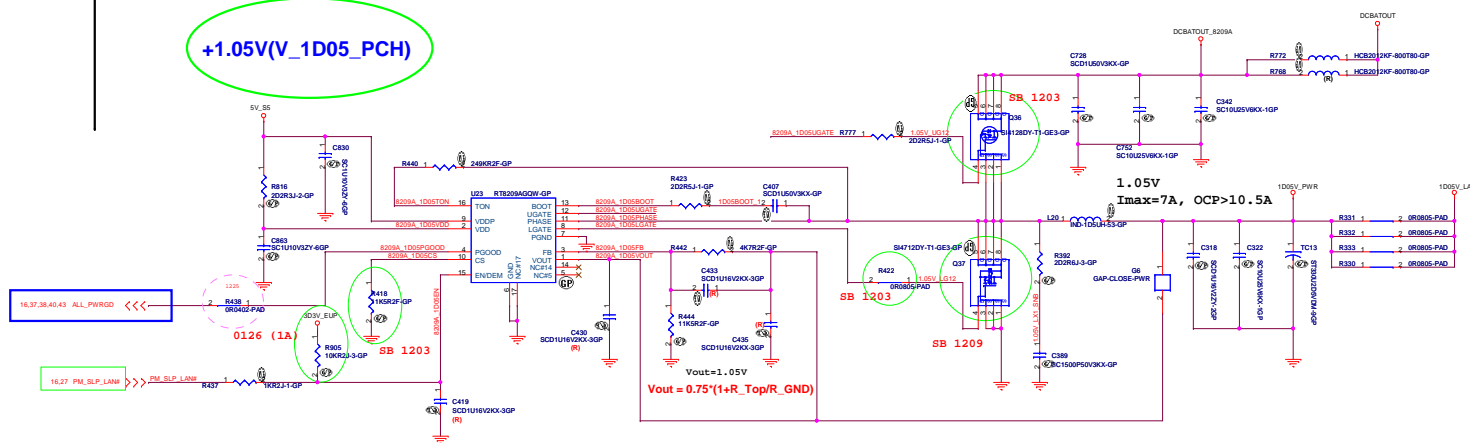
84.04468.037 AO4468
Vgs @ 4.5V,
Id = 10A,
Rds(on) = 17.4-22mohm,
Qg = 9-12nC

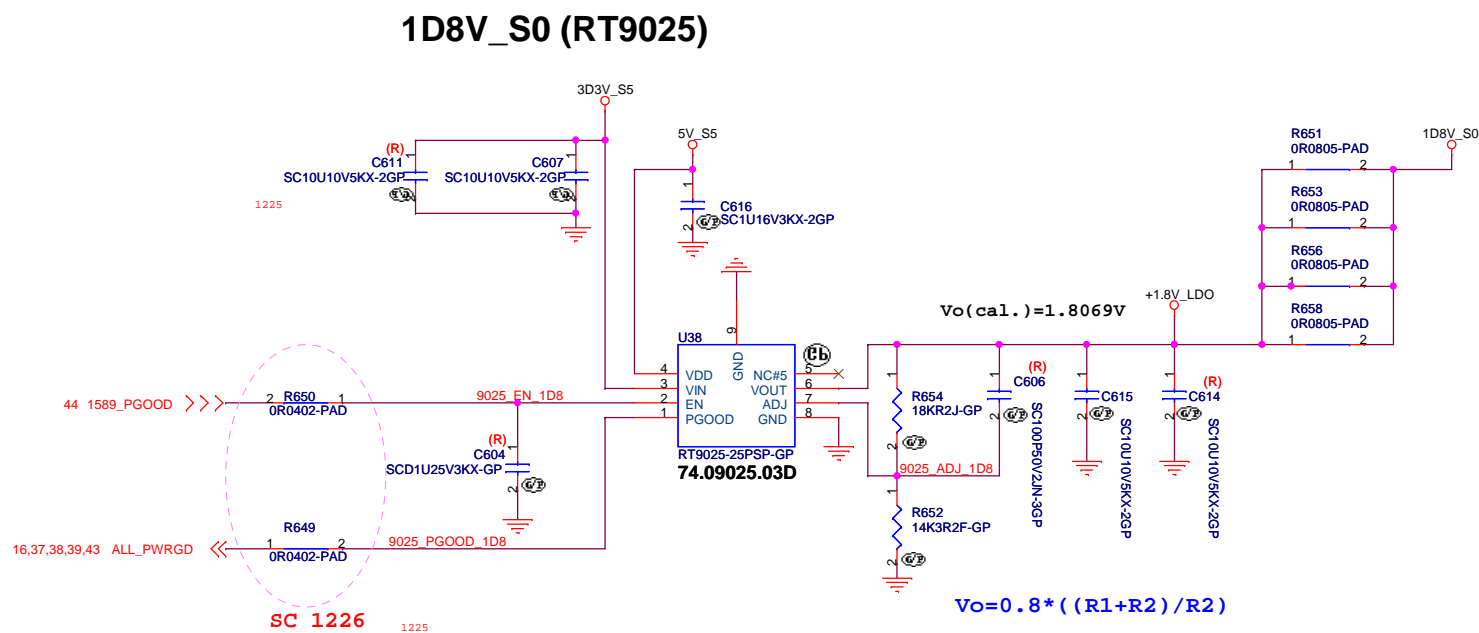


+1.05V(V_1D05_VTT)



+1.05V(V_1D05_PCH)

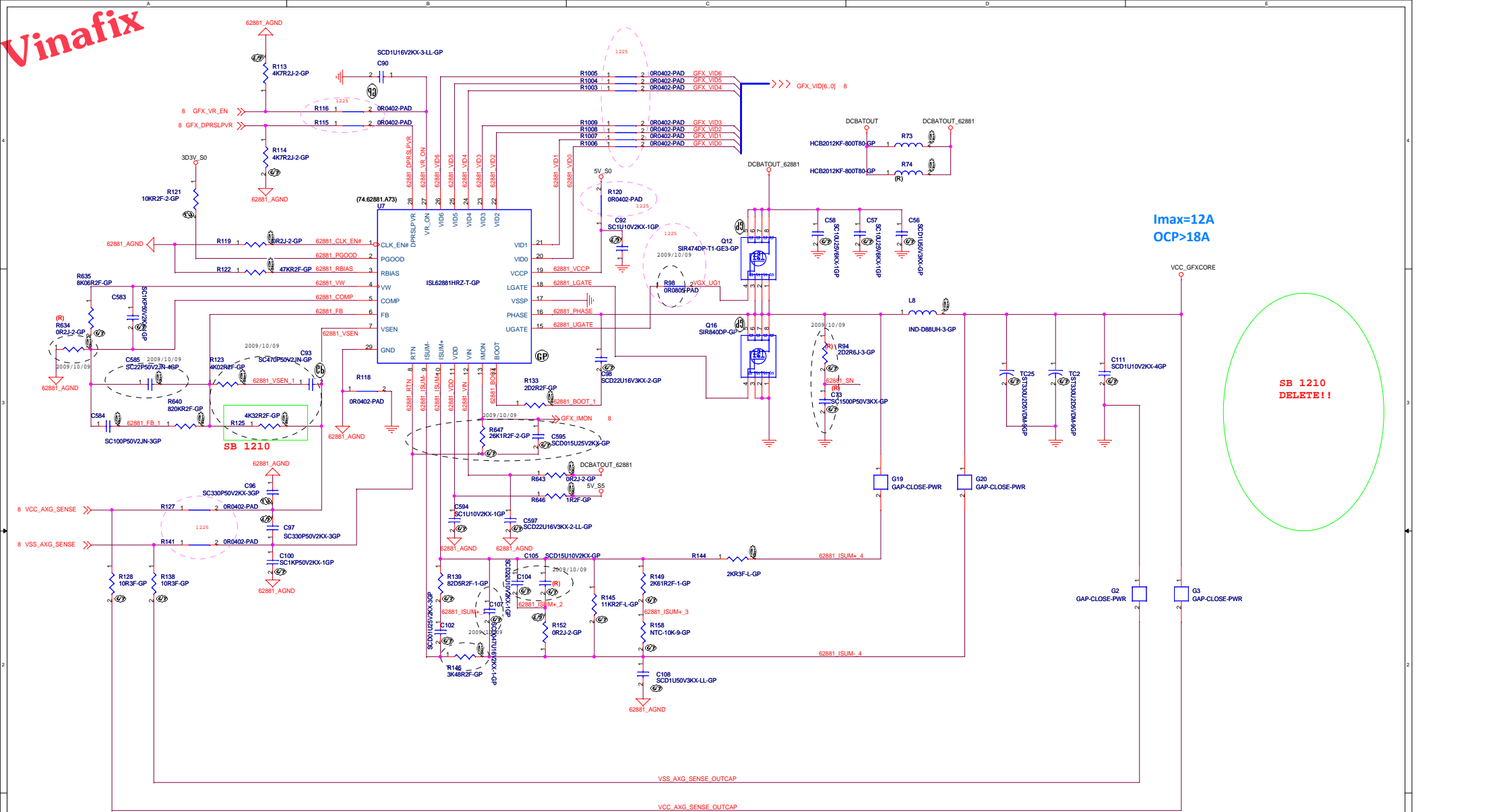




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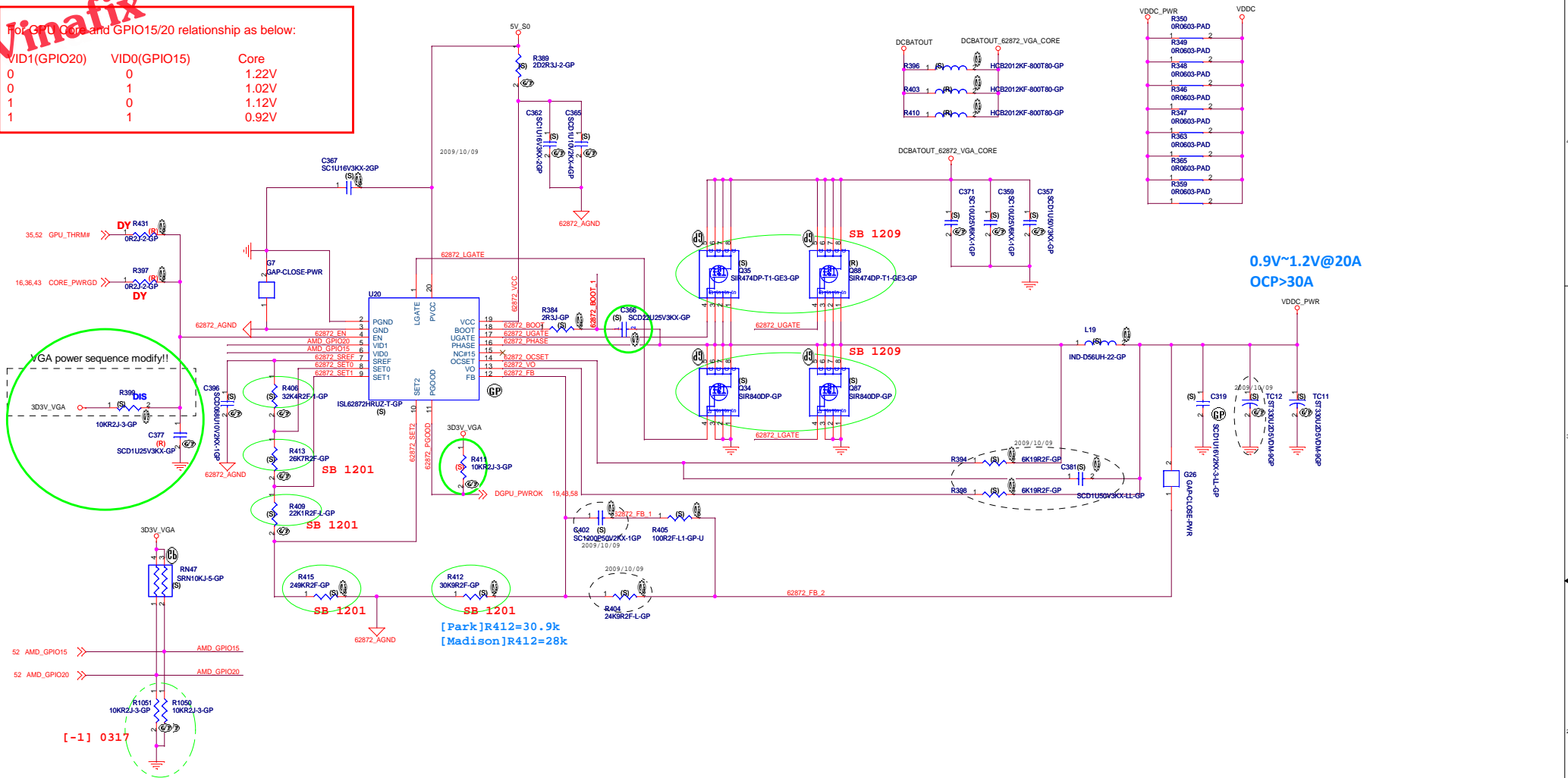
Title			
1D8V POWER			
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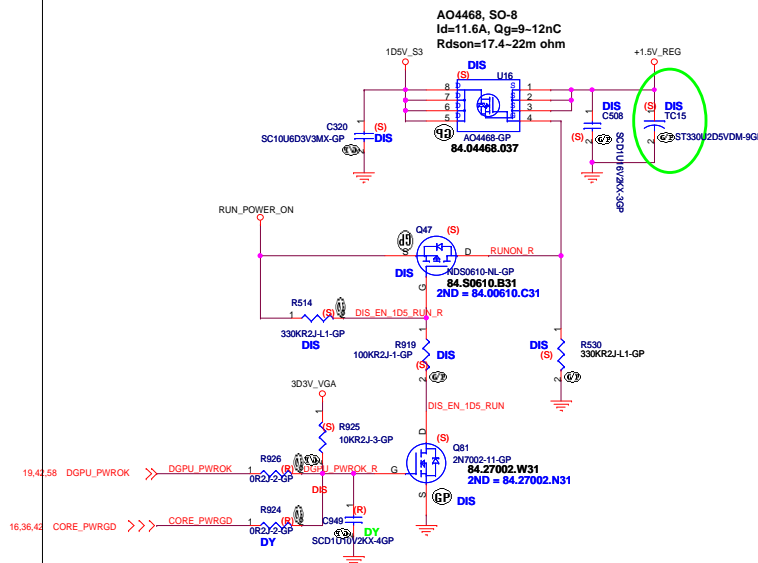
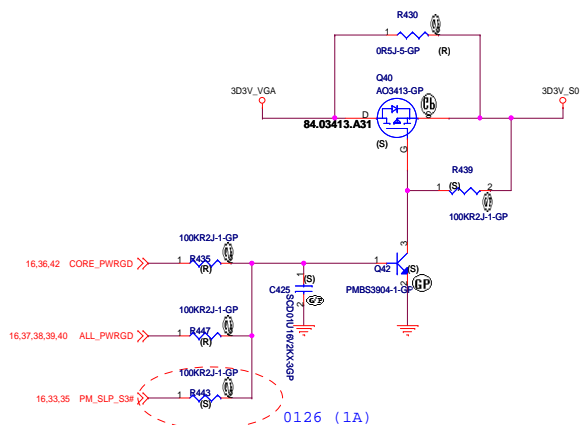
For GPU Core and GPIO15/20 relationship as below:

VID1(GPIO20)	VID0(GPIO15)	Core
0	0	1.22V
0	1	1.02V
1	0	1.12V
1	1	0.92V



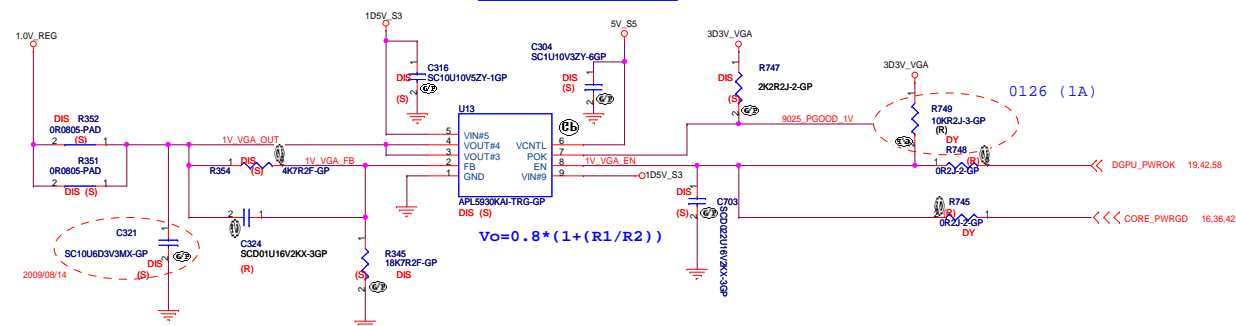
0.9V~1.2V@20A
OCP>30A

3D3V_S0 to 3D3V_DELAY Transfer



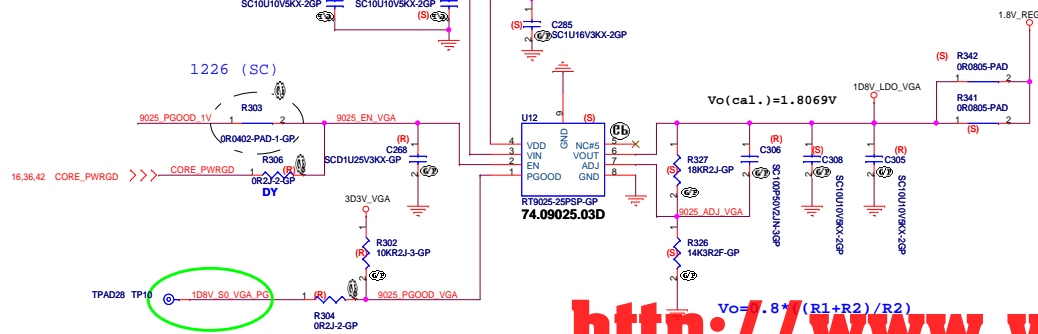
Iout=1.5A

Vout= 1V_VGA



1226 (SC)

1D8V_VGA
(RT9025)

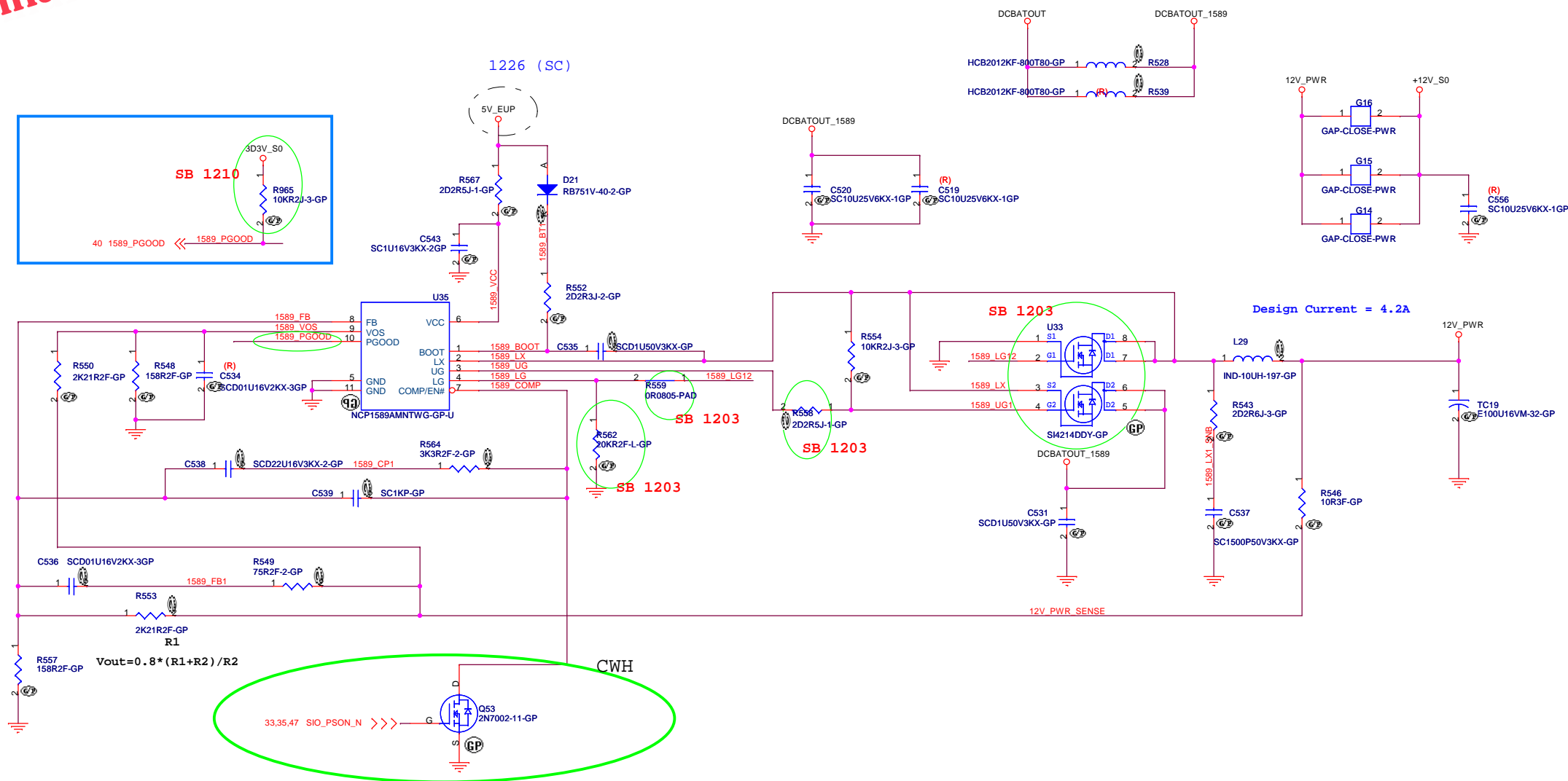


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Title																													

+12V

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Custom	

Document Number

Catalina

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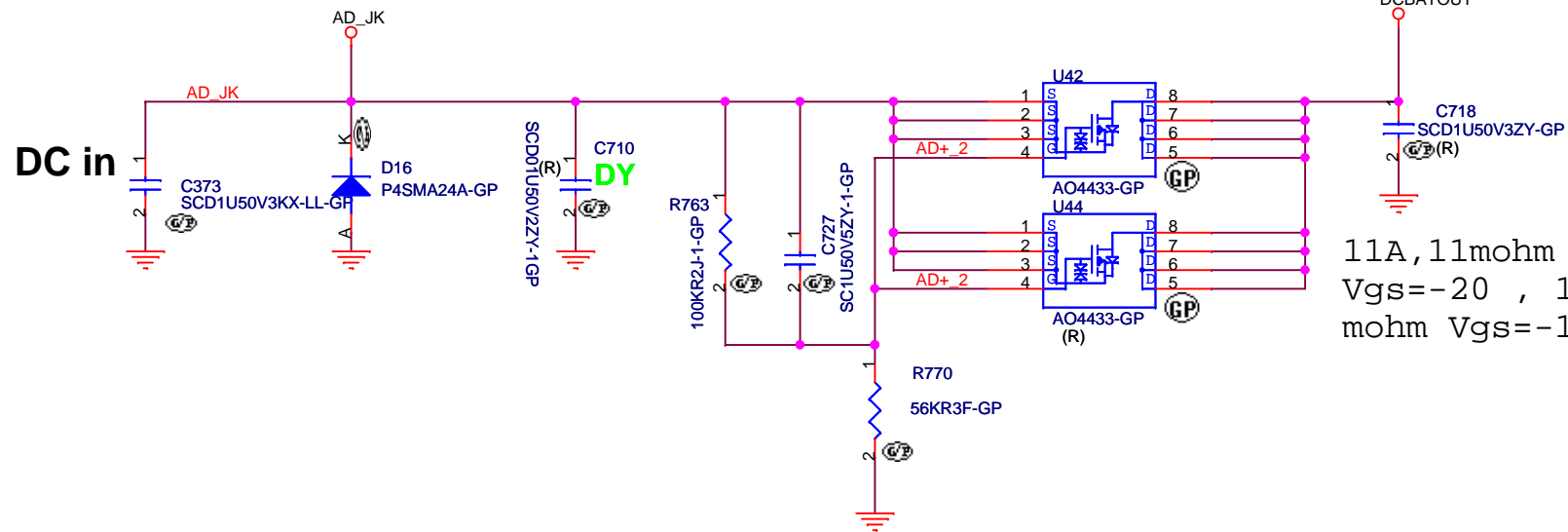
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Adaptor in to generate DCBATOUT

Add alternate 84.01403.A37



11A, 11mohm < 14mohm
 $V_{gs} = -20$, 14mohm < 18mohm
 $V_{gs} = -10$

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DC IN

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 A4

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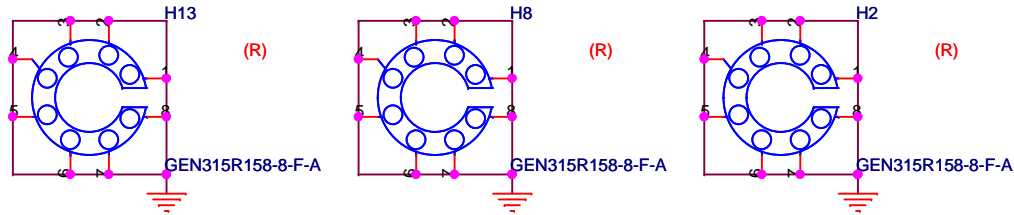
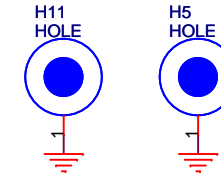
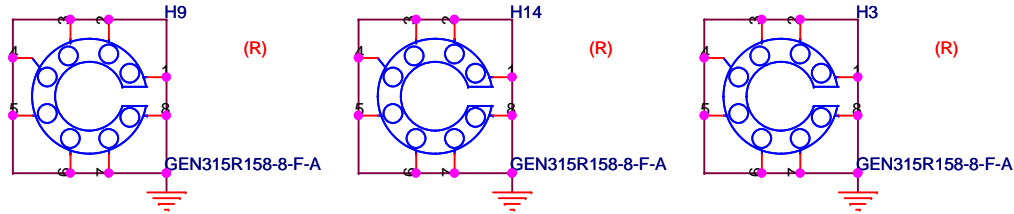
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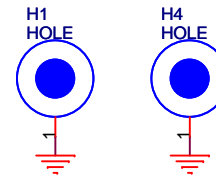
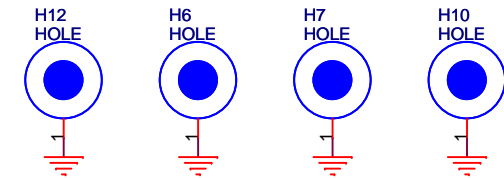
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Mini PCIE holder

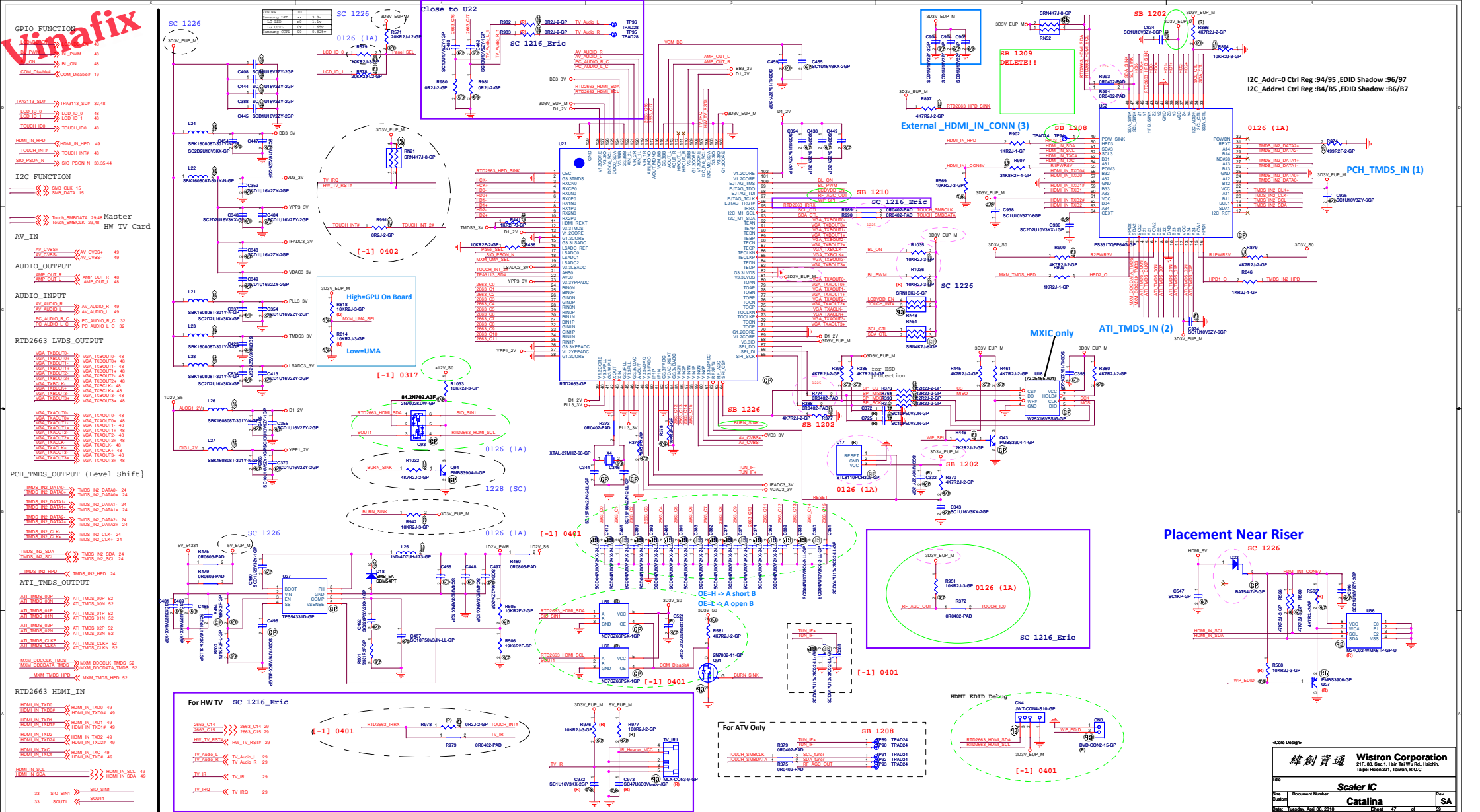


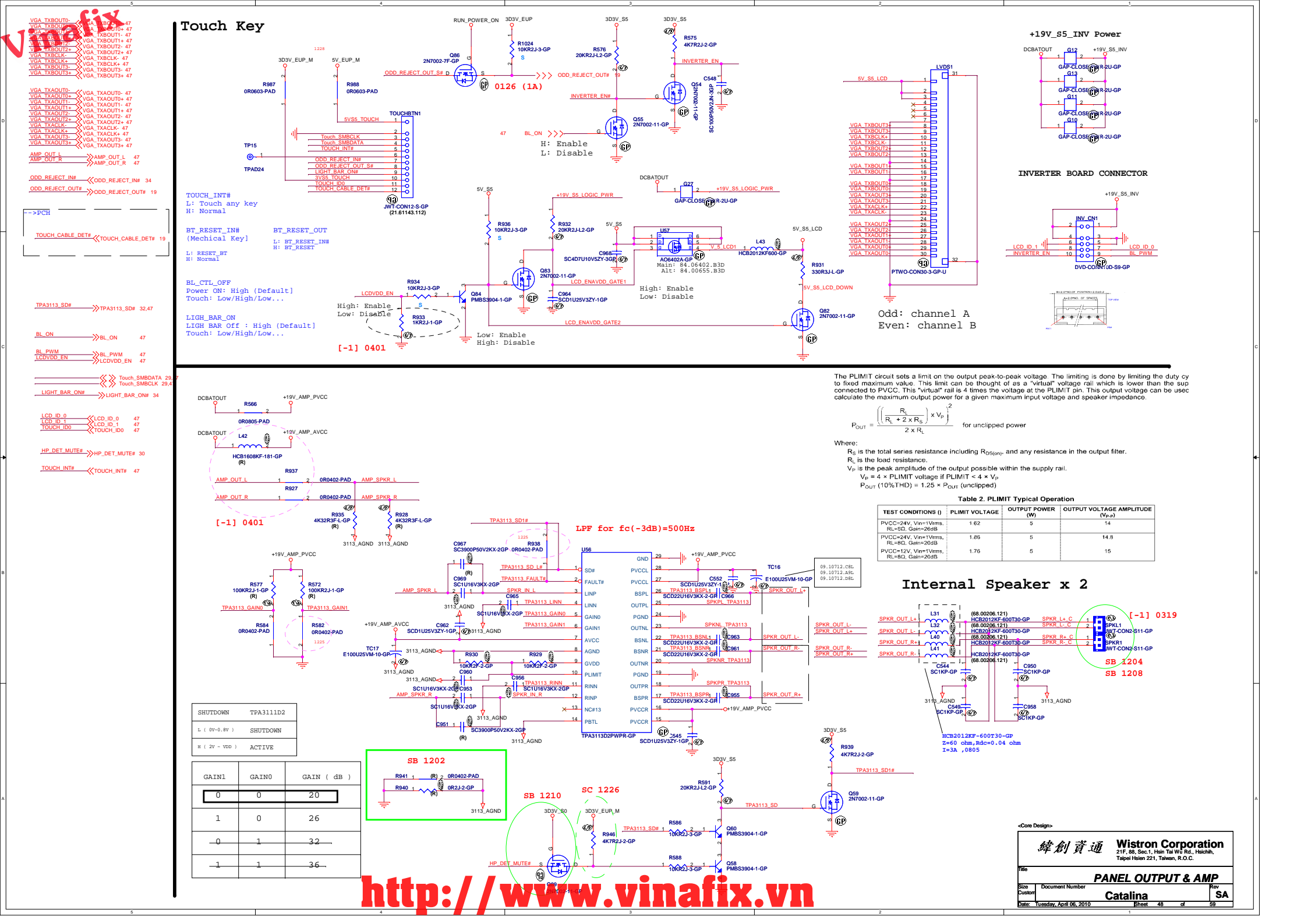
FAN holder



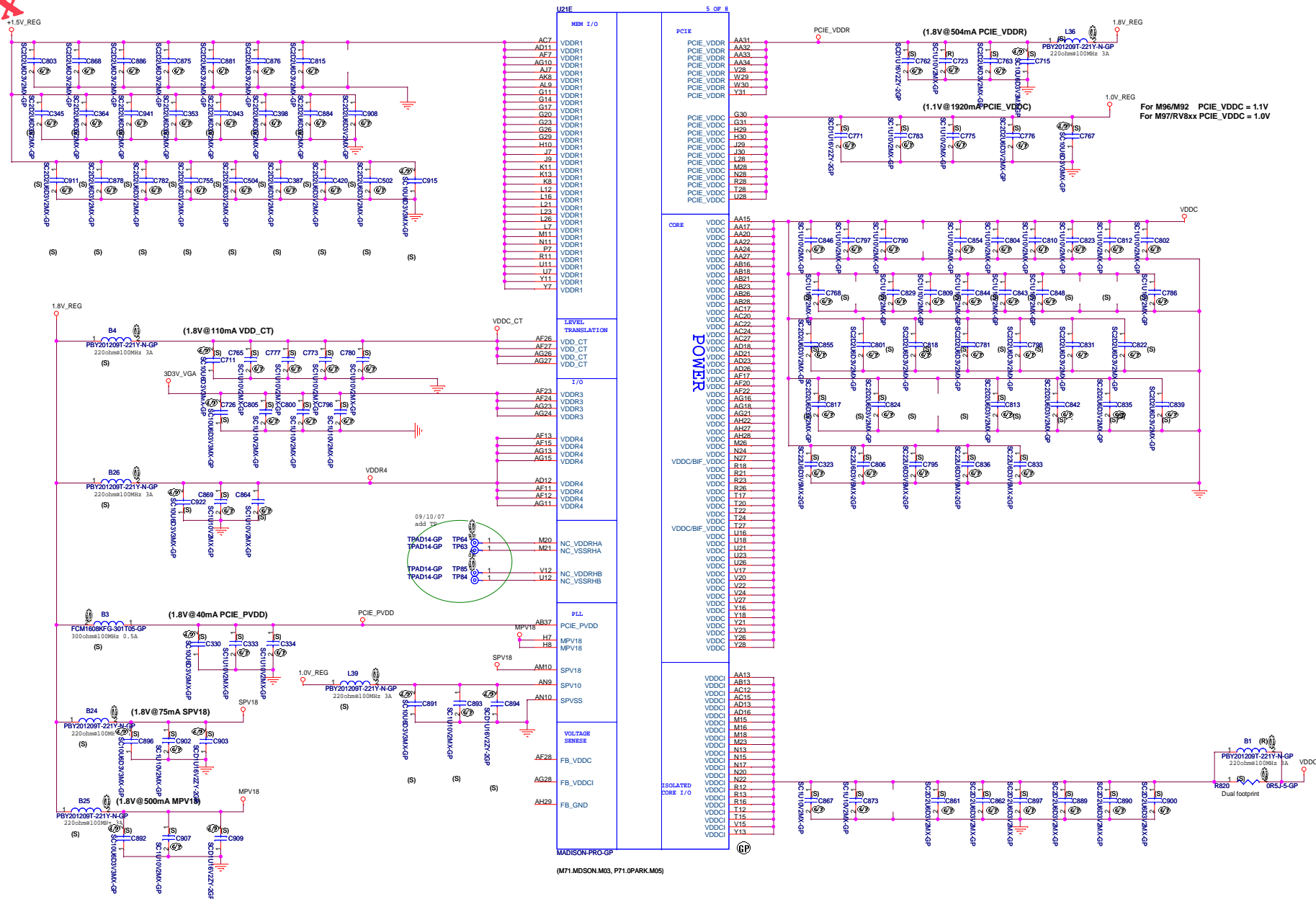
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Screw hole			
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POWER REGULATORS		
+3.3V 190 mA	VDDR3	60 mA
	A2VDD	130 mA
+0.95/+1V 33 A	VDDC	29 A
	VDDCI	4 A
+1.5V	VDDR1	TBD
	MVDDQ/C	
+1.8V 1.384 A	VDD_CT	17 mA
	DP[F:A]_PVDD	20 mA
	DP[D:A]_VDD18	130 mA
	DP[F:E]_VDD18	130 mA
	SPV18	50 mA
	MPV18	150 mA
	DPLL_PVDD	75 mA
	PCIE_PVDD	40 mA
	PCIE_VDDR	400 mA
	TSVDD	5 mA
	VDDR4	
	AVDD	TBD
	VDD1DI	70 mA
	VDD2DI	45 mA
	A2VDDQ	50 mA
		1.5 mA
+1.0V 1.42 A	DP[D:A]_VDD10	110 mA
	DP[F:E]_VDD10	110 mA
	SPV10	100 mA
	DPLL_VDDC	1.00 A
	PCIE_VDDC	1.1 A



**BACO
needed??**

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ATI_Mad_POWER

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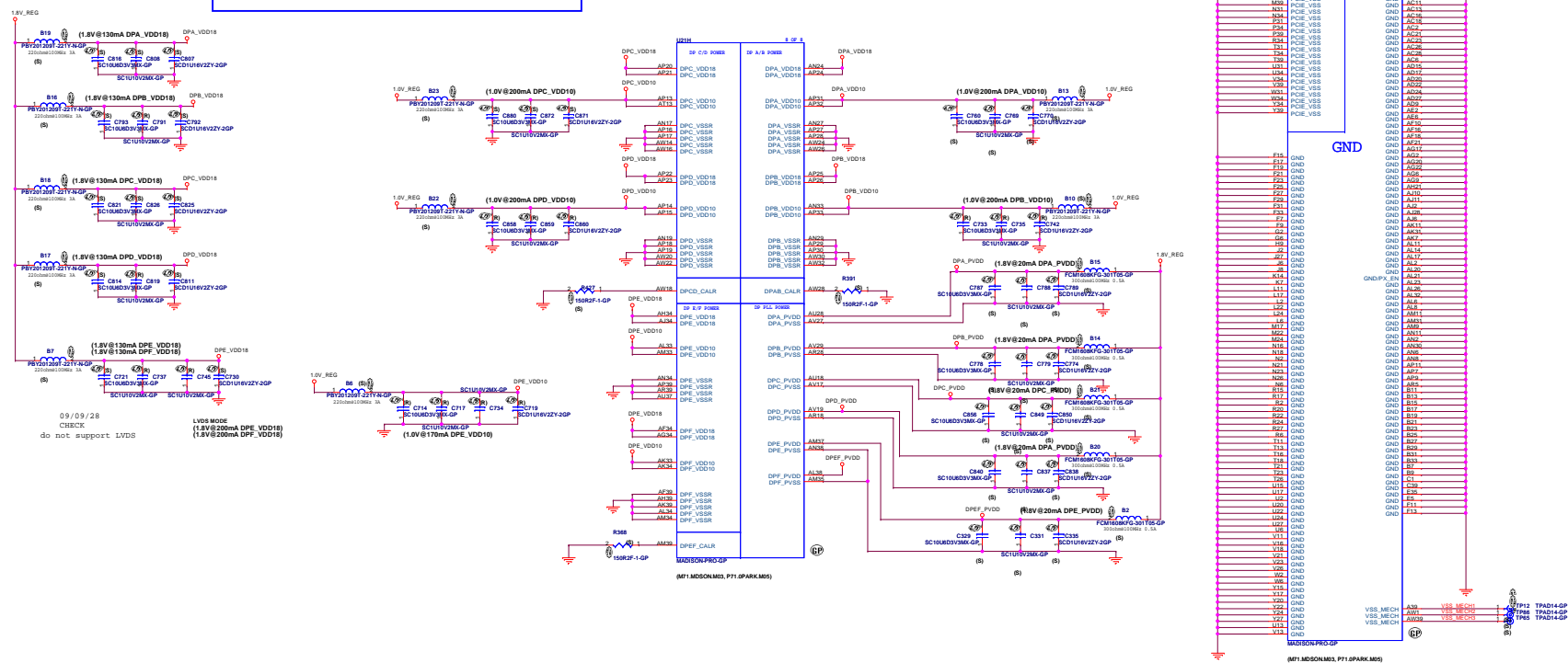
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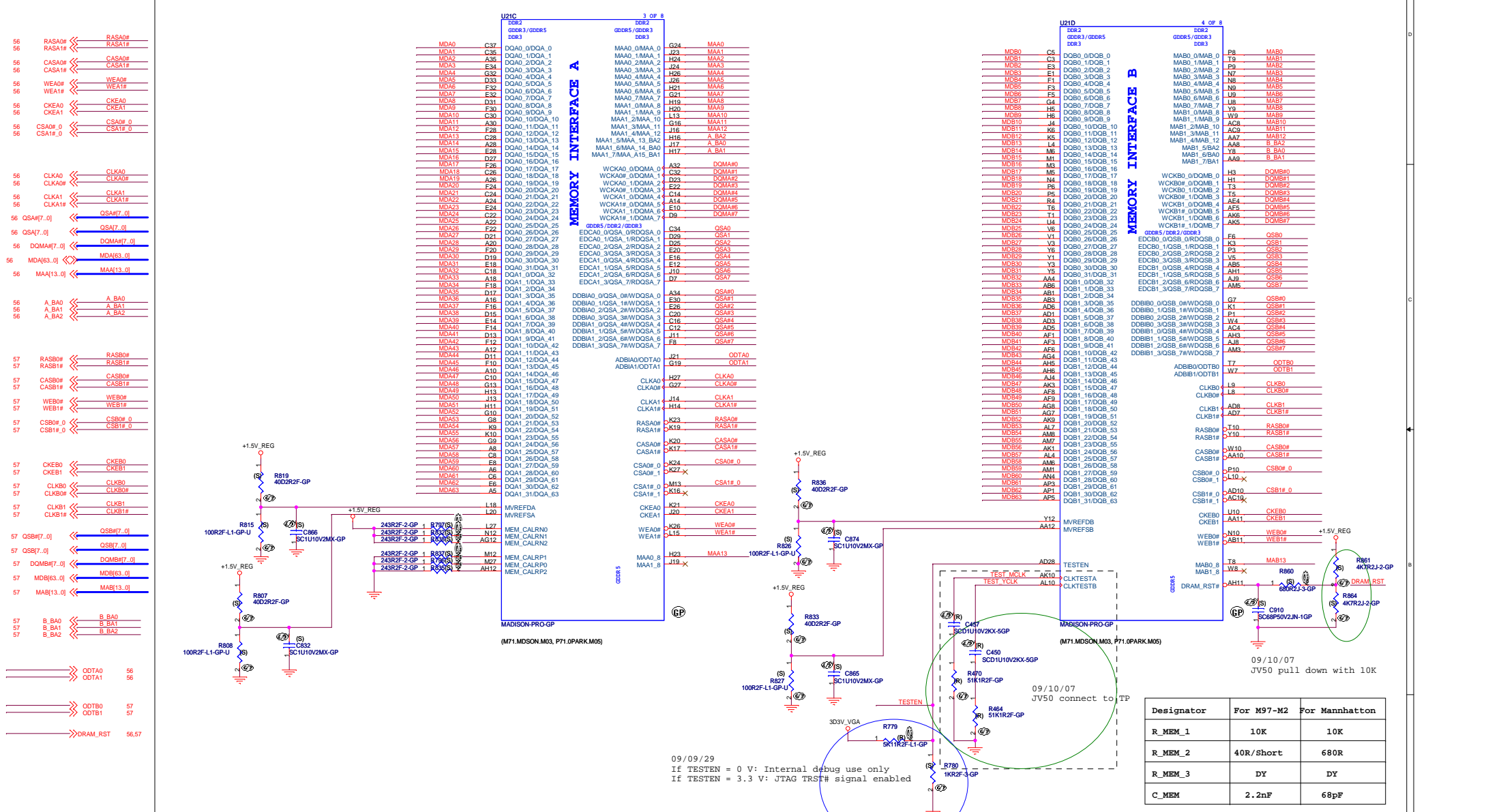
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09/09/28
For dual-link TMDS, the associated power supply rails can share the filters/decoupling capacitors.
We use single HDMI, share or ?
need check!



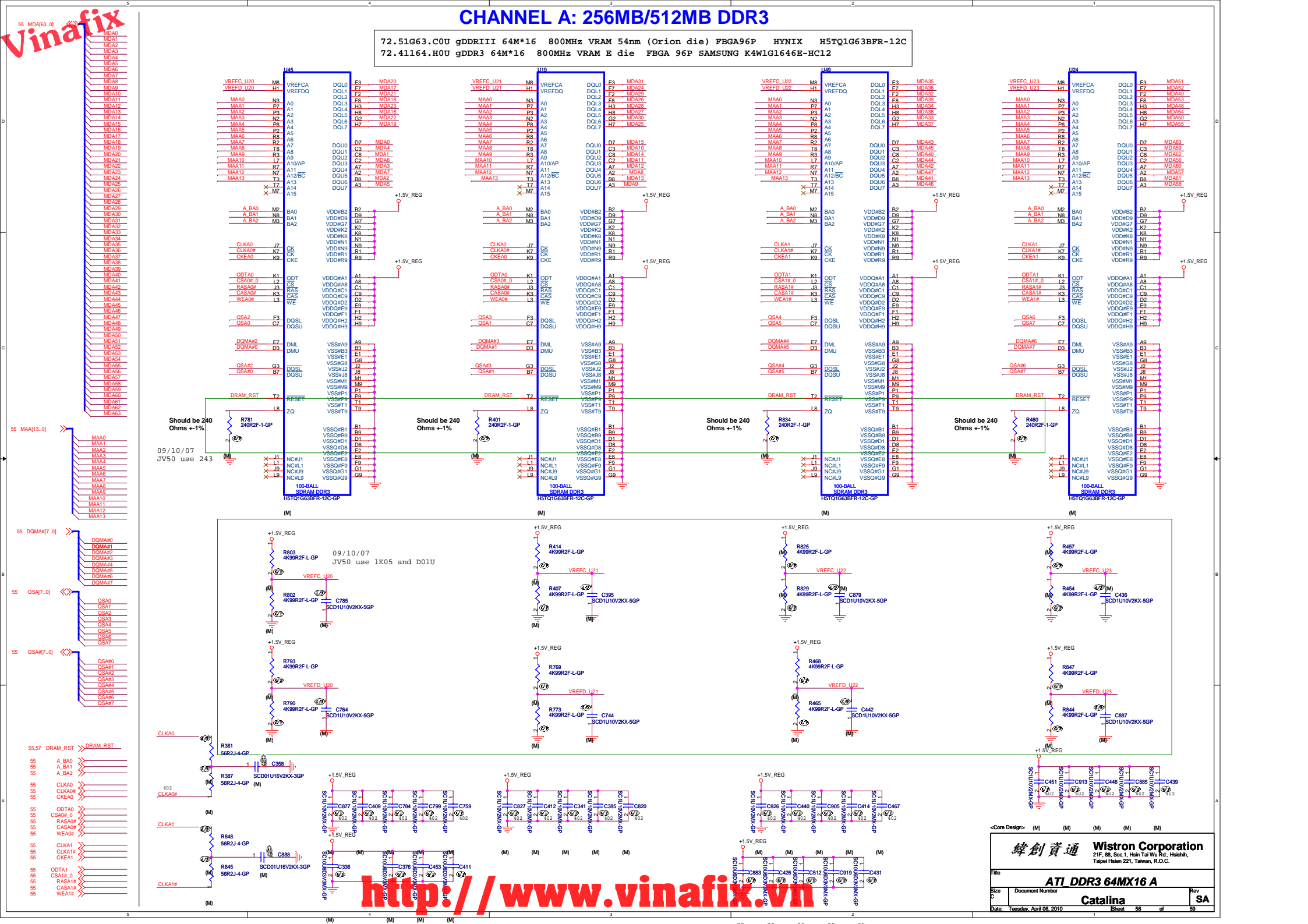


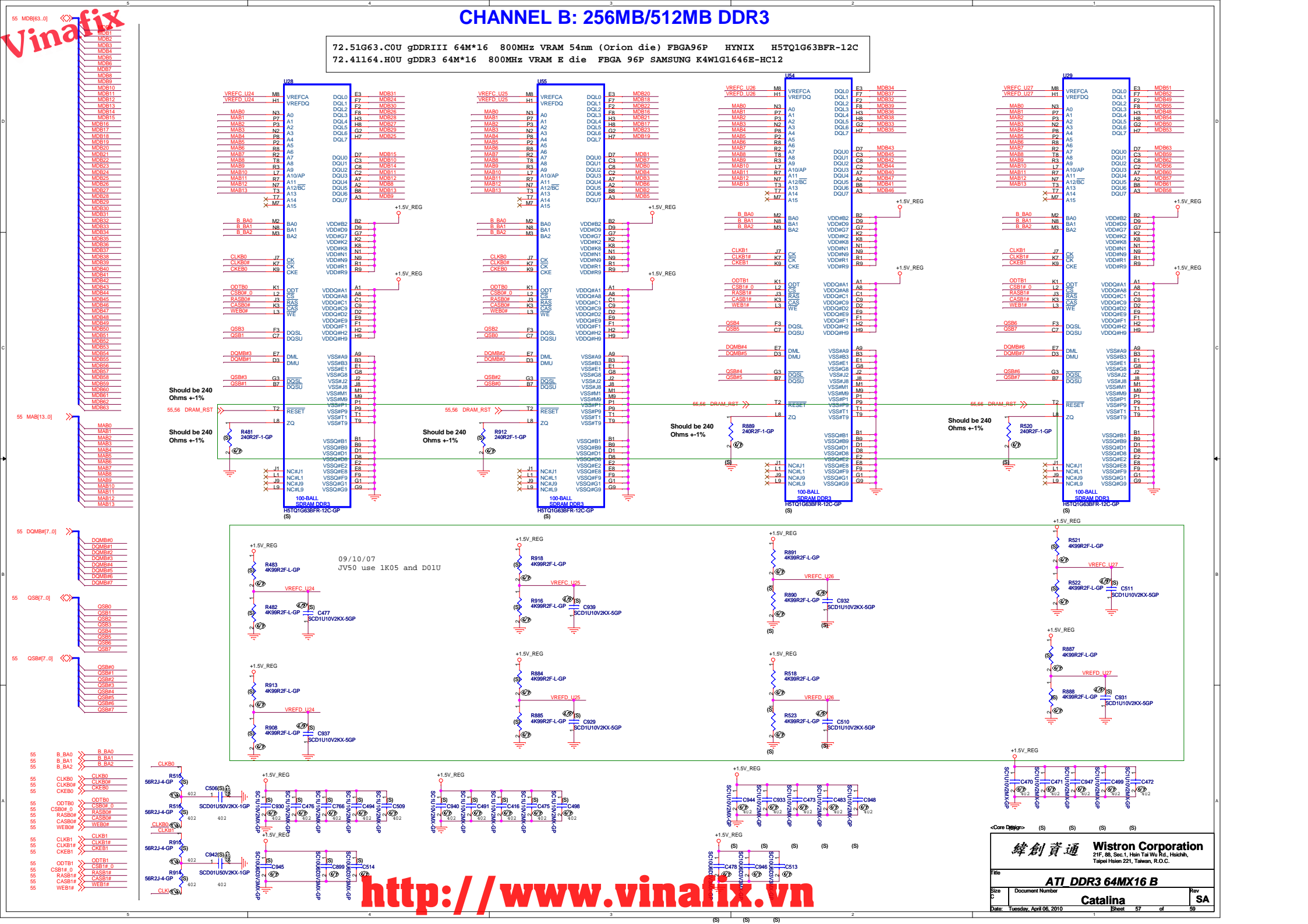
Designator	For M97-M2	For Mannheim
R_MEM_1	10K	10K
R_MEM_2	40R/Short	680R
R_MEM_3	DY	DY
C_MEM	2.2nF	68pF

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Reserve		
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