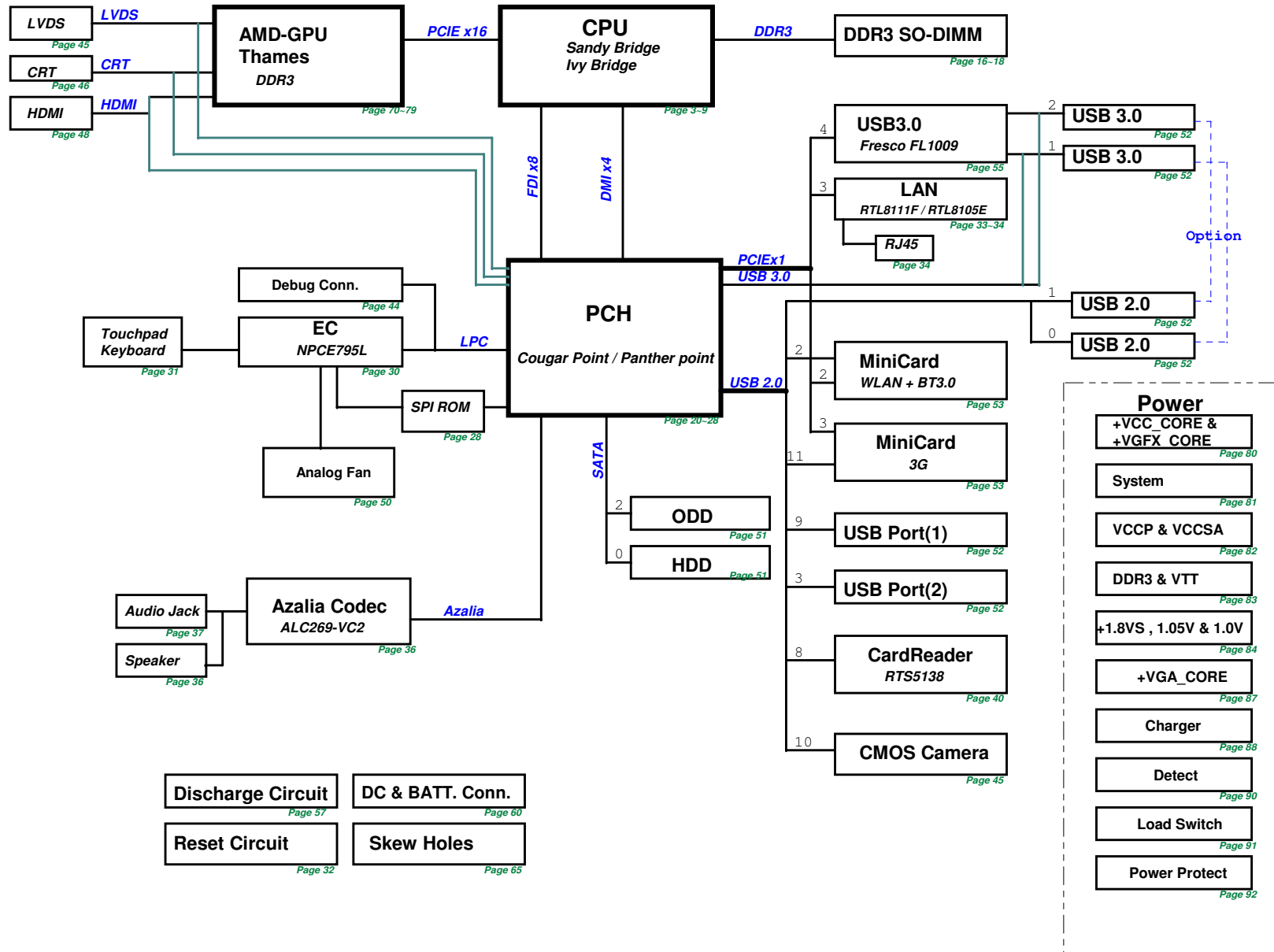


- 01. Block Diagram
- 02. System Setting
- 03. CPU(1)_DMI,DP,PEG,FDI
- 04. CPU(2)_CLK,MSIC,JTAG
- 05. CPU(3)_DDR3
- 06. CPU(4)_PROCSSOE POWER
- 07. CPU(5)_GRAPHICS POWER
- 08. CPU(6)_GND
- 09. CPU(7)_RESERVED
- 10. CPU_PCH_XDP*****
- 16. DDR3(1)_SO-DIMM0
- 17. DDR3(2)_SO-DIMM1
- 18. DDR3(3)_CA/DQ Voltage
- 20. PCH(1)_SATA,IHDA,RTC,LPC
- 21. PCH(2)_PCIE,CLK,SMB,PEG
- 22. PCH(3)_FDI,DMI,SYS PWR
- 23. PCH(4)_DP,LVDS,CRT
- 24. PCH(5)_PCI,NVRAM,USB
- 25. PCH(6)_CPU,GPIO,MISC
- 26. PCH(7)_POWER,GND
- 27. PCH(8)_POWER,GND
- 28. PCH(9)_SPI,SMB
- 30. EC_NPCE795(1)
- 31.KB/ TP
- 32. RST_Reset Circuit
- 33. LAN_RTL8105E/RTL8111F-Colay
- 34. LAN_RJ45
- 36. AUD_ALC269-VC2
- 37. AUDIO_HP/ MIC JACK
- 40. Card Reader RTS5138
- 44. BUG_Debug
- 45. LVDS CON
- 46. CRT CON
- 48. HDMI CON
- 50. FAN / Thermal Sensor
- 51. SATA HDD/ODD
- 52. USB JACK
- 53. MINICARD_WLAN+3G
- 55. USB3.0_FL1009(1)
- 56. LED
- 57. Discharge
- 60. DC_IN/Batt Connector
- 65. ME_CONN,Skew Hole
- 66. PWRBRD/IO BRD
- 70. AMD_GPU-M2--PCIE
- 71. AMD_GPU-M2-HDMI/DAC/LVDS
- 72. AMD_GPU-M2-(1)MEM_CTRL_CHA
- 73. AMD_GPU-M2-(2)MEM_CTRL_CHB
- 74. AMD_GPU-M2-STRAP_MISC
- 75. AMD_GPU-M2--(1)POWER/GND
- 76. AMD_GPU-M2--(2)DP POWER
- 77. AMD_GPU-M2--MEM_CHA
- 78. AMD_GPU-M2--MEM_CHB
- 79. AMD_GPU-M2--POWER FLOW
- 80_POWER_VCORE&VGFX
- 81_POWER_SYSTEM
- 82_POWER_VCCP & VCCSA
- 83_POWER_DDR & VTT
- 84_POWER_+1.8VS_1.05V_1.0V
- 87_POWER_+VGA_CORE
- 88_POWER_CHARGER
- 90_POWER_DETECT
- 91_POWER_LOAD SWITCH
- 92_POWER_PROTECT
- 93_POWER_SIGNAL
- 94_POWER_FLOWCHART
- 95_POWER_HISTORY
- 97.SYSTEM_HISTORY
- 98. Power On Sequence
- 99. Power On Timing

- A01 Power SW
- A02 ODD
- A03 TP
- A04 IO_USB
- A05 Card Reader RTS5138

Port Louis HR/CR platform Rev 2.0

BLOCK DIAGRAM



PCH_CPT
GPIO

| PCH_CPT GPIO | Use As | Signal Name | Internal & External Pull-up/down | Power |
|-----------------|-------------|------------------------|--|------------|
| GPIO 00 | | GPIO0 | EXT PU | +3VS |
| GPIO 01 | | USB30_EXT_SMI# | REV PU | +3VS |
| GPIO 02 | | MPC_PWR_CTRL# | EXT PU REV PD | +3VS |
| GPIO 03 | | SATA_ODD_DA# | EXT PU | +3VS |
| GPIO[4:5] | | EXTTS_SMI_DRV[0:1]_PCH | EXT PU | +3VS |
| GPIO 06 | | DGPU_HPD_INTR# | EXT PU | +3VS |
| GPIO 07 | ID USB3.0 | PCB_ID3 | EXT PD REV PU | +3VS |
| GPIO 08 | | GPIO8 | EXT PU | +3VSUS_ORG |
| GPIO 09 | | GPIO9 | EXT PU | +3VSUS_ORG |
| GPIO 10 | | GPIO10 | EXT PU | +3VSUS_ORG |
| GPIO 11 | | EXT_SCI# | EXT PU | +3VSUS_ORG |
| GPIO 12 | | GPIO12 | EXT PU | +3VSUS_ORG |
| GPIO 13 | | 3G_ON | EXT PU | +3VSUS_ORG |
| GPIO 14 | | GPIO14 | EXT PU | +3VSUS_ORG |
| GPIO 15 | | EXT_SMI# | EXT PU | +3VSUS_ORG |
| GPIO 16 | Clear FWD | GPIO16 | EXT PU | +3VS |
| GPIO 17 | | DGPU_PWROK | EXT PU REV PD | +3VS |
| GPIO 18 | | CLK_REQ1# | EXT PU | +3VS |
| GPIO 19 | | BBS_BIT0 | REV PD | |
| GPIO 20 | WLAN | CLK_REQ2# | EXT PU REV PD | +3VS |
| GPIO 21 | | SATA_DET#0_R | EXT PU | +3VS |
| GPIO 22 | | GPIO 22 | | |
| GPIO 23 | | GPIO23 | TEST POINT | |
| GPIO 24 | | GPIO24 | EXT PU | +3VSUS_ORG |
| GPIO 25 | 3G | CLK_REQ_3G# | EXT PU REV PD | +3VSUS_ORG |
| GPIO 26 | USB3.0 | CLK_REQ_USB30# | EXT PU REV PD | +3VSUS_ORG |
| GPIO 27 | | GPIO27 | PD | |
| GPIO 28 | | PLL_ODVR_EN | REV PD | |
| GPIO 29 | | GPIO29 | REV PU | +3VSUS_ORG |
| GPIO 30 | | ME_SUSPWRDNACK | EXT PU | +3VSUS_ORG |
| GPIO 31 | | ME_AC_PRESENT | EXT PU | +3VSUS_ORG |
| GPIO 32 | | PM_CLKRUN# | EXT PU | +3VS |
| GPIO 33 | | HDA_DOCK_EN# | TEST POINT | |
| GPIO 34 | SD HDMI SKU | PCB_ID2 | PD REV PU | +3VS |
| GPIO 35 | | CRT_IN# | EXT PU | +3VS |
| GPIO 36 | | SATA_ODD_PRSNT#_R | EXT PU | +3VS |
| GPIO 37 | | FDI_OVRVLTG | PD REV PU | +3VS |
| GPIO 38 | | PCB_ID0 | PD REV PU | +3VS |
| GPIO 39 | | PCB_ID1 | PD REV PU | +3VS |
| GPIO 40 | | GPIO40 | EXT PU | +3VSUS_ORG |
| GPIO 41 | | GPIO41 | EXT PU | +3VSUS_ORG |
| GPIO 42 | | GPIO42 | EXT PU | +3VSUS_ORG |
| GPIO 43 | | GPIO43 | EXT PU | +3VSUS_ORG |
| GPIO 44 | | CLK_REQ5# | EXT PU | +3VSUS_ORG |
| GPIO 45 | LAN | CLK_REQ_LAN# | EXT PU REV PD | +3VSUS_ORG |
| GPIO 46 | | CLK_REQ7# | EXT PU | +3VSUS_ORG |
| GPIO 47 | | CLKREQ_PEG# | EXT PU REV PD | +3VSUS_ORG |
| GPIO 48 | | BT_ON/OFF# | EXT PU | +3VS_WLAN |
| GPIO 49 | | PCB_ID5 | EXT PU | +3VS |
| GPIO 50 | | DGPU_HOLD_RST# | EXT PU | +3VS |
| GPIO 51 | | BBS_BIT1 | REV PD | |
| GPIO 52 | | DGPU_SELECT# | EXT PU | +3VS |
| GPIO 53 | | DGPU_PWM_SELECT# | REV PU | +3VS |
| GPIO 54 | | DGPU_PWR_EN | EXT PU | +3VS |
| GPIO 55 | | STP_A16OVR | REV PD | |
| GPIO 56 | | CLK_REQ_PEG_B# | EXT PU | +3VSUS_ORG |
| GPIO 57 | AOAC | WLAN_ON | | |
| GPIO 58 | | SML1_CLK | EXT PU | +3VSUS_ORG |
| GPIO 59 | | GPIO59 | EXT PU | +3VSUS_ORG |
| GPIO 60 | | DRAMRST_CNTRL_PCH | EXT PU | +3VSUS_ORG |
| GPIO 61 | | PM_SUS_STAT# | TEST POINT | |
| GPIO 62 | | SUSCLK | | |
| GPIO 63 | | SLP_S5# | TEST POINT | |
| GPIO 64 | | DGPU_EDID_SELECT# | REV PU | +3VS |
| GPIO 65 | | CLK_USB48_CR | | |
| GPIO 66 | | GPIO66 | TEST POINT | |
| GPIO 67 | | DGPU_PRSNT# | PD REV PU | +3VS |
| GPIO 68 | | SATA_ODD_PWRGT | PU | +3VS |
| GPIO 69 | | GPIO69 | PD | |
| GPIO[70:71] | | GPIO[70:71] | EXT PU | +3VS |
| GPIO 72 | | BATLOW# | EXT PU& TP | +3VSUS_ORG |
| GPIO 73 | | CLK_REQ0# | EXT PU | +3VSUS_ORG |
| GPIO 74 | | WLAN_LED | EXT PU& TP | +3VSUS_ORG |
| GPIO 75 | | SML1_DAT | EXT PU | +3VSUS_ORG |

EC
NPCE7951L

| EC GPIO | Use As | Signal Name |
|---------|--------|----------------------|
| GPIO00 | | SUSCLK |
| GPIO01 | | FAN0_TACH |
| GPIO02 | | ME_SUSPWRDNACK |
| GPIO03 | | PWR_SW_S# |
| GPIO04 | | BAT1_IN_OC# |
| GPIO05 | | AC_IN_OC |
| GPIO06 | | WLAN_WAKE# |
| GPIO07 | | CHGCB2# |
| GPIO10 | | SUSB_EC# |
| GPIO11 | | PM_CLKRUN# |
| GPIO13 | | PM_PWROK |
| GPIO14 | | USB_OC2#_EC |
| GPIO15 | | PWR_WHITE_LED# |
| GPIO16 | | DC_IN_LED# |
| GPIO17 | | SMB0_CLK |
| GPIO20 | | USB_OC01#_EC |
| GPIO21 | | PWR_AMBER_LED# |
| GPIO22 | | SMB0_DAT |
| GPIO23 | | PLT_ID0 |
| GPIO24 | | AOAC_PWREN |
| GPIO26 | | TP_CLK |
| GPIO27 | | TP_DAT |
| GPIO30 | | VSUS_ON |
| GPIO31 | | PCH_FLASH_DESCRIPTOR |
| GPIO32 | | LCD_BL_PWM |
| GPIO33 | | NC |
| GPIO34 | | ME_AC_PRESENT |
| GPIO35 | | HDMI_HPD_M |
| GPIO36 | | NUM_LED# |
| GPIO37 | | HDMI_ALERT# |
| GPIO40 | | NC |
| GPIO41 | | AOAC_RST# |
| GPIO42 | | PM_PWRBTN# |
| GPIO43 | | PM_RSMRST# |
| GPIO44 | | ALL_SYSTEM_PWRGD |
| GPIO45 | | BAT_ORG_LED# |
| GPIO46 | | NC |
| GPIO47 | | PM_SUSC# |
| GPIO50 | | LCD_BACKOFF# |
| GPIO51 | | CAP_LED# |
| GPIO52 | | THRO_CPU |
| GPIO53 | | SUS_PWRGD |
| GPIO54 | | EXT_SCI# |
| GPIO55 | | NC |
| GPIO56 | | PLT_ID1 |
| GPIO57 | | KS017 |
| GPIO60 | | KS016 |
| GPIO61 | | KS015 |
| GPIO62 | | KS014 |
| GPIO63 | | KS013 |
| GPIO64 | | KS012 |
| GPIO65 | | EXT_SMI# |
| GPIO66 | | NC |
| GPIO67 | | SUSC_EC# |
| GPIO70 | | OP_SD# |
| GPIO71 | | PM_SUSB# |
| GPIO72 | | LID_SW# |
| GPIO73 | | SMB1_CLK |
| GPIO74 | | SMB1_DAT |
| GPIO75 | | BAT_LEARN |
| GPIO76 | | CHGCB0# |
| GPIO77 | | NC |
| GPIO81 | | CPU_VRON |
| GPIO82 | | USBSLP_EN |
| GPIO83 | | CHGCB1# |
| GPIO84 | | USBP01_EN |
| GPIO85 | | A20GATE |
| GPIO86 | | RCIN# |
| GPIO87 | | RF_ON |
| GPIO90 | | AD_IINP |
| GPIO91 | | ADAPT_AD |
| GPIO92 | | NC |
| GPIO93 | | NC |
| GPIO94 | | BACK_EN_C |
| GPIO95 | | NC |
| GPIO96 | | CTL_FAN |
| GPIO97 | | VRM_PWRGD |

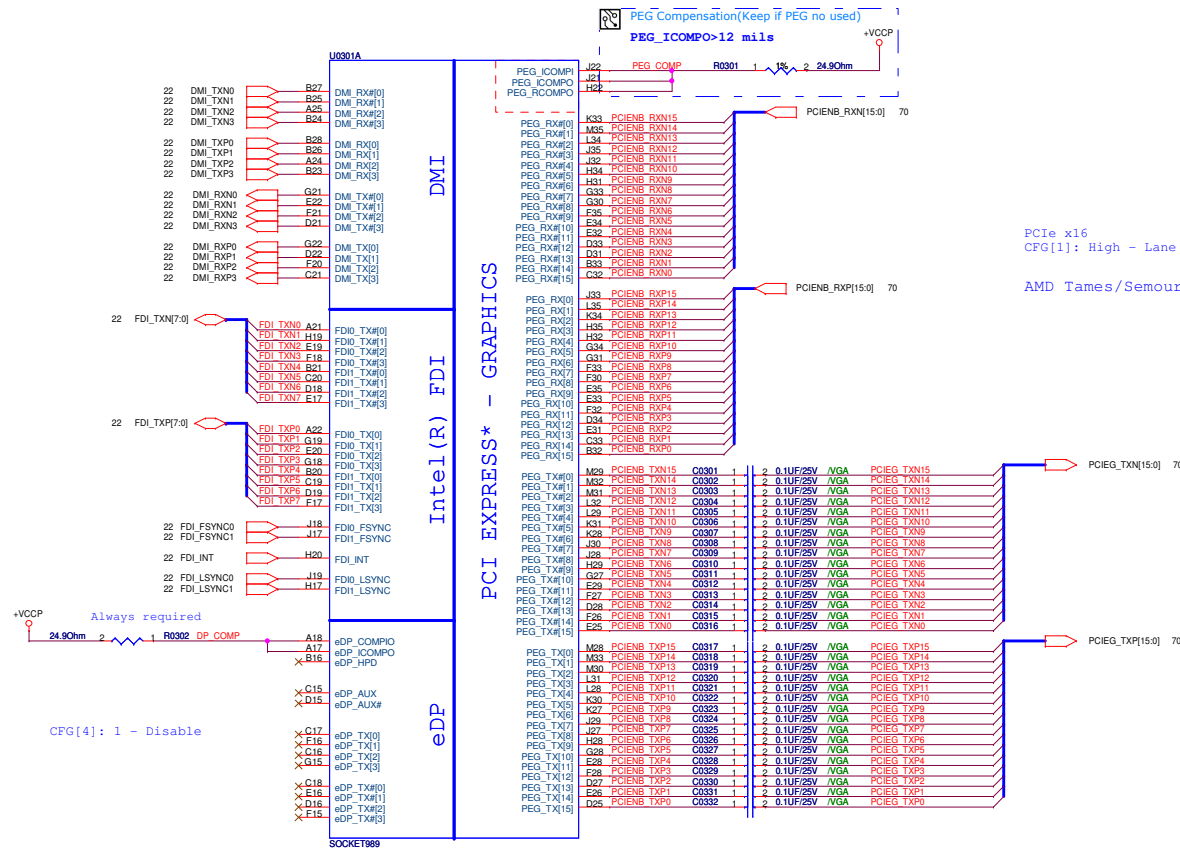
| EC Name | Use As | Signal Name |
|----------|--------|----------------|
| LAD0 | | LPC_AD0 |
| LAD1 | | LPC_AD1 |
| LAD2 | | LPC_AD2 |
| LAD3 | | LPC_AD3 |
| LCLK | | CLK_KBCPCI_PCH |
| LFRAME# | | LPC_FRAME# |
| LRESET# | | BUF_PLT_RST# |
| SERIRQ | | INT_SERIRQ |
| VCC_POR# | | EC_RST# |
| PECI | | H_PECI_EC |
| F5CK | | SPI_CLK_EC |
| F_SDIO | | SPI_SI_EC |
| F_SDI | | SPI_SO_EC |
| F_CS0# | | SPI_CS#1_EC |
| KSIO | | KSIO |
| KSII | | KSII |
| KSI2 | | KSI2 |
| KSI3 | | KSI3 |
| KSI4 | | KSI4 |
| KSI5 | | KSI5 |
| KSI6 | | KSI6 |
| KSI7 | | KSI7 |
| KS00 | | KS00 |
| KS01 | | KS01 |
| KS02 | | KS02 |
| KS03 | | KS03 |
| KS04 | | KS04 |
| KS05 | | KS05 |
| KS06 | | KS06 |
| KS07 | | KS07 |
| KS08 | | KS08 |
| KS09 | | KS09 |
| KS010 | | KS010 |
| KS011 | | KS011 |

SM_BUS ADDRESS :

| SM-Bus Device | SM-Bus Address |
|---------------|------------------|
| SO-DIMM 0 | 1010000x (A0h) |
| SO-DIMM 1 | 1010001x (A4h) |
| | |
| | |
| | |
| | |
| | |

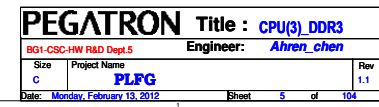
| | |
|--------|----------|
| PCIE 1 | N/A |
| PCIE 2 | WLAN |
| PCIE 3 | LAN |
| PCIE 4 | USB3.0 |
| PCIE 5 | N/A |
| PCIE 6 | N/A |
| PCIE 7 | N/A |
| PCIE 8 | N/A |
| SATA0 | SATA HDD |
| SATA1 | N/A |
| SATA2 | SATA ODD |
| SATA3 | N/A |
| SATA4 | N/A |
| SATA5 | N/A |

| | |
|--------|---------------------------|
| USB 0 | USB 3.0 Port(Right Front) |
| USB 1 | USB 3.0 Port (Right Back) |
| USB 2 | WiFi/BT |
| USB 3 | USB-17 Only |
| USB 4 | N/A |
| USB 5 | N/A |
| USB 6 | N/A |
| USB 7 | N/A |
| USB 8 | Card reader |
| USB 9 | USB |
| USB 10 | Camera |
| USB 11 | 3G Card |
| USB 12 | N/A |
| USB 13 | N/A |



```
PCIe x16
CFG[1]: High - Lane Reversal
```

AMD Tames/Semour support to GEN2



45W
MAX:94A
TDC:54.6A

POWER

MAX:8.5A
TDC:8.5A

Decoupling guide from Intel (POWER + EE)
+VCORE 22uF * 16pcs
10uF * 10pcs
470uF * 4pcs
Decoupling guide for Everest (EE)
+VCORE 22uF * 16pcs (8 nostuff)
10uF * 10pcs (3 nostuff)

VCORE
VOLTERRA REQUIRE:22UF*26PCS+ 6PCS
for power noise issue
EE:22UF*24PCS(3PCS no stuff)
PWR:22UF*8PCS(3PCS no stuff)

Decoupling guide from Intel (POWER + EE)
+VCCP 22uF * 19pcs (7 nostuff)
330uF * 3pcs
Decoupling guide for Everest (EE)
+VCCP 22uF * 19pcs (7 no stuff)

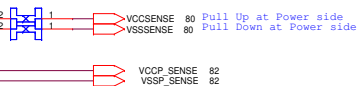
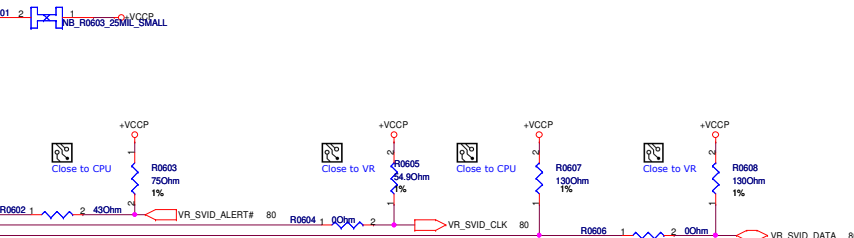
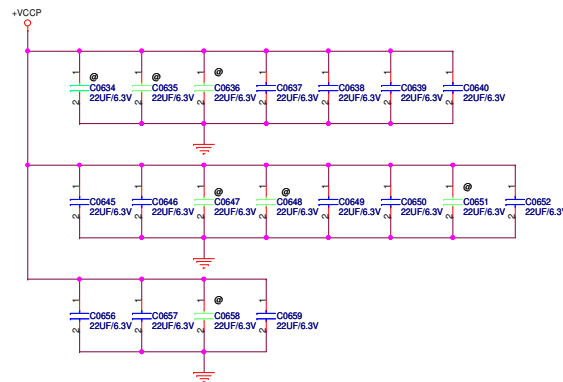
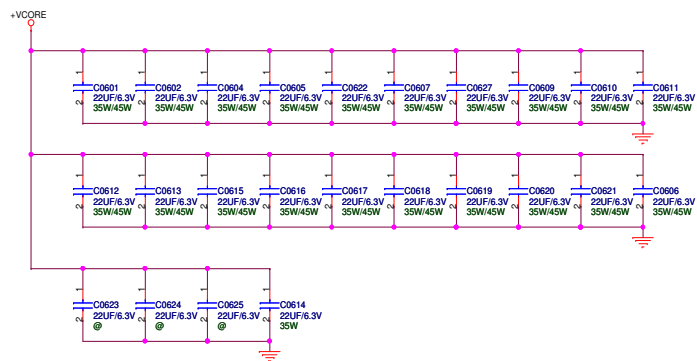
+VCCP 3.4,7,26,27,30,32,82
+VCORE 80

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES



| | | | |
|------------|--|------------|----------------------|
| +VCCP | | +VCCP | 3,4,6,26,27,30,32,82 |
| +1.5V | | +1.5V | 5,57,83 |
| +VCCSA | | +VCCSA | 82 |
| +1.8VS | | +1.8VS | 25,26,80,84 |
| +VGFX_CORE | | +VGFX_CORE | 80 |
| +V_SM_VREF | | +V_SM_VREF | 18 |

Decoupling guide from Intel (POWER + EE)
+VGFX_CORE 22uF * 12pcs
470uF * 2pcs

Decoupling guide for Everest (EE)
+VGFX_CORE 22uF * 12pcs (2 nostuff)

VGFX_CORE
VOLTERRA REQUIRE:22UF*23PCS
EE:22UF*19PCS
PWR:22UF*4PCS

SV-QC ICCMAX_VAXG 46A ICCTDC_VAXG 35A
SV-DC ICCMAX_VAXG 33A ICCTDC_VAXG 21.5A

Graphics core voltage
Voltage range: 0 - 1.52V

POWER

SENSE LINES

VREF

DDR3 - 1.5V RAILS

SA RAIL

MISC

1.8V RAIL

Close to CPU

Close to CPU

Close to CPU

Close to CPU

Close to CPU

Close to CPU

Close to CPU

VAXG1
VAXG2
VAXG3
VAXG4
VAXG5
VAXG6
VAXG7
VAXG8
VAXG9
VAXG10
VAXG11
VAXG12
VAXG13
VAXG14
VAXG15
VAXG16
VAXG17
VAXG18
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VAXG49
VAXG50
VAXG51
VAXG52
VAXG53
VAXG54

SM_VREF

VDDQ1
VDDQ2
VDDQ3
VDDQ4
VDDQ5
VDDQ6
VDDQ7
VDDQ8
VDDQ9
VDDQ10
VDDQ11
VDDQ12
VDDQ13
VDDQ14
VDDQ15

VCCSA1
VCCSA2
VCCSA3
VCCSA4
VCCSA5
VCCSA6
VCCSA7
VCCSA8

VCCP
VCCP1
VCCP2
VCCP3

VCCSA_SEN0
VCCSA_SEN1

VCCSA_SEN0
VCCSA_SEN1

VCCSA_SEN0
VCCSA_SEN1

VCCSA_SEN0
VCCSA_SEN1

VCCSA_SEN0
VCCSA_SEN1

VCCSA_SEN0
VCCSA_SEN1

VCCSA_SEN0
VCCSA_SEN1

VCCSA_SEN0
VCCSA_SEN1

VCCGT_SENSE 80
VSSGT_SENSE 80

+V_SM_VREF 10mV
+V_SM_VREF CNT

MAX:1.0A
+1.5V_VCCDDQ

MAX:6A
TDC:6A

VCCSA_SEN0
VCCSA_SEN1

VCCSA_SEN0
VCCSA_SEN1

VCCSA_SEN0
VCCSA_SEN1

VCCSA_SEN0
VCCSA_SEN1

VCCSA_SEN0
VCCSA_SEN1

VCCSA_SEN0
VCCSA_SEN1

VCCSA_SEN0
VCCSA_SEN1

VCCSA_SEN0
VCCSA_SEN1

VCCSA_SEN0
VCCSA_SEN1

PS_S3CNTRL 1.5V 22

PS_S3CNTRL 1.5V R

PS_S3CNTRL 1.5V R

PS_S3CNTRL 1.5V R

PS_S3CNTRL 1.5V R

PS_S3CNTRL 1.5V R

PS_S3CNTRL 1.5V R

PS_S3CNTRL 1.5V R

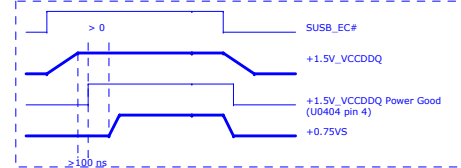
PS_S3CNTRL 1.5V R

PS_S3CNTRL 1.5V R

PS_S3CNTRL 1.5V R

PS_S3CNTRL 1.5V R

PS_S3CNTRL 1.5V R



CFG strapping information:

CFG[2]: PCIE Static Numbering Lane Reversal- CFG[2] is for the 16x

- 1: Normal Operation, Lane # definition matches socket pin map definition
- 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG[4]: Embedded DisplayPort Detection

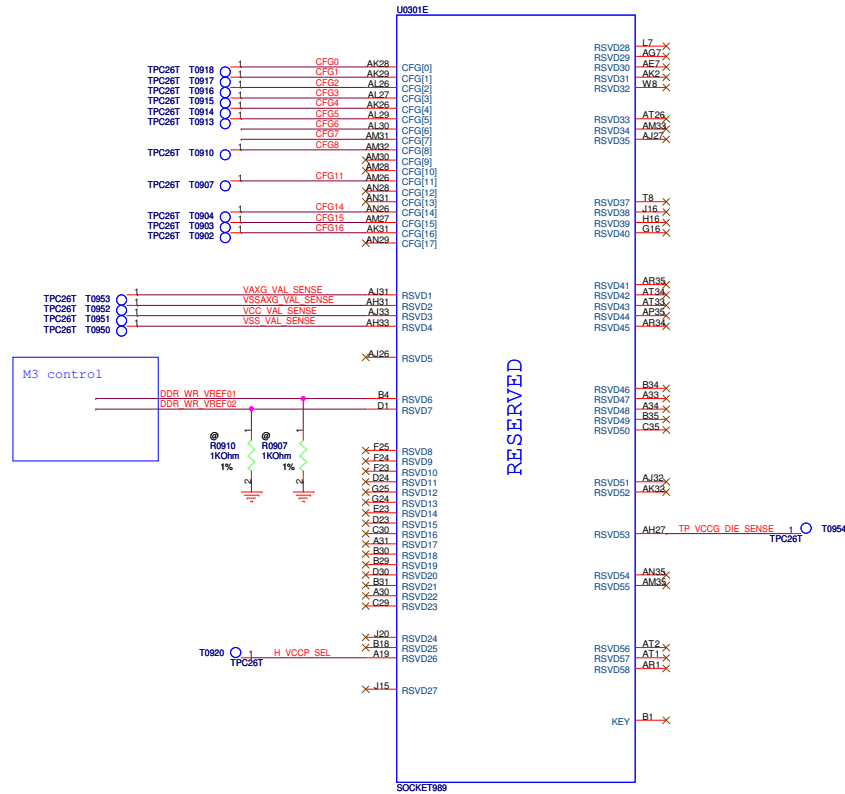
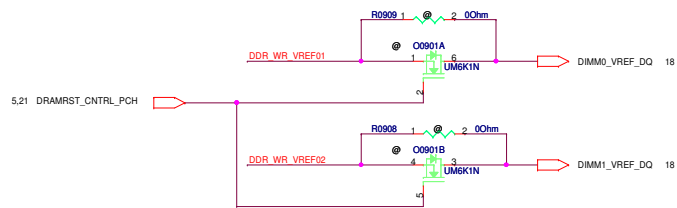
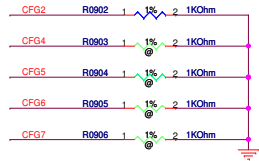
- 1: Disabled ; No Physical Display Port attached to Embedded DisplayPort
- 0: Enabled ; An external Display Port device is connected to the Embedded Display Port

CFG[6:5]: PCI Express Port Bifurcation Straps

- 11 : x 1 6
- 10 : x 8 , x 8
- 01 : Reserved
- 00 : x 8 , x 4 , x 4

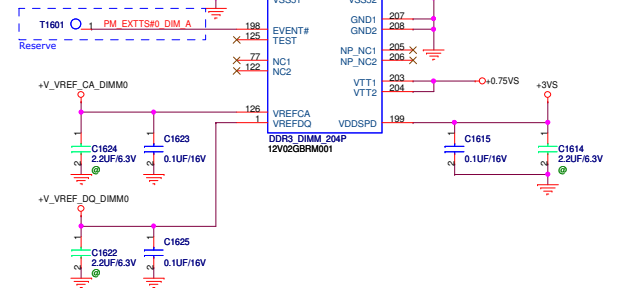
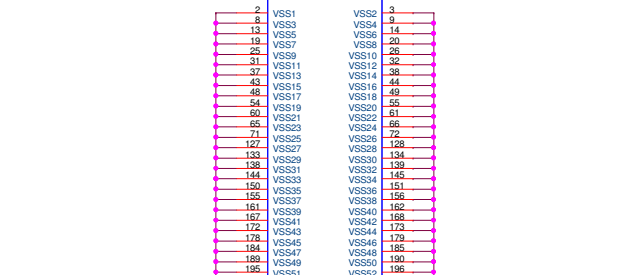
CFG[7]: PEG DEFER TRAINING

- 1: PEG Train immediately following xxRESETB de assertion
- 0: PEG Wait for BIOS training





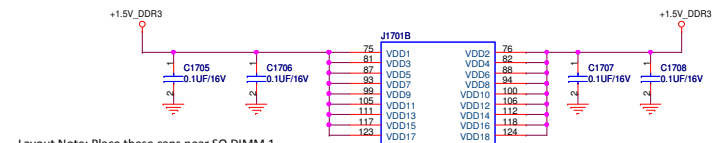
| | | | |
|---------------------------------|--------------|--------------------------|--------|
| PEGATRON | | Title : CPU_PCH_XDP***** | |
| BG1-CSC-HW R&D Dept.5 | | Engineer: Ahren_chen | |
| Size | Project Name | | Rev |
| Custom | PLFG | | 1.1 |
| Date: Monday, February 13, 2012 | Sheet | 10 | of 104 |



Layout Note: Place these caps near SO DIMM 0

The diagram shows two power rails with decoupling capacitors. The left rail is labeled +1.5V DDR3 and has six capacitors: C1609, C1610, C1611, C1612, C1613, and C1620. The right rail is labeled +0.75VS and has four capacitors: C1616, C1617, C1618, and C1619. All capacitors are 10uF/6.3V. A note above the left rail says 'Layout Note: Place these caps near SO DIMM 0'.





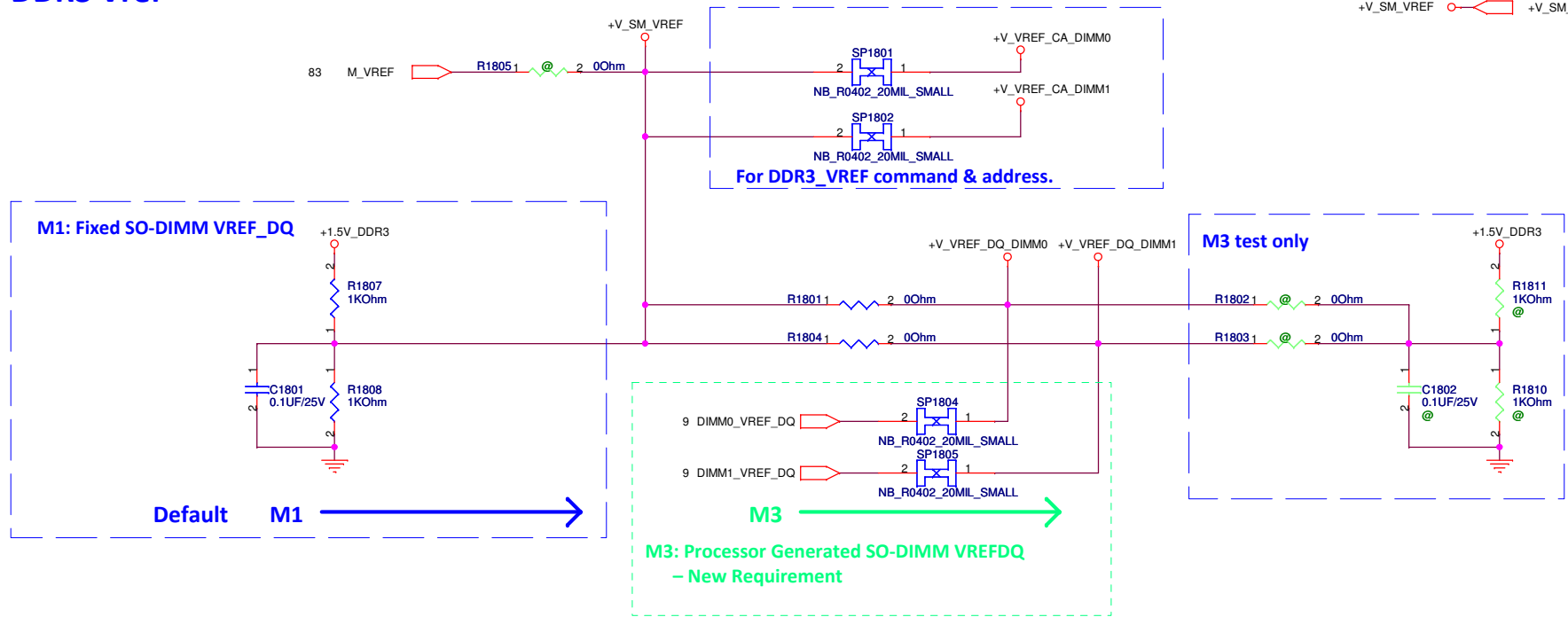
| | | | |
|-----|-------|-------|-----|
| 2 | VS51 | VS52 | 3 |
| 8 | VS53 | VS54 | 9 |
| 13 | VS55 | VS56 | 14 |
| 19 | VS57 | VS58 | 20 |
| 25 | VS59 | VS510 | 26 |
| 31 | | | 32 |
| 37 | VS511 | VS512 | 38 |
| 43 | VS513 | VS514 | 44 |
| 49 | VS515 | VS516 | 50 |
| 54 | VS517 | VS518 | 55 |
| 59 | VS519 | VS520 | 60 |
| 65 | VS521 | VS522 | 66 |
| 71 | VS523 | VS524 | 72 |
| 77 | VS525 | VS526 | 78 |
| 83 | VS527 | VS528 | 84 |
| 89 | VS529 | VS530 | 90 |
| 95 | VS531 | VS532 | 96 |
| 101 | VS533 | VS534 | 102 |
| 107 | VS535 | VS536 | 108 |
| 113 | VS537 | VS538 | 114 |
| 119 | VS539 | VS540 | 116 |
| 125 | VS541 | VS542 | 118 |
| 131 | VS543 | VS544 | 119 |
| 137 | VS545 | VS546 | 120 |
| 143 | VS547 | VS548 | 121 |
| 149 | VS549 | VS550 | 122 |
| 155 | VS551 | VS552 | 123 |



Layout Note: Place these caps near SO DIMM 1



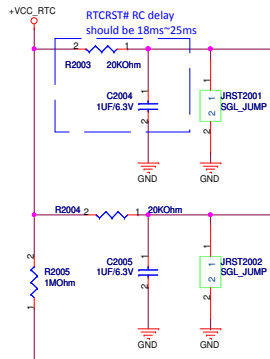
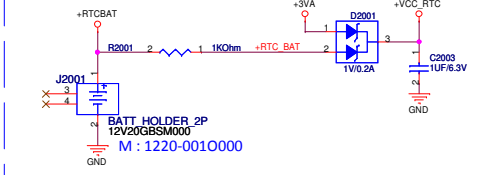
DDR3 Vref



If support M3 :
 1. Mount R1802,R1803,R1805,R1806,R1810,R1811,C1802
 2. Un mount R1801,R1804

| | | | |
|------------------|--|------------------|----------------|
| +1.5V_DDR3 | | +1.5V_DDR3 | 16,17,83,84,91 |
| +V_VREF_CA_DIMM0 | | +V_VREF_CA_DIMM0 | 16 |
| +V_VREF_DQ_DIMM0 | | +V_VREF_DQ_DIMM0 | 16 |
| +V_VREF_CA_DIMM1 | | +V_VREF_CA_DIMM1 | 17 |
| +V_VREF_DQ_DIMM1 | | +V_VREF_DQ_DIMM1 | 17 |
| +V_SM_VREF | | +V_SM_VREF | 7 |

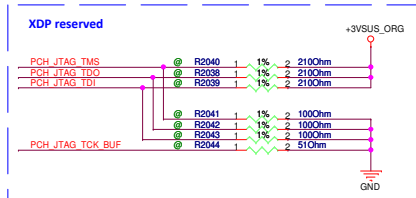
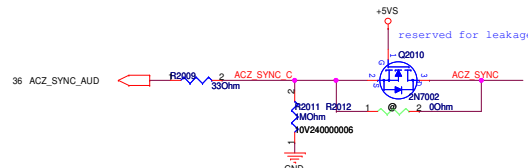
RTC battery



Request by CSC for CMOS clear function

| CMOS Settings | JRST2001 | TPM Settings | JRST2002 |
|---------------|----------|------------------------|----------|
| Clear CMOS | Shunt | Clear ME RTC Registers | Shunt |
| Keep CMOS | Open | Keep ME RTC Registers | Open |

INTVRMEN: Integrated SUS 1.05V VRM Enables
Low: Enable External VRs
High: Enable Internal VRs



Strap information:

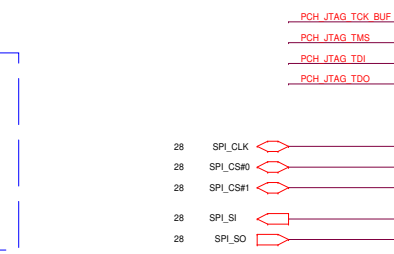
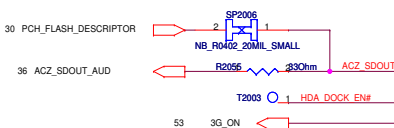
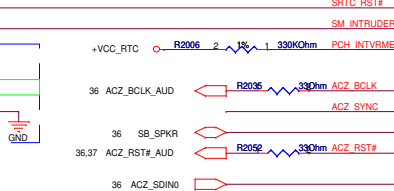
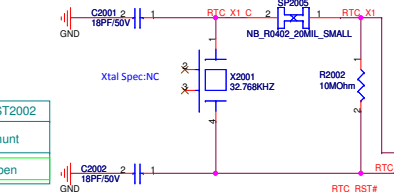
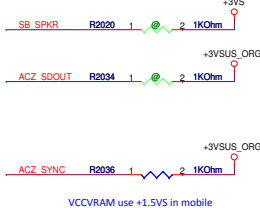
SB_SPKR: No reboot strap
Low: Disable
High: Enable

ACZ_SDOUT:
1. Flash descriptor security:
Sampled Low: in effect.
Sampled High: override

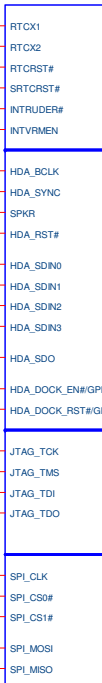
2. ACZ_SDOUT which sample high on the rising edge of PWROK will also disable Intel ME.

ACZ_SYNC: On Die PLL VR voltage selector
Low: 1.8V
High: 1.5V

note:
CRB has no strap
Hiron River Platform Schematic Design Checklist(438390 page 48)



U2001A



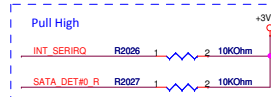
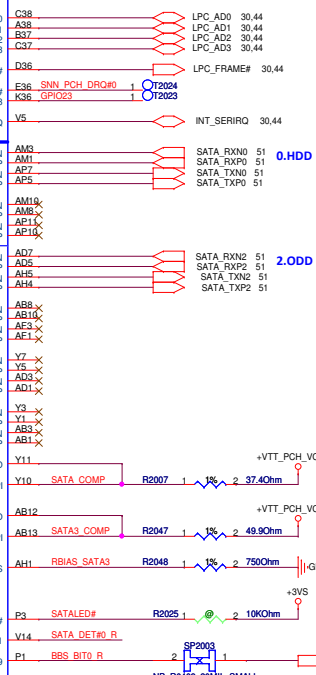
COUGAR_POINT_ES1

PANTHERPOINT

M : 0200-00MNOTB (ES2)

S : 0200-00ME0TB (ES1)

+VCC_RTC 22.27
+3VA 30.40,48.57,60.65,81.88,93
+3VS 4.16,17.21,22.23,24.25,26.27,28.30,31.32,33.36,37.40,45.46,48.50,51.53,57.75,80.91,92
+3VSUS_ORG 21.22,24.25,27
+VTT_PCH_VCCIO 26.27
+5VS 27.30,31.36,46,48.50,51.56,57.80,91



2.WLAN
3.LAN
4.USB3.0

2.WLAN
3.LAN
4.USB3.0

U2001B

PCI-E*

SMBUS

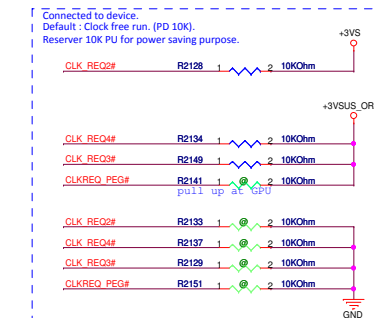
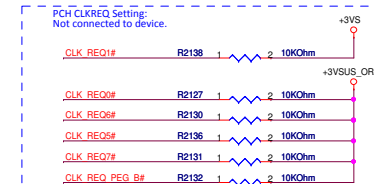
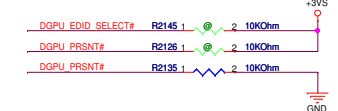
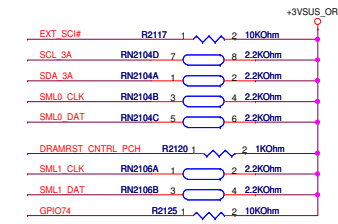
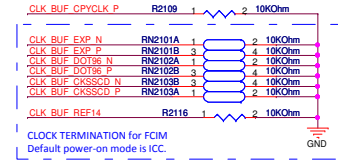
Controller Link

CLOCKS

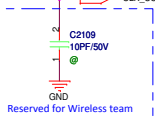
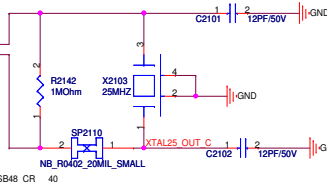
FLEX CLOCKS

PANTHERPOINT
M : 0200-00MN0TB (ES2)
S : 0200-00ME0TB (ES1)

+3VS_O -> +3VS 4,16,17,20,22,23,24,25,26,27,28,30,31,32,33,36,37,40,45,46,48,50,51,53,57,75,80,91,92
+VTT_PCH_ORG -> +VTT_PCH_ORG 22,26,27
+3VSUS_ORG -> +3VSUS_ORG 20,22,24,25,27



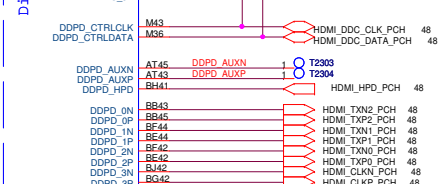
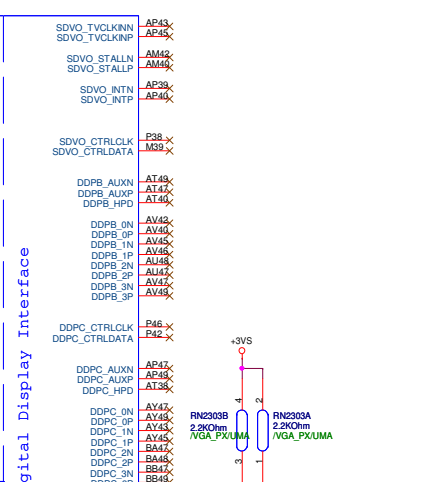
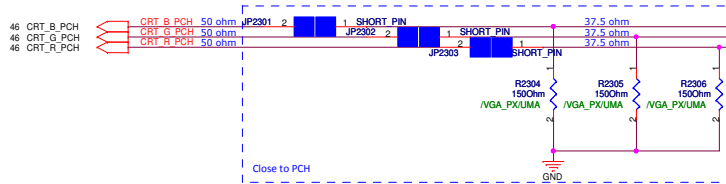
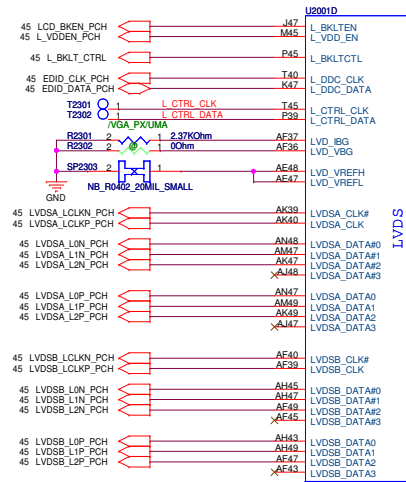
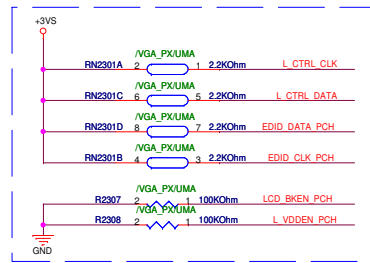
NOTE: Pull-down can be shared between P and N signals.
25-MHz is required in:
1. FCIM
2. BTM for PCH Display Clock generation in Integrated Graphics platforms



PEGATRON Title : PCH(2)_PCIE,CLK,SMB,PEG

BG1-GSC-HW R&D Dept.5 Engineer: Ahren_chen

Size C Project Name PLFG Rev 1.1
Date: Monday, February 13, 2012 Sheet 21 of 104



PANTHERPOINT
M : 0200-00MNOTB (ES2)
S : 0200-00ME0TB (ES1)

CRT Disable: (For discrete graphic)

1. NC:
CRT_RED, CRT_GREEN, CRT_BLUE
CRT_HSYN, CRT_VSYN
2. 1-kΩ ±0.5% pull-down to GND:
DAC_IREF
3. Connected to GND:
CRT_ITRN
4. Connect to +V3.3:
VCCADAC

DisPlay Port Disable: (For discrete graphic)

1. NC:
ALL

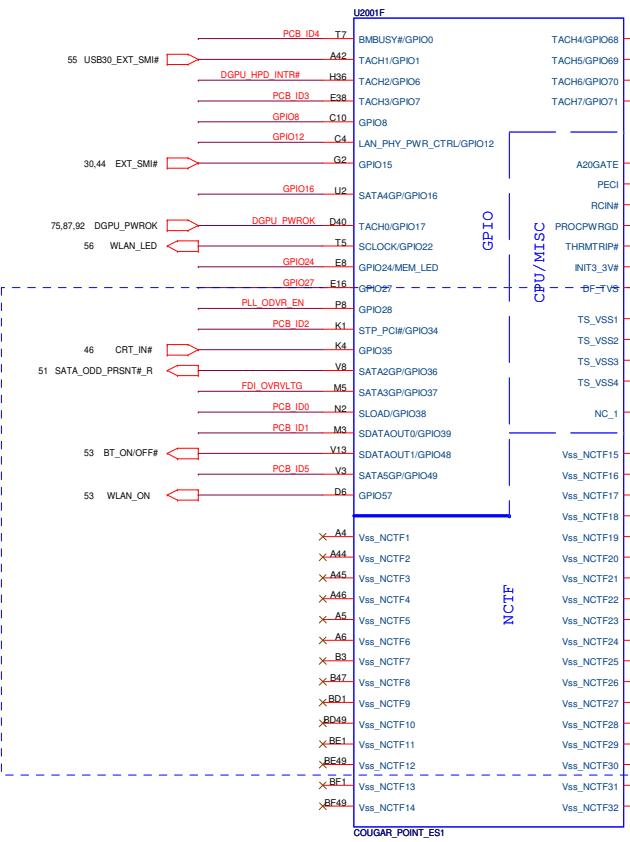
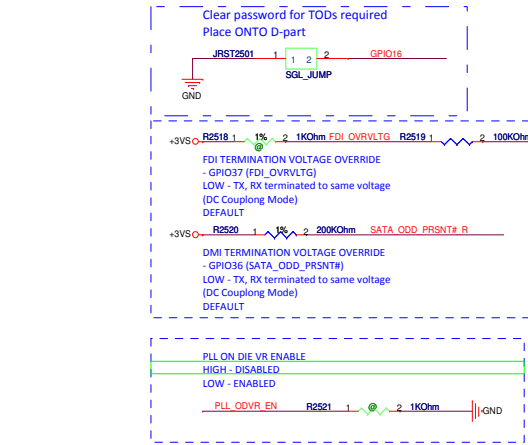
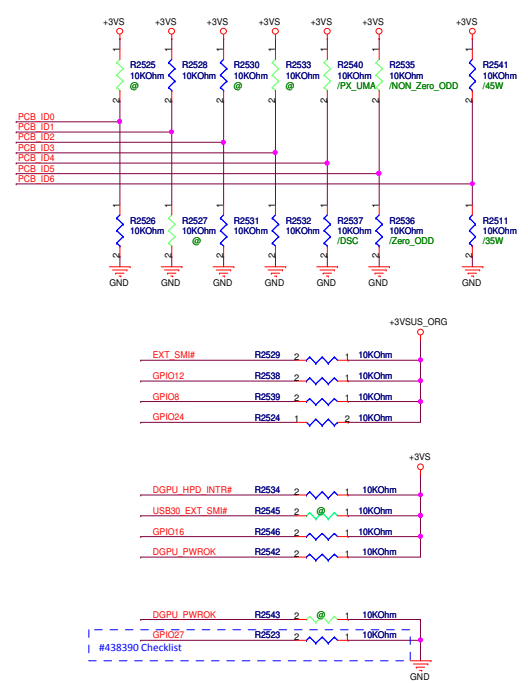
LVDS Disable: (For discrete graphic)

1. NC:
LVDSA_DATA [3:0], LVDSA_DATA# [3:0],
LVDSA_CLK, LVDSA_CLK#, LVDSB_DATA [3:0],
LVDSB_DATA# [3:0], LVDSB_CLK, LVDSB_CLK#
L_VDD_EN, L_BKLTEN, L_BKLTCTL, LVD_VREFH
LVD_VREFL, LVD_IBG, LVD_VBG
2. Connected to GND:
VccALVDS, VccTX_LVDS

Display Port D

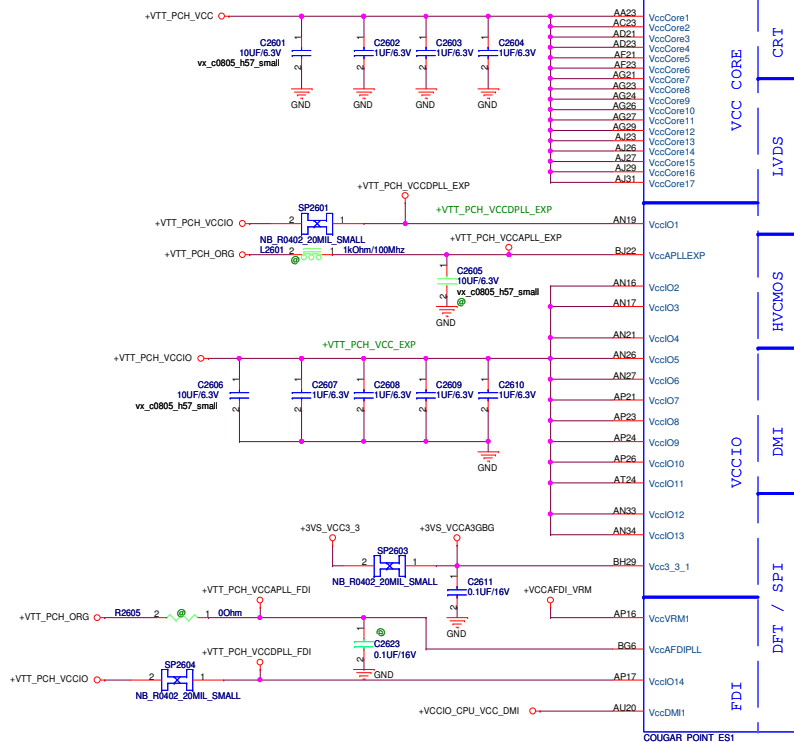
BIOS Rev. SKU











| ID0 | ID1 | PCB Rev. | PCB_ID2 | PCB_ID3 | PCB_ID4 | PCB_ID5 | PCB_ID6 |
|-----|-----|----------|------------|--------------|------------|-----------------|------------|
| 0 | 0 | R1.0 | 0: HDMI | 0: USB3.0 | 0:DSC only | 0: Zero_ODD | 0: CPU 35W |
| 0 | 1 | R1.1 | | | | | |
| 1 | 0 | R2.0 | 1:non-HDMI | 1:non-USB3.0 | 1:PX & UMA | 1: NON_Zero_ODD | 1: CPU 45W |
| 1 | 1 | R2.1 | | | | | |

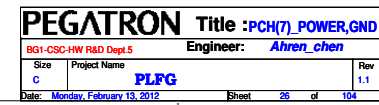
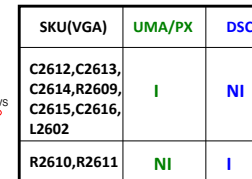


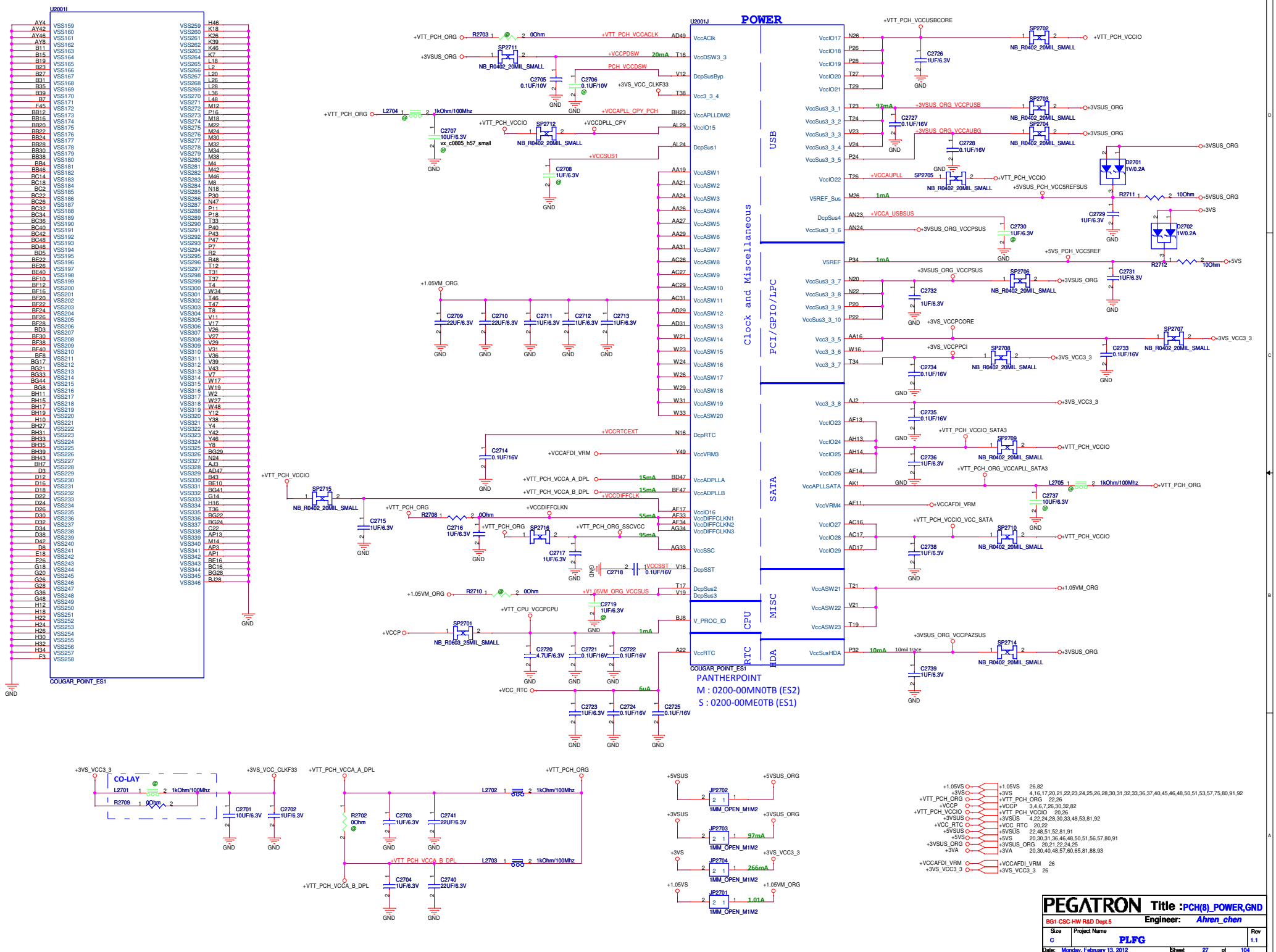
PANTHERPOINT
M : 0200-00MNOTB (E52)
S : 0200-00MEOTB (E51)

| | |
|------------|---|
| +3VS | 4,16,17,20,21,22,23,24,26,27,28,30,31,32,33,36,37,40,45,46,48,50,51,53,57,75,80,91,92 |
| +VCCP | 3,4,6,7,26,27,30,32,82 |
| +3VSUS_ORG | 20,21,22,24,27 |
| +1.8VS | 7,26,80,84 |



| | | | |
|----------------|--|----------------|---|
| +VTT_PCH_VCCIO |  | +VTT_PCH_VCCIO | 20,27 |
| +VTT_PCH_ORG |  | +VTT_PCH_ORG | 22,27 |
| +VCCP |  | +VCCP | 3,4,6,7,27,30,32,82 |
| +1.8VS |  | +1.8VS | 7,25,80,84 |
| +1.5VS |  | +1.5VS | 53,57,91 |
| +3VS |  | +3VS | 4,16,17,20,21,22,23,24,25,27,28,30,31,32,33,36,37,40,45,46,48,50,51,53,57,75,80,91,92 |
| +1.05VS |  | +1.05VS | 27,82 |
| +3VS_VCC3_3 |  | +3VS_VCC3_3 | 27 |
| +3VM_SPI |  | +3VM_SPI | 28 |
| +VCCAFDI_VIRM |  | +VCCAFDI_VIRM | 27 |





PCH SPI ROM

+3VA_EC reserved for share ROM



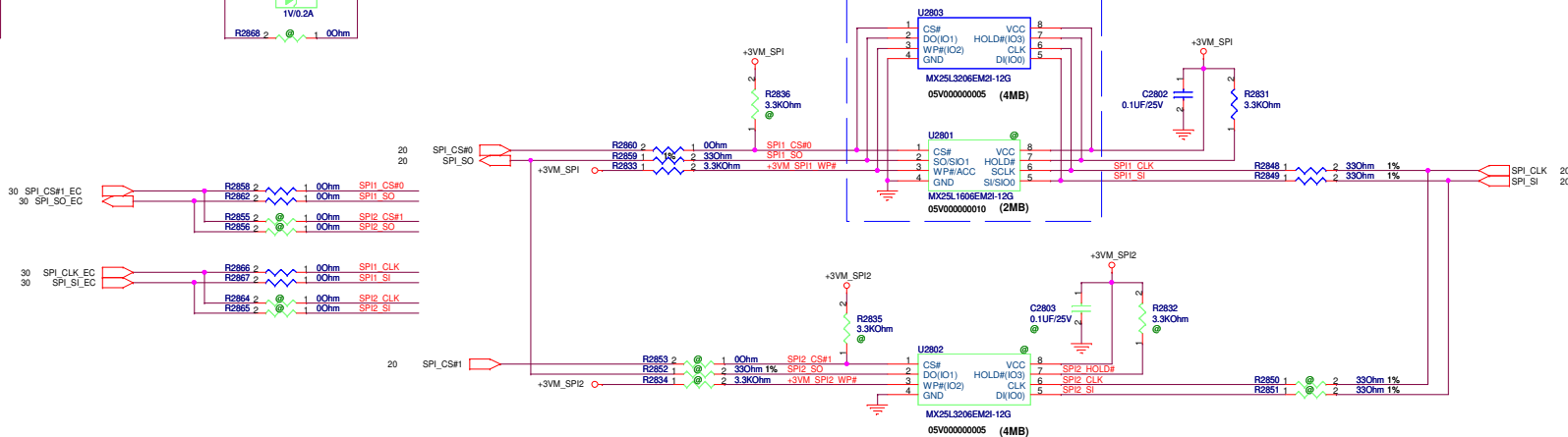
Configuration1

| | | |
|--|------------|-----|
| U2801 | @ | |
| U2802 | @ | |
| U2803 | ME+BIOS+EC | 4MB |
| ummount: R2855, R2856, R2864, R2865, R2853, R2852, R2834, R2850, R2851, R2832, C2803, U2802, R2869, R2870, R2868, D2802, U2801, R2835, R2836 | | |

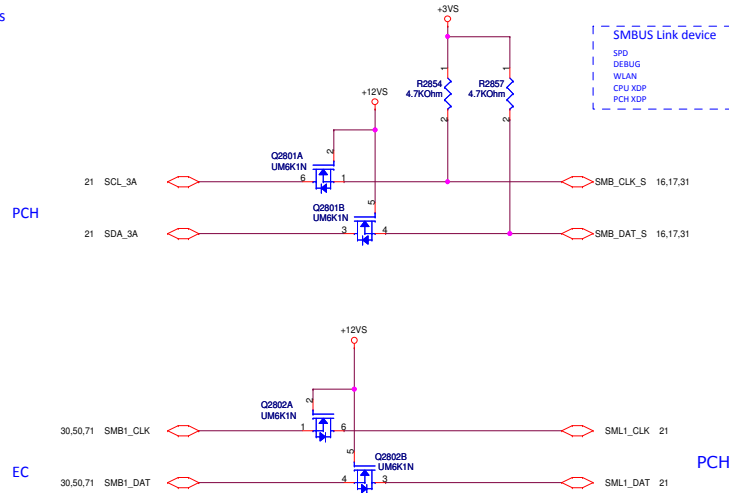
Configuration2

| | | |
|---|-------------|-----|
| U2801 | ME Firmware | 2MB |
| U2802 | EC+BIOS | 4MB |
| ummount: R2858, R2862, R2866, R2867, U2803 | | |

co-lay on the same location



PCH SMBus

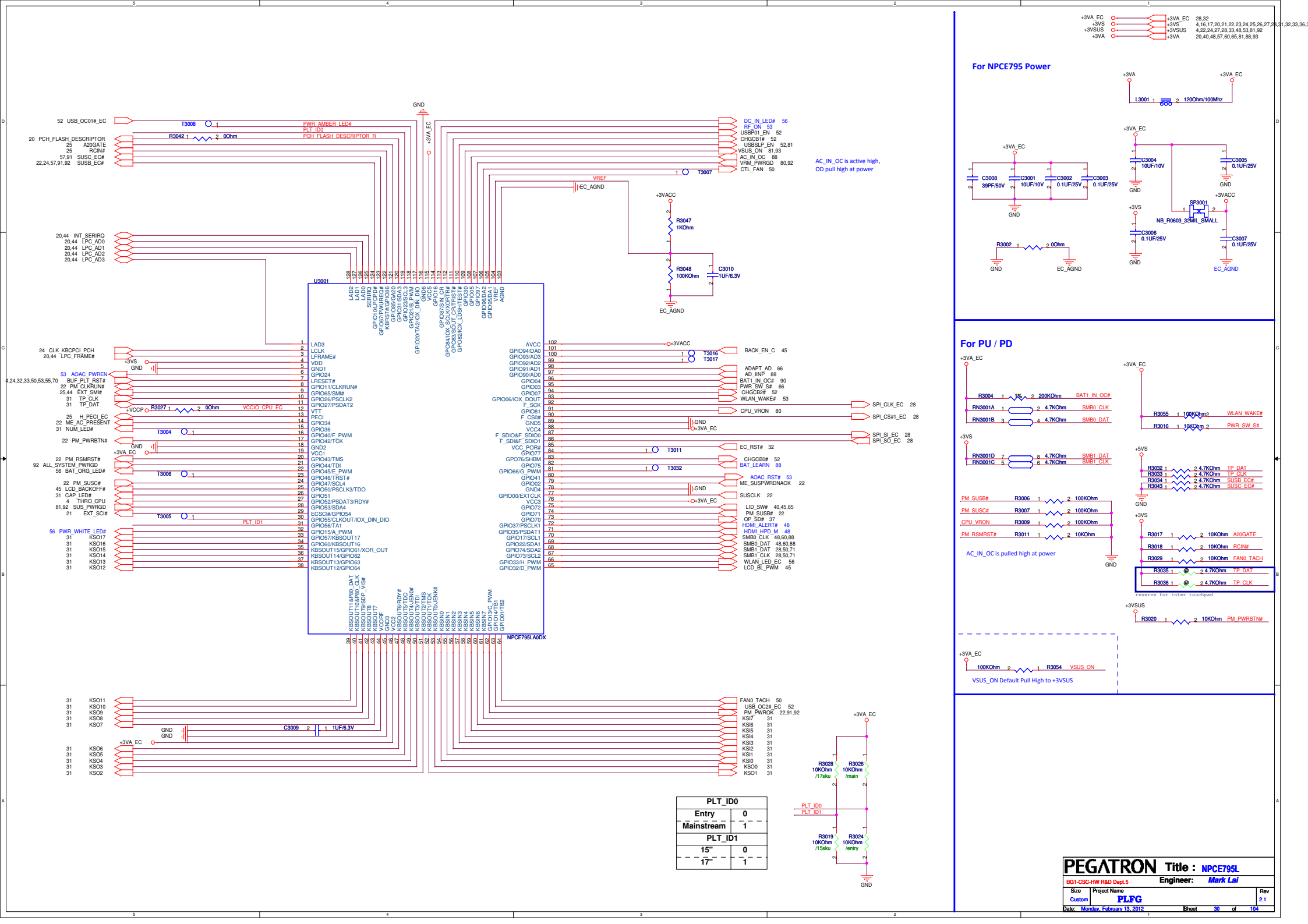


PEGATRON Title : PCH(9)_SPI,SMB

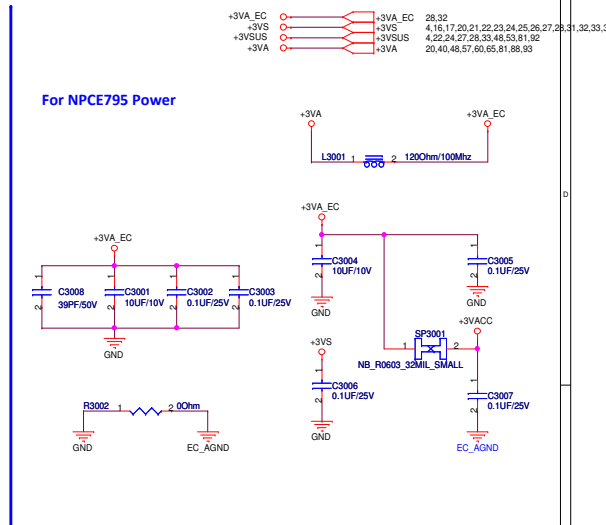
BG1-CSC-HW R&D Dept.5 Engineer: Ahren_chen

Size Project Name PLFG Rev

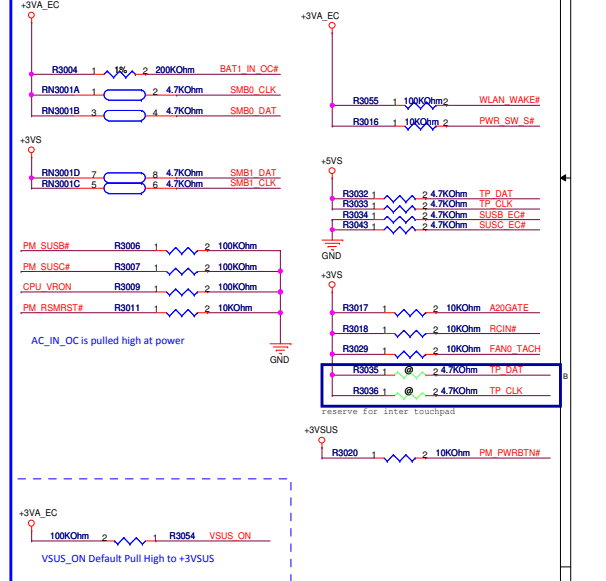
Date: Monday, February 13, 2012 Sheet 26 of 104



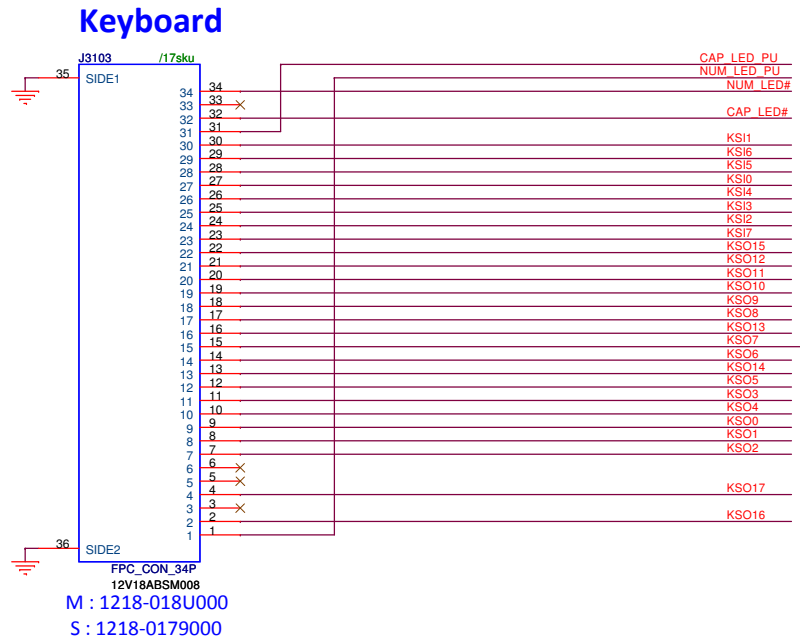
For NPCE795 Power



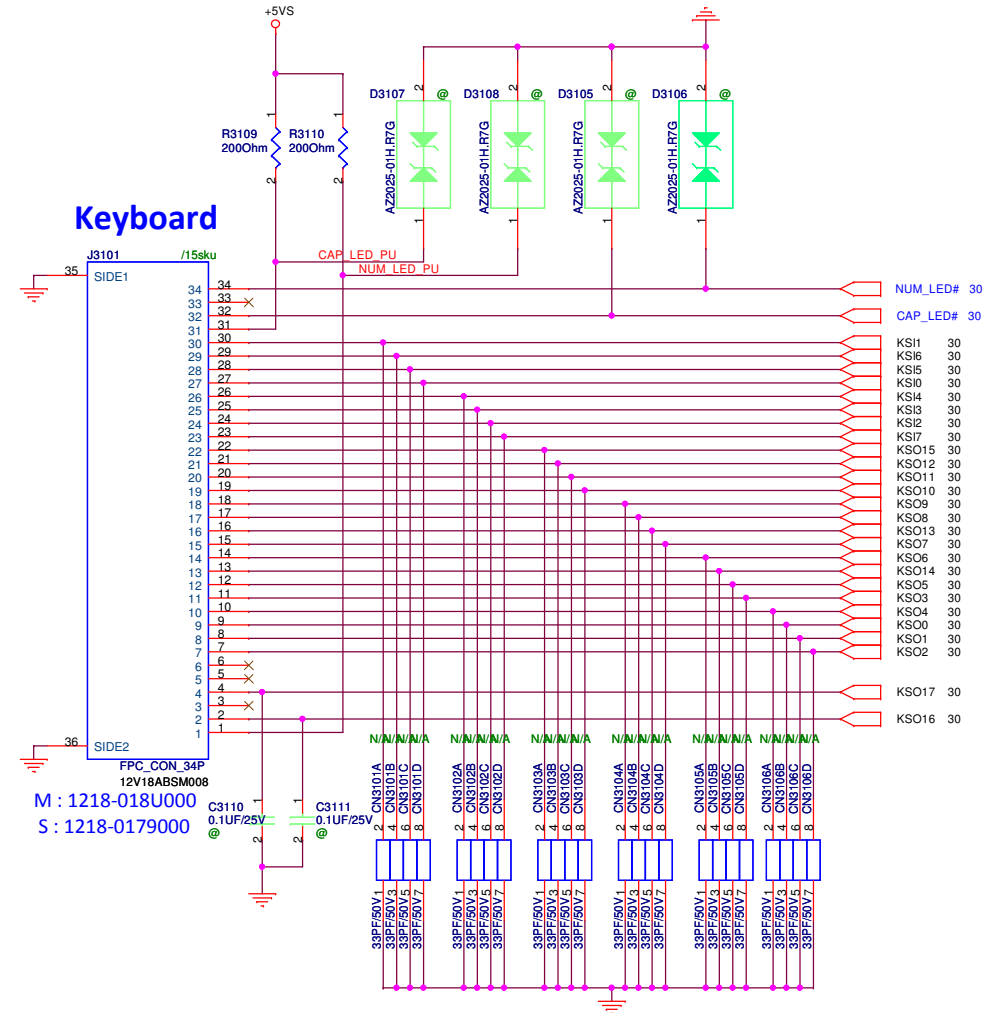
For PU / PD



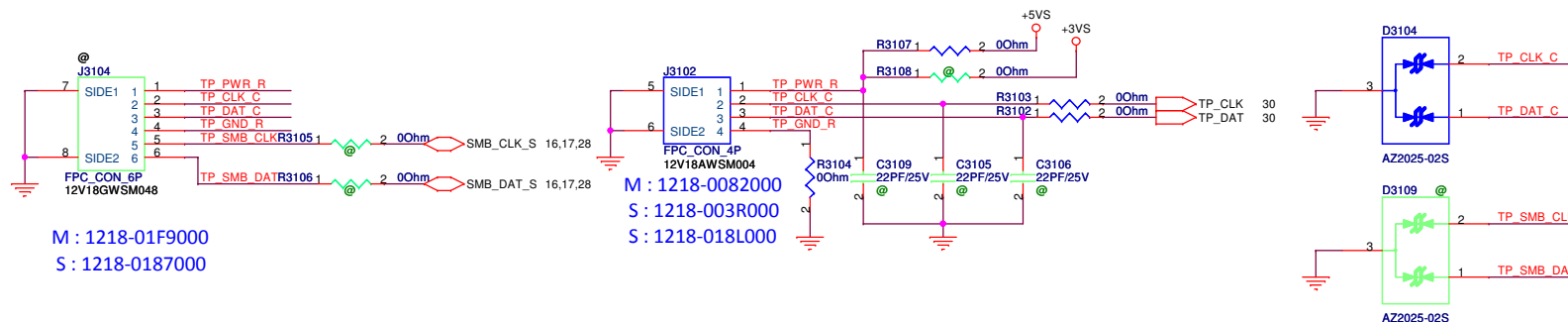
KB CONNECTER FOR 17"



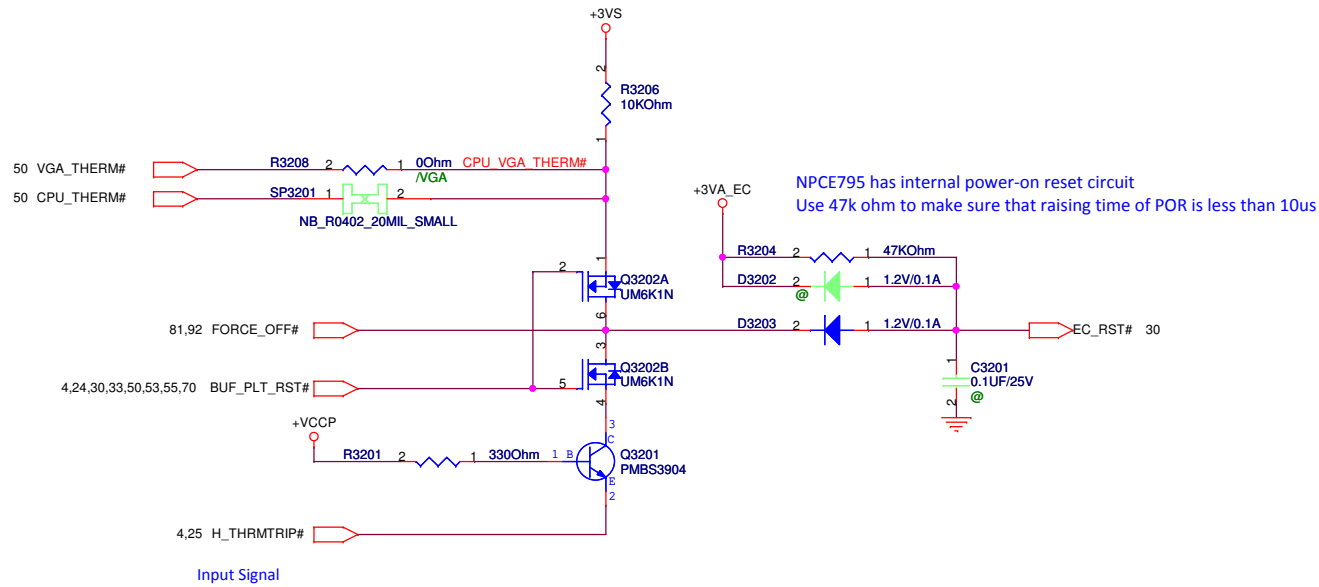
KB CONNECTER FOR 15"



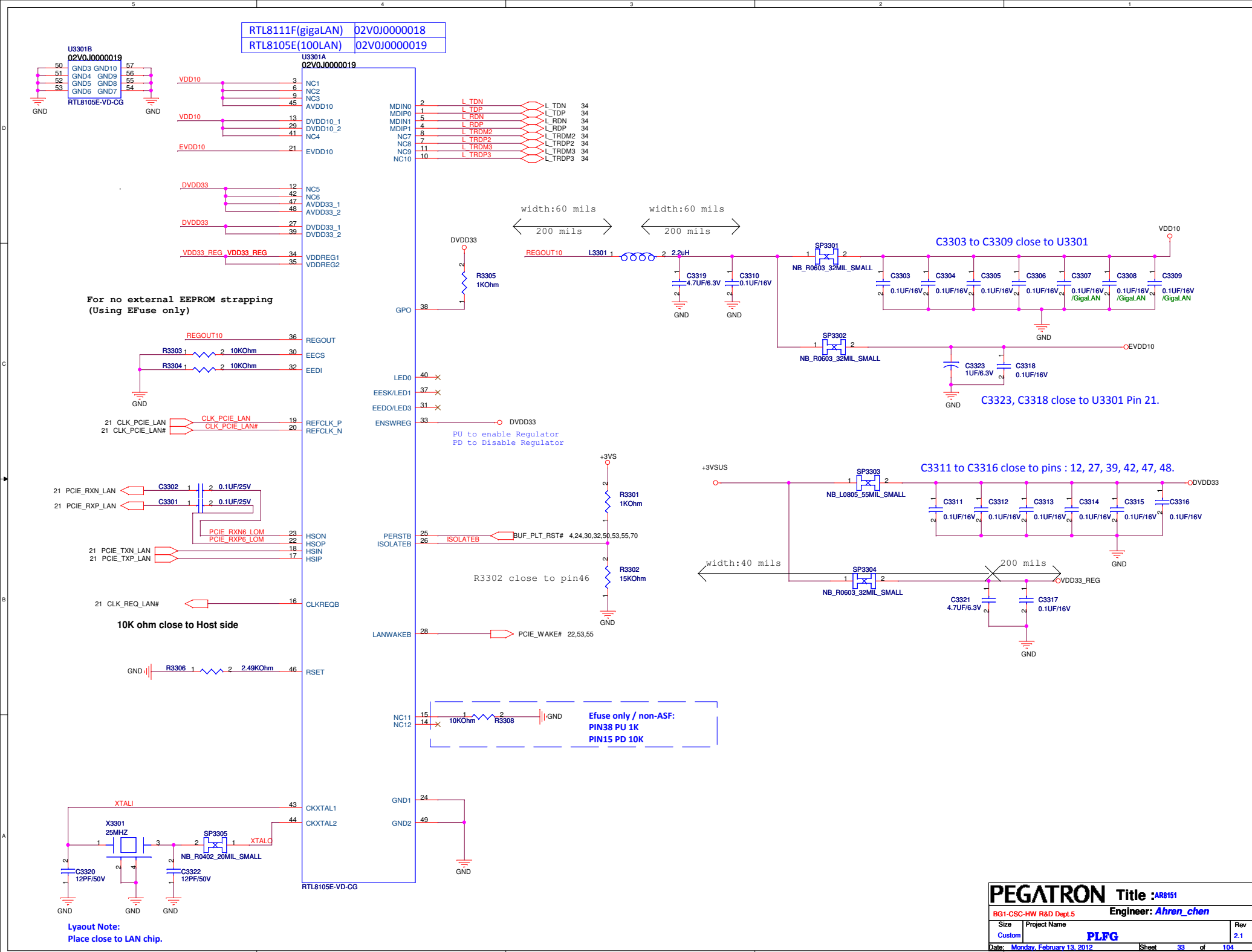
Touch Pad Module

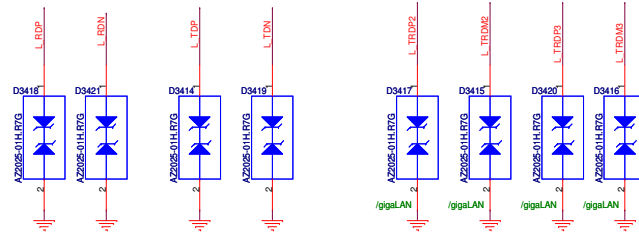
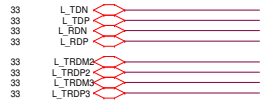


Thermal Policy

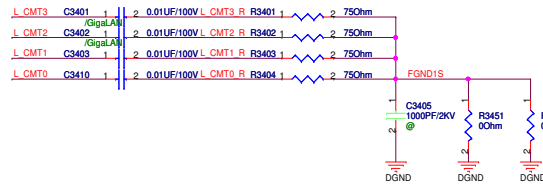
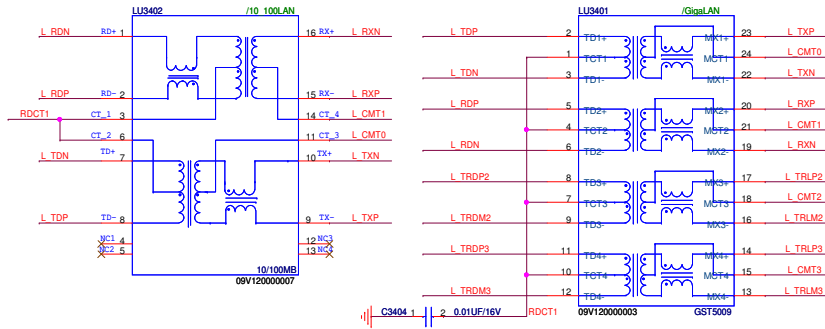


| | | | |
|--|-----------------------------|----------------------------------|------------|
| PEGATRON | | Title : RST_Reset Circuit | |
| BG1-CSC-HW R&D Dept.5 | | Engineer: Ahren_chen | |
| Size B | Project Name PLFG | | Rev 2.1 |
| Date: Monday, February 13, 2012 | | Sheet | 32 of 104 |

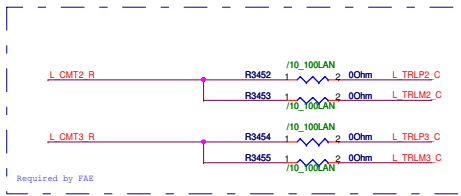
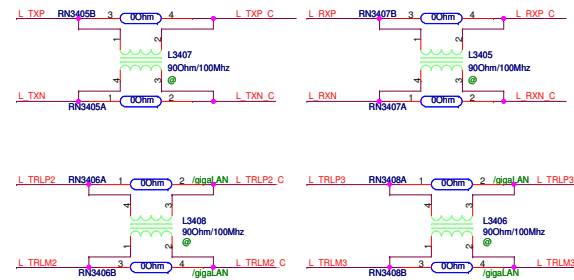




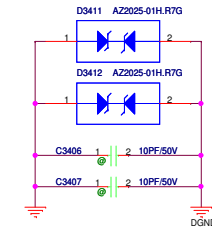
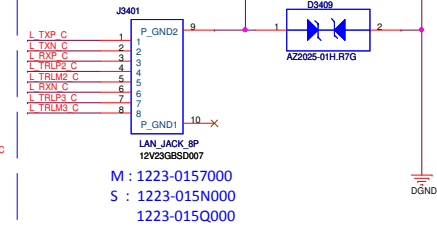
Transformer Co-Layout



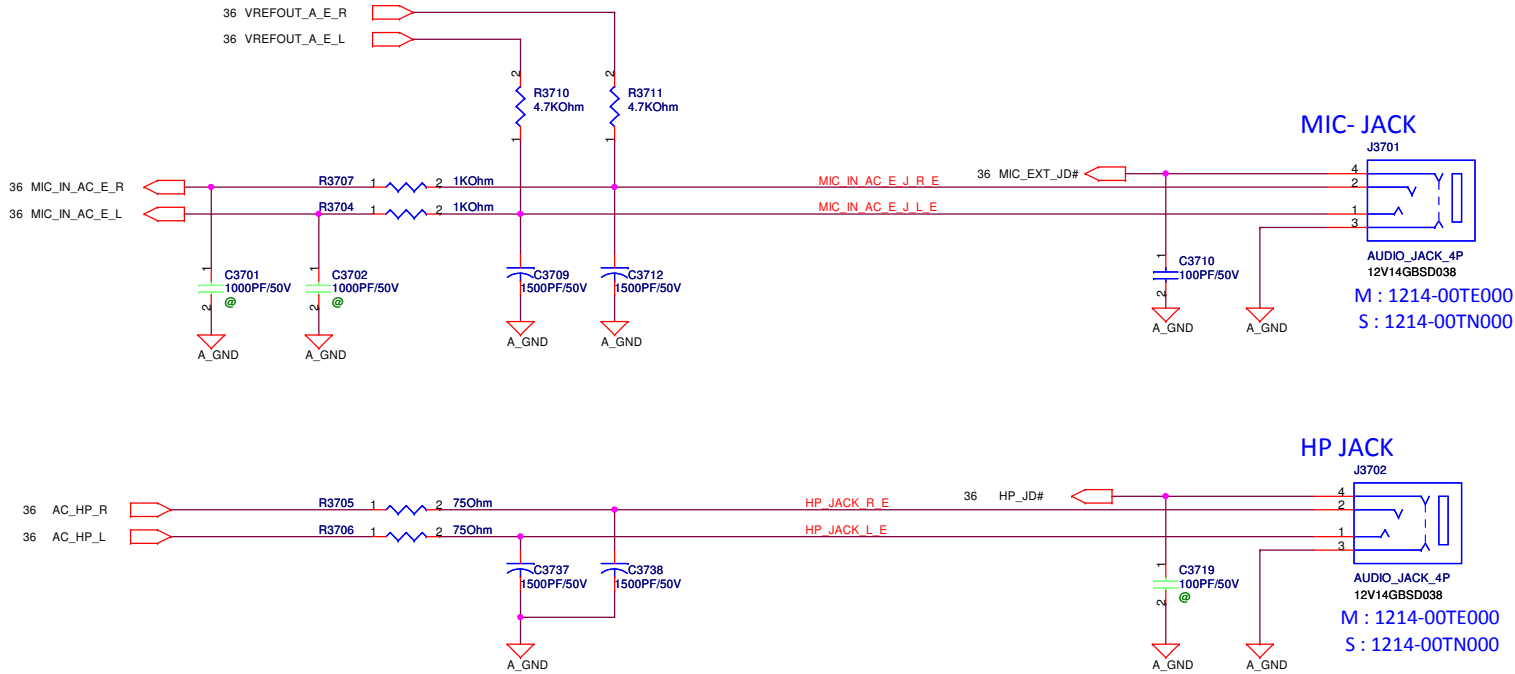
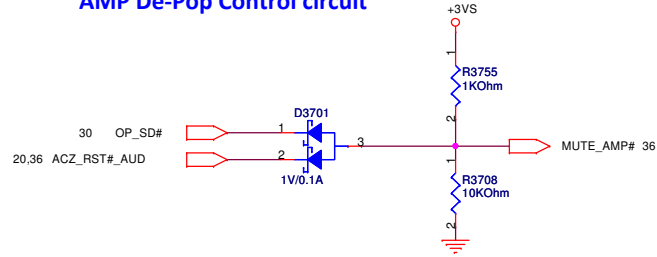
Required by EMC



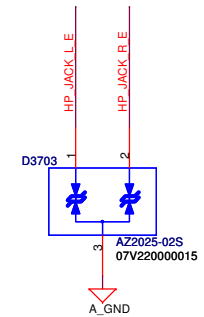
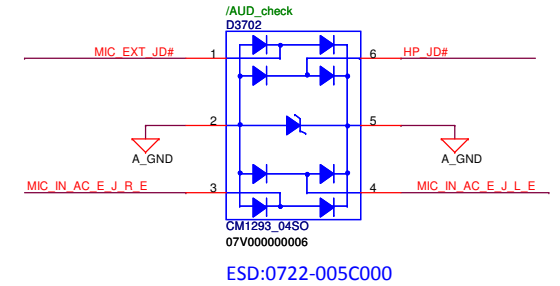
RJ45

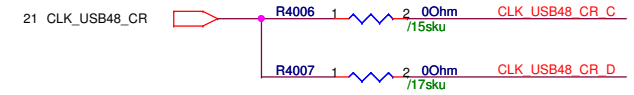
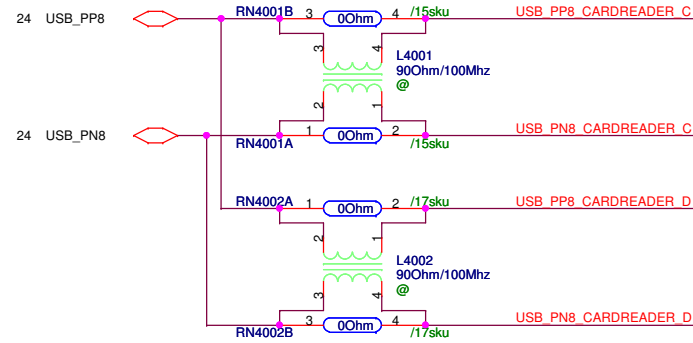
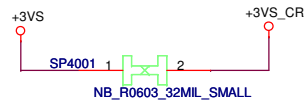


AMP De-Pop Control circuit

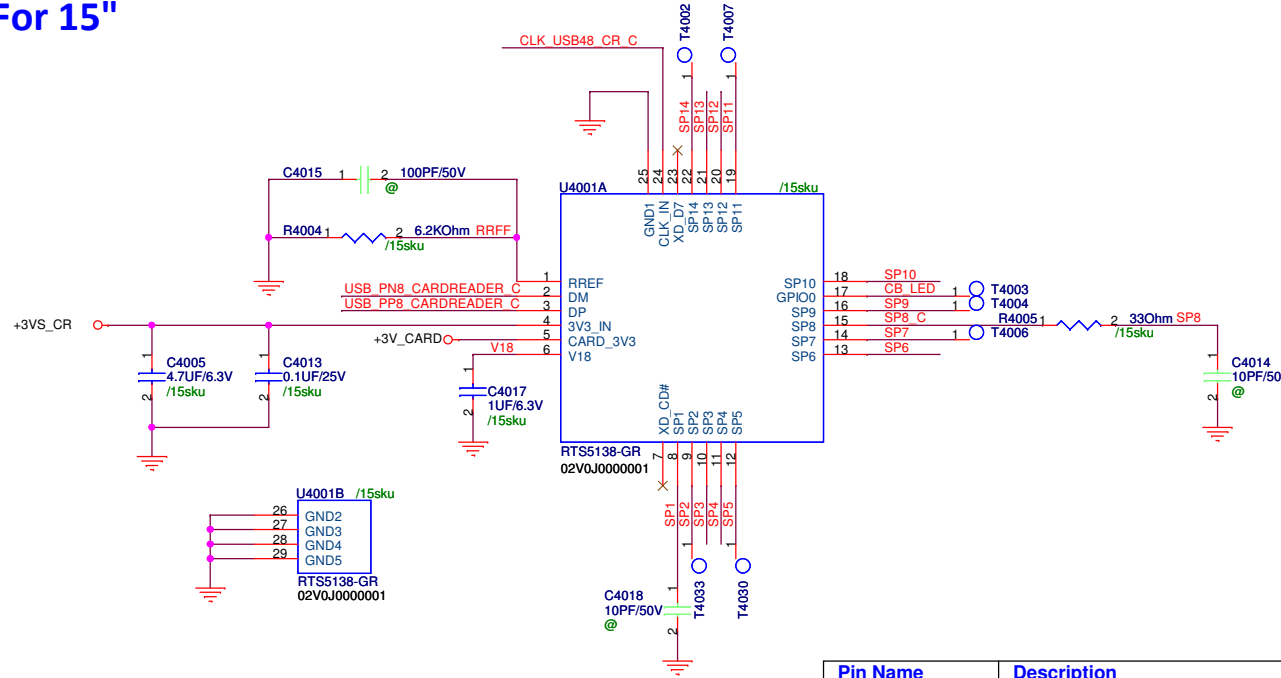


Please use 0722-005C000 for ESD



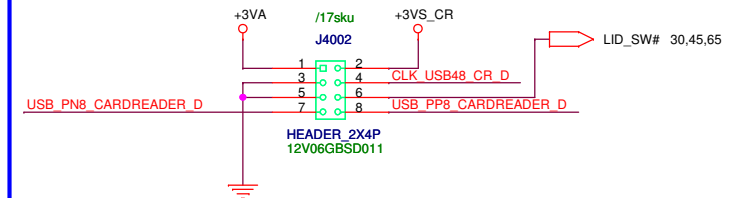


For 15"

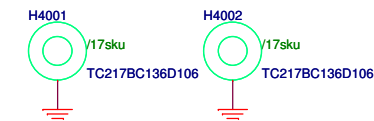


| Pin Name | Description |
|----------|-----------------|
| SP1 | SDWP# / MSCLK |
| SP2 | MS_INS# |
| SP3 | SD_DAT1 |
| SP4 | SD_DAT0 |
| SP5 | MS_D3 |
| SP6 | SD_CD# |
| SP8 | SD_CLK / MS_D2 |
| SP9 | MS_D0 |
| SP10 | SD_CMD |
| SP12 | SD_DAT3 / MS_D1 |
| SP13 | SD_DAT2 |
| SP14 | MS_BS |

For 17"

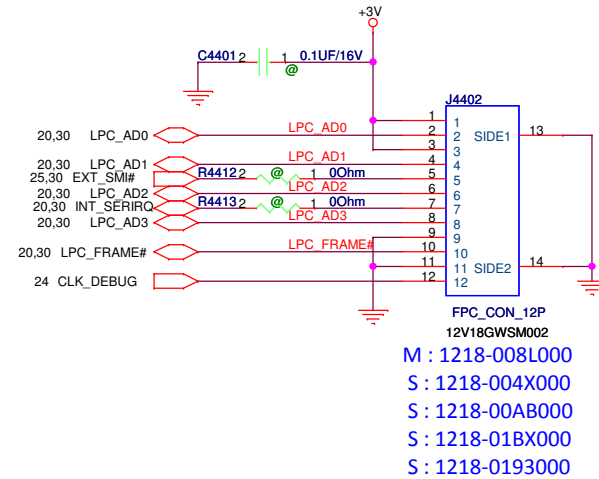


NUT



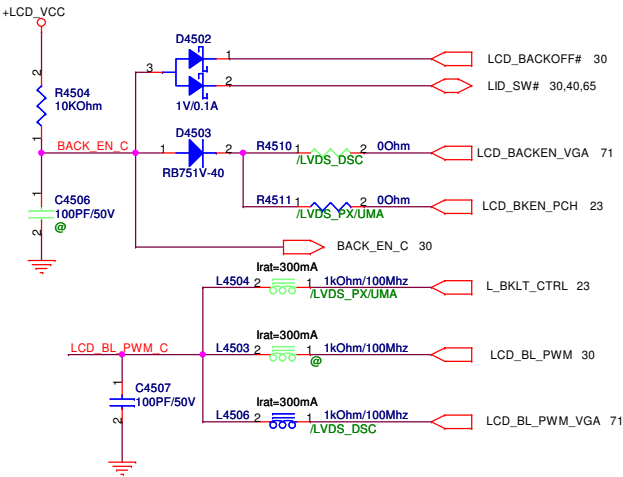
M : 13N0-4HU0201

DEBUG CARD CONN.

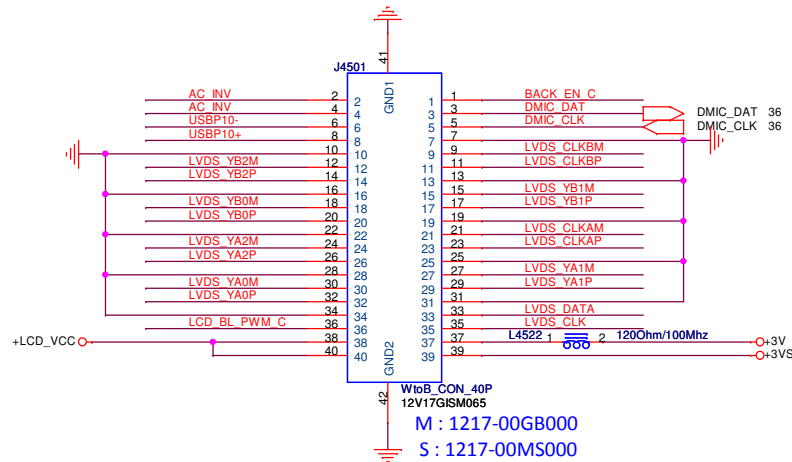


| | | | |
|--|-----------------------------|-----------------------------|-------------------------|
| PEGATRON | | Title : BUG_Debug | |
| BG1-CSC-HW R&D Dept.5 | | Engineer: Ahren_chen | |
| Size B | Project Name PLFG | Rev 2.1 | |
| Date: Monday, February 13, 2012 | | Sheet | 44 of 104 |

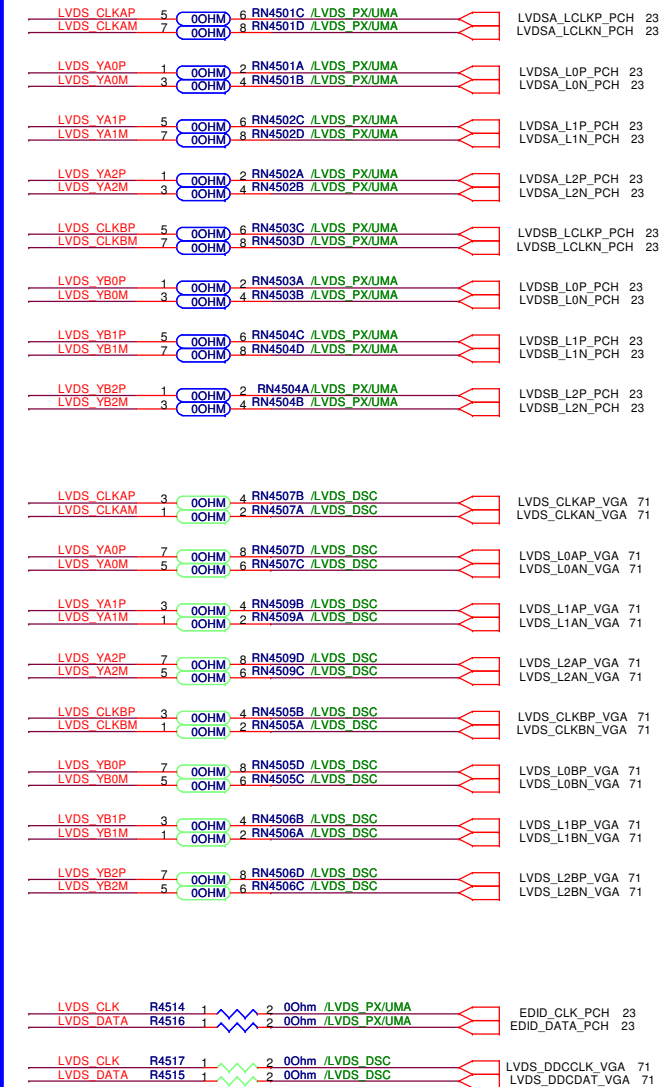
Controller circuit



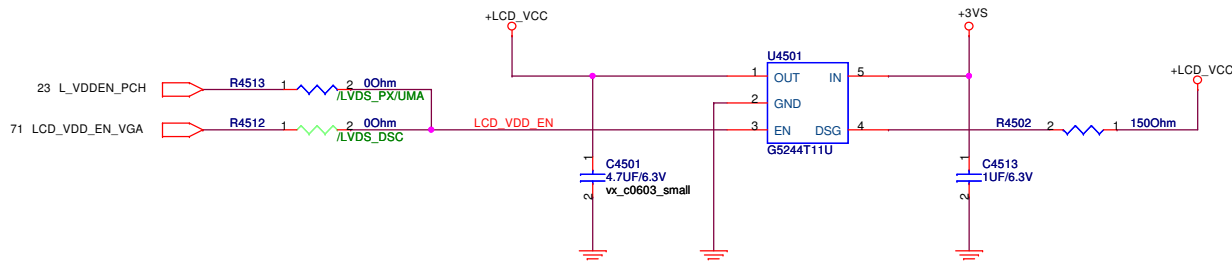
LVDS Conn w/Camera Module & Dig. Mic

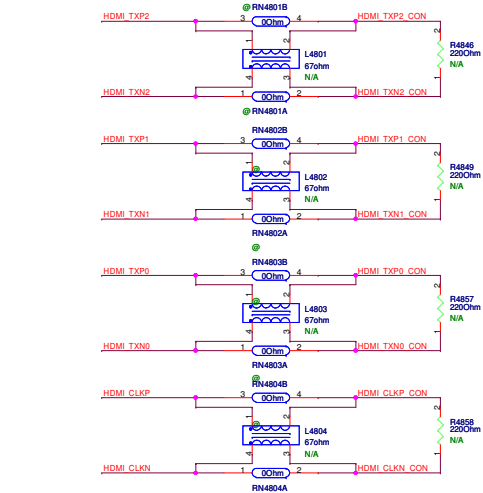
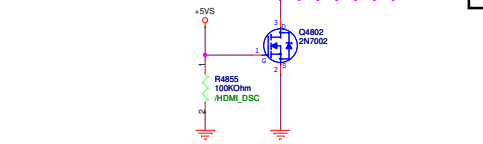
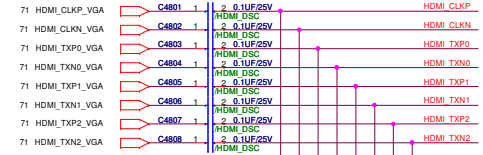
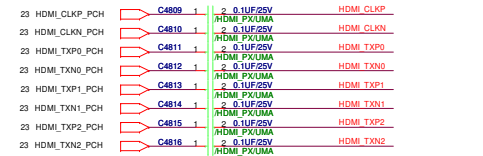


PCH / VGA

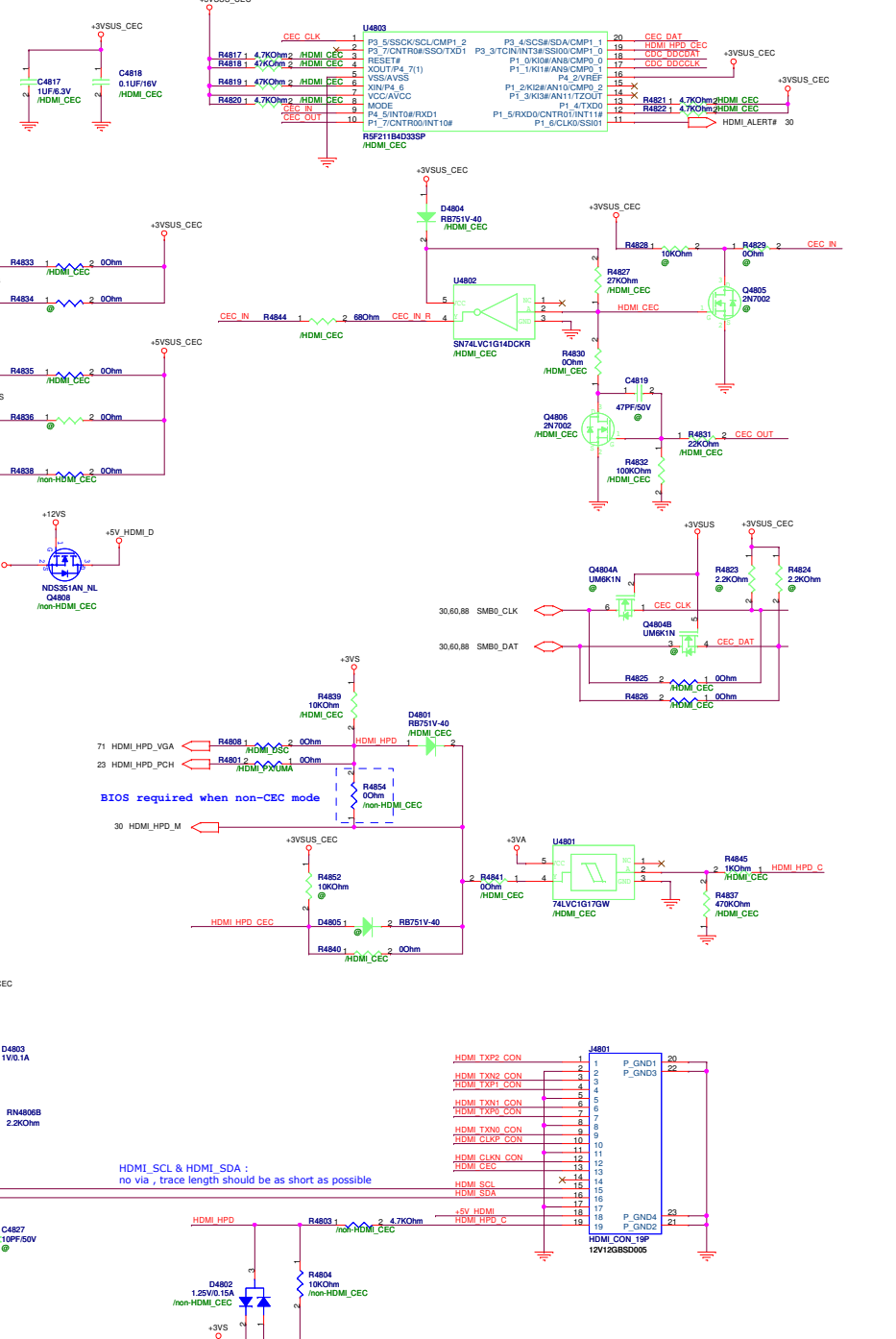
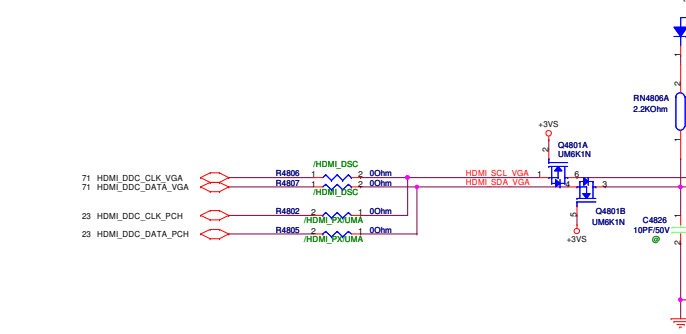
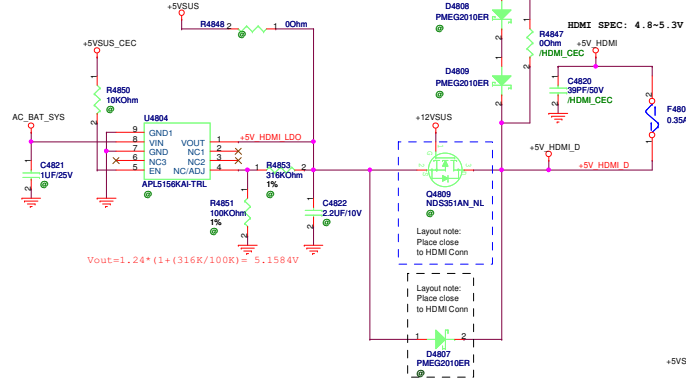


LCD VDDEN / +LED_VCC

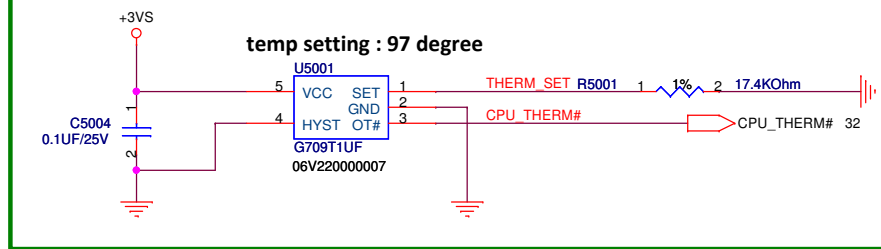




| SKU | HDMI_UMA/PX | HDMI_DSC |
|---|---|---|
| R4809,R4810, R4811,R4812, R4813,R4814, R4815,R4816 | 680 Ohm VX:10V240000041 PN:1024-0051000 | 499 Ohm VX:10V220000076 PN:1022-00DA000 |

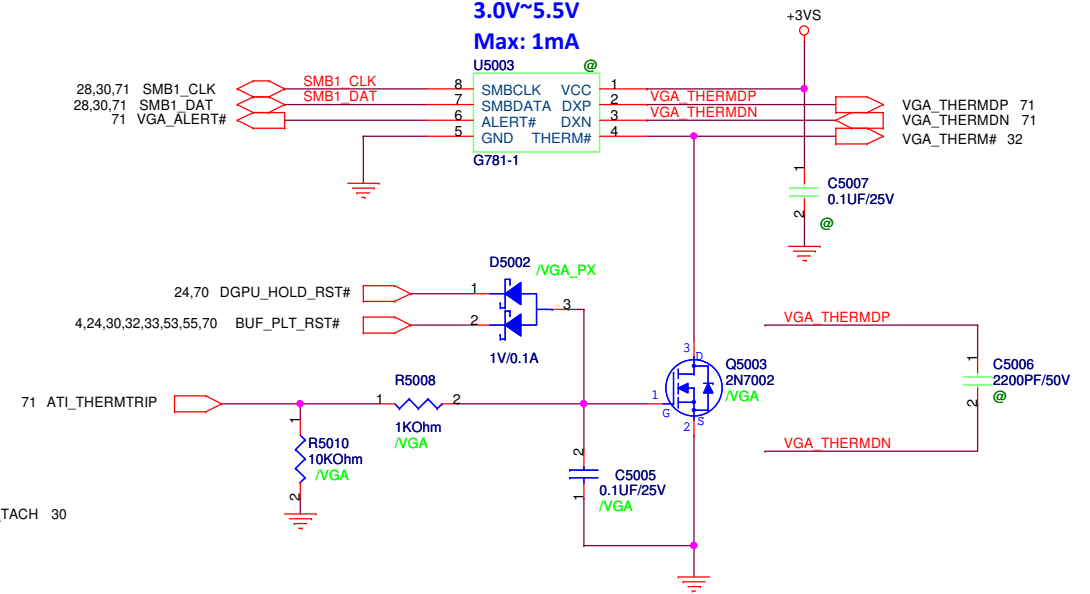


U5001 Close to CPU

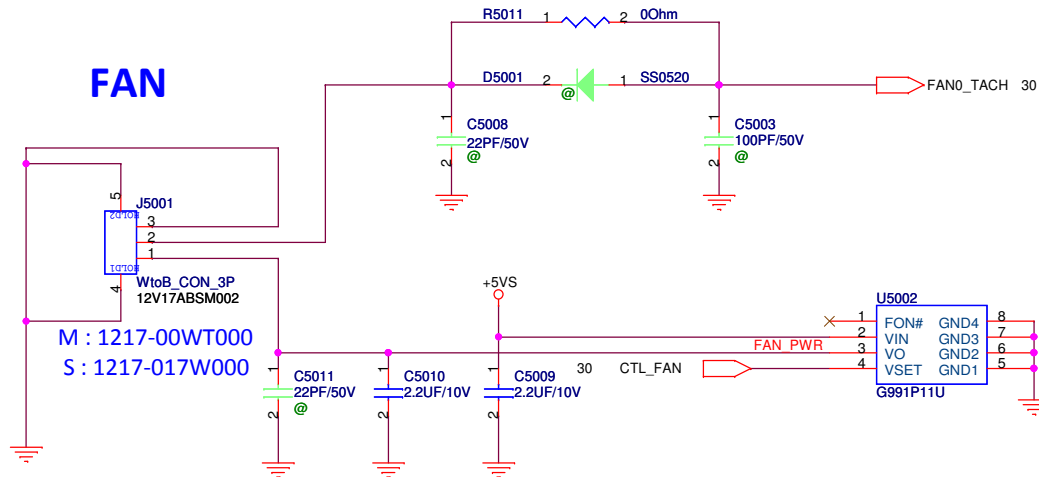


U5003 Close to GPU

3.0V~5.5V
Max: 1mA



FAN

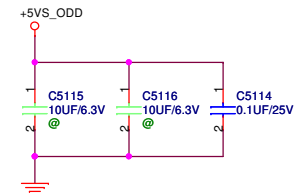


| PEGATRON | | Title : FAN / Thermal Sensor | |
|---------------------------------|--------------|-------------------------------|--------|
| Size | | Engineer: Peter5 Huang | |
| Custom | Project Name | PLFG | Rev |
| Date: Monday, February 13, 2012 | Sheet | 50 | of 104 |



ODD

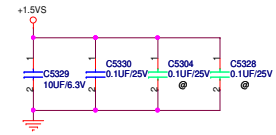
support Hokey turn off ODD power



WLAN

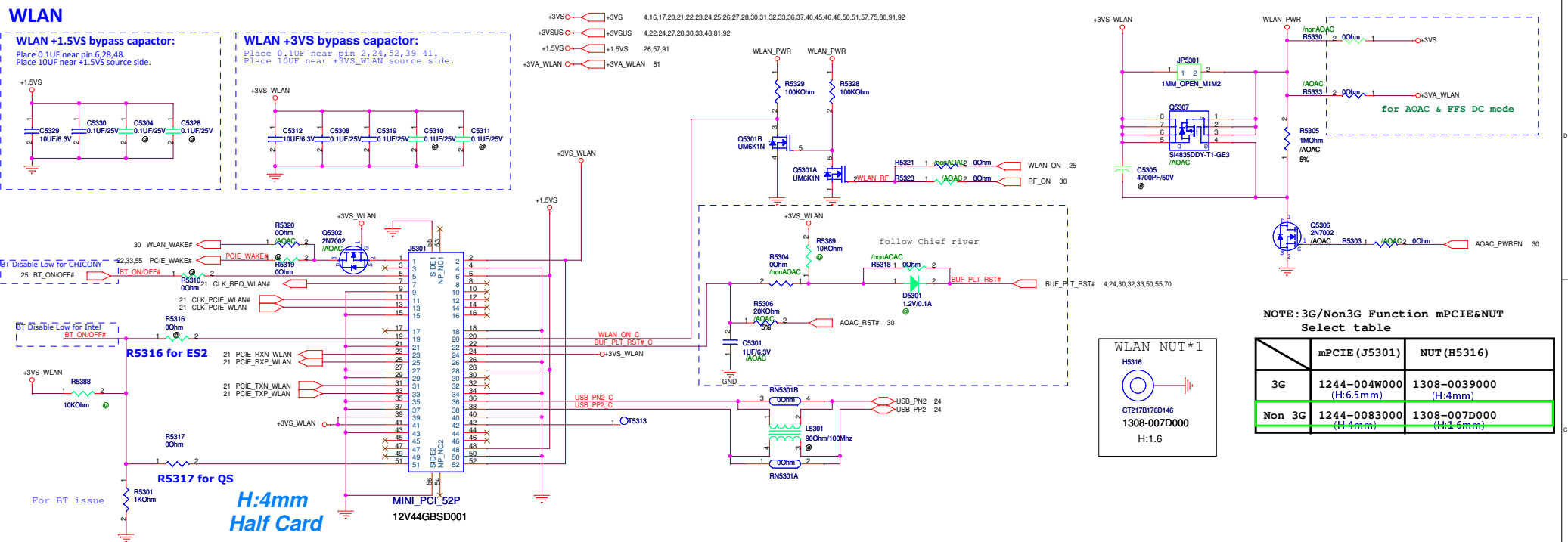
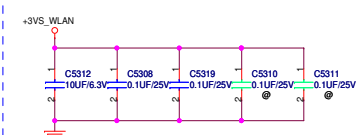
WLAN +1.5VS bypass capactor:

Place 0.1UF near pin 6,28,48.
Place 10UF near +1.5VS source side.

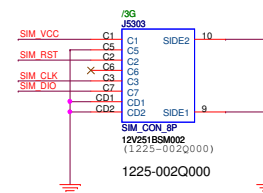
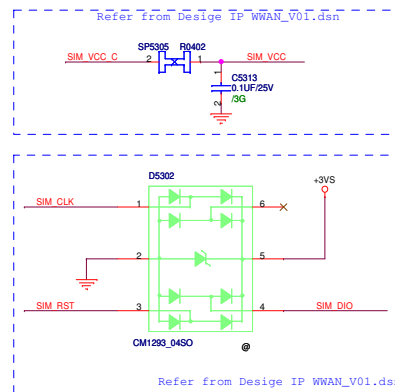
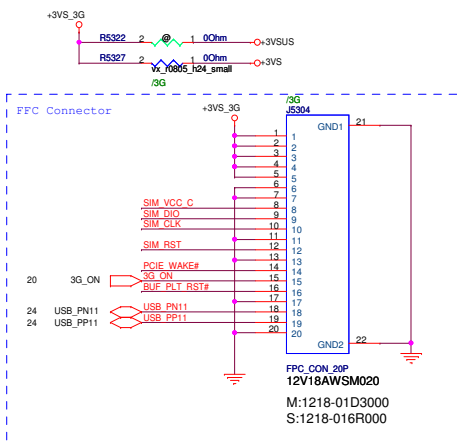


WLAN +3VS bypass capactor:

Place 0.1UF near pin 2,24,52,39 41.
Place 10UF near +3VS_WLAN source side.

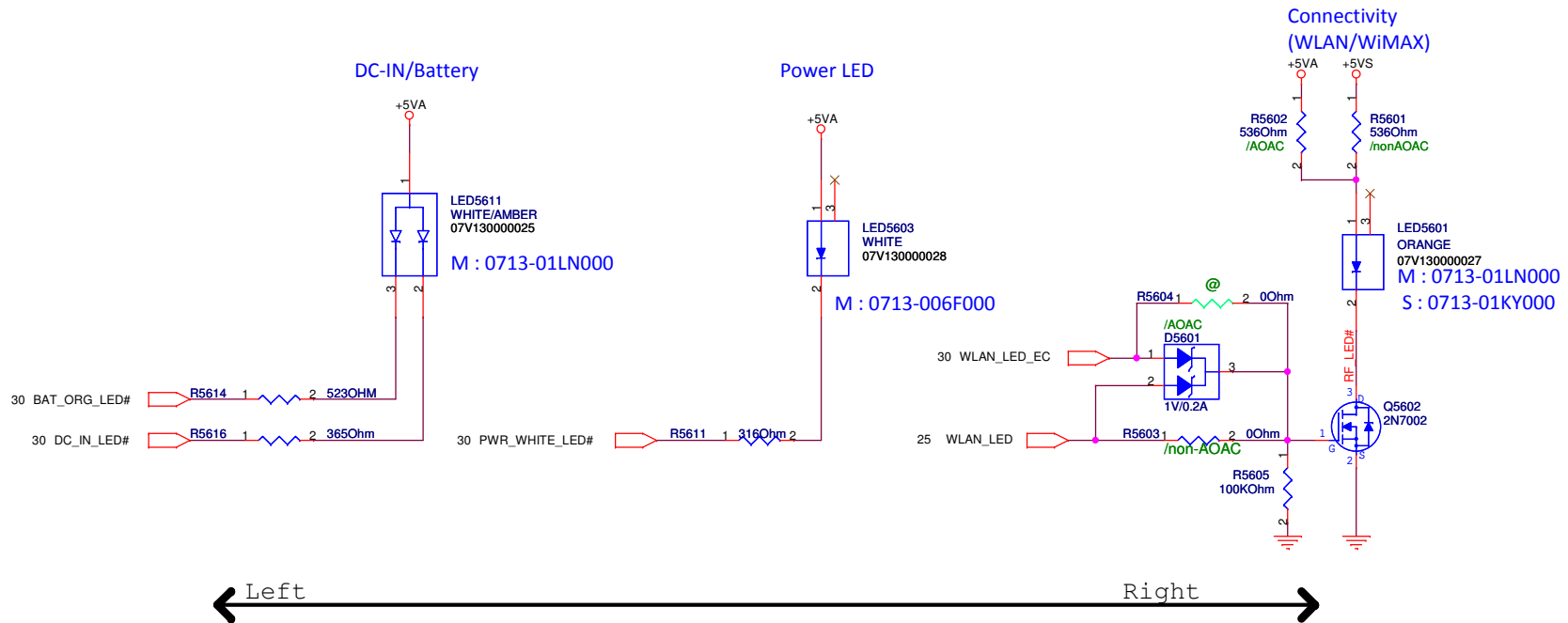


3G

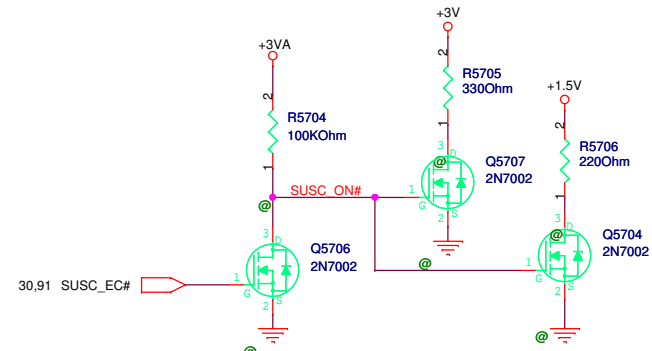
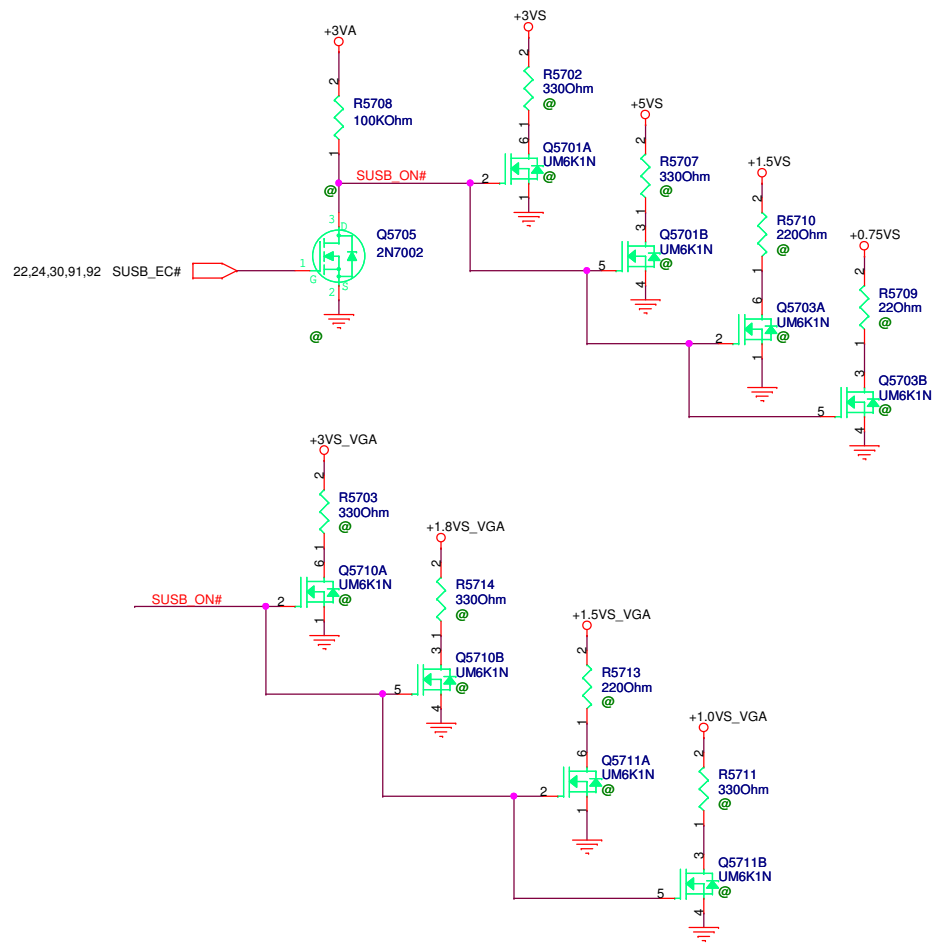


Order of Indicator LEDs

DC-IN/Battery Power WiFi

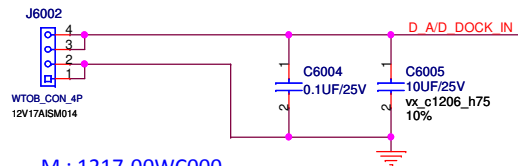
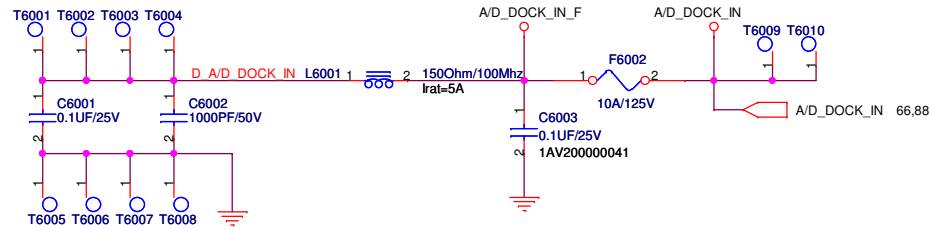


Discharge Circuit



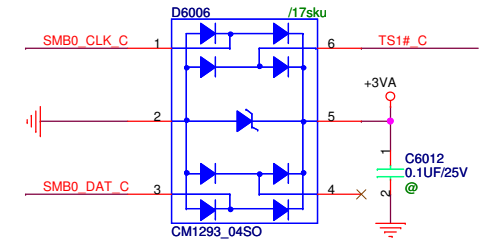
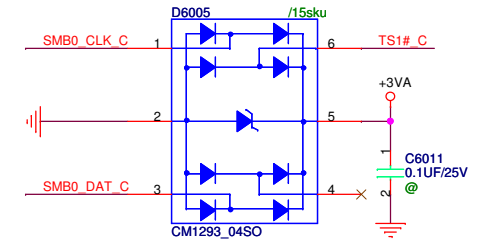
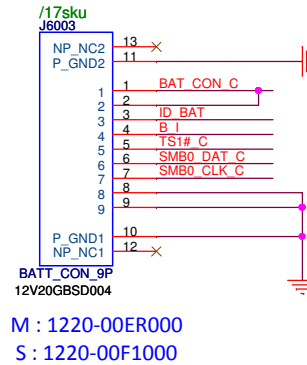
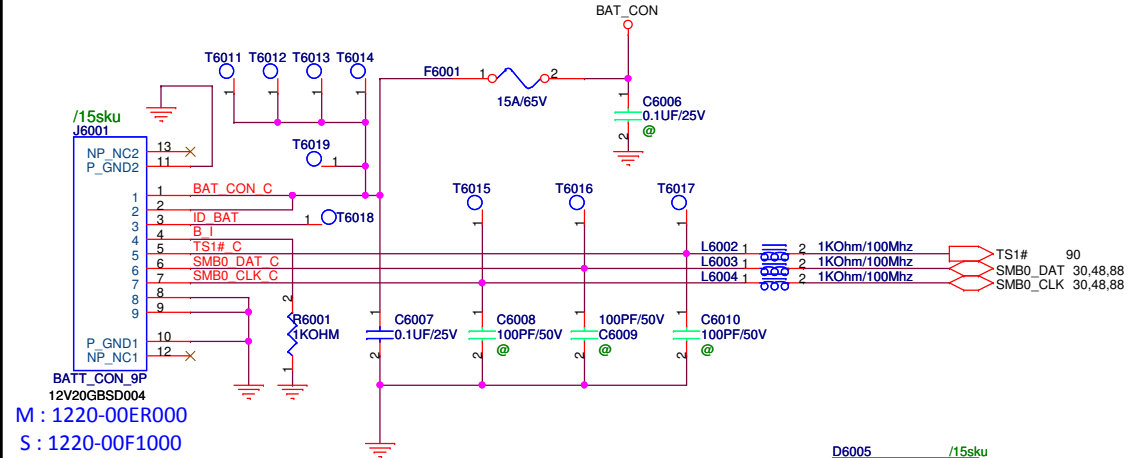
| | | | |
|---------------------------------|-----------------------------|--------------------------|------------|
| PEGATRON | | Title : DC-IN/ DISCHARGE | |
| BG1-CSC-HW R&D Dept.5 | | Engineer: Ahren_chen | |
| Size B | Project Name PLFG | | Rev 2.1 |
| Date: Monday, February 13, 2012 | | Sheet | 57 of 104 |

DC IN



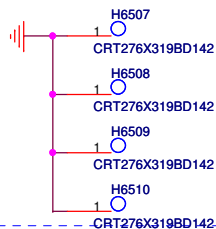
M : 1217-00WC000
S : 1208-01C1000

Battery Connector

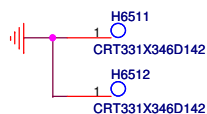


| PEGATRON | | Title : DC-IN/ DISCHARGE | |
|---------------------------------|----------------------|--------------------------|------------|
| BG1-CSC-HW R&D Dept.5 | | Engineer: Ahren_chen | |
| Size B | Project Name PLFG | | Rev 2.1 |
| Date: Monday, February 13, 2012 | | Sheet 60 | of 104 |

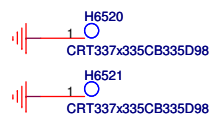
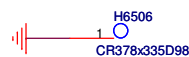
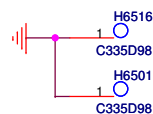
CPU : Screw Ex4
DXF : DETAIL A



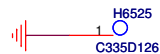
VGA : Screw Fx2
DXF : DETAIL B



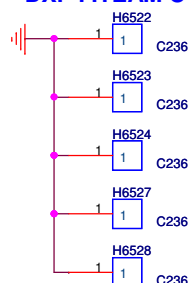
PCB : Screw Ax10
DXF : ITEAM A



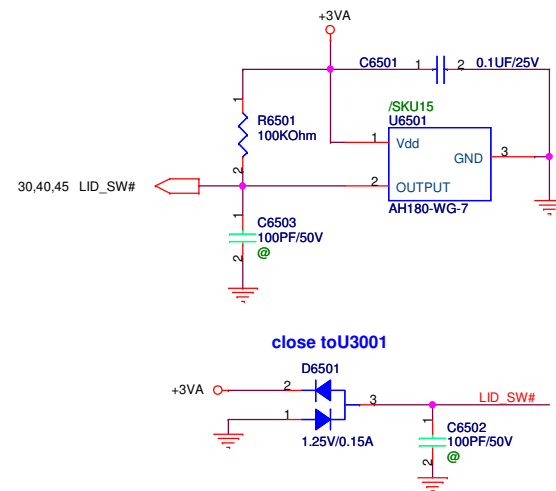
Locate : Screw Dx1
DXF : ITEAM D



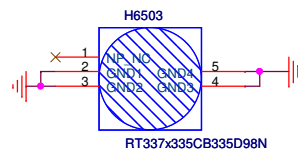
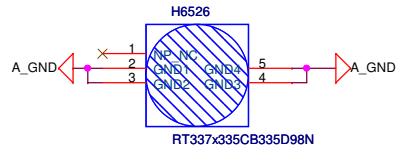
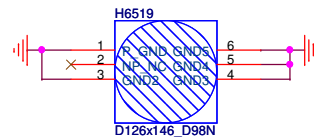
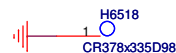
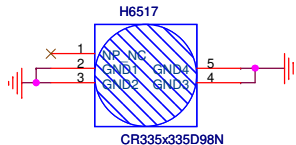
TOP/BOT : GND Cx5
DXF : ITEAM C



LID Switch(Hall sensor)

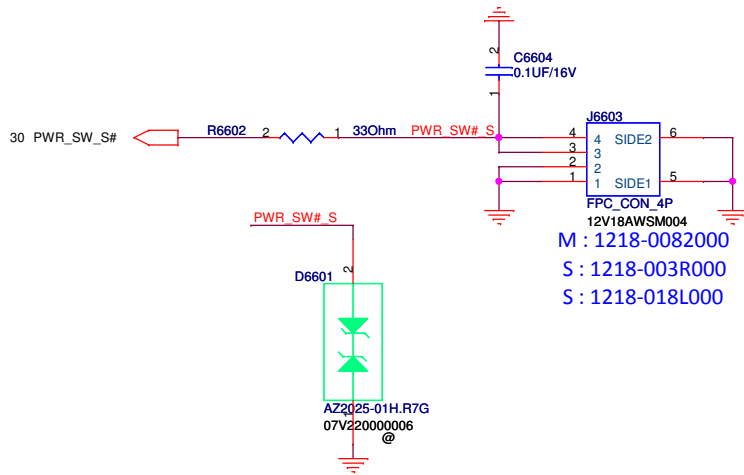


Note:
LID_SW# is easy to cause high voltage damage when plugging inverter board connector to M/B with AC present. Need to add bidirectional diode to protect this pin.

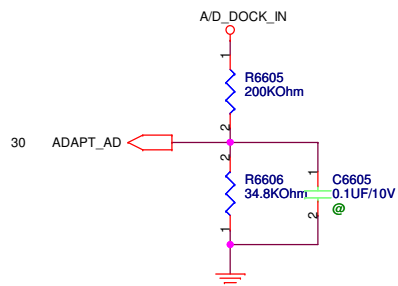


| | | | |
|--|--|--------------------------------|--|
| PEGATRON | | Title ME_CONN,Skew Hole | |
| Size B | | Engineer: Ahren_chen | |
| Project Name PLFG | | Rev 2.1 | |
| Date: Monday, February 13, 2012 | | Sheet 65 of 104 | |

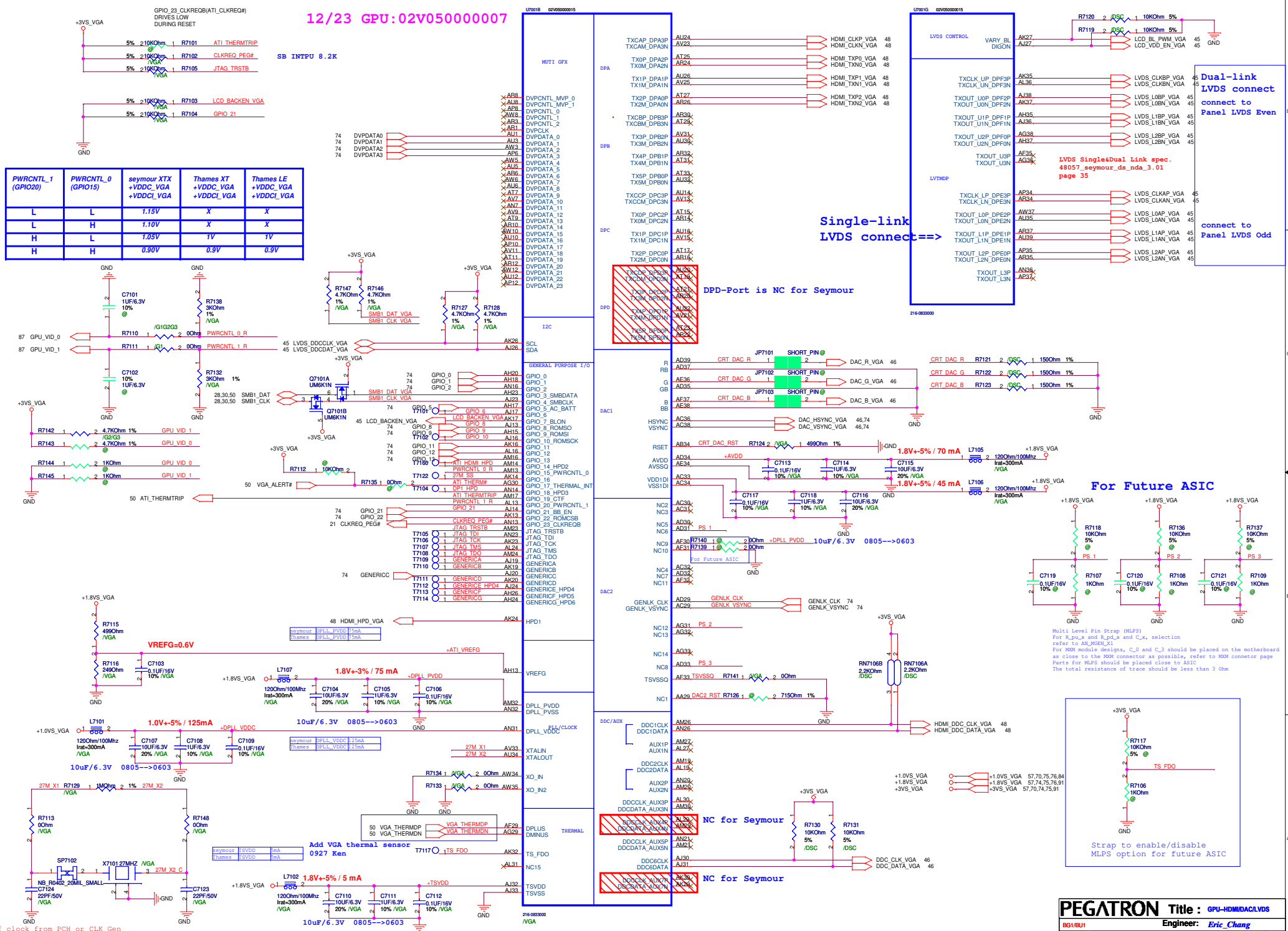
PWR BRD



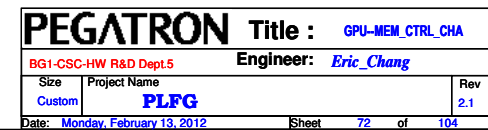
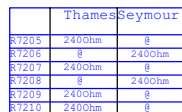
ADAPTOR VOLTAGE DETECTOR.



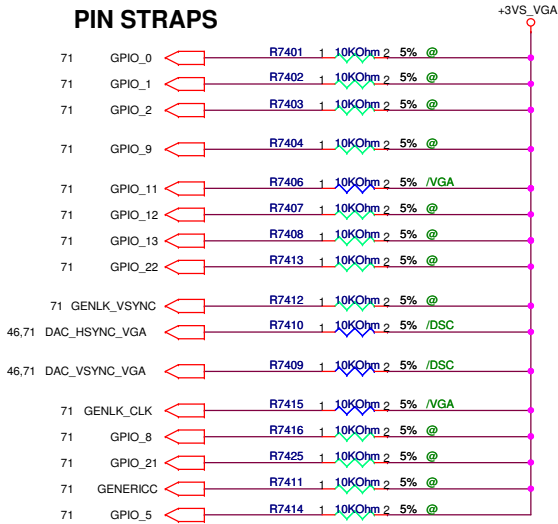
| | | | |
|--|-----------------------------|-------------------------------|------------|
| PEGATRON | | Title : PEW BRD/IO BRD | |
| BG1-CSC-HW R&D Dept.5 | | Engineer: Ahren_chen | |
| Size B | Project Name PLFG | | Rev 2.1 |
| Date: Monday, February 13, 2012 | | Sheet 66 of 104 | |



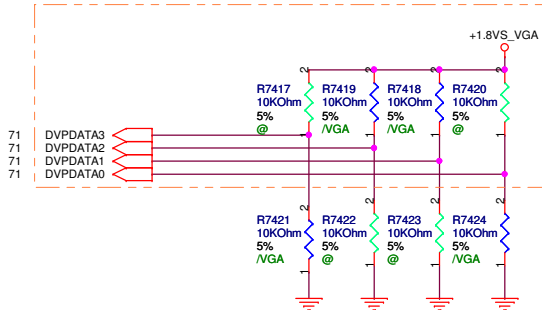
If clock from PCH or CLK Gen then 27M_X1, 27M_X2 must to GND(C7123, C7123 are 0 ohm)
If clock from X7101 then C7123, C7123 are 22pF



PIN STRAPS



VRAM size define by VBIOS



| STRAPS | PIN | DESCRIPTION |
|--|--|--|
| TX_PWRS_ENB (Internal PD) | GPIO0 | Transmitter Power Savings Enable ▼ 0= 50% Tx output swing 1= Full Tx output swing |
| TX_DEEMPH_EN (Internal PD) | GPIO1 | Transmitter De-emphasis Enable ▼ 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled |
| BIF_GEN3_EN_A (Default = 0) | GPIO2 | PCIe Gen3 Enable(NOTE: RESERVED for Thames/Whistler/Seymour) ▼ 0: GEN3 not supported at power-on 1: VGA controller capacity disabled (for multi-GPU) |
| GPIO_5_AC_BATT (PD-reset) | GPIO5 (no use) | GPIO_5_AC_BATT is an input which allows the system to request (AC) performance mode or battery mode operation. ▼ 0 = Battery saving mode 1 = AC (Performance mode) |
| BIF_VGA_DIS (Internal PD) | GPIO9 | VGA Control ▼ 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU) |
| ROMIDCFG[2:0] (Internal PD) | GPIO[13:11] | if BIOS_ROM_EN=1,then Config[2:0] defines the ROM type ▼ if BIOS_ROM_EN=0,then Config[2:0] defines the primary memory aperture size |
| BIOS_ROM_EN (Internal PD) | GPIO22 | Enable external BIOS ROM device ▼ 0= Disable external BIOS ROM device 1= Enable external BIOS ROM device |
| AUD[1] AUD[0] (Internal PD) | HSYNC VSYNC | AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if adapter is detected; 11 - Audio for both DisplayPort and HDMI. ▼ HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature. |
| CEC_DIS (Internal PD) | GENLK_VSYNC | Enable CEC function. Reserved for Thames/Whistler/Seymour 1: Enabled ▼ 0: Disabled |
| RESERVED RESERVED RESERVED RESERVED | GENLK_CLK GPIO8 GPIO21 GENERICC | RESERVED RESERVED RESERVED RESERVED (for Thames/Whistler/Seymour only) |

| AMD RESERVED CONFIGURATION STRAPS | | | | |
|--|--|---------------------------|--|---------------------------------|
| ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET | | | | |
| GPIO_21_BB_EN | DAC2_V2SYNC | GENERICC | GPIO_8_ROMSO | GPIO_2 |
| If BIOS_ROM_EN (GPIO22) = 0 | | | | |
| If BIOS_ROM_EN (GPIO22) = 1 | | | | |
| Size of the primary memory apertures | GPIO[13:11] | Manufacturer | Part Number | GPIO[13:11] |
| ▼ 128MB 256MB 64MB 32MB 512MB 1GB 2GB 4GB | 000 001 010 Not Supported Not Supported Not Supported Not Supported Not Supported | ST Microelectronics | M25P05A M25P10A M25P20 M25P40 M25P80 | 100 101 101 101 101 |
| | | Chingis (formerly PMC) | Pm25LV512A Pm25LV010A | 100 101 |

Memory ID Board Straps

| Vendor | DVPDATA(3,2,1,0) | ID | DDR3 Memory Type | VRAM Vendor Part |
|---------|------------------|----|--------------------|----------------------------|
| Hynix | 0000 | 0 | 128M*16*8 pcs(2GB) | H5TQ2G63BFR-11C (1800Mbps) |
| | 0001 | 1 | 128M*16*8 pcs(2GB) | H5TQ2G63DFR-11C (1800Mbps) |
| | 0010 | 2 | | |
| | 0011 | 3 | | |
| | 0100 | 4 | 64M*16*8 pcs(1GB) | H5TQ1G63DFR-11C (1800Mbps) |
| Samsung | 0101 | 5 | | |
| | 0110 | 6 | 128M*16*8 pcs(2GB) | K4W2G1646C-HC11 (1866Mbps) |
| | 0111 | 7 | | |
| | 1000 | 8 | 64M*16*8 pcs(1GB) | K4W1G1646G-BC11 (1866Mbps) |
| | 1001 | 9 | | |
| AMD | 1010 | 10 | 128M*16*8 pcs(2GB) | 23EY4187MA11 (1800Mbps) |
| | 1011 | 11 | | |
| | 1100 | 12 | 64M*16*8 pcs(1GB) | 23EY2387MC11 (1800Mbps) |
| | 1101 | 13 | | |

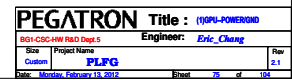
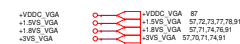
2011/9/6 Not yet Qualification in AMD

+1.8VS_VGA
+3VS_VGA

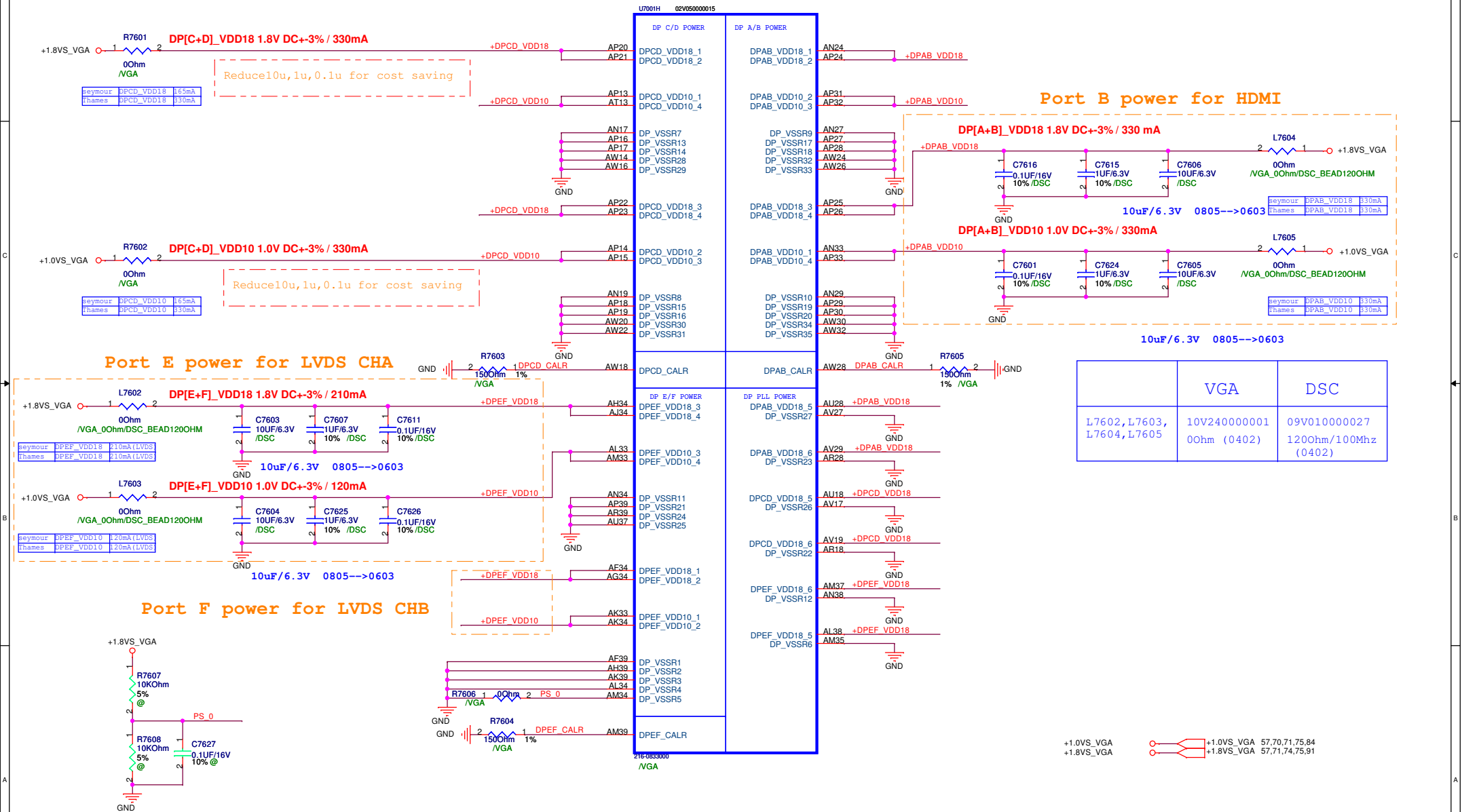
+1.8VS_VGA 57,71,75,76,91
+3VS_VGA 57,70,71,75,91

| PEGATRON Title : GPU-STRAP_MISC | | | |
|---------------------------------|--------------|----------------------|--------|
| BG1-CSC-HW R&D Dept.5 | | Engineer: Eric_Chang | |
| Size | Project Name | | Rev |
| Custom | PLFG | | 2.1 |
| Date: Monday, February 13, 2012 | Sheet | 74 | of 104 |

```
Power Rail spec. ref
48057_seymour_ds_nda_3.01
49385_thames_ds_nda_1.01
```

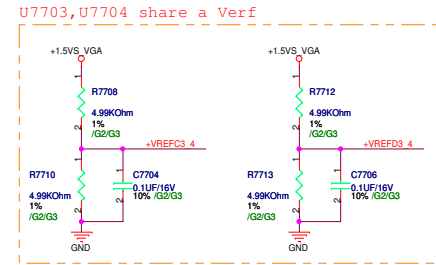
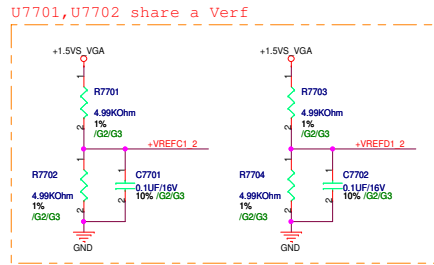
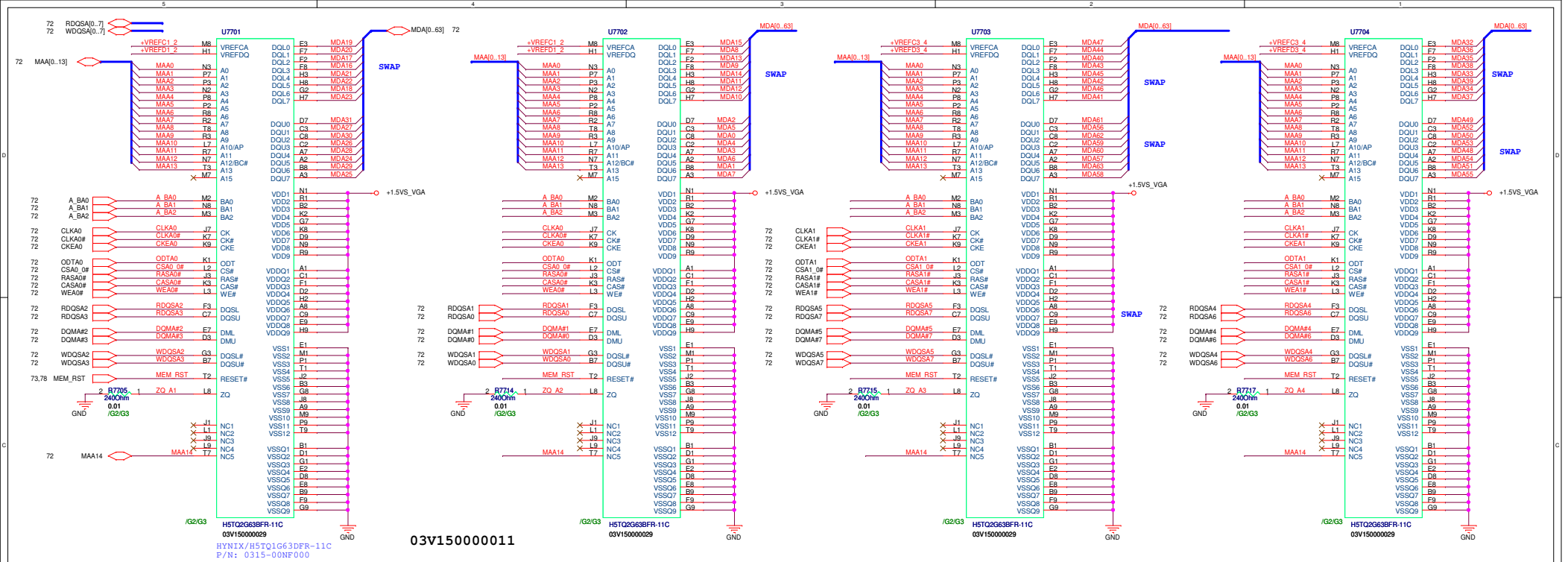


```
Power Rail spec. ref
48057_seymour_ds_nda_3.01
49385_thames_ds_nda_1.01
```

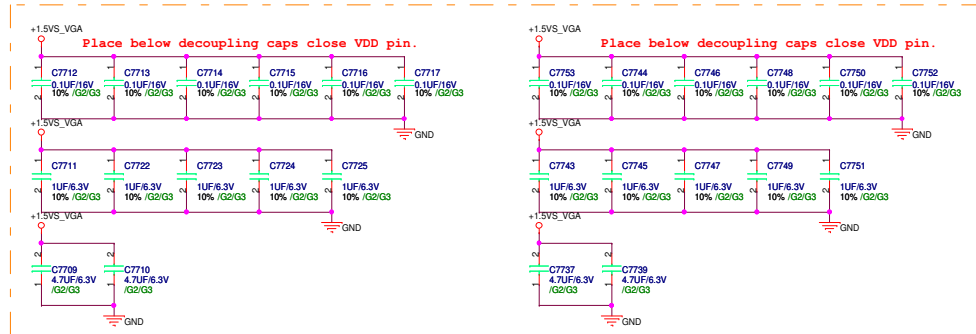


| | VGA | DSC |
|-------------------------------|-----------------------------|---|
| L7602, L7603, L7604, L7605 | 10V240000001 00hm (0402) | 09V010000027 1200hm/100Mhz (0402) |

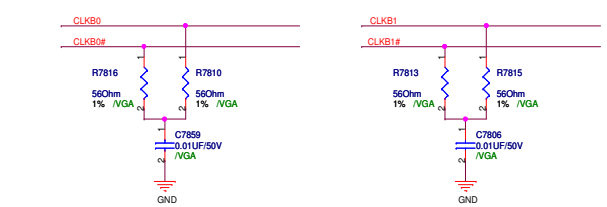
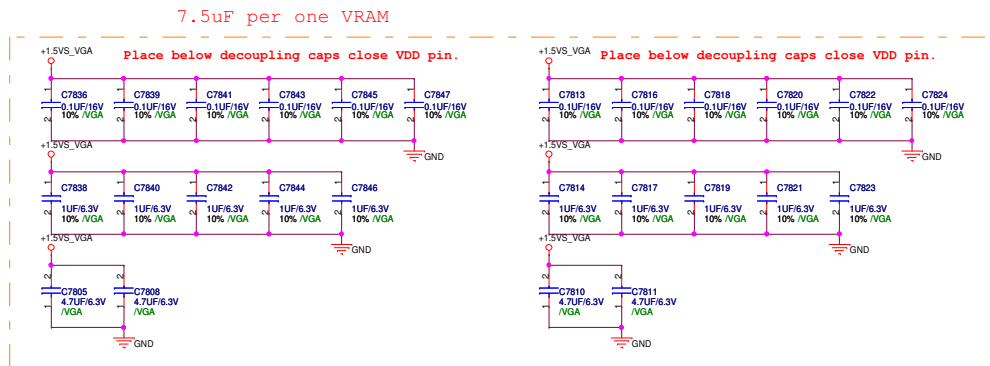
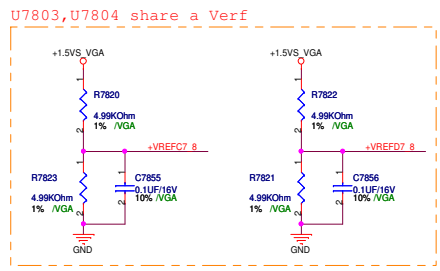
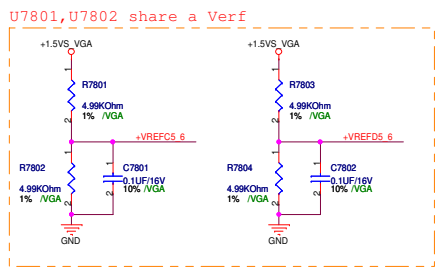
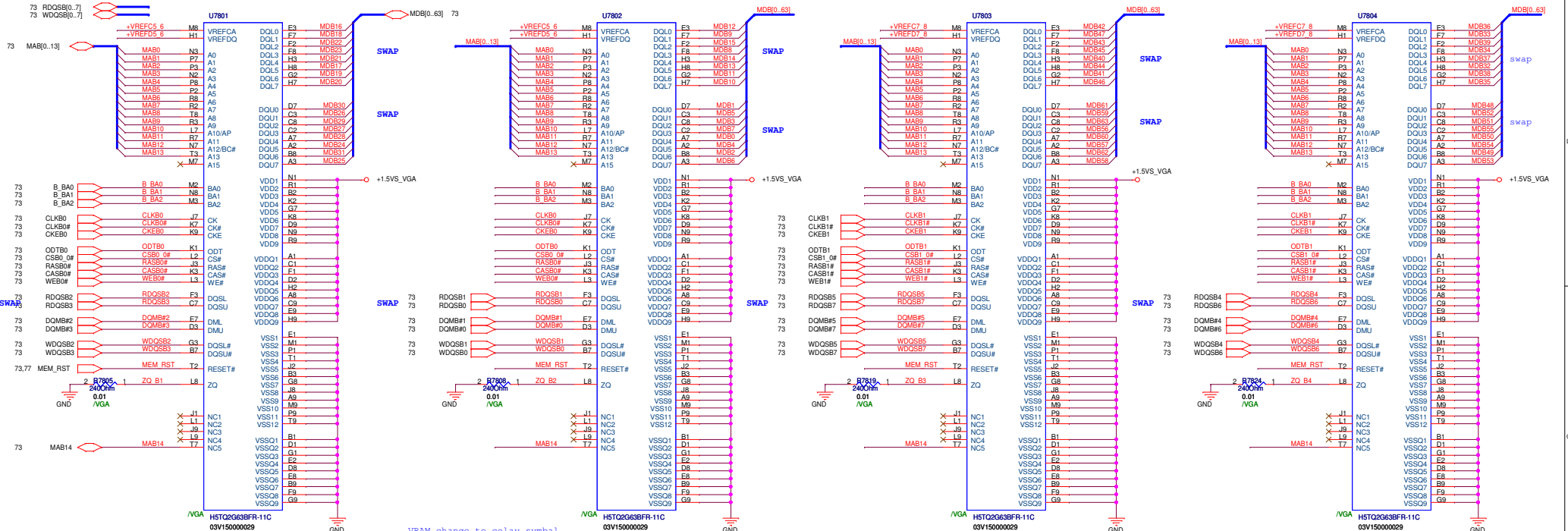
| | | | |
|------------|---|------------|----------------|
| +1.0VS_VGA |  | +1.0VS_VGA | 57,70,71,75,84 |
| +1.8VS_VGA | | +1.8VS_VGA | 57,71,74,75,91 |



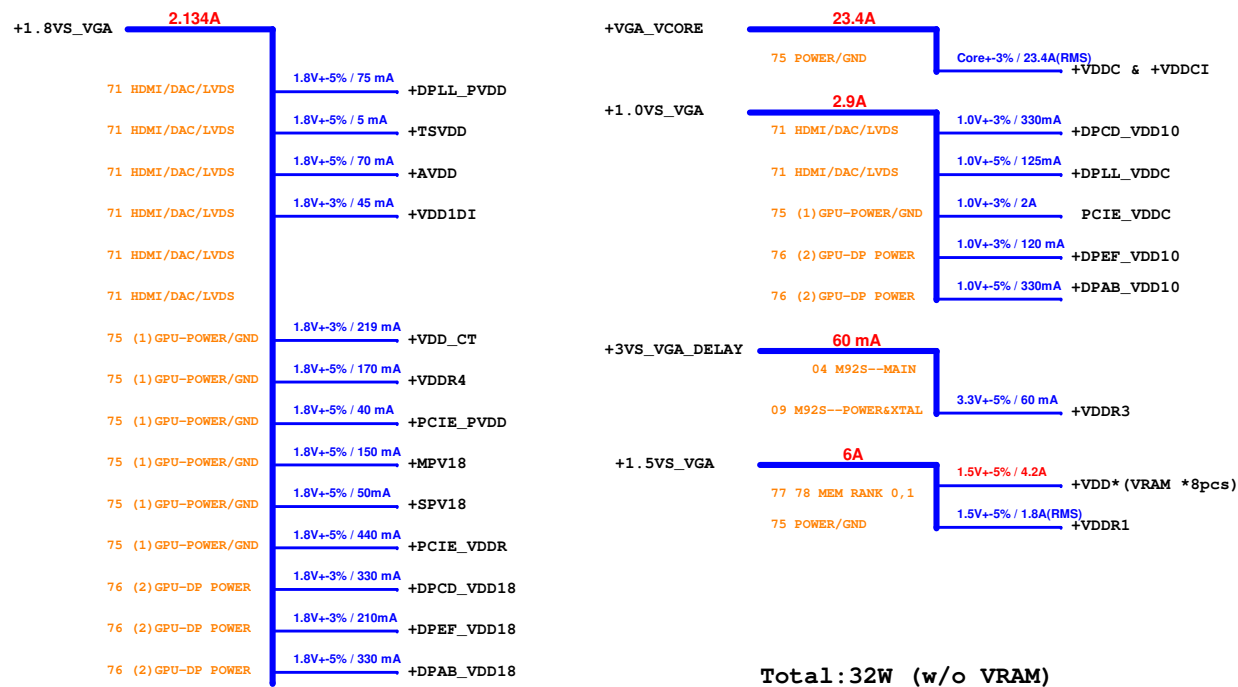
7.5uF per one VRAM



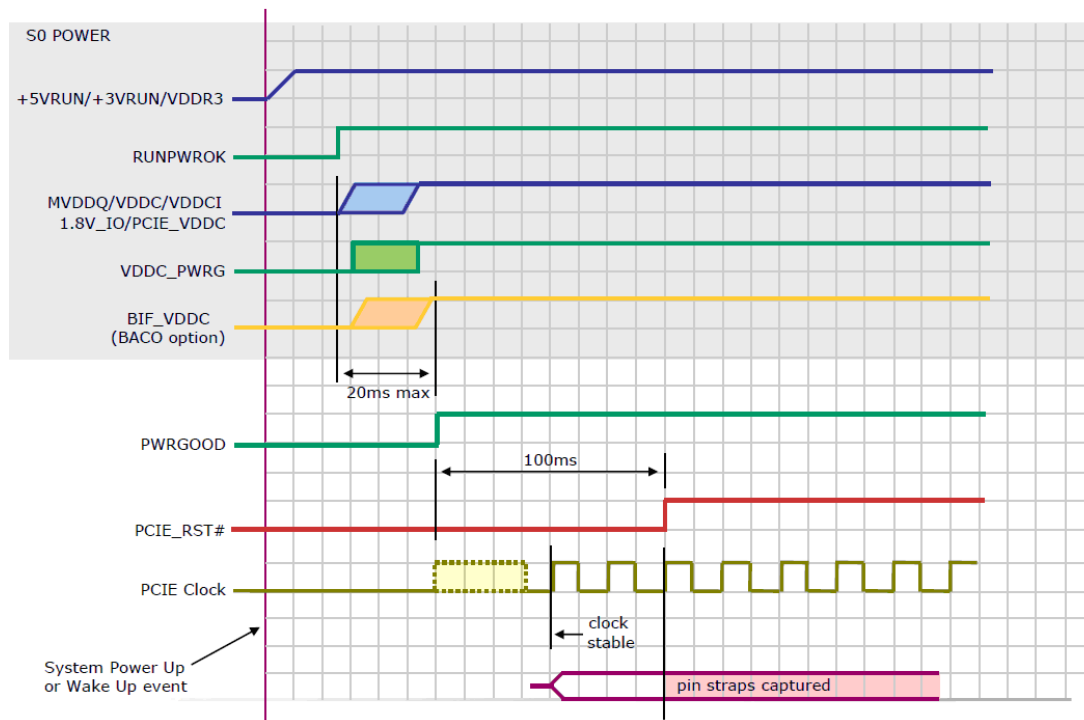
"Seymour"-M2 uses memory group B only. (DataBook Page28)



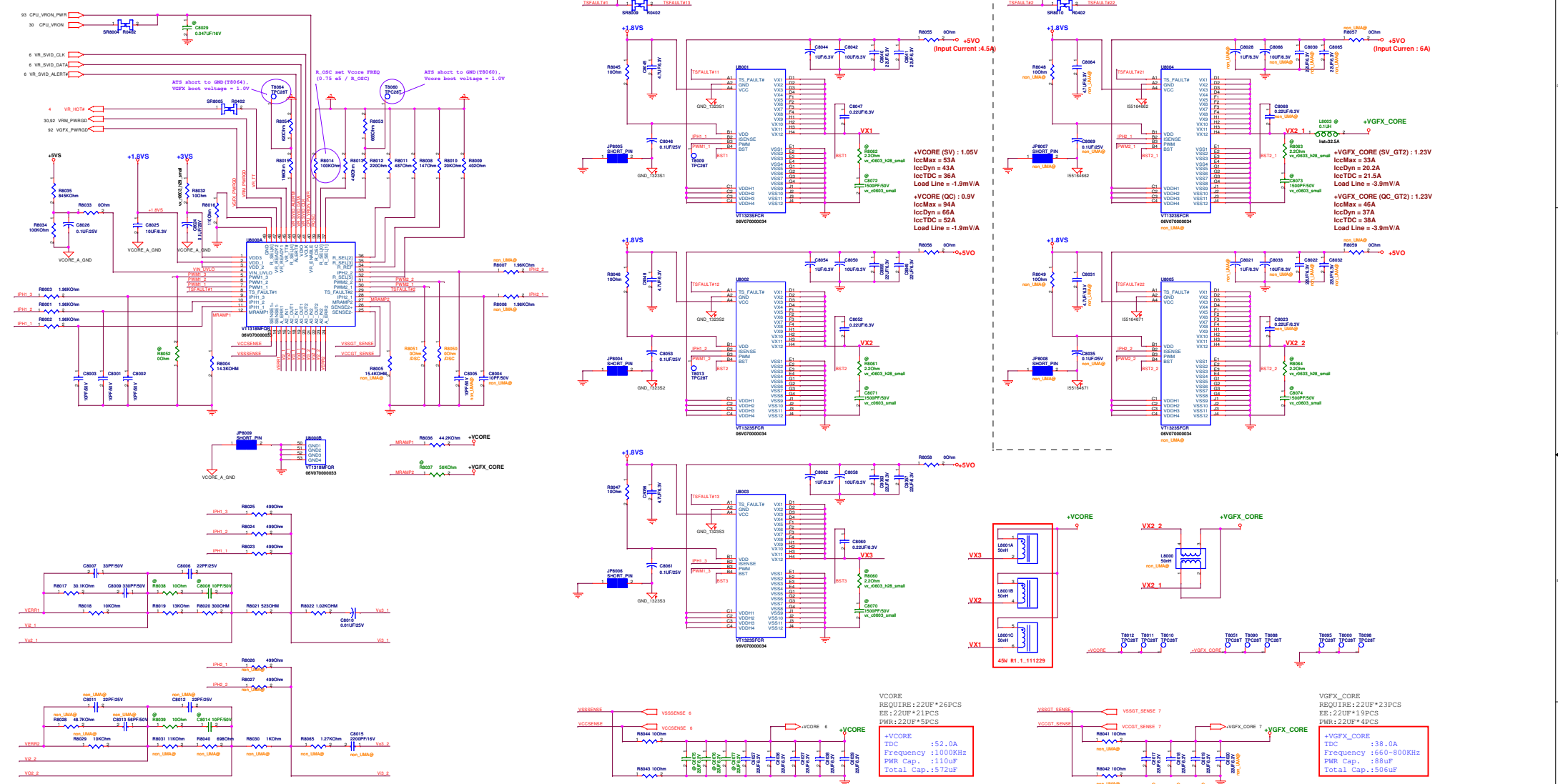
+1.5VS_VGA 57.72,73,75,77,91



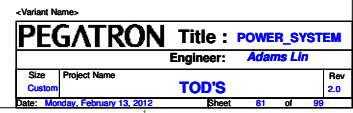
POWER UP RESET SEQUENCE – THAMES



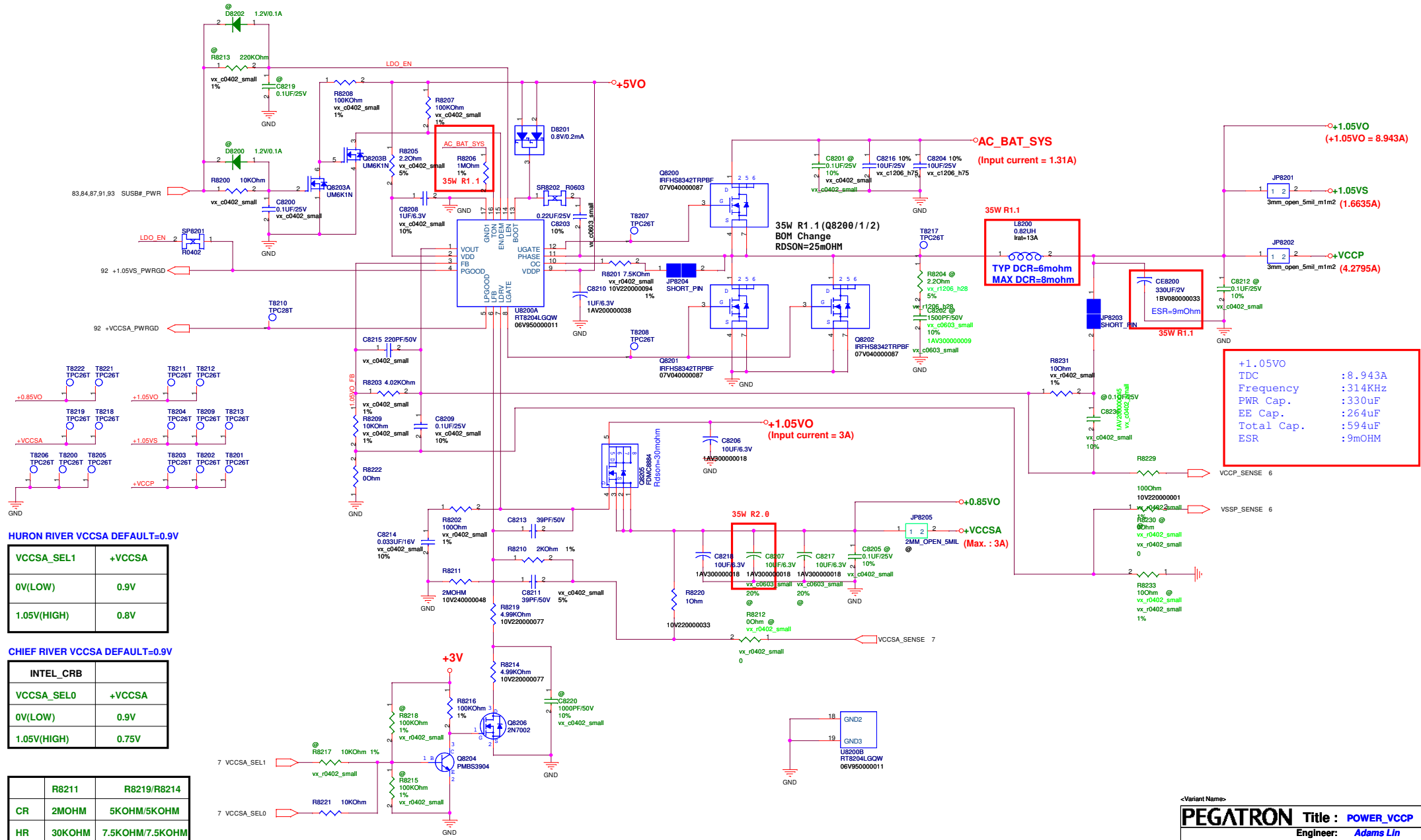
Chief River_+VCORE & +VGFX_CORE PPWER SUPPLY



Support ACOC => AOAC_@ 上件, nonAOAC_@ 不上件
nonsupport AOAC => nonAOAC_@上件, AOAC_@ 不上件



VCCP & VCCSA POWER SUPPLY

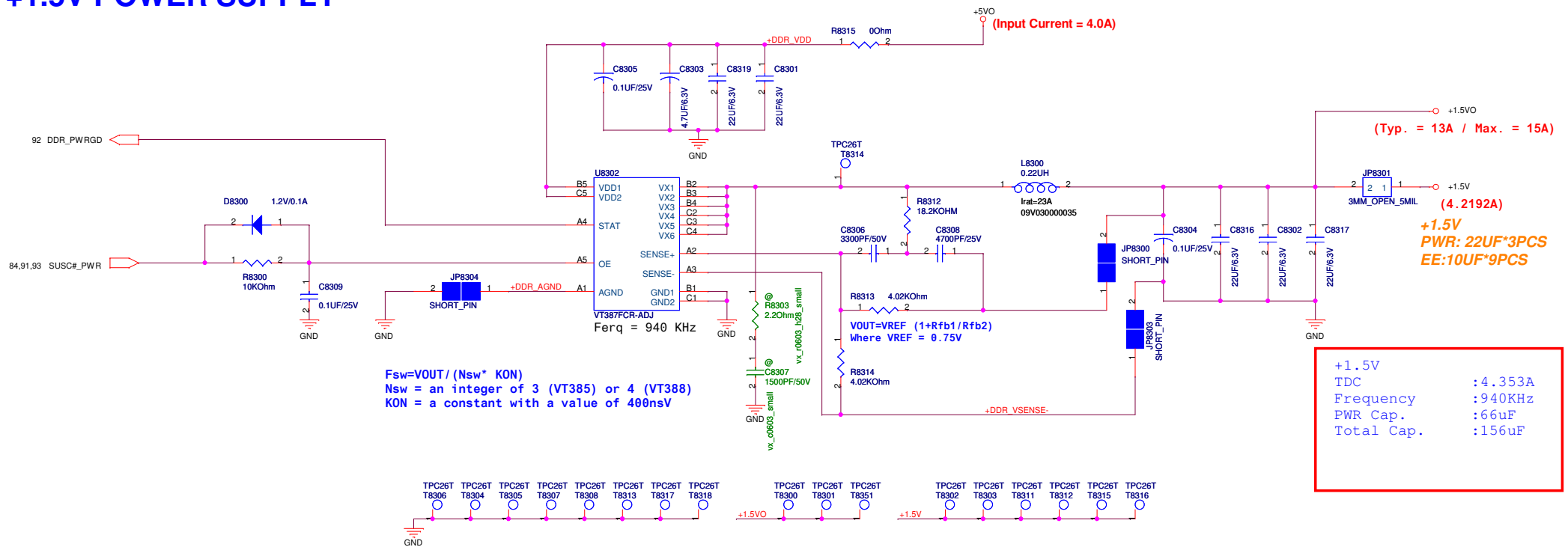


<Variant Name>

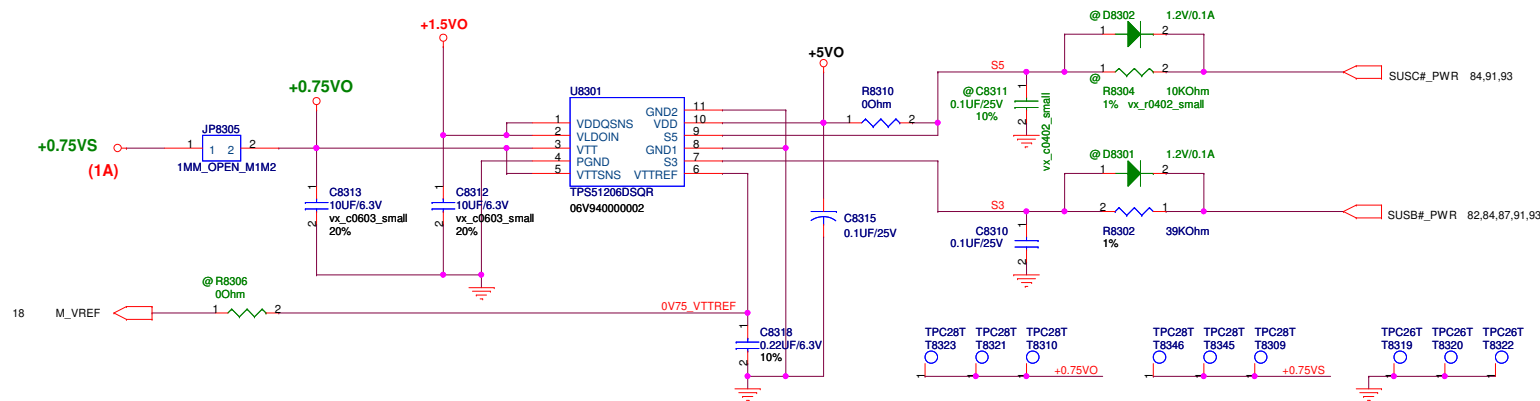
PEGATRON Title : POWER_VCCP

| | |
|--|------------------------------|
| Engineer: Adams Lin | |
| Size Custom | Project Name TOD'S |
| Date: Monday, February 13, 2012 | Sheet 82 of 99 |

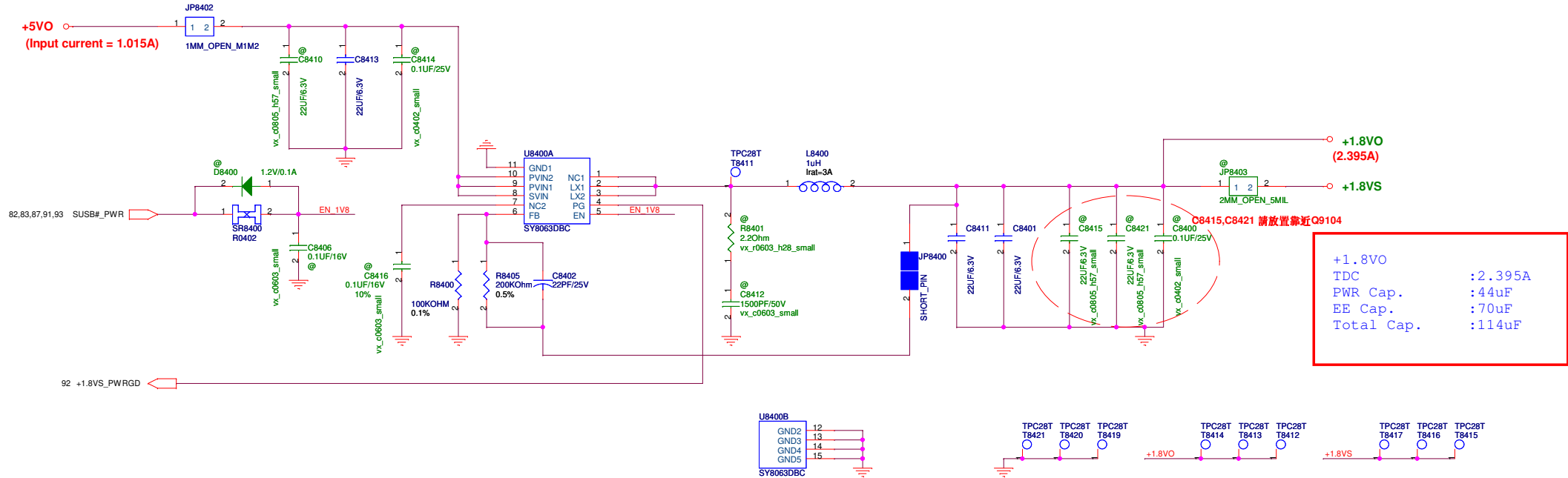
+1.5V POWER SUPPLY



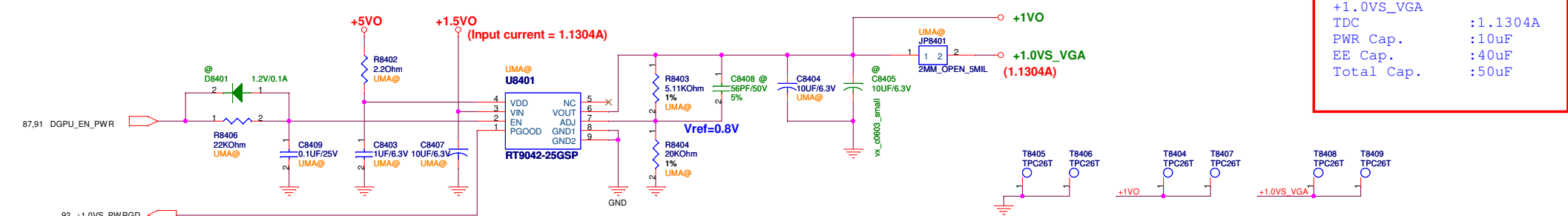
+0.75VS POWER SUPPLY



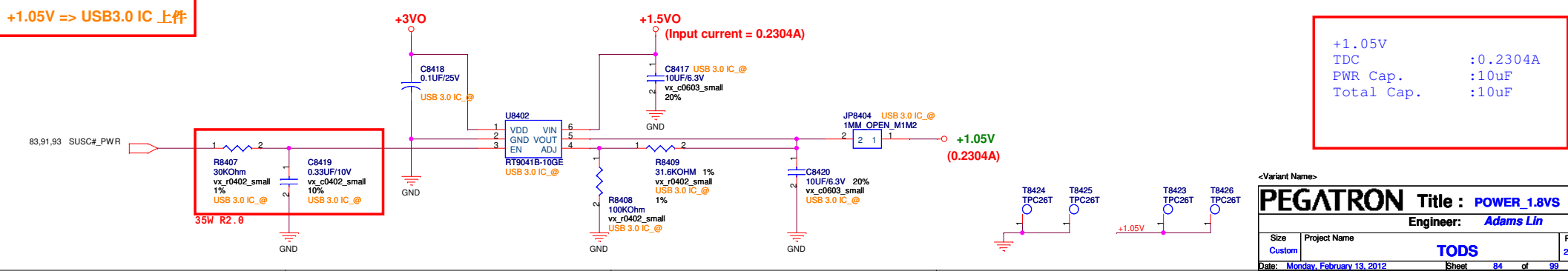
1.8VS POWER SUPPLY

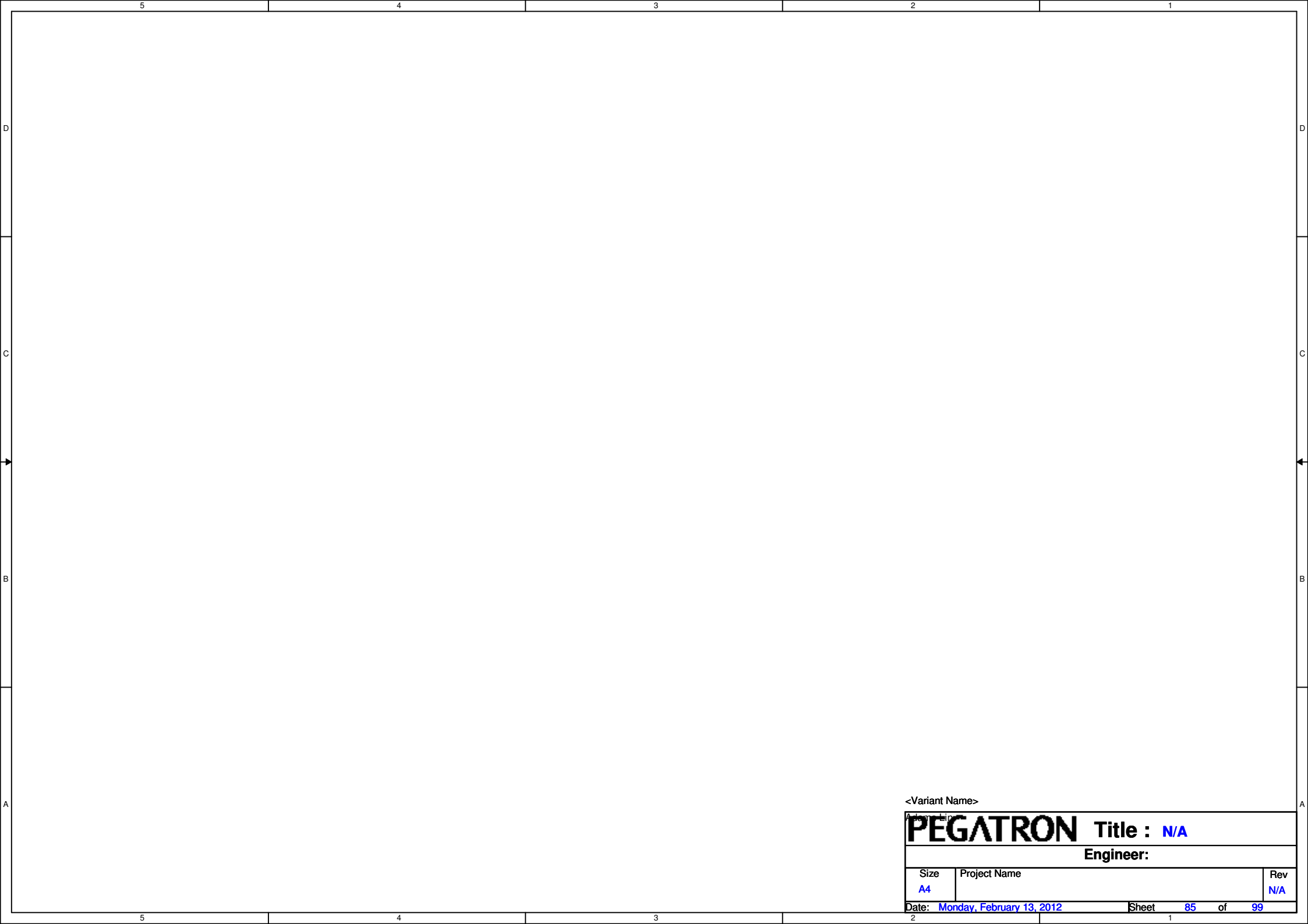


1VS_VGA POWER SUPPLY

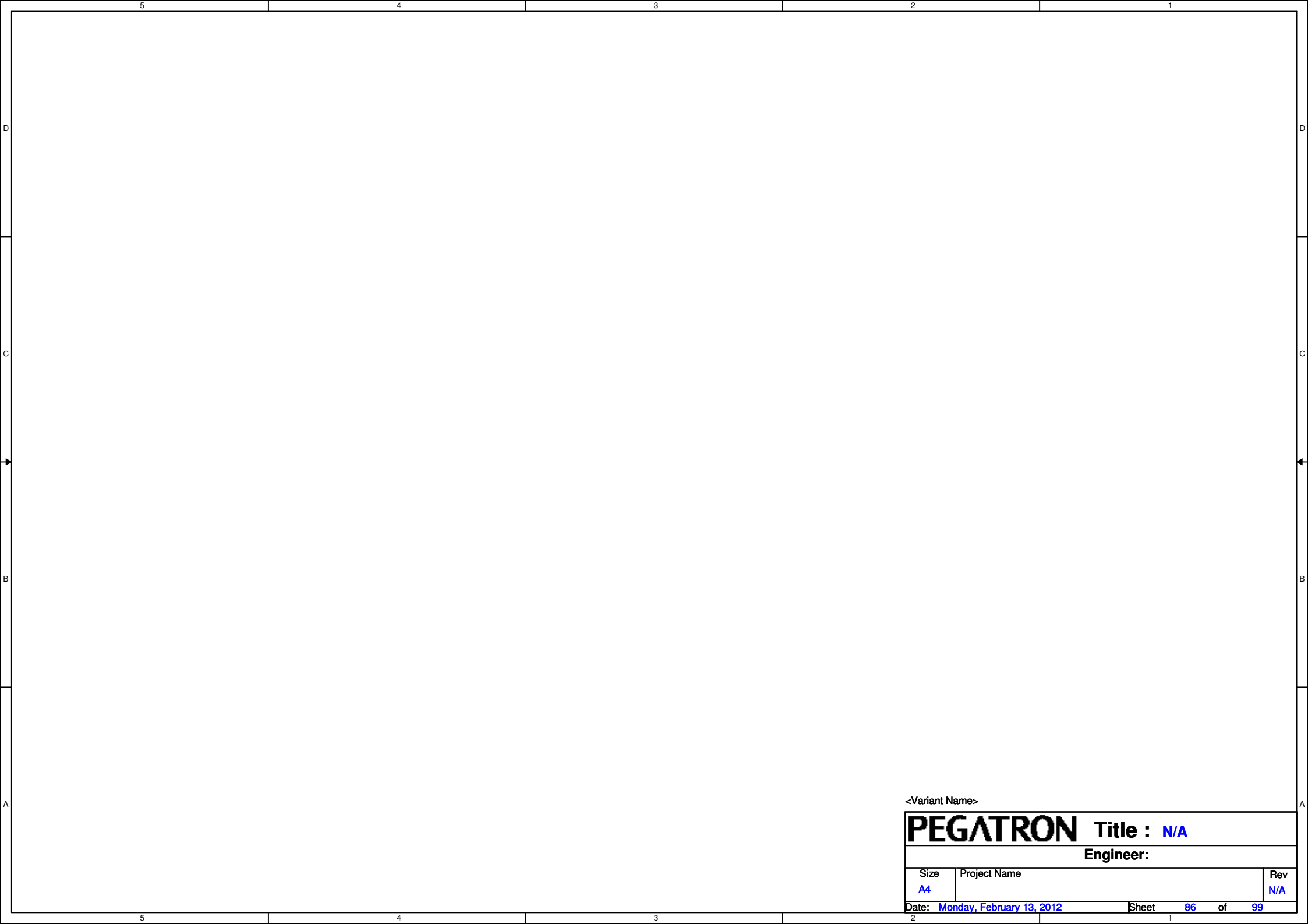


1.05V POWER SUPPLY



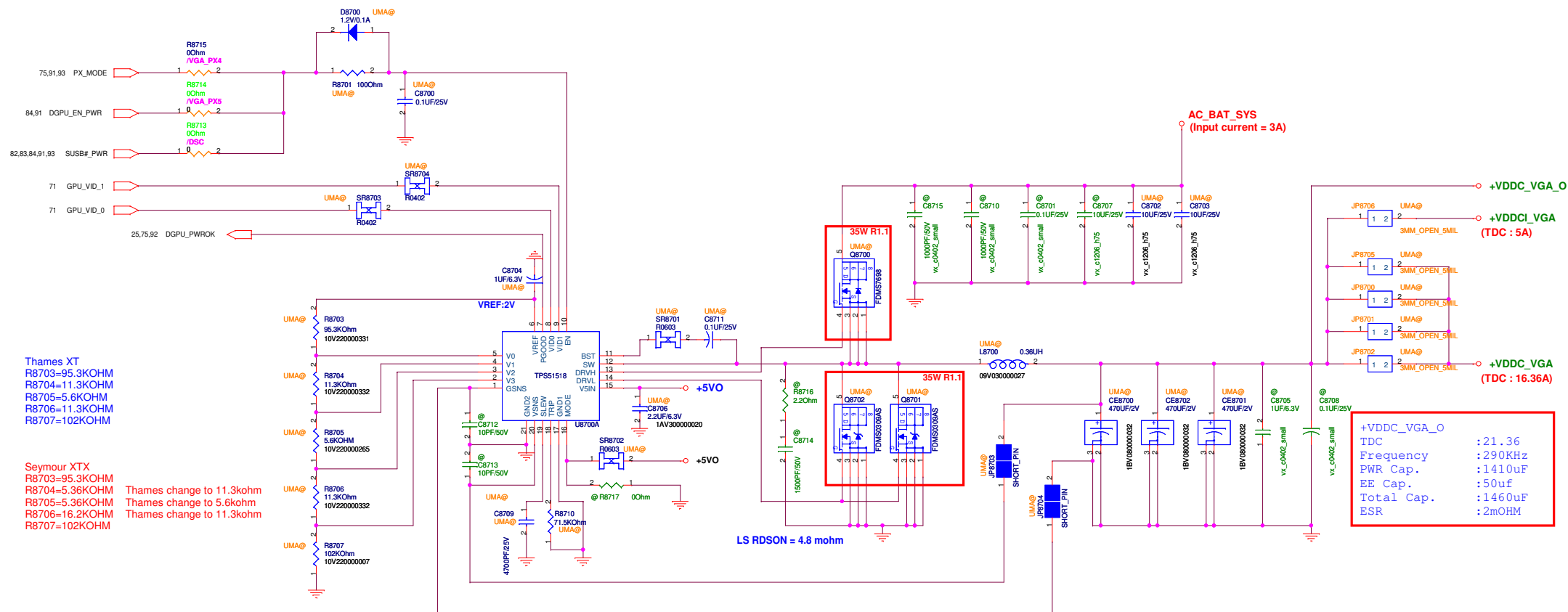


| | | |
|----------------|---------------------------|----------------|
| <Variant Name> | | |
| A4 | | |
| PEGATRON | | |
| Title : N/A | | |
| Engineer: | | |
| Size | Project Name | Rev |
| A4 | | N/A |
| Date: | Monday, February 13, 2012 | Sheet 85 of 99 |



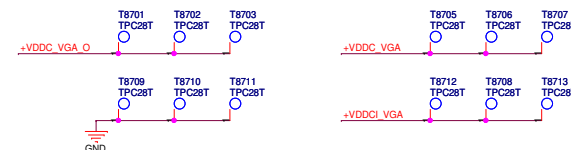
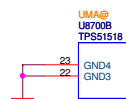
| | | |
|--|------------------------------|-------------------|
| <Variant Name> | | |
| PEGATRON Title : N/A | | |
| Engineer: | | |
| Size A4 | Project Name | Rev N/A |
| Date: Monday, February 13, 2012 | Sheet 86 of 99 | |

+VDDC_VGA POWER SUPPLY

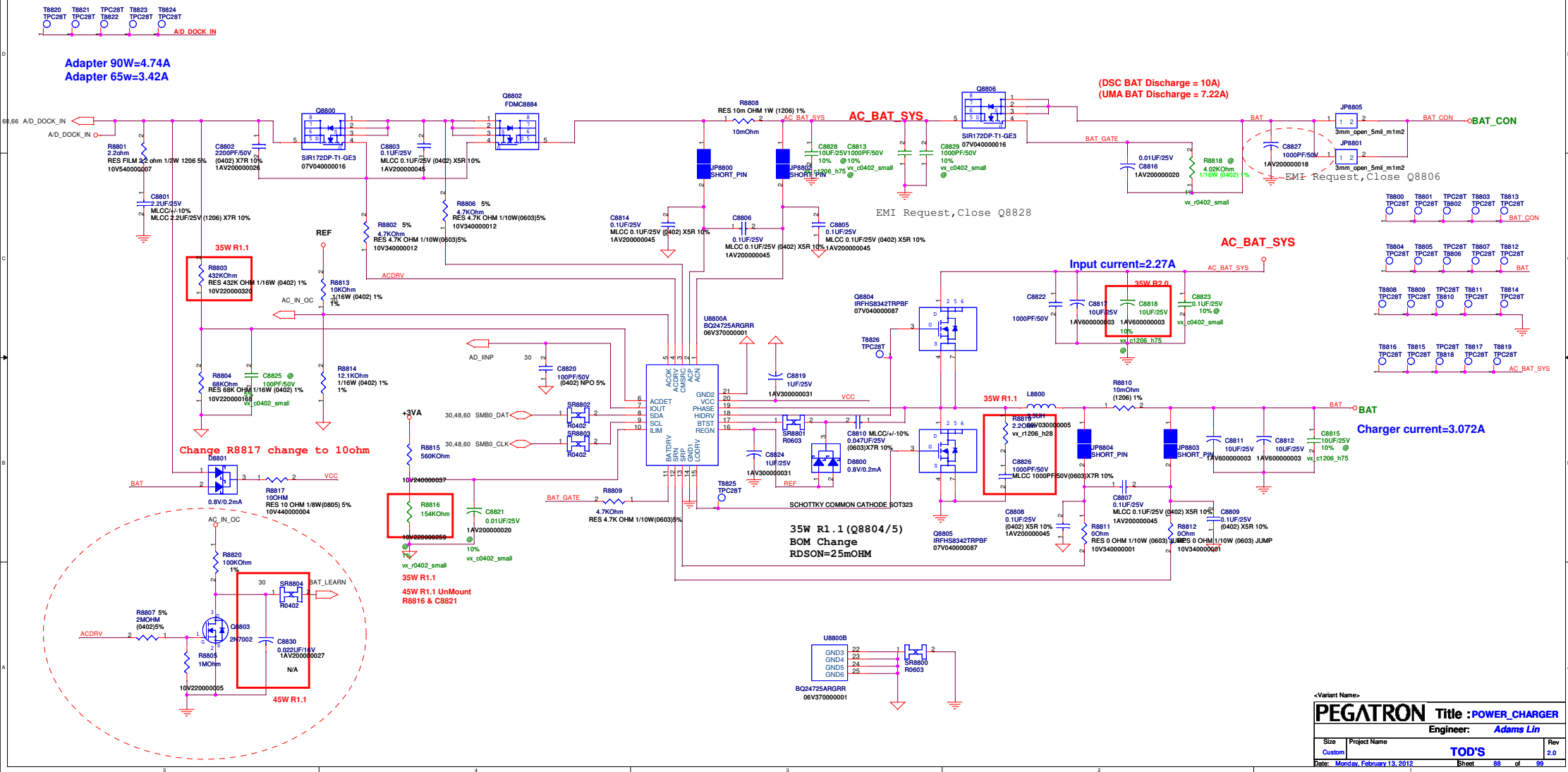


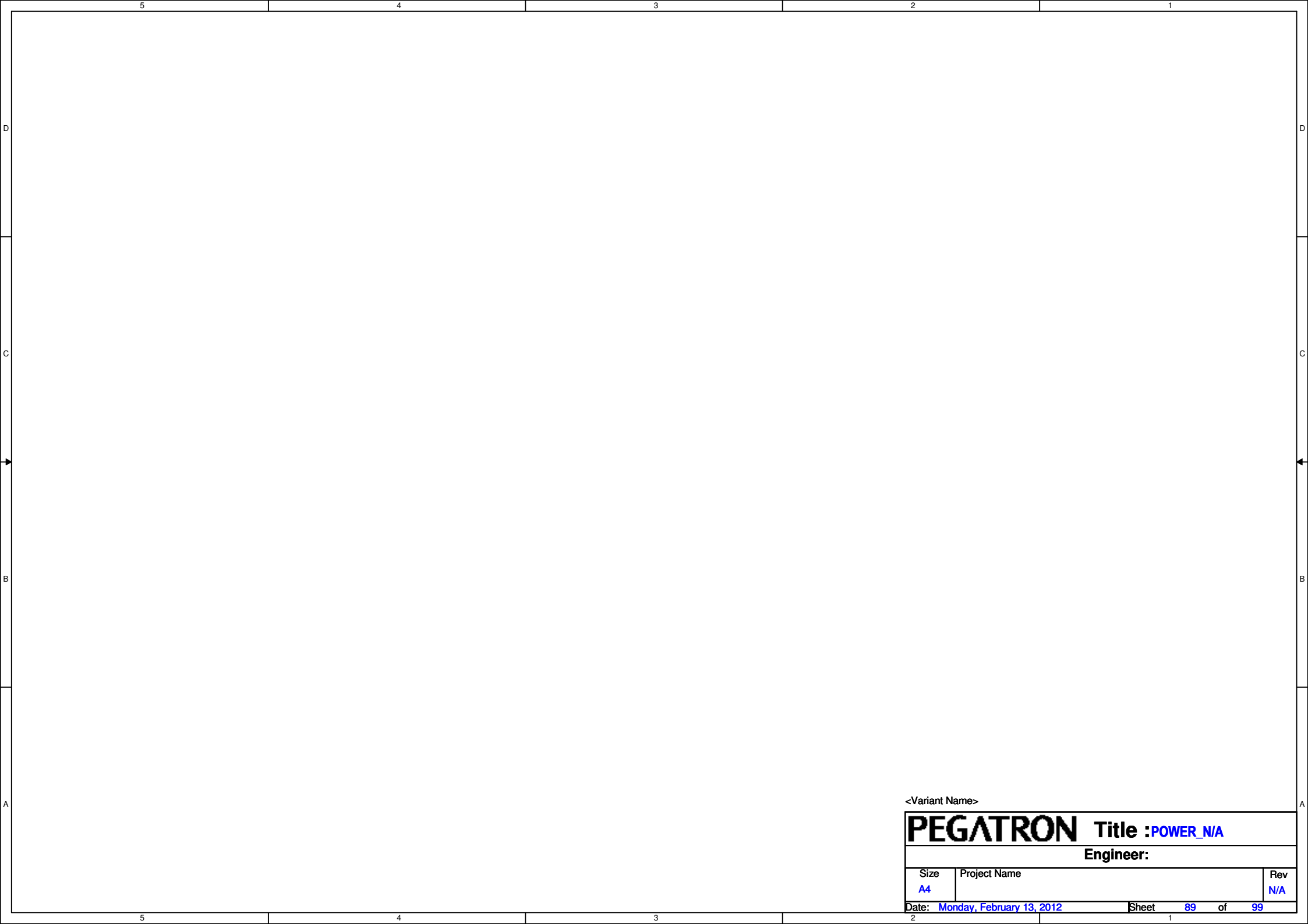
| <i>VID1</i> | <i>VID0</i> | <i>Seymour TTX</i> | <i>Thames XT</i> | <i>Thames LE</i> |
|-------------|-------------|--------------------|------------------|------------------|
| L | L | 1.15V | x | x |
| L | H | 1.1V | x | x |
| H | L | 105V | 1V | x |
| H | H | 0.9V | 0.9V | 0.9V |

| TPS51518 Pin16 (Mode) | | |
|-----------------------|-----------------|-----------|
| | Mode definition | Frequency |
| +5VO | DCAP2 | 350KHz |
| GND | DCAP | 350KHz |



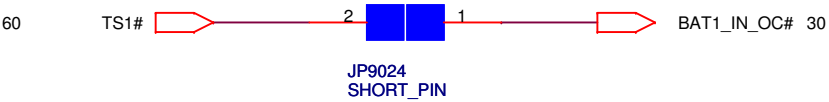
BATTERY CHARGER



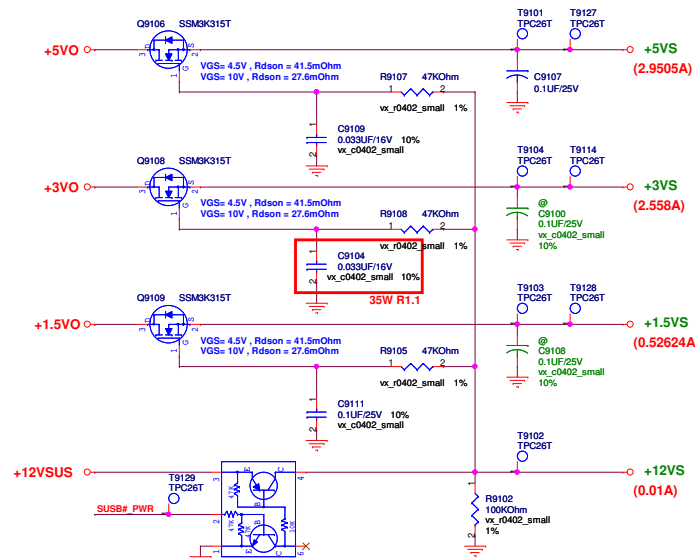


| | | |
|---------------------------------|--------------|--------------------------|
| <Variant Name> | | |
| PEGATRON | | Title : POWER_N/A |
| Engineer: | | |
| Size A4 | Project Name | Rev N/A |
| Date: Monday, February 13, 2012 | | Sheet 89 of 99 |

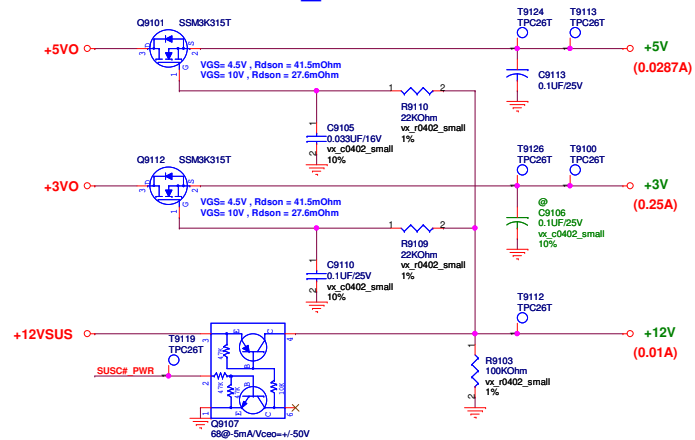
BATTERY IN DETECT



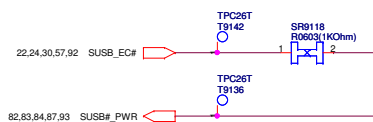
SUSB#_PWR POWER



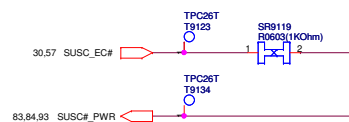
SUSC#_PWR POWER



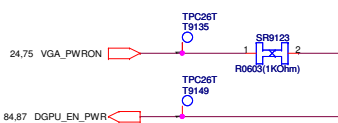
SUSB#_PWR POWER Control



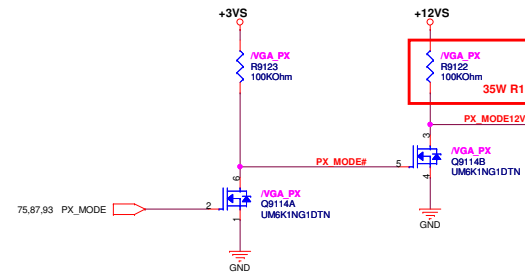
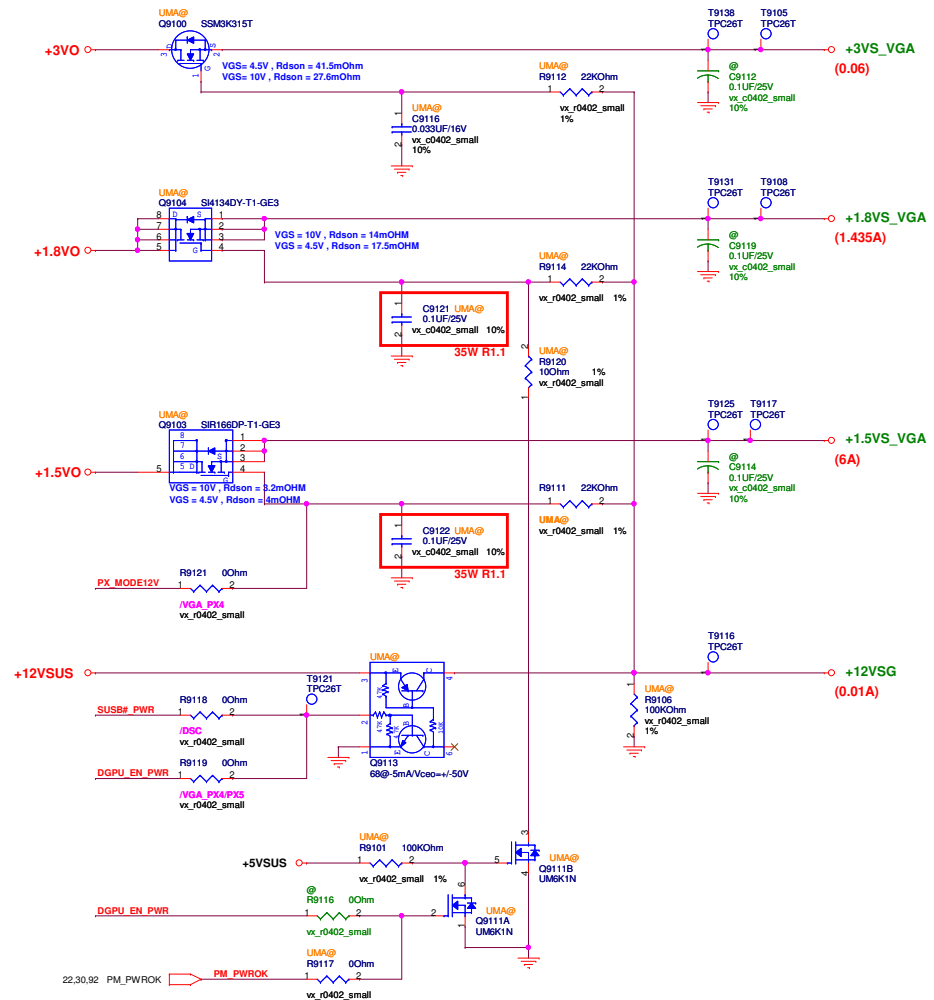
SUSC#_PWR POWER Control



DSC_VGA_PWR POWER Control



DSC#_PWR POWER



<Variant Name>

PEGATRON Title : POWER_LOAD SWITCH

Engineer: Adams Lin

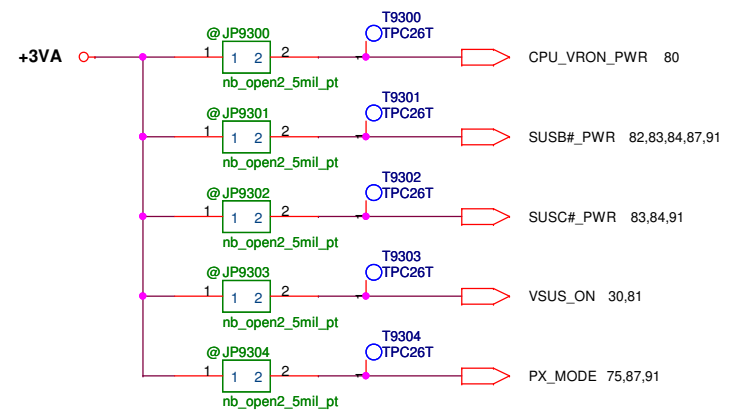
| | | |
|--------|--------------|-----|
| Size | Project Name | Rev |
| Custom | | 2.0 |

Date: Monday, February 13, 2012 Sheet 91 of 99

| | |
|--|------------------------------|
| <Variant Name> | |
| PEGATRON | Title : POWER_PROTECT |
| Engineer: Adams Lin | |
| Size Custom | Project Name Tod's |
| Date: Monday, February 13, 2012 | Sheet 92 of 99 |
| | Rev 2.0 |

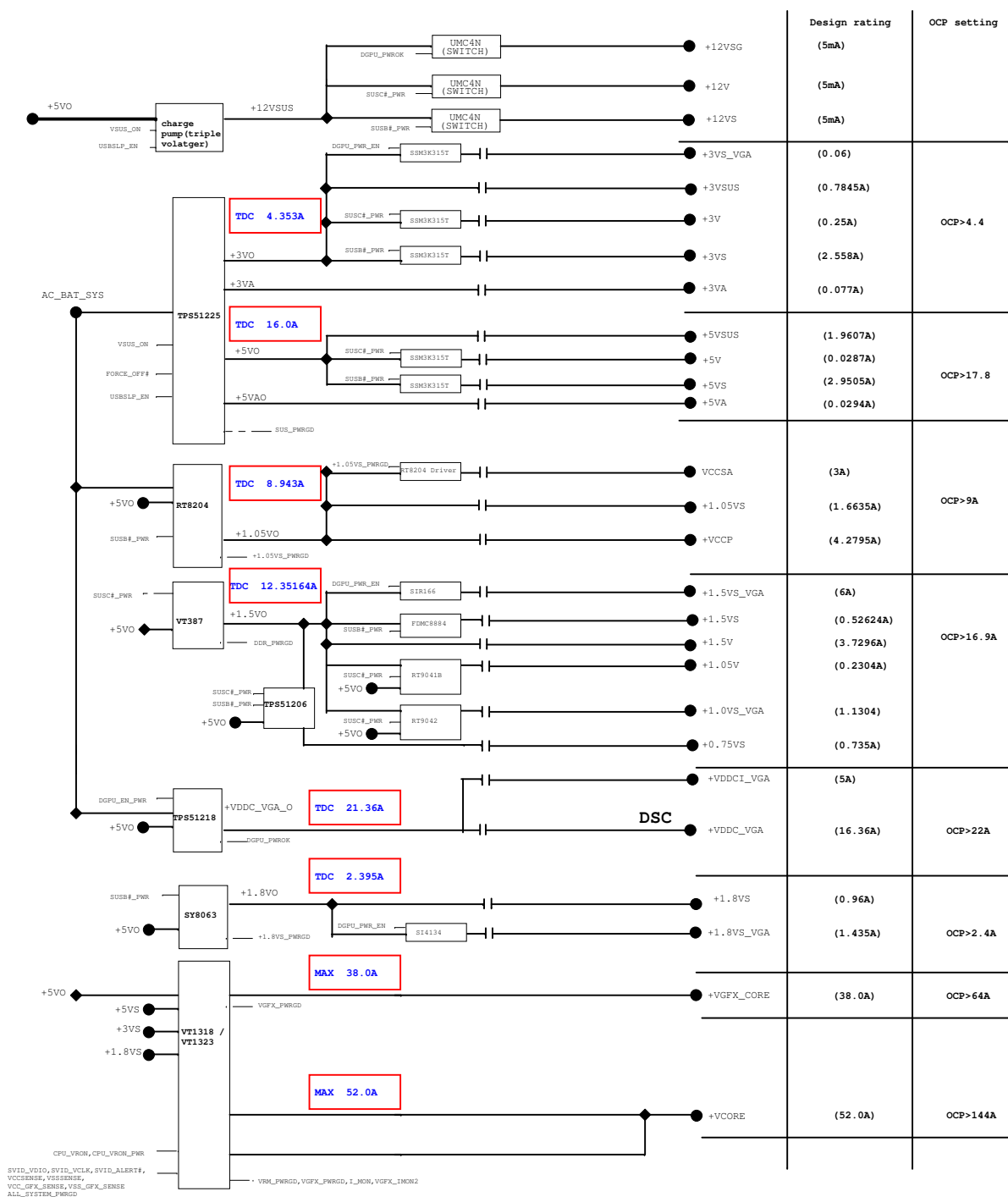
FOR POWER TEST

| | | | |
|------------|--|------------|--|
| AC_BAT_SYS | | AC_BAT_SYS | 45,48,81,82,87,88 |
| BAT_CON | | BAT_CON | 60,88 |
| | | | |
| +5VA | | +5VA | 48,52,56,81 |
| +3VA | | +3VA | 20,30,40,48,57,60,65,81,88 |
| +3VA_WLAN | | +3VA_WLAN | 53,81 |
| | | | |
| +5VO | | +5VO | 80,81,82,83,84,87,91 |
| +3VO | | +3VO | 81,84,91 |
| +1.8VO | | +1.8VO | 84,91 |
| +1.5VO | | +1.5VO | 16,17,18,83,84,91 |
| +1.05VO | | +1.05VO | 82 |
| | | | |
| +12VSUS | | +12VSUS | 22,48,51,81,91 |
| +5VSUS | | +5VSUS | 22,27,48,51,52,81,91 |
| +3VSUS | | +3VSUS | 4,22,24,27,28,30,33,48,53,81,92 |
| | | | |
| +12V | | +12V | 91 |
| +5V | | +5V | 91 |
| +3V | | +3V | 4,24,44,45,55,57,82,91 |
| +1.5V | | +1.5V | 5,7,57,83 |
| | | | |
| +12VS | | +12VS | 28,48,75,91 |
| +5VS | | +5VS | 20,27,30,31,36,46,48,50,51,56,57,80,91 |
| +3VS | | +3VS | 4,16,17,20,21,22,23,24,25,26,27,28,30,31,32,33,36,37,40,45,46,48,50,51,53,57,75,80,91,92 |
| +1.8VS | | +1.8VS | 7,25,26,80,84 |
| +1.5VS | | +1.5VS | 26,53,57,91 |
| +1.05VS | | +1.05VS | 26,27,82 |
| +0.75VS | | +0.75VS | 16,17,57,83 |
| | | | |
| +3VS_VGA | | +3VS_VGA | 57,70,71,74,75,91 |
| +1.0VS_VGA | | +1.0VS_VGA | 57,70,71,75,76,84 |
| +VDDC_VGA | | +VDDC_VGA | 75,87 |
| | | | |
| +VCCSA | | +VCCSA | 7,82 |
| +VCCP | | +VCCP | 3,4,6,7,26,27,30,32,82 |
| +VGFX_CORE | | +VGFX_CORE | 7,80 |
| +VCORE | | +VCORE | 6,80 |

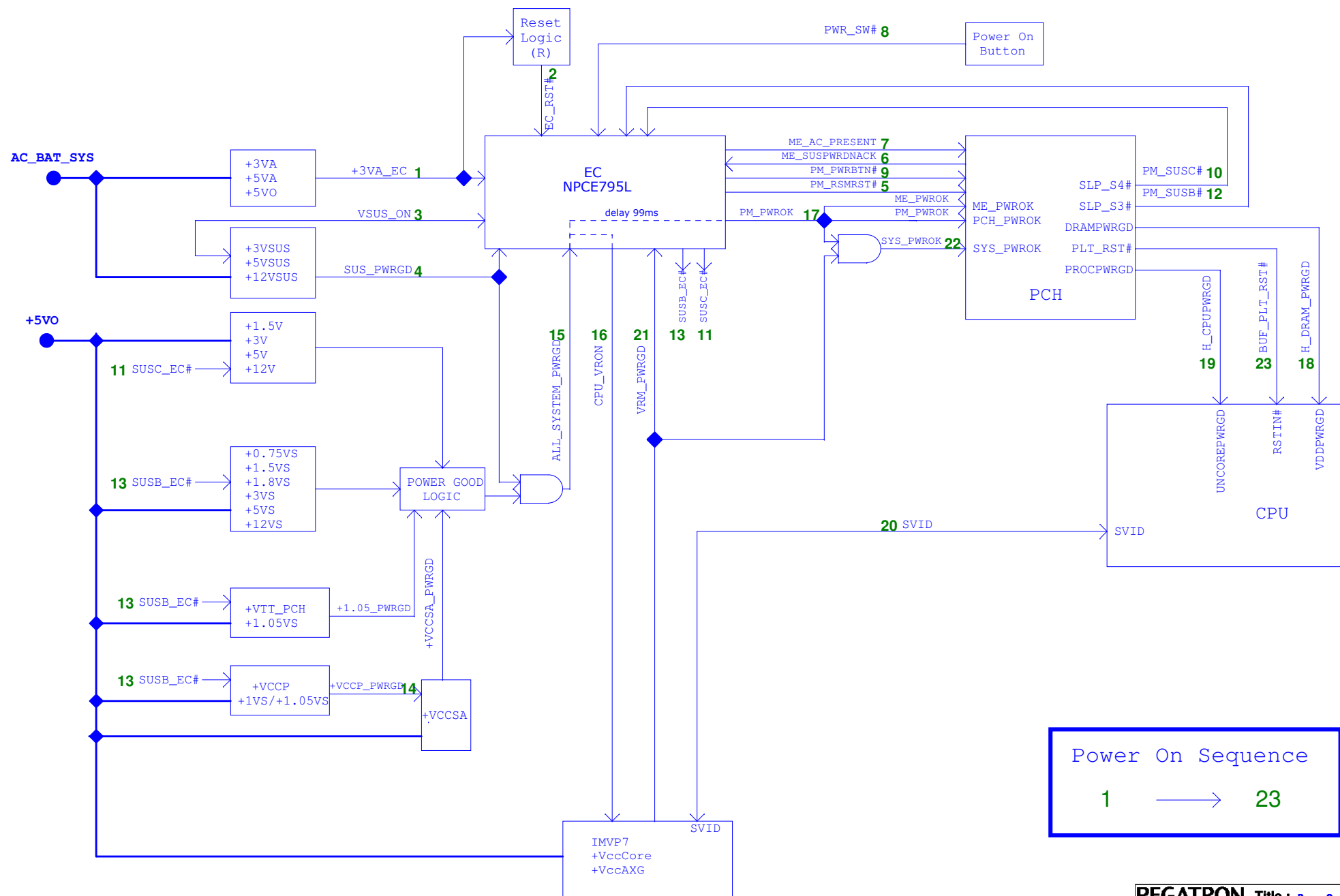


<Variant Name>

| | | | |
|---------------------------------|--------------|-----------------------------|---------|
| PEGATRON | | Title : POWER_SIGNAL | |
| Size | | Engineer: Adams Lin | |
| Custom | Project Name | Tod's | Rev 2.0 |
| Date: Monday, February 13, 2012 | | Sheet 93 | of 99 |



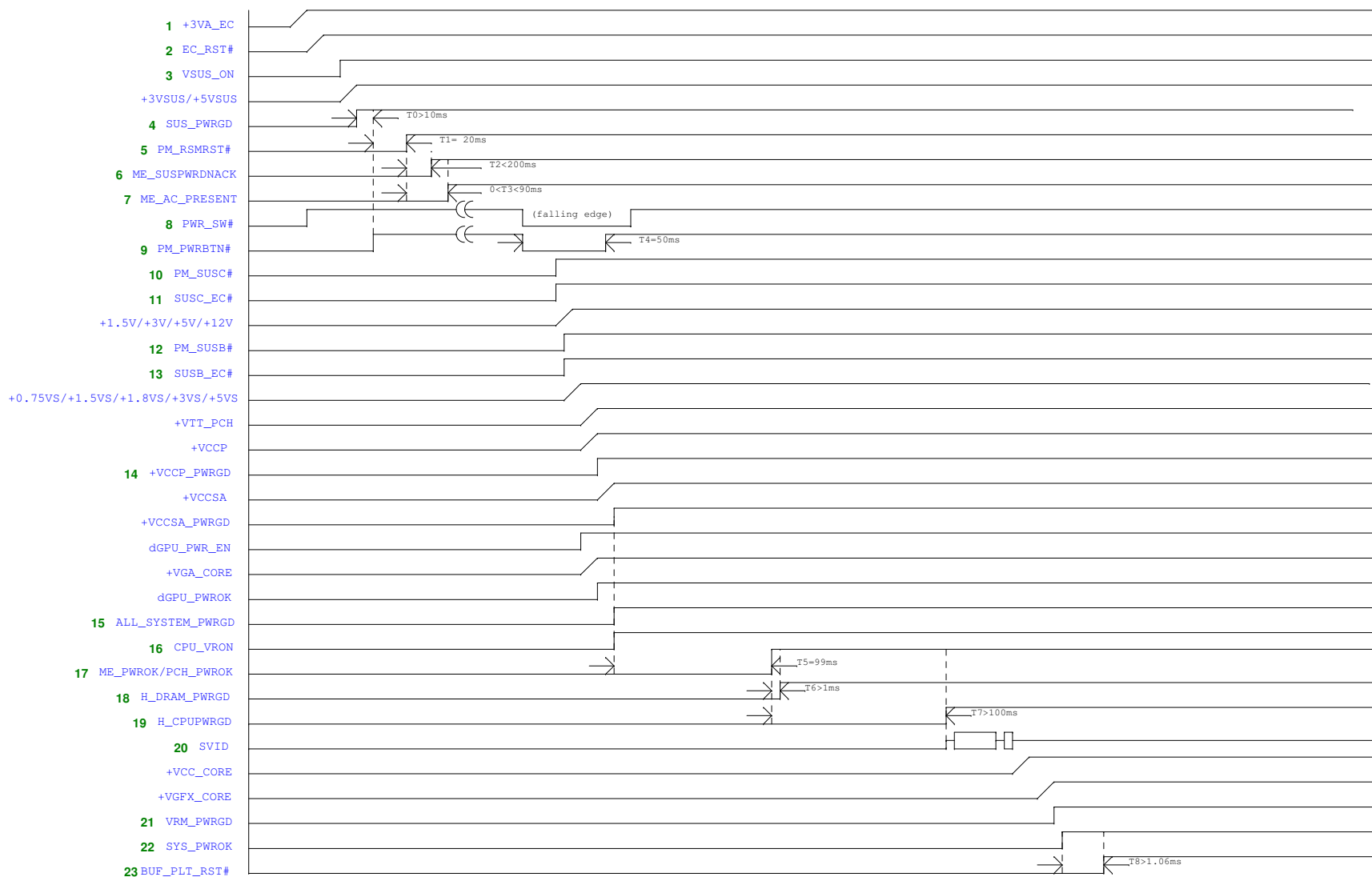
Power On Sequence Diagram G3-S0 R0.3 (non-iAMT, non-Deep Sx)

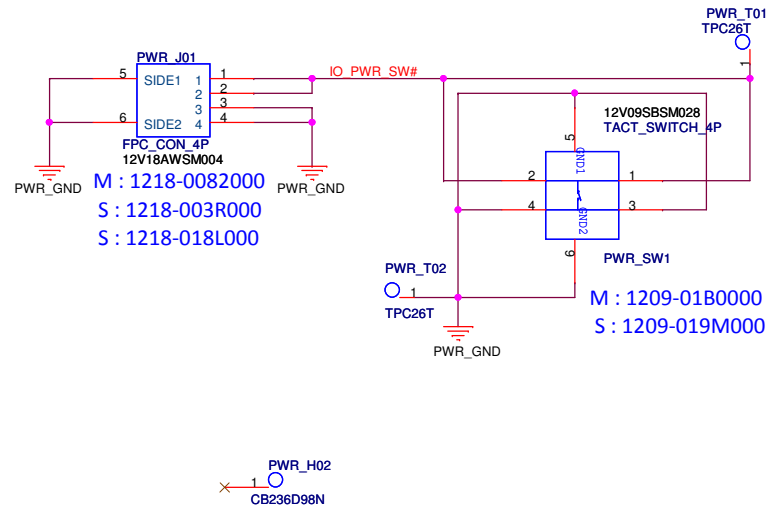


Power On Sequence

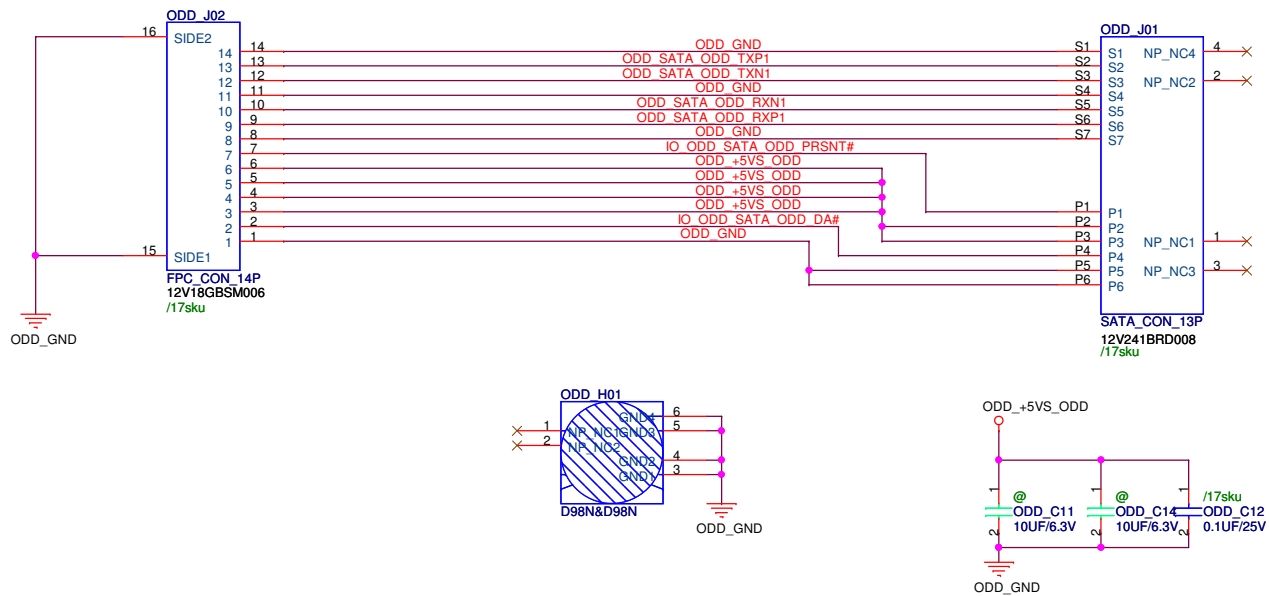
1 → 23

Power On Sequence Diagram G3-S0 R0.3 (non-iAMT, non-Deep Sx)

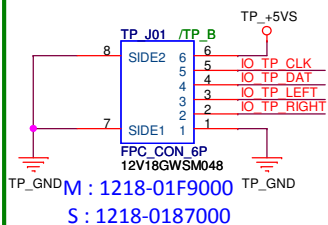




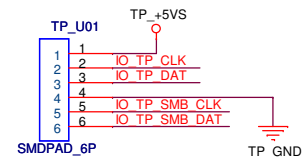
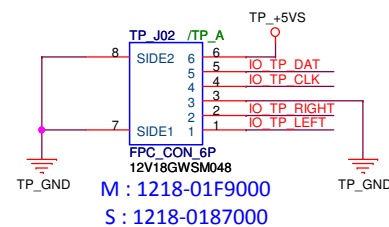
| | | | |
|---------------------------------|-----------------------------|--------------------|------------|
| PEGATRON | | Title : ODD | |
| BG1-CSC-HW R&D Dept.5 | | Engineer: | |
| Size B | Project Name PLFG | | Rev 2.1 |
| Date: Monday, February 13, 2012 | | Sheet 100 of 104 | |



For TM-01146-003

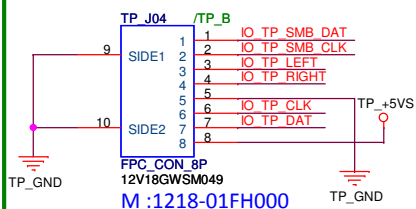


For TM-01680-001

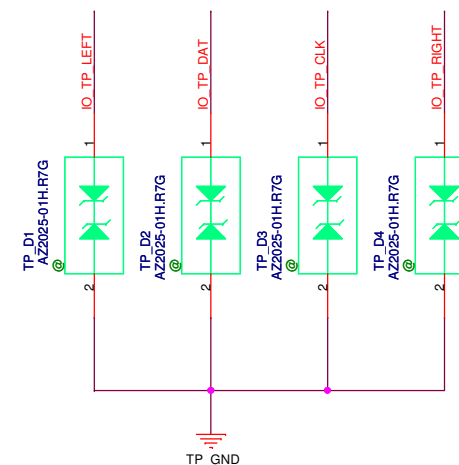
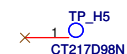
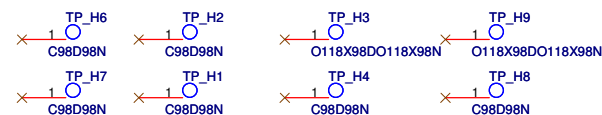
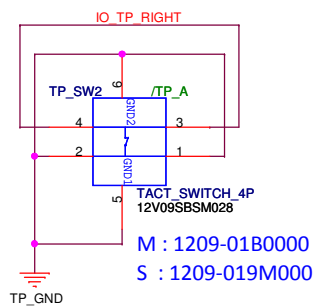
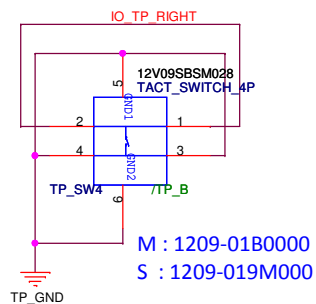
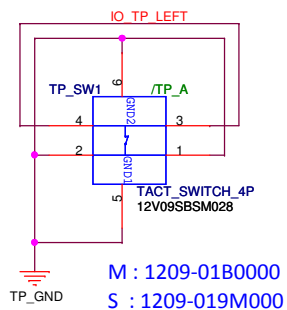
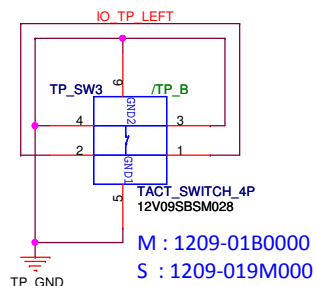
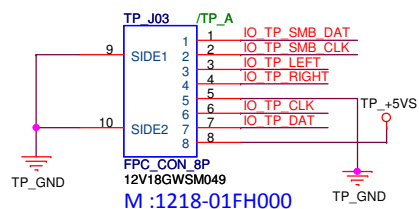


| TP_MODEL | BOM Optional |
|--------------|--------------|
| TM-01680-001 | TP_A |
| TM-01146-003 | TP_B |

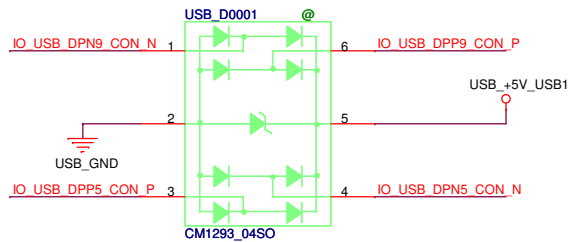
For 515-001540-01 p3



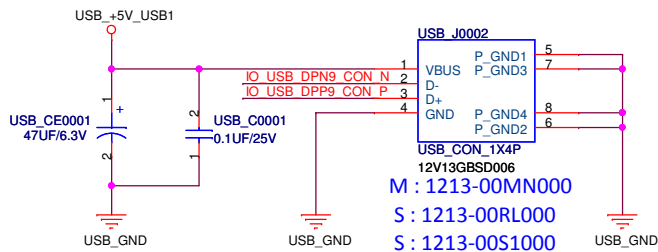
For 515-001539-01 p3



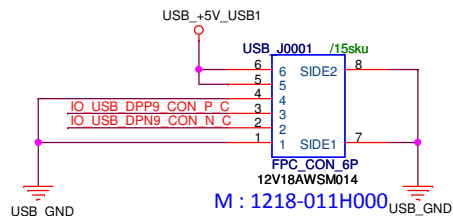
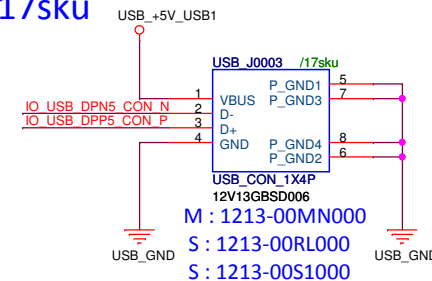
| PEGATRON Title :TP | | |
|---|-----------------------------|------------|
| BG1-CSC-HW R&D Dept.5 Engineer: <i>Eric_Chang</i> | | |
| Size B | Project Name PLFG | Rev 2.1 |
| Date: Monday, February 13, 2012 | Sheet 102 of 104 | |



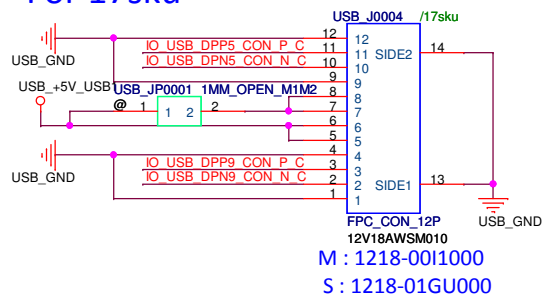
PLACE ESD Diodes near USB Connector



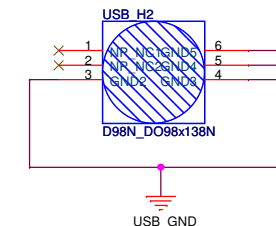
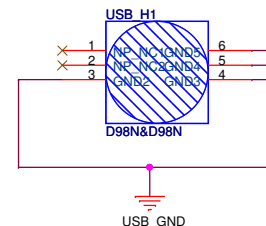
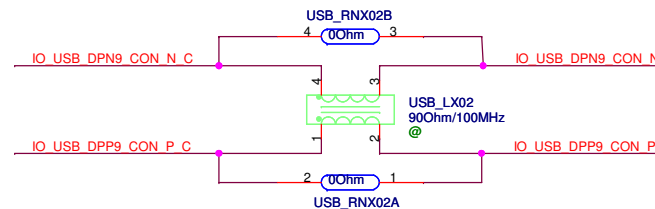
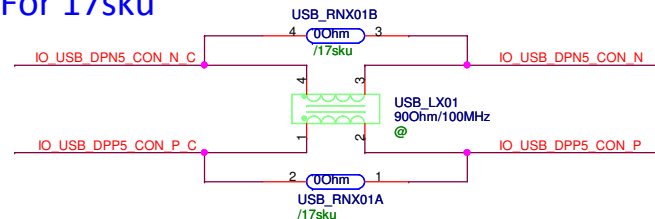
For 17sku



For 17sku



For 17sku



USB2.0(port 9 for Intel)
USB2.0(port 0 for Amd)

USB2.0(port 5 for Intel)
USB2.0(port 3 for Amd)
(For 17sku)

USB Port

TP

USB3.0 (port 2)
/USB2.0 (port 1)

USB3.0 (port 3)
/USB2.0 (port 2)
(S & C)

PEGATRON Title :IO_USB

BG1-CSC-HW R&D Dept.5

Engineer:

Size B Project Name

Date: Monday, February 13, 2012

PLF

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Rev 2.1

