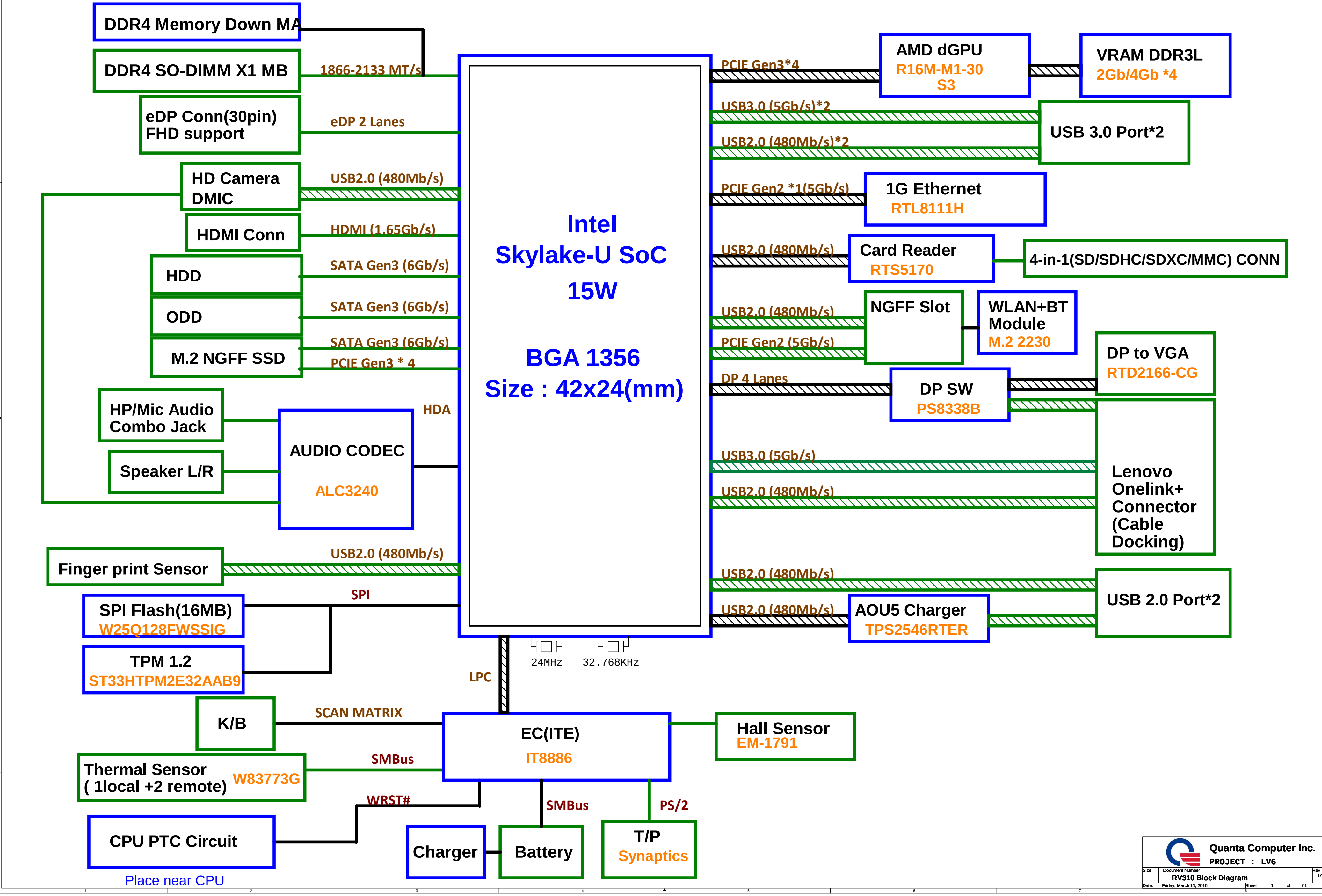
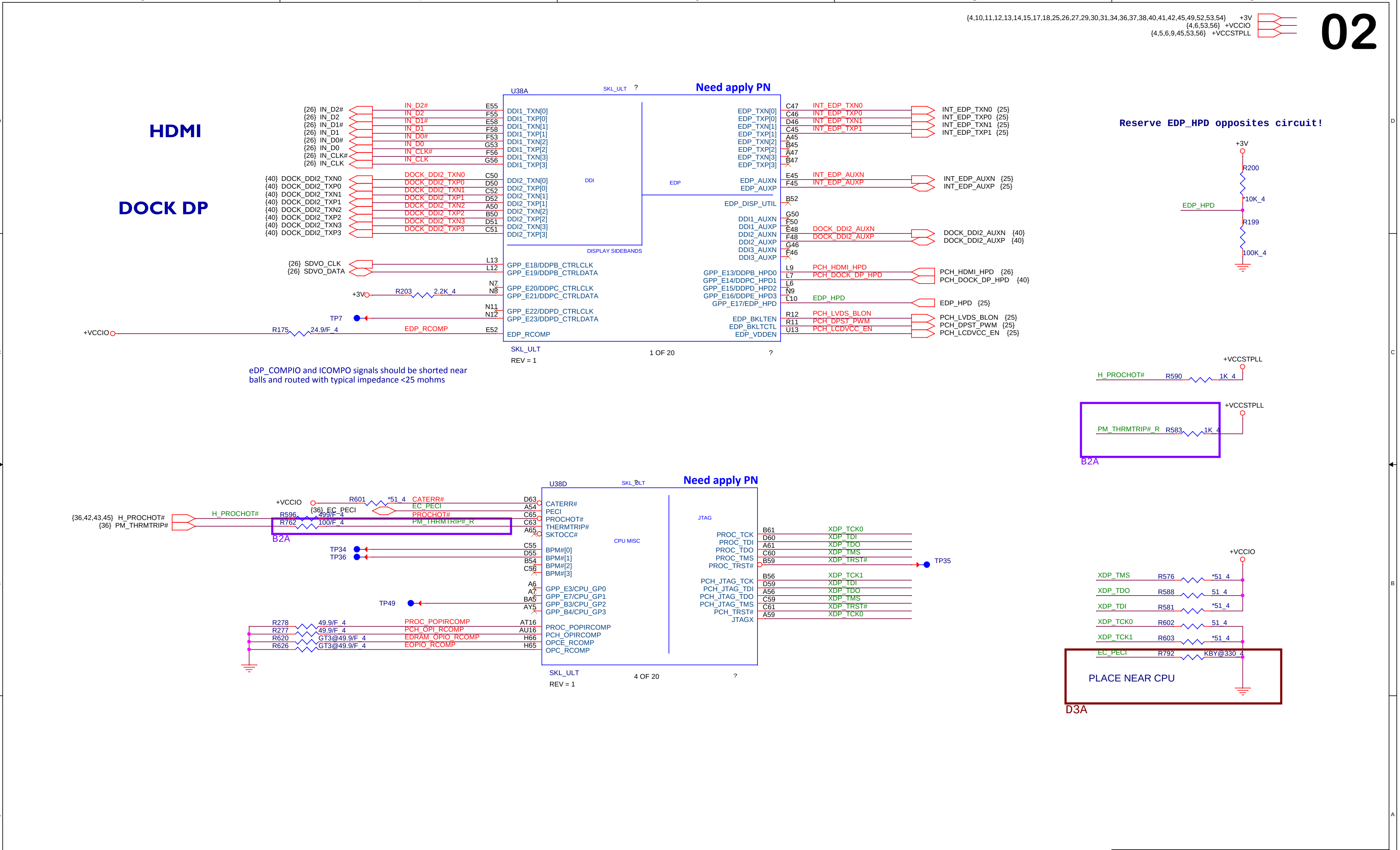
Intel Skylake-U Platform Block Diagram (Windows)





Quanta Computer Inc.

PROJECT : LV6

Size	Document Number	Rev
	SKYLAKE 1/15 eDP/DDI/MISC	1A

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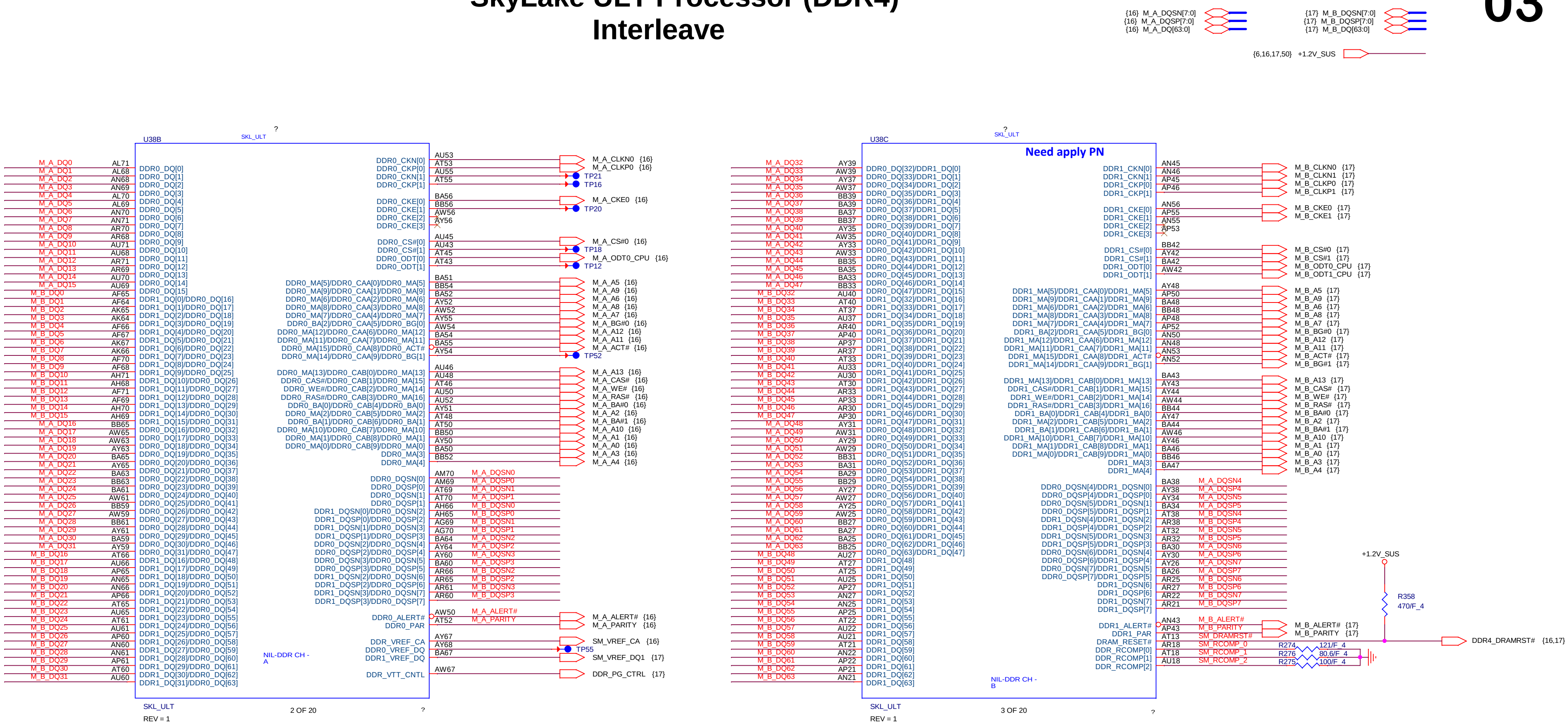
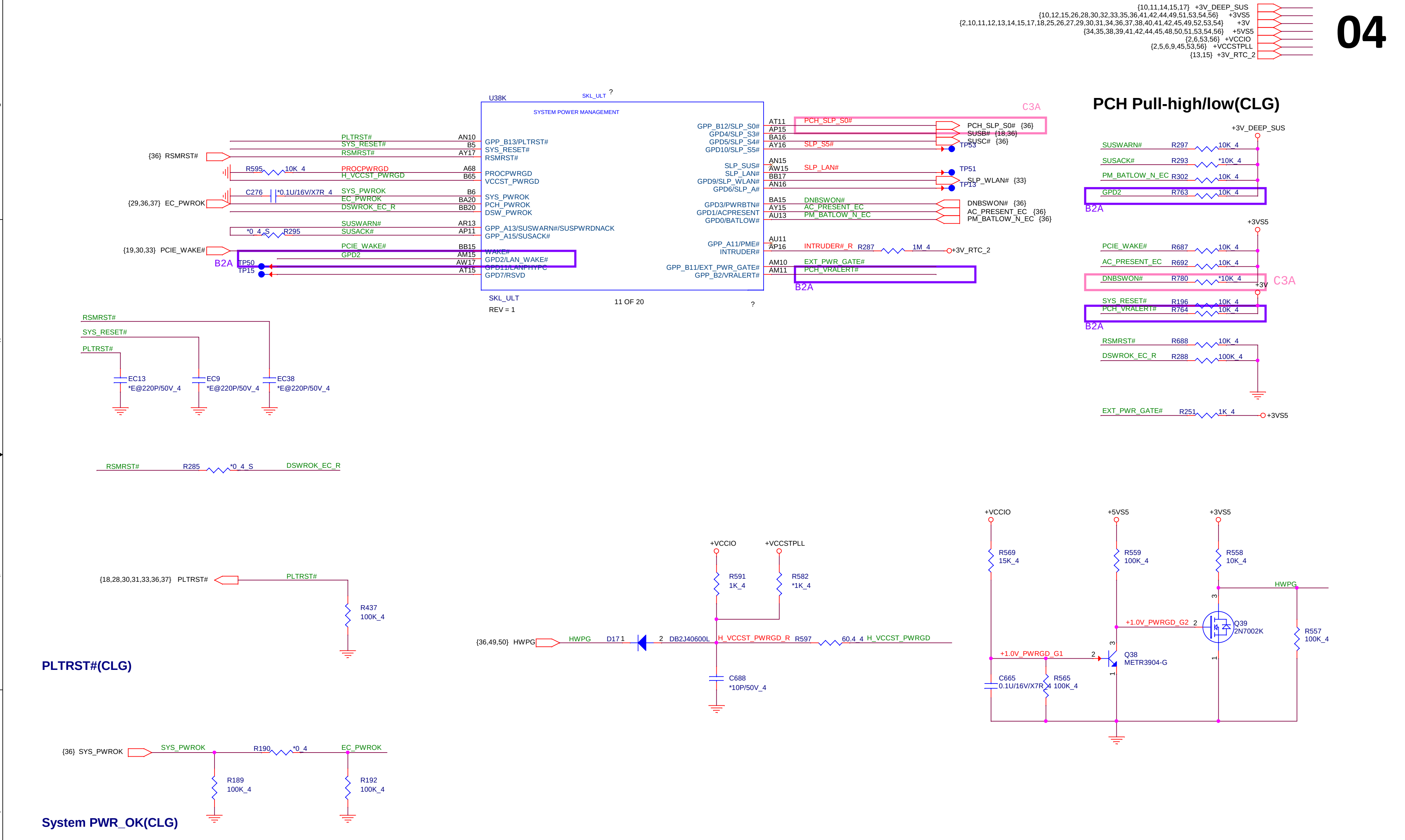
SkyLake ULT Processor (DDR4) Interleave

03



	Quanta Computer Inc.		
	PROJECT : LV6		
Size	Document Number: SKYLAKE 2/15(DDR4 I/F)		Rev 1A
Date: Friday, March 11, 2016	Sheet 3 of 61		

04



Quanta Computer Inc.

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Size	Document Number	Rev
	SKYLAKE 3/15(PowerManger)	1A

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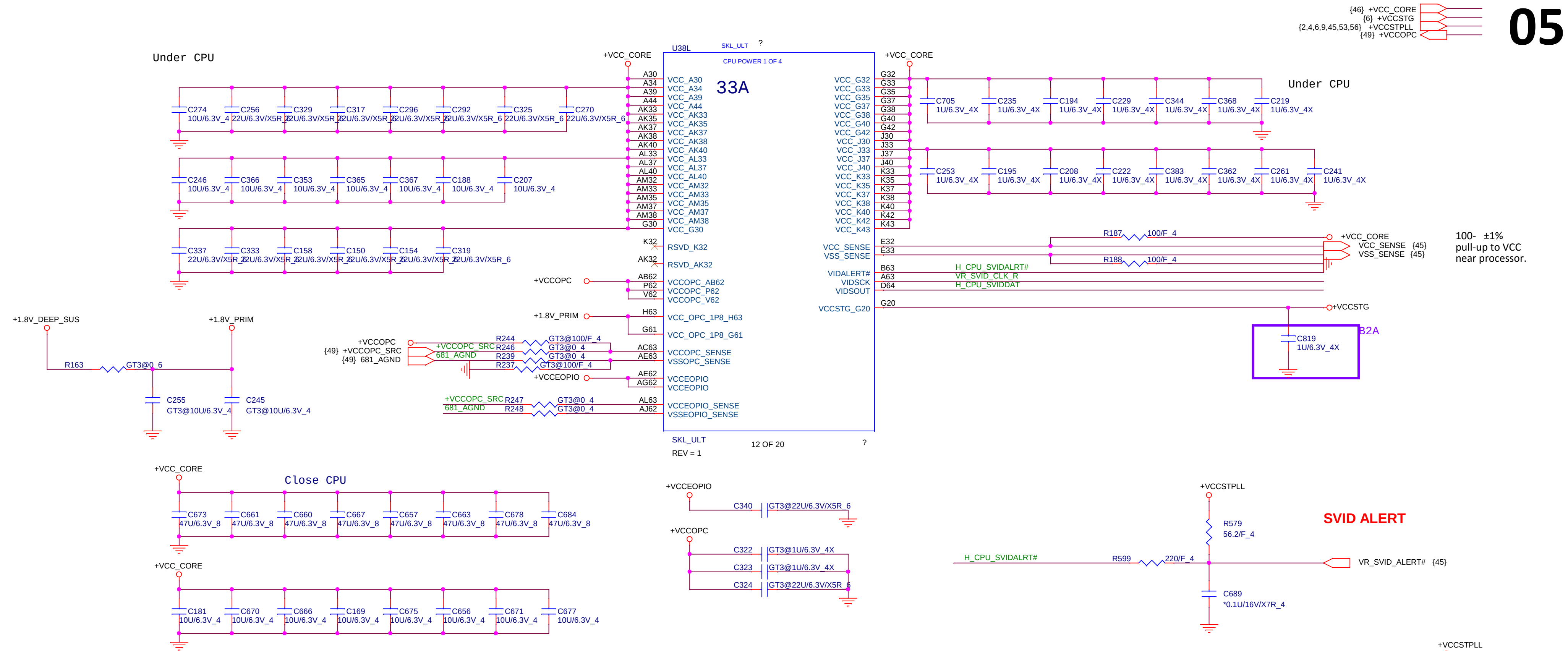

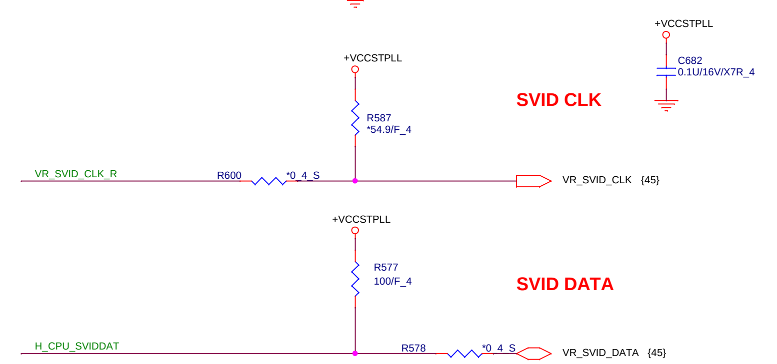

Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

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Size | Document Number: SKYLAKE 4/15 (POWER-1) | Rev 1A

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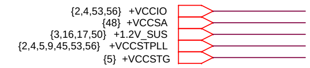
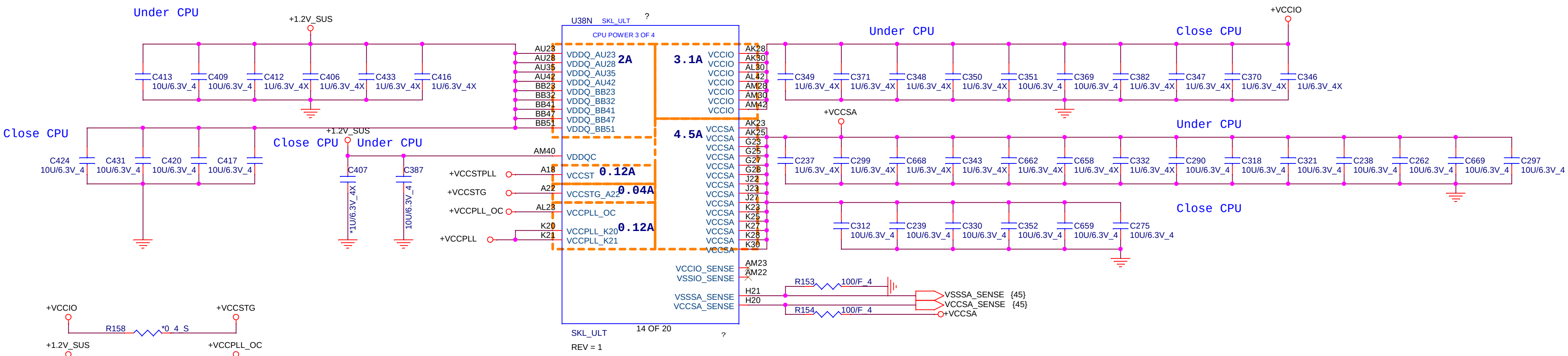
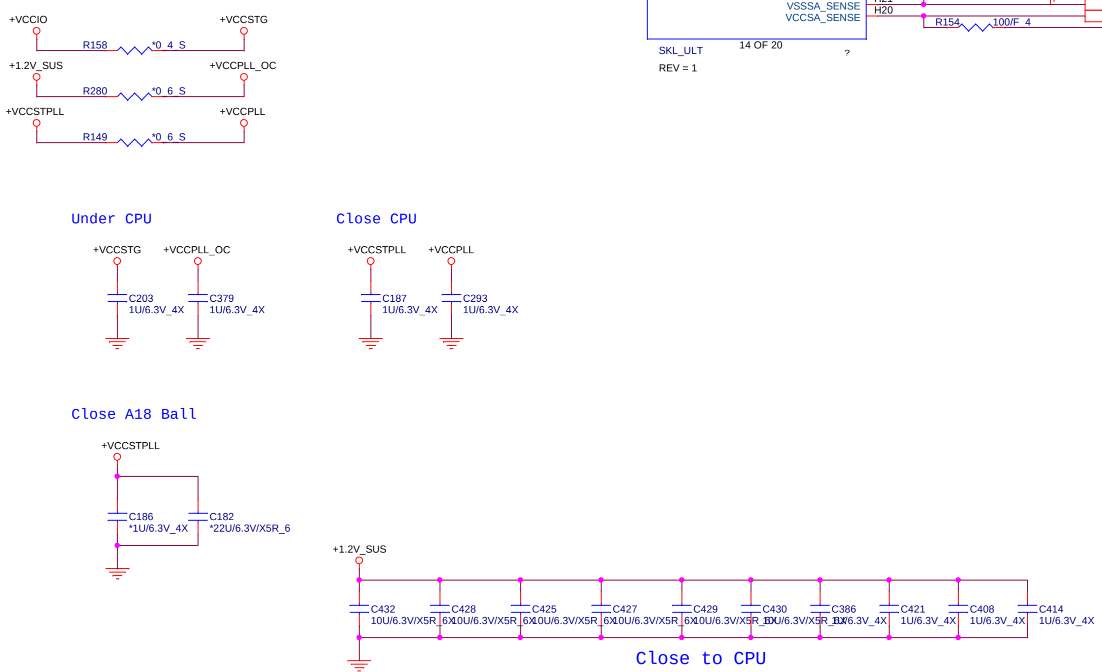
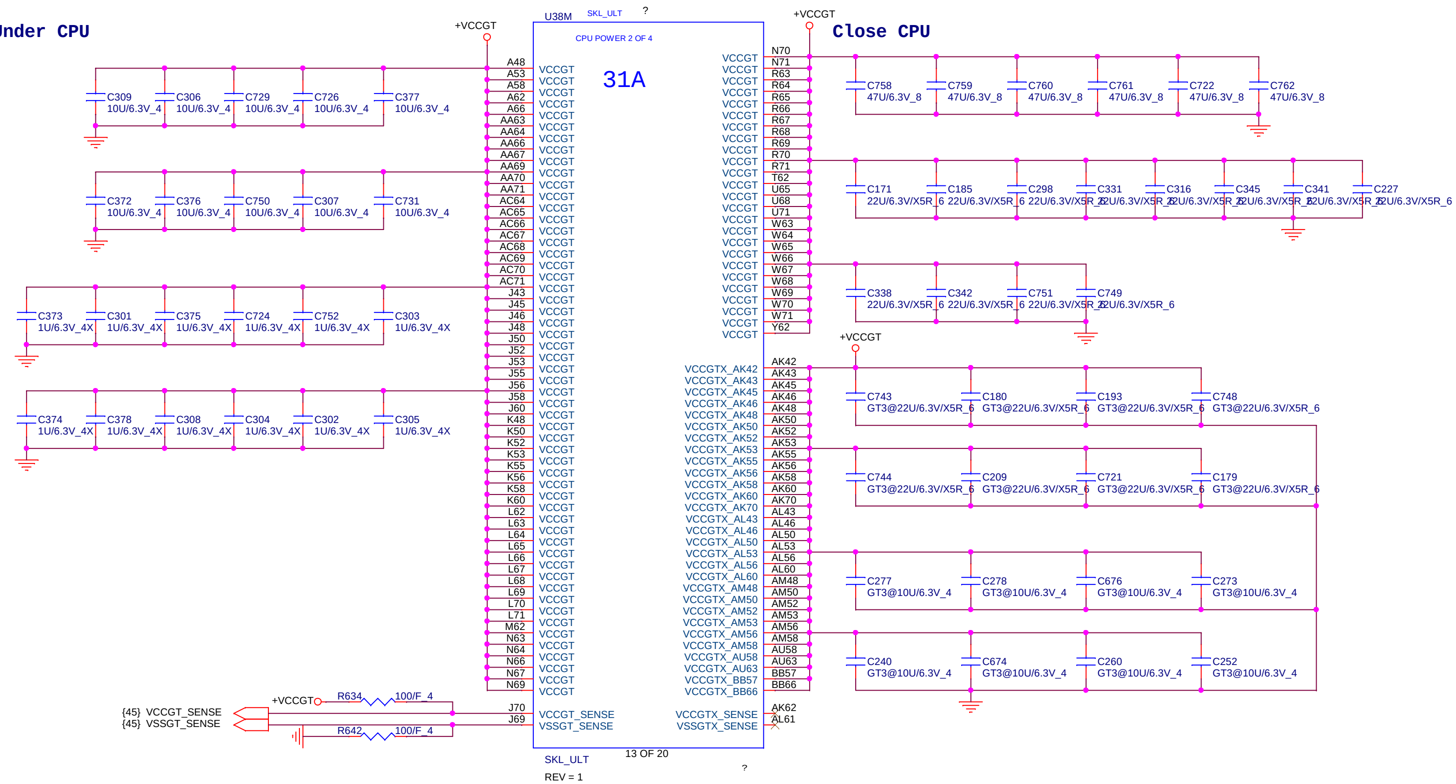






Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

+VCCGT {47}



Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

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	SKYLAKE 6/15 (POWER-3)	1A

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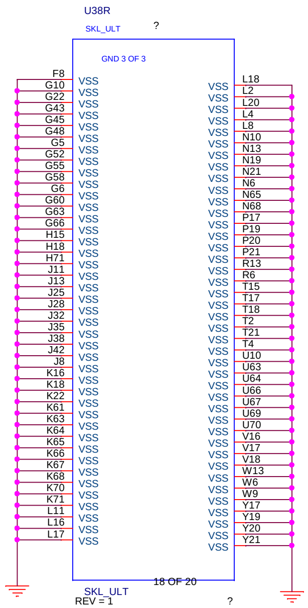

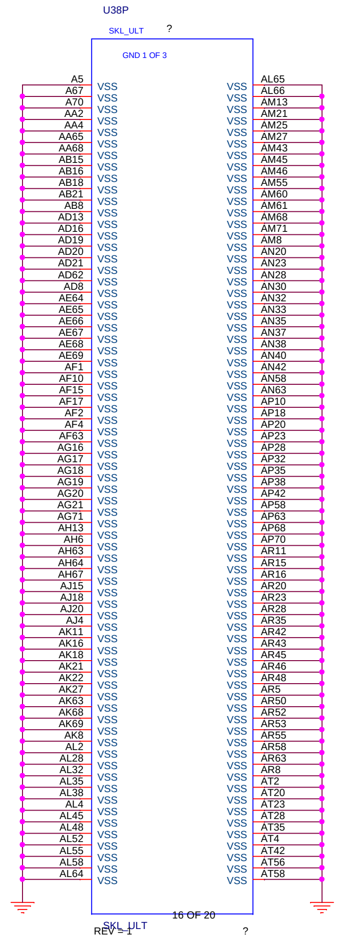

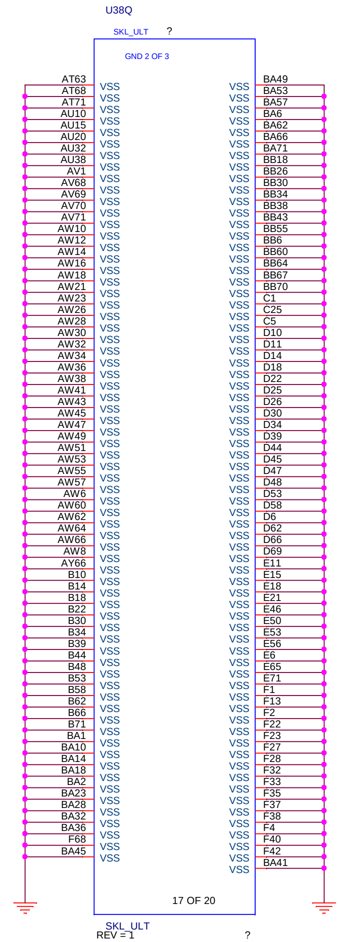

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	SKYLAKE 7/15 (GND)	1A

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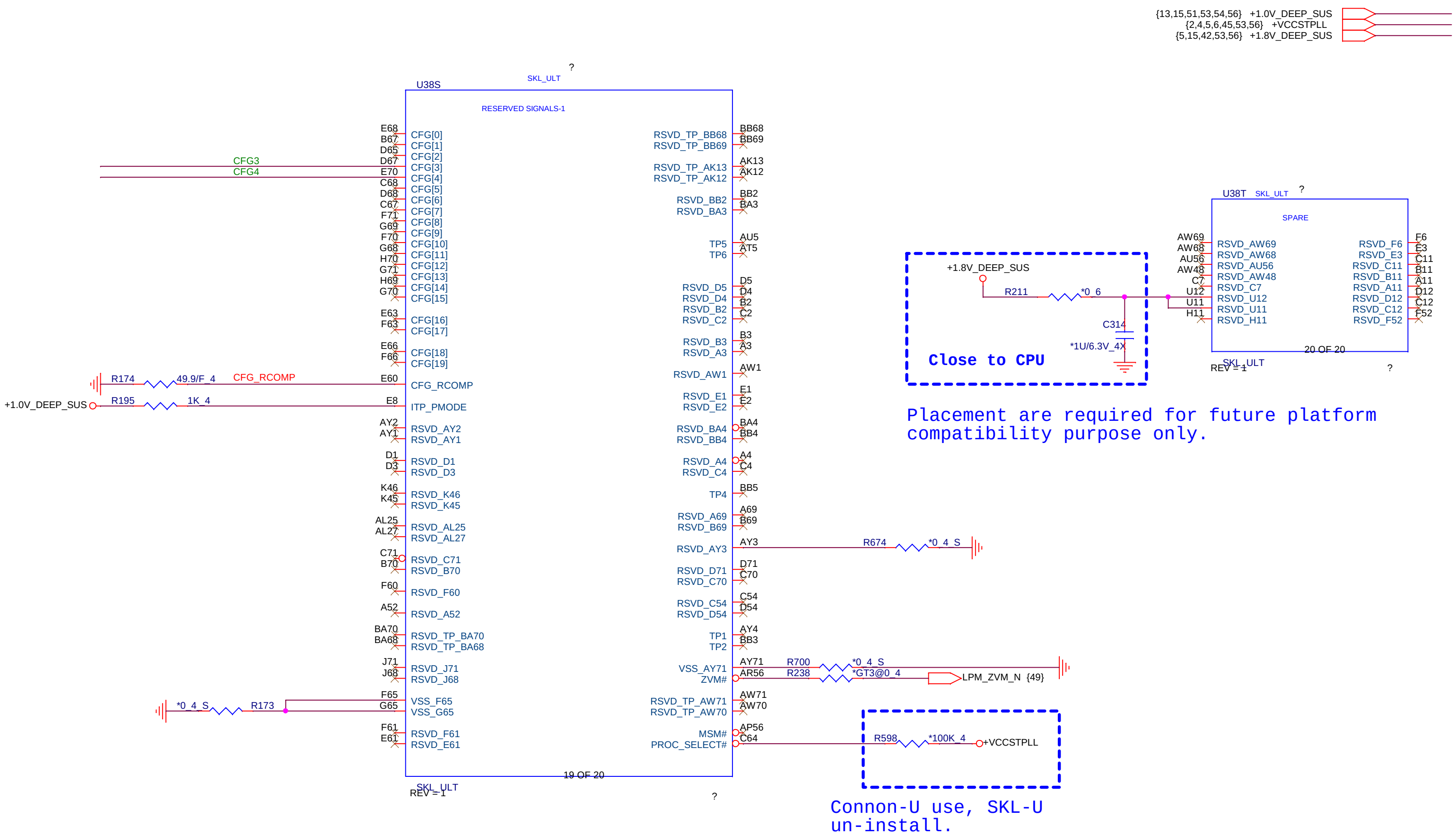

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physcial Debug Enable) DFX_Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R611 *1K_4
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R617 1K_4

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	SKYLAKE 8/15 (RSV)	1A

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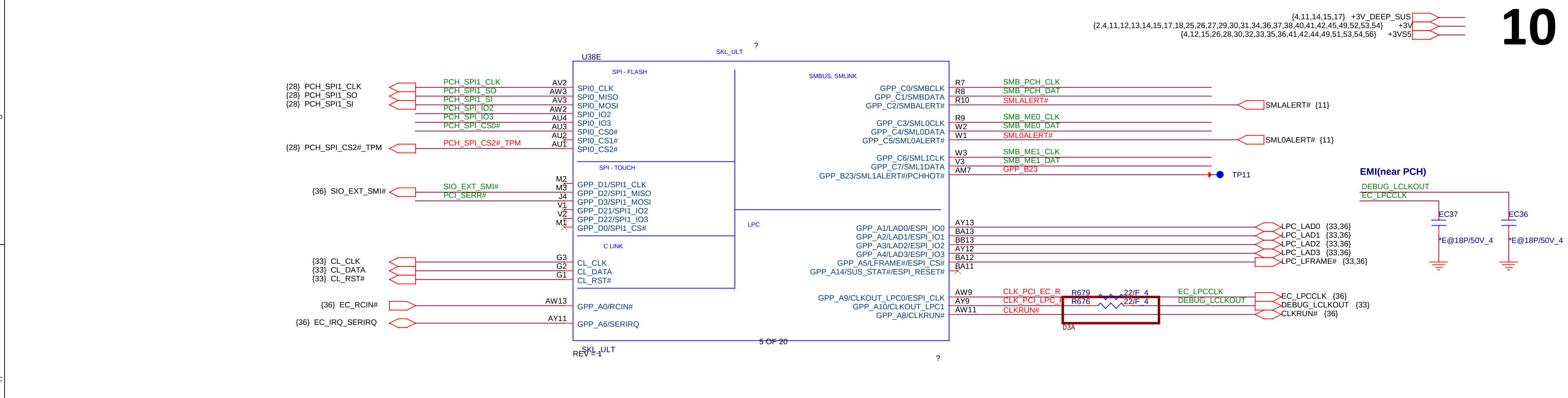
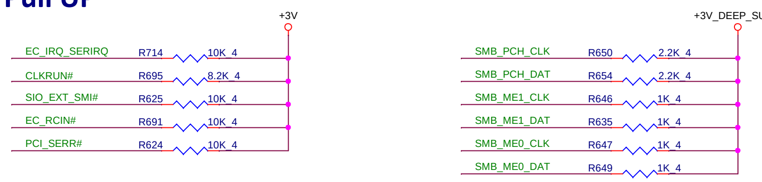
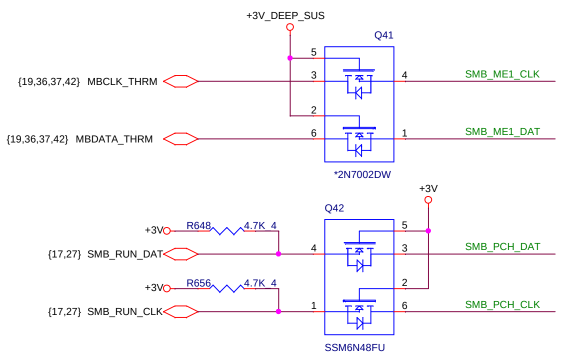


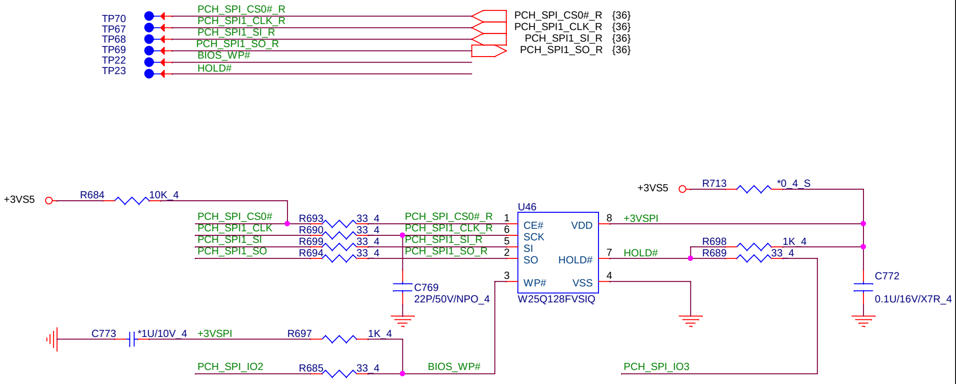
GPIO Pull UP



SMBus/Pull-up(CLG)



PCH SPI ROM(CLG)



Vender	Size	P/N
EON	16MB	AKE3DZNKQ00(EN25QH128AHIP)
GGD	16MB	AKE3DF00Q00 (GD25B128CSIGR)
Socket		DFHS08FS023

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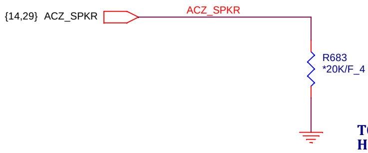
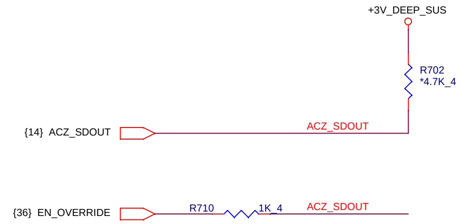
{4,10,14,15,17} +3V_DEEP_SUS
{2,4,10,12,13,14,15,17,18,25,26,27,29,30,31,34,36,37,38,40,41,42,45,49,52,53,54} +3V

Functional Strap Definitions

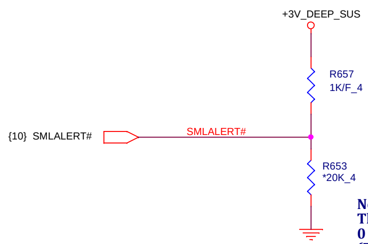
DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET



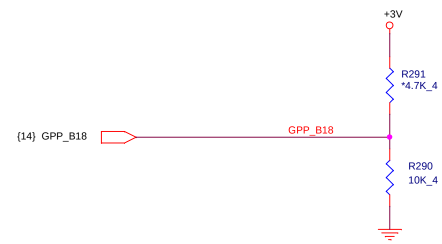
TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD



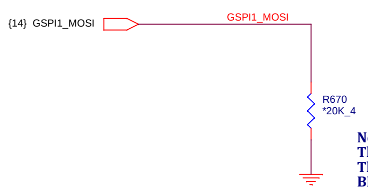
No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.
This function is useful when running ITP/XDP.



No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

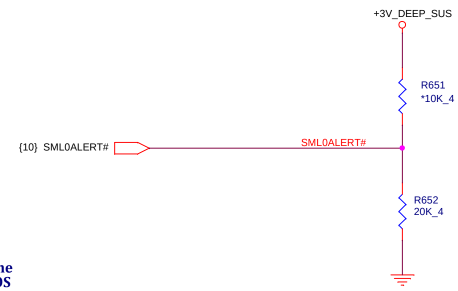


No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode
(PCH will disable the TCO Timer system reboot feature).
This function is useful when running ITP/XDP.

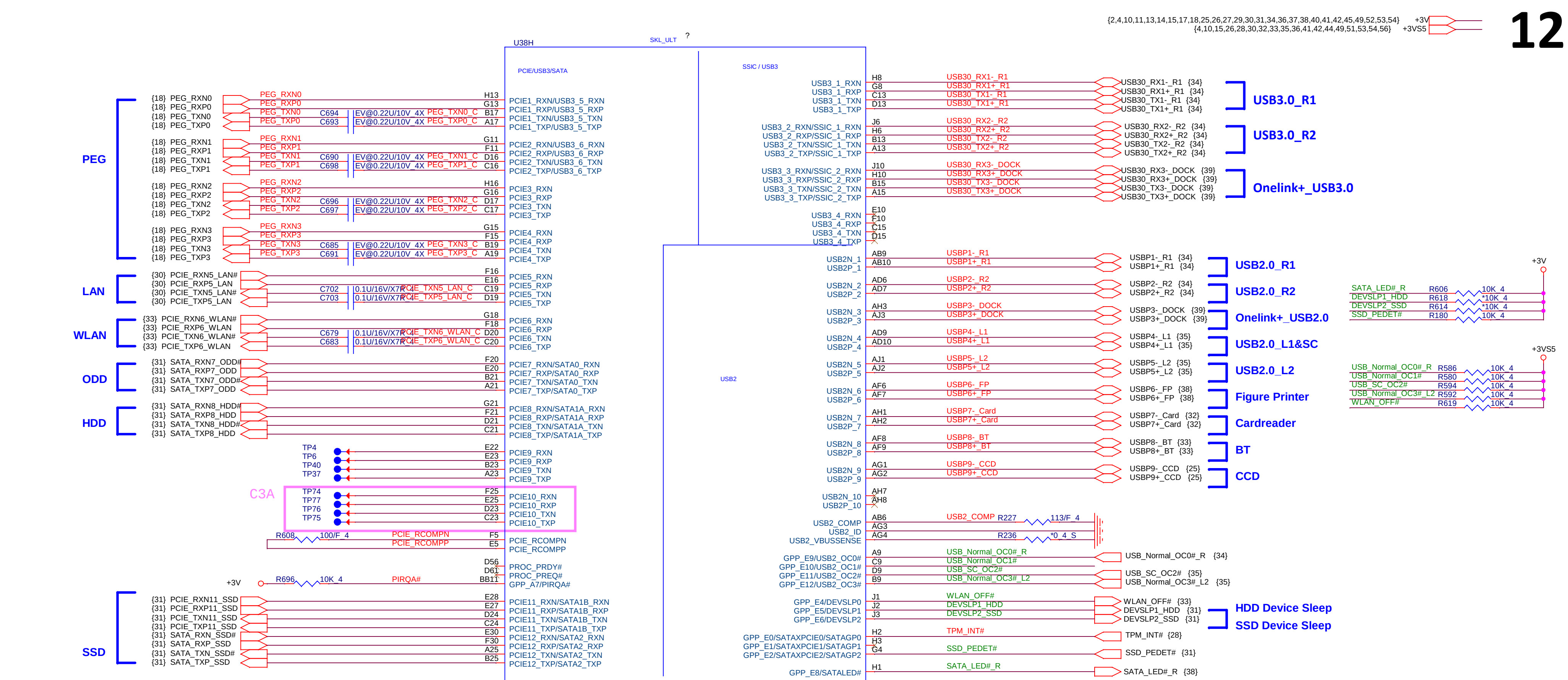


No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.

Bit 10	Boot BIOS Destination
0	SPI
1	LPC



No Boot:
The signal has a weak internal pull-down.
0 = LPC Is selected for EC.
1 = eSPI Is selected for EC.



PCI-E Port Mapping Table

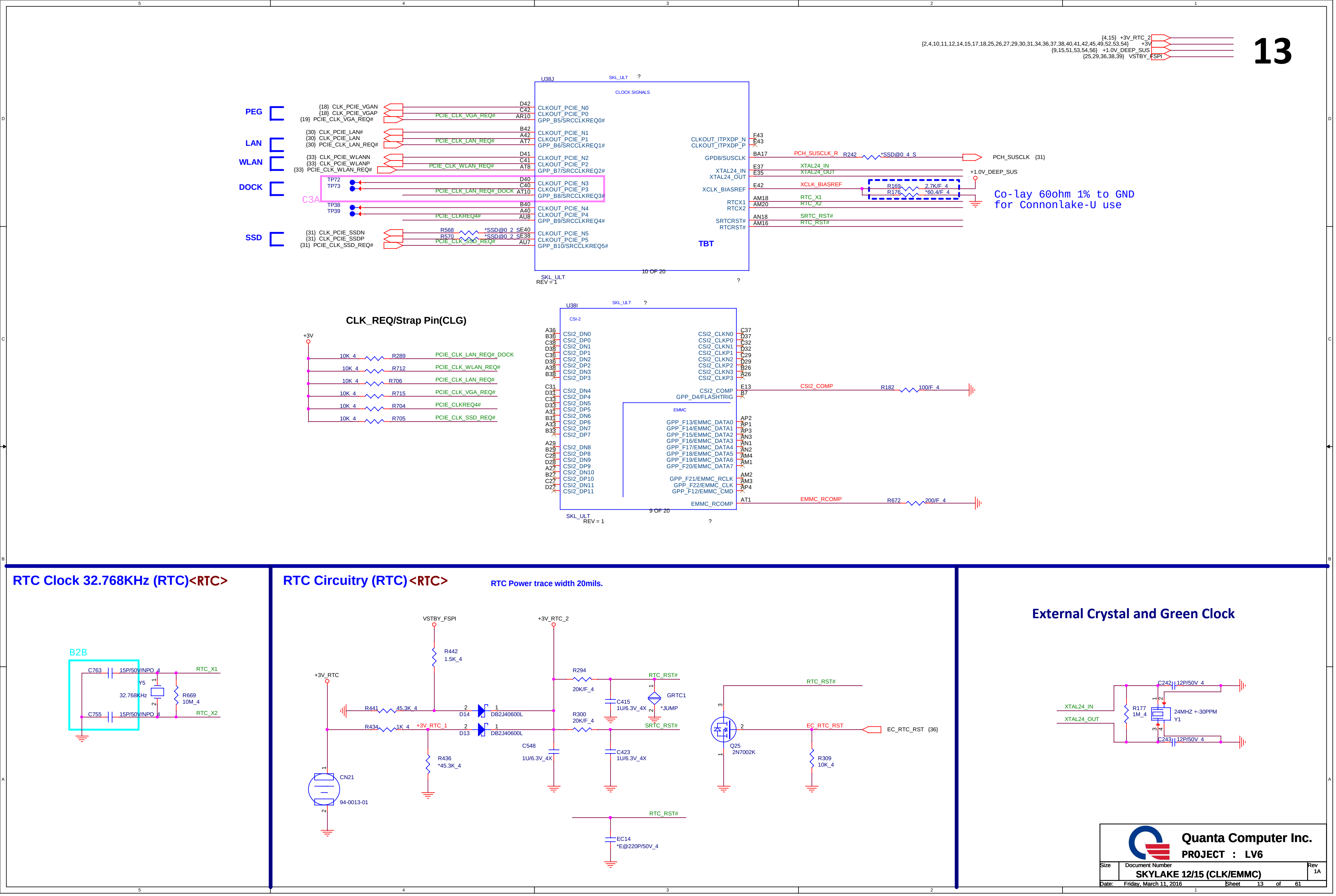
PCI-E Port	Function	CLK RQ Port	Function
Port1	dGPU	Port0	dGPU
Port2		Port1	LAN
Port3		Port2	WLAN
Port4		Port3	DOCK
Port5	LAN	Port4	Un-used
Port6	WLAN	Port5	SSD
Port7	ODD		
Port8	HDD		
Port9	Un-used		
Port10	DOCK		
Port11	SSD if Pcie Bus will lane reverse. if SATA BUS is SATA2.		
Port12			

USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	USB3.0_R1
PORT-2	USB3.0_R2
PORT-3	USB3.0_DOCK
PORT-4	

USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	USB2.0_R1
PORT-2	USB2.0_R2
PORT-3	USB2.0_DOCK
PORT-4	USB2.0_L1_S&C
PORT-5	USB2.0_L2
PORT-6	Figure Printer
PORT-7	Cardreader
PORT-8	BT
PORT-9	CCD
PORT-10	NC


13
{4,15} +3V_RTC_2
{2,4,10,11,12,14,15,17,18,25,26,27,29,30,31,34,36,37,38,40,41,42,45,49,52,53,54} +3V
{9,15,51,53,54,56} +1.0V_DEEP_SUS
{25,29,36,38,39} VSTBY_FSPI
U38J
SKL_ULT
CLOCK SIGNALS
PEG
LAN
WLAN
DOCK
SSD
{18} CLK_PCIE_VGAN
{18} CLK_PCIE_VGAP
{19} PCIE_CLK_VGA_REQ#
{30} CLK_PCIE_LAN#
{30} CLK_PCIE_LAN
{30} PCIE_CLK_LAN_REQ#
{33} CLK_PCIE_WLANN
{33} CLK_PCIE_WLANP
{33} PCIE_CLK_WLAN_REQ#
{31} CLK_PCIE_SSDN
{31} CLK_PCIE_SSDP
{31} PCIE_CLK_SSD_REQ#
PCIE_CLK_VGA_REQ#
PCIE_CLK_LAN_REQ#
PCIE_CLK_WLAN_REQ#
PCIE_CLK_LAN_REQ#_DOCK
PCIE_CLKREQ4#
PCIE_CLK_SSD_REQ#
TP72
TP73
TP38
TP39
C3A
R568 *SSD@0_2
R570 *SSD@0_2
CLKOUT_PCIE_N0
CLKOUT_PCIE_P0
GPP_B5/SRCCLKREQ0#
CLKOUT_PCIE_N1
CLKOUT_PCIE_P1
GPP_B6/SRCCLKREQ1#
CLKOUT_PCIE_N2
CLKOUT_PCIE_P2
GPP_B7/SRCCLKREQ2#
CLKOUT_PCIE_N3
CLKOUT_PCIE_P3
GPP_B8/SRCCLKREQ3#
CLKOUT_PCIE_N4
CLKOUT_PCIE_P4
GPP_B9/SRCCLKREQ4#
CLKOUT_PCIE_N5
CLKOUT_PCIE_P5
GPP_B10/SRCCLKREQ5#
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
GPD8/SUSCLK
XTAL24_IN
XTAL24_OUT
XCLK_BIASREF
RTCX1
RTCX2
SRTCRST#
RTCRST#
TBT
10 OF 20
REV = 1
PCH_SUSCLK_R
R242 *SSD@0_4_S
PCH_SUSCLK {31}
XTAL24_IN
XTAL24_OUT
+1.0V_DEEP_SUS
XCLK_BIASREF
R169 2.7K/F_4
R176 *60.4/F_4
RTC_X1
RTC_X2
SRTC_RST#
RTC_RST#
Co-lay 60ohm 1% to GND
for Connonlake-U use
CLK_REQ/Strap Pin(CLG)
+3V
10K_4 R289 PCIE_CLK_LAN_REQ#_DOCK
10K_4 R712 PCIE_CLK_WLAN_REQ#
10K_4 R706 PCIE_CLK_LAN_REQ#
10K_4 R715 PCIE_CLK_VGA_REQ#
10K_4 R704 PCIE_CLKREQ4#
10K_4 R705 PCIE_CLK_SSD_REQ#
U38I
CSI-2
CSI2_DN0 … CSI2_DN11 / CSI2_DP0 … CSI2_DP11
CSI2_CLKN0 … CSI2_CLKN3 / CSI2_CLKP0 … CSI2_CLKP3
CSI2_COMP
GPP_D4/FLASHTRIG
EMMC
GPP_F13/EMMC_DATA0
GPP_F14/EMMC_DATA1
GPP_F15/EMMC_DATA2
GPP_F16/EMMC_DATA3
GPP_F17/EMMC_DATA4
GPP_F18/EMMC_DATA5
GPP_F19/EMMC_DATA6
GPP_F20/EMMC_DATA7
GPP_F21/EMMC_RCLK
GPP_F22/EMMC_CLK
GPP_F12/EMMC_CMD
EMMC_RCOMP
9 OF 20
CSI2_COMP R182 100/F_4
EMMC_RCOMP R672 200/F_4
RTC Clock 32.768KHz (RTC)<RTC>
B2B
C763 15P/50V/NPO_4
C755 15P/50V/NPO_4
Y5 32.768KHz
R669 10M_4
RTC_X1
RTC_X2
RTC Circuitry (RTC)<RTC>
RTC Power trace width 20mils.
VSTBY_FSPI
+3V_RTC_2
+3V_RTC
R442 1.5K_4
R441 45.3K_4
R434 1K_4
+3V_RTC_1
D14 DB2J40600L
D13 DB2J40600L
R436 *45.3K_4
CN21 94-0013-01
R294 20K/F_4
R300 20K/F_4
C415 1U/6.3V_4X
C423 1U/6.3V_4X
C548 1U/6.3V_4X
RTC_RST#
SRTC_RST#
GRTC1 *JUMP
EC14 *E@220P/50V_4
Q25 2N7002K
EC_RTC_RST
EC_RTC_RST {36}
R309 10K_4
External Crystal and Green Clock
XTAL24_IN
XTAL24_OUT
R177 1M_4
C242 12P/50V_4
C243 12P/50V_4
24MHZ +-30PPM Y1
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SKYLAKE 12/15 (CLK/EMMC)
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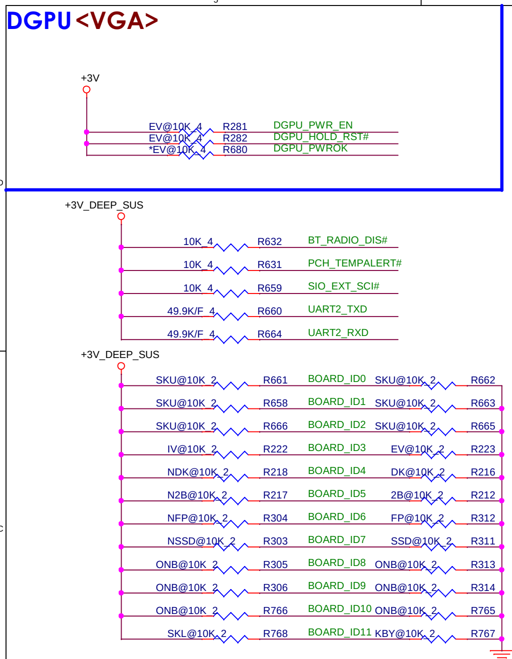
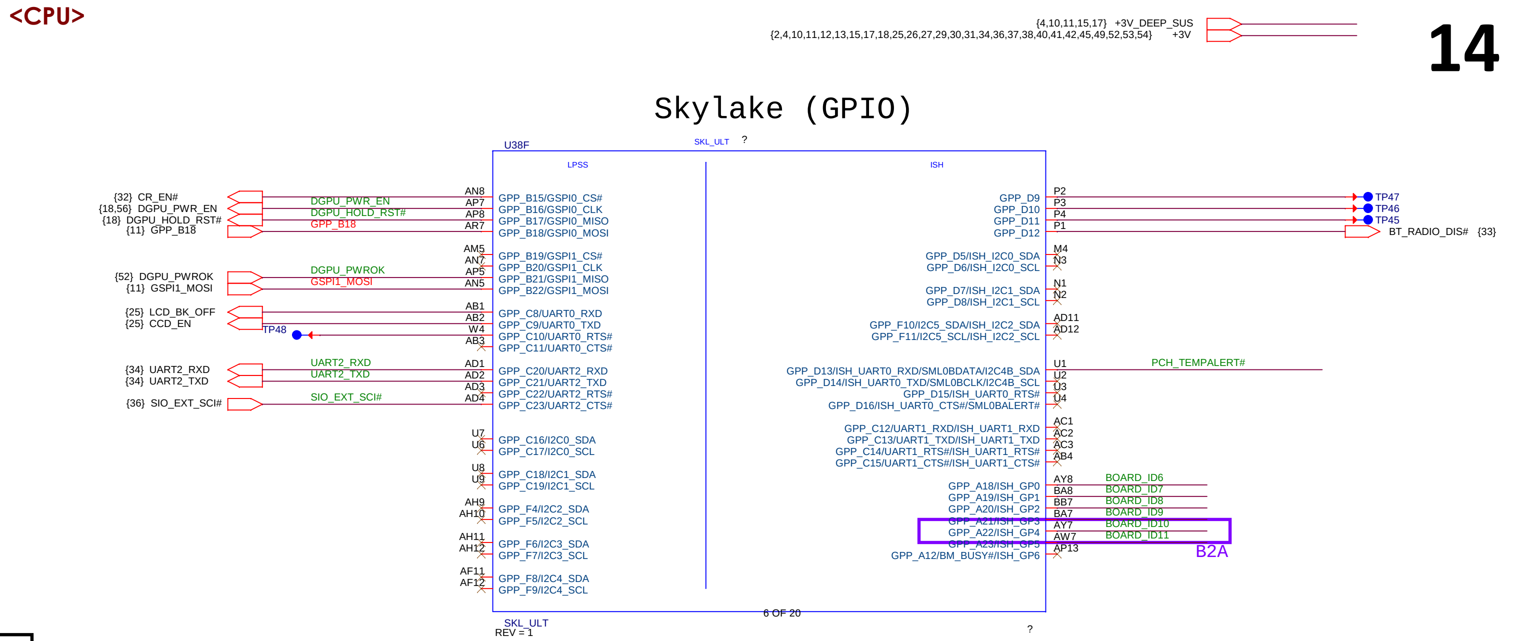
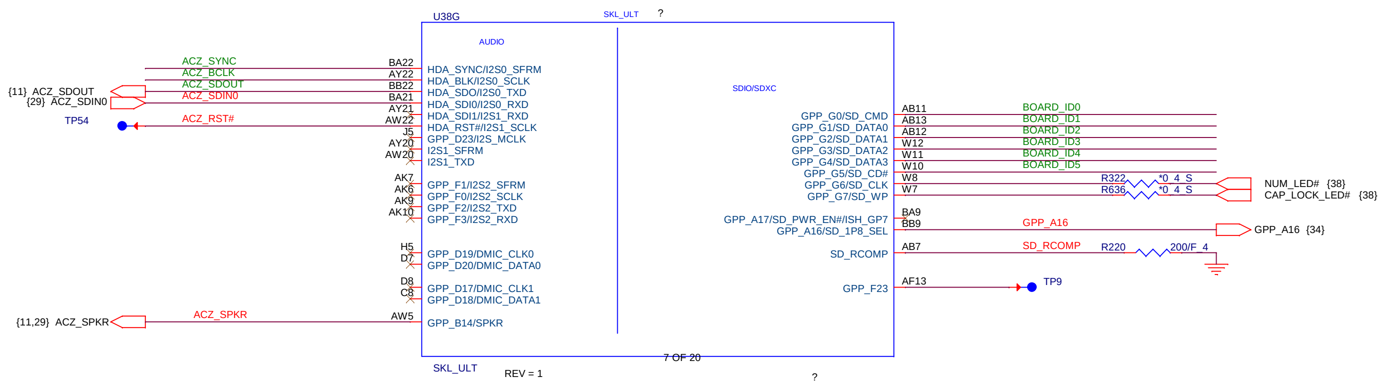
Skylake (GPIO)



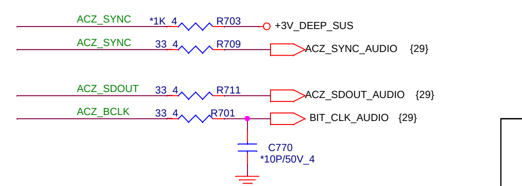




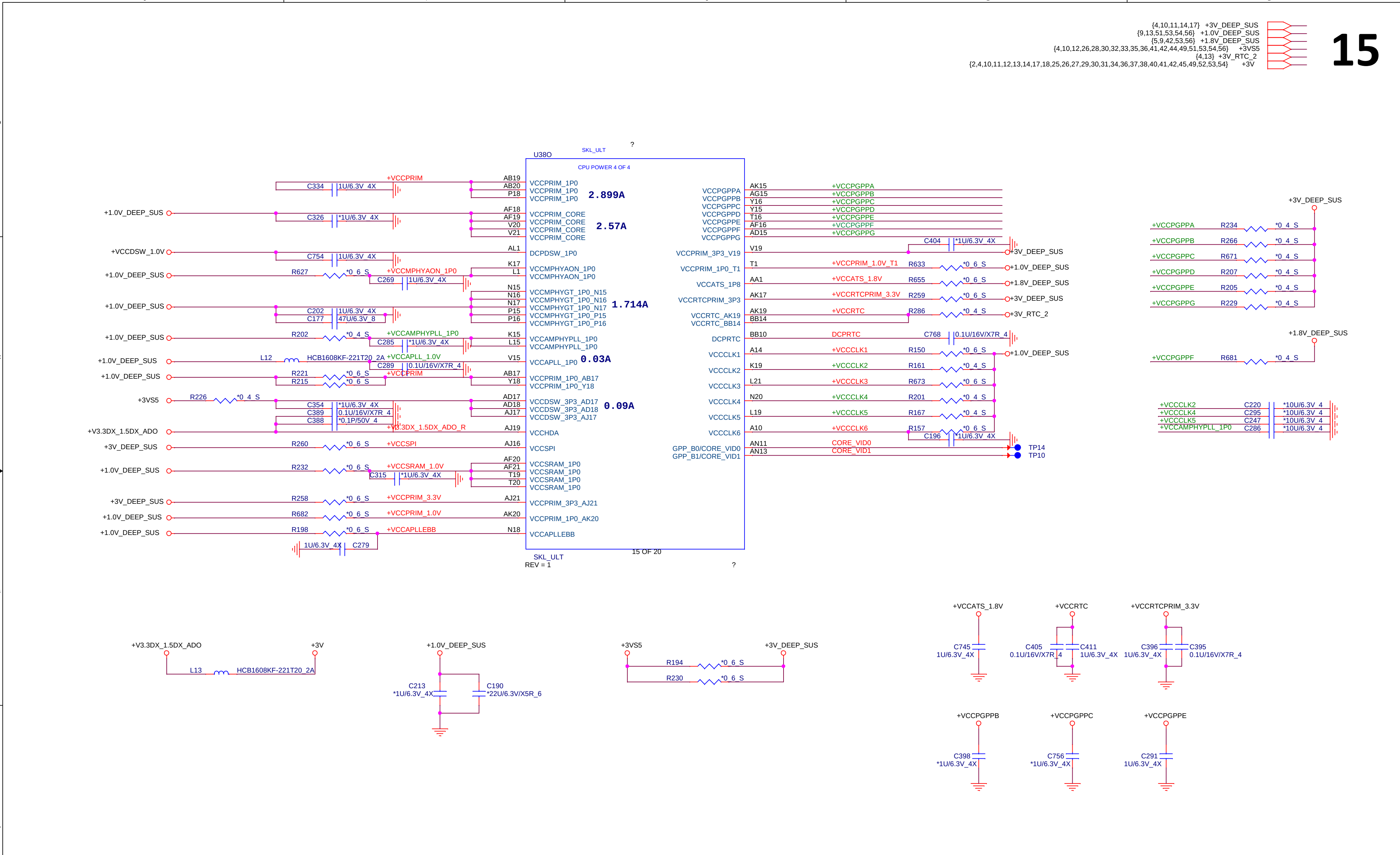
Sku	Model	BOARD_ID0	BOARD_ID1	BOARD_ID2
0	E42(R310_14)	0	0	0
1	E52(R310_15)	0	0	1
2	V310_14	0	1	0
3	V310_15	0	1	1
4	Tianyi310_14	1	0	0
5	Tianyi310_15	1	0	1
6	Reserved	1	1	0
7	Reserved	1	1	1

BOARD_ID3	Hi = UMA	Lo = Discrete
BOARD_ID4	Hi = wo Prolink	Lo = w Prolink
BOARD_ID5	Hi = wo 2nd Battery	Lo = w 2nd Battery
BOARD_ID6	Hi = wo Figure Printer	Lo = w Figure Printer
BOARD_ID7	Hi = wo SSD	Lo = w SSD
On Board Memory	[1, 1, 1] = Samsung K4A8G165WB-BCRC [1, 1, 0] = Micro MT40A512M16JY-083E:B [1, 0, 1] = SMART [1, 0, 0] = Teikon [0, 1, 1] = Samsung K4A8G165WB-BCPB [0, 1, 0] = Micro MT40A512M16HA-083E:A [0, 0, 1] = Hynix H5AN8G6NAFR-TFC [0, 0, 0] = No Memory Down	
BOARD_ID10		
BOARD_ID9		
BOARD_ID8		
BOARD_ID11	Hi = Skylake	Lo = Kaby lake

D3A
B2A
C3A
B2A



15



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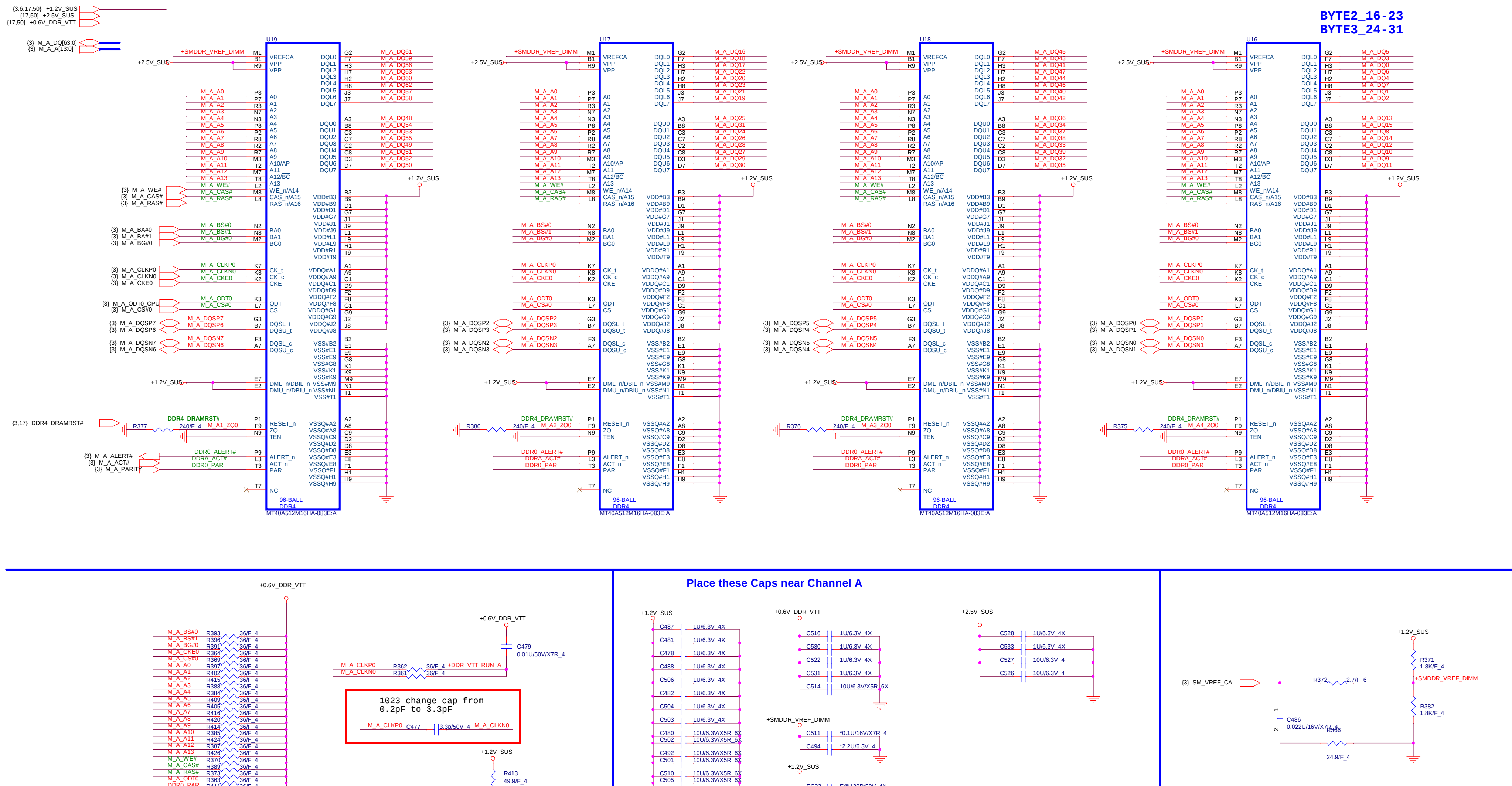
<DDR> (Memory Down)

BYTE2_16-23
BYTE3_24-31



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DDR4 MEMORY DOWN | 1A
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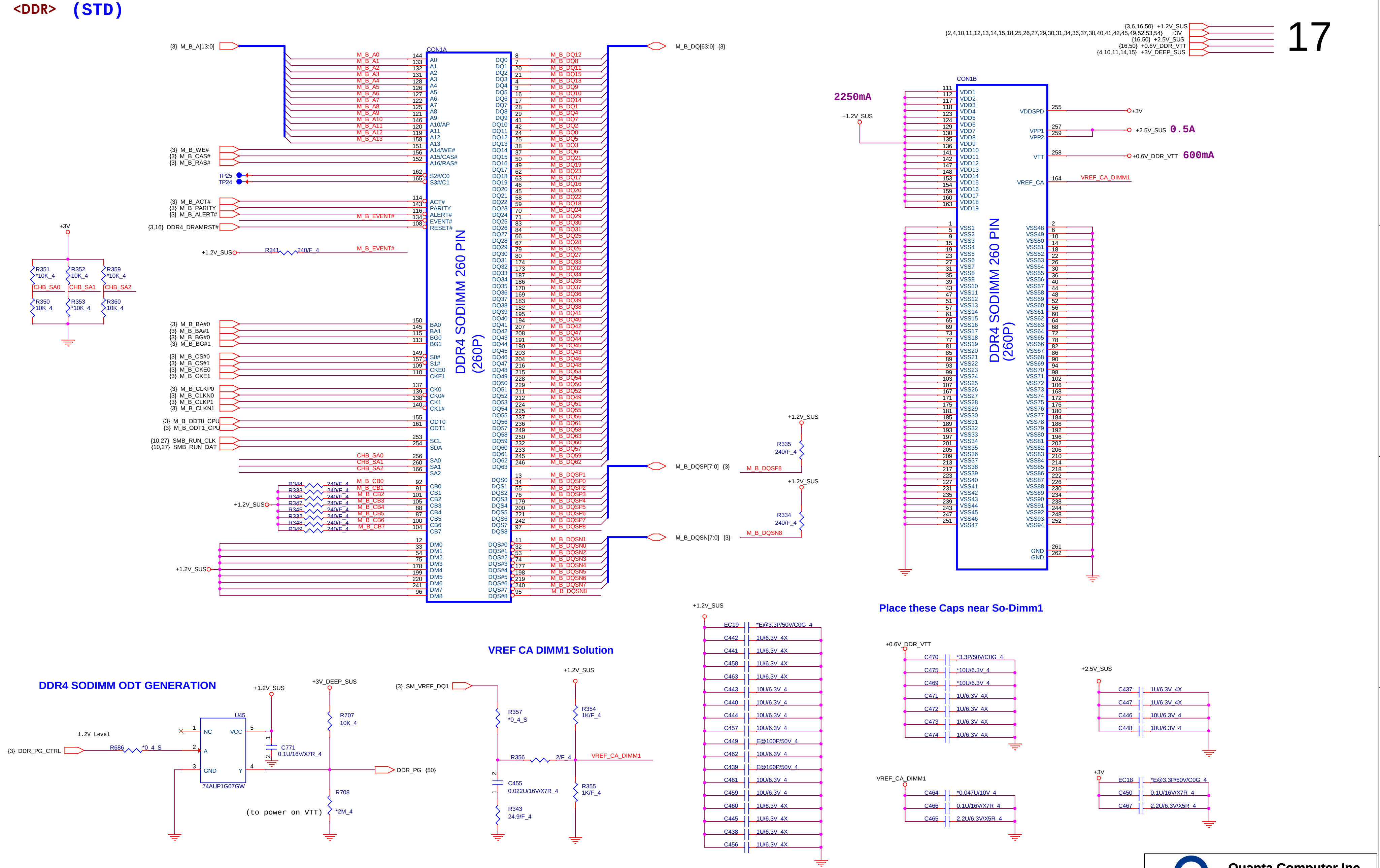
<DDR> (STD)



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Size	Document Number	Rev
	DDR4 DIMM1-RVS	1A

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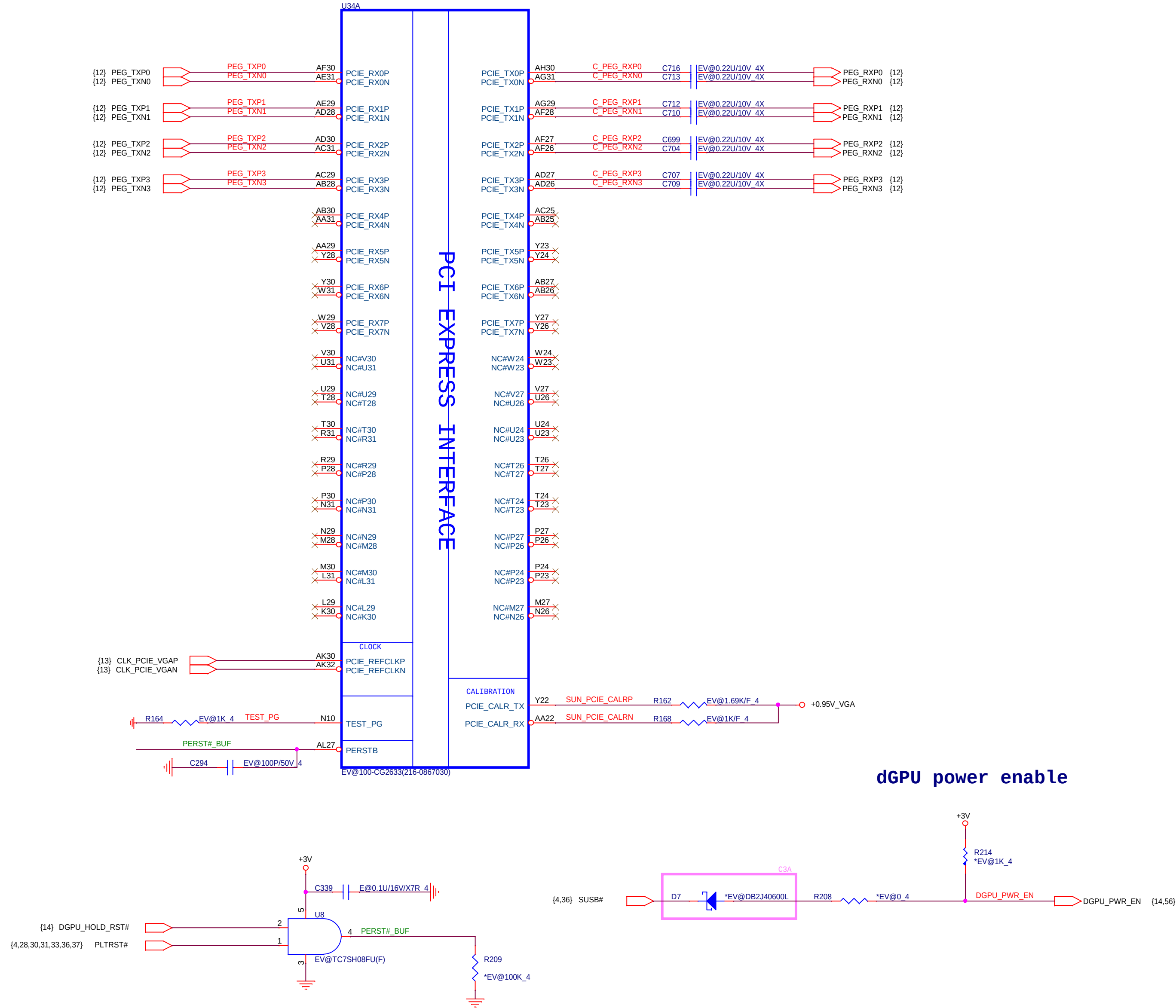
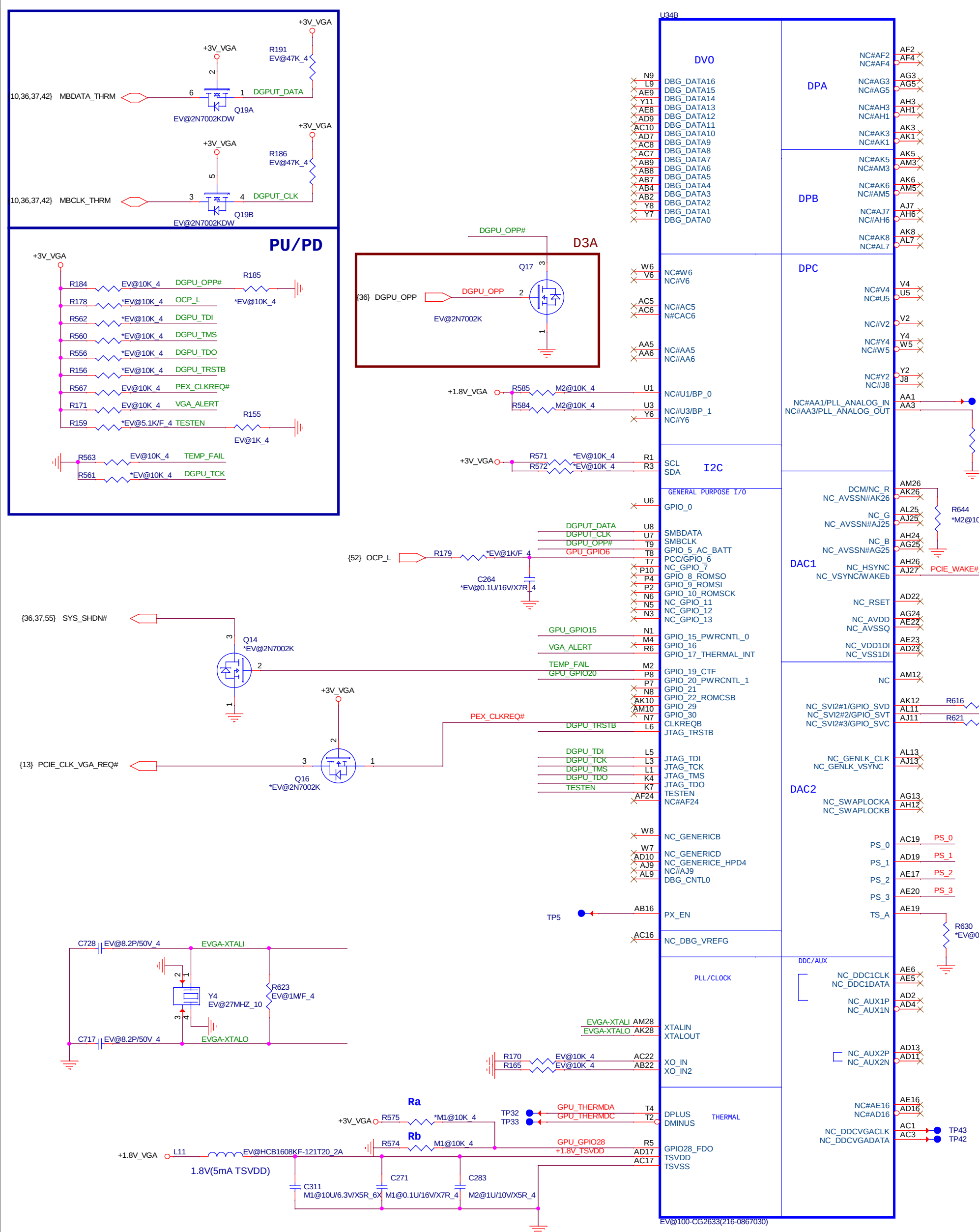
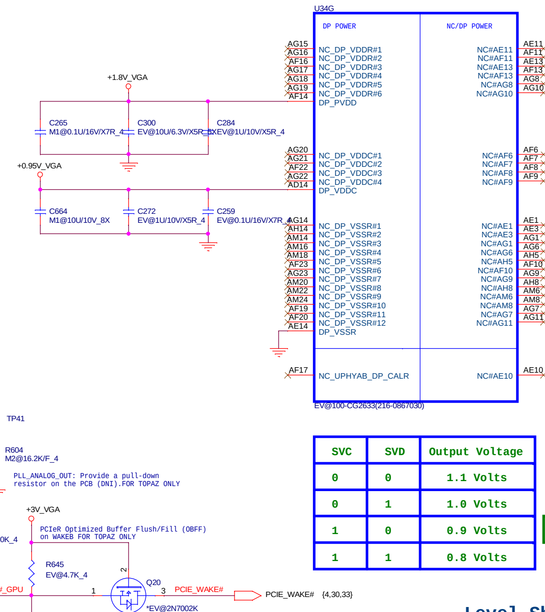


Quanta Computer Inc.		
PROJECT : LV6		
Size	Document Number: JET_S3_PCIE_Interface	Rev 1A
Date: Friday, March 11, 2016	Sheet 18 of 61	

The SMBus slave ID is default 0x41

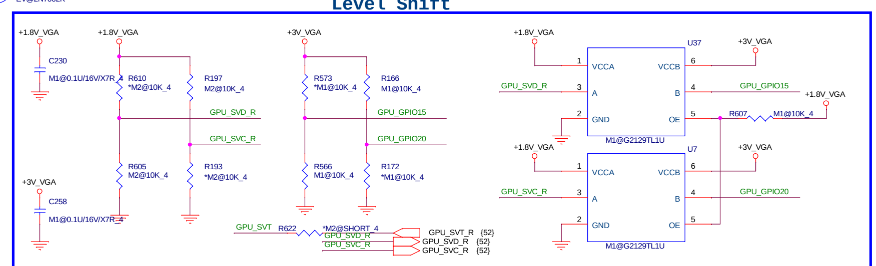




SVC	SVD	Output Voltage
0	0	1.1 Volts
0	1	1.0 Volts
1	0	0.9 Volts
1	1	0.8 Volts

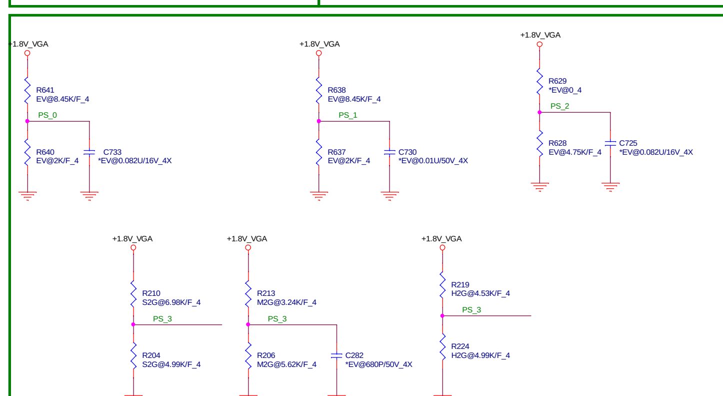
R16M Boot

Level Shift



	R16M-M1-30	R16M-M2-50
PS0[5:1]	11001	11001
PS1[5:1]	11001	11001
PS2[5:1]	11000	11000
PS3[5:1]	11xxx	11xxx

PS_3[3:1]	Vendor	Type	Vendor P/N	R3pu	R3pd
011	Samsung- 2G	256Mx16 *4, 900Mhz	K4W4G1646E-BC1A	6.98K	4.99K
100	Hynix- 2G	256Mx16 *4, 900Mhz	H5TC4G63CFR-N0C	4.53K	4.99K
101	Micro- 2G	256Mx16 *4, 900Mhz	MT41J256M16LY-091G:N	3.24K	5.62K

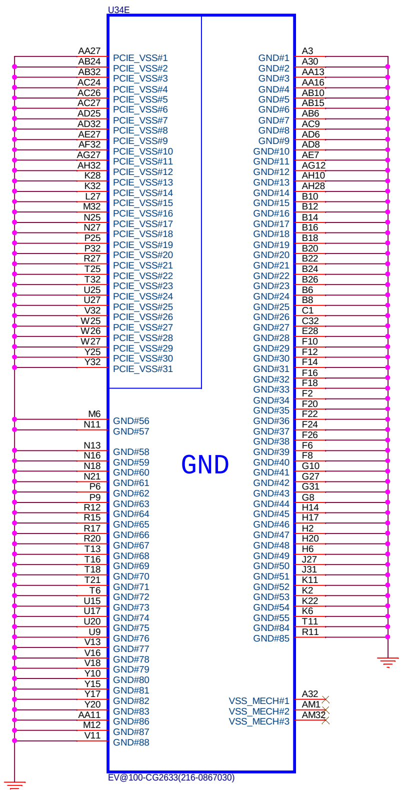


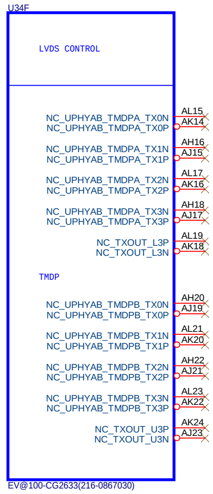
BIT[5:4]	C (nF)
00	680
01	82
10	10
11	NC

BIT[3:1]	Rpu	Rpd
000	NC	4750
001	8450	2000
010	4530	2000
011	6980	4990
100	4530	4990
101	3240	5620
110	3400	10000
111	4750	NC

M1 MLPS setting
M2 no mount

M1 ONLY: stuff Ra=> disable MLPS
stuff Rb=> enable MLPS





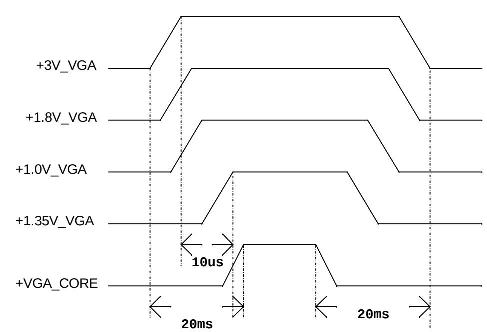
All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µs.

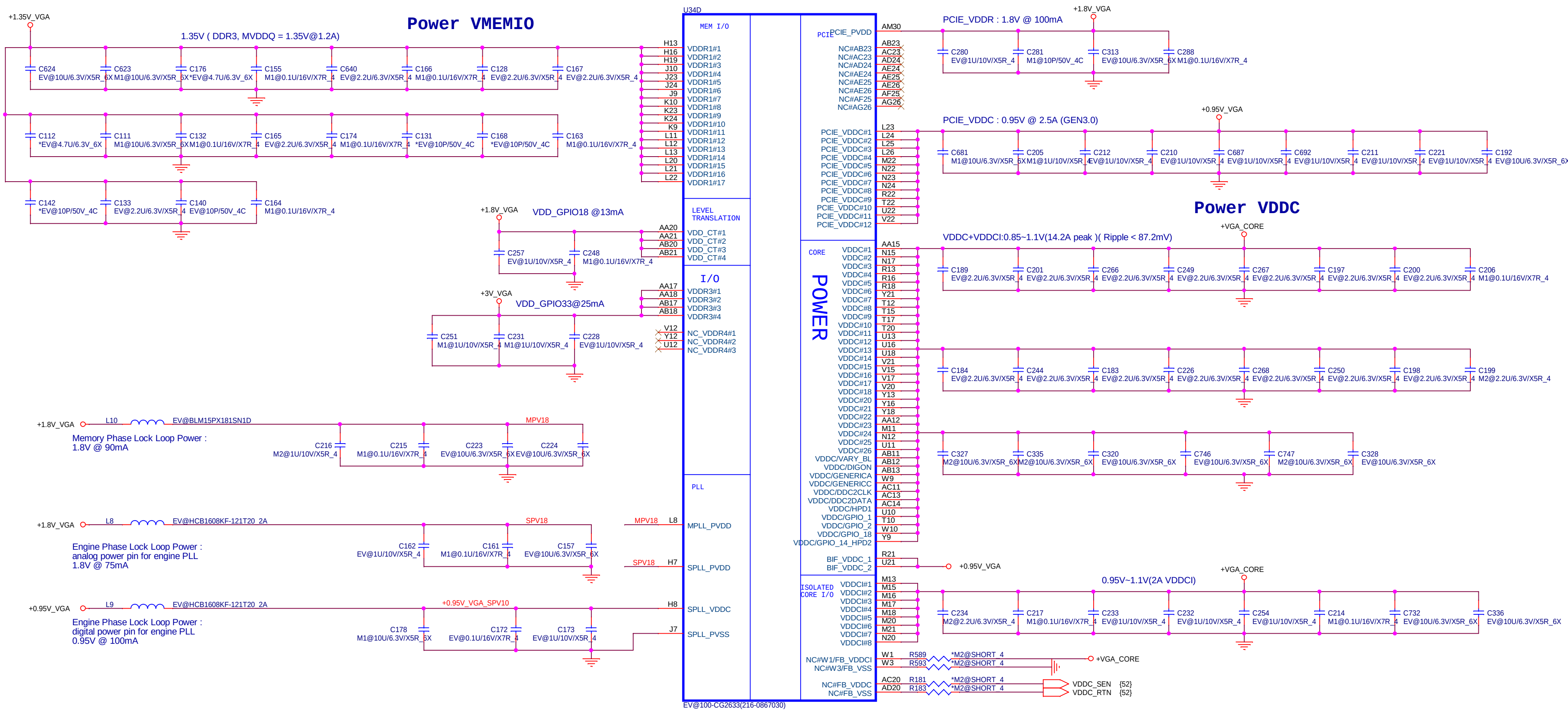
It is recommended that the 3.3-V rail ramp up first

The 3.3-V, 1.8-V, and 1.0-V rails must reach their ready state at least 10 µs before VDDC, VDDCI, and VMEMIO start to ramp up.

For power down, reversing the ramp-up sequence is recommended.

Power Up/Down Sequence





Quanta Computer Inc.

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	JET_S3_Power	1A

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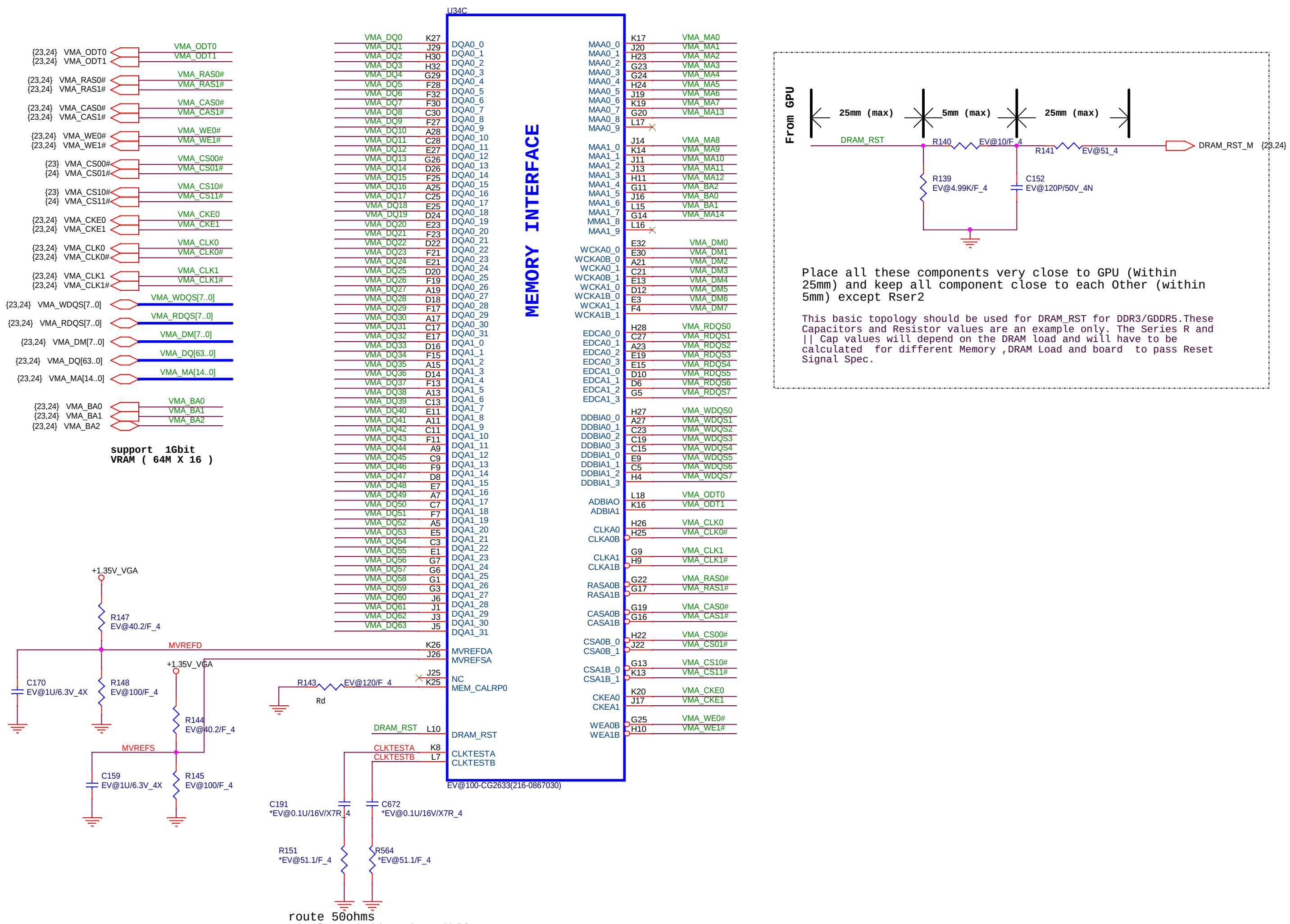


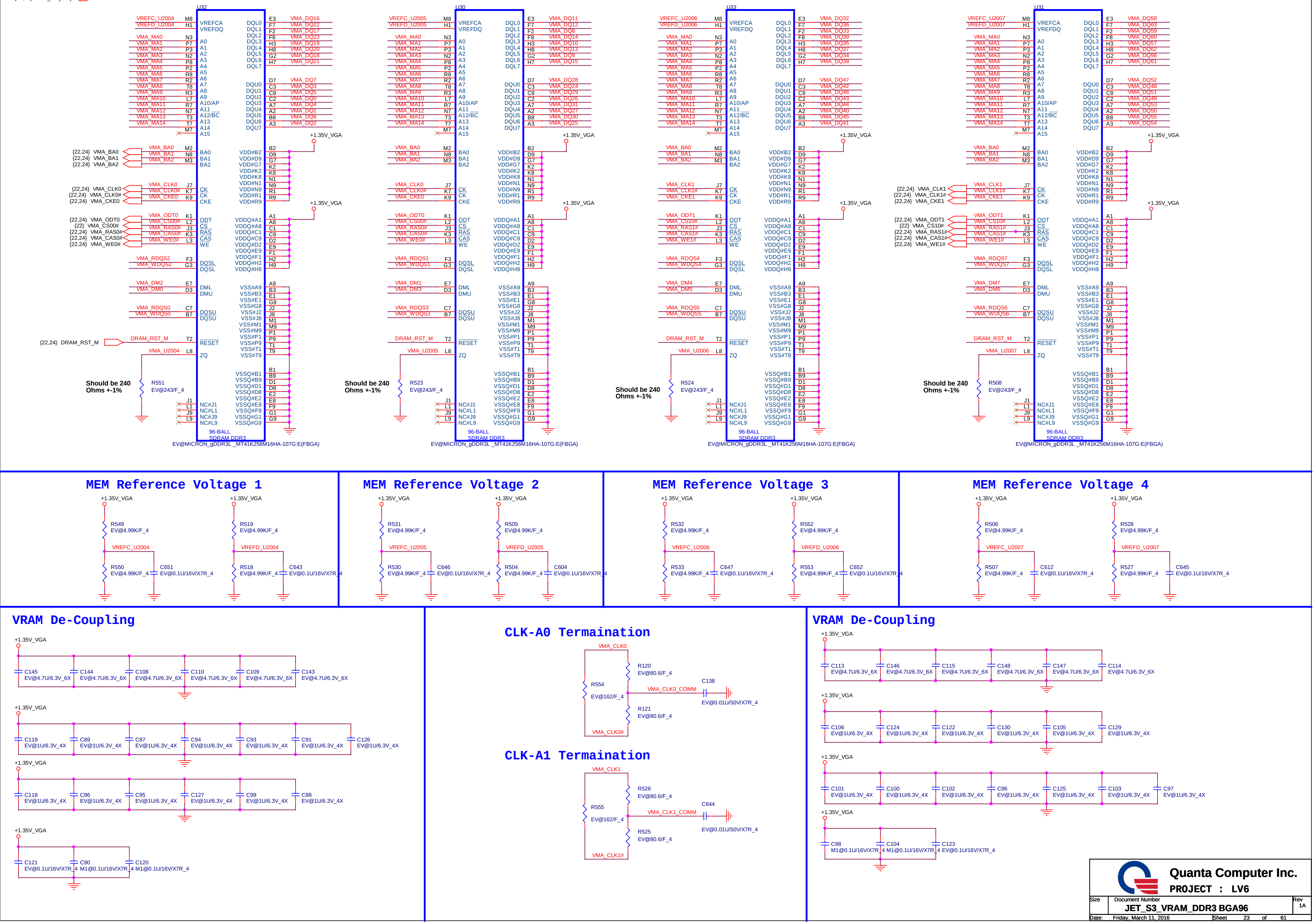
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

support 1Gbit
VRAM (64M X 16)

route 50ohms
single-ended/100ohms diff
and keep short

Channel A _Rank0: 2Gb/4Gb gDDR3L



Quanta Computer Inc.

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Size	Document Number	Rev
	JET_S3_VRAM_DDR3 BGA96	1A

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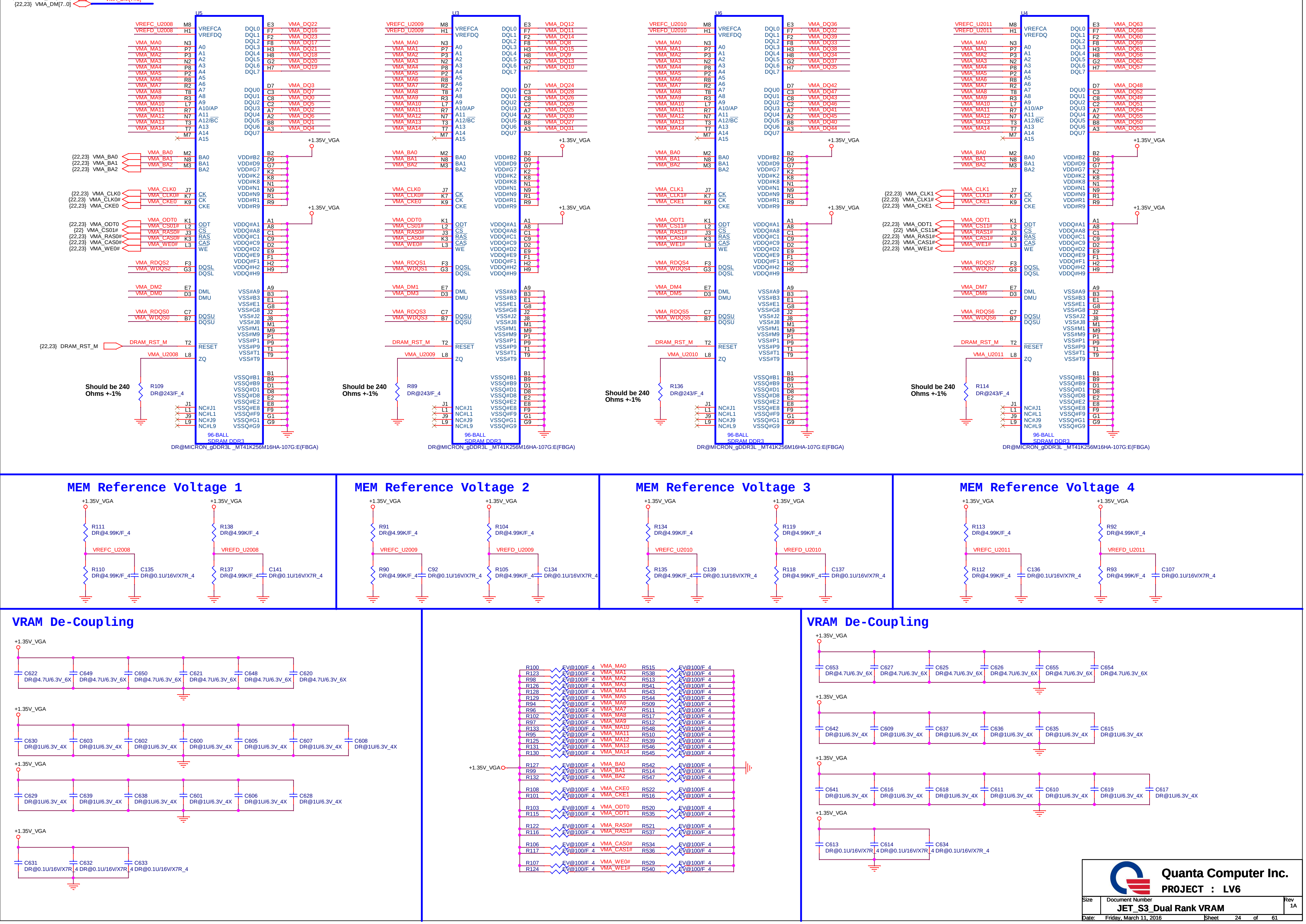
Channel A _Rank1: DR@2Gb/4Gb gDDR3L



Quanta Computer Inc.

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Document Number: JET_S3_Dual Rank VRAM

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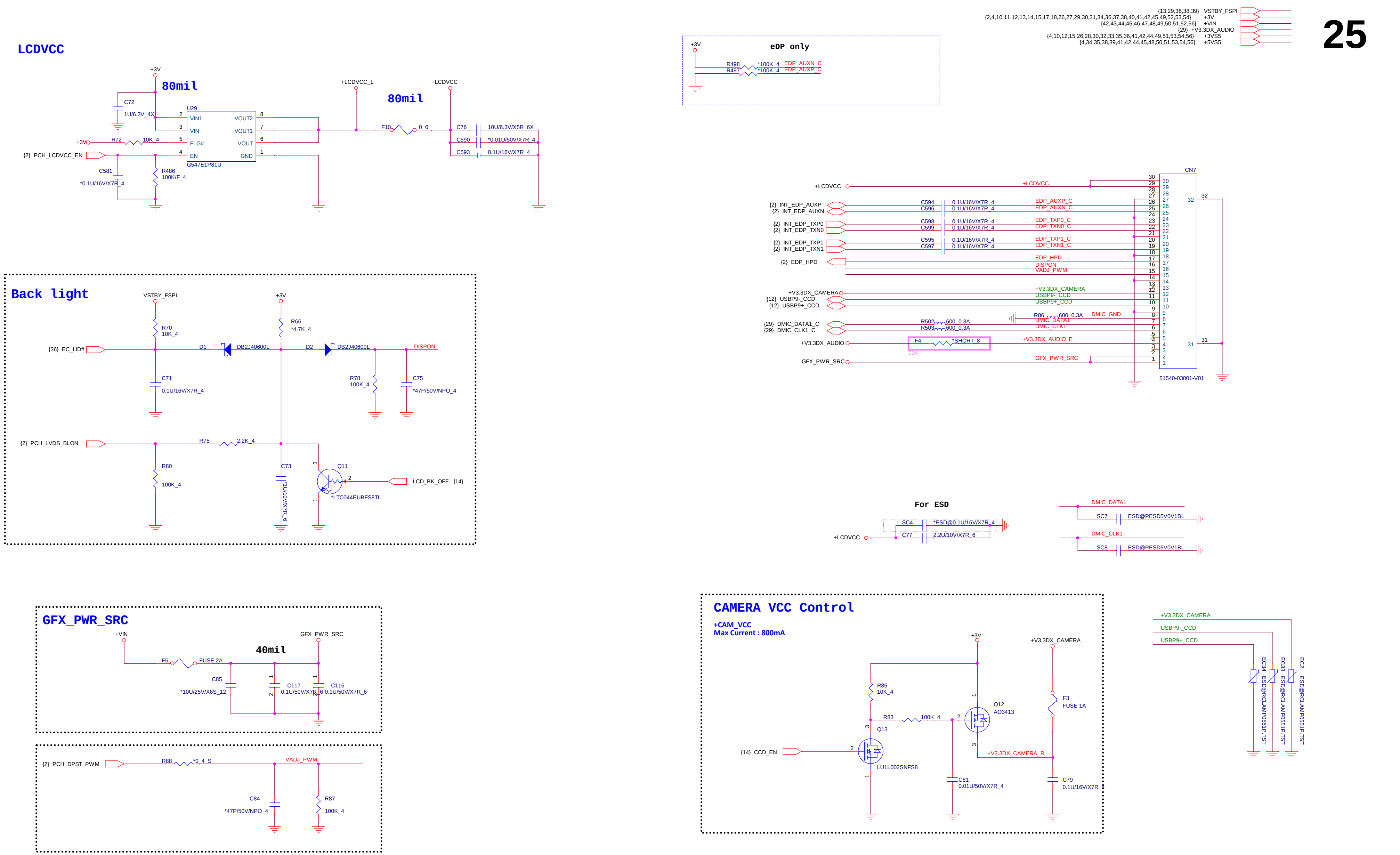

Quanta Computer Inc.

PROJECT : LV6

Size	Document Number	Rev
	LCD/CAMERA/MIC	1A

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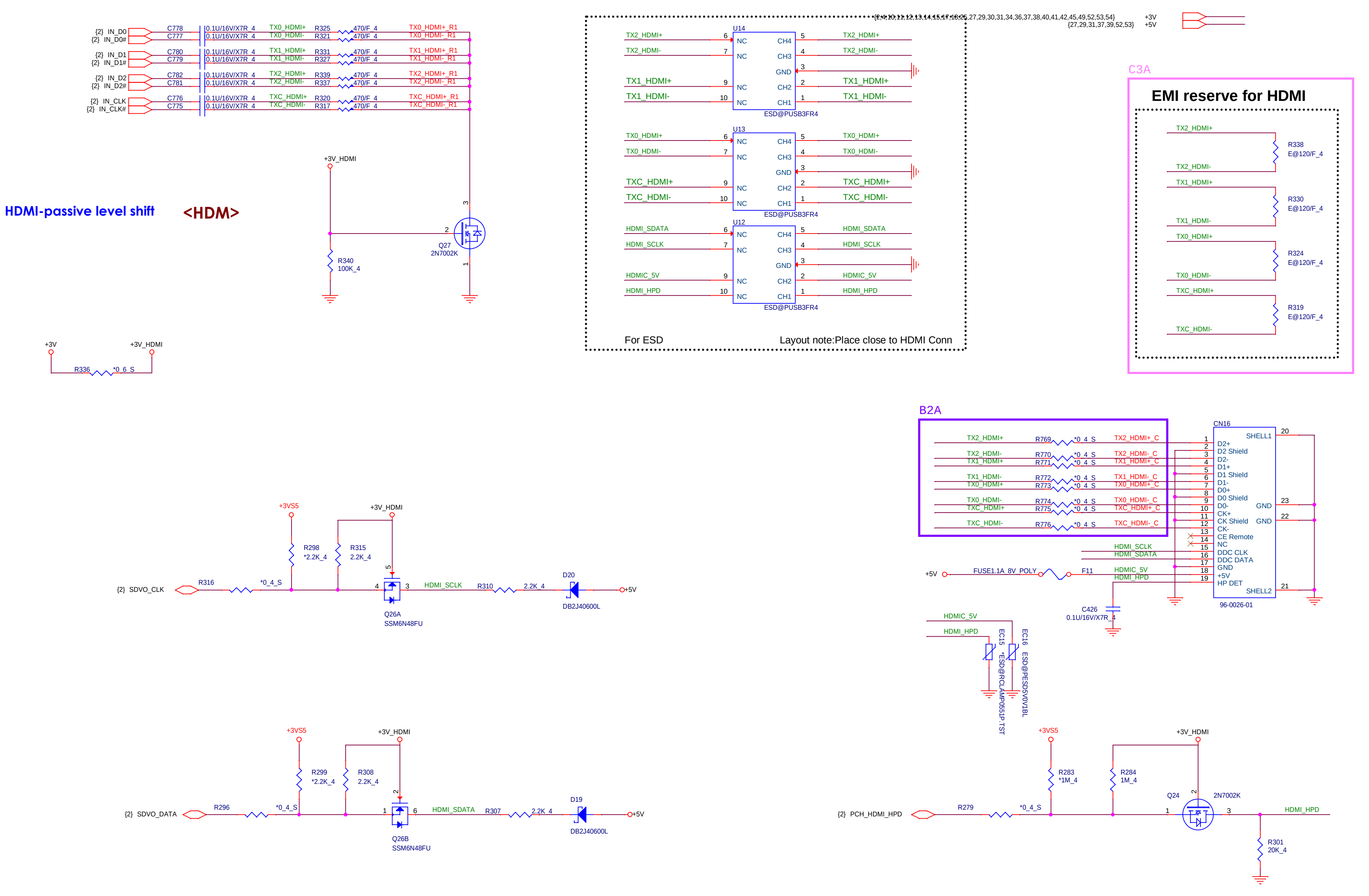
HDMI Conn <HDM>



Quanta Computer Inc.
PROJECT : LV6

Size	Document Number	Rev
	HDMI CONN	1A

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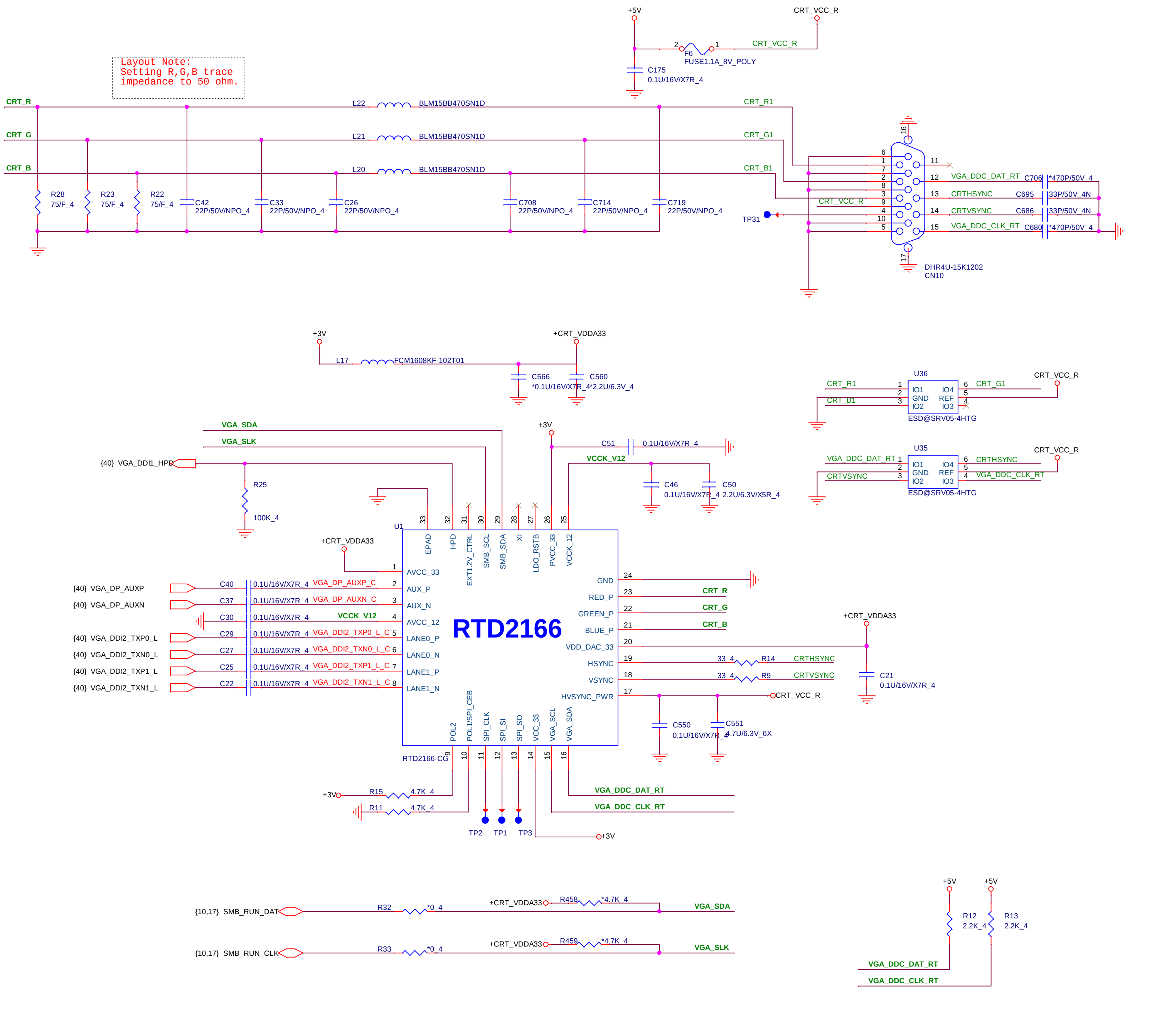
CRT Conn <CRT>

+5V {26,29,31,37,39,52,53}
+3V {2,4,10,11,12,13,14,15,17,18,25,26,29,30,31,34,36,37,38,40,41,42,45,49,52,53,54}



Quanta Computer Inc.

PROJECT : LV6

Size	Document Number	Rev
	DP to CRT(RTD2166-CG)	1A

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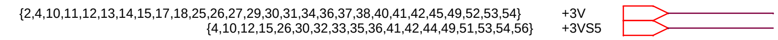
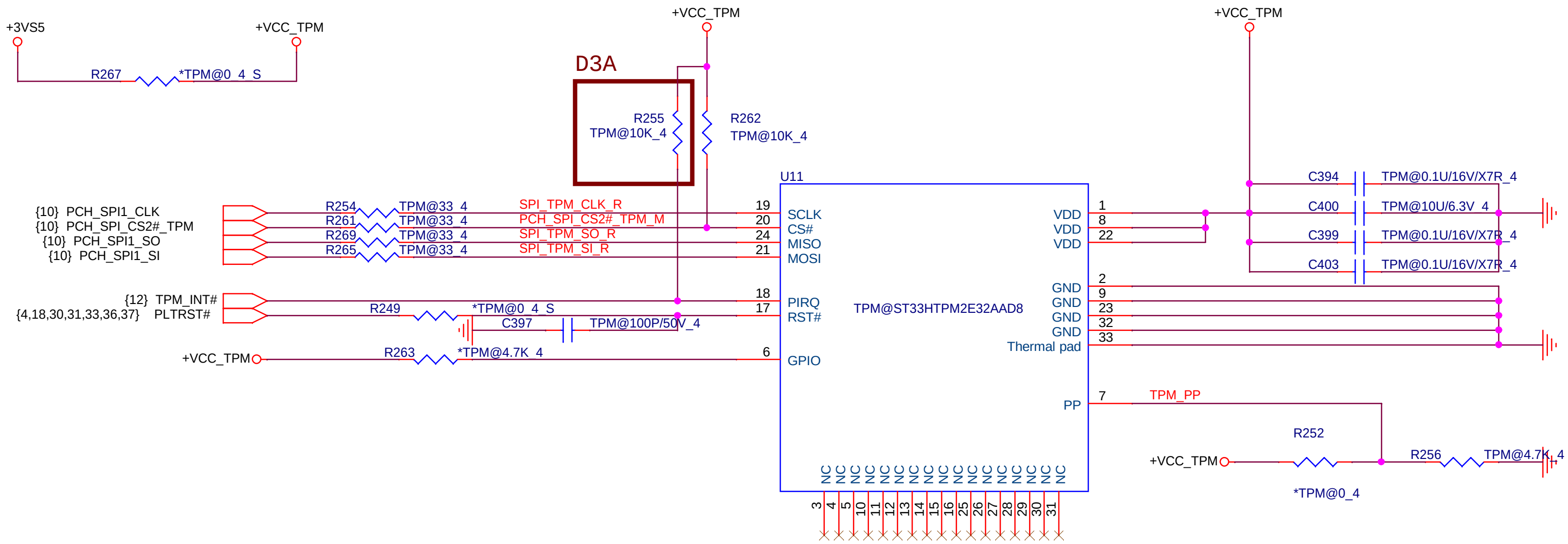
TPM <TPM>





Quanta Computer Inc.

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Size	Document Number	Rev
	TPM	1A

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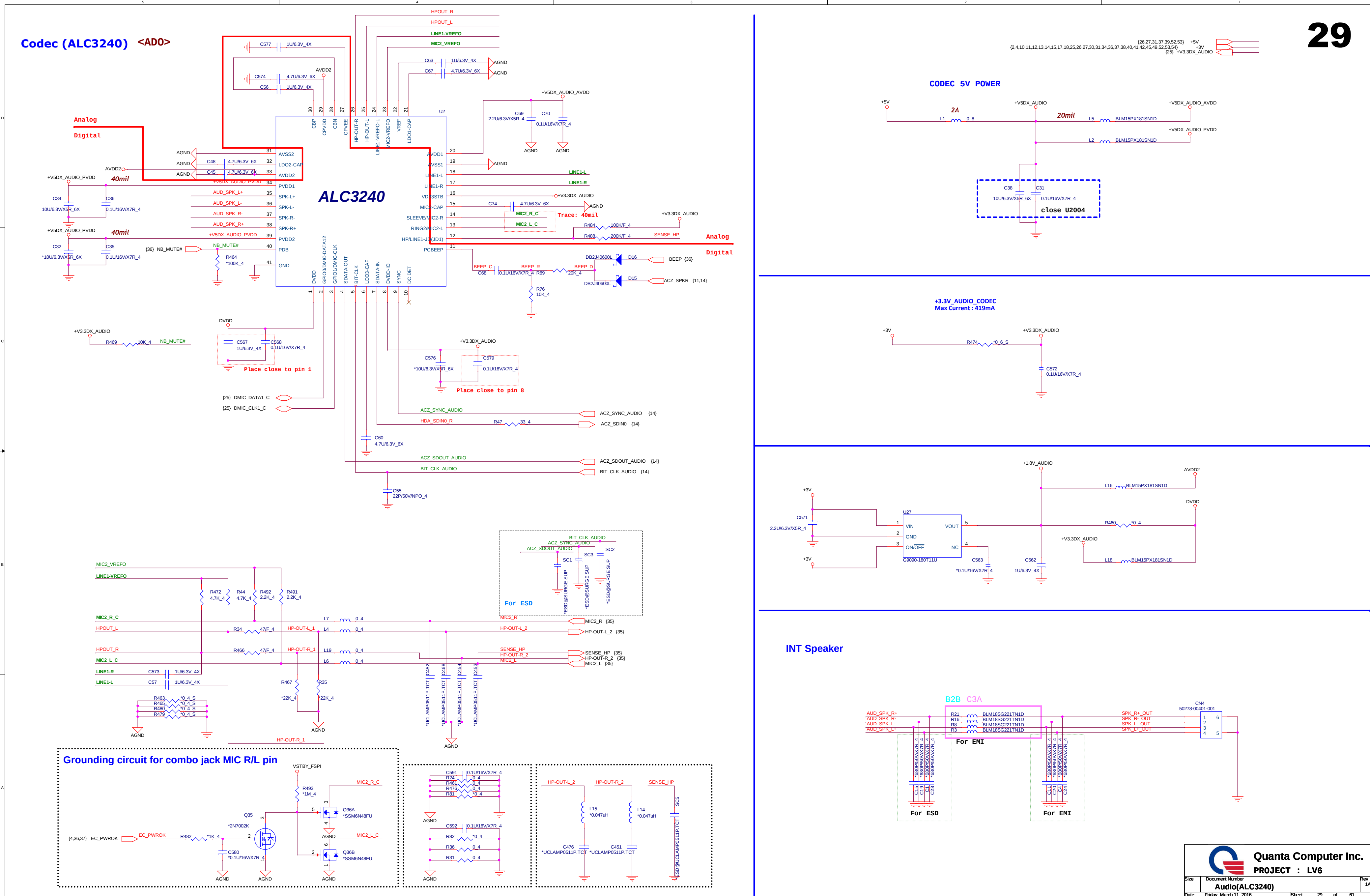

Quanta Computer Inc.

PROJECT : LV6

Size	Document Number	Rev
	Audio(ALC3240)	1A

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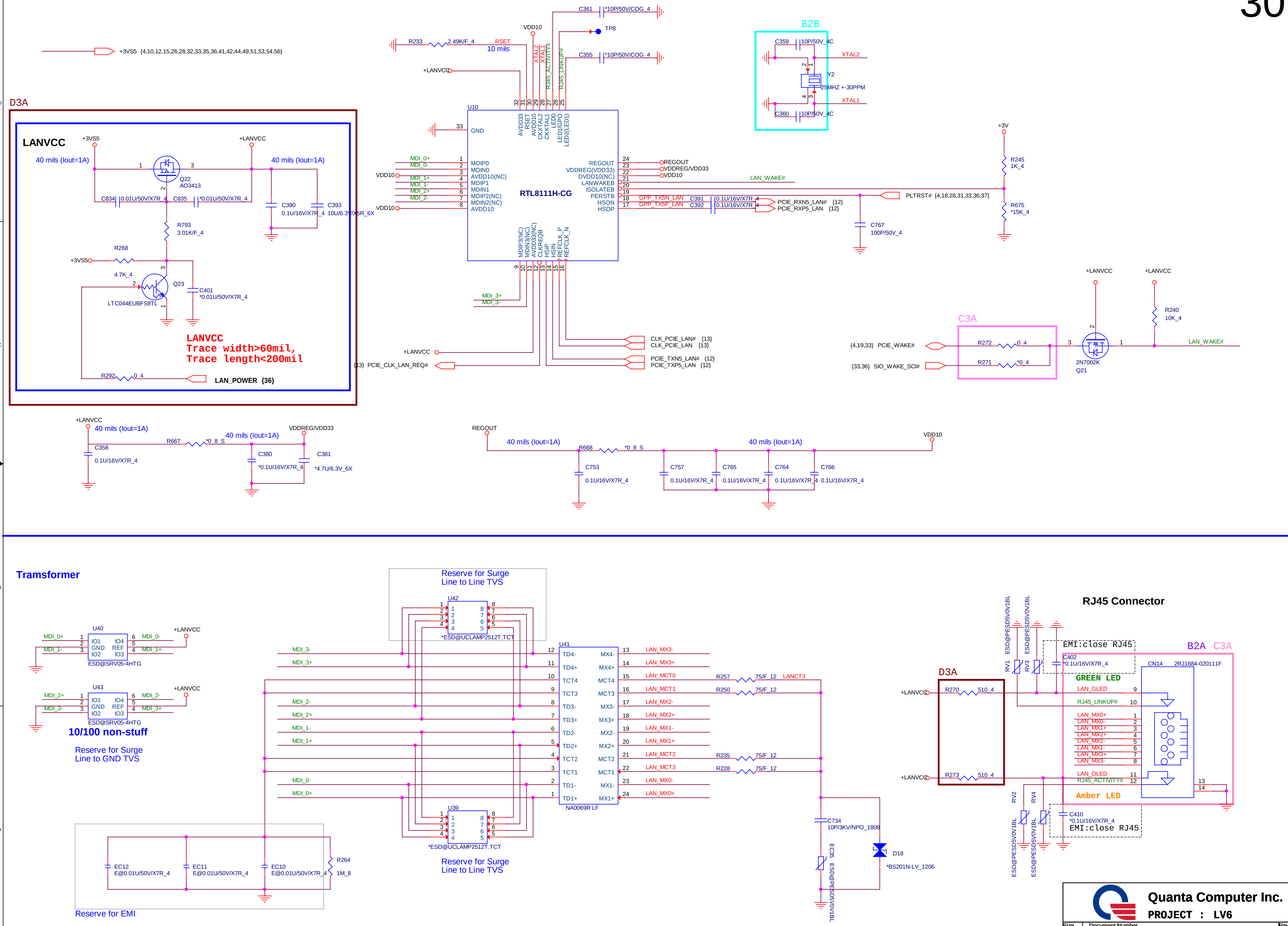
LAN LDO <LAN>



Quanta Computer Inc.	
PROJECT : LV6	
Size	Document Number: LAN and Switch(TS3L500AE)
Rev	1A
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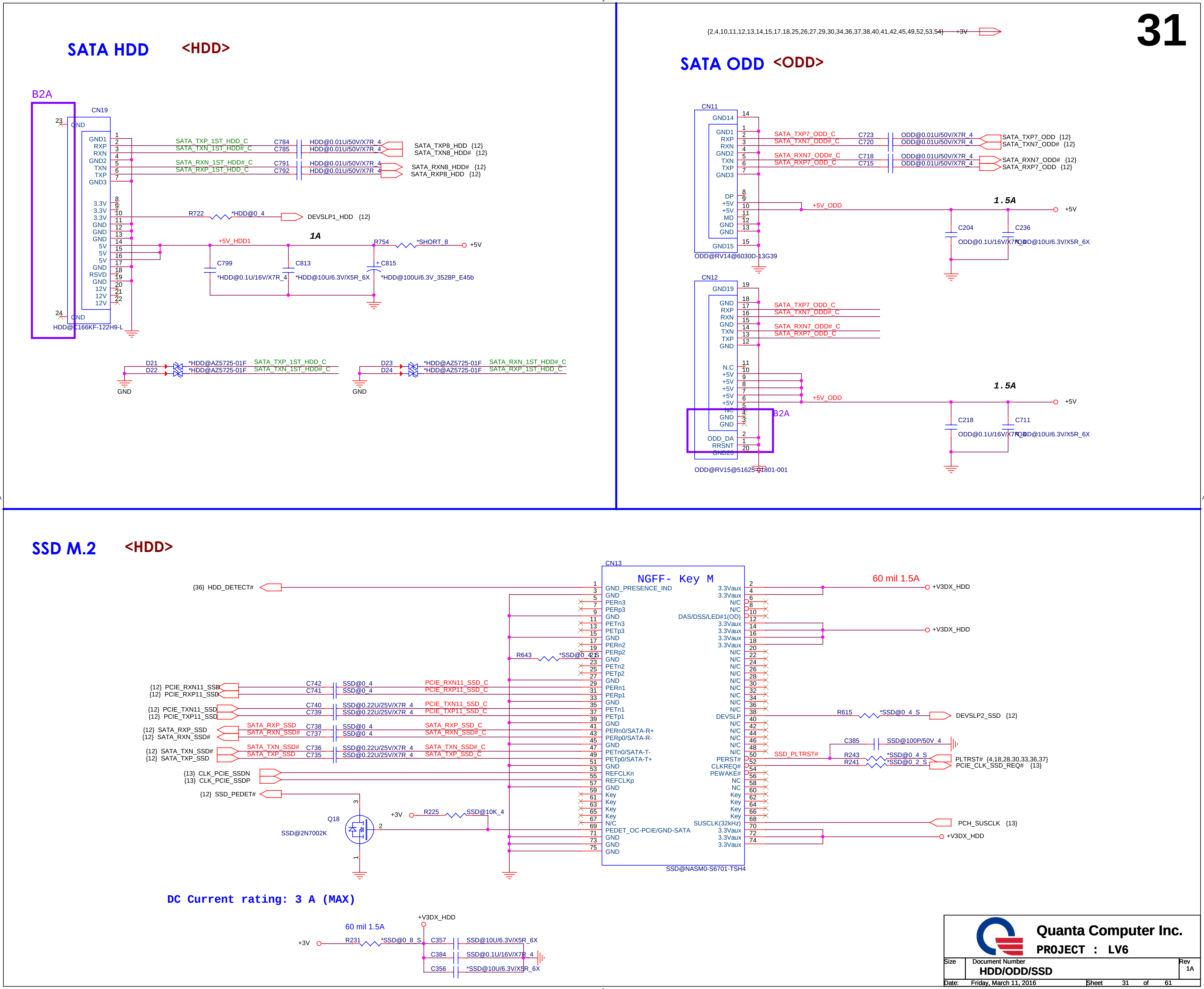

Quanta Computer Inc.

PROJECT : LV6

Size	Document Number	Rev
	HDD/ODD/SSD	1A

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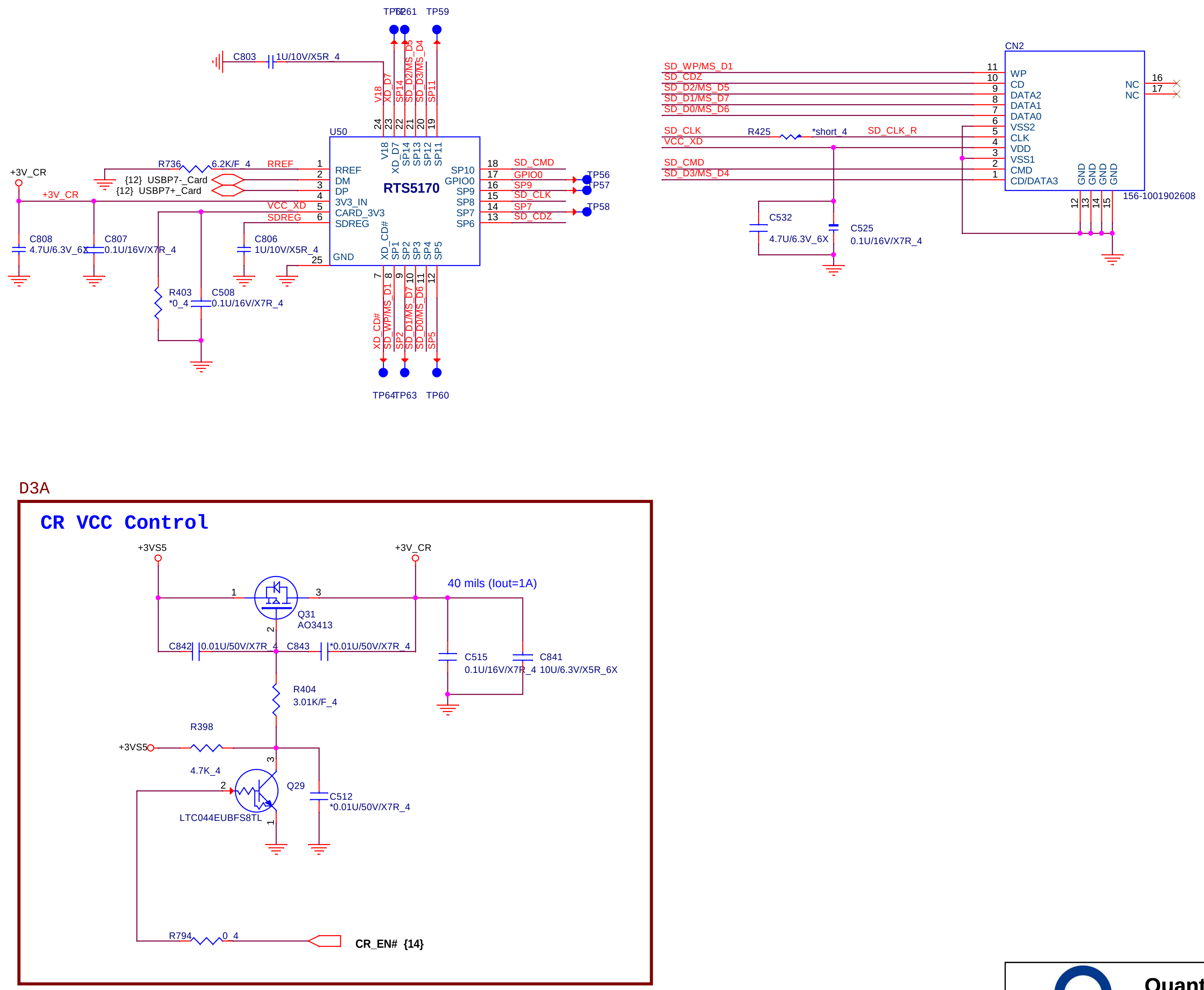
Card Reader(RTS5170) <CRD>



Quanta Computer Inc.			
PROJECT : LV6			
Size	Document Number: Card Reader		Rev 1A
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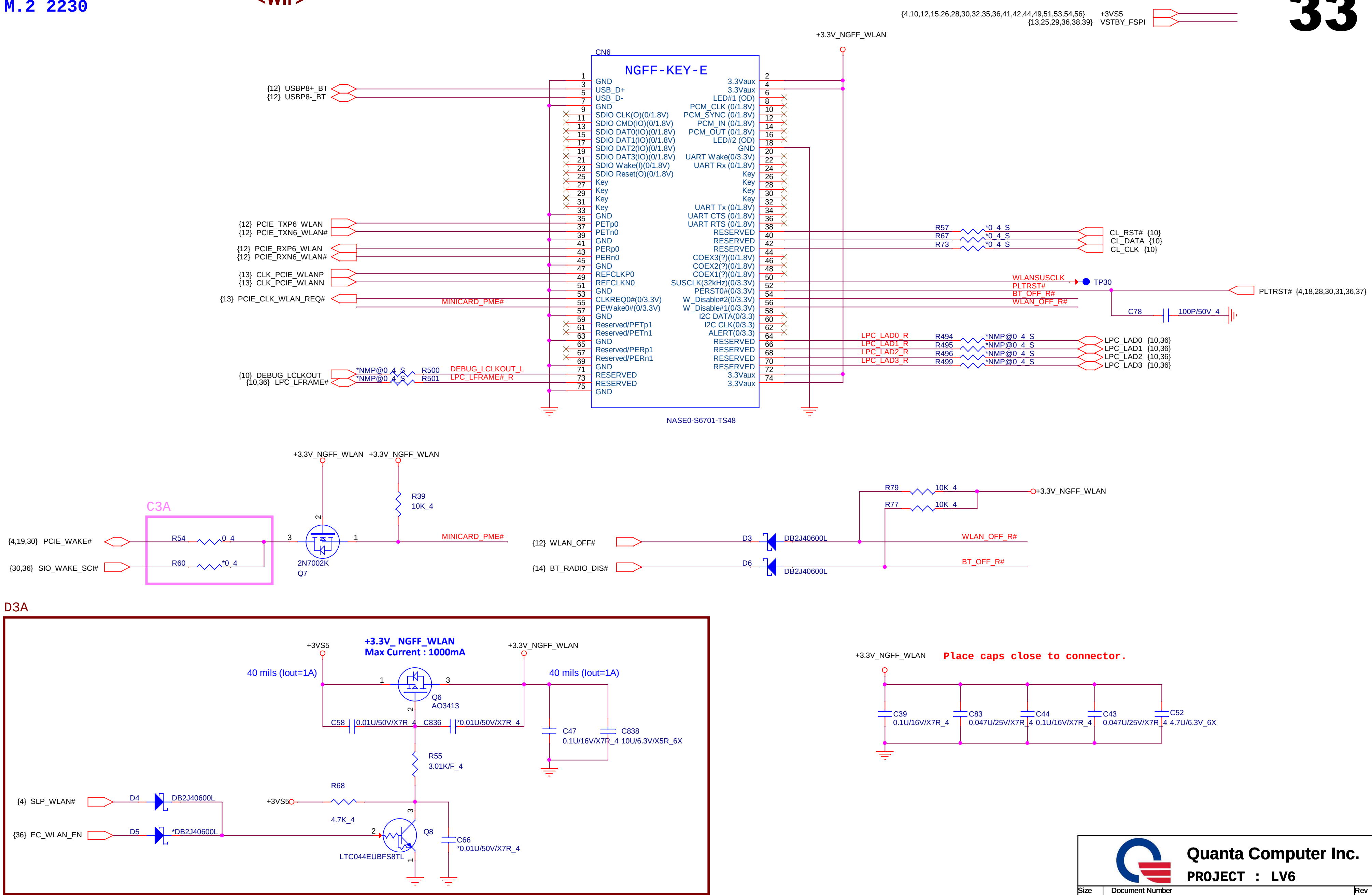
NGFF WiFi/BT connector
M.2 2230

<WIF>



Quanta Computer Inc.

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Size	Document Number	Rev
	Wifi/BT NGFF	1A

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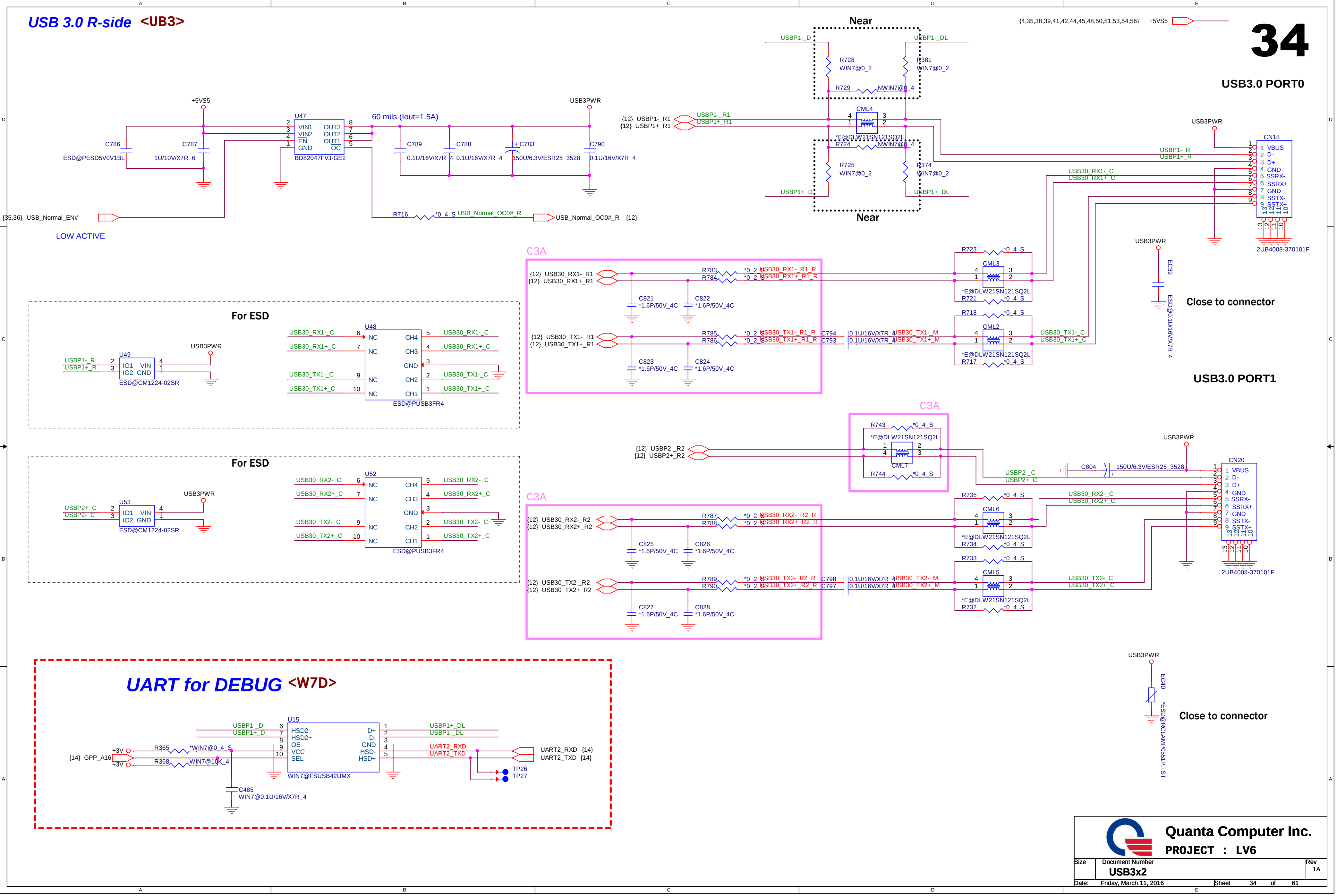

USB 3.0 R-side <UB3>
34
USB3.0 PORT0
USB3.0 PORT1
{4,35,38,39,41,42,44,45,48,50,51,53,54,56} +5VS5
Near
60 mils (Iout=1.5A)
U47 BD82047FVJ-GE2
VIN1 VIN2 EN GND OUT3 OUT2 OUT1 OC
C786 ESD@PESD5V0V1BL
C787 1U/10V/X7R_6
C789 0.1U/16V/X7R_4
C788 0.1U/16V/X7R_4
C783 150U/6.3V/ESR25_3528
C790 0.1U/16V/X7R_4
{35,36} USB_Normal_EN#
LOW ACTIVE
R716 *0_4_S USB_Normal_OC0#_R
USB_Normal_OC0#_R {12}
{12} USBP1-_R1
{12} USBP1+_R1
R728 WIN7@0_2
R381 WIN7@0_2
R729 NWIN7@0_4
CML4 *E@DLW21SN121SQ2L
R724 NWIN7@0_4
R725 WIN7@0_2
R374 WIN7@0_2
USBP1-_D USBP1-_DL USBP1+_D USBP1+_DL
CN18 2UB4008-370101F
1 VBUS 2 D- 3 D+ 4 GND 5 SSRX- 6 SSRX+ 7 GND 8 SSTX- 9 SSTX+
C3A
{12} USB30_RX1-_R1
{12} USB30_RX1+_R1
R783 R784 *0_2_S
C821 *1.6P/50V_4C
C822 *1.6P/50V_4C
R723 *0_4_S
CML3 *E@DLW21SN121SQ2L
R721 *0_4_S
{12} USB30_TX1-_R1
{12} USB30_TX1+_R1
R785 R786 *0_2_S
C794 C793 0.1U/16V/X7R_4
C823 *1.6P/50V_4C
C824 *1.6P/50V_4C
R718 *0_4_S
CML2 *E@DLW21SN121SQ2L
R717 *0_4_S
EC39 ESD@0.1U/16V/X7R_4
Close to connector
For ESD
U49 ESD@CM1224-02SR
U48 ESD@PUSB3FR4
U53 ESD@CM1224-02SR
U52 ESD@PUSB3FR4
{12} USBP2-_R2
{12} USBP2+_R2
R743 *0_4_S
CML7 *E@DLW21SN121SQ2L
R744 *0_4_S
C804 150U/6.3V/ESR25_3528
CN20 2UB4008-370101F
{12} USB30_RX2-_R2
{12} USB30_RX2+_R2
R787 R788 *0_2_S
C825 C826 *1.6P/50V_4C
R735 *0_4_S
CML6 *E@DLW21SN121SQ2L
R734 *0_4_S
{12} USB30_TX2-_R2
{12} USB30_TX2+_R2
R789 R790 *0_2_S
C798 C797 0.1U/16V/X7R_4
C827 C828 *1.6P/50V_4C
R733 *0_4_S
CML5 *E@DLW21SN121SQ2L
R732 *0_4_S
EC40 *ESD@RCLAMP0551P_TST
UART for DEBUG <W7D>
U15 WIN7@FSUSB42UMX
HSD2- HSD2+ OE VCC SEL D+ D- GND HSD- HSD+
{14} GPP_A16
R365 *WIN7@0_4_S
R368 WIN7@10K_4
C485 WIN7@0.1U/16V/X7R_4
UART2_RXD {14}
UART2_TXD {14}
TP26 TP27
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USB3x2
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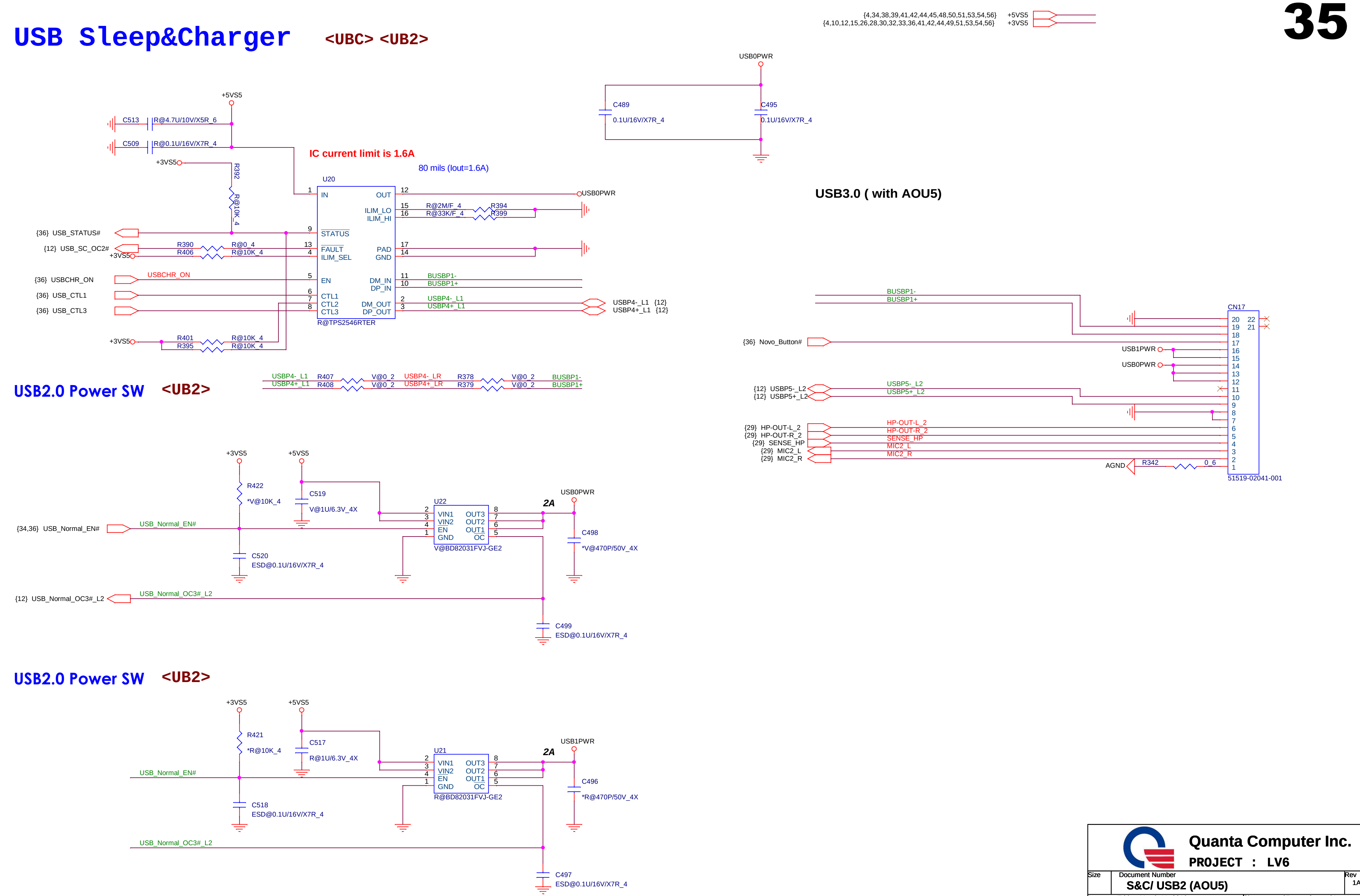
USB Sleep&Charger <UBC> <UB2>



Quanta Computer Inc.

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Size	Document Number	Rev
	S&C/ USB2 (AOU5)	1A

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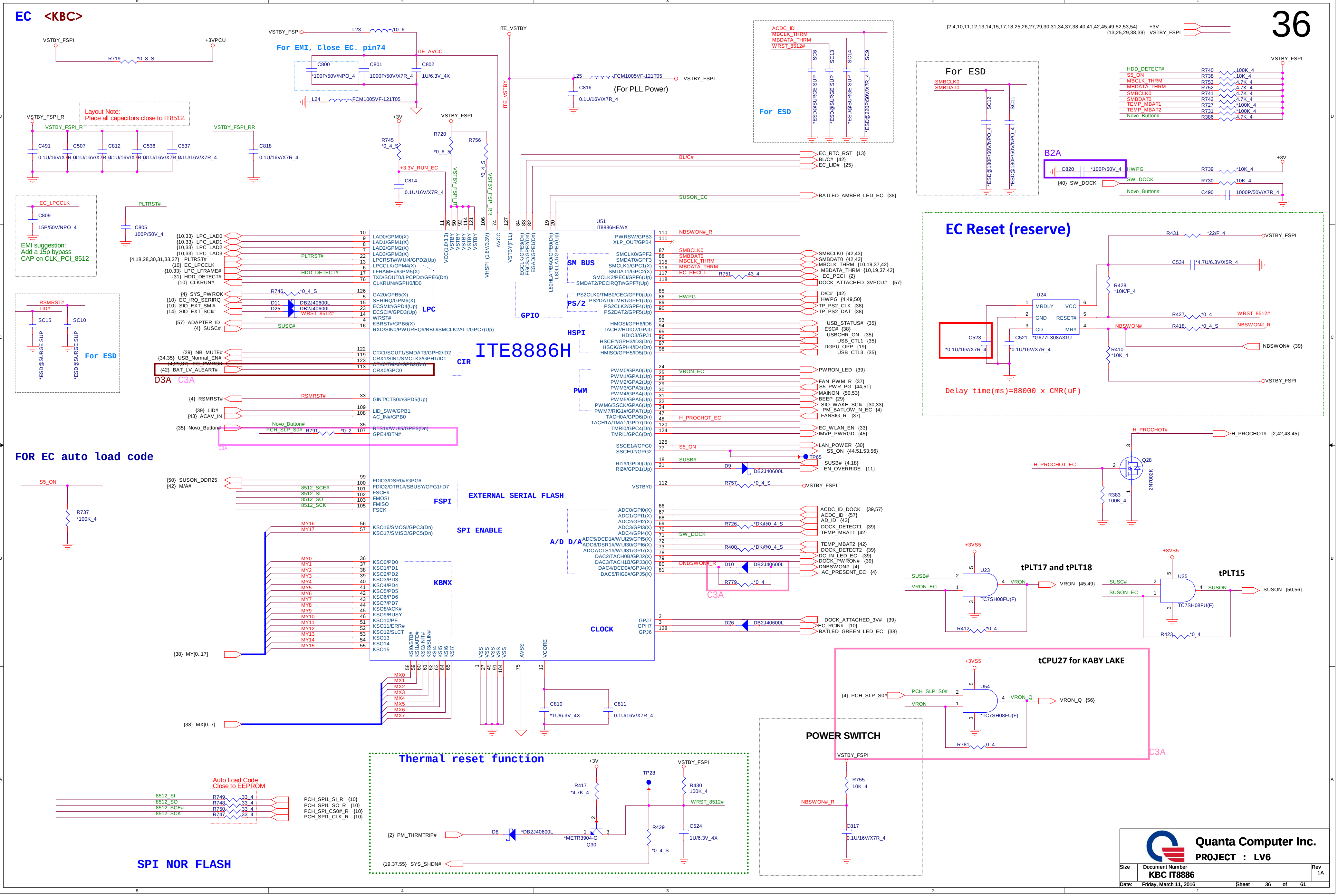
EC <KBC>
For EMI, Close EC. pin74
Layout Note:
Place all capacitors close to IT8512.
(For PLL Power)
For ESD
EMI suggestion:
Add a 15p bypass
CAP on CLK_PCI_8512
ITE8886H
U51
IT8886HE/AX
LPC
SM BUS
PS/2
GPIO
HSPI
CIR
PWM
FSPI
EXTERNAL SERIAL FLASH
SPI ENABLE
A/D D/A
KBMX
CLOCK
EC Reset (reserve)
Delay time(ms)=88000 x CMR(uF)
B2A
D3A
C3A
FOR EC auto load code
tPLT17 and tPLT18
tPLT15
tCPU27 for KABY LAKE
POWER SWITCH
Thermal reset function
Auto Load Code
Close to EEPROM
SPI NOR FLASH
Quanta Computer Inc.
PROJECT : LV6
Document Number
KBC IT8886
Rev
1A
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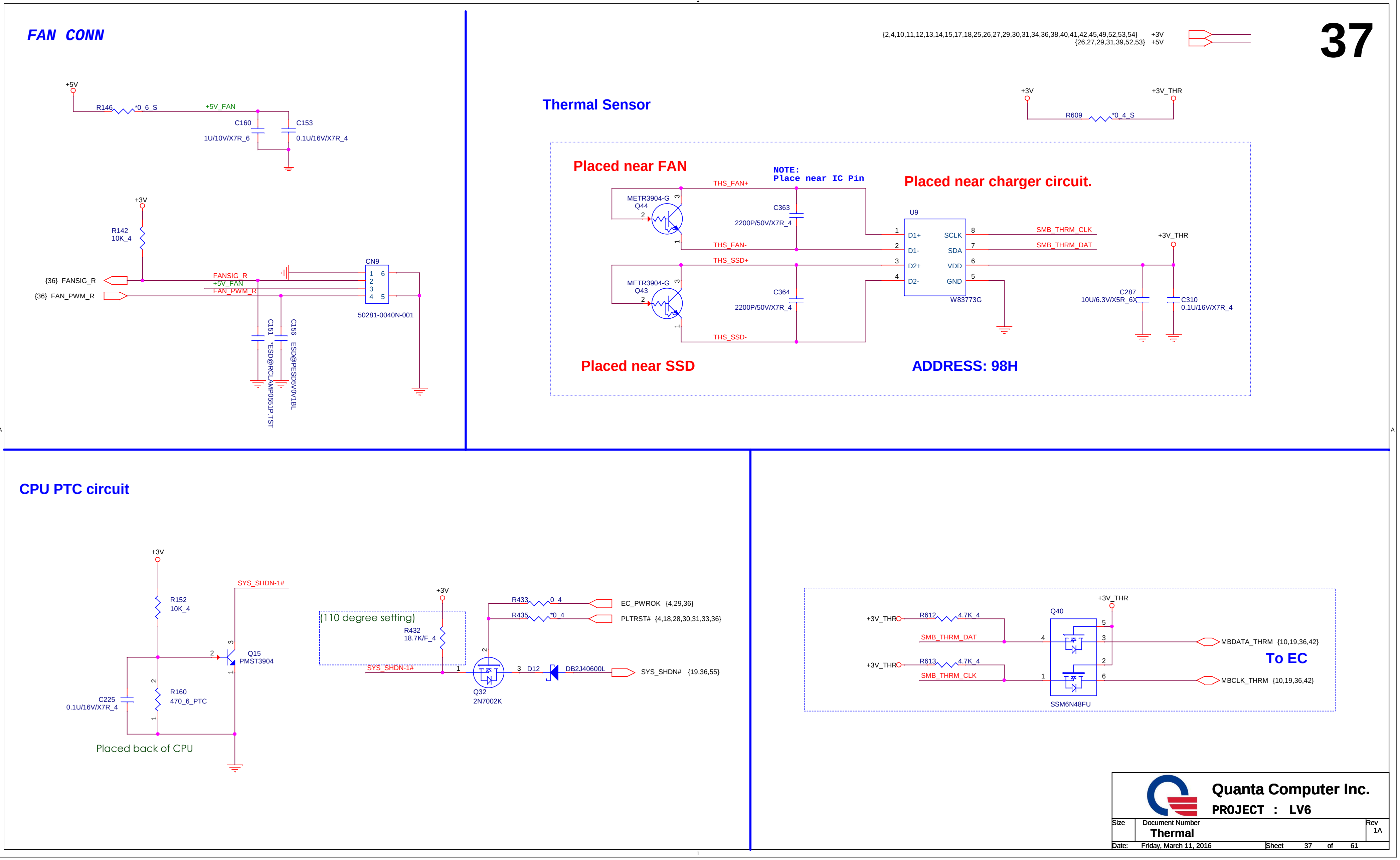
37
FAN CONN
+5V
R146
*0_6_S
+5V_FAN
C160
1U/10V/X7R_6
C153
0.1U/16V/X7R_4
+3V
R142
10K_4
{36} FANSIG_R
{36} FAN_PWM_R
FANSIG_R
+5V_FAN
FAN_PWM_R
CN9
50281-0040N-001
C151
*ESD@RCLAMP0551P.TST
C156
ESD@PESD5V0V1BL
{2,4,10,11,12,13,14,15,17,18,25,26,27,29,30,31,34,36,38,40,41,42,45,49,52,53,54} +3V
{26,27,29,31,39,52,53} +5V
Thermal Sensor
+3V
+3V_THR
R609
*0_4_S
Placed near FAN
NOTE:
Place near IC Pin
Placed near charger circuit.
THS_FAN+
METR3904-G
Q44
C363
2200P/50V/X7R_4
U9
D1+
D1-
D2+
D2-
SCLK
SDA
VDD
GND
W83773G
SMB_THRM_CLK
SMB_THRM_DAT
THS_FAN-
THS_SSD+
METR3904-G
Q43
C364
2200P/50V/X7R_4
THS_SSD-
+3V_THR
C287
10U/6.3V/X5R_6X
C310
0.1U/16V/X7R_4
Placed near SSD
ADDRESS: 98H
CPU PTC circuit
+3V
R152
10K_4
SYS_SHDN-1#
Q15
PMST3904
R160
470_6_PTC
C225
0.1U/16V/X7R_4
Placed back of CPU
(110 degree setting)
+3V
R432
18.7K/F_4
SYS_SHDN-1#
R433
0_4
R435
*0_4
EC_PWROK {4,29,36}
PLTRST# {4,18,28,30,31,33,36}
Q32
2N7002K
D12
DB2J40600L
SYS_SHDN# {19,36,55}
+3V_THR
+3V_THR
R612
4.7K_4
SMB_THRM_DAT
+3V_THR
R613
4.7K_4
SMB_THRM_CLK
Q40
SSM6N48FU
MBDATA_THRM {10,19,36,42}
To EC
MBCLK_THRM {10,19,36,42}
Quanta Computer Inc.
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Thermal
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1A
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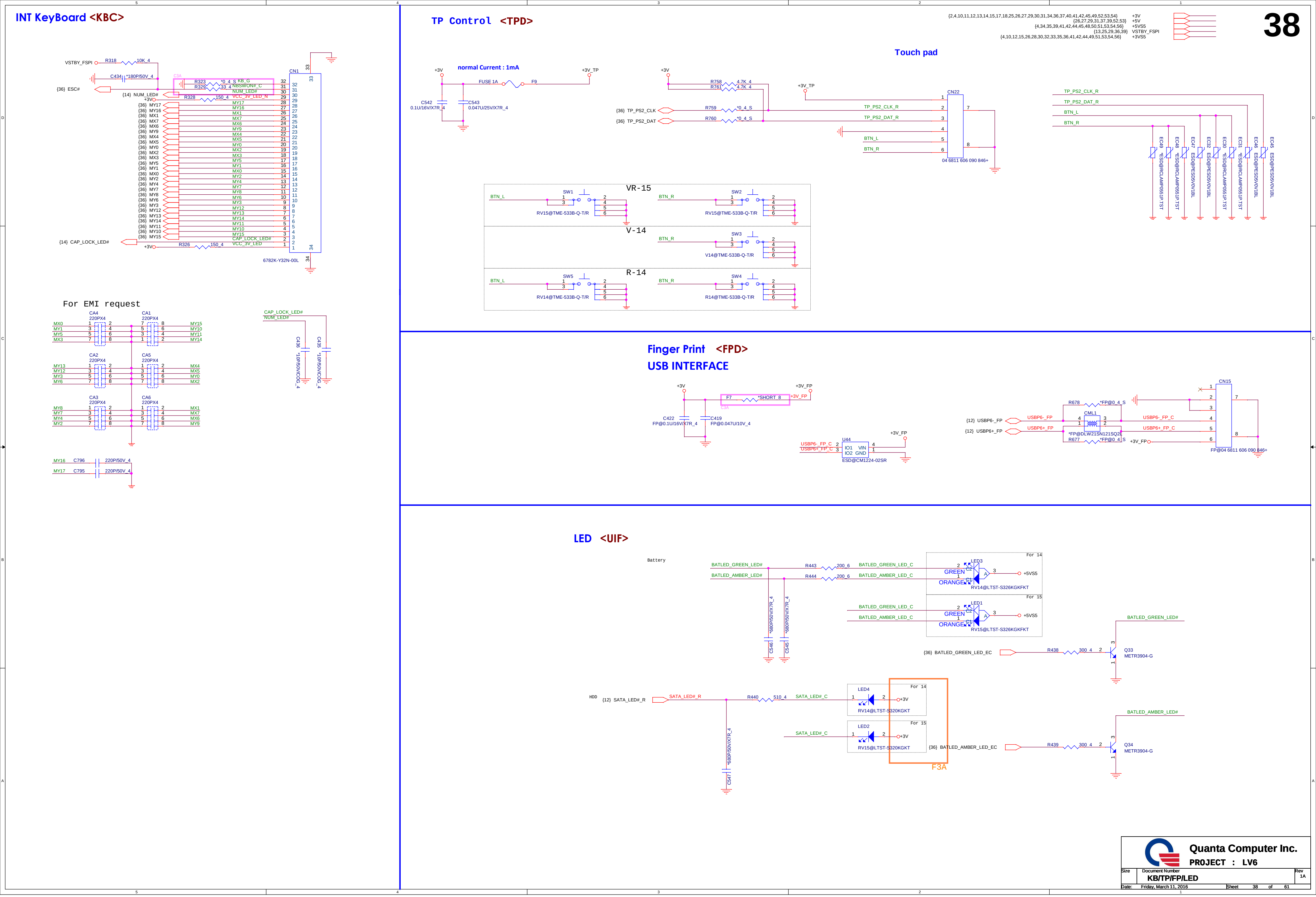
38
INT KeyBoard <KBC>
TP Control <TPD>
Touch pad
normal Current : 1mA
VSTBY_FSPI
R318 10K_4
C434 *180P/50V_4
(36) ESC#
(14) NUM_LED#
R323 *0_4_S KB_G
R329 33_4 NBSWON#_C
NUM_LED#
R328 150_4 VCC_3V_LED_N
CN1
6782K-Y32N-00L
(14) CAP_LOCK_LED#
R326 150_4 CAP_LOCK_LED#
VCC_3V_LED
For EMI request
CA4 220PX4
CA1 220PX4
CA2 220PX4
CA5 220PX4
CA3 220PX4
CA6 220PX4
C796 220P/50V_4
C795 220P/50V_4
C436 *10P/50V/COG_4
C435 *10P/50V/COG_4
FUSE 1A F9
C542 0.1U/16V/X7R_4
C543 0.047U/25V/X7R_4
+3V_TP
R758 4.7K_4
R761 4.7K_4
(36) TP_PS2_CLK
(36) TP_PS2_DAT
R759 *0_4_S
R760 *0_4_S
TP_PS2_CLK_R
TP_PS2_DAT_R
BTN_L
BTN_R
CN22
04 6811 606 090 846+
EC49 *ESD@RCLAMP0551P.TST
EC48 *ESD@RCLAMP0551P.TST
EC47 ESD@PESD5V0V1BL
EC32 ESD@PESD5V0V1BL
EC30 *ESD@RCLAMP0551P.TST
EC31 *ESD@RCLAMP0551P.TST
EC46 ESD@PESD5V0V1BL
EC45 ESD@PESD5V0V1BL
VR-15
SW1 RV15@TME-533B-Q-T/R
SW2 RV15@TME-533B-Q-T/R
V-14
SW3 V14@TME-533B-Q-T/R
R-14
SW5 RV14@TME-533B-Q-T/R
SW4 R14@TME-533B-Q-T/R
Finger Print <FPD>
USB INTERFACE
+3V_FP
F7 *SHORT_8
C422 FP@0.1U/16V/X7R_4
C419 FP@0.047U/10V_4
U44 ESD@CM1224-02SR
USBP6-_FP_C
USBP6+_FP_C
(12) USBP6-_FP
(12) USBP6+_FP
R678 *FP@0_4_S
R677 *FP@0_4_S
CML1 *FP@DLW21SN121SQ2L
CN15
FP@04 6811 606 090 846+
LED <UIF>
Battery
BATLED_GREEN_LED#
BATLED_AMBER_LED#
R443 200_6
R444 200_6
BATLED_GREEN_LED_C
BATLED_AMBER_LED_C
LED3 RV14@LTST-S326KGKFKT
LED1 RV15@LTST-S326KGKFKT
For 14
For 15
GREEN
ORANGE
+5VS5
C546 *680P/50V/X7R_4
C545 *680P/50V/X7R_4
(36) BATLED_GREEN_LED_EC
R438 300_4
Q33 METR3904-G
HDD
(12) SATA_LED#_R
R440 510_4
SATA_LED#_C
LED4 RV14@LTST-S320KGKT
LED2 RV15@LTST-S320KGKT
C547 *680P/50V/X7R_4
(36) BATLED_AMBER_LED_EC
R439 300_4
Q34 METR3904-G
F3A
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Document Number
KB/TP/FP/LED
Rev 1A
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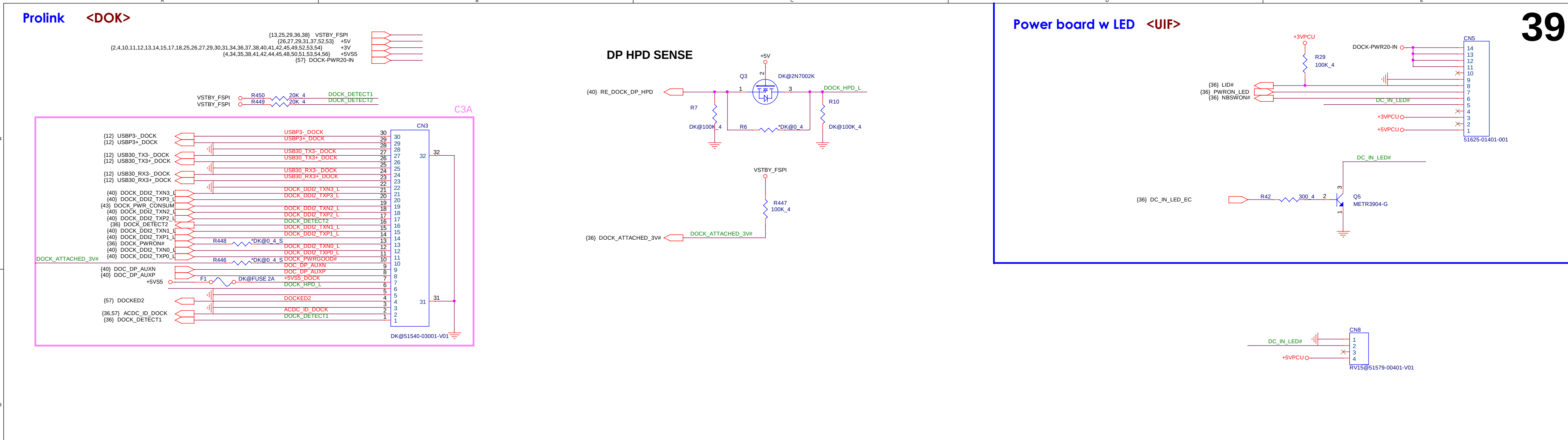

Quanta Computer Inc.

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Size	Document Number	Rev
	Prolink	1A

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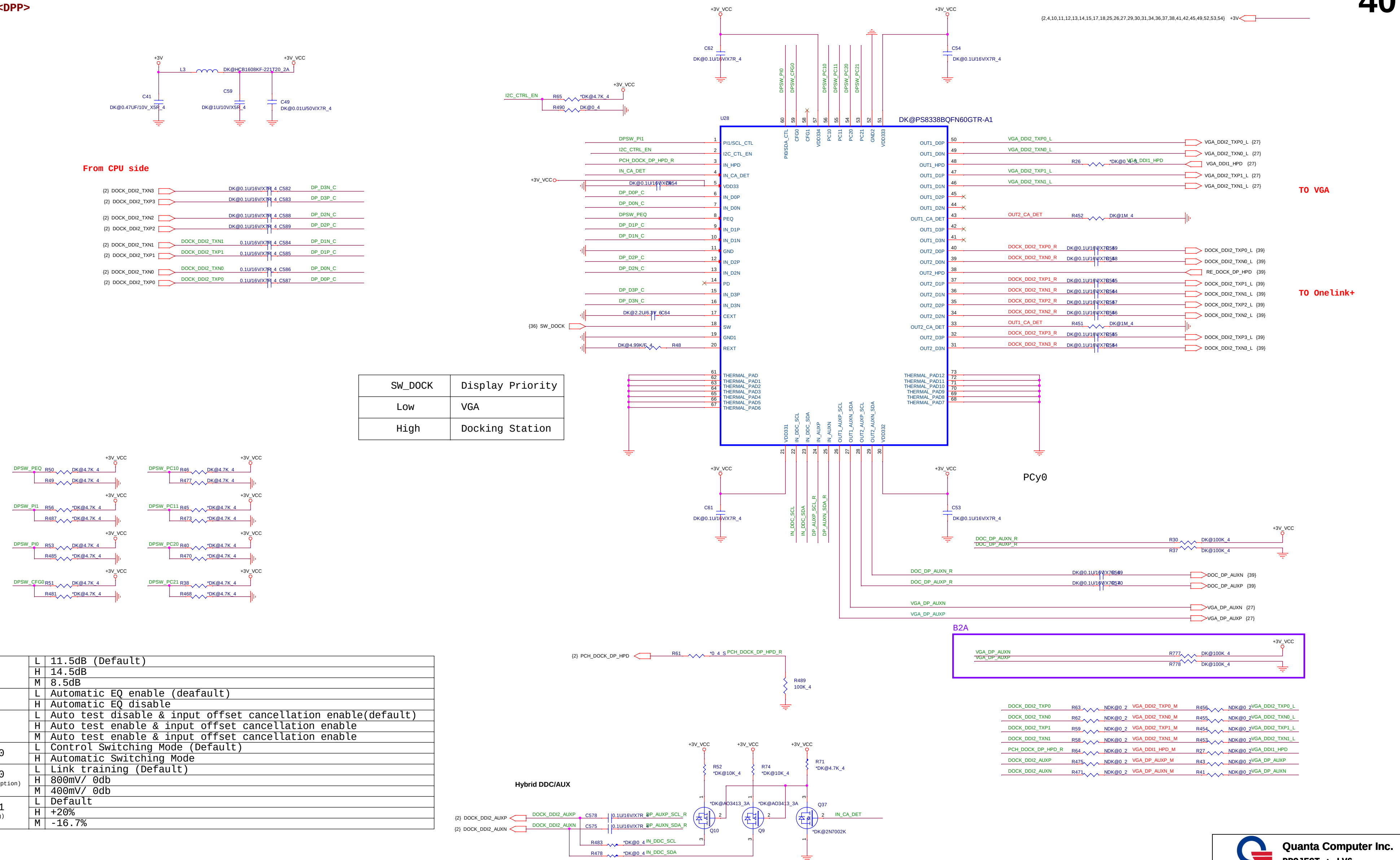
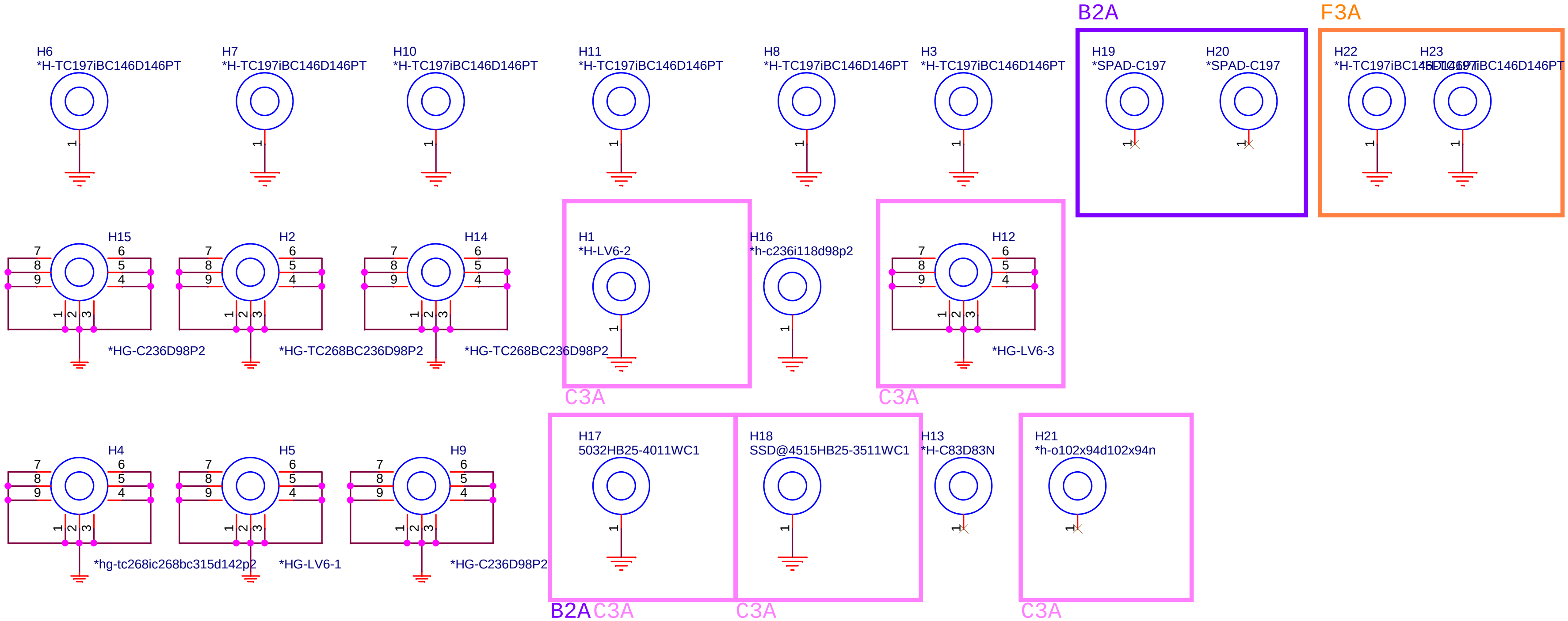
DP SWITCH <DPP>



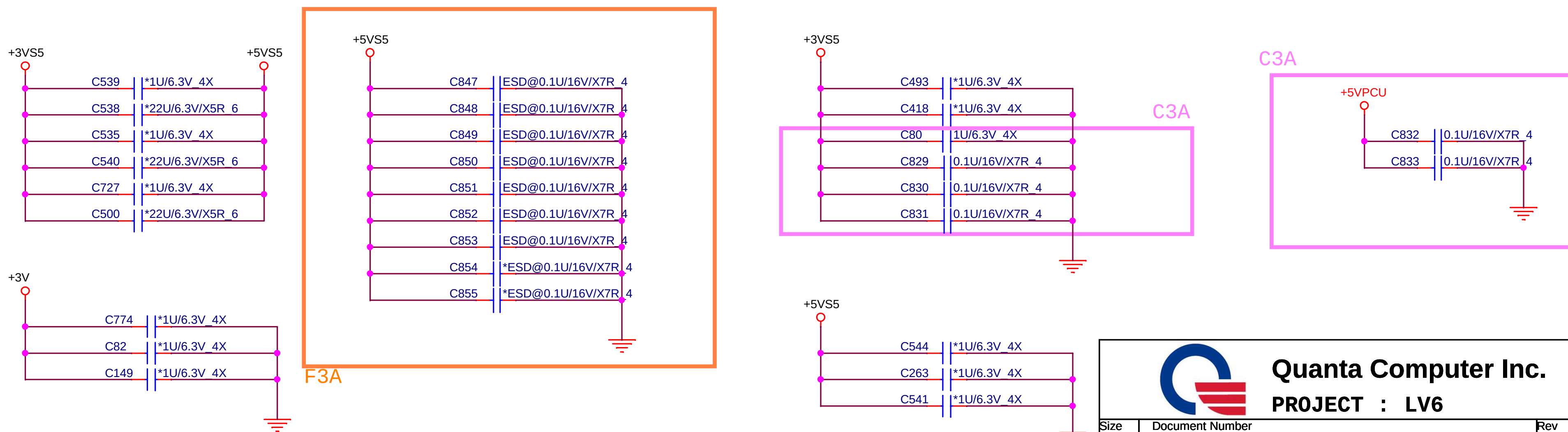
SW_DOCK	Display Priority
Low	VGA
High	Docking Station

PEQ	L	11.5dB (Default)
	H	14.5dB
	M	8.5dB
PI0	L	Automatic EQ enable (deafault)
	H	Automatic EQ disable
PI1	L	Auto test disable & input offset cancellation enable(default)
	H	Auto test enable & input offset cancellation enable
	M	Auto test enable & input offset cancellation enable
CFG0	L	Control Switching Mode (Default)
	H	Automatic Switching Mode
PCy0 (AUX Interception)	L	Link training (Default)
	H	800mV/ 0db
	M	400mV/ 0db
PCy1 (Swing)	L	Default
	H	+20%
	M	-16.7%

HOLE



<EMC>



Quanta Computer Inc.

PROJECT : LV6

Size	Document Number	Rev
	EMC/Screw Hole	1A

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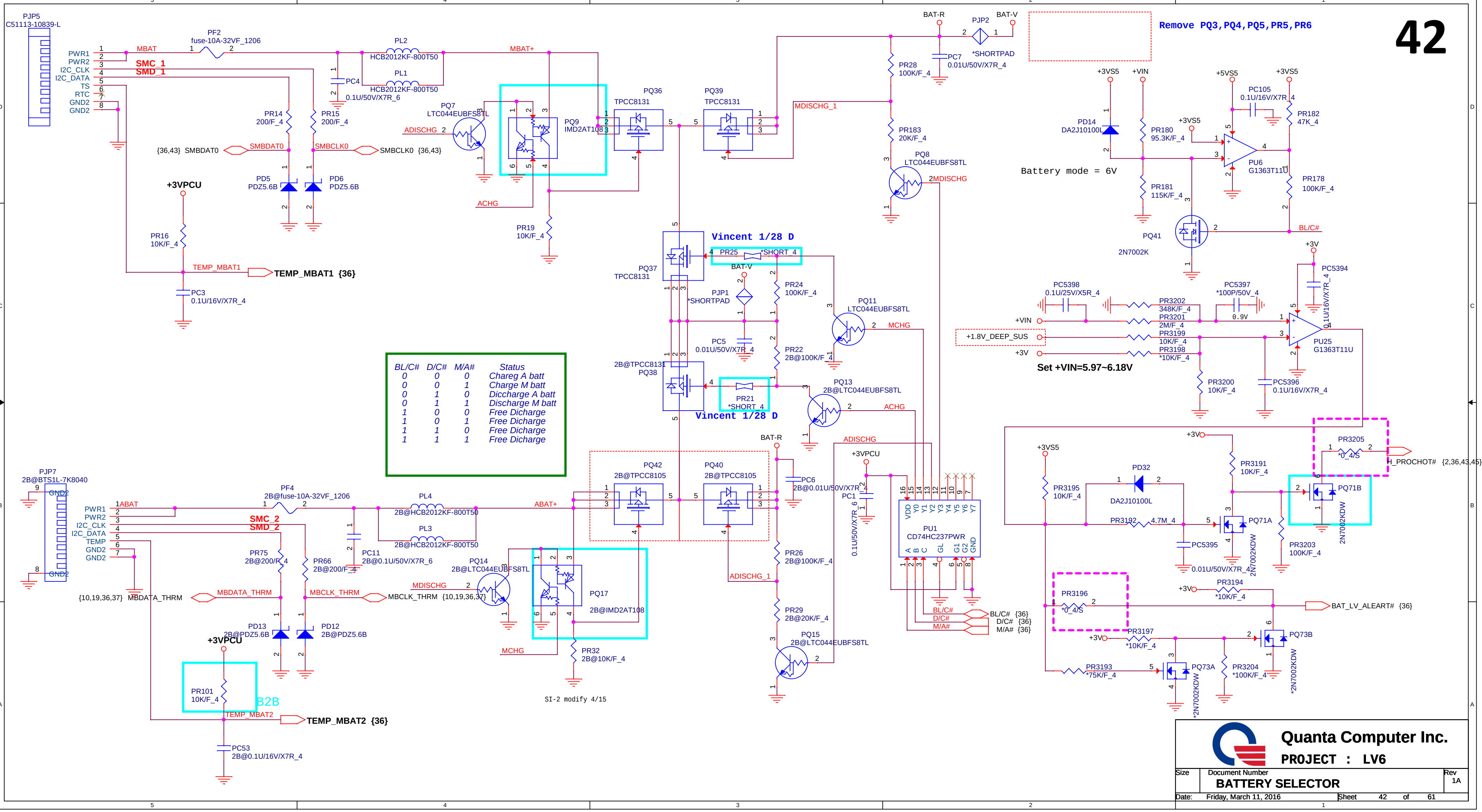

BL/C#	D/C#	M/A#	Status
0	0	0	Chareg A batt
0	0	1	Charge M batt
0	1	0	Diccharge A batt
0	1	1	Discharge M batt
1	0	0	Free Dicharge
1	0	1	Free Dicharge
1	1	0	Free Dicharge
1	1	1	Free Dicharge

Quanta Computer Inc.

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Size	Document Number	Rev
	BATTERY SELECTOR	1A

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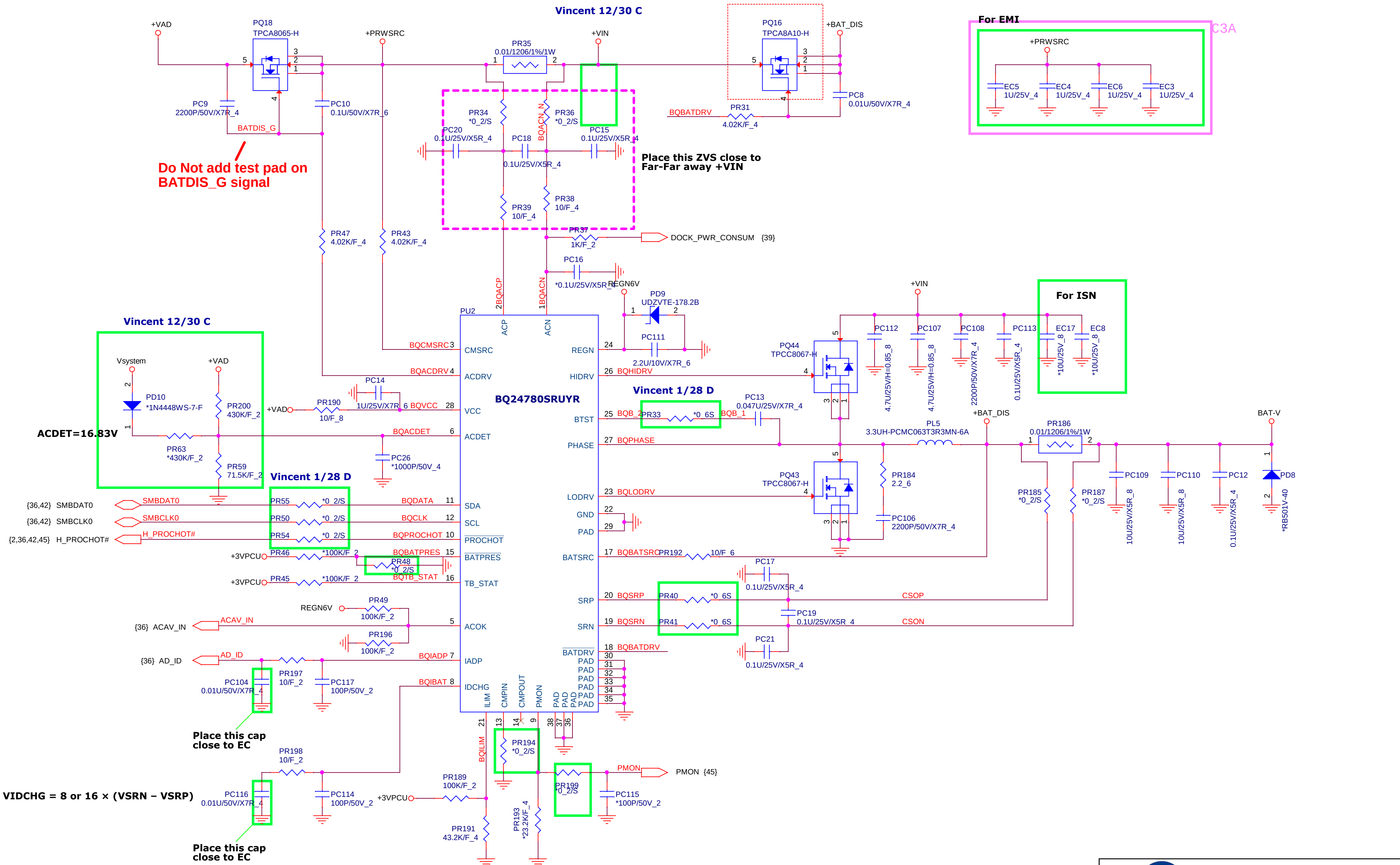

Quanta Computer Inc.

PROJECT : LV6

Size	Document Number	Rev
	+VBATA - BQ24780SRUYR	1A

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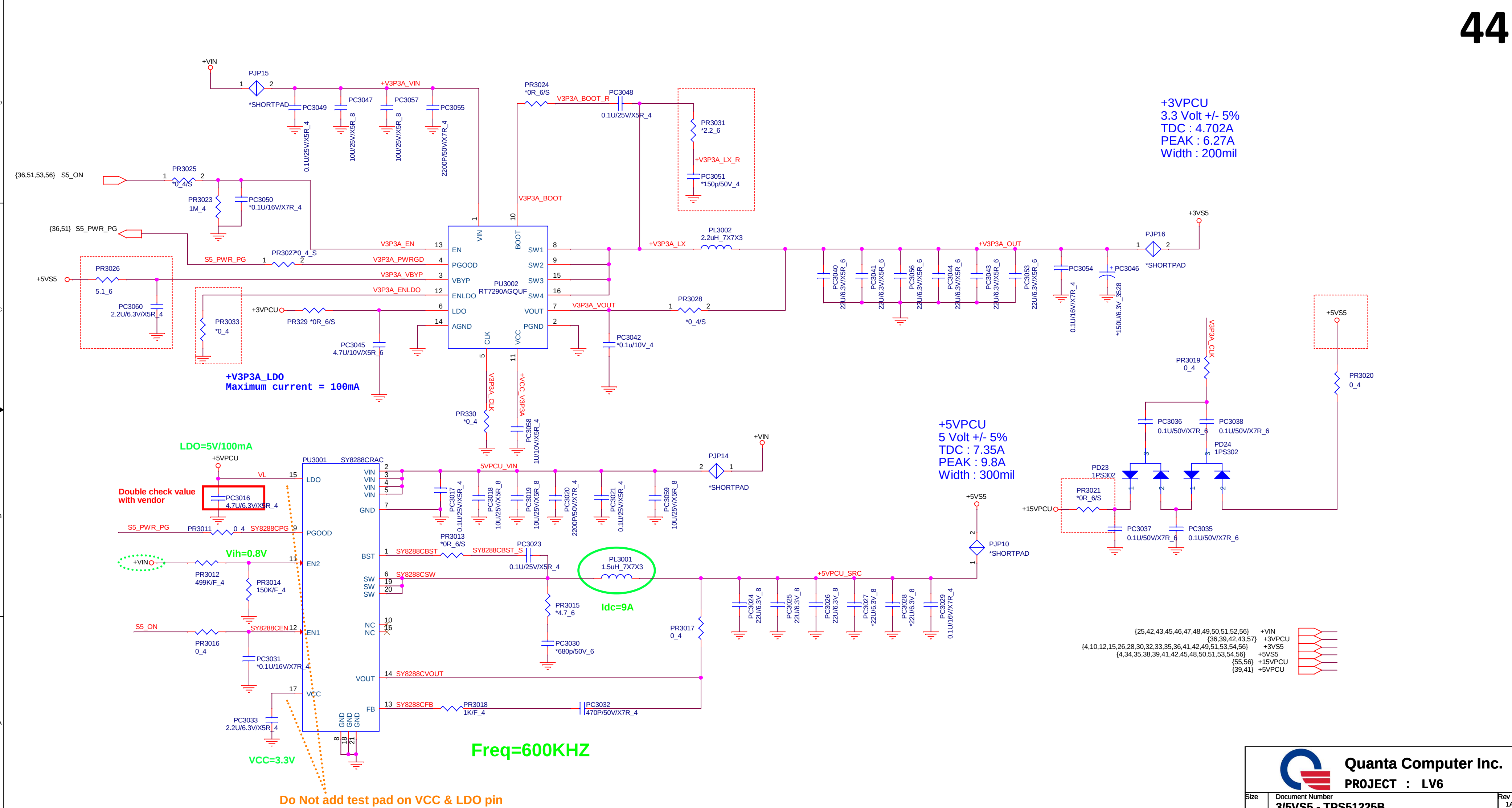

Quanta Computer Inc.

PROJECT : LV6

Size	Document Number	Rev
	3/5VS5 - TPS51225B	1A

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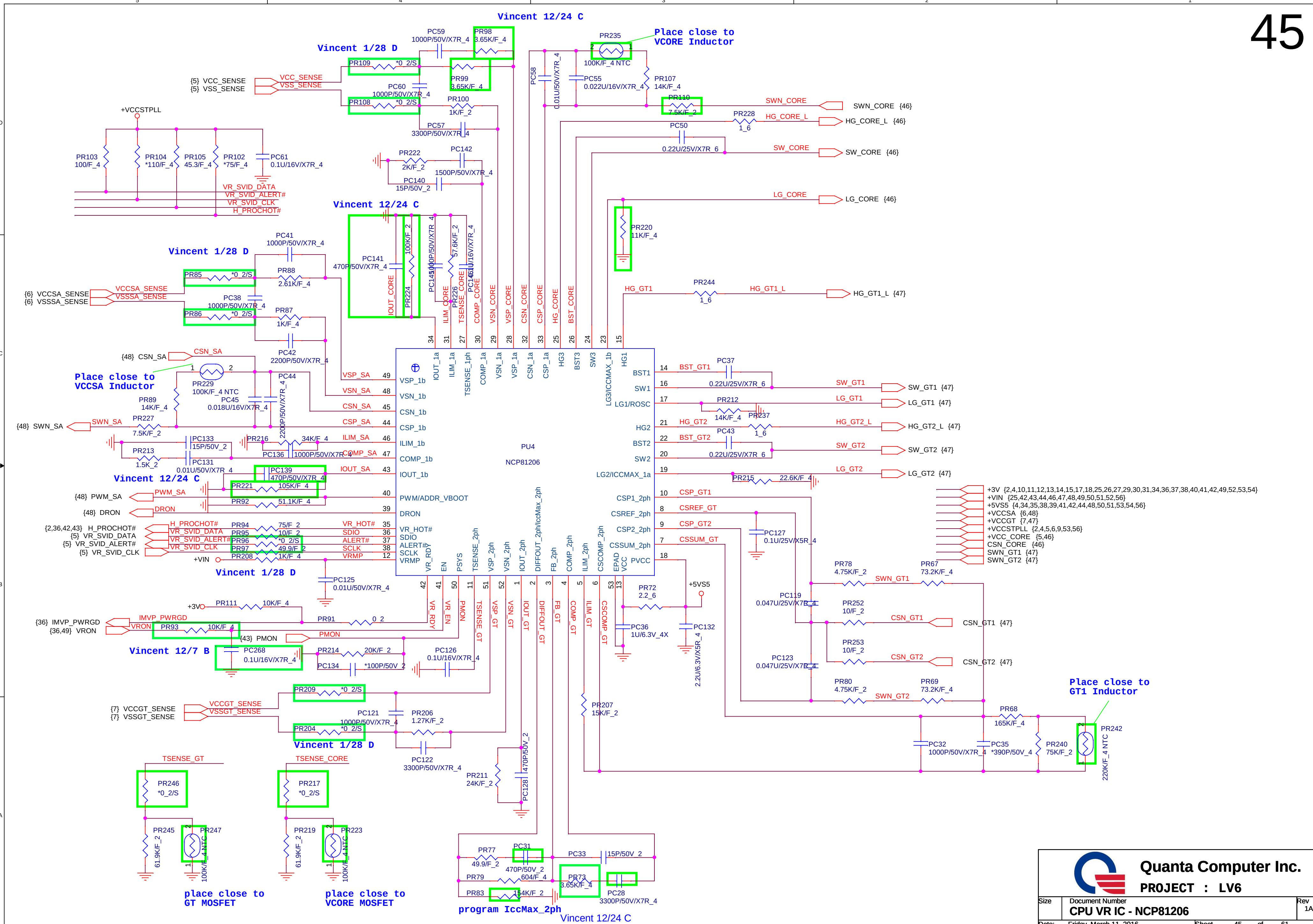

Quanta Computer Inc.

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Size	Document Number	Rev
	CPU VR IC - NCP81206	1A
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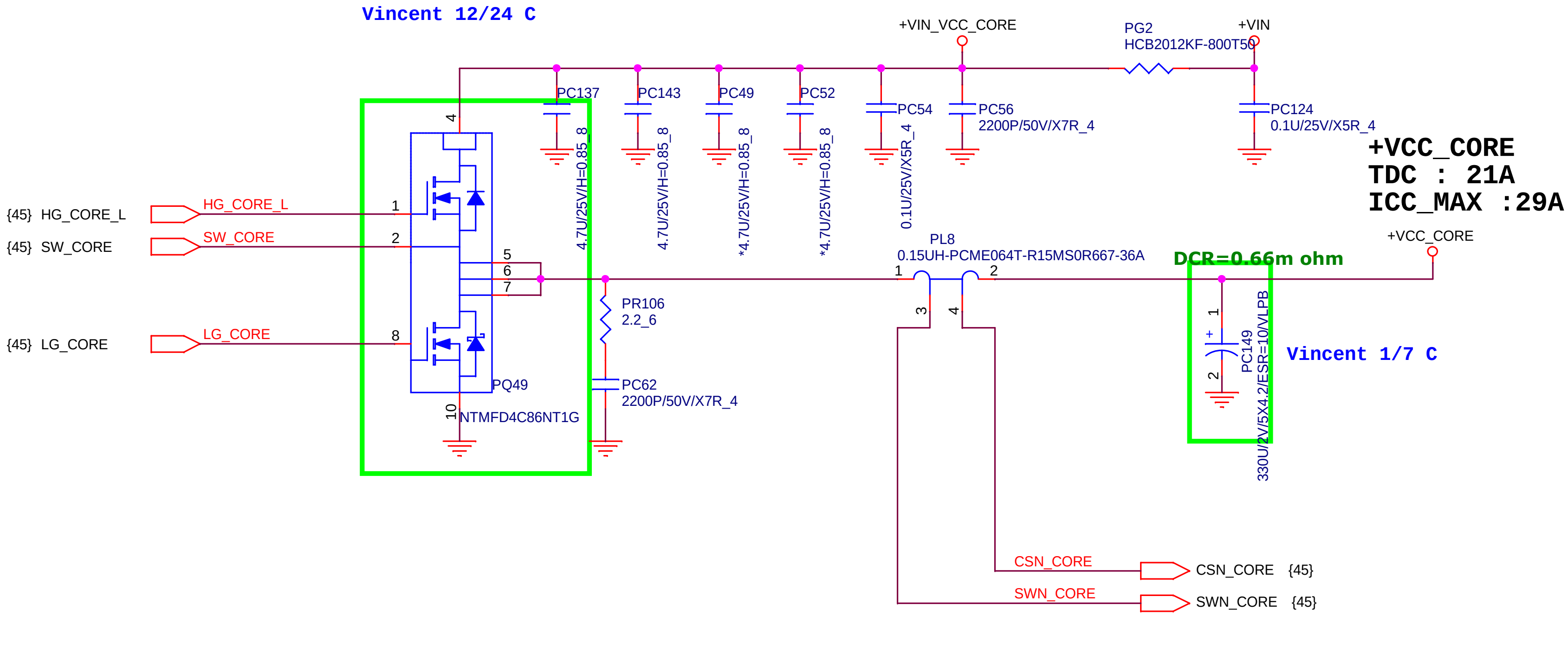

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Size	Document Number	Rev
	VCCORE	1A

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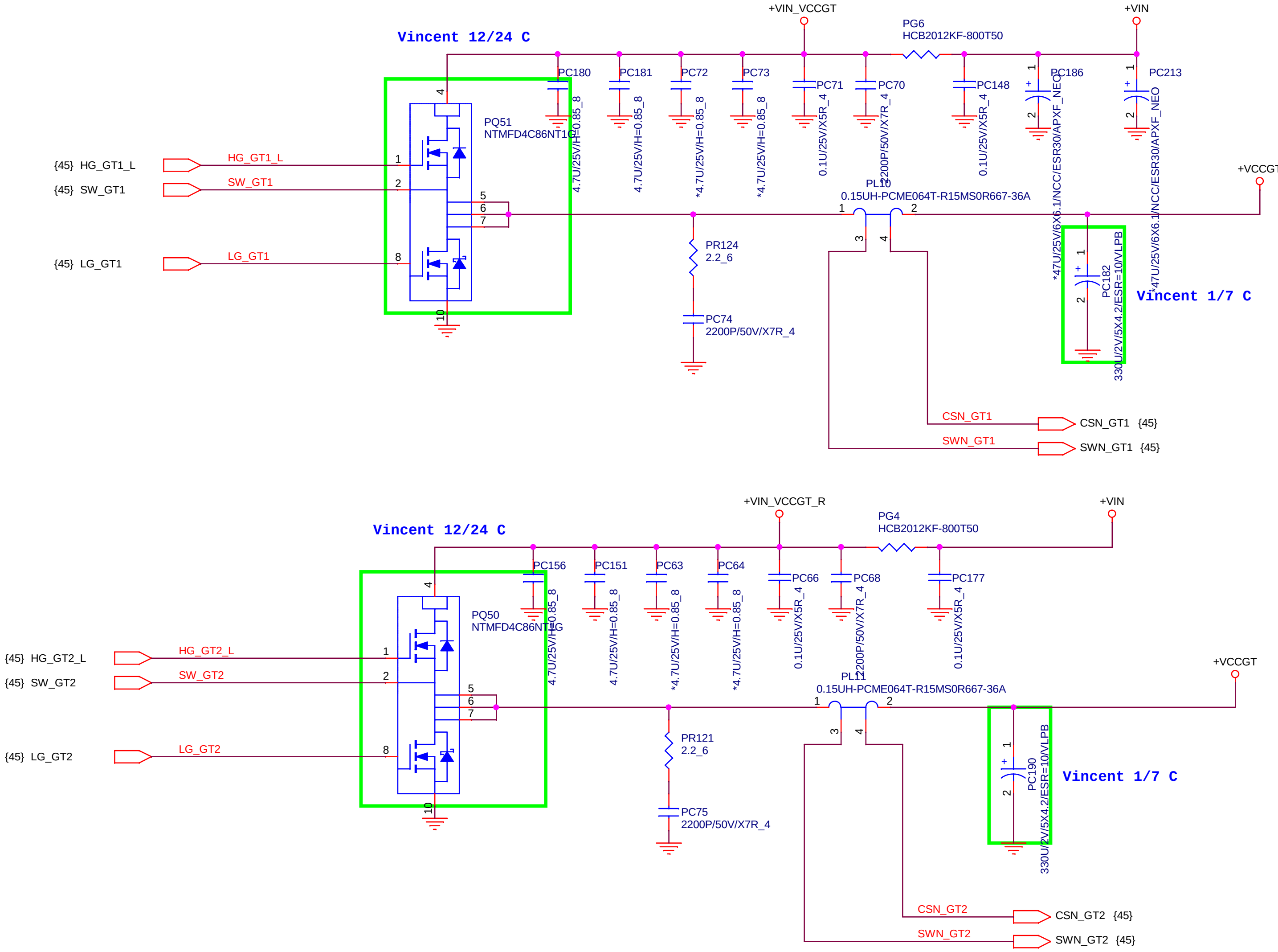

+VCCGT
TDC :A
ICC_MAX :64A

Quanta Computer Inc.		
PROJECT : LV6		
Size	Document Number: **VCCGT**	Rev 1A
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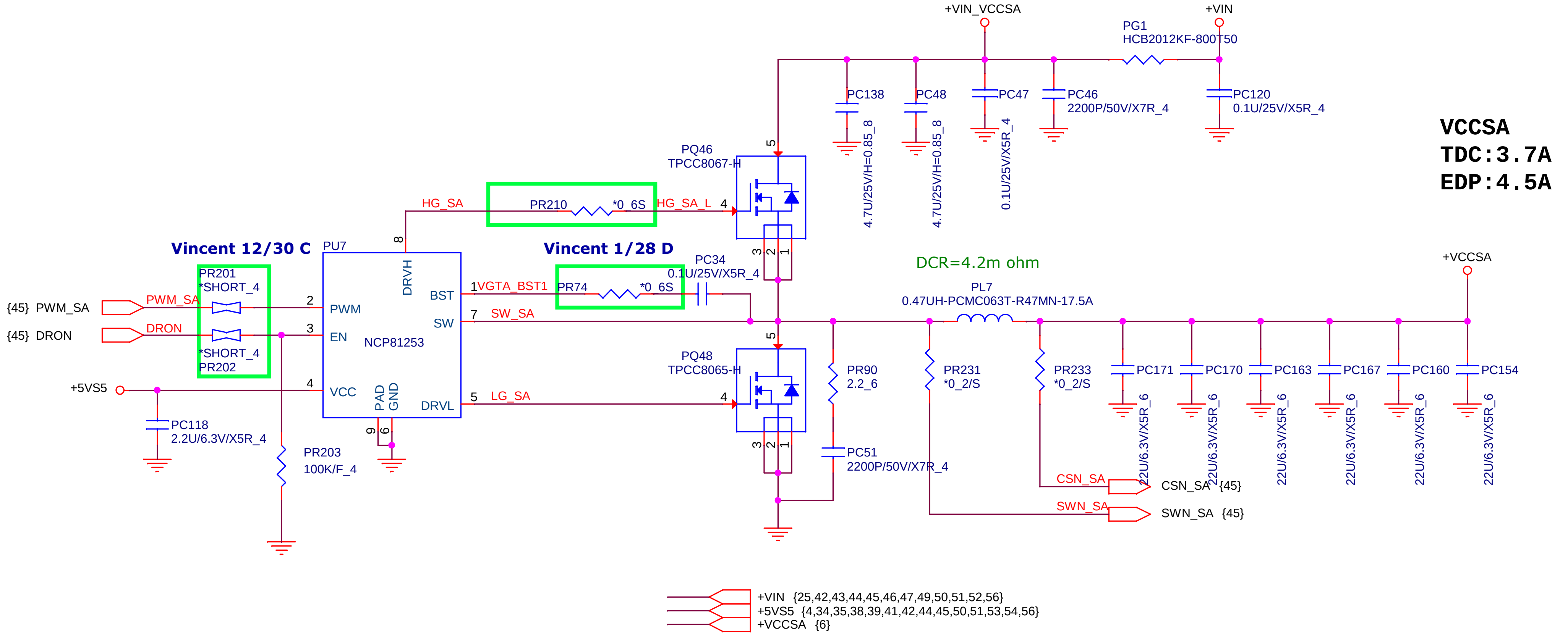
VCCSA



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Size	Document Number	Rev
	VCCSA - NCP81253	1A

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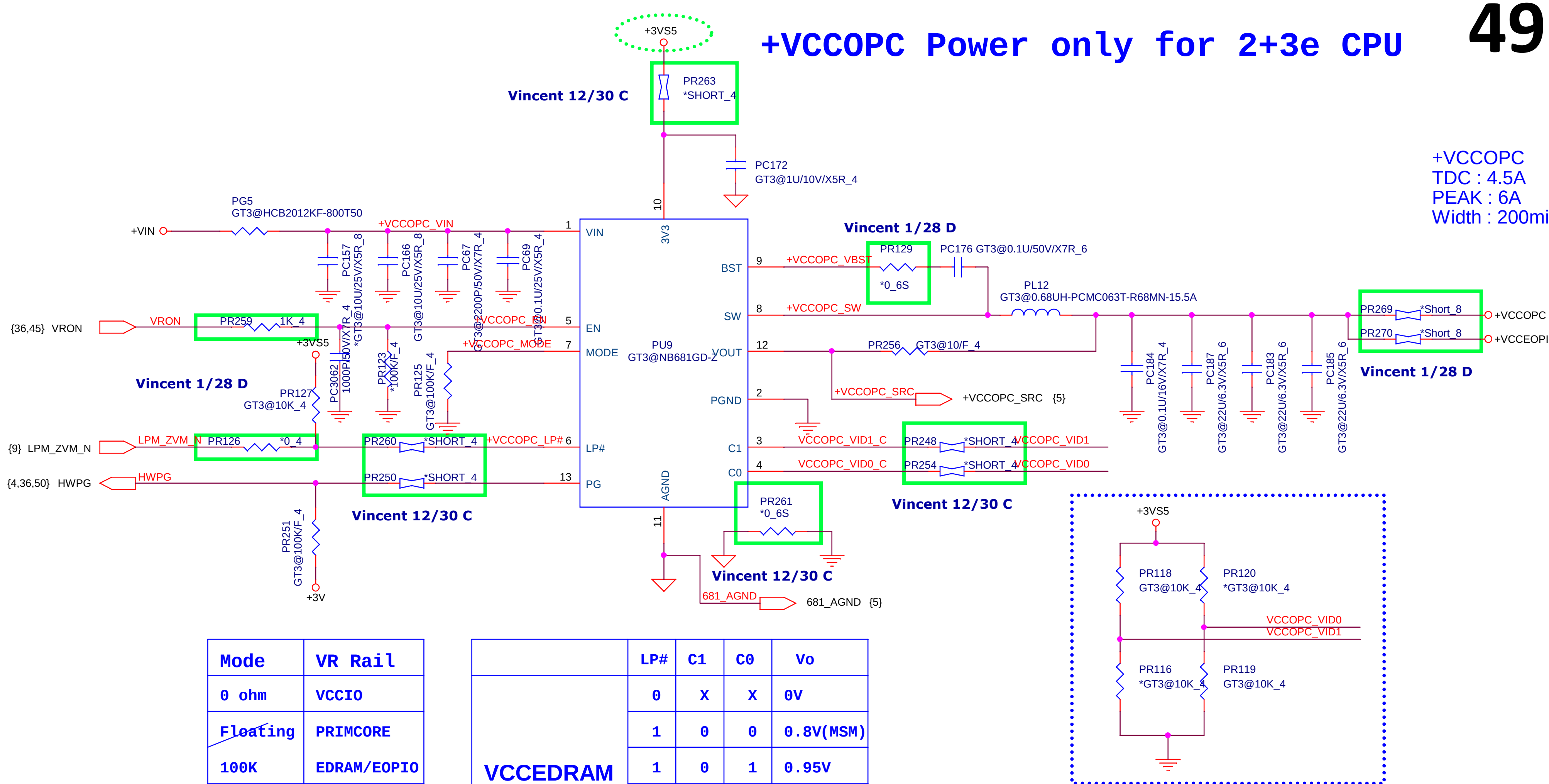
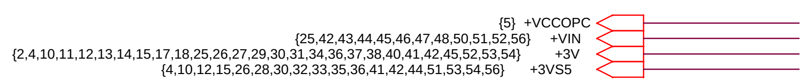
+VCCOPC Power only for 2+3e CPU

+VCCOPC
TDC : 4.5A
PEAK : 6A
Width : 200mil



Mode	VR Rail
0 ohm	VCCIO
~~Floating~~	PRIMCORE
100K	EDRAM/EOPIO
150K	Other

	LP#	C1	C0	Vo
VCCEDRAM	0	X	X	0V
	1	0	0	0.8V(MSM)
	1	0	1	0.95V
	1	1	0	1.0V
	1	1	1	1.05V



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Size	Document Number	Rev
	+VCCOPC (NB681GD-Z)	1A

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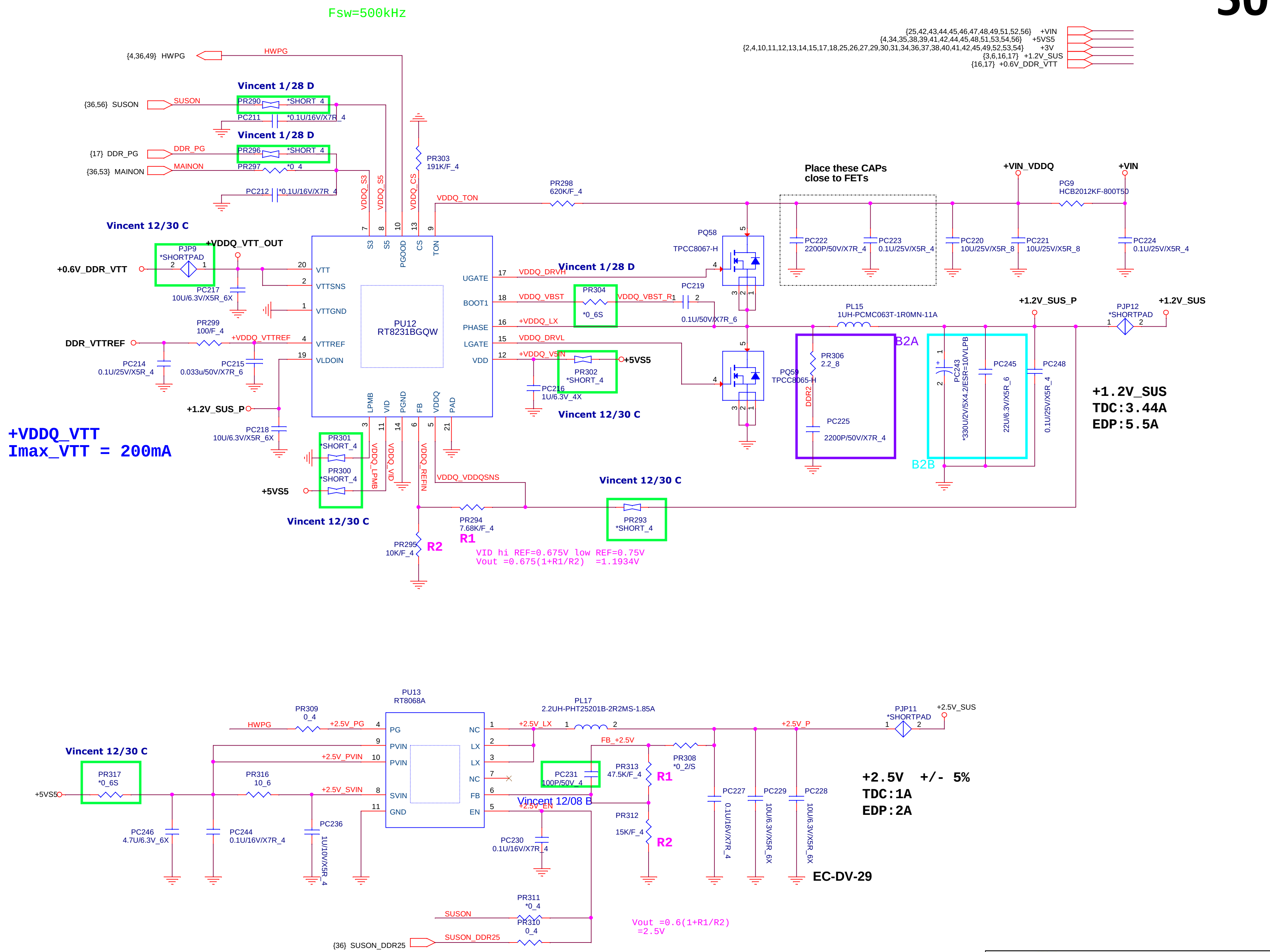
VR PAGE: +VDDQ



Quanta Computer Inc.

PROJECT : LV6

Size	Document Number	Rev
	VDDQ - TPS51716	1A

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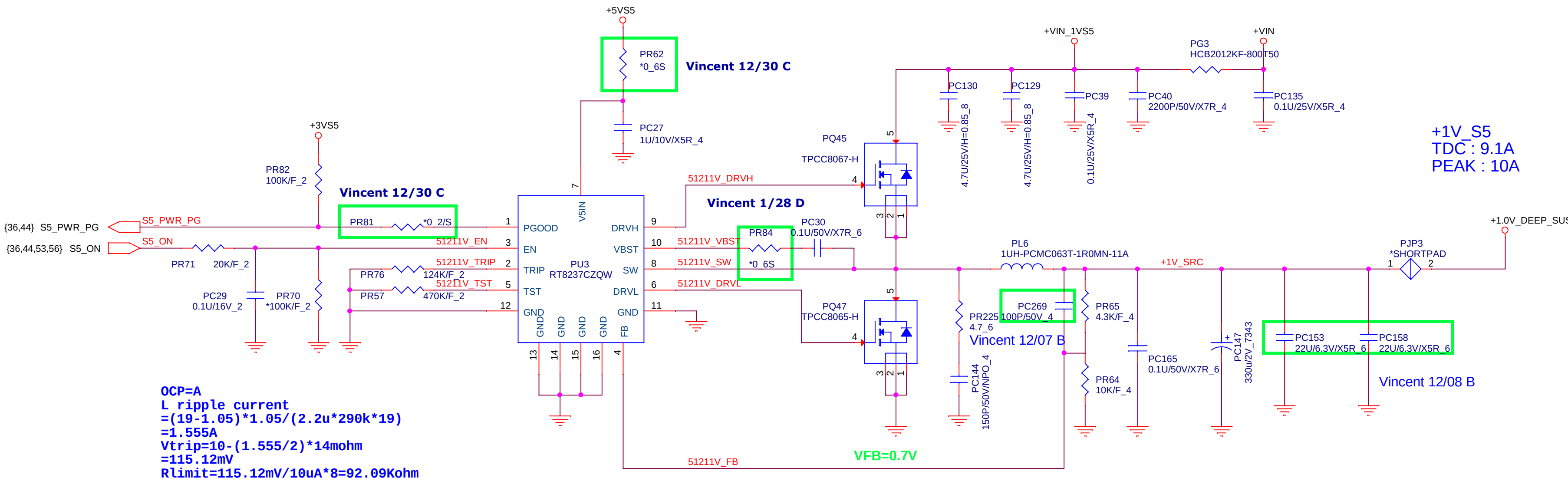
V1P0A (RT8237CZQW)



OCP=A
L ripple current
=(19-1.05)*1.05/(2.2u*290k*19)
=1.555A
Vtrip=10-(1.555/2)*14mohm
=115.12mV
Rlimit=115.12mV/10uA*8=92.09Kohm

Quanta Computer Inc.
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Size	Document Number	Rev
	+1V_DS - RT8237CZQW	1A
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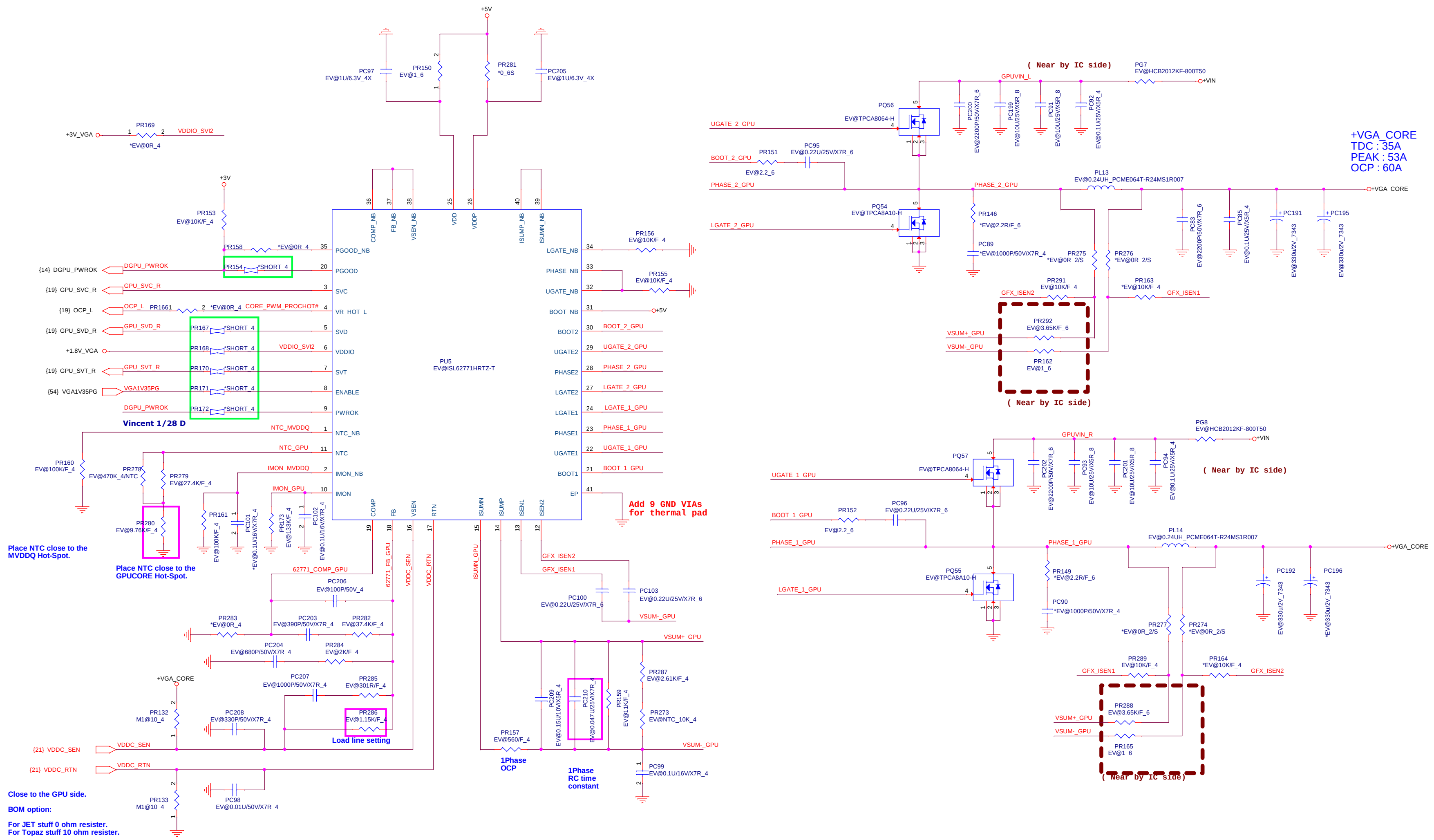
VGA-CORE



Quanta Computer Inc.

PROJECT : LV6

Size	Document Number	Rev
	GPU_CORE (ISL62771)	1A

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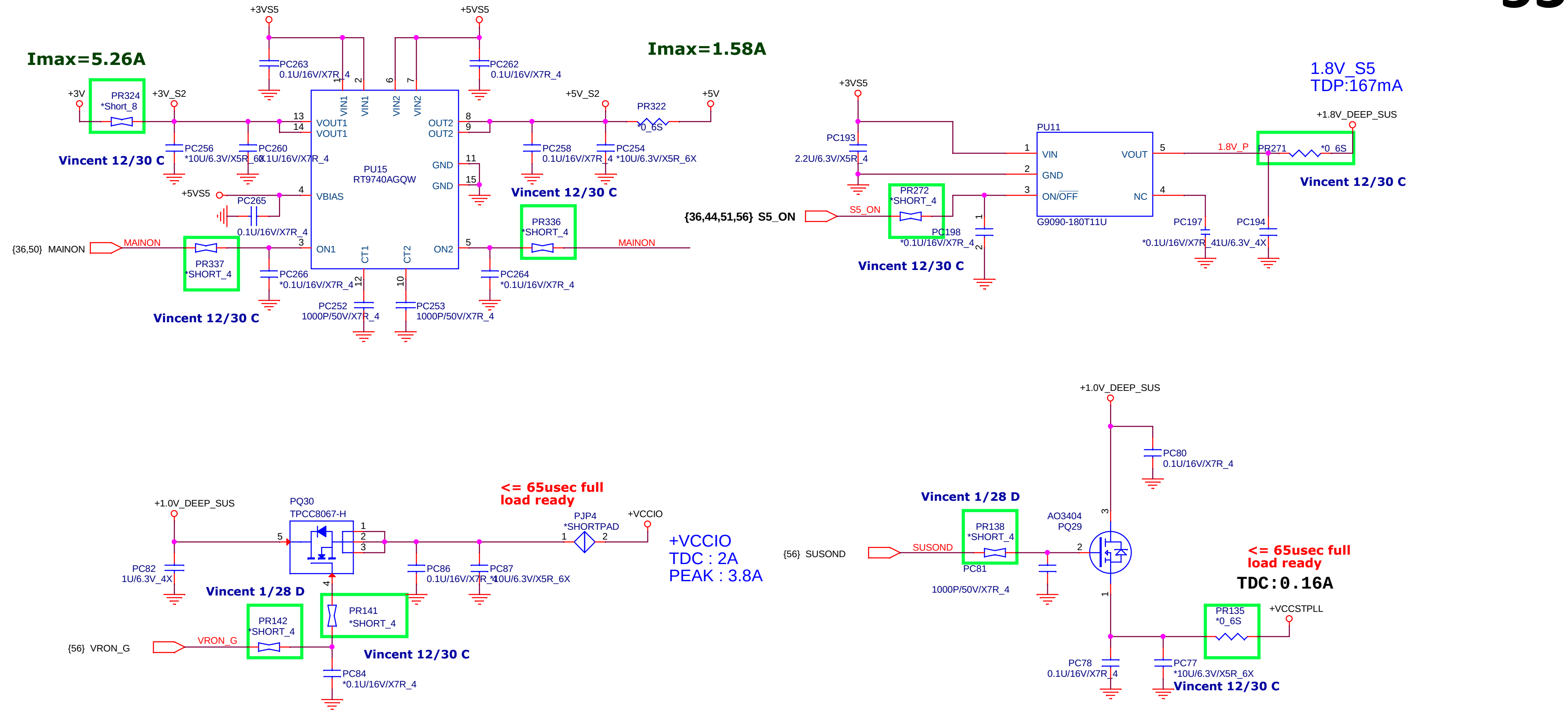

Quanta Computer Inc.

PROJECT : LV6

Size	Document Number	Rev
	+1.0V/+3V/+5V SW	1A

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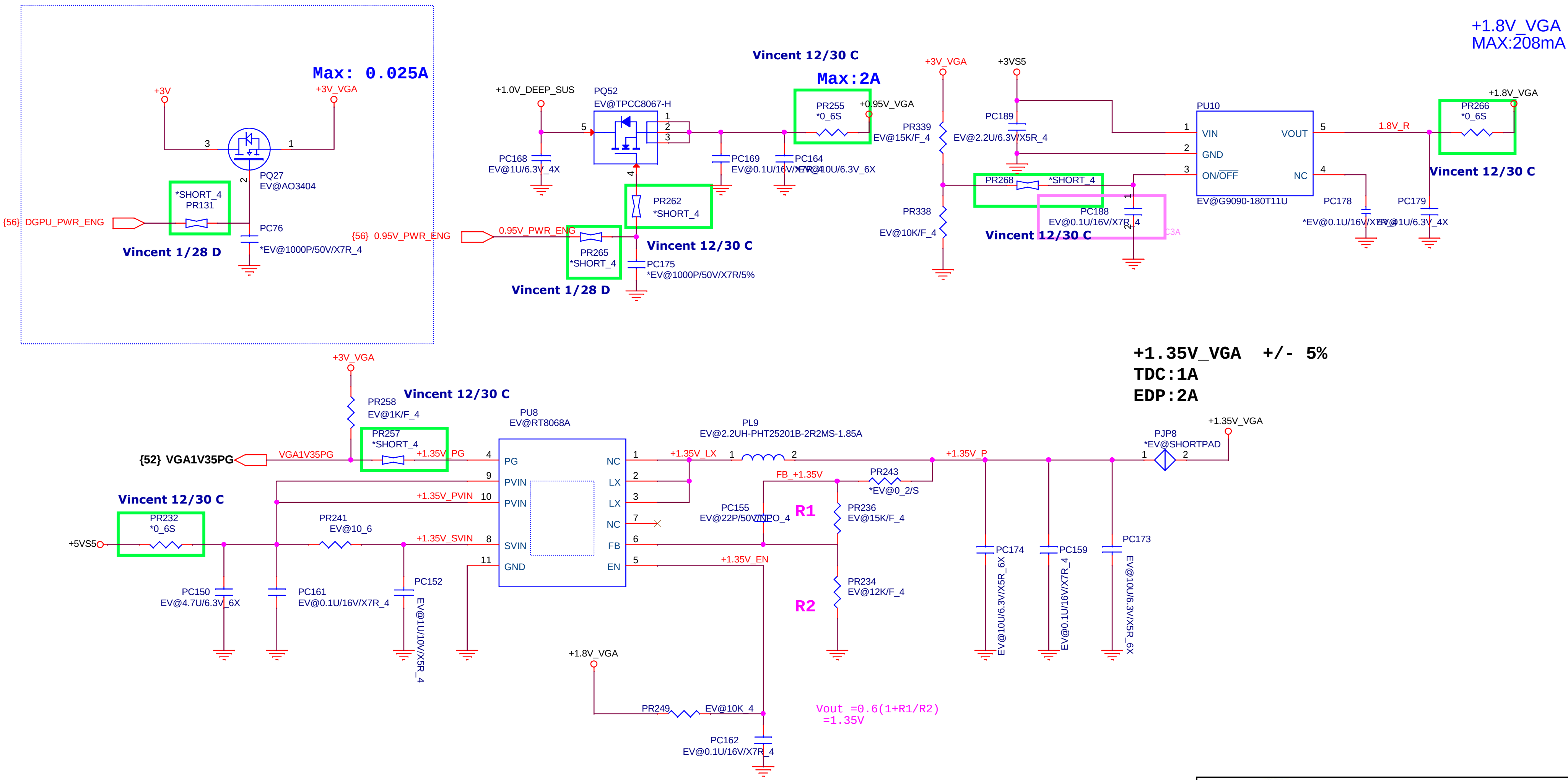
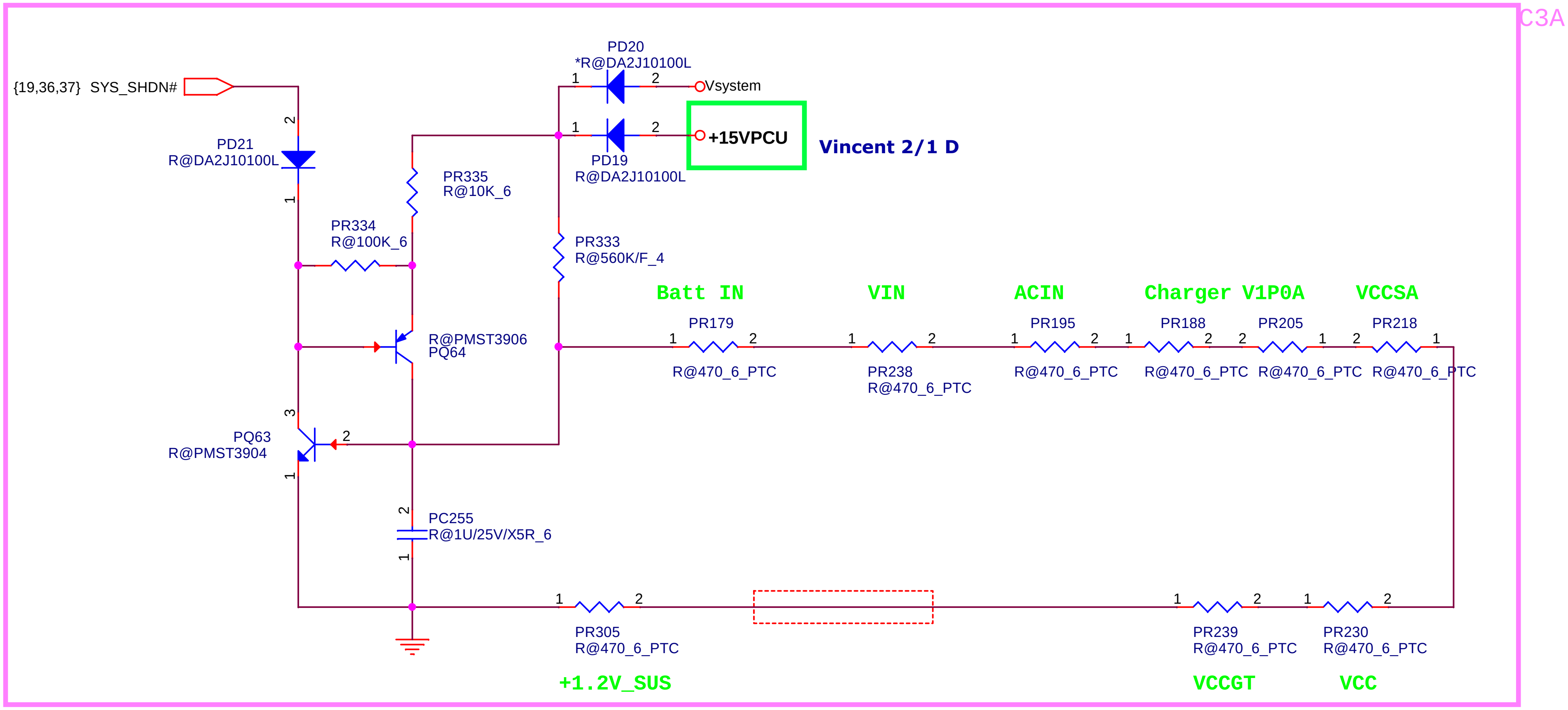
+1.8V_VGA(G9090-180T11U)
+1.35V_VGA(RT8068A)



Quanta Computer Inc.		
PROJECT : LV6		
Size	Document Number: +1.8V/+1.35V/+3V_VGA	Rev 1A
Date: Friday, March 11, 2016	Sheet 54 of 61	



Quanta Computer Inc.

PROJECT : LV6

Size	Document Number	Rev
	PTC Circuit	1A

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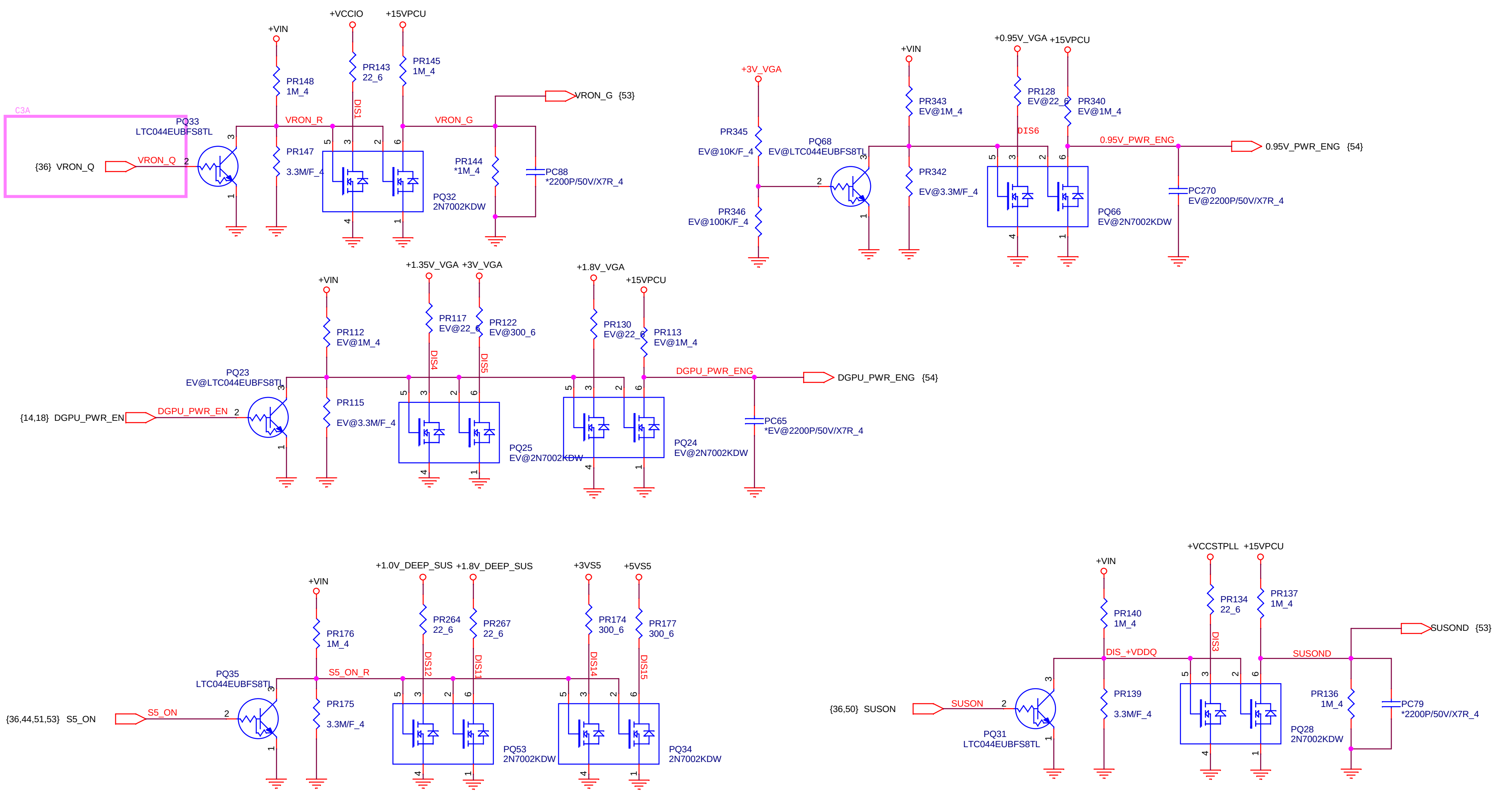
DISCHARGE



Quanta Computer Inc.

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Size	Document Number	Rev
	Discharge	1A

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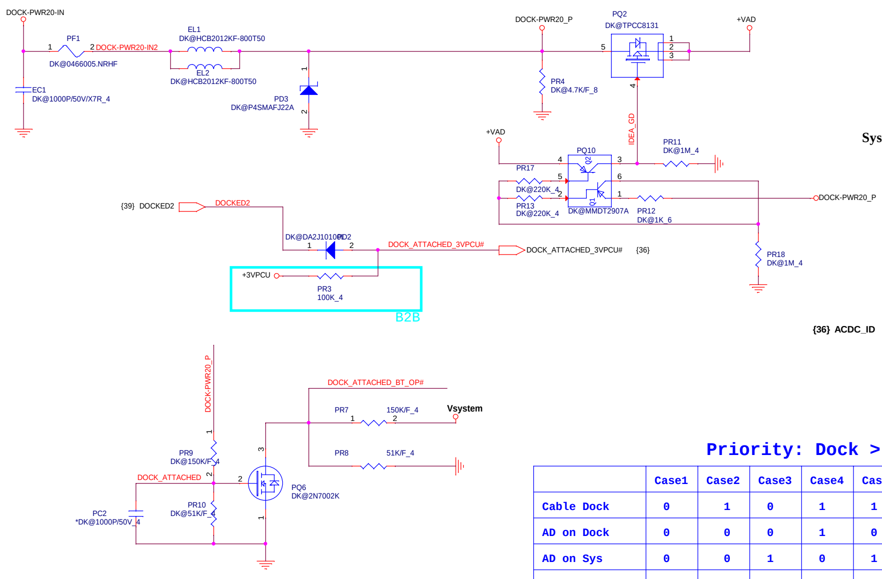
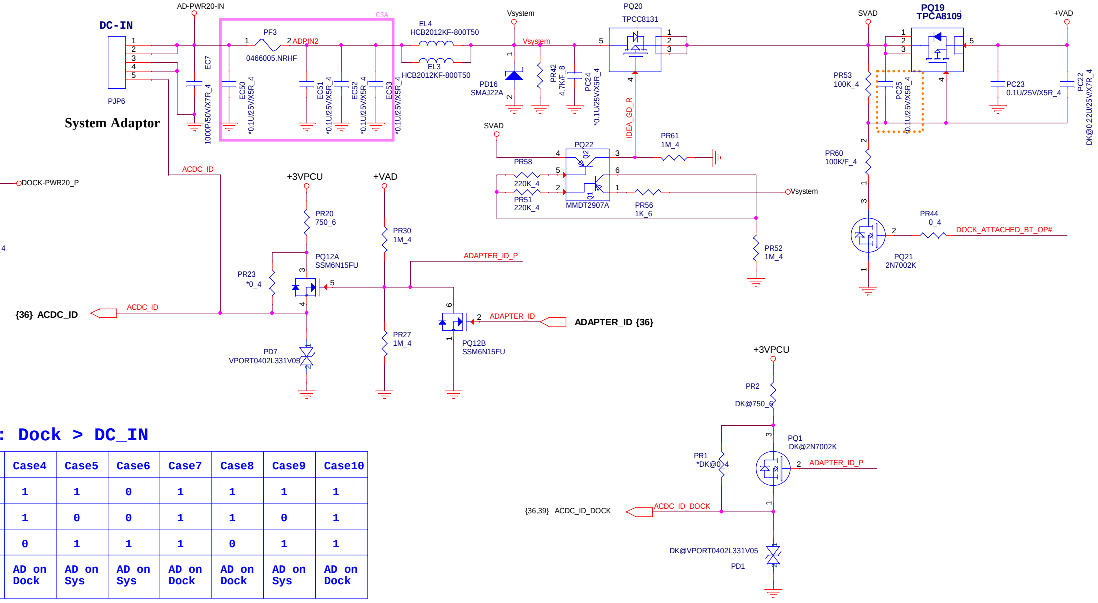
For Dock



For System



Priority: Dock > DC_IN

	Case1	Case2	Case3	Case4	Case5	Case6	Case7	Case8	Case9	Case10
Cable Dock	0	1	0	1	1	0	1	1	1	1
AD on Dock	0	0	0	1	0	0	1	1	0	1
AD on Sys	0	0	1	0	1	1	1	0	1	1
Power Source	Batt	Batt	AD on Sys	AD on Dock	AD on Sys	AD on Sys	AD on Dock	AD on Dock	AD on Sys	AD on Dock

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Size | Document Number: Power Source In Gate | Rev 1A
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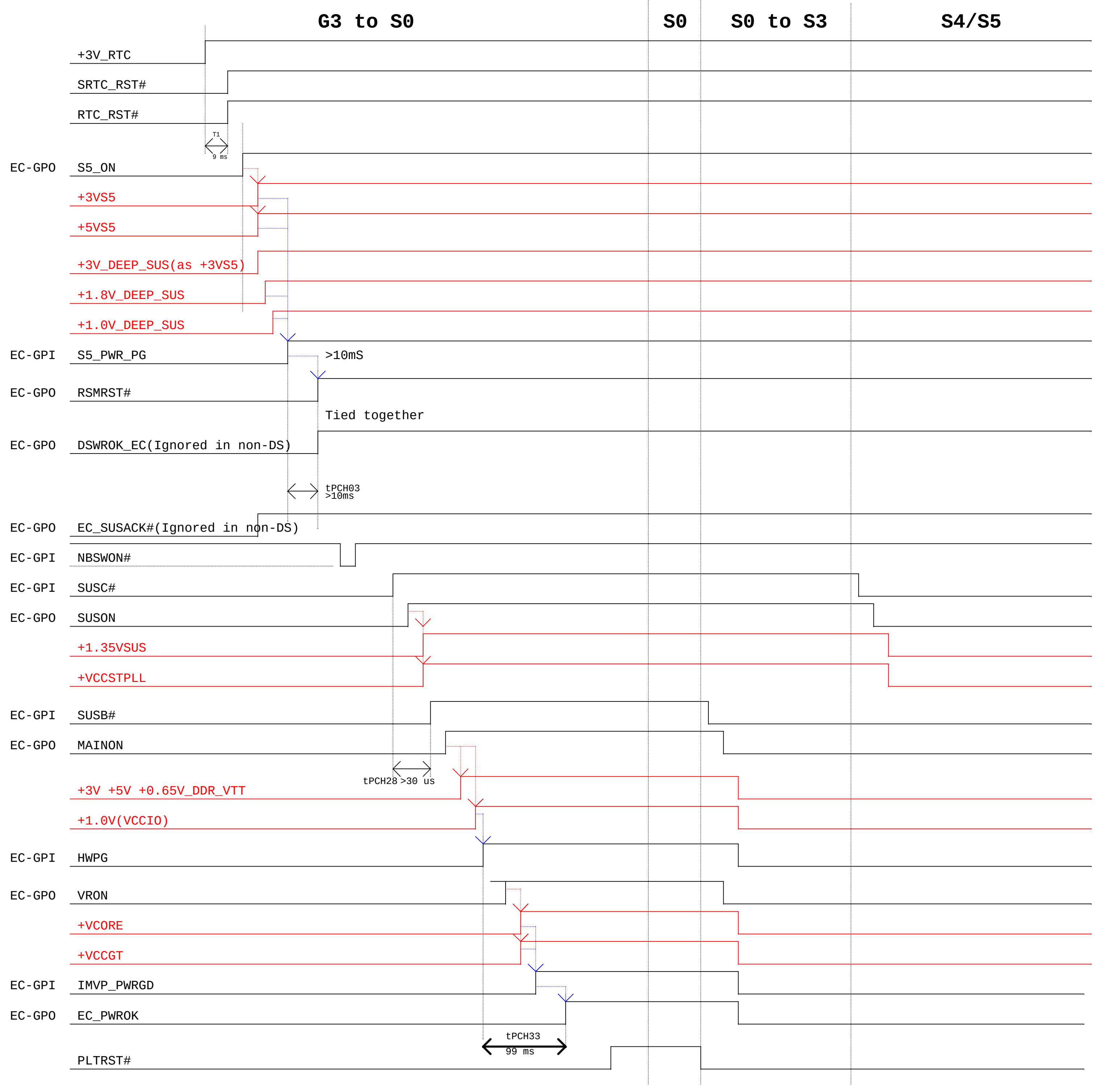

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PROJECT : LV6

Size	Document Number	Rev
	Power sequence2	1A

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	EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
2015	B2A	2	12/7	R780	Reserve PU 10K for
		4	12/7	R763	Add PU Res 10K for LAN_WAKE#.
		4	12/7	R764	Add PU Res 10K for VRALERT#.
		5	12/7	C819	Add Cap 1U for VCCSTG_G20.
		14	12/7	R768, R767	Add Board ID for SKYLAKE/ KABYLAKE.
		26	12/7	R769、R770、R771、R772、R773、R774、R775、R776	Add ohm for HDMI test
		30	12/7	CN14	Modify LAN connect pin define for LED
		31	12/7	CN19	Remove GND of stand pin for HDD connect
		31	12/7	CN12	Modify ODD connect to match FFC pin define
SDV-STAGE					
	B2B (R310)	30	12/18	CN14	Modify LAN connect pin define for LED
		4, 36	12/18	D10、R779、R780	Reserve DNBSWON# PU to +3VS5 and short 0 ohm
		13, 30	12/25	C755、C763、C359、C360	RTC CAP tuning
		29	12/25	R21、R16、R3、R8	FOR EMI

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Size	Document Number	Rev
	EC list 1	1A

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	EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
2015	C3A	4	1/8	R780	Reserve PU 10K for DNBSWON#
SIV-STAGE		4	1/8	U54、R781	Reserve PCH_SLP_S0# for power sequence
		12、13、39	1/8	C2、C3、C5、C6、C7、C8、C9、C10、C12、C13、C14、C16、C17、C18、C23、C549、C552、C553、C561、Q1、Q2、Q4、R1、R2、R4、R5、R17、R18、R19、R20、R445、R457、R462、TP29、U26、Y3、C700、C701	Remove DOCK LAN
		25、32、33、38	1/8	F2、F4、F7、F8	Change fuse to short pad
		30	1/8	CN14	Modify LED control signal
		34	1/8	C821、C822、C823、C824、R783、R784、R785、R786、C825、C826、C827、C828、R787、R788、R789、R790	Reserve EMI request
		36	1/8	R779	Reserve 0 ohm to jump diode for DNBSWON#
		38	1/8	R323、R329	Mount keyboard RES
		39	1/8	CN3	Change connect from 40 pin to 30 pin that remove DOCK LAN
		14	1/8		No memory down config
		41	1/8	C829、C830、C831、C832、C833	Add CAP for EMI request
		43	1/8	EC3、EC4、EC5、EC6	Add CAP for EMI request

2015

SIT-STAGE

EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION

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Size	Document Number	Rev
	EC list 3	1A

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