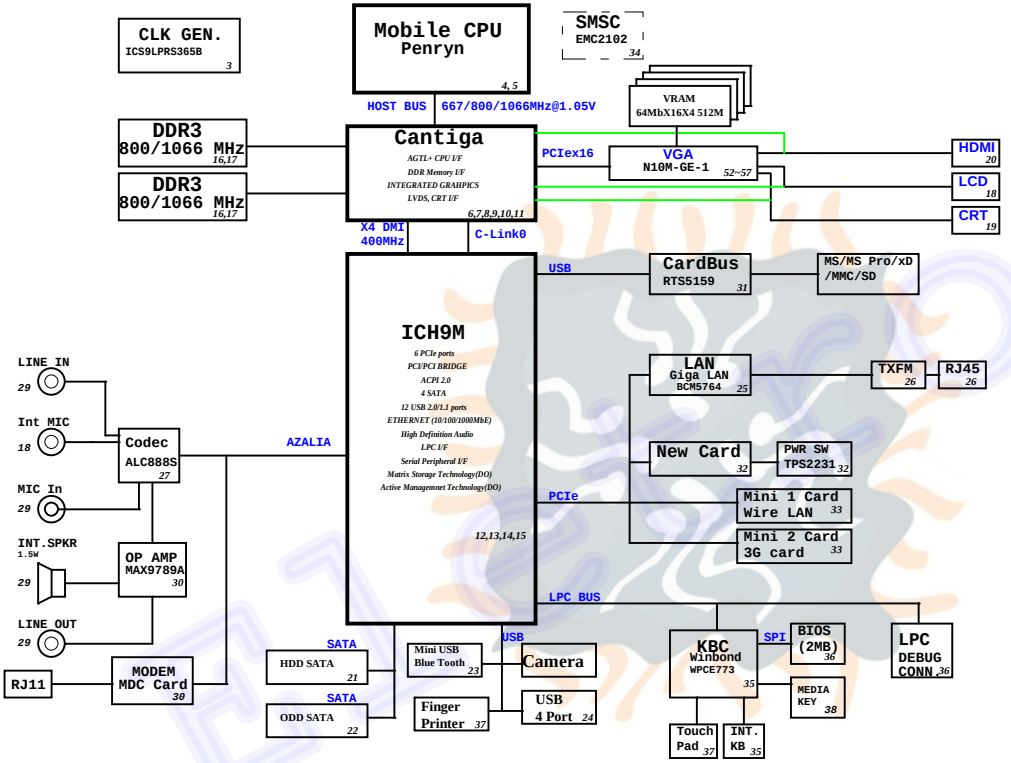
Project code: 91.4CG01.001
PCB P/N : 48.4CG01.0SA
REVISION : 08245-SA



PCB STACKUP

TOP		L1
GND		L2
S		L3
S		L4
GND		L5
BOTTOM		L6

SYSTEM DC/DC ISL62392 42

INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(7A) 5V_AUX_S5 3D3V_AUX_S5

SYSTEM DC/DC TPS51124 43

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(9A) 1D5V_S3(12A)

RT9026 44

1D5V_S3	DDR_VREF_S3 (1.2A)

RT9018 44

1D5V_S3	1D1V_S0(2A)

TPS51117 45

DCBATOUT	FBVDD(4A)

CHARGER ISL88731A 47

INPUTS	OUTPUTS
DCBATOUT	BT+

CPU DC/DC ISL6266A 41

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 38A

VGA_CORE RT8202A 47

INPUTS	OUTPUTS
DCBATOUT	VGA_CORE 13A

GFXCORE ISL6263A 46

INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE (7A)

JV50

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Title: BLOCK DIAGRAM
Size: A2 Document Number: JV50
Date: Thursday, January 08, 2009 Sheet 1 of

Check test point

3D3V_S0 — TP214 AFTE14P-GP
3D3V_AUX_S5 — TP213 AFTE14P-GP
3D3V_S5 — TP210 AFTE14P-GP
5V_S5 — TP209 AFTE14P-GP
13,35 PM_PWRBTN# — TP142 AFTE14P-GP
4,12,39 H_PWRGD — TP161 AFTE14P-GP
35,42 S5_ENABLE — TP160 AFTE14P-GP
4,6 H_CPURST# — TP112 AFTE14P-GP

Test Point放在Dimm Door打開可量測處

AMIC1 Conn. Test Point keep on connector side

18,27 INT_MIC1 — TP6 AFTE14P-GP
TP5 AFTE14P-GP

BT1 Conn. Test Point keep on connector side

13,23 USBPN7 — TP217 AFTE14P-GP
13,23 USBPP7 — TP218 AFTE14P-GP
TP220 AFTE14P-GP
3D3V_BT_S0 — TP219 AFTE14P-GP

USBCN1 Conn. Test Point keep on connector side

TP168 AFTE14P-GP
13,24 USB_OC#1 — TP163 AFTE14P-GP
TP162 AFTE14P-GP
13,24 USBPN1 — TP164 AFTE14P-GP
13,24 USBPP1 — TP166 AFTE14P-GP
13,24 USBPN2 — TP165 AFTE14P-GP
13,24 USBPP2 — TP167 AFTE14P-GP
24,35 USB_PWR_EN# — TP169 AFTE14P-GP
5V_S5 — TP170 AFTE14P-GP
5V_S5 — TP171 AFTE14P-GP

SPKR_R1 Conn. Test Point keep on conector side

28,29 SPKR_R+ — TP24 AFTE14P-GP
28,29 SPKR_R- — TP21 AFTE14P-GP

SPKR_L1 Conn. Test Point keep on conector side

28,29 SPKR_L+ — TP7 AFTE14P-GP
28,29 SPKR_L- — TP8 AFTE14P-GP

FAN1 Conn. Test Point keep on conector side

34 EMC2102_FAN_TACH_1 — TP175 AFTE14P-GP
34 EMC2102_FAN_DRIVE — TP176 AFTE14P-GP
TP177 AFTE14P-GP

KB1 Conn. Test Point keep on connector side

35 KCOL1 — TP48 AFTE14P-GP
35 KCOL2 — TP64 AFTE14P-GP
35 KCOL3 — TP47 AFTE14P-GP
35 KCOL4 — TP55 AFTE14P-GP
35 KCOL5 — TP38 AFTE14P-GP
35 KCOL6 — TP65 AFTE14P-GP
35 KCOL7 — TP42 AFTE14P-GP
35 KCOL8 — TP61 AFTE14P-GP
35 KCOL9 — TP45 AFTE14P-GP
35 KCOL10 — TP56 AFTE14P-GP
35 KCOL11 — TP39 AFTE14P-GP
35 KCOL12 — TP62 AFTE14P-GP
35 KCOL13 — TP46 AFTE14P-GP
35 KCOL14 — TP59 AFTE14P-GP
35 KCOL15 — TP43 AFTE14P-GP
35 KCOL16 — TP60 AFTE14P-GP
35 KCOL17 — TP44 AFTE14P-GP
35 KCOL18 — TP57 AFTE14P-GP

35 KROW1 — TP40 AFTE14P-GP
35 KROW2 — TP52 AFTE14P-GP
35 KROW3 — TP35 AFTE14P-GP
35 KROW4 — TP53 AFTE14P-GP
35 KROW5 — TP36 AFTE14P-GP
35 KROW6 — TP37 AFTE14P-GP
35 KROW7 — TP54 AFTE14P-GP
35 KROW8 — TP51 AFTE14P-GP
TP66 AFTE14P-GP

DB1 Conn. Test Point keep on conector side

3D3V_S0 — TP141 AFTE14P-GP
12,35,36 LPC_LAD0 — TP140 AFTE14P-GP
12,35,36 LPC_LAD1 — TP138 AFTE14P-GP
12,35,36 LPC_LAD2 — TP137 AFTE14P-GP
12,35,36 LPC_LAD3 — TP135 AFTE14P-GP
12,35,36 LPC_LFRAME# — TP133 AFTE14P-GP
7,13,25,31,32,33,35,36,52 PLT_RST1# — TP123 AFTE14P-GP
3,36 PCLK_FWH — TP117 AFTE14P-GP
TP143 AFTE14P-GP

TPCN1 Conn. Test Point keep on conector side

5V_S0 — TP77 AFTE14P-GP
5V_S0 — TP93 AFTE14P-GP
37 TP_DATA — TP108 AFTE14P-GP
37 TP_CLK — TP106 AFTE14P-GP
TP91 AFTE14P-GP
TP90 AFTE14P-GP
37 TP_RIGHT — TP80 AFTE14P-GP
37 TP_LEFT — TP79 AFTE14P-GP

FPCN1 Conn. Test Point keep on connector side

3D3V_FP_S0 — TP126 AFTE14P-GP
3D3V_FP_S0 — TP125 AFTE14P-GP
37 USBPP6_1 — TP128 AFTE14P-GP
37 USBPN6_1 — TP127 AFTE14P-GP
35,37 FP_DETECT# — TP132 AFTE14P-GP
37 TP_LEFT — TP124 AFTE14P-GP
37 TP_RIGHT — TP131 AFTE14P-GP
TP136 AFTE14P-GP
TP134 AFTE14P-GP
TP139 AFTE14P-GP

PSCN1 Conn. Test Point keep on connector side

3D3V_S0 — TP70 AFTE14P-GP
38 PWR_CON_BTN#_1 — TP69 AFTE14P-GP
38 PWR_CON_LED# — TP67 AFTE14P-GP
38 Volume_Up#_1 — TP58 AFTE14P-GP
38 Volume_Down#_1 — TP63 AFTE14P-GP
TP41 AFTE14P-GP

DCIN1 Conn. Test Point keep on connector side

AD_JK — TP9 AFTE14P-GP
TP10 AFTE14P-GP
TP11 AFTE14P-GP
TP12 AFTE14P-GP

TPCN1 Conn. Test Point keep on conector side

TP13 AFTE14P-GP
TP19 AFTE14P-GP
48 BATA_SDA_1 — TP14 AFTE14P-GP
48 BATA_SCL_1 — TP15 AFTE14P-GP
48 BAT_IN#_1 — TP16 AFTE14P-GP
BT+ — TP17 AFTE14P-GP
BT+ — TP18 AFTE14P-GP

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Title: AFTE TP

Size: A3 | Document Number: JV50 | Rev: 1A

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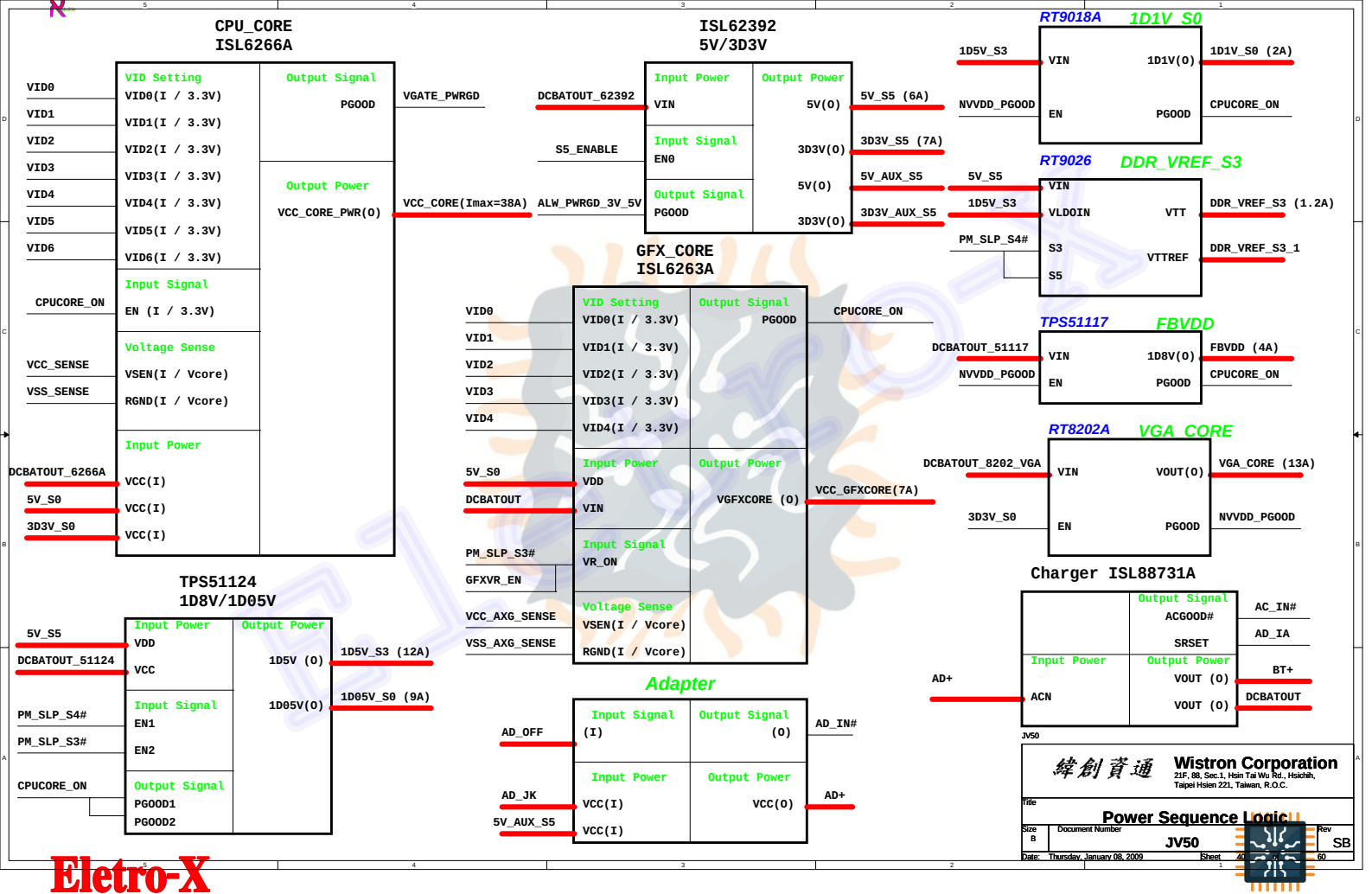
CPU_CORE
ISL6266A
VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)
VID6(I / 3.3V)
Output Signal
PGOOD
Output Power
VCC_CORE_PWR(O)
Input Signal
EN (I / 3.3V)
Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)
Input Power
VCC(I)
VCC(I)
VCC(I)
VID0
VID1
VID2
VID3
VID4
VID5
VID6
CPUCORE_ON
VCC_SENSE
VSS_SENSE
DCBATOUT_6266A
5V_S0
3D3V_S0
VGATE_PWRGD
VCC_CORE(Imax=38A)
ISL62392
5V/3D3V
Input Power
VIN
Input Signal
EN0
Output Signal
PGOOD
Output Power
5V(0)
3D3V(0)
5V(0)
3D3V(0)
DCBATOUT_62392
S5_ENABLE
ALW_PWRGD_3V_5V
5V_S5 (6A)
3D3V_S5 (7A)
5V_AUX_S5
3D3V_AUX_S5
GFX_CORE
ISL6263A
VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
Output Signal
PGOOD
Input Power
VDD
VIN
Output Power
VGFXCORE (O)
Input Signal
VR_ON
Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)
VID0
VID1
VID2
VID3
VID4
CPUCORE_ON
5V_S0
DCBATOUT
PM_SLP_S3#
GFXVR_EN
VCC_AXG_SENSE
VSS_AXG_SENSE
VCC_GFXCORE(7A)
RT9018A
1D1V_S0
1D5V_S3
VIN
1D1V(O)
1D1V_S0 (2A)
NVVDD_PGOOD
EN
PGOOD
CPUCORE_ON
RT9026
DDR_VREF_S3
5V_S5
1D5V_S3
PM_SLP_S4#
VIN
VLDOIN
VTT
S3
VTTREF
S5
DDR_VREF_S3 (1.2A)
DDR_VREF_S3_1
TPS51117
FBVDD
DCBATOUT_51117
NVVDD_PGOOD
VIN
1D8V(O)
EN
PGOOD
FBVDD (4A)
CPUCORE_ON
RT8202A
VGA_CORE
DCBATOUT_8202_VGA
3D3V_S0
VIN
VOUT(O)
EN
PGOOD
VGA_CORE (13A)
NVVDD_PGOOD
TPS51124
1D8V/1D05V
Input Power
VDD
VCC
Output Power
1D5V (O)
1D05V(O)
Input Signal
EN1
EN2
Output Signal
PGOOD1
PGOOD2
5V_S5
DCBATOUT_51124
PM_SLP_S4#
PM_SLP_S3#
CPUCORE_ON
1D5V_S3 (12A)
1D05V_S0 (9A)
Adapter
Input Signal
(I)
Output Signal
(O)
Input Power
VCC(I)
VCC(I)
Output Power
VCC(O)
AD_OFF
AD_JK
5V_AUX_S5
AD_IN#
AD+
Charger ISL88731A
Output Signal
ACGOOD#
SRSET
Input Power
ACN
Output Power
VOUT (O)
VOUT (O)
AD+
AC_IN#
AD_IA
BT+
DCBATOUT
JV50
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Title
Power Sequence Logic
Size
B
Document Number
JV50
Rev
SB
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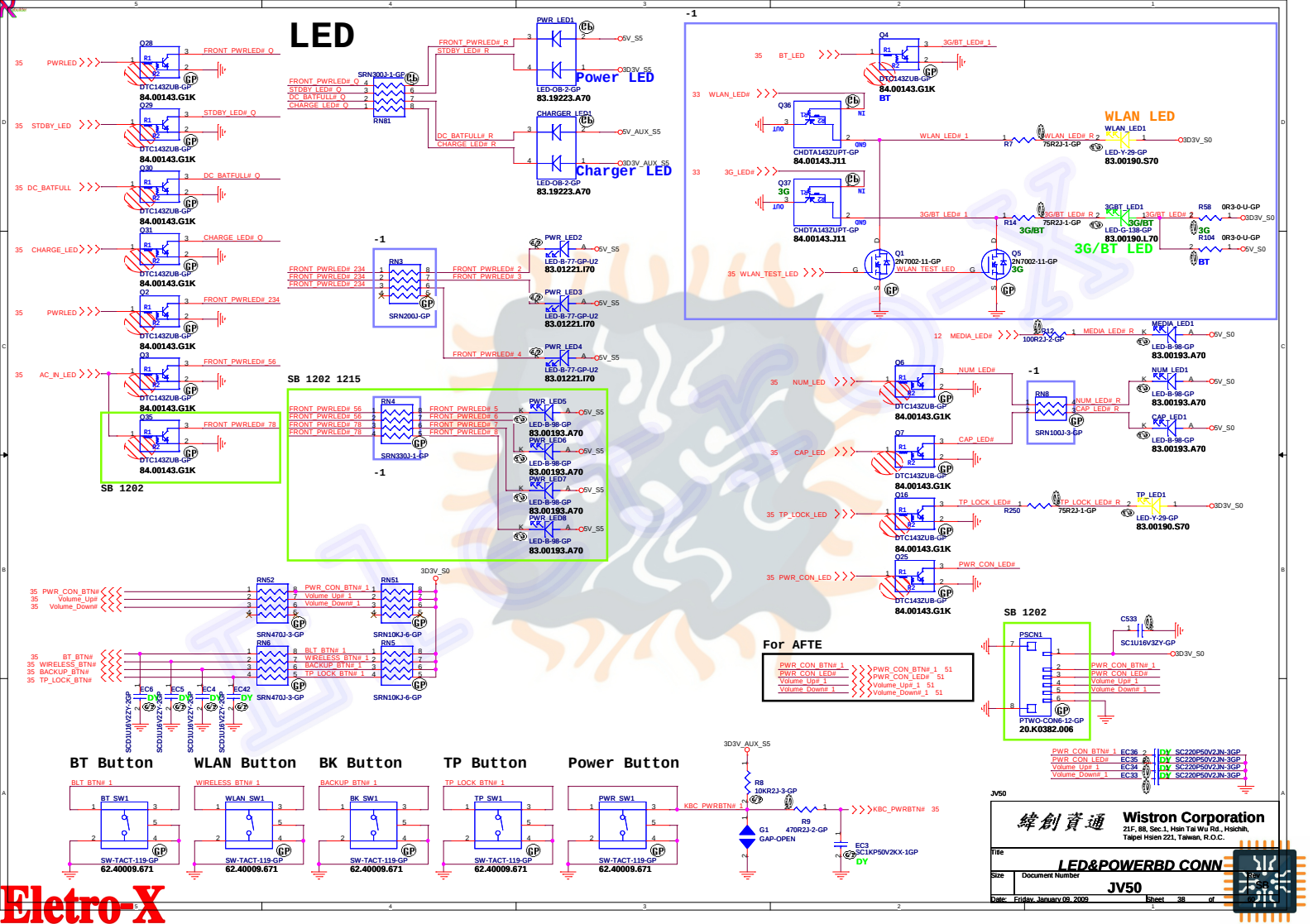
Eletro-X

LED


Power LED
Charger LED
WLAN LED
3G/BT LED
SB 1202
SB 1202 1215
For AFTE
BT Button
WLAN Button
BK Button
TP Button
Power Button
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LED&POWERBD CONN
JV50
Friday, January 09, 2009
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ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=The iTPM Host Interface is disalbed(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	0 = Only Digital Display Port or PCIE is operational (Default) 1 =Digital display Port and PCIe afe operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

JV50

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Title: Reference

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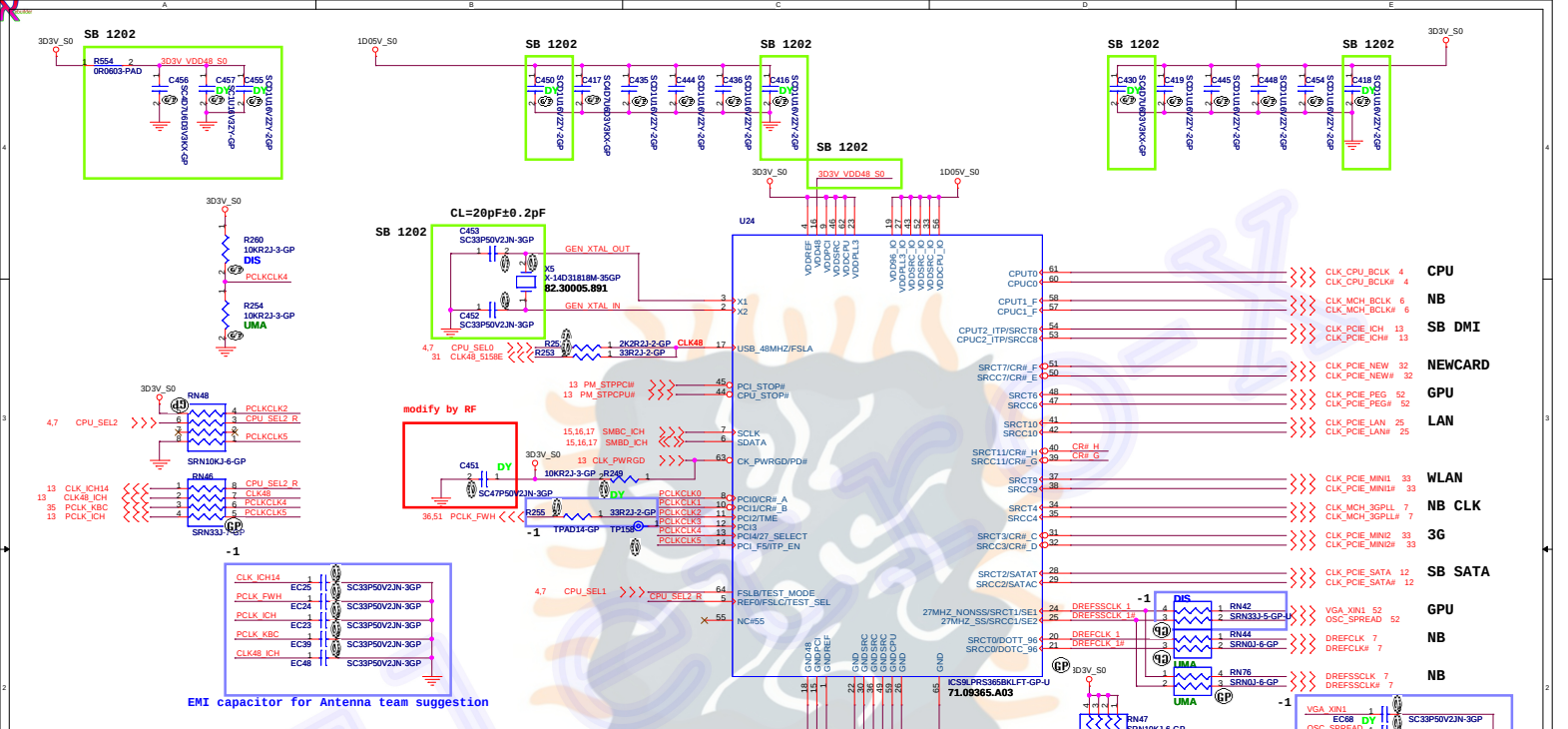

ICS9LPRS365YGLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

JV50

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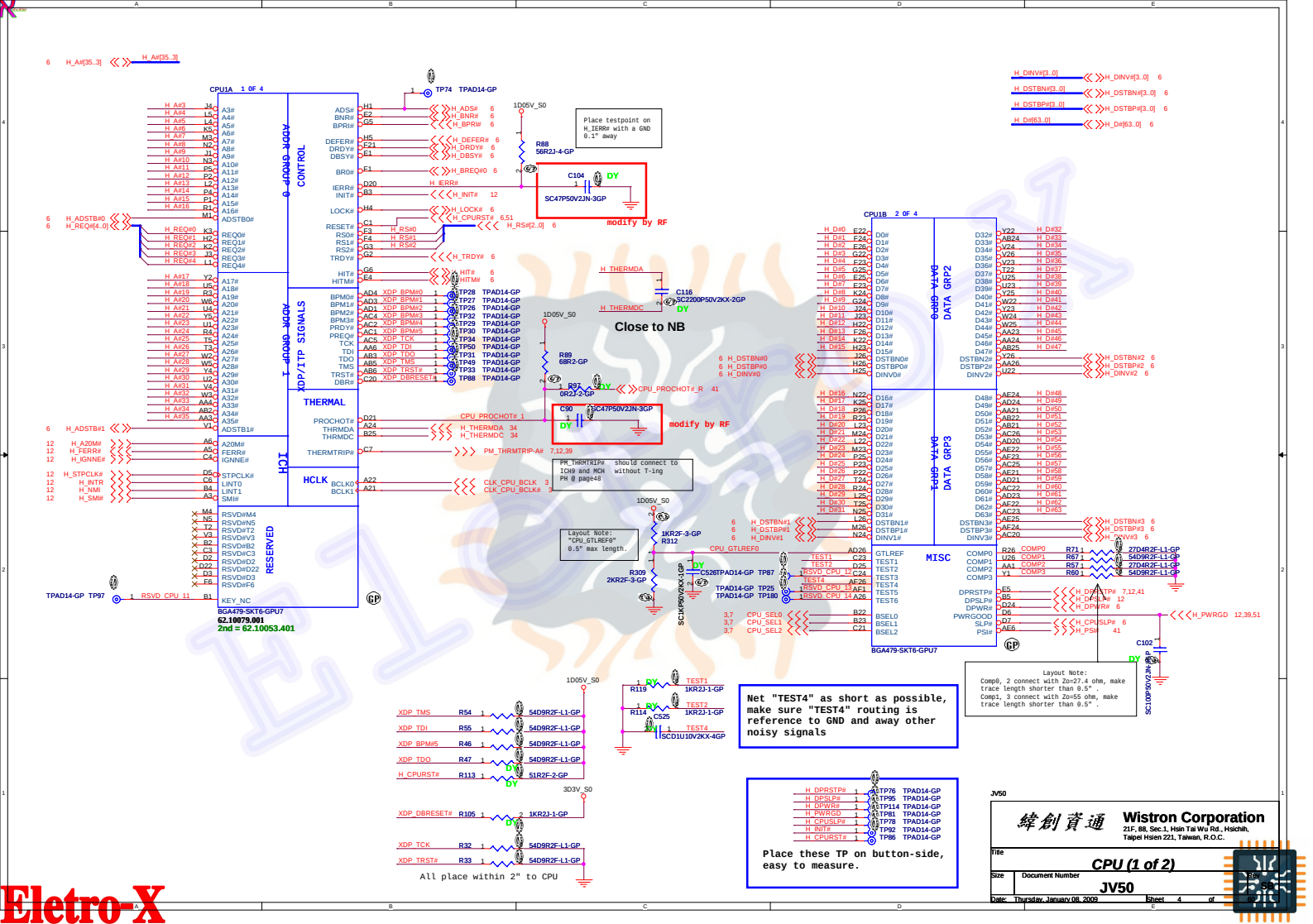
Title: Clock Generator
Size: Document Number: JV50
Date: Thursday, January 08, 2009 Sheet 3 of 53


CPU1A 1 OF 4
CPU1B 2 OF 4
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
HCLK
RESERVED
DATA GRP2
DATA GRP3
MISC
BGA479-SKT6-GPU7
62.10079.001
2nd = 62.10053.401
BGA479-SKT6-GPU7
Close to NB
modify by RF
modify by RF
Place testpoint on H_IERR# with a GND 0.1" away
PM_THRMTRIP# should connect to ICH9 and MCH without T-ing PH @ page48
Layout Note: "CPU_GTLREF0" 0.5" max length.
Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals
Place these TP on button-side, easy to measure.
All place within 2" to CPU
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
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CPU (1 of 2)
JV50
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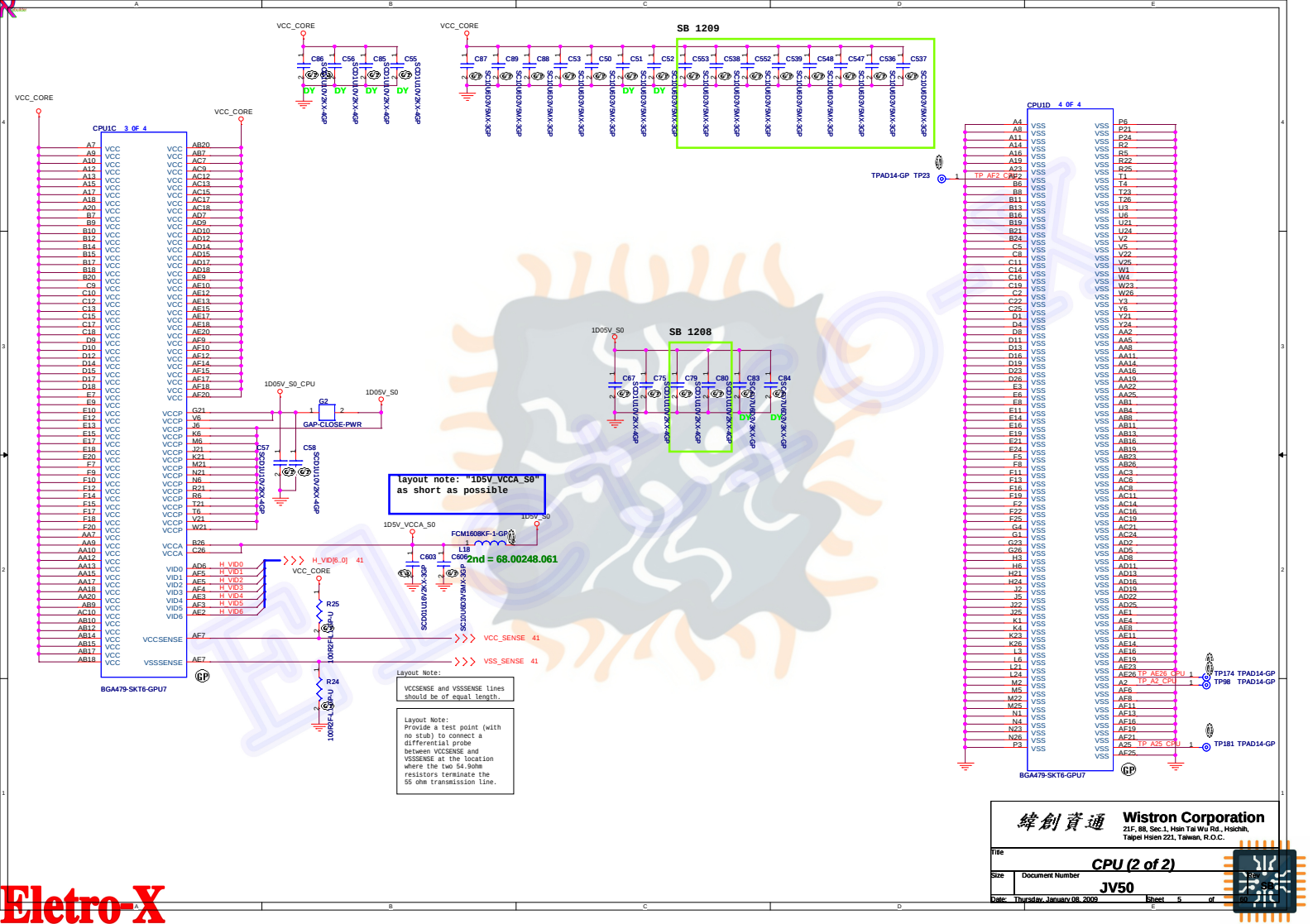
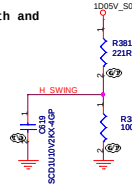

SB 1209
SB 1208
CPU1C 3 OF 4
CPU1D 4 OF 4
BGA479-SKT6-GPU7
VCC_CORE
1D05V_S0
1D05V_S0_CPU
1D05V_VCCA_S0
GAP-CLOSE-PWR
FCM1608KF-1-GP
TPAD14-GP
layout note: "1D5V_VCCA_S0" as short as possible
2nd = 68.00248.061
H_VID[6..0]
VCC_SENSE
VSS_SENSE
Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.
Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU (2 of 2)
JV50
Thursday, January 08, 2009
Sheet 5 of 50
Electro-X

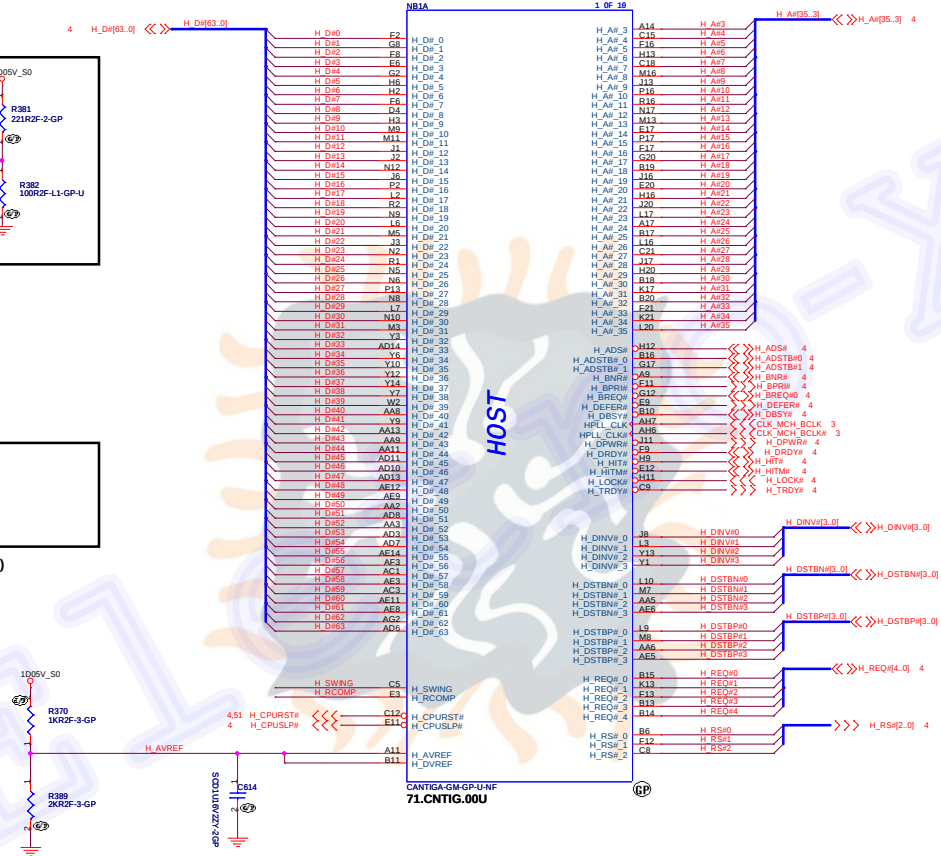
H_SWING routing Trace width and Spacing use 10 / 20 mil

H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil

Place them near to the chip (< 0.5")



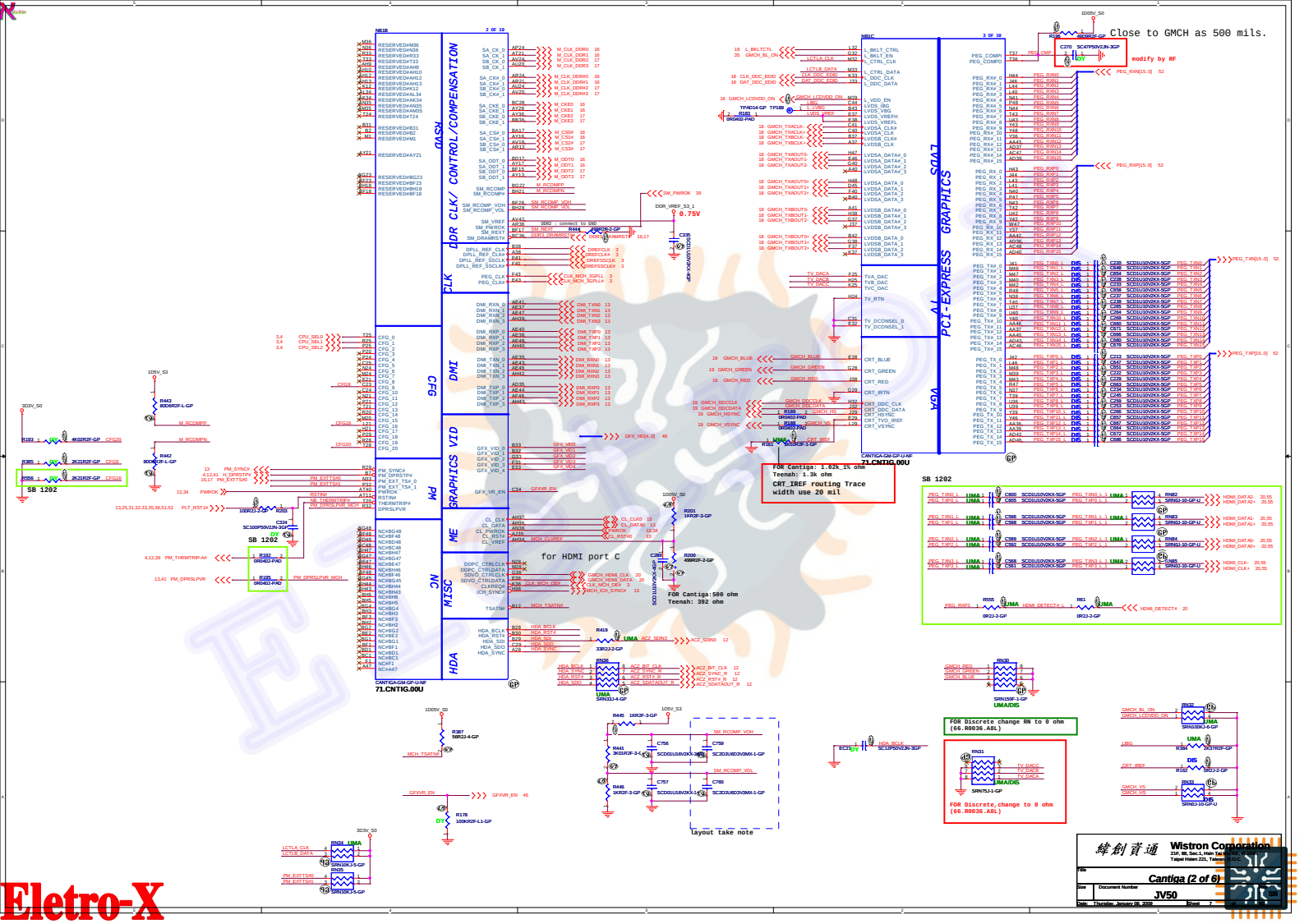
JV50

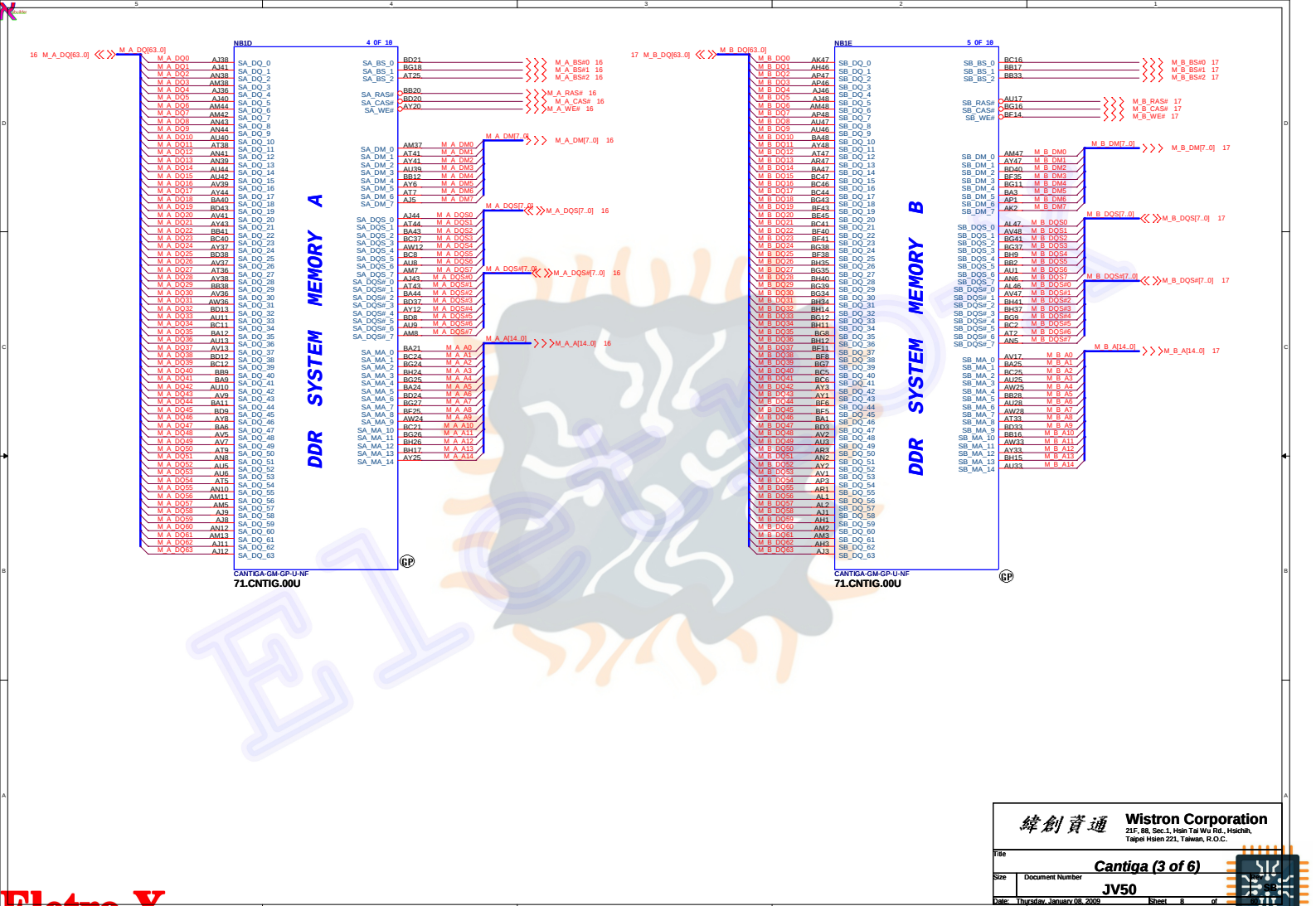
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga (1 of 6)

Size: | Document Number: JV50 | Rev: 0B

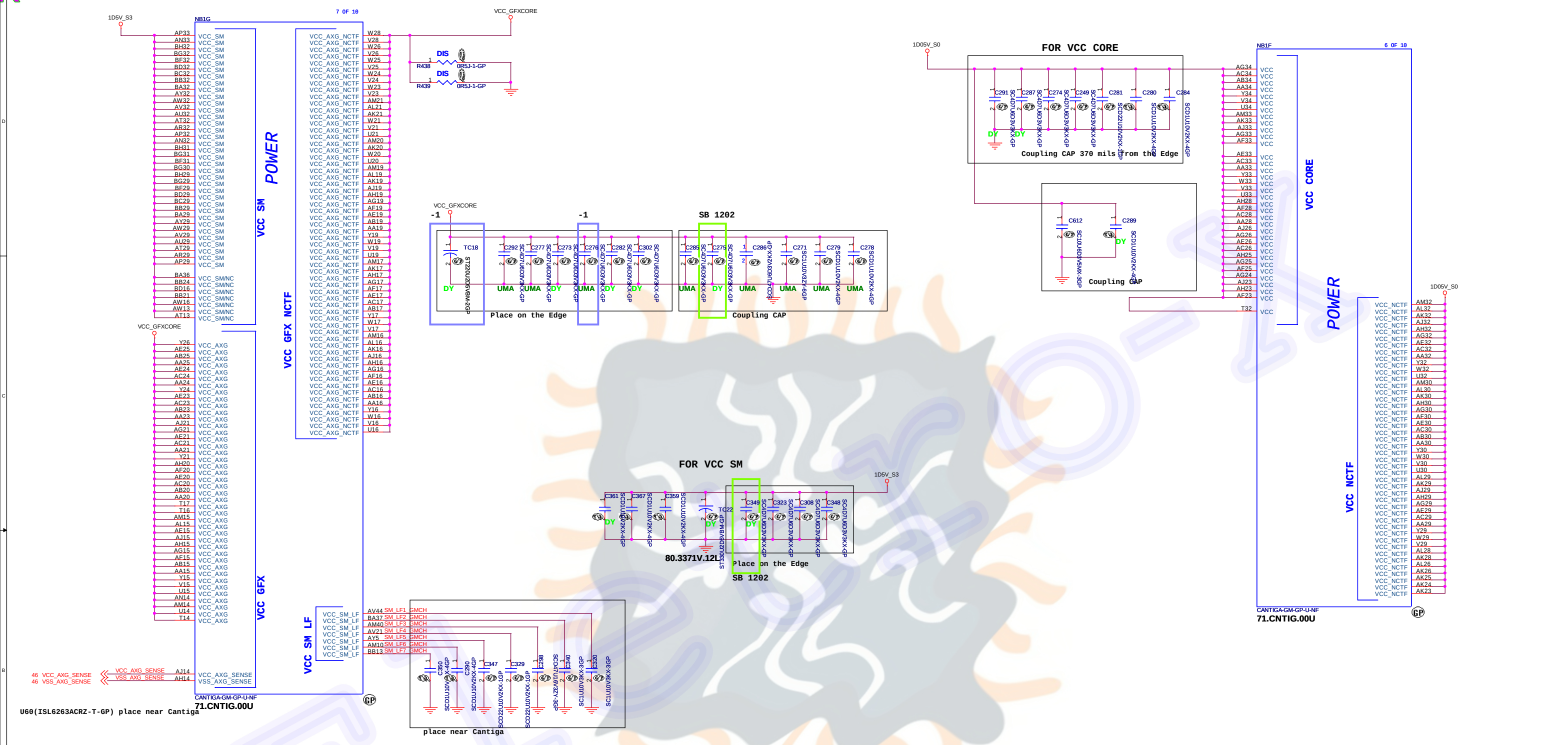
Date: Thursday, January 08, 2009 | Sheet 6 of


Close to GMCH as 500 mils.
modify by RF
DDR CLK / CONTROL/COMPENSATION
CFG
CLK
DMI
GRAPHICS VID
PM
ME
MISC
NC
HDA
LVDS
PCI-EXPRESS GRAPHICS
VGA
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
SB 1202
for HDMI port C
FOR Cantiga: 1.02k 1% ohm
Teenah: 1.3k ohm
CRT_IREF routing Trace
width use 20 mil
FOR Cantiga:500 ohm
Teenah: 392 ohm
FOR Discrete change RN to 0 ohm
(66.R0036.ABL)
FOR Discrete,change to 0 ohm
(66.R0036.ABL)
layout take note
UMA/DIS
Wistron Corporation
Cantiga (2 of 6)
JV50



Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: Cantiga (3 of 6)	
Size:	Document Number: JV50
Date: Thursday, January 08, 2009	Sheet 8 of 45

Eletro-X

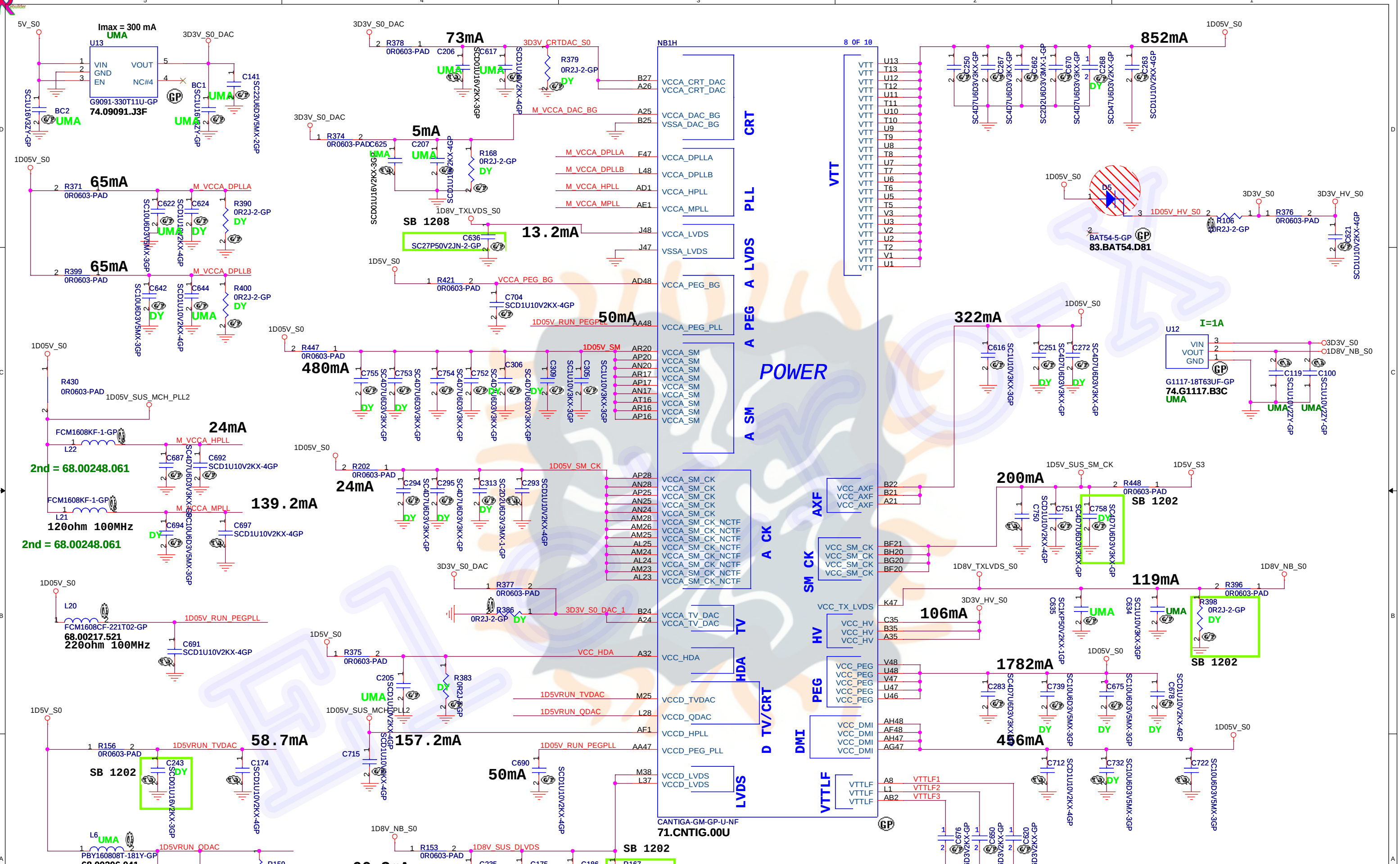


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Cantiga (4 of 6)**

Size | Document Number: **JV50** | Rev: SB

Date: Thursday, January 08, 2009 | Sheet 9 of 50



NB1H
8 OF 10
POWER
CRT
PLL
LVDS
A PEG
A SM
A CK
AXF
SM CK
TV
HV
HDA
PEG
D TV/CRT
DMI
LVDS
VTTLF
VTT
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
Imax = 300 mA
U13
G9091-330T11U-GP
74.09091.J3F
73mA
5mA
65mA
13.2mA
50mA
480mA
24mA
139.2mA
58.7mA
157.2mA
60.3mA
852mA
322mA
200mA
119mA
106mA
1782mA
456mA
I=1A
U12
G1117-18T63UF-GP
74.G1117.B3C
BAT54-5-GP
83.BAT54.D81
SB 1208
SB 1202
2nd = 68.00248.061
120ohm 100MHz
220ohm 100MHz
180ohm 100MHz
FCM1608CF-221T02-GP
68.00217.521
PBY160808T-181Y-GP
68.00206.041

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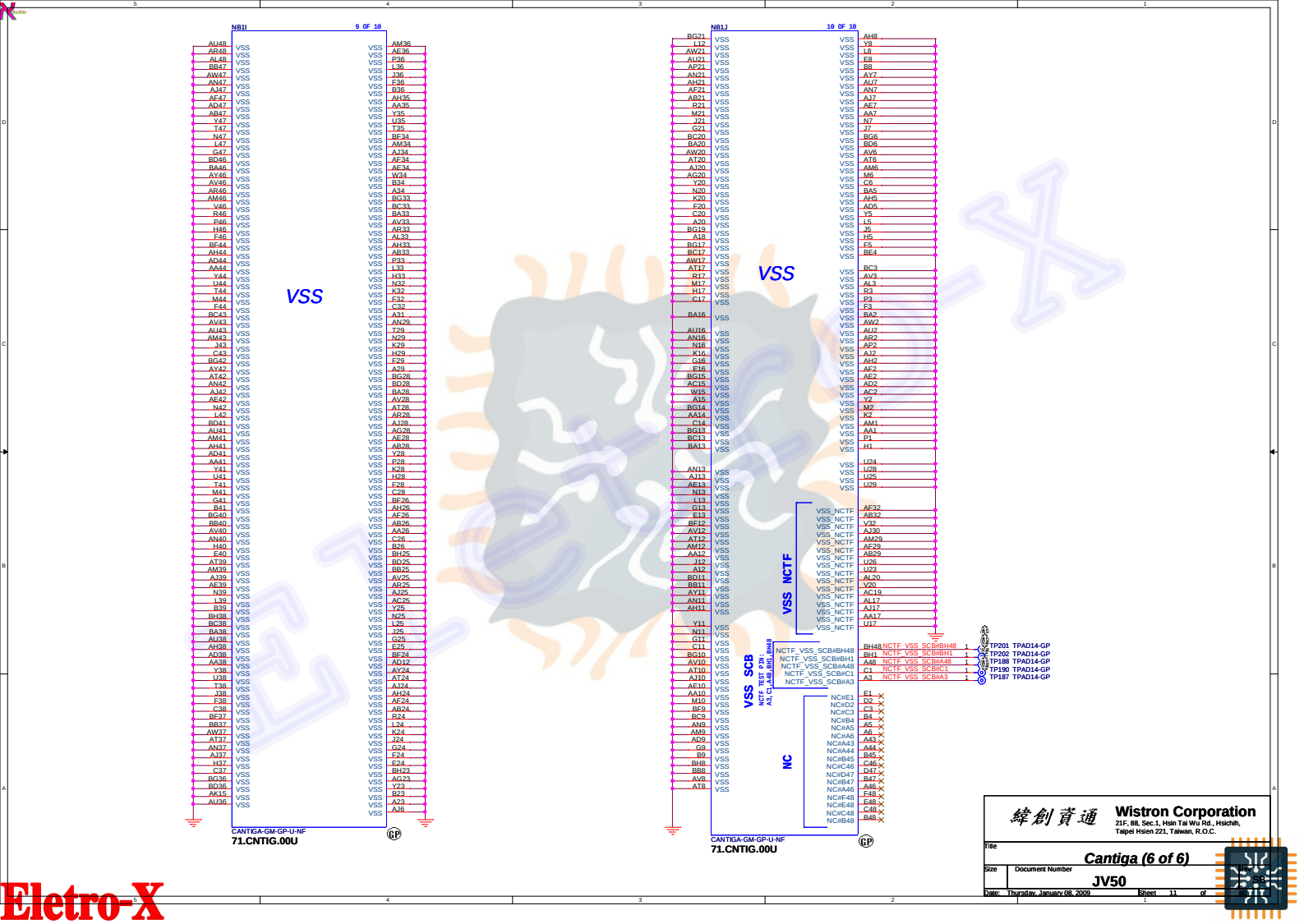
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga (5 of 6)

Size | Document Number: JV50 | Rev: SB

Date: Thursday, January 08, 2009 | Sheet 10 of 60

Eletro-X



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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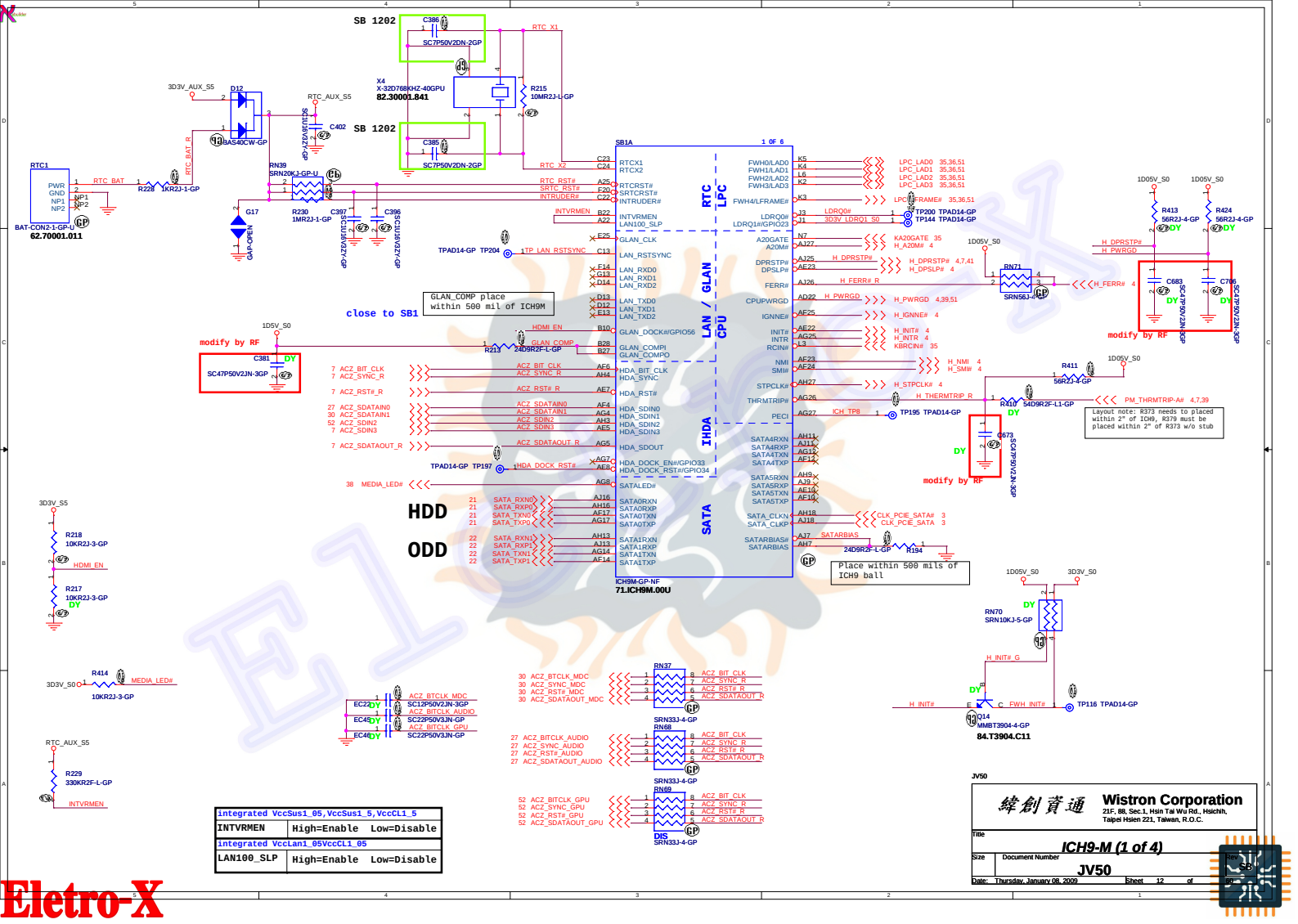
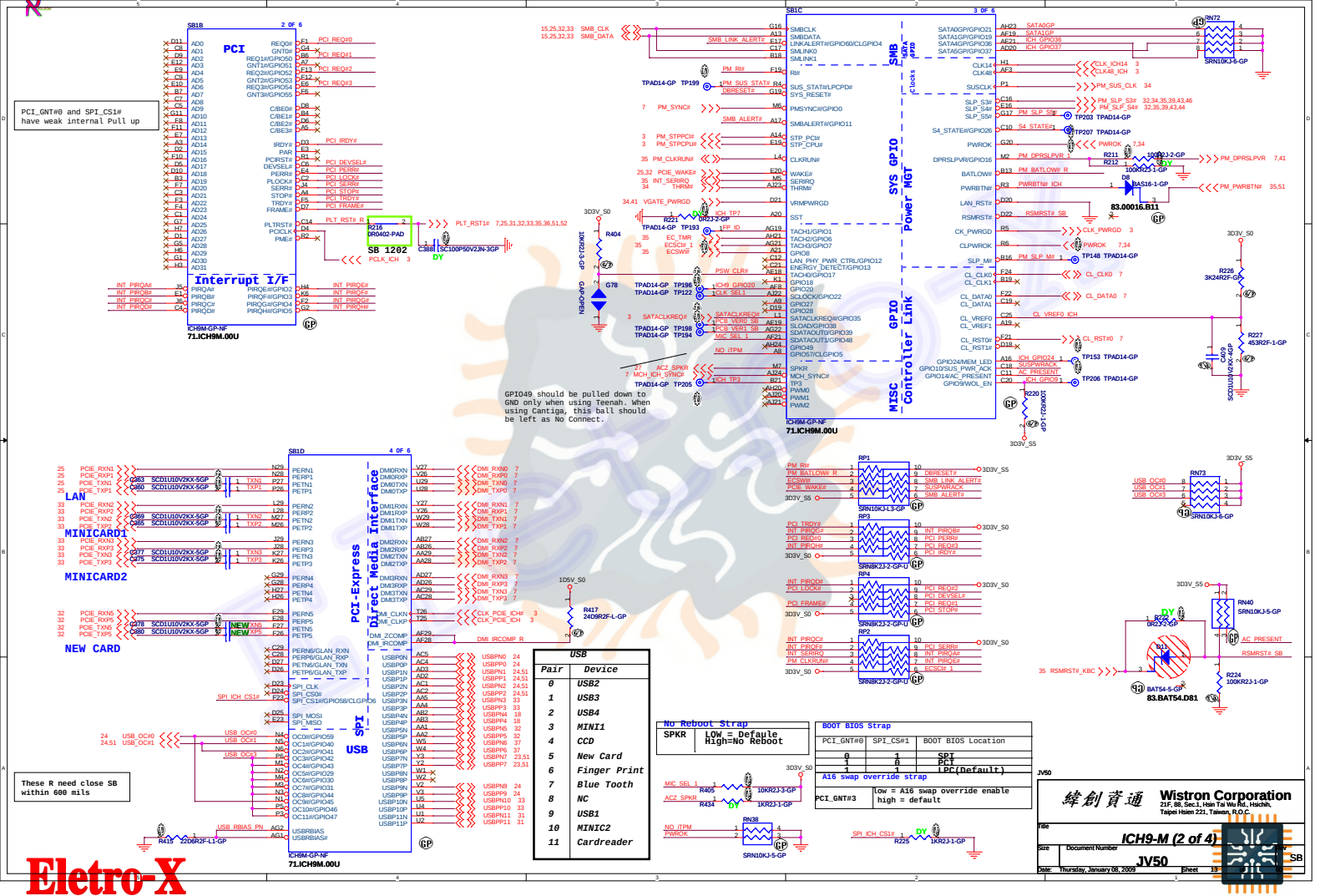
Title: Cantiga (6 of 6)

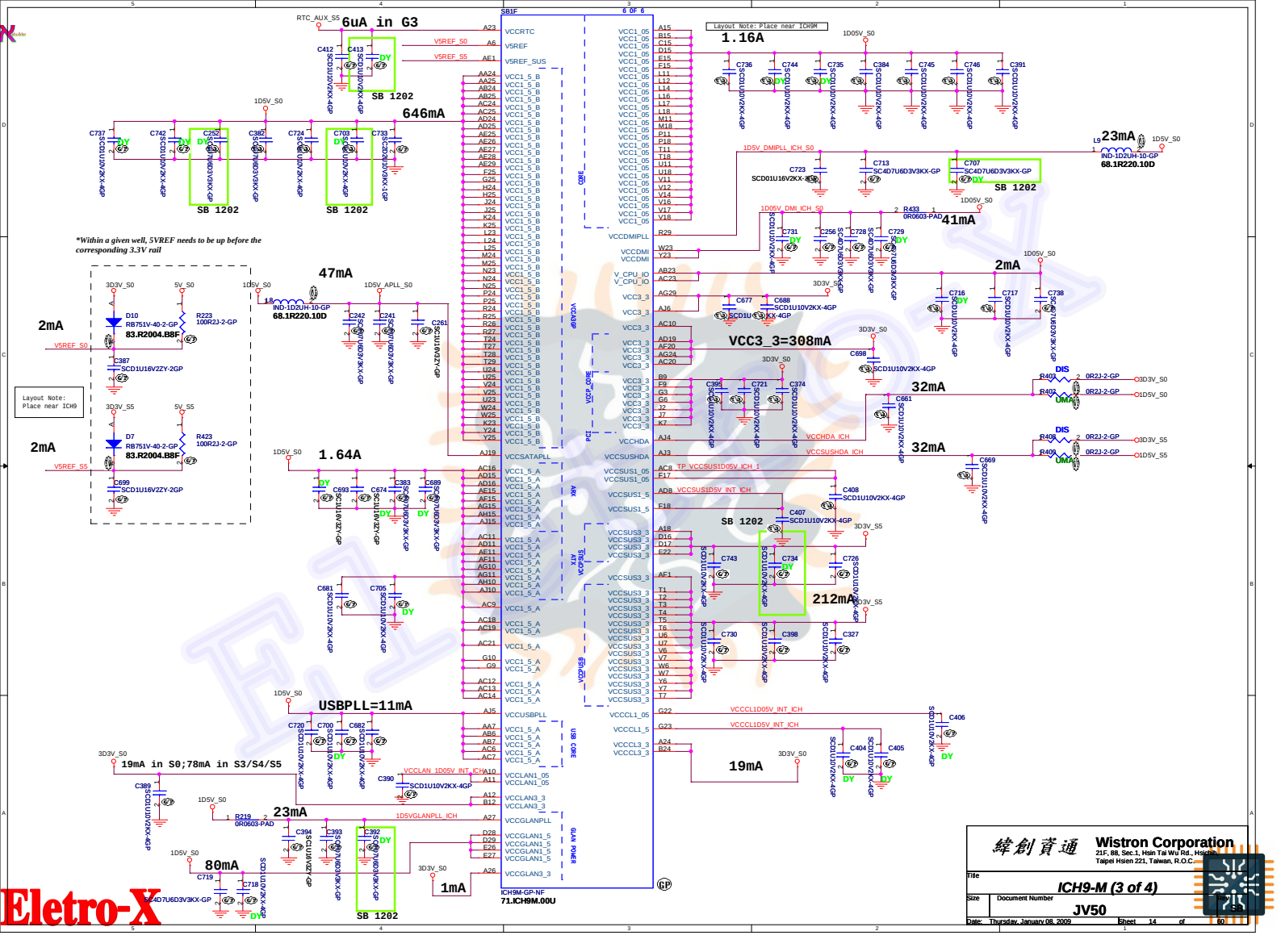
Size: | Document Number: JV50 | Rev: 0B

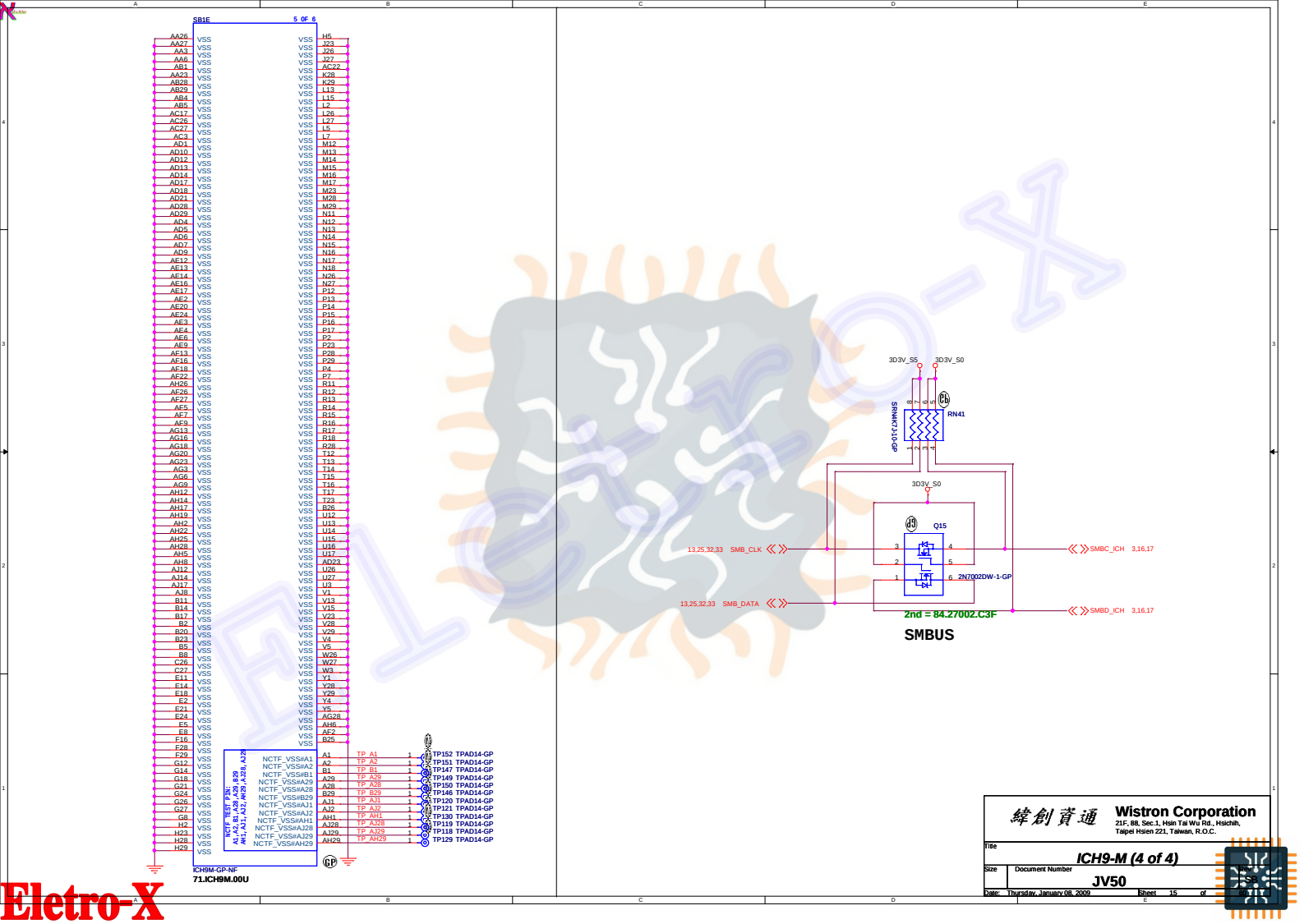
Date: Thursday, January 08, 2009 | Sheet 11 of 45

Eletro-X


SB 1202
SC7P50V2DN-2GP
X4
X-32D768KHZ-40GPU
82.30001.841
R215
10MR2J-L-GP
C386
C385
RTC_X1
RTC_X2
RTC1
BAT-CON2-1-GP-U
62.70001.011
RTC_BAT
RTC_BAT_R
R228
1KR2J-1-GP
D12
BAS40CW-GP
3D3V_AUX_S5
RTC_AUX_S5
C402
SC1U10V2ZY-2GP
RN39
SRN20K-J-GP-U
R230
1MR2J-1-GP
C397
C396
SC15P50V2JN-2GP
SC15P50V2JY-2GP
G17
GLP-OPEN
RTC_RST#
SRTC_RST#
INTRUDER#
INTVRMEN
TPAD14-GP TP204
TP_LAN_RSTSYNC
SB1A
1 OF 6
RTCX1
RTCX2
SRTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO56
GLAN_COMPI
GLAN_COMPO
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
PECI
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
LPC_LAD0 35,36,51
LPC_LAD1 35,36,51
LPC_LAD2 35,36,51
LPC_LAD3 35,36,51
LPC_FRAME# 35,36,51
LDRQ0# TP200 TPAD14-GP
3D3V_LDRQ1_S0 TP144 TPAD14-GP
KA20GATE 35
H_A20M# 4
H_DPRSTP# 4,7,41
H_DPSLP# 4
H_FERR# R
H_PWRGD 4,39,51
H_IGNNE# 4
H_INIT# 4
H_INTR 4
KBRCIN# 35
H_NMI 4
H_SMI# 4
H_STPCLK# 4
H_THRMTRIP_R
ICH_TP8
TP195 TPAD14-GP
CLK_PCIE_SATA# 3
CLK_PCIE_SATA 3
SATARBIAS
24D9R2F-L-GP
R194
ICH9M-GP-NF
71.ICH9M.00U
close to SB1
GLAN_COMP place within 500 mil of ICH9M
Place within 500 mils of ICH9 ball
1D05V_S0
modify by RF
C381
SC47P50V2JN-3GP
HDMI_EN
R213
24D9R2F-L-GP
GLAN_COMP
ACZ_BIT_CLK
ACZ_SYNC_R
ACZ_RST#_R
ACZ_SDATAIN0
ACZ_SDATAIN1
ACZ_SDIN2
ACZ_SDIN3
ACZ_SDATAOUT_R
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
HDA_DOCK_RST#
SATALED#
TPAD14-GP TP197
MEDIA_LED#
HDD
ODD
SATA_RXN0
SATA_RXP0
SATA_TXN0
SATA_TXP0
SATA_RXN1
SATA_RXP1
SATA_TXN1
SATA_TXP1
R218
10KR2J-3-GP
R217
10KR2J-3-GP
3D3V_S5
R414
10KR2J-3-GP
3D3V_S0
R229
330KR2F-L-GP
INTVRMEN
EC22DY
EC45DY
SC12P50V2JN-3GP
SC22P50V3JN-GP
ACZ_BTCLK_MDC
ACZ_BTCLK_AUDIO
ACZ_BTCLK_GPU
RN37
RN68
RN69
SRN33J-4-GP
ACZ_SYNC_MDC
ACZ_RST#_MDC
ACZ_SDATAOUT_MDC
ACZ_SYNC_AUDIO
ACZ_RST#_AUDIO
ACZ_SDATAOUT_AUDIO
ACZ_SYNC_GPU
ACZ_RST#_GPU
ACZ_SDATAOUT_GPU
DIS
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
R411
56R2J-3-GP
R410
54D9R2F-L1-GP
PM_THRMTRIP-A# 4,7,39
Layout note: R373 needs to placed within 2" of ICH9, R379 must be placed within 2" of R373 w/o stub
C673
SC47P50V2JN-3GP
RN71
SRN56J-4-GP
H_FERR# 4
R413
56R2J-4-GP
R424
56R2J-4-GP
H_DPRSTP#
H_PWRGD
C683
C706
SC47P50V2JN-3GP
RN70
SRN10KJ-5-GP
H_INIT#_G
H_INIT#
TP116 TPAD14-GP
Q14
MMBT3904-4-GP
84.T3904.C11
JV50
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (1 of 4)
Size
Document Number
JV50
Rev
1.0
Date: Thursday, January 08, 2009
Sheet 12 of

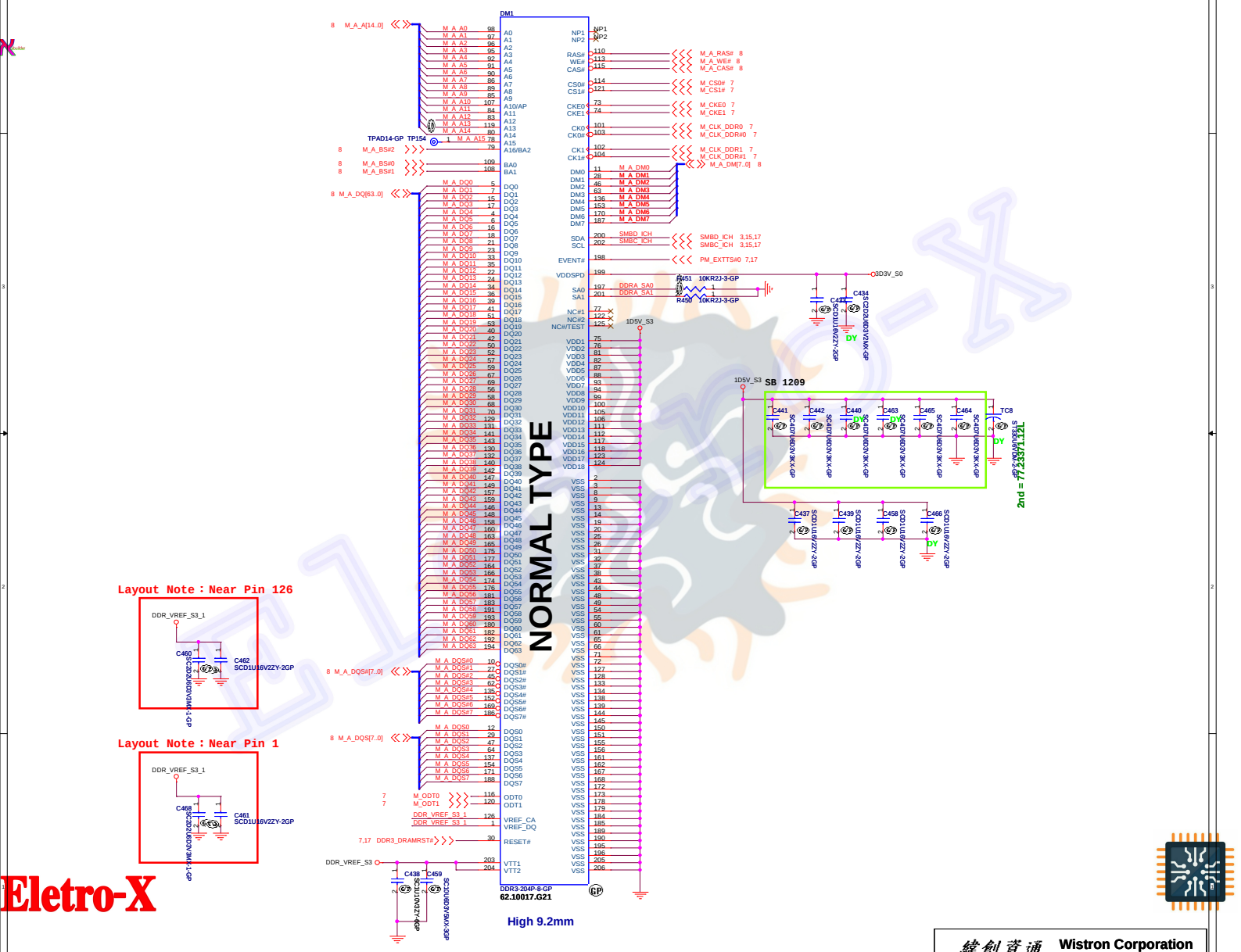

PCI_GNT#0 and SPI_CS1# have weak internal Pull up
SB1B 2 OF 6
PCI
Interrupt I/F
ICH9M-GP-NF
71.ICH9M.00U
SB 1202
SC100P50V2JN-3GP
PCLK_ICH
PLT_RST# R
R216 0R0402-PAD
PLT_RST# 7,25,31,32,33,35,36,51,52
SB1C 3 OF 6
SMB
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA0GP/GPIO36
SATA5GP/GPIO37
ICH GPIO37
ICH GPIO36
SRN10KJ-6-GP
CLK_ICH14 3
CLK48_ICH 3
PM_SUS_CLK 34
PM_SLP_S3# 32,34,35,39,43,46
PM_SLP_S4# 32,35,39,43,44
PM_SLP_S5# 7
TP203 TPAD14-GP
S4_STATE# 7
TP207 TPAD14-GP
PWROK 7,34
PM_DPRSLPVR 7,41
PM_BATLOW# R
PWRBTN# ICH
BAS16-1-GP
PM_PWRBT# 35,51
83.00016.B11
RSMRST# SB
CLK_PWRGD 3
PWROK 7,34
PM_SLP_M# 1
TP148 TPAD14-GP
CL_CLK0 7
CL_DATA0 7
CL_VREF0 ICH
CL_RST#0 7
TP153 TPAD14-GP
ICH_GPIO24 1
SUSPWRACK
AC_PRESENT
ICH_GPIO9 1
TP206 TPAD14-GP
SCD01U16V2KX-4GP
SB1D 4 OF 6
LAN
MINICARD1
MINICARD2
NEW CARD
PCI-Express
Direct Media Interface
SPI
USB
ICH9M-GP-NF
71.ICH9M.00U
These R need close SB within 600 mils
GPIO49 should be pulled down to GND only when using Teenah. When using Cantiga, this ball should be left as No Connect.
USB
Pair Device
0 USB2
1 USB3
2 USB4
3 MINI1
4 CCD
5 New Card
6 Finger Print
7 Blue Tooth
8 NC
9 USB1
10 MINIC2
11 Cardreader
No Reboot Strap
SPKR LOW = Defaule
High=No Reboot
BOOT BIOS Strap
PCI_GNT#0 SPI_CS#1 BOOT BIOS Location
0 1 SPI
1 0 PCI
1 1 LPC(Default)
A16 swap override strap
PCI_GNT#3 low = A16 swap override enable
high = default
JV50
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (2 of 4)
Size Document Number Rev
JV50 SB
Date: Thursday, January 08, 2009 Sheet 15
Electro-X

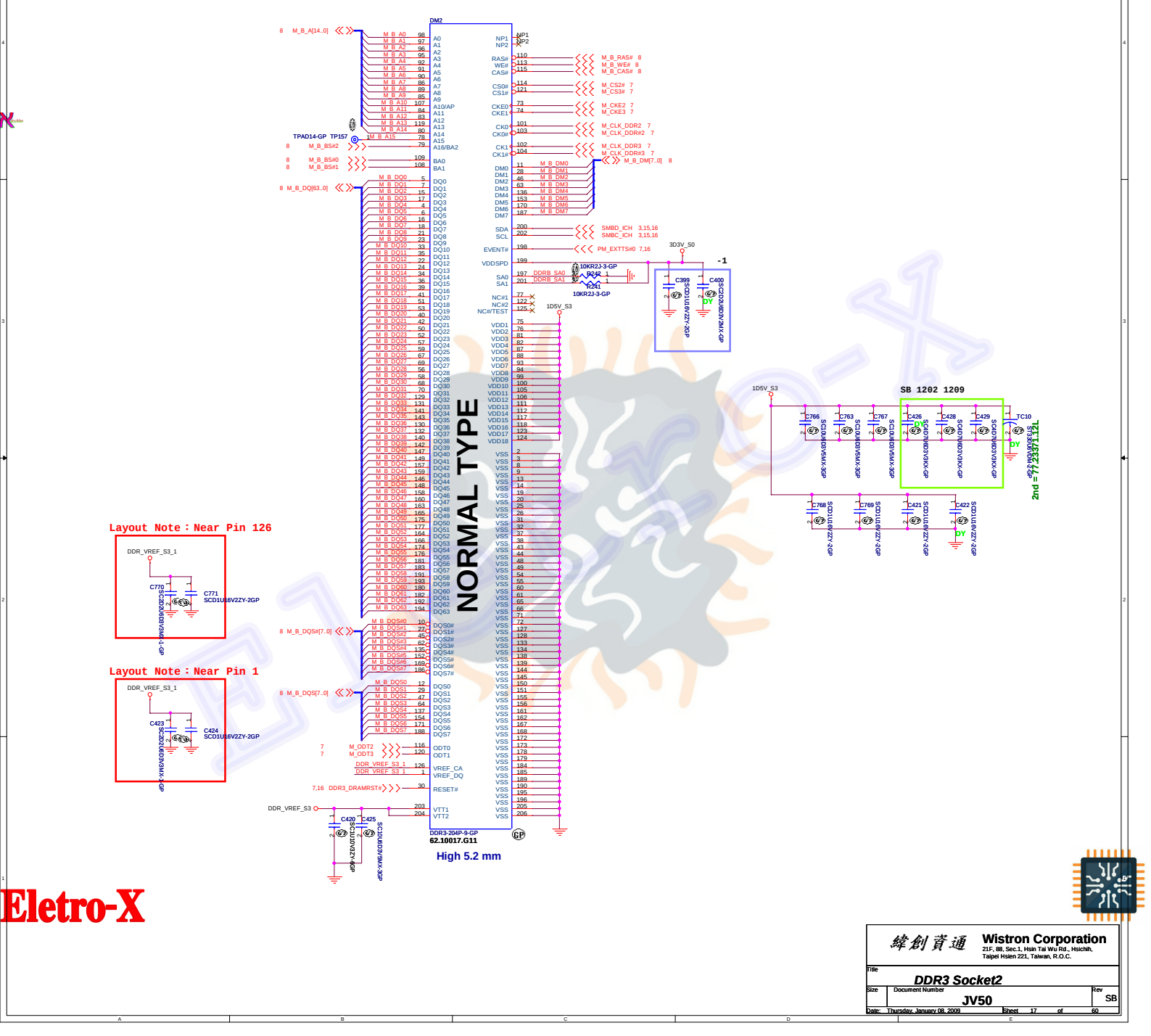

6uA in G3
646mA
SB 1202
1.16A
23mA
68.1R220.10D
41mA
2mA
47mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
VCC3_3=308mA
32mA
1.64A
USBPLL=11mA
19mA in S0;78mA in S3/S4/S5
212mA
80mA
1mA
ICH9M-GP-NF
71.ICH9M.00U
Layout Note: Place near ICH9M
Wistron Corporation
ICH9-M (3 of 4)
JV50



Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ICH9-M (4 of 4)	
Size:	Document Number: JV50
Date: Thursday, January 08, 2009	Sheet 15 of

Eletro-X


DM1
NORMAL TYPE
DDR3-204P-8-GP
62.10017.G21
High 9.2mm
TPAD14-GP TP154
SB 1209
2nd = 77.23371.12L
Layout Note : Near Pin 126
Layout Note : Near Pin 1
DDR_VREF_S3_1
C460
C462
SCD1U16V2ZY-2GP
C468
C461
C438
C459
C441
C442
C440
C463
C465
C464
TC8
C437
C439
C458
C466
R451
R450
10KR2J-3-GP
C434
SC2R2U6V3NX-GP
SCD1U16V2ZY-2GP
SC47U6V3MX-GP
SC1U6V3KX-3GP
M_A_A[14..0]
M_A_BS#2
M_A_BS#0
M_A_BS#1
M_A_DQ[63..0]
M_A_DQS#[7..0]
M_A_DQS[7..0]
M_ODT0
M_ODT1
DDR3_DRAMRST#
M_A_RAS#
M_A_WE#
M_A_CAS#
M_CS0#
M_CS1#
M_CKE0
M_CKE1
M_CLK_DDR0
M_CLK_DDR#0
M_CLK_DDR1
M_CLK_DDR#1
M_A_DM[7..0]
SMBD_ICH
SMBC_ICH
PM_EXTTS#0
3D3V_S0
1D5V_S3
DDRA_SA0
DDRA_SA1
DDR_VREF_S3
Eletro-X
緯創資通 Wistron Corporation



Eletro-X

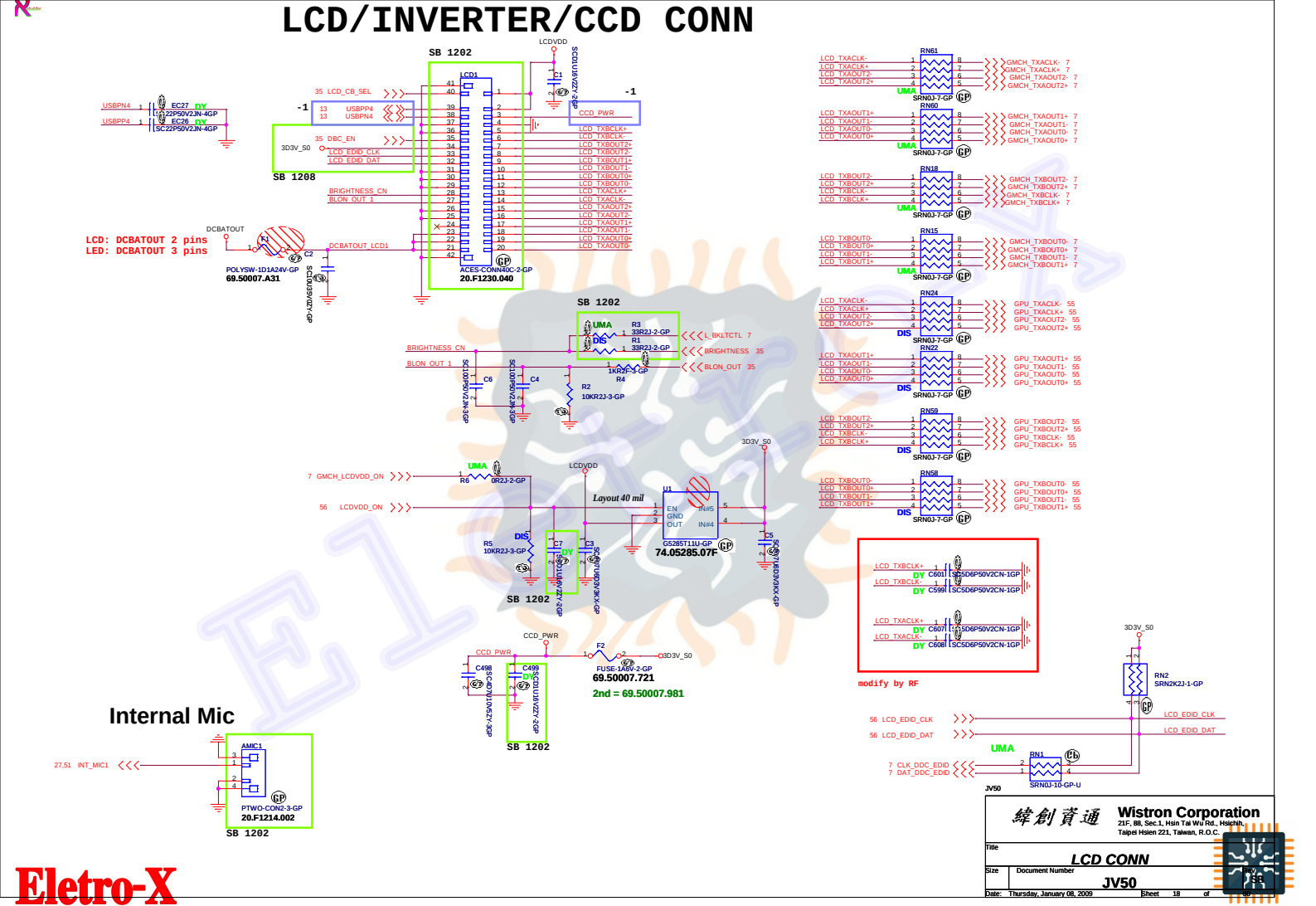
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

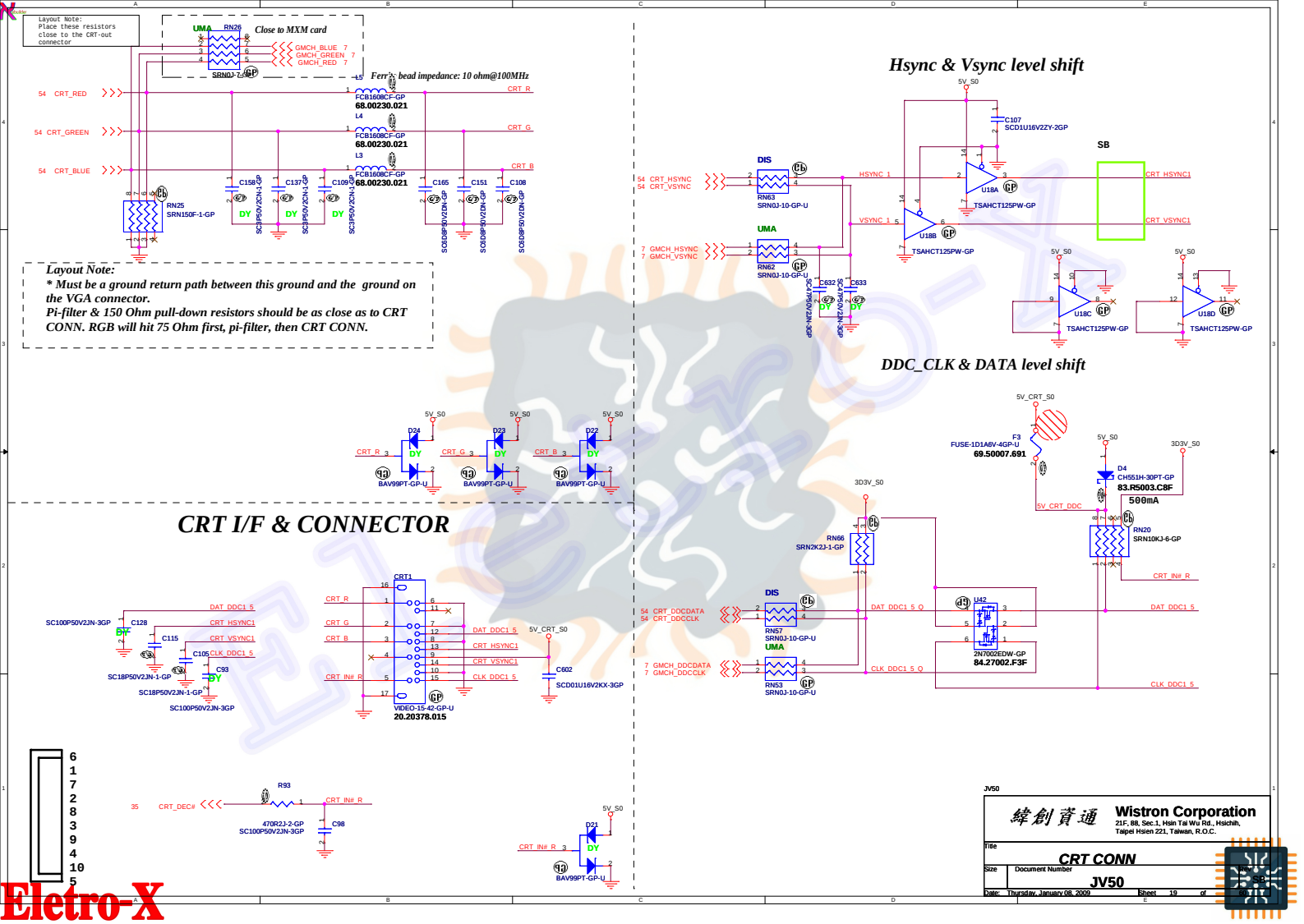
Title: DDR3 Socket2

Size	Document Number	Rev
	JV50	SB

Date: Thursday, January 08, 2009 Sheet 17 of 60

LCD/INVERTER/CCD CONN




Layout Note:
Place these resistors close to the CRT-out connector
UMA
RN26
SRN0J-7-GP
Close to MXM card
GMCH_BLUE 7
GMCH_GREEN 7
GMCH_RED 7
54 CRT_RED
54 CRT_GREEN
54 CRT_BLUE
L5
L4
L3
FCB1608CF-GP
68.00230.021
Ferrite bead impedance: 10 ohm@100MHz
CRT_R
CRT_G
CRT_B
RN25
SRN150F-1-GP
C158
C137
C109
C165
C151
C108
SC18P50V2CN-1-GP
SCD1U16V2KX-3GP
DY
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.
Hsync & Vsync level shift
5V_S0
DIS
UMA
54 CRT_HSYNC
54 CRT_VSYNC
7 GMCH_HSYNC
7 GMCH_VSYNC
RN63
RN62
SRN0J-10-GP-U
HSYNC_1
VSYNC_1
C107
SCD1U16V2ZY-2GP
SB
U18A
U18B
U18C
U18D
TSAHTC125PW-GP
CRT_HSYNC1
CRT_VSYNC1
C632
C633
SC47P50V2JN-3GP
DDC_CLK & DATA level shift
D24
D23
D22
BAV99PT-GP-U
3D3V_S0
5V_CRT_S0
F3
FUSE-1D1A6V-4GP-U
69.50007.691
D4
CH551H-30PT-GP
83.R5003.C8F
500mA
5V_CRT_DDC
RN20
SRN10KJ-6-GP
CRT_IN#_R
RN66
SRN2K2J-1-GP
54 CRT_DDCDATA
54 CRT_DDCCLK
7 GMCH_DDCDATA
7 GMCH_DDCCLK
RN57
RN53
SRN0J-10-GP-U
DAT_DDC1_5_Q
CLK_DDC1_5_Q
U42
2N7002EDW-GP
84.27002.F3F
DAT_DDC1_5
CLK_DDC1_5
CRT I/F & CONNECTOR
CRT1
VIDEO-15-42-GP-U
20.20378.015
SC100P50V2JN-3GP
C128
C115
C105
C93
C602
SCD01U16V2KX-3GP
SC18P50V2JN-1-GP
SC100P50V2JN-3GP
DAT_DDC1_5
CRT_HSYNC1
CRT_VSYNC1
CLK_DDC1_5
R93
CRT_DEC#
470R2J-2-GP
C98
D21
BAV99PT-GP-U
6 1 7 2 8 3 9 4 10 5
JV50
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CRT CONN
Size
Document Number
JV50
Rev
SB
Date: Thursday, January 08, 2009
Sheet 19 of 45
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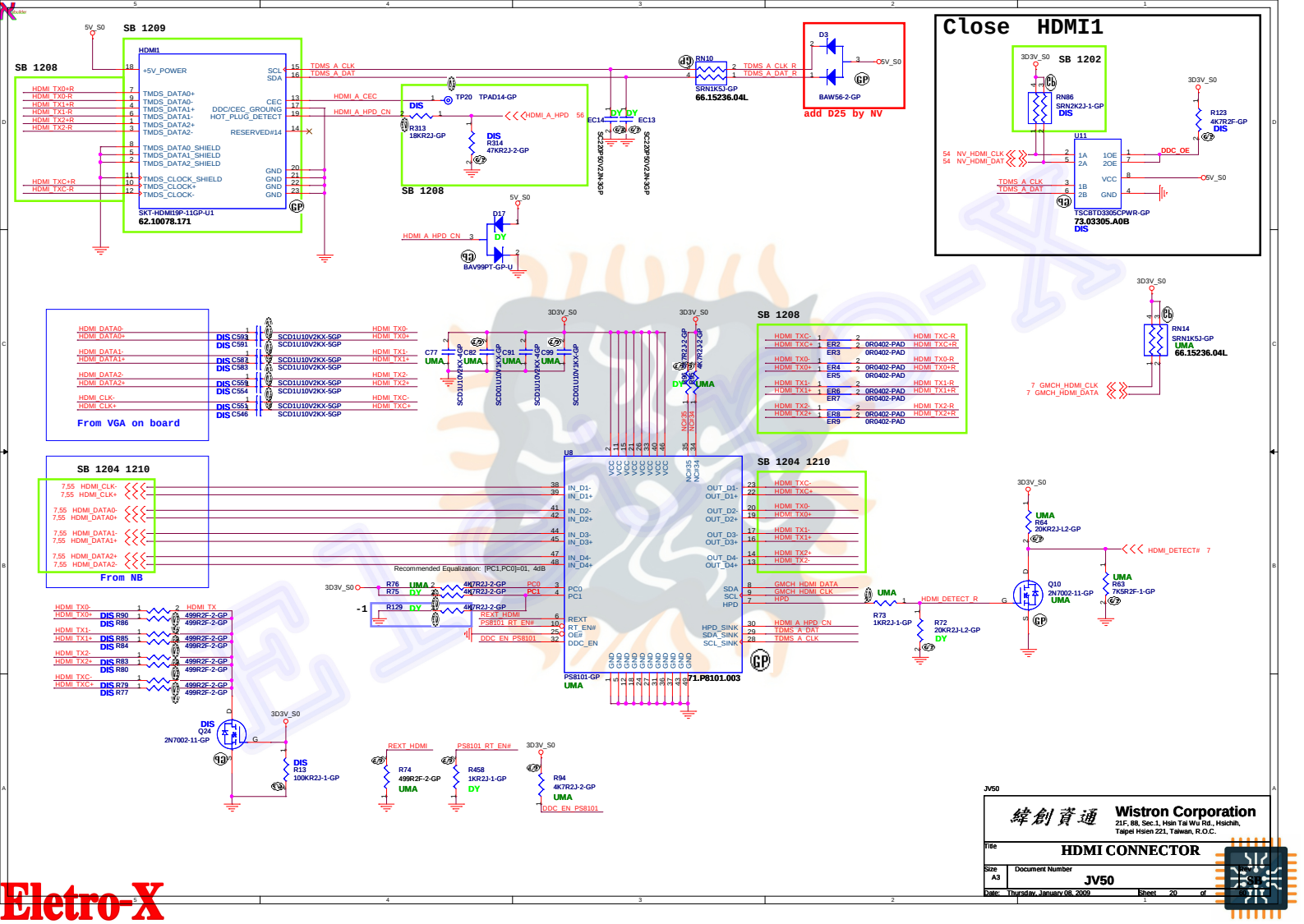
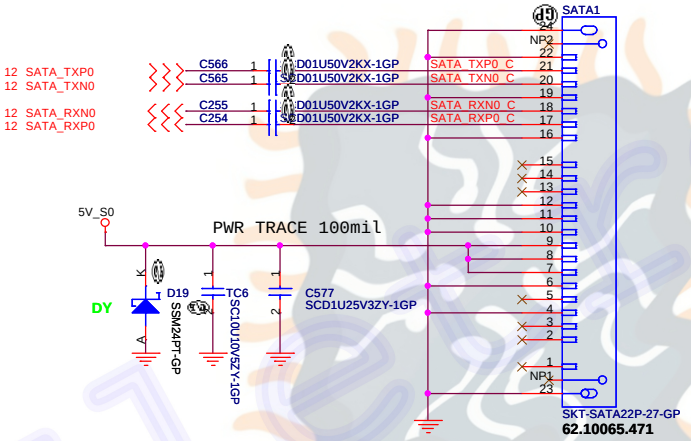


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI CONNECTOR
Size: A3
Document Number: JV50
Date: Thursday, January 08, 2009
Sheet 20 of

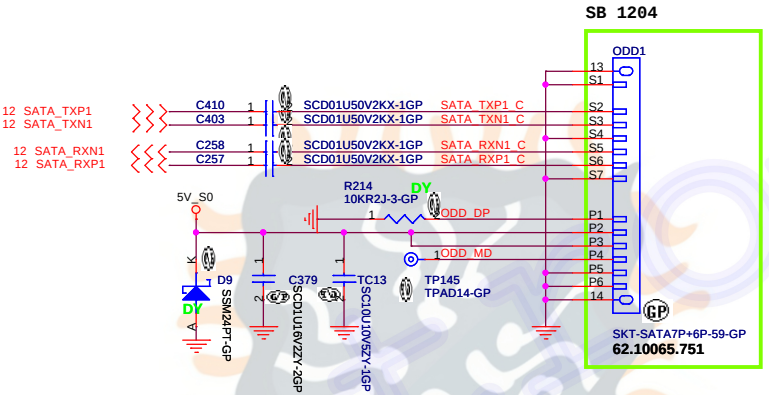
SATA Connector



JV50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**HDD CONN**
Size	Document Number: **JV50**
Date: Thursday, January 08, 2009	Sheet 21 of

ODD Connector



JV50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***ODD***
Size / Document Number	**JV50**
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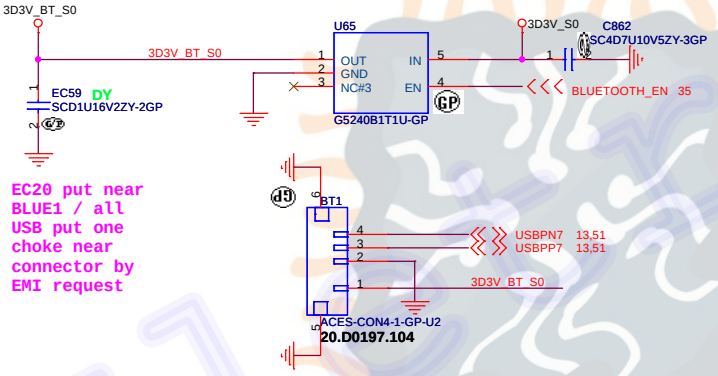
BLUETOOTH MODULE



JV50

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BLUETOOTH**

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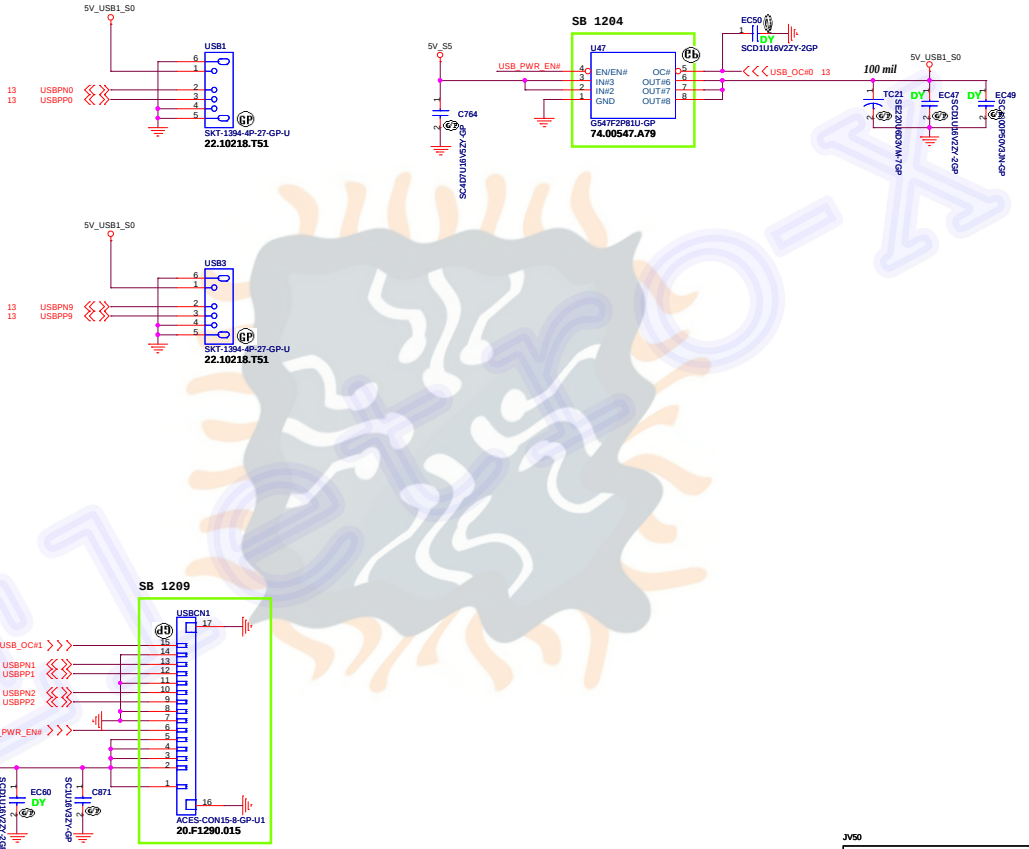
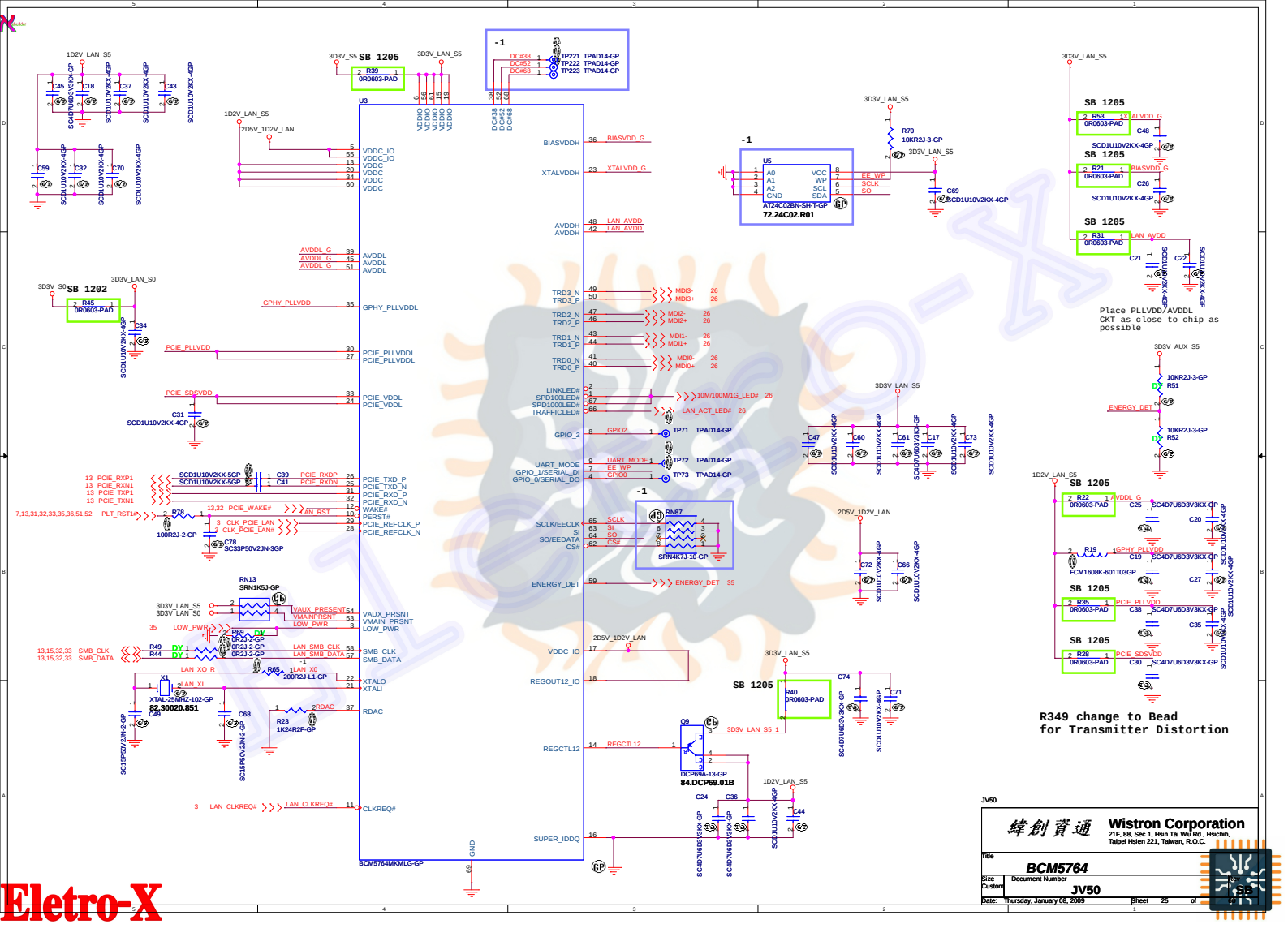


JV50

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	USB CONN	
Size	Document Number	JV50
Date: Thursday, January 08, 2009	Sheet 24 of	

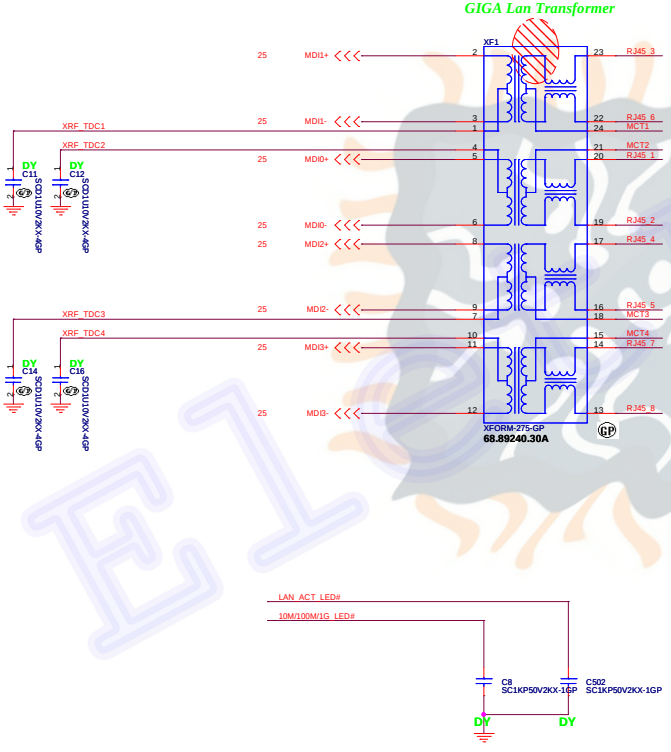

U3
BCM5764MKMLG-GP
SB 1205
SB 1202
Place PLLVDD/AVDDL CKT as close to chip as possible
R349 change to Bead for Transmitter Distortion
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
BCM5764
JV50
Thursday, January 08, 2009
Eletro-X

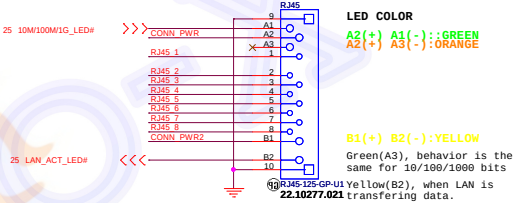
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

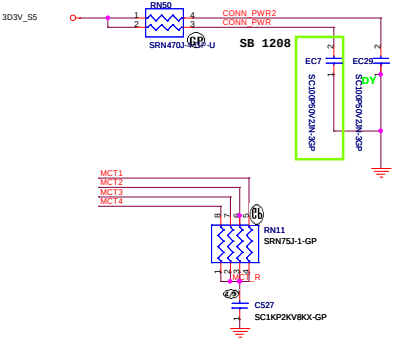
LAN Connector

LAN Connector

GIGA Lan Transformer







JV50

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LAN CONN	
Size A3	Document Number JV50	Rev 1.0
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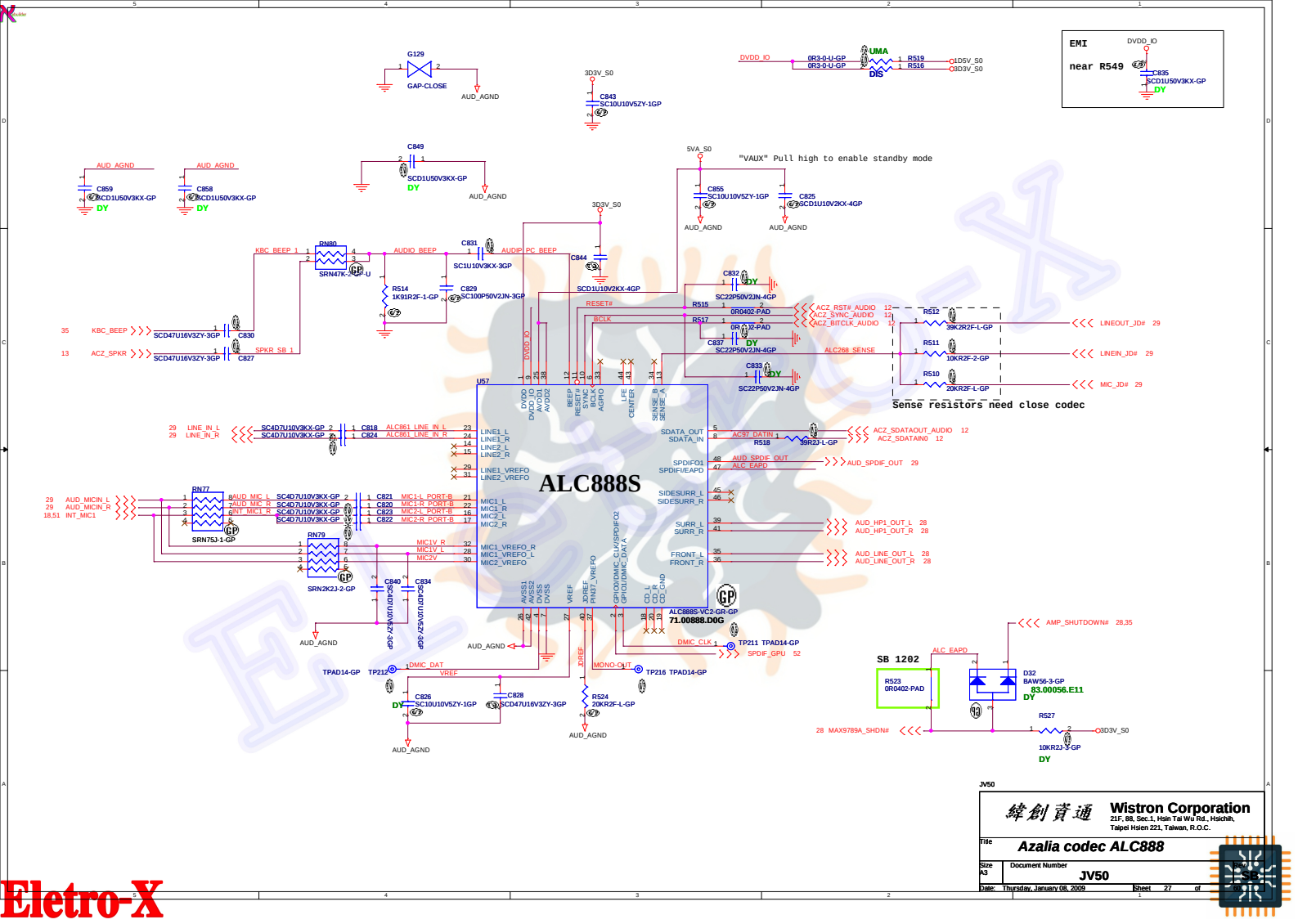
ALC888S
U57
"VAUX" Pull high to enable standby mode
Sense resistors need close codec
EMI
near R549
DVDD_IO
C835
SC1U50V3KX-GP
DY
G129
GAP-CLOSE
AUD_AGND
3D3V_S0
C843
SC10U10V5ZY-1GP
DVDD_IO
0R3-0-U-GP
0R3-0-U-GP
UMA
DIS
R519
R516
1D5V_S0
3D3V_S0
C849
SCD1U50V3KX-GP
C859
C858
SCD1U50V3KX-GP
5VA_S0
C855
SC10U10V5ZY-1GP
C825
SCD1U10V2KX-4GP
KBC_BEEP_1
RN80
SRN47K-2-GP-U
AUDIO_BEEP
AUDIP_PC_BEEP
C831
SC1U10V3KX-3GP
C829
SC100P50V2JN-3GP
R514
1K91R2F-1-GP
C844
SCD1U10V2KX-4GP
C832
SC22P50V2JN-4GP
R515
0R0402-PAD
R517
0R0402-PAD
C837
SC22P50V2JN-4GP
C833
SC22P50V2JN-4GP
RESET#
BCLK
ACZ_RST#_AUDIO
ACZ_SYNC_AUDIO
ACZ_BITCLK_AUDIO
ALC268_SENSE
R512
39K2R2F-L-GP
R511
10KR2F-2-GP
R510
20KR2F-1-GP
LINEOUT_JD#
LINEIN_JD#
MIC_JD#
KBC_BEEP
ACZ_SPKR
C830
SCD47U16V3ZY-3GP
C827
SCD47U16V3ZY-3GP
SPKR_SB_1
LINE_IN_L
LINE_IN_R
SC4D7U10V3KX-GP
C818
C824
ALC861_LINE_IN_L
ALC861_LINE_IN_R
LINE1_L
LINE1_R
LINE2_L
LINE2_R
LINE1_VREFO
LINE2_VREFO
SDATA_OUT
SDATA_IN
AC97_DATIN_1
R518
39R2J-L-GP
ACZ_SDATAOUT_AUDIO
ACZ_SDATAIN0
SPDIFO1
SPDIFI/EAPD
AUD_SPDIF_OUT
ALC_EAPD
SIDESURR_L
SIDESURR_R
SURR_L
SURR_R
AUD_HP1_OUT_L
AUD_HP1_OUT_R
FRONT_L
FRONT_R
AUD_LINE_OUT_L
AUD_LINE_OUT_R
AUD_MICIN_L
AUD_MICIN_R
INT_MIC1
RN77
SRN75J-1-GP
SC4D7U10V3KX-GP
C821
C820
C823
C822
MIC1-L_PORT-B
MIC1-R_PORT-B
MIC2-L_PORT-B
MIC2-R_PORT-B
MIC1_L
MIC1_R
MIC2_L
MIC2_R
RN79
SRN2K2J-2-GP
MIC1V_R
MIC1V_L
MIC2V
MIC1_VREFO_R
MIC1_VREFO_L
MIC2_VREFO
C840
C834
SC4D7U10V3KX-GP
ALC888S-VC2-GR-GP
71.00888.D0G
DMIC_CLK
TP211
TPAD14-GP
SPDIF_GPU
52
DMIC_DAT
TP212
TPAD14-GP
VREF
C826
SC10U10V5ZY-1GP
C828
SCD47U16V3ZY-3GP
JDREF
R524
20KR2F-L-GP
MONO_OUT
TP216
TPAD14-GP
SB 1202
ALC_EAPD
R523
0R0402-PAD
D32
BAW56-3-GP
83.00056.E11
AMP_SHUTDOWN#
28,35
28
MAX9789A_SHDN#
R527
10KR2J-3-GP
JV50
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Azalia codec ALC888
Size
A3
Document Number
JV50
Rev
SB
Date: Thursday, January 08, 2009
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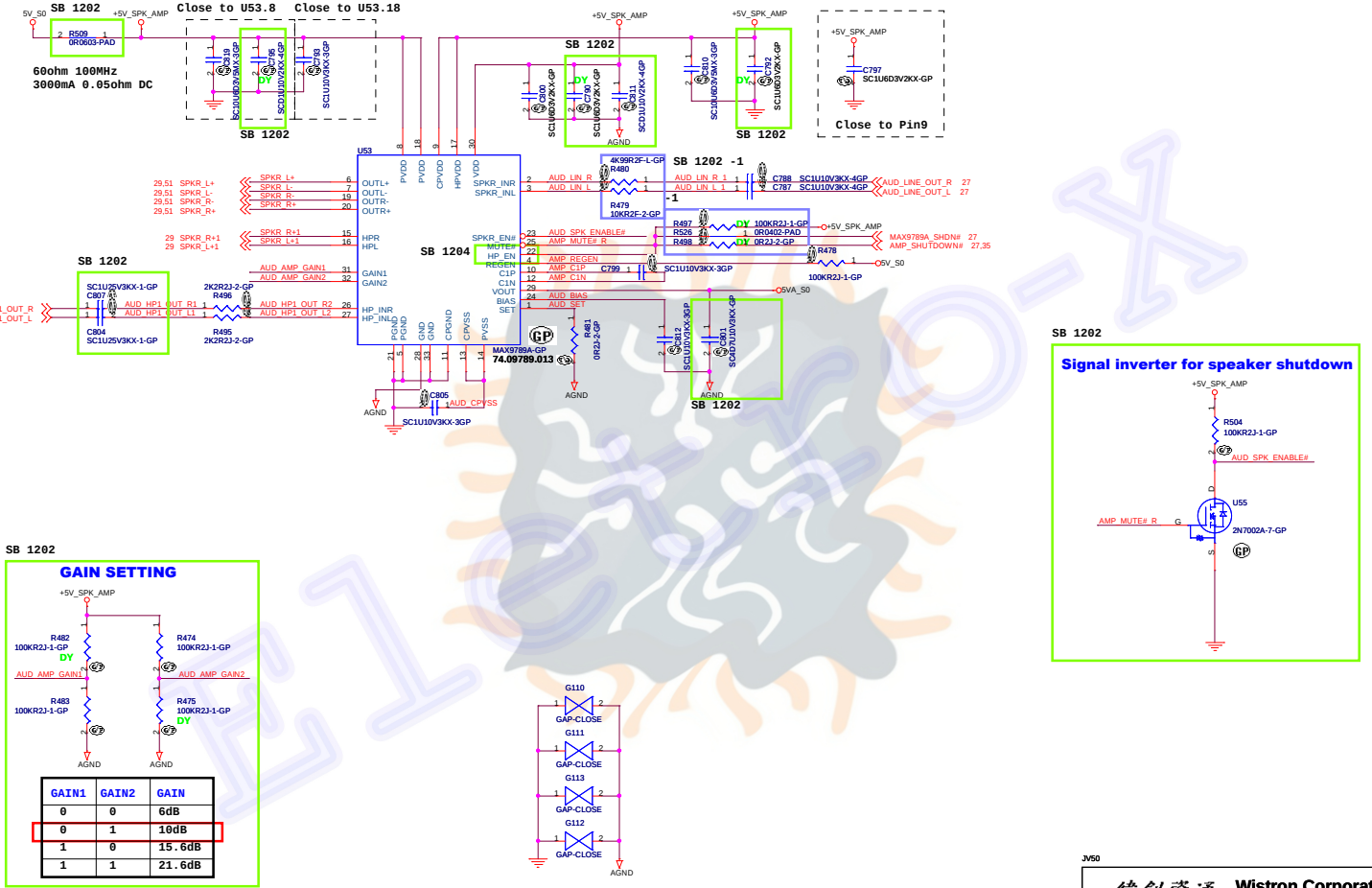

GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

JV50

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO AMP

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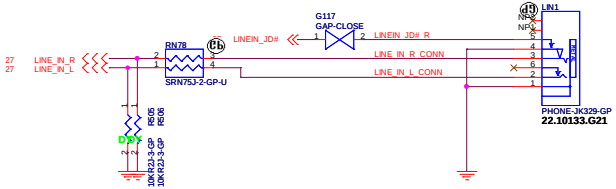
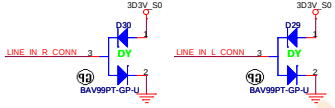
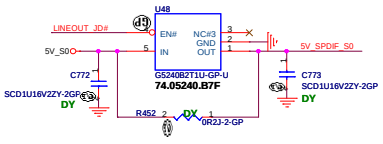
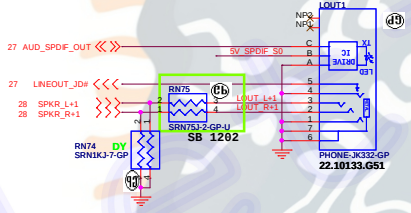
LINE IN



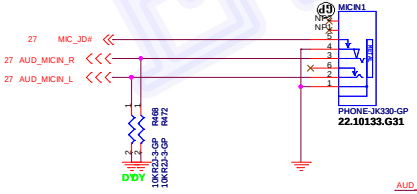


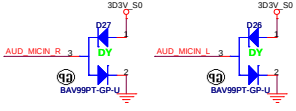
LINE OUT



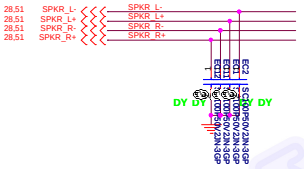


MIC IN

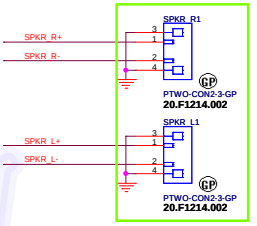




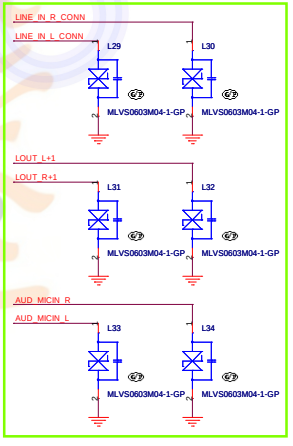
Internal Speaker



SB 1202



SB 1202



JV50

緯創資通	Wistron Corporation 21F., 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	AUDIO jack	
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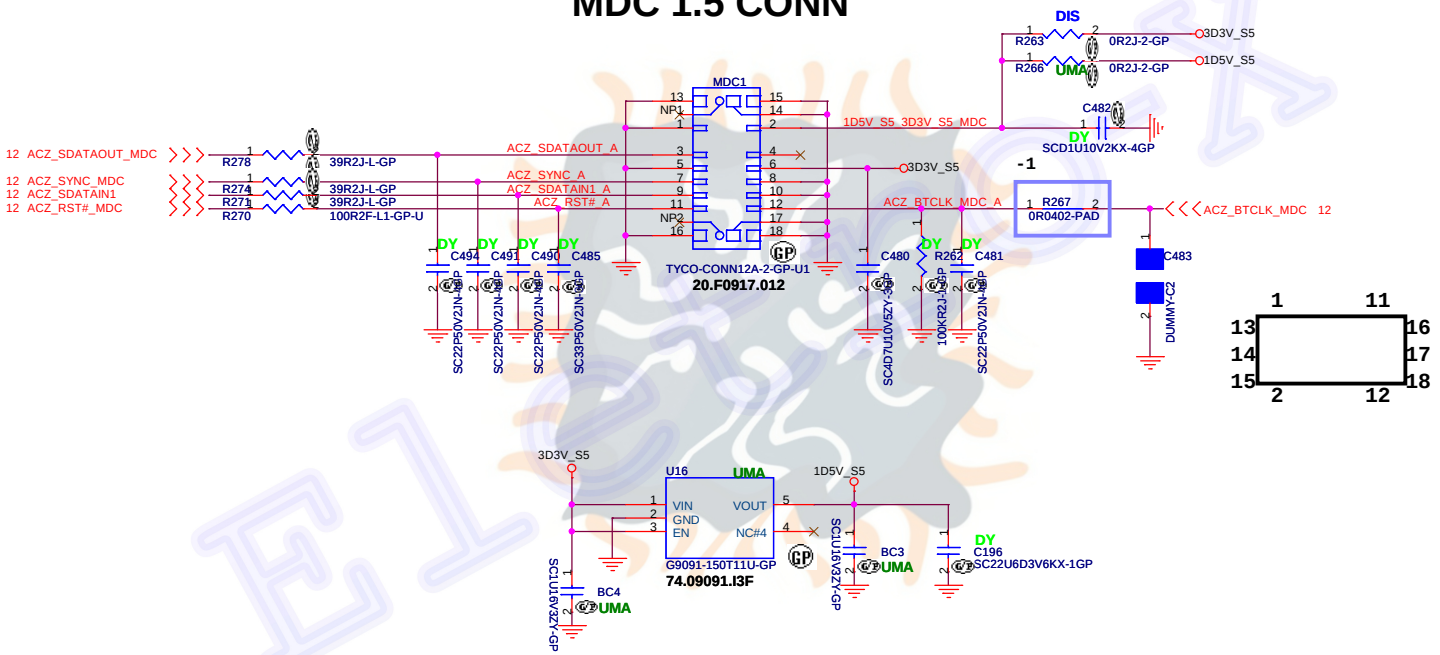
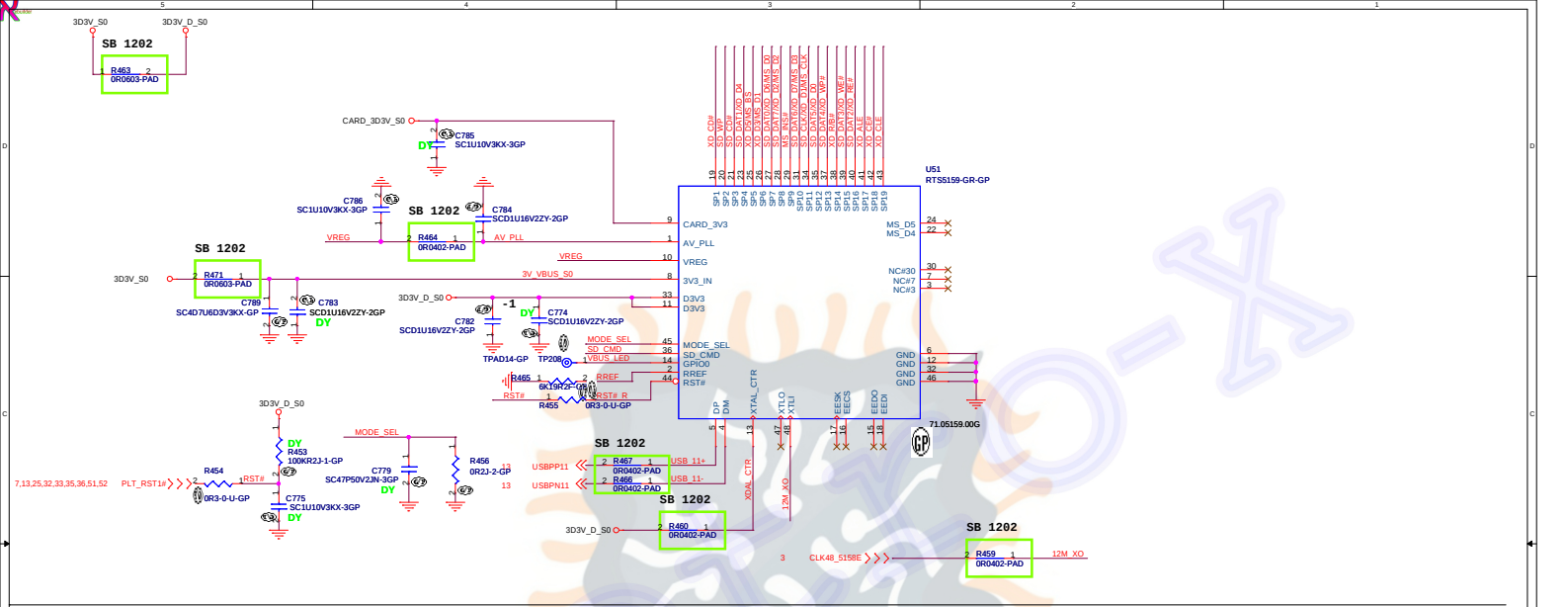
MDC 1.5 CONN

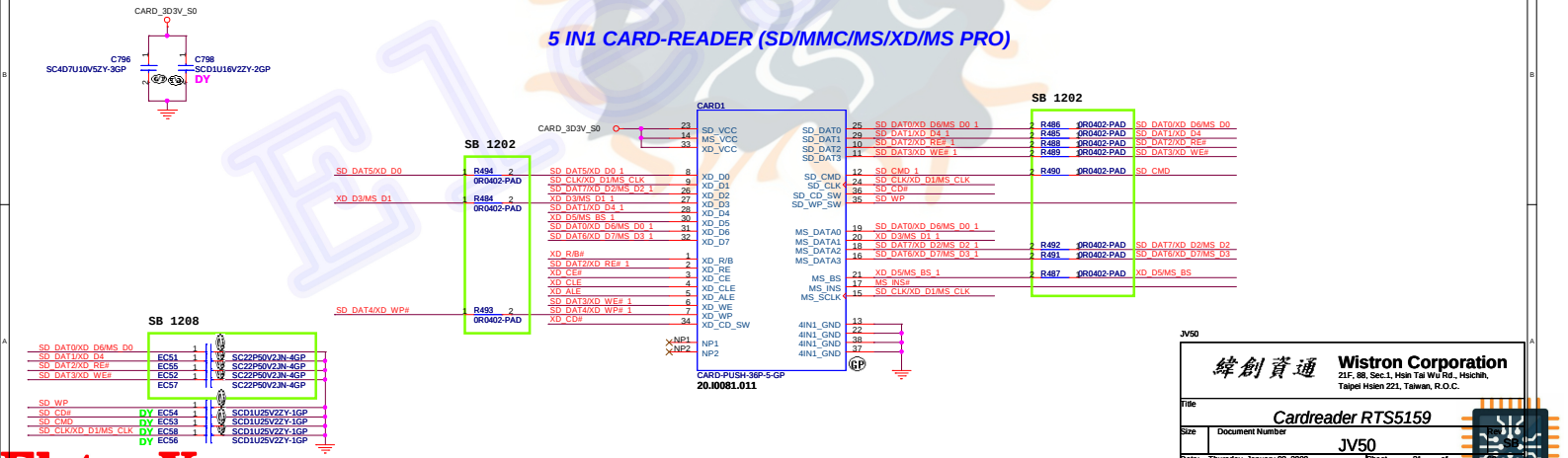


JV50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***MDC***
Size	Document Number: **JV50**
Date: Thursday, January 08, 2009	Sheet 30 of



5 IN1 CARD-READER (SD/MMC/MS/XD/MS PRO)



JV50

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Cardreader RTS5159	
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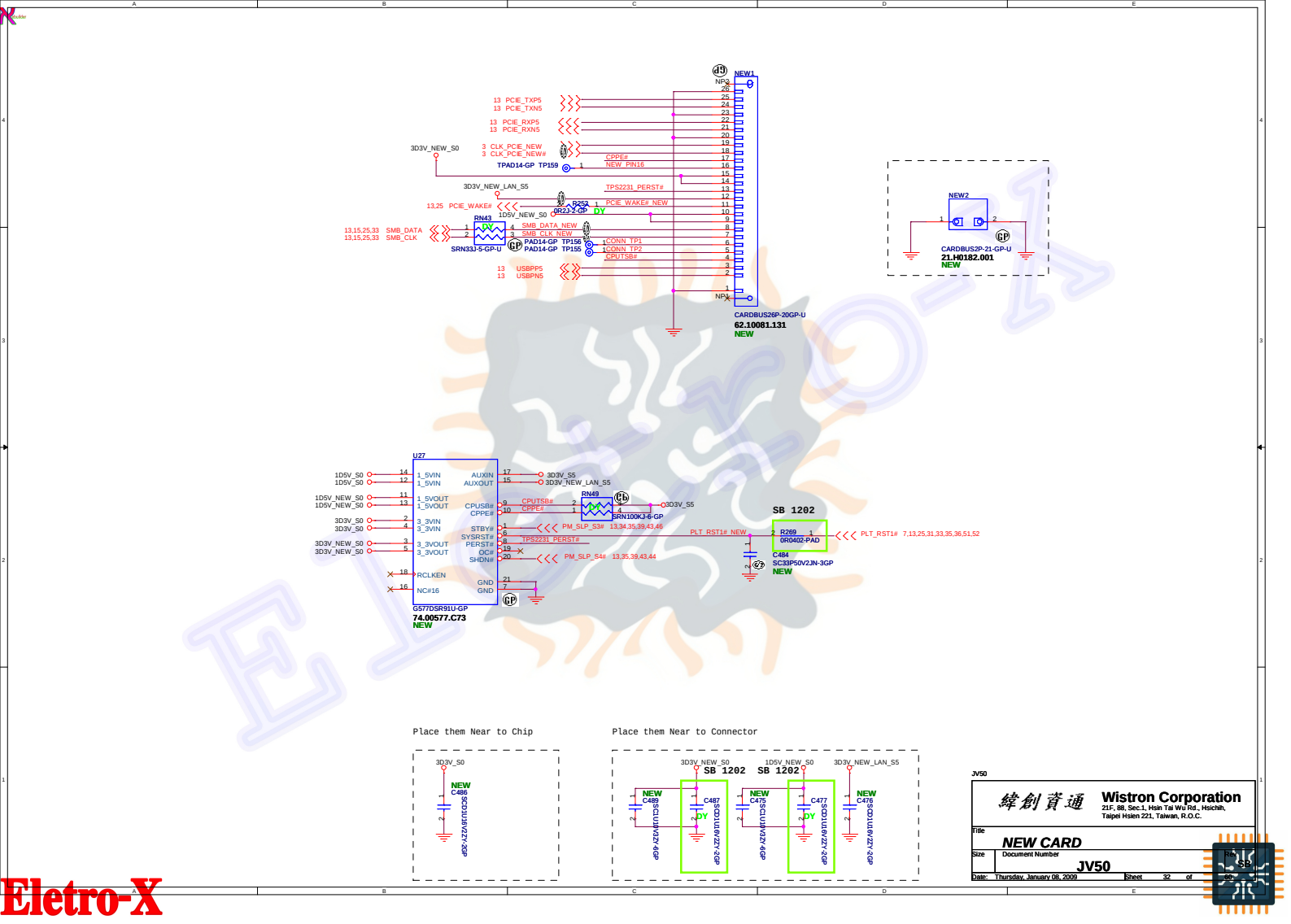
NEW1
CARDBUS26P-20GP-U
62.10081.131
NEW
NEW2
CARDBUS2P-21-GP-U
21.H0182.001
NEW
U27
G577DSR91U-GP
74.00577.C73
NEW
RN49
SRN100KJ-6-GP
SB 1202
R269
0R0402-PAD
C484
SC33P50V2JN-3GP
NEW
RN43
SRN33J-5-GP-U
DY
R252
0R2J-2-GP
TPAD14-GP TP159
PAD14-GP TP156
PAD14-GP TP155
Place them Near to Chip
Place them Near to Connector
C486
SC01U16V2ZY-2GP
C489
C487
C475
C477
C476
SC01U16V2ZY-6GP
SC01U16V2ZY-4GP
JV50
緯創資通
Wistron Corporation
21F., 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
NEW CARD
Size
Document Number
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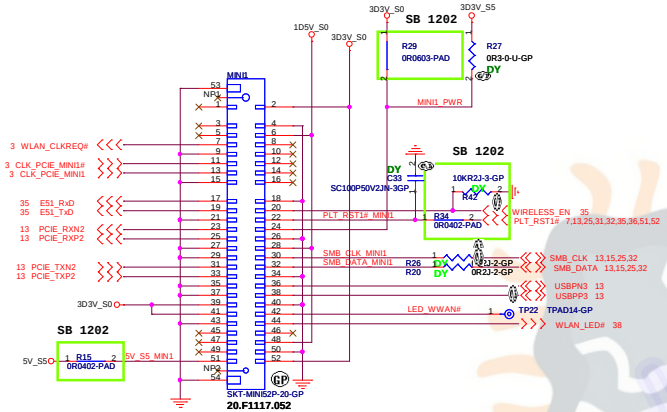
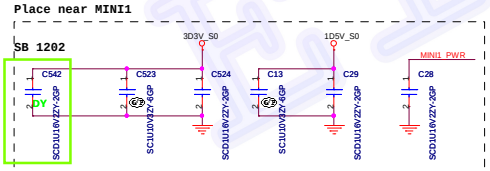
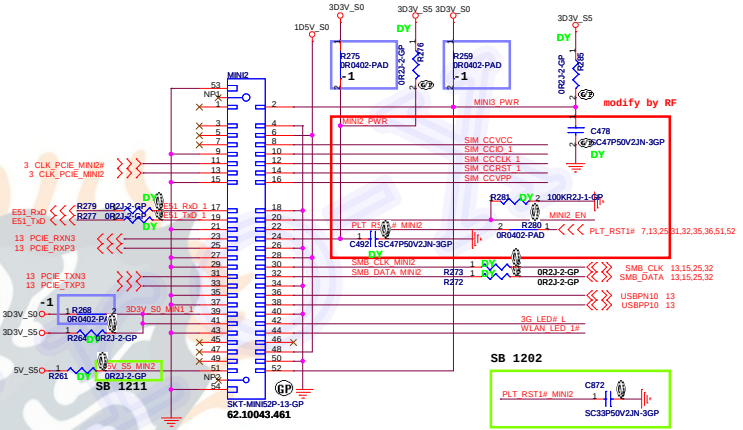
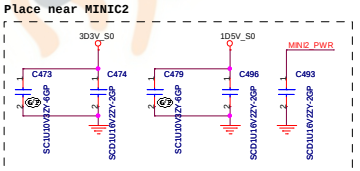
Mini Card Connector(WLAN)
Support debug-card





Mini Card Connector(Robson2 and 3G)





JV50	緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	MINI CARD		
Size A3	Document Number JV50		Rev SB
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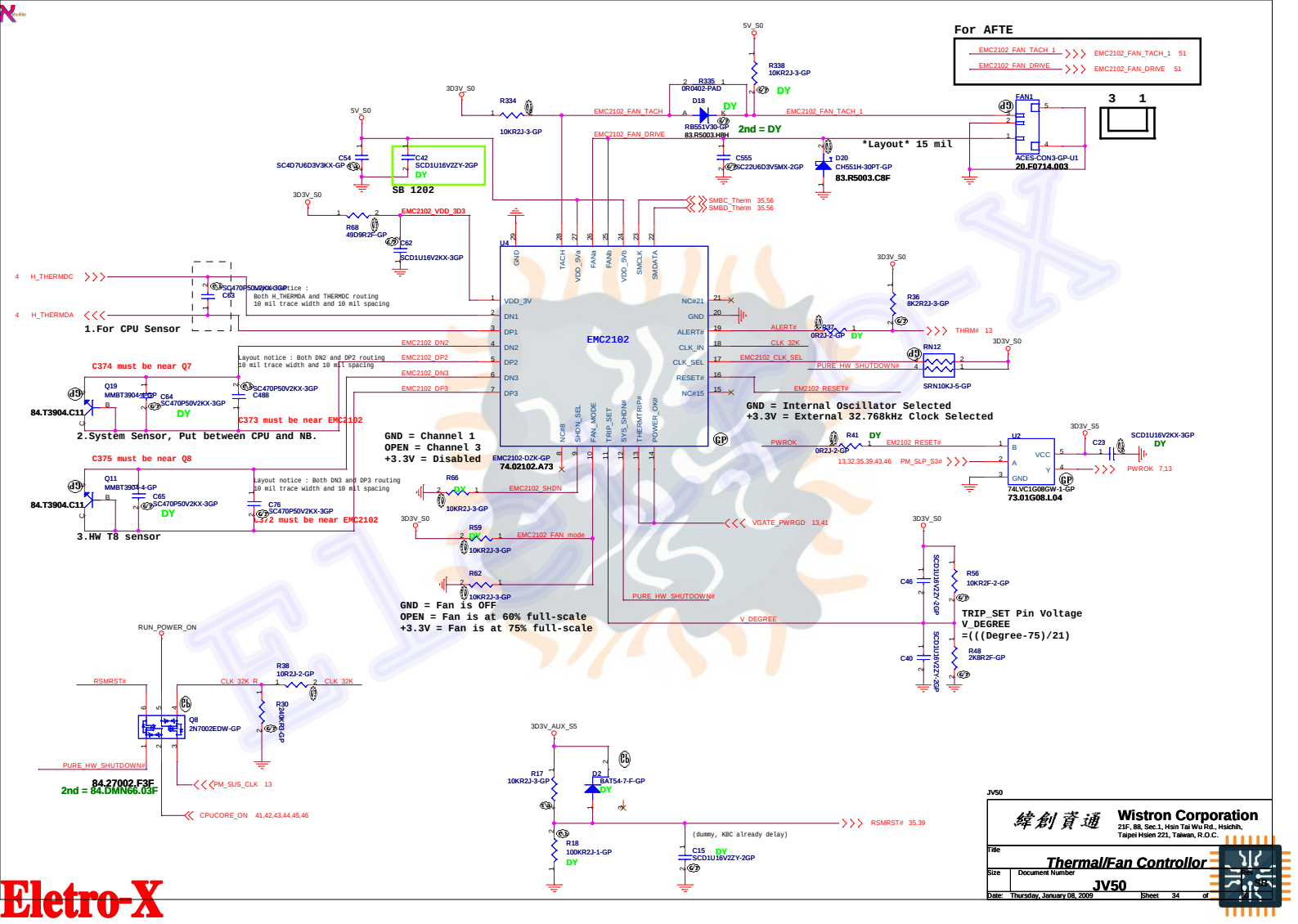
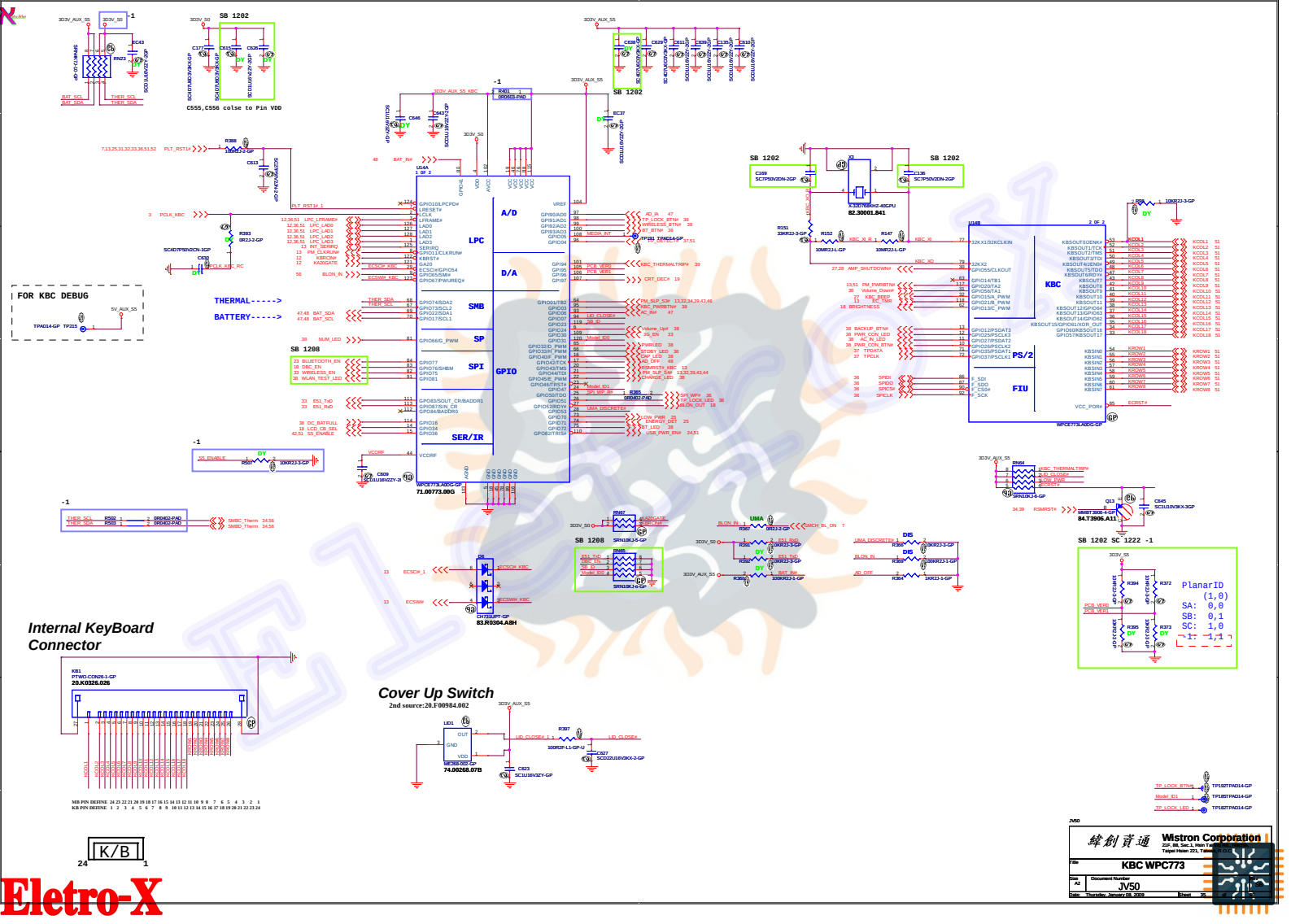
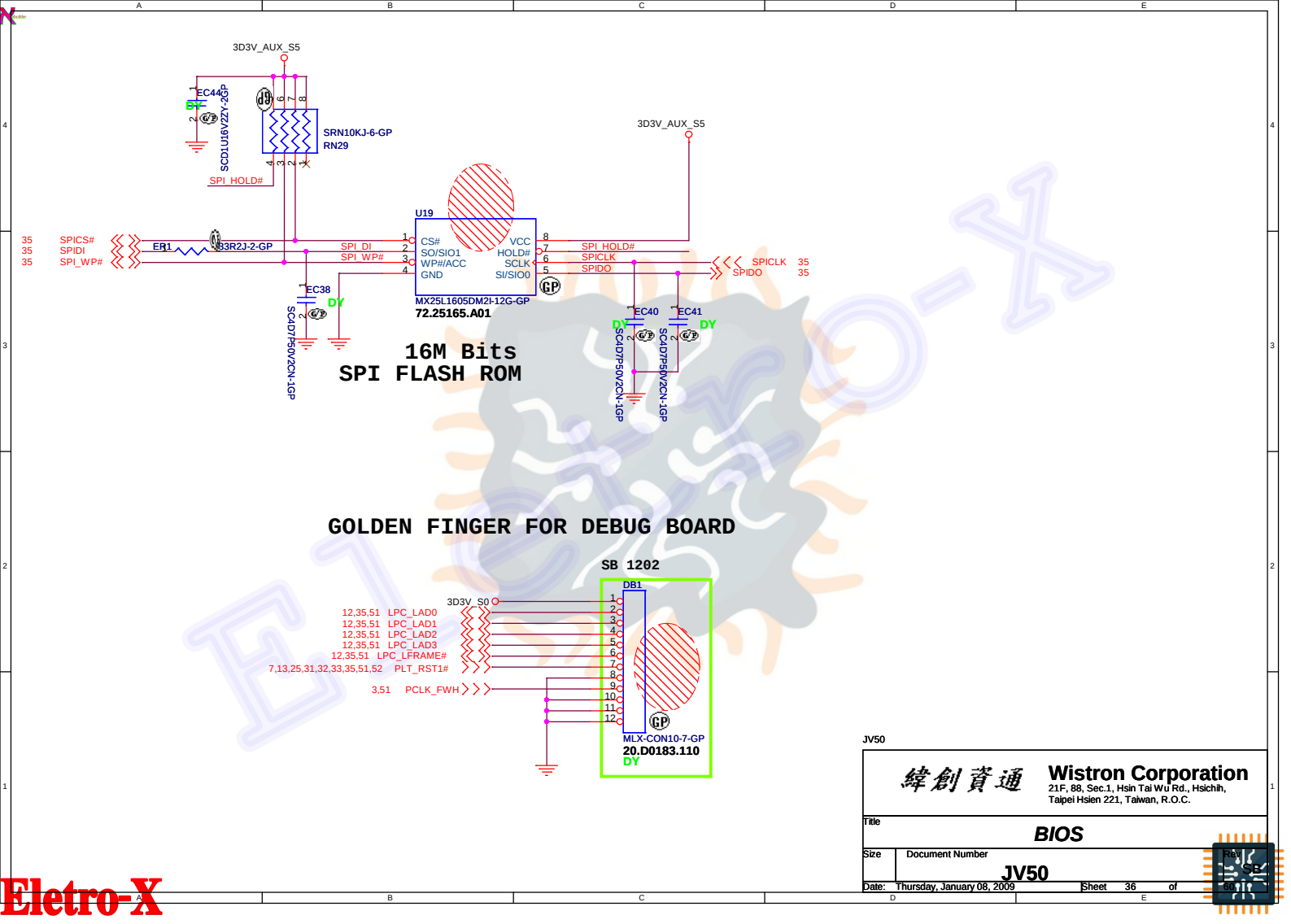

For AFTE
EMC2102_FAN_TACH_1
EMC2102_FAN_DRIVE
EMC2102_FAN_TACH_1 51
EMC2102_FAN_DRIVE 51
5V_S0
3D3V_S0
R338 10KR2J-3-GP
DY
R335 0R0402-PAD
D18 RB551V30-GP 83.R5003.H8H
2nd = DY
R334 10KR2J-3-GP
EMC2102_FAN_TACH
EMC2102_FAN_DRIVE
EMC2102_FAN_TACH_1
Layout 15 mil
C555 SC22U6D3V5MX-2GP
D20 CH551H-30PT-GP 83.R5003.C8F
FAN1 ACES-CON3-GP-U1 20.F0714.003
3 1
C54 SC4D7U6D3V3KX-GP
C42 SCD1U16V2ZY-2GP DY
SB 1202
R68 49D9R2F-GP
EMC2102_VDD_3D3
C62 SCD1U16V2KX-3GP
SMBC_Therm 35,56
SMBD_Therm 35,56
U4
EMC2102
GND
TACH
VDD_3V
FANa
FANb
VDD_3V
SMCLK
SMDATA
VDD_3V
DN1
DP1
DN2
DP2
DN3
DP3
NC#21
GND
ALERT#
CLK_IN
CLK_SEL
RESET#
NC#15
N_C#8
SHDN_SEL
FAN_MODE
TRIP_SET
SYS_SHDN#
THERMTRIP#
POWER_OK#
EMC2102-DZK-GP 74.02102.A73
4 H_THERMDC
4 H_THERMDA
C63 SC470P50V2KX-3GP
Notice : Both H_THERMDA and THERMDC routing 10 mil trace width and 10 mil spacing
1.For CPU Sensor
EMC2102_DN2
EMC2102_DP2
EMC2102_DN3
EMC2102_DP3
Layout notice : Both DN2 and DP2 routing 10 mil trace width and 10 mil spacing
C374 must be near Q7
Q19 MMBT3904-3-GP 84.T3904.C11
C64 SC470P50V2KX-3GP
C488 SC470P50V2KX-3GP
DY
C373 must be near EMC2102
2.System Sensor, Put between CPU and NB.
C375 must be near Q8
Q11 MMBT3904-4-GP 84.T3904.C11
C65 SC470P50V2KX-3GP
C76 SC470P50V2KX-3GP
DY
C372 must be near EMC2102
3.HW T8 sensor
GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled
R66 10KR2J-3-GP
EMC2102_SHDN
R59 10KR2J-3-GP
EMC2102_FAN_mode
R62 10KR2J-3-GP
GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale
R36 8K2R2J-3-GP
THRM# 13
R37 0R2J-2-GP DY
ALERT#
CLK_32K
EMC2102_CLK_SEL
PURE_HW_SHUTDOWN#
EM2102_RESET#
RN12 SRN10KJ-5-GP
GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected
PWROK
R41 0R2J-2-GP DY
EM2102_RESET#
13,32,35,39,43,46 PM_SLP_S3#
U2 74LVC1G08GW-1-GP 73.01G08.L04
3D3V_S5
C23
SCD1U16V2KX-3GP DY
PWROK 7,13
VGATE_PWRGD 13,41
PURE_HW_SHUTDOWN#
V_DEGREE
C46 SCD1U16V2ZY-2GP
R56 10KR2F-2-GP
C40 SCD1U16V2ZY-2GP
R48 2K8R2F-GP
TRIP_SET Pin Voltage
V_DEGREE
=(((Degree-75)/21)
RUN_POWER_ON
RSMRST#
R38 10R2J-2-GP
CLK_32K_R
CLK_32K
R30 20KR2J-3-GP
Q8 2N7002EDW-GP
PURE_HW_SHUTDOWN#
84.27002.F3F
2nd = 84.DMN66.03F
PM_SUS_CLK 13
CPUCORE_ON 41,42,43,44,45,46
3D3V_AUX_S5
R17 10KR2J-3-GP
D2 BAT54-7-F-GP DY
R18 100KR2J-1-GP DY
C15 SCD1U16V2ZY-2GP DY
(dummy, KBC already delay)
RSMRST# 35,39
JV50
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Thermal/Fan Controllor
Size
Document Number
JV50
Date: Thursday, January 08, 2009
Sheet 34 of


SB 1202
C555, C556 colse to Pin VDD
SB 1202
SB 1202
SB 1202
FOR KBC DEBUG
THERMAL ----->
BATTERY ----->
SB 1208
SB 1208
SB 1202 SC 1222 -1
LPC
A/D
D/A
SMB
SP
SPI
GPIO
SER/IR
KBC
PS/2
FIU
Internal KeyBoard Connector
Cover Up Switch
2nd source:20.F00984.002
PlanarID (1,0)
SA: 0,0
SB: 0,1
SC: 1,0
Wistron Corporation
KBC WPC773
JV50
Eletro-X



JV50

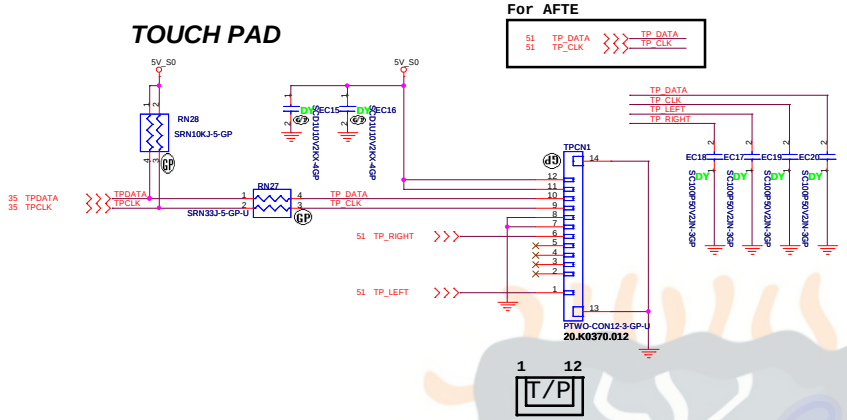
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BIOS**

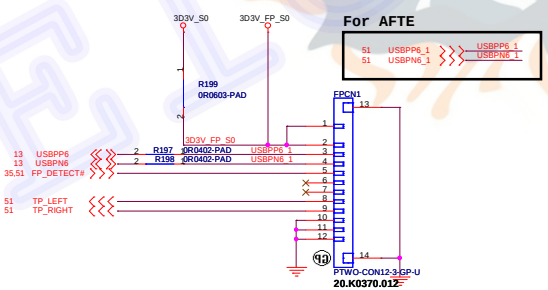
Size	Document Number	Rev
	JV50	SB

Date: Thursday, January 08, 2009 Sheet 36 of 60

TOUCH PAD



Finger printer



JV50

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

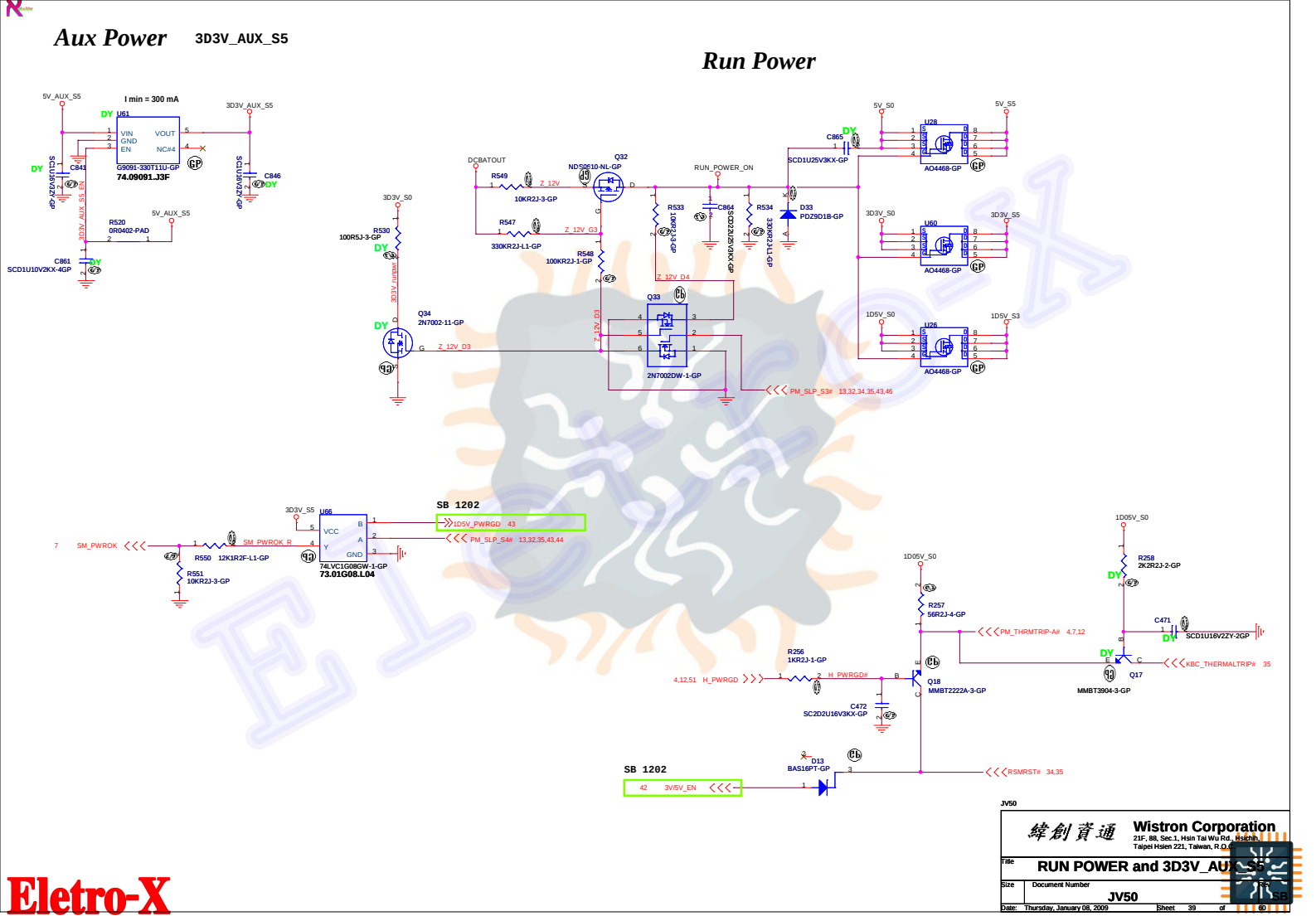
Title: Touch PAD and FP

Size	Document Number	Rev
	JV50	1.0

Date: Thursday, January 08, 2009 Sheet 37 of

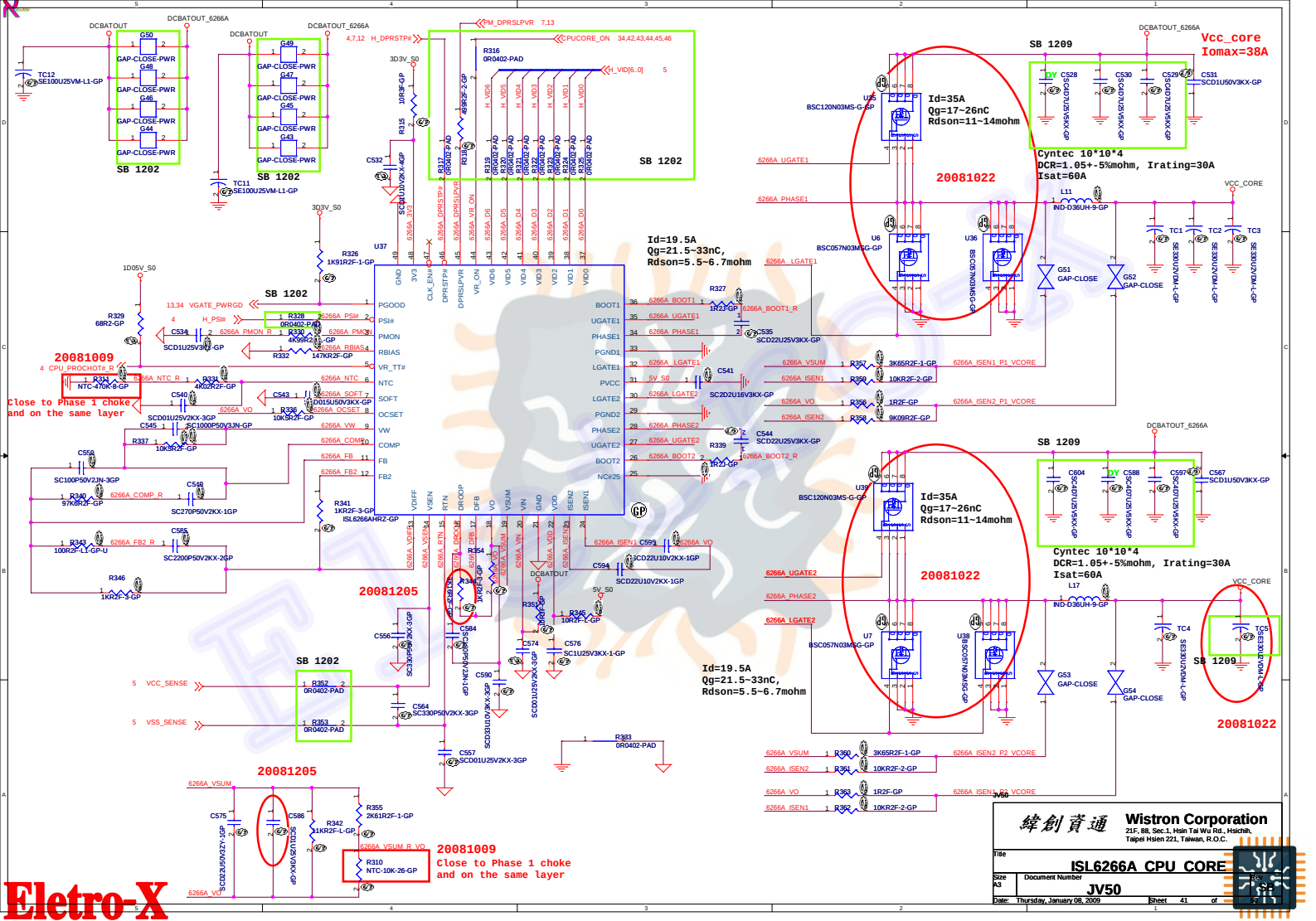
Aux Power 3D3V_AUX_S5

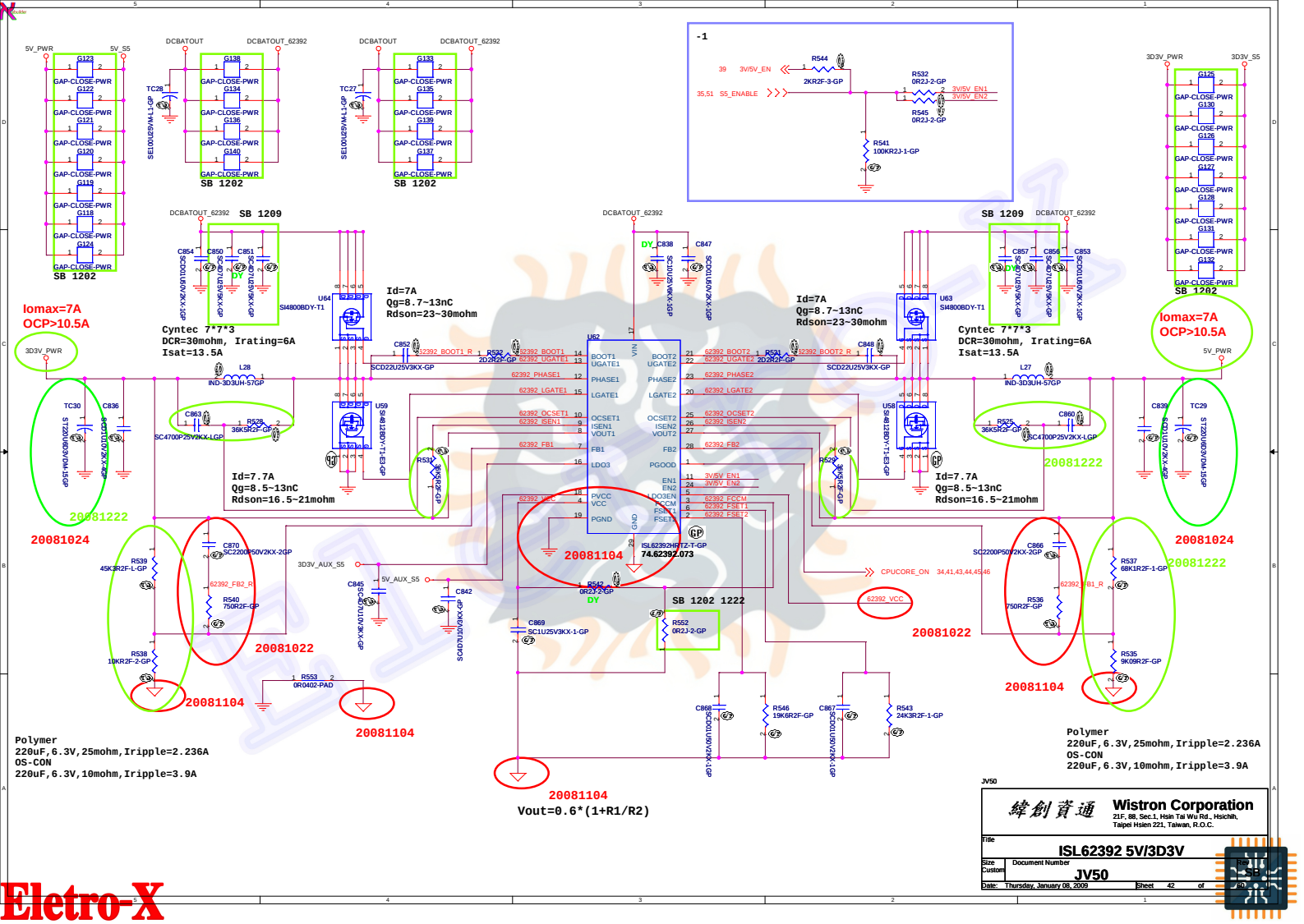
Run Power

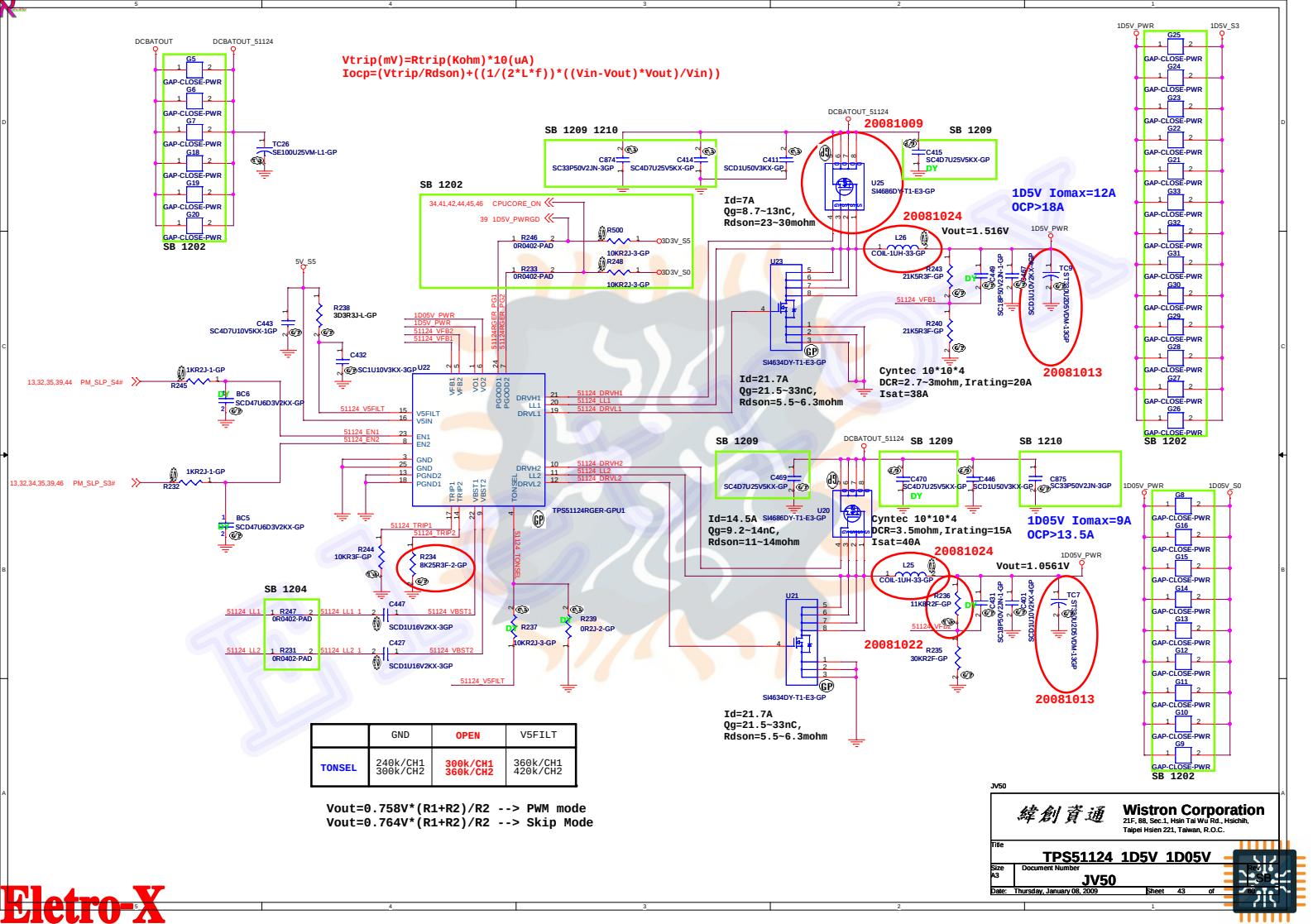


JV50

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	RUN POWER and 3D3V_AUX_S5	
Size	Document Number	Rev
	JV50	SB
Date: Thursday, January 08, 2009	Sheet 39 of 60	


Vcc_core
Iomax=38A
SB 1209
SB 1202
Id=35A
Qg=17~26nC
Rdson=11~14mohm
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=30A
Isat=60A
20081022
Id=19.5A
Qg=21.5~33nC,
Rdson=5.5~6.7mohm
20081009
Close to Phase 1 choke
and on the same layer
20081205
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ISL6266A CPU CORE
JV50
Thursday, January 08, 2009
41
Eletro-X


-1
R544
2KR2F-3-GP
R532
0R2J-2-GP
R545
0R2J-2-GP
R541
100KR2J-1-GP
39 3V/5V_EN
35,51 S5_ENABLE
3V/5V_EN1
3V/5V_EN2
5V_PWR
5V_S5
3D3V_PWR
3D3V_S5
DCBATOUT
DCBATOUT_62392
SB 1202
SB 1209
GAP-CLOSE-PWR
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
Iomax=7A
OCP>10.5A
Id=7A
Qg=8.5~13nC
Rdson=16.5~21mohm
20081222
20081024
20081104
20081022
U62
ISL62392HRTZ-T-GP
74.62392.073
VIN
BOOT1
UGATE1
PHASE1
LGATE1
OCSET1
ISEN1
VOUT1
FB1
LDO3
PVCC
VCC
PGND
BOOT2
UGATE2
PHASE2
LGATE2
OCSET2
ISEN2
VOUT2
FB2
PGOOD
EN1
EN2
DO3EN
FCCM
FSET1
FSET2
GND
62392_VCC
CPUCORE_ON 34,41,43,44,45,46
3D3V_AUX_S5
5V_AUX_S5
SB 1202 1222
R542
0R2J-2-GP
DY
R552
0R2J-2-GP
Polymer
220uF,6.3V,25mohm,Iripple=2.236A
OS-CON
220uF,6.3V,10mohm,Iripple=3.9A
Vout=0.6*(1+R1/R2)
Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL62392 5V/3D3V
Size
Custom
Document Number
JV50
Rev
Date: Thursday, January 08, 2009
Sheet 42 of 50



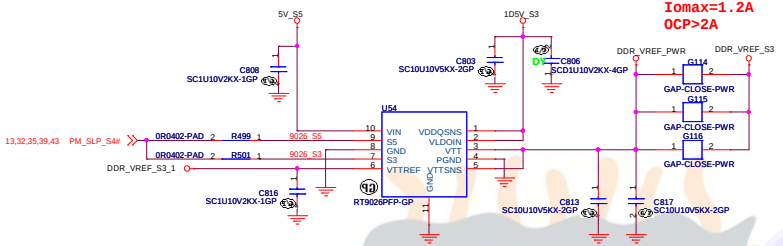
	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

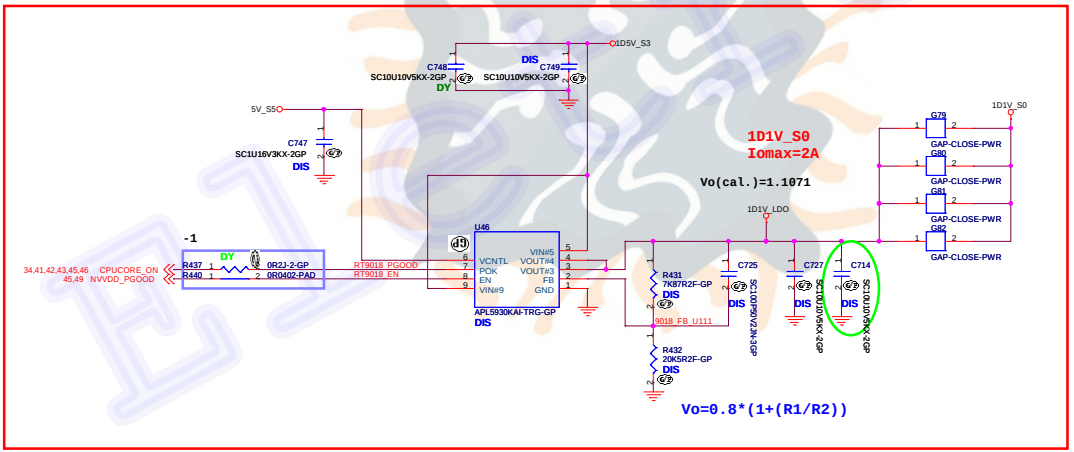
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124 1D5V 1D05V

Size: A3 | Document Number: JV50 | Rev: 0.5

Date: Thursday, January 08, 2009 | Sheet 43 of

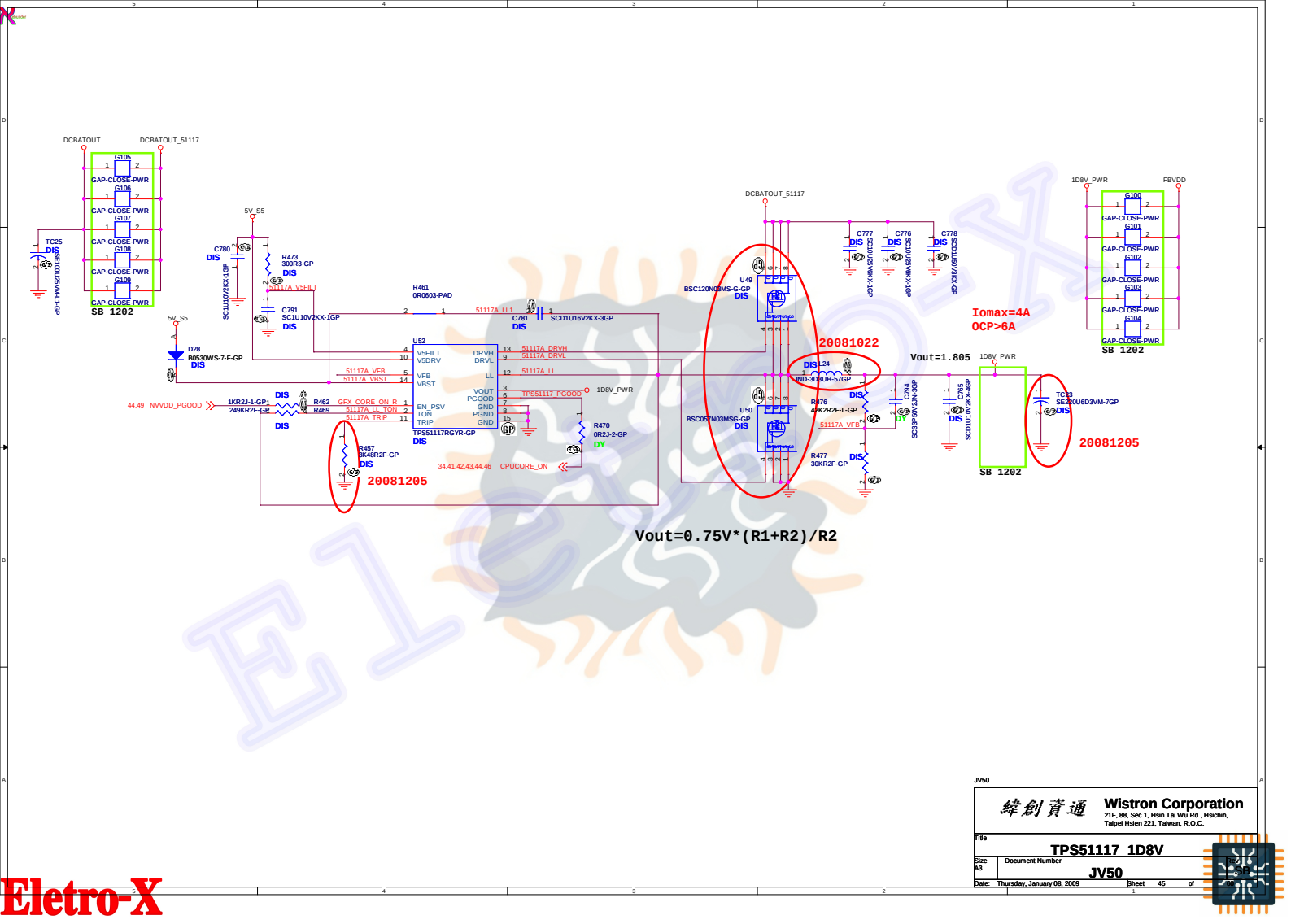




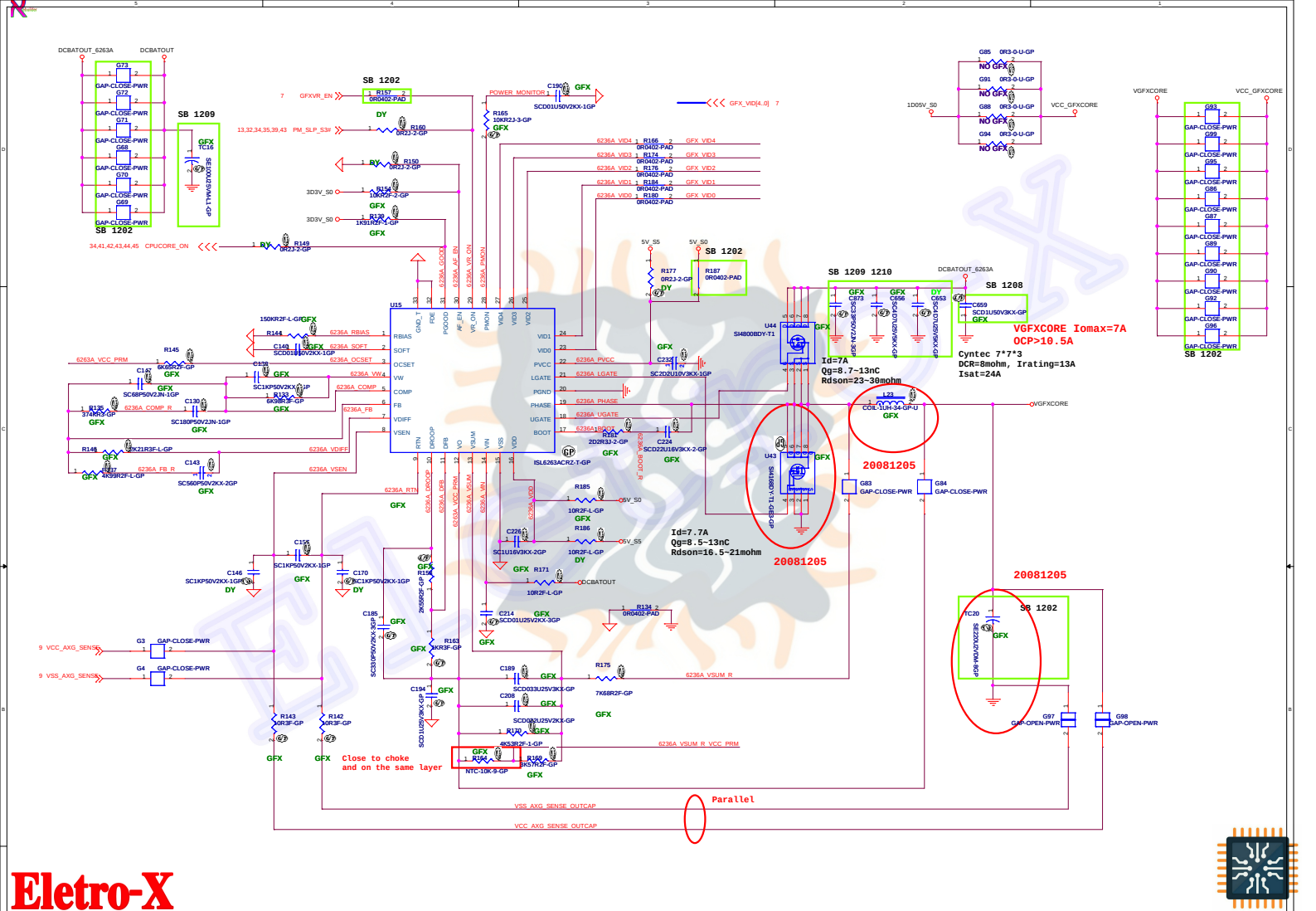
20090106

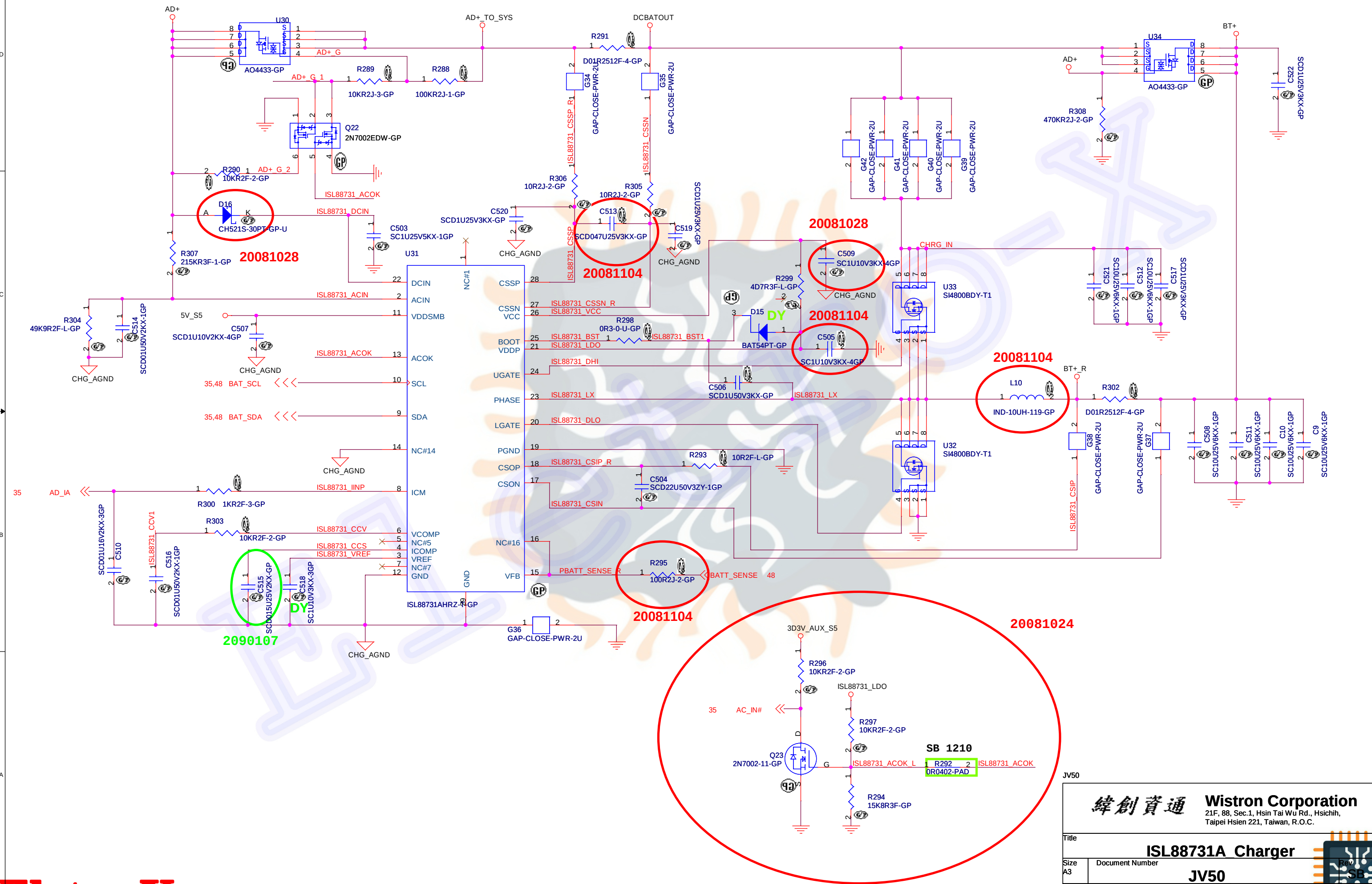
JV50

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	0D75V/1D1V	
Size A3	Document Number JV50	Rev SB
Date: Thursday, January 08, 2009	Sheet 44 of	



JV50	
緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	TPS51117 1D8V
Size A3	Document Number JV50
Date: Thursday, January 08, 2009	Sheet 45 of


VGFXCORE Iomax=7A
OCP>10.5A
Cyntec 7*7*3
DCR=8mohm, Irating=13A
Isat=24A
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
20081205
20081205
20081205
Close to choke
and on the same layer
Parallel
SB 1202
SB 1209
SB 1209 1210
SB 1208
DCBATOUT_6263A
DCBATOUT
VCC_GFXCORE
VGFXCORE
1D05V_S0
5V_S0
5V_S5
3D3V_S0
GFXVR_EN
POWER_MONITOR
PM_SLP_S3#
CPUCORE_ON
GFX_VID[4..0]
6236A_VID4
6236A_VID3
6236A_VID2
6236A_VID1
6236A_VID0
6263A_VCC_PRM
6236A_VSUM_R_VCC_PRM
VSS_AXG_SENSE_OUTCAP
VCC_AXG_SENSE_OUTCAP
VCC_AXG_SENSE
VSS_AXG_SENSE
U15
ISL6263ACRZ-T-GP
U44
SI4800BDY-T1
U43
SI4888DY-T1-GE3-GP
L23
COIL-1UH-34-GP-U
Eletro-X

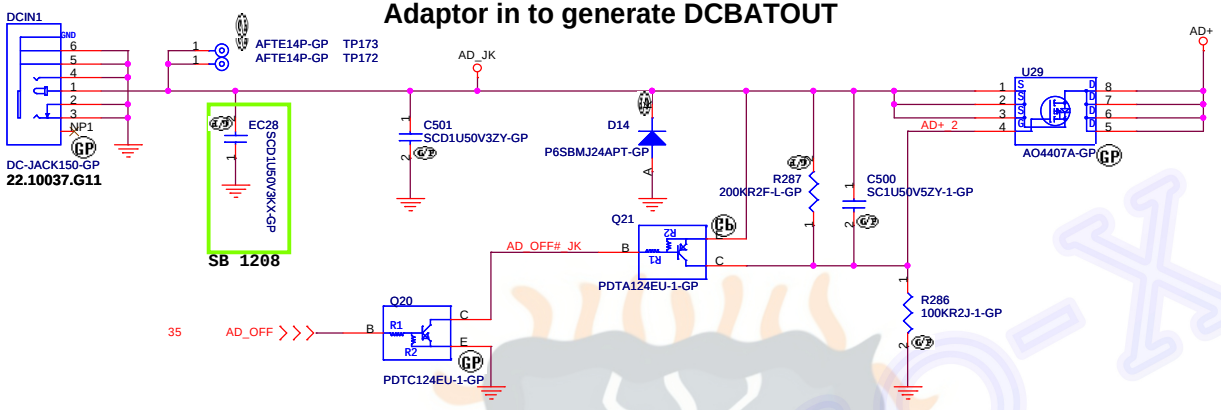

AD+
U30
AO4433-GP
AD+_G
AD+_TO_SYS
DCBATOUT
R291
D01R2512F-4-GP
R289
10KR2J-3-GP
R288
100KR2J-1-GP
AD+_G_1
Q22
2N7002EDW-GP
G34
GAP-CLOSE-PWR-2U
G35
GAP-CLOSE-PWR-2U
ISL88731_CSSP_R
ISL88731_CSSN
R290
10KR2F-2-GP
AD+_G_2
ISL88731_ACOK
D16
CH521S-30PT-GP-U
ISL88731_DCIN
20081028
R307
215KR3F-1-GP
C503
SC1U25V5KX-1GP
R306
10R2J-2-GP
R305
10R2J-2-GP
C520
SCD1U25V3KX-GP
C513
SCD047U25V3KX-GP
C519
SCD1U25V3KX-GP
CHG_AGND
20081104
U31
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
ICM
VCOMP
NC#5
ICOMP
VREF
NC#7
GND
NC#1
CSSP
CSSN
VCC
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
ISL88731AHRZ-T-GP
ISL88731_ACIN
R304
49K9R2F-L-GP
C514
SCD01U50V2KX-1GP
5V_S5
C507
SCD1U10V2KX-4GP
35,48 BAT_SCL
35,48 BAT_SDA
ISL88731_CSSN_R
ISL88731_VCC
R298
0R3-0-U-GP
ISL88731_BST
ISL88731_BST1
ISL88731_LDO
ISL88731_DHI
ISL88731_LX
ISL88731_DLO
D15
BAT54PT-GP
DY
R299
4D7R3F-L-GP
C509
SC1U10V3KX-4GP
C505
SC1U10V3KX-4GP
C506
SCD1U50V3KX-GP
CHRG_IN
U33
SI4800BDY-T1
U32
SI4800BDY-T1
G42 G41 G40 G39
GAP-CLOSE-PWR-2U
BT+
U34
AO4433-GP
R308
470KR2J-2-GP
C522
SC1U25V3KX-GP
C521 C512 C517
SC10U25V6KX-1GP
L10
IND-10UH-119-GP
BT+_R
R302
D01R2512F-4-GP
G38
G37
GAP-CLOSE-PWR-2U
C508 C511 C10 C9
SC10U25V6KX-1GP
ISL88731_CSIP
R293
10R2F-L-GP
ISL88731_CSIP_R
C504
SCD22U50V3ZY-1GP
ISL88731_CSIN
35 AD_IA
R300 1KR2F-3-GP
ISL88731_IINP
R303
10KR2F-2-GP
ISL88731_CCV
ISL88731_CCS
ISL88731_VREF
C510
SCD01U16V2KX-3GP
C516
SCD01U50V2KX-1GP
C515
SCD015U25V2KX-GP
C518
SC1U10V3KX-3GP
2090107
R295
100R2J-2-GP
PBATT_SENSE_R
BATT_SENSE 48
G36
GAP-CLOSE-PWR-2U
20081024
3D3V_AUX_S5
R296
10KR2F-2-GP
ISL88731_LDO
35 AC_IN#
Q23
2N7002-11-GP
R297
10KR2F-2-GP
SB 1210
ISL88731_ACOK_L
R292
0R0402-PAD
ISL88731_ACOK
R294
15K8R3F-GP

JV50

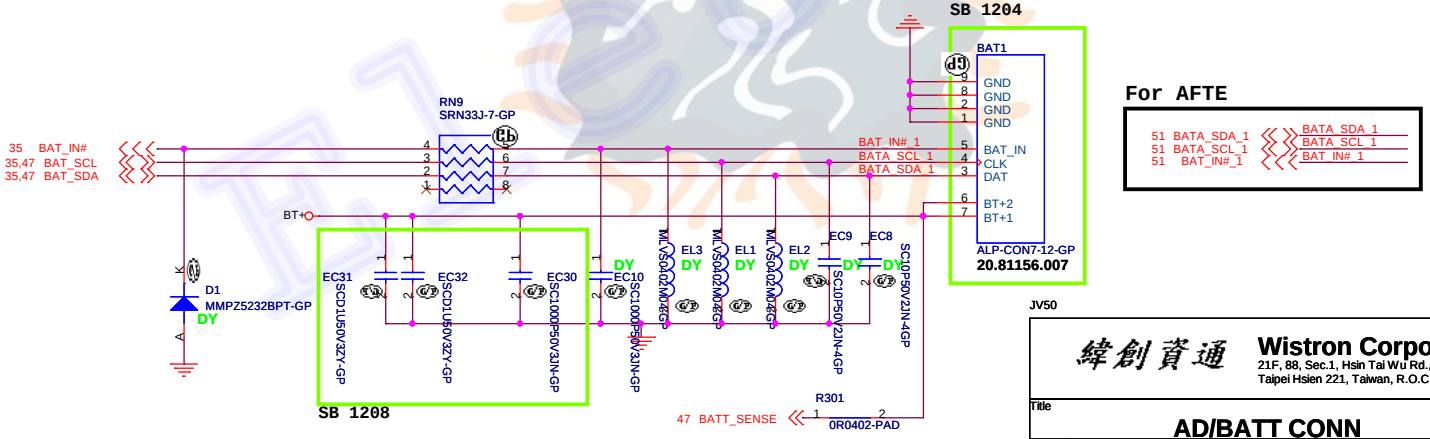
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	ISL88731A_Charger	
Size A3	Document Number JV50	Rev SB
Date: Thursday, January 08, 2009	Sheet 47 of 60	

Adaptor in to generate DCBATOUT



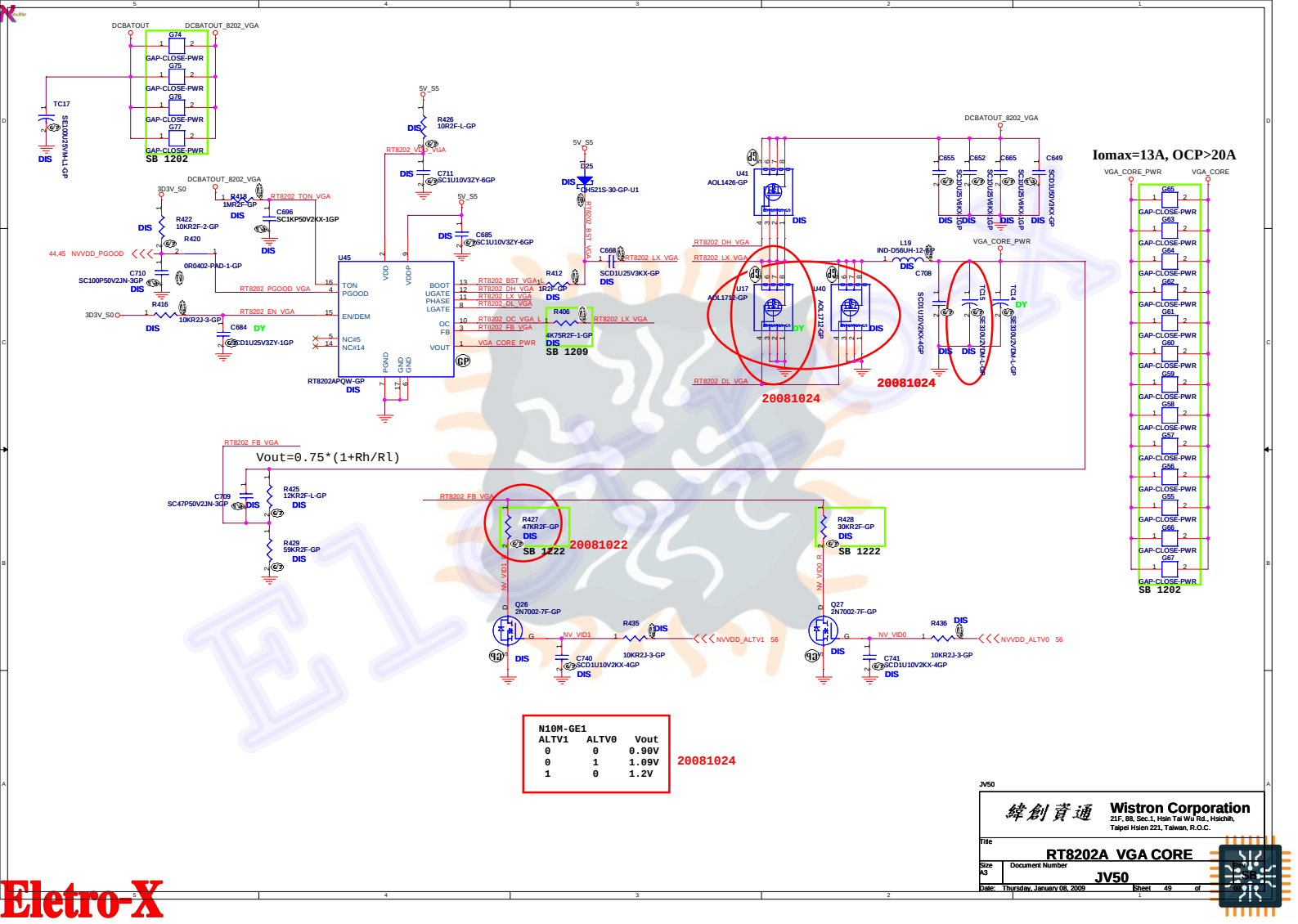
BATTERY CONNECTOR

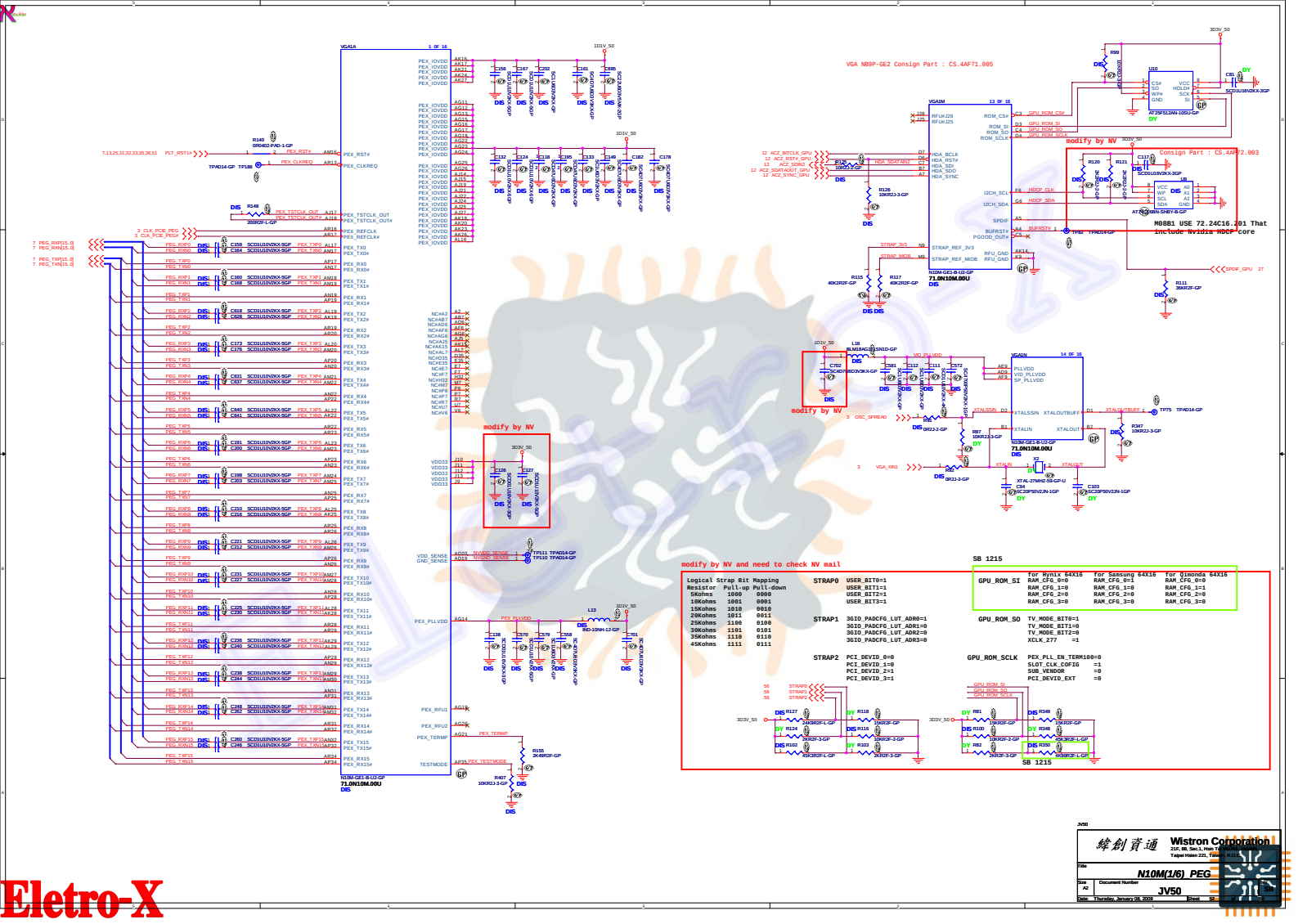


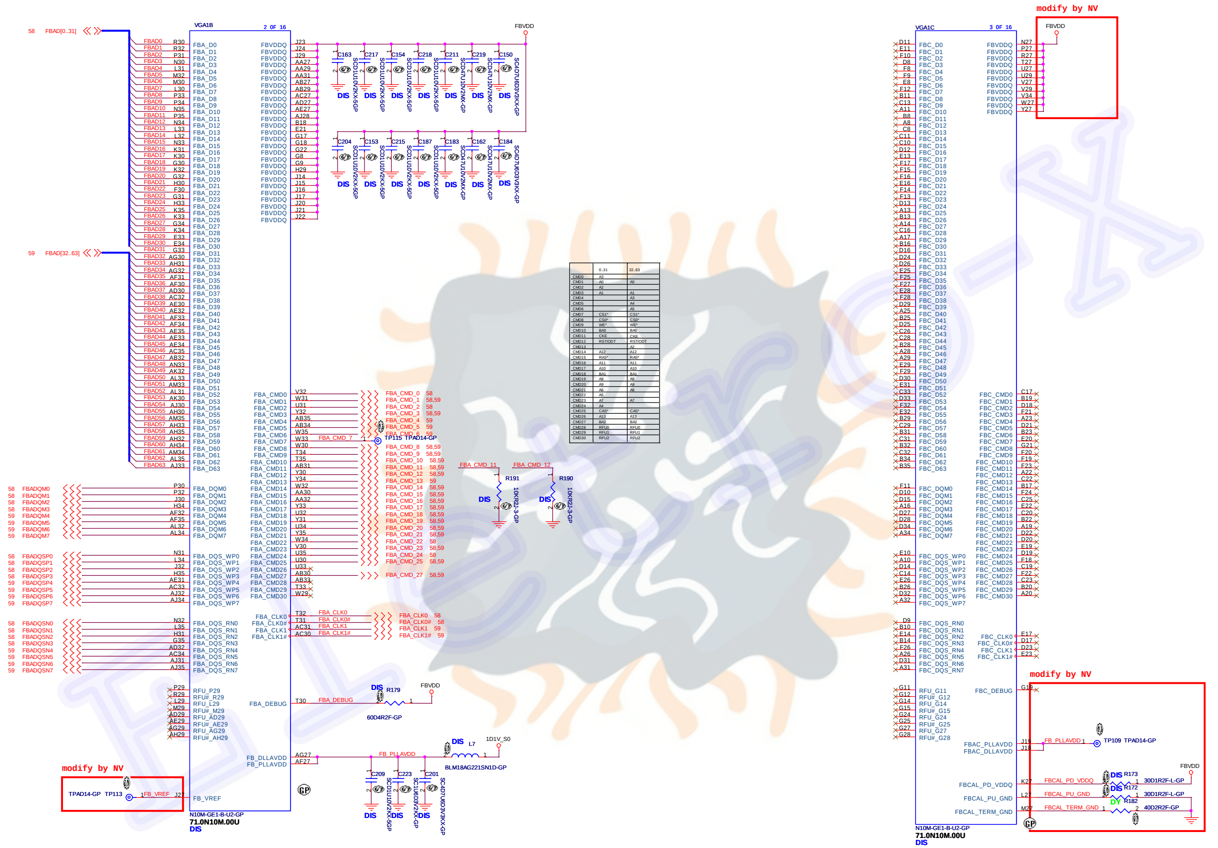
For AFTE

JV50

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	AD/BATT CONN	
Size	Document Number: JV50	Rev: SD
Date: Thursday, January 08, 2009	Sheet 48 of 60	


DCBATOUT
DCBATOUT_8202_VGA
G74
G75
G76
G77
GAP-CLOSE-PWR
TC17
SE330U2V4K-L-GP
DIS
SB 1202
3D3V_S0
R418
1MR2F-GP
RT8202_TON_VGA
R422
10KR2F-2-GP
R420
0R0402-PAD-1-GP
C696
SC1KP50V2KX-1GP
44,45 NVVDD_PGOOD
C710
SC100P50V2JN-3GP
RT8202_PGOOD_VGA
R416
10KR2J-3-GP
RT8202_EN_VGA
C684
DY
SCD1U25V3ZY-1GP
U45
TON
PGOOD
EN/DEM
NC#5
NC#14
VDD
VDDP
PGND
GND
BOOT
UGATE
PHASE
LGATE
OC
FB
VOUT
RT8202APQW-GP
5V_S5
R426
10R2F-L-GP
RT8202_VDD_VGA
C711
SC1U10V3ZY-6GP
C685
SC1U10V3ZY-6GP
D25
CH521S-30-GP-U1
RT8202_BST_VGA
C668
SCD1U25V3KX-GP
RT8202_LX_VGA
R412
1R2F-GP
RT8202_BST_VGA1
RT8202_DH_VGA
RT8202_LX_VGA
RT8202_DL_VGA
RT8202_OC_VGA
RT8202_FB_VGA
R406
4K75R2F-1-GP
SB 1209
VGA_CORE_PWR
Vout=0.75*(1+Rh/Rl)
C709
SC47P50V2JN-3GP
R425
12KR2F-L-GP
R429
59KR2F-GP
R427
47KR2F-GP
SB 1222
20081022
R428
30KR2F-GP
Q26
2N7002-7F-GP
Q27
2N7002-7F-GP
NV_VID1
NV_VID0
R435
10KR2J-3-GP
R436
C740
C741
SCD1U10V2KX-4GP
NVVDD_ALTV1
NVVDD_ALTV0
56
U41
AOL1426-GP
U17
AOL1712-GP
U40
AOL1712-GP
C655
C652
C665
C649
SCD1U25V6KX-1GP
SE330U2V4M-L-GP
L19
IND-DS6UH-12-GP
C708
SCD1U10V2KX-4GP
TC15
TC14
20081024
Iomax=13A, OCP>20A
VGA_CORE_PWR
VGA_CORE
GAP-CLOSE-PWR
SB 1202
N10M-GE1
ALTV1 ALTV0 Vout
0 0 0.90V
0 1 1.09V
1 0 1.2V
20081024
JV50
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
RT8202A VGA CORE
Size
A3
Document Number
JV50
Rev
1.0
Date: Thursday, January 08, 2009
Sheet 49 of


VGA N89P-GE2 Consign Part : CS.4AF71.005
modify by NV
Consign Part : CS.4AP72.003
M08B1 USE 72.24C16.201 That include Nvidia HDCP core
modify by NV and need to check NV mail
Logical Strap Bit Mapping
Resistor Pull-up Pull-down
5Kohms 1000 0000
10Kohms 1001 0001
15Kohms 1010 0010
20Kohms 1011 0011
25Kohms 1100 0100
30Kohms 1101 0101
35Kohms 1110 0110
45Kohms 1111 0111
STRAP0 USER_BIT0=1
USER_BIT1=1
USER_BIT2=1
USER_BIT3=1
STRAP1 3GIO_PADCFG_LUT_ADR0=1
3GIO_PADCFG_LUT_ADR1=0
3GIO_PADCFG_LUT_ADR2=0
3GIO_PADCFG_LUT_ADR3=0
STRAP2 PCI_DEVID_0=0
PCI_DEVID_1=0
PCI_DEVID_2=1
PCI_DEVID_3=1
SB 1215
GPU_ROM_SI
GPU_ROM_SO
GPU_ROM_SCLK
for Hynix 64X16
for Samsung 64X16
for Qimonda 64X16
RAM_CFG_0=0
RAM_CFG_1=0
RAM_CFG_2=0
RAM_CFG_3=0
TV_MODE_BIT0=1
TV_MODE_BIT1=0
TV_MODE_BIT2=0
XCLK_277 =1
PEX_PLL_EN_TERM100=0
SLOT_CLK_CONFIG =1
SUB_VENDOR =0
PCI_DEVID_EXT =0
SB 1215
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
N10M(1/6) PEG
Size
A2
Document Number
JV50
Date: Thursday, January 08, 2009
Sheet
Eletro-X



JV50

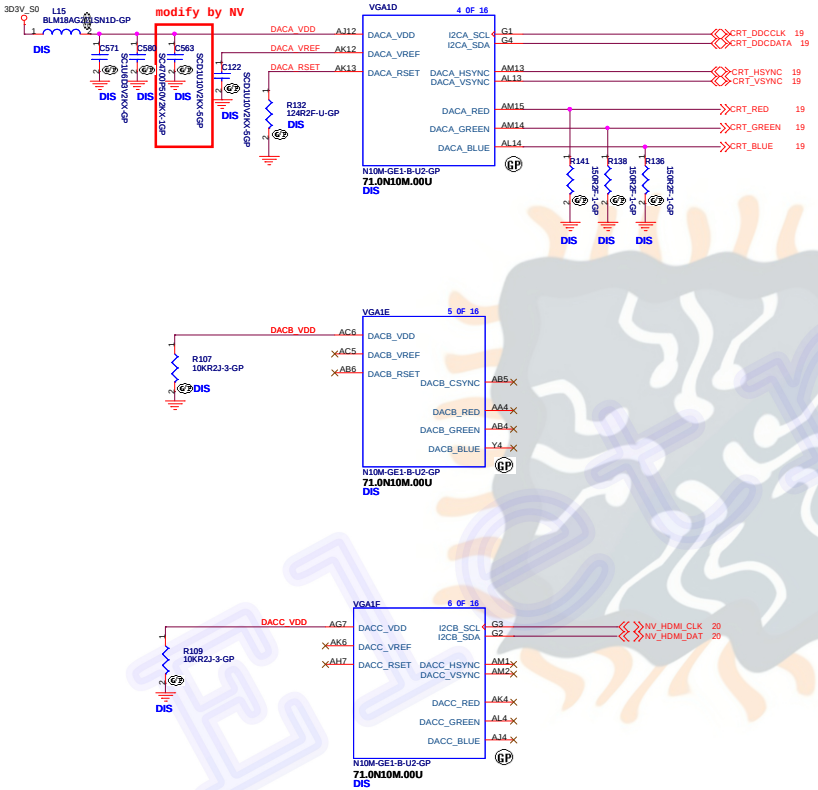
緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: N10M(2/6)_MEMORY

Size: A2 | Document Number: JV50 | Rev: SB

Date: Thursday, January 08, 2009 | Sheet 53 of 99



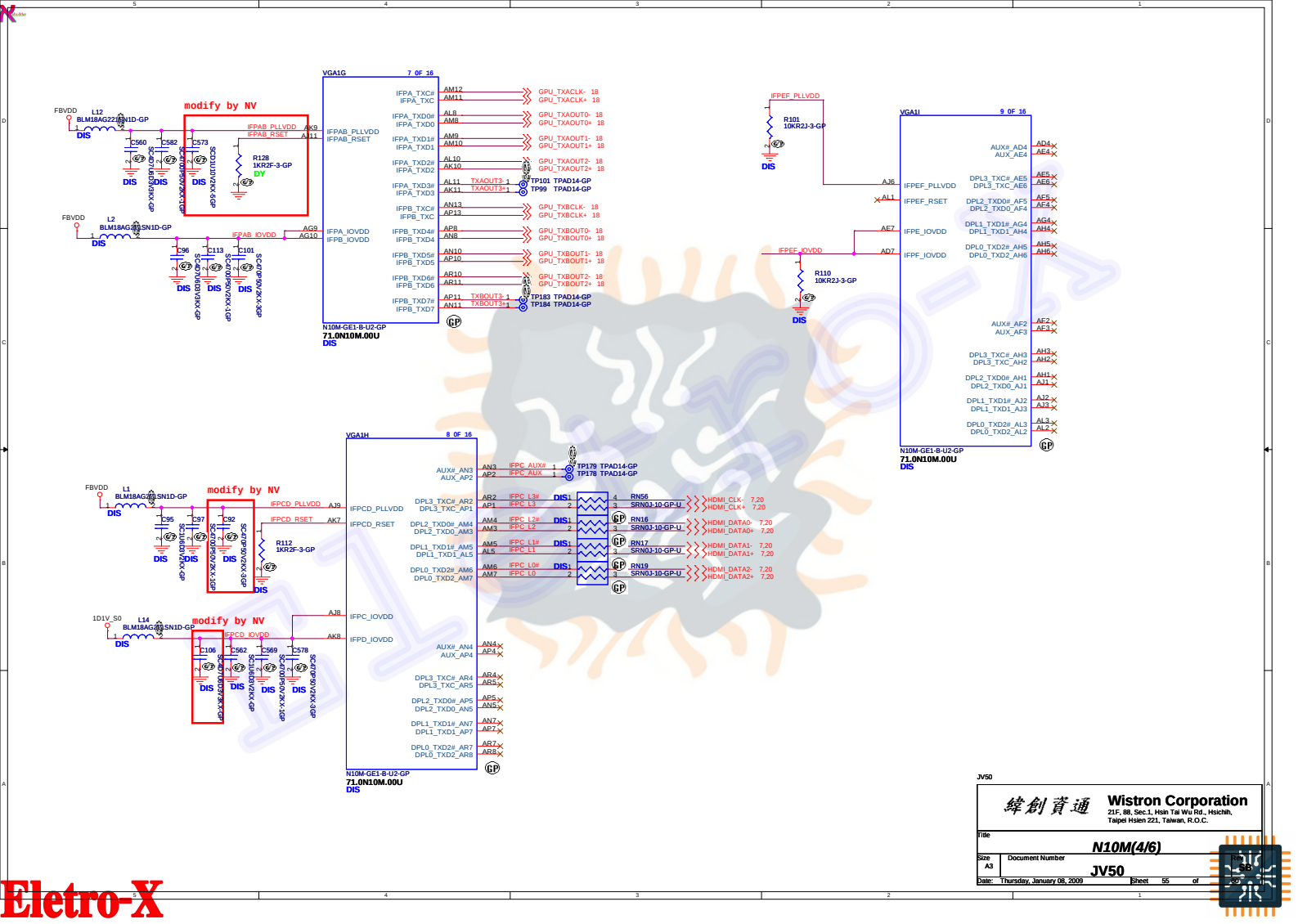
JV50

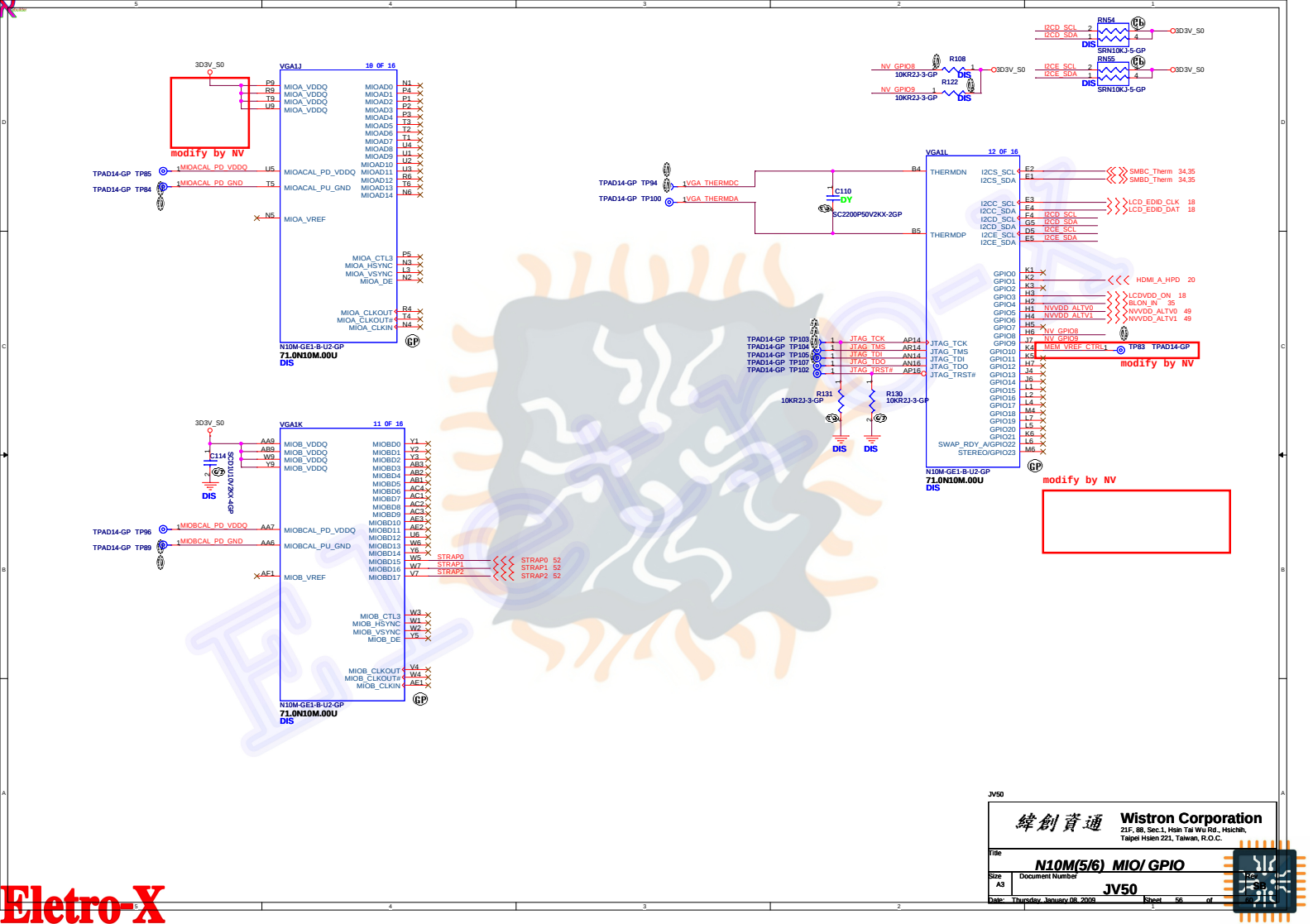
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: N10M(3/6)_DAC

Size: A3 | Document Number: JV50 | Rev: SA

Date: Thursday, January 08, 2009 | Sheet 54 of


modify by NV
VGA1G
7 OF 16
N10M-GE1-B-U2-GP
71.0N10M.00U
DIS
VGA1I
9 OF 16
VGA1H
8 OF 16
IFPAB_PLLVDD
IFPAB_RSET
IFPAB_IOVDD
IFPCD_PLLVDD
IFPCD_RSET
IFPCD_IOVDD
IFPD_IOVDD
IFPEF_PLLVDD
IFPEF_RSET
IFPEF_IOVDD
R128 1KR2F-3-GP DY
R101 10KR2J-3-GP
R110 10KR2J-3-GP
R112 1KR2F-3-GP
RN56 SRN0J-10-GP-U
RN16 SRN0J-10-GP-U
RN17 SRN0J-10-GP-U
RN19 SRN0J-10-GP-U
TP101 TPAD14-GP
TP99 TPAD14-GP
TP183 TPAD14-GP
TP184 TPAD14-GP
TP179 TPAD14-GP
TP178 TPAD14-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
N10M(4/6)
JV50
Thursday, January 08, 2009
Sheet 55 of



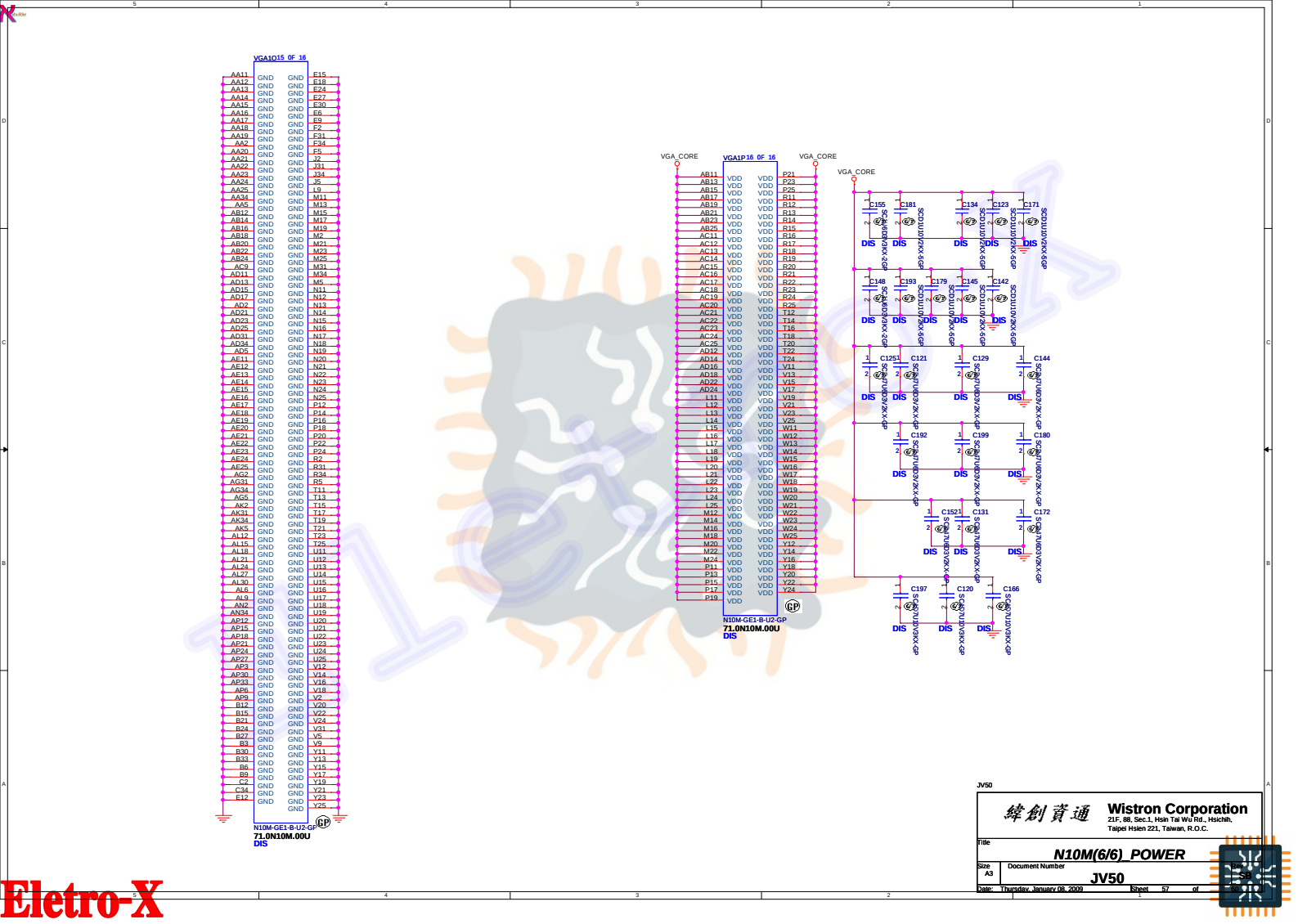
JV50

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: N10M(5/6) MIO/ GPIO

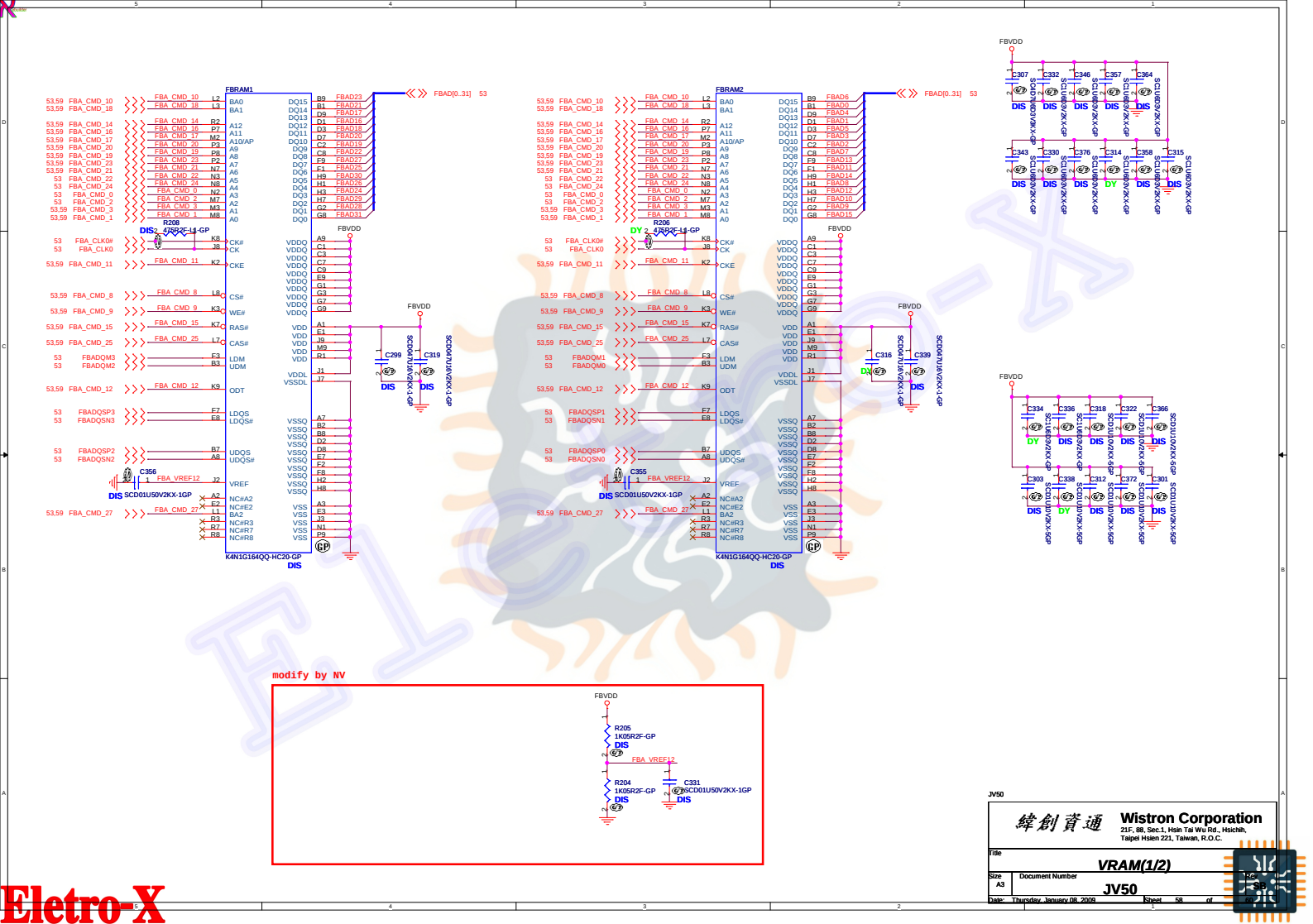
Size	Document Number	Rev
A3	JV50	SA

Date: Thursday, January 08, 2009 Sheet 56 of



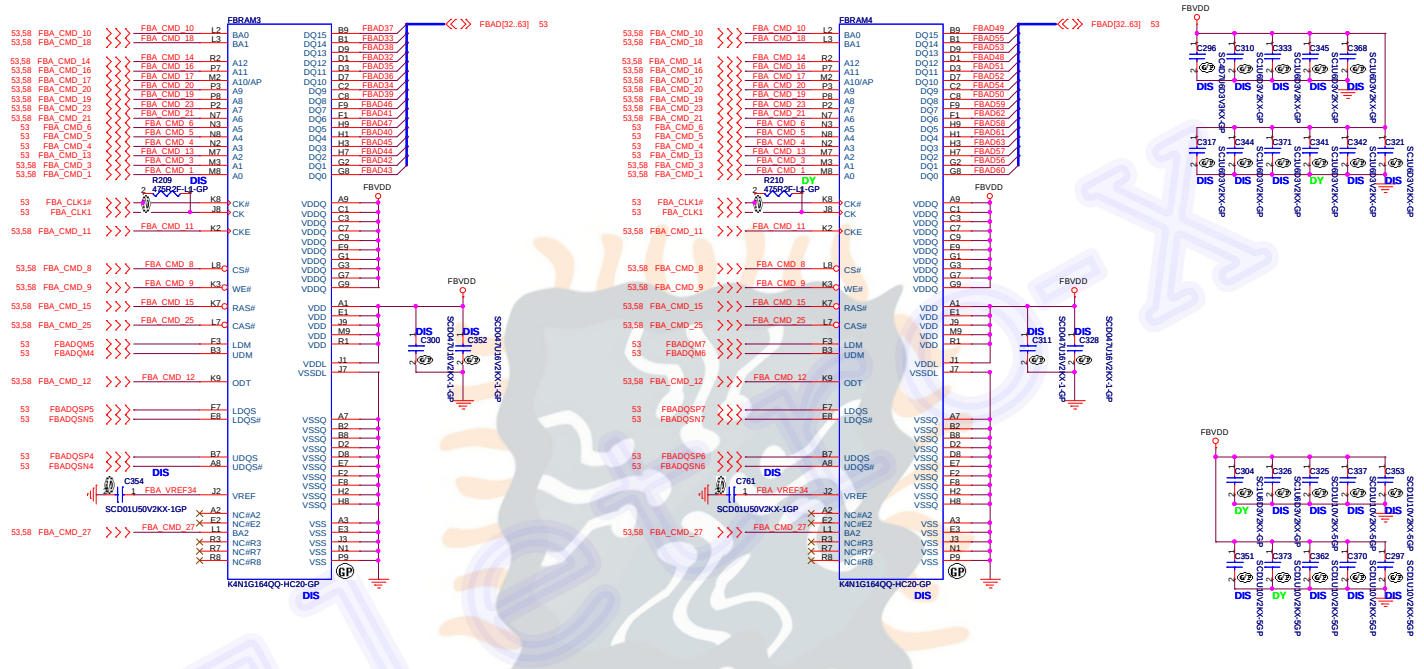
JV50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*N10M(6/6)_POWER*
Size A3	Document Number JV50
Date: Thursday, January 08, 2009	Sheet 57 of

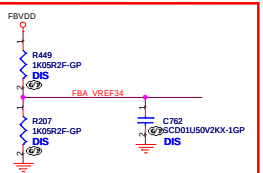


JV50

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	VRAM(1/2)	
Size A3	Document Number JV50	Rev SA
Date: Thursday, January 08, 2009	Sheet 58 of	



modify by NV



SB
All Component for NB9P-GE2

JV50

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: VRAM(2/2)		
Size: A3	Document Number: JV50	Rev: SA
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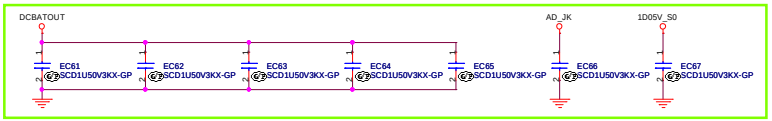
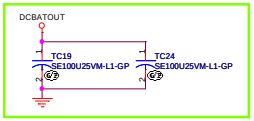
SB 1208



SB 1209



-1 0109

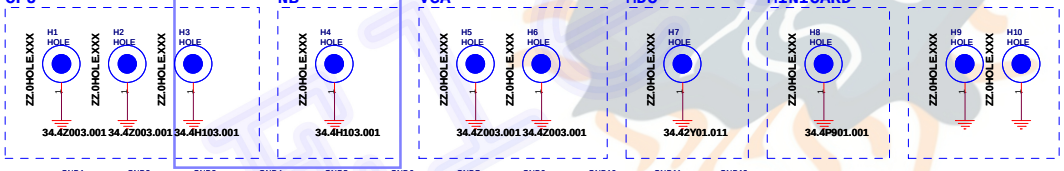
CPU

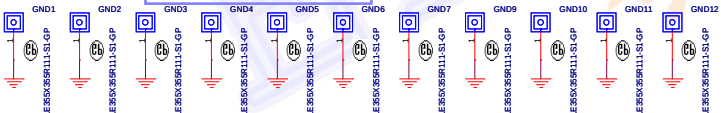
NB

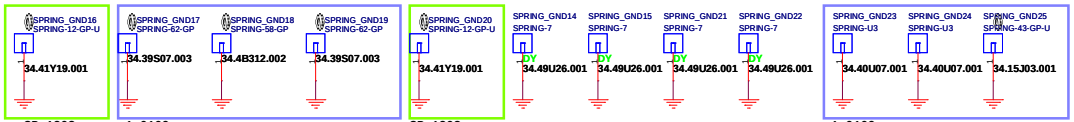
VGA

MDC

MINICARD







SB 1208 -1 0109 SB 1208 -1 0109

JV50

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EMI/Spring/Boss

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SB SB SC -1

12/02

Page3: change C452 C453 from 27P to 33P by vendor's request

Page33: add C872 33P for SIV

Page29: change SPKR_R1 SPKR_L1 from 20.F1396.002 to 20.F1214.002 by CE's request

Page18: change LCD1 from 20.F1296.040 to 20.F1230.040 by CE's request

Page24: change USBCN1 from 20.F1290.015 to 20.F1035.015 by CE's request

Page38: change PSCN1 from 20.K0356.006 to 20.K0382.006 by CE's request

Page18: change AMIC1 from 20.F1396.002 to 20.F1214.002 by CE's request

Page3: add R554 and change U24 pin16 from 3D3V_S0 to 3D3V_VDD48_S0

Page3: change C457 C450 C416 C430 C418 from mount to DY and change C456 from DY to mount

Page7: change R192 R195 from 0ohm resistor to 0ohm pad and add R555 RN82 RN83 RN84 RN85 for reflection

Page9: change C275 from UMA to DY and change C349 from mount to DY

Page10: change C243 C758 from mount to DY and change R167 R398 from DIS to DY

Page13: change R216 from 0ohm resistor to 0ohm pad

Page14: change C413 C252 C703 C392 C707 C734 from mount to DY

Page17: change C426 C429 from mount to DY

Page18: change C7 C499 from mount to DY and change R1 from mount to DIS and change R3 from DY to UMA

Page20: add RN86 for DIS HDMI SMbus

Page25: change R45 from 0ohm resistor to 0ohm pad

Page27: change R523 from 0ohm resistor to 0ohm pad

Page7: add R556 pull-low DY for A1 NB

Page28: change AGND & GND and change R509 from 0ohm resistor to 0ohm pad

Page28: change C795 C790 C792 from mount to DY and change R480 R479 from 0ohm to 6K2 and 8K2

Page28: combine C801 C802 two 1u to C801 4.7u

Page28: delete C815 C814 C809 R500 R503 R513 R507 R502 R508 D31 U56 and change U55 to 84.2N702.E31

Page28: change R474 from DY to mount and change R475 from mount to DY for 10dB

Page29: add L29 L30 L31 L32 L33 L34 for ESD

Page31: change R463 R464 R471 R467 R466 R460 R459 R494 R484 R493 R486 R485 R488 R489 R490 R492 R491 R487 from 0ohm resistor to 0ohm pad

Page32: change C487 C477 from mount to DY and change R269 from 0ohm resistor to 0ohm pad

Page12: change C385 C386 from 10p to 7p by vendor's request

Page35: change C136 C169 from 15p to 7p by vendor's request

Page33: change R15 R29 R34 from 0ohm resistor to 0ohm pad and change C542 from mount to DY

Page34: change C42 from mount to DY

Page35: change C615 C626 C638 R395 from mount to DY and change R394 from DY to mount for PCB version

Page36: change DB1 from mount to DY

Page38: add Q35 PWR_LED7 PWR_LED8 and change RN4 from 4P2R to 8P4R and change PWR_LED5 PWR_LED6 from 83.01221.I70 to 83.00193.A70 for LED type

Page39: change U66 pin1 from CPUCORE_ON to 1D5V_PWRGD and change D13 pin1 from S5_ENABLE to 3V/5V_EN

Page40: update power sequence logic

Page41: change G43-G50 from open gap to close gap and change R328 R352 R353 R317 R316 R319-R325 from 0ohm resistor to 0ohm pad

Page42: change R532 R545 R552 from 0ohm resistor to 0ohm pad and change G118-G128 G130-G140 from open gap to close gap

Page43: change R246 R233 from 0ohm resistor to 0ohm pad and change G5-G16 G18-G33 from open gap to close gap

Page43: change R246 pin2 from CPUCORE_ON to 1D5V_PWRGD and add R500 pull-high 10K 3D3V_S5

Page45: change G100-G109 from open gap to close gap

Page46: change R157 R187 from 0ohm resistor to 0ohm pad and change G68-G73 G86 G87 G89 G90 G92 G93 G95 G96 G99 from open gap to close gap

Page46: delete TC19 and change TC20 from DY to GFX

Page49: change G55-G67 G74-G77 from open gap to close gap

Page29: change RN75 from 47ohm to 75ohm

Page28: change C804 C807 from 4.7u to 1u 25V X5R

Page45: delete TC24

Page10: delete R209 R129

12/04

Page24: change U47 from 74.00545.A79 to 74.00547.A79

Page20: swap HDMI signals for routing

Page28: change U53 pin22 from AUD_HP1_EN to AMP_MUTE#_R

Page48: change BAT1 from 20.81094.007 to 20.81156.007

Page22: change ODD1 from 62.10065.541 to 62.10065.751

Page22: change R231 R247 from 0ohm resistor to 0ohm pad

12/05

Page25: change R39 R53 R21 R31 R22 R35 R28 from 0ohm resistor to 0ohm pad

Page46: change L23 from 68.R8210.10V to 68.1R01A.20B and change U43 from 84.04812.A37 to 84.04168.037 by power team's request

Page41: change R344 from 2K87 to 3K16 and change C586 from 0.47u to 0.1u by power team's request

Page41: change U35 U39 from 84.01426.037 to 84.12003.A37 and change U6 U7 U36 U38 from 84.01712.037 to 84.57N03.A37 by power team's request

Page45: change R457 from 11K to 3K48 and change TC23 from 390u to 220u by power team's request

12/08

Page26: change EC7 from DY to mount EMI's request

Page48: change EC28 EC30 EC31 EC32 from DY to mount EMI's request

Page31: change EC51 EC52 EC55 EC57 from 0.1u DY to 22p mount EMI's request

Page5: change C79 C80 from DY to mount EMI's request

Page46: change C659 from DY to GFX EMI's request

Page50: change SPRING_GND16-SPRING_GND20 from DY to mount EMI's request

Page50: add EC61-EC67 0.1u by EMI's request

Page20: change R313 R314 from 10K 100K to 18K 47K by NV's request

Page35: change U14 pin83 RN65 pin2 from SHBM to DBC_EN by annie's request

Page18: change LCD1 pin35 from NC to DBC_EN by annie's request

Page20: add ER1-ER8 0ohm pad by EMI's request

Page10: change C636 from 1000p DY to 27p mount by RF's request

12/09

Page49: change R406 from 6K2 to 4K75 by power team's request

Page46: change TC16 from mount to GFX

Page50: add TC19 TC24 100u

Page41: change C528 C529 530 C588 C597 C604 from 10u to 4.7u and change C528 C588 from mount to DY

Page46: change C656 C653 from 10u to 4.7u and change C653 from GFX to DY

Page42: change C856 C857 C851 C850 from 10u to 4.7u and change C857 C850 from mount to DY

Page41: change TC5 from DY to mount

Page5: change C553 C538 C552 C539 C547 C536 C548 C537 from DY to mount

Page17: change C426 C428 C429 from 10u to 4.7u and change C429 from DY to mount

Page16: change C440-C442 C463-C465 from 10u to 4.7u and change C440 from DY to mount and change C464 from DY to mount

Page20: change HDMI from 62.10078.161 to 62.10078.171 by CE's request

Page24: change USBCN1 from 20.F1035.015 to 20.F1290.015 by CE's request

12/10

Page46: add C873 33p GFX by RF's request

Page43: add C874 C875 33p by RF's request

Page20: swap U8 pin13 14 47 48

Page33: change R16 from DY to mount

Page47: change R292 from 0ohm resistor to 0ohm pad

12/11

Page33: change MINI2 pin 51 from 5V_S5_MIN1 to 5V_S5_MIN2

12/15

Page52: change VRAM strap R350

JV50

緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: HISTORY

Size: A2 | Document Number: JV50 | Rev: SA

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Electro X

SB SB SC -1

12/22

Page49: change R427 from 30K 47K and R428 from 47K to 30K

SC

12/22

Page42: modify by power team's request

Page35: change R372 R395 from DY to mount and change R373 R394 from mount to DY

-1

01/06

Page17: change C400 from mount to DY and change C399 from DY to mount

Page30: change R267 from 39R to 0ohm pad

Page38: delete RN7 and add Q36 Q37

Page25: change U3 pin 38 52 from LAN_AVDD to TP and change U3 pin 68 from NC to TP

Page25: delete R58 and add RN87 and change U5 to 72.24C02.R01

Page3: change R255 from 22R to 33R and change RN42 from 0ohm to 33R

Page33: change R268 R275 R259 from 0ohm resistor to 0ohm pad

Page35: change R394 from DY to mount and change R395 from mount to DY

Page28: change R526 from 0ohm resistor to 0ohm pad

Page35: change R401 from 0ohm resistor to 0ohm pad

Page35: delete Q12 and add R502 R503

Page35: change RN23 pin 5 6 from 3D3V_AUX_S5 to 3D3V_S0

Page44: change U46 to APL5930 by power team's request

Page38: add 3G and BT option

Page28: change R479 from 8K2 to 10K and change R480 from 6K2 to 4K99 for audio speaker gain

Page28: merge CCD1 to LCD1

01/07

Page44: change R437 from 0ohm pad to 0ohm resistor

Page9: change TC18 from UMA to DY and change C276 from DY to mount

Page35: delete RN21 and add R507 10K DY

Page38: change RN4 to 330R and change RN8 to 100R and delete R10 and change RN3 to 8P4R 200R

Page47: change C515 to 78.15322.2FL by power team's request

Page3: mount 33p on EC23 EC24 EC25 EC39 EC48 for RF's request

Page3: add EC68 EC69 33p DY by RF's request

Page20: add R129 4K7 for diffierent vendor

01/08

Page42: change R541 from 200K to 100K and change R544 location

Page42: change R532 R545 from 0ohm pad to 0ohm resistor

01/09

Page38: change name from 3G/BT_LED1 to 3GBT_LED1

Page50: add SPRING_GND23 34.40U07.001, SPRING_GND24 34.40U07.001, SPRING_GND25 34.15J03.001

Page50: SPRING_GND17, SPRING_GND19 change from 34.41Y19.001 to 34.39S07.003

Page50: SPRING_GND18 change from 34.41Y19.001 to 34.4B312.002