QL2 (14W) BLOCK DIAGRAM

01

PCB STACK UP
8L Dis. & UMA

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : VCC
- LAYER 5 : IN2
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

DDRIII-SODIMM1 PAGE 12
DDRIII-SODIMM2 PAGE 13
DDRIII 800/1066 MT/s
1333MT/s CFD only

CPU
Auburndale 35W
Clarksfield 45W
PAGE 3~6

PCI-Express 16X

27MHz
nVIDIA (40nm)
N11M-GE1
64 Bit
PAGE 14~18
533p

HDMI CON PAGE 20
CRT PAGE 20
Dual Link
LCD CONN PAGE 19

DMI LINK
32.768KHz 25MHz

HDMI Level Shifter
Chrontel CH7318C-BF-TR
PAGE 2

CRT
LVDS

SATA - HDD PAGE 29
SATA0 150MB
SATA - CD-ROM PAGE 29
SATA1 150MB
E-SATA PAGE 28
SATA5 150MB

PCH
Ibex-M
PAGE 7~11

CLOCK GEN
9LRS3197
PAGE 2
14.318MHz

Mini PCI-E Card x2
Express Card x1
6,8,10

USB2.0
0,1,2 USB2.0 Ports X3 PAGE 22
12 BlueTooth PAGE 22
5 Webcam PAGE 26
4 RTS5159 PAGE 21

PCI-E
X1 Mini PCI-E Card (Wireless LAN / Robson) PAGE 28
X1 LAN Atheros PCIE-LAN AR8131(M) GagaLAN PAGE 24
X1 Express Card PAGE 25

25MHz
RJ45 PAGE 24

Azalia
Analog ALC272 PAGE 22

AUDIO Amplifier TPA6017A2 PAGE 23

microphone PAGE 22
Audio Jacks (Phone/ MIC) PAGE 22
Jack to Speaker PAGE 23

32.768KHz
Keyboard PAGE 26
Touch Pad PAGE 25
ENE KBC
KB3926 C0
PAGE 27
LPC

GMT G9931P1U
FAN PAGE 26
SPI PAGE 27

ONFI
Braidwood PAGE 29
SPI PAGE 7
MDC CONN PAGE 24

- UMA GPU CORE (RT8152A) PAGE 30
- SYSTEM POWER RT8206B PAGE 31
- VCCP +1.1VTT(RT8208A) AND PCH 1.05V(RT8204) PAGE 32
- CPU CORE ADP3212 PAGE 33
- VGACORE(1.025V) RT8208A PAGE 34
- DDR III SMDDR_VTERM 1.5V/1.5VSUS(RT8207) PAGE 35
- SYSTEM CHARGER(ISL6251AHAZ-T) PAGE 37

NB5

PROJECT : QL2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

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CLOCK GENERATOR

+1.05V — L28 HCB1608KF-181T15_6 — +VDDIO_CLK

C640 .1U/10V_4
C644 .1U/10V_4
C643 10U/6.3V_6S
C642 *10U/6.3V_6S

Place each 0.1uF cap as close as possible to each VDD IO pin. Place the 10uF caps on the VDD_IO plane.

U17 — RTM875N-632-GRT — QFN32

+3V
C646 4.7U/6.3V_6
C654 4.7U/6.3V_6
C652 .1U/10V_4
C641 .1U/10V_4
C645 .1U/10V_4
C651 .1U/10V_4
C653 .1U/10V_4

+VDDIO_CLK

VDD_USB (1), VDD_LCD (5), VDD_SRC (17), VDD_CPU (24), VDD_REF (29)
VDD_CPU_IO (18), VDD_SRC_IO (15)
SDATA (31), SCLK (32)
CPU_STOP# (16), REF_0/CPU_SEL (30)
CK_PWRGD/PD#_3.3 (25)
XOUT (27), XIN (28)
VSS_SATA (9), VSS_USB (2), VSS_LCD (8)

CPU-0 (23), CPU-0# (22)
CPU-1 (20), CPU-1# (19)
DOT96T_LPR (3), DOT96C_LPR (4)
SRC-1 (13), SRC-1# (14)
SATA (10), SATA# (11)
27MHz_nonSS (6), 27MHz_SS (7)
GND (33), VSS_REF (26), VSS_CPU (21), VSS_SRC (12)

[8,12,13,25] CGDAT_SMB
[8,12,13,25] CGCLK_SMB

[8] CLK_ICH_14M — +3V — R273 10K/F_4 — R295 33_4 — CPU_SEL — C389 *10P/50V_4

Place the 33 ohm resistors close to the CK 505

CK_PWRGD_R

XTAL_OUT — XTAL_IN

CLK_BUF_BCLK_P [8]
CLK_BUF_BCLK_N [8]
133 or 100 Mhz output to PCH

CLK_BUF_DREFCLK [8]
CLK_BUF_DREFCLK# [8]
96Mhz output for generate 48Mhz (USB) and 24 Mhz (HDA)clk

CLK_BUF_PCIE_3GPLL [8]
CLK_BUF_PCIE_3GPLL# [8]
100Mhz output for DMI reference clk

CLK_BUF_DREFSSCLK [8]
CLK_BUF_DREFSSCLK# [8]
100Mhz output for SATA reference clk

CLK_VGA_27M_NONSS — R280 33_4 — CLK_27M_NONSS [16]
CLK_VGA_27M_SS — R278 33_4 — CLK_27M_SS [16]
Discrete Only

RTM875N-632-VB-GRT

+3V — R297 1K/F_4 — CK_PWRGD_R — Q28 2N7002E — [35] VR_PWRGD_CLKEN# — R298 100K/F_4

Y3 14.318MHZ — XTAL_IN — XTAL_OUT
C388 33P/50V_4
C387 33P/50V_4

+3V — R294 *10K/F_4 — CPU_SEL — R296 10K/F_4

	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

CPU bracket Hole.

H10 *H-D295DC220D161P2
H4 *H-D295DC220D161P2
H3 *H-D295DC220D161P2
H11 *H-D295DC220D161P2

VGA bracket Hole.

H12 *H-D295DC220D161P2
H13 *H-D295DC220D161P2
H8 *H-D295DC220D161P2

PAD and HOLE

H17 *H-C315D118P2
H25 *H-C315D118P2
H6 *H-C315D118P2
H5 *H-C315D118P2
H1 *H-C315D110P2
H2 *H-C315D118P2
H24 *H-C315D118P2
H27 *H-C315D118P2
H9 *H-C315I48D118P2

H14 *H-O472X236N
H26 *H-O173X114D173X114N
H23 *H-O173X114D173X114N
H7 *H-C114D114N

MINI CARD Hole.

H15 H-C276D67P2
H16 H-C276D161P2
H21 H-C276D161P2
H19 *H-C276D67P2
H20 *H-C276D161P2

[7,8,9,11,27,32,34,35,40] +1.05V
[3,7,8,9,10,11,12,13,19,20,21,22,23,24,25,26,27,28,29,30,31,32,35,38,40] +3V

MDC Hole.

H22 H-C256DJ46P2
H18 H-C256DJ46P2

EMI capacitive

+VIN — C336 .1U/25V_4, C481 .1U/25V_4, C565 .1U/25V_4
+3V — C31 .1U/10V_4, C323 .1U/10V_4, C133 .1U/10V_4, C427 .1U/10V_4

NB5

PROJECT : QL2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CLOCK & Screw Holes	1A

Date: Thursday, October 29, 2009 Sheet 2 of 46

	DIS	UMA
Ra	NA	0 ohm
Rb	0 ohm	NA
Rc	0 ohm	NA

03

U22A

DMI

Intel(R) FDI

PCI EXPRESS -- GRAPHICS

IC,AUB_CFD_rPGA,R1P0

2.7GT/s data rate

Discrete Only

FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (Check list 1.0).

U22B

MISC

THERMAL

CLOCKS

DDR3 MISC

PWR MANAGEMENT

JTAG & BPM

IC,AUB_CFD_rPGA,R1P0

For ITP CLk

JTAG MAPPING

Scan Chain (Default)	STUFF -> R97, R89, R90 NO STUFF -> R84, R512
CPU Only	STUFF -> R97, R84 NO STUFF -> R89, R512, R90
GMCH Only	STUFF -> R512, R90 NO STUFF -> R97, R84, R89

Use a voltage divider with VDDQ (1.5V) rail (ON in S3) and resistor combination of 4.75K (to VDDQ)/12K(to GND) to generate the required voltage.
Note: CRB uses a 3.3V (always ON) rail with 2K and 1K combination.

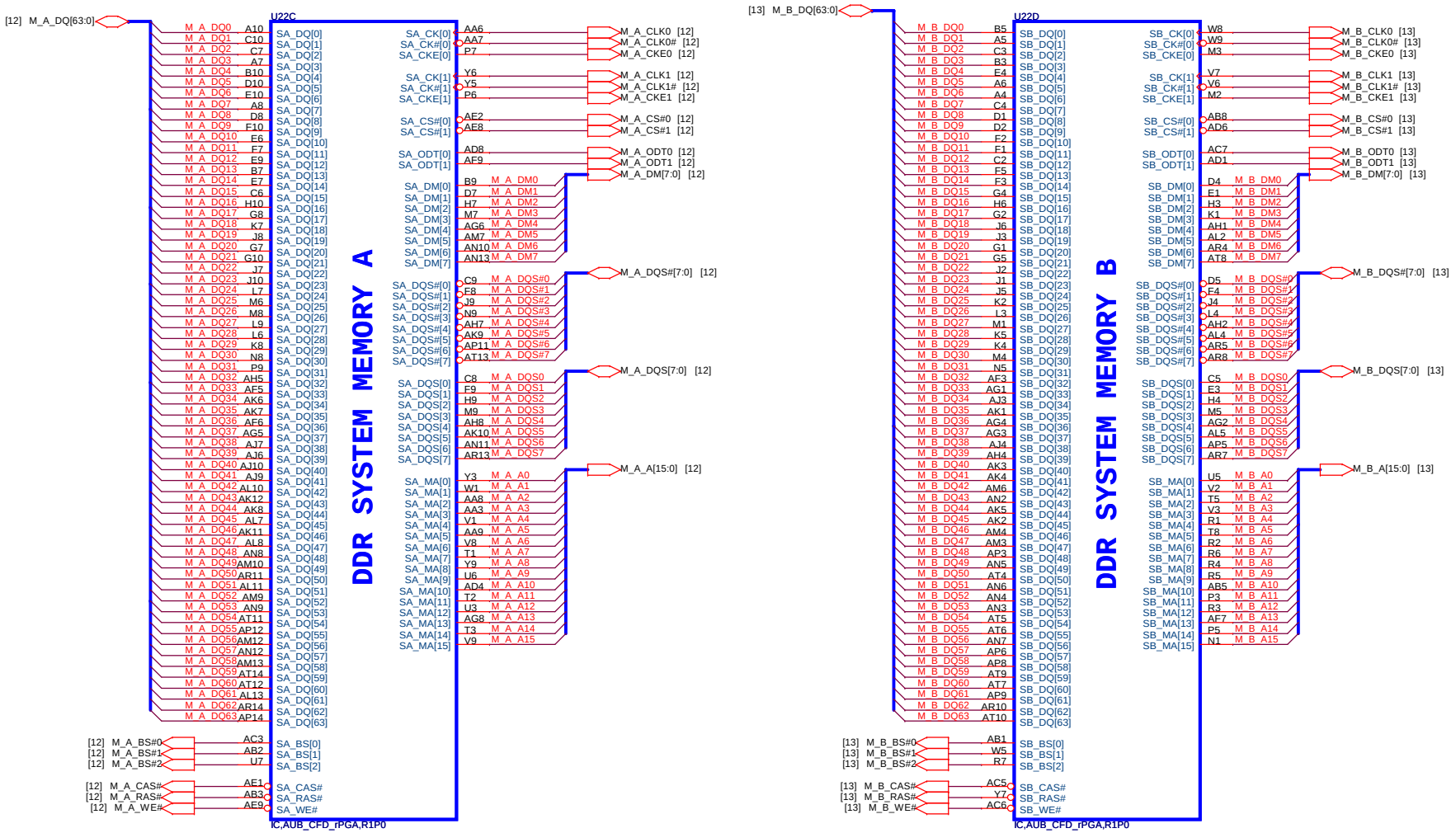
NB5

PROJECT : QL2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 1/4(HOST&PEX)	1A

Date: Thursday, October 29, 2009 Sheet 3 of 46

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



PROJECT : QL2
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	PROCESSER 2/4(DDR)	1A

Date: Monday, October 26, 2009 | Sheet 4 of 46

	DIS	UMA
Rc	NA	4.7K
Rd	NA	0 ohm
Re	NA	0 ohm
Rf	NA	NA

	DIS	UMA
Ra	0 ohm	NA

Please note that +VCC_GFX_CORE should be 1.05V in Auburndale

VTT Rail Values are
Auburndal VTT=1.05V
Clarksfield VTT=1.1V

H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V

HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

U22F — IC,AUB_CFD_rPGA,R1P0

U22G — IC,AUB_CFD_rPGA,R1P0

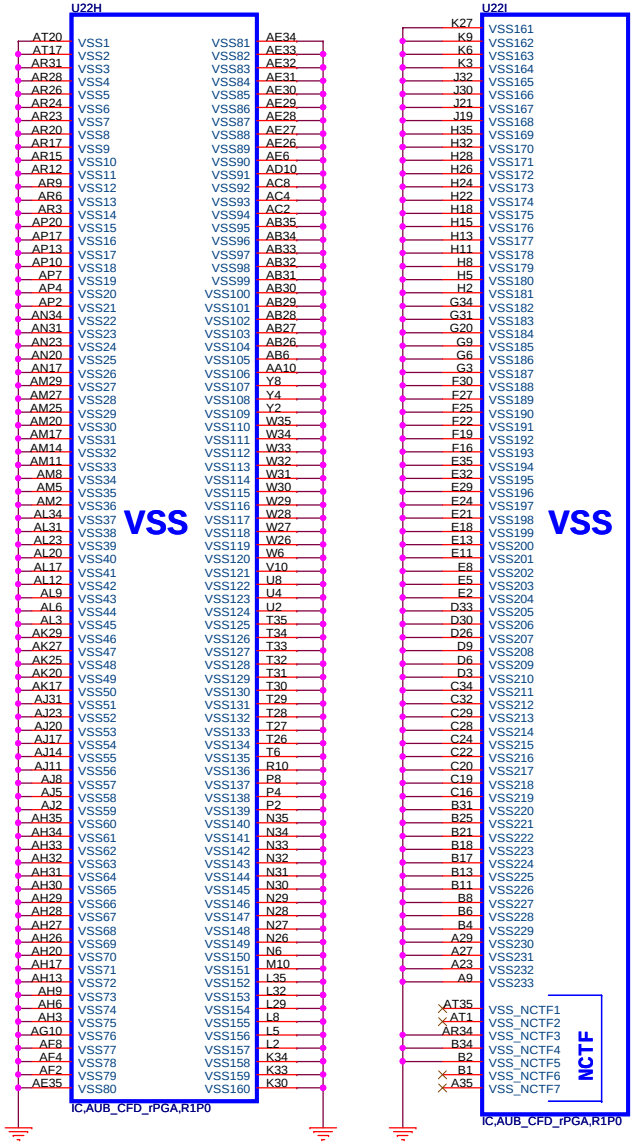
PROJECT : QL2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 3/4(POWER)	1A

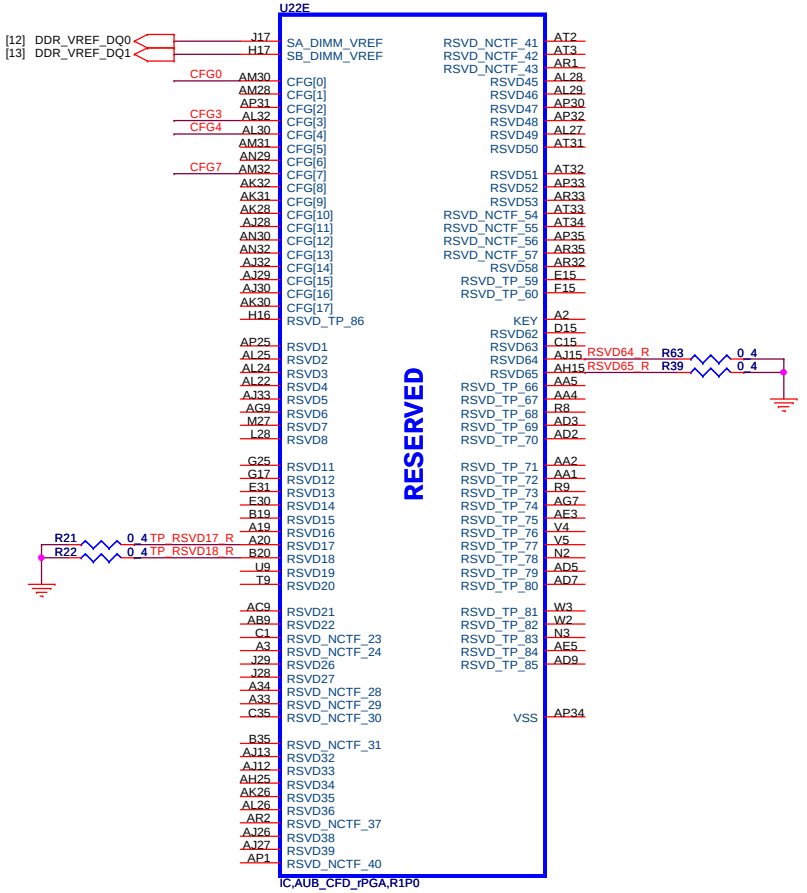
Date: Monday, October 26, 2009 Sheet 5 of 46

NB5

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



For discrete only

CFG[1:0] - PCI_Epress Configuration Select
*** 11= 1 x 16 PEG**
*** 10= 2 x 8 PEG**

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

NB5

PROJECT : QL2
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Size	Document Number	Rev
Custom	PROCESSER 4/4(GND)	1A

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INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)

U29A

Ibex-M 1 OF 10

RTC
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN

LPC
FWH0 / LAD0
FWH1 / LAD1
FWH2 / LAD2
FWH3 / LAD3
FWH4 / LFRAME#
LDRQ0#
(+3V) LDRQ1# / GPIO23
SERIRQ

SATA HDD1
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP

SATA ODD
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP

E-SATA
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP

IHDA
HDA_BCLK
HDA_SYNC
SPKR
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDO
HDA_DOCK_EN# / GPIO33 (+3V)
HDA_DOCK_RST# / GPIO13 (+3V_S5)

SATA
SATA3RXN
SATA3RXP
SATA3TXN
SATA3TXP
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATAICOMPO
SATAICOMPI
SATALED#

JTAG
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
TRST#

SPI
SPI_CLK
SPI_CS0#
SPI_CS1#
SPI_MOSI
SPI_MISO

(+3V) (+3V_S5) SATA0GP / GPIO21
SATA1GP / GPIO19

IbexPeak-M_Rev1_0

UMA LVDS & CRT signals

IBEX PEAK-M (LVDS,DDI)

U29D

Ibex-M 4 OF 10

LVDS--A
LVDSA_CLK#
LVDSA_CLK
LVDSA_DATA#0
LVDSA_DATA#1
LVDSA_DATA#2
LVDSA_DATA#3
LVDSA_DATA0
LVDSA_DATA1
LVDSA_DATA2
LVDSA_DATA3

LVDS--B
LVDSB_CLK#
LVDSB_CLK
LVDSB_DATA#0
LVDSB_DATA#1
LVDSB_DATA#2
LVDSB_DATA#3
LVDSB_DATA0
LVDSB_DATA1
LVDSB_DATA2
LVDSB_DATA3

CRT
CRT_BLUE
CRT_GREEN
CRT_RED
CRT_DDC_CLK
CRT_DDC_DATA
CRT_HSYNC
CRT_VSYNC
DAC_IREF
CRT_IRTN

SDVO
SDVO_TVCLKINN
SDVO_TVCLKINP
SDVO_STALLN
SDVO_STALLP
SDVO_INTN
SDVO_INTP
SDVO_CTRLCLK
SDVO_CTRLDATA

Digital Display Interface
DISPLAY PORT B
DDPB_AUXN
DDPB_AUXP
DDPB_HPD
DDPB_0N
DDPB_0P
DDPB_1N
DDPB_1P
DDPB_2N
DDPB_2P
DDPB_3N
DDPB_3P

DISPLAY PORT C
DDPC_CTRLCLK
DDPC_CTRLDATA
DDPC_AUXN
DDPC_AUXP
DDPC_HPD
DDPC_0N
DDPC_0P
DDPC_1N
DDPC_1P
DDPC_2N
DDPC_2P
DDPC_3N
DDPC_3P

DISPLAY PORT D
DDPD_CTRLCLK
DDPD_CTRLDATA
DDPD_AUXN
DDPD_AUXP
DDPD_HPD
DDPD_0N
DDPD_0P
DDPD_1N
DDPD_1P
DDPD_2N
DDPD_2P
DDPD_3N
DDPD_3P

IbexPeak-M_Rev1_0

UMA HDMI signals

Q24
*2N7002K

1205 The SATALED# signal is open-collector and requires a weak external pull-up (8.2 k to 10 k) to +V3.3.

UMA ony

For AUDIO

For MDC

RTC

2M byte SPI ROM for ME

U32
AKE38FP0Z00
X6179-10XXXX-8P-SOCKET

2M byte SPI ROM for ME
MXIC: AKE38FP0Z00
WINBOND: AKE38FP0N01
AIT: AKE38ZN0800

SPI ROM Socket
DG008000031

Size: Custom	Document Number: PCH 1/5 (SATA,HDA,LPC)		Rev: 1A
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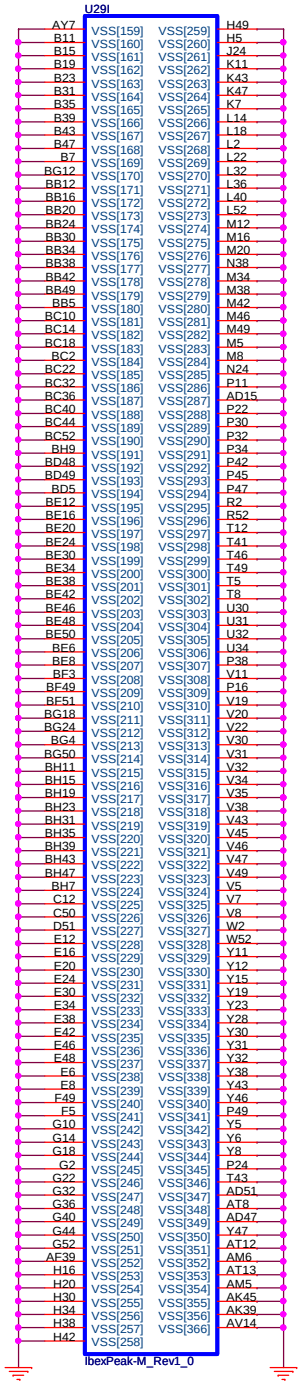
PROJECT : QL2
Quanta Computer Inc.

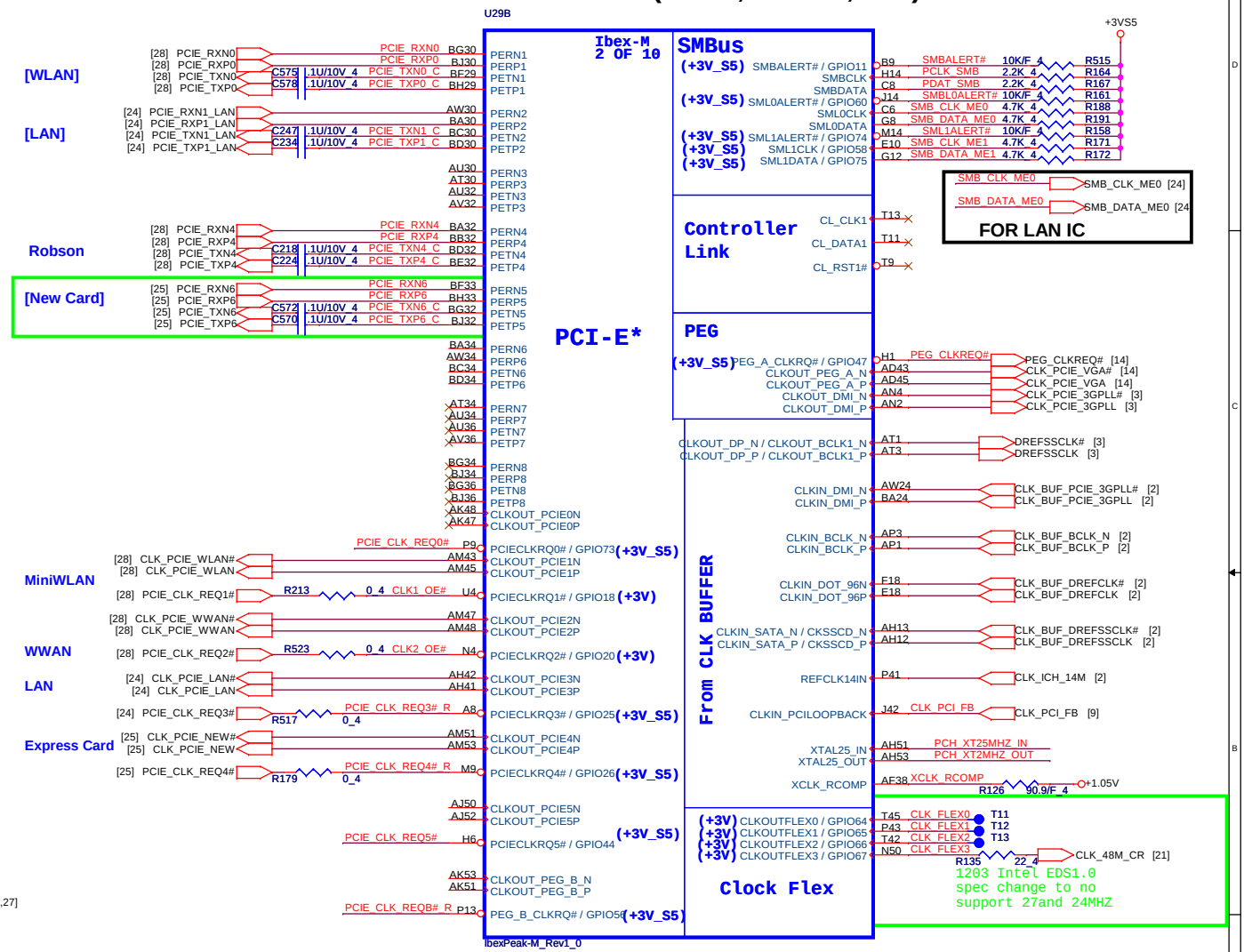
NB5

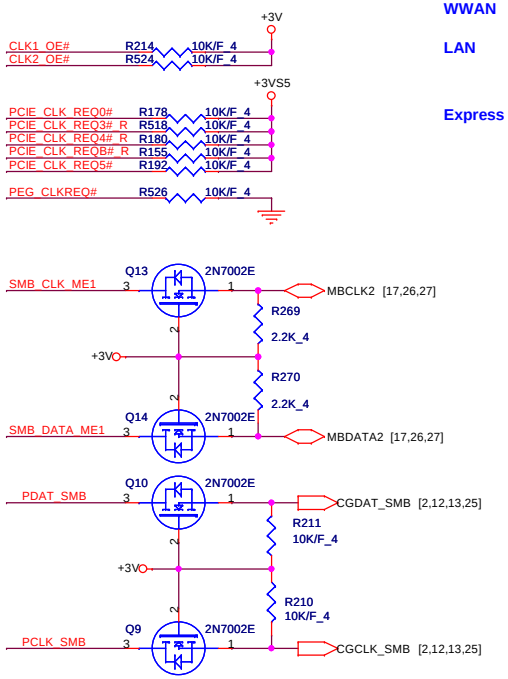
IBEX PEAK-M (GND)

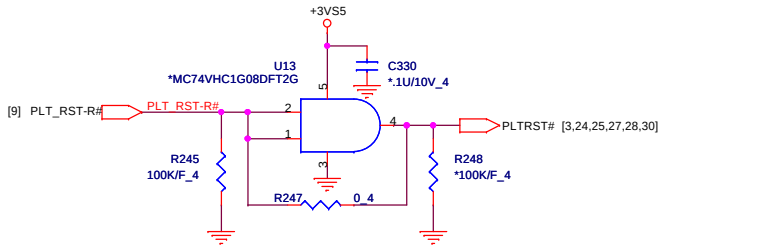


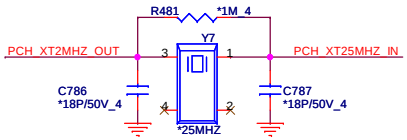
IBEX PEAK-M (PCI-E,SMBUS,CLK)

08









[3,9,10,11,14,25,38] +3VS5
[2,7,9,11,27,32,34,35,40] +1.05V
[2,3,7,9,10,11,12,13,19,20,21,22,23,24,25,26,27,28,29,30,31,32,35,38,40] +3V

NB5

PROJECT : QL2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 2/5 (PCIE, SMBUS,CK)	1A

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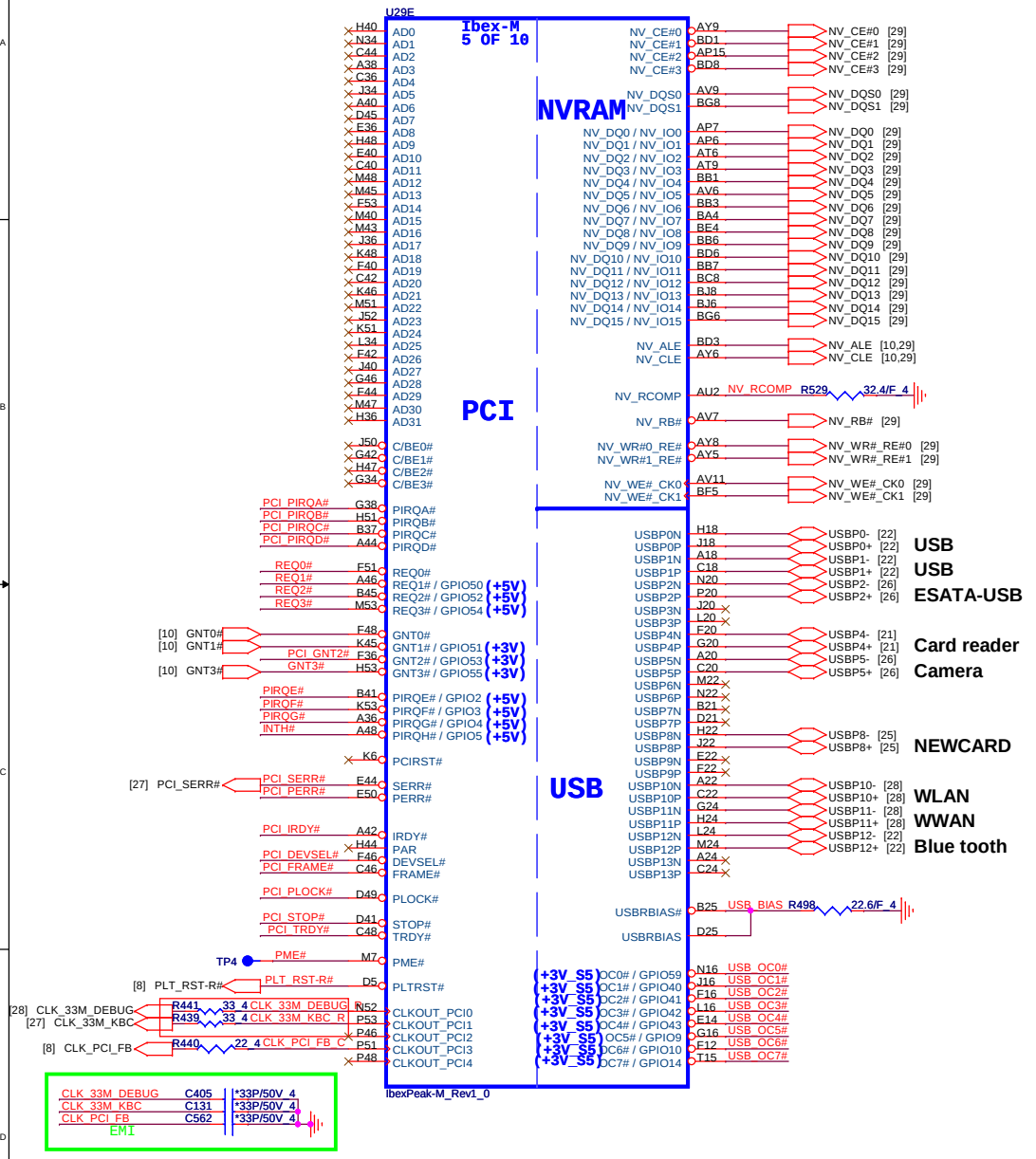
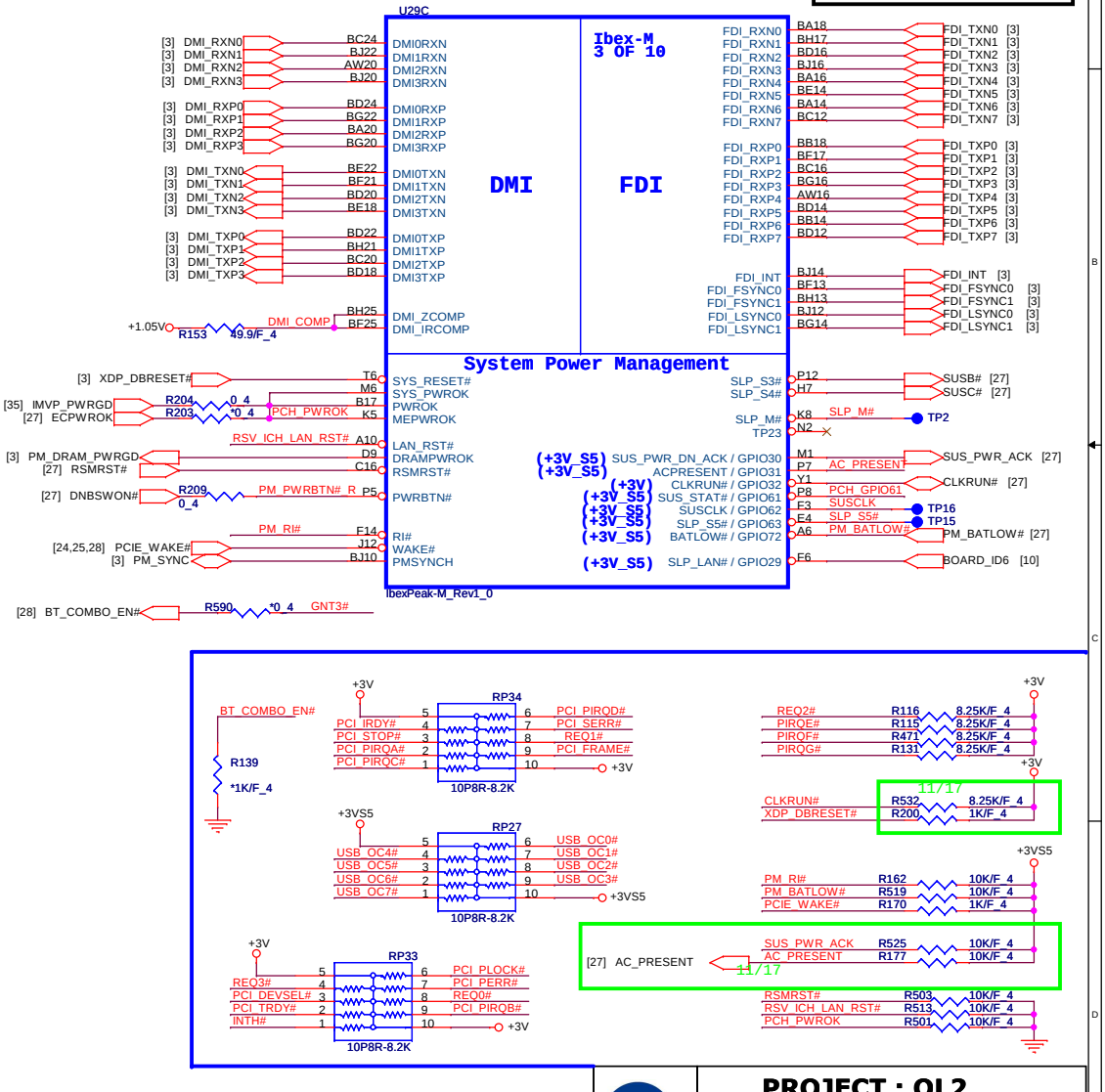
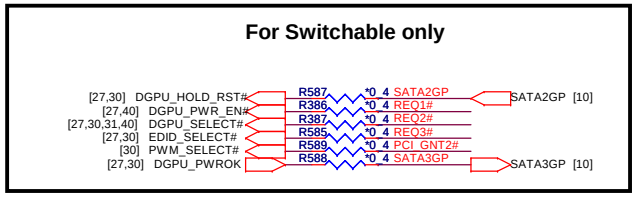
IBEX PEAK-M (PCI,USB,NVRAM)



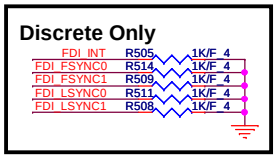
IBEX PEAK-M (DMI,FDI,GPIO)

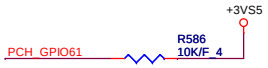


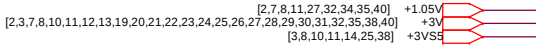
For Switchable only



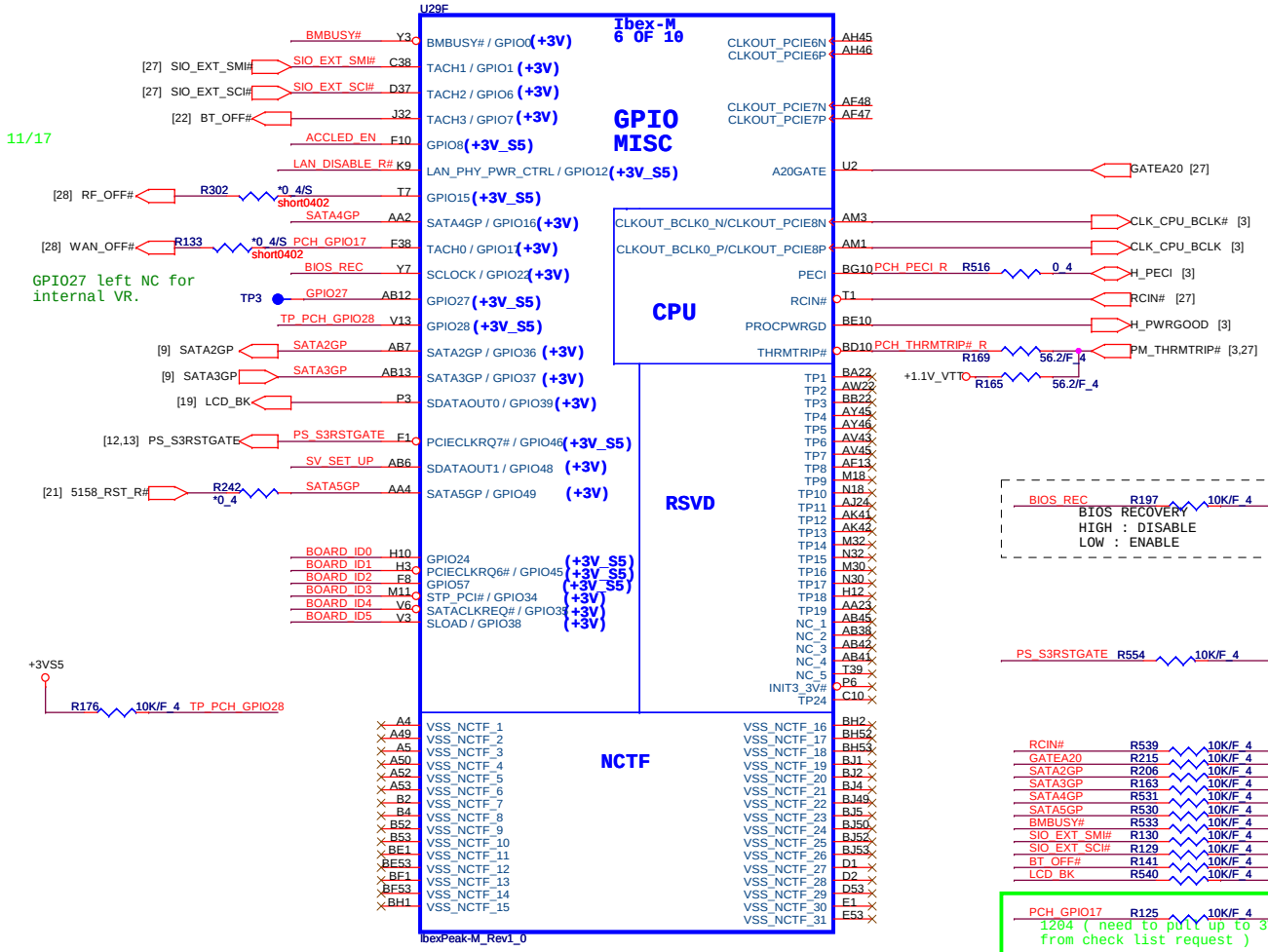
Discrete Only



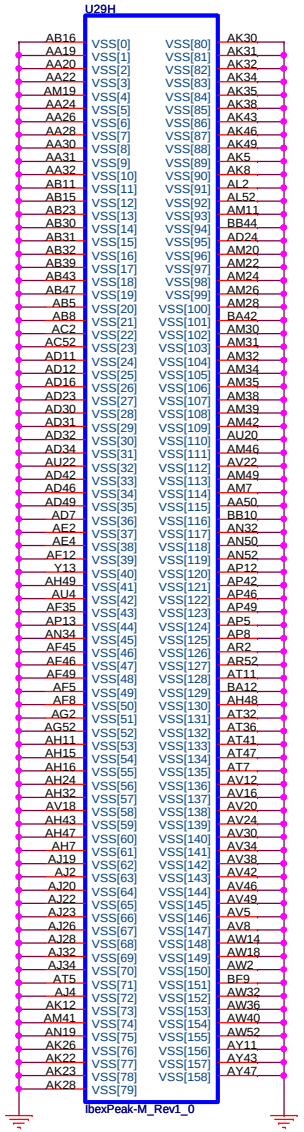


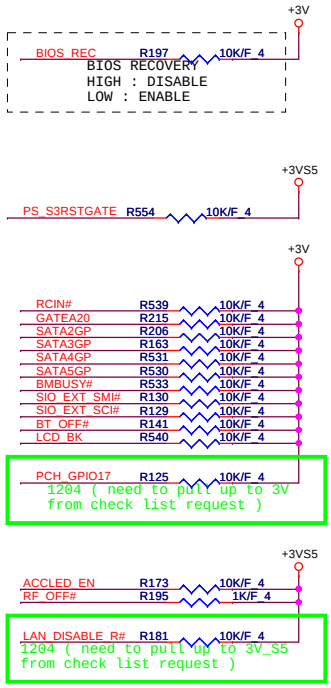


IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



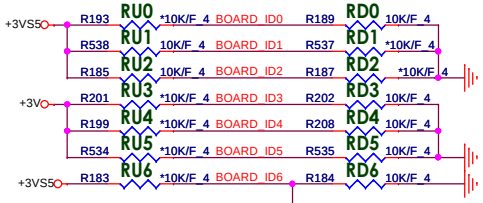
IBEX PEAK-M (GND)





Board ID	ID0	ID1	ID2	ID3	ID4	ID5	ID6
LG/CB	0=LG 1=CB						
UMA/Dis.		0=UMA 1=Dis.					
15.6"/ 14"			0=QL4/TW9 1=QL2/SW9				
MDC				0=YES 1=NO			
Braidwood					0=YES 1=NO		

BOARD ID SETTING



Board ID	ID6	ID5	ID4	ID3	ID2	ID1	ID0
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RD1 (0)	RU0 (1)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RD0 (0)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RU0 (1)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RD0 (0)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RU0 (1)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RD0 (0)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RU0 (1)

[3,5,11,35,36] +1.1V_VTT
[5,11,29,34,38,40] +1.8V
[2,3,7,8,9,11,12,13,19,20,21,22,23,24,25,26,27,28,29,30,31,32,35,38,40] +3V
[3,8,9,11,14,25,38] +3VS5

10

[9] GNT3# R470 *10K_NC

A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

SV_SET_UP R198 10K/F_4 +3V

SV_SET_UP	1-X High = Strong (Default)

[9] GNT0# GNT0# R106 *1K/F_4
[9] GNT1# GNT1# R107 *1K/F_4

Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

[9,29] NV_ALE R521 *1K/F_4
[9,29] NV_CLE R520 *1K/F_4 +1.8V
11/17

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

No Reboot Strap

[7,22] SPKR SPKR *1K/F_4 R541 +3V
[7] PCH_GPIO33 R142 *100K/F_4

NB5

PROJECT : QL2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 4/5 (GPIO & Strap)	1A
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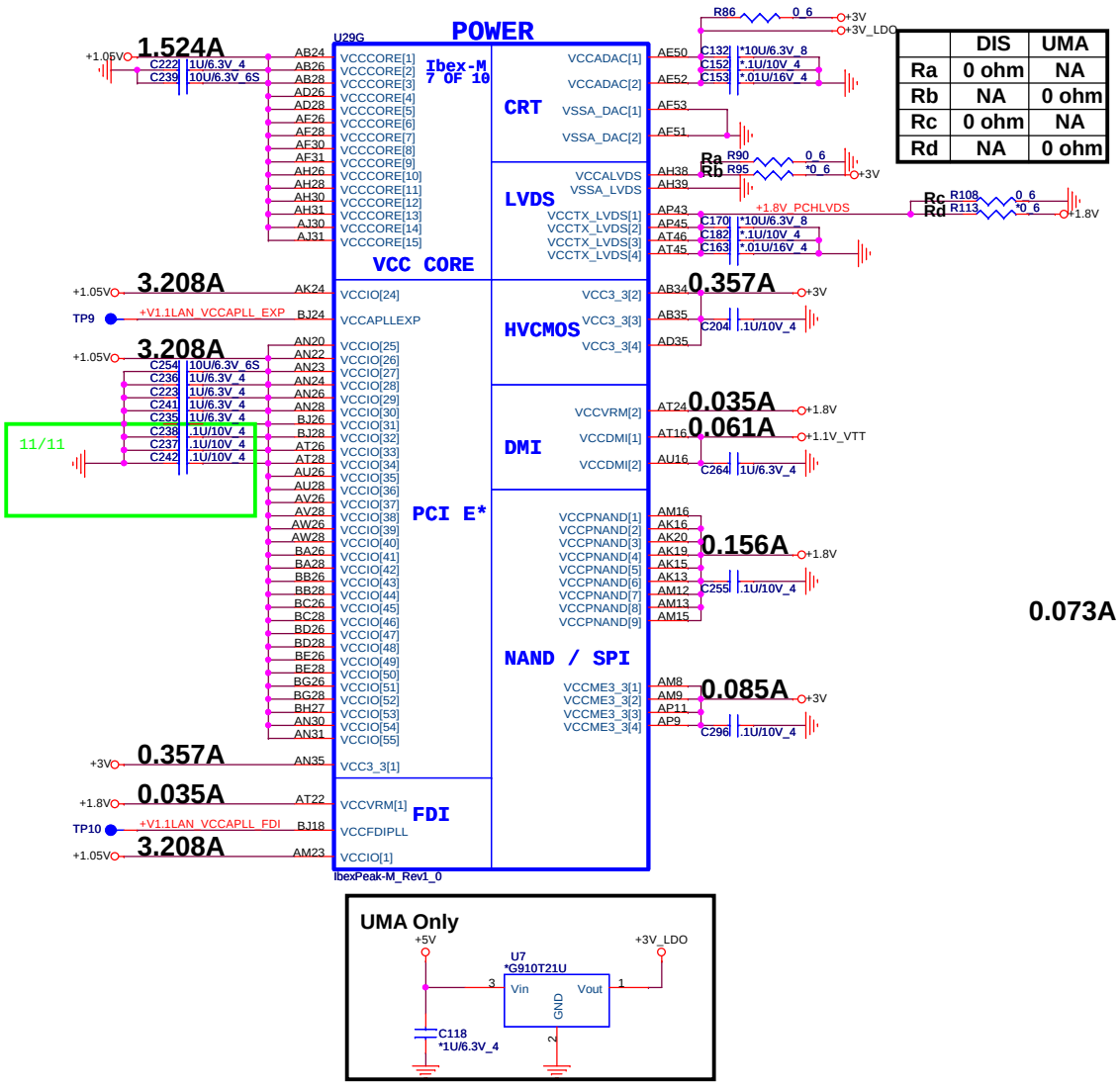
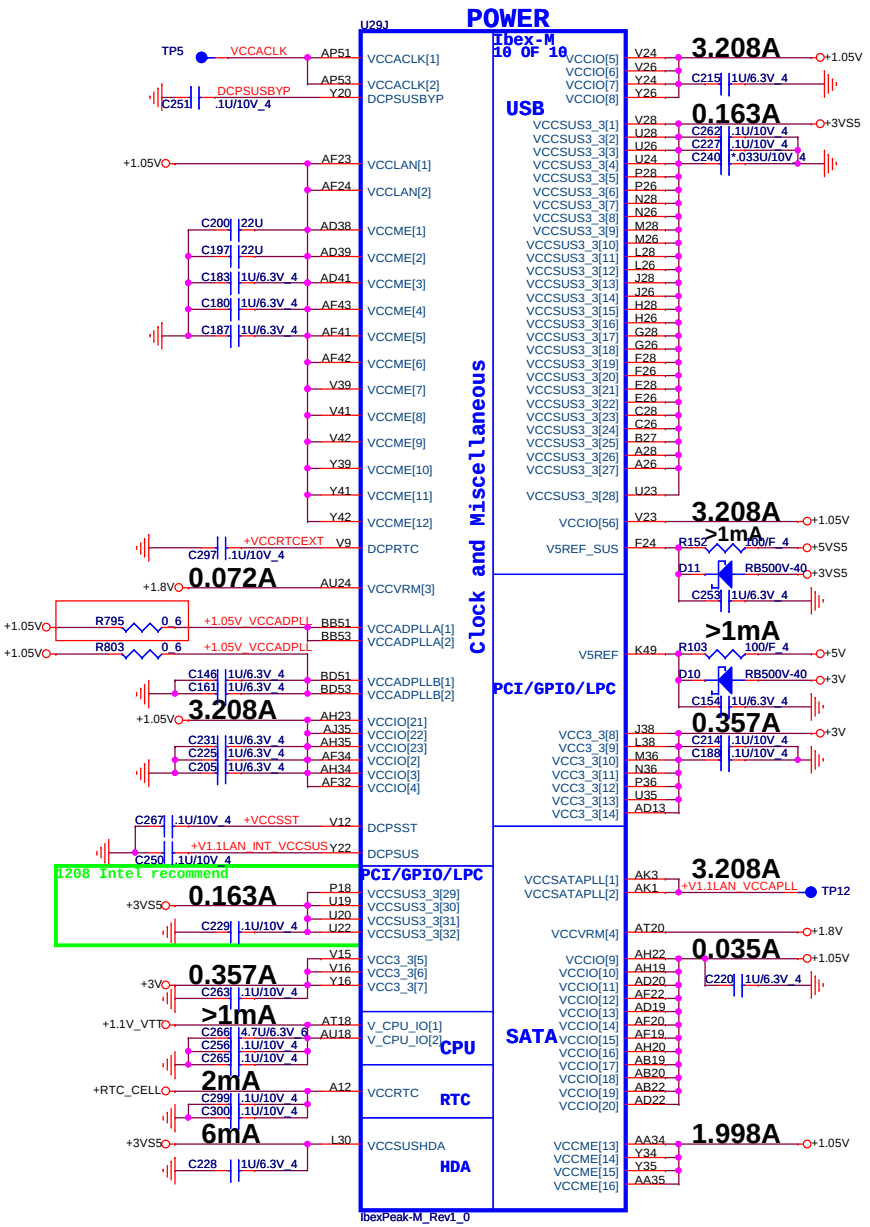


	DIS	UMA
Ra	0 ohm	NA
Rb	NA	0 ohm
Rc	0 ohm	NA
Rd	NA	0 ohm



[2,7,8,9,27,32,34,35,40] +1.05V
[3,5,10,35,36] +1.1V_VTT
[5,10,29,34,38,40] +1.8V
[2,3,7,8,9,10,12,13,19,20,21,22,23,24,25,26,27,28,29,30,31,32,35,38,40] +3V
[3,8,9,10,14,25,38] +3VS5
[20,22,23,25,26,28,30,31,38] +5V
[38] +5VS5

PROJECT : QL2
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	PCH 5/5 (POWER)	1A

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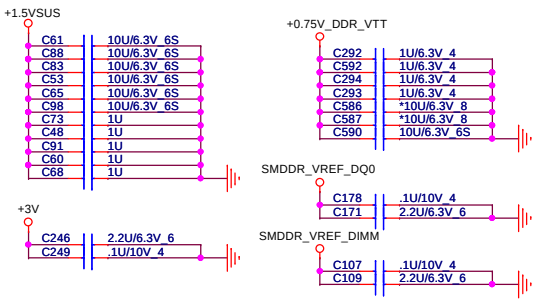
SO-DIMMA SPD Address is 0XA0
SO-DIMMA TS Address is 0X30

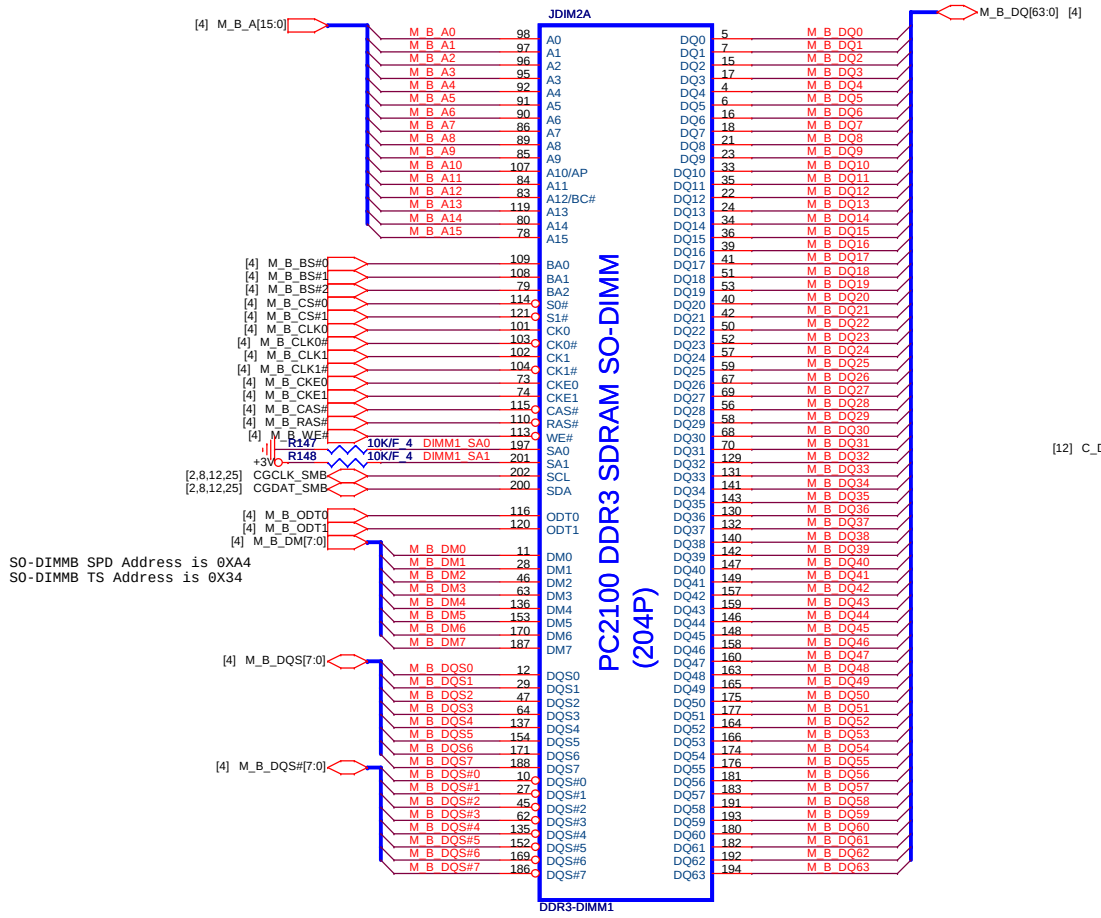
JDIM1A
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM0

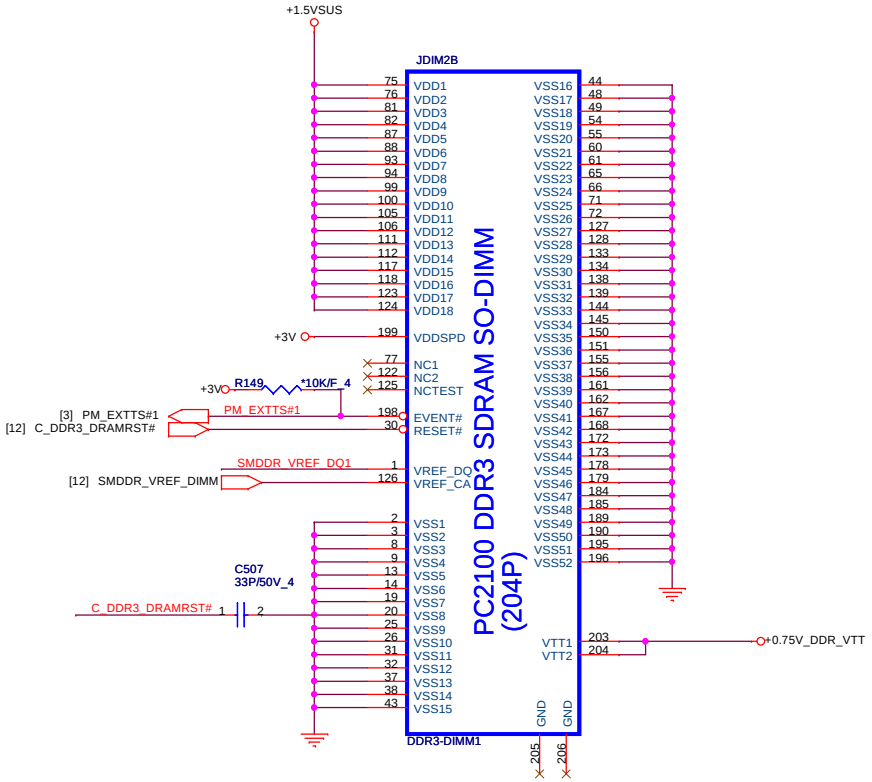
JDIM1B
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM0

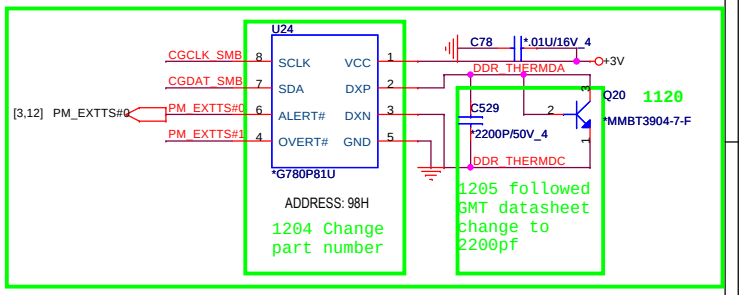
Place these Caps near So-Dimm0.

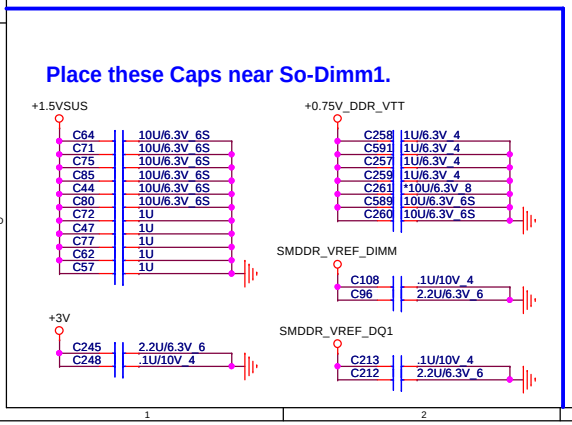
11/6

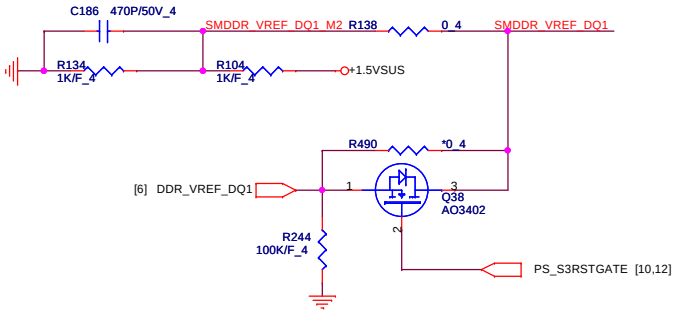












[12,37] +0.75V_DDR_VTT
[3,5,12,37,38,40] +1.5VSUS
[2,3,7,8,9,10,11,12,19,20,21,22,23,24,25,26,27,28,29,30,31,32,35,38,40] +3V
[7,19,23,26,27,28,32,33,34,36,38,39,40] +3VPCU
[27,32,33,34,35,36,37,38] +5VPCU

NB5

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Quanta Computer Inc.

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Custom	DDR3 DIMM-1	1A
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U27A

PBGA533-NVIDIA-GEFORCE6250
N10M

1/13 PCI_EXPRESS

~ 500mA

1600mA

10.87A

80mA

110mA
12~16 mils

PLACE UNDER BALLS

PLACE NEAR BALLS

C144
330u_2.5V_3528

7/22

+VGACORE

+1.05V_GFX

+3V_GFX

[36] GPU_VDD_SENSE

L24
100nH_6

L25
0_6

R442 *200_4

2.49K/F_4 R432 PEX_TERMP

+PEX_PLLVDD

+PEX_SVDD_3V3

(NC) PEX_CLKREQ

PEX_RST* — R81 10K/F_4 — R80 100/F_4 — PEGX_RST# [30]

PEX_REFCLK — CLK_PCIE_VGA — CLK_PCIE_VGA [8]
PEX_REFCLK* — CLK_PCIE_VGA# — CLK_PCIE_VGA# [8]

PEX_TX0	AD10	C_PEG_RX0 C99	PEG_RX15 [3]
PEX_TX0*	AD11	C_PEG_RX#0 C100	PEG_RX#15 [3]
PEX_TX1	AD12	C_PEG_RX1 C101	PEG_RX14 [3]
PEX_TX1*	AC12	C_PEG_RX#1 C105	PEG_RX#14 [3]
PEX_TX2	AB11	C_PEG_RX2 C94	PEG_RX13 [3]
PEX_TX2*	AB12	C_PEG_RX#2 C97	PEG_RX#13 [3]
PEX_TX3	AD13	C_PEG_RX3 C106	PEG_RX12 [3]
PEX_TX3*	AD14	C_PEG_RX#3 C112	PEG_RX#12 [3]
PEX_TX4	AD15	C_PEG_RX4 C113	PEG_RX11 [3]
PEX_TX4*	AC15	C_PEG_RX#4 C119	PEG_RX#11 [3]
PEX_TX5	AB14	C_PEG_RX5 C120	PEG_RX10 [3]
PEX_TX5*	AB15	C_PEG_RX#5 C129	PEG_RX#10 [3]
PEX_TX6	AC16	C_PEG_RX6 C130	PEG_RX9 [3]
PEX_TX6*	AD16	C_PEG_RX#6 C135	PEG_RX#9 [3]
PEX_TX7	AD17	C_PEG_RX7 C136	PEG_RX8 [3]
PEX_TX7*	AD18	C_PEG_RX#7 C140	PEG_RX#8 [3]
PEX_TX8	AC18	C_PEG_RX8 C143	PEG_RX7 [3]
PEX_TX8*	AB18	C_PEG_RX#8 C147	PEG_RX#7 [3]
PEX_TX9	AB19	C_PEG_RX9 C150	PEG_RX6 [3]
PEX_TX9*	AB20	C_PEG_RX#9 C156	PEG_RX#6 [3]
PEX_TX10	AD19	C_PEG_RX10 C158	PEG_RX5 [3]
PEX_TX10*	AD20	C_PEG_RX#10 C167	PEG_RX#5 [3]
PEX_TX11	AD21	C_PEG_RX11 C168	PEG_RX4 [3]
PEX_TX11*	AC21	C_PEG_RX#11 C176	PEG_RX#4 [3]
PEX_TX12	AB21	C_PEG_RX12 C177	PEG_RX3 [3]
PEX_TX12*	AB22	C_PEG_RX#12 C181	PEG_RX#3 [3]
PEX_TX13	AC22	C_PEG_RX13 C185	PEG_RX2 [3]
PEX_TX13*	AD22	C_PEG_RX#13 C190	PEG_RX#2 [3]
PEX_TX14	AD23	C_PEG_RX14 C194	PEG_RX1 [3]
PEX_TX14*	AD24	C_PEG_RX#14 C199	PEG_RX#1 [3]
PEX_TX15	AE25	C_PEG_RX15 C203	PEG_RX0 [3]
PEX_TX15*	AE26	C_PEG_RX#15 C210	PEG_RX#0 [3]

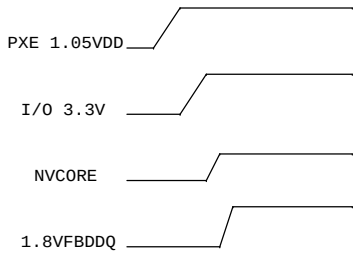
PEX_RX0	AE12	PEG_TX15	PEG_TX15 [3]
PEX_RX0*	AF12	PEG_TX#15	PEG_TX#15 [3]
PEX_RX1	AG12	PEG_TX14	PEG_TX14 [3]
PEX_RX1*	AG13	PEG_TX#14	PEG_TX#14 [3]
PEX_RX2	AF13	PEG_TX13	PEG_TX13 [3]
PEX_RX2*	AE13	PEG_TX#13	PEG_TX#13 [3]
PEX_RX3	AE15	PEG_TX12	PEG_TX12 [3]
PEX_RX3*	AF15	PEG_TX#12	PEG_TX#12 [3]
PEX_RX4	AG15	PEG_TX11	PEG_TX11 [3]
PEX_RX4*	AG16	PEG_TX#11	PEG_TX#11 [3]
PEX_RX5	AF16	PEG_TX10	PEG_TX10 [3]
PEX_RX5*	AE16	PEG_TX#10	PEG_TX#10 [3]
PEX_RX6	AE18	PEG_TX9	PEG_TX9 [3]
PEX_RX6*	AF18	PEG_TX#9	PEG_TX#9 [3]
PEX_RX7	AG18	PEG_TX8	PEG_TX8 [3]
PEX_RX7*	AG19	PEG_TX#8	PEG_TX#8 [3]
PEX_RX8	AF19	PEG_TX7	PEG_TX7 [3]
PEX_RX8*	AE19	PEG_TX#7	PEG_TX#7 [3]
PEX_RX9	AE21	PEG_TX6	PEG_TX6 [3]
PEX_RX9*	AF21	PEG_TX#6	PEG_TX#6 [3]
PEX_RX10	AG21	PEG_TX5	PEG_TX5 [3]
PEX_RX10*	AG22	PEG_TX#5	PEG_TX#5 [3]
PEX_RX11	AF22	PEG_TX4	PEG_TX4 [3]
PEX_RX11*	AE22	PEG_TX#4	PEG_TX#4 [3]
PEX_RX12	AE24	PEG_TX3	PEG_TX3 [3]
PEX_RX12*	AF24	PEG_TX#3	PEG_TX#3 [3]
PEX_RX13	AG24	PEG_TX2	PEG_TX2 [3]
PEX_RX13*	AF25	PEG_TX#2	PEG_TX#2 [3]
PEX_RX14	AG25	PEG_TX1	PEG_TX1 [3]
PEX_RX14*	AG26	PEG_TX#1	PEG_TX#1 [3]
PEX_RX15	AF27	PEG_TX0	PEG_TX0 [3]
PEX_RX15*	AE27	PEG_TX#0	PEG_TX#0 [3]

VDD_01	J10	
VDD_02	J12	
VDD_03	J13	
VDD_04	J9	
VDD_05	L9	
VDD_06	M11	
VDD_07	M17	
VDD_08	M9	
VDD_09	N11	
VDD_10	N12	
VDD_11	N13	
VDD_12	N14	
VDD_13	N15	
VDD_14	N16	
VDD_15	N17	
VDD_16	N19	
VDD_17	N9	
VDD_18	P11	
VDD_19	P12	
VDD_20	P13	
VDD_21	P14	
VDD_22	P15	
VDD_23	P16	
VDD_24	P17	
VDD_25	R11	
VDD_26	R12	
VDD_27	R13	
VDD_28	R14	
VDD_29	R15	
VDD_30	R16	
VDD_31	R17	
VDD_32	R9	
VDD_33	T11	
VDD_34	T17	
VDD_35	T9	
VDD_36	U19	
VDD_37	U9	
VDD_38	W10	
VDD_39	W12	
VDD_40	W13	
VDD_41	W18	
VDD_42	W19	
VDD_43	W9	
VDD_SENSE	W15	
GND_SENSE	W16	
VDD_SENSE (NC)	E15	
GND_SENSE (GND)	E14	
VDD33_01	A12	
VDD33_02	B12	
VDD33_03	C12	
VDD33_04	D12	
VDD33_05	E12	
VDD33_06	F12	
PEX_PLLVDD	AF9	
PEX_TSTCLK_OUT*	AE10	
PEX_TSTCLK_OUT	AF10	
PEG_SVDD (NC)	AG9	
PEX_TERMP	AG10	

For Switchable only

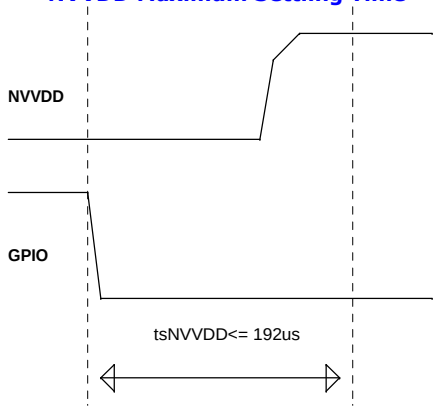
+3V_GFX — R633 *10K/F_4 — +3VS5
R634 *10K/F_4
PEG_CLKREQ# [8]
CLKRQ1
Q32 *DTC144EUA
Q34 *DTC144EUA
PEX_CLKREQ#

power up sequence

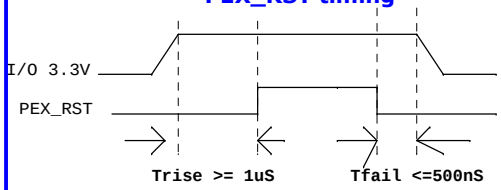


NB9M: VGACORE +0.90V (Normal) , +1.09V

NVVDD Maximum Settling Time



PEX_RST timing



VGA Thermal Circuit ==> Del 6/16

NB5

PROJECT : QL2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N10M-GE (PCIE I/F) 1/5	1A

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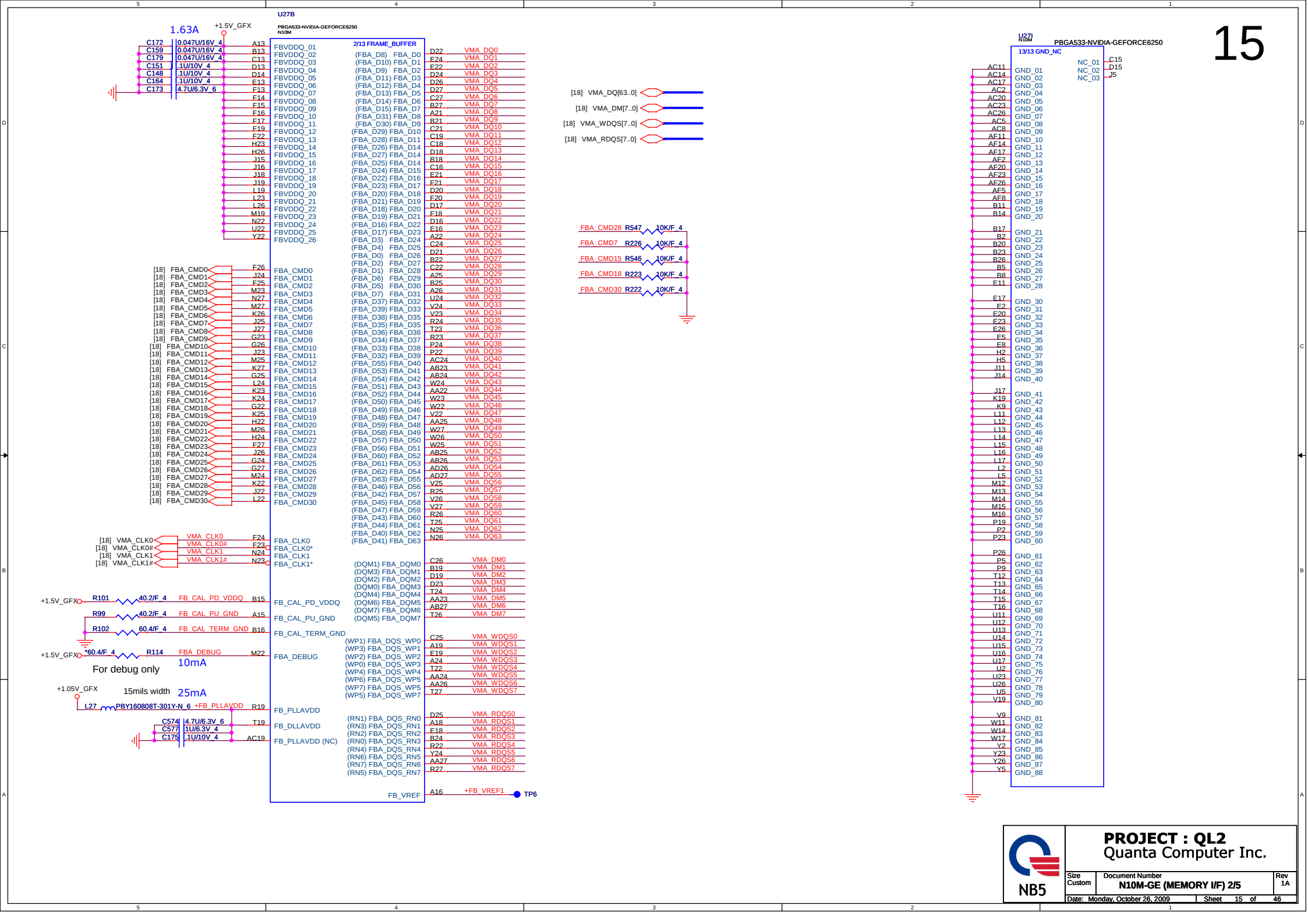
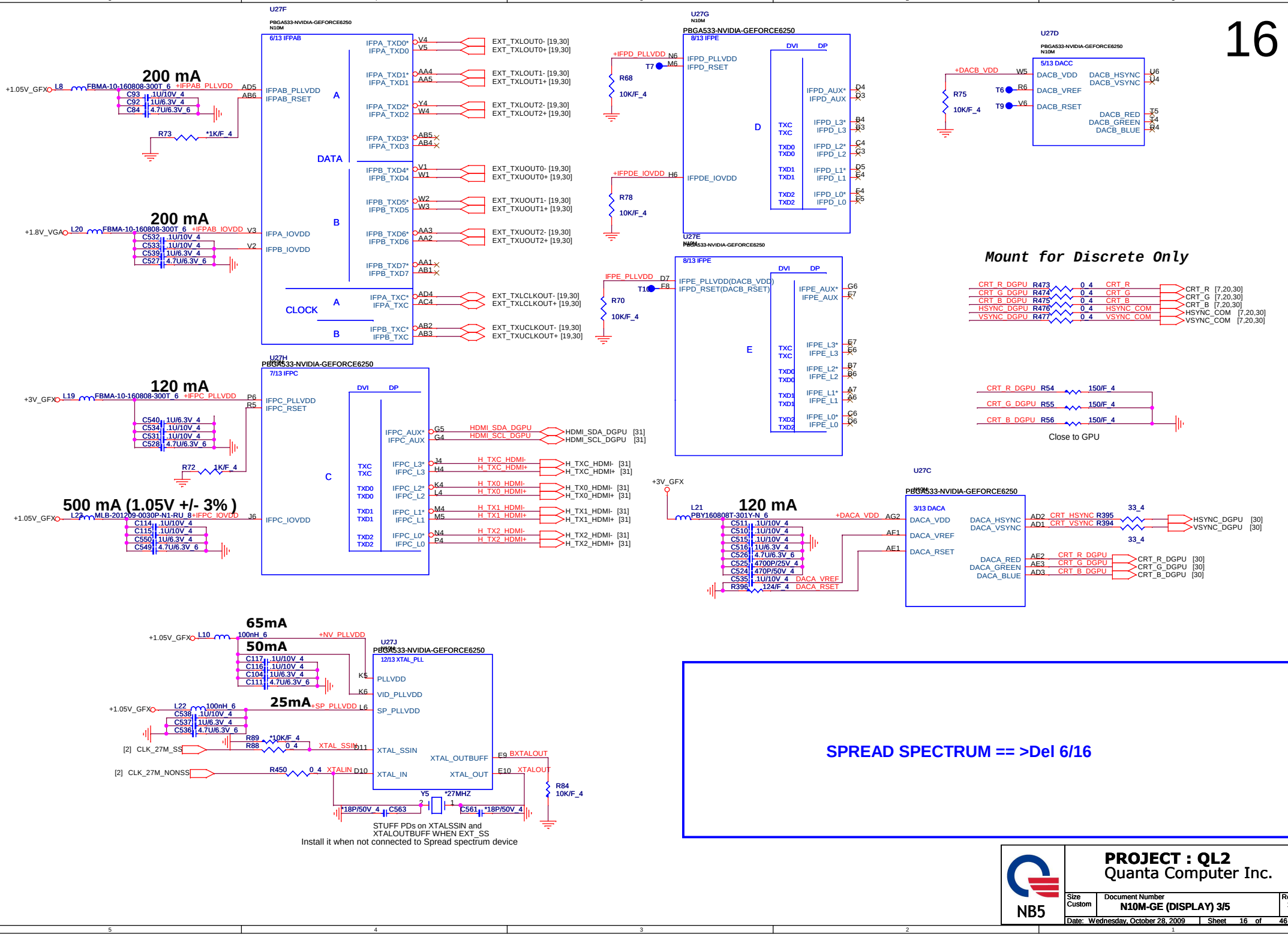

U27B
PBGA533-NVIDIA-GEFORCE6250
N10M
2/13 FRAME_BUFFER
1.63A
+1.5V_GFX
C172 0.047U/16V_4
C159 0.047U/16V_4
C179 0.047U/16V_4
C151 .1U/10V_4
C148 .1U/10V_4
C164 .1U/10V_4
C173 4.7U/6.3V_6
FBVDDQ_01 A13
FBVDDQ_02 B13
FBVDDQ_03 C13
FBVDDQ_04 D13
FBVDDQ_05 D14
FBVDDQ_06 E13
FBVDDQ_07 F13
FBVDDQ_08 F14
FBVDDQ_09 F15
FBVDDQ_10 F16
FBVDDQ_11 F17
FBVDDQ_12 F19
FBVDDQ_13 F22
FBVDDQ_14 H23
FBVDDQ_15 H26
FBVDDQ_16 J15
FBVDDQ_17 J16
FBVDDQ_18 J18
FBVDDQ_19 J19
FBVDDQ_20 L19
FBVDDQ_21 L23
FBVDDQ_22 L26
FBVDDQ_23 M19
FBVDDQ_24 N22
FBVDDQ_25 U22
FBVDDQ_26 Y22
[18] FBA_CMD0 F26 FBA_CMD0
[18] FBA_CMD1 J24 FBA_CMD1
[18] FBA_CMD2 F25 FBA_CMD2
[18] FBA_CMD3 M23 FBA_CMD3
[18] FBA_CMD4 N27 FBA_CMD4
[18] FBA_CMD5 M27 FBA_CMD5
[18] FBA_CMD6 K26 FBA_CMD6
[18] FBA_CMD7 J25 FBA_CMD7
[18] FBA_CMD8 J27 FBA_CMD8
[18] FBA_CMD9 G23 FBA_CMD9
[18] FBA_CMD10 G26 FBA_CMD10
[18] FBA_CMD11 J23 FBA_CMD11
[18] FBA_CMD12 M25 FBA_CMD12
[18] FBA_CMD13 K27 FBA_CMD13
[18] FBA_CMD14 G25 FBA_CMD14
[18] FBA_CMD15 L24 FBA_CMD15
[18] FBA_CMD16 K23 FBA_CMD16
[18] FBA_CMD17 K24 FBA_CMD17
[18] FBA_CMD18 G22 FBA_CMD18
[18] FBA_CMD19 K25 FBA_CMD19
[18] FBA_CMD20 H22 FBA_CMD20
[18] FBA_CMD21 M26 FBA_CMD21
[18] FBA_CMD22 H24 FBA_CMD22
[18] FBA_CMD23 F27 FBA_CMD23
[18] FBA_CMD24 J26 FBA_CMD24
[18] FBA_CMD25 G24 FBA_CMD25
[18] FBA_CMD26 G27 FBA_CMD26
[18] FBA_CMD27 M24 FBA_CMD27
[18] FBA_CMD28 K22 FBA_CMD28
[18] FBA_CMD29 J22 FBA_CMD29
[18] FBA_CMD30 L22 FBA_CMD30
[18] VMA_CLK0 VMA_CLK0 F24 FBA_CLK0
[18] VMA_CLK0# VMA_CLK0# F23 FBA_CLK0*
[18] VMA_CLK1 VMA_CLK1 N24 FBA_CLK1
[18] VMA_CLK1# VMA_CLK1# N23 FBA_CLK1*
+1.5V_GFX R101 40.2/F_4 FB_CAL_PD_VDDQ B15 FB_CAL_PD_VDDQ
R99 40.2/F_4 FB_CAL_PU_GND A15 FB_CAL_PU_GND
R102 60.4/F_4 FB_CAL_TERM_GND B16 FB_CAL_TERM_GND
+1.5V_GFX *60.4/F_4 R114 FBA_DEBUG M22 FBA_DEBUG
For debug only
10mA
+1.05V_GFX
15mils width
25mA
L27 PBY160808T-301Y-N_6 +FB_PLLAVDD R19 FB_PLLAVDD
C574 4.7U/6.3V_6
C577 1U/6.3V_4 T19 FB_DLLAVDD
C175 .1U/10V_4 AC19 FB_PLLAVDD (NC)
(DQM1) FBA_DQM0 C26 VMA_DM0
(DQM3) FBA_DQM1 B19 VMA_DM1
(DQM2) FBA_DQM2 D19 VMA_DM2
(DQM0) FBA_DQM3 D23 VMA_DM3
(DQM4) FBA_DQM4 T24 VMA_DM4
(DQM5) FBA_DQM5 AA23 VMA_DM5
(DQM7) FBA_DQM6 AB27 VMA_DM6
(DQM5) FBA_DQM7 T26 VMA_DM7
(WP1) FBA_DQS_WP0 C25 VMA_WDQS0
(WP3) FBA_DQS_WP1 A19 VMA_WDQS1
(WP2) FBA_DQS_WP2 E19 VMA_WDQS2
(WP0) FBA_DQS_WP3 A24 VMA_WDQS3
(WP4) FBA_DQS_WP4 T22 VMA_WDQS4
(WP6) FBA_DQS_WP5 AA24 VMA_WDQS5
(WP7) FBA_DQS_WP5 AA26 VMA_WDQS6
(WP5) FBA_DQS_WP7 T27 VMA_WDQS7
(RN1) FBA_DQS_RN0 D25 VMA_RDQS0
(RN3) FBA_DQS_RN1 A18 VMA_RDQS1
(RN2) FBA_DQS_RN2 E18 VMA_RDQS2
(RN0) FBA_DQS_RN3 B24 VMA_RDQS3
(RN4) FBA_DQS_RN4 R22 VMA_RDQS4
(RN6) FBA_DQS_RN5 Y24 VMA_RDQS5
(RN7) FBA_DQS_RN6 AA27 VMA_RDQS6
(RN5) FBA_DQS_RN7 R27 VMA_RDQS7
FB_VREF A16 +FB_VREF1 TP6
FBA_DD0 (FBA_D8) FBA_D0 D22 VMA_DQ0
(FBA_D10) FBA_D1 E24 VMA_DQ1
(FBA_D9) FBA_D2 E22 VMA_DQ2
(FBA_D11) FBA_D3 D24 VMA_DQ3
(FBA_D12) FBA_D4 D26 VMA_DQ4
(FBA_D13) FBA_D5 D27 VMA_DQ5
(FBA_D14) FBA_D6 C27 VMA_DQ6
(FBA_D15) FBA_D7 B27 VMA_DQ7
(FBA_D31) FBA_D8 A21 VMA_DQ8
(FBA_D30) FBA_D9 B21 VMA_DQ9
(FBA_D29) FBA_D10 C21 VMA_DQ10
(FBA_D28) FBA_D11 C19 VMA_DQ11
(FBA_D26) FBA_D14 C18 VMA_DQ12
(FBA_D27) FBA_D14 D18 VMA_DQ13
(FBA_D25) FBA_D14 B18 VMA_DQ14
(FBA_D24) FBA_D15 C16 VMA_DQ15
(FBA_D22) FBA_D16 E21 VMA_DQ16
(FBA_D23) FBA_D17 F21 VMA_DQ17
(FBA_D20) FBA_D18 D20 VMA_DQ18
(FBA_D21) FBA_D19 F20 VMA_DQ19
(FBA_D18) FBA_D20 D17 VMA_DQ20
(FBA_D19) FBA_D21 F18 VMA_DQ21
(FBA_D16) FBA_D22 D16 VMA_DQ22
(FBA_D17) FBA_D23 E16 VMA_DQ23
(FBA_D3) FBA_D24 A22 VMA_DQ24
(FBA_D4) FBA_D25 C24 VMA_DQ25
(FBA_D0) FBA_D26 D21 VMA_DQ26
(FBA_D2) FBA_D27 B22 VMA_DQ27
(FBA_D1) FBA_D28 C22 VMA_DQ28
(FBA_D6) FBA_D29 A25 VMA_DQ29
(FBA_D5) FBA_D30 B25 VMA_DQ30
(FBA_D7) FBA_D31 A26 VMA_DQ31
(FBA_D37) FBA_D32 U24 VMA_DQ32
(FBA_D39) FBA_D33 V24 VMA_DQ33
(FBA_D38) FBA_D35 V23 VMA_DQ34
(FBA_D35) FBA_D35 R24 VMA_DQ35
(FBA_D36) FBA_D36 T23 VMA_DQ36
(FBA_D34) FBA_D37 R23 VMA_DQ37
(FBA_D33) FBA_D38 P24 VMA_DQ38
(FBA_D32) FBA_D39 P22 VMA_DQ39
(FBA_D55) FBA_D40 AC24 VMA_DQ40
(FBA_D53) FBA_D41 AB23 VMA_DQ41
(FBA_D54) FBA_D42 AB24 VMA_DQ42
(FBA_D51) FBA_D43 W24 VMA_DQ43
(FBA_D52) FBA_D44 AA22 VMA_DQ44
(FBA_D50) FBA_D45 W23 VMA_DQ45
(FBA_D49) FBA_D46 W22 VMA_DQ46
(FBA_D48) FBA_D47 V22 VMA_DQ47
(FBA_D59) FBA_D48 AA25 VMA_DQ48
(FBA_D58) FBA_D49 W27 VMA_DQ49
(FBA_D57) FBA_D50 W26 VMA_DQ50
(FBA_D56) FBA_D51 W25 VMA_DQ51
(FBA_D60) FBA_D52 AB25 VMA_DQ52
(FBA_D61) FBA_D53 AB26 VMA_DQ53
(FBA_D62) FBA_D54 AD26 VMA_DQ54
(FBA_D63) FBA_D55 AD27 VMA_DQ55
(FBA_D46) FBA_D56 V25 VMA_DQ56
(FBA_D42) FBA_D57 R25 VMA_DQ57
(FBA_D45) FBA_D58 V26 VMA_DQ58
(FBA_D47) FBA_D59 V27 VMA_DQ59
(FBA_D43) FBA_D60 R26 VMA_DQ60
(FBA_D44) FBA_D61 T25 VMA_DQ61
(FBA_D40) FBA_D62 N25 VMA_DQ62
(FBA_D41) FBA_D63 N26 VMA_DQ63
[18] VMA_DQ[63..0]
[18] VMA_DM[7..0]
[18] VMA_WDQS[7..0]
[18] VMA_RDQS[7..0]
FBA_CMD28 R547 10K/F_4
FBA_CMD7 R226 10K/F_4
FBA_CMD15 R546 10K/F_4
FBA_CMD18 R223 10K/F_4
FBA_CMD30 R222 10K/F_4
U27I
N10M
PBGA533-NVIDIA-GEFORCE6250
13/13 GND_NC
NC_01 C15
NC_02 D15
NC_03 J5
AC11 GND_01
AC14 GND_02
AC17 GND_03
AC2 GND_04
AC20 GND_05
AC23 GND_06
AC26 GND_07
AC5 GND_08
AC8 GND_09
AE11 GND_10
AE14 GND_11
AE17 GND_12
AE2 GND_13
AE20 GND_14
AE23 GND_15
AE26 GND_16
AE5 GND_17
AE8 GND_18
B11 GND_19
B14 GND_20
B17 GND_21
B2 GND_22
B20 GND_23
B23 GND_24
B26 GND_25
B5 GND_26
B8 GND_27
E11 GND_28
E17 GND_30
E2 GND_31
E20 GND_32
E23 GND_33
E26 GND_34
E5 GND_35
E8 GND_36
H2 GND_37
H5 GND_38
J11 GND_39
J14 GND_40
J17 GND_41
K19 GND_42
K9 GND_43
L11 GND_44
L12 GND_45
L13 GND_46
L14 GND_47
L15 GND_48
L16 GND_49
L17 GND_50
L2 GND_51
L5 GND_52
M12 GND_53
M13 GND_54
M14 GND_55
M15 GND_56
M16 GND_57
P19 GND_58
P2 GND_59
P23 GND_60
P26 GND_61
P5 GND_62
P9 GND_63
T12 GND_64
T13 GND_65
T14 GND_66
T15 GND_67
T16 GND_68
U11 GND_69
U12 GND_70
U13 GND_71
U14 GND_72
U15 GND_73
U16 GND_74
U17 GND_75
U2 GND_76
U23 GND_77
U26 GND_78
U5 GND_79
V19 GND_80
V9 GND_81
W11 GND_82
W14 GND_83
W17 GND_84
Y2 GND_85
Y23 GND_86
Y26 GND_87
Y5 GND_88
PROJECT : QL2
Quanta Computer Inc.
NB5
Size Custom
Document Number N10M-GE (MEMORY I/F) 2/5
Rev 1A
Date: Monday, October 26, 2009
Sheet 15 of 46



NB5	PROJECT : QL2 Quanta Computer Inc.	
Size: Custom	Document Number: N10M-GE (DISPLAY) 3/5	Rev: 1A
Date: Wednesday, October 28, 2009	Sheet 16 of 46	

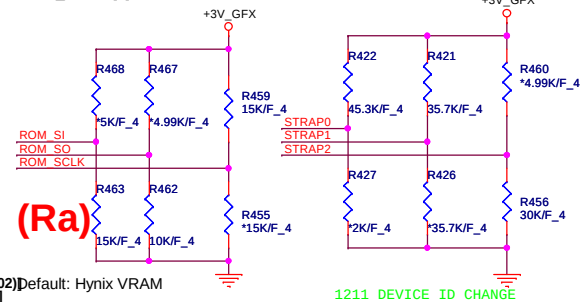
CHIP	PCI_DEVID:	STRAP2
N11P-GE1	0x0A29	1001 PU 10K
N11M-GE1	0x0A75	1010 PD 30K

SEE Datasheet for details on N10P Straps!

Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

PCI_DEVID[4]/SUBVENDOR



1211 DEVICE ID CHANGE

4.99K/F_4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)] Default: Hynix VRAM
10K/F_4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
15K/F_4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
30.1K/F_4: CS33012FB18 [RES CHIP 30.1K 1/16W +-1%(0402)]
35.7K/F_4: CS33572FB13 [RES CHIP 35.7K 1/16W +-1%(0402)]
45.3K/F_4: CS34532FB18 [RES CHIP 45.3K 1/16W +-1% (0402)]

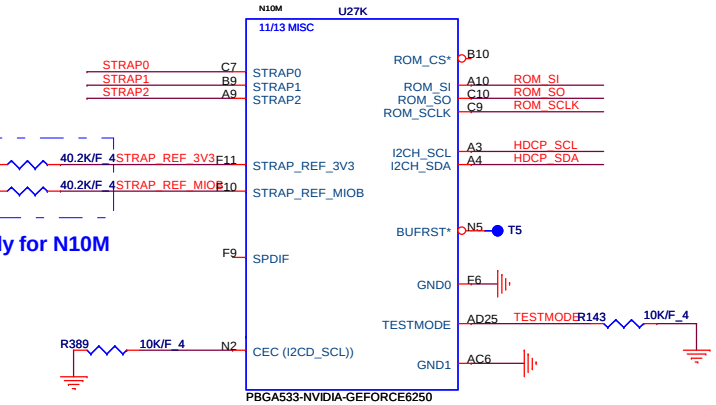
	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1000
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

VRAM Configuration Table

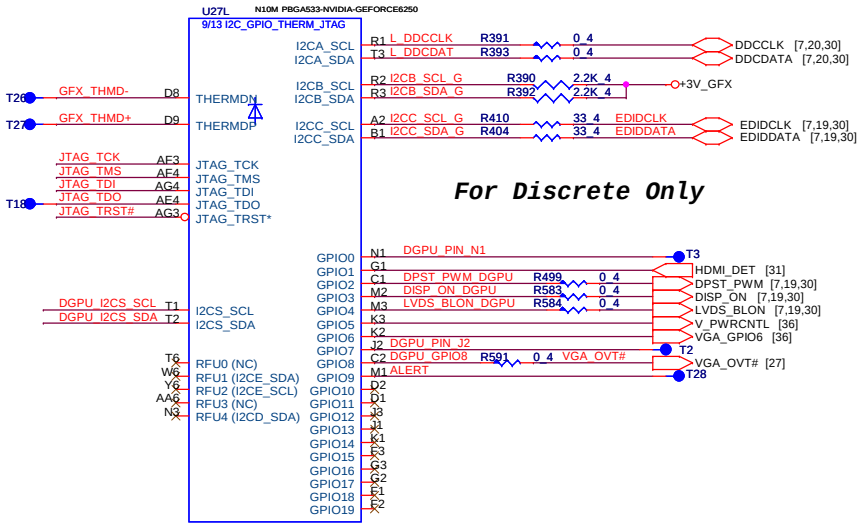
RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000		Reserved		
0001	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Qimonda	IDGH1G-04A1F1C-16X	PD 10K
0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix	H5TQ1G63BFR-12C	PD 15K
0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung	K4W1G1646E-EC12	PD 20K
0101		Reserved		
0110				
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Hynix	H5TQ1G63AFR-14C	
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Samsung	K4W1G1646D-EC12	

AKD58GGT^01
AKD5LZGTW00
AKD5LGGT502

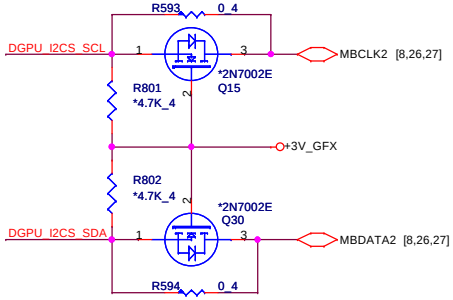
(Ra)



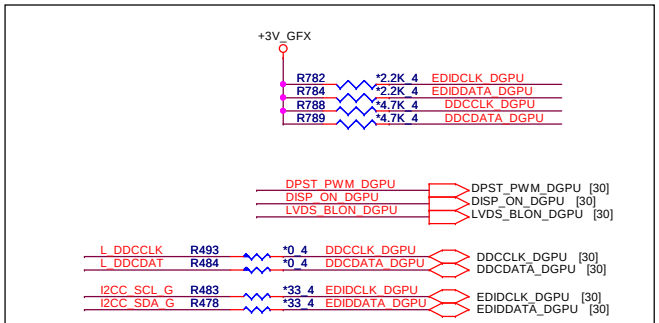
Only for N10M



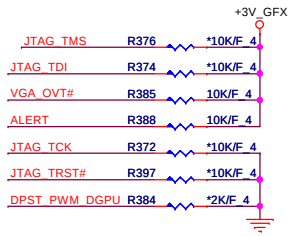
For Discrete Only



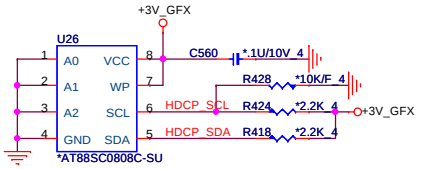
Mount Q15 , Q30 , R801 , R802
For Switchable only



For Switchable only



HDCP ROM



DHCP ROM	
HDCP_SCL	Low: Crypto ROM Hi: I2C ROM

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2 11/13
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL 11/13
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

NB5

PROJECT : QL2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N10M-GE (GPIO&STRAPS) 4/5	1A
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CHANNEL A: 256MB/512MB DDR3

[15] VMA_DQ[63..0]
[15] VMA_DM[7..0]
[15] VMA_WDQS[7..0]
[15] VMA_RDQS[7..0]

U11 — VRAM _DDR3 — 96-BALL SDRAM DDR3 — 3/27 Swap
U30 — VRAM _DDR3 — 96-BALL SDRAM DDR3 — 3/27 Swap
U12 — VRAM _DDR3 — 96-BALL SDRAM DDR3 — 3/27 Swap
U31 — VRAM _DDR3 — 96-BALL SDRAM DDR3 — 3/27 Swap

Should be 240 Ohms +-1%
R166 243/F_4
R543 243/F_4
R231 243/F_4
R507 243/F_4

11/12 VMA_WDQS2 VMA_RDQS2 DQSL DQSL
11/12 VMA_WDQS0 VMA_RDQS0 DQSU DQSU
3/27 Swap VMA_WDQS1 VMA_RDQS1 DQSL DQSL
3/27 Swap VMA_WDQS3 VMA_RDQS3 DQSU DQSU
11/17 Swap VMA_WDQS5 VMA_RDQS5 DQSL DQSL
11/17 Swap VMA_WDQS7 VMA_RDQS7 DQSL DQSL

+1.5V_GFX

2/19 VMA_CLK0 R216 243/F_4 VMA_CLK0#
2/19 VMA_CLK1 R217 243/F_4 VMA_CLK1#

11/11 +1.5V_GFX R545 1.33K/F_4 VREFC_VMA1 R544 1.33K/F_4 C602 .1U/10V_4
11/11 +1.5V_GFX R220 1.33K/F_4 VREFD_VMA1 R221 1.33K/F_4 C309 .1U/10V_4
11/11 +1.5V_GFX R224 1.33K/F_4 VREFC_VMA3 R225 1.33K/F_4 C317 .1U/10V_4
11/11 +1.5V_GFX R549 1.33K/F_4 VREFD_VMA3 R548 1.33K/F_4 C607 .1U/10V_4

+1.5V_GFX C604 C585 C584 C601 1U/6.3V_4
+1.5V_GFX C318 C298 C610 C315 C316 C314 10U/6.3V_6S .1U/10V_4
+1.5V_GFX C603 C313 C609 C596 C598 C611 C608 C595 .1U/10V_4
+1.5V_GFX C599 C605 C597 C606 C612 C600 C308 C613 .1U/10V_4
+1.5V_GFX C311 C295 C310 C312 .1U/10V_4

1211 for Nvidia request add transition cap

[15,30,40] +1.5V_GFX

NB5

PROJECT : QL2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N10M-GE VRAM-1(DDR3 BGA96	1A
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1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B

OPTION SIGNAL FROM NB FOR UMA VGA

[7,30] LA_CLK	RP8	*4P2R-S-0	TXLCLKOUT+
[7,30] LA_CLK#			TXLCLKOUT-
[7,30] LA_DATAP0	RP6	*4P2R-S-0	TXLOUT0+
[7,30] LA_DATAN0			TXLOUT0-
[7,30] LA_DATAP1	RP5	*4P2R-S-0	TXLOUT1+
[7,30] LA_DATAN1			TXLOUT1-
[7,30] LA_DATAP2	RP7	*4P2R-S-0	TXLOUT2+
[7,30] LA_DATAN2			TXLOUT2-
[7,30] LB_CLK#	RP1	*4P2R-S-0	TXUCLKOUT-
[7,30] LB_CLK			TXUCLKOUT+
[7,30] LB_DATAP0	RP4	*4P2R-S-0	TXUOUT0+
[7,30] LB_DATAN0			TXUOUT0-
[7,30] LB_DATAP1	RP2	*4P2R-S-0	TXUOUT1+
[7,30] LB_DATAN1			TXUOUT1-
[7,30] LB_DATAP2	RP3	*4P2R-S-0	TXUOUT2+
[7,30] LB_DATAN2			TXUOUT2-

OPTION SIGNAL FROM Nvidia to VGA

[16,30] EXT_TXLCLKOUT+	RP16	4P2R-S-0	TXLCLKOUT+
[16,30] EXT_TXLCLKOUT-			TXLCLKOUT-
[16,30] EXT_TXLOUT0-	RP14	4P2R-S-0	TXLOUT0-
[16,30] EXT_TXLOUT0+			TXLOUT0+
[16,30] EXT_TXLOUT1+	RP13	4P2R-S-0	TXLOUT1+
[16,30] EXT_TXLOUT1-			TXLOUT1-
[16,30] EXT_TXLOUT2+	RP15	4P2R-S-0	TXLOUT2+
[16,30] EXT_TXLOUT2-			TXLOUT2-
[16,30] EXT_TXUCLKOUT+	RP9	4P2R-S-0	TXUCLKOUT+
[16,30] EXT_TXUCLKOUT-			TXUCLKOUT-
[16,30] EXT_TXUOUT0+	RP12	4P2R-S-0	TXUOUT0+
[16,30] EXT_TXUOUT0-			TXUOUT0-
[16,30] EXT_TXUOUT1+	RP10	4P2R-S-0	TXUOUT1+
[16,30] EXT_TXUOUT1-			TXUOUT1-
[16,30] EXT_TXUOUT2+	RP11	4P2R-S-0	TXUOUT2+
[16,30] EXT_TXUOUT2-			TXUOUT2-

CN2

+3VLCD_CON
C13 1000P/50V_4
+3V
[7,17,30] EDIDCLK
[7,17,30] EDIDDATA
[30] TXLOUT0- TXLOUT0-
[30] TXLOUT0+ TXLOUT0+
[30] TXLOUT1- TXLOUT1-
[30] TXLOUT1+ TXLOUT1+
[30] TXLOUT2- TXLOUT2-
[30] TXLOUT2+ TXLOUT2+
[30] TXLCLKOUT- TXLCLKOUT-
[30] TXLCLKOUT+ TXLCLKOUT+
[30] TXUOUT0- TXUOUT0-
[30] TXUOUT0+ TXUOUT0+
[30] TXUOUT1- TXUOUT1-
[30] TXUOUT1+ TXUOUT1+
[30] TXUOUT2- TXUOUT2-
[30] TXUOUT2+ TXUOUT2+
[30] TXUCLKOUT- TXUCLKOUT-
[30] TXUCLKOUT+ TXUCLKOUT+
[7,17,30] DPST_PWM
[27] PWM_VADJ
R2 0_4
R1 *0_4
LCDBL_PWM
BLON_CON
C9 *4.7U/6.3V_6
C10 *.1U/10V_4
+VIN_BLIGHT
FOX-GS12401-1011

+5VSUS
14.5v
+15VALW
+3V
AO3404 ID current 5.8A
R16 330K_6
C23 .1U/10V_4
R17 100K/F_4
Q4 AO3404
+3VLCD
+3VLCD_CON
LCDONG
L5 PBY201209T-4A/08
C20 *.01U/25V_4
C19 .1U/10V_4
C28 *10U/6.3V_8
R15 22_8
Q6 2N7002E
C30 .027U/25V_6
LCDDISCHG
Q7 DTC144EUA
[7,17,30] DISP_ON
LCDON#
Q5 2N7002E

+3V
R7 2.2K_4 EDIDCLK
R6 2.2K_4 EDIDDATA
DISP_ON R18 100K/F_4
LVDS_BLON R13 100K/F_4

+VIN_BLIGHT
+VIN
L1 FBM2125 HM330-T +VIN_BLIGHT
C2 .1U/50V_6
C5 *10U/25V_12
C3 .1U/50V_6
C1 .01U/16V_4

R8 100K/F_4
C22 22P/50V_4
PN_BLON
BLON_CON
D2 RB500V-40
R10 47K_4
+3VPCU
Close to EC
[7,17,30] LVDS_BLON
R12 1K/F_4
D1 RB501V-40
D3 *RB501V-40
LID_EC# [26,27]
HWPG [3,27,32,33,34,36,37]
[10] LCD_BK
Q2 DTC144EUA

[2,3,7,8,9,10,11,12,13,20,21,22,23,24,25,26,27,28,29,30,31,32,35,38,40] +3V
[7,23,26,27,28,32,33,34,36,38,39,40] +3VPCU
[22,25,26,38] +5VSUS
[33,38] +15VALW
[2,32,33,34,35,36,37,38,39,40] +VIN

NB5

PROJECT : QL2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN	1A
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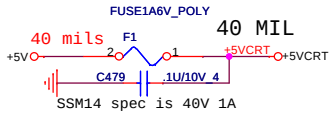
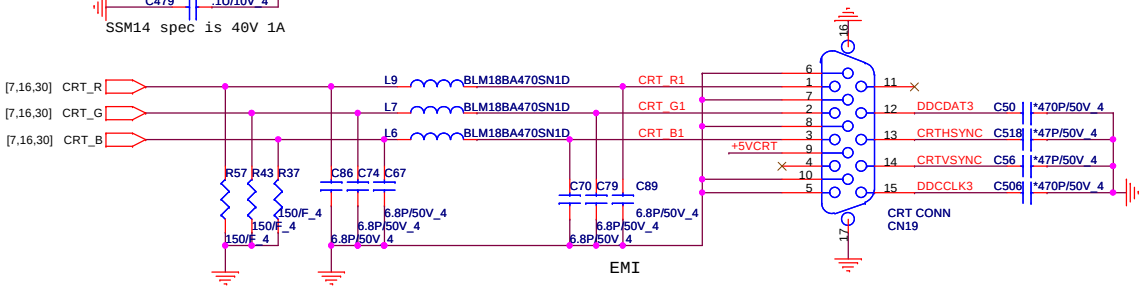
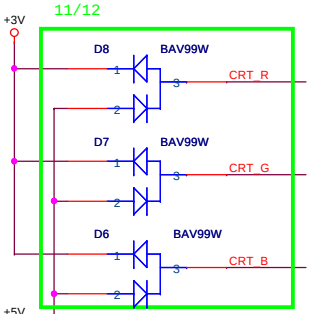
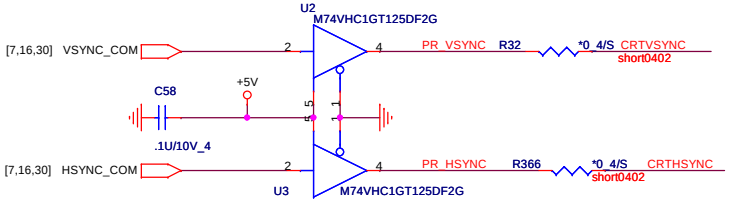
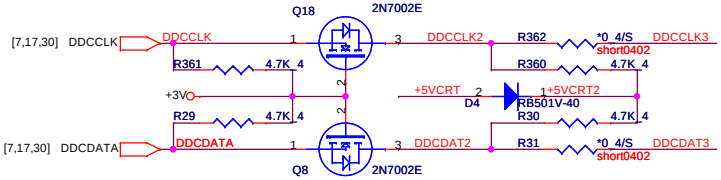
CRT PORT

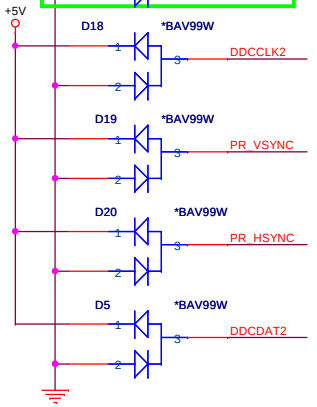










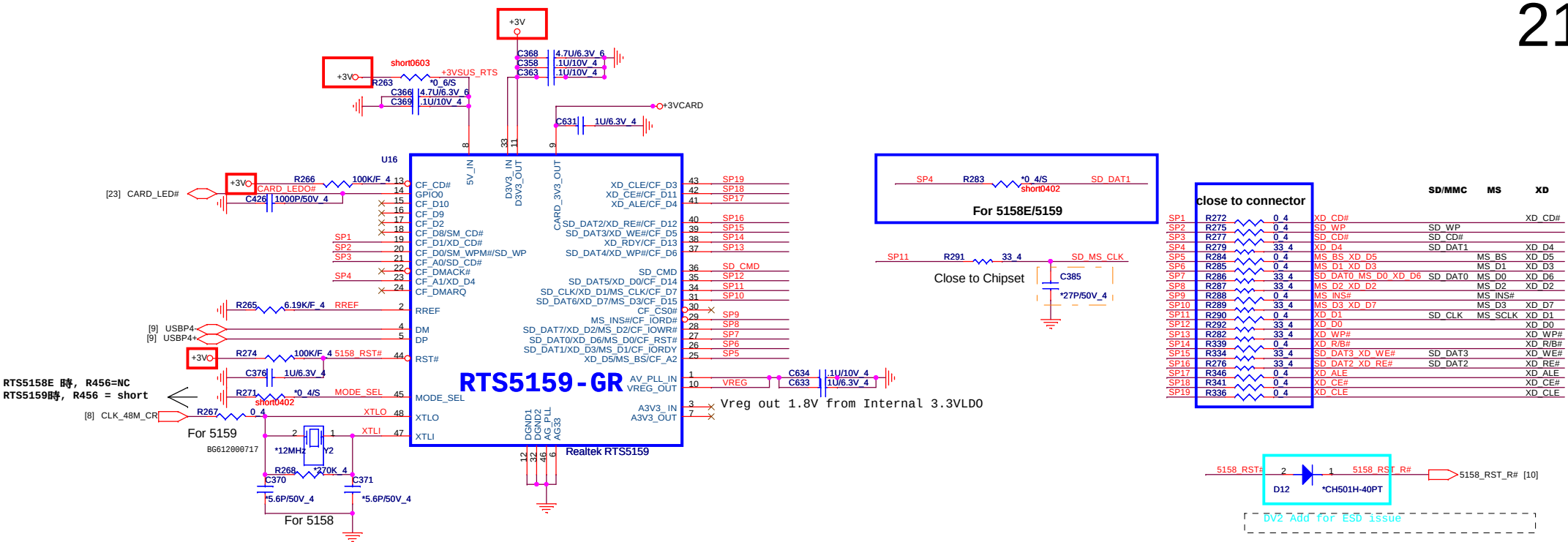


[2,3,7,8,9,10,11,12,13,19,21,22,23,24,25,26,27,28,29,30,31,32,35,38,40] +3V
[11,22,23,25,26,28,30,31,38] +5V

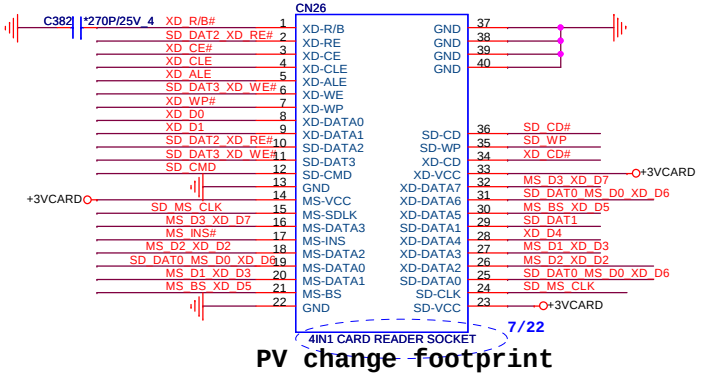
NB5

PROJECT : QL2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT/HDMI Conn	1A
Date: Monday, October 26, 2009	Sheet 20 of 46	

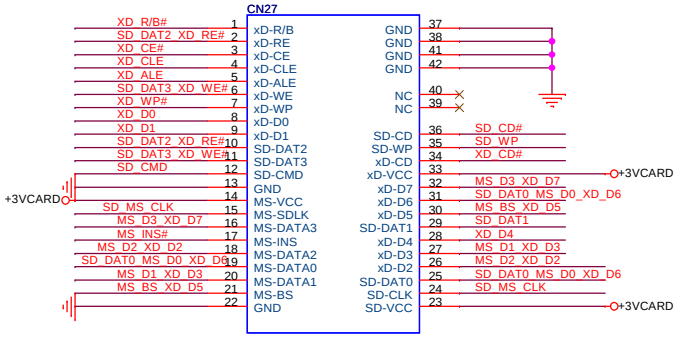


4 IN1 CARD READER
XD,MMC/SD,MS/MSP

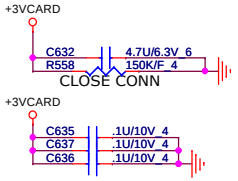


PV change footprint

DV2 add 2'nd source

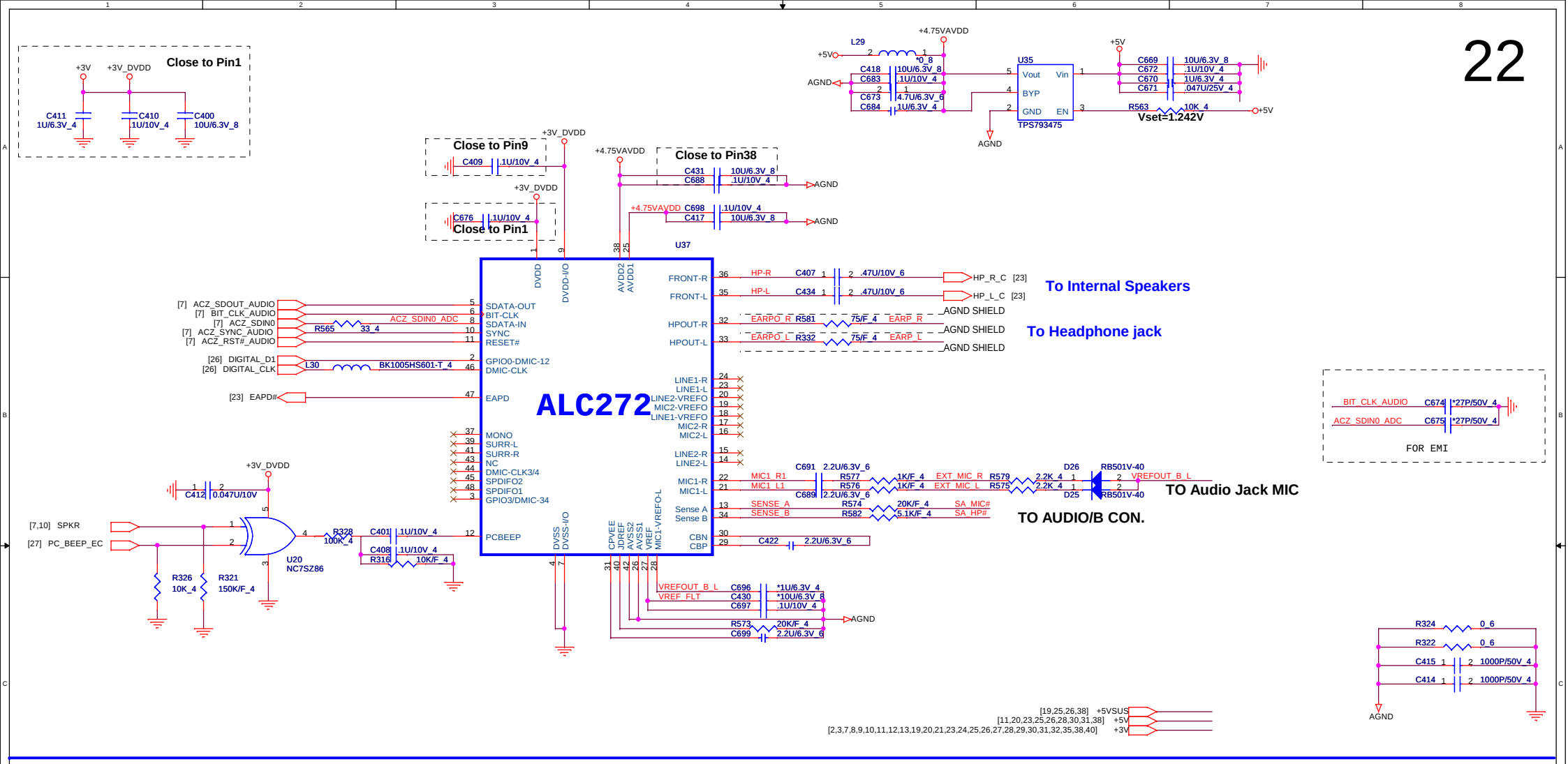


PV change footprint

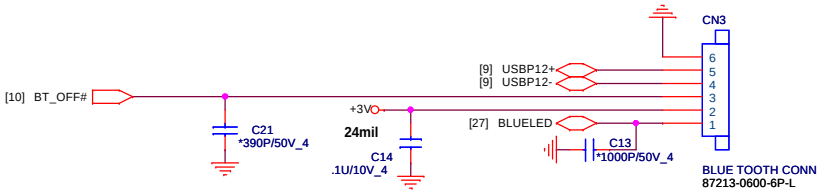


[2,3,7,8,9,10,11,12,13,19,20,22,23,24,25,26,27,28,29,30,31,32,35,38,40] +3V

PROJECT : QL2	
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: RTS5159 &CR SOCKET
Rev: 1A	
Date: Monday, October 26, 2009	Sheet 21 of 46

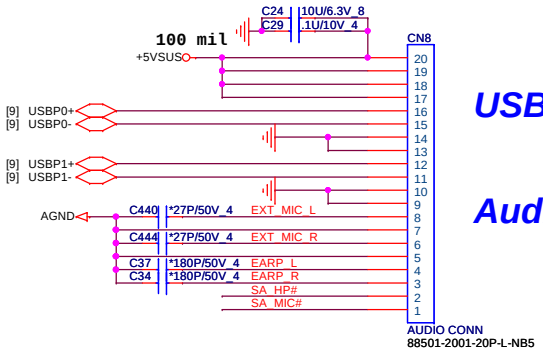


Bluetooth



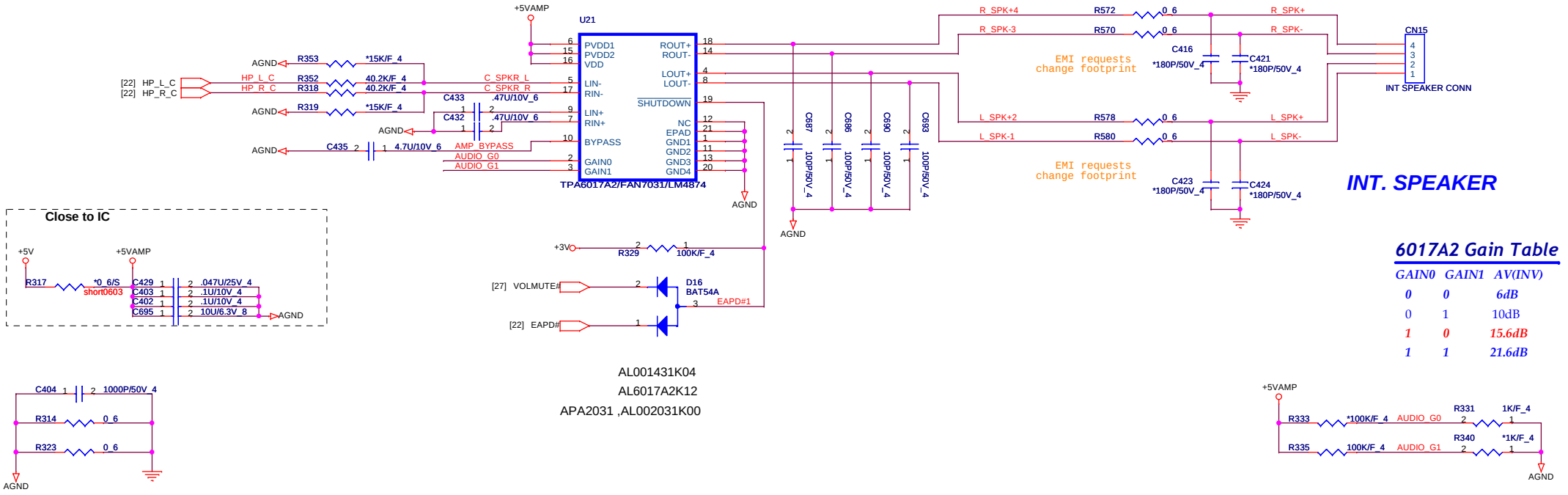
USB

Audio



NB5	PROJECT : QL2 Quanta Computer Inc.	
Size: Custom	Document Number: Azalia ALC272/BT CONN	Rev: 1A
Date: Thursday, October 29, 2009	Sheet 22 of 46	

AUDIO AMPLIFIER



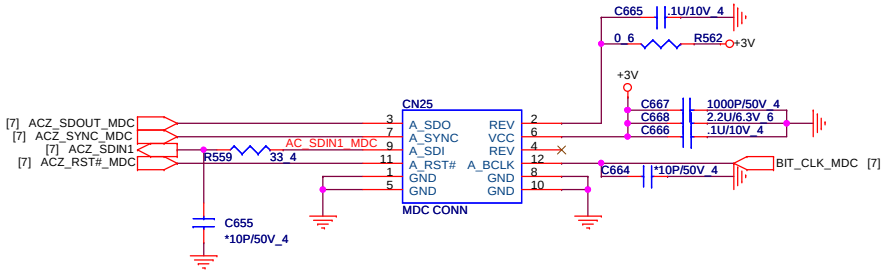
INT. SPEAKER

AL001431K04
AL6017A2K12
APA2031 ,AL002031K00

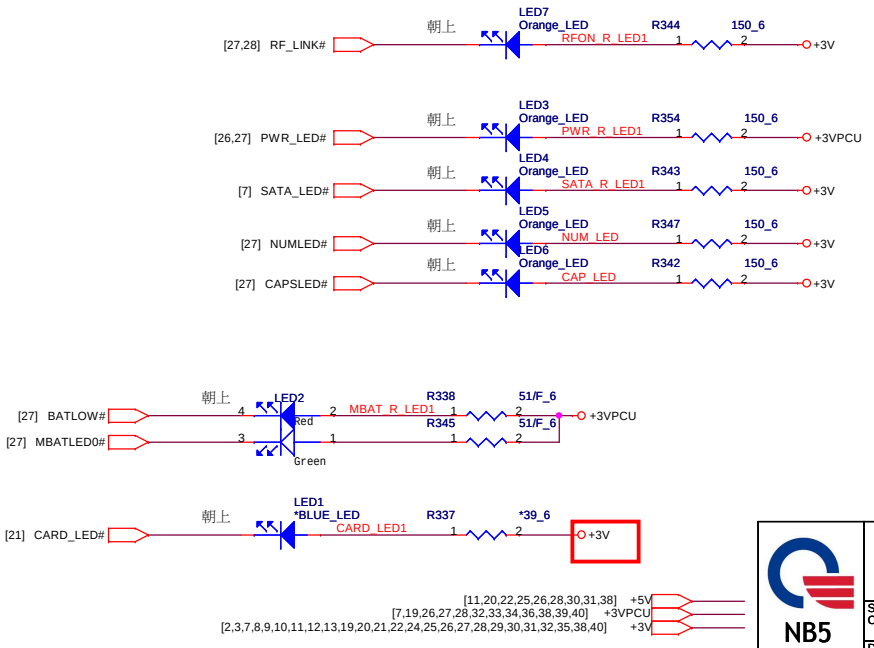
6017A2 Gain Table

GAIN0	GAIN1	AV(INV)
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

MDC CONNECTOR



LED

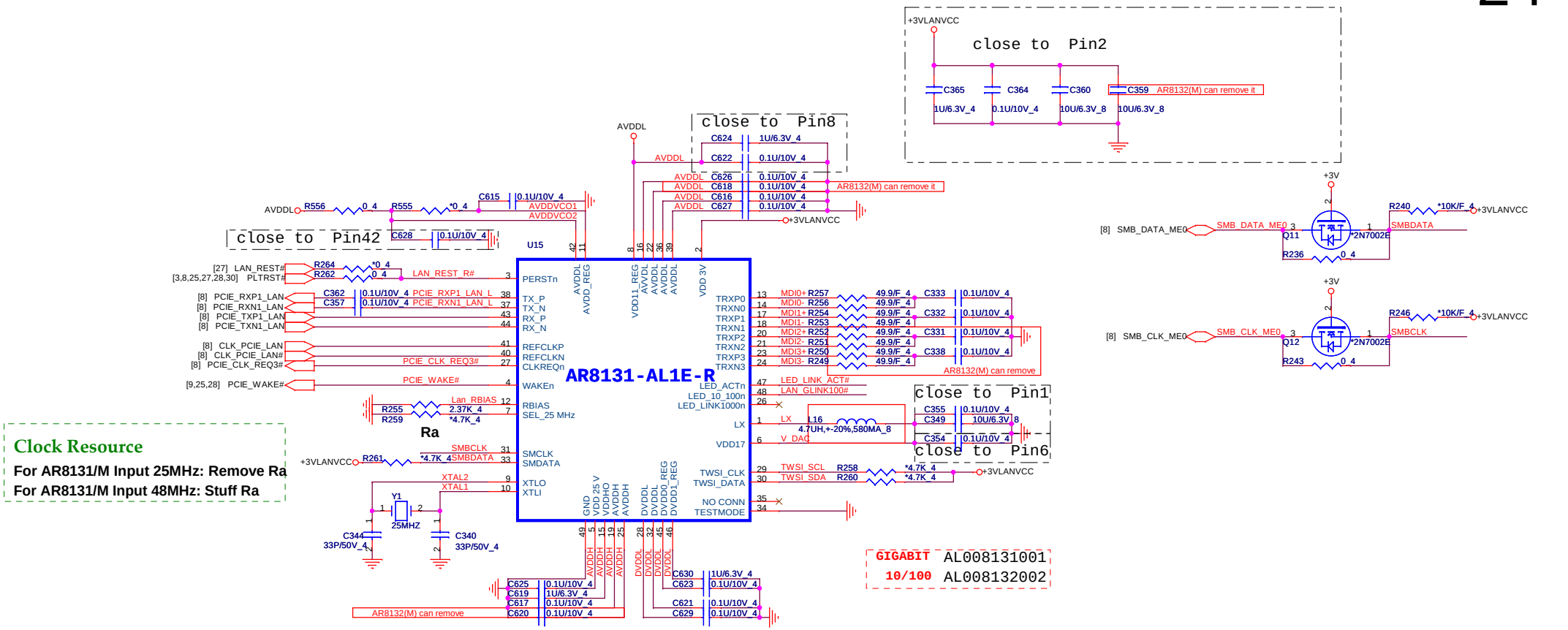


NB5

PROJECT : QL2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AMP_TPA6017/SPK/MDC/LED	1A

Date: Thursday, October 29, 2009 Sheet 23 of 46



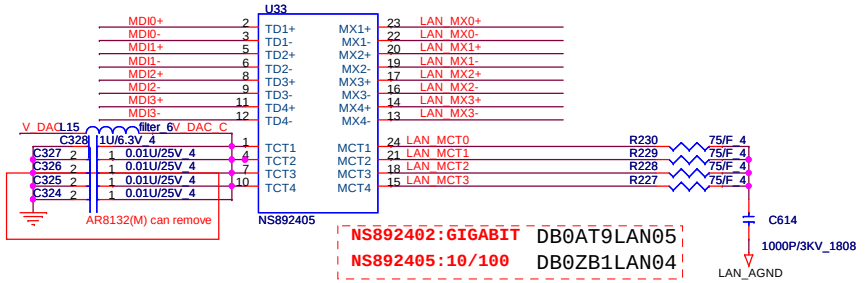
Clock Resource

For AR8131/M Input 25MHz: Remove Ra

For AR8131/M Input 48MHz: Stuff Ra

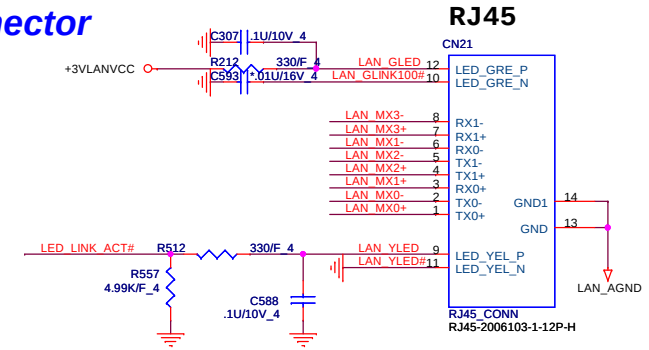
GIGABIT	AL008131001
10/100	AL008132002

Transformer for 10/100/1000



NS892402:GIGABIT	DB0AT9LAN05
NS892405:10/100	DB0ZB1LAN04

Lan Connector

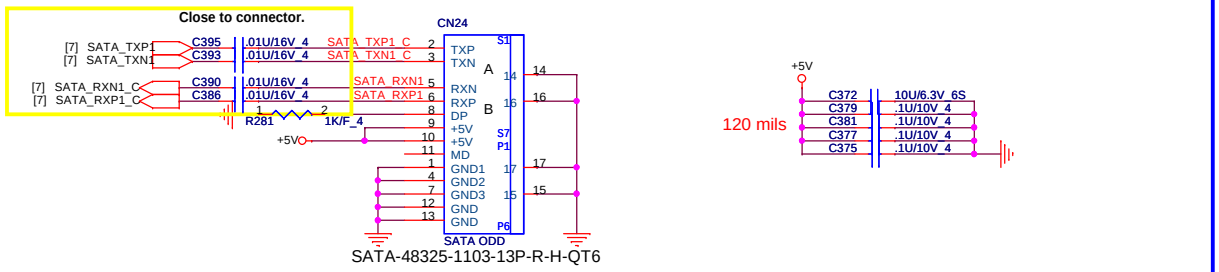


NB5

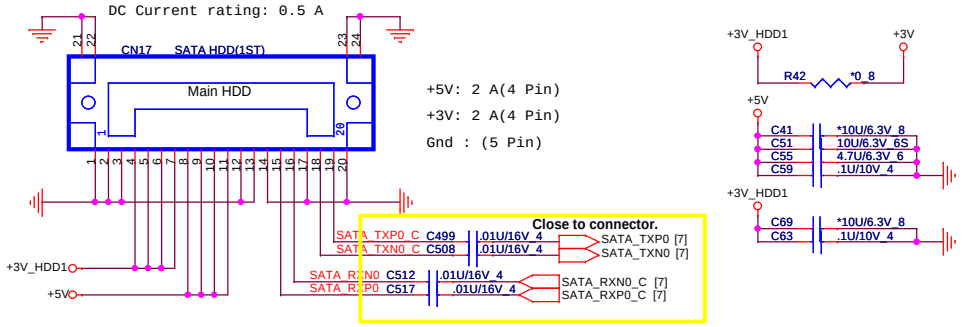
PROJECT : QL2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AR8131(M)/RJ45	1A
Date: Monday, October 26, 2009	Sheet 24 of 46	

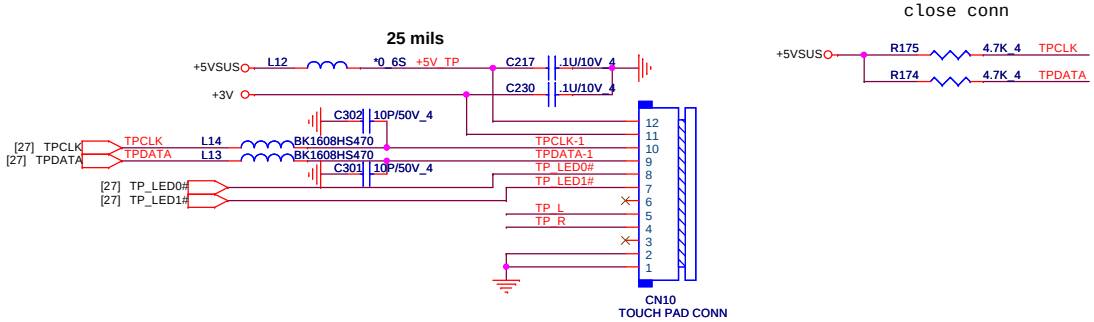
SATA ODD



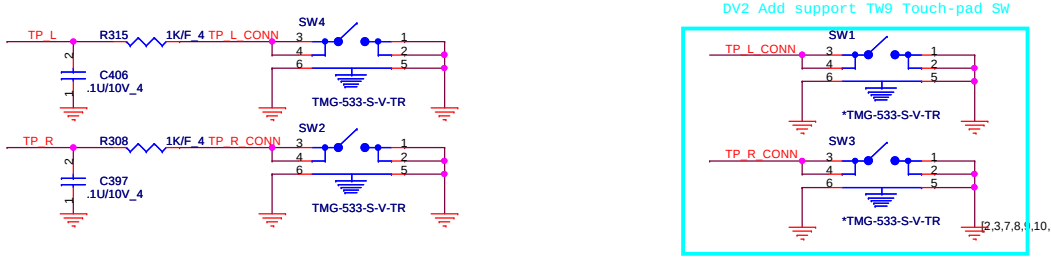
SATA_1 CONNECTOR



TOUCH PAD CONNECTOR

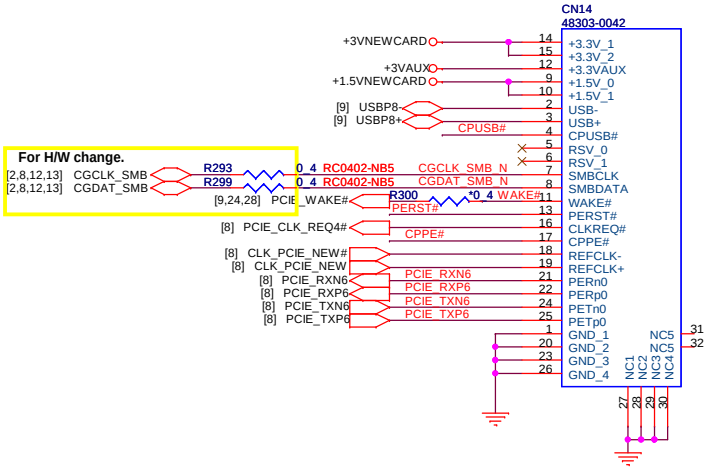


TOUCH PAD L/R SW2,SW4 in QL2 use, SW1,SW3 in SW9 use

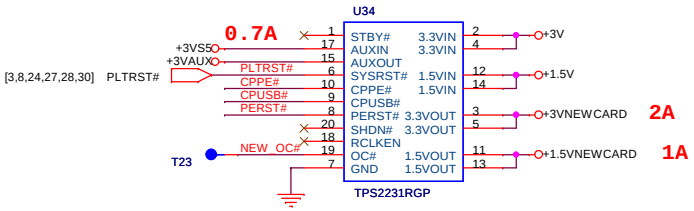


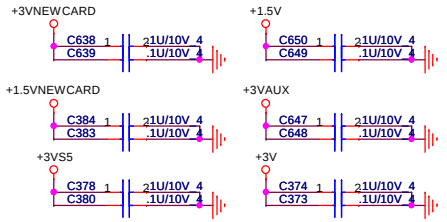
NEWCARD

NEWCARD (PCIEXPRESS*1 + USB*1)



Change CN15#31,32 as ME request for Hole pad
expcard-48303-0042-26p-l-qt6 as ME modify Pad size(pin31,32)
Move CN15#29,30 Pin as ME request(Molex confirm drawing)





[28,38] +1.5V
[2,3,7,8,9,10,11,12,13,19,20,21,22,23,24,26,27,28,29,30,31,32,35,38,40] +3V
[11,20,22,23,26,28,30,31,38] +5V
[19,22,26,38] +5VSUS

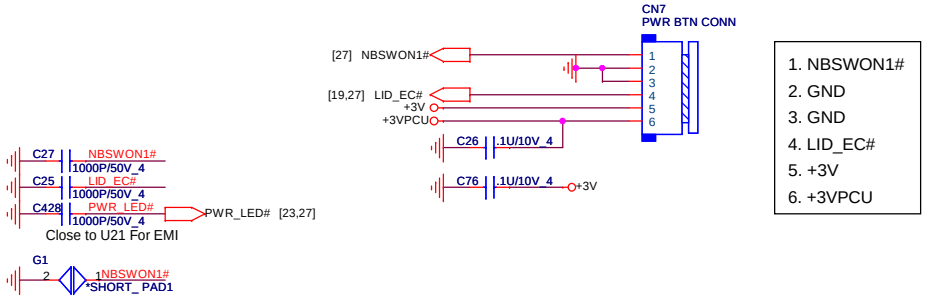
NB5

PROJECT : QL2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ODD/HDD/NEW CARD/TP	1A

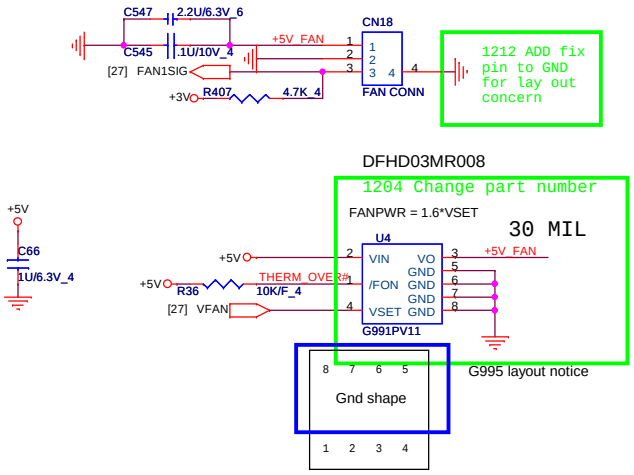
Date: Thursday, October 29, 2009 Sheet 25 of 46

POWER BOTTON CONNECT

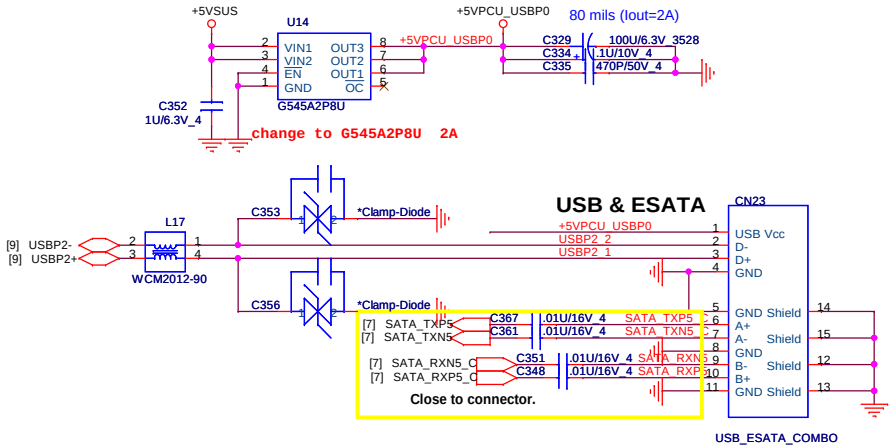


1. NBSWON1#
2. GND
3. GND
4. LID_EC#
5. +3V
6. +3VPCU

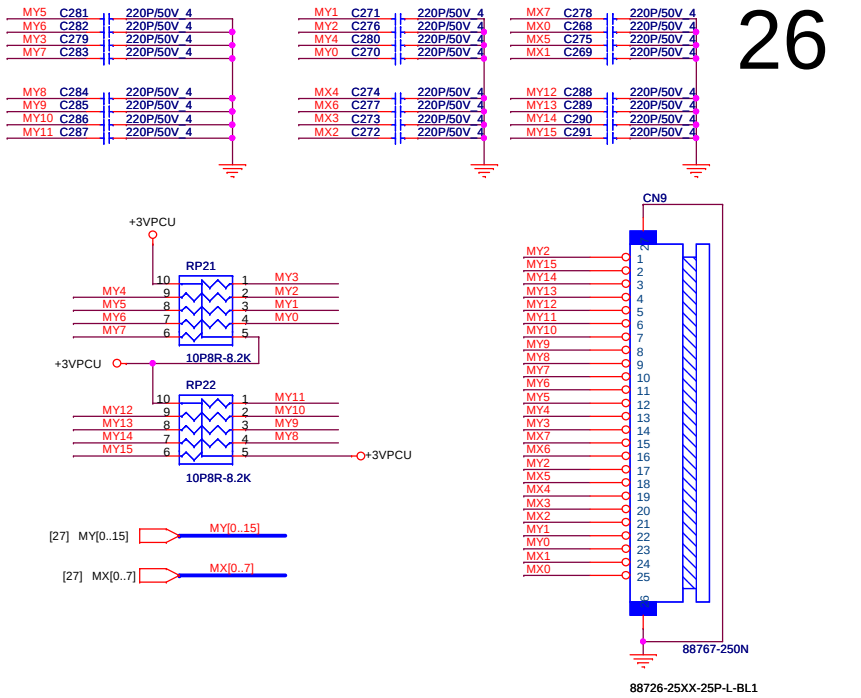
CPU FAN



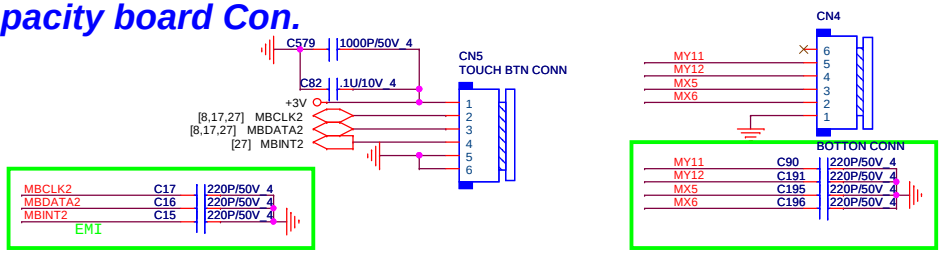
E-SATA/USB COMBO



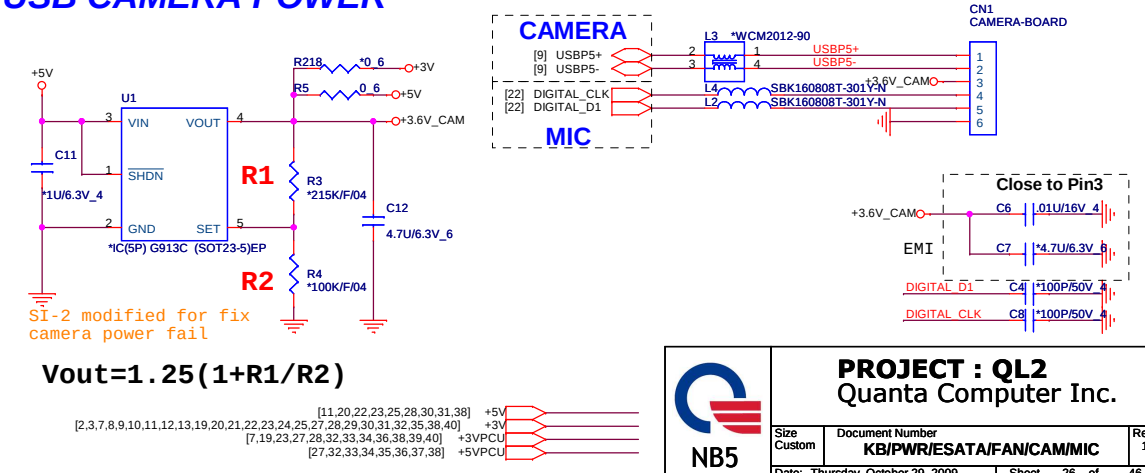
KEYBOARD Con.



Capacity board Con.



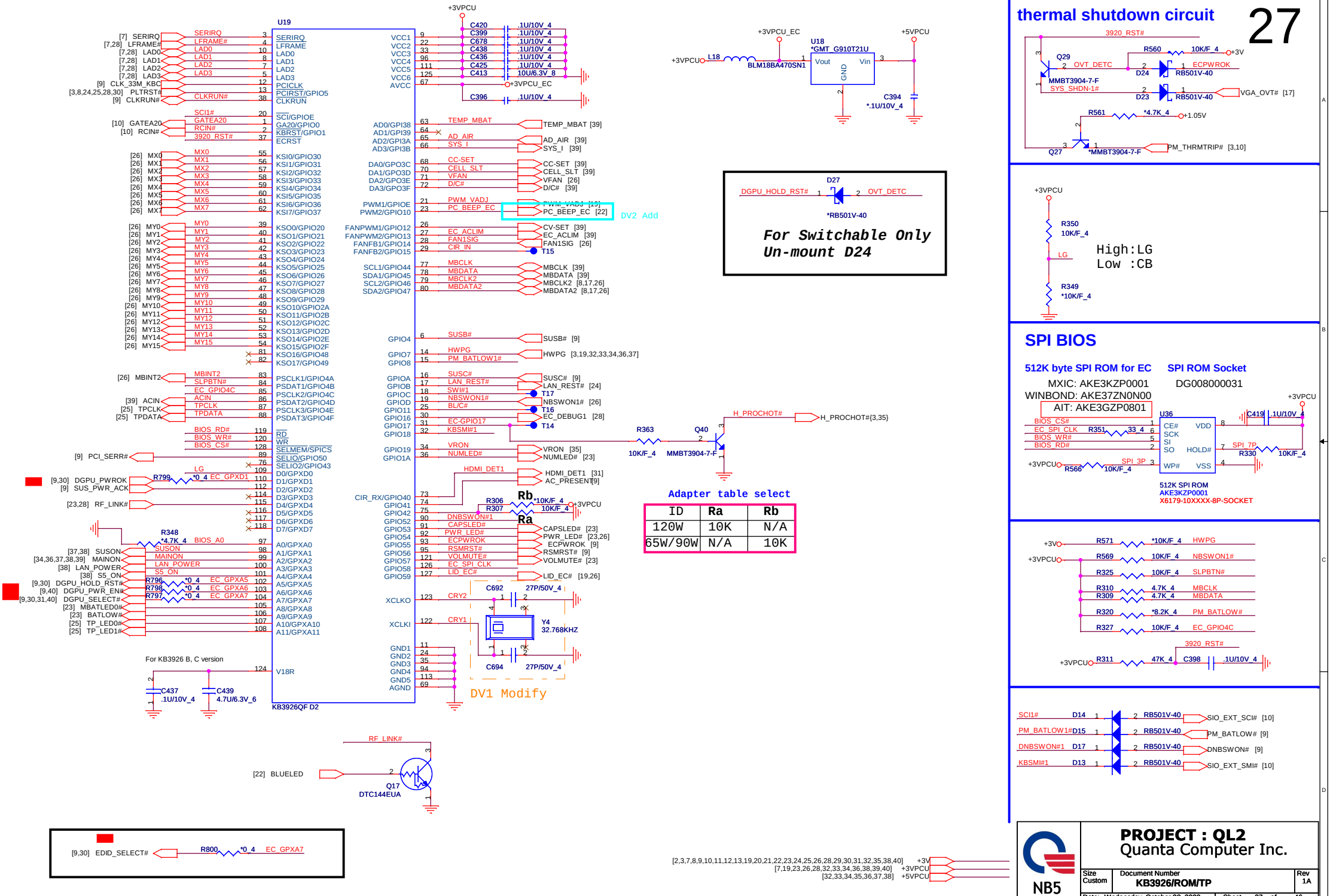
USB CAMERA POWER



NB5

PROJECT : QL2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB/PWR/ESATA/FAN/CAM/MIC	1A
Date: Thursday, October 29, 2009	Sheet 26 of 46	



thermal shutdown circuit

27

SPI BIOS

512K byte SPI ROM for EC

MXIC: AKE3KZP0001
WINBOND: AKE37ZN0N00
AIT: AKE3GZP0801

SPI ROM Socket

DG008000031

512K SPI ROM
AKE3KZP0001
X6179-10XXXX-8P-SOCKET

NB5

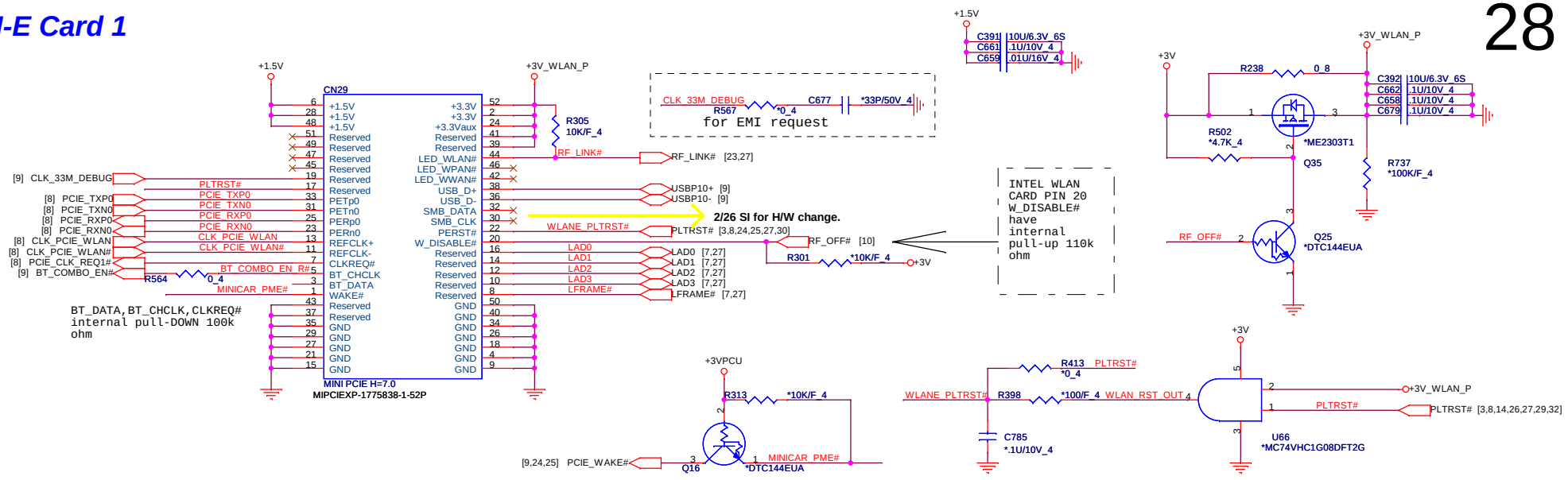
PROJECT : QL2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB3926/ROM/TP	1A

Date: Wednesday, October 28, 2009 Sheet 27 of 46

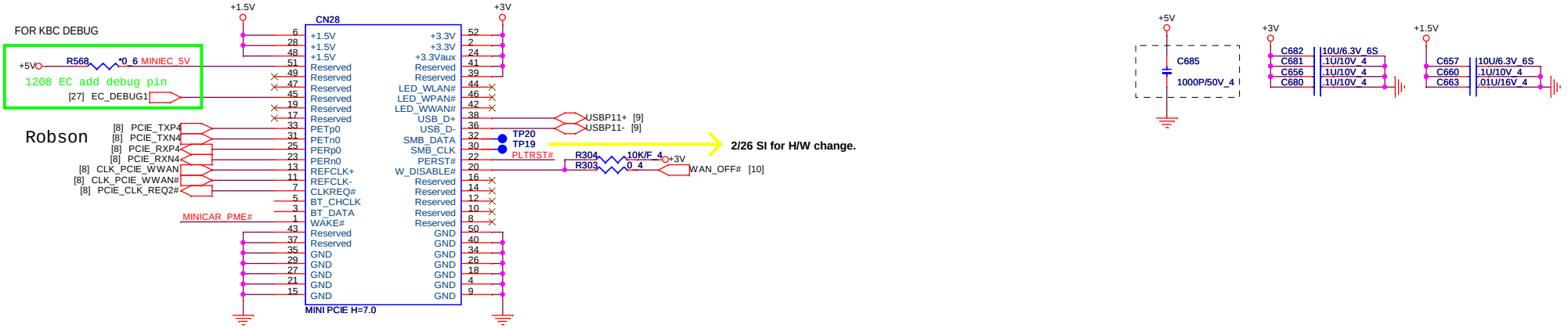
Mini PCI-E Card 1

WLAN



Mini PCI-E Card 2

Robson

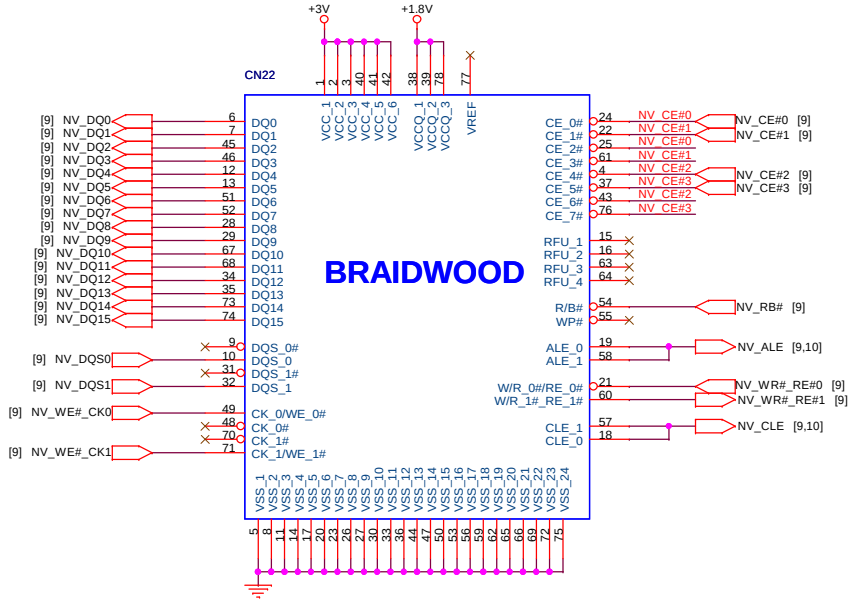


[25,38] +1.5V
[2,3,7,8,9,10,11,12,13,19,20,21,22,23,24,25,26,27,29,30,31,32,35,38,40] +3V
[7,19,23,26,27,32,33,34,36,38,39,40] +3VPCU
[11,20,22,23,25,26,30,31,38] +5V

NB5

PROJECT : QL2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI PCIE CONN X2	1A
Date: Thursday, October 29, 2009	Sheet 28 of 46	



[3,5,10,11,35,36] +1.1V_VTT
[2,7,8,9,11,27,32,34,35,40] +1.05V
[5,10,11,34,38,40] +1.8V
[2,3,7,8,9,10,11,12,13,19,20,21,22,23,24,25,26,27,28,30,31,32,35,38,40] +3V
[3,8,9,10,11,14,25,38] +3VS5

NB5

PROJECT : QL2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	XDP/BRAIDWOOD	1A
Date: Monday, October 26, 2009	Sheet 29 of 46	

DGPU_Channel-A/B

LVDS Channel Switch

U38

[16,19] EXT_TXUCLKOUT-
[16,19] EXT_TXUCLKOUT+
[16,19] EXT_TXUOUT0+
[16,19] EXT_TXUOUT0-
[16,19] EXT_TXUOUT1+
[16,19] EXT_TXUOUT1-
[16,19] EXT_TXUOUT2+
[16,19] EXT_TXUOUT2-
[16,19] EXT_TXLCLKOUT+
[16,19] EXT_TXLCLKOUT-
[16,19] EXT_TXLOUT0+
[16,19] EXT_TXLOUT0-
[16,19] EXT_TXLOUT1+
[16,19] EXT_TXLOUT1-
[16,19] EXT_TXLOUT2+
[16,19] EXT_TXLOUT2-
[17] LVDS_BLON_DGPU
[17] DISP_ON_DGPU

0B1 1B1 2B1 3B1 4B1 5B1 6B1 7B1 8B1 9B1 10B1 11B1 12B1 13B1 14B1 15B1 16B1 17B1 18B1 19B1

VDD ×8
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9
SEL1 OE1#

TXUCLKOUT- [19]
TXUCLKOUT+ [19]
TXUOUT0+ [19]
TXUOUT0- [19]
TXUOUT1+ [19]
TXUOUT1- [19]
TXUOUT2+ [19]
TXUOUT2- [19]

DGPU_SELECT#

C941 *0.1U/10V_4
C942 *0.1U/10V_4
C943 *0.1U/10V_4
C944 *0.1U/10V_4

+3V

To LVDS Conn.

IGPU_Channel-A /B

[7,19] LB_CLK#
[7,19] LB_CLK
[7,19] LB_DATAP0
[7,19] LB_DATAN0
[7,19] LB_DATAP1
[7,19] LB_DATAN1
[7,19] LB_DATAP2
[7,19] LB_DATAN2
[7,19] LA_CLK
[7,19] LA_CLK#
[7,19] LA_DATAP0
[7,19] LA_DATAN0
[7,19] LA_DATAP1
[7,19] LA_DATAN1
[7,19] LA_DATAP2
[7,19] LA_DATAN2
[7] LVDS_BLON_PCH
[7] DISP_ON_PCH

0B2 1B2 2B2 3B2 4B2 5B2 6B2 7B2 8B2 9B2 10B2 11B2 12B2 13B2 14B2 15B2 16B2 17B2 18B2 19B2

*PI3LVD1012

A10 A11 A12 A13 A14 A15 A16 A17 A18 A19
SEL2 OE2#

TXLCLKOUT+ [19]
TXLCLKOUT- [19]
TXLOUT0+ [19]
TXLOUT0- [19]
TXLOUT1+ [19]
TXLOUT1- [19]
TXLOUT2+ [19]
TXLOUT2- [19]
LVDS_BLON [7,17,19]
DISP_ON [7,17,19]

DGPU_SELECT# [9,27,31,40]

To LVDS Conn.

BKLTEN / LVDDEN

SEL	FUNCTION
LOW	DGPU
HIGH	IGPU

SELx	Ay
LOW	B1
HIGH	B2

+3V_GFX
+3V
+1.05V_GFX
+1.8V_VGA
+1.5V_GFX

R744 *4.7K_4
R747 *4.7K_4
R746 *4.7K_4
R745 *4.7K_4
R742 *4.7K_4
R736 *100K/F_4

DGPU_PWROK [9,27]
DGPU_PGOK-1
DGPU_POK4
DGPU_POK3
DGPU_POK2

Q71 *DTC144EUA
Q70 *MMBT3904-7-F
Q69 *MMBT3904-7-F
Q67 *MMBT3904-7-F

C964 *1000P/50V_4
C963 *1000P/50V_4
C961 *1000P/50V_4
C960 *1000P/50V_4

+3V

R783 *2.2K_4 EDIDCLK_PCH
R785 *2.2K_4 EDIDDATA_PCH
R787 *2.2K_4 DDCCLK_PCH
R786 *2.2K_4 DDCDATA_PCH

LVDS_BLON_PCH R758 *100K/F_4
DISP_ON_PCH R759 *100K/F_4
LVDS_BLON_DGPU R791 *100K/F_4
DISP_ON_DGPU R790 *100K/F_4

LVDS/CRT DDC Switch

U59

[17] EDIDCLK_DGPU
[7] EDIDCLK_PCH
[17] EDIDDATA_DGPU
[7] EDIDDATA_PCH
[17] DDCCLK_DGPU
[7] DDCCLK_PCH
[17] DDCDATA_DGPU
[7] DDCDATA_PCH
[9,27] EDID_SELECT#

IA0 IA1 IB0 IB1 IC0 IC1 ID0 ID1 SEL /E
YA YB YC YD VCC GND

EDIDCLK [7,17,19]
EDIDDATA [7,17,19]
DDCCLK [7,17,20]
DDCDATA [7,17,20]

+5V
C939 *.1U/10V_4

*74CBT3257

VGA SWITCH

U62

[16] CRT_R_DGPU
[16] CRT_G_DGPU
[16] CRT_B_DGPU
[16] HSYNC_DGPU
[16] VSYNC_DGPU
[7] CRT_R_PCH
[7] CRT_G_PCH
[7] CRT_B_PCH
[7] HSYNC_PCH
[7] VSYNC_PCH

IA0 IB0 IC0 ID0 IE0 IA1 IB1 IC1 ID1 IE1 SEL
YA YB YC YD YE

CRT_R [7,16,20]
CRT_G [7,16,20]
CRT_B [7,16,20]
HSYNC_COM [7,16,20]
VSYNC_COM [7,16,20]

DGPU_SELECT#

GND ×4 VDD3 ×4

+3V
C946 *.1U/10V_4
C947 *.1U/10V_4

*PI3V512

S	Yn
0	B0
1	B1

C965 *.1U/10V_4

U65

VCC S B0 YA B1 GND

PWM_SELECT# [9]
[17] DPST_PWM_DGPU
DPST_PWM
DPST_PWM [7,17,19]
[7] DPST_PWM_PCH

*74LVC1G3157GW

BKLTCTL_PWM

Discrete Only

PLTRST# R472 0_4 PEGX_RST#

U63 *MC74VHC1G08DFT2G

C948 .1U/10V_4

[3,8,24,25,27,28] PLTRST#
[9,27] DGPU_HOLD_RST#
R219 *330/F_4
DGPU_HRST_EN
PEGX_RST#
PEGX_RST# [14]
R733 *100K/F_4

DGPU_PGOK-1
Q72 *DTC144EUA

NB5

PROJECT : QL2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LVDS / CRT Switch	1A
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DGPU_HDMI

[16] H_TX2_HDMI+ C226 .1U/10V_4 DGPU_TX2_HDMI+
[16] H_TX2_HDMI- C233 .1U/10V_4 DGPU_TX2_HDMI-
[16] H_TX1_HDMI+ C219 .1U/10V_4 DGPU_TX1_HDMI+
[16] H_TX1_HDMI- C209 .1U/10V_4 DGPU_TX1_HDMI-
[16] H_TX0_HDMI+ C243 .1U/10V_4 DGPU_TX0_HDMI+
[16] H_TX0_HDMI- C252 .1U/10V_4 DGPU_TX0_HDMI-

[16] H_TXC_HDMI+ C202 .1U/10V_4 DGPU_TXC_HDMI+
[16] H_TXC_HDMI- C193 .1U/10V_4 DGPU_TXC_HDMI-

HDMISwitch

U64 *PI3HDMI201

DGPU_TXC_HDMI- 55 CLK-A
DGPU_TXC_HDMI+ 56 CLK+A
DGPU_TX0_HDMI- 2 D0-A
DGPU_TX0_HDMI+ 3 D0+A
DGPU_TX1_HDMI- 5 D1-A
DGPU_TX1_HDMI+ 6 D1+A
DGPU_TX2_HDMI- 8 D2-A
DGPU_TX2_HDMI+ 9 D2+A

[17] HDMI_DET 51 HPDA
[16] HDMI_SDA_DGPU 52 SDAA
[16] HDMI_SCL_DGPU 53 SCLA
[7] HDMI_HPD_CON 23 HPDB
[7] SDVO_DATA 24 SDAB
[7] SDVO_CLK 25 SCLB

[7] IN_CLK# 11 CLK-B
[7] IN_CLK 12 CLK+B
[7] IN_D0# 14 D0-B
[7] IN_D0 15 D0+B
[7] IN_D1# 17 D1-B
[7] IN_D1 18 D1+B
[7] IN_D2# 20 D2-B
[7] IN_D2 21 D2+B

HPD_SINK 47 HDMI_DET_S
SDA_SINK 46 HDMI_SDATA
SCL_SINK 45 HDMI_SCLK

CLK- 43 C_TXC_HDMI-
CLK+ 42 C_TXC_HDMI+
D0- 40 C_TX0_HDMI-
D0+ 39 C_TX0_HDMI+
D1- 37 C_TX1_HDMI-
D1+ 36 C_TX1_HDMI+
D2- 34 C_TX2_HDMI-
D2+ 33 C_TX2_HDMI+

PAD_GND 57
GND 4, 10, 16, 22, 32, 38, 44, 54

VDD 48, 41, 35, 19, 13, 7, 1

EQ_S1 26
EQ_S0 28
OC_S2 29
OC_S1 30
OC_S0 31
OE# 50
SEL2 27
SEL1 49

HSW_EQS1, HSW_EQS0, HSW_OCS2, HSW_OCS1, HSW_OCS0, HSW_ON#, HSW_SEL2, HSW_SEL1

To HDMI Conn.

Only for NVIDIA

Q26 2N7002E
+3V_GFX

R146 499/F_4 DGPU_TXC_HDMI-
R150 499/F_4 DGPU_TXC_HDMI+
R144 499/F_4 DGPU_TX0_HDMI-
R137 499/F_4 DGPU_TX0_HDMI+
R151 499/F_4 DGPU_TX1_HDMI-
R156 499/F_4 DGPU_TX1_HDMI+
R136 499/F_4 DGPU_TX2_HDMI-
R124 499/F_4 DGPU_TX2_HDMI+

DGPU_TXC_HDMI- RP35 C_TXC_HDMI-
DGPU_TXC_HDMI+ 0_4P2R C_TXC_HDMI+
DGPU_TX0_HDMI- RP38 C_TX0_HDMI-
DGPU_TX0_HDMI+ 0_4P2R C_TX0_HDMI+
DGPU_TX1_HDMI- RP36 C_TX1_HDMI-
DGPU_TX1_HDMI+ 0_4P2R C_TX1_HDMI+
DGPU_TX2_HDMI- RP37 C_TX2_HDMI-
DGPU_TX2_HDMI+ 0_4P2R C_TX2_HDMI+

HDMI_DET R469 0_4 HDMI_DET_S

HDMI_SCL_DGPU R458 4.7K_4 FDV301N Q23 HDMI_SCLK
D28 RB501V-40 +3V_GFX +3V
HDMI_SDA_DGPU R457 4.7K_4 FDV301N Q22 HDMI_SDATA
D21 RB501V-40 +3V_GFX

For Switchable Only

IGPU_HDMI

+3V
R486 *2K/F_4 SDVO_DATA
R500 *2K/F_4 SDVO_CLK

C955 0.1U/10V_4
C954 0.1U/10V_4
C945 0.1U/10V_4
C950 0.1U/10V_4

OC SETTING
S2 S1 S0 = 1 : 1 : 1 500mV 0dB Defualt
S2 S1 S0 = 1 : 1 : 0 750mV 0dB
S2 S1 S0 = 1 : 0 : 1 1000mV 0dB
S2 S1 S0 = 1 : 0 : 0 600mV 0dB
S2 S1 S0 = 0 : 1 : 1 500mV 0dB
S2 S1 S0 = 0 : 1 : 0 500mV 1.5dB
S2 S1 S0 = 0 : 0 : 1 500mV 3.5dB
S2 S1 S0 = 0 : 0 : 0 500mV 6dB

EQ SETTING
S1 S0 = 1 : 1 3dB Defualt
S1 S0 = 1 : 0 8dB
S1 S0 = 0 : 1 3dB
S1 S0 = 0 : 0 15dB

HSW_EQS1 R628 *4.7K_4
HSW_EQS0 R627 *4.7K_4
HSW_OCS2 R626 *4.7K_4
HSW_OCS1 R625 *4.7K_4
HSW_OCS0 R624 *4.7K_4
HSW_ON# R623 *4.7K_4

OE#	SEL2	SEL1	Ay
0	X	1	A
0	1	0	B

SEL	FUNCTION
LOW	DGPU
HIGH	IGPU

+3V
R630 *4.7K_4
HSW_SEL1
Q33 *DTC144EUA
R629 *4.7K_4
DGPU_SELECT# DGPU_SELECT# [9,27,30,40]
R631 *0_4 HSW_SEL2
R632 *4.7K_4
+3V

Mount R629 / R632 for UMA only

HDMI PORT

CN20 HDMI CONN

C_TX2_HDMI+ 1 D2+
C_TX2_HDMI- 3 D2-
C_TX1_HDMI+ 4 D1+
C_TX1_HDMI- 6 D1-
C_TX0_HDMI+ 7 D0+
C_TX0_HDMI- 9 D0-
C_TXC_HDMI+ 10 CK+
C_TXC_HDMI- 12 CK-

SHELL1 20
SHELL2 21
SHELL3 22
SHELL4 23
D2 Shield 2
D1 Shield 5
D0 Shield 8
CK Shield 11
GND 17

+5V_HDMIC
D29 RB501V-40
D9 RB501V-40

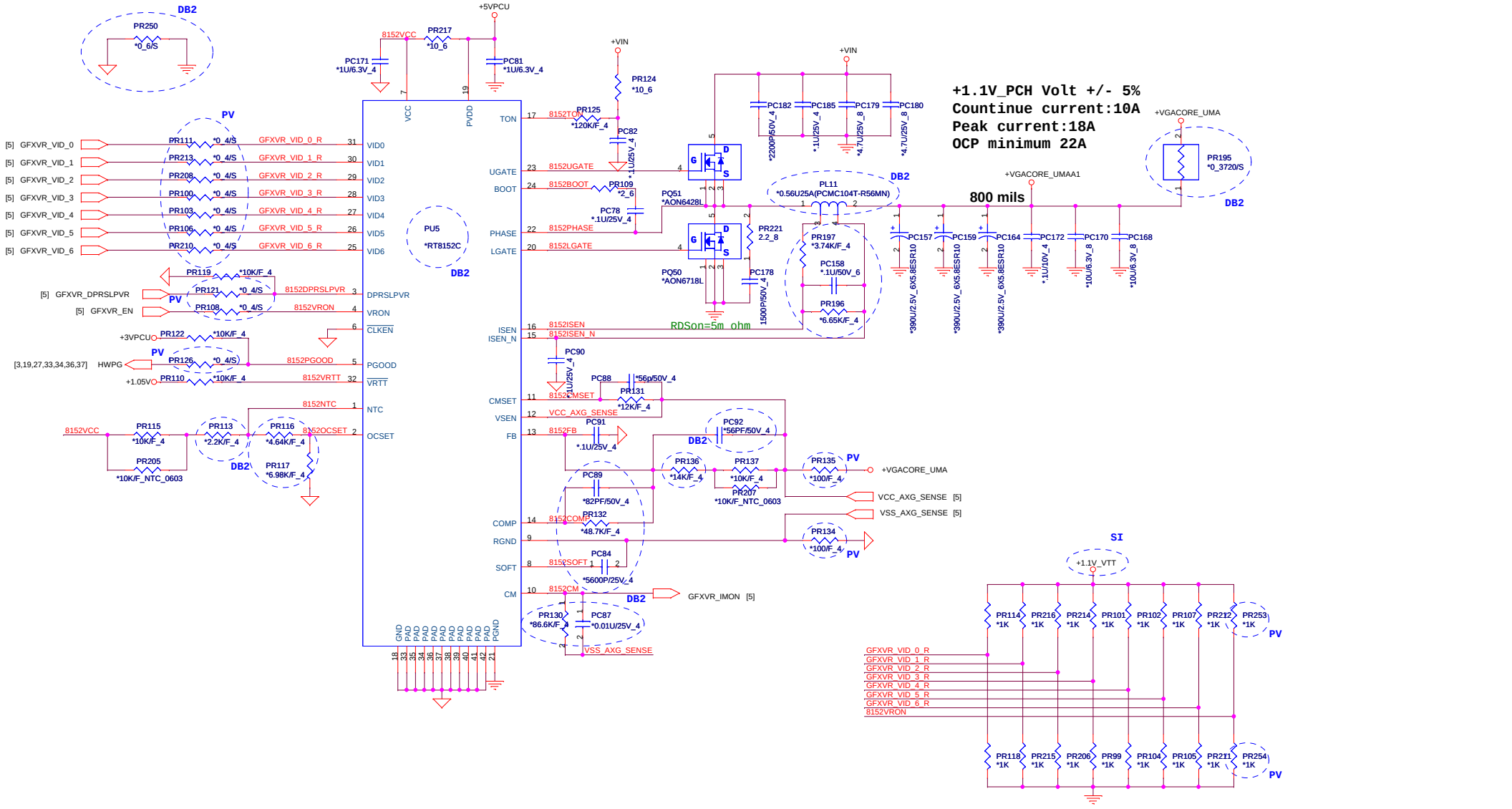
R112 2.2K/F_4
R109 2.2K/F_4
R111 0_4
R110 0_4
HDMI_SCLK
HDMI_SDATA
HDMISCL 15
HDMISDA 16
C567 *10P/50V_4
C566 *10P/50V_4
DDC CLK CE Remote 13
DDC DATA NC 14

+5V
F2 FUSE1A6V_POLY +5V_HDMIC 18

[27] HDMI_DET1
R464 *0_4
HDMI_DET_S
R461 10K/F_4
HDMI_DET_N
L26 BLM18BA470SN1D
HDMI_DET_C 19
HP DET
C564 220P/50V_4

D22 BAV99W
+3V
R488 110K/F_4

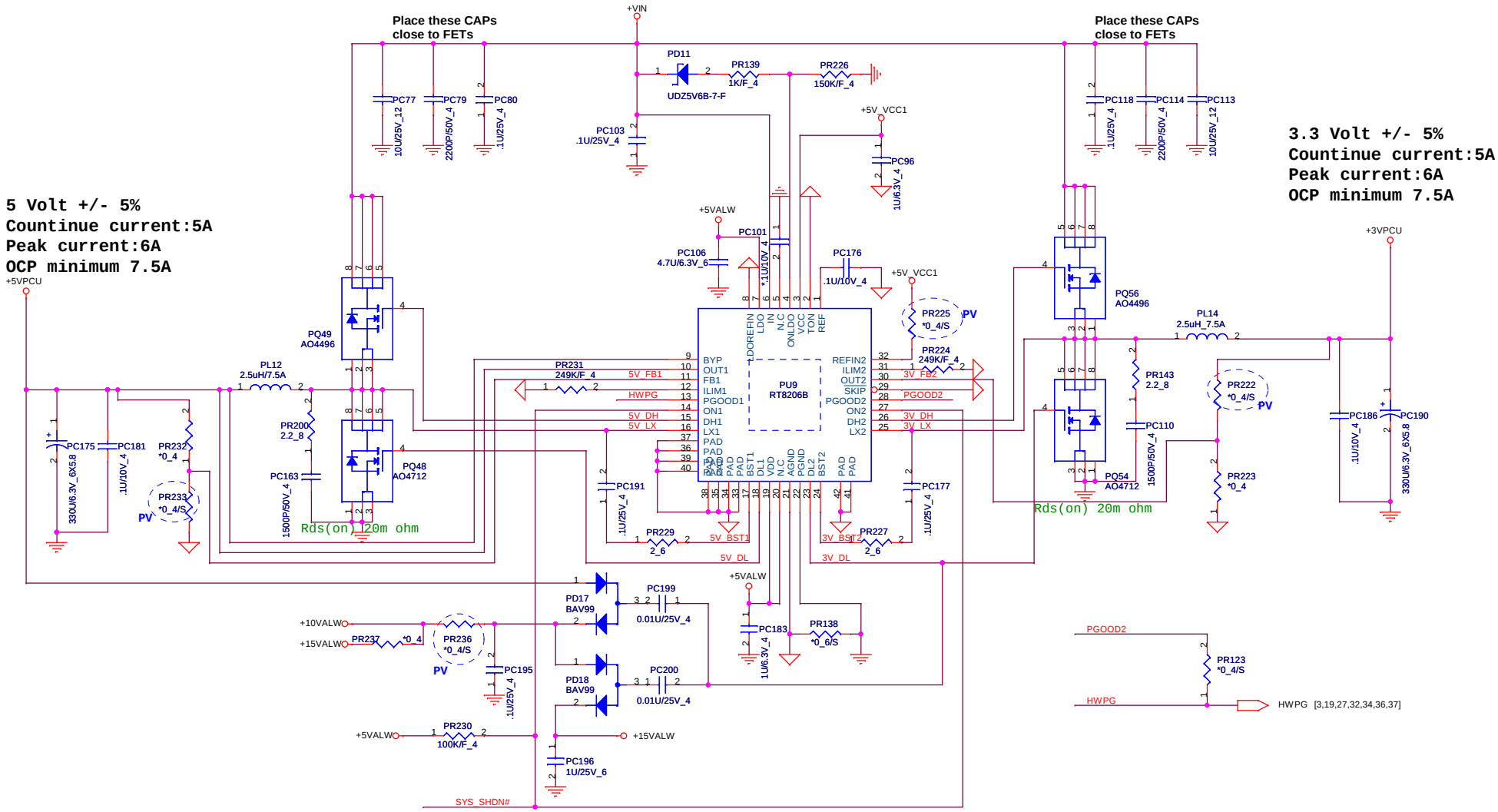
+5V_HDMIC
C157 *.01U/16V_4
for EMI request



PROJECT : QL2	Quanta Computer Inc.
Size: Custom	Document Number: UMA GPU CORE (RT8152C)
Rev: PV	
Date: Monday, October 26, 2009	Sheet 32 of 46

NB5

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

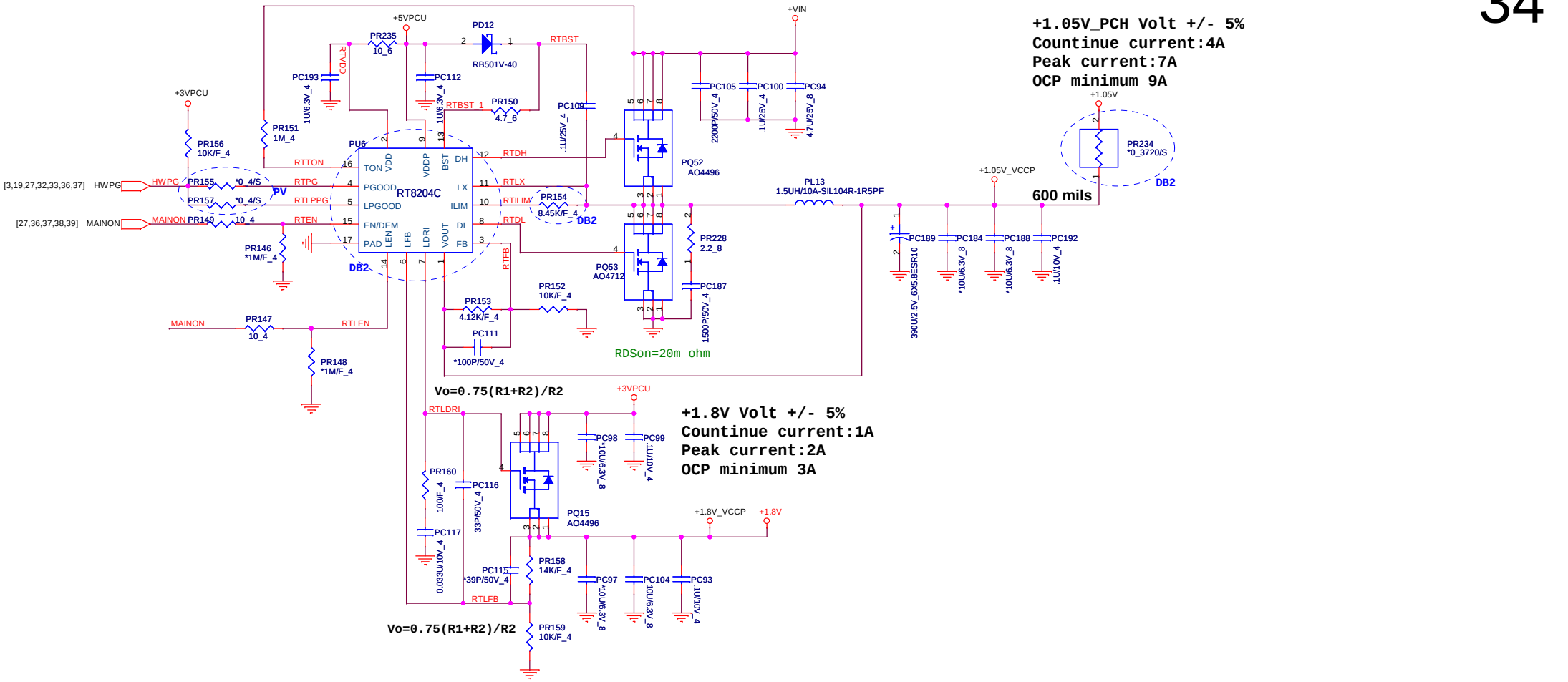


PROJECT : QL2
Quanta Computer Inc.

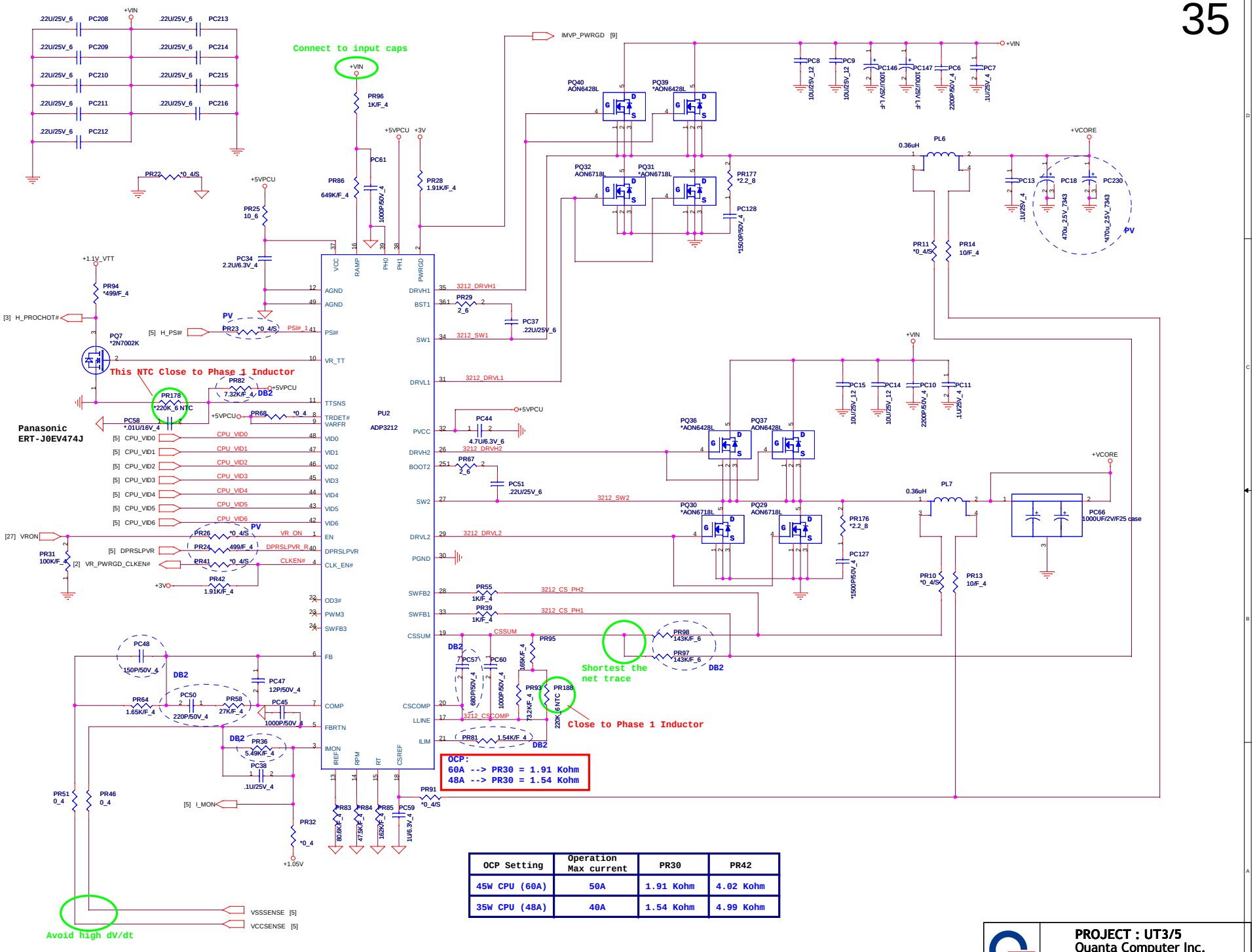
NB5

Size	Document Number	Rev
Custom	+5V/+3V (RT8206B)	PV

Date: Monday, October 26, 2009 Sheet 33 of 46



NB5	PROJECT : QL2 Quanta Computer Inc.		
	Size: Custom	Document Number: PCH +1.05V (RT8204)	Rev: PV
	Date: Monday, October 26, 2009	Sheet 34 of 46	

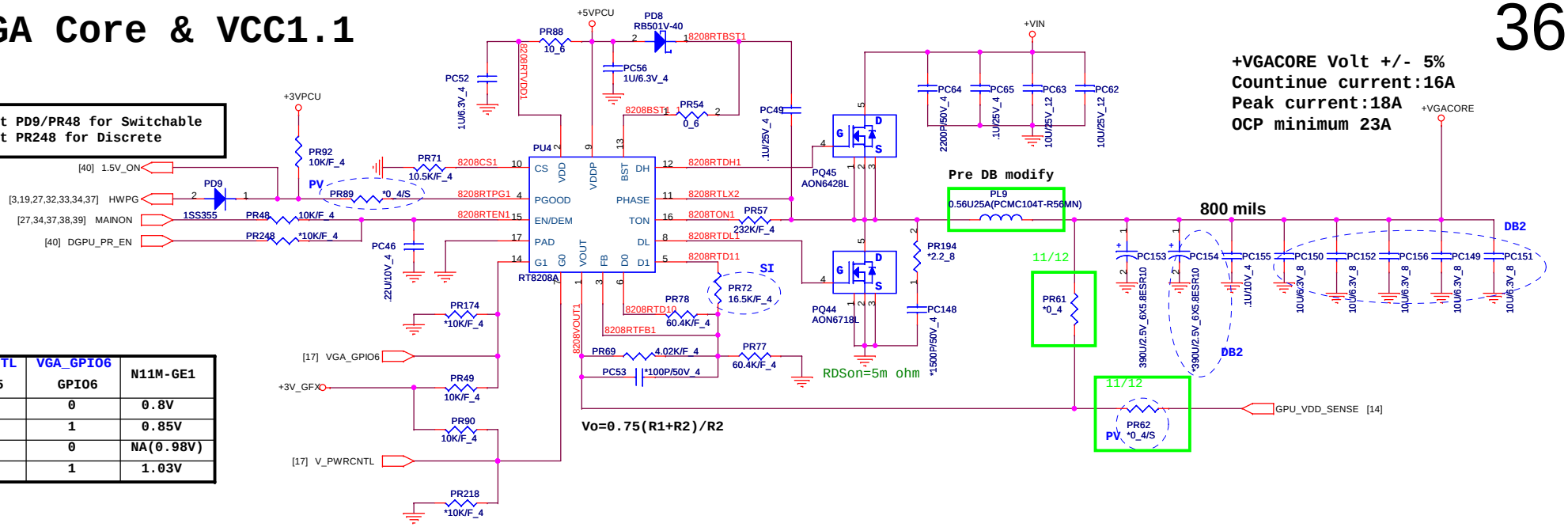


OCP Setting	Operation Max current	PR30	PR42
45W CPU (60A)	50A	1.91 Kohm	4.02 Kohm
35W CPU (48A)	40A	1.54 Kohm	4.99 Kohm

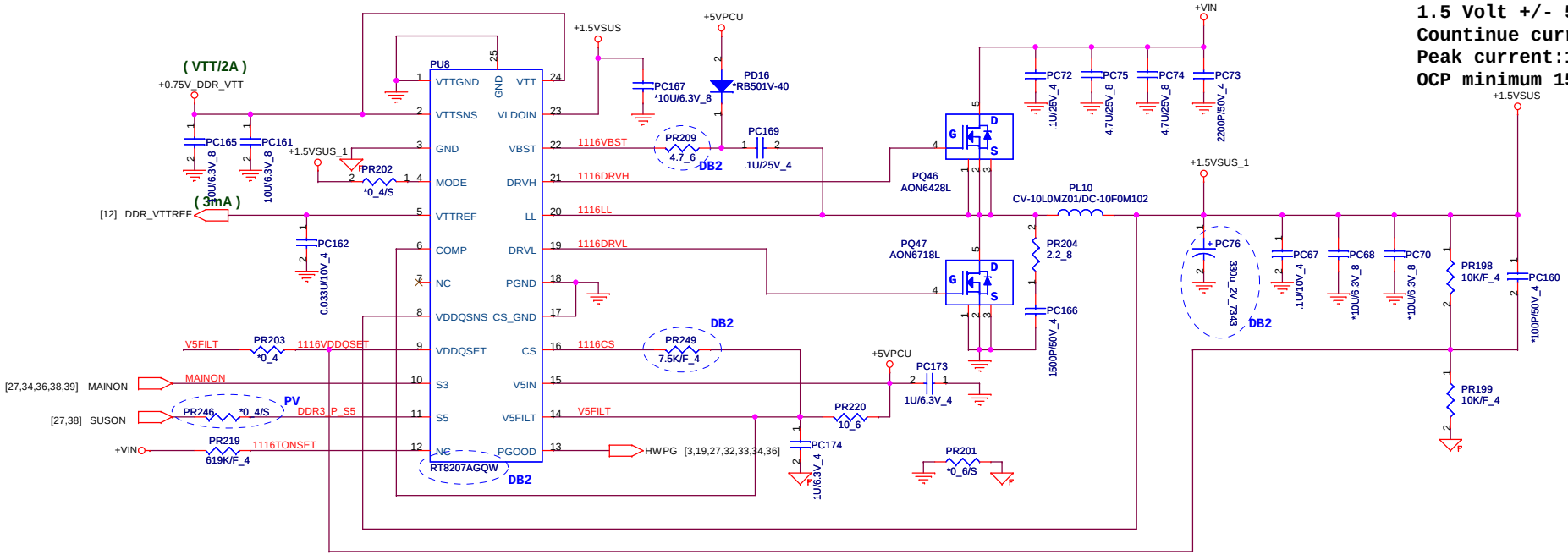
VGA Core & VCC1.1

1 : un-Mount PD9/PR48 for Switchable
2 : un-Mount PR248 for Discrete

V_PWRCNTL GPIO5	VGA_GPIO6 GPIO6	N11M-GE1
0	0	0.8V
0	1	0.85V
1	0	NA(0.98V)
1	1	1.03V

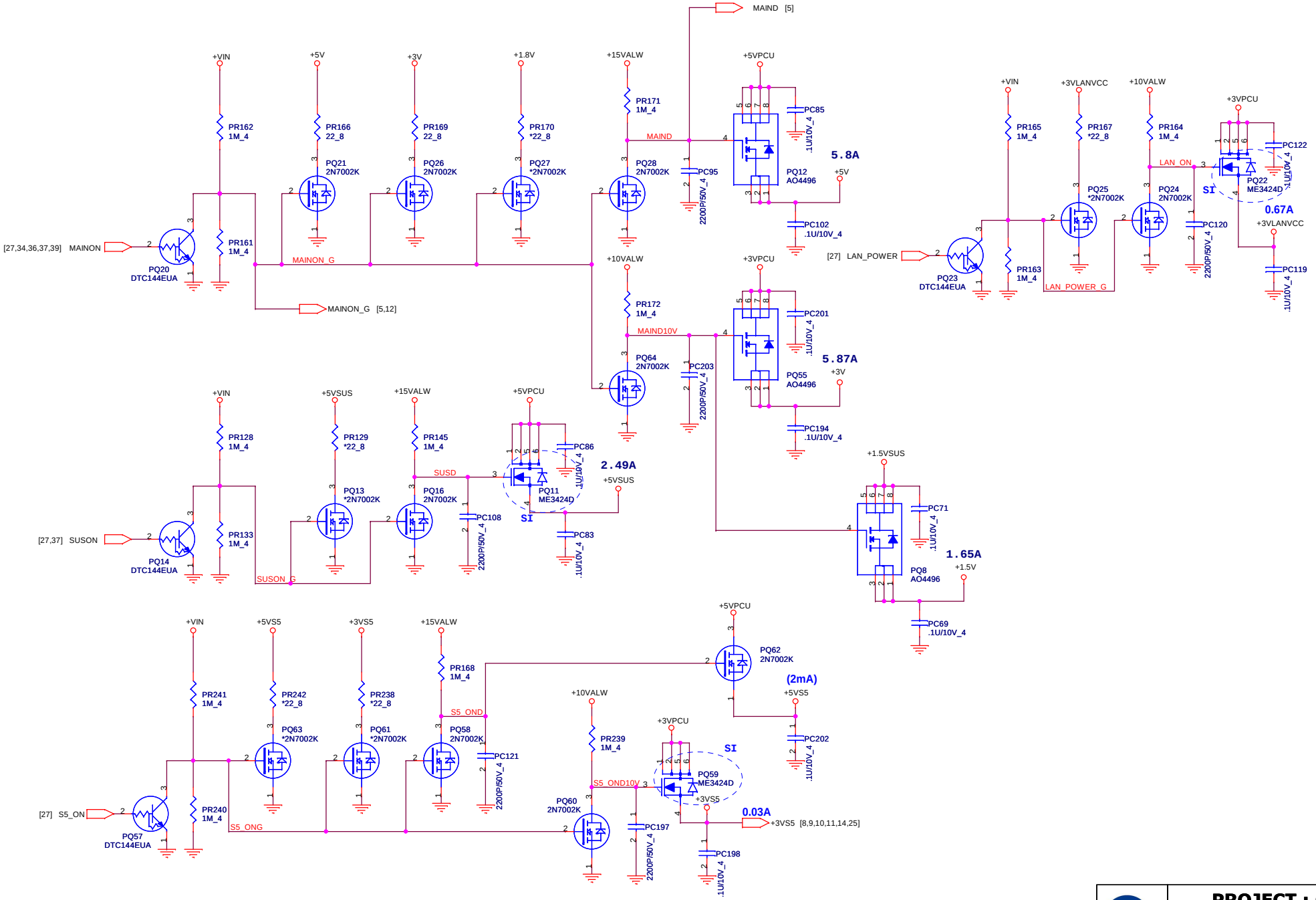


PROJECT : QL2	Quanta Computer Inc.
NB5	Size: Custom; Document Number: +1.1V_VTT/VGA Core RT820A; Rev: PV
	Date: Monday, October 26, 2009; Sheet 36 of 46

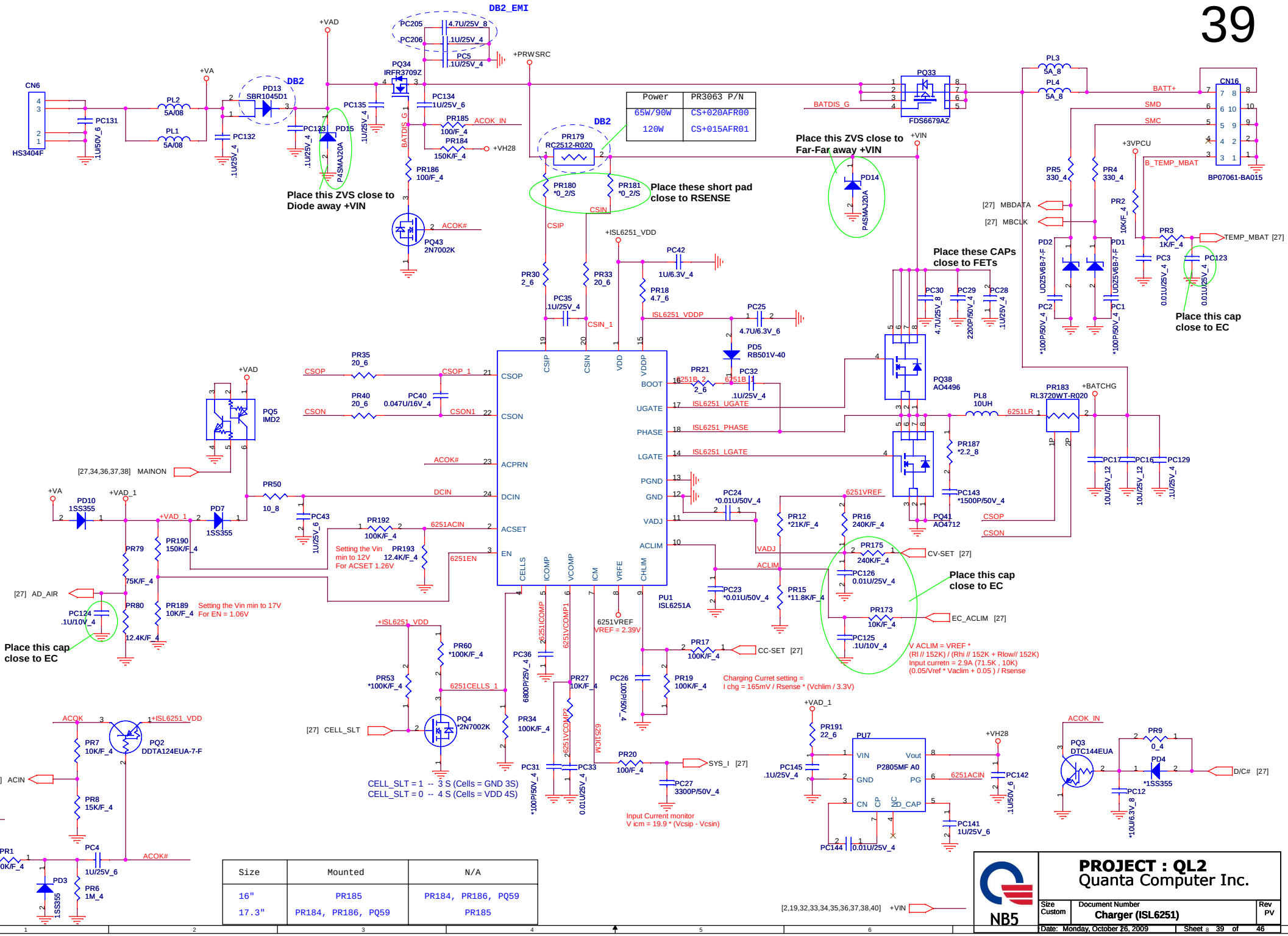


1.5 Volt +/- 5%
Countinue current:6A
Peak current:12A
OCP minimum 15A

NB5	PROJECT : QL2 Quanta Computer Inc.	
Size: Custom	Document Number: DDR3 (RT8207)	Rev: PV
Date: Thursday, October 29, 2009	Sheet 37 of 46	



NB5	**PROJECT : QL2** Quanta Computer Inc.	
Size: Custom	Document Number: DISCHARGE/3VS5/5VS5/LAN	Rev: PV
Date: Monday, October 26, 2009	Sheet 38 of 46	



Size	Mounted	N/A
16"	PR185	PR184, PR186, PQ59
17.3"	PR184, PR186, PQ59	PR185

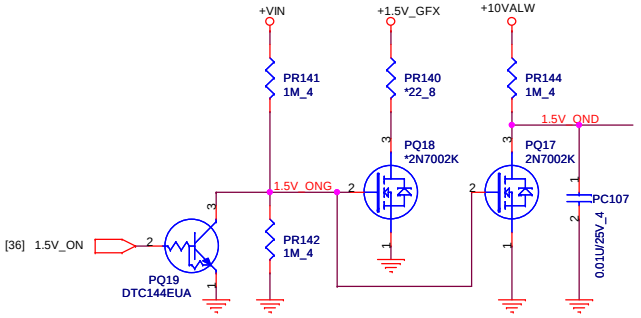
NB5

PROJECT : QL2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Charger (ISL6251)	PV

Date: Monday, October 26, 2009 Sheet 39 of 46

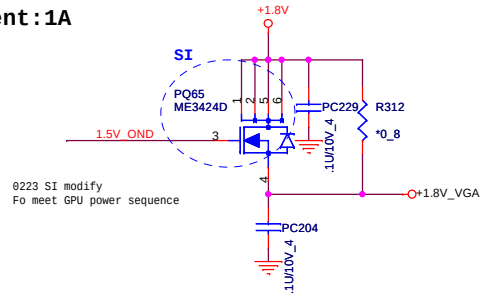
For Discrete or switchable Only

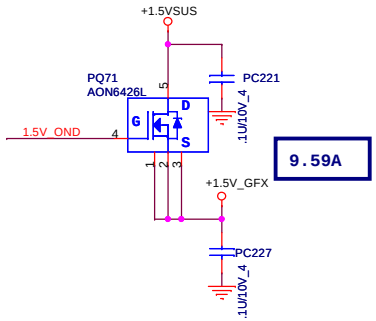


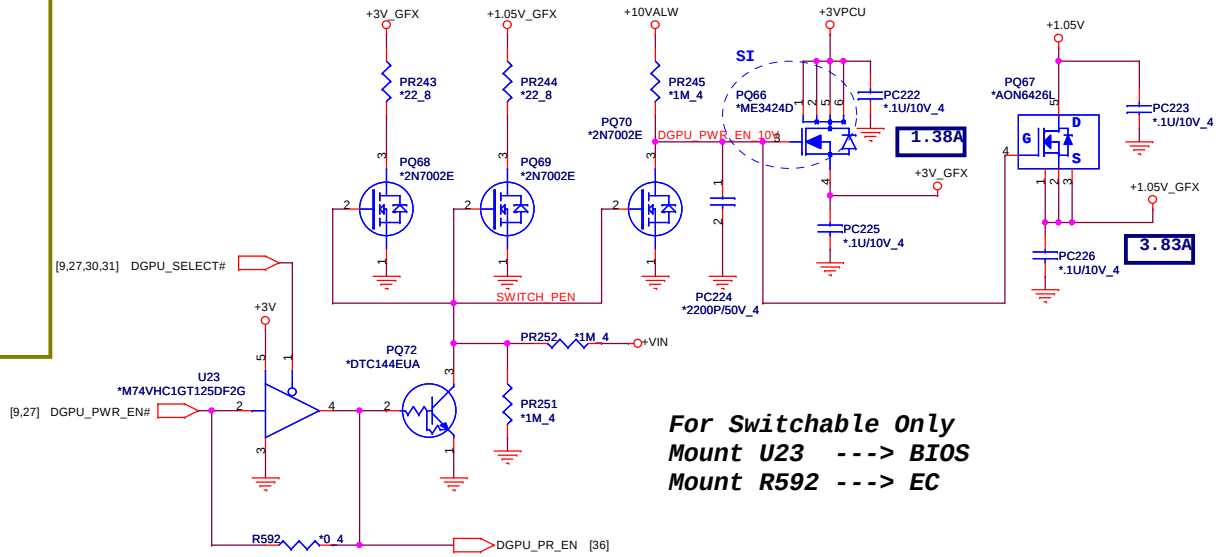
Change PC119 to 0.01u/25v as Discrete power sequence

For Discrete or switchable Only

+1.8 Volt +/- 0.1V
Countinue current:0.3A
Peak current:1A



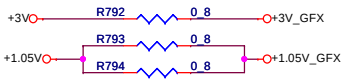




For Switchable Only
Mount U23 ---> BIOS
Mount R592 ---> EC

R51 co-lay PQ71
R53/R54 co-lay PQ68

For Discrete Only

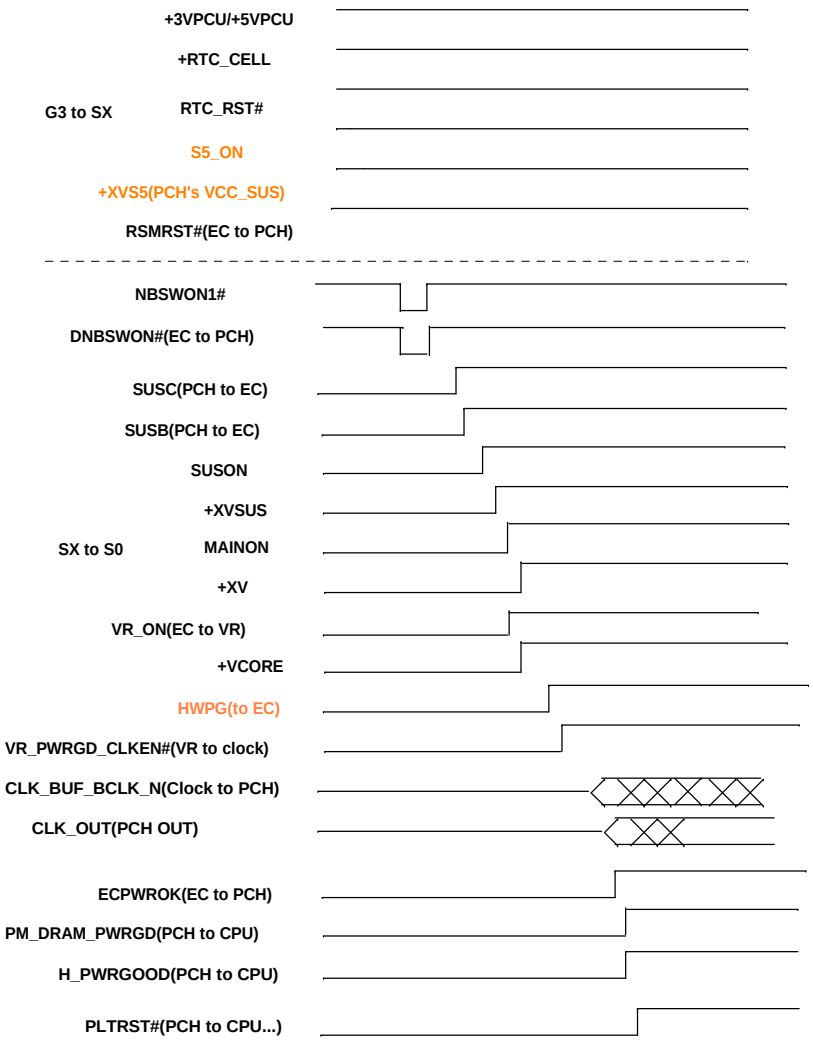


For Hybrid DGPU Power Rails Sequence
1. +3V_GFX, +1.05V_GFX
2. +VGA_CORE -> DGPU_PG
3. 1.5V_GFX, +1.8V_GFX

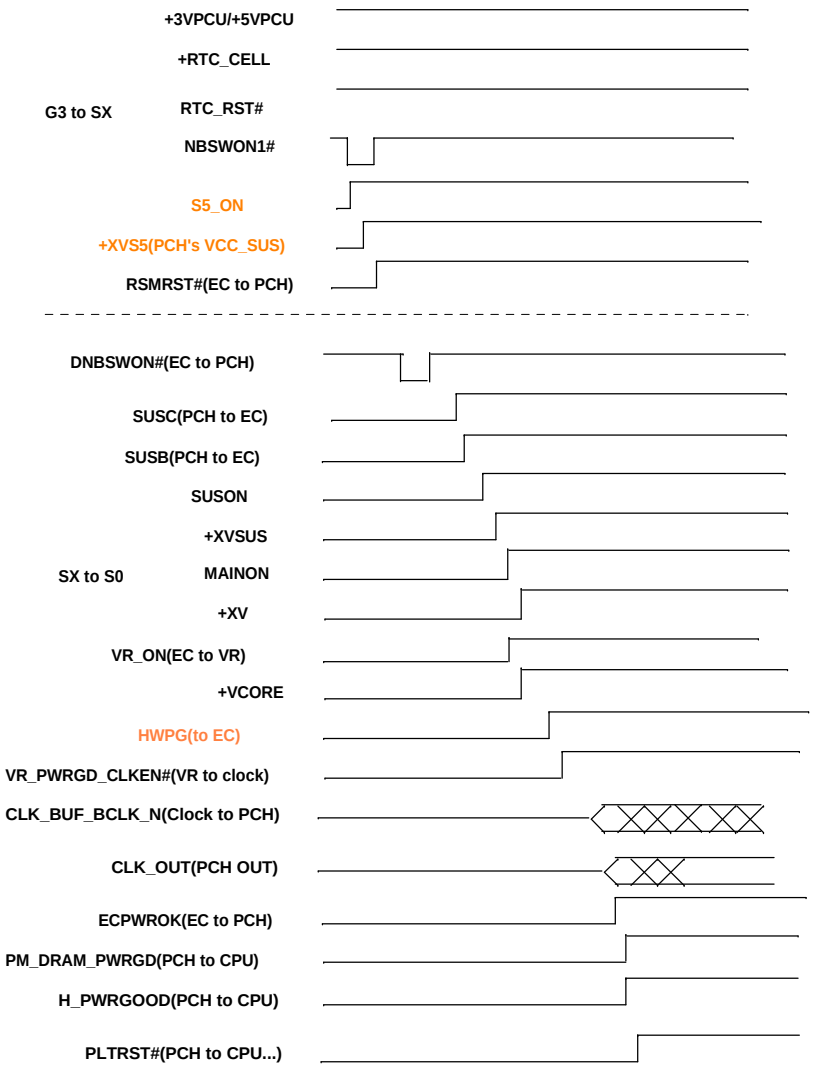
NB5	**PROJECT : QL4** Quanta Computer Inc.	
	Size: A3 — Document Number: **Switchable Power**	Rev: PV
	Date: Monday, October 26, 2009 — Sheet 40 of 46	

Power up sequence

LAN/RTC WAKE UP ENABLE.



LAN/RTC WAKE UP DISABLE.



NB5

PROJECT : QL2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Power up sequence	1A

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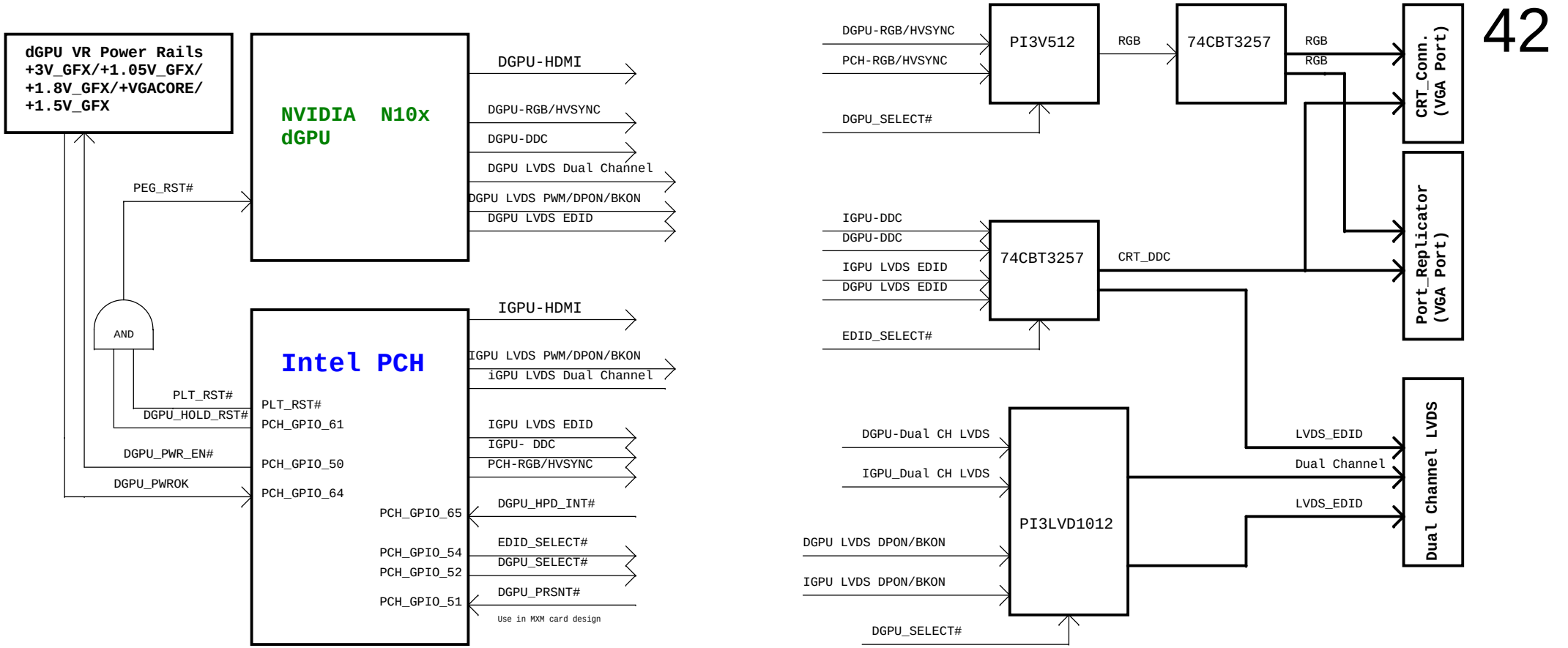

Switchable GPIOs	Descriptions
PCH_GPIO52	DGPU_SELECT#
PCH_GPIO61	DGPU_HOLD_RST#
PCH_GPIO50	DGPU_PWR_EN#
PCH_GPIO64	DGPU_PWR_OK
PCH_GPIO54	EDID_ELECT#
PCH_GPIO51	DGPU_PRSNT#
PCH_GPIO53	PWM_SELECT#

NB5

PROJECT : QL2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Switch Blockdiagram	1A

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