COMPAL CONFIDENTIAL

MODEL NAME : LOKI N3V3 KBL UMA

PCB NO : DA60022P010

BOM P/N : 431AET31L01~L10&L51~L57

KBL-U & R + MEC1416 board

2018-11-06

REV : 1.0 (A00)

PCB R1

ZZZ

DA60022P010

PCBR1@

PCB 2EI LA-G714P REV1 M/B 5

DAZ R1

ZZZ

DAZ2EI00200

DAZR1@

PCB EDI72 LA-G714P LS-F112P/F114P/F117P

DAZ R3

ZZZ

DAZ2EI00201

DAZR3@

PCB EDI72 LA-G714P LS-F112P GOLD A31

X4E#

ZZZ

X4EAET31L51

100@X4E@

SMT EMC N3 KBL UMA EE AG714 EDI73

X4E#

ZZZ

X4EAET31L01

1000@X4E@

SMT EMC N3V3 KBL UMA EE AG714 EDI72

KBL R3

UC1

SA0000A377L

i5KBLU_R3@

S IC FJ8067702739739 SR342 H0 2.5G A31!

UC1

SA0000BLD1L

i3KBLU42_SMB0_R3@

S IC FJ8067703282620 SR3LD Y0 2.3G A31!

UC1

SA0000BVB1L

i3KBLU23_SMB0_R3@

S IC FH8067703037315 SR3N6 J1 2.3G A31!

UC1

SA0000A346L

i7KBLU_R3@

S IC FJ8067702739740 SR341 H0 2.7G A31!

UC1

SA0000ADL3L

KBLU_Celeron_R3@

S IC FJ8067702739933 SR349 H0 1.8G A31!

UC1

SA0000ADV3L

KBLU_Pentium_R3@

S IC FJ8067702739932 SR348 H0 2.3G A31!

UC1

SA0000BKN3L

i3KBLR_R3@

S IC FJ8067703282227 SR3W0 Y0 2.2G A31 !

UC1

SA0000AWB3L

i5KBLR_R3@

S IC FJ8067703282221 SR3LB Y0 1.6G A31!

UC1

SA0000AWC2L

i7KBLR_R3@

S IC FJ8067703281816 SR3LC Y0 1.8G A31!

UC1

SA0000BLH1L

i3KBLU22_SMB0_R3@

S IC FJ8067702739769 SR3TK H0 2.3G A31!

@ : Un-pop Component
UMA@/DIS@ : UMA & DIS Type
U22@/U42@ : KBL U/KBL U-R
EC@ : EC
JP@/PJP@ : JUMP

EMI@/ESD@/RF@ : EMI, ESD and RF Component
@EMI@/@ESD@/@RF@ : EMI, ESD and RF Un-POP Component
CMC@ : XDP Component
CONN@ : Connector Component
TP_WAKE@/NTP_WAKE@ : TouchPad wake
KBBL@ : KB Backlight
TPM@/FTPM@ : HW TPM/SW TPM
MMC@ : eMMC
FFS@ : Free Fall Sensor
MODS@ : Modern Standby

Layout Dell logo

REV: X00
PWB: 9HTP8

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: Cover Page

Size | Document Number: LA-G714P | Rev: 1.0

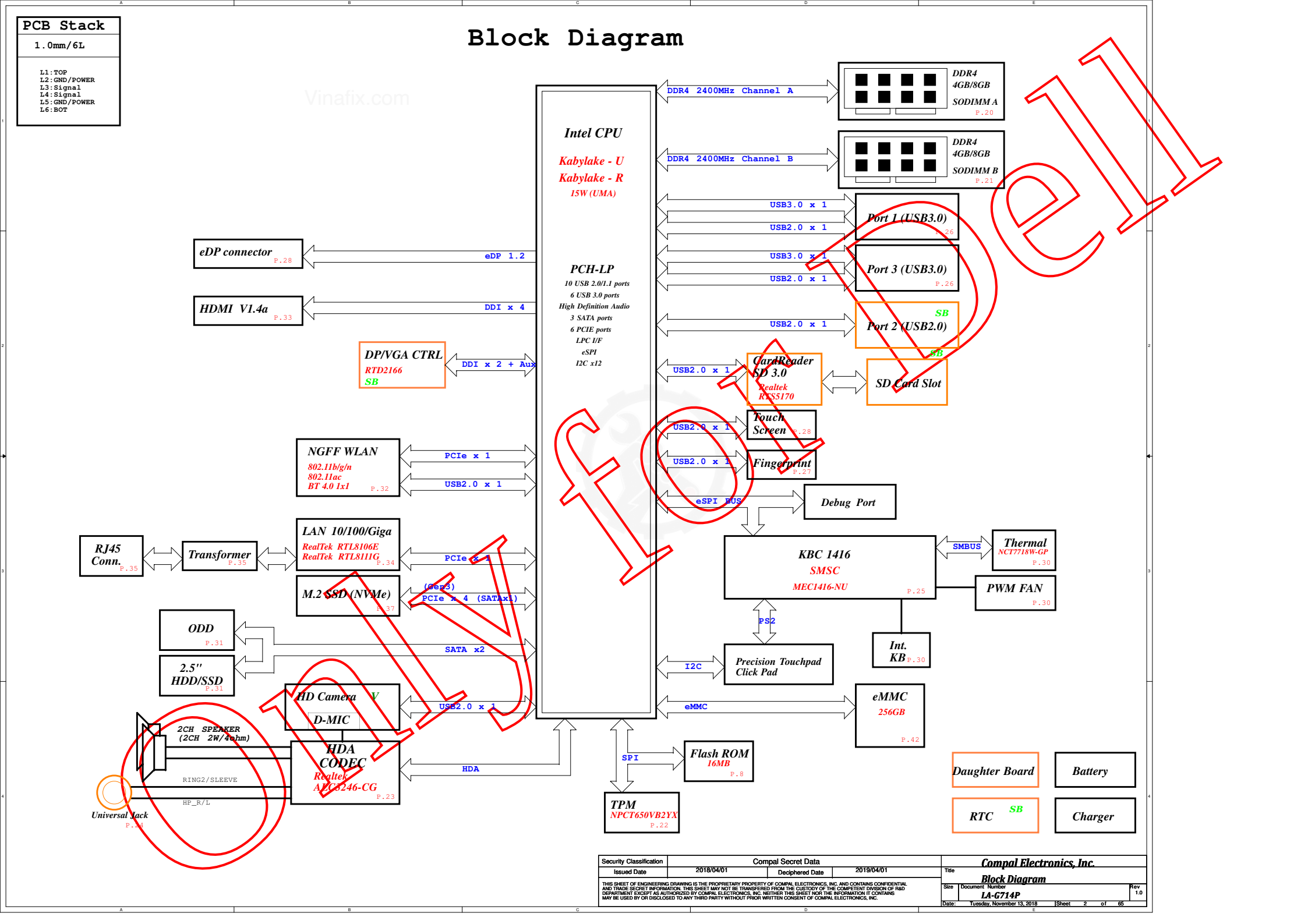
Date: Tuesday, November 13, 2018 | Sheet 1 of 65

Block Diagram

PCB Stack

1.0mm/6L

L1:TOP
L2:GND/POWER
L3:Signal
L4:Signal
L5:GND/POWER
L6:BOT



Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: Block Diagram

Size	Document Number	Rev
	LA-G714P	1.0

Date: Tuesday, November 13, 2018 Sheet 2 of 65

POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	ON	OFF	OFF	OFF
G3	OFF	OFF	OFF	OFF	OFF	OFF	OFF

USB PORT#	DESTINATION
1	USB2.0 Port1
2	USB2.0 Port2 , IO/B
3	USB2.0 Port3
4	NC
5	CCD
6	Card Reader IO/B
7	BT
8	Touch Screen
9	Finger Printer
10	NC

USB3.0	PCIE	SATA	DESTINATION
USB3.0-1			USB3.0 Port1
USB3.0-2			NC
USB3.0-3			USB3.0 Port3
USB3.0-4			NC
USB3.0-5	PCIE-1		NC
USB3.0-6	PCIE-2		NC
	PCIE-3		NC
	PCIE-4		NC
	PCIE-5		10/100M LAN
	PCIE-6		WLAN
	PCIE-7	SATA-0	SATA HDD
	PCIE-8	SATA-1	SATA ODD
	PCIE-9		NVME SSD
	PCIE-10		NVME SSD
	PCIE-11	SATA-1*	NVME SSD
	PCIE-12	SATA-2	NVME SSD

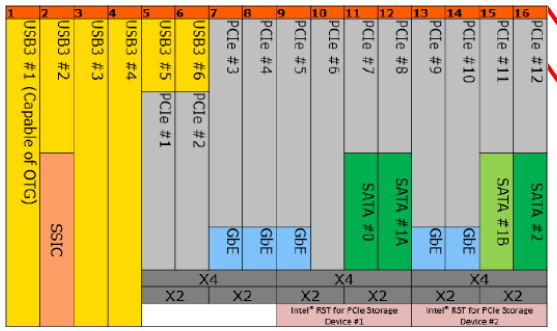
PM TABLE

power plane / State	+RTC_CELL	B+	+1.0V_PRIM +1.0V_MPHYGT +1.8V_PRIM +3VALW +3VALW_PCH +3.3V_ALW_DSW +5VALW	+1.0V_VCCST +1.2V_DDR +2.5V_MEM	+1.0VS_VCCIO +1.0V_VCCSTG +VCC_GT +VCC_SA +VGA_CORE +VCC_CORE +0.6V_DDR_VTT
S0	ON	ON	ON	ON	ON
S3	ON	ON	ON	ON	OFF
M3	ON	ON	ON	ON	OFF
S4&S5 / AC	ON	ON	ON	OFF	OFF
S4&S5 / AC doesn't exist	ON	ON	OFF	OFF	OFF
G3	ON	OFF	OFF	OFF	OFF

Board ID table

Item	Pull-down	Pull-up	Voltage	Board ID/Model ID
1	100	10K	3.000	EVT
2	100	17.8K	2.801	DVT1
3	100	27K	2.598	DVT2
4	100	37.4K	2.402	
5	100	49.9K	2.201	Pilot
6	100	64.9K	2.001	
7	100	82.5K	1.808	
8	100	107K	1.594	
9	100	154K	1.299	
10	100	200K	1.1	
11	100	TBD	0.9	
12	100	TBD	0.7	
13	100	TBD	0.5	
14	100	TBD	0.3	

High Speed I/O (HSIO) Lane Multiplexing in KBL U PCH-LP

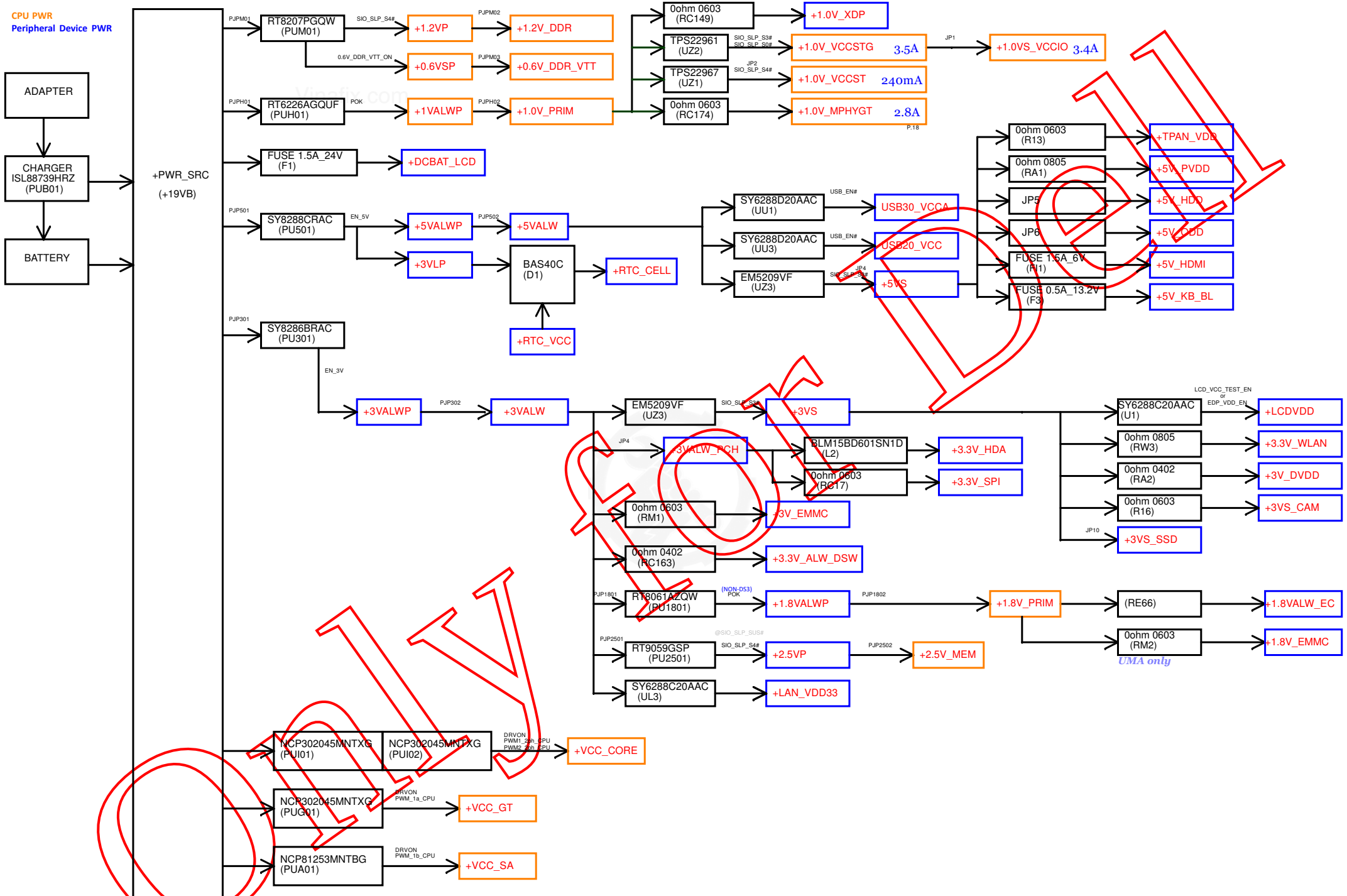


Compal Electronics, Inc.

Title: Index and Configuration

Size: | Document Number: LA-G714P | Rev: 1.0

Date: Tuesday, November 13, 2018 | Sheet 3 of 65



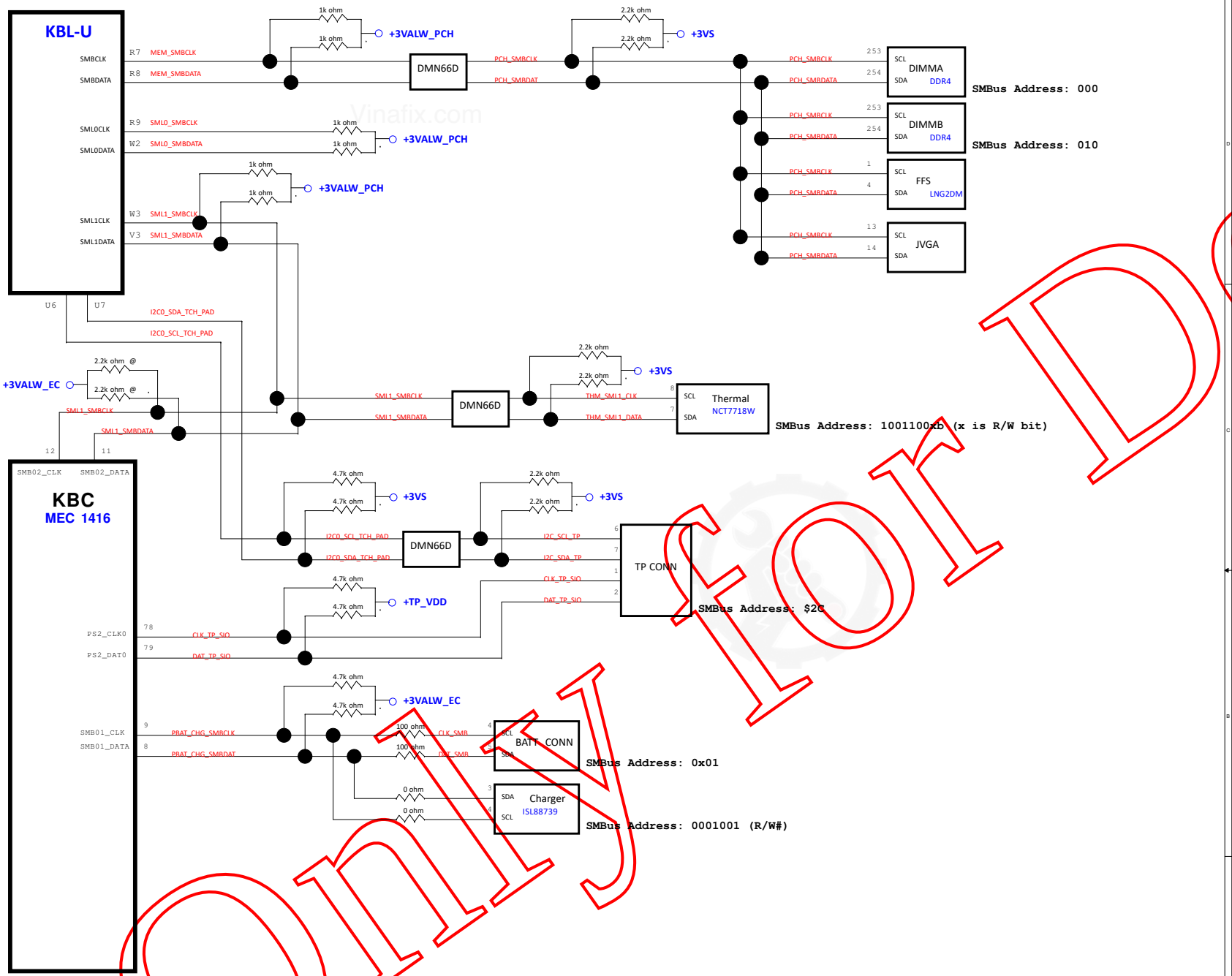
Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: Power Rail

Size	Document Number	Rev
	LA-G714P	1.0

Date: Tuesday, November 13, 2018 Sheet 4 of 65



Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

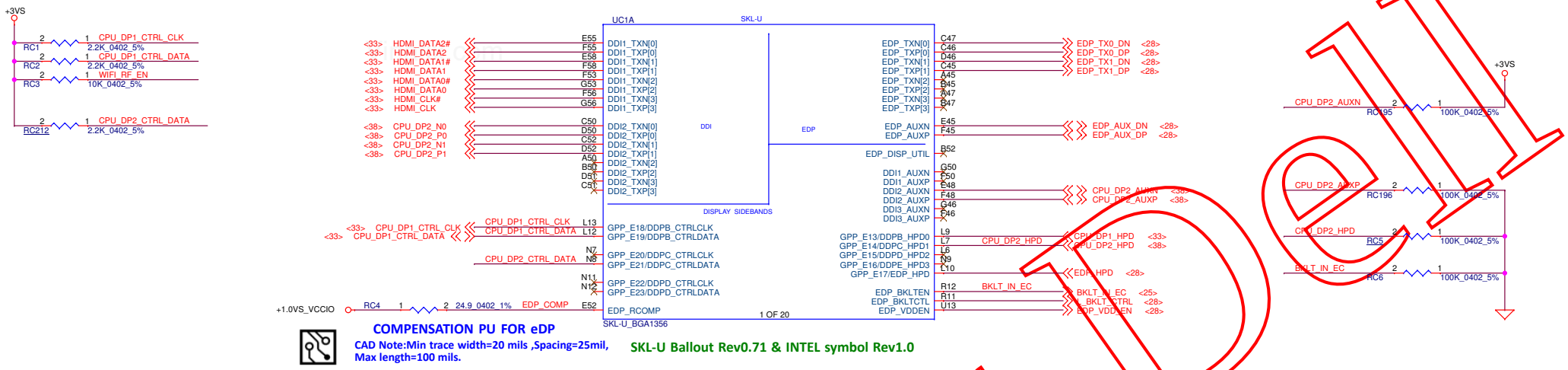
Compal Electronics, Inc.

Title: **SMbus Block Diagram**

Size	Document Number	Rev
	LA-G714P	1.0

Date: Tuesday, November 13, 2018 | Sheet 5 of 65

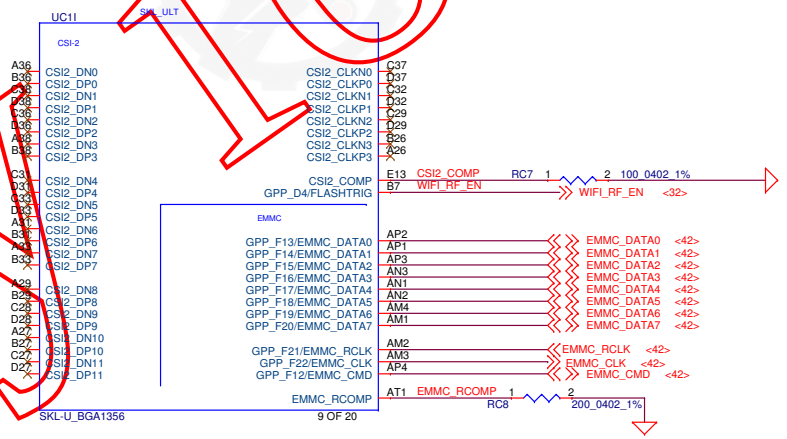
Main Func = CPU



COMPENSATION PU FOR eDP

CAD Note:Min trace width=20 mils ,Spacing=25mil, Max length=100 mils.

SKL-U Ballout Rev0.71 & INTEL symbol Rev1.0

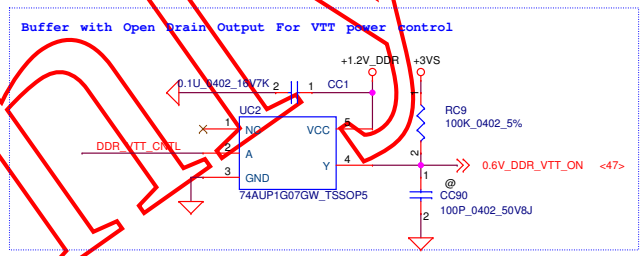


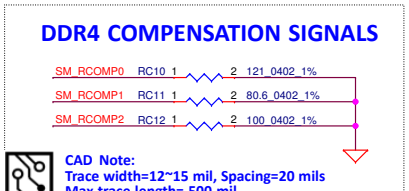
Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.			
Title	MCP(1/14)DDI,EDP,CSI2,EMMC		
Size	Document Number LA-G714P		Rev 1.0
Date: Tuesday, November 13, 2018	Sheet 6 of 65		

Main Func = CPU

DDR4 Interleaved Memory





Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.			
Title	MCP(2/14)DDR4		
Size	Document Number	LA-G714P	Rev 1.0
Date: Tuesday, November 13, 2018	Sheet 7 of 65		

Main Func = CPU

SPI_MOSI= SPI_IO0
SPI_MISO= SPI_IO1
PCH EDS R0.7 p.235~236

UC1E — SKL-U

SPI - FLASH
SPI0_CLK
SPI0_MISO
SPI0_MOSI
SPI0_IO2
SPI0_IO3
SPI0_CS0#
SPI0_CS1#
SPI0_CS2#

SPI - TOUCH
GPP_D1/SPI1_CLK
GPP_D2/SPI1_MISO
GPP_D3/SPI1_MOSI
GPP_D21/SPI1_IO2
GPP_D22/SPI1_IO3
GPP_D0/SPI1_CS#

C LINK
CL_CLK
CL_DATA
CL_RST#

GPP_A0/RCIN#
GPP_A6/SERIRQ

SMBUS, SMLINK
GPP_C0/SMBCLK
GPP_C1/SMBDATA
GPP_C2/SMBALERT#
GPP_C3/SML0CLK
GPP_C4/SML0DATA
GPP_C5/SML0ALERT#
GPP_C6/SML1CLK
GPP_C7/SML1DATA
GPP_B23/SML1ALERT#/PCHHOT#

LPC
GPP_A1/LAD0/ESPI_IO0
GPP_A2/LAD1/ESPI_IO1
GPP_A3/LAD2/ESPI_IO2
GPP_A4/LAD3/ESPI_IO3
GPP_A5/LFRAME#/ESPI_CS#
GPP_A14/SUS_STAT#/ESPI_RESET#
GPP_A9/CLKOUT_LPC0/ESPI_CLK
GPP_A10/CLKOUT_LPC1
GPP_A8/CLKRUN#

SKL-U_BGA1356 — 5 OF 20

QC1A L2N7002DW1T1G 2N SC88-6
QC1B L2N7002DW1T1G 2N SC88-6
MEM_SMBCLK — PCH_SMBCLK <20,21,31,38>
MEM_SMBDATA — PCH_SMBDATA <20,21,31,38>

SMB -> DDR4, FFS

SML1_SMBCLK <25,30>
SML1_SMBDATA <25,30>

SML1 -> EC, THM

PCH_ESPI_IO0 — ESPI_IO0 <25>
PCH_ESPI_IO1 — ESPI_IO1 <25>
PCH_ESPI_IO2 — ESPI_IO2 <25>
PCH_ESPI_IO3 — ESPI_IO3 <25>
RPC2 15_0804_8P4R_5%

ESPI_CS# <25>
ESPI_RESET# <25>
ESPI_CLK <25>
PCH_ESPI_CLK — RC15 EMI@ 22_0402_5%
CC88 @RF@ 10P_0402_50V8J

PCH_SMBDATA 2.2K_0402_5% RC27
PCH_SMBCLK 2.2K_0402_5% RC28

RPC3 1K_0804_8P4R_1%
MEM_SMBCLK
MEM_SMBDATA
SML1_SMBCLK
SML1_SMBDATA

SML0_SMBCLK RC33 1K_0402_5%
SML0_SMBDATA RC34 1K_0402_5%

+3VS — RC35 FFS_INT1 10K_0402_5%
+3VS — RC209 HDD_EN_PCH 10K_0402_5%
+1.8V_PRIM — RC14 10K_0402_5% — ESPI_ALERT# <25>

TPM_SPI_IRQ# <31>
FFS_INT1 <31>
HDD_EN_PCH <31>

PCH_SPI_CLK <22>
PCH_SPI_D1 <22>
PCH_SPI_D0 <22>
PCH_SPI_D2
PCH_SPI_D3
PCH_SPI_CS#0
PCH_SPI_CS#2 <22>

+3VALW_PCH — RC17 0_0603_5% — +3.3V_SPI
+3.3V_SPI — RC18 PCH_SPI_CS#0 4.7K_0402_5%
+3.3V_SPI MOW 2015WW06 — RC19 PCH_SPI_D2 1K_0402_5% — RC20 PCH_SPI_D3 1K_0402_5%

XDP_SPI_S <14> — RC40 CMC@ 1K_0402_1% PCH_SPI_D0
XDP_SPI_IO2 <14> — RC41 CMC@ 1K_0402_1% PCH_SPI_D2
RC40/41 place to within 1100 mil of SPI0_MOSI/SPI0_IO2 pin for XDP

+3.3V_SPI — CC3 0.1U_0402_25V6

UC3 W25Q128JVSIQ_SO8
CS# WP# HOLD# GND VCC SCLK SI/SIO0 SO/SIO1

PCH_SPI_D2 — RC176 TPM@ 15_0402_5% — PCH_SPI_D2_R
PCH_SPI_D3 — RC177 TPM@ 15_0402_5% — PCH_SPI_D3_R
PCH_SPI_CS#0 — RC178 TPM@ 15_0402_5% — PCH_SPI_CS#0_R
PCH_SPI_CLK_R — RC178 TPM@ 15_0402_5% — PCH_SPI_CLK
PCH_SPI_IO0_R — RC179 TPM@ 15_0402_5% — PCH_SPI_D0
PCH_SPI_IO1_R — RC180 TPM@ 15_0402_5% — PCH_SPI_D1

RC178 TPM@ 33_0402_5% SD028330A80
RC177 TPM@ 33_0402_5% SD028330A80
RC178 TPM@ 33_0402_5% SD028330A80
RC179 TPM@ 33_0402_5% SD028330A80
RC180 TPM@ 33_0402_5% SD028330A80

128Mb Flash ROM
UC3 place colse to UX1

PCH_SPI_CLK — RC21 @EM@ 33_0402_5% — CC2 @EM@ 33P_0402_50V8J
place colse to UC3

Int. PD. +3VALW_PCH
SMB_ALERT# — RC37 2.2K_0402_5%

TLS CONFIDENTIALITY	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

Int. PD. +3VALW_PCH
GPP_C5 — RC38 4.7K_0402_5%

EC interface	
HIGH	ESPI
LOW(DEFAULT)	LPC

+3VALW_PCH
Modify Value to 150k for WW52 MOW
2015/03/03 Jason
GPP_B23 — RC39 CMC@ 150K_0402_5%

EXI BOOT STALL BYPASS	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

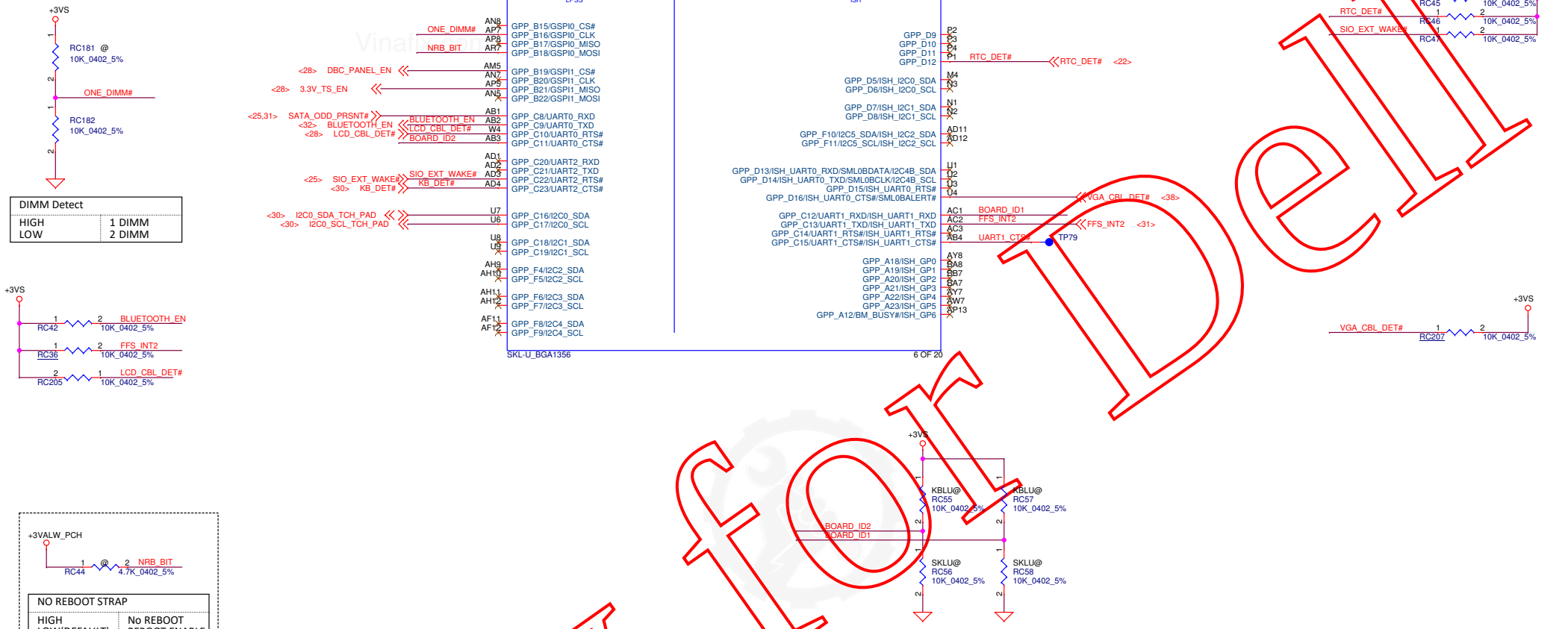
Compal Electronics, Inc.

Title: MCP(3/14)SPI,SMB,LPC

Size	Document Number	Rev
	LA-G714P	1.0

Date: Tuesday, November 13, 2018 | Sheet 8 of 65

Main Func = CPU



CPU ID (PCBA VRAM Size Config.)	BOARD_ID2 (GPP_C11)	BOARD_ID1 (GPP_C12)
KBL-U	1	1
KBL-R	1	0
Reserved	0	1
SKL-U	0	0

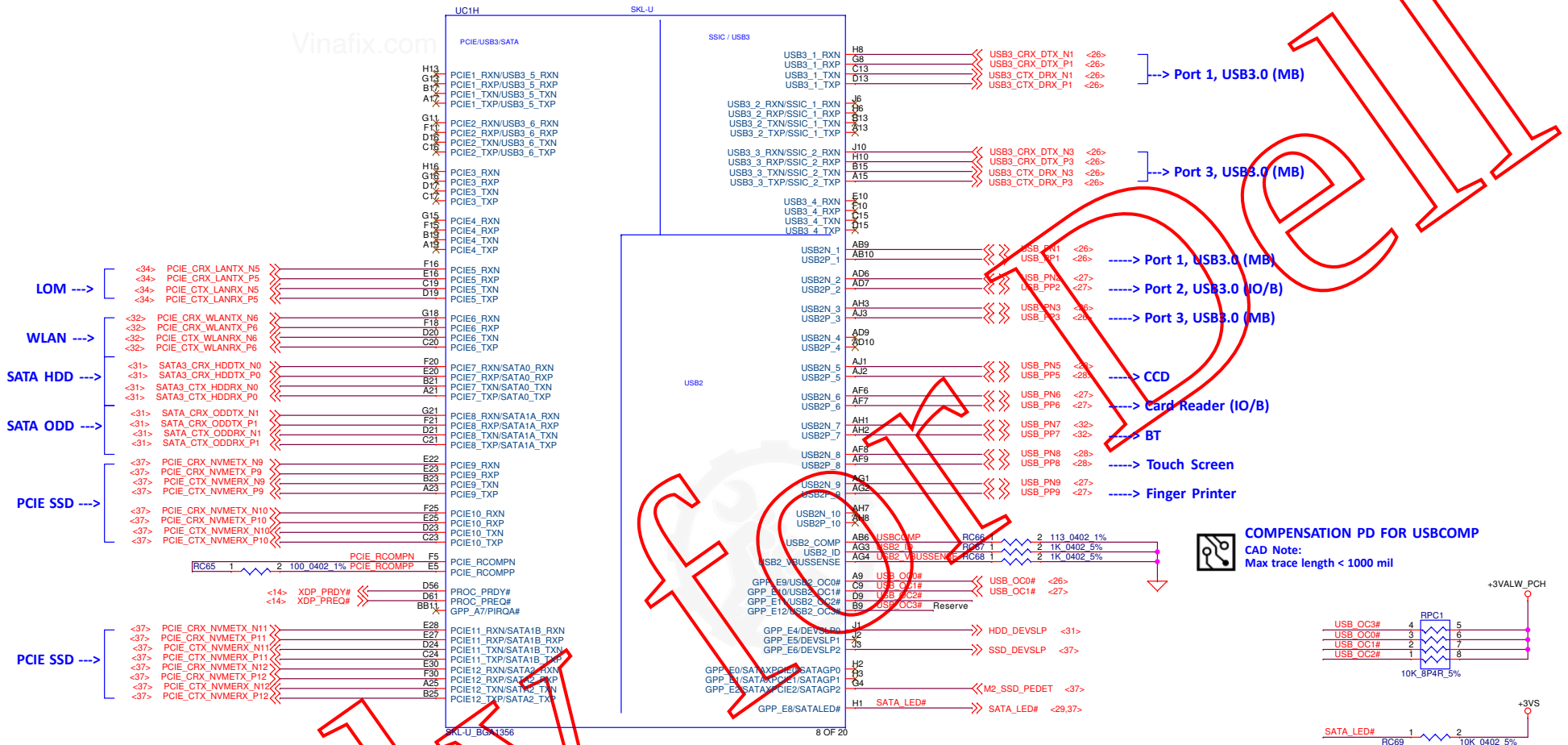
RC55 KBLR@ 10K_0402_5% SD028100280

RC58 KBLR@ 10K_0402_5% SD028100280

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.	
Title	MCP(4/14)GSPI,I2C,UART,ISH
Size	Document Number: LA-G714P
Rev	1.0
Date:	Tuesday, November 13, 2018
Sheet	9 of 65

Main Func = CPU

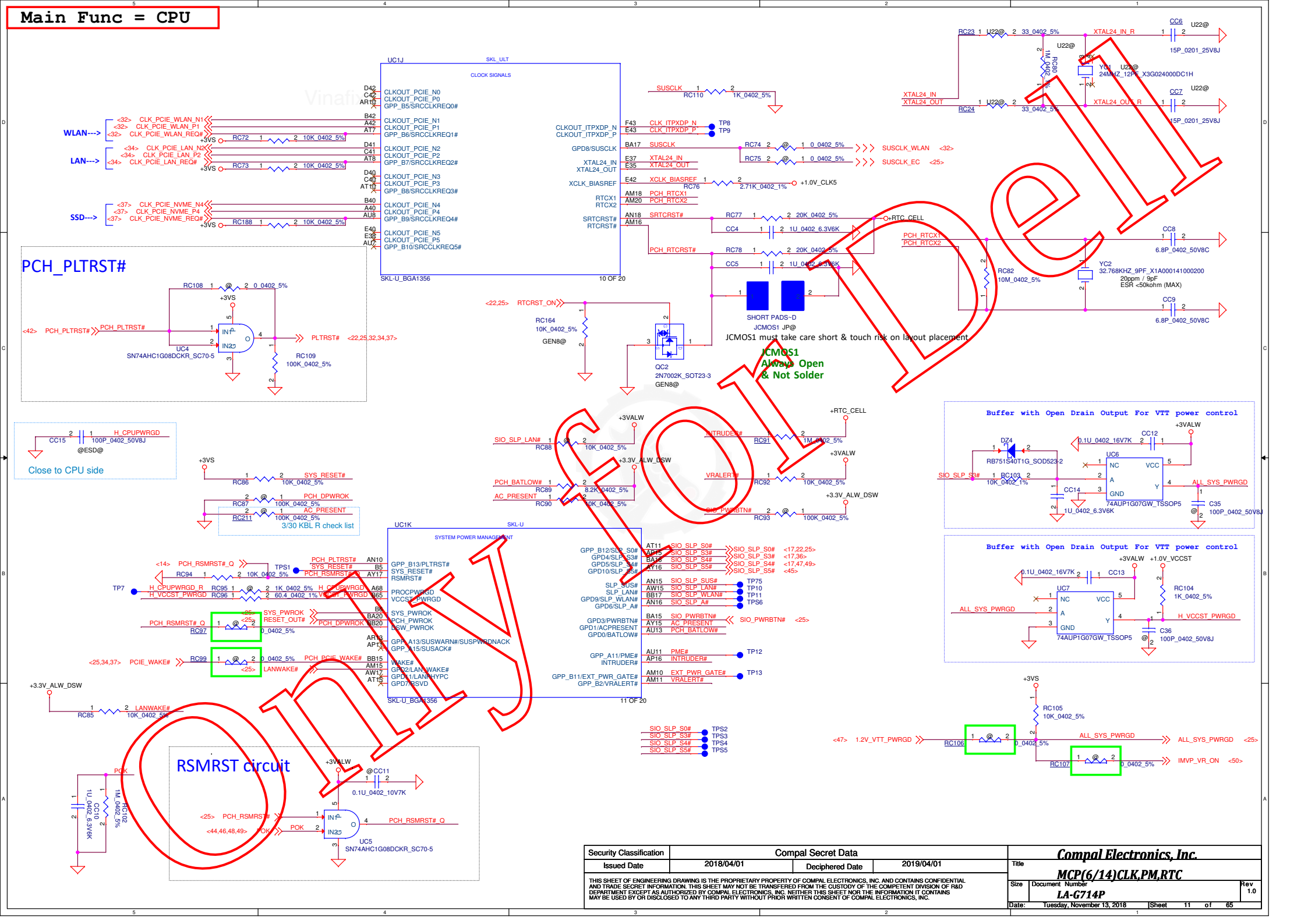


GPIO	Device Control
USB_OC0#	USB Port 1&Port3
USB_OC1#	USB Port 6
USB_OC2#	NA
USB_OC3#	NA

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.			
Title	MCP(5/14)PCIE,USB,SATA		
Size	Document Number	LA-G714P	Rev 1.0
Date: Tuesday, November 13, 2018	Sheet 10 of 65		

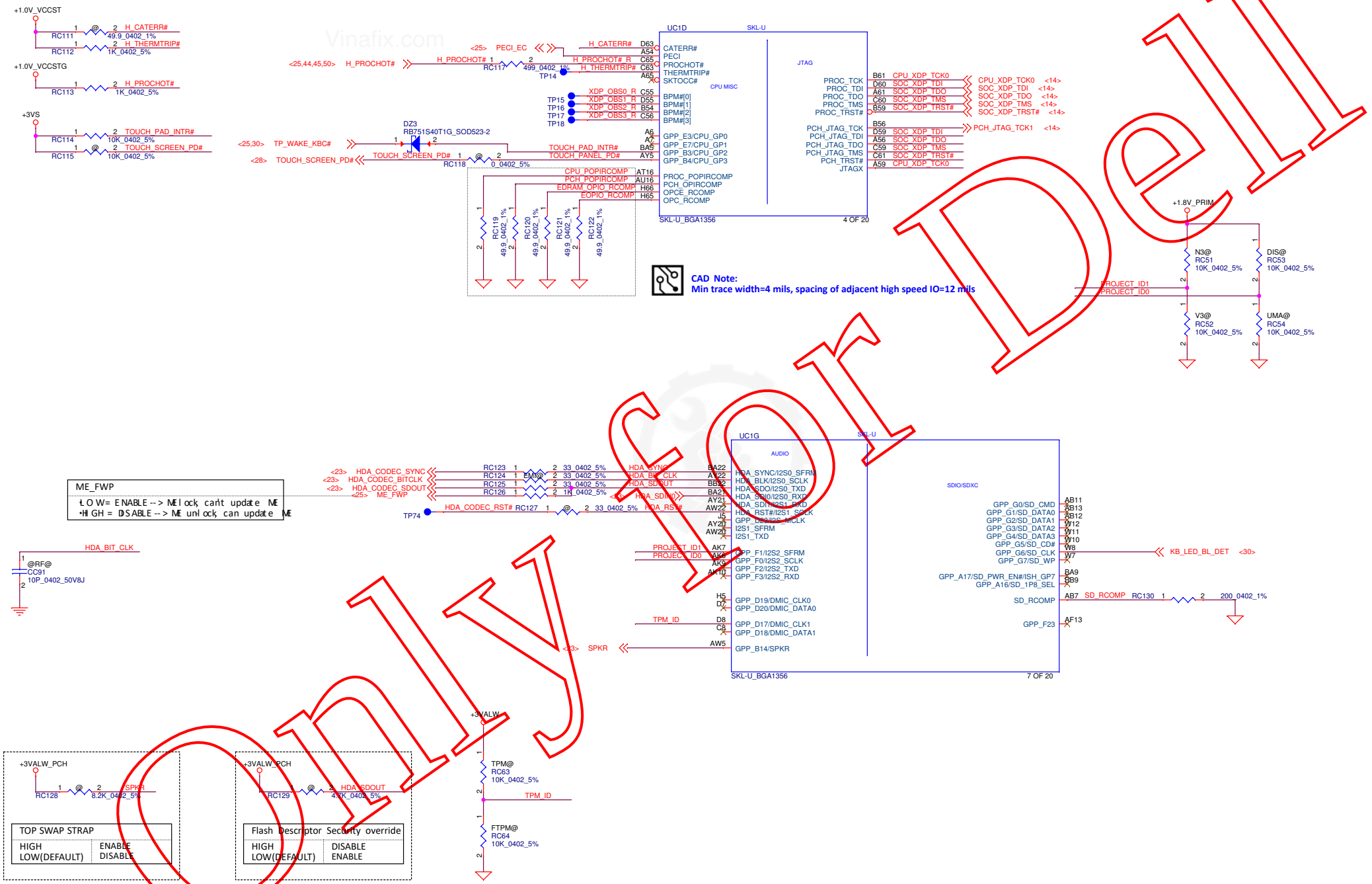
Main Func = CPU



Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Title	Compal Electronics, Inc.
	MCP(6/14)CLK,PM,RTC
Size	Document Number: LA-G714P
Rev	1.0
Date:	Tuesday, November 13, 2018
Sheet	11 of 65

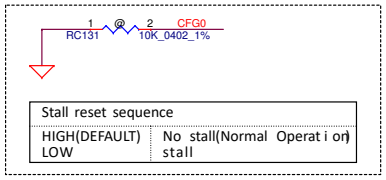
Main Func = CPU

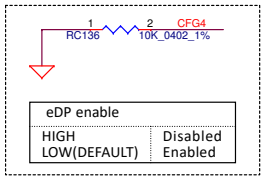


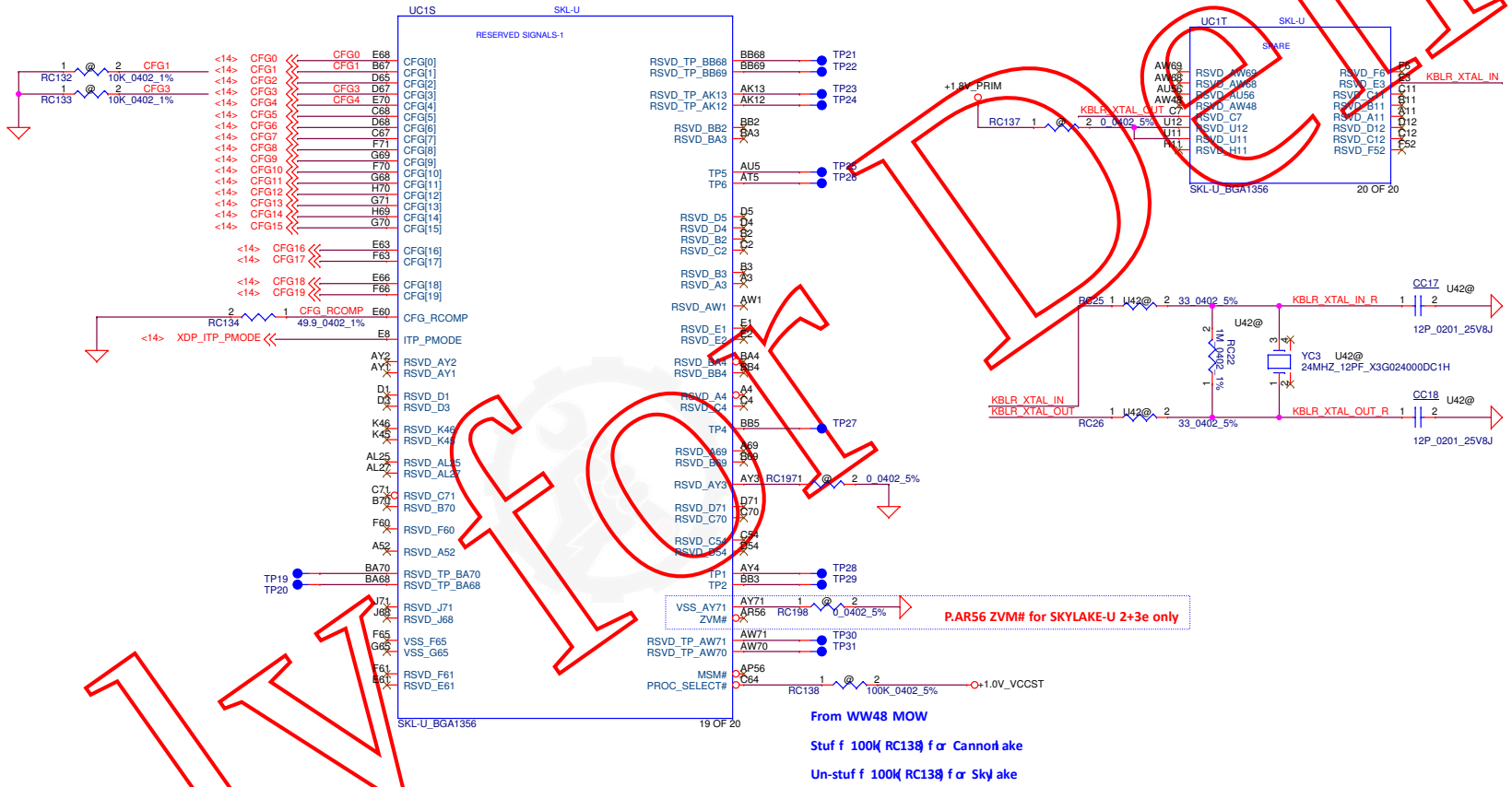
Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.		
Title	MCP(7/14)MISC,JTAG,HDA,SDIO	
Size	Document Number LA-G714P	Rev 1.0
Date: Tuesday, November 13, 2018	Sheet 12 of 65	

Main Func = CPU







Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

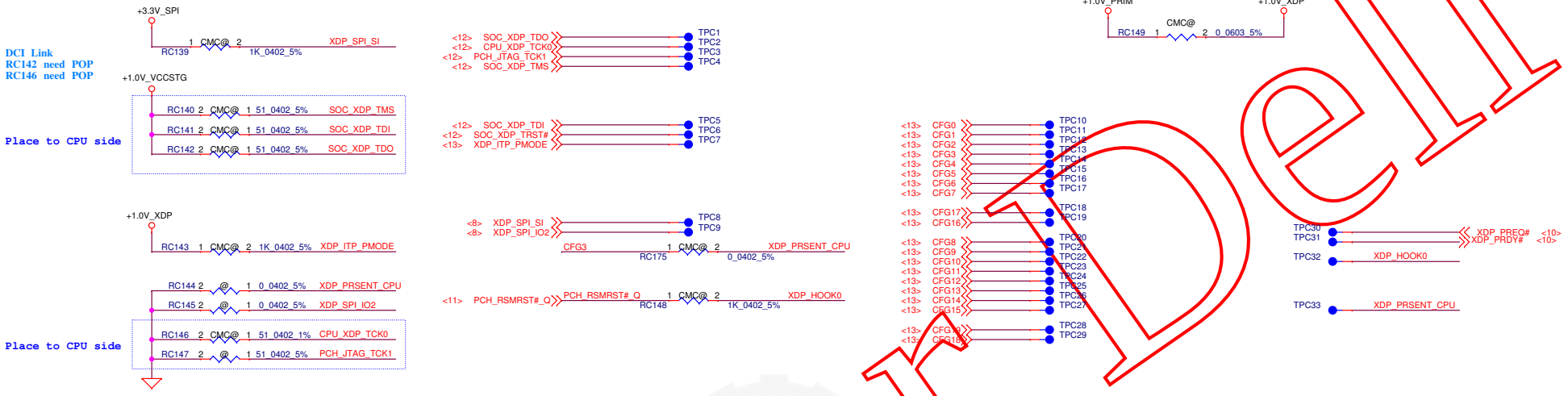
Title: MCP(8/14)CFG,RSVD

Size: | Document Number: LA-G714P | Rev: 1.0

Date: Tuesday, November 13, 2018 | Sheet 13 of 65

Main Func = CPU

Connector Less Routing Topology



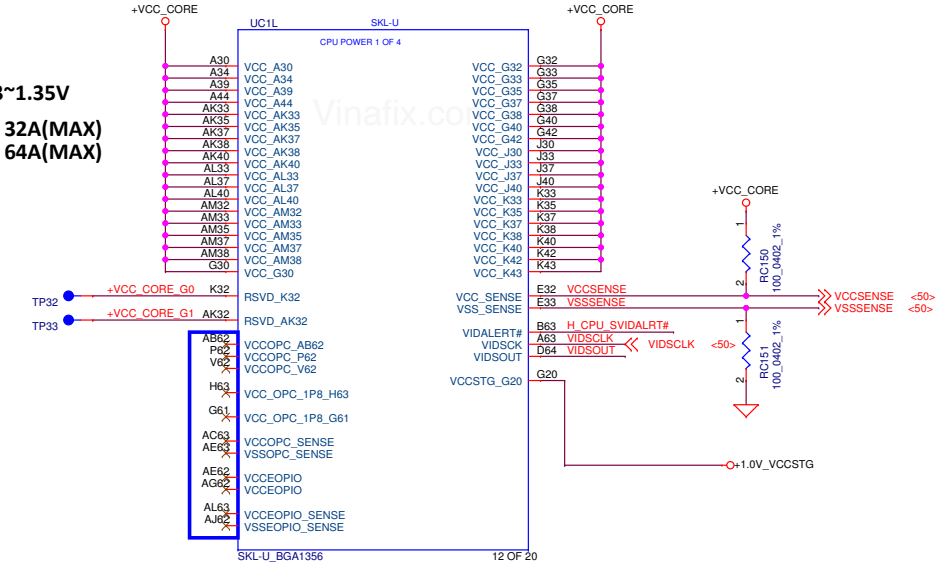
Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.		
Title: MCP(9/14)XDP		
Size	Document Number: LA-G714P	Rev: 1.0
Date: Tuesday, November 13, 2018	Sheet 14 of 65	

Main Func = CPU

+VCC_CORE: 0.3~1.35V

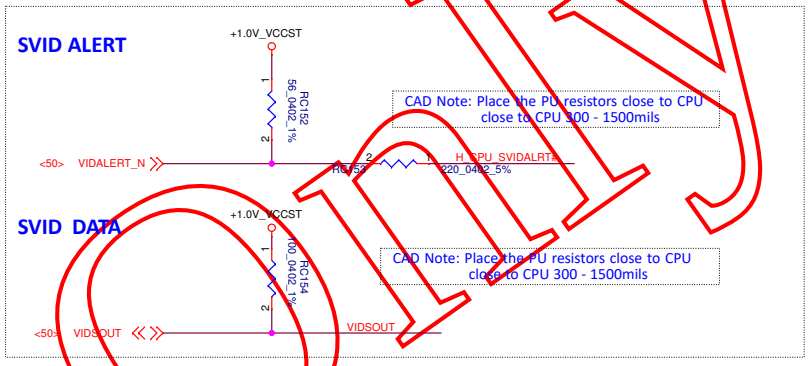
+VCC_CORE(U22): 32A(MAX)
+VCC_CORE(U42): 64A(MAX)



VCCOPC,VCCOPC_1P8,VCCEOPIO for SKYLAKE-U 2+3e
(w/ on package cache)

PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps >Power source



Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: MCP(10/14)PWR-VCC CORE

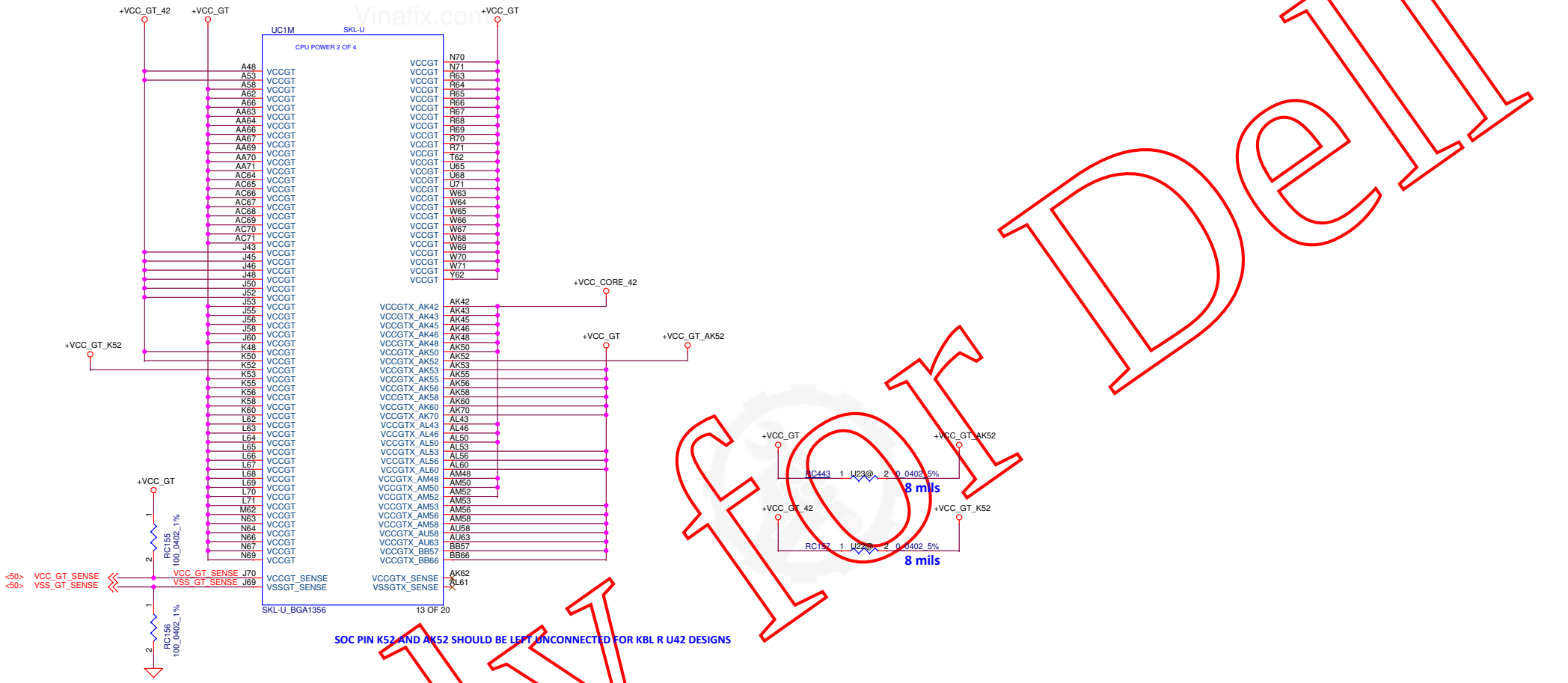
Size: | Document Number: LA-G714P | Rev: 1.0

Date: Tuesday, November 13, 2018 | Sheet 15 of 65

Main Func = CPU

+VCCGT: 0.3~1.35V
+VCCGTX : 0.3~1.35V

+VCC_GT(U22): 31A(MAX)
+VCC_GT(U42): 28A(MAX)



SOC PIN K52 AND AK52 SHOULD BE LEFT UNCONNECTED FOR KBL R U42 DESIGNS

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

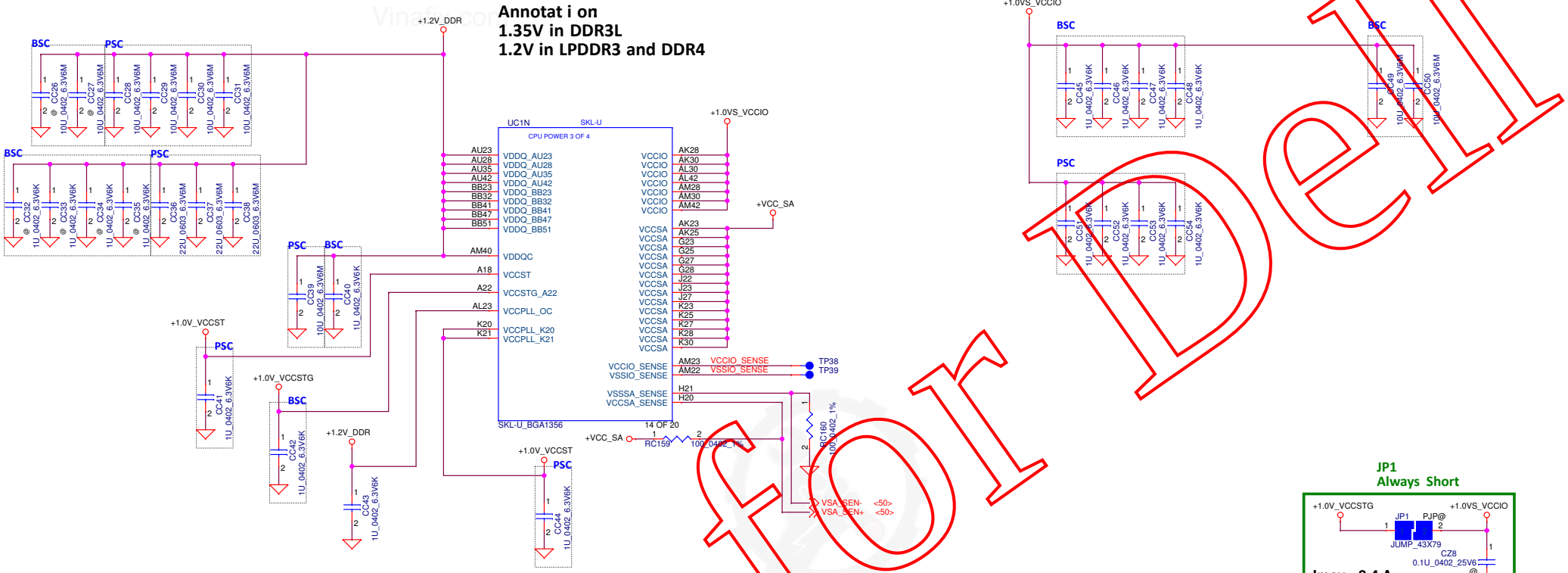
Title: MCP(11/14)PWR-VCCGT

Size | Document Number: LA-G714P | Rev: 1.0

Date: Tuesday, November 13, 2018 | Sheet 16 of 65

Main Func = CPU

Annotat i on
1.35V in DDR3L
1.2V in LPDDR3 and DDR4



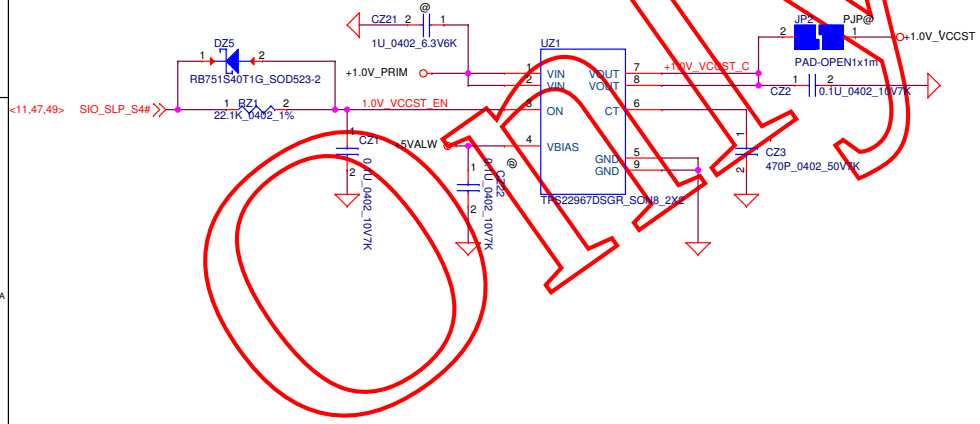
JP1
Always Short

Imax : 3.4 A
POP option with Volume

+1.0V_VCCST source

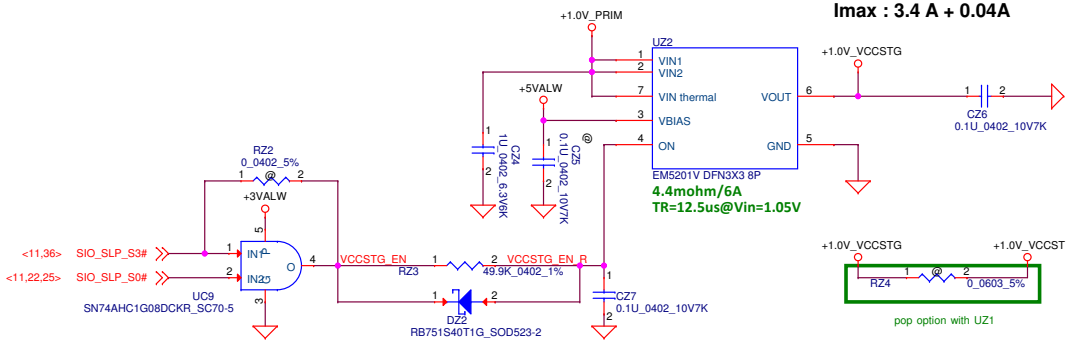
Imax : 0.24 A

JP2
Always Short



+1.0V_VCCSTG source

Imax : 3.4 A + 0.04A



Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: **MCP(12/14)PWR-VCCIO,MEM**

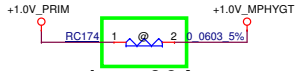
Size	Document Number	Rev
	LA-G714P	1.0

Date: Tuesday, November 13, 2018 | Sheet 17 of 65

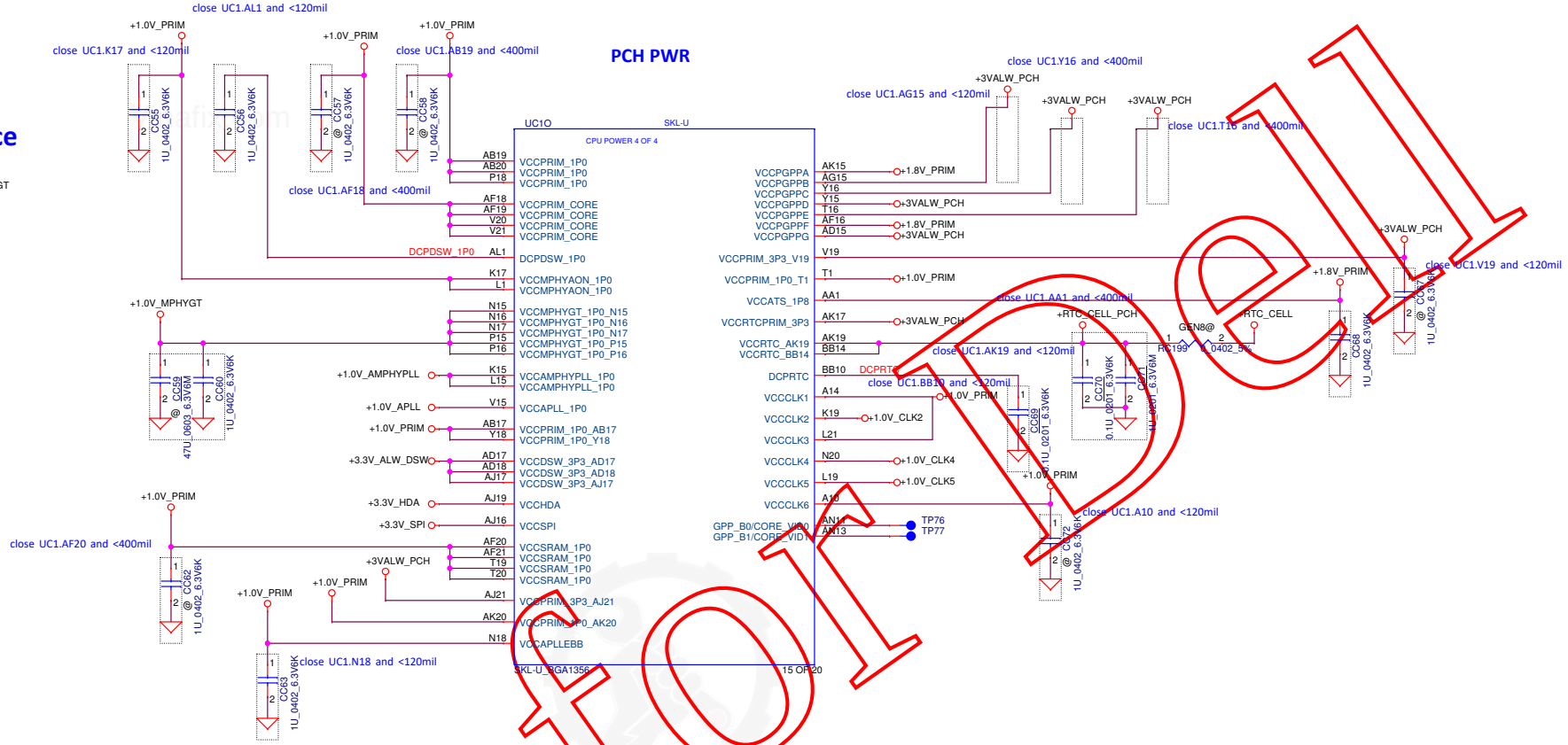
Main Func = CPU

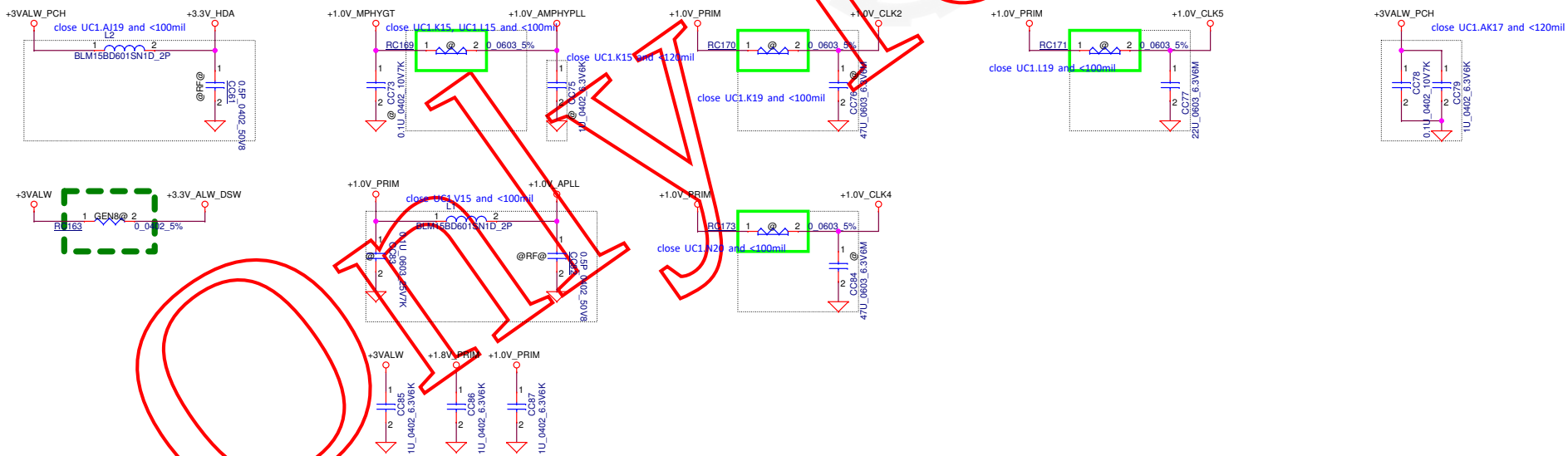
PCH PWR

+1.0V_MPHYGT source



Imax : 2.8 A

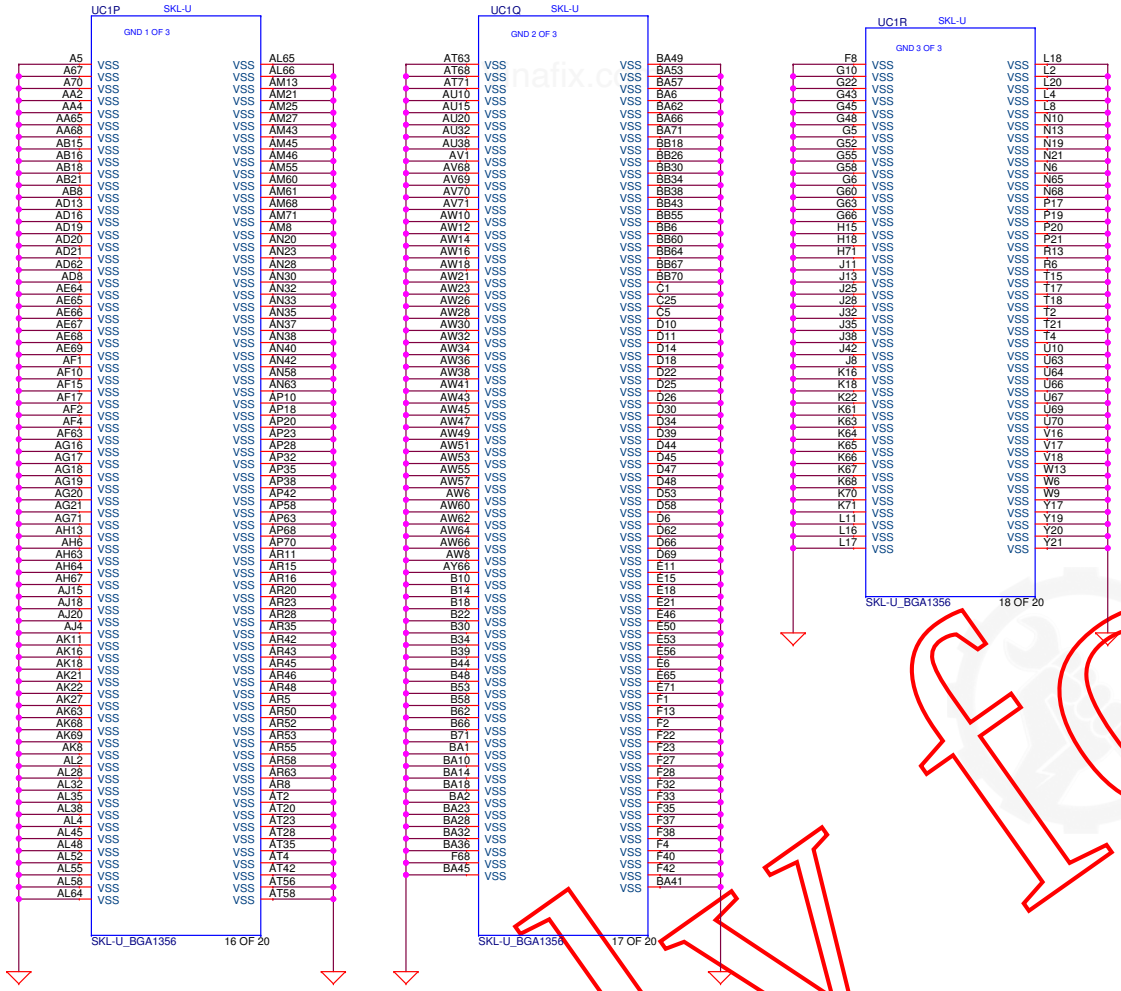




Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.			
Title	MCP(13/14)PCH PWR		
Size	Document Number		Rev
	LA-G714P		1.0
Date:	Tuesday, November 13, 2018	Sheet	18 of 65

Main Func = CPU



For Pre-ES Parts: Disconnect PCH CORE_VID[1:0] to the VR and fix PCH VCCPRIM_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: MCP(14/14)VSS

Size: | Document Number: LA-G714P | Rev: 1.0

Date: Tuesday, November 13, 2018 | Sheet 19 of 65

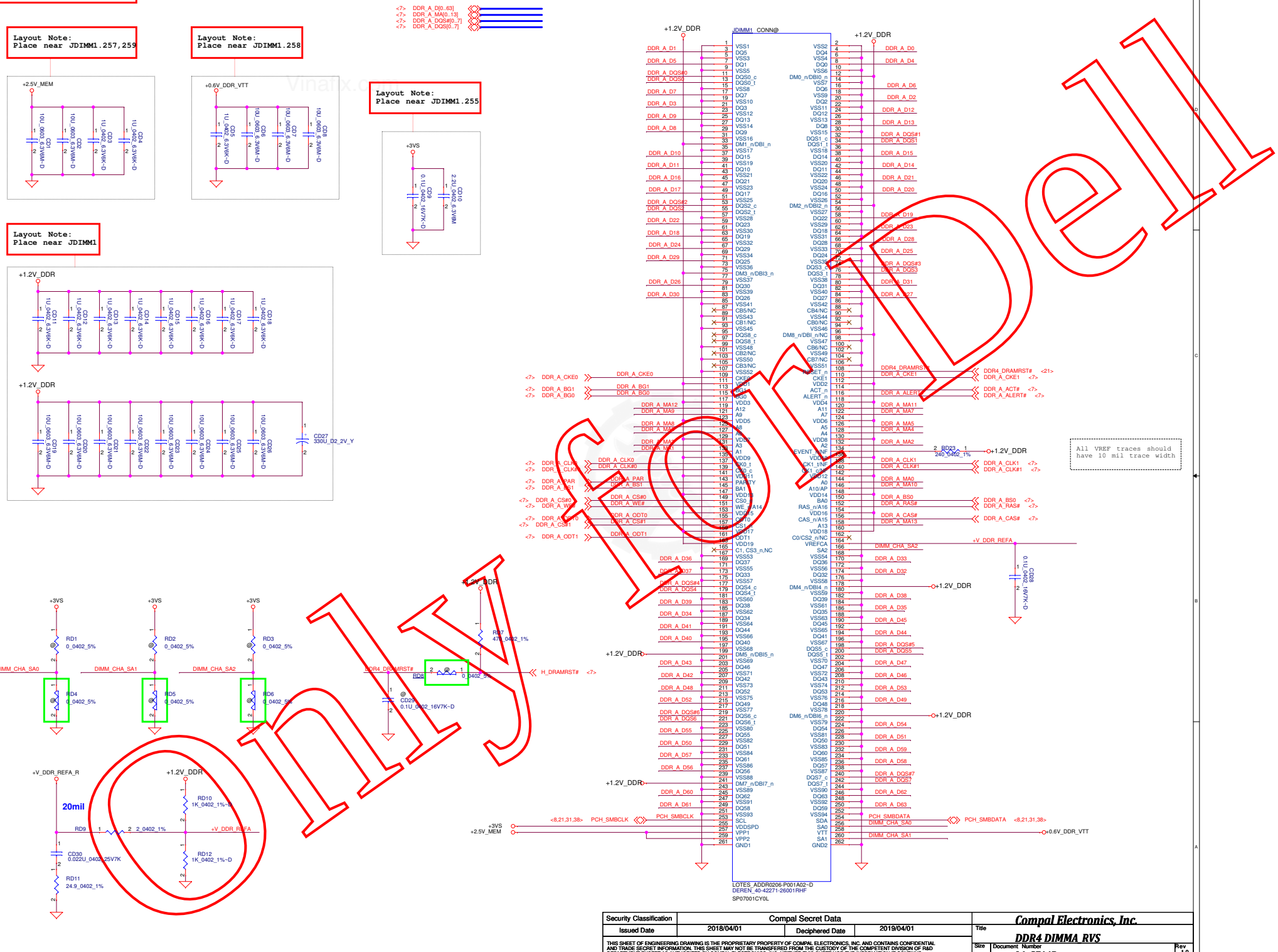
Main Func = DDR

Layout Note:
Place near JDIMM1.257,259

Layout Note:
Place near JDIMM1.258

Layout Note:
Place near JDIMM1.255

Layout Note:
Place near JDIMM1



Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: DDR4 DIMMA_RVS

Size	Document Number	Rev
	LA-G714P	1.0

Date: Tuesday, November 13, 2018 | Sheet 20 of 65

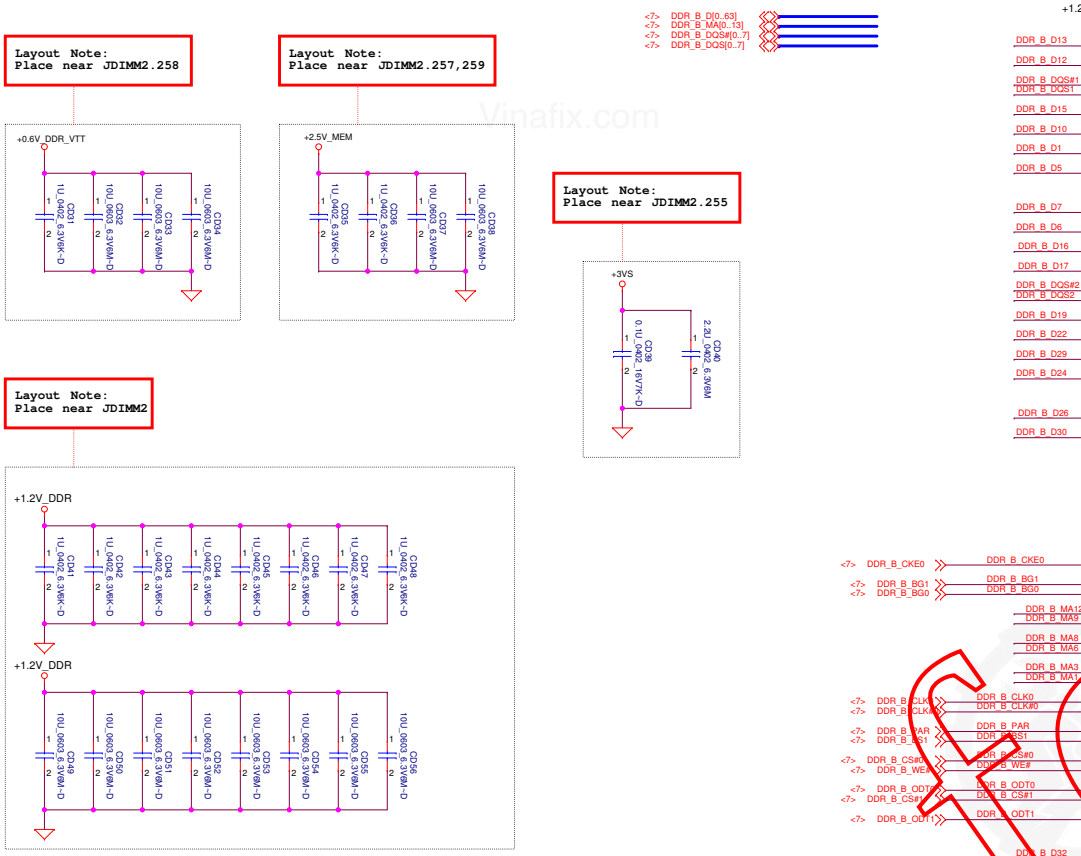
Main Func = DDR

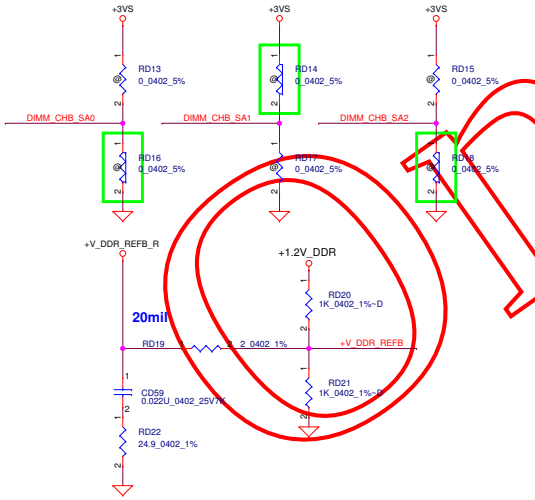
Layout Note:
Place near JDIMM2.258

Layout Note:
Place near JDIMM2.257,259

Layout Note:
Place near JDIMM2.255

Layout Note:
Place near JDIMM2





All VREF traces should have 10 mil trace width

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: **DDR4 DIMMB STD**

Size: | Document Number: **LA-G714P** | Rev: 1.0

Date: Tuesday, November 13, 2018 | Sheet 21 of 65

Main Func = TPM

Screw hole/FD

H1 HOLEA H_3P0
H2 HOLEA H_3P0
H3 HOLEA H_3P0
H4 HOLEA H_3P0
H5 HOLEA H_3P0
H6 HOLEA H_5P0
H7 HOLEA H_3P0
H8 HOLEA H_3P3
H12 HOLEA H_3P2
H13 HOLEA H_3P0X4P0
H14 HOLEA H_5P6N

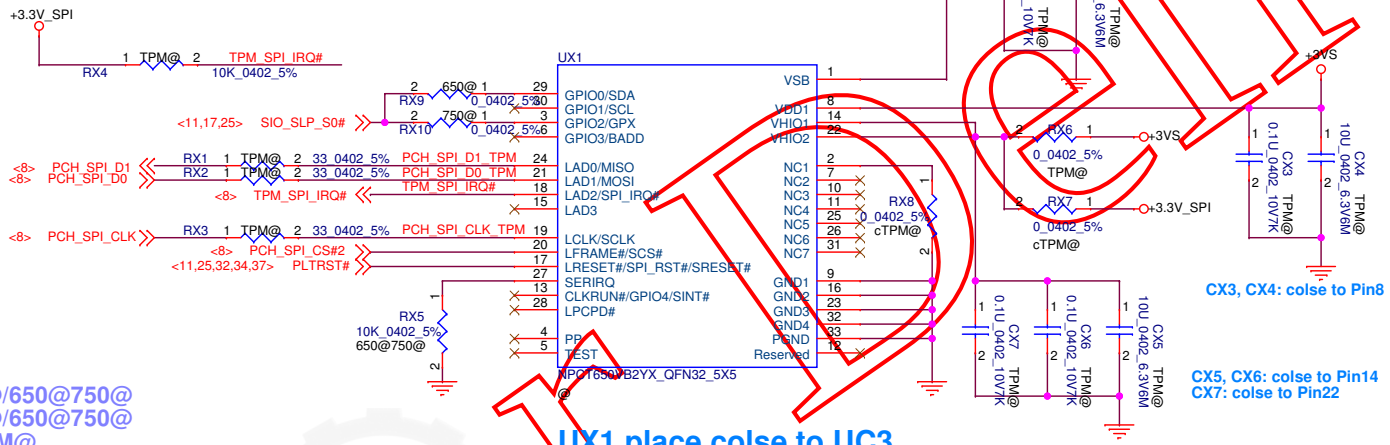
H12 WLAN STANDOFF

HCPU1 HOLEA H_4P0X3P7H_3P7
HCPU2 HOLEA H_4P0
HCPU3 HOLEA H_4P0
HCPU4 HOLEA H_4P0X3P7

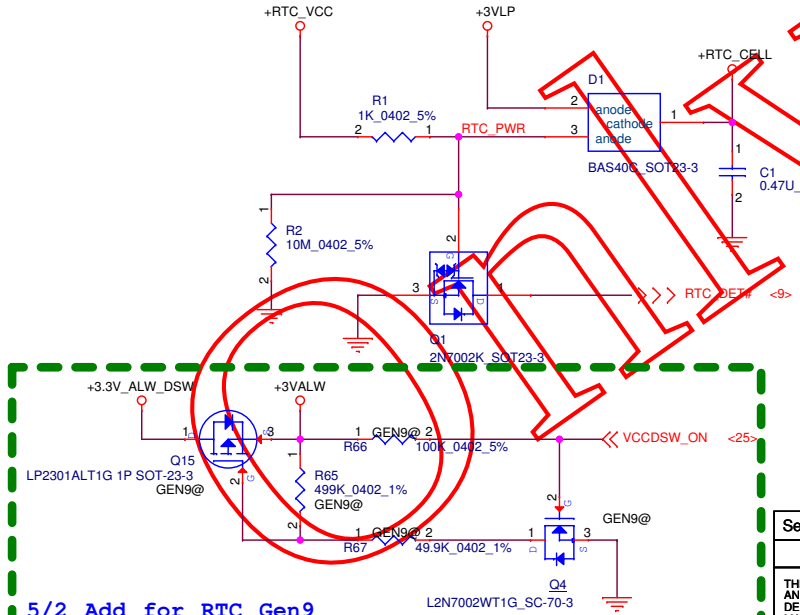
FD1 FD2 FD3 FD4

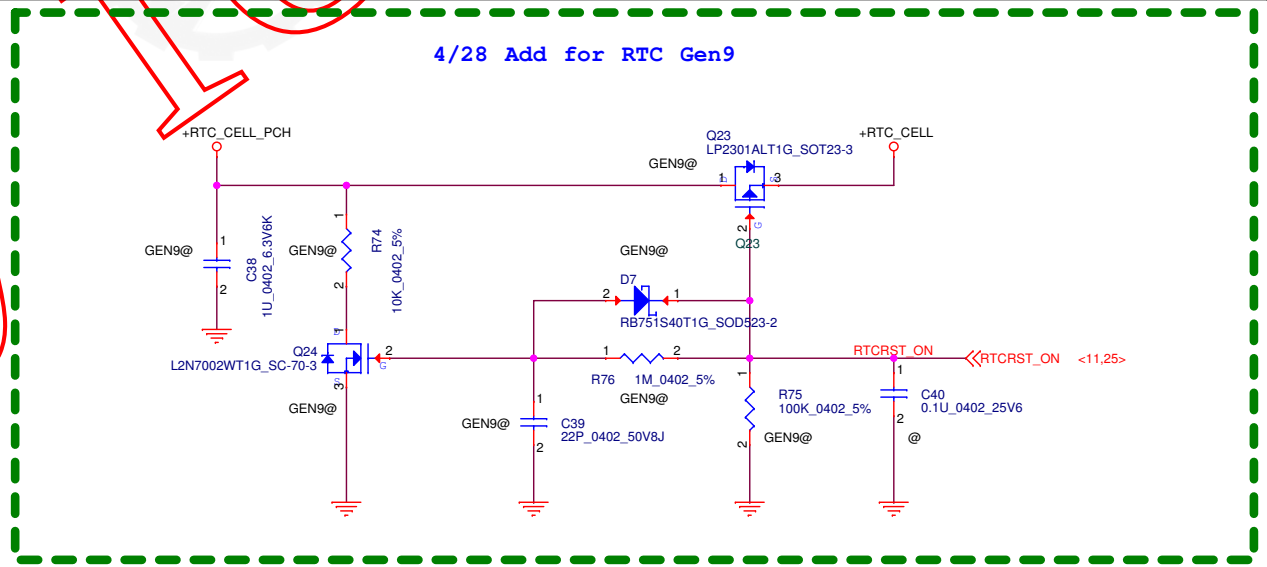
UX1 SA0000AQ270 TPM@
UX1 SA00008EL90 650@
S IC NPCT750JABYX QFN 32P TPM FW 7.2.1.0 S IC NPCT650VBBYX QFN 32P TPM

NPCT650:TPM@/650@/650@750@
NPCT750:TPM@/750@/650@750@
ChinaTPM:TPM@/cTPM@
SW TPM:fTPM@



Main Func = RTC





Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

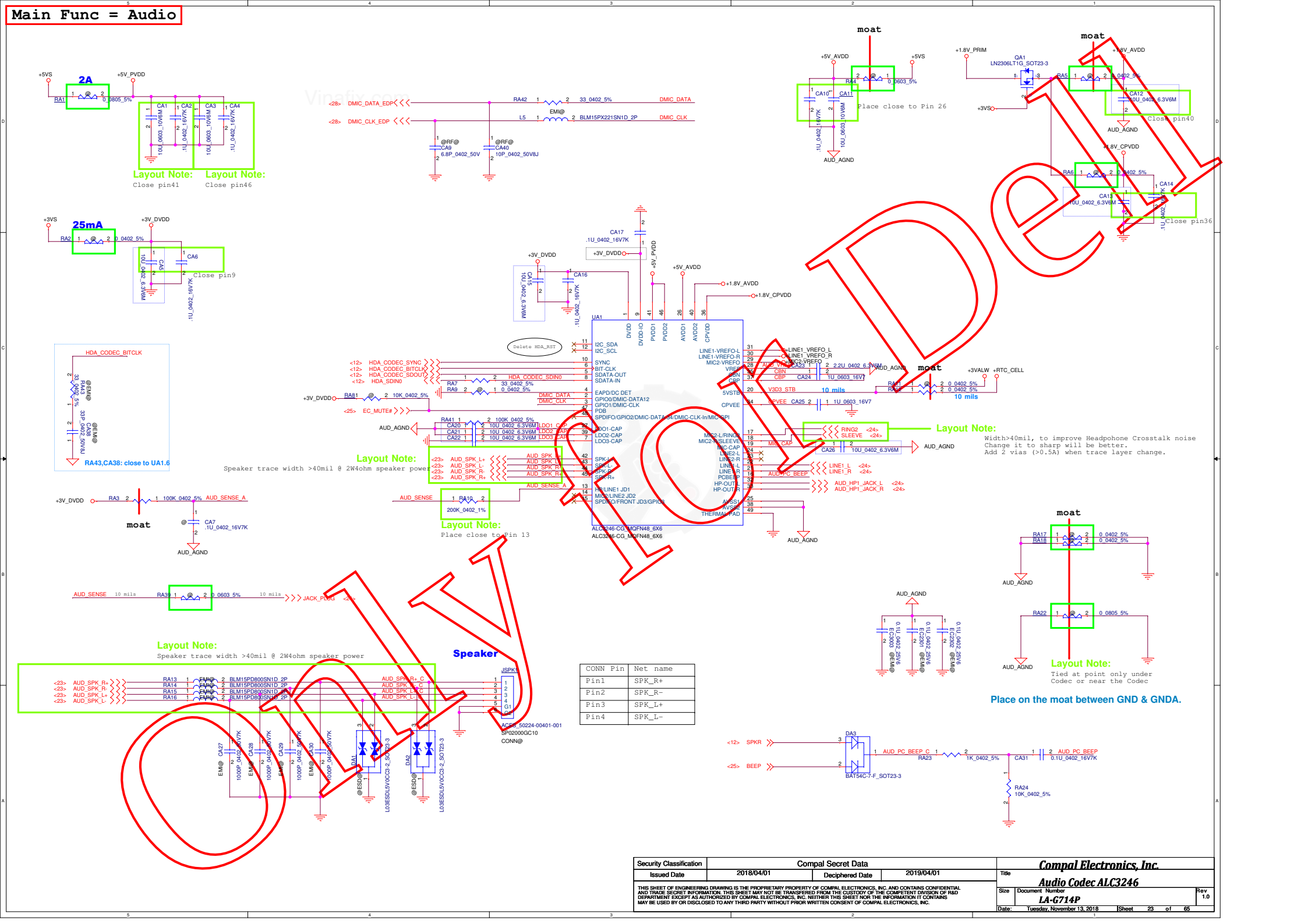
Compal Electronics, Inc.

Title: TPM/RTC/Screw hole

Size	Document Number	Rev
	LA-G714P	1.0

Date: Tuesday, November 13, 2018 Sheet 22 of 65

Main Func = Audio



CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

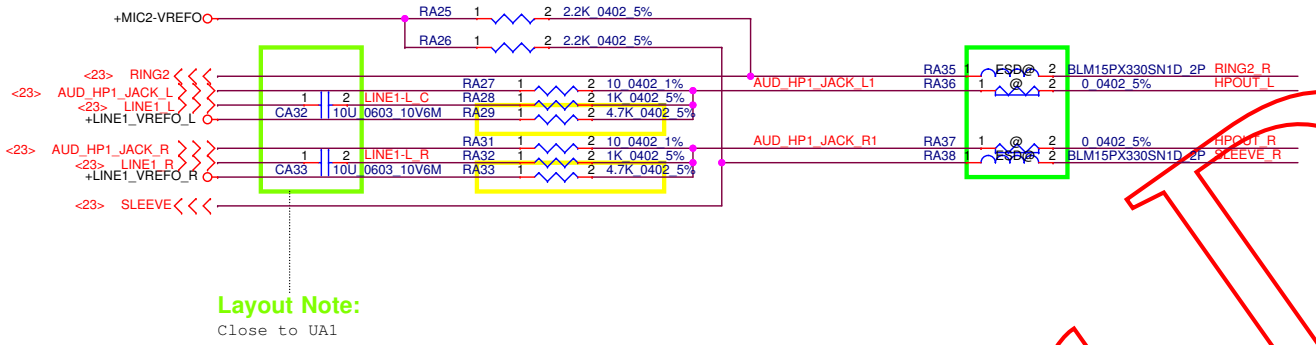
Compal Electronics, Inc.

Title: Audio Codec ALC3246

Size	Document Number	Rev
	LA-G714P	1.0

Date: Tuesday, November 13, 2018 Sheet 23 of 65

Main Func = Audio Jack

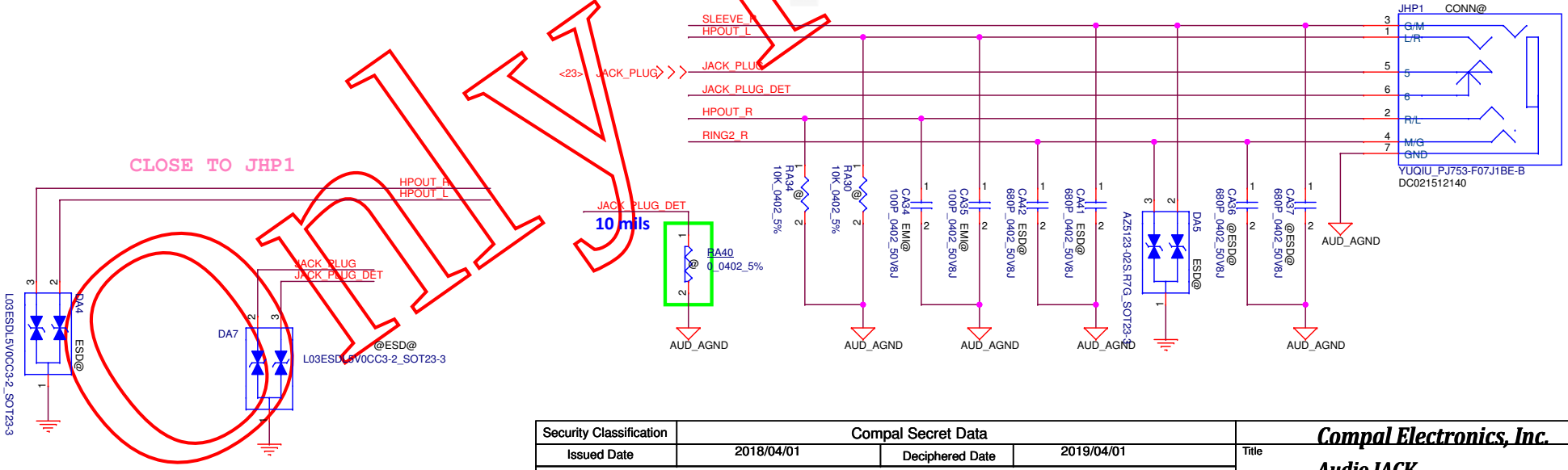


Layout Note:
Close to UA1

Universal Jack
(Global Headset Jack + mic phone in + line in support)

Main Func = Audio Jack

Universal Jack
(Global Headset Jack + mic phone in + line in support)



Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

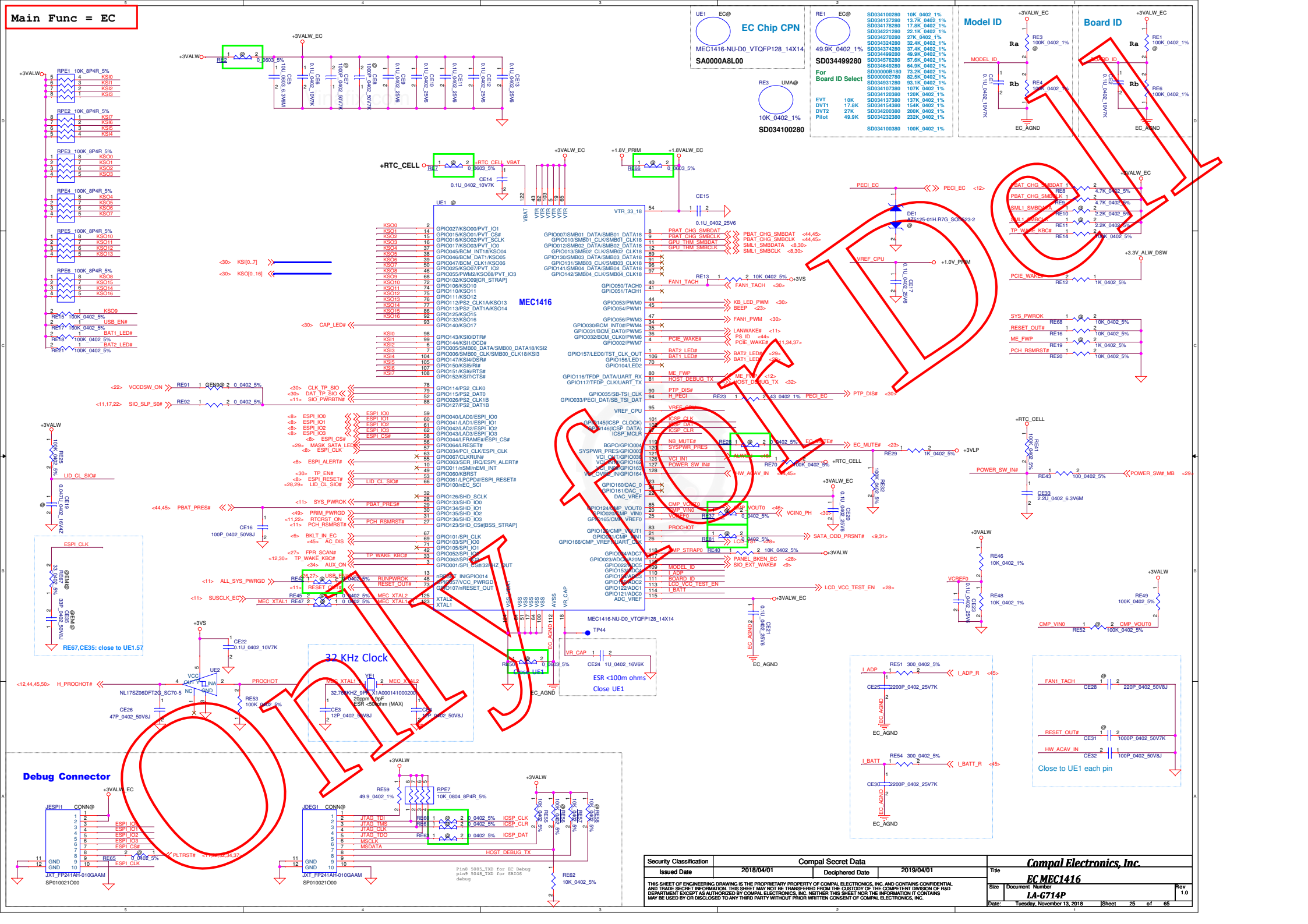
Compal Electronics, Inc.

Title: Audio JACK

Size	Document Number	Rev
	LA-G714P	1.0

Date: Tuesday, November 13, 2018 Sheet 24 of 65

Main Func = EC


EC Chip CPN
MEC1416-NU-D0_VTQFP128_14X14
SA0000A8L00
For Board ID Select
Model ID
Board ID
MEC1416
MEC1416-NU-D0_VTQFP128_14X14
32 KHz Clock
Debug Connector
RE67,CE35: close to UE1.57
Close UE1
ESR <100m ohms
Close UE1
Close to UE1 each pin
Pin8 5085_TXD for EC Debug
pin9 5048_TXD for SBIOS debug
SP010021O00
JXT_FP241AH-010GAAM
NL17SZ06DFT2G_SC70-5
32.768KHZ_9PF_X1A000141000200
200ppm
ESR <50kohm (MAX)
Security Classification
Compal Secret Data
Issued Date
2018/04/01
Deciphered Date
2019/04/01
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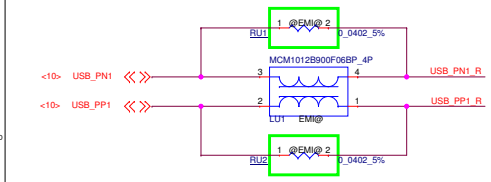
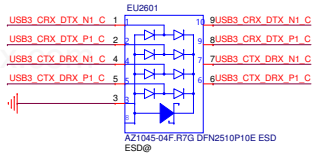
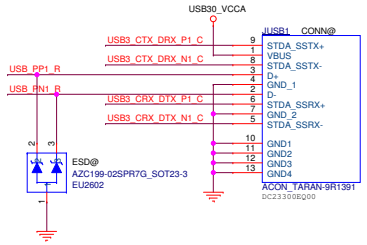
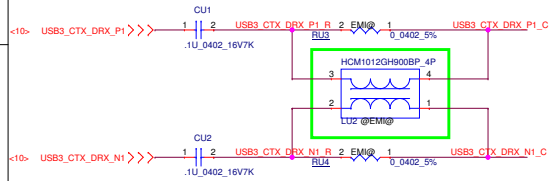
Compal Electronics, Inc.
Title
EC MEC1416
Size
Document Number
LA-G714P
Rev
1.0
Date: Tuesday, November 13, 2018
Sheet 25 of 65

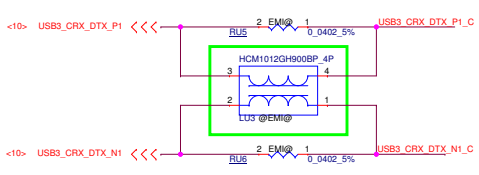
Main Func = USB3.0 Port1



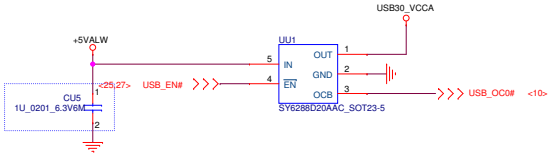


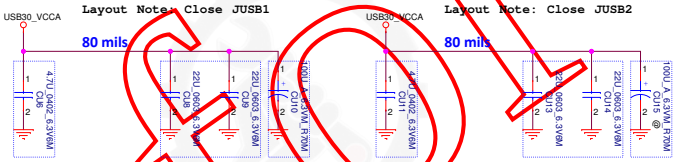




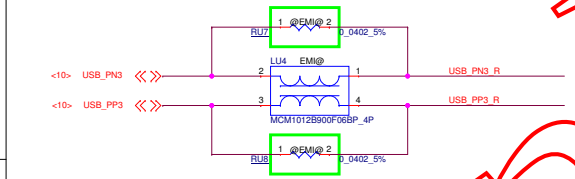


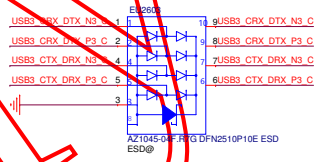
Maximum Output Current 2A

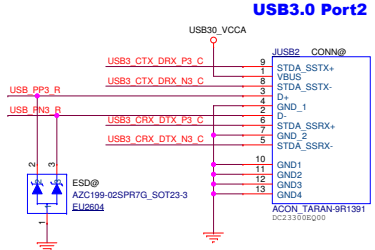


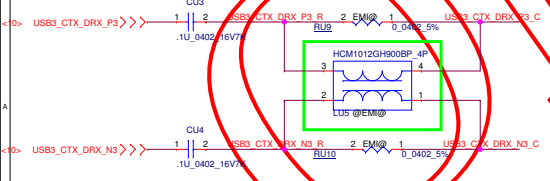


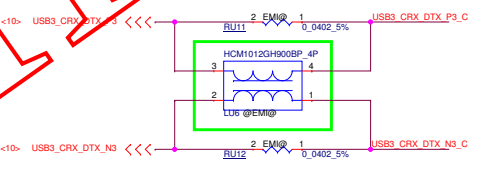
Main Func = USB3.0 Port2











Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

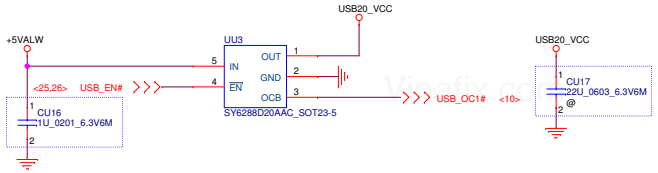
Title: USB3.0 CONN

Size | Document Number: LA-G714P | Rev: 1.0

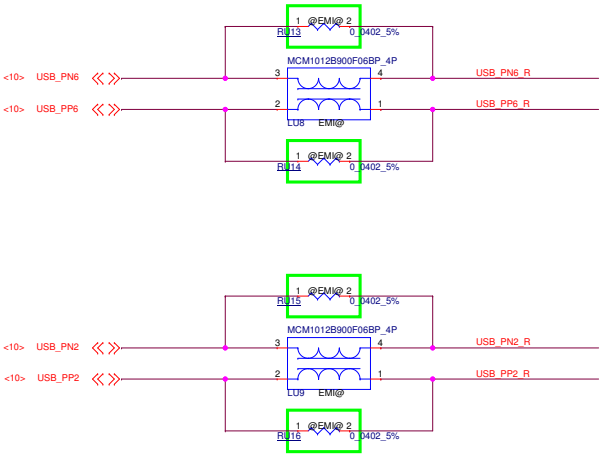
Date: Tuesday, November 13, 2018 | Sheet 26 of 65

Main Func = USB2.0 + Card Reader on IO/B

SY6288D Support 2A

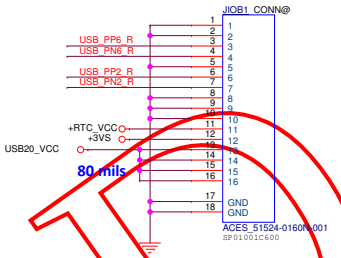


CardReader

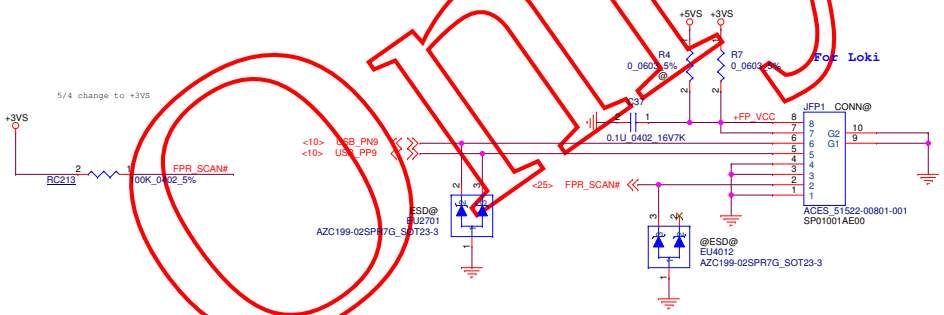


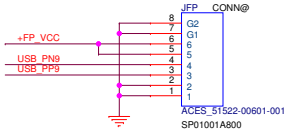
I/O Board Connector

CardReader



Main Func = Finger Printer





Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: FP/IO Board

Size | Document Number: LA-G714P | Rev: 1.0

Date: Tuesday, November 13, 2018 | Sheet 27 of 65

Main Func = LCD

INVERTER POWER

JEDP1 CONN@
ACES_51540-04001-P01
SP010029F00

+DCBAT_LCD
Trace width = 60mil
+LCDVDD_LCD
LCD_TST_C
DBC_PANEL_EN_R
EDP_HPD <6>
LCD_CBL_DET# <9>
EDP_AUX
EDP_AUX#
EDP_TX0#
EDP_TX0
EDP_TX1#
EDP_TX1
IR_GND
LCD_BRIGHTNESS
BLON_OUT_C
+3VS_CAM
DMIC_DATA_EDP <23>
DMIC_CLK_EDP <23>
USB_CAMERA_EDP#
USB_CAMERA_EDP
USB_PN8_TPNL
USB_PP8_TPNL
TP_EN
+TPAN_VDD

C2 0.1U_0402_16V7K
C3 1U_0402_10V6K
C12 10P_0402_50V8J

+LCDVDD_LCD → R3 0_0805_5% → +LCDVDD

EE note: Never change R3 to short pad after MP

+19VB → F1 1.5A_24V_SMD1812P150TF-24 → +DCBAT_LCD
850mA
C4 0.1U_0603_50V7K
C5 1000P_0402_50V7K

+3VS → R5 10K_0402_5%
DBC_PANEL_EN_R → R6 0_0402_5% → DBC_PANEL_EN <9>

RP1 100K_8P4R_5%
BKLT_CTRL
BLON_OUT_C
EDP_HPD

RP2 100_8P4R_5%
BLON_OUT_C
LCD_BRIGHTNESS
LCD_TST_C
BKLT_CTRL
LCD_TST
PANEL_BKEN_EC <25>

R9 0_0402_5%
D3 BAT54C-7-F_SOT23-3
eDP_BKLT_CTRL
LCD_TST → LCD_TST <25>

EC (BIST MODE)

<6> EDP_TX0_DN / EDP_TX0_DP → C6 C7 0.1U_0402_16V7K → EDP_TX0# / EDP_TX0
<6> EDP_TX1_DN / EDP_TX1_DP → C8 C9 0.1U_0402_16V7K → EDP_TX1# / EDP_TX1
<6> EDP_AUX_DN / EDP_AUX_DP → C10 C11 0.1U_0402_16V7K → EDP_AUX# / EDP_AUX

Brightness
<6> L_BKLT_CTRL → R8 0_0402_5% → eDP_BKLT_CTRL

+3VS → C17 1U_0402_6.3V6K
U1 SY6288C20AAC_SOT23-5
40mil
LCDVDD
R57 100K_0402_5%

<6> EDP_VDD_EN
<25> LCD_VCC_TEST_EN
D4 BAT54C-7-F_SOT23-3
R10 100K_0402_5%
LCDVDD_EN

High Active
EC (BIST MODE)

Main Func = CAM

EE note: Never change R16 to short pad after MP

+3VS → R16 0_0603_5% → +3VS_CAM
SP040007G00
S FUSE T0603FF1000TM 1A 65V UL FAST
C14 33P_0402_50V8J
C15 4.7U_0402_6.3V6M

R17 @EMI@ 0_0402_5%
MCM1012B900F06BP_4P
USB_CAMERA_EDP# → USB_PN5 <10>
USB_CAMERA_EDP → USB_PP5 <10>
L2 @EMI@
R18 @EMI@ 0_0402_5%

Main Func = TS

Touch Panel
<25,29> LID_CL_SIO#
D5 RB551V-30_SOD323-2
TP_EN → R19 33_0402_5% → TOUCH_SCREEN_PD# <12>
C16 10P_0402_50V8J

USB_PN8_TPNL → R20 EMI@ 0_0402_5% → USB_PN8 <10>
USB_PP8_TPNL → R21 EMI@ 0_0402_5% → USB_PP8 <10>
MCM1012B900F06BP_4P
L4 @EMI@

USB_PN8_TPNL
USB_PP8_TPNL
DA6 @ESD@
AZC199-02SPR7G_SOT23-3

+3VS → R11 0_0603_5%
+5VS → R12 0_0603_5%
TPAN_VDD_F → F2 S FUSE T0603FF1000TM 1A 65V UL FAST → +TPAN_VDD
R13 0_0603_5%

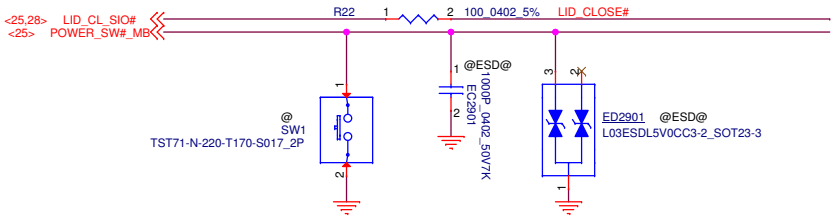
EE note: Never change R12/R13 to short pad after MP

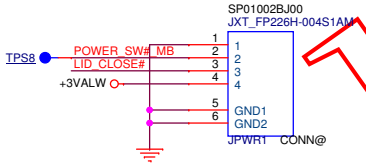
+TPAN_VDD_F
C31 MODS@ 1U_0402_10V6K
40mil
U3 SY6288C20AAC_SOT23-5 MODS@
40mil
+TPAN_VDD
<9> 3.3V_TS_EN
R72 MODS@ 100K_0402_5%
R30 MODS@ 10K_0402_5%
+TPAN_VDD_F

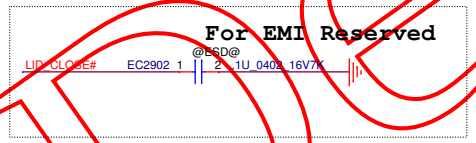
Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.
Title: LCD/Cam/MIC/T.Panel
Size: Document Number: LA-G714P
Rev: 1.0
Date: Tuesday, November 13, 2018 Sheet 28 of 65

Main Func = Power BTN



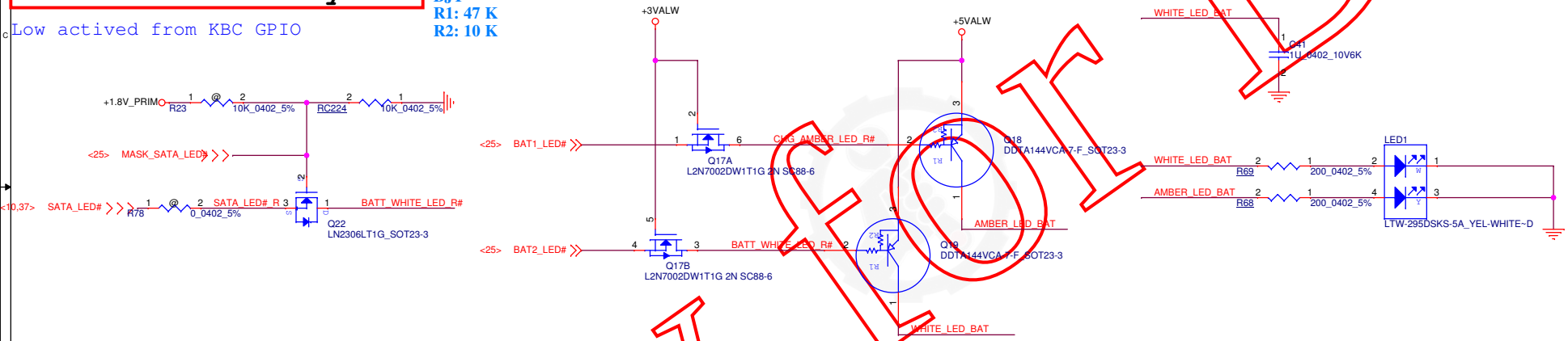


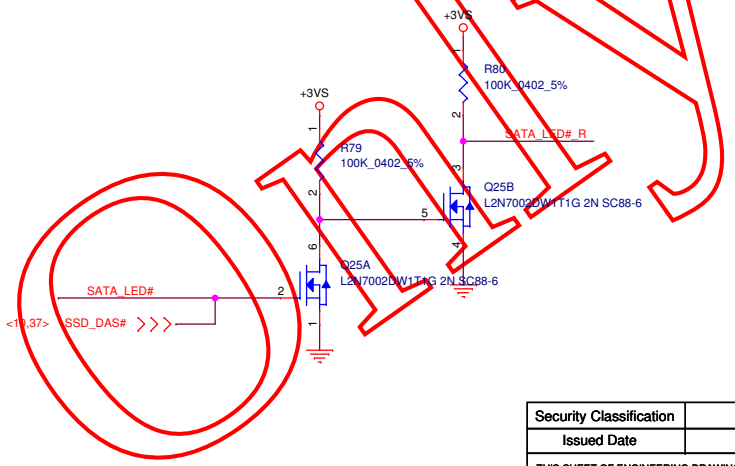


Main Func = Battery LED

BJT
R1: 47 K
R2: 10 K

Low actived from KBC GPIO





Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

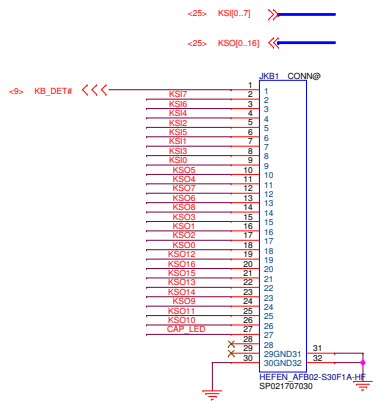
Compal Electronics, Inc.

Title: LED Board/Power Button

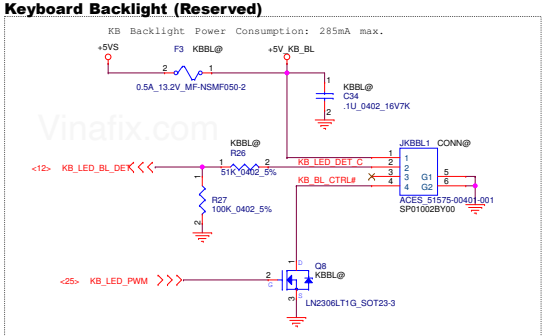
Size	Document Number	Rev
	LA-G714P	1.0

Date: Tuesday, November 13, 2018 Sheet 29 of 65

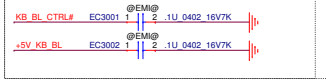
Main Func = KB



Keyboard Backlight (Reserved)

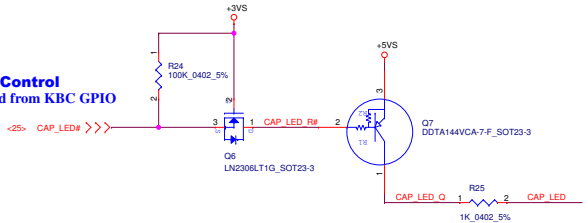


For EMI Reserved



CAP LED Control

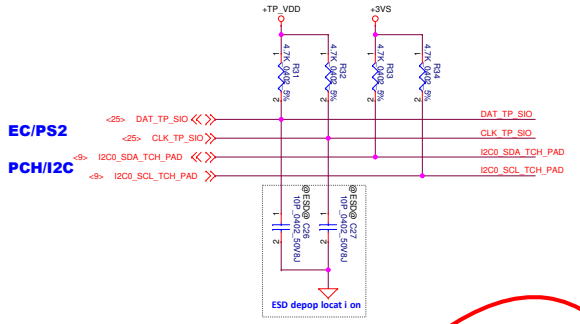
LOW actived from KBC GPIO

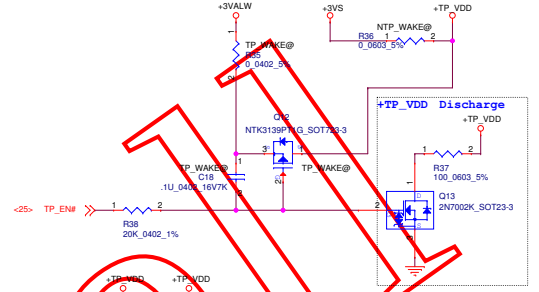


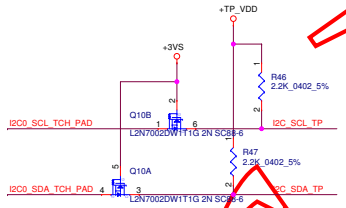
Main Func = TPAD

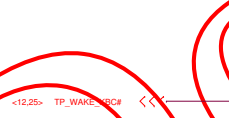
EC/PS2

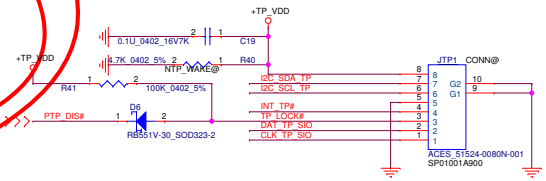
PCH/I2C



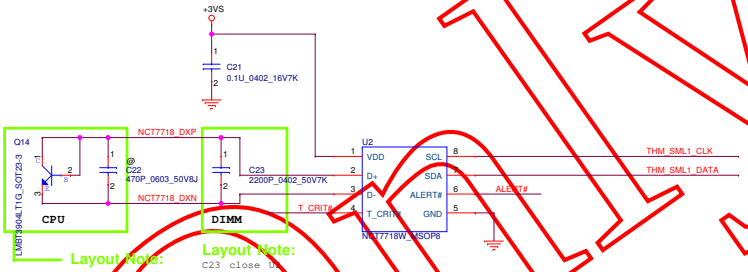


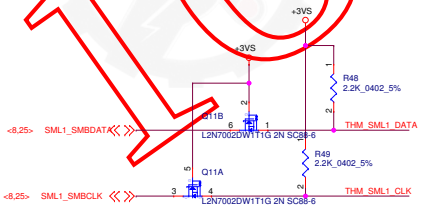


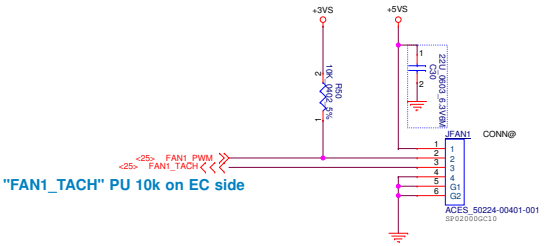


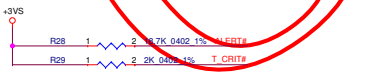


Main Func = Thermal







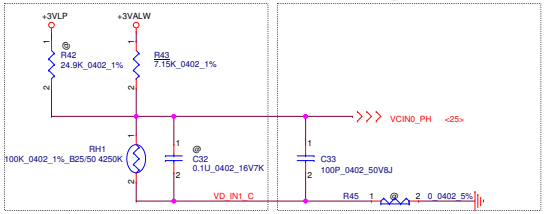


TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

Main Func = OTP

Close to Thermal sensor

Close to KBC
VD_IN1 for system thermal sensor



Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

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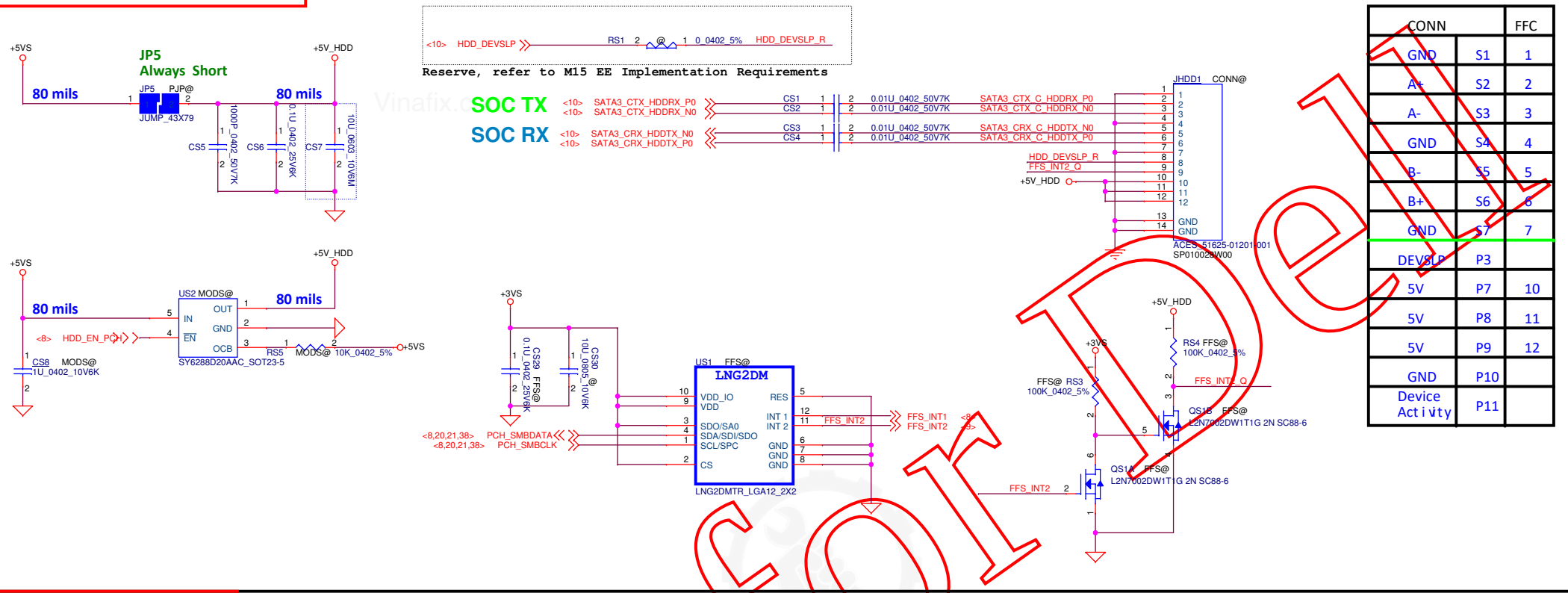
Compal Electronics, Inc.

Title: Keyboard/Touch Pad/Thermal/FAN

Size: | Document Number: LA-G714P | Rev: 1.0

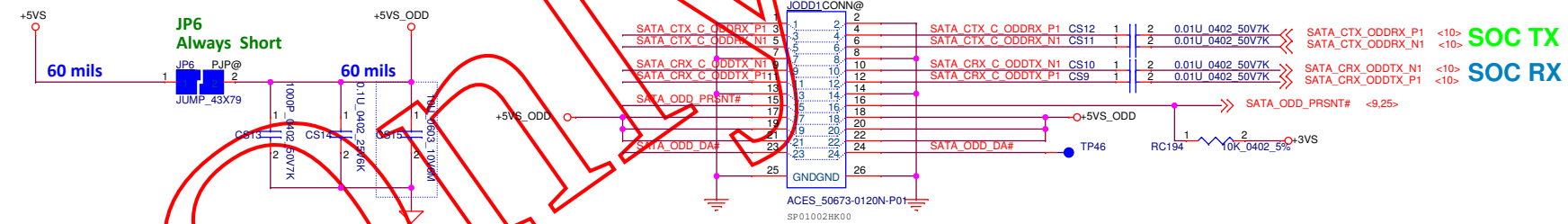
Date: Tuesday, November 13, 2018 | Sheet 30 of 65

Main Func = HDD&FFS



CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
DEVSLP	P3	
5V	P7	10
5V	P8	11
5V	P9	12
GND	P10	
Device Activity	P11	

Main Func = ODD



CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
PRSNT	P1	8
5V	P2	9
5V	P3	10
Attentio	P4	11
GND	P5	12
GND	P6	

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

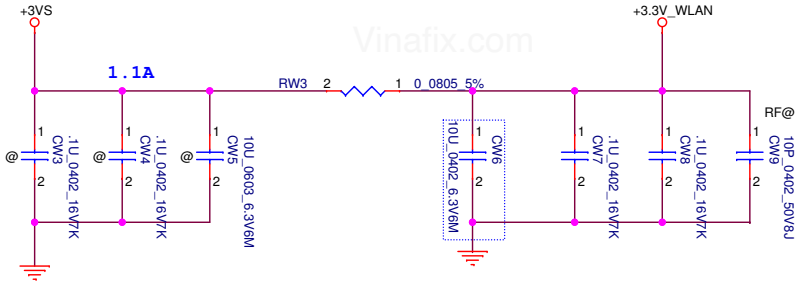
Title: **HDD/FFS/ODD**

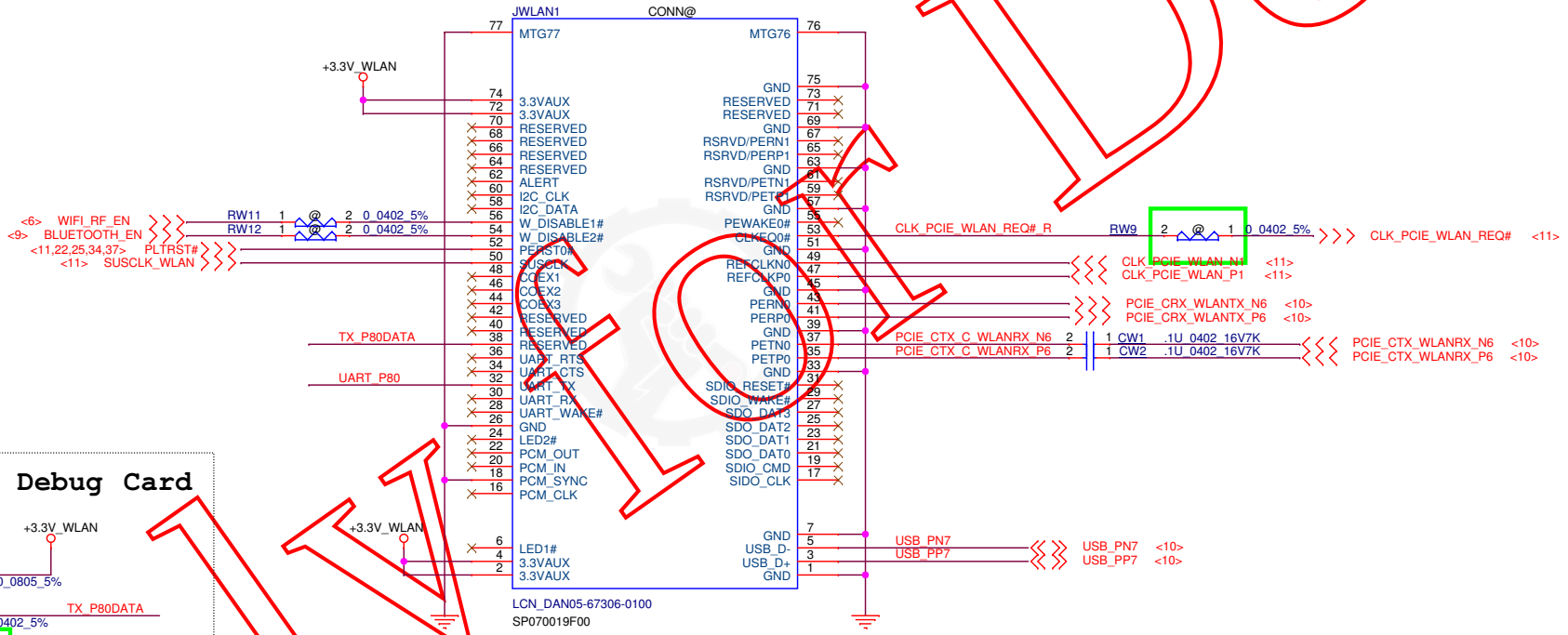
Size | Document Number: **LA-G714P** | Rev: 1.0

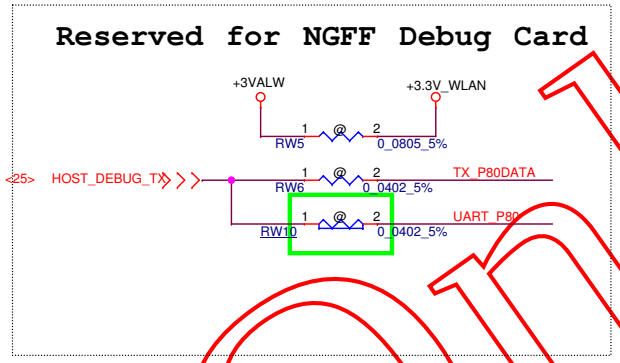
Date: Tuesday, November 13, 2018 | Sheet 31 of 65

Main Func = WLAN

A Key CONN



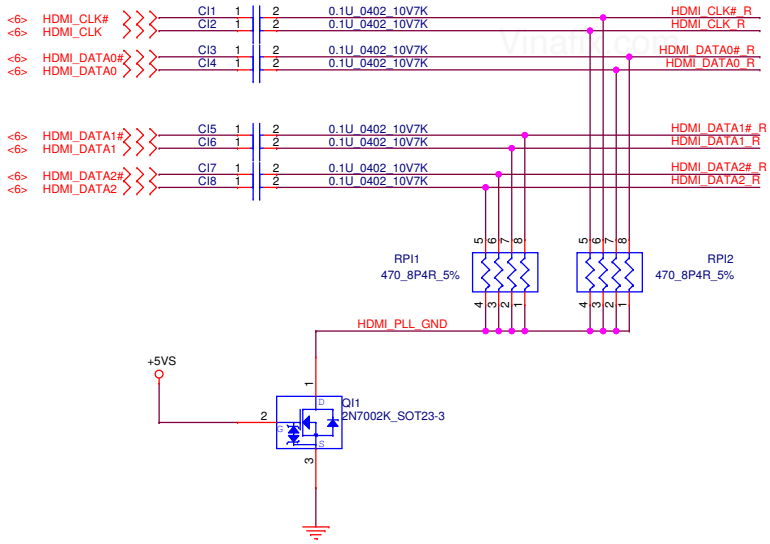


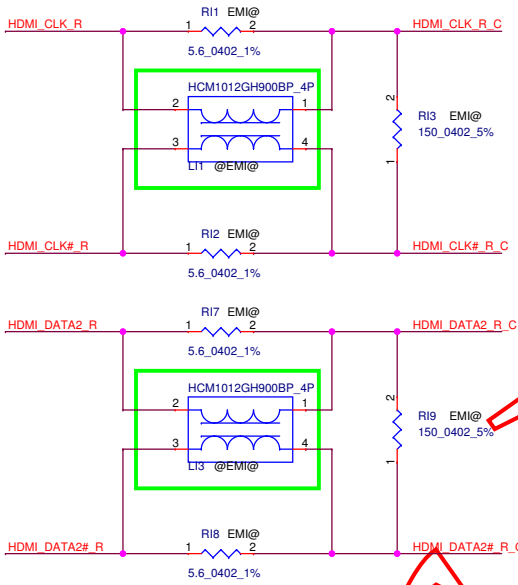


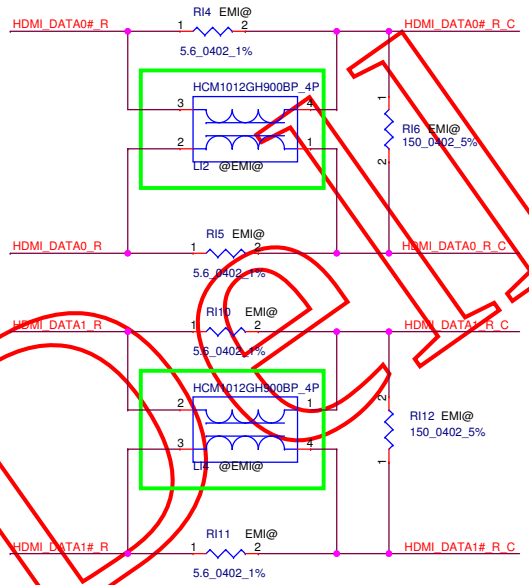
Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

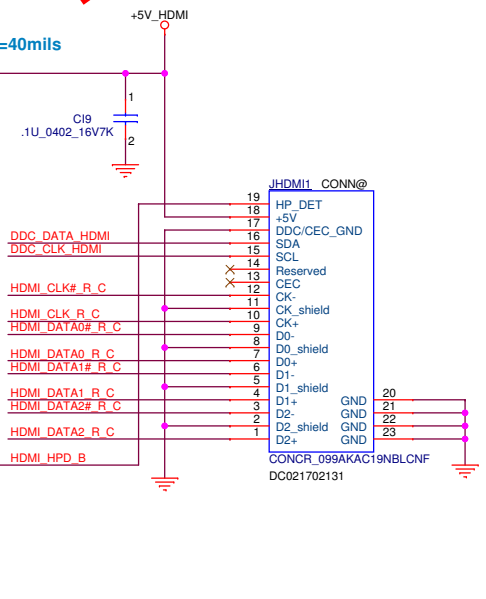
Compal Electronics, Inc.			
Title	NGFF_WLAN CONN		
Size	Document Number LA-G714P		Rev 1.0
Date: Tuesday, November 13, 2018	Sheet 32 of 65		

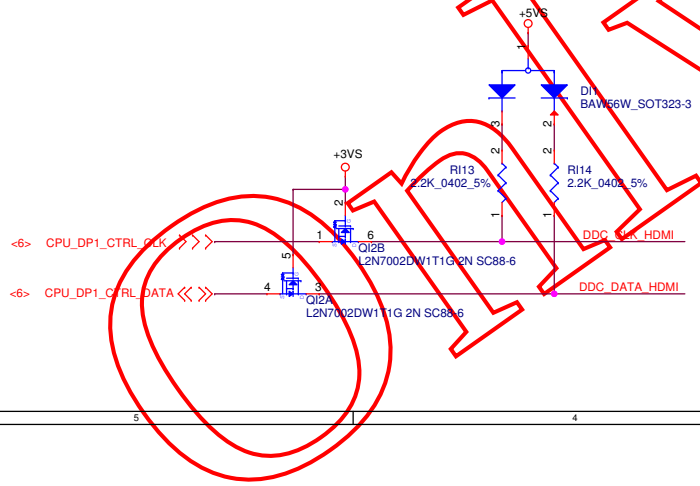
Main Func = HDMI

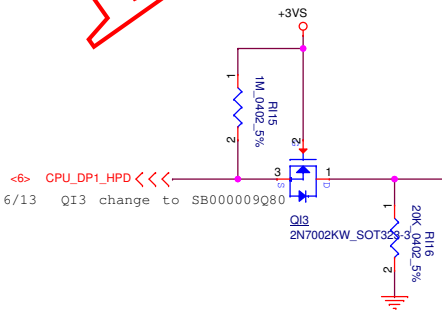












Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

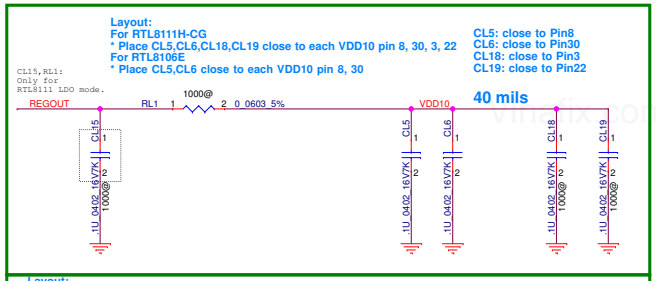
Compal Electronics, Inc.

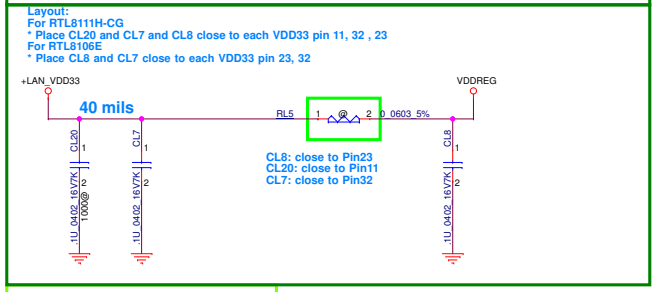
Title: **HDMI L.Shifter/Conn**

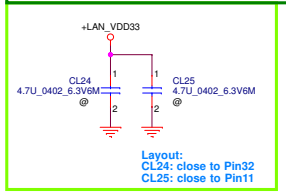
Size	Document Number	Rev
	LA-G714P	1.0

Date: Tuesday, November 13, 2018 Sheet 33 of 65

Main Func = LAN





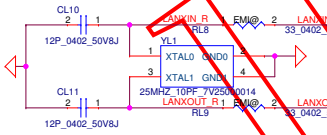


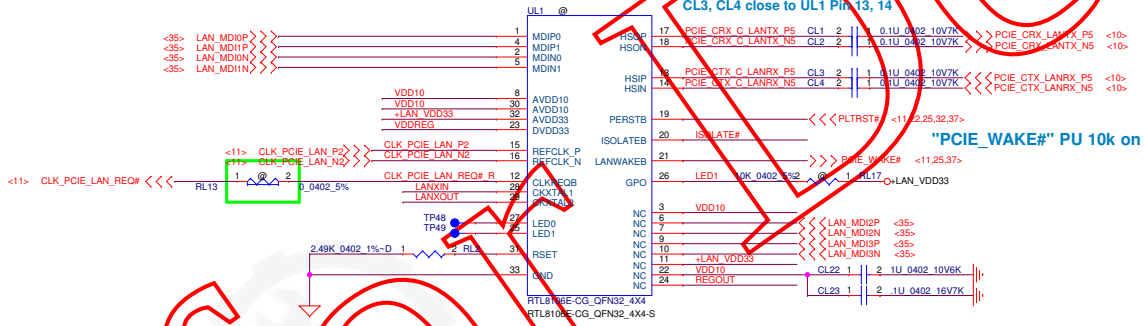
LAN CHIP 10/100/1000

RTL8111H-CG	RTL8106E-CG
SA000080P00	SA000065Y00
LDO mode	LDO mode
10/100/1000M	10/100M

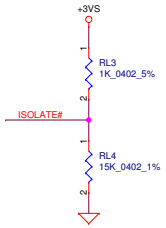
UL1 1000@
RTL8111H-CG QFN 32P E-LAN CTRL
SA000080P00

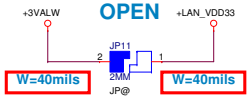
UL1 100@
RTL8106E-CG_QFN32_4X4
SA000065Y00



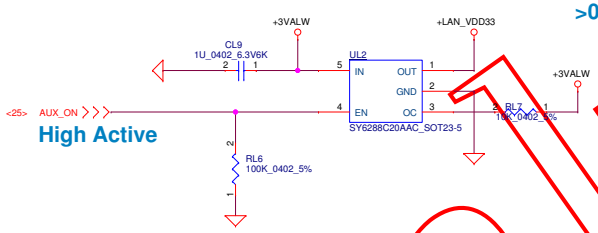


"PCIE_WAKE#" PU 10k on EC side





+LAN_VDD33 Rising time (10%~90%) need >0.5mS and <100mS.



	1.0V Source	RL1	CL15	CL18	CL19	CL20	CL8
RTL8111H-CG RTL8111G-CGT (71.08111.U03)	LDO	O	O	O	O	O	X
RTL8106E-CG (071.08106.0003)	LDO	X	X	X	X	X	O

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: LAN RTL8111/RTL8106

Size	Document Number	Rev
	LA-G714P	1.0

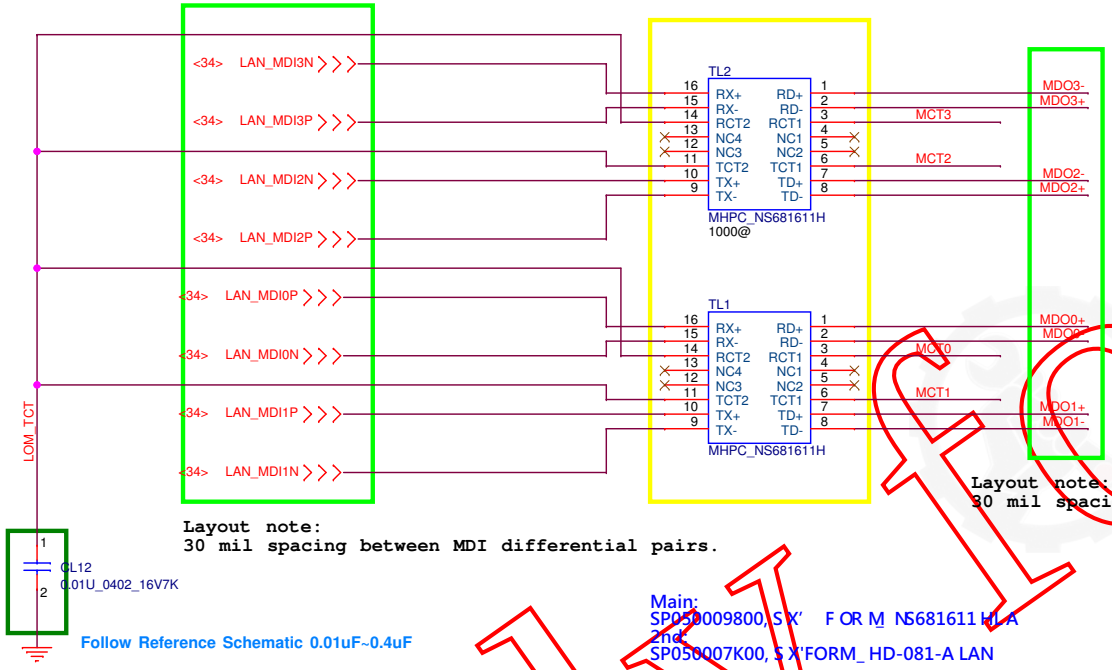
Date: Tuesday, November 13, 2018 Sheet 34 of 65

Main Func = LAN

LAN TransFormer 10/100M x2

LAN TransFormer (Giga & 10/100 co-layout)

Dont use SP050006H00 on Giga LAN SKU due to EMI test failure.



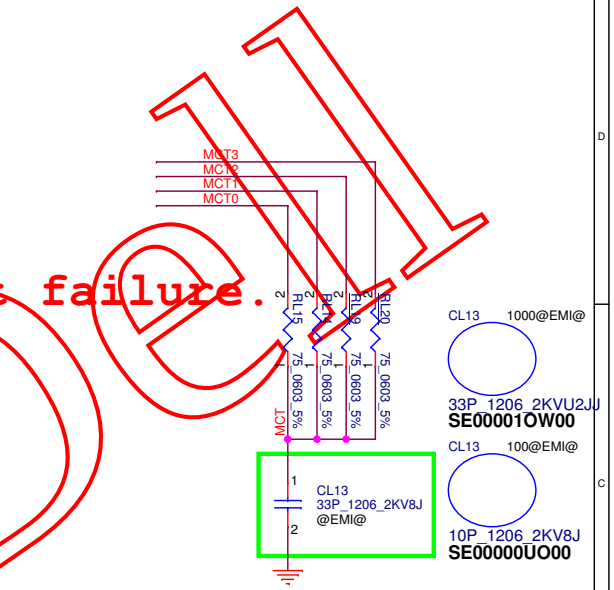
Layout note:
30 mil spacing between MDI differential pairs.

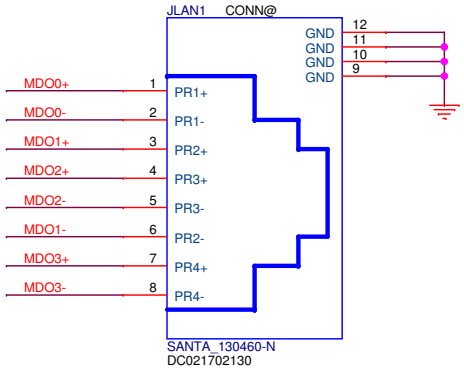
Follow Reference Schematic 0.01uF~0.4uF

TL1 TOP, TL2 BOT
7/13 change footprint

Layout note:
30 mil spacing between MDI differential pairs.

Main:
SP050009800, S X' F OR M NS681611 H L A
2nd:
SP050007K00, S X'FORM_ HD-081-A LAN





Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

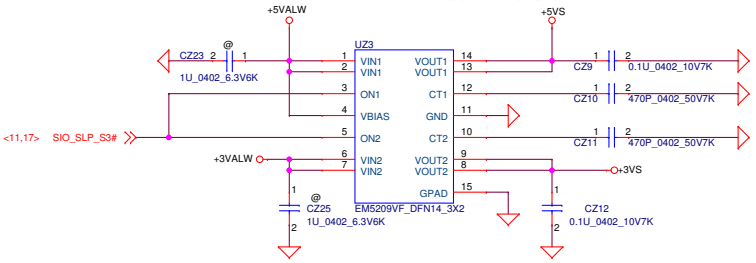
Title: XFOM&RJ45

Size | Document Number: LA-G714P | Rev: 1.0

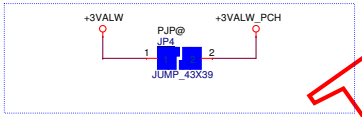
Date: Tuesday, November 13, 2018 | Sheet 35 of 65

Main Func = DC/DC

+5VS/+3VS for System



+3VALW_PCH for System



JP4 Short for NON-DS3

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: DC/DC

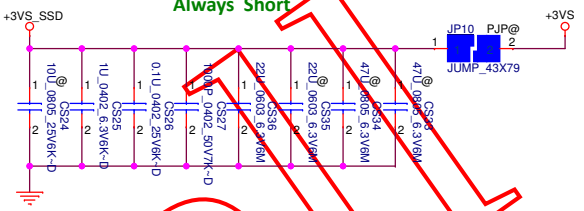
Size | Document Number: LA-G714P | Rev: 1.0

Date: Tuesday, November 13, 2018 | Sheet 36 of 65

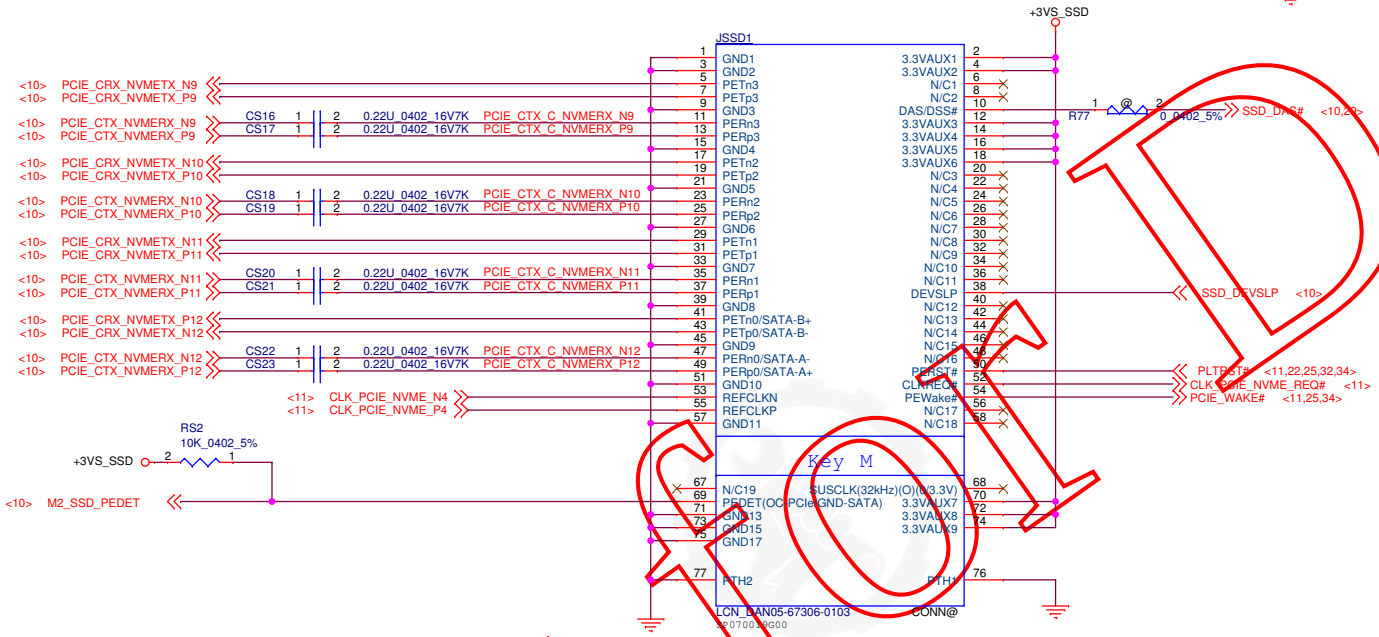
Main Func = SSD

M Key CONN

JP10
Always Short



NGFF Key M



PEDET	Module Type
0	SATA
1	PCIE

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

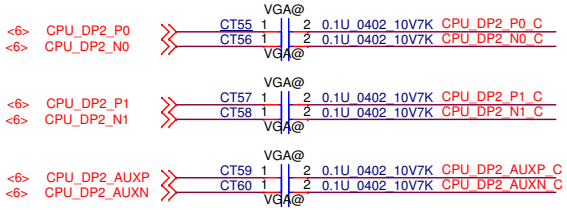
Compal Electronics, Inc.

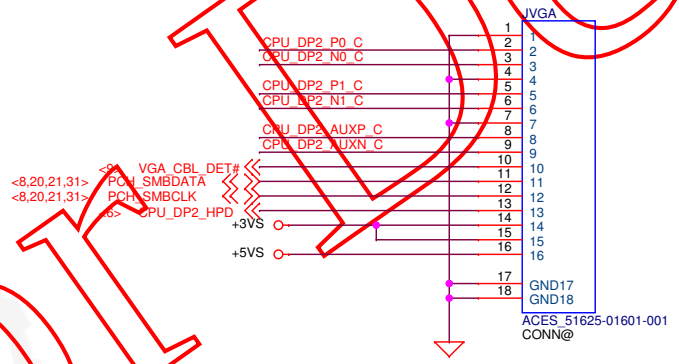
Title: NVME SSD

Size | Document Number: LA-G714P | Rev: 1.0

Date: Tuesday, November 13, 2018 | Sheet 37 of 65

Main Func = VGA/B





Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: **VGA CONN**

Size	Document Number	Rev
	LA-G714P	1.0

Date: Tuesday, November 13, 2018 Sheet 38 of 65

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: **RSV**

Size	Document Number	Rev
	LA-G714P	1.0

Date: Tuesday, November 13, 2018 | Sheet 39 of 65

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

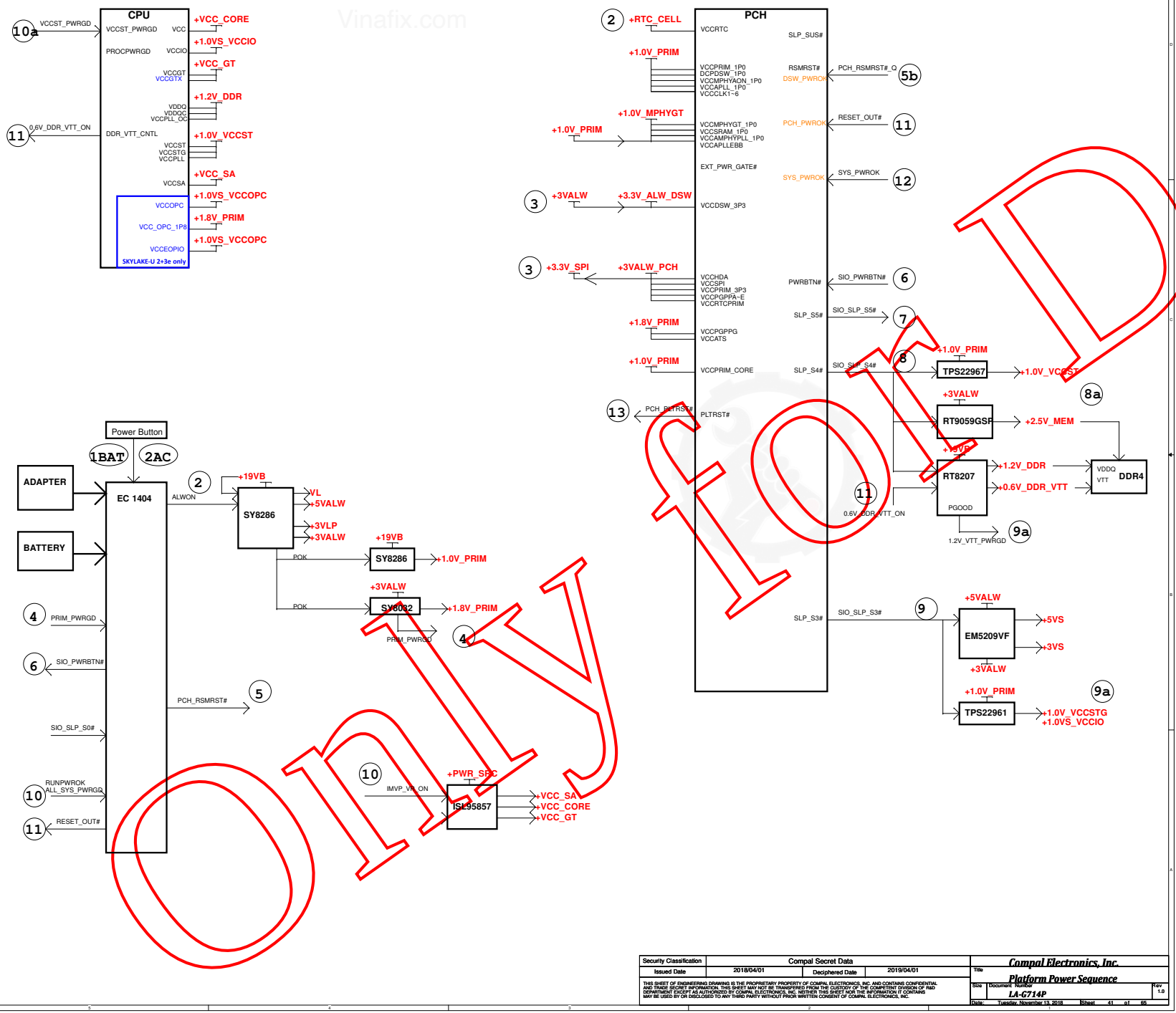
Compal Electronics, Inc.

Title: **RSV**

Size	Document Number	Rev
	LA-G714P	1.0

Date: Tuesday, November 13, 2018 | Sheet 40 of 65

Timing Diagram for S5 to S0 mode



Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

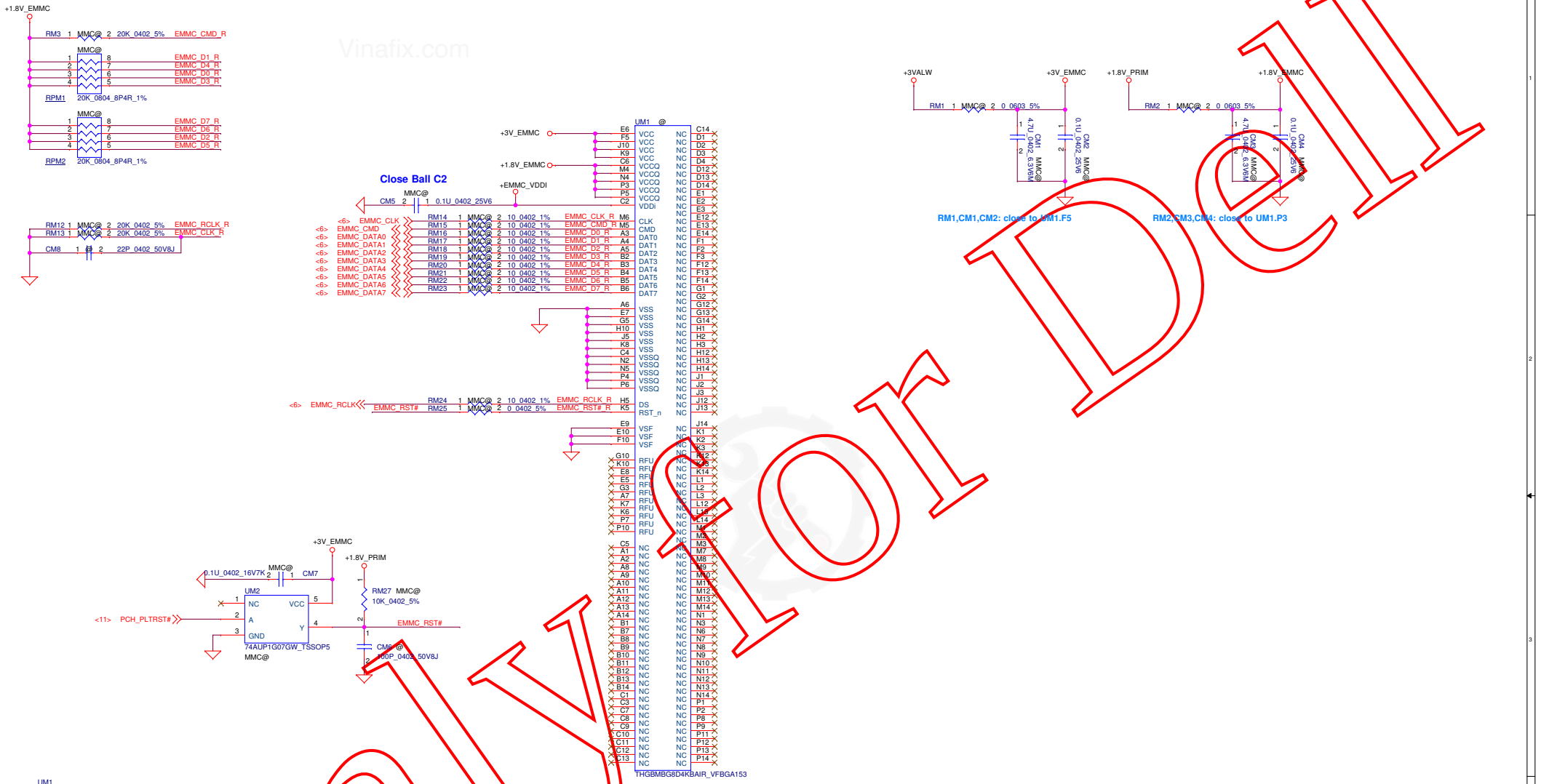
Compal Electronics, Inc.

Title: Platform Power Sequence

Size: | Document Number: LA-G714P | Rev: 1.0

Date: Tuesday, November 13, 2018 | Sheet 41 of 65

Main Func = eMMC



UM1

HYNIX

SA00009N50L

HYNIX_128G@

S IC FL 128G H26M88002AMR FBGA 153P

UM1

SANDISK

SA00009ML0L

SANDISK_128G@

S IC FL 128G SDINADF4-128G-859 TFBGA

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: eMMC

Size: | Document Number: LA-G714P | Rev: 1.0

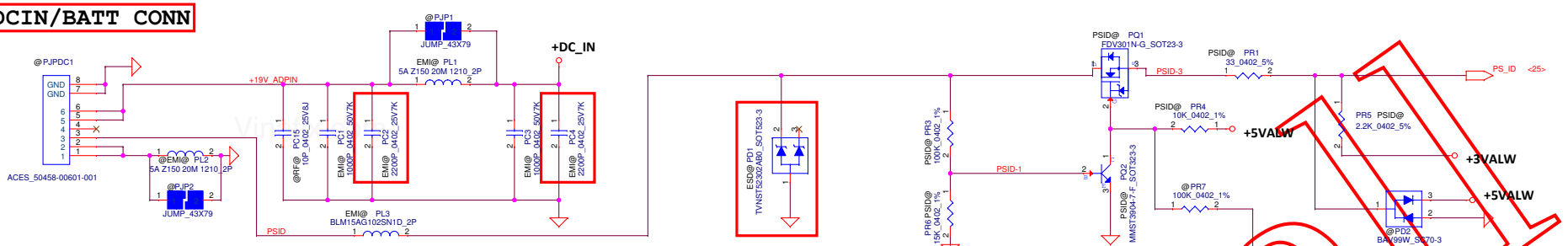
Date: Tuesday, November 13, 2018 | Sheet 42 of 65

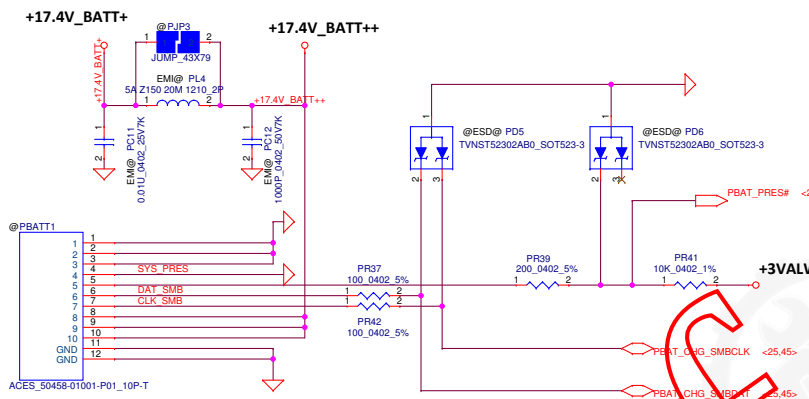
Version Change List (P. I. R. List)

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.		
Title: EE Change list		
Size	Document Number: LA-G714P	Rev: 1.0
Date: Tuesday, November 13, 2018	Sheet 43 of 65	

Main Func = DCIN/BATT CONN





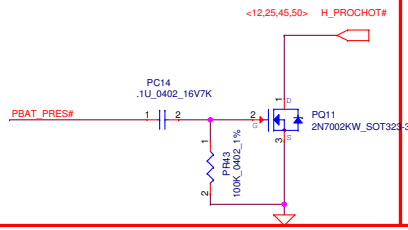
Battery Bat Side

PIN1 GND
PIN2 GND
PIN3 GND
PIN4 SYS_PRES
PIN5 BATT_PRS
PIN6 DAT_SMB
PIN7 CLK_SMB
PIN8 Bat t+
PIN9 Bat t+
PIN10 Bat t+
SP021412220

ACES_50458-01001-P01_10P-T

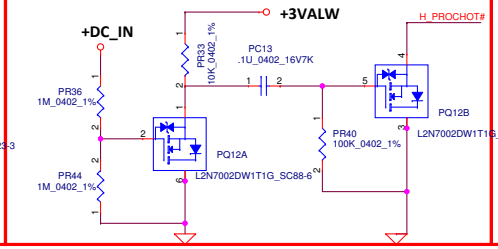
Adapter protection

if battery removed, adaptor only,
then trigger the H_PROCHOT#,
keep @ in BOM since battery can not
be removed by end user

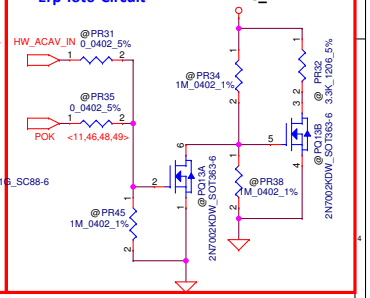


Battery protection

asserts H_PROCHOT# when adaptor is
unplugged, keep low for 10ms
till SW PROCHOT# is issued by EC



Erp lot6 Circuit

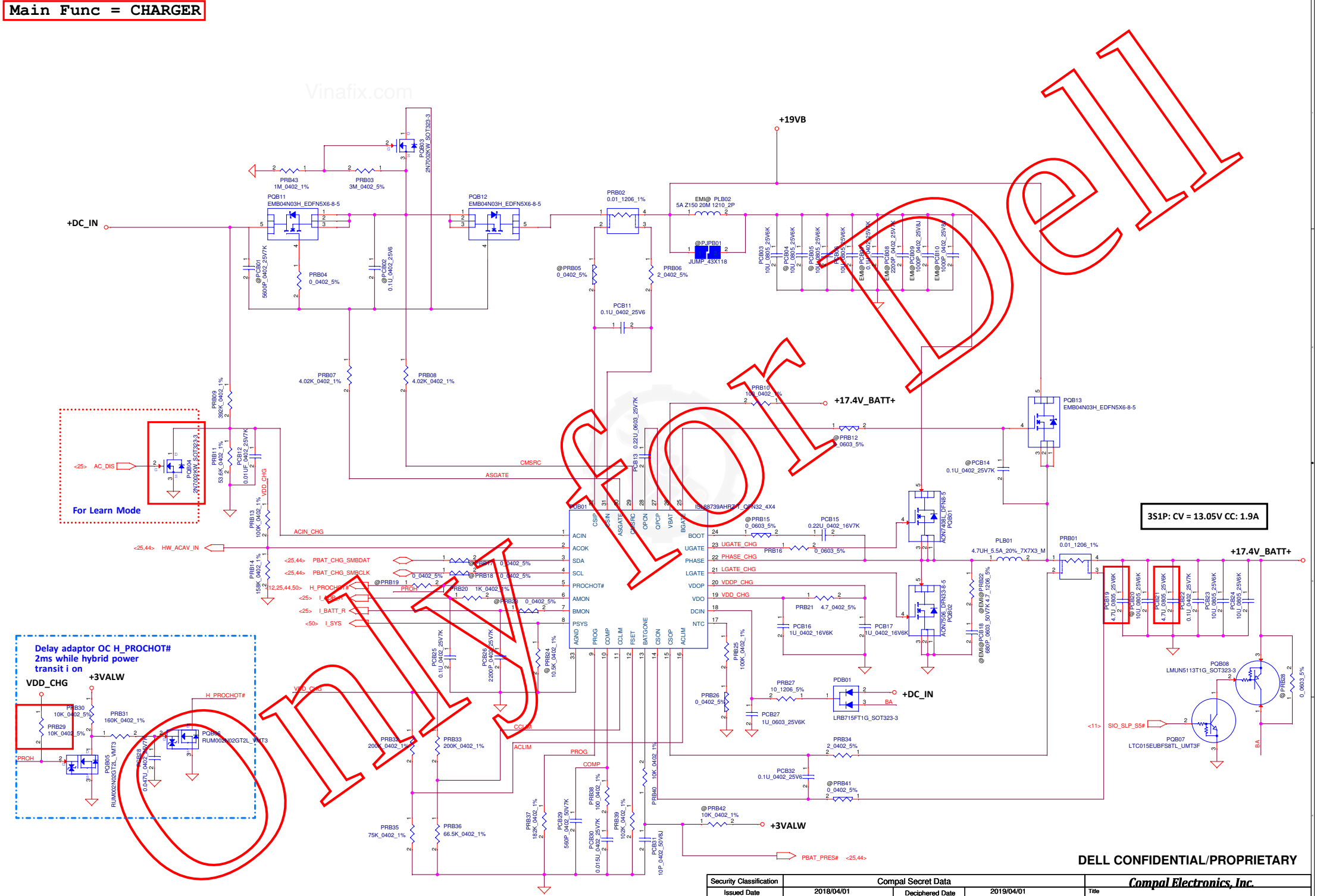


DELL CONFIDENTIAL/PROPRIETARY

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.			
Title	PWR DCIN/BATT CONN		
Size	Document Number		Rev
	LA-G714P		0.1
Date:	Tuesday, November 13, 2018	Sheet	44 of 65

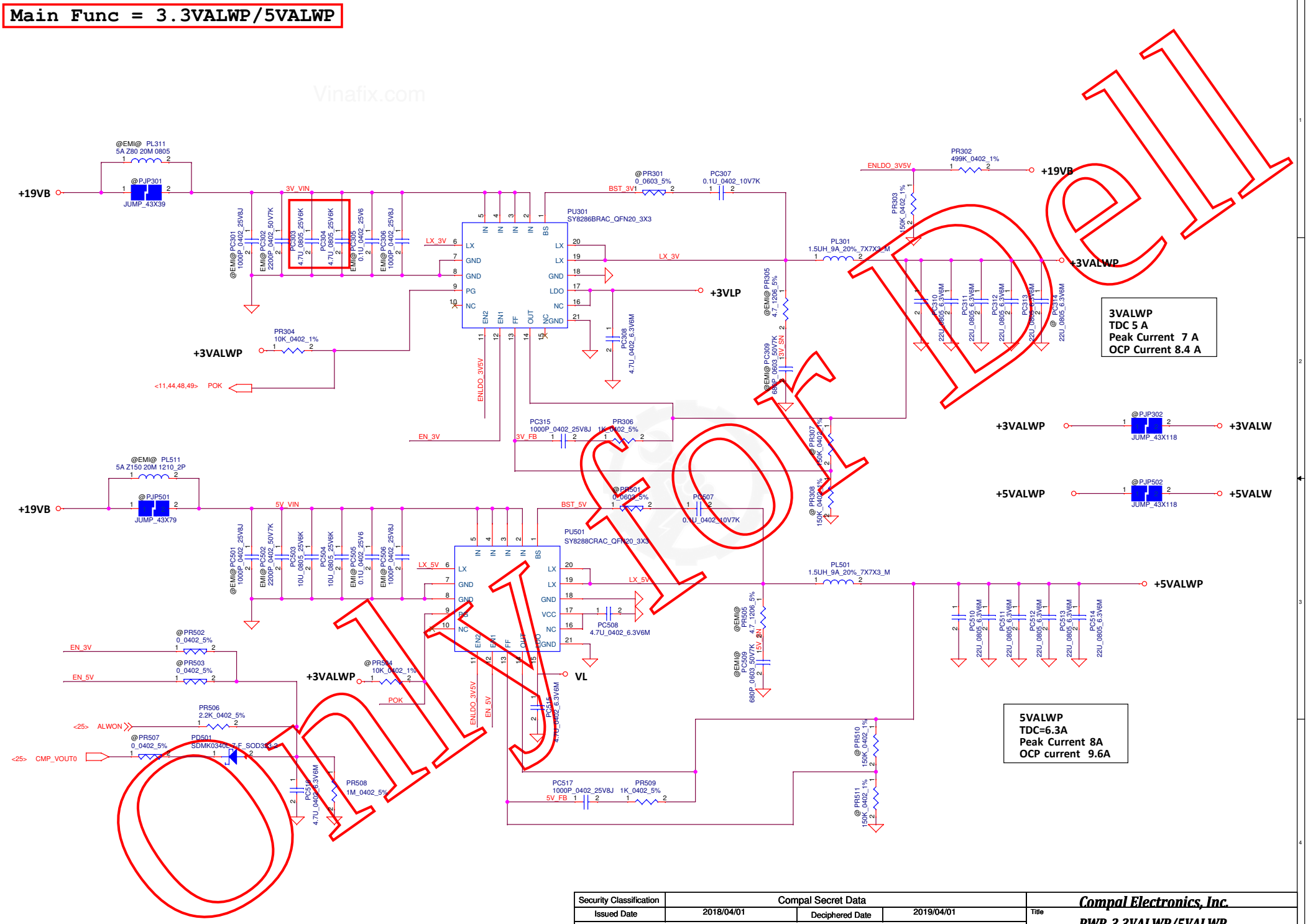
Main Func = CHARGER



Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.			
Title	PWR CHARGER		
Size	Document Number		Rev
	LA-G714P		0.1
Date:	Tuesday, November 13, 2018	Sheet	45 of 65

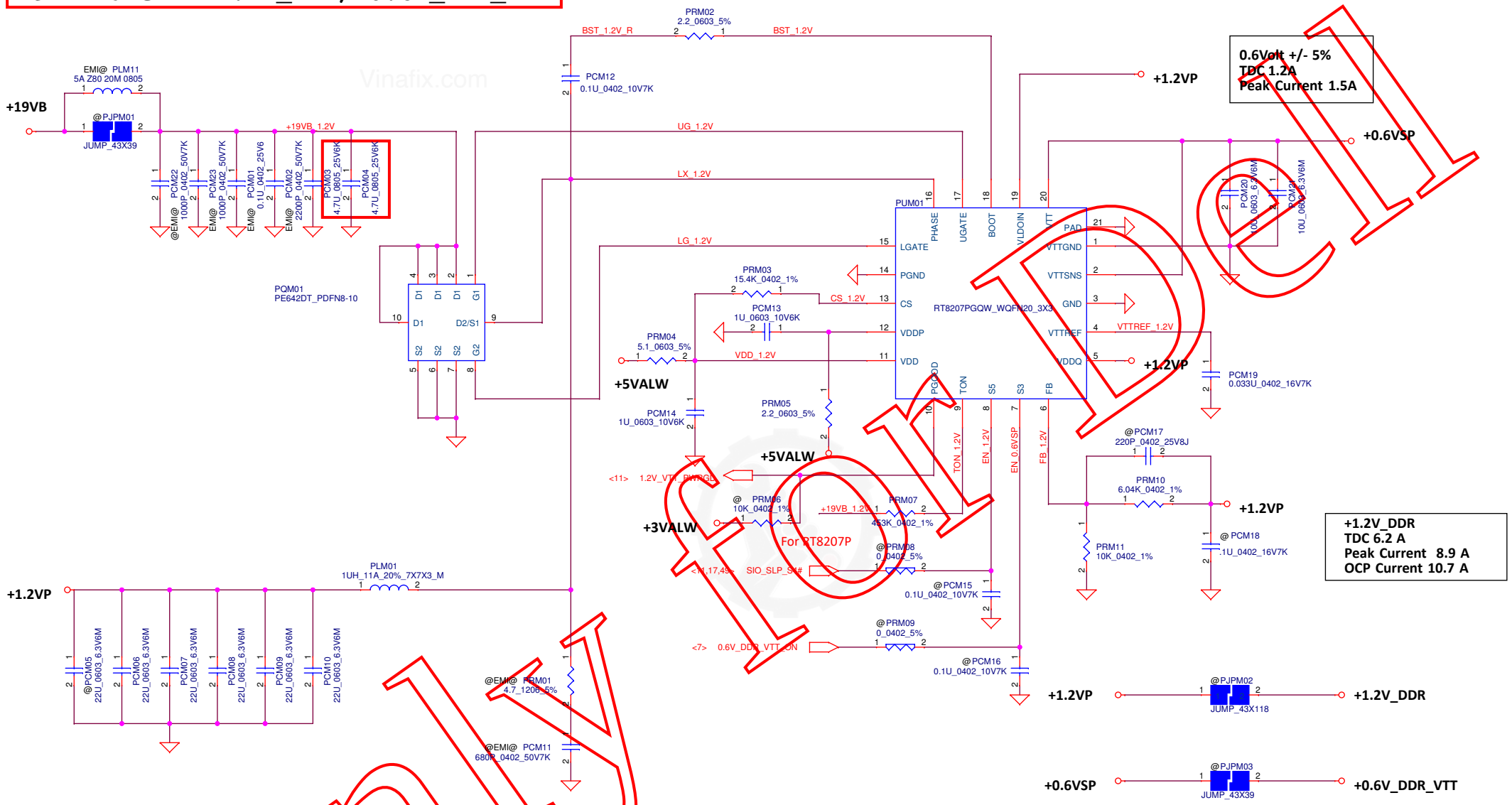
Main Func = 3.3VALWP/5VALWP



Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.			
Title: PWR 3.3VALWP/5VALWP			
Size	Document Number: LA-G714P		Rev: 0.1
Date: Tuesday, November 13, 2018	Sheet 46 of 65		

Main Func = +1.2V_DDR/+0.6V_DDR_VTT



Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

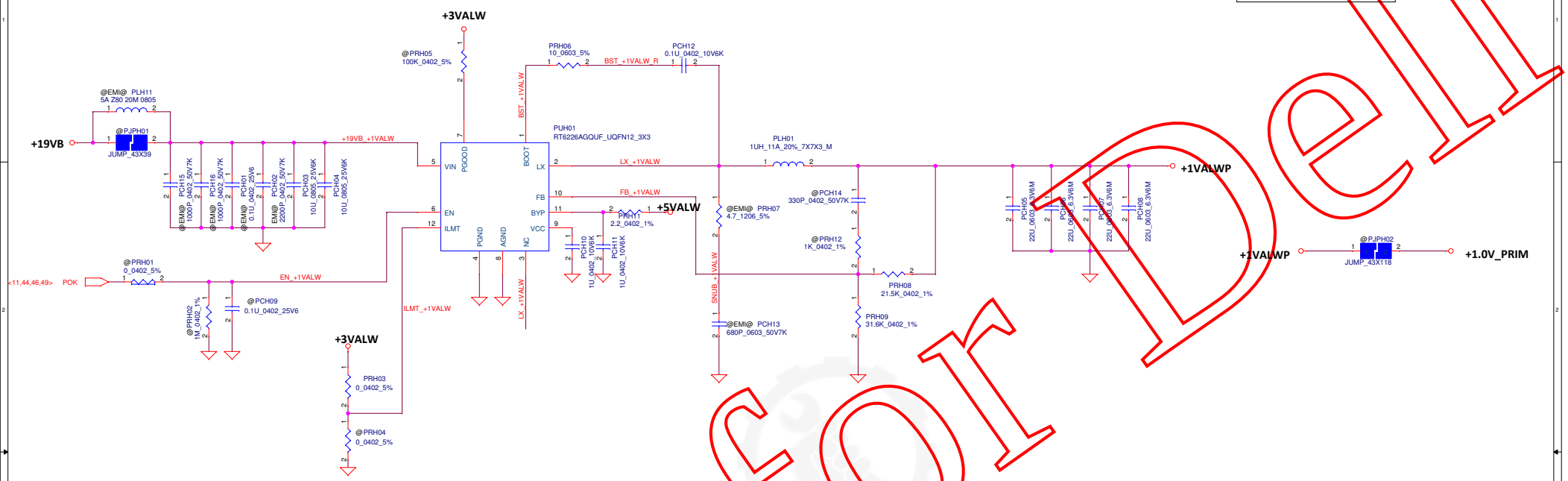
Title: PWR +1.2V DDR/+0.6V DDR VTT

Size	Document Number	Rev
	LA-G714P	0.1

Date: Tuesday, November 13, 2018 | Sheet 47 of 65

Main Func = +1VALWP

+1.0V_PRIM
TDC 5.2 A
Peak Current 6.5 A
OCP Current 9 A Fix by IC



Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

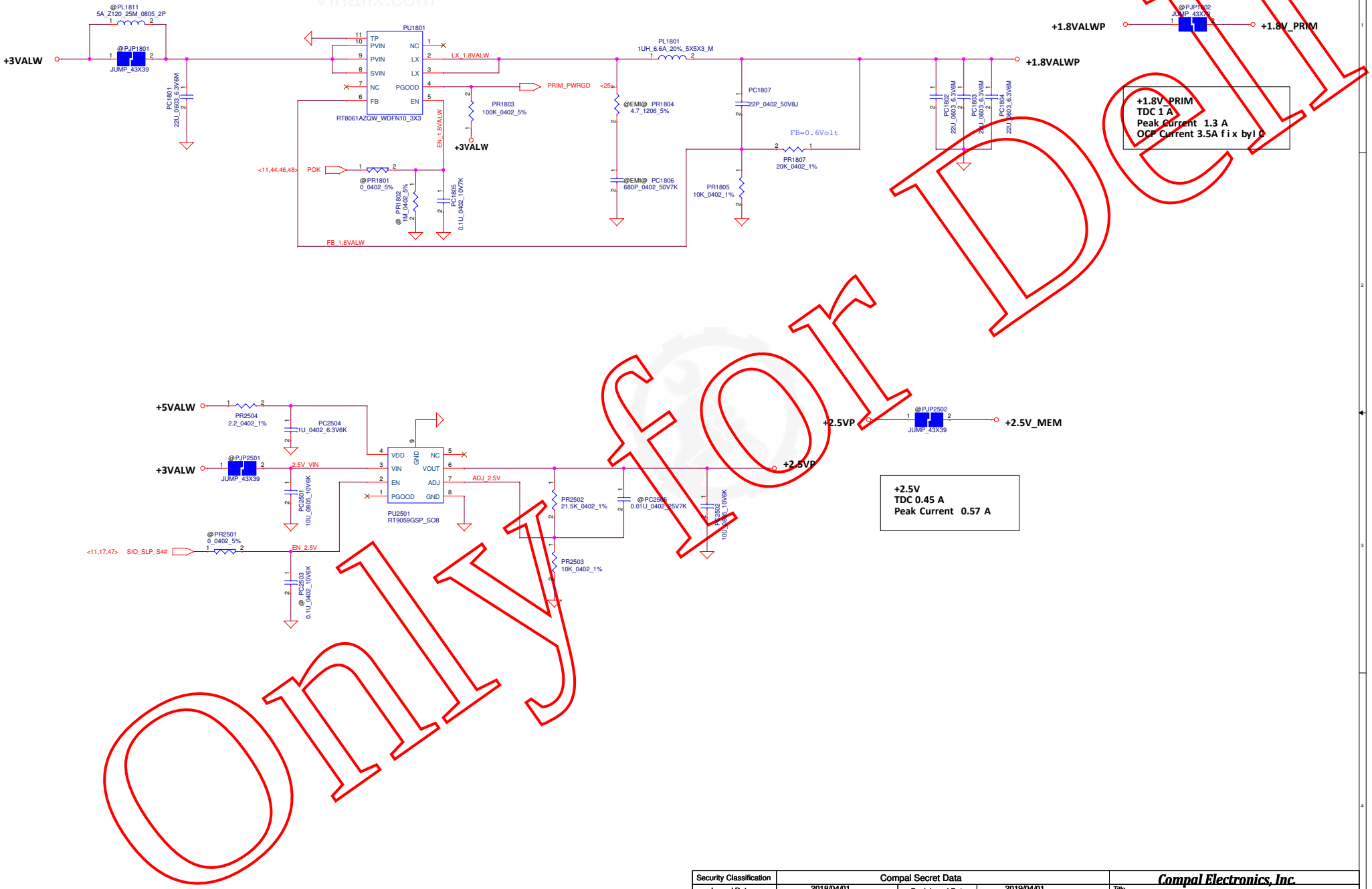
Compal Electronics, Inc.

Title: PWR +1VALWP

Size	Document Number	Rev
	LA-G714P	0.1

Date: Tuesday, November 13, 2018 Sheet 48 of 65

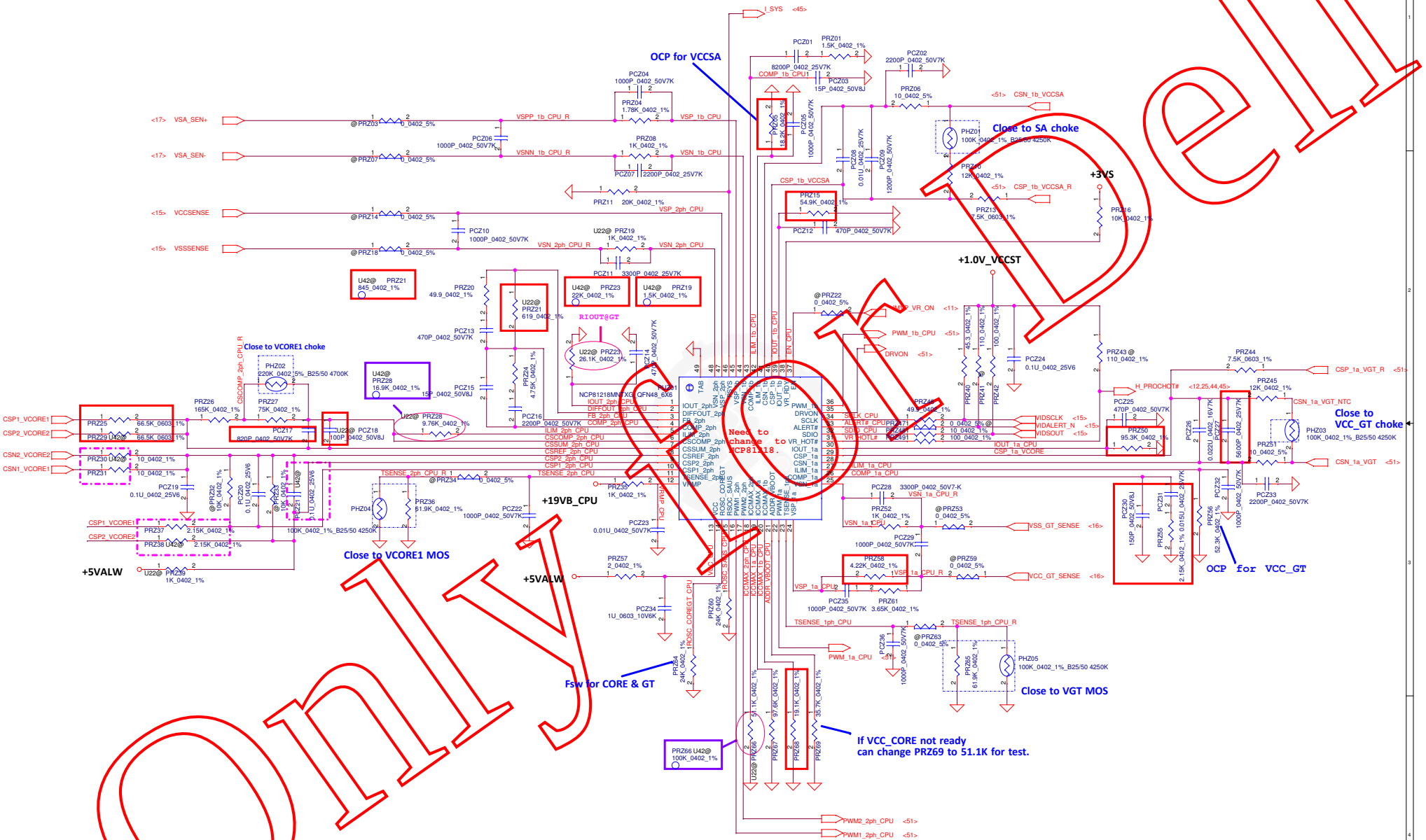
Main Func = +1.8VALWP / +2.5VP



Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.			
Title	PWR +1.8VALWP / +2.5VP		
Size	Document Number LA-G714P		Rev 0.1
Date: Tuesday, November 13, 2018	Sheet 49 of 65		

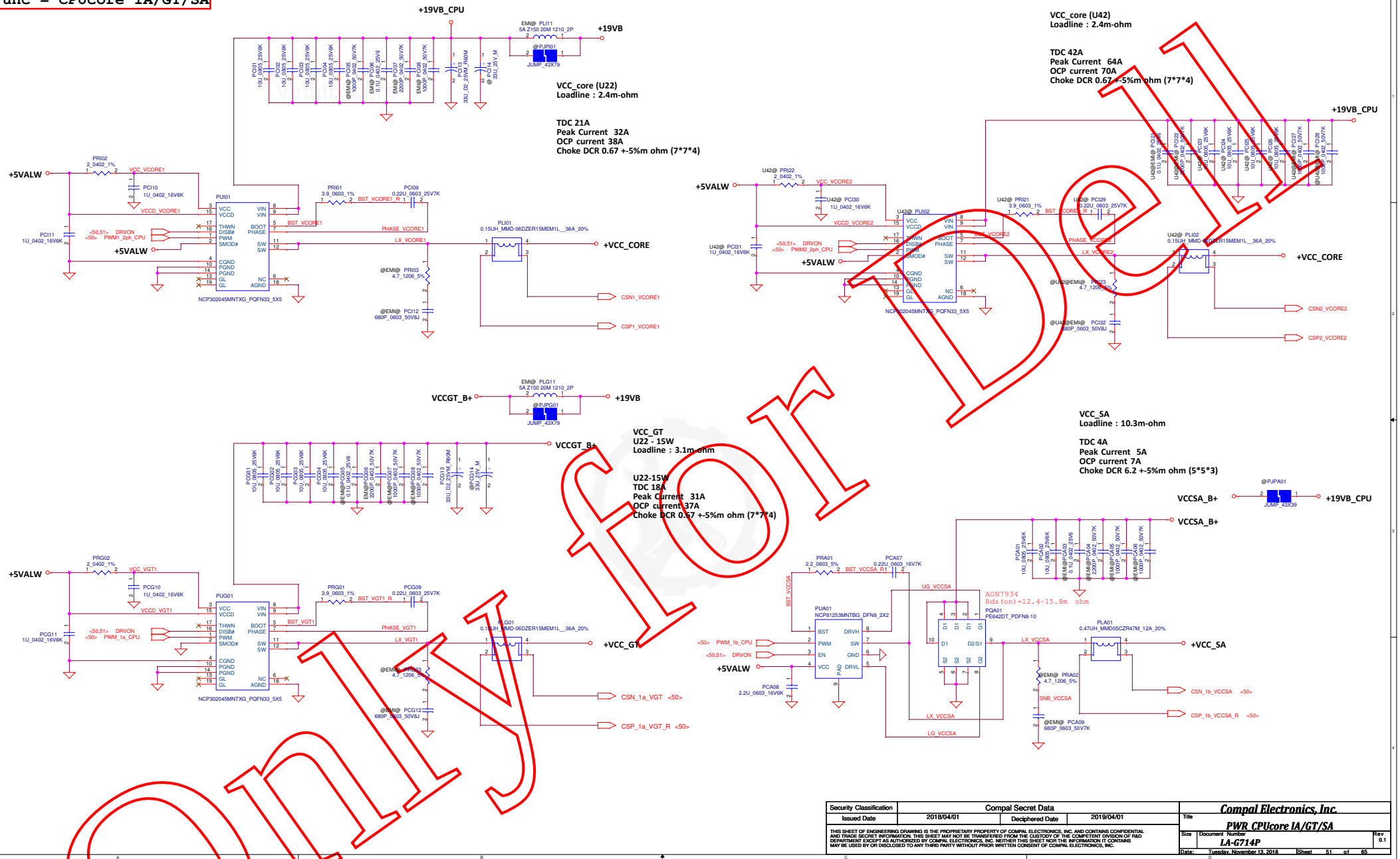
Main Func = CPU



Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.			
Title: PWR CPU			
Size	Document Number: LA-G714P		Rev: 0.1
Date: Tuesday, November 13, 2018	Sheet 50 of 65		

Main Func = CPUcore IA/GT/SA



Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.			
Title: PWR_CPUcore IA/GT/SA			
Size:	Document Number: LA-G714P		Rev: 0.1
Date: Tuesday, November 13, 2018	Sheet 51 of 65		

Main Func = CPU/ VGA / SA MLCC

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: PWR_CPU/ VGA / SA MLCC

Size	Document Number	Rev
	LA-G714P	0.1

Date: Tuesday, November 13, 2018 | Sheet 52 of 65

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P51	PWR	20160321	COMPAL			0.1(X00)
2							
3							
4							
5							
6							
7							
8							

Security Classification	Compal Secret Data		
Issued Date	2018/04/01	Deciphered Date	2019/04/01

Compal Electronics, Inc.

Title: Changed-List PWR History

Size | Document Number: LA-G714P | Rev: 0.1

Date: Tuesday, November 13, 2018 | Sheet 53 of 65