COMPAL CONFIDENTIAL

MODEL NAME : ADP80/81

PCB NO : LA-C841P

BOM P/N : 4319YK31LXX

GPIO MAP: Gen7 GPIO Master_0115

Park City 15" H DSC

Skylake H

2015-09-08

REV : 1.0 (A00)

@ : Nopop Component

EMC@ : EMI, ESD and RF Component

@EMC@ : EMI, ESD and RF Nopop Component

XDP@ : XDP Component

CONN@ : Connector Component

TB@ : AR TBT Component

DIS@ : GPU Component

UMA@ : UMA Component

Litho@ : GPU Litho Component

Tropo@ : GPU Tropo Component

H/P Check RE300

MB PCB

Part Number	Description
DA21E000101	PCB ADP80 LA-C841P LS-C641P

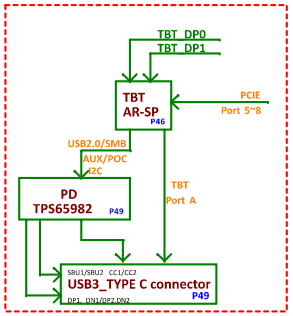
Layout Dell logo

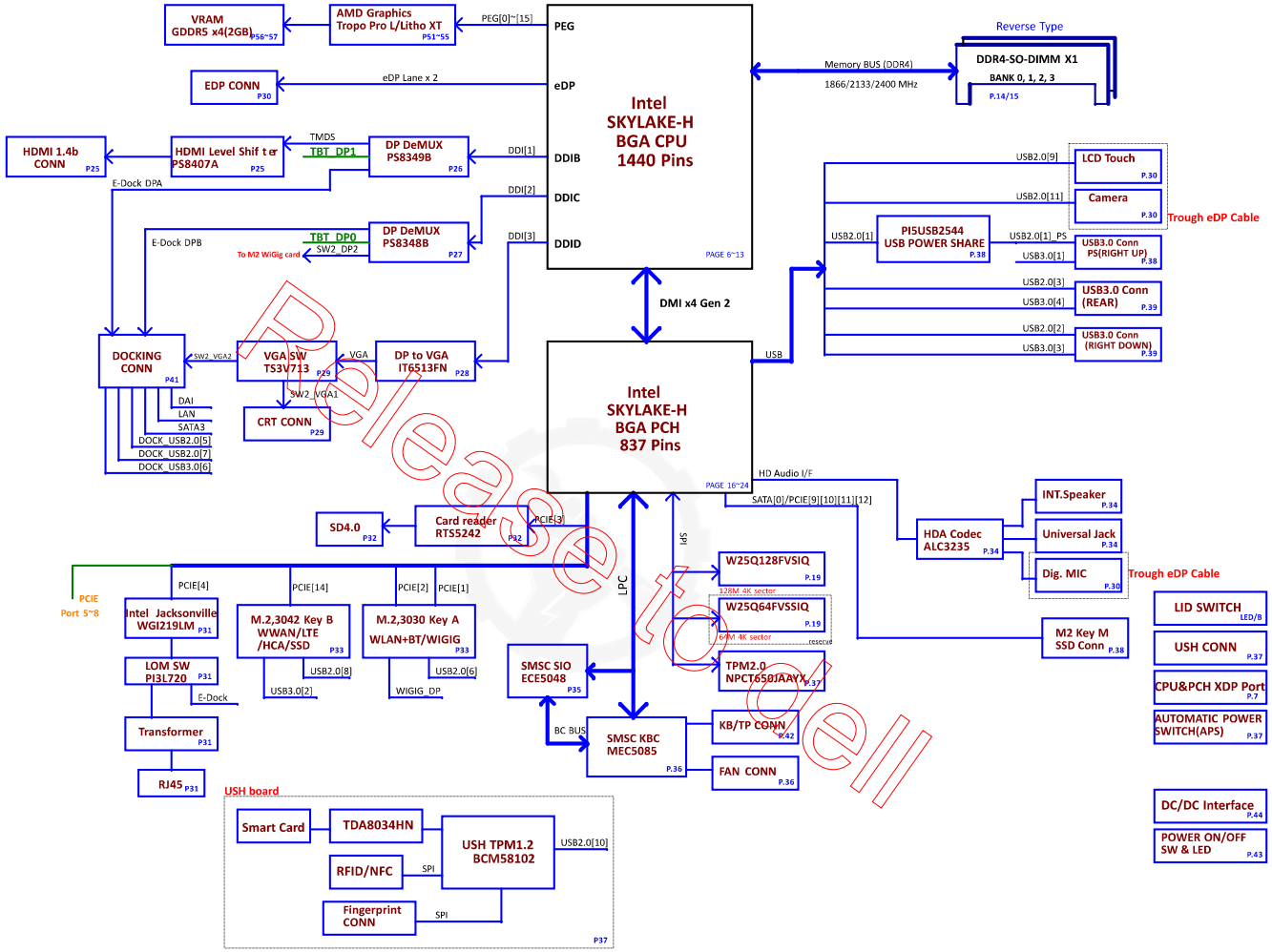
Compal Electronics, Inc.

Title: Cover Sheet

Size | Document Number: LA-C841P | Rev: 0.1

Date: Tuesday, September 08, 2015 | Sheet 1 of 74





Compal Electronics, Inc.

Title: Block diagram

Size: Document Number: LA-C841P Rev: 0.1

Date: Tuesday, September 08, 2015 Sheet 2 of 74

POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ power plane	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT	+3.3V_SUS +1.2V_MEM +1.0V_VCCST +2.5V_MEM	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.5V_RUN	+3.3V_M	(M-OFF) +3.3V_M +VCC_CORE +VCC_GT +1.0VS_VCCIO +VCC_SA
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF	OFF	OFF

USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				JUSB3-->Right up
USB3.0-2	SSIC-1			JNGFF2-->M2 3042(LTE)
USB3.0-3	SSIC-2			JUSB1-->Right down
USB3.0-4				JUSB2-->Rear
USB3.0-5				NA
USB3.0-6				EDOCK
USB3.0-7		PCIE-1		JNGFF1-->M.2 3030(WIGIG)
USB3.0-8		PCIE-2		JNGFF1-->M.2 3030(WLAN)
USB3.0-9		PCIE-3		Card Reader
USB3.0-10		PCIE-4		LOM
		PCIE-5		
		PCIE-6		Alpine Ridge - SP (pop only on Precision SKU)
		PCIE-7		
		PCIE-8		
		PCIE-9	SATA-0A	
		PCIE-10	SATA-1A	M.2 Socket 3 (Key M) M.2 2280 SSD (PCIex4 or SATA)
		PCIE-11		
		PCIE-12		
		PCIE-13	SATA-0B	NA
		PCIE-14	SATA-1B	M.2 3042 (HCA or QCA LTE) SSD Cache
		PCIE-15	SATA-2	JSATA1-->HDD SATA
		PCIE-16	SATA-3	EDOCK E-SATA
		PCIE-17	SATA-4	NA
		PCIE-18	SATA-5	NA
		PCIE-19		NA
		PCIE-20		NA

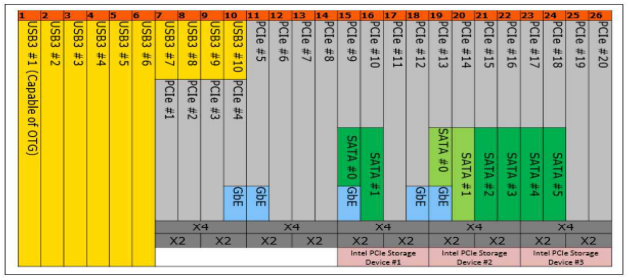
USB PORT#	DESTINATION
1	JUSB3-->Right up
2	JUSB1-->Right down
3	JUSB2 ->Rear
4	NA
5	EDOCK Port B
6	JNGFF1--> M.2 3030(BT)
7	EDOCK Port A
8	JNGFF2-->M2 3042(WWAN)
9	JEDP1-->Touch Screen
10	JUSH1-->USH
11	JEDP1-->Camera

USH		
	0	BIO
	1	NA

Check

VIDEO		DESTINATION
eDP		LCD
DDI-C	DeMux 1	M.2 3030 (WiGig)
		EDOCK Port B
DDI-B	DeMux 2	Alpine Ridge - SP (pop only on Precision SKU
		EDOCK Port A
		JHDMI1
DDI-D	CONV	MB VGA
	VGA SW	DOCK VGA

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	TU662	0.5
			Add Plating		
1	Top		Copper foil	0.5oz+plating	1.8
		3.7	Prepreg	1080	2.6
2	GND		Copper foil	1oz	1.25
		3.7	Core	4mil	3.87
3	IN 1		Copper foil	1oz	1.25
		3.8	Prepreg	2116H	4.3
4	GND/PWR		Copper foil	1oz	1.25
		3.7	Core	4mil	3.87
5	IN 2		Copper foil	1oz	1.25
		3.8	Prepreg	1080H x2	4.4
6	IN 3		Copper foil	1oz	1.25
		3.7	Core	4mil	3.87
7	GND/PWR		Copper foil	1oz	1.25
		3.8	Prepreg	2116H	4.3
8	IN 4		Copper foil	1oz	1.25
		3.7	Core	4mil	3.87
9	GND		Copper foil	1oz	1.25
		3.7	Prepreg	1080	2.6
10	Bottom		Copper foil	0.5oz+plating	1.8
			Add Plating		
			SolderMask	TU662	0.5
Overall Thickness (1.2mm ± 10%)					48.28000 1.226312



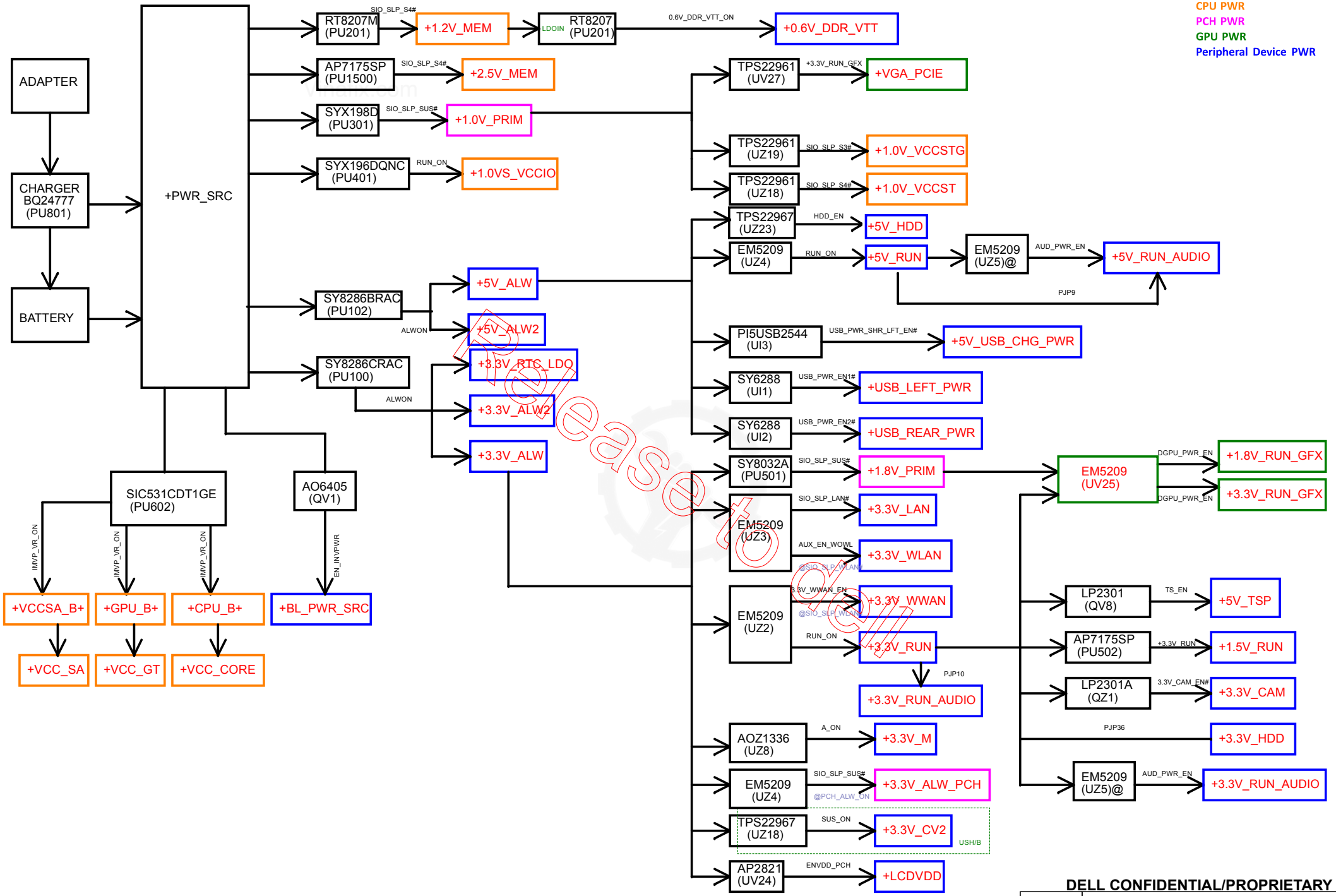
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: Port assignment

Size: | Document Number: LA-C841P | Rev: 0.1

Date: Tuesday, September 08, 2015 | Sheet 3 of 74



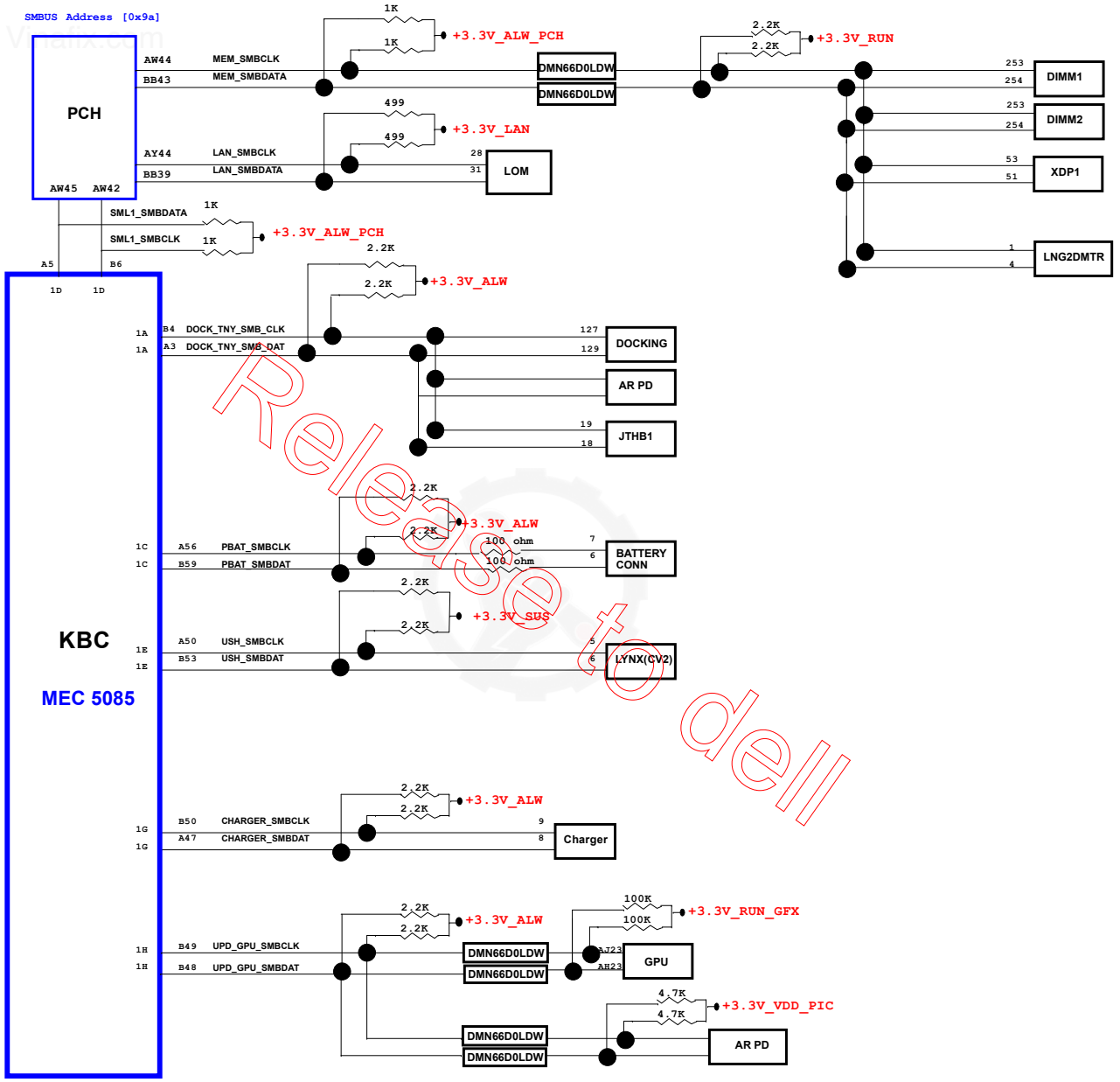
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: Power rails

Size | Document Number: LA-C841P | Rev: 0.1

Date: Tuesday, September 08, 2015 | Sheet 4 of 74



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: SMbus Block diagram

Size | Document Number: LA-C841P | Rev: 0.1

Date: Tuesday, September 08, 2015 | Sheet 5 of 74

PEG_CRX_GTX_P[0..15] PEG_CRX_GTX_P[0..15] <50>
PEG_CRX_GTX_N[0..15] PEG_CRX_GTX_N[0..15] <50>
PEG_CTX_C_GRX_P[0..15] PEG_CTX_C_GRX_P[0..15] <50>
PEG_CTX_C_GRX_N[0..15] PEG_CTX_C_GRX_N[0..15] <50>

CPU1C SKYLAKE_HALO
BGA1440

PEG_CRX_GTX_P15	E25	PEG_RXP[0]	PEG_TXP[0]	B25	PEG_CTX_GRX_P15	Tropo@	CC67	2	1	0.22U 0402 10V6K	PEG_CTX_C_GRX_P15
PEG_CRX_GTX_N15	D25	PEG_RXN[0]	PEG_TXN[0]	A25	PEG_CTX_GRX_N15	Tropo@	CC44	2	1	0.22U 0402 10V6K	PEG_CTX_C_GRX_N15
PEG_CRX_GTX_P14	E24	PEG_RXP[1]	PEG_TXP[1]	B24	PEG_CTX_GRX_P14	Tropo@	CC68	2	1	0.22U 0402 10V6K	PEG_CTX_C_GRX_P14
PEG_CRX_GTX_N14	F24	PEG_RXN[1]	PEG_TXN[1]	C24	PEG_CTX_GRX_N14	Tropo@	CC45	2	1	0.22U 0402 10V6K	PEG_CTX_C_GRX_N14
PEG_CRX_GTX_P13	E23	PEG_RXP[2]	PEG_TXP[2]	B23	PEG_CTX_GRX_P13	Tropo@	CC51	2	1	0.22U 0402 10V6K	PEG_CTX_C_GRX_P13
PEG_CRX_GTX_N13	D23	PEG_RXN[2]	PEG_TXN[2]	A23	PEG_CTX_GRX_N13	Tropo@	CC53	2	1	0.22U 0402 10V6K	PEG_CTX_C_GRX_N13
PEG_CRX_GTX_P12	E22	PEG_RXP[3]	PEG_TXP[3]	B22	PEG_CTX_GRX_P12	Tropo@	CC52	2	1	0.22U 0402 10V6K	PEG_CTX_C_GRX_P12
PEG_CRX_GTX_N12	F22	PEG_RXN[3]	PEG_TXN[3]	C22	PEG_CTX_GRX_N12	Tropo@	CC73	2	1	0.22U 0402 10V6K	PEG_CTX_C_GRX_N12
PEG_CRX_GTX_P11	E21	PEG_RXP[4]	PEG_TXP[4]	B21	PEG_CTX_GRX_P11	Tropo@	CC69	2	1	0.22U 0402 10V6K	PEG_CTX_C_GRX_P11
PEG_CRX_GTX_N11	D21	PEG_RXN[4]	PEG_TXN[4]	A21	PEG_CTX_GRX_N11	Tropo@	CC46	2	1	0.22U 0402 10V6K	PEG_CTX_C_GRX_N11
PEG_CRX_GTX_P10	E20	PEG_RXP[5]	PEG_TXP[5]	B20	PEG_CTX_GRX_P10	Tropo@	CC54	2	1	0.22U 0402 10V6K	PEG_CTX_C_GRX_P10
PEG_CRX_GTX_N10	F20	PEG_RXN[5]	PEG_TXN[5]	C20	PEG_CTX_GRX_N10	Tropo@	CC74	2	1	0.22U 0402 10V6K	PEG_CTX_C_GRX_N10
PEG_CRX_GTX_P9	E19	PEG_RXP[6]	PEG_TXP[6]	B19	PEG_CTX_GRX_P9	Tropo@	CC55	2	1	0.22U 0402 10V6K	PEG_CTX_C_GRX_P9
PEG_CRX_GTX_N9	D19	PEG_RXN[6]	PEG_TXN[6]	A19	PEG_CTX_GRX_N9	Tropo@	CC47	2	1	0.22U 0402 10V6K	PEG_CTX_C_GRX_N9
PEG_CRX_GTX_P8	E18	PEG_RXP[7]	PEG_TXP[7]	B18	PEG_CTX_GRX_P8	Tropo@	CC70	2	1	0.22U 0402 10V6K	PEG_CTX_C_GRX_P8
PEG_CRX_GTX_N8	F18	PEG_RXN[7]	PEG_TXN[7]	C18	PEG_CTX_GRX_N8	Tropo@	CC56	2	1	0.22U 0402 10V6K	PEG_CTX_C_GRX_N8
PEG_CRX_GTX_P7	D17	PEG_RXP[8]	PEG_TXP[8]	A17	PEG_CTX_GRX_P7	DIS@	CC57	2	1	0.22U 0402 10V6K	PEG_CTX_C_GRX_P7
PEG_CRX_GTX_N7	E17	PEG_RXN[8]	PEG_TXN[8]	B17	PEG_CTX_GRX_N7	DIS@	CC75	2	1	0.22U 0402 10V6K	PEG_CTX_C_GRX_N7
PEG_CRX_GTX_P6	F16	PEG_RXP[9]	PEG_TXP[9]	C16	PEG_CTX_GRX_P6	DIS@	CC58	2	1	0.22U 0402 10V6K	PEG_CTX_C_GRX_P6
PEG_CRX_GTX_N6	E16	PEG_RXN[9]	PEG_TXN[9]	B16	PEG_CTX_GRX_N6	DIS@	CC48	2	1	0.22U 0402 10V6K	PEG_CTX_C_GRX_N6
PEG_CRX_GTX_P5	D15	PEG_RXP[10]	PEG_TXP[10]	A15	PEG_CTX_GRX_P5	DIS@	CC71	2	1	0.22U 0402 10V6K	PEG_CTX_C_GRX_P5
PEG_CRX_GTX_N5	E15	PEG_RXN[10]	PEG_TXN[10]	B15	PEG_CTX_GRX_N5	DIS@	CC59	2	1	0.22U 0402 10V6K	PEG_CTX_C_GRX_N5
PEG_CRX_GTX_P4	F14	PEG_RXP[11]	PEG_TXP[11]	C14	PEG_CTX_GRX_P4	DIS@	CC60	2	1	0.22U 0402 10V6K	PEG_CTX_C_GRX_P4
PEG_CRX_GTX_N4	E14	PEG_RXN[11]	PEG_TXN[11]	B14	PEG_CTX_GRX_N4	DIS@	CC76	2	1	0.22U 0402 10V6K	PEG_CTX_C_GRX_N4
PEG_CRX_GTX_P3	D13	PEG_RXP[12]	PEG_TXP[12]	A13	PEG_CTX_GRX_P3	DIS@	CC61	2	1	0.22U 0402 10V6K	PEG_CTX_C_GRX_P3
PEG_CRX_GTX_N3	E13	PEG_RXN[12]	PEG_TXN[12]	B13	PEG_CTX_GRX_N3	DIS@	CC49	2	1	0.22U 0402 10V6K	PEG_CTX_C_GRX_N3
PEG_CRX_GTX_P2	F12	PEG_RXP[13]	PEG_TXP[13]	C12	PEG_CTX_GRX_P2	DIS@	CC72	2	1	0.22U 0402 10V6K	PEG_CTX_C_GRX_P2
PEG_CRX_GTX_N2	E12	PEG_RXN[13]	PEG_TXN[13]	B12	PEG_CTX_GRX_N2	DIS@	CC62	2	1	0.22U 0402 10V6K	PEG_CTX_C_GRX_N2
PEG_CRX_GTX_P1	D11	PEG_RXP[14]	PEG_TXP[14]	A11	PEG_CTX_GRX_P1	DIS@	CC63	2	1	0.22U 0402 10V6K	PEG_CTX_C_GRX_P1
PEG_CRX_GTX_N1	E11	PEG_RXN[14]	PEG_TXN[14]	B11	PEG_CTX_GRX_N1	DIS@	CC77	2	1	0.22U 0402 10V6K	PEG_CTX_C_GRX_N1
PEG_CRX_GTX_P0	F10	PEG_RXP[15]	PEG_TXP[15]	C10	PEG_CTX_GRX_P0	DIS@	CC64	2	1	0.22U 0402 10V6K	PEG_CTX_C_GRX_P0
PEG_CRX_GTX_N0	E10	PEG_RXN[15]	PEG_TXN[15]	B10	PEG_CTX_GRX_N0	DIS@	CC50	2	1	0.22U 0402 10V6K	PEG_CTX_C_GRX_N0

PEG_COMP G2 — PEG_RCOMP

+1.0VS_VCCIO
PEG_COMP 2 — 24.9_0402_1% — 1 RC2

CAD Note:
Trace width=12 mils ,Spacing=15mil Max length= 400 mils.

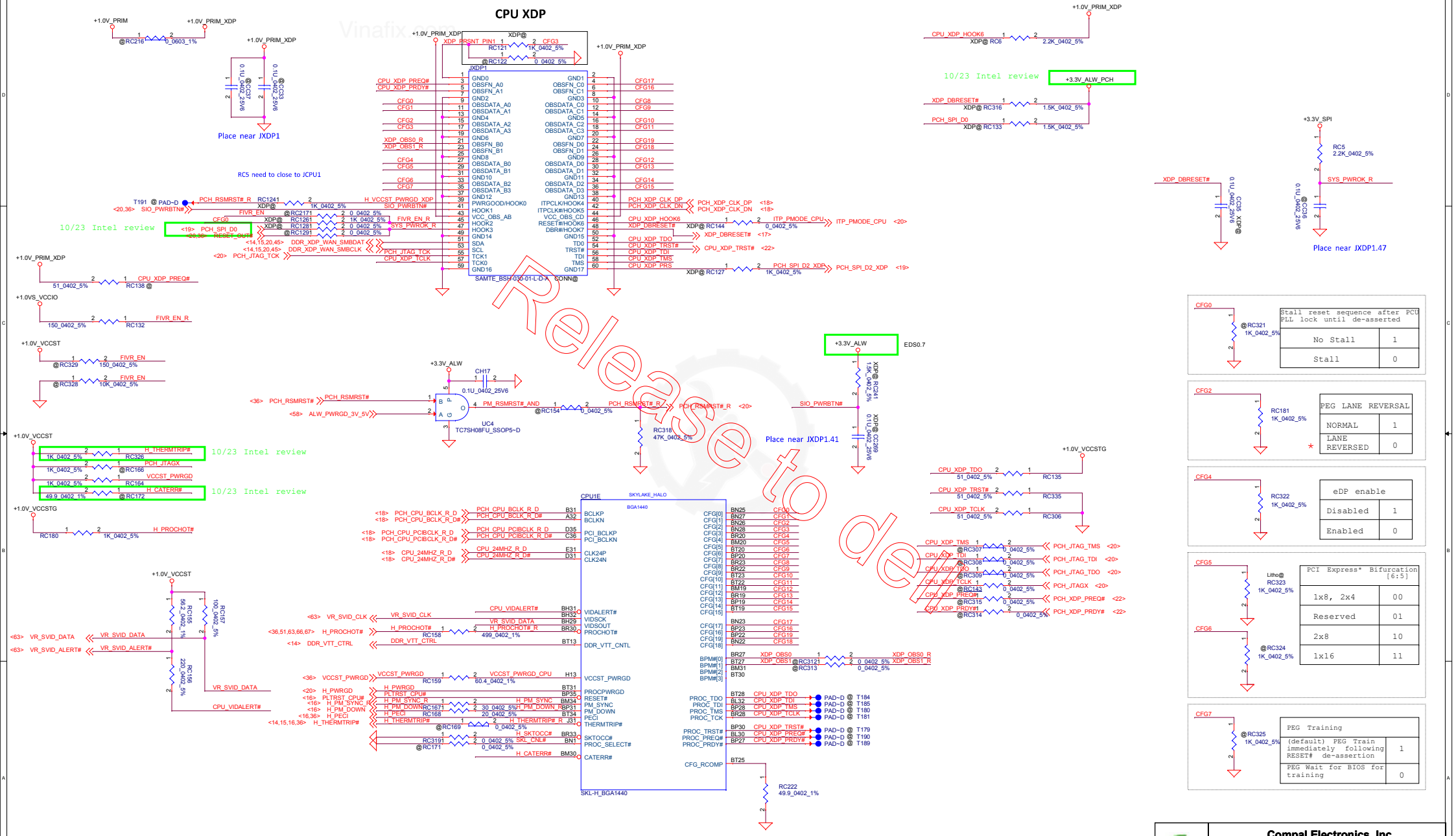
<17> DMI_CRX_PTX_P0	DMI_CRX_PTX_P0	D8	DMI_RXP[0]	DMI_TXP[0]	B8	DMI_CTX_PRX_P0	DMI_CTX_PRX_P0 <17>
<17> DMI_CRX_PTX_N0	DMI_CRX_PTX_N0	E8	DMI_RXN[0]	DMI_TXN[0]	A8	DMI_CTX_PRX_N0	DMI_CTX_PRX_N0 <17>
<17> DMI_CRX_PTX_P1	DMI_CRX_PTX_P1	E6	DMI_RXP[1]	DMI_TXP[1]	C6	DMI_CTX_PRX_P1	DMI_CTX_PRX_P1 <17>
<17> DMI_CRX_PTX_N1	DMI_CRX_PTX_N1	F6	DMI_RXN[1]	DMI_TXN[1]	B6	DMI_CTX_PRX_N1	DMI_CTX_PRX_N1 <17>
<17> DMI_CRX_PTX_P2	DMI_CRX_PTX_P2	D5	DMI_RXP[2]	DMI_TXP[2]	B5	DMI_CTX_PRX_P2	DMI_CTX_PRX_P2 <17>
<17> DMI_CRX_PTX_N2	DMI_CRX_PTX_N2	E5	DMI_RXN[2]	DMI_TXN[2]	A5	DMI_CTX_PRX_N2	DMI_CTX_PRX_N2 <17>
<17> DMI_CRX_PTX_P3	DMI_CRX_PTX_P3	J8	DMI_RXP[3]	DMI_TXP[3]	D4	DMI_CTX_PRX_P3	DMI_CTX_PRX_P3 <17>
<17> DMI_CRX_PTX_N3	DMI_CRX_PTX_N3	J9	DMI_RXN[3]	DMI_TXN[3]	B4	DMI_CTX_PRX_N3	DMI_CTX_PRX_N3 <17>

3 OF 14
REV = 1
SKL-H_BGA1440

Compal Electronics, Inc.

Title: SKL-H (1/8)
Size: Document Number: LA-C841P
Rev: 0.1
Date: Tuesday, September 08, 2015
Sheet 6 of 74

CPU XDP



CFG0	Stall reset sequence after PCU PLL lock until de-asserted
	No Stall 1
	Stall 0

CFG2	PEG LANE REVERSAL
	NORMAL 1
*	LANE REVERSED 0

CFG4	eDP enable
	Disabled 1
	Enabled 0

CFG5	PCI Express* Bifurcation [6:5]
	1x8, 2x4 00
	Reserved 01
	2x8 10
	1x16 11

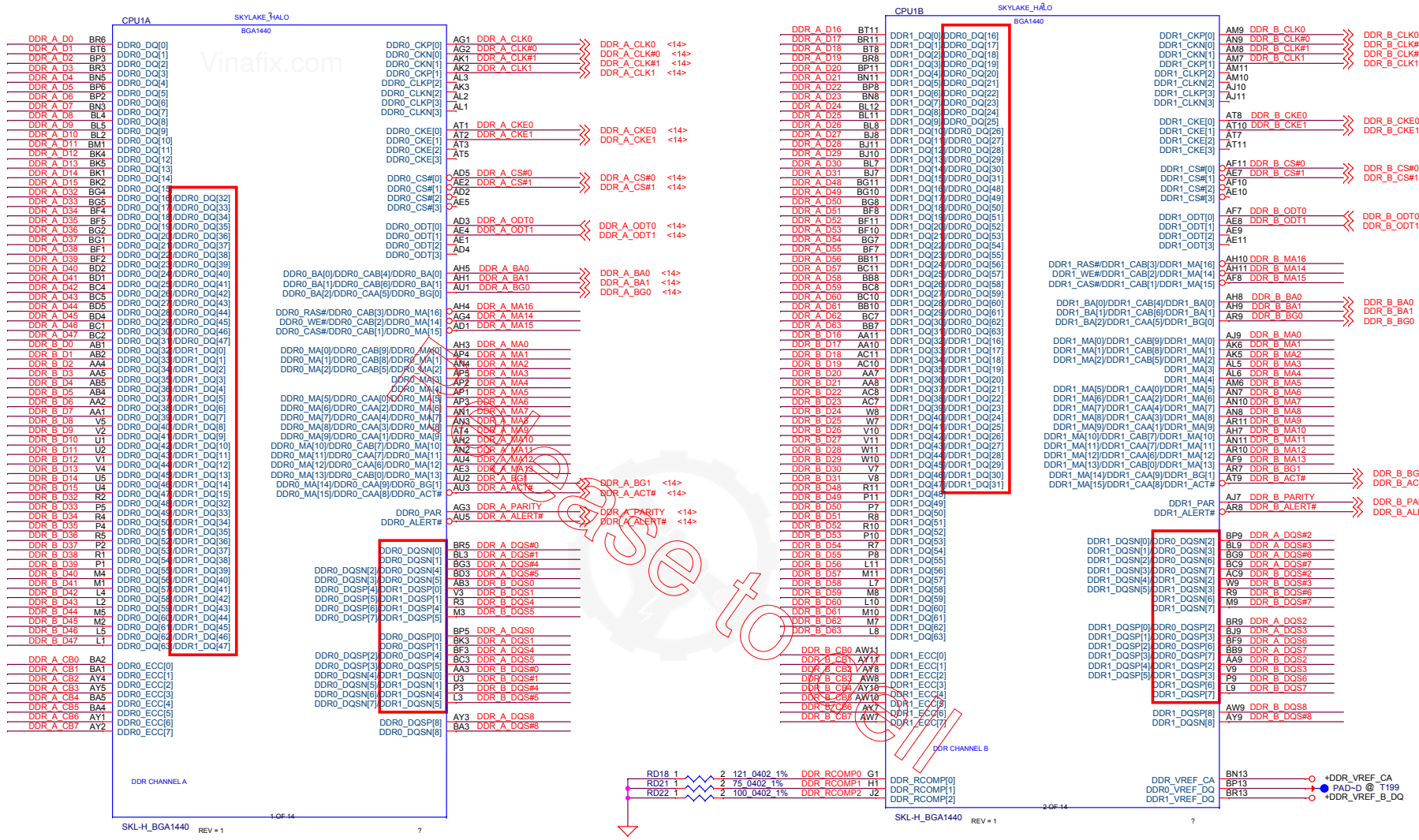
CFG7	PEG Training
	(default) PEG Train immediately following RESET# de-assertion 1
	PEG Wait for BIOS for training 0

Compal Electronics, Inc.

Title: SKL-H (2/8)

Size: | Document Number: LA-C841P | Rev: 0.1

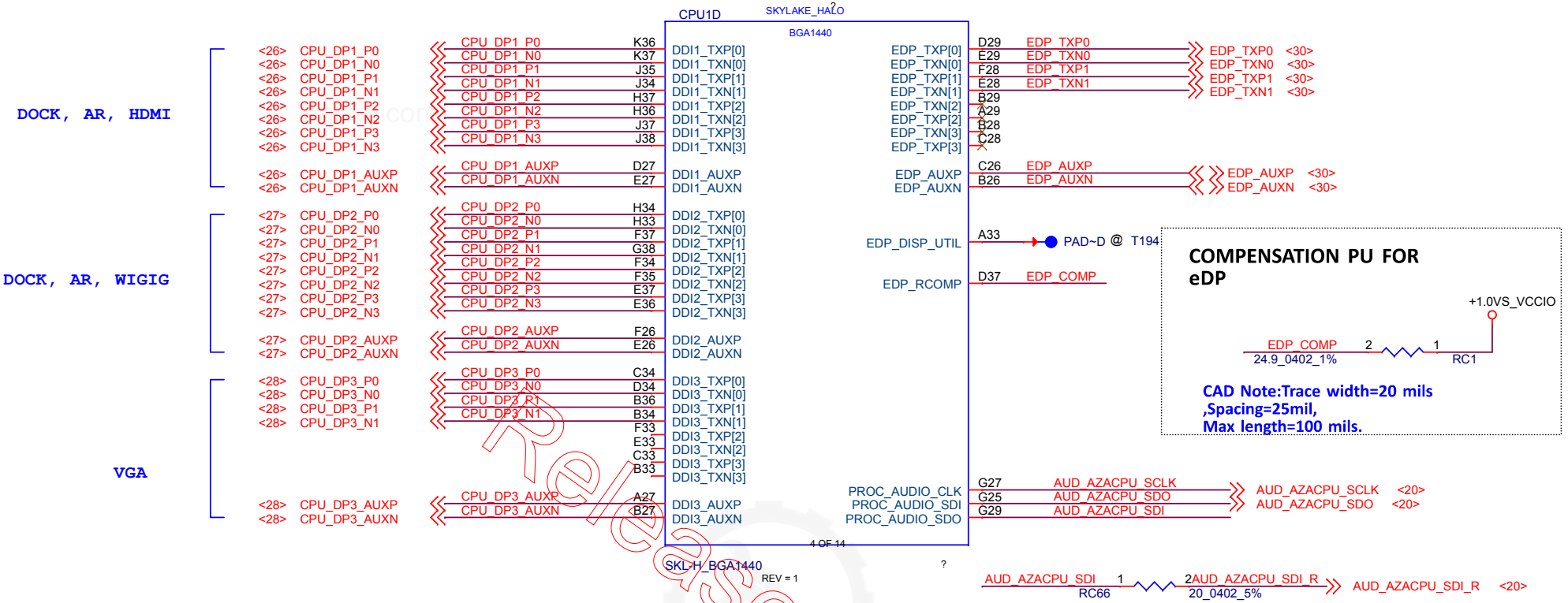
Date: Tuesday, September 08, 2015 | Sheet 7 of 74



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

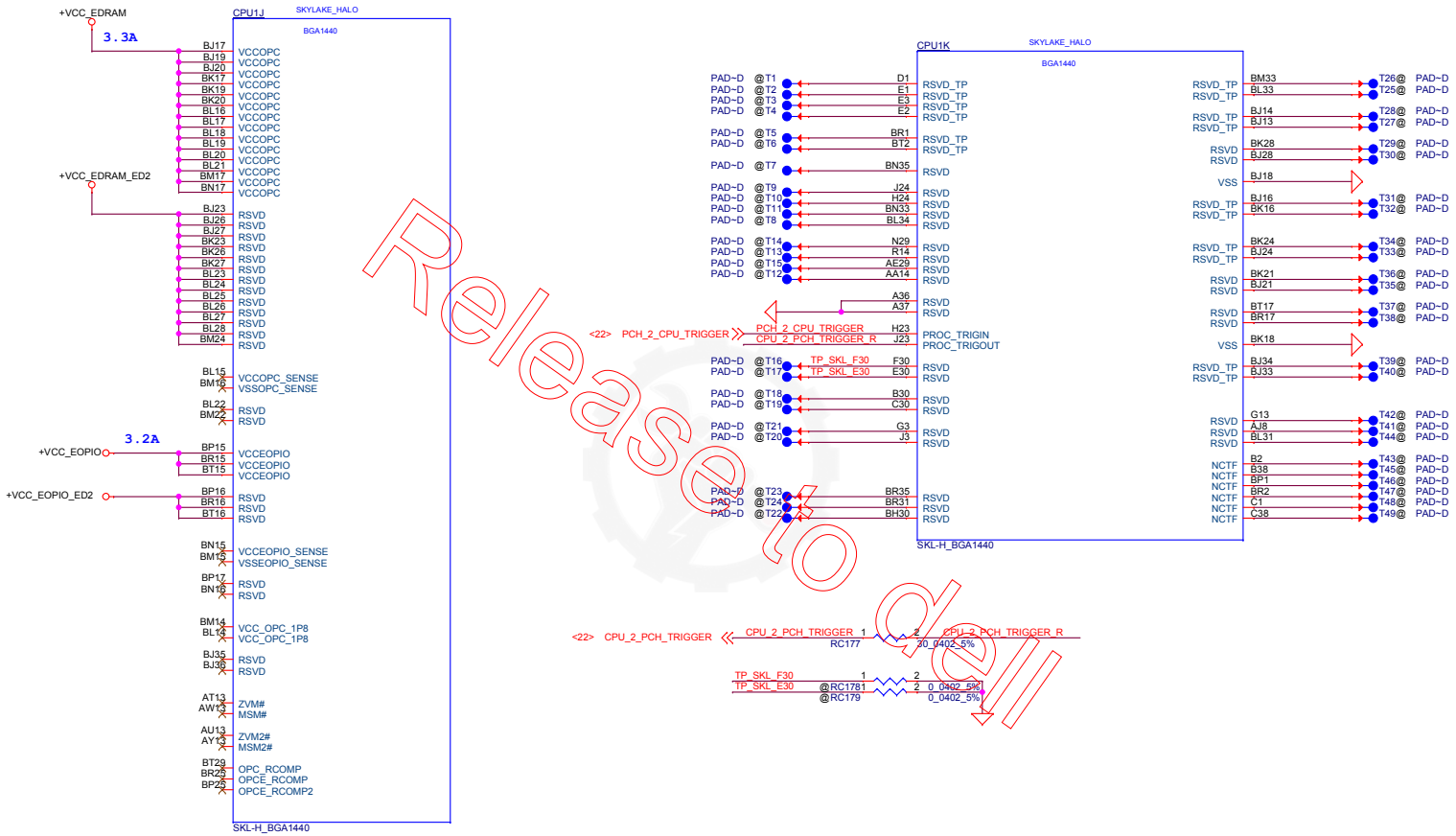
Title	SKL-H (3/8)	
Size	Document Number: LA-C841P	Rev: 0.1
Date: Tuesday, September 08, 2015	Sheet 8 of 74	



DELL CONFIDENTIAL/PROPRIETARY

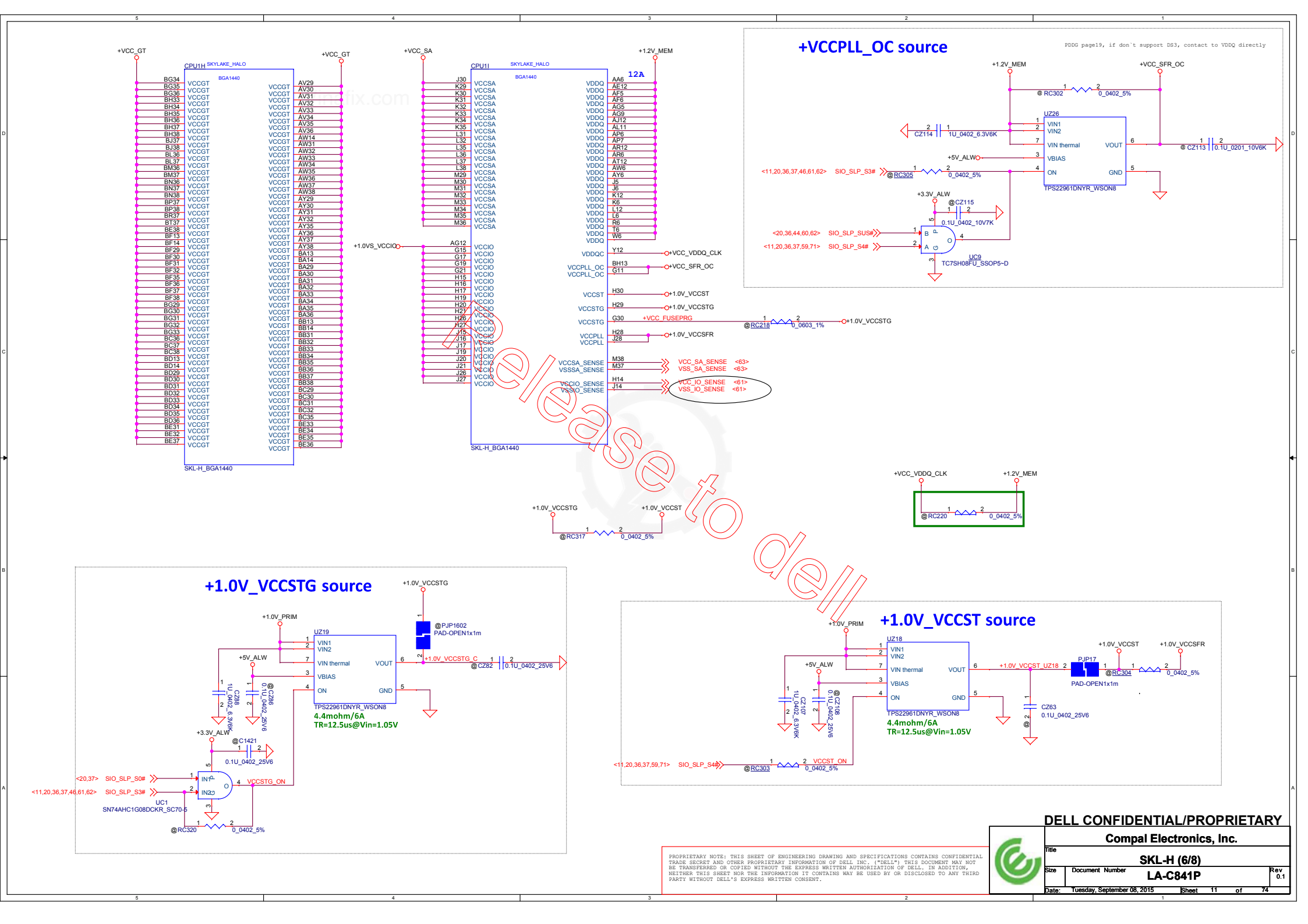
Compal Electronics, Inc.

Title	SKL-H (4/8)	
Size	Document Number LA-C841P	Rev 0.1
Date: Tuesday, September 08, 2015	Sheet 9 of 74	



Compal Electronics, Inc.

Title	SKL-H (5/8)	
Size	Document Number: LA-C841P	Rev: 0.1
Date: Tuesday, September 08, 2015	Sheet 10 of 74	


+VCC_GT
CPU1H SKYLAKE_HALO
BGA1440
+VCC_SA
CPU1I SKYLAKE_HALO
BGA1440
+1.2V_MEM
12A
SKL-H_BGA1440
+1.0VS_VCCIO
+VCC_VDDQ_CLK
+VCC_SFR_OC
+1.0V_VCCST
+1.0V_VCCSTG
+1.0V_VCCSFR
+VCC_FUSEPRG
@RC218
0_0603_1%
VCC_SA_SENSE <63>
VSS_SA_SENSE <63>
VCC_IO_SENSE <61>
VSS_IO_SENSE <61>
+VCCPLL_OC source
PDDG page19, if don`t support DS3, contact to VDDQ directly
@RC302
0_0402_5%
UZ26
CZ114
1U_0402_6.3V6K
@CZ113
0.1U_0201_10V6K
+5V_ALW
<11,20,36,37,46,61,62> SIO_SLP_S3#
@RC305
+3.3V_ALW
@CZ115
0.1U_0402_10V7K
<20,36,44,60,62> SIO_SLP_SUS#
<11,20,36,37,59,71> SIO_SLP_S4#
UC9
TC7SH08FU_SSOP5-D
TPS22961DNYR_WSON8
+1.0V_VCCSTG source
+1.0V_PRIM
UZ19
@PJP1602
PAD-OPEN1x1m
+1.0V_VCCSTG_C
@CZ282
0.1U_0402_25V6
CZ288
1U_0402_6.3V6K
@CZ296
0.1U_0402_25V6
4.4mohm/6A
TR=12.5us@Vin=1.05V
@C1421
<20,37> SIO_SLP_S0#
VCCSTG_ON
UC1
SN74AHC1G08DCKR_SC70-5
@RC320
+1.0V_VCCST source
UZ18
+1.0V_VCCST_UZ18
PJP17
PAD-OPEN1x1m
@RC304
CZ107
CZ108
CZ263
@RC303
VCCST_ON
@RC220
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
Title
SKL-H (6/8)
Size
Document Number
LA-C841P
Rev
0.1
Date: Tuesday, September 08, 2015
Sheet 11 of 74

For SKL-H 4+2
Remove VCCOPC/VCCEOPIO/
VCCOPC_1P8 Cap

PLACE CAP BACKSIDE

+VCC_VDDQ_CLK
10U_0603_6.3V6M~D CC185

+1.0V_VCCSTG
1U_0402_6.3V6K CC186
1U_0402_6.3V6K CC195

+1.0V_VCCSFR
1U_0402_6.3V6K CC192

+1.0V_VCCST
1U_0402_6.3V6K CC191

+VCC_SFR_OC
1U_0402_6.3V6K CC210
1U_0402_6.3V6K CC209

+1.0VS_VCCIO
PLACE CAP BACKSIDE
22U_0603_6.3V6M CC188
22U_0603_6.3V6M CC189
22U_0603_6.3V6M CC187
22U_0603_6.3V6M CC222

Remove VCC_SA cap
from EE side.

+1.0V_VCCST
1U_0402_6.3V6K CC193
1U_0402_6.3V6K CC194

+1.2V_MEM
+1.2V_MEM DECOUPLING
PLACE CAP BACKSIDE
10U_0603_6.3V6M~D CC161
10U_0603_6.3V6M~D CC170
10U_0603_6.3V6M~D CC164
10U_0603_6.3V6M~D CC168
10U_0603_6.3V6M~D CC163
10U_0603_6.3V6M~D CC166
10U_0603_6.3V6M~D CC171
10U_0603_6.3V6M~D CC165
10U_0603_6.3V6M~D CC172
10U_0603_6.3V6M~D CC167
22U_0603_6.3V6M CC230
22U_0603_6.3V6M CC82
22U_0603_6.3V6M CC83
22U_0603_6.3V6M CC84

+VCC_GT
+VCC_GTU

CPU1N SKYLAKE_HALO BGA1440

VCCGT: AJ29 AJ30 AJ31 AJ32 AJ33 AJ34 AJ35 AJ36 AK31 AK32 AK33 AK34 AK35 AK36 AK37 AK38 AL13 AL29 AL30 AL31 AL32 AL35 AL36 AL37 AL38 AM13 AM14 AM29 AM30 AM31 AM32 AM33 AM34 AM35 AM36 AN13 AN14 AN31 AN32 AN33 AN34 AN35 AN36 AN37 AN38 AP13 AP14 AP29 AP30 AP31 AP32 AP35 AP36 AP37 AP38 AR29 AR30 AR31 AR32 AR33 AR34 AR35 AR36 AT14 AT31 AT32 AT33 AT34 AT35 AT36 AT37 AT38 AU14 AU29 AU30 AU31 AU32 AU35 AU36 AU37 AU38

VCCGTX: AF29 AF30 AF31 AF32 AF33 AF34 AG13 AG14 AG31 AG32 AG33 AG34 AG35 AG36 AH13 AH14 AH29 AH30 AH31 AH32 AJ13 AJ14

VCCGT_SENSE AH38 → VCC_GT_SENSE <63>
VSSGTX_SENSE AH35
VSSGT_SENSE AH37 → VSS_GT_SENSE <63>
VCCGTX_SENSE AH36

SKL-H_BGA1440

+VCC_CORE
+VCC_CORE

CPU1G SKYLAKE_HALO BGA1440

VCC: AA13 AA31 AA32 AA33 AA34 AA35 AA36 AA37 AA38 AB29 AB30 AB31 AB32 AB35 AB36 AB37 AB38 AC13 AC14 AC29 AC30 AC31 AC32 AC33 AC34 AC35 AC36 AD13 AD14 AD31 AD32 AD33 AD34 AD35 AD36 AD37 AD38 AE13 AE14 AE30 AE31 AE32 AE35 AE36 AE37 AE38 AF35 AF36 AF37 AF38 K13 K14 L13 N13 N14 N30 N31 N32 N35 N36 N37 N38 P13

VCC: V32 V33 V34 V35 V36 V37 V38 W13 W14 W29 W30 W31 W32 W35 W36 W37 W38 Y29 Y30 Y31 Y32 Y33 Y34 Y35 Y36 L14 P29 P30 P31 P32 P33 P34 P35 P36 R13 R31 R32 R33 R34 R35 R36 R37 R38 T29 T30 T31 T32 T35 T36 T37 T38 U29 U30 U31 U32 U33 U34 U35 U36 V13 V14 V31 P14

VCC_SENSE
VSS_SENSE

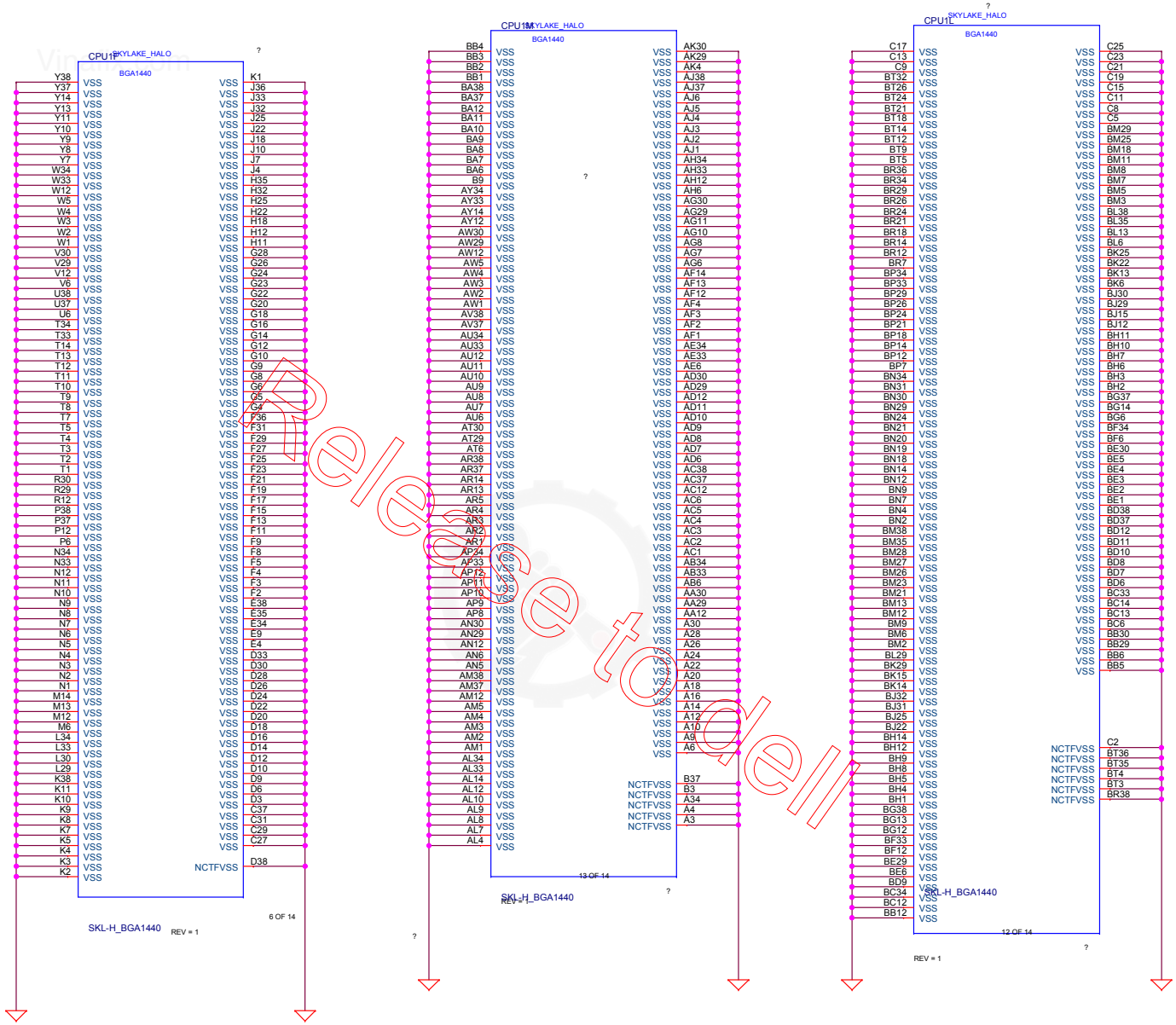
SKL-H_BGA1440

+VCC_CORE
RC140 100_0402_1%
AG37 VCC_SENSE → VCC_SENSE <63>
AG38 VSS_SENSE → VSS_SENSE <63>
RC141 100_0402_1%

VSS_SENSE @RC221 49.9_0402_1% VCC_SENSE

Compal Electronics, Inc.

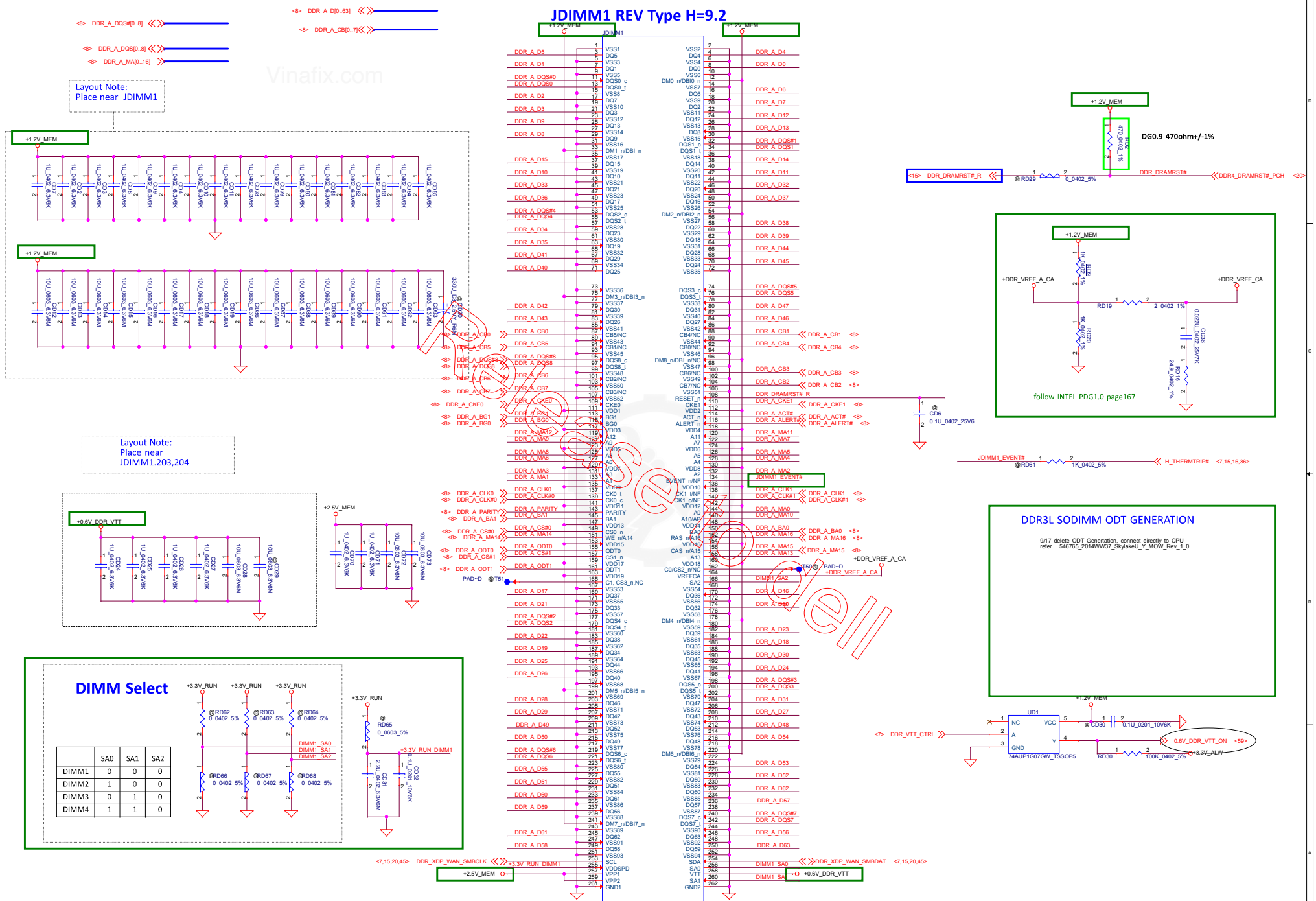
Title: SKL-H (7/8)
Size: Document Number: LA-C841P
Rev: 0.1
Date: Tuesday, September 08, 2015
Sheet 12 of 74



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	SKL-H (8/8)
Size	Document Number: LA-C841P
Rev	0.1
Date: Tuesday, September 08, 2015	Sheet 13 of 74

JDIMM1 REV Type H=9.2

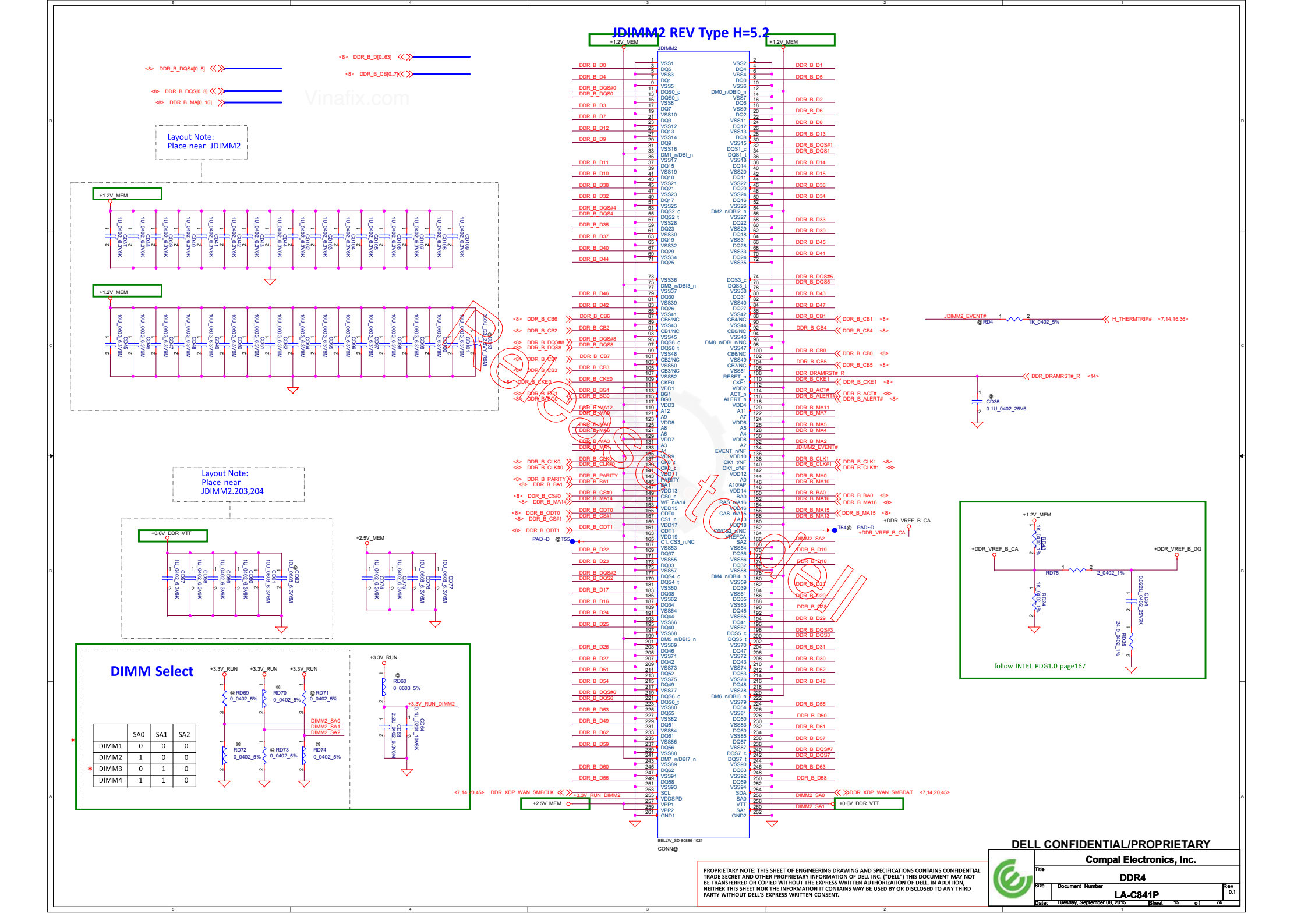


	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0

Compal Electronics, Inc.

Title	DDR4	
Size	Document Number: LA-C841P	Rev: 0.1
Date: Tuesday, September 08, 2015	Sheet 14 of 74	

JDIMM2 REV Type H=5.2



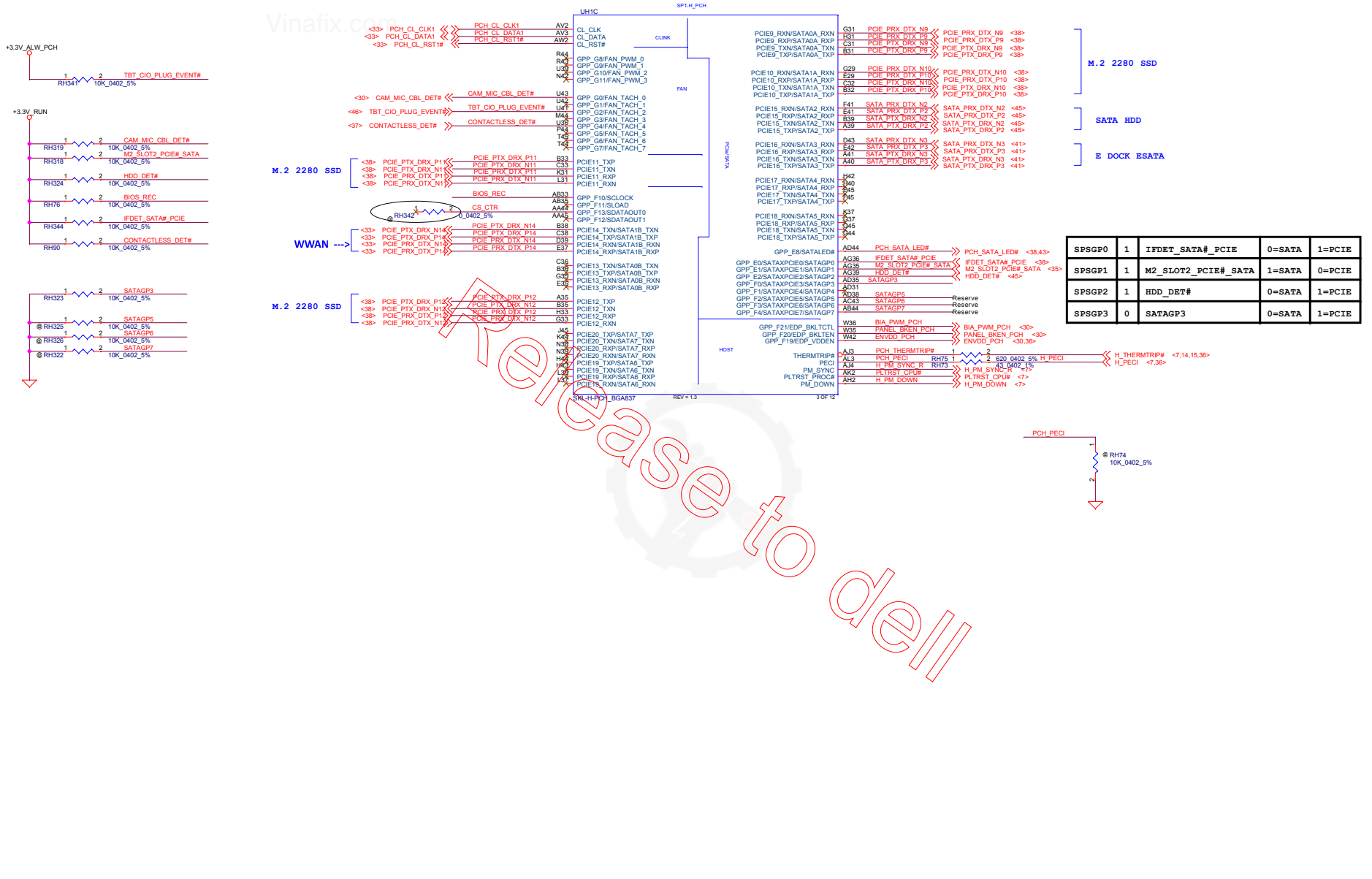
	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
* DIMM3	0	1	0
DIMM4	1	1	0

Compal Electronics, Inc.

Title: DDR4

Size: | Document Number: LA-C841P | Rev: 0.1

Date: Tuesday, September 08, 2015 | Sheet 15 of 74



SPSGP0	1	IFDET_SATA#_PCIE	0=SATA	1=PCIE
SPSGP1	1	M2_SLOT2_PCIE#_SATA	1=SATA	0=PCIE
SPSGP2	1	HDD_DET#	0=SATA	1=PCIE
SPSGP3	0	SATAGP3	0=SATA	1=PCIE

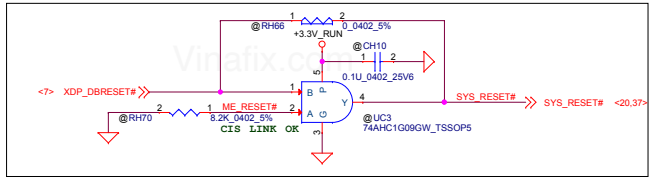
DELL CONFIDENTIAL/PROPRIETARY

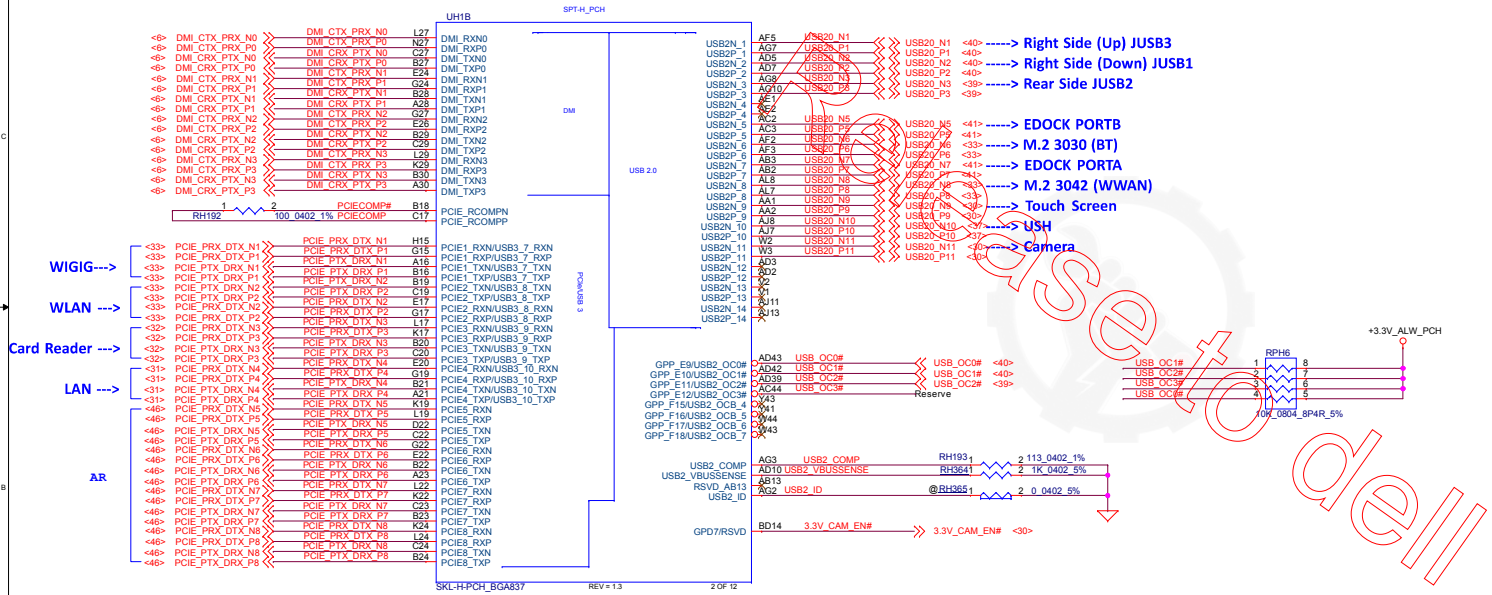
Compal Electronics, Inc.

Title: SKYLAKE PCH-H (1/9)

Size: | Document Number: LA-C841P | Rev: 0.1

Date: Tuesday, September 08, 2015 | Sheet 16 of 74



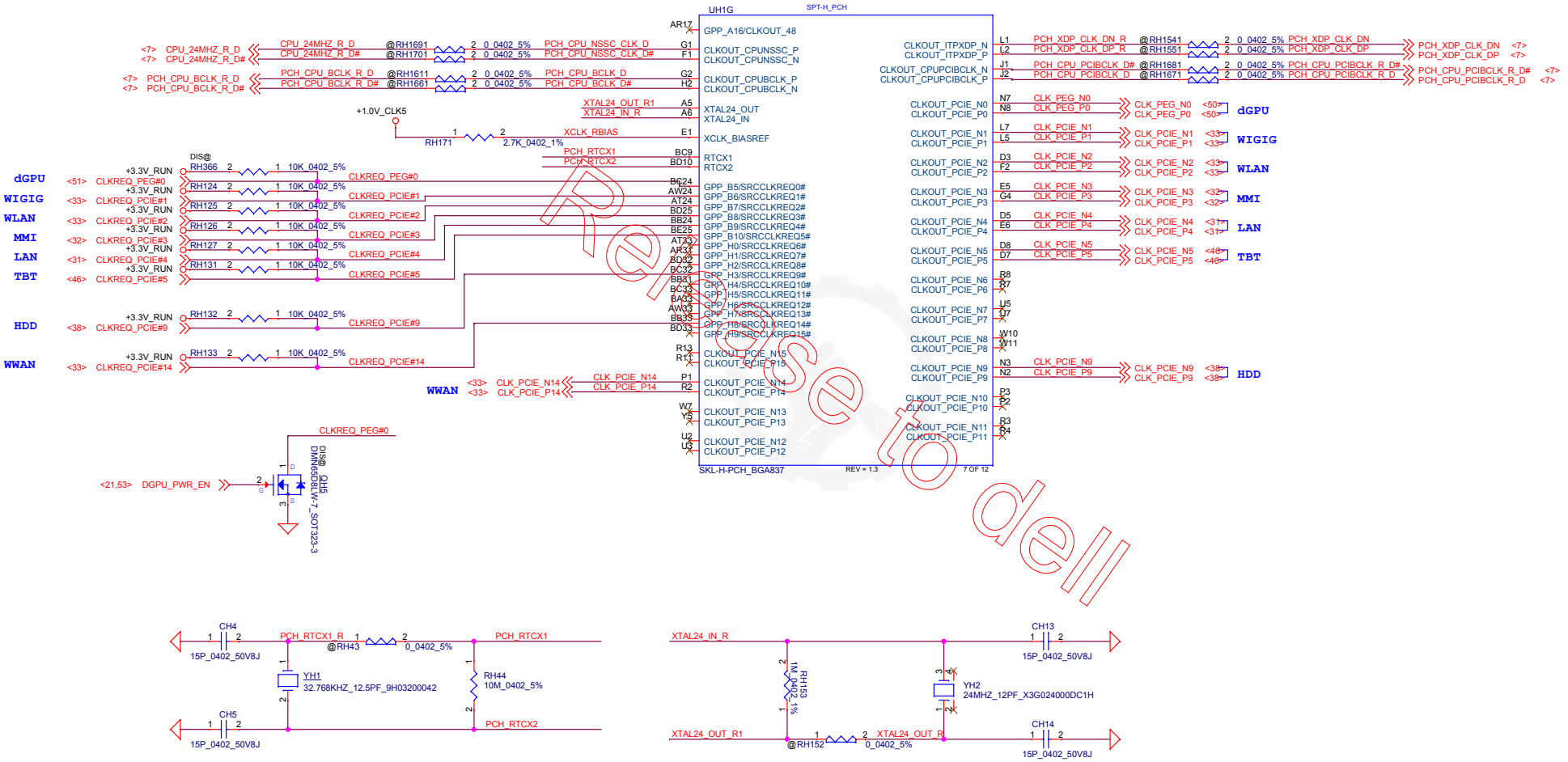


Compal Electronics, Inc.

Title: SKYLAKE PCH-H (2/9)

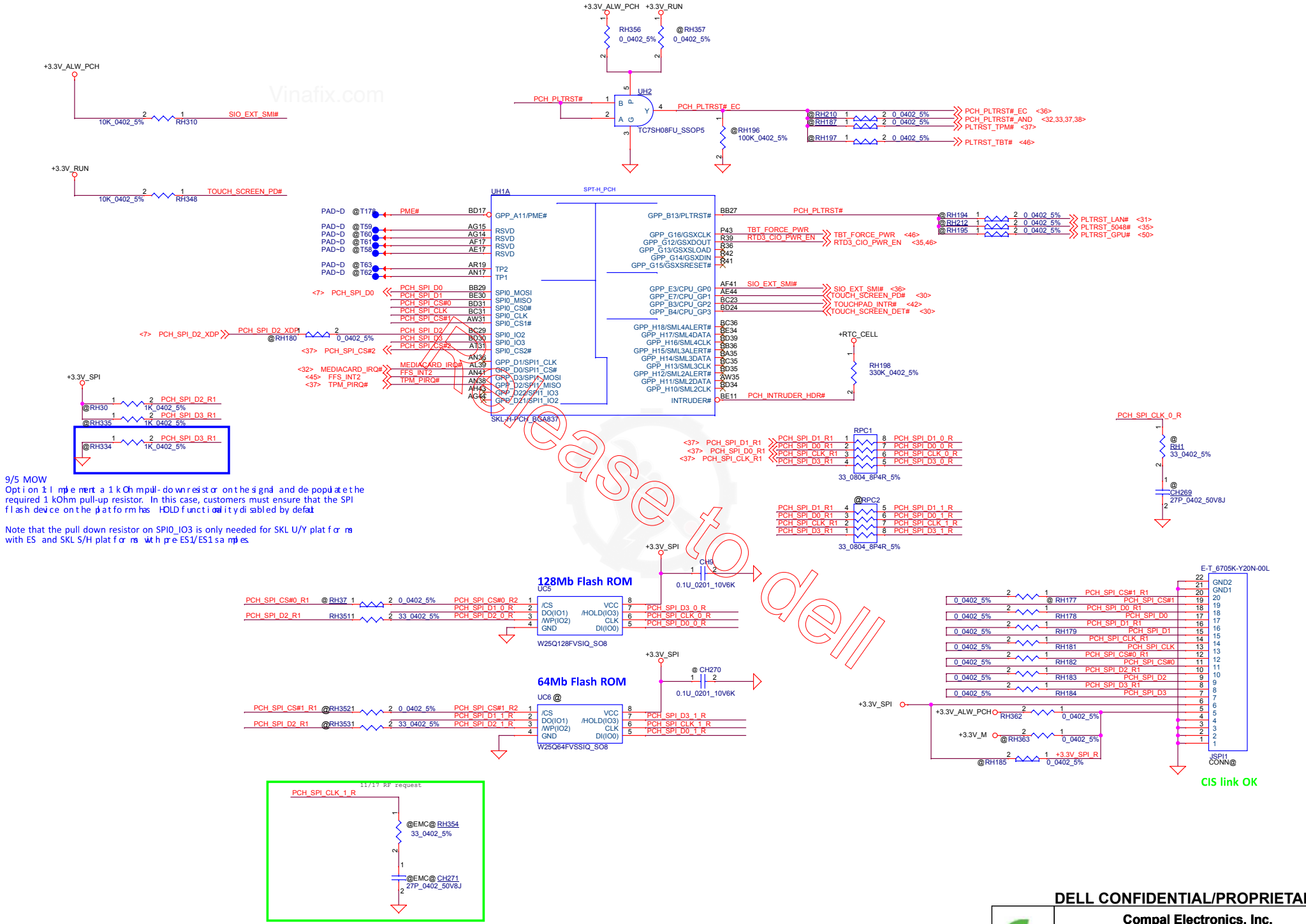
Size: | Document Number: LA-C841P | Rev: 0.1

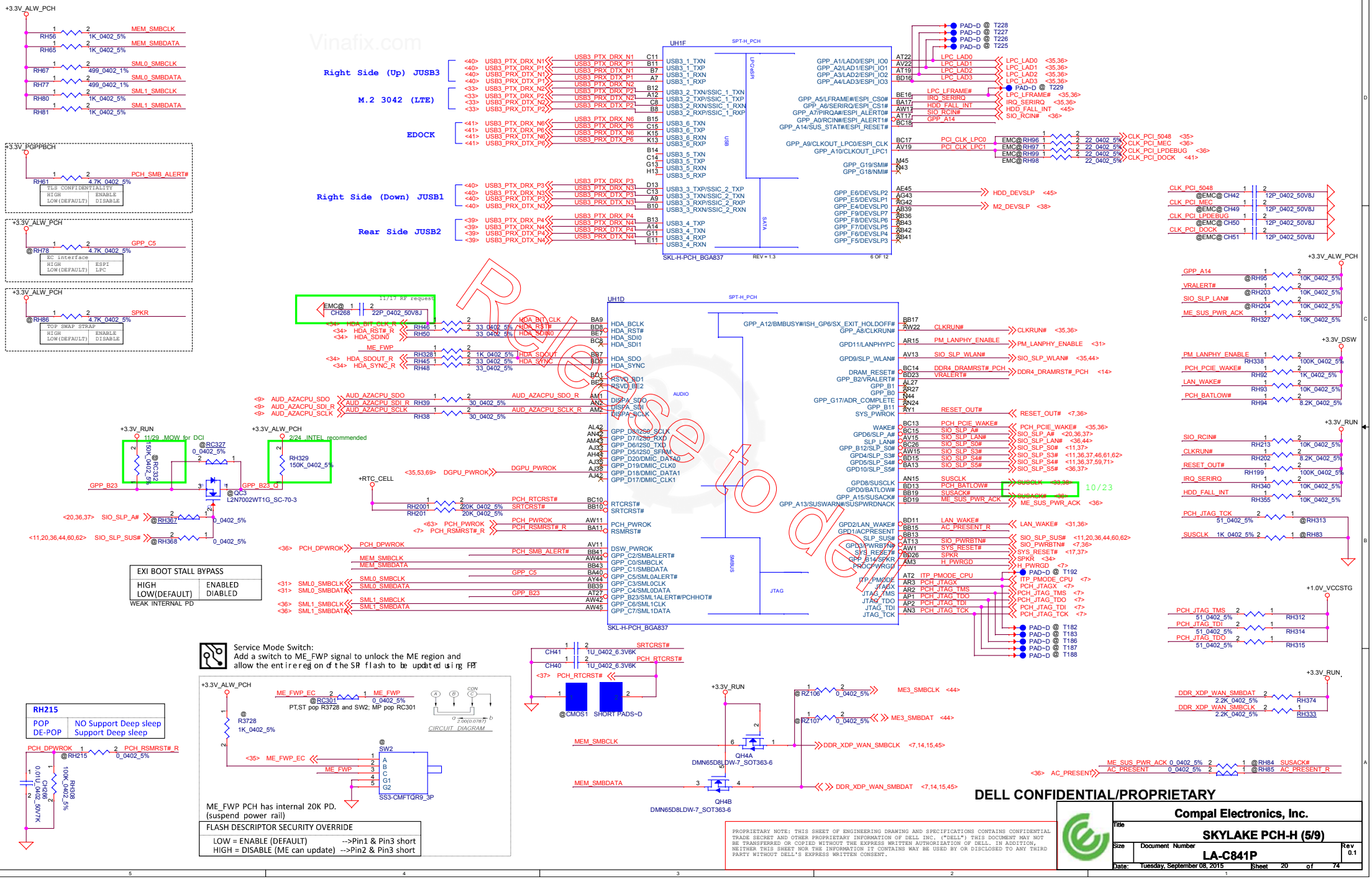
Date: Tuesday, September 08, 2015 | Sheet 17 of 74

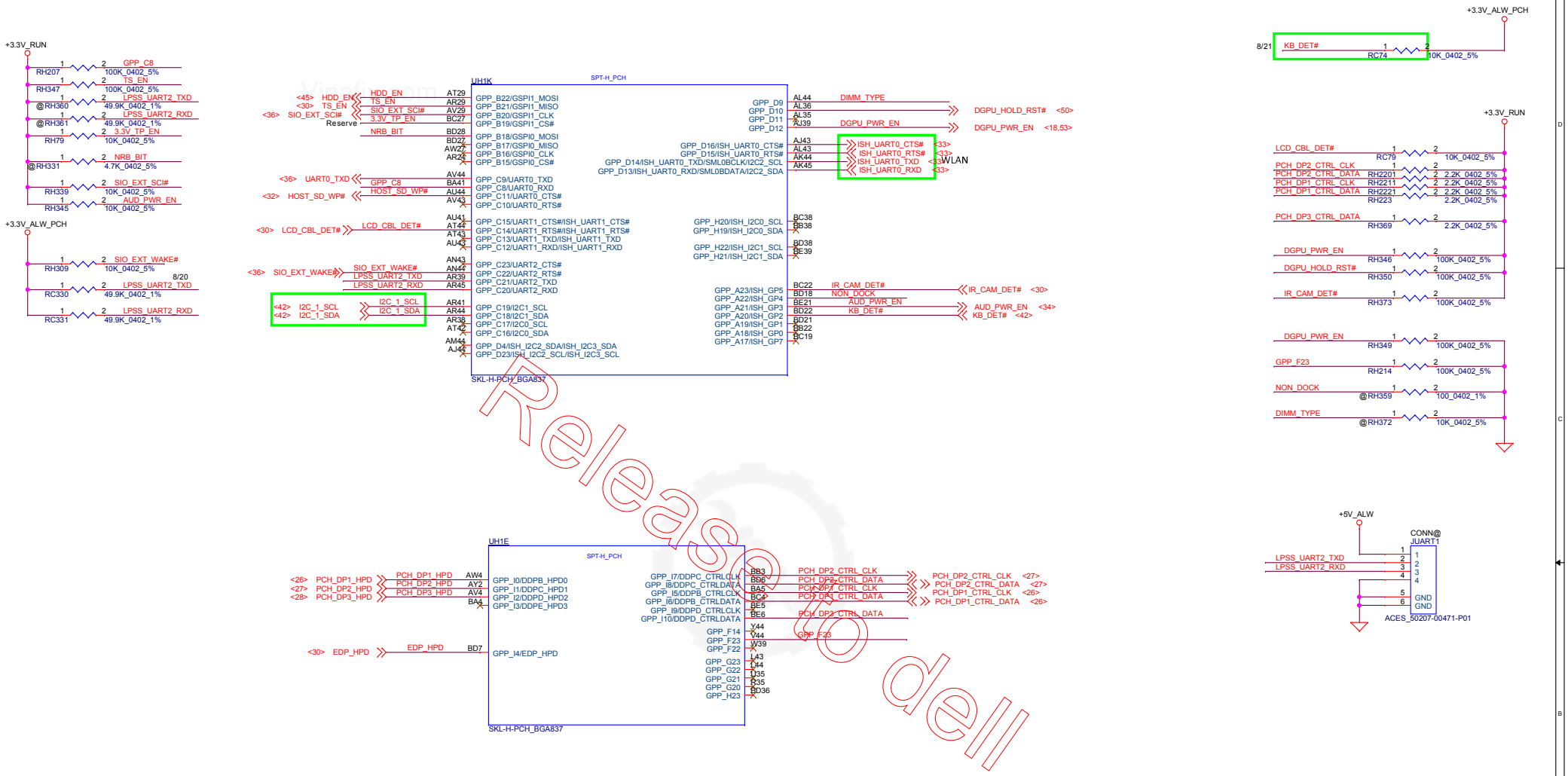


DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	SKYLAKE PCH-H (3/9)
Size	Document Number: LA-C841P
Rev	0.1
Date: Tuesday, September 08, 2015	Sheet 18 of 74




Right Side (Up) JUSB3
M.2 3042 (LTE)
EDOCK
Right Side (Down) JUSB1
Rear Side JUSB2
UH1F
SPT-H_PCH
SKL-H-PCH_BGA837
UH1D
Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FPT
ME_FWP PCH has internal 20K PD. (suspend power rail)
EXI BOOT STALL BYPASS
HIGH ENABLED
LOW(DEFAULT) DIABLED
WEAK INTERNAL PD
FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = ENABLE (DEFAULT) -->Pin1 & Pin3 short
HIGH = DISABLE (ME can update) -->Pin2 & Pin3 short
RH215
POP NO Support Deep sleep
DE-POP Support Deep sleep
Vinafix.com
Reserved
10/23
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
SKYLAKE PCH-H (5/9)
LA-C841P
Rev 0.1
Tuesday, September 08, 2015
Sheet 20 of 74



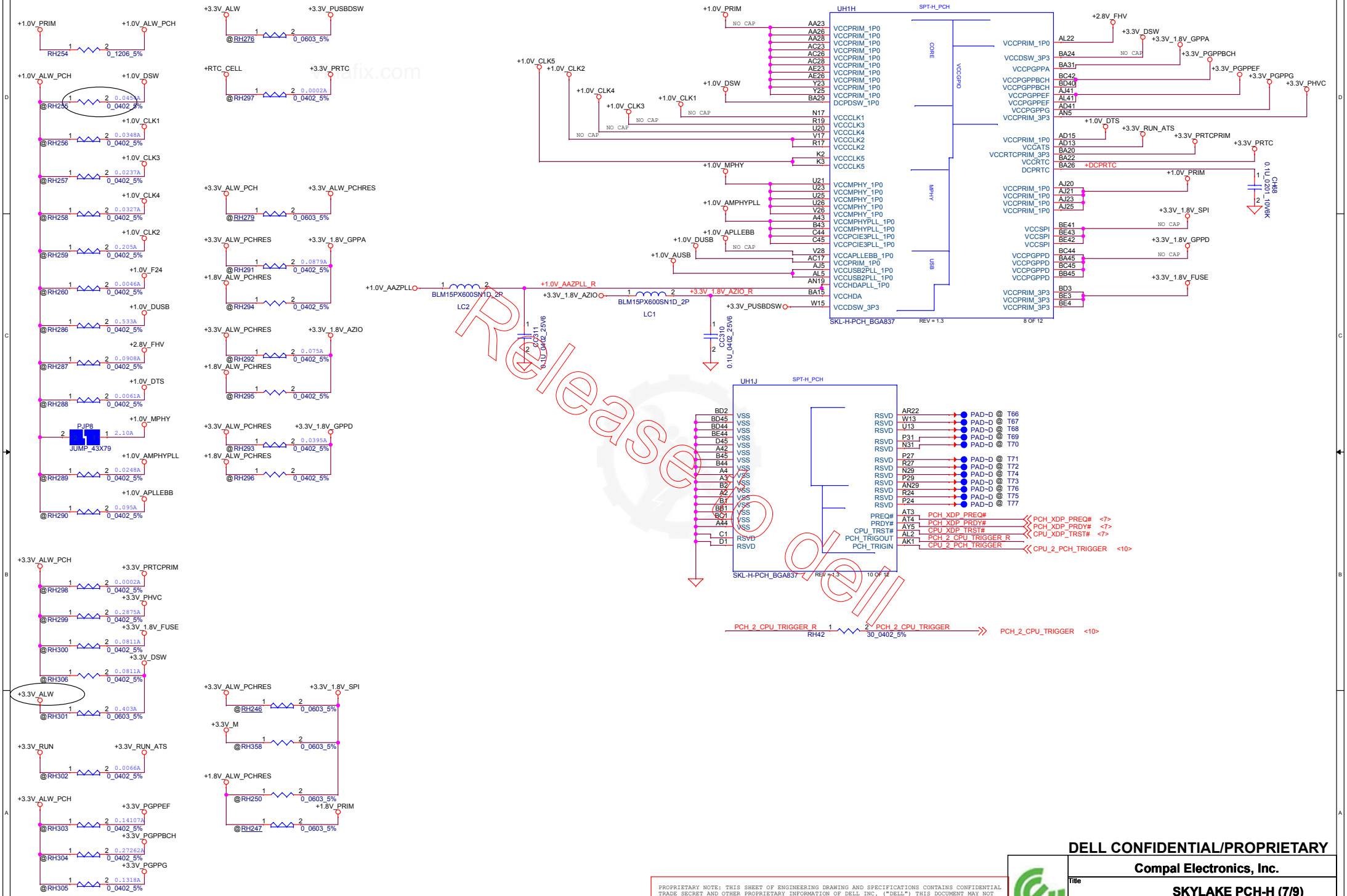
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: SKYLAKE PCH-H (6/9)

Size: | Document Number: LA-C841P | Rev: 0.1

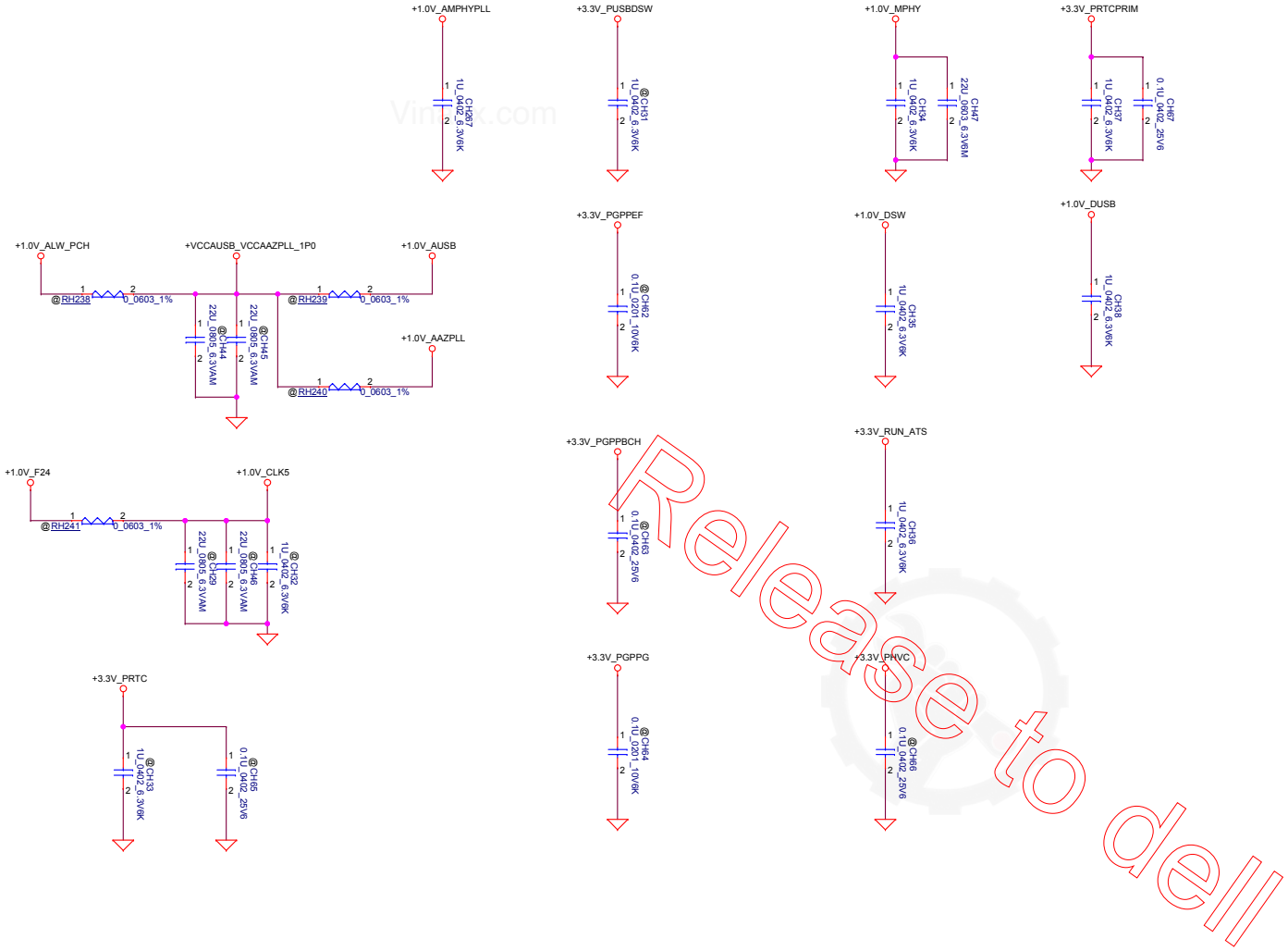
Date: Tuesday, September 08, 2015 | Sheet 21 of 74



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title	SKYLAKE PCH-H (7/9)	
Size	Document Number LA-C841P	Rev 0.1
Date: Tuesday, September 08, 2015	Sheet 22 of 74	



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	SKYLAKE PCH-H (8/9)
Size	Document Number: LA-C841P
Rev	0.1
Date: Tuesday, September 08, 2015	Sheet 23 of 74

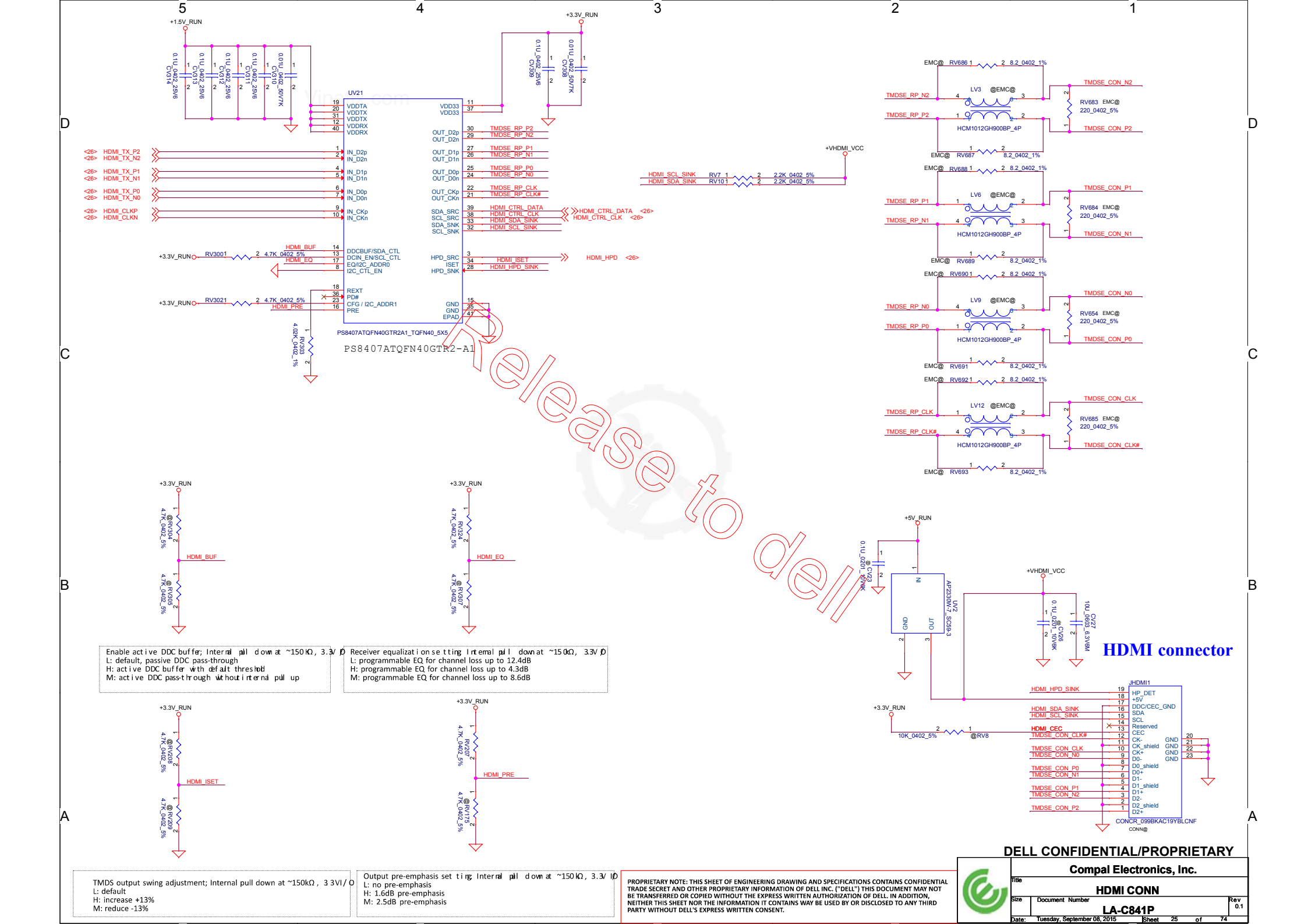
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: SKYLAKE PCH-H (9/9)

Size | Document Number: LA-C841P | Rev: 0.1

Date: Tuesday, September 08, 2015 | Sheet 24 of 74



Enable active DDC buffer; Internal pull down at ~150kΩ, 3.3V I/O
L: default, passive DDC pass-through
H: active DDC buffer with default threshold
M: active DDC pass-through without internal pull up

Receiver equalization setting Internal pull down at ~150kΩ, 3.3V I/O
L: programmable EQ for channel loss up to 12.4dB
H: programmable EQ for channel loss up to 4.3dB
M: programmable EQ for channel loss up to 8.6dB

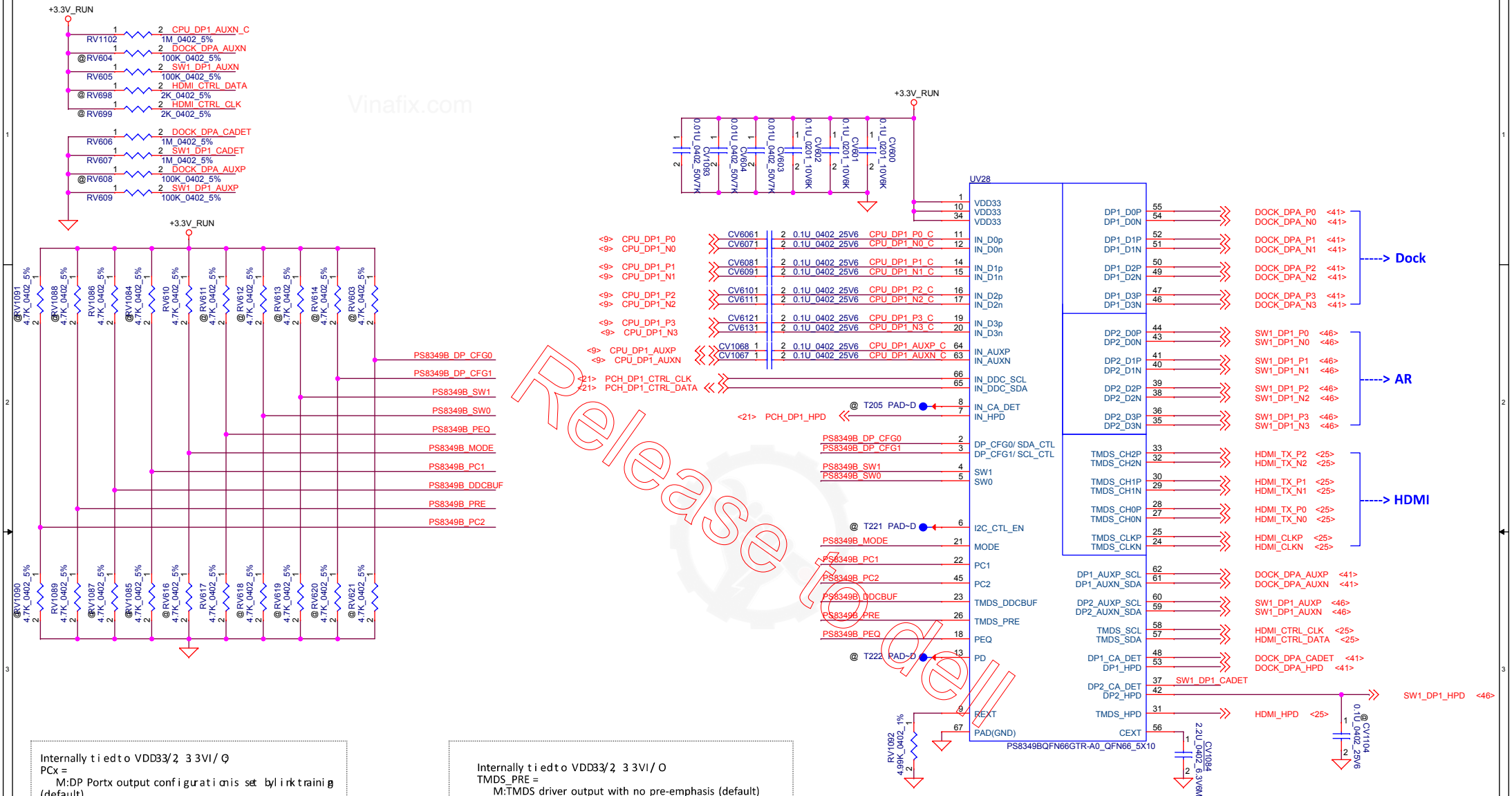
TMDS output swing adjustment; Internal pull down at ~150kΩ, 3.3V I/O
L: default
H: increase +13%
M: reduce -13%

Output pre-emphasis setting Internal pull down at ~150kΩ, 3.3V I/O
L: no pre-emphasis
H: 1.6dB pre-emphasis
M: 2.5dB pre-emphasis

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

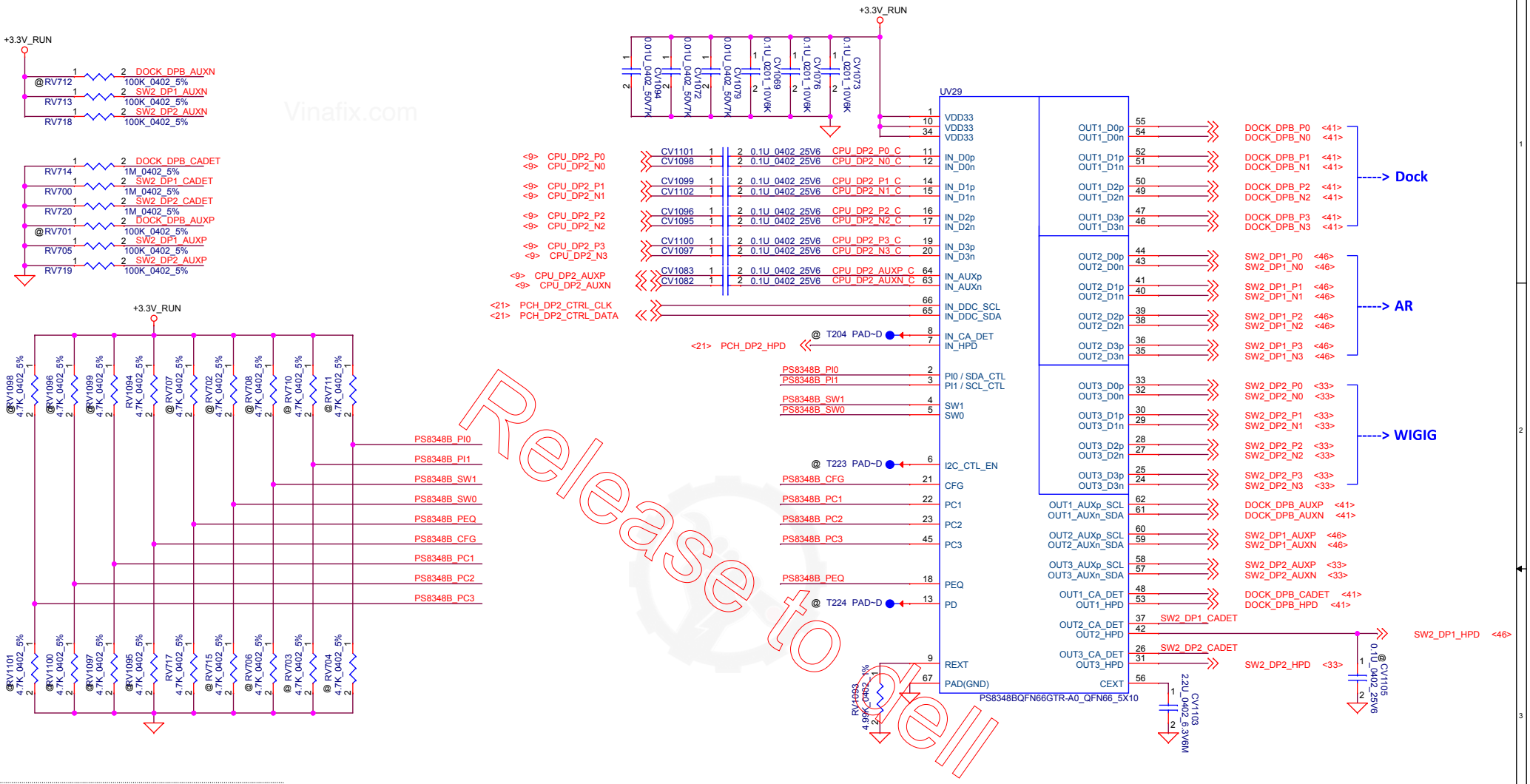
Title	HDMI CONN	
Size	Document Number: LA-C841P	Rev: 0.1
Date: Tuesday, September 08, 2015	Sheet 25 of 74	



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title	DP SW PS8349B	
Size	Document Number LA-C841P	Rev 0.1
Date: Tuesday, September 08, 2015	Sheet 26 of 74	



Internally tied to VDD33/2, 3.3V I/O
PCx =
M:Portx output configuration is set by link training (default)
H:Portx output with fixed 800 mV and 0dB
L:Portx output with fixed 400 mV and 0dB
x=1, 2, 3

Internally pull down ~150K.3.3V I/O
For Control Switching Mode (CFG = L):
[SW1,SW0]= [L,L], Port1 is selected (default)
[SW1,SW0]= [L,H], Port2 is selected
[SW1,SW0]= [H,L], Port3 is selected
[SW1,SW0]= [H,H], Port3 is selected
For Automatic Switching Mode(CFG= H):
[SW1,SW0]= [L,L], Port1 >Port2 >Port3 (default)
[SW1,SW0]= [L,H], Port1 >Port3 >Port2
[SW1,SW0]= [H,L], Port3 >Port2 >Port1
[SW1,SW0]= [H,H], Port3 >Port1 >Port2
[SW1,SW0]= [L,M], Port2 >Port1 >Port3
[SW1,SW0]= [M,M], Port2 >Port3 >Port1

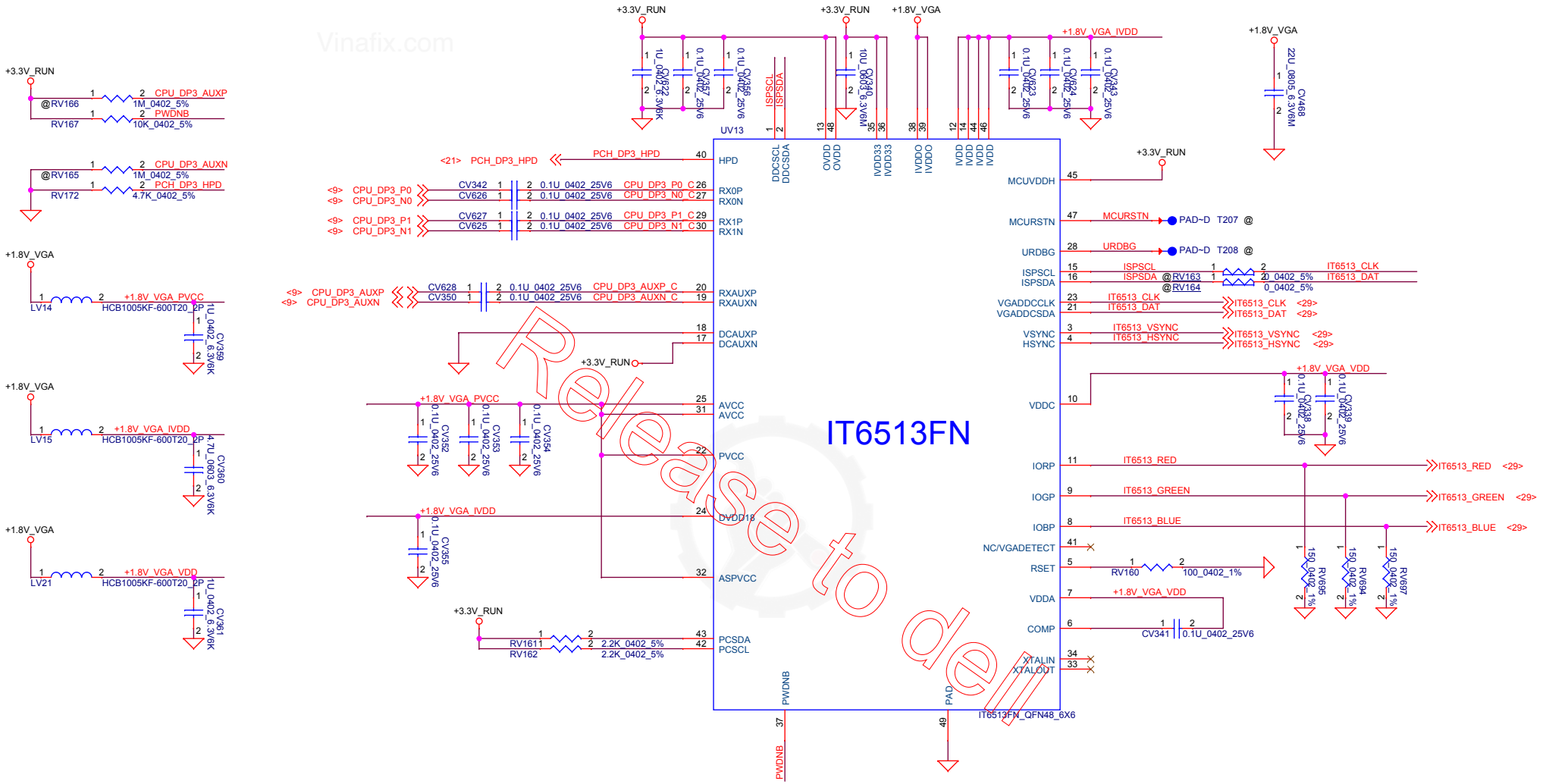
Internally tied to VDD33/2, 3.3V I/O
PEQ =
M:default, LEQ, compensate channel loss up to 11.5dB @ HBR2
H:HEQ, compensate channel loss up to 14.5dB @ HBR2
L:LLEQ, compensate channel loss up to 8.5dB @ HBR2

Compal Electronics, Inc.

Title: DP MUX PS8348B

Size | Document Number: LA-C841P | Rev: 0.1

Date: Tuesday, September 08, 2015 | Sheet 27 of 74

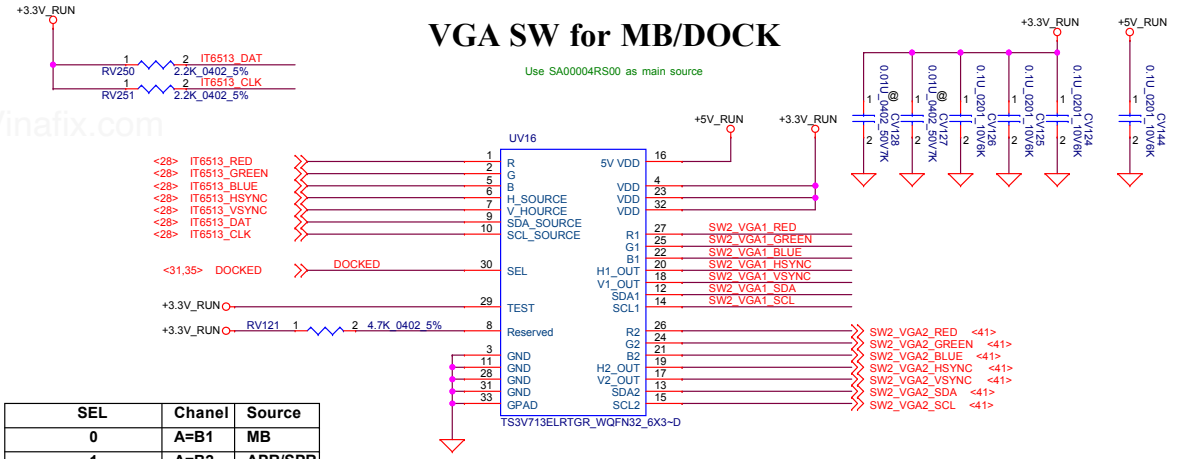


DELL CONFIDENTIAL/PROPRIETARY

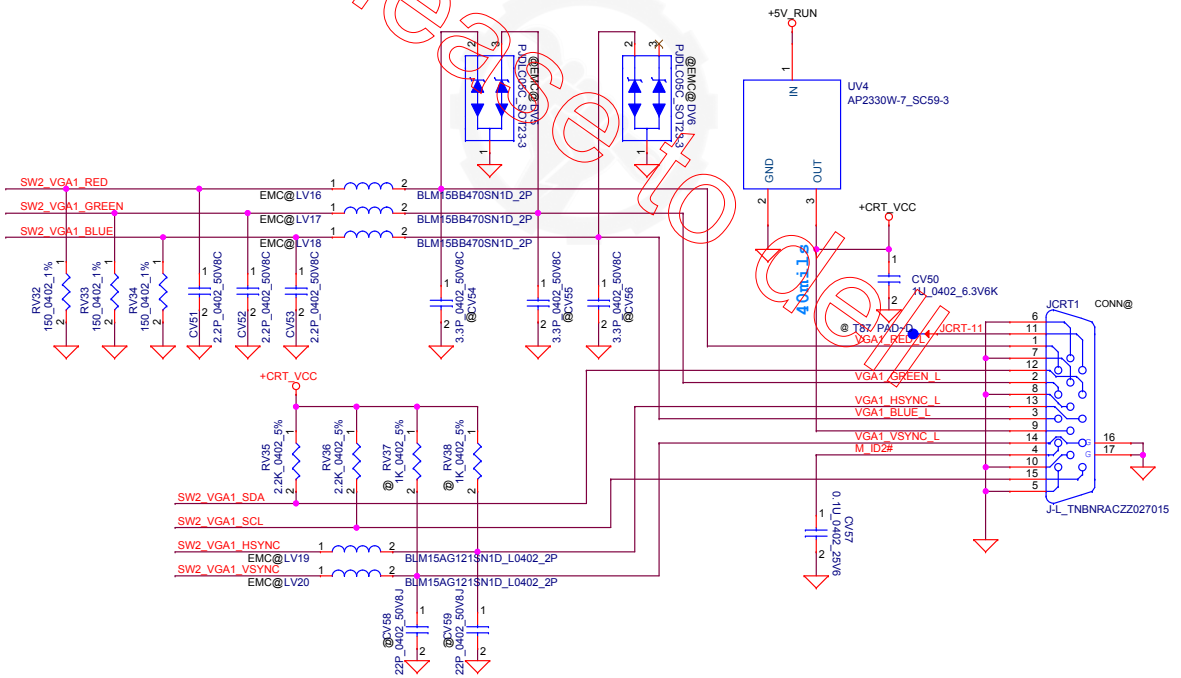
Compal Electronics, Inc.	
Title	DP - VGA
Size	Document Number: LA-C841P
Rev	0.1
Date:	Tuesday, September 08, 2015
Sheet	28 of 74

VGA SW for MB/DOCK

Use SA00004RS00 as main source



SEL	Chanel	Source
0	A=B1	MB
1	A=B2	APR/SPR

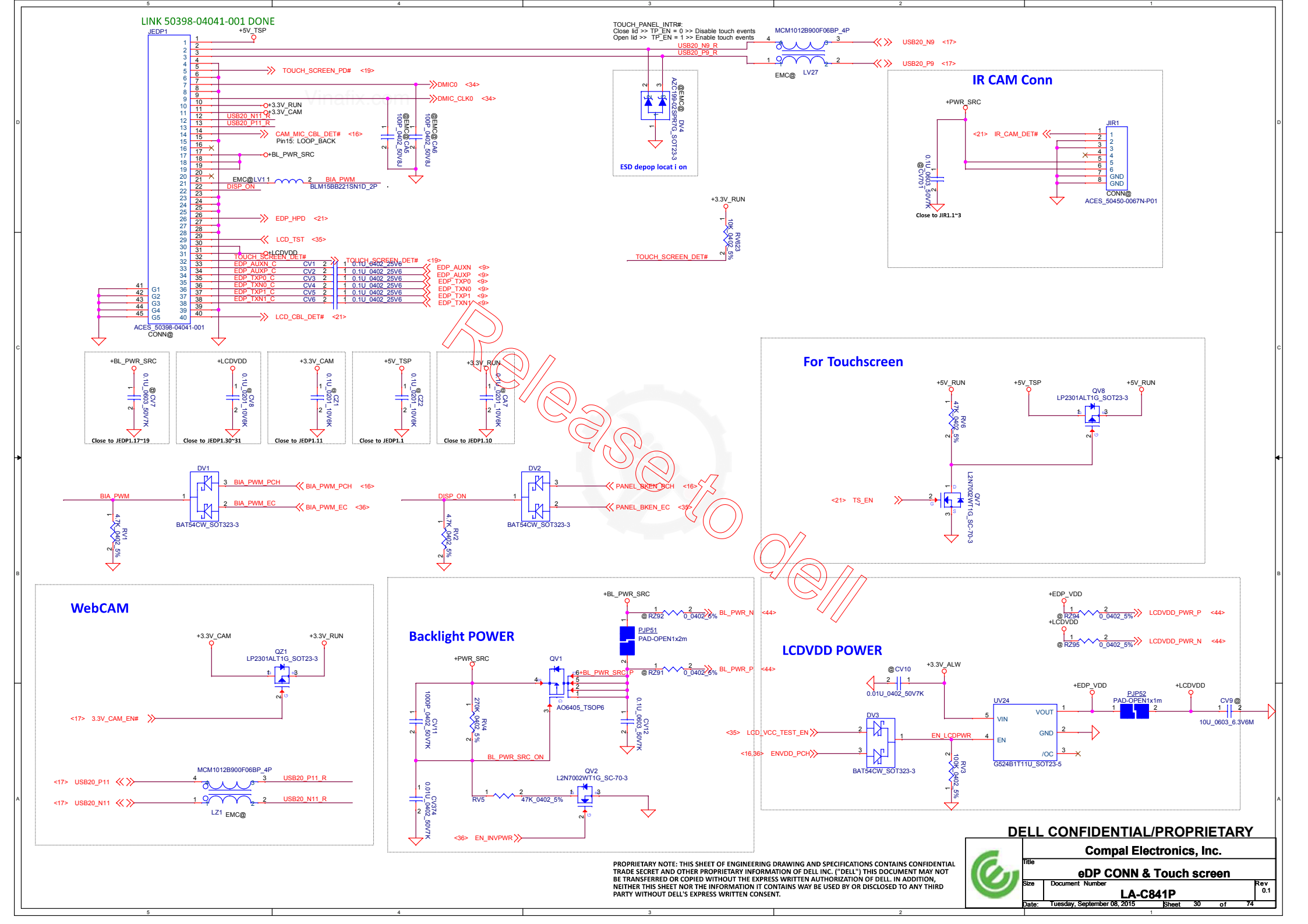


Compal Electronics, Inc.

Title: VGA / DP SW

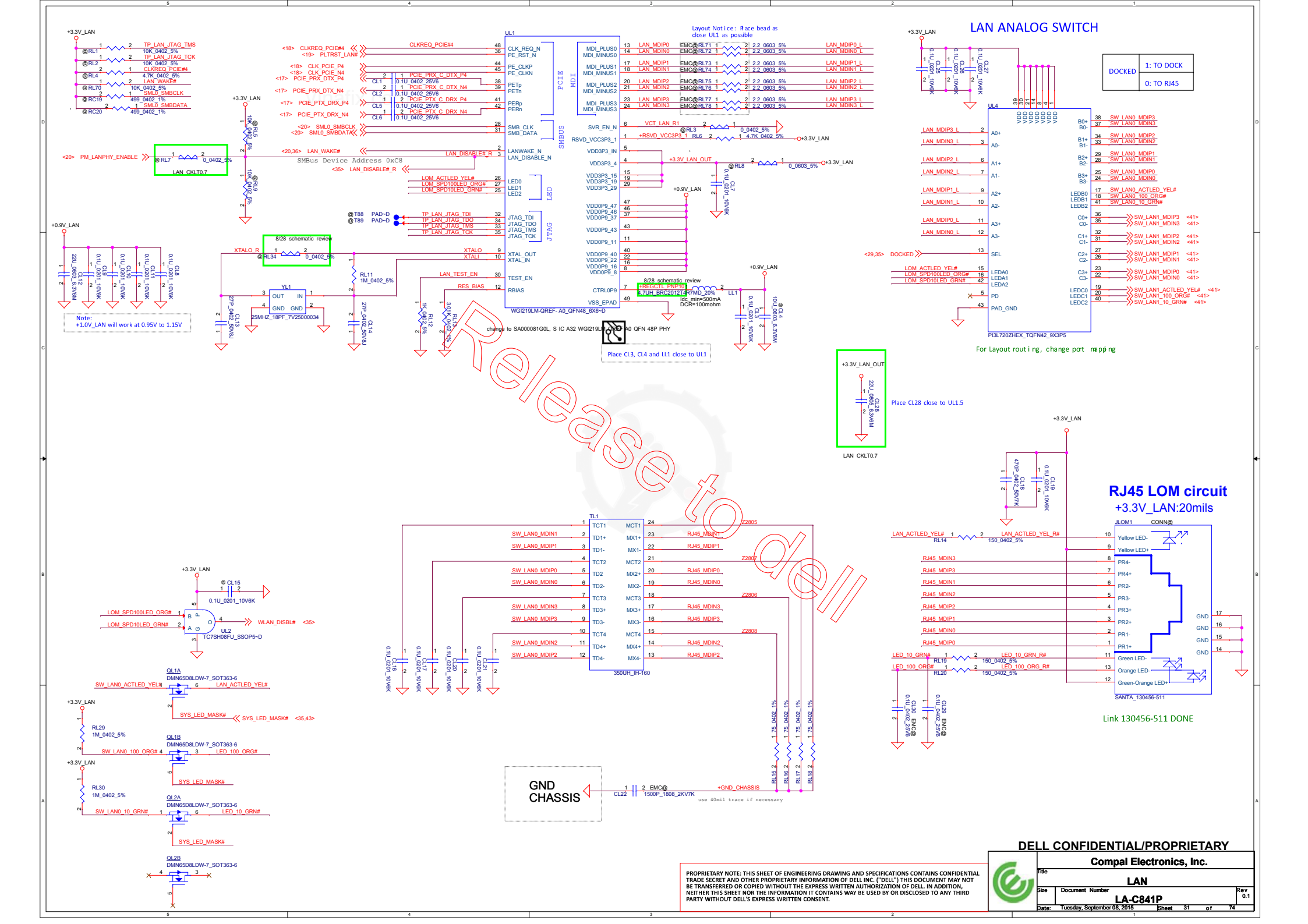
Size: | Document Number: LA-C841P | Rev: 0.1

Date: Tuesday, September 08, 2015 | Sheet 29 of 74

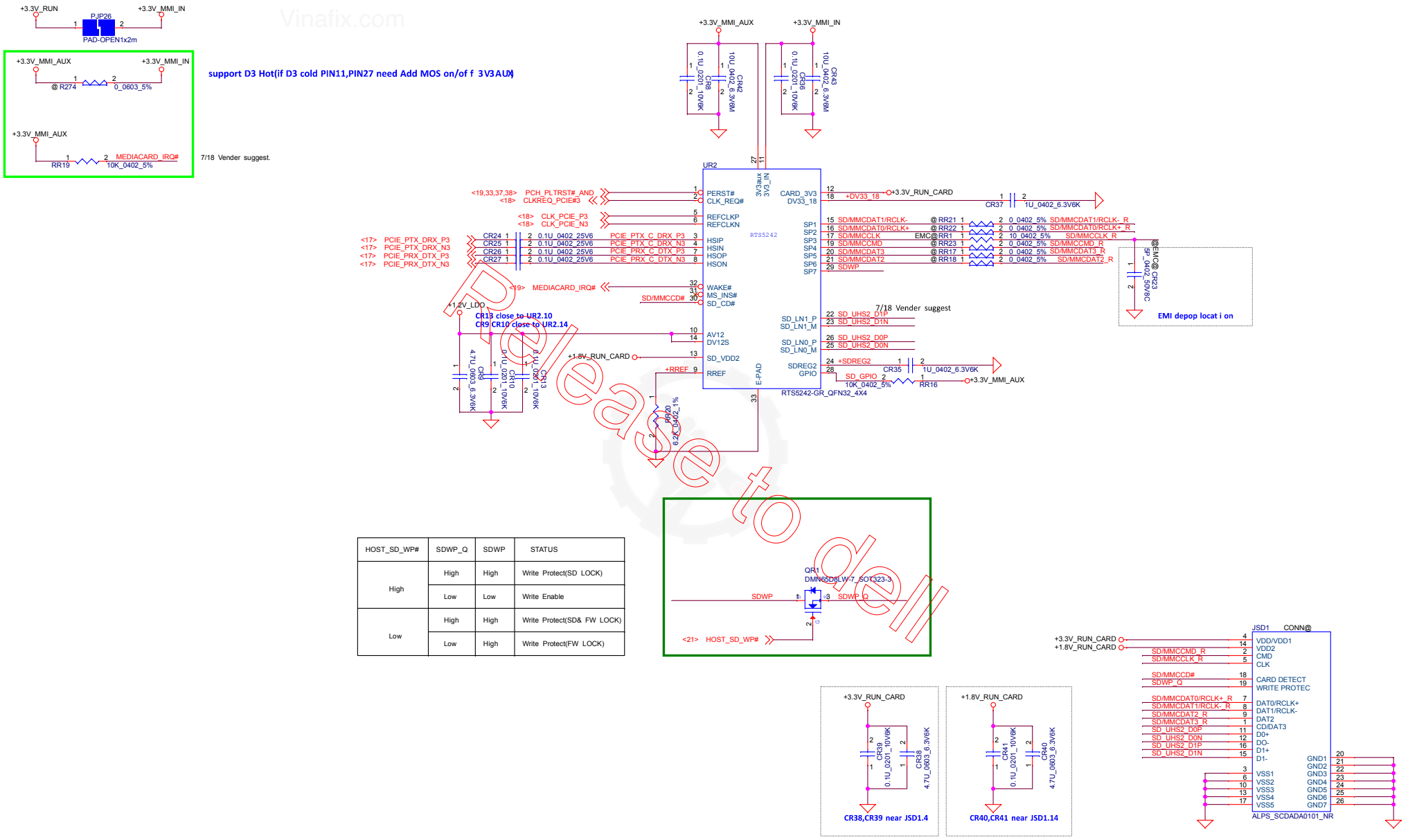


DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	eDP CONN & Touch screen
Size	Document Number: LA-C841P
Rev	0.1
Date:	Tuesday, September 08, 2015
Sheet	30 of 74



PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.



HOST_SD_WP#	SDWP_Q	SDWP	STATUS
High	High	High	Write Protect(SD LOCK)
	Low	Low	Write Enable
Low	High	High	Write Protect(SD& FW LOCK)
	Low	High	Write Protect(FW LOCK)

DELL CONFIDENTIAL/PROPRIETARY

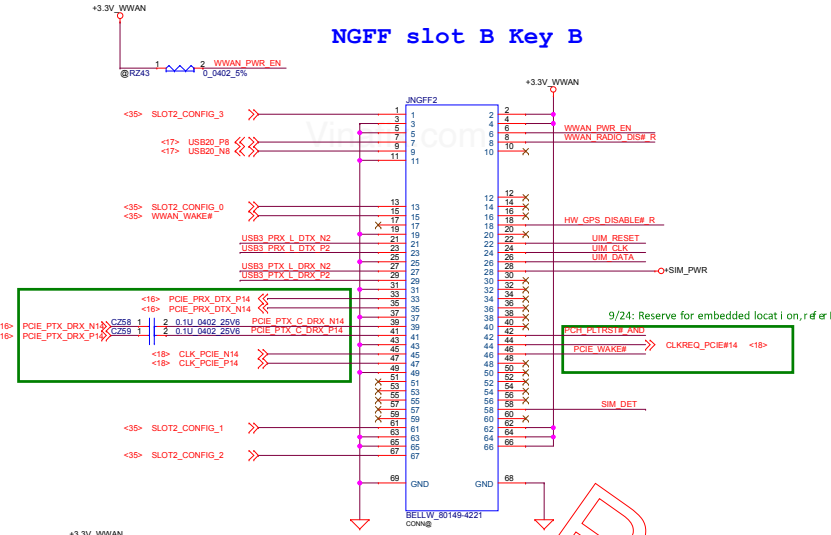
Compal Electronics, Inc.

Title: Card Reader

Size | Document Number: LA-C841P | Rev: 0.1

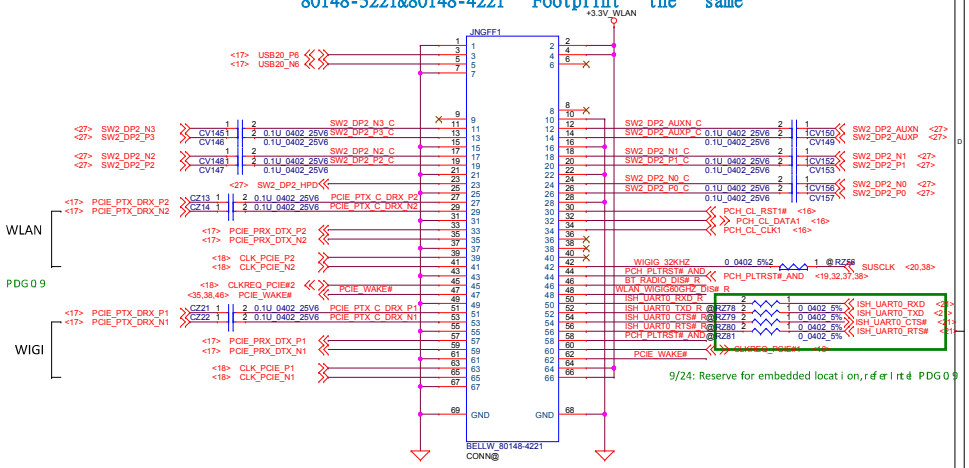
Date: Tuesday, September 08, 2015 | Sheet 32 of 74

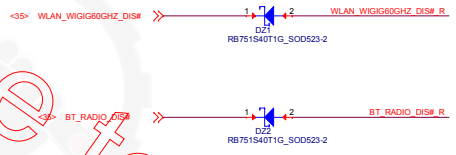
NGFF slot B Key B

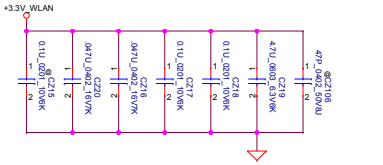


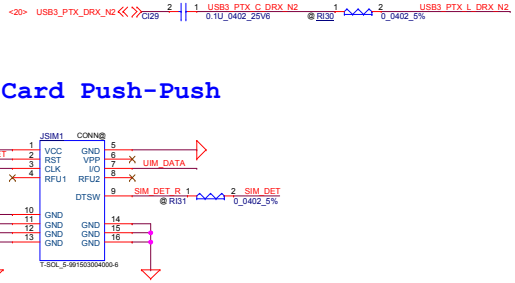
NGFF slot A Key A

80148-3221&80148-4221 Footprint the same





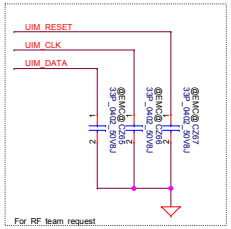




Power Rating TBD

PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V				

SIM Card Push-Push



Compal Electronics, Inc.

Title: NGFF Card

Size: | Document Number: LA-C841P | Rev: 0.1

Date: Tuesday, September 08, 2015 | Sheet 33 of 74

1W x 1ch, 4ohm (Transducer spec is 8Ohm/0.5Watt per unit, there are two transducer units in one speaker box.)

Internal Speakers Header

40 mils trace keep 20 mil spacing

CONN@ JSPK1

ACES_50279-0040N-001

Link 50279-0040N-001 DONE

Close to UA1

Close to UA1 pin6

UA1 — ALC3235-CG_MQFN48_6X6

BCLK: Audio serial data bus bit clock input/output
LRCK: Audio serial data bus word clock input/output

Place RA9 close to codec

Place RA32 close to codec

Place CA29 close to Codec

Verb table configures as 1JD mode with internal 47K pull high to save external rBOM.

Place closely to Pin 13.

Add for solve pop noise and detect issue

Place closely to Pin 14 for DOCK only

Power sequence +5V_RUN_AUDIO(501us) > +3.3V_RUN_AUDIO(1204 us) > +1.5V_RUN

Reserve for support D3 cold

Max 2.5A

500mA

EM5209VF_SON14_2X3

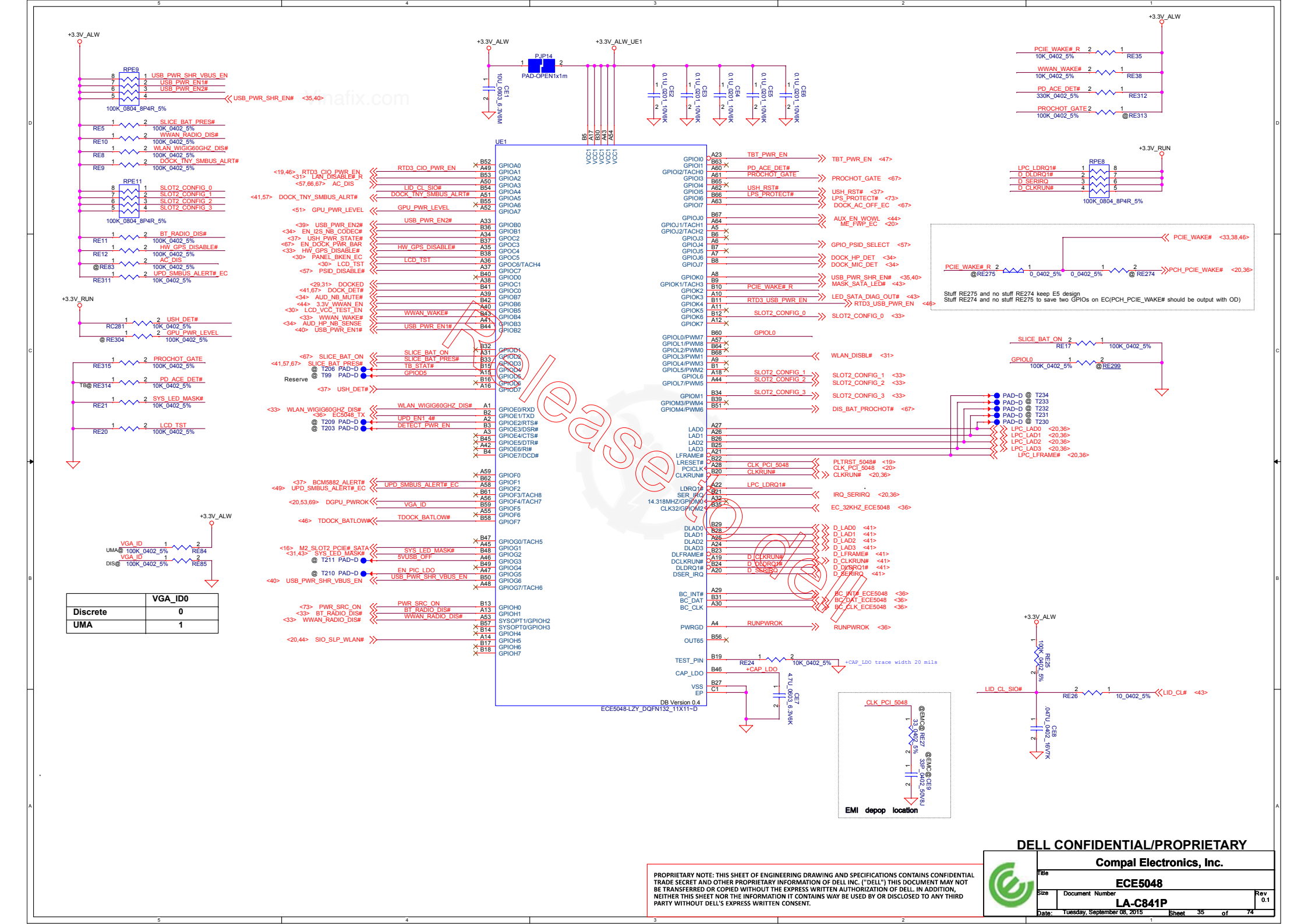
Realtek feedback
Prevent the Noise from Combo Jack while system entry into S3 / S4 /S5

HP-Out-Right
HP-Out-Left
Nokia-MIC
iPhone-MIC
Global Headset
Universal Jack

Normal
Open

SINGA_2SJ3095-059111F

Compal Electronics, Inc.	
Title	Codec ALC3235
Size	Document Number: LA-C841P
Rev	0.1
Date: Tuesday, September 08, 2015	Sheet 34 of 74



	VGA_ID0
Discrete	0
UMA	1

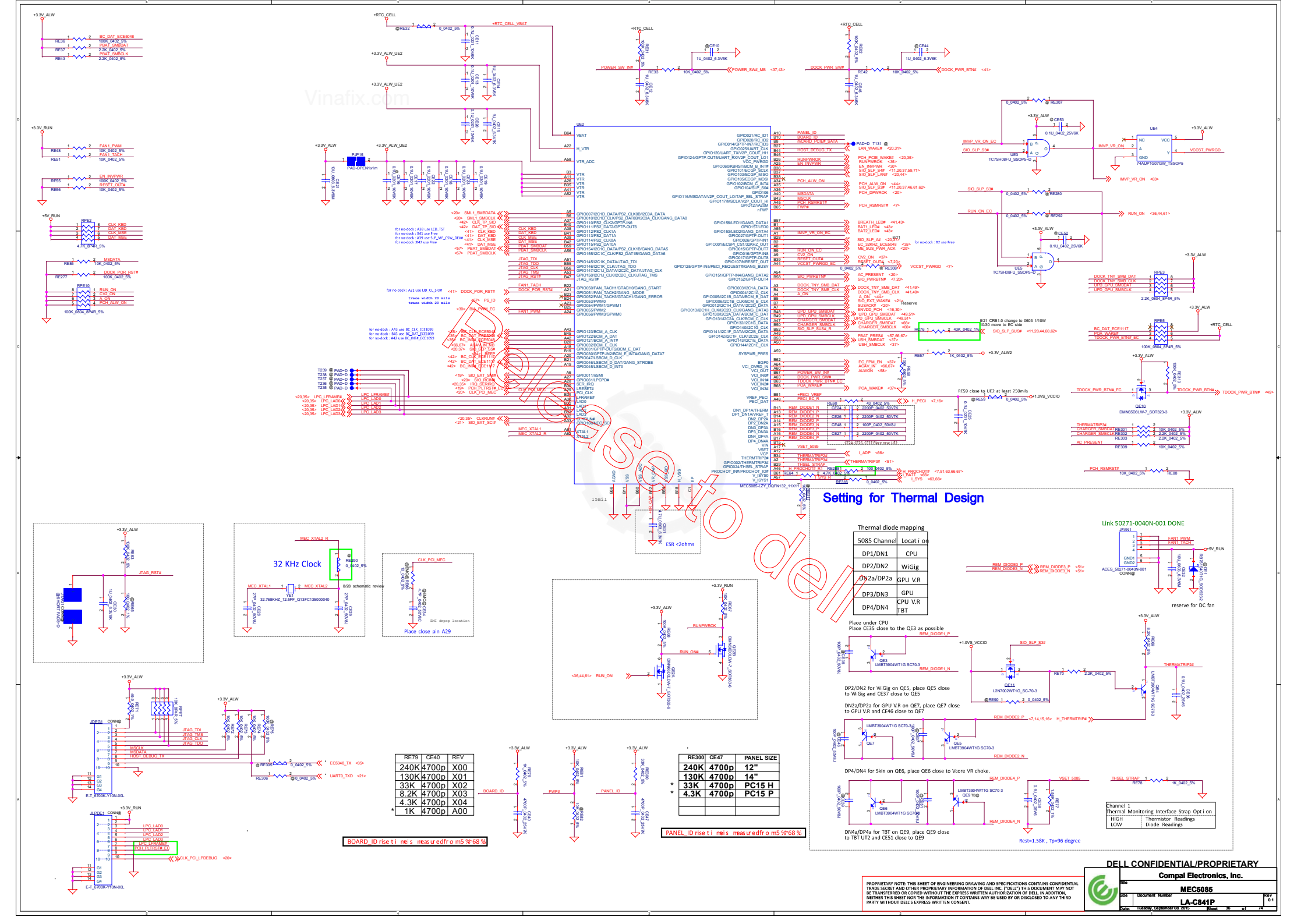
DELL CONFIDENTIAL/PROPRIETARY

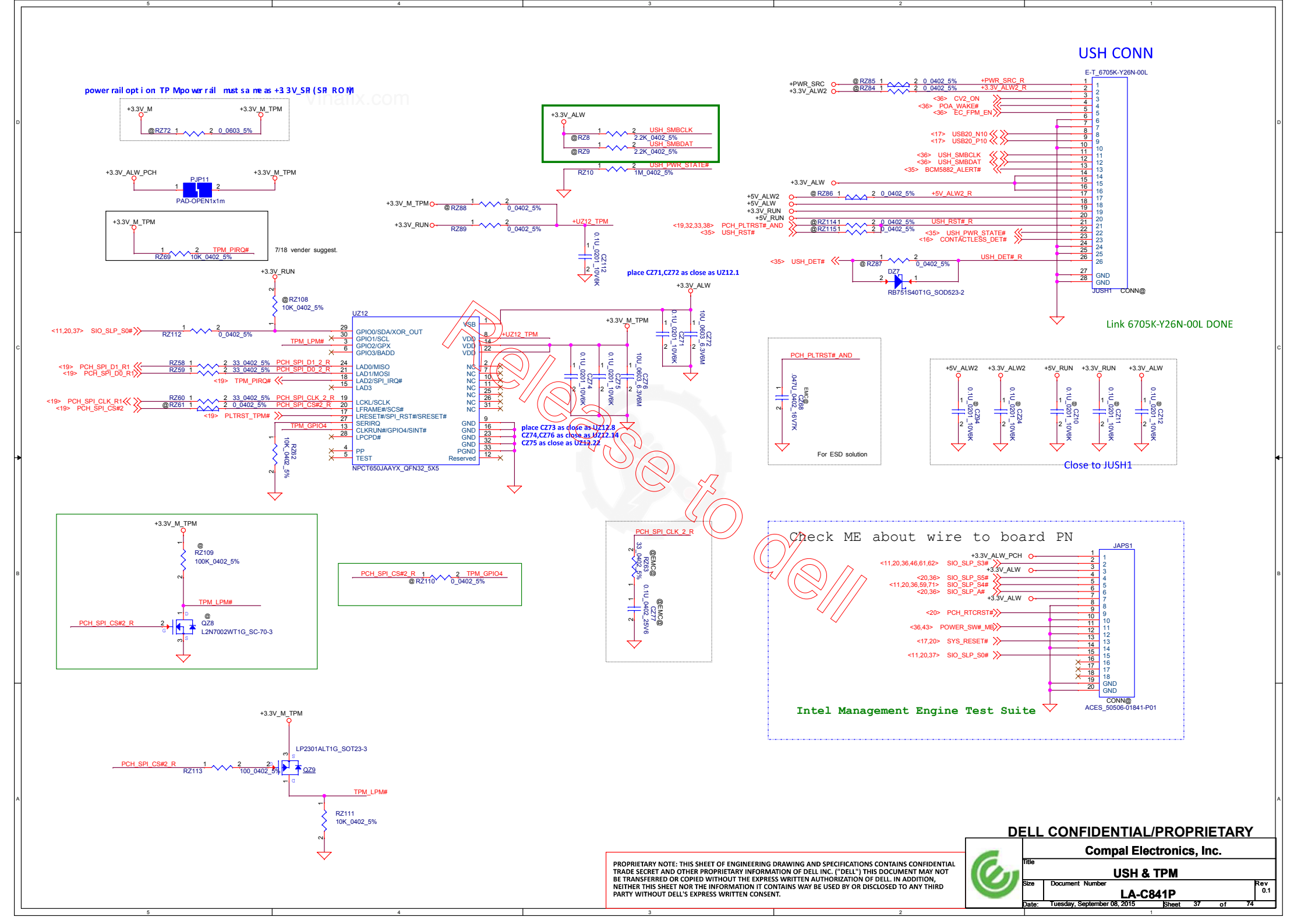
Compal Electronics, Inc.

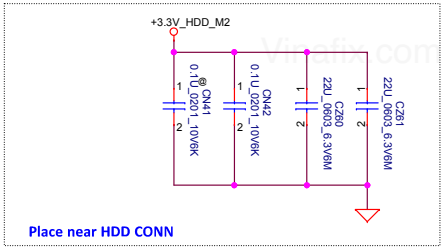
Title: ECE5048

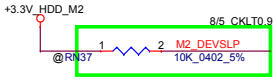
Size: Document Number: LA-C841P Rev: 0.1

Date: Tuesday, September 08, 2015 Sheet 35 of 74


Setting for Thermal Design
Thermal diode mapping
5085 Channel
Locat i on
DP1/DN1
CPU
DP2/DN2
WiGig
DN2a/DP2a
GPU V.R
DP3/DN3
GPU
DP4/DN4
CPU V.R
TBT
Place under CPU
Place CE35 close to the QE3 as possible
DP2/DN2 for WiGig on QE5, place QE5 close to WiGig and CE37 close to QE5
DN2a/DP2a for GPU V.R on QE7, place QE7 close to GPU V.R and CE46 close to QE7
DP4/DN4 for Skin on QE6, place QE6 close to Vcore VR choke.
DN4a/DP4a for TBT on QE9, place QE9 close to TBT UT2 and CE51 close to QE9
Rest=1.58K , Tp=96 degree
Channel 1
Thermal Monitoring Interface Strap Opt i on
HIGH
Thermistor Readings
LOW
Diode Readings
Link 50271-0040N-001 DONE
reserve for DC fan
32 KHz Clock
ESR <2ohms
Place close pin A29
BOARD_ID rise t i me is measured fro m 5 %~68 %
PANEL_ID rise t i me is measured fro m 5 %~68 %
RE79 CE40 REV
240K 4700p X00
130K 4700p X01
33K 4700p X02
8.2K 4700p X03
4.3K 4700p X04
* 1K 4700p A00
RE300 CE47 PANEL SIZE
240K 4700p 12"
130K 4700p 14"
* 33K 4700p PC15 H
* 4.3K 4700p PC15 P
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
MEC5085
LA-C841P
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL"). THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.
Tuesday, September 08, 2015
Sheet 38 of 74

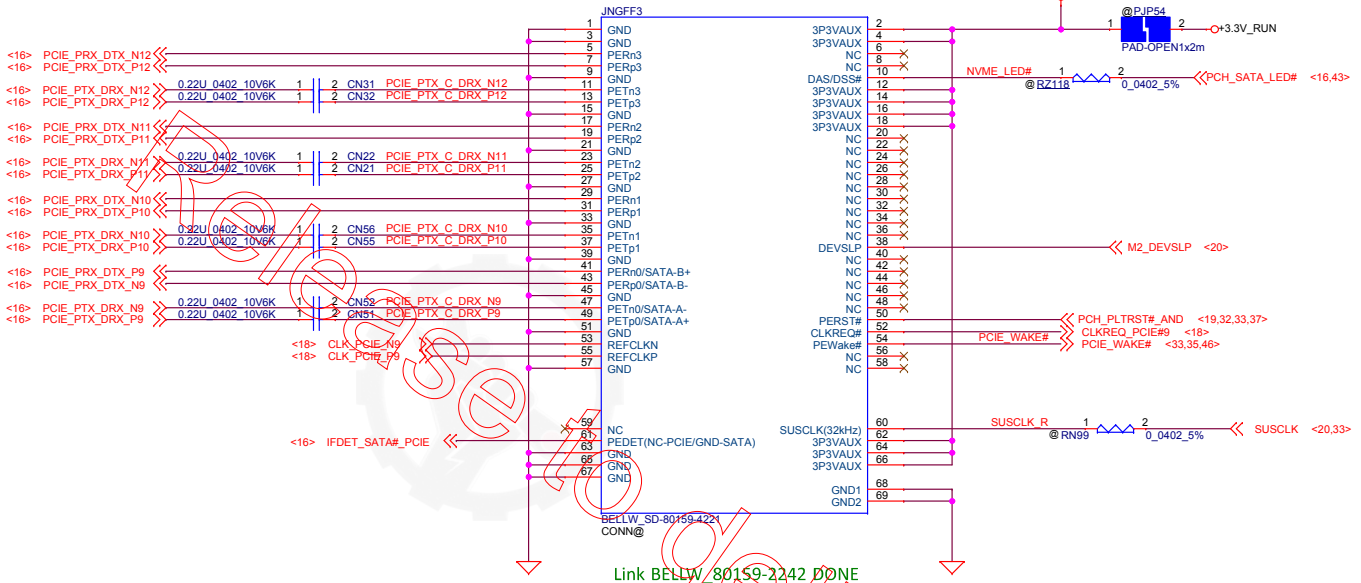

USH CONN
power rail option TP Mpower rail must same as +3.3V_SPI (SPI ROM)
+3.3V_M
+3.3V_M_TPM
@RZ72 1 2 0 0603 5%
+3.3V_ALW_PCH
PJP11
PAD-OPEN1x1m
+3.3V_M_TPM
RZ69 1 2 TPM_PIRQ# 10K_0402_5%
7/18 vender suggest.
+3.3V_ALW
@RZ8 1 2 USH_SMBCLK 2.2K_0402_5%
@RZ9 1 2 USH_SMBDAT 2.2K_0402_5%
RZ10 1 2 USH_PWR_STATE# 1M_0402_5%
+3.3V_M_TPM
@RZ88 1 2 0_0402_5%
+3.3V_RUN
RZ89 1 2 0_0402_5%
+UZ12_TPM
CZ112 0.1U_0201_10V6K
place CZ71,CZ72 as close as UZ12.1
+3.3V_RUN
@RZ108 10K_0402_5%
<11,20,37> SIO_SLP_S0#
RZ112 1 2 0_0402_5%
UZ12
GPIO0/SDA/XOR_OUT
GPIO1/SCL
GPIO2/GPX
GPIO3/BADD
LAD0/MISO
LAD1/MOSI
LAD2/SPI_IRQ#
LAD3
LCKL/SCLK
LFRAME#/SCS#
LRESET#/SPI_RST#/SRESET#
SERIRQ
CLKRUN#/GPIO4/SINT#
LPCPD#
PP
TEST
VSB
VDD
GND
PGND
Reserved
NC
NPCT650JAAYX_QFN32_5X5
TPM_LPM#
<19> PCH_SPI_D1_R1
<19> PCH_SPI_D0_R1
RZ58 1 2 33_0402_5% PCH_SPI_D1_2_R
RZ59 1 2 33_0402_5% PCH_SPI_D0_2_R
<19> TPM_PIRQ#
<19> PCH_SPI_CLK_R1
<19> PCH_SPI_CS#2
RZ60 1 2 33_0402_5% PCH_SPI_CLK_2_R
@RZ61 1 2 0_0402_5% PCH_SPI_CS#2_R
<19> PLTRST_TPM#
TPM_GPIO4
RZ62 10K_0402_5%
+3.3V_ALW
+3.3V_M_TPM
+UZ12_TPM
CZ74 0.1U_0201_10V6K
CZ75 0.1U_0201_10V6K
CZ76 10U_0603_6.3V6M
CZ71 0.1U_0201_10V6K
CZ72 10U_0603_6.3V6M
place CZ73 as close as UZ12.8
CZ74,CZ76 as close as UZ12.14
CZ75 as close as UZ12.22
+3.3V_M_TPM
@ RZ109 100K_0402_5%
TPM_LPM#
PCH_SPI_CS#2_R
@ QZ8 L2N7002WT1G_SC-70-3
PCH_SPI_CS#2_R 1 2 TPM_GPIO4
@RZ110 0_0402_5%
PCH_SPI_CLK_2_R
RZ23 33_0402_5%
@EMC@
CZ77 0.1U_0402_25V6
+3.3V_M_TPM
LP2301ALT1G_SOT23-3
PCH_SPI_CS#2_R
RZ113 1 2 100_0402_5%
QZ9
TPM_LPM#
RZ111 10K_0402_5%
+PWR_SRC
+3.3V_ALW2
@RZ85 1 2 0_0402_5% +PWR_SRC_R
@RZ84 1 2 0_0402_5% +3.3V_ALW2_R
<36> CV2_ON
<36> PCA_WAKE#
<36> EC_FPM_EN
<17> USB20_N10
<17> USB20_P10
<36> USH_SMBCLK
<36> USH_SMBDAT
<35> BCM5882_ALERT#
+3.3V_ALW
@RZ86 1 2 0_0402_5% +5V_ALW2_R
+5V_ALW2
+5V_ALW
+3.3V_RUN
+5V_RUN
<19,32,33,38> PCH_PLTRST#_AND
<35> USH_RST#
@RZ1141 2 0_0402_5% USH_RST#_R
@RZ1151 2 0_0402_5%
<35> USH_PWR_STATE#
<16> CONTACTLESS_DET#
<35> USH_DET#
@RZ87 1 2 0_0402_5% USH_DET#_R
DZ7
RB751S40T1G_SOD523-2
E-T_6705K-Y26N-00L
GND
JUSH1 CONN@
Link 6705K-Y26N-00L DONE
PCH_PLTRST#_AND
CZ68 .047U_0402_16V7K
EMC@
For ESD solution
+5V_ALW2
+3.3V_ALW2
+5V_RUN
+3.3V_RUN
+3.3V_ALW
CZ234 0.1U_0201_10V6K @
CZ224 0.1U_0201_10V6K @
CZ210 0.1U_0201_10V6K @
CZ211 0.1U_0201_10V6K @
CZ212 0.1U_0201_10V6K @
Close to JUSH1
Check ME about wire to board PN
+3.3V_ALW_PCH
<11,20,36,46,61,62> SIO_SLP_S3#
+3.3V_ALW
<20,36> SIO_SLP_S5#
<11,20,36,59,71> SIO_SLP_S4#
<20,36> SIO_SLP_A#
+3.3V_ALW
<20> PCH_RTCRST#
<36,43> POWER_SW#_ME
<17,20> SYS_RESET#
<11,20,37> SIO_SLP_S0#
JAPS1
GND
CONN@
ACES_50506-01841-P01
Intel Management Engine Test Suite
Release to dell
DELL CONFIDENTIAL/PROPRIETARY
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.
Compal Electronics, Inc.
Title
USH & TPM
Size
Document Number
LA-C841P
Rev
0.1
Date: Tuesday, September 08, 2015
Sheet 37 of 74





2280 SSD

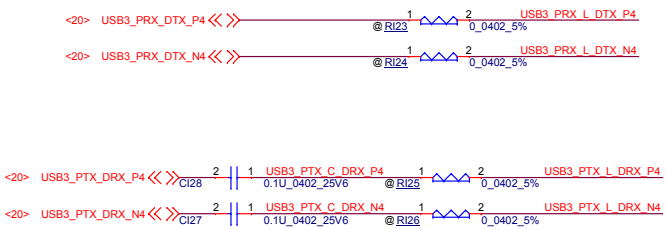
NGFF slot C Key M

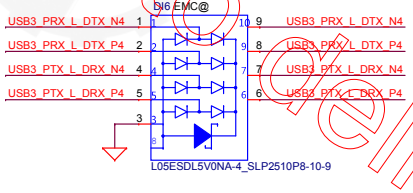


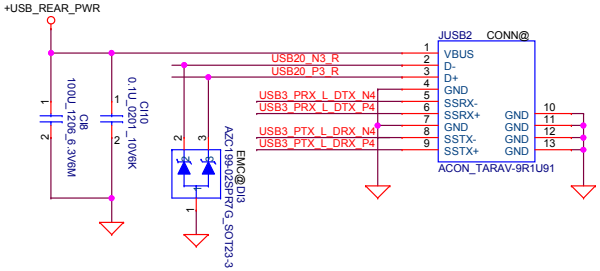
DELL CONFIDENTIAL/PROPRIETARY

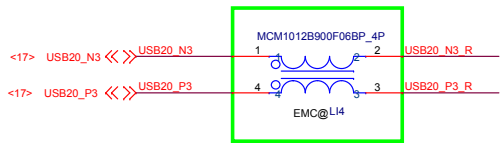
Compal Electronics, Inc.

Title	HDD CONN	
Size	Document Number LA-C841P	Rev 0.1
Date: Tuesday, September 08, 2015	Sheet 38 of 74	

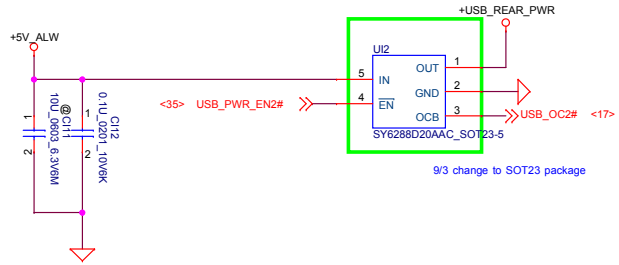








8/19 for layout routing change



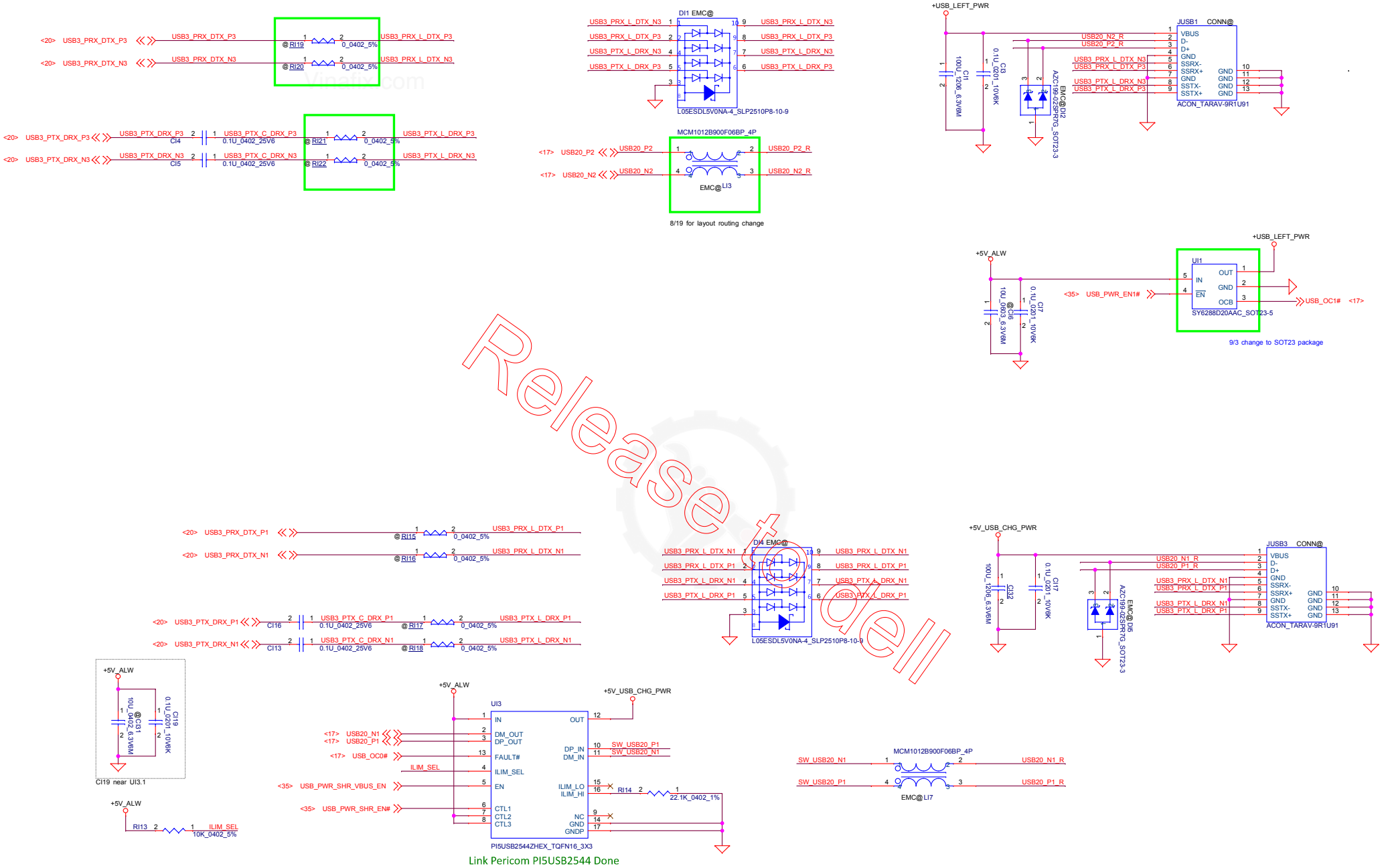
9/3 change to SOT23 package

Compal Electronics, Inc.

Title: USB SW

Size | Document Number: LA-C841P | Rev: 0.1

Date: Tuesday, September 08, 2015 | Sheet 39 of 74

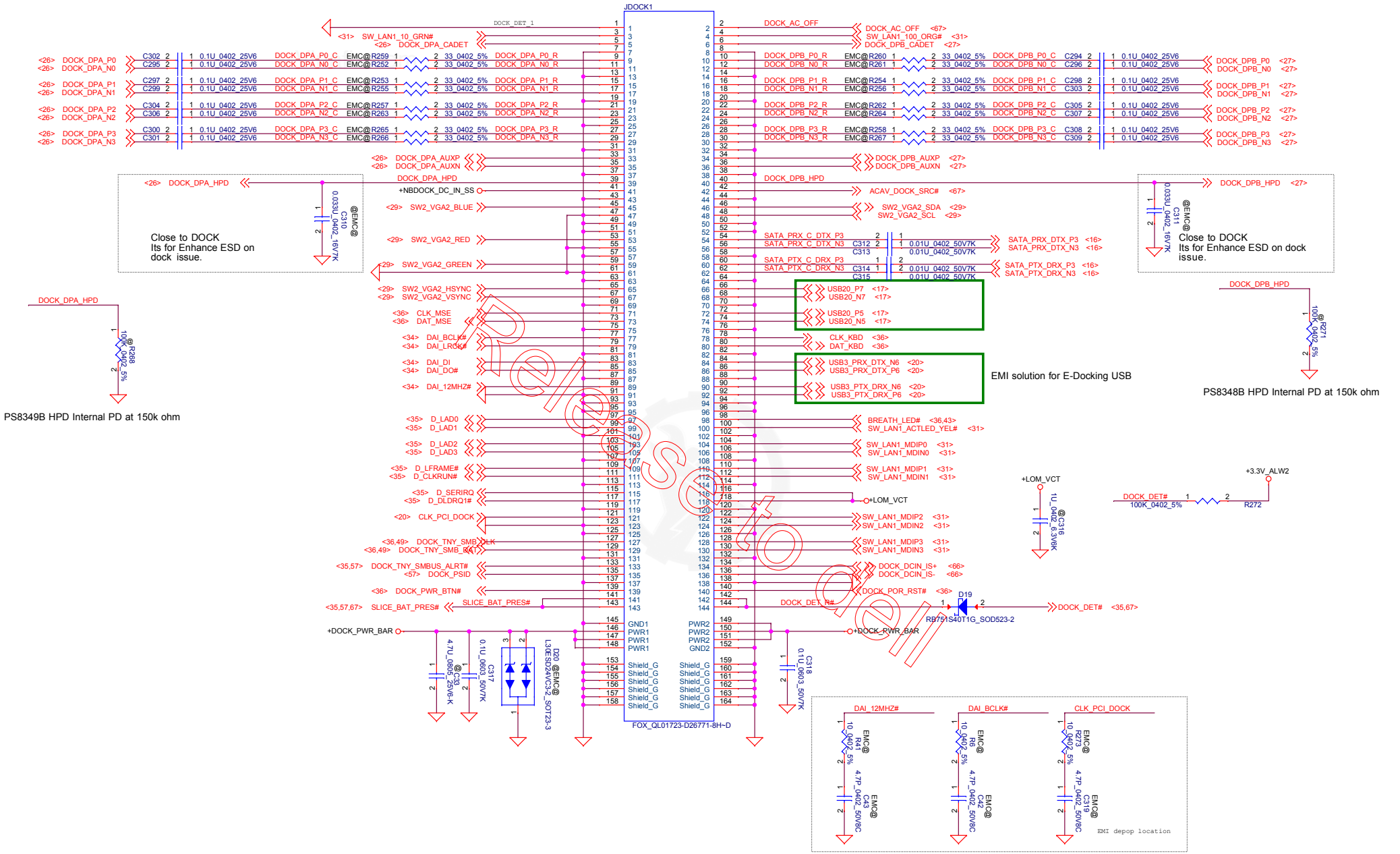


Compal Electronics, Inc.

Title: USB3.0

Size | Document Number: LA-C841P | Rev: 0.1

Date: Tuesday, September 08, 2015 | Sheet 40 of 74

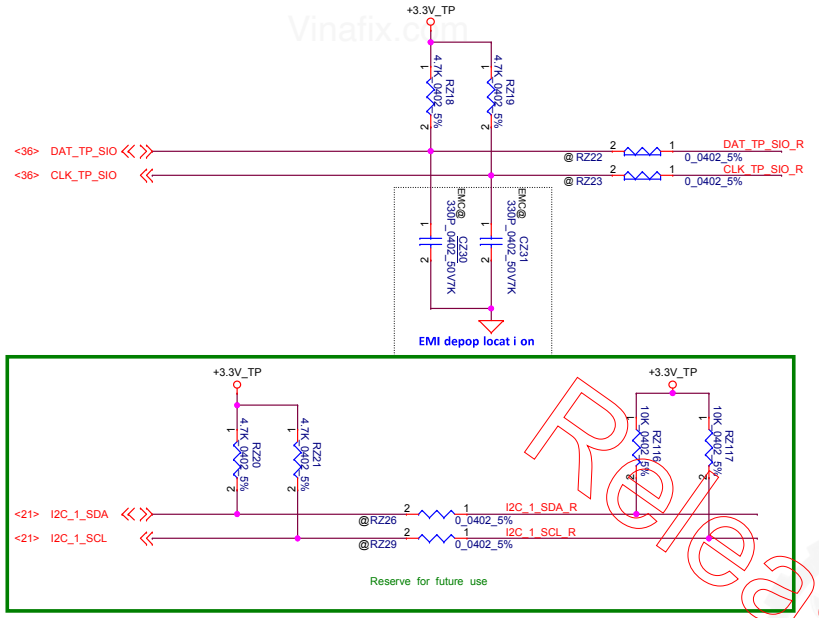


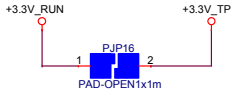
DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

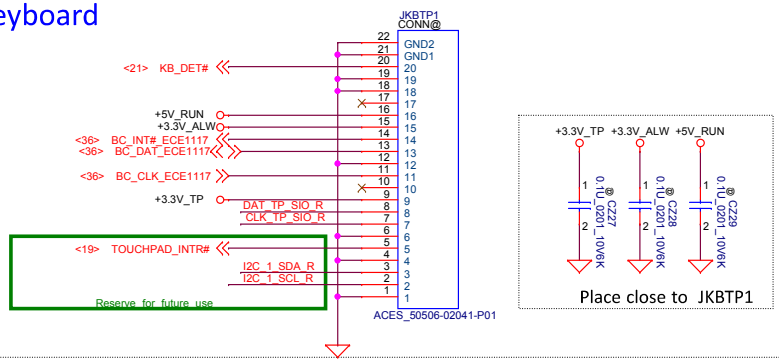
Compal Electronics, Inc.	
Title	E-Dock
Size	Document Number: LA-C841P
Rev	0.1
Date:	Tuesday, September 08, 2015
Sheet	41 of 74

Touch Pad





Keyboard



Link 50506-02041-P0 DONE

@eDP Cable W CAM

Part Number	Description
DC02C007600	H-CONN SET 13D MB-EDP-CAMERA

@eDP TS Cable W CAM

Part Number	Description
DC02C007C00	H-CONN SET 13D MB-EDP-CAMERA-TS

@eDP Cable W/O CAM

Part Number	Description
DC02C007D00	H-CONN SET 13D MB-EDP

@SATA SPINDLE Cable

Part Number	Description
DC02C007F00	H-CONN SET 13D MB-SPINDLE HDD

@SATA Cable

Part Number	Description
DC02C007400	H-CONN SET 13D MB-MSATA HDD

@DC-IN Cable

Part Number	Description
DC30100Q100	CONN SET 13F DCJACK-MB 2DW1003-041110F

@BATT Cable

Part Number	Description
DC02001X800	H-CONN SET 13D MB-BATT CABLE

@LED FFC

Part Number	Description
NBX0001JG00	FFC 10P F P0.5 PAD0.3 172MM MB-LED/B 13D

@FP FFC

Part Number	Description
NBX0001JK00	FFC 8P F P0.5 PAD.3 123MM MB-FP VALIDITY

@TP FFC

Part Number	Description
NBX0001JI00	FFC 16P F P0.5 PAD=0.3 119MM MB-TP 13D

@USH Board FFC

Part Number	Description
NBX0001JJ00	FFC 26P G P0.5 PAD.3 88MM MB-USH/B 13D

@RTC BATT

Part Number	Description
GC02001DS00	BATT CR2032 3V 225MAH PA 5 W/C 30MM

@FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

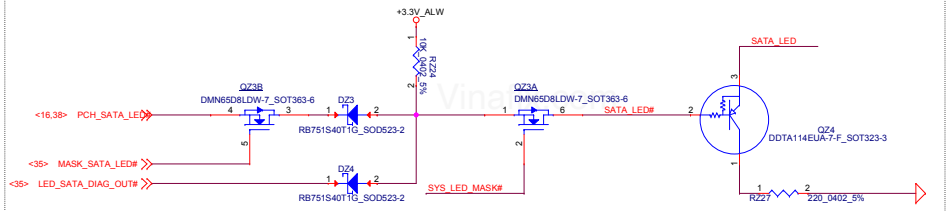
@Speak

Part Number	Description
PK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

RSMRST circuit

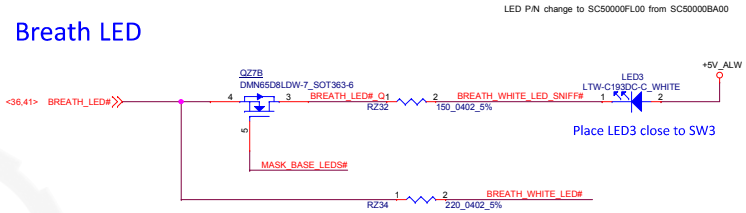
Move to CPU page

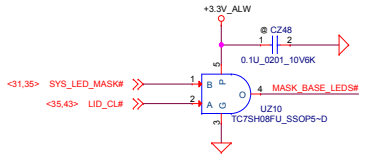
HDD LED solution for White LED



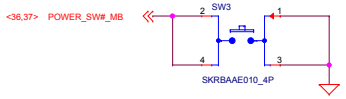
Battery LED

Breath LED

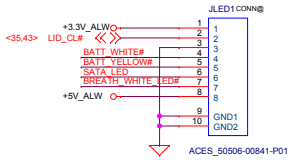




POWER & INSTANT ON SWITCH



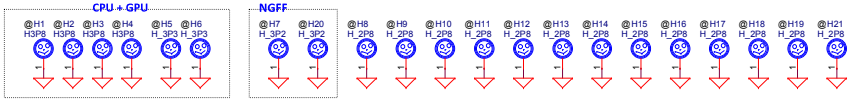
LED board CONN



Fiducial Mark

@FD1 FIDUCIAL MARK~D
@FD2 FIDUCIAL MARK~D
@FD3 FIDUCIAL MARK~D
@FD4 FIDUCIAL MARK~D

LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



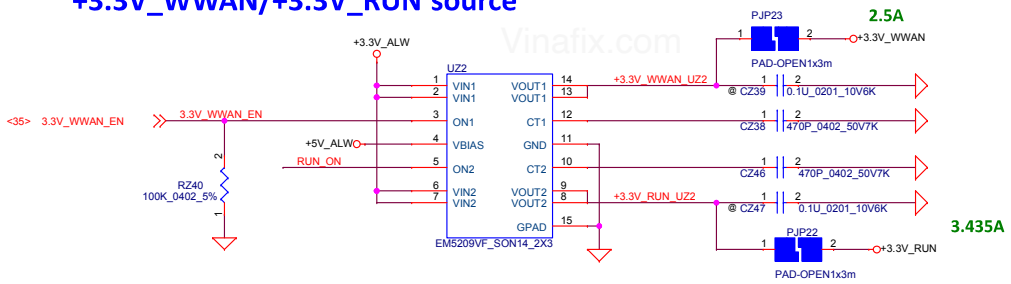
Compal Electronics, Inc.

Title: PAD, LED

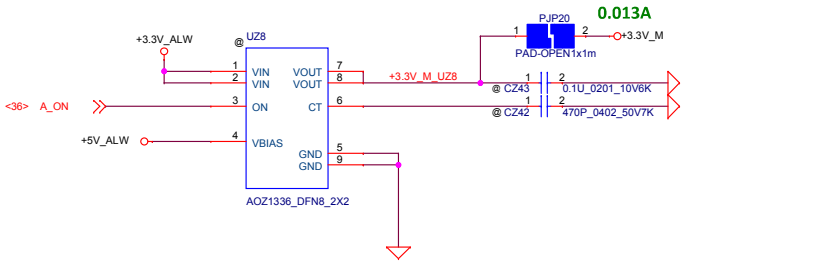
Size: | Document Number: LA-C841P | Rev: 0.1

Date: Tuesday, September 08, 2015 | Sheet 43 of 74

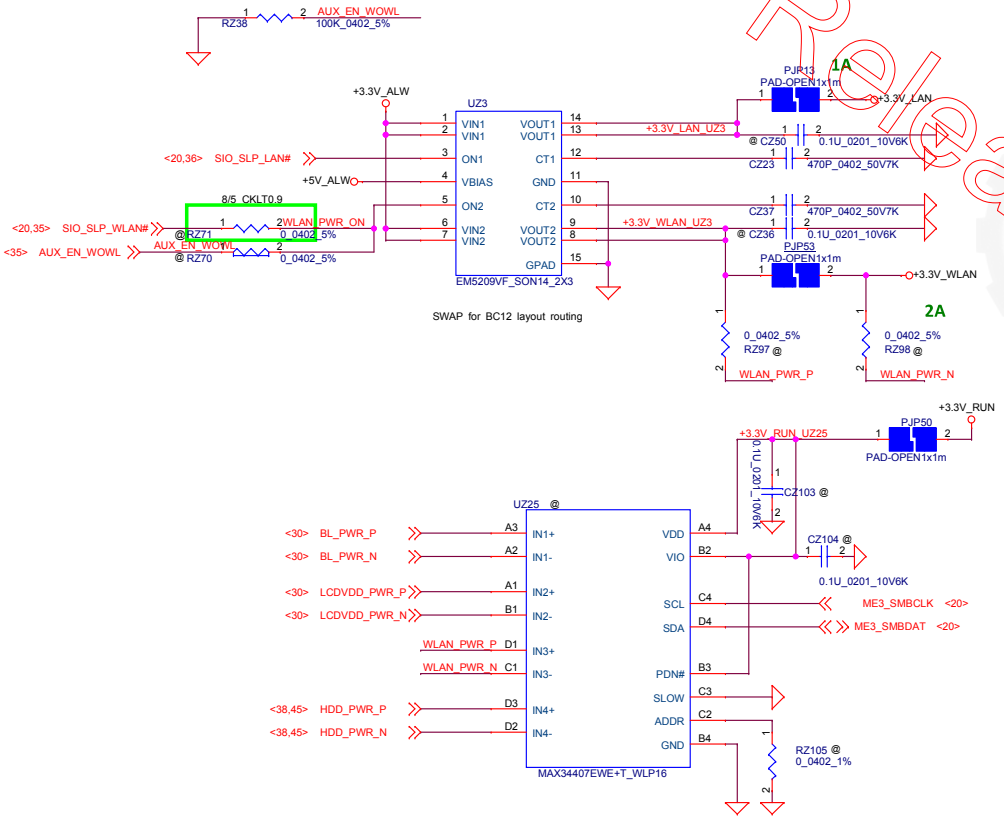
+3.3V_WWAN/+3.3V_RUN source



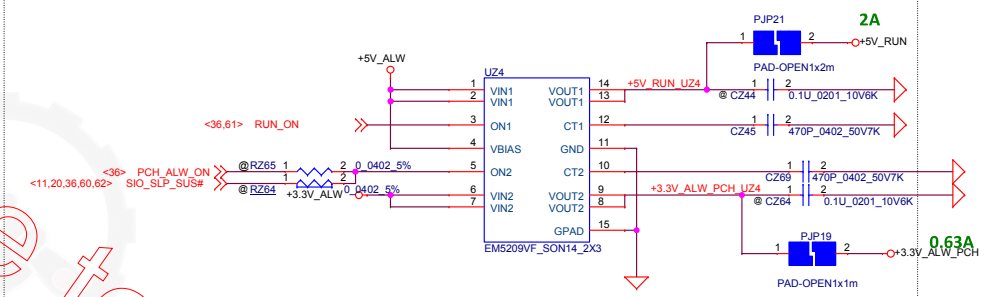
+3.3V_M source



+3.3V_WLAN/+3.3V_LAN source



+5V_RUN/+3.3V_ALW_PCH source



+3.3V_SUS source

Move to USH/B

Compal Electronics, Inc.

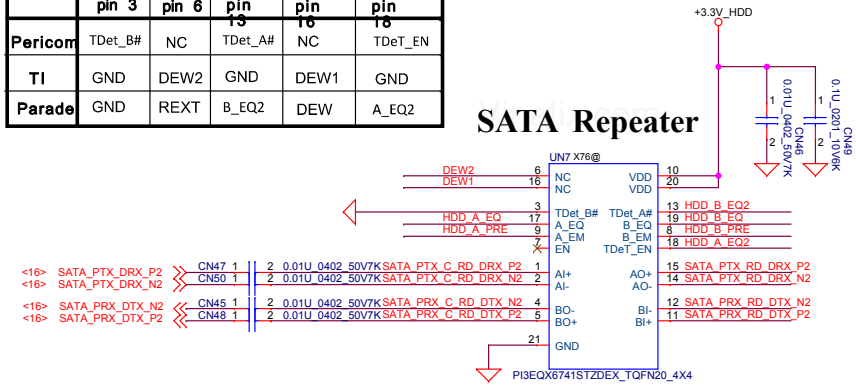
Title: Power control

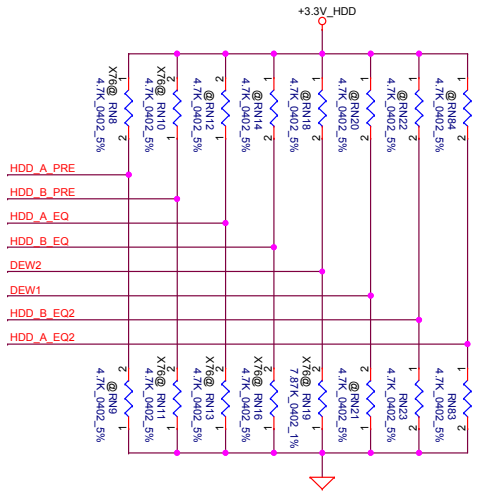
Size | Document Number: LA-C841P | Rev: 0.1

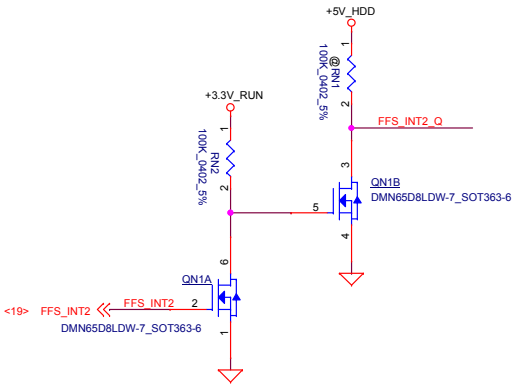
Date: Tuesday, September 08, 2015 | Sheet 44 of 74

	pin 3	pin 6	pin 13	pin 16	pin 18
Pericom	TDet_B#	NC	TDet_A#	NC	TDeT_EN
TI	GND	DEW2	GND	DEW1	GND
Parade	GND	REXT	B_EQ2	DEW	A_EQ2

SATA Repeater



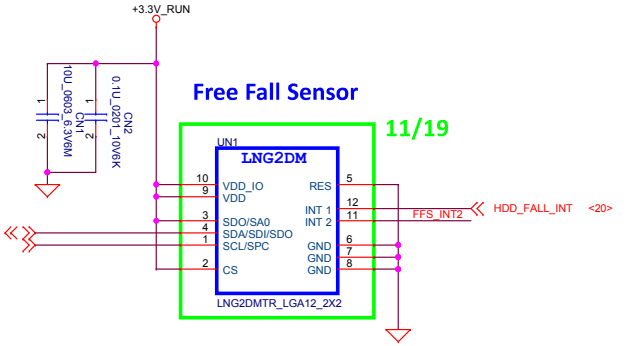


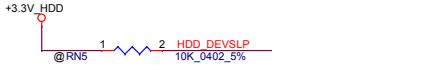


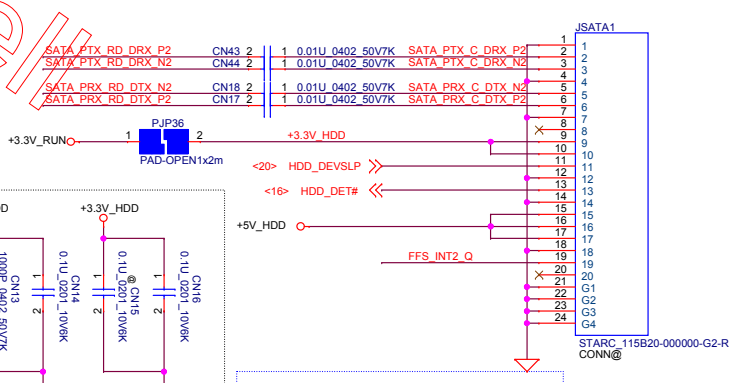
	HDD_A_EQ	HDD_B_EQ	HDD_A_EQ2	HDD_B_EQ2	DEW1	DEW2	HDD_A_PRE	HDD_B_PRE
	PIN17	PIN19	PIN18	PIN13	PIN16	PIN6	PIN9	PIN8
Pericom PI3EQX6741ST	NC	PD (RN16)	PD (RN83)	PD (RN23)	NC	NC	NC (IPU)	PD (RN11)
TI SN75LVCP601	PD (RN13)	NC	PD (RN83)	PD (RN23)	NC (IPU)	NC (IPU)	PH (RN8)	PH (RN10)
Parade PS8527C	PD (RN13)	PD (RN16)	PD (RN83)	PD (RN23)	NC (1/2 VDD)	PD (RN19)	NC (1/2 VDD)	NC (1/2 VDD)

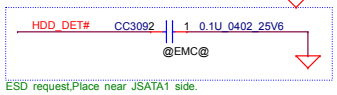
			A_EQ	B_EQ		A_EM	B_EM
Main	Pericom	0	3dB	3dB	0	0dB	0dB
		NC	6dB	6dB	NC		
		1	9dB	9dB	1	1.5dB	1.5dB
2nd	TI	0	7dB	7dB	0	0dB	0dB
		NC	0dB	0dB	NC	-4dB	-4dB
		1	14dB	14dB	1	-2dB	-2dB
3rd	Parade	EQ2 EQ1	A_EQ	B_EQ		A_EM	B_EM
		(M = VDD/2)					
		0 M	2.4dB	2.4dB			
		0 0	7.4dB	7.4dB			
		0 1	14.4dB	14.4dB	0	0dB	0dB
		M M	12.2dB	12.2dB	M	-3.5dB	-3.5dB
		M 0	9.4dB	9.4dB	1	-1.5dB	-1.5dB
		M 1	13.3dB	13.3dB			
		1 M	6.2dB	6.2dB			
		1 0	11.2dB	11.2dB			
		1 1	5dB	5dB			

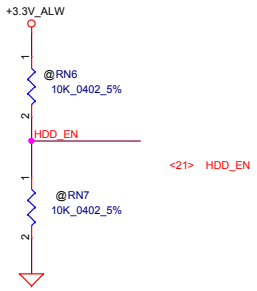
* red color is current setting



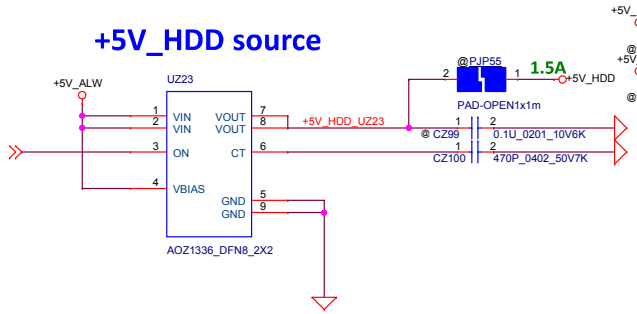








+5V_HDD source



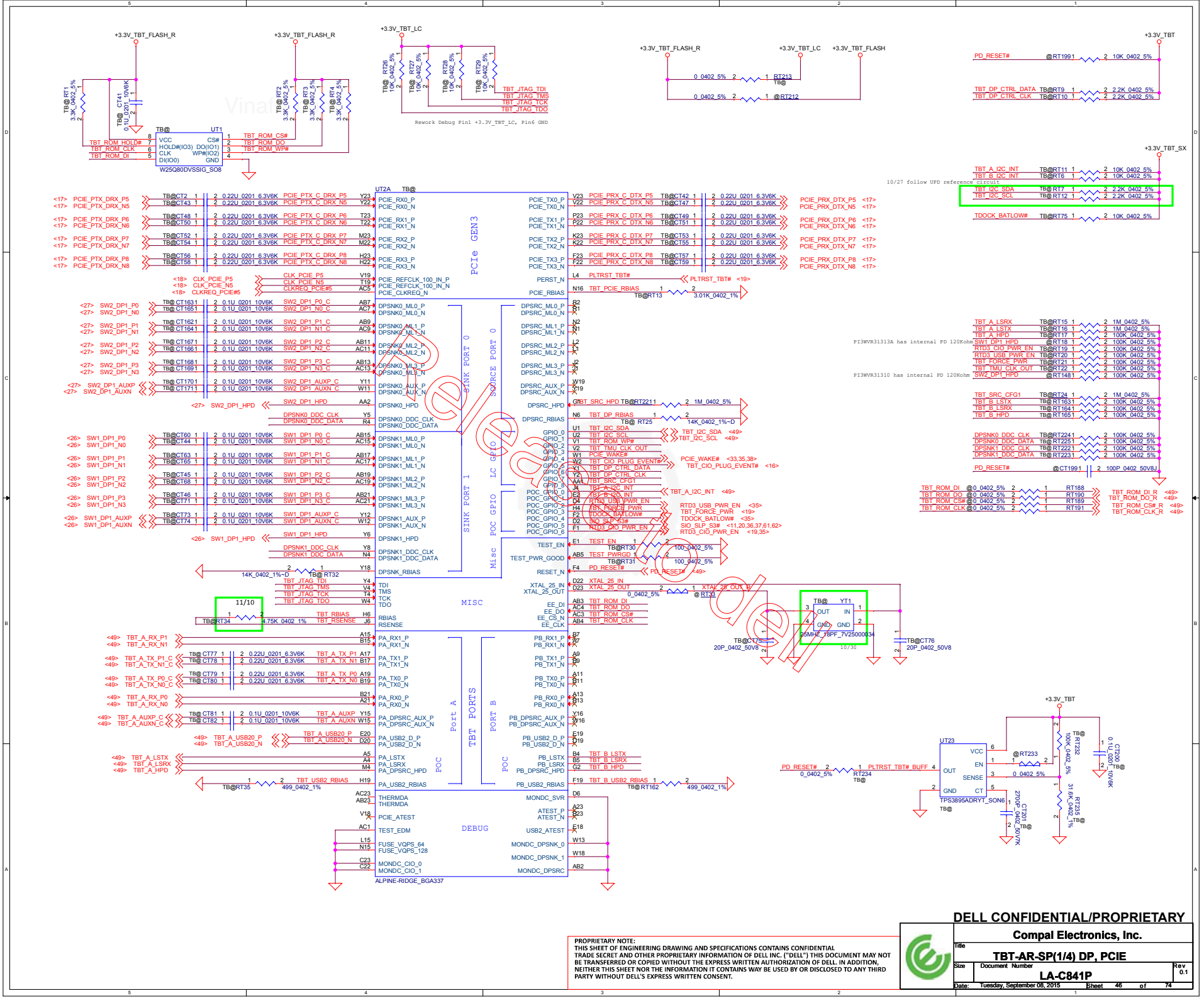
DELL CONFIDENTIAL/PROPRIETARY

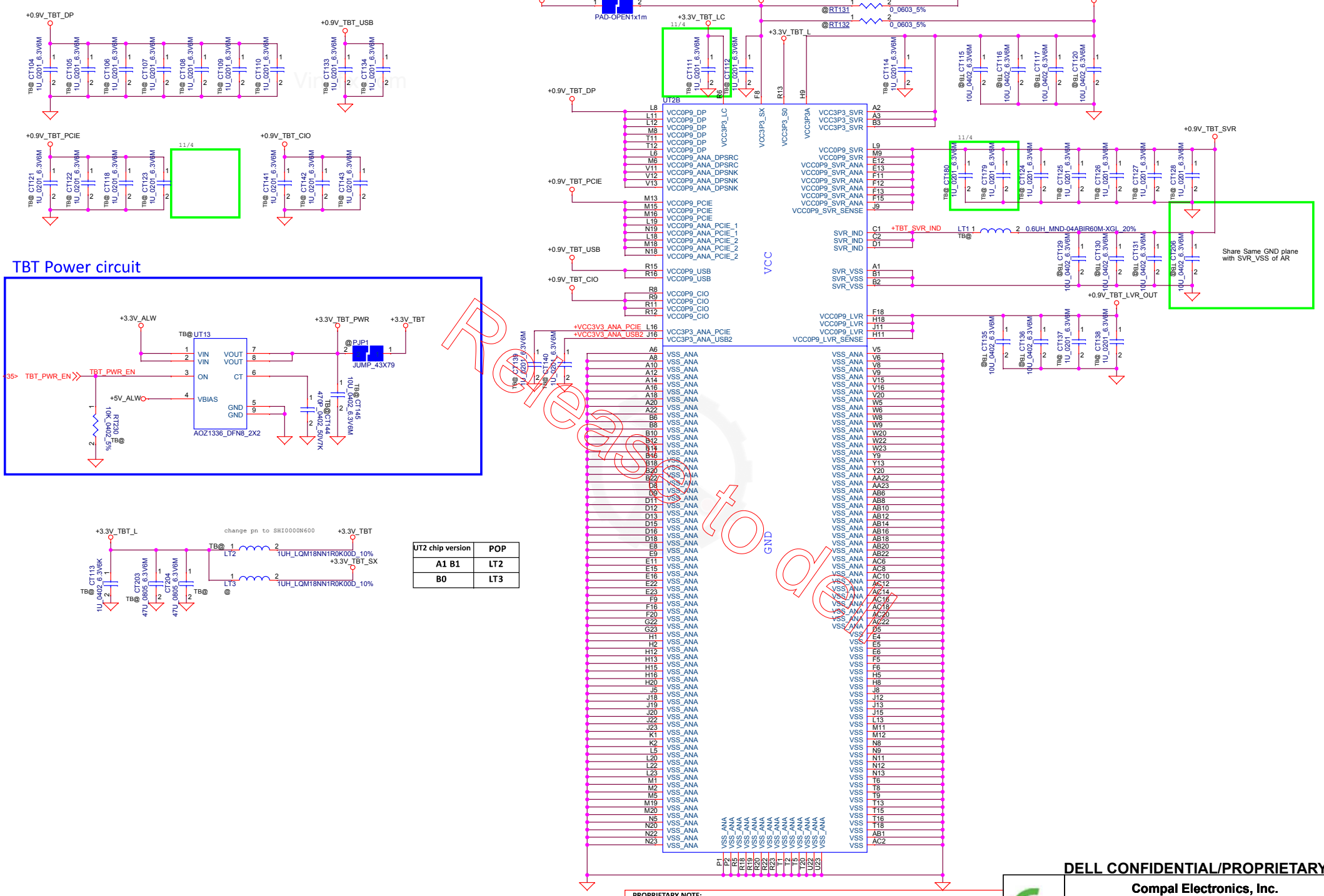
Compal Electronics, Inc.

Title: HDD CONN

Size | Document Number: LA-C841P | Rev: 1.0

Date: Tuesday, September 08, 2015 | Sheet 45 of 74


+3.3V_TBT_FLASH_R
+3.3V_TBT_LC
+3.3V_TBT
+3.3V_TBT_SX
UT2A
PCIe GEN3
SINK PORT 0
SOURCE PORT 0
SINK PORT 1
LC GPIO
POC GPIO
Misc
MISC
TBT PORTS
Port A
PORT B
POC
DEBUG
ALPINE-RIDGE_BGA337
W25Q80DVSSIG_SO8
TPS3895ADRYT_SON6
PI3MVR31313A has internal PD 120Kohm
PI3MVR31310 has internal PD 120Kohm
10/27 follow UPD reference circuit
Rework Debug Pin1 +3.3V_TBT_LC, Pin6 GND
10/30
11/10
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
TBT-AR-SP(1/4) DP, PCIE
LA-C841P
Rev 0.1
Tuesday, September 08, 2015
Sheet 46 of 74



UT2 chip version	POP
A1 B1	LT2
B0	LT3

PROPRIETARY NOTE:
THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

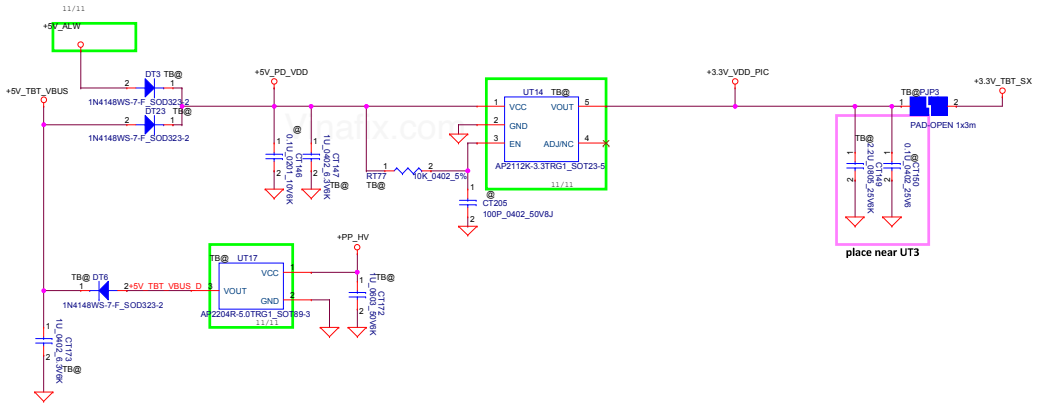
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: TBT-AR-SP(2/4) PWR,VSS

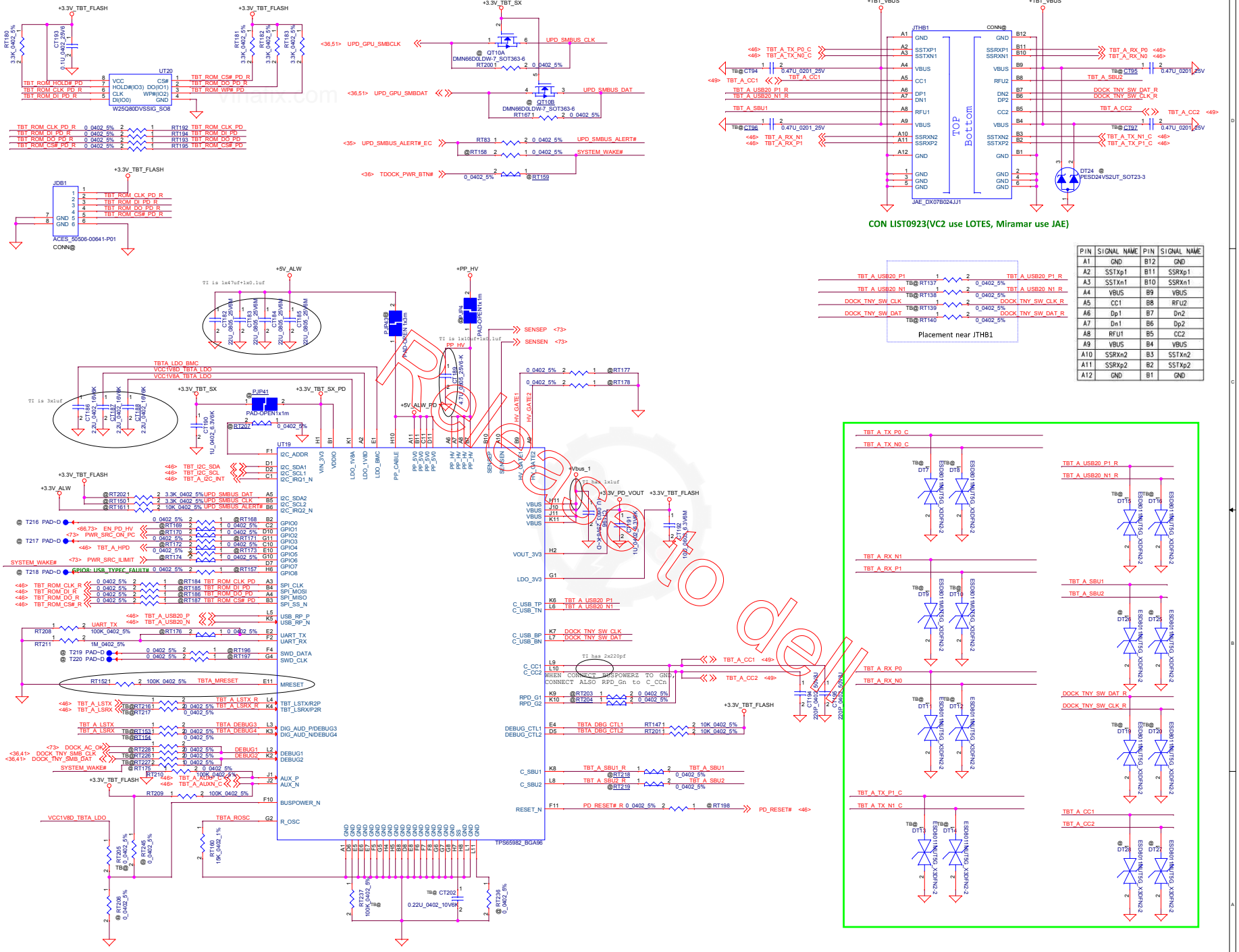
Size: | Document Number: LA-C841P | Rev: 0.1

Date: Tuesday, September 08, 2015 | Sheet 47 of 74



Compal Electronics, Inc.

Title	TBT-AR-SP(3/4) PD	
Size	Document Number LA-C841P	Rev 0.1
Date: Tuesday, September 08, 2015	Sheet 48 of 74	



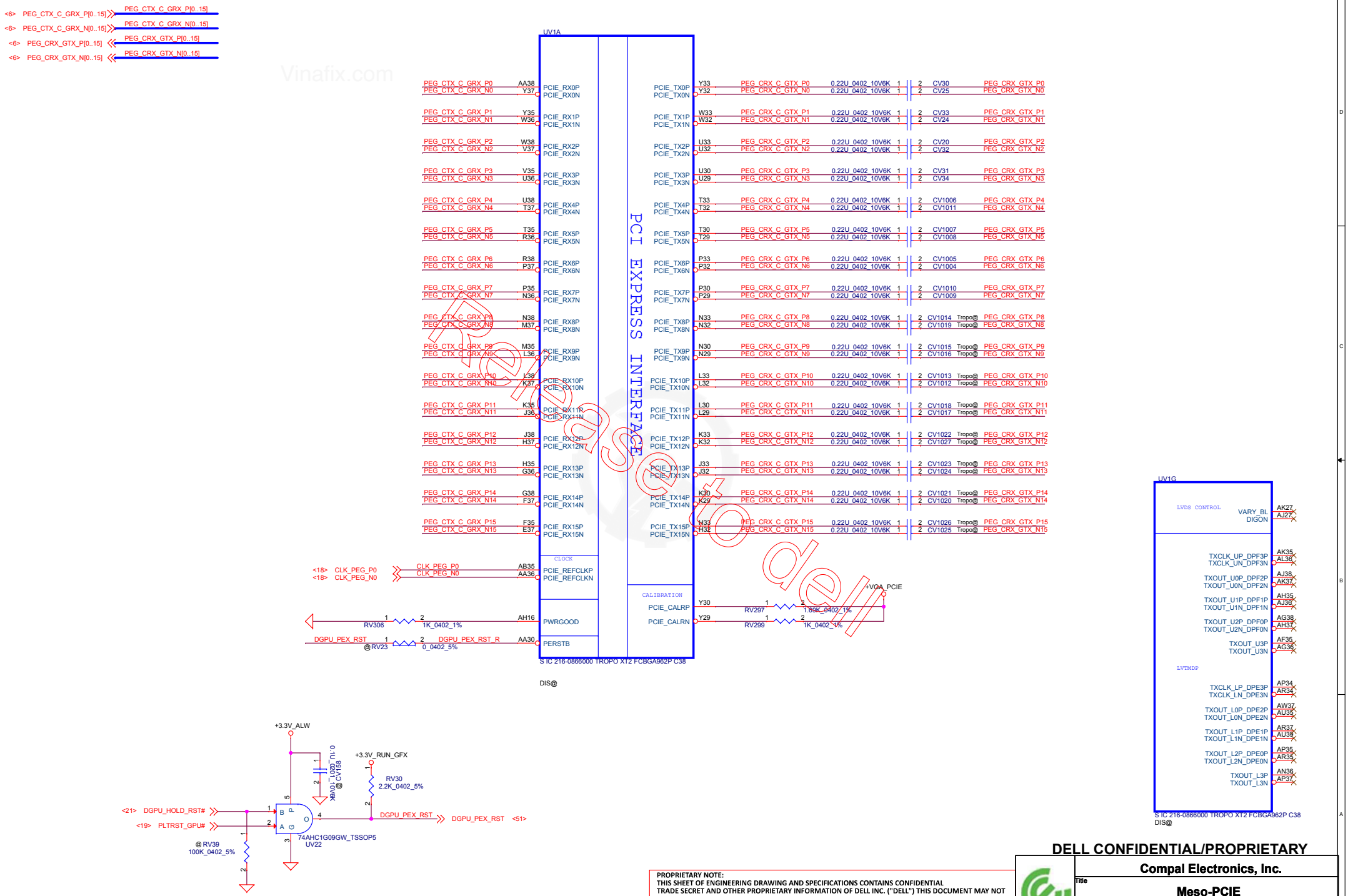
PIN	SIGNAL NAME	PIN	SIGNAL NAME
A1	GND	B12	GND
A2	SSTXp1	B11	SSRXp1
A3	SSTXn1	B10	SSRXn1
A4	VBUS	B9	VBUS
A5	CC1	B8	RFU2
A6	Dp1	B7	Dn2
A7	Dn1	B6	Dp2
A8	RFU1	B5	CC2
A9	VBUS	B4	VBUS
A10	SSRXn2	B3	SSTXn2
A11	SSRXp2	B2	SSTXp2
A12	GND	B1	GND

Compal Electronics, Inc.

Title: TBT-AR-SP(4/4) AUX SW,conn

Size: | Document Number: LA-C841P | Rev: 0.1

Date: Tuesday, September 08, 2015 | Sheet 49 of 74



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	Meso-PCIE
Size	Document Number: LA-C841P
Rev	0.1
Date:	Tuesday, September 08, 2015
Sheet	50 of 74

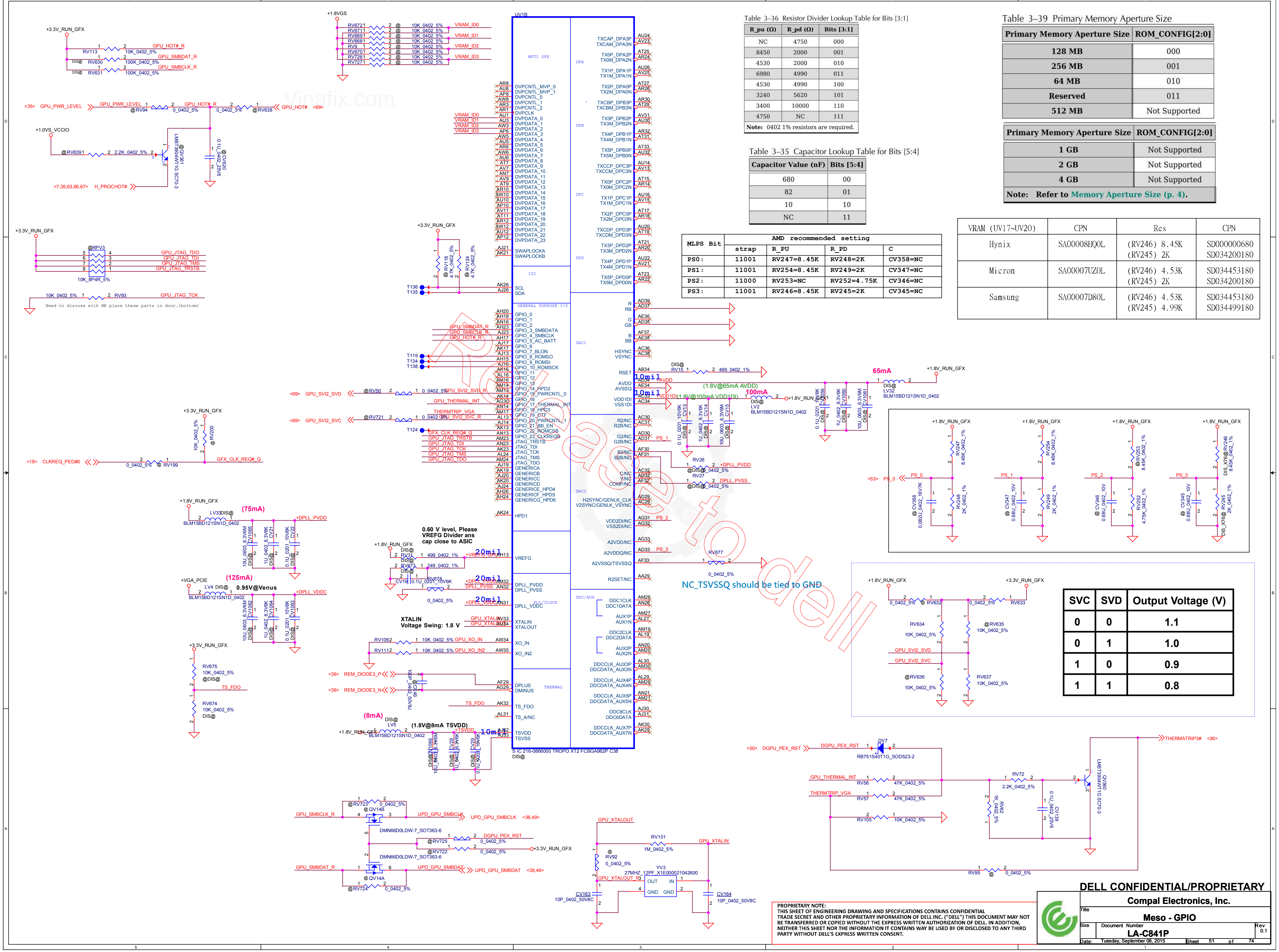


Table 3–36 Resistor Divider Lookup Table for Bits [3:1]

R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

Table 3–35 Capacitor Lookup Table for Bits [5:4]

Capacitor Value (nF)	Bits [5:4]
680	00
82	01
10	10
NC	11

Table 3–39 Primary Memory Aperture Size

Primary Memory Aperture Size	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011
512 MB	Not Supported

Primary Memory Aperture Size	ROM_CONFIG[2:0]
1 GB	Not Supported
2 GB	Not Supported
4 GB	Not Supported

Note: Refer to Memory Aperture Size (p. 4).

MLPS Bit	AMD recommended setting			
	strap	R_PU	R_PD	C
PS0:	11001	RV247=8.45K	RV248=2K	CV358=NC
PS1:	11001	RV254=8.45K	RV249=2K	CV347=NC
PS2:	11000	RV253=NC	RV252=4.75K	CV346=NC
PS3:	11001	RV246=8.45K	RV245=2K	CV345=NC

VRAM (UV17~UV20)	CPN	Res	CPN
Hynix	SA00008HQ0L	(RV246) 8.45K (RV245) 2K	SD000000680 SD034200180
Micron	SA00007UZ0L	(RV246) 4.53K (RV245) 2K	SD034453180 SD034200180
Samsung	SA00007D80L	(RV246) 4.53K (RV245) 4.99K	SD034453180 SD034499180

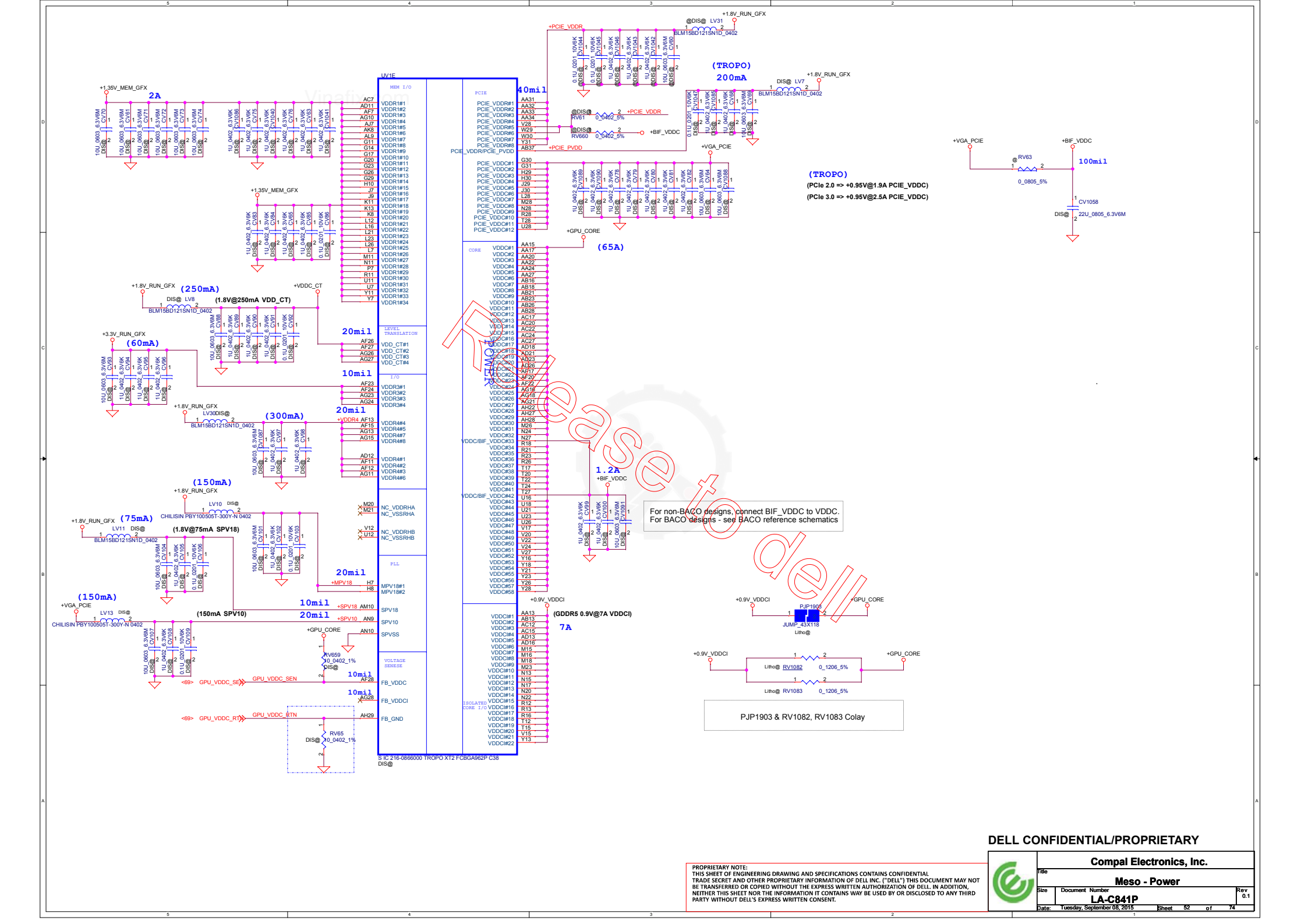
SVC	SVD	Output Voltage (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

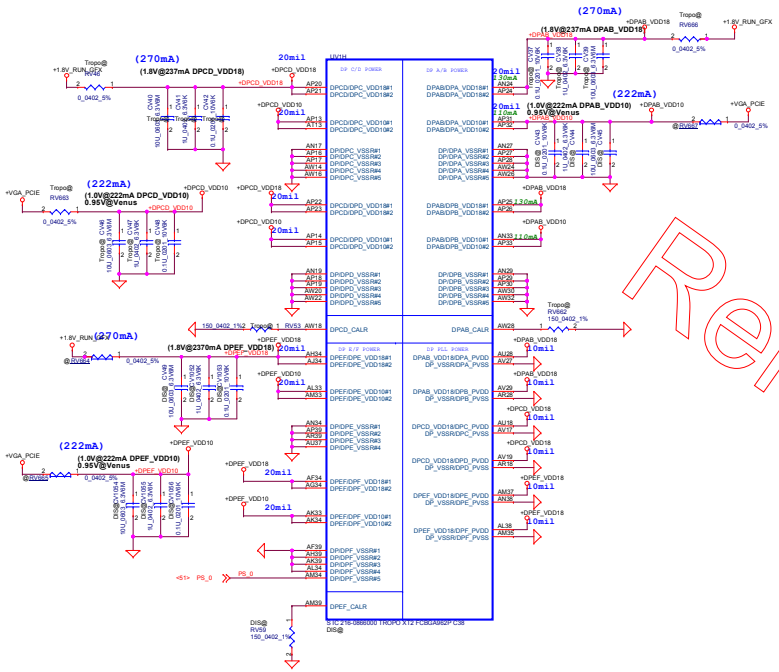
Compal Electronics, Inc.

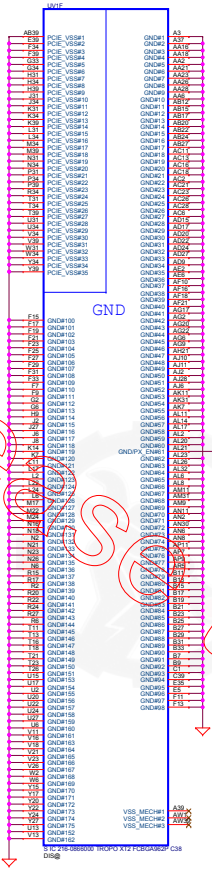
Title: Meso - GPIO

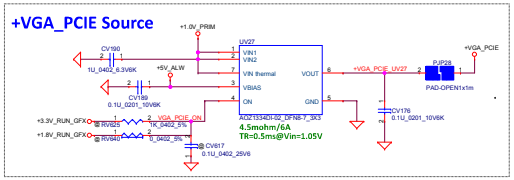
Document Number: LA-C841P — Rev 0.1

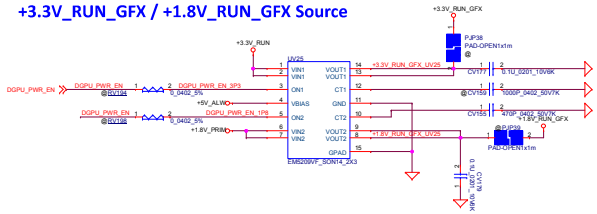
Date: Tuesday, September 08, 2015 — Sheet 51 of 74


UV1E
SIC 216-0866000 TROPO X12 FCBGA962P C38
DIS@
(TROPO)
200mA
(TROPO)
(PCIe 2.0 => +0.95V@1.9A PCIE_VDDC)
(PCIe 3.0 => +0.95V@2.5A PCIE_VDDC)
(65A)
1.2A
(GDDR5 0.9V@7A VDDCI)
7A
(250mA)
(60mA)
(300mA)
(150mA)
(75mA)
(150mA)
2A
(1.8V@250mA VDD_CT)
(1.8V@75mA SPV18)
(150mA SPV10)
20mil
10mil
40mil
100mil
For non-BACO designs, connect BIF_VDDC to VDDC.
For BACO designs - see BACO reference schematics
PJP1903 & RV1082, RV1083 Colay
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
Meso - Power
LA-C841P
Tuesday, September 08, 2015
PROPRIETARY NOTE:
THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

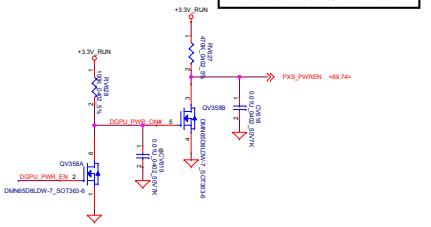








check CT setting and confirm 0.95V source from which CPU rail



DELL CONFIDENTIAL/PROPRIETARY

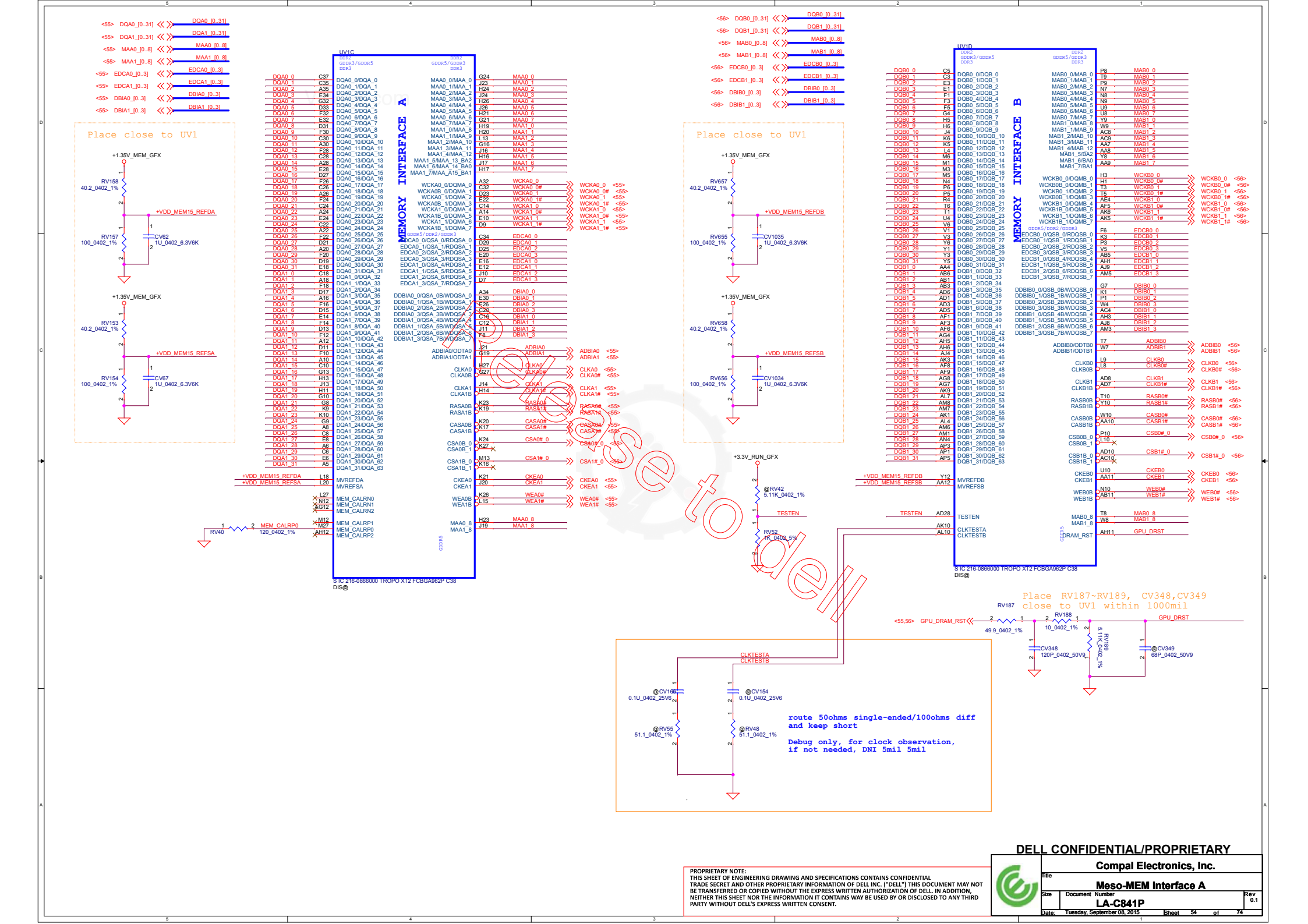
Compal Electronics, Inc.

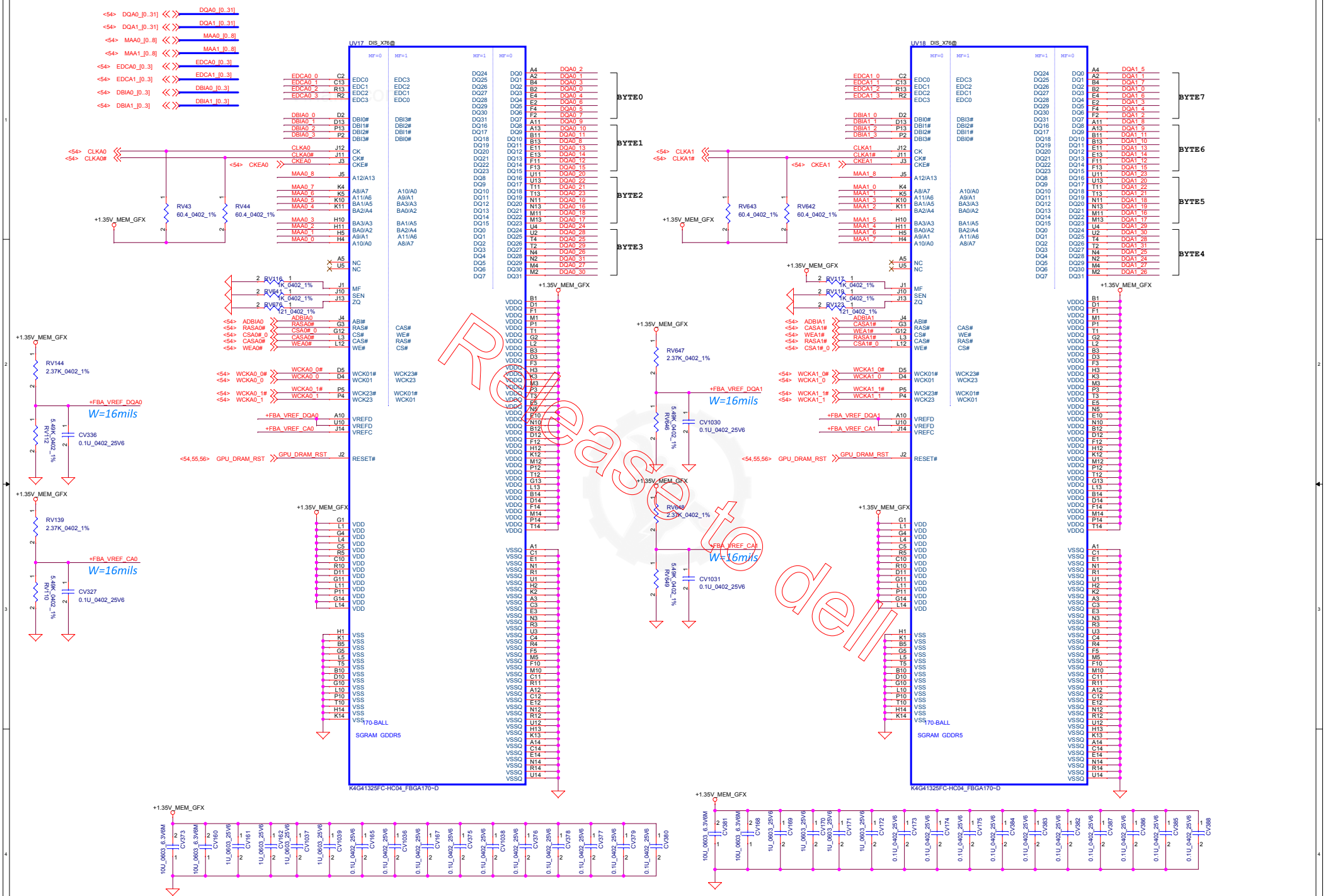
Title: Meso - DP Power,GND

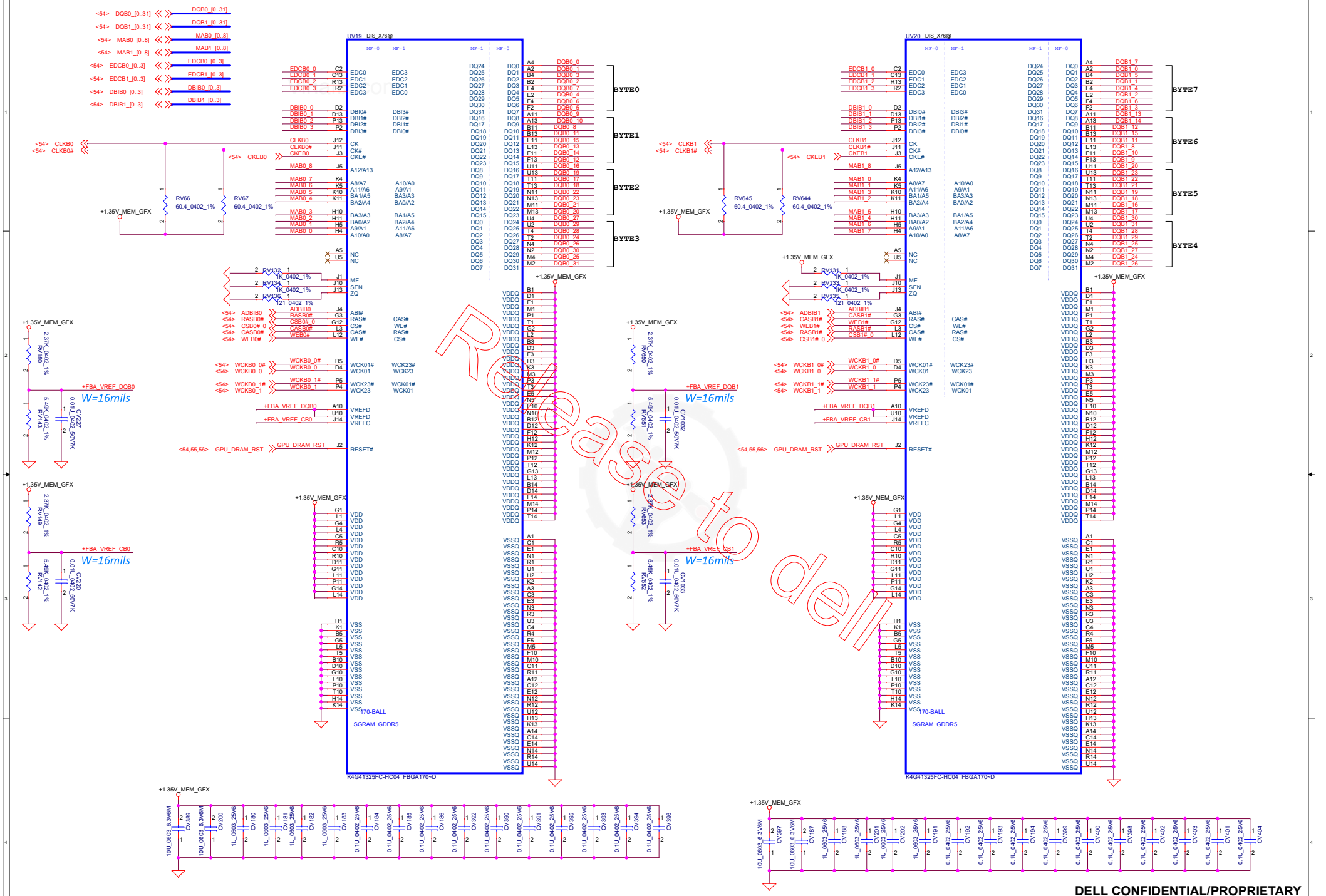
Size: Document Number: LA-C841P

Rev: 0.1

Date: Tuesday, September 08, 2015 Sheet 53 of 74


MEMORY INTERFACE A
MEMORY INTERFACE B
Place close to UV1
Place RV187~RV189, CV348,CV349 close to UV1 within 1000mil
route 50ohms single-ended/100ohms diff and keep short
Debug only, for clock observation, if not needed, DNI 5mil 5mil
S IC 216-0866000 TROPO XT2 FCBGA962P C38
DIS@
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
Meso-MEM Interface A
LA-C841P
Tuesday, September 08, 2015
PROPRIETARY NOTE:
THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.


UV17 DIS_X76@
UV18 DIS_X76@
K4G41325FC-HC04_FBGA170-D
170-BALL
SGRAM GDDR5
BYTE0
BYTE1
BYTE2
BYTE3
BYTE4
BYTE5
BYTE6
BYTE7
+1.35V_MEM_GFX
+FBA_VREF_DQA0
+FBA_VREF_CA0
+FBA_VREF_DQA1
+FBA_VREF_CA1
W=16mils
GPU_DRAM_RST
RV43 60.4_0402_1%
RV44 60.4_0402_1%
RV642 60.4_0402_1%
RV643 60.4_0402_1%
RV144 2.37K_0402_1%
RV139 2.37K_0402_1%
RV647 2.37K_0402_1%
RV648 2.37K_0402_1%
RV112 5.49K_0402_1%
RV110 5.49K_0402_1%
RV645 5.49K_0402_1%
RV649 5.49K_0402_1%
CV336 0.1U_0402_25V6
CV327 0.1U_0402_25V6
CV1030 0.1U_0402_25V6
CV1031 0.1U_0402_25V6
10U_0603_6.3V6M
0.1U_0402_25V6
1K_0402_1%
121_0402_1%
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
GDDR5 VRAM A
LA-C841P
Rev 0.1
Tuesday, September 08, 2015
Sheet 55 of 74
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

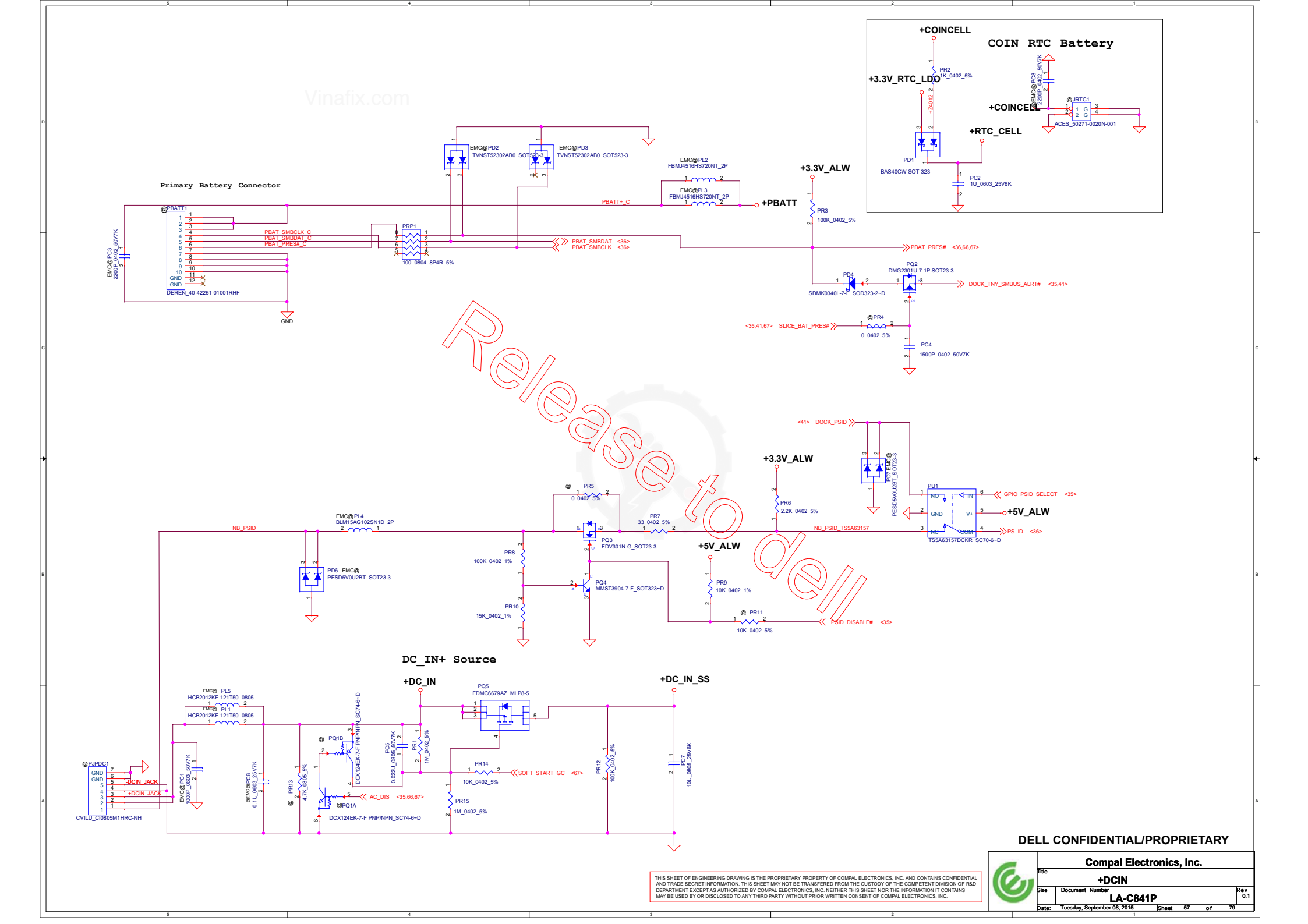


Compal Electronics, Inc.

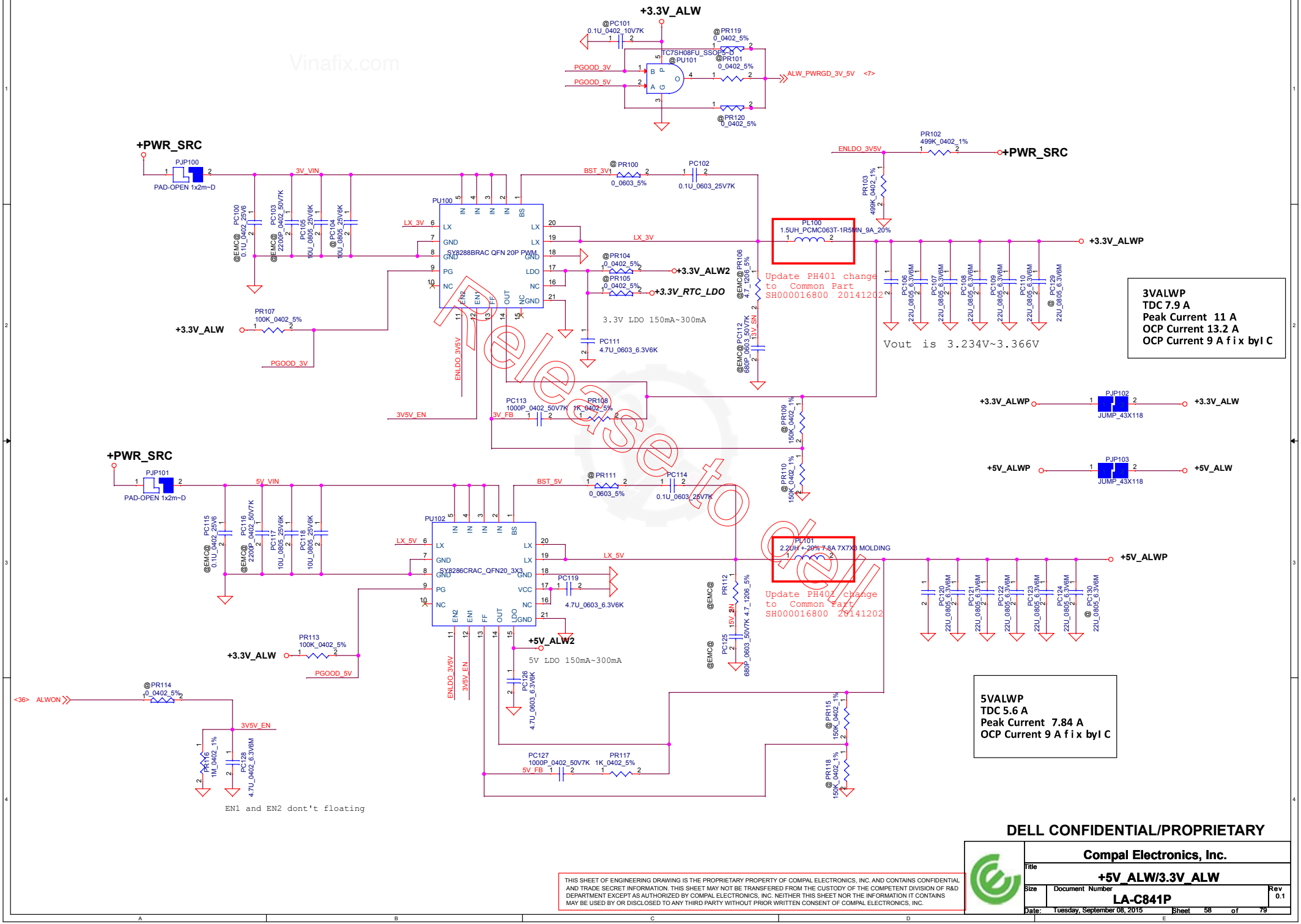
Title: GDDR5 VRAM B

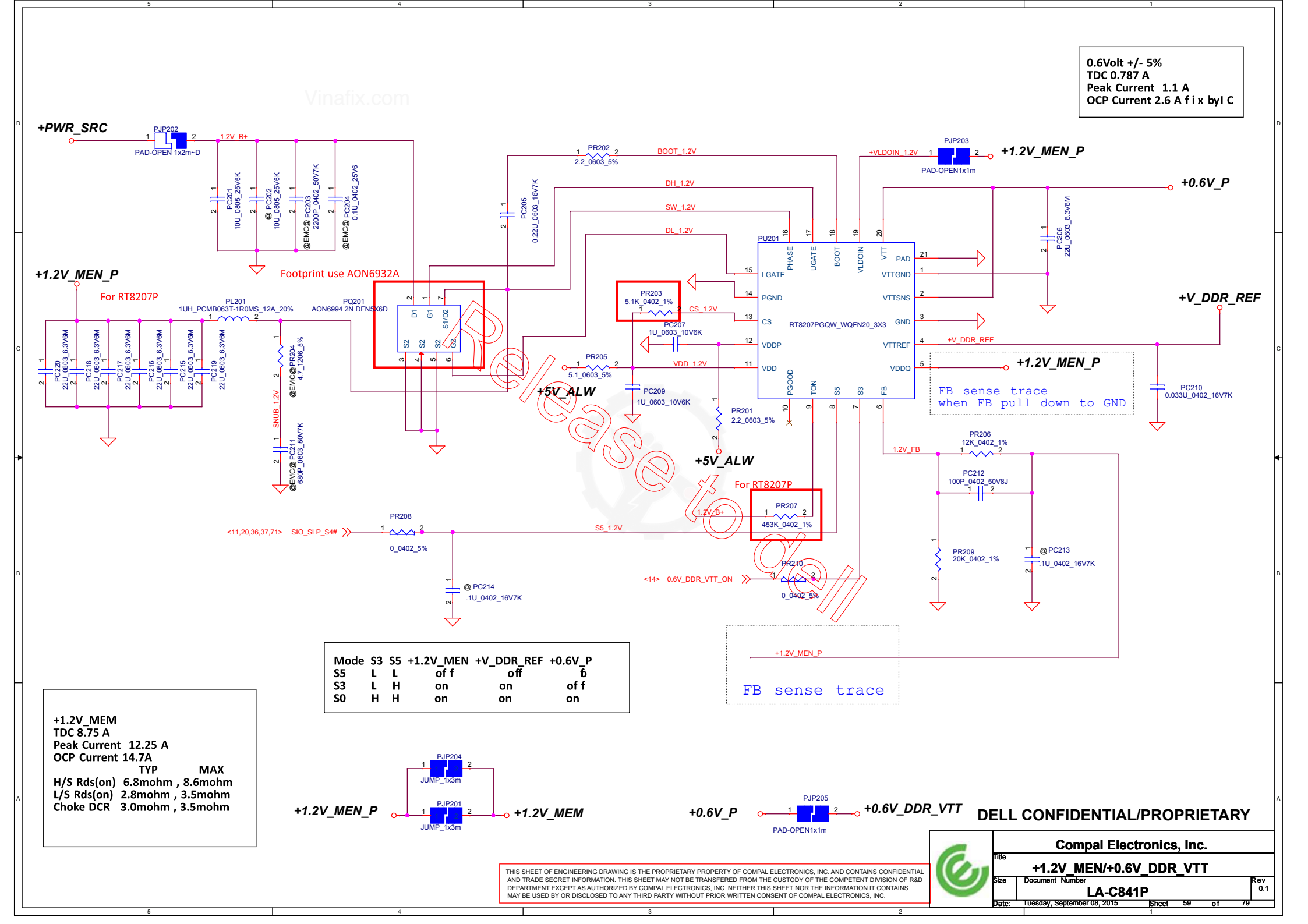
Size: | Document Number: LA-C841P | Rev: 0.1

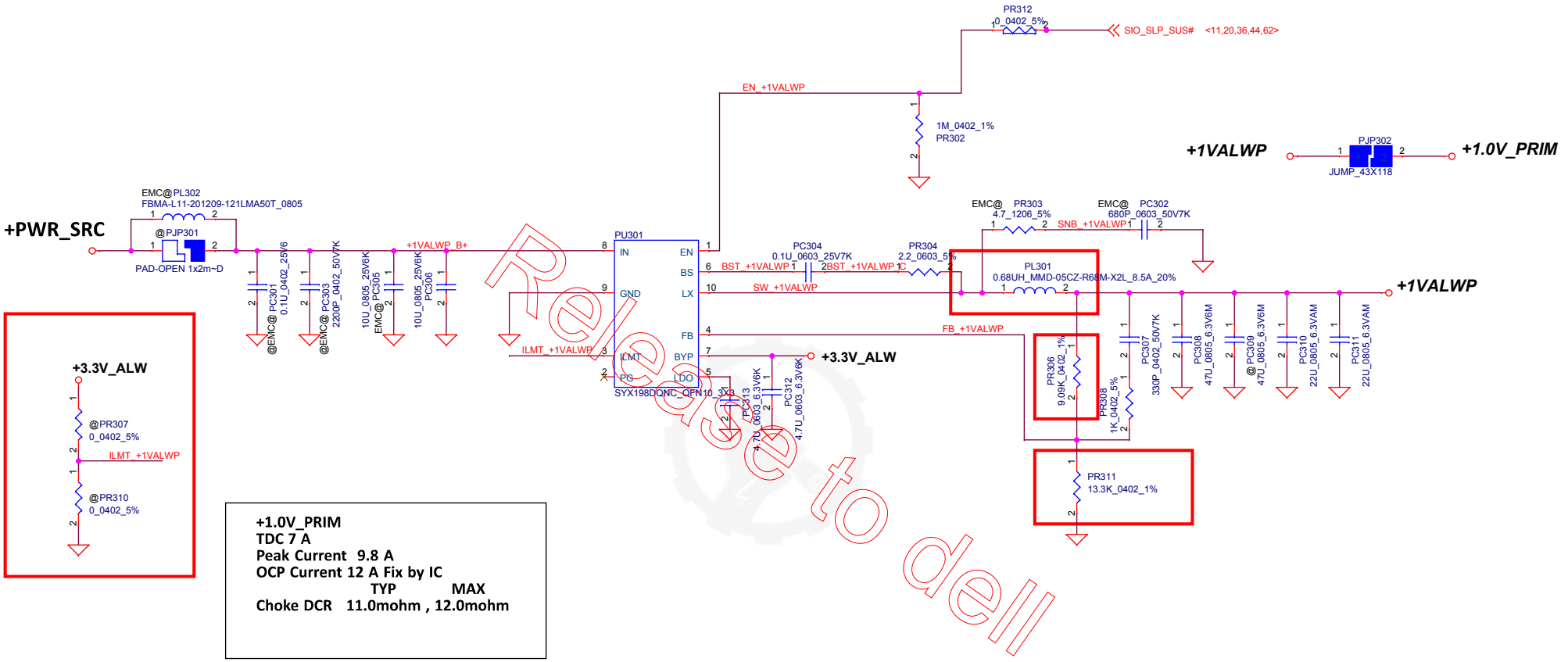
Date: Tuesday, September 08, 2015 | Sheet 56 of 74



Compal Electronics, Inc.		
Title: +DCIN		
Size	Document Number: LA-C841P	Rev: 0.1
Date: Tuesday, September 08, 2015	Sheet 57 of 79	

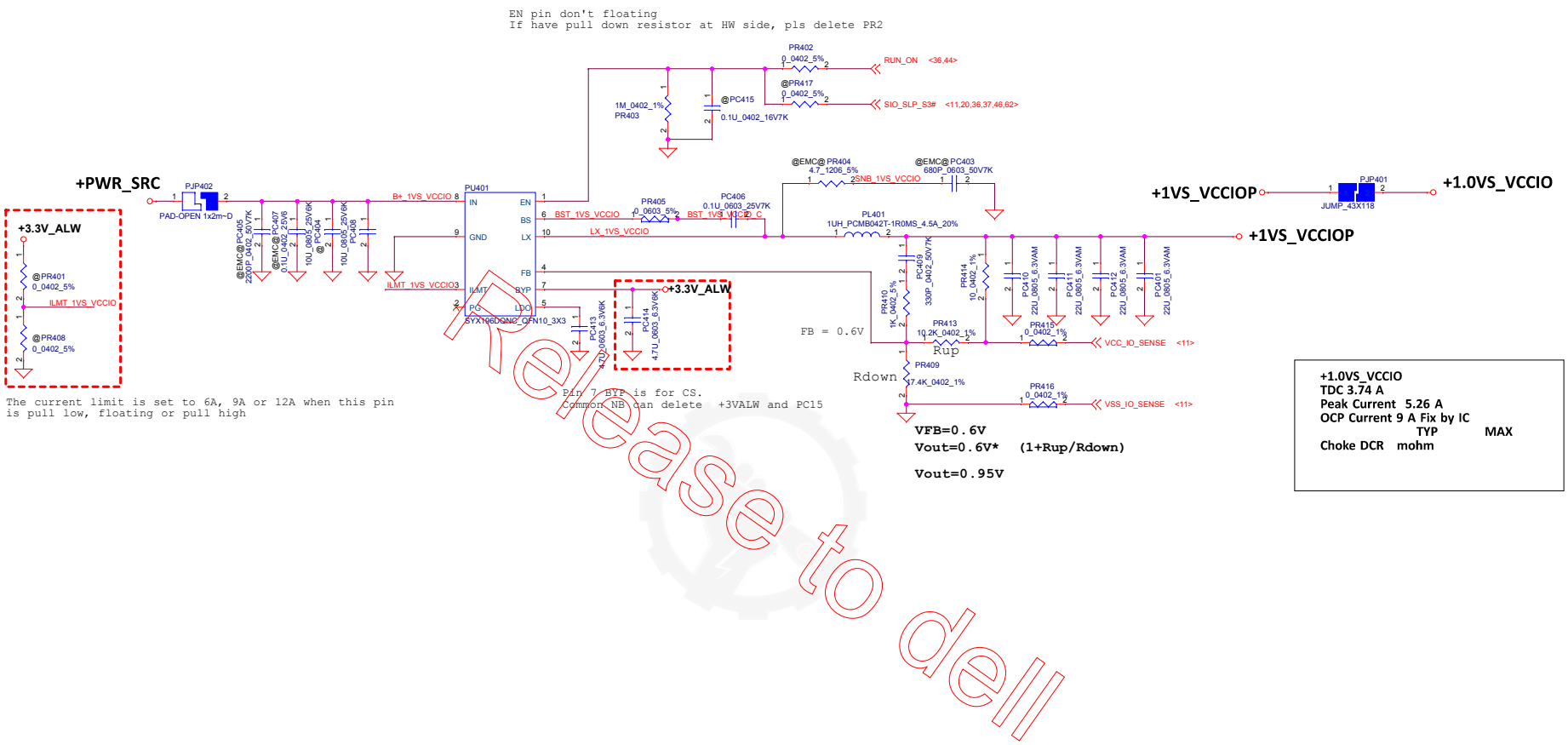



0.6Volt +/- 5%
TDC 0.787 A
Peak Current 1.1 A
OCP Current 2.6 A f i x by l C
+PWR_SRC
PJP202
PAD-OPEN 1x2m~D
1.2V_B+
PC201 10U_0805_25V6K
@ PC202 10U_0805_25V6K
@EMC@ PC203 2200P_0402_50V7K
@EMC@ PC204 0.1U_0402_25V6
PC205 0.22U_0603_16V7K
PR202 2.2_0603_5%
BOOT_1.2V
DH_1.2V
SW_1.2V
DL_1.2V
PU201
RT8207PGQW_WQFN20_3X3
PHASE
UGATE
BOOT
VLDOIN
VTT
PAD
LGATE
PGND
CS
VDDP
VDD
VTTGND
VTTSNS
GND
VTTREF
VDDQ
PGOOD
TON
S5
S3
FB
+VLDOIN_1.2V
PJP203
PAD-OPEN1x1m
+1.2V_MEN_P
+0.6V_P
PC206 22U_0603_6.3V6M
+V_DDR_REF
PC210 0.033U_0402_16V7K
+1.2V_MEN_P
FB sense trace
when FB pull down to GND
+1.2V_MEN_P
For RT8207P
PL201 1UH_PCMB063T-1R0MS_12A_20%
PQ201 AON6994 2N DFN5X6D
Footprint use AON6932A
PC220 22U_0603_6.3V6M
PC218 22U_0603_6.3V6M
PC217 22U_0603_6.3V6M
PC216 22U_0603_6.3V6M
PC215 22U_0603_6.3V6M
PC219 22U_0603_6.3V6M
SNUB_1.2V
@EMC@ PR204 4.7_1206_5%
@EMC@ PC211 680P_0603_50V7K
PR203 5.1K_0402_1%
CS_1.2V
PC207 1U_0603_10V6K
PR205 5.1_0603_5%
VDD_1.2V
PC209 1U_0603_10V6K
PR201 2.2_0603_5%
+5V_ALW
+5V_ALW
For RT8207P
PR206 12K_0402_1%
1.2V_FB
PC212 100P_0402_50V8J
PR207 453K_0402_1%
1.2V_B+
PR209 20K_0402_1%
@ PC213 .1U_0402_16V7K
PR208
<11,20,36,37,71> SIO_SLP_S4#
0_0402_5%
S5_1.2V
@ PC214 .1U_0402_16V7K
PR210
<14> 0.6V_DDR_VTT_ON
0_0402_5%
+1.2V_MEN_P
FB sense trace
Mode S3 S5 +1.2V_MEN +V_DDR_REF +0.6V_P
S5 L L of f off of f
S3 L H on on of f
S0 H H on on on
+1.2V_MEM
TDC 8.75 A
Peak Current 12.25 A
OCP Current 14.7A
TYP MAX
H/S Rds(on) 6.8mohm , 8.6mohm
L/S Rds(on) 2.8mohm , 3.5mohm
Choke DCR 3.0mohm , 3.5mohm
PJP204
JUMP_1x3m
PJP201
JUMP_1x3m
+1.2V_MEN_P
+1.2V_MEM
+0.6V_P
PJP205
PAD-OPEN1x1m
+0.6V_DDR_VTT
DELL CONFIDENTIAL/PROPRIETARY
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.
Compal Electronics, Inc.
Title
+1.2V_MEN/+0.6V_DDR_VTT
Size
Document Number
LA-C841P
Rev
0.1
Date: Tuesday, September 08, 2015
Sheet 59 of 79

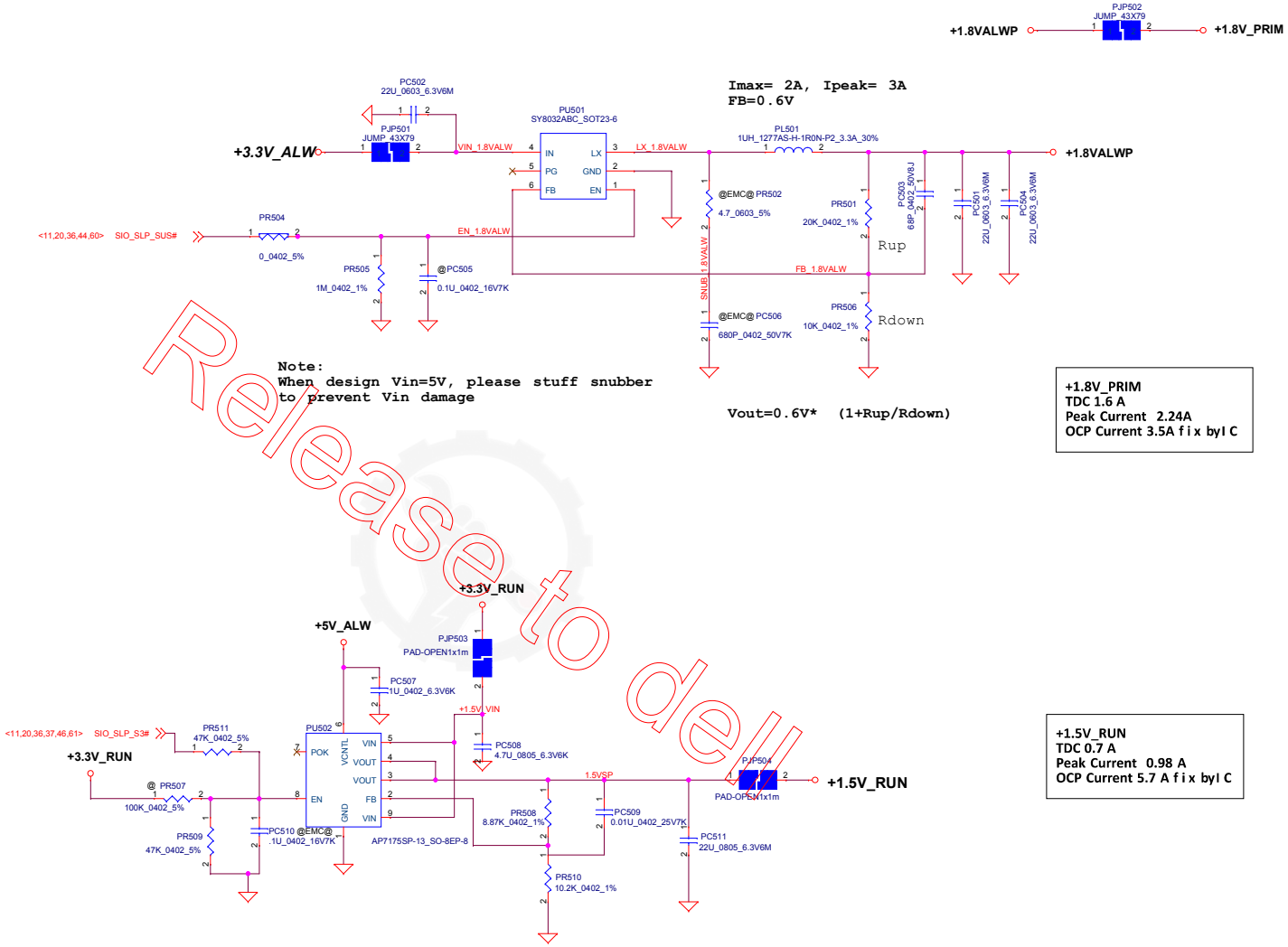


DELL CONFIDENTIAL/PROPRIETARY

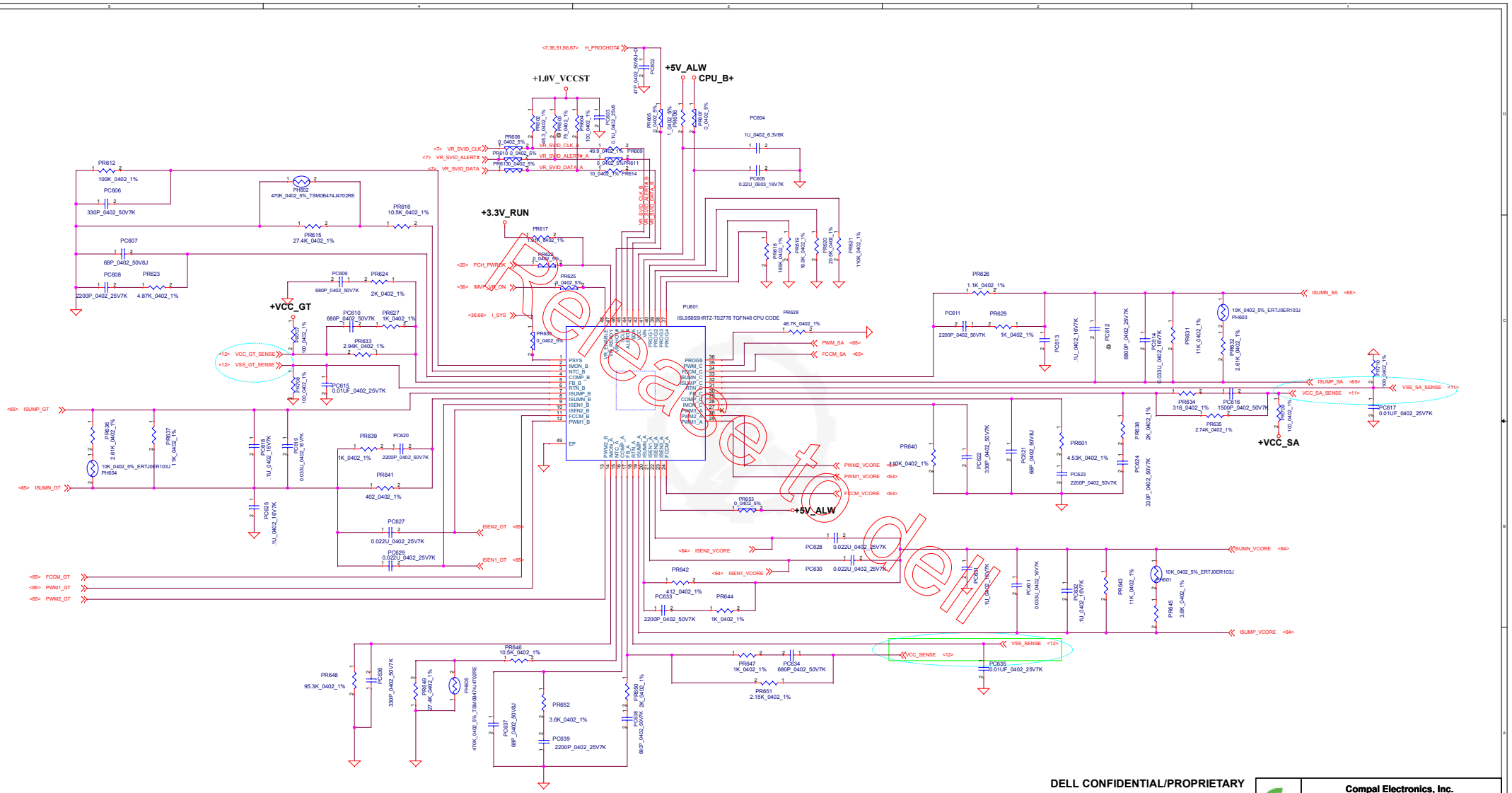
Compal Electronics, Inc.		
Title: +1VALWP		
Size	Document Number: LA-C841P	Rev: 0.1
Date: Tuesday, September 08, 2015	Sheet 60 of 79	



Compal Electronics, Inc.	
Title	+1VS_VCCIO
Size	Document Number: LA-C841P
Rev	0.1
Date:	Tuesday, September 08, 2015
Sheet	61 of 79



Compal Electronics, Inc.		
Title: +1.8VALWP/+1.5VSP		
Size	Document Number: LA-C841P	Rev: 0.1
Date: Tuesday, September 08, 2015	Sheet 62 of 79	

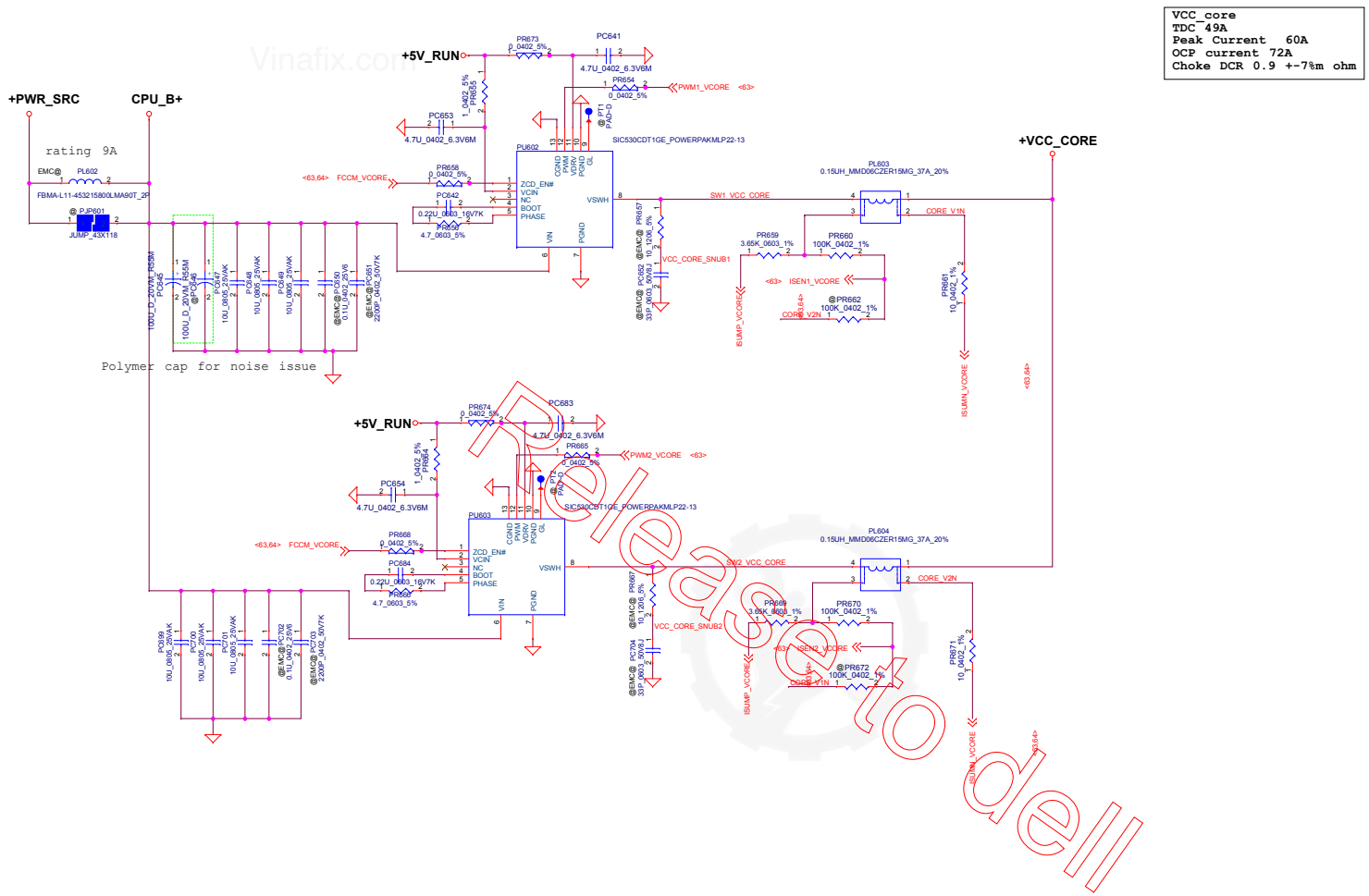


Compal Electronics, Inc.

File: VCORE_ISL95855

Size: | Document Number: LA-C841P | Rev: 0.1

Date: Tuesday, September 08, 2015 | Sheet 63 of 79



DELL CONFIDENTIAL/PROPRIETARY

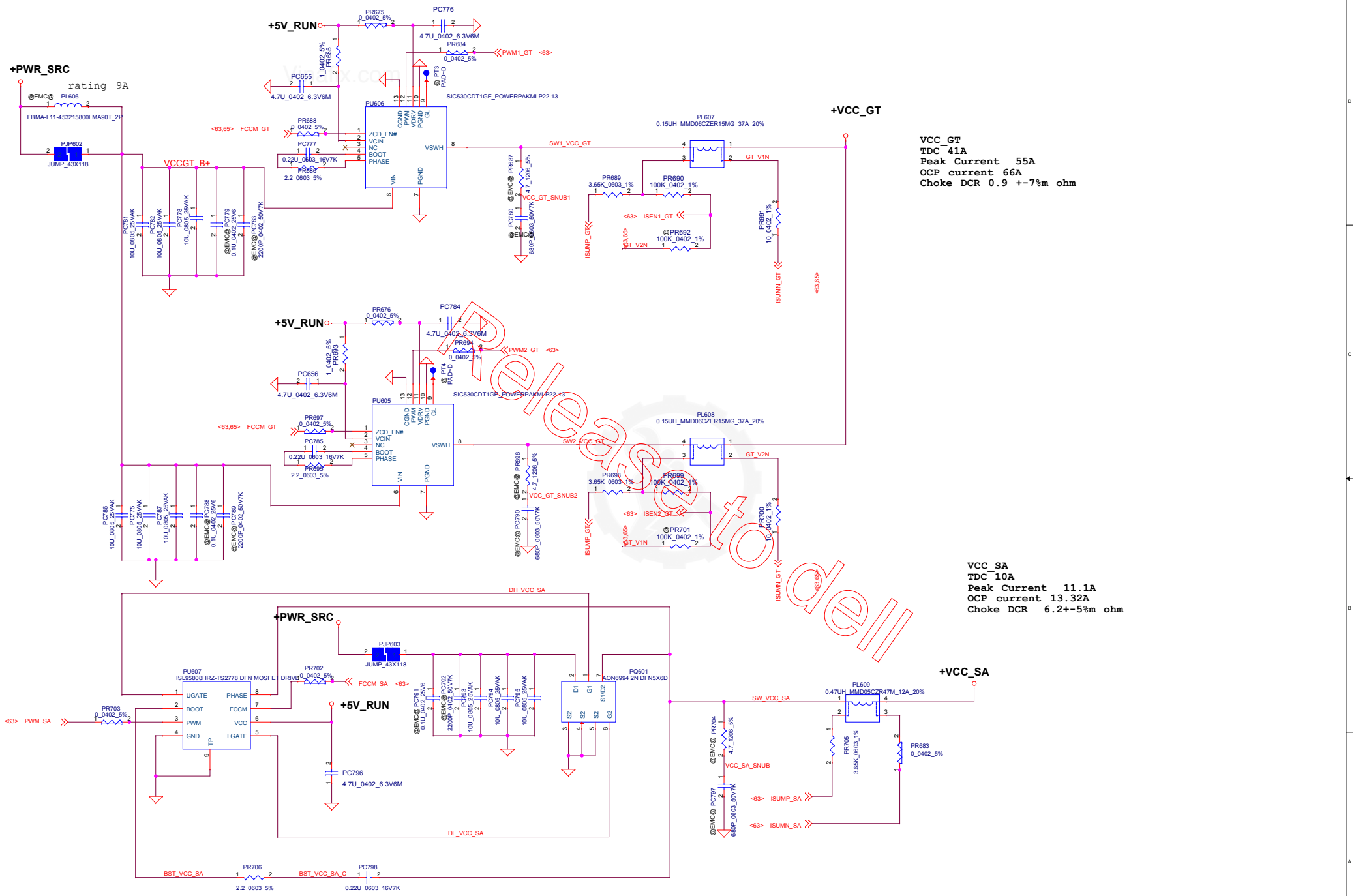
Compal Electronics, Inc.

Title: VCORE

Size: Document Number: LA-C841P

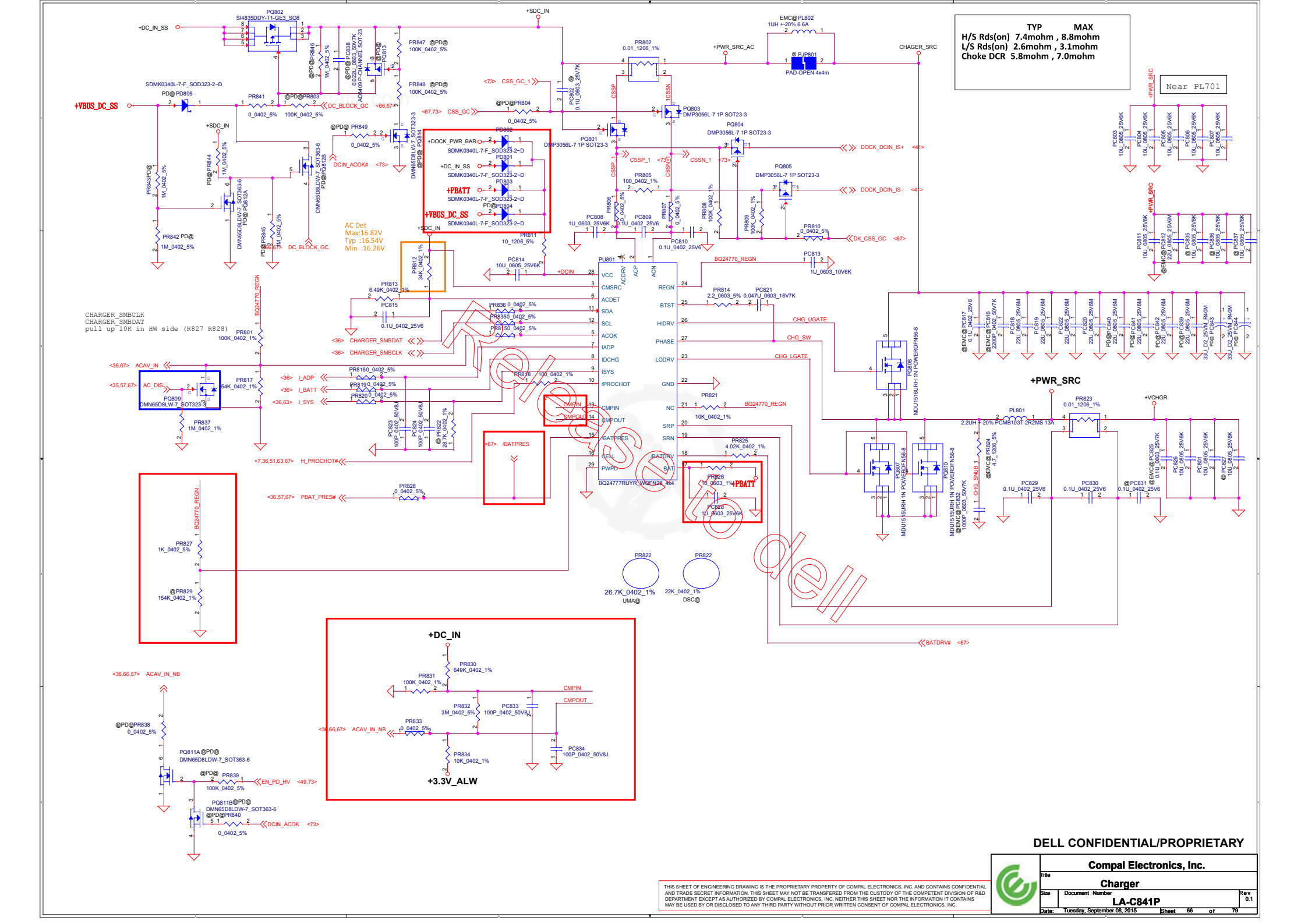
Rev: 0.1

Date: Tuesday, September 08, 2015 Sheet 64 of 79



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	VGT_VSA
Size	Document Number: LA-C841P
Rev	0.1
Date:	Tuesday, September 08, 2015
Sheet	65 of 79


TYP MAX
H/S Rds(on) 7.4mohm , 8.8mohm
L/S Rds(on) 2.6mohm , 3.1mohm
Choke DCR 5.8mohm , 7.0mohm
Near PL701
AC Det
Max:16.82V
Typ :16.54V
Min :16.26V
CHARGER_SMBCLK
CHARGER_SMBDAT
pull up 10K in HW side (R827 R828)
+DC_IN
+3.3V_ALW
+PWR_SRC
+VBUS_DC_SS
+PBATT
BQ24777RUYR_WQFN28_4X4
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
Charger
LA-C841P
Rev 0.1
Tuesday, September 08, 2015
Sheet 66 of 79

Purpose: Trigger PROCHOT# when active battery is removed from system.
Allows EC to re-establish system performance for battery next in line.

Purpose: Turn on the PQ817 for primary or module bay battery to provide power to dock side without AC exist.

Vth=0.5-1.5V

Compal Electronics, Inc.

Title: Selector

Size | Document Number: LA-C841P | Rev: 0.1

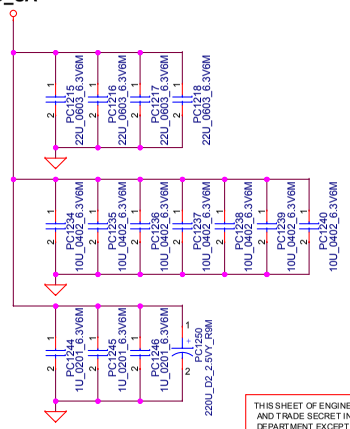
Date: Tuesday, September 08, 2015 | Sheet 67 of 79

VCC_CORE Place on CPU
Back Side.
22U_0603 * 8 pcs + 10U_0402*28 pcs + 1U_0201*35 pcs
Primary Side.
22U_0603 * 8 pcs+330u_D2*2 pcs

+VCC_CORE

VCC_CORE Place on CPU
Back Side.
22U_0603 * 2 pcs + 10U_0402*7 pcs + 1U_0201*3 pcs
Primary Side.
22U_0603 * 2 pcs + 220u_D2*1 pcs

+VCC_SA



VCC_GT Place on CPU
Back Side.
22U_0603 * 8 pcs +10U_0402*35 pcs +1U_0201*68 pcs
Primary Side.
22U_0603 * 12 pcs +470u_D2*2 pcs

+VCC_GT

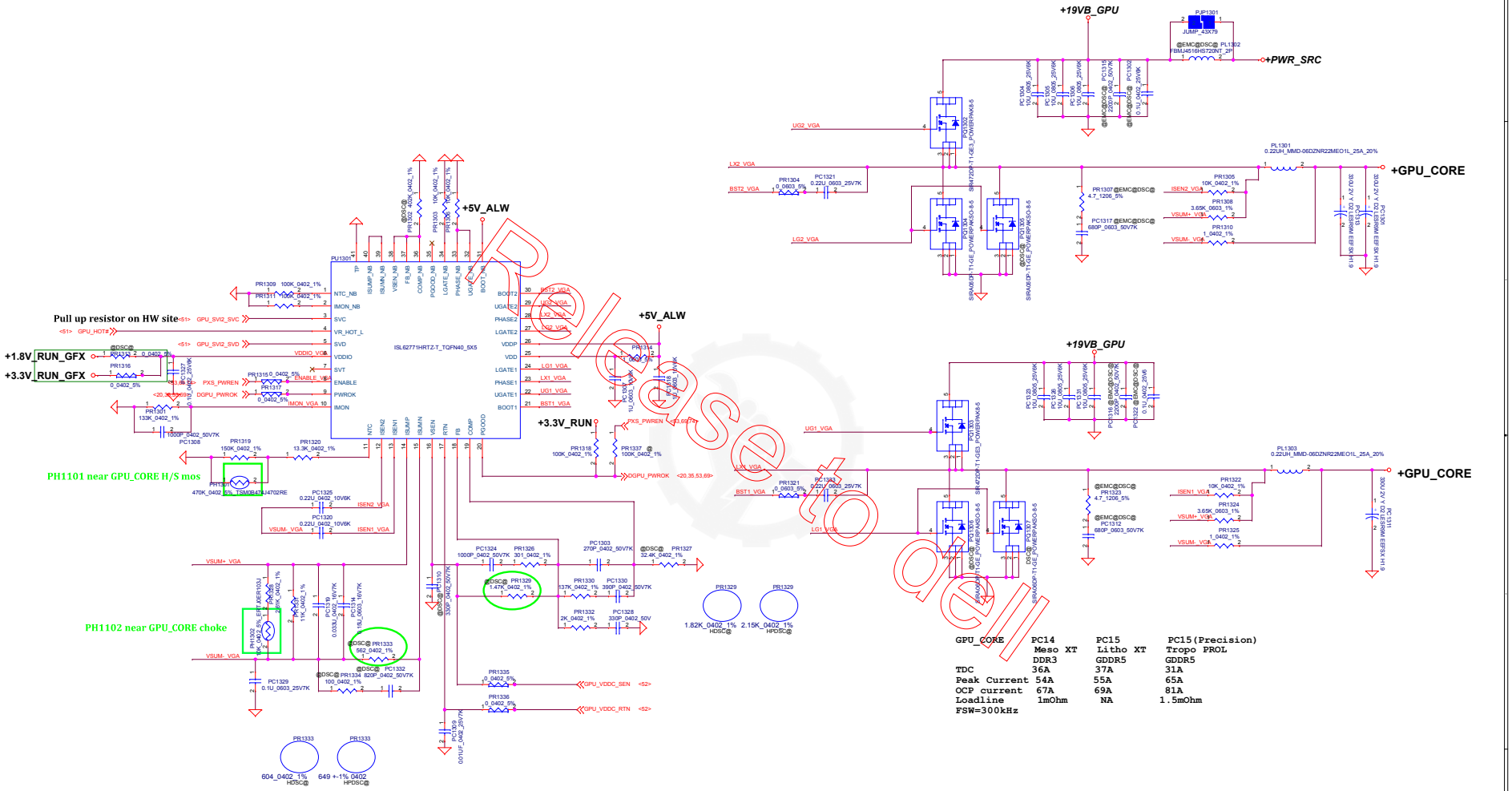
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

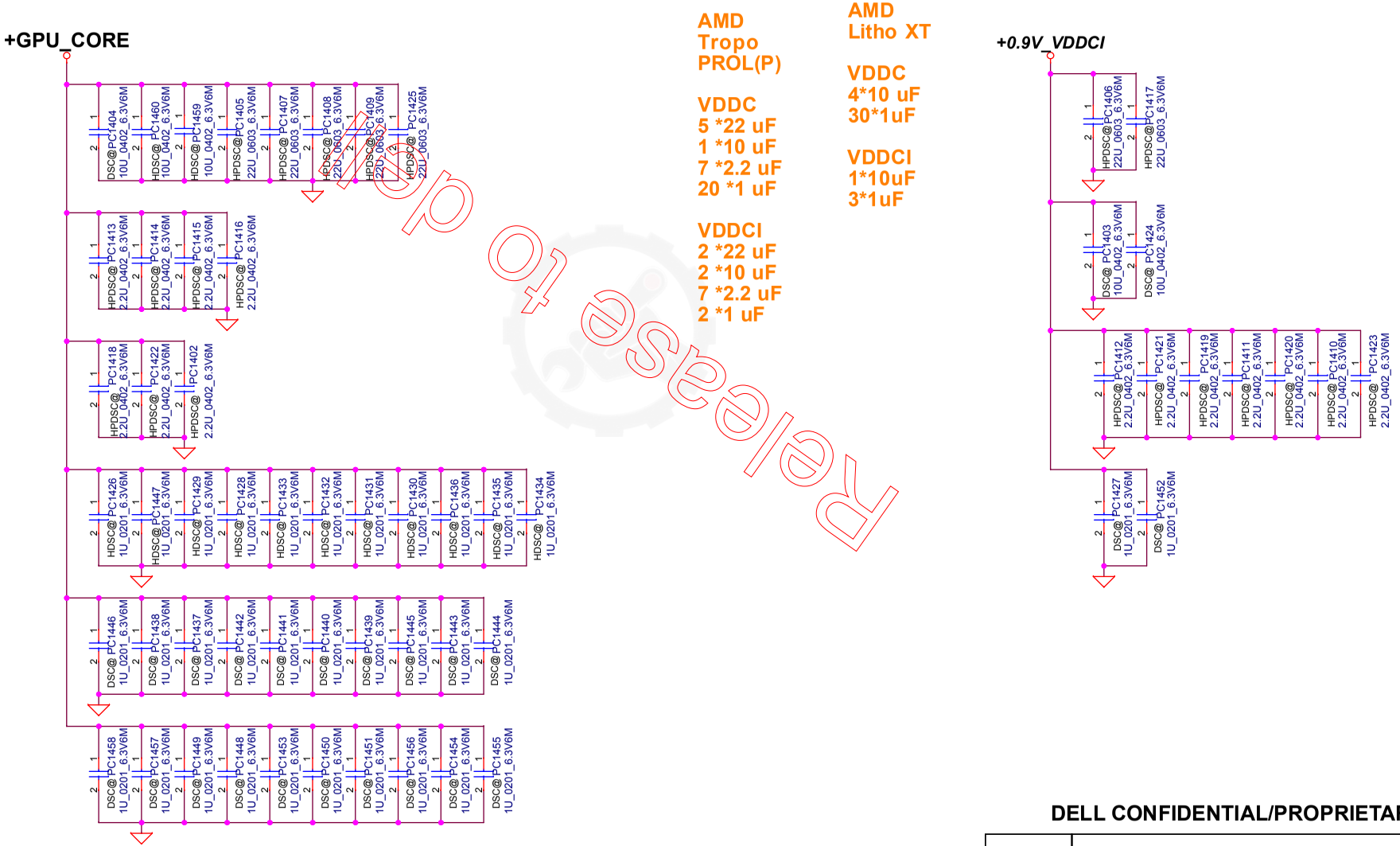
Title: PROCESSOR DECOUPLING

Size: | Document Number: LA-C841P | Rev: 0.1

Date: Tuesday, September 08, 2015 | Sheet 68 of 79

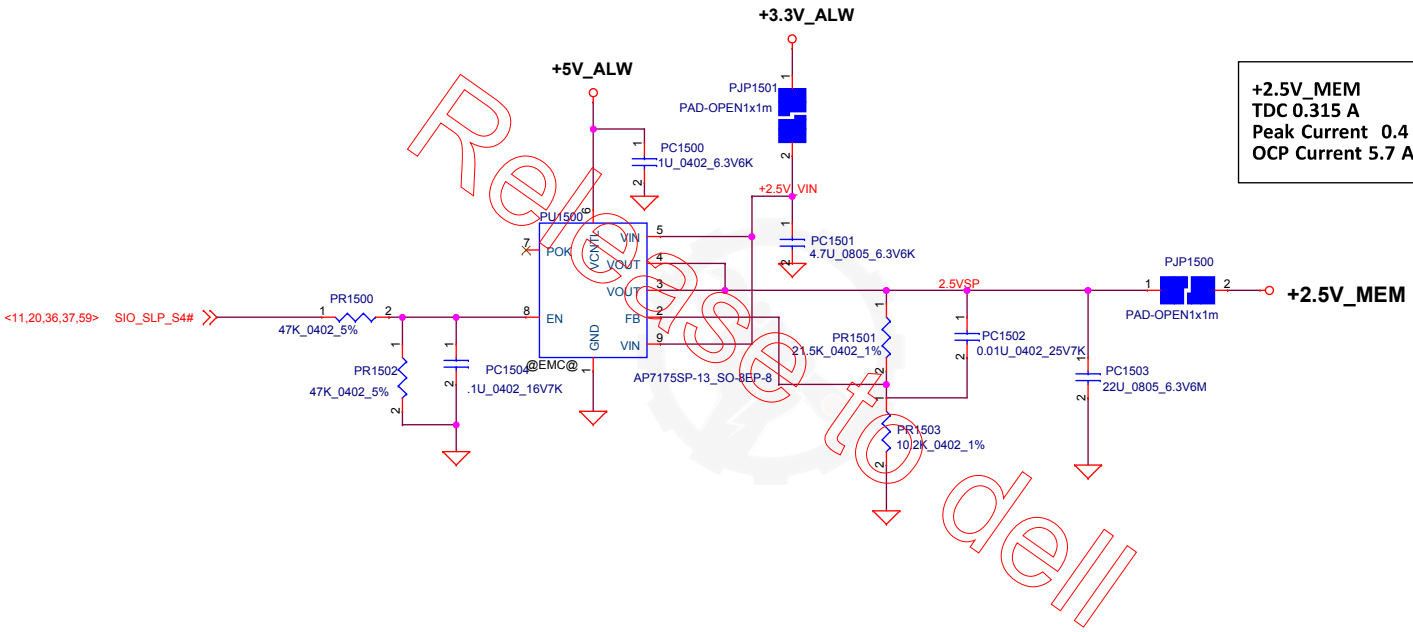


Compal Electronics, Inc.			
Title: +GPU_CORE			
Size	Document Number: LA-C841P		Rev: 0.1
Date: Tuesday, September 08, 2015	Sheet 69 of 79		



DELL CONFIDENTIAL/PROPRIETARY

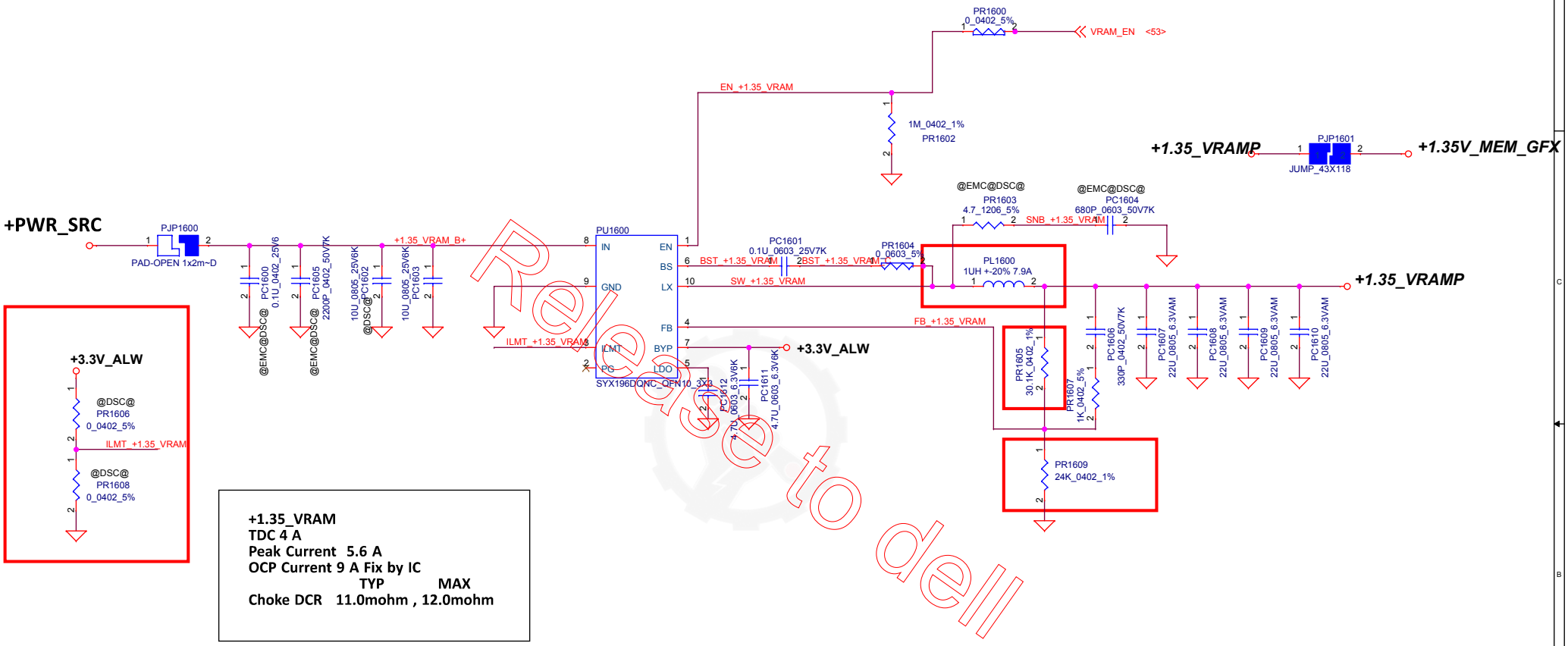
Compal Electronics, Inc.	
Title	GPU DECOUPLING
Size	Document Number: LA-C841P
Rev	0.1
Date:	Tuesday, September 08, 2015
Sheet	70 of 79



+2.5V_MEM
TDC 0.315 A
Peak Current 0.4 A
OCP Current 5.7 A f i x byl C

Compal Electronics, Inc.

Title	**+2.5V_MEM**	
Size	Document Number **LA-C841P**	Rev 0.1
Date: Tuesday, September 08, 2015	Sheet 71 of 79	

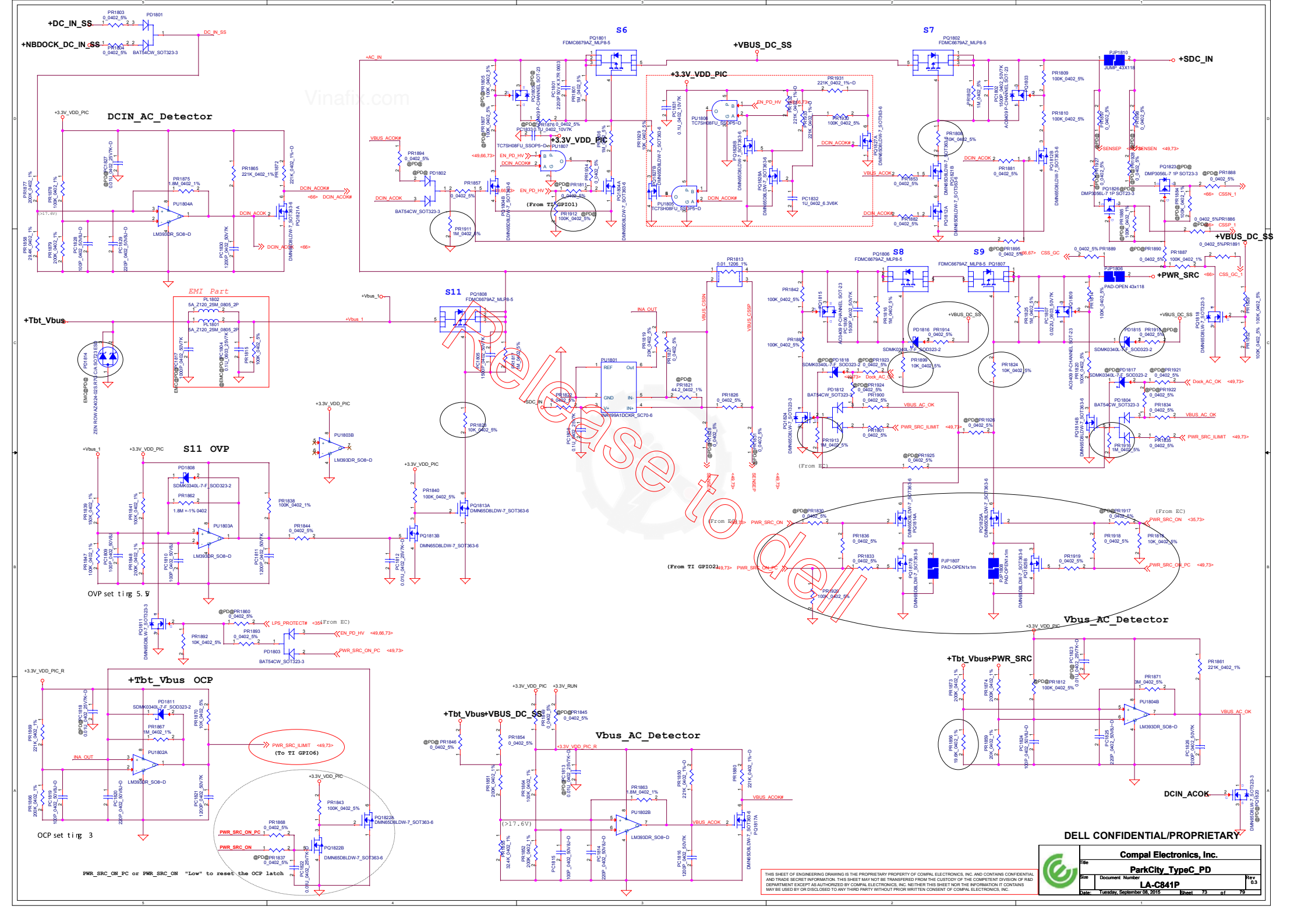


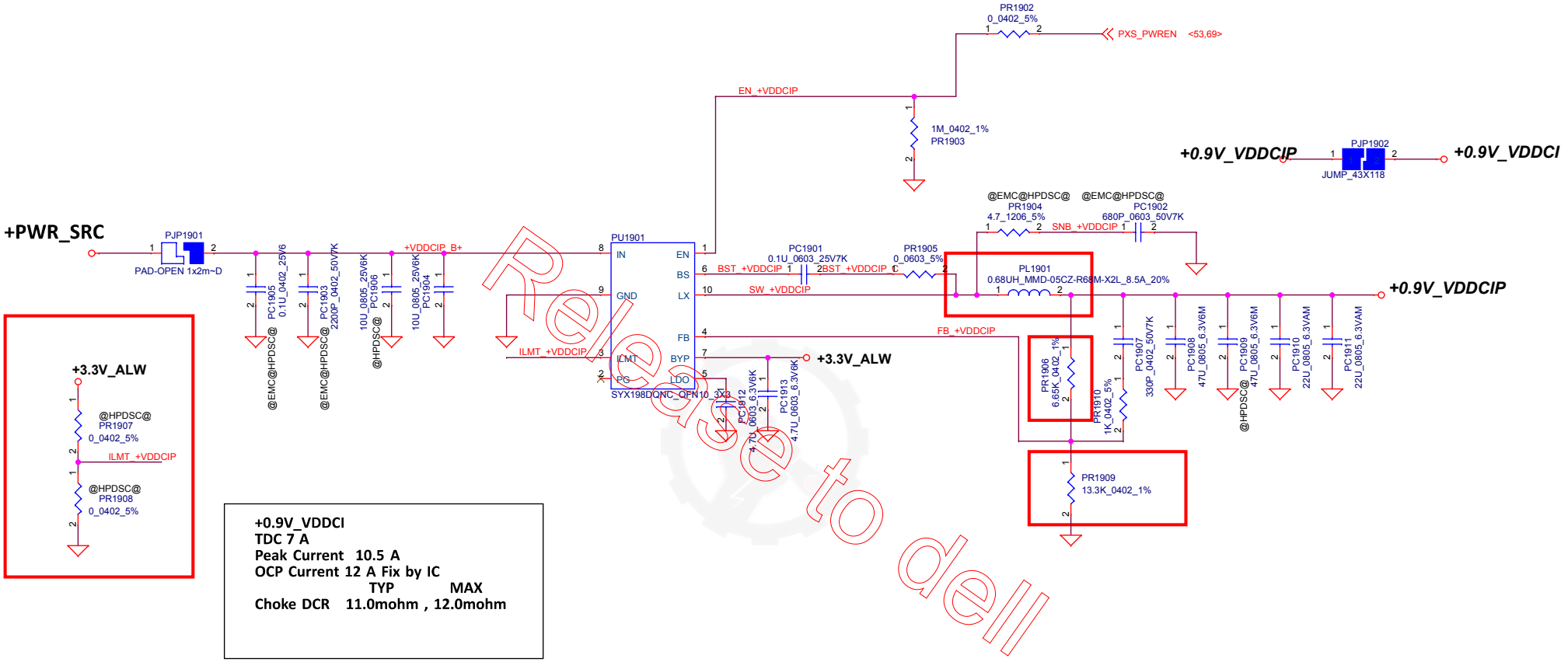
Compal Electronics, Inc.

Title: GPU_VRAM(SYX198D)

Size | Document Number: LA-C841P | Rev: 0.1

Date: Tuesday, September 08, 2015 | Sheet 72 of 79


+DC_IN_SS
+NBDOCK_DC_IN_SS
DC_IN_SS
DCIN_AC_Detector
S6
S7
+VBUS_DC_SS
+3.3V_VDD_PIC
+SDC_IN
+AC_IN
+VBUS_DC_SS
S8
S9
+PWR_SRC
+Tbt_Vbus
EMI Part
S11
S11 OVP
OVP set ting 5.5V
+Tbt_Vbus OCP
OCP set ting 3
PWR_SRC_ON_PC or PWR_SRC_ON "Low" to reset the OCP latch
Vbus_AC_Detector
+Tbt_Vbus+PWR_SRC
+Tbt_Vbus+VBUS_DC_SS
DCIN_ACOK
(From TI GPIO1)
(From TI GPIO2)
(From EC)
Vinafix.com
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
ParkCity_TypeC_PD
LA-C841P
Rev 0.3
Tuesday, September 08, 2015
Sheet 73 of 79



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	GPU_VDDCI(SYX198D)
Size	Document Number: LA-C841P
Rev	0.1
Date:	Tuesday, September 08, 2015
Sheet	74 of 79

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	74	Type-C PD	3/23	Compal	Ensure the DCIN_ACOK voltage level can not be divide.	Change the PR1865 PR1861 to 10K	X01
2	74	Type-C PD	3/23	Compal	Ensure the S6 Mosfet turn on sequency after PQ802 turn off to avoid the +SDC_IN oscillate to cause audible noise when with M/B AC and TypeC AC then pulg out M/B AC	Change the PR1806 to 40.2K	X01
3	74	Type-C PD	3/23	Compal	Voiad the +Vbus_DC_ss leak to +PWR_SRC when tininty dock with AC and M/B without AC	Depop PD1815 and PR1915	X01
4	74	Type-C PD	3/23	Compal	Reserve Dock_AC_OK circuit to turn off the S8 and S9 when trinity dock plug in AC	Reserve PR1921 PD1817 PR1922 PR1926 PR1925 PR1923 PR1924 PD1818	X01
5	67	Cherger	3/23	Compal	Provide the charger operate voltage when M/B just has TypeC AC only	Add PD804	X01
6	67	Cherger	3/23	Compal	Avoid the +SDC_IN oscillation to cause audible noise when system with M/B AC and TypeC AC then plug out M/B AC	Add PD805 PR843 PR842 PQ812 PR845 PR844 PR841 PR838 PQ811 PR839 PR840	X01
7	68	Selector	3/23	Compal	Avoid the +SDC_IN oscillation to cause audible noise when system with E-DOCK AC and TypeC adapter then plug out E-DOCK AC	Add PD906 PR943 PR944 PQ999 PR942 PR940 PR941	X01
8	74	Type-C PD	4/10	Compal	Reserve circuit for charger adapter monitor function when system with trinity dock AC only	Add PR1927 PR1928 PQ1826 PQ1823 PR1885 PR1888 PR1884 PR1886 PR1887 PR1829 PR1832 PQ1818 PR1889 PR1890 PR1891	X02
9	67	Cherger	4/10	Compal	Avoid the +SDC_IN oscillation to cause audible noise when system with M/B AC and TypeC AC then plug out M/B AC	Add PR1891 PR1889 PR1890 PR846 PC838 PQ813 PR847 PR848 PQ814 PR849	X02
10	74	Type-C PD	4/10	Compal	Add pull down for OVP circuit to enable OVP initial. Reserve control circuit from GPIO1 and GPIO2 for OVP function enable.	Add PR1927 PR1928 PQ1826 PQ1823 PR1885 PR1888 PR1884 PR1886 PR1887 PR1829 PR1832 PQ1818 PR1889 PR1890 PR1891	X02
11	74	Type-C PD	4/29	Compal	For reduce inrush current when dual AC and single AC (Dell request)	Add PU1805,PU1806,PC1831,PC1832,PQ1828,,PQ1827,PR1929,PR1930,PR1931 ,PR1932,PR1933	X02
12	74	Type-C PD	6/11	Compal	For reduce inrush current (PQ1805 close late), change method for S6 control	Depop PR1805,PR1807,PR1811 Add PU1807,PR1934 PC1833	X02
13	68	Selector	6/11	Compal	add 1 GPIO to program PROCHOT_GATE	Add PQ912 PR945 PC909 PU904 PR946 PR947	X02
14							
15							
16							
17							

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	21	PCH-H(6/9)	2015/02/28	COMPAL	Align PC14 GPIO for Non-DOCK	Reserve RH359 100K Pull down	0.2(X01)
2	6, 9	+VCC_IO	2015/02/28	COMPAL	PC15 H Can't boot issue	Change +VCC_IO to +1.0VS_VCCIO	0.2(X01)
3	20, 21	LAN_WAKE#	2015/02/28	COMPAL	LAN_WAKE# shut down auto pwr on issue	Pop RH93, Depop RL70	0.2(X01)
4	17	PCH-H(2/9)	2015/03/02	COMPAL	DCI (Direct Connect Interface) test	Add RH364, RH365	0.2(X01)
5	31	LAN	2015/03/02	COMPAL	IEEE EA measurement	Change LL2 ~ LL9 to 2.2 ohm Res (RL71~RL78)	0.2(X01)
6	36	MEC5085	2015/03/09	COMPAL	AC_PRESENT need PH.	Add RE309 PH to +3.3V_ALW	0.2(X01)
7	21	VGA	2015/03/09	COMPAL	0.1(X00) VGA no function	PH 2.2K ohm(RH369) to +3.3V_RUN on UH1.BE6 (DDPD_CTRLDATA)	0.2(X01)
8	46	AR	2015/03/09	COMPAL	AR circuit modify	Add RT212 ~RT221, Reserve RT212 & RT214	0.2(X01)
9	52	GPU	2015/03/09	COMPAL	Can't have different stencil for different GPU PWR jump	PJP1903 & RV1082, RV1083 Colay	0.2(X01)
10	46	AR	2015/03/11	COMPAL	AR circuit modify	LSTX and LSRX link to Debug 3 and 4	0.2(X01)
11	46	AR	2015/03/11	COMPAL	TBT & HDMI Priority	Swap AR DP0 & DP1	0.2(X01)
12	20	PCH-H(5/9)	2015/03/11	COMPAL	HDD_FALL_INT PH	Add RH355	0.2(X01)
13	46	AR	2015/03/12	COMPAL	AR circuit modify	Add RT222, RT223, RT224, RT225	0.2(X01)
14	37	TPM	2015/03/12	COMPAL	TPM circuit modify	Add RZ112, RZ113, Depop RZ108	0.2(X01)
15	21	PCH-H(6/9)	2015/03/12	COMPAL	DIMM TYPE GPIO	Add RH372	0.2(X01)
16	26, 27	DP DeMux	2015/03/19	COMPAL	HDMI & DP EA Fail	UV28, UV29 change from Pericom to Parade solution.	0.2(X01)
17	49	AR	2015/03/02	COMPAL	AR circuit modify	DOCK_AC_OK and SYSTEM_WAKE# link to Debug 1 and 2	0.2(X01)
18	21	PCH-H(6/9)	2015/03/27	COMPAL	IR_CAM_DET# GPIO	IR Camera pin change and new GPIO on GPP_A23, include PU RH373	0.3(X02)
19	46	TBT AR	2015/03/30	COMPAL	AR ROM PWR RAIL Modify	Remove RT214, RT215; Add PWR Rail +3.3V_TBT_FLASH_R	0.3(X02)
20	37	USH & TPM2.0	2015/03/30	COMPAL	USH RST#	Add RZ114, RZ115 & Depop, USH RST#	0.3(X02)
21	47	TBT AR	2015/03/30	COMPAL	Modify AR +3.3V_TBT_SX	DEPOP RT131	0.3(X02)
22	46	TBT AR	2015/03/30	COMPAL	Add Reset IC for PD_RESET# AR reset must assert after +3.3V_TBT 100us	Add UT23, CT200, CT201, RT232, RT233, RT234, RT235	0.3(X02)

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
24	46	TBT AR	2015/03/30	COMPAL	Vendor recommend add PD_RESET# cap	Add @CT199	0.3(X02)
25	47	TBT AR	2015/03/31	COMPAL	Give TBT_PWR_EN default value	Add pull down 10k(RT230)	0.3(X02)
26	*	X'tal	2015/04/01	COMPAL	X'tal EA	Change CE28, CE29 from 33p to 27p Change CH4, CH5 from 18p to 15p Change CH13, CH14 from 22p to 15p Change CV163, CV163 from 6.8p to 10p	0.3(X02)
27	49	TBT-AR	2015/04/02	COMPAL	AR PD TPS65982 Soft-start pin	Add CT202 0.22u	0.3(X02)
28	48	TBT-AR	2015/04/02	COMPAL	UT17 LDO source change from +Vbus_1 to +PP_HV	UT17 LDO source change from +Vbus_1 to +PP_HV	0.3(X02)
29	49	TBT-AR	2015/04/02	COMPAL	AR PD TPS65982 BUSPOWER_N change to VCC1V8D_TBTA_LDO	AR PD TPS65982 BUSPOWER_N change to VCC1V8D_TBTA_LDO	0.3(X02)
30	30	eDP	2015/04/02	COMPAL	IR CAM Pin Define	NC JIR1 Pin4	0.3(X02)
31	49	TBT-AR	2015/04/02	COMPAL	AR PD DEBUG	Add @RT236, RT237	0.3(X02)
32	47	TBT-AR	2015/04/02	COMPAL	Follow CRB0.998	change UT2.R13 to +3.3V_TBT_L,add CT203,CT204,LT2.change CT129,CT130,CT131 to 47uF,remove CT132	0.3(X02)
33	36	MEC5085	2015/04/03	COMPAL	Change Board ID to X02	Change RE79 to 33K ohm	0.3(X02)
34	20, 31	LAN SMBUS	2015/04/07	COMPAL	+3.3V_ALW_PCH and +3.3V_RUN backdrive EA	Pop RH67, RH77; Depop RC19, RC20	0.3(X02)
35	33	JSIM1	2015/04/07	COMPAL	ME CONN	Change footprint to T-SOL_5-991503004000-6_8P-T	0.3(X02)
36	33	JTHB1	2015/04/07	COMPAL	ME CONN	Change footprint to JAE_DX07B024XJ1R1100_24P-T	0.3(X02)
37	25	HDMI	2015/04/08	COMPAL	HDMI EA	Depop RV302, RV654, RV683-RV693; Pop LV3, LV6, LV9, LV12, RV207	0.3(X02)
38	25	HDMI	2015/04/08	COMPAL	HDMI EA	Remove RV654, RV683, RV684, RV685	0.3(X02)
39	48	TBT-AR	2015/04/09	COMPAL	AR LDO PWR EN ADD Cap	Add CT205 & Depop	0.3(X02)
40	26	PS8349B	2015/04/10	COMPAL	E-DOCK DP Port1 can't display	Add RV1102 CPU_DP1_AUXN_C 1M pull high +3.3V_RUN	0.3(X02)
41	21	GPU PWR EN	2015/04/13	COMPAL	GPU lost imtermittently	Pop RH346, Depop RH349	0.3(X02)
42	35, 51	GPU_PWR_LEVEL	2015/04/13	COMPAL	GPIO[A7] (GPU_PWR_LEVEL) need to seeting to PP, so we can de-pop RV113,RE304.	Depop RV113, RE304	0.3(X02)
43	41	DOCK_DP_HPD	2015/04/13	COMPAL	Depop DOCK_DP_HPD PD resistor for PS8349B/PS8348B internal PD.	Depop R268, R271	0.3(X02)

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
44	43	PAD & ME & LED	2015/04/14	COMPAL	JSIM1 CONN 2nd JAE	JSIM1 CONN 2nd JAE	0.4(X03)
45	33	SIM Detect	2015/04/14	COMPAL	Add SIM Detect for Hot Plug	Add RI31 for SIM Detect	0.4(X03)
46	35	EC	2015/04/20	COMPAL	Align PC U & H GPIO for EC common code	Add RE311 PU for AR_SMBUS_ALERT#	0.4(X03)
47	42	KB	2015/04/20	COMPAL	Add PU for I2C TP Module	Add RZ116, RZ117	0.4(X03)
48	26,27	Parade DeMux	2015/04/20	COMPAL	Vendor Parade suggest Parade DeMux ouput to Parade Redriver no need AUX PD/PU	Depop RV604, RV608, RV701, RV712	0.4(X03)
49	46	TBT AR	2015/04/23	COMPAL	For layout space	Remove RT149, RT166	0.4(X03)
50	46	TBT AR	2015/04/24	COMPAL	Follow Intel AR Reference	Change CT129~CT131 from 47u to 10u. Add CT206 10u	0.4(X03)
51	49	TBT AR	2015/04/29	COMPAL	CONN Impact Type C return loss	Change JTHB1 from Hybrid to SMD type	0.4(X03)
52	42	KB_TP	2015/05/05	COMPAL	TP function sometimes lag	CZ30, CZ31 change from 10p to 330p improve signal quality	0.5(X03)
53	40	USB Charger	2015/05/05	COMPAL	Insert USB HDD Shut Down Issue	Add CI32 Poly 150U	0.5(X03)
54	36	MEC5085	2015/05/05	COMPAL	AR no function at AC S5	UPD_GPU_SMBDAT/UPD_GPU_SMBCLK PU change from +3.3V_RUN to +3.3V_ALW	0.5(X03)
55	38	M2280	2015/05/26	COMPAL	Insert NVME SATA LED no function	JNGFF3.10 connected to PCH_SATA_LED#	0.5(X03)
56	35	EC	2015/05/26	COMPAL	For Type-C function	1. Add 5048 GPIO(PROCHOT_GATE) and reserve RE313 pull high 2. Add 5048(PD_ACE_DET#) for AR config? and pull high on RE312, PD ON RE314	0.5(X03)
57	22	PCH(7/9)	2015/06/01	COMPAL	5.76GHz noise observed on thie Wi-Fi antenna	1.Add RC349 and CC310 on VCCHDA 2.Add RC350 and CC311 on VCCAPLL_1P0	0.5(X03)
58	47	TBT AR	2015/06/01	COMPAL	AR IC PWR different by version	Add LT3	0.5(X03)
59	47	TBT AR	2015/06/09	COMPAL	PWR Consumption measurement	Add PJP41, PJP42	0.5(X03)
60	47	TBT AR	2015/06/09	COMPAL	ESD	Reserve DT25~DT28	0.5(X03)
61	51	GPU	2015/06/10	COMPAL	For AR SMBUS	Depop QV14	0.5(X03)
62	25	HDMI	2015/06/11	COMPAL	Remove HDMI choke	Add RV683, RV684, RV685, RV654; Pop RV686, RV687, RV688, RV689, RV690, RV691, RV692, RV693; Depop LV3, LV6, LV9, LV12; Change RV303 from 4.99K to 4.02K	0.5(X03)
63	26, 27	*	2015/06/11	COMPAL	Dell recommend	Change RE312 from 100K to 330K Reserve CV1104, CV1105 for SW1_DP1_HPD & SW2_DP1_HPD	0.5(X03)
64	35	EC	2015/06/11	COMPAL	PROCHOT_GATE default PD	Add RE315 PD 100K	0.5(X03)
65	36	EC	2015/06/11	COMPAL	Win PE Global Reset Issue	Add QE11	0.6(X04)
66	36	EC	2015/06/11	COMPAL	Intel Sequence Fail	Add UE5	0.6(X04)

Compal Electronics, Inc.

Title: EE P.I.R (3/3)

Size | Document Number: LA-C841P | Rev: 0.2

Date: Tuesday, September 08, 2015 | Sheet 78 of 78

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
67	37	TPM	2015/07/07	COMPAL	Deep Sleep TPM Fail	Change TPM IC VSB from +3.3V_ALW_PCH to +3.3V_ALW	1.0(A00)
68	30	eDP	2015/07/20	COMPAL	Material shortage	Changed DV1, DV2 and DV3 from SCS00003800 to SCS00006400	1.0(A00)
69	37	TPM	2015/07/20	COMPAL	Change TPM FW to 1.2 version	Changed UZ12 from SA000082D00 to SA00008EL20	1.0(A00)
70	40	HW	2015/07/20	COMPAL	For Sourcer request	CI32 change from SGA00002N80 to SGA00004E10	1.0(A00)
71	36	MEC5085	2015/07/20	COMPAL	change BID to A00	change RE79 to 1K ohm.	1.0(A00)
72	11	CPU(6/8)	2015/08/03	COMPAL	Follow Intel DG1.5	Add load switch (UZ26) control(S3) to +VCCPLL_OC power rail	1.0(A00)
73	22	PCH(7/9)	2015/08/03	COMPAL	5.76GHz noise observed on thie Wi-Fi antenna	Change RC349 and RC350 to LC1 and LC2	1.0(A00)
74	53	GPU	2015/08/03	COMPAL	+VGA_PCIE cause +1.0V_PRIM droop	Change UV27 to Trise 0.5ms part SA00007T400	1.0(A00)
75	11	CPU	2015/08/11	COMPAL	Folow intel DG1.5	Add UC9, CZ115	1.0(A00)