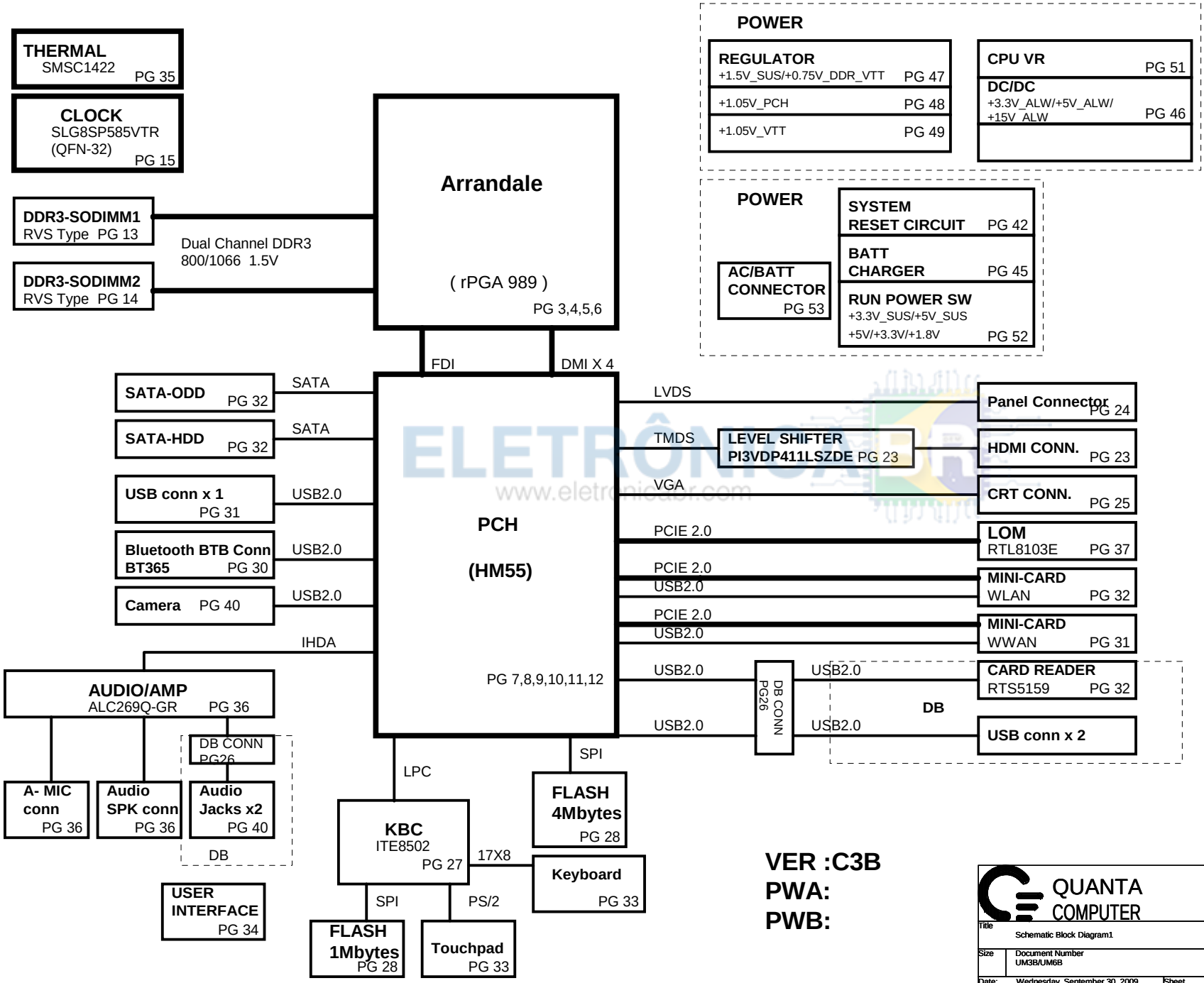
UM3B/UM6B SYSTEM BLOCK DIAGRAM



QUANTA COMPUTER

Title	Schematic Block Diagram1	
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Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,30,45,46,47,48,49,50,51	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	08,11,29,30	RTC		S0~S5
+5V_ALW2	+5V	37,46,52,53	LARGE POWER	MAIN POWER	S0~S5
+5V_ALW	+5V	13,33,44,46,47,48,49,50,51,52	LARGE POWER	ALW_ON	S0~S5
+3.3V_ALW	+3.3V	29,30,35,36,37,42,44,45,46,47,51,52,53	8051 POWER	3.3V_ALW_ON	S0~S5
+5V_SUS	+5V	11,33,34,37,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	07,08,09,10,11,13,14,19,24,28,29,37,41,42,44 ,48,49,50,52	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.5V	03,05,13,14,47,50,52	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	13,14,47,52	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	11,18,24,25,35,36,38,39,40,51,52	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,7,8,9,10,11,13,14,15,17,24,25,26,28,29,30 ,31,32,33,35,37,38,39,40,41,42,46,51,52,60	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	05,11,44,52	SDVO POWER	RUN_ON	
+1.05V_VTT	+1.1V	03,05,10,11,49,60	CPU POWER	RUN_ON	
+1.5V_RUN	+1.5V	11,28,31,32,52	Express Card/Min Card	RUN_ON	
+5V_HDD	+5V	35	HDD Power	HDDC_EN	
+1.05V_PCH	+1.05V	08,09,11,15,48	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.77V	05,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	24	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	35	MOD Power	MODC_EN	

GND PLANE	PAGE	DESCRIPTION
GND	ALL	

QUANTA COMPUTER

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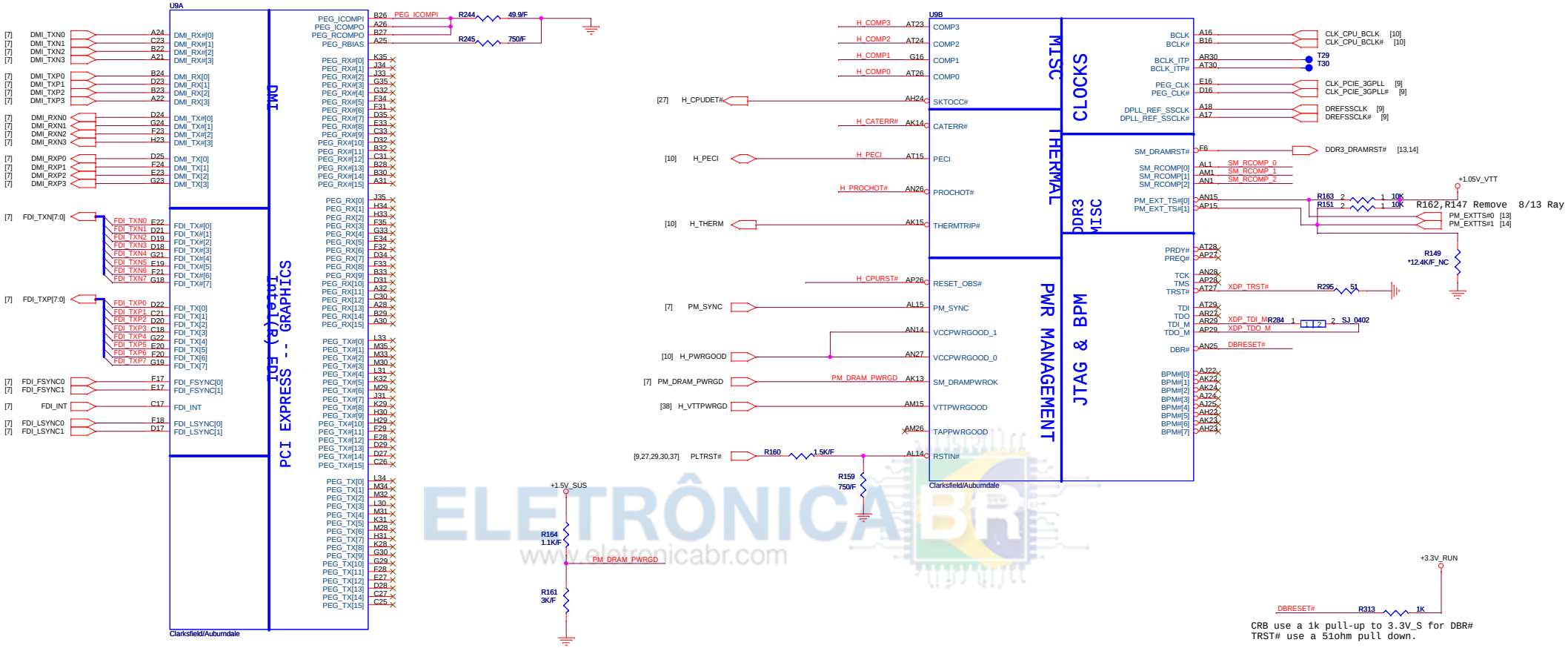
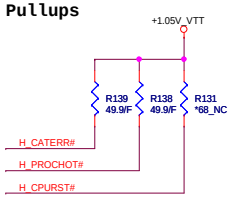
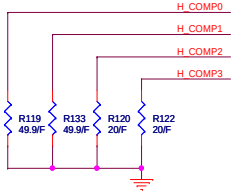


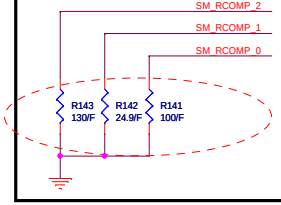
Processor Pullups



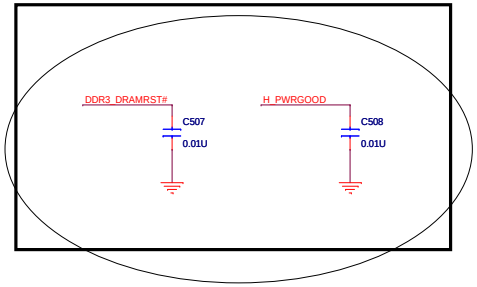
Processor Compensation Signals



DDR3 Compensation Signals



Layout Note: Place these resistors near Processor



QUANTA COMPUTER		
Title: AUBURNDA 1/4		
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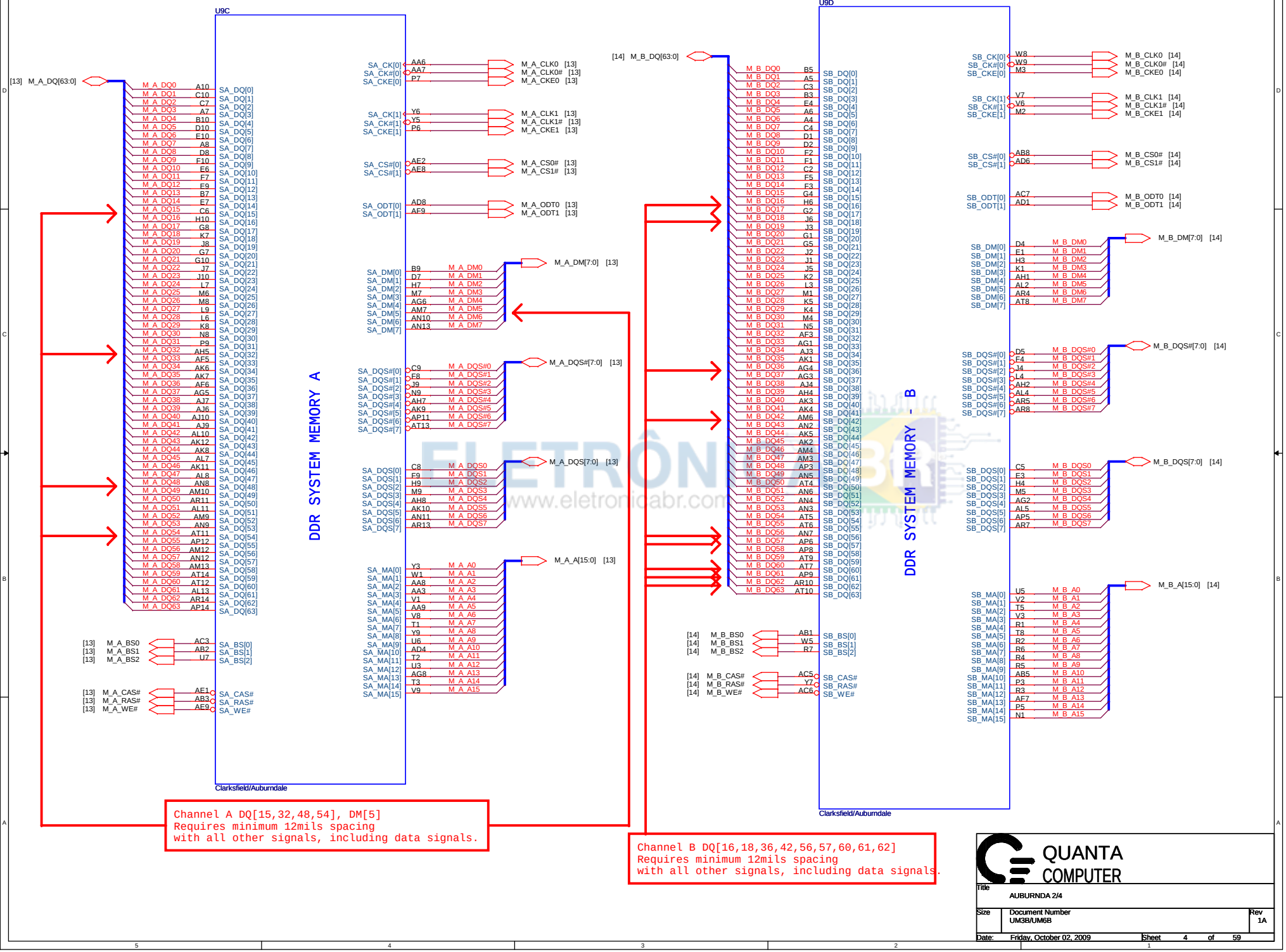
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



QUANTA COMPUTER

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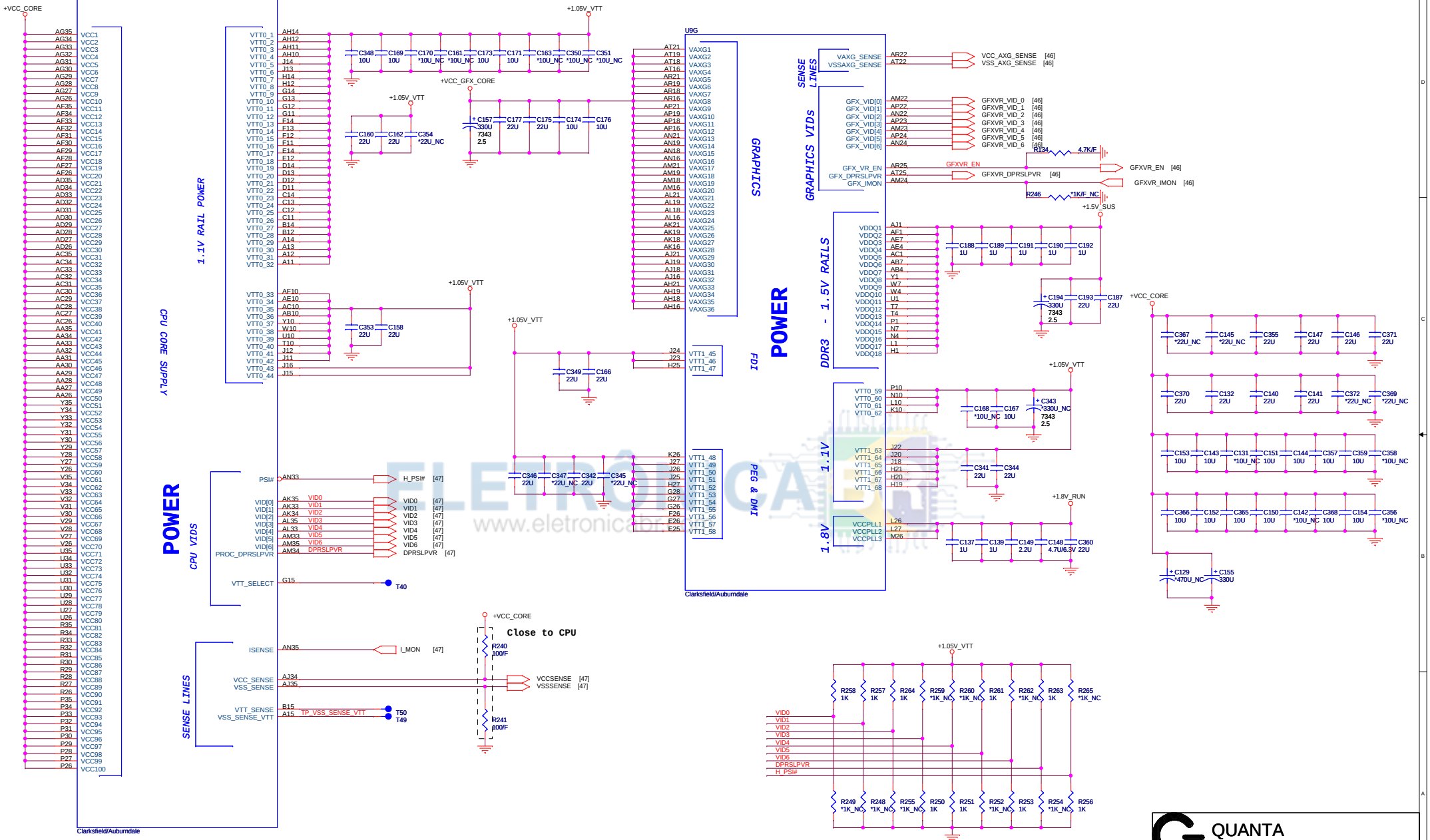
CPU Core Power

AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)



AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

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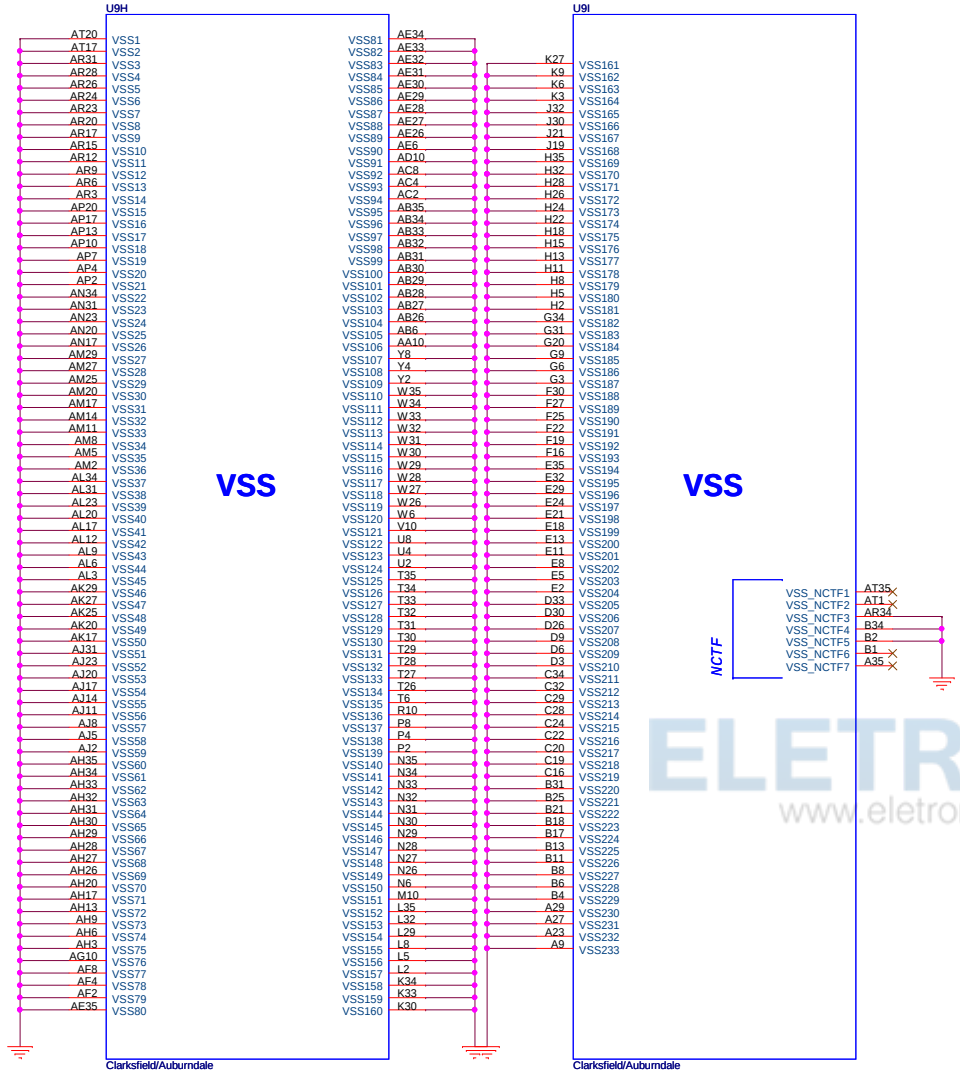
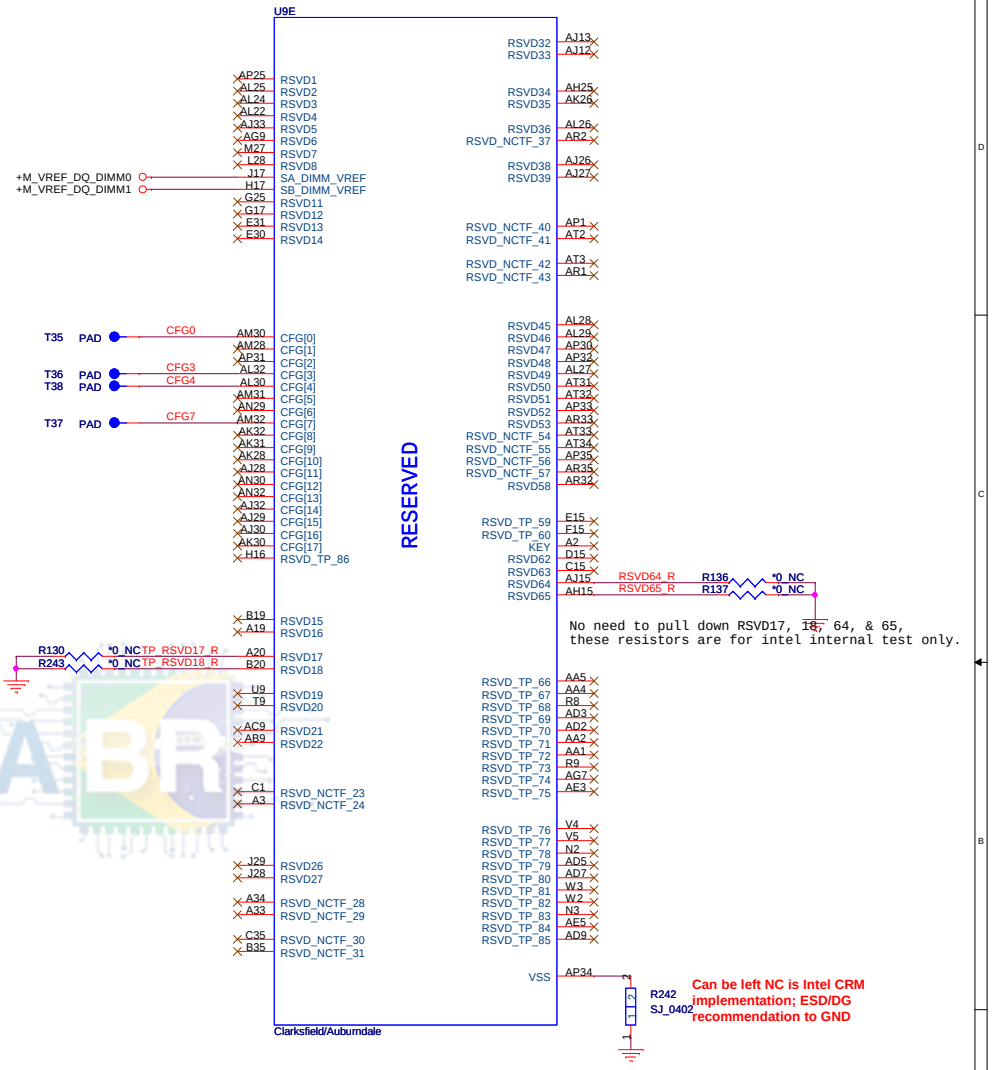
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

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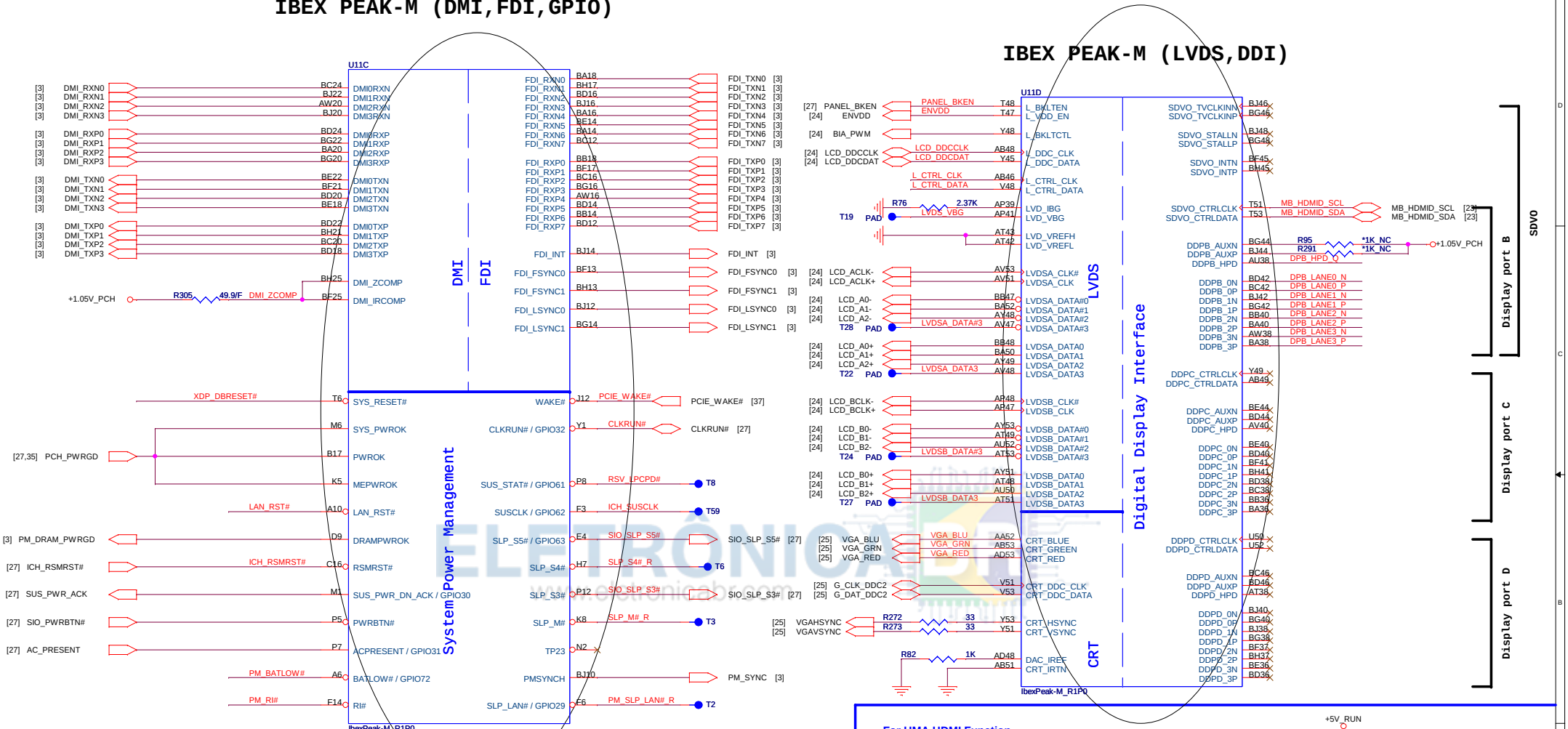
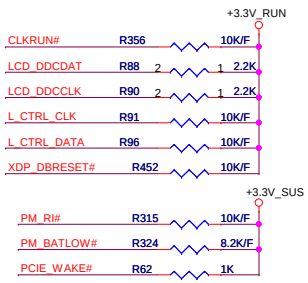
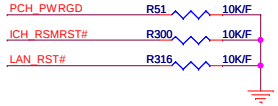
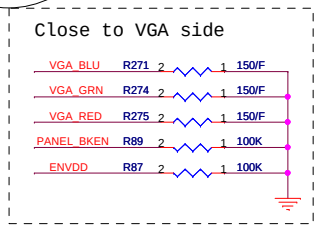
IBEX PEAK-M (DMI,FDI,GPIO)

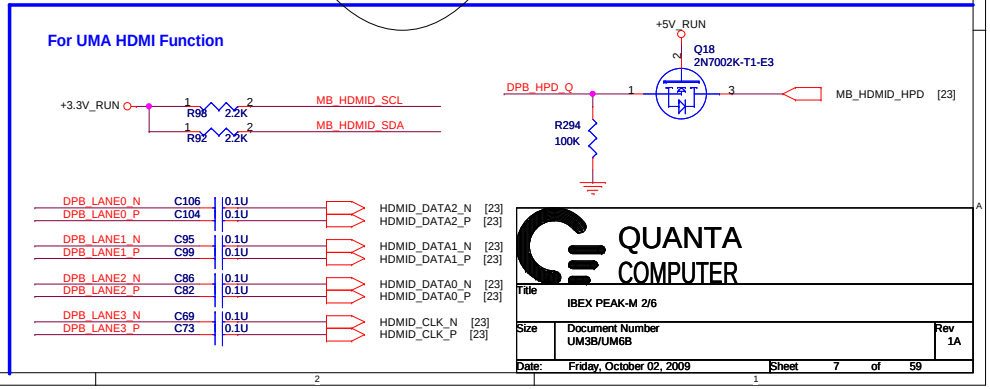
IBEX PEAK-M (LVDS,DDI)











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Title	IBEX PEAK-M 2/6	
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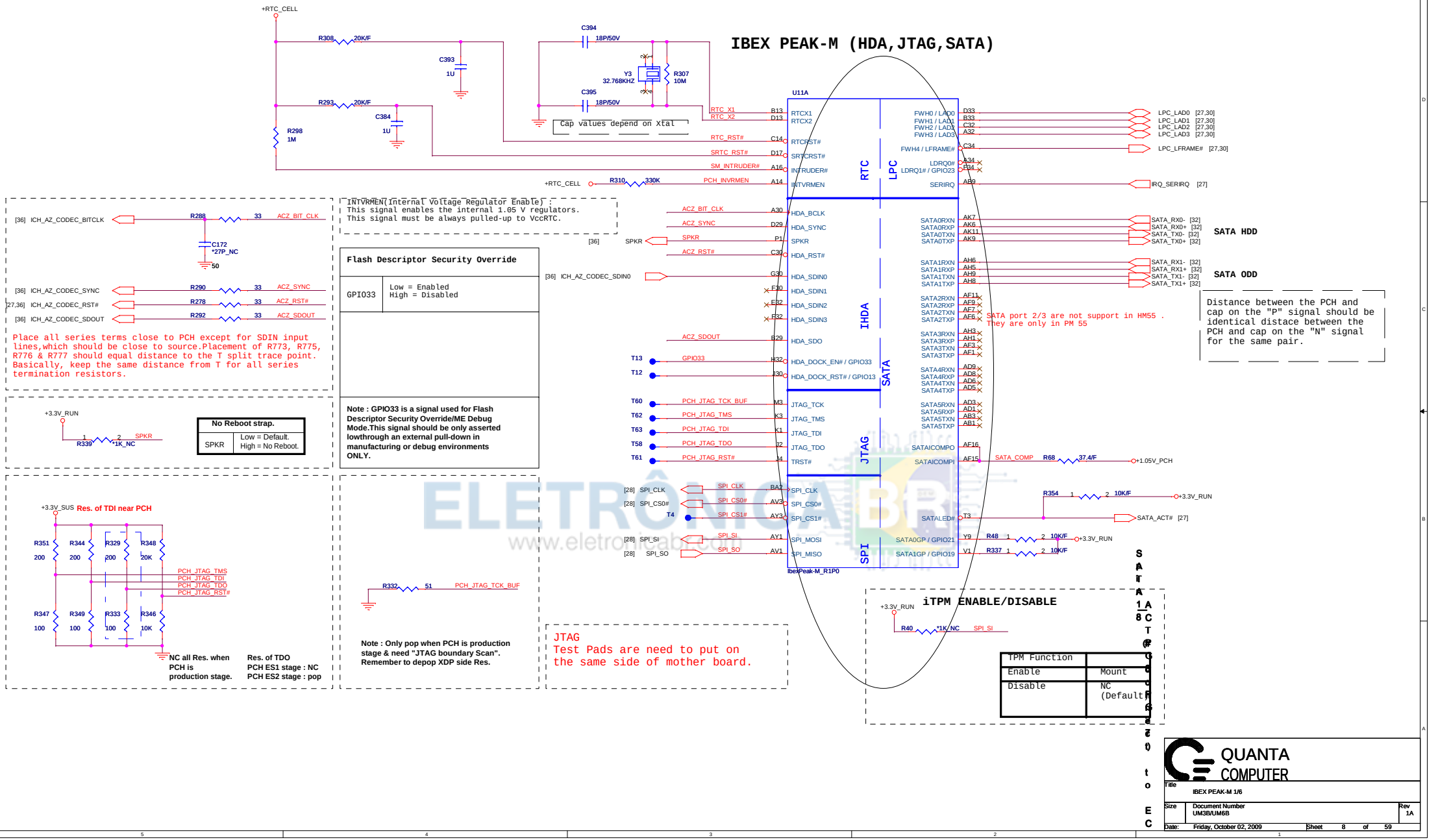
IBEX PEAK-M (HDA,JTAG,SATA)



INTVRMEN(Internal Voltage Regulator Enable) :
This signal enables the internal 1.05 V regulators.
This signal must be always pulled-up to VccRTC.

Distance between the PCH and cap on the "P" signal should be identical distace between the PCH and cap on the "N" signal for the same pair.

Place all series terms close to PCH except for SDIN input lines,which should be close to source.Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

Flash Descriptor Security Override

GPIO33	Low = Enabled High = Disabled

Note : GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode.This signal should be only asserted lowthrough an external pull-down in manufacturing or debug environments ONLY.

+3.3V_RUN
R339 *1K_NC SPKR

No Reboot strap.

SPKR	Low = Default. High = No Reboot.

+3.3V_SUS **Res. of TDI near PCH**

R351 200 R344 200 R329 200 R348 20K
PCH_JTAG_TMS
PCH_JTAG_TDI
PCH_JTAG_TDO
PCH_JTAG_RST#
R347 100 R349 100 R333 100 R346 10K

NC all Res. when PCH is production stage.

Res. of TDO
PCH ES1 stage : NC
PCH ES2 stage : pop

R332 51 PCH_JTAG_TCK_BUF

Note : Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.

JTAG
Test Pads are need to put on the same side of mother board.

iTPM ENABLE/DISABLE

+3.3V_RUN R40 *1K_NC SPI_SI

TPM Function	
Enable	Mount
Disable	NC (Default)

SATA1ACTP (Pull to EC)

QUANTA COMPUTER

Title	IBEX PEAK-M 1/6	
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IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (PCI-E,SMBUS,CLK)

Place TX DC blocking caps close PCH.

U11E

U11B

PCI

NVRAM

USB

PCI-E*

SMBus

Controller Link

PEG

From CLK BUFFER

Clock Flex

MiniWWAN

MiniWLAN

LOM

10/100 LOM

Right Side pair to DB

Right Side pair to DB

Left Side pair

Left Side pair for 17"

Mini Card (WLAN)

Mini Card (WWAN)

USB port 6/7 are not support in HM55 .
They are only in PM 55

Mini Card (WPAN)

Express Card

Camera

Card reader

Note : place these resistors near to PCIe Slots

PCIRST#:
DG(V1.0) P277
Can be left unconnected.

PAR:
SC(V1.0) P36
Can be left unconnected
if not using PCI.

PME:
DG(V1.0) P277
Can be left unconnected.

0214

CLKOUT_PCI[0..4]:
22 ohm series resistor is recommend
(single & double load) on PDG v1.1

OC0#~OC7#:
DG(V1.0)P214
Pin Default Port Mapping
OC0# Port0,Port1
OC1# Port2,Port3

CLKOUT_PEG_A_P/N, CLKOUT_PEG_B_P/N,
CLKOUT_DMI_P/N,support GEN-1 and GEN-2

CLKOUTFLEX3:
EDS(V1.0) :support 48MHz
33MHz and 14.31818MHz.

CLKOUTFLEX[0..3]:
PDG v1.1: 22 ohm series resistor is
recommend (PCI & non PCI routing,
single & double load)

SML0CLK/SML0DATA:
DG(V1.1) P255: The 82577 SMBus signals
(SMB_DATA and SMB_CLK) cannot be connected to any other devices other than the PCH. Connect the SMB_DATA and SMB_CLK pins to the PCH SML0DATA and SML0CLK pins, respectively.

Reserve capacitor pads for improving WWAN.

PCIE Clock Request

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +V3.3A.PCIECLKRQ{1,2} should have a 10K pull-up to +3.3S

Non-iAMT

Add Buffers as needed for Loading and fanout concerns.

ibexPeak-M_R1P0

ibexPeak-M_R1P0

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Title	IBEX PEAK-M 3/6
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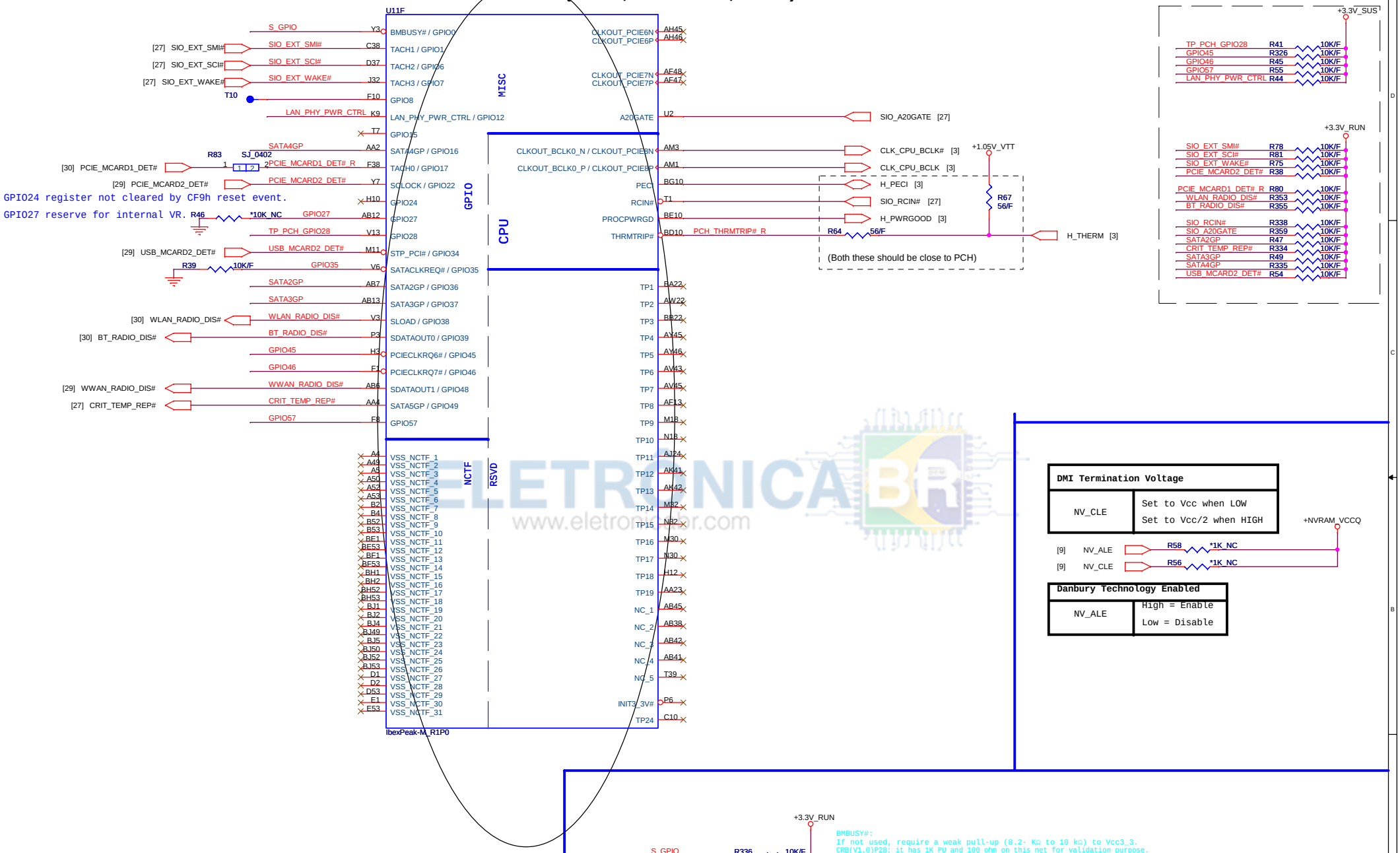
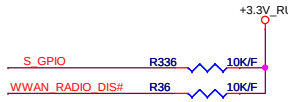
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable



BMBUSY#:
If not used, require a weak pull-up (8.2- KΩ to 10 kΩ) to Vcc3_3.
CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

BMBUSY#:(Intel feedback)
Follow CRB checklist, 1K is
for intel BIOS validation purpose.

WWAN_RADIO_DIS#	1-X High = Strong (Default)

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Title	IBEX PEAK-M 4/6	
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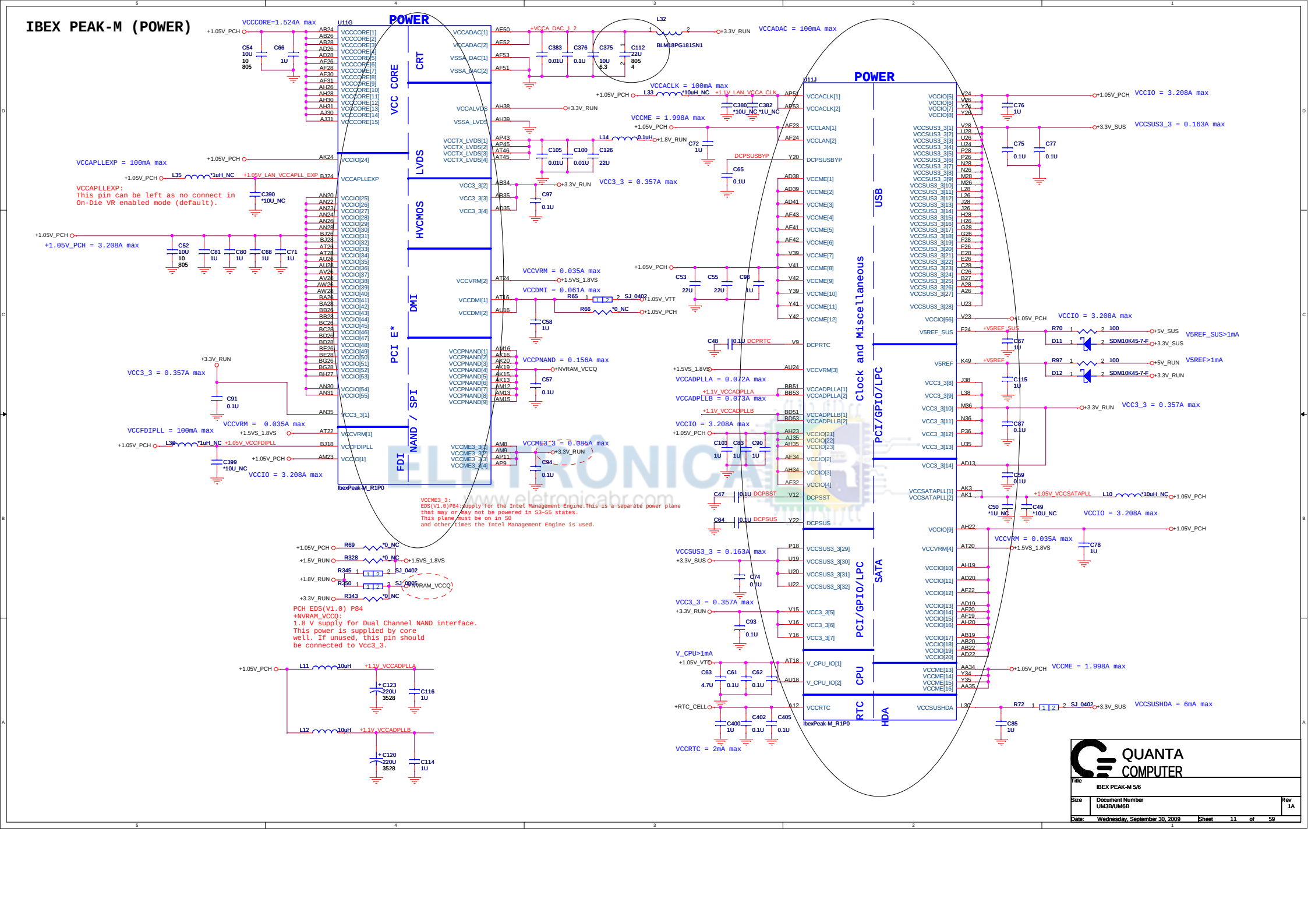
IBEX PEAK-M (POWER)



Title	IBEX PEAK-M 5/6
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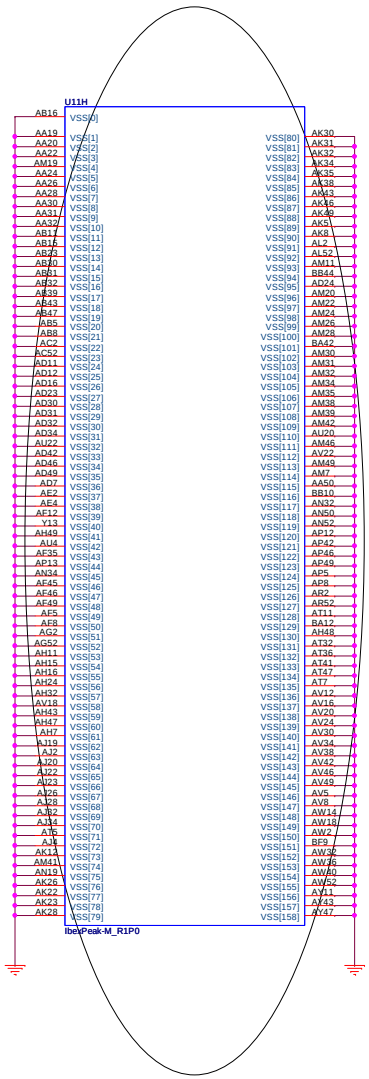
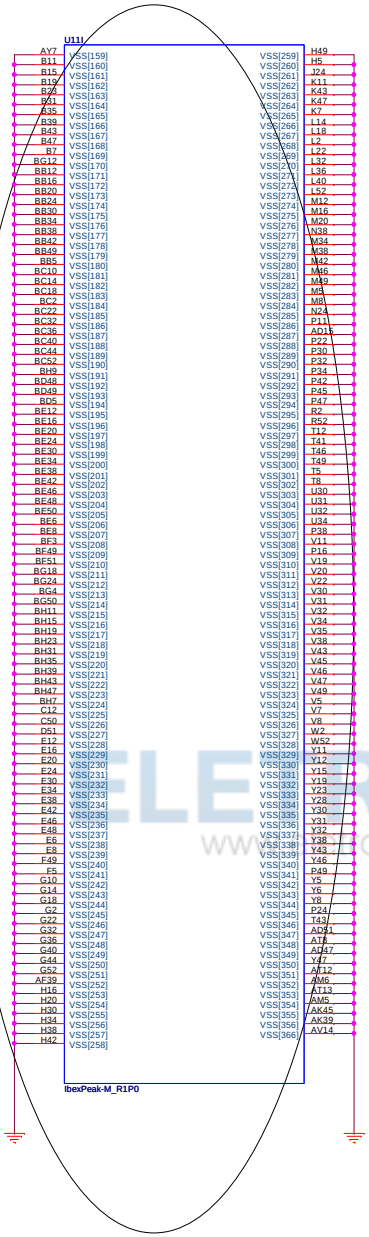
IBEX PEAK-M (GND)





QUANTA COMPUTER

Title	IBEX PEAK-M 6/6	
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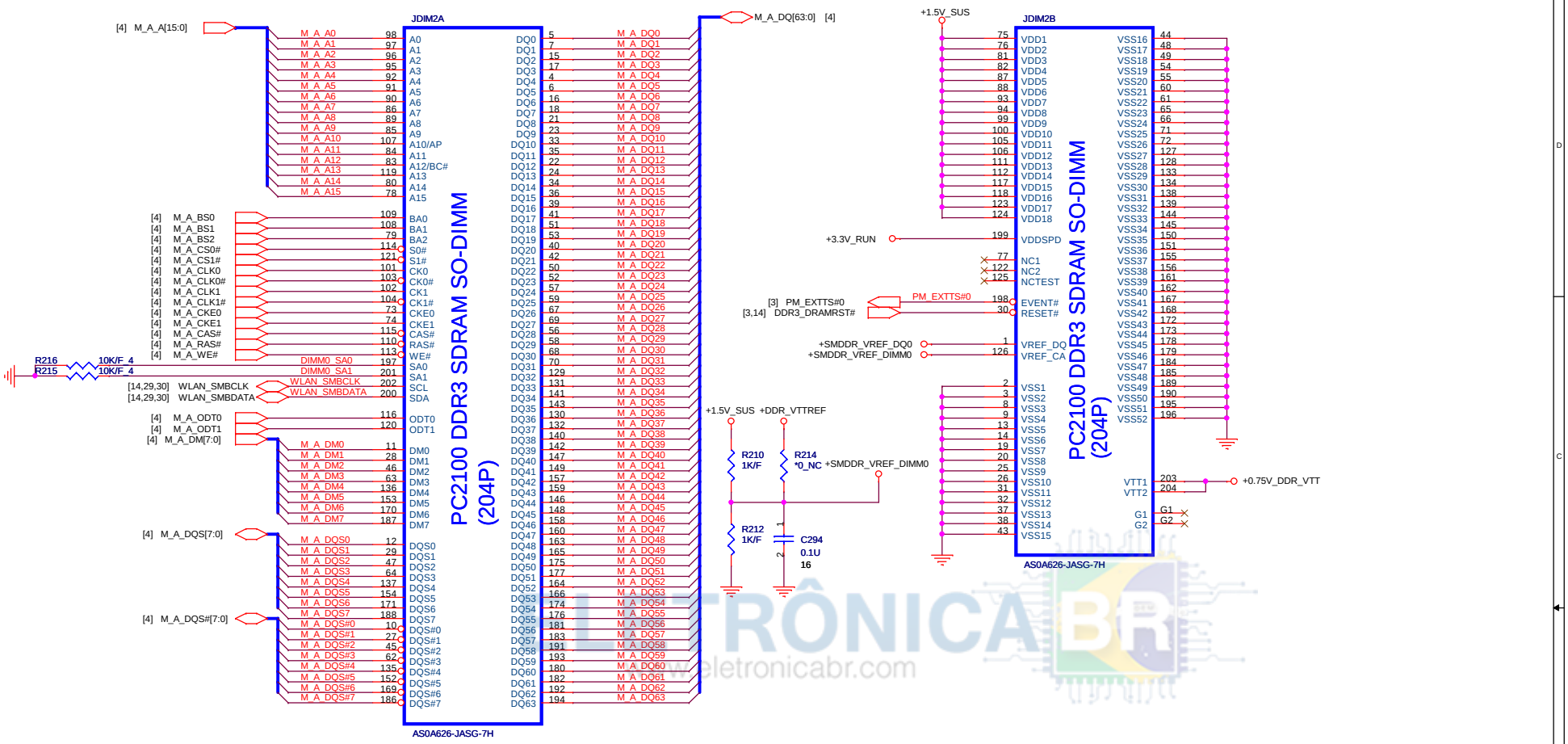

QUANTA COMPUTER

Title	DDR3 DIMM-0	
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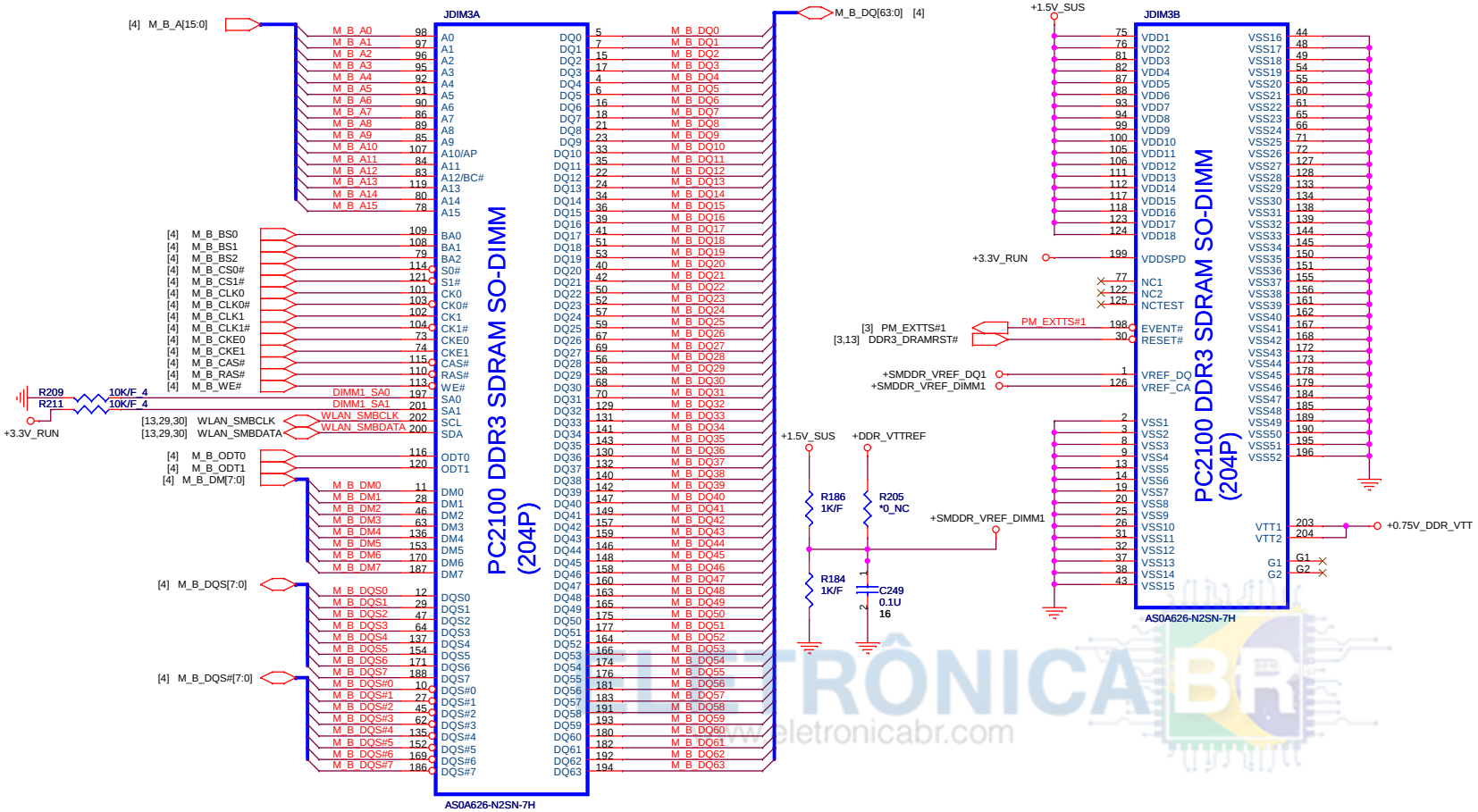
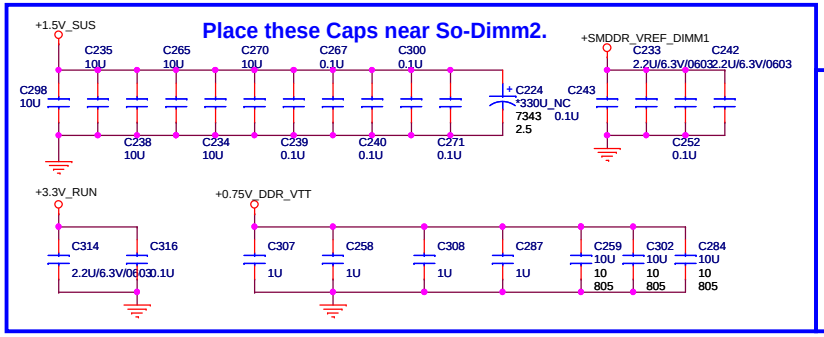
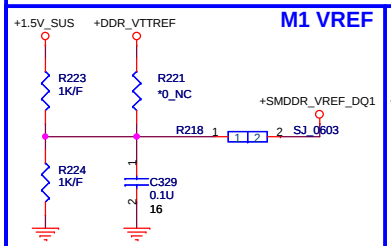


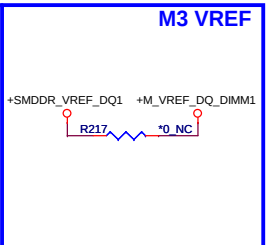
Place these Caps near So-Dimm2.



M1 VREF



M3 VREF



QUANTA COMPUTER		
Title: DDR3 DIMM-1		
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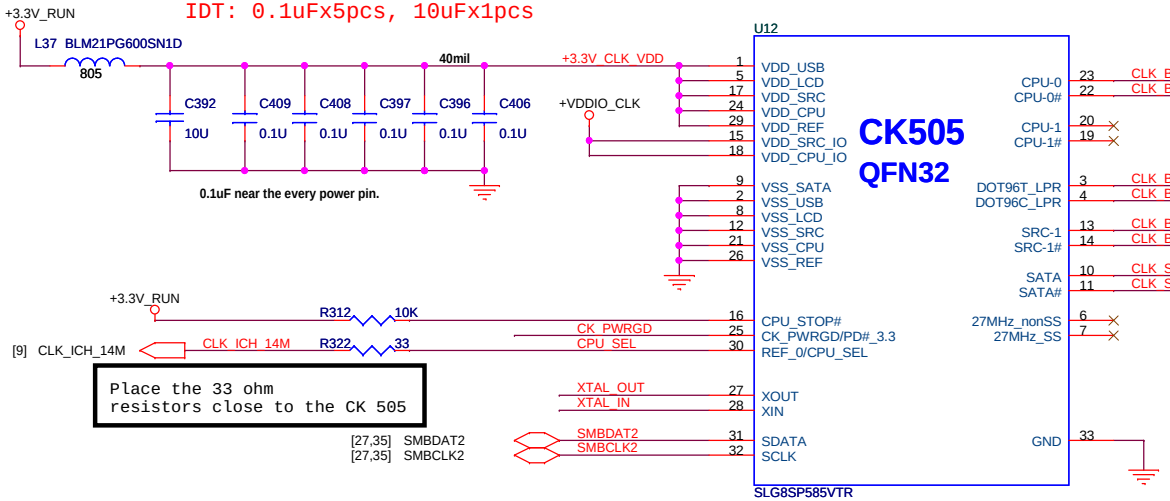
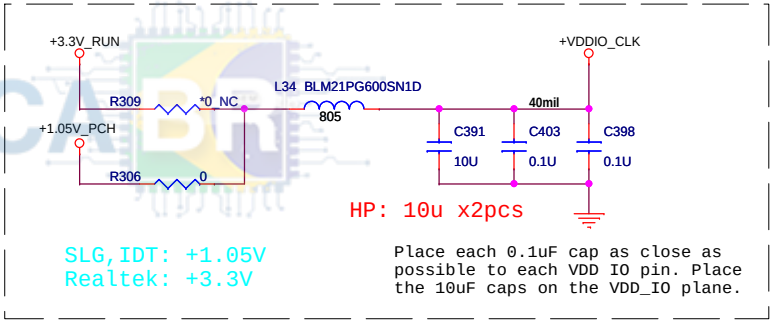
Realtek: 0.1uFx6pcs, 22uFx1pcs
IDT: 0.1uFx5pcs, 10uFx1pcs



Place within 0.5" of CLKGEN

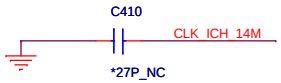
Place the 33 ohm resistors close to the CK 505

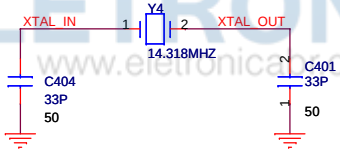
Realtek: 0.1uFx3pcs, 22uFx1pcs
IDT: 0.1uFx2pcs, 10uFx1pcs

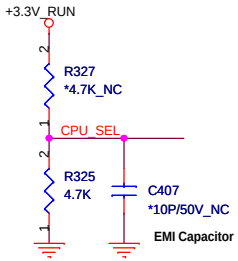


+VDDIO_CLK:
SLG date sheet (V0.2) P15: Min 1.05V,Max3.465V.
Realtek date sheet(V1.2) P11: Min 1.05V,Max 3.3V.
IDT date sheet(V0.7) P10: Min 0.9975V,Max 3.465V.

Add capacitor pads for improving WWAN.

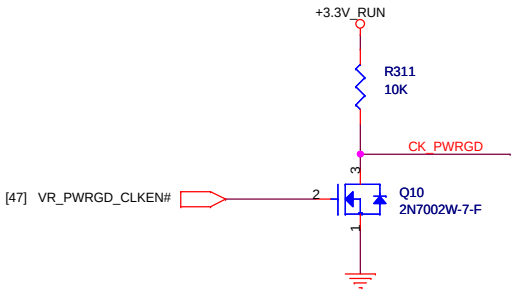






PIN 30	CPU_0	CPU_1
0(default)	133MHz	133MHz
1(0.7V-1.5V)	100MHz	100MHz

CPU_SEL:
SLG date sheet (V0.2) P15:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
Realtek date sheet(V1.2) P11:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
IDT date sheet(V0.7) P10:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.



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QUANTA COMPUTER

Title	VGA-M92-XT (PCIe)	
Size	Document Number UM3B/UM6B	Rev 1A
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QUANTA COMPUTER

Title	VGA-M92-XT (PCIe)	
Size	Document Number UM3B/UM6B	Rev 1A
Date: Wednesday, September 30, 2009	Sheet 19 of 59	

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QUANTA COMPUTER

Title	VGA-M92-S (VRAM)	
Size	Document Number UM3B/UM6B	Rev 1A
Date: Wednesday, September 30, 2009	Sheet 20 of 59	

BLANK PAGE FOR PAGE NUMBER SAME AS DISCRETE

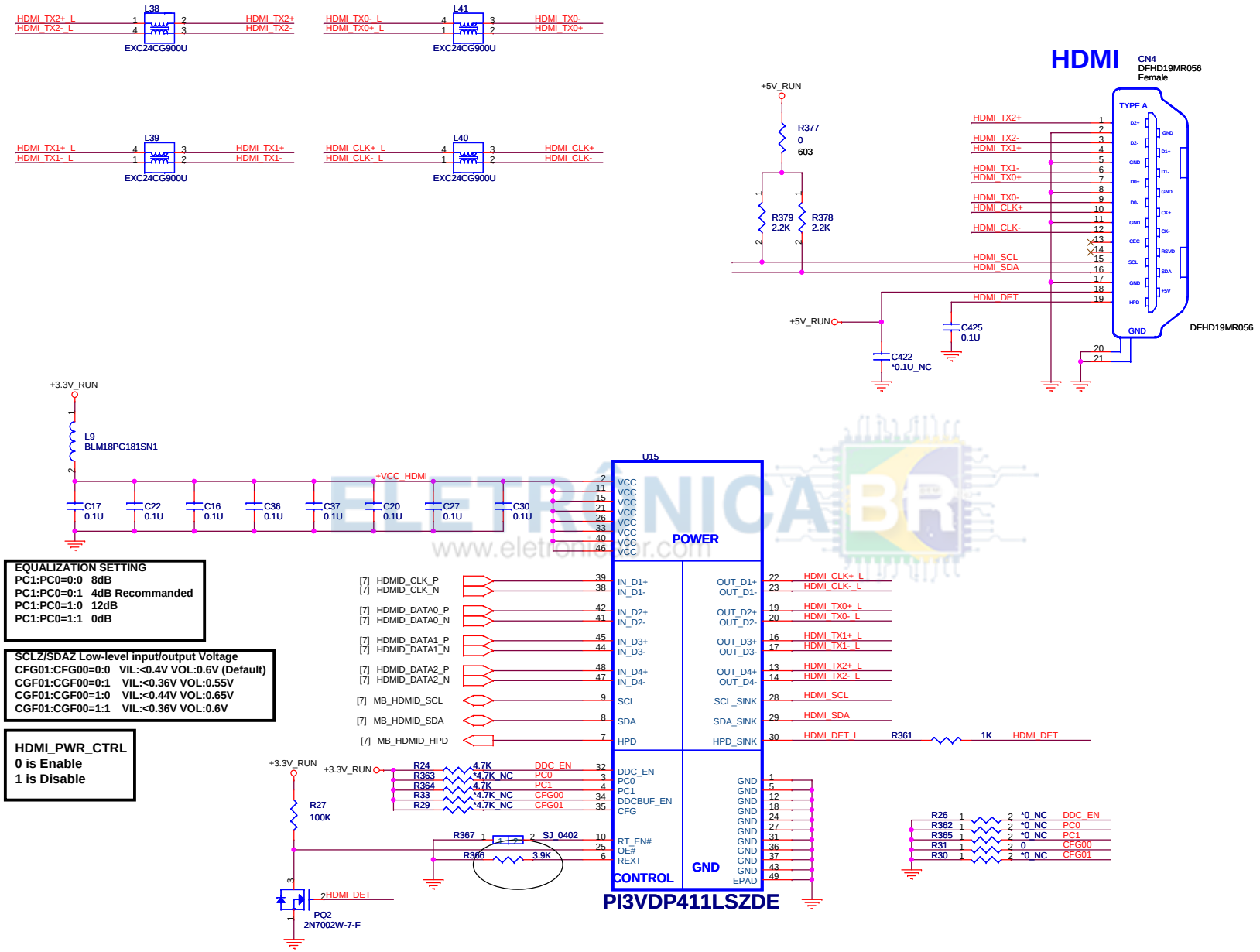
QUANTA COMPUTER

Title	VGA-M92-XT (PCIe)	
Size	Document Number UM3B/UM6B	Rev 1A
Date: Wednesday, September 30, 2009	Sheet 21 of 59	

BLANK PAGE FOR PAGE NUMBER SAME AS DISCRETE

QUANTA COMPUTER

Title	VGA-M92-XT (PCIe)	
Size	Document Number UM3B/UM6B	Rev 1A
Date: Wednesday, September 30, 2009	Sheet 22 of 59	


HDMI
CN4
DFHD19MR056
Female
TYPE A
DFHD19MR056
L38
L39
L40
L41
EXC24CG900U
HDMI_TX2+_L
HDMI_TX2-_L
HDMI_TX2+
HDMI_TX2-
HDMI_TX1+_L
HDMI_TX1-_L
HDMI_TX1+
HDMI_TX1-
HDMI_TX0-_L
HDMI_TX0+_L
HDMI_TX0-
HDMI_TX0+
HDMI_CLK+_L
HDMI_CLK-_L
HDMI_CLK+
HDMI_CLK-
+5V_RUN
R377
0
603
R379
2.2K
R378
2.2K
HDMI_SCL
HDMI_SDA
HDMI_DET
C425
0.1U
C422
*0.1U_NC
GND
+3.3V_RUN
L9
BLM18PG181SN1
+VCC_HDMI
C17
0.1U
C22
0.1U
C16
0.1U
C36
0.1U
C37
0.1U
C20
0.1U
C27
0.1U
C30
0.1U
U15
POWER
VCC
GND
EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB
SCLZ/SDAZ Low-level input/output Voltage
CFG01:CFG00=0:0 VIL:<0.4V VOL:0.6V (Default)
CGF01:CGF00=0:1 VIL:<0.36V VOL:0.55V
CGF01:CGF00=1:0 VIL:<0.44V VOL:0.65V
CGF01:CGF00=1:1 VIL:<0.36V VOL:0.6V
HDMI_PWR_CTRL
0 is Enable
1 is Disable
[7] HDMID_CLK_P
[7] HDMID_CLK_N
[7] HDMID_DATA0_P
[7] HDMID_DATA0_N
[7] HDMID_DATA1_P
[7] HDMID_DATA1_N
[7] HDMID_DATA2_P
[7] HDMID_DATA2_N
[7] MB_HDMID_SCL
[7] MB_HDMID_SDA
[7] MB_HDMID_HPD
IN_D1+
IN_D1-
IN_D2+
IN_D2-
IN_D3+
IN_D3-
IN_D4+
IN_D4-
SCL
SDA
HPD
OUT_D1+
OUT_D1-
OUT_D2+
OUT_D2-
OUT_D3+
OUT_D3-
OUT_D4+
OUT_D4-
SCL_SINK
SDA_SINK
HPD_SINK
HDMI_CLK+_L
HDMI_CLK-_L
HDMI_TX0+_L
HDMI_TX0-_L
HDMI_TX1+_L
HDMI_TX1-_L
HDMI_TX2+_L
HDMI_TX2-_L
HDMI_SCL
HDMI_SDA
HDMI_DET_L
R361
1K
HDMI_DET
DDC_EN
PC0
PC1
DDCBUF_EN
CFG
RT_EN#
OE#
REXT
CONTROL
EPAD
R24
4.7K
R363
*4.7K_NC
R364
4.7K
R33
*4.7K_NC
R29
*4.7K_NC
CFG00
CFG01
R27
100K
R367
SJ_0402
R366
3.9K
PQ2
2N7002W-7-F
R26
R362
R365
R31
R30
*0_NC
0
PI3VDP411LSZDE
QUANTA
COMPUTER
Title
HDMI
Size
Document Number
UM3B/UM6B
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1A
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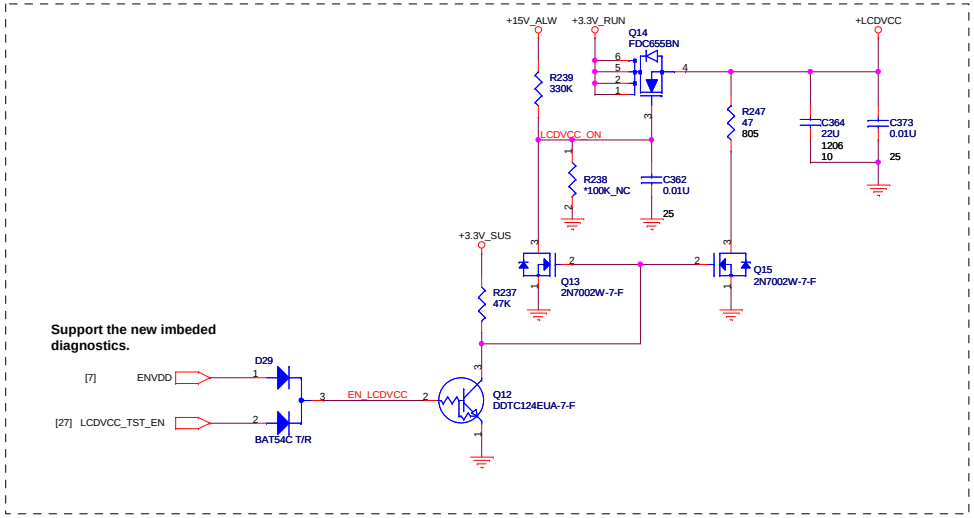
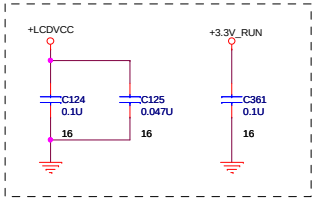
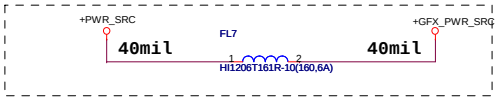
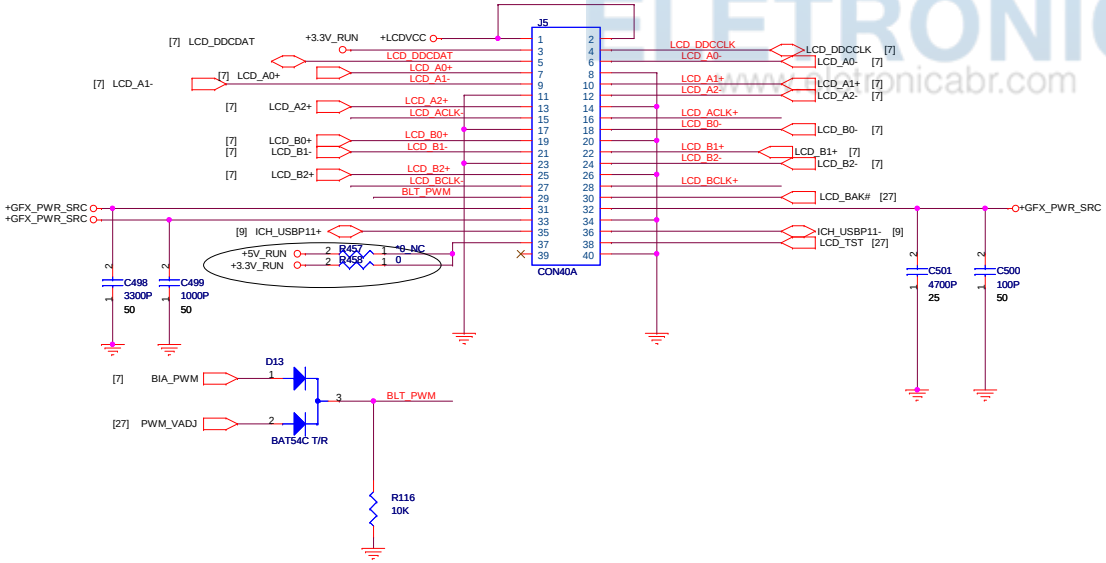
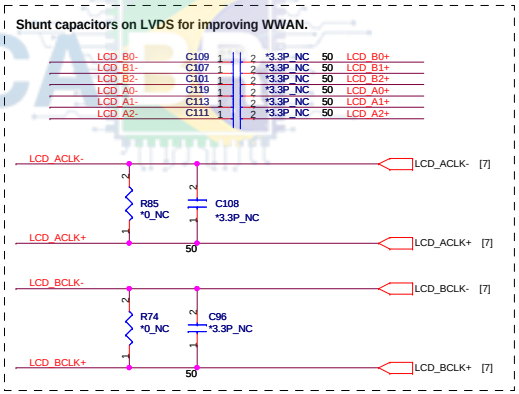
23
of
59











QUANTA COMPUTER

Title	LCD CONN & CK-SSCD	
Size	Document Number UM3B/UM6B	Rev 1A
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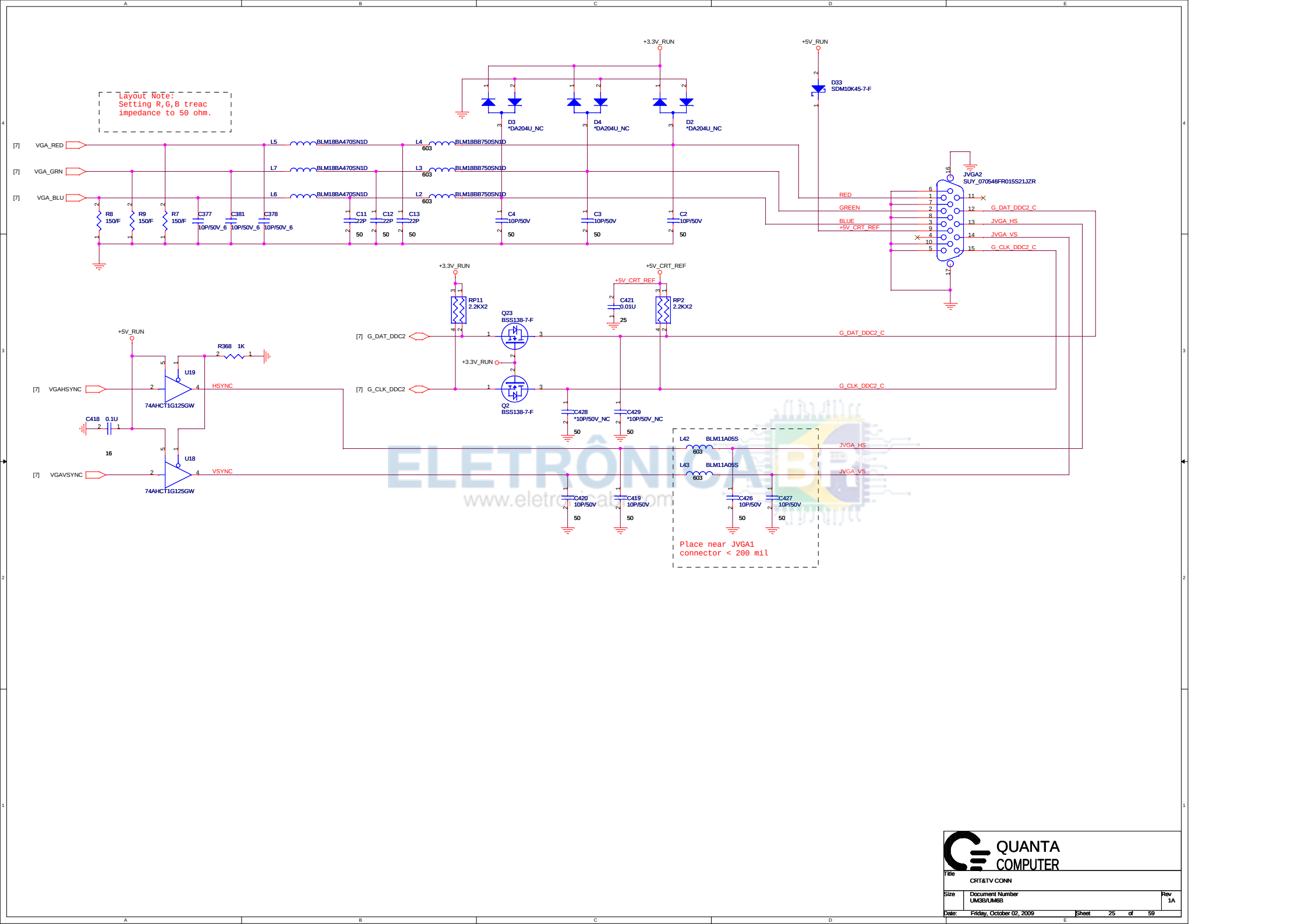

QUANTA COMPUTER

Title	CRT&TV CONN	
Size	Document Number UM3B/UM6B	Rev 1A
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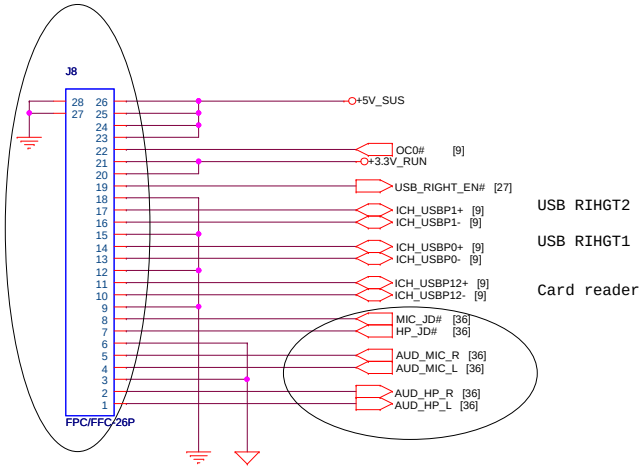
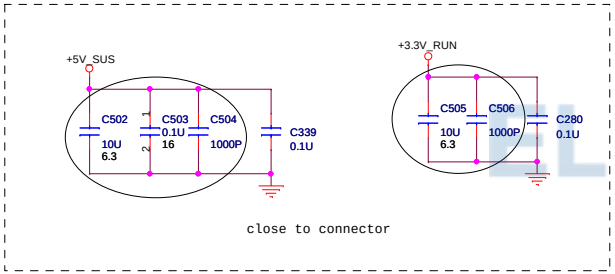


USB RIHGT2

USB RIHGT1

Card reader



QUANTA COMPUTER

Title	DB(USB PORT/CARD READER/AUDIO JACK) CONN	
Size	Document Number UM3B/UM6B	Rev 1A
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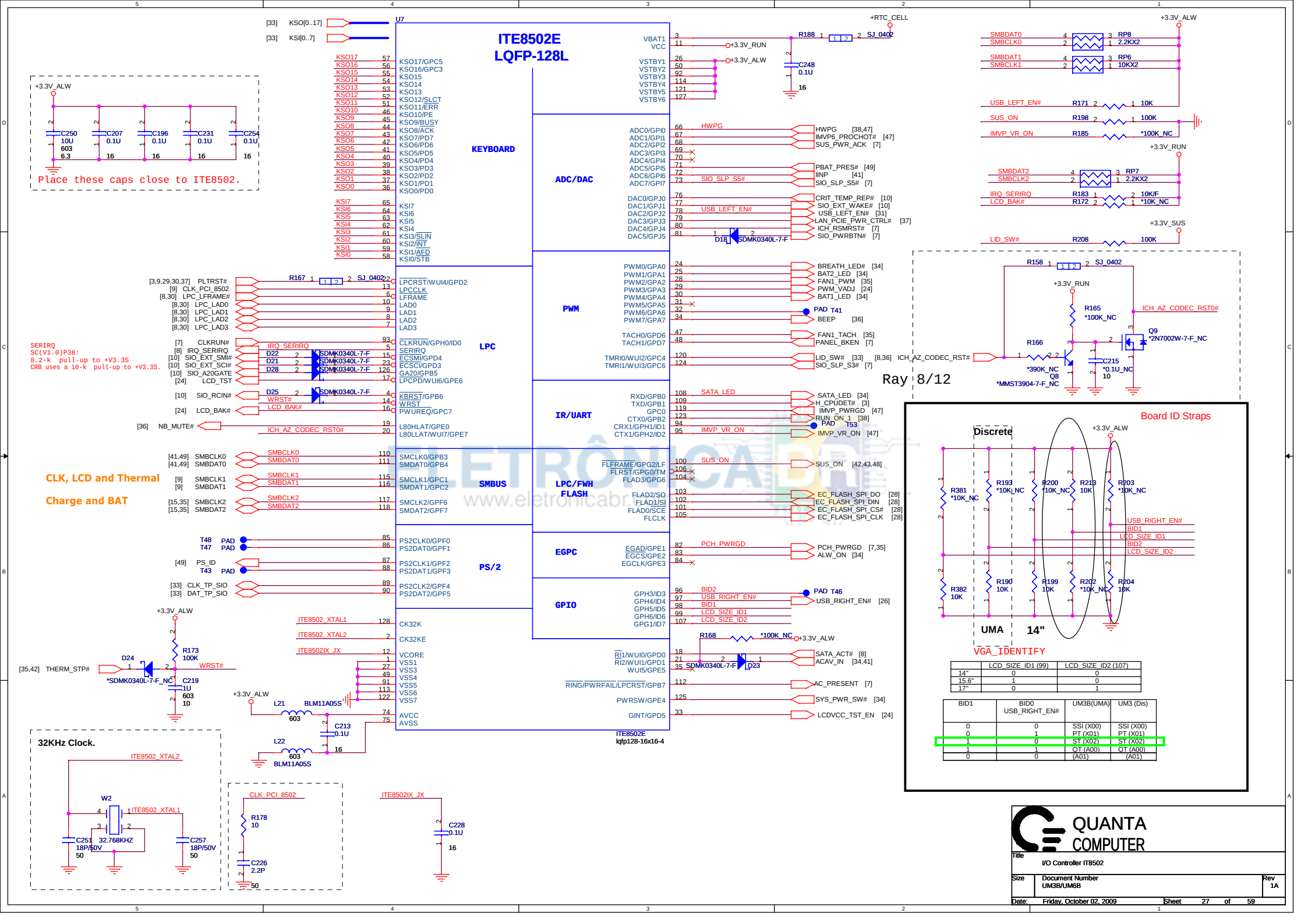
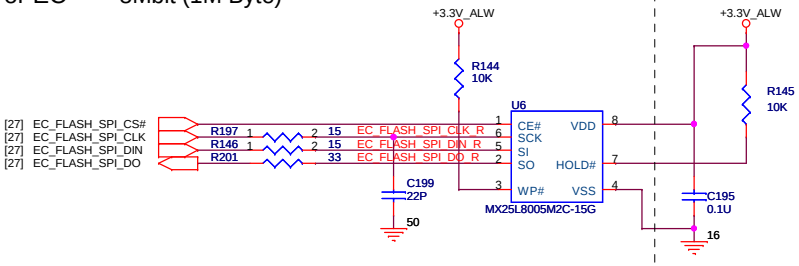


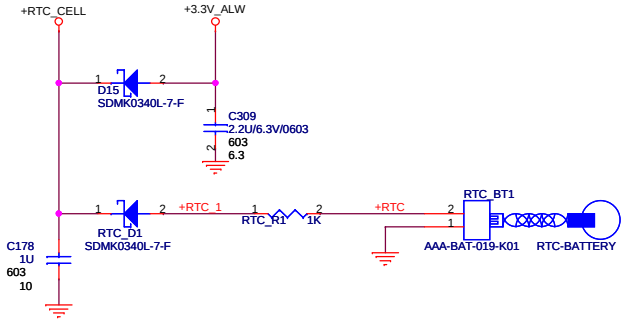
	LCD_SIZE_ID1 (99)	LCD_SIZE_ID2 (107)
14"	0	0
15.6"	1	0
17"	0	1

BID1	BID0 USB_RIGHT_EN#	UM3B(UMA)	UM3 (Dis)
0	0	SSI (X00)	SSI (X00)
0	1	PT (X01)	PT (X01)
1	0	ST (X02)	ST (X02)
1	1	QT (A00)	QT (A00)
0	0	(A01)	(A01)

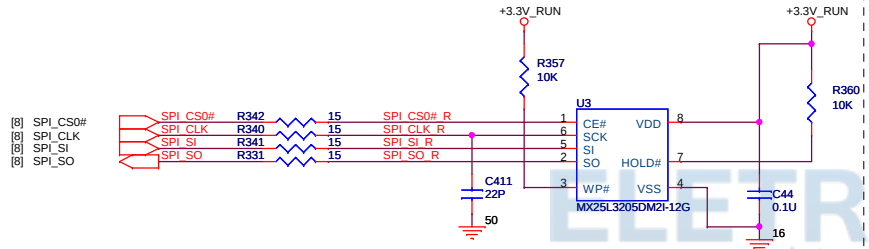
For EC 8Mbit (1M Byte)



RTC BATTERY



For PCH 32Mbit (4M Byte)



QUANTA COMPUTER

Title	Ultra I/O Controller ECE5028	
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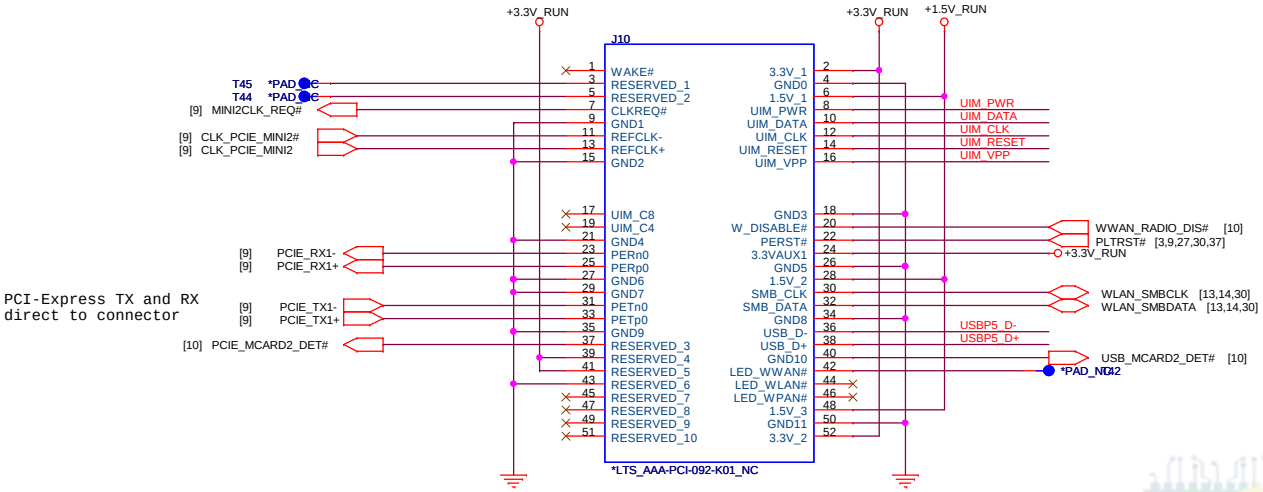
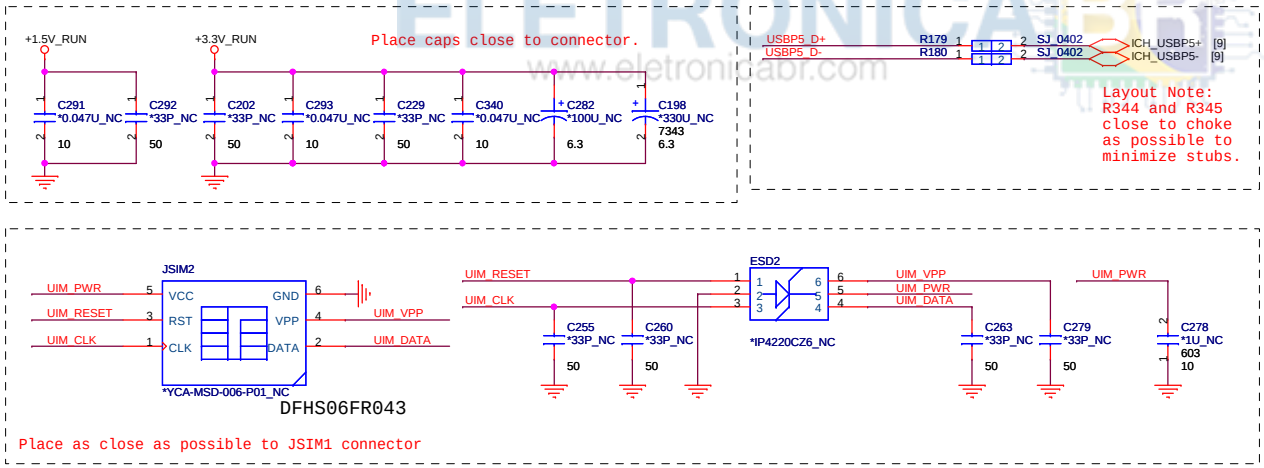
MiniCard WWAN connector





QUANTA COMPUTER

Title	MINI-PCI	
Size	Document Number UM3B/UM6B	Rev 1A
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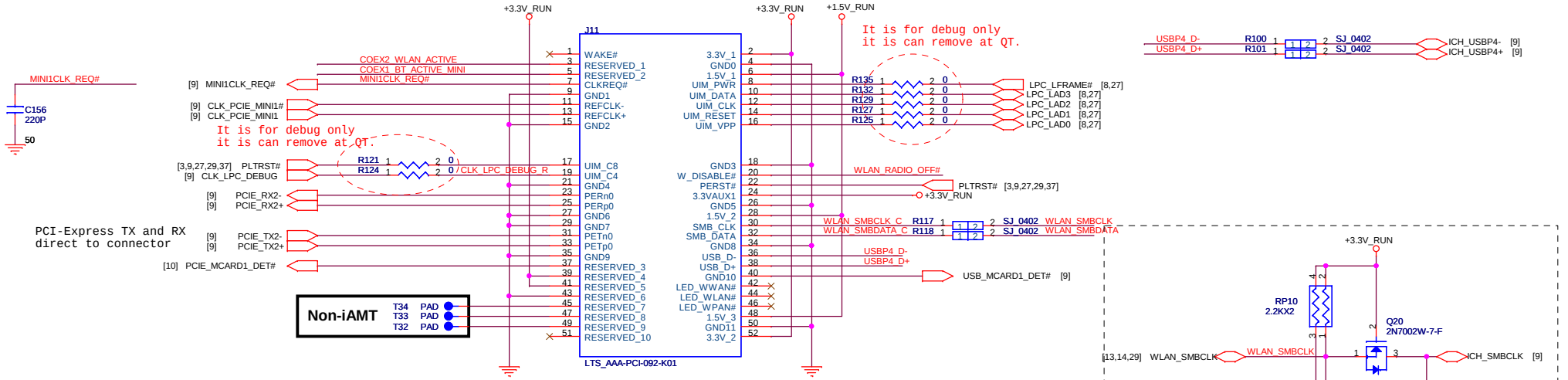
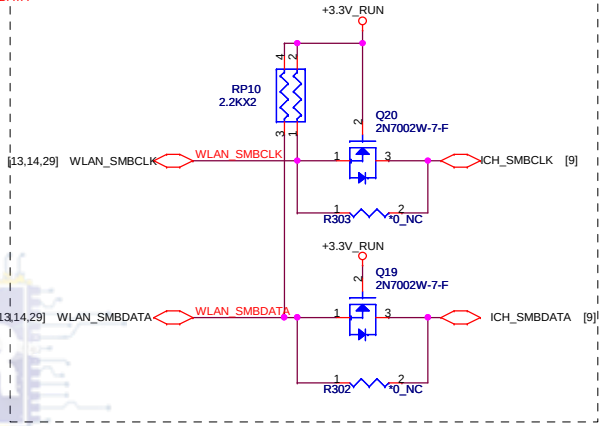
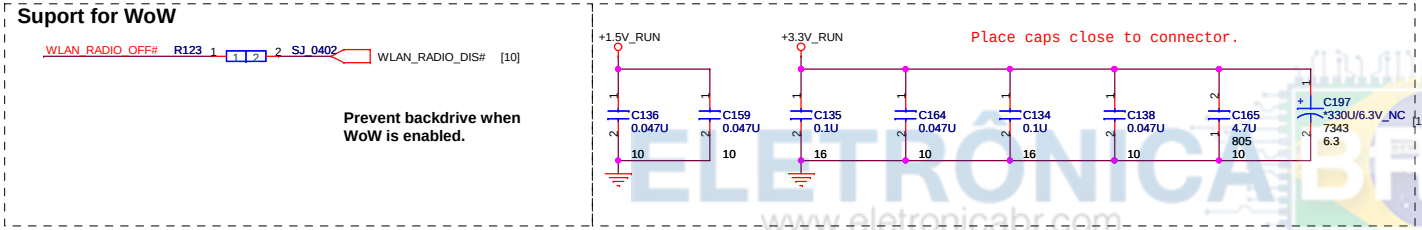
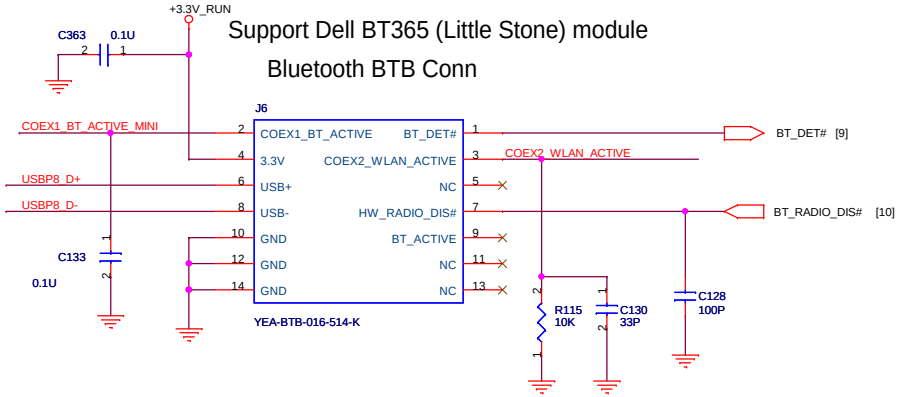
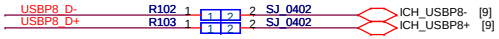
MiniCard WLAN connector











QUANTA COMPUTER

Title	BT/ MINICARD	
Size	Document Number UM3B/UM6B	Rev 1A
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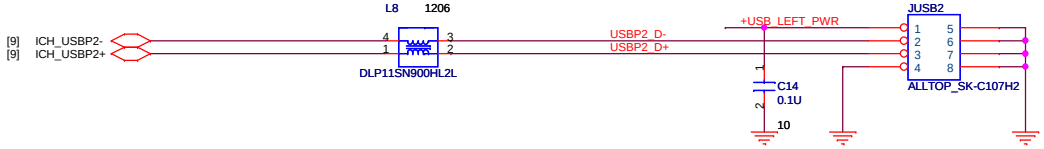
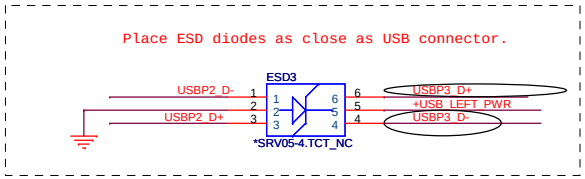
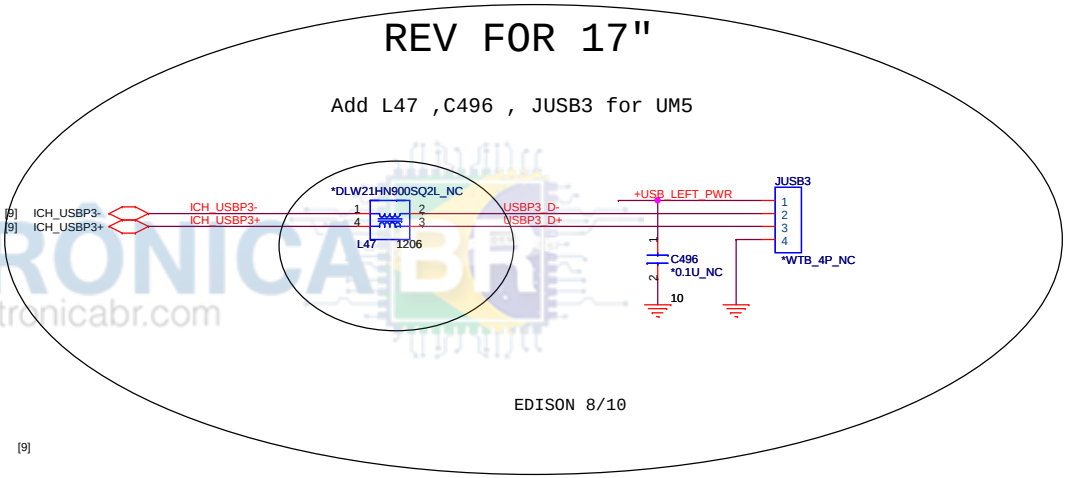
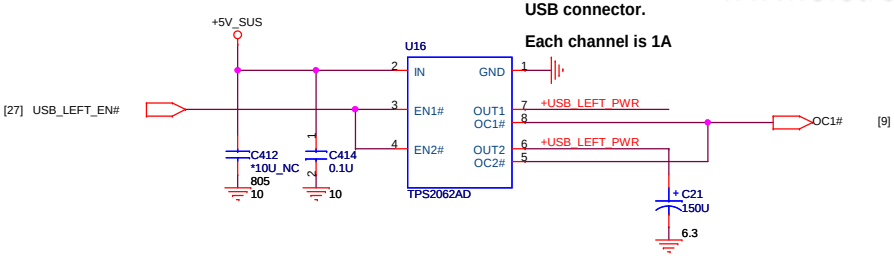






Place one 150uF cap by each USB connector.

Each channel is 1A



QUANTA COMPUTER		
Title: USB		
Size	Document Number: UM3B/UM6B	Rev: 1A
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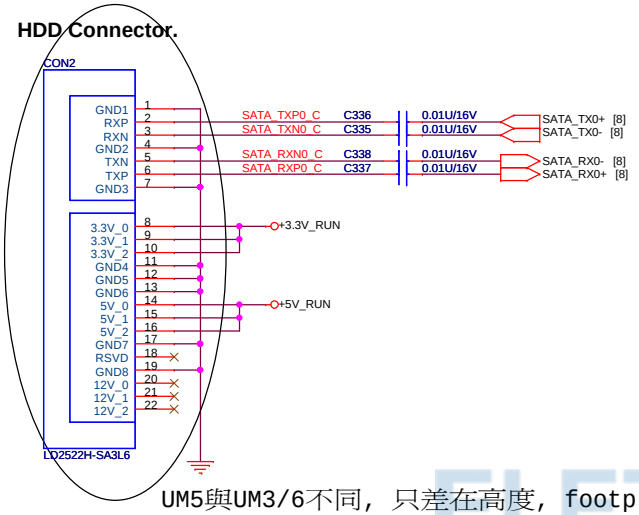
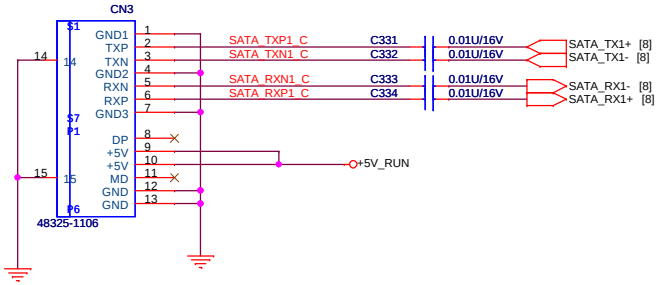
HDD Connector.



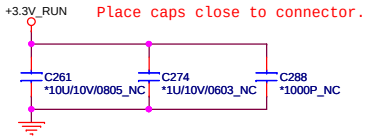
ODD Connector

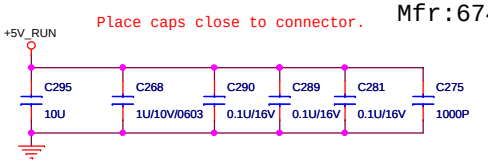


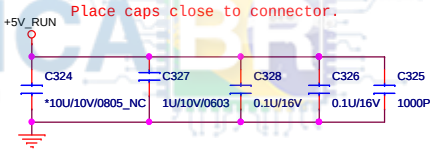
UM5與UM3/6不同, 只差在高度, footprint沒變

UM5/UM5B
PN:DFHS22FR137
Mfr:67492-1224

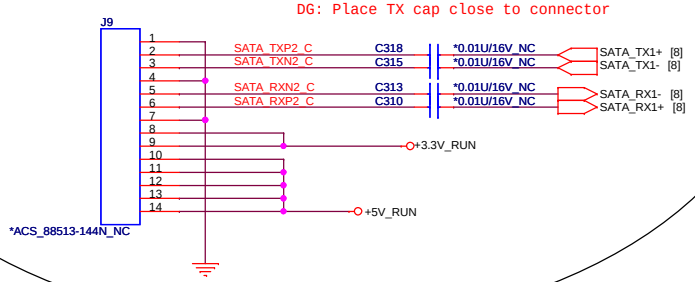
UM3/UM3B/UM6/UM6B
PN:
Mfr:67492-1730







REV FOR 15.6"



QUANTA COMPUTER

Title	SATA (HDD&CD_ROM)	
Size	Document Number UM3B/UM6B	Rev 1A
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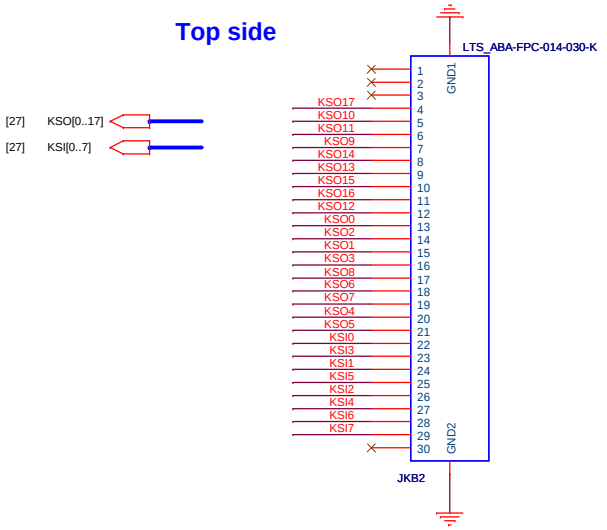
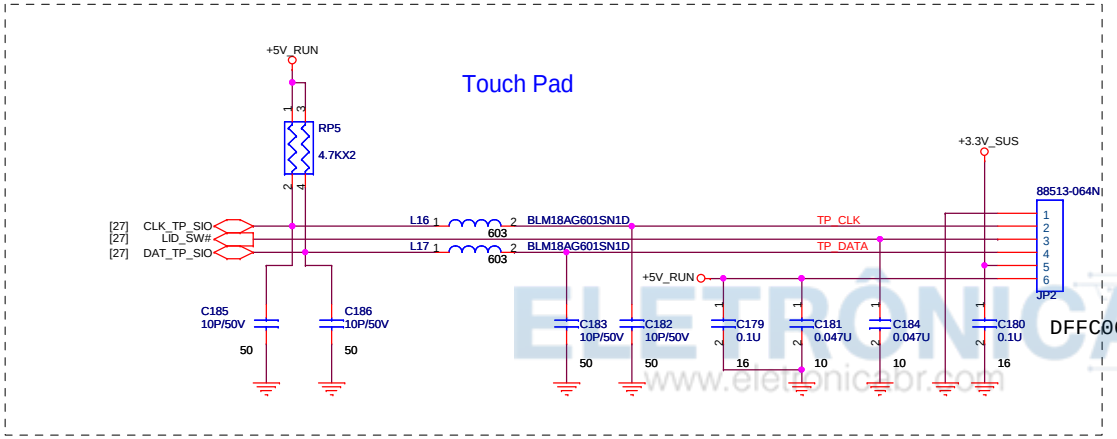
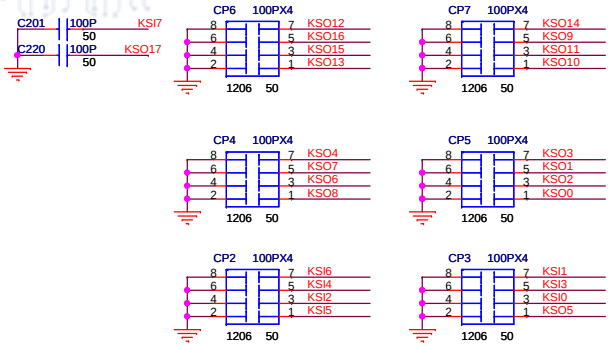
KEYBOARD CONNECTOR

Top side



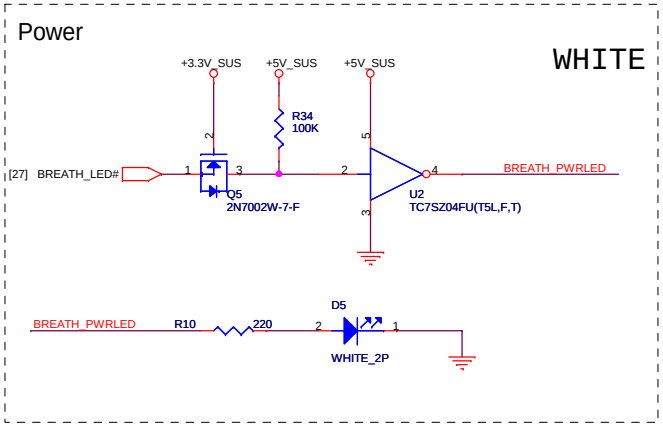
Touch Pad

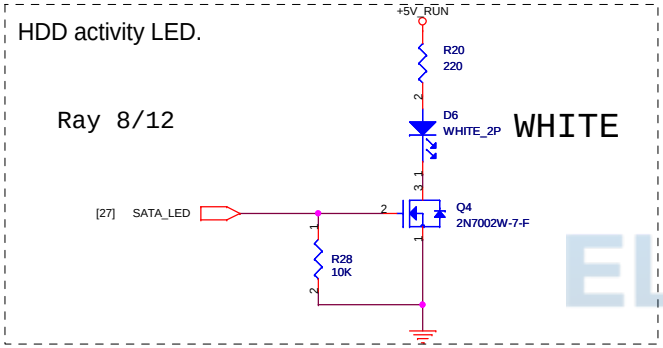


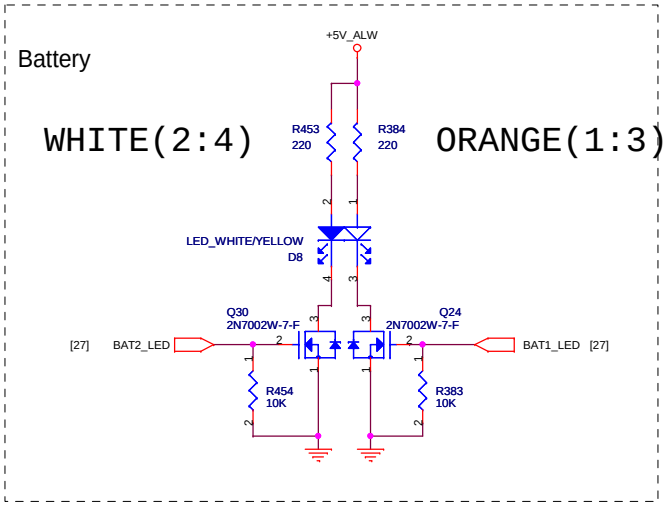


QUANTA COMPUTER

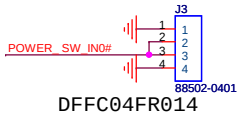
Title	TOUCH PAD, KB CONN	
Size	Document Number UM3B/UM6B	Rev 1A
Date: Friday, October 02, 2009	Sheet 33 of 59	







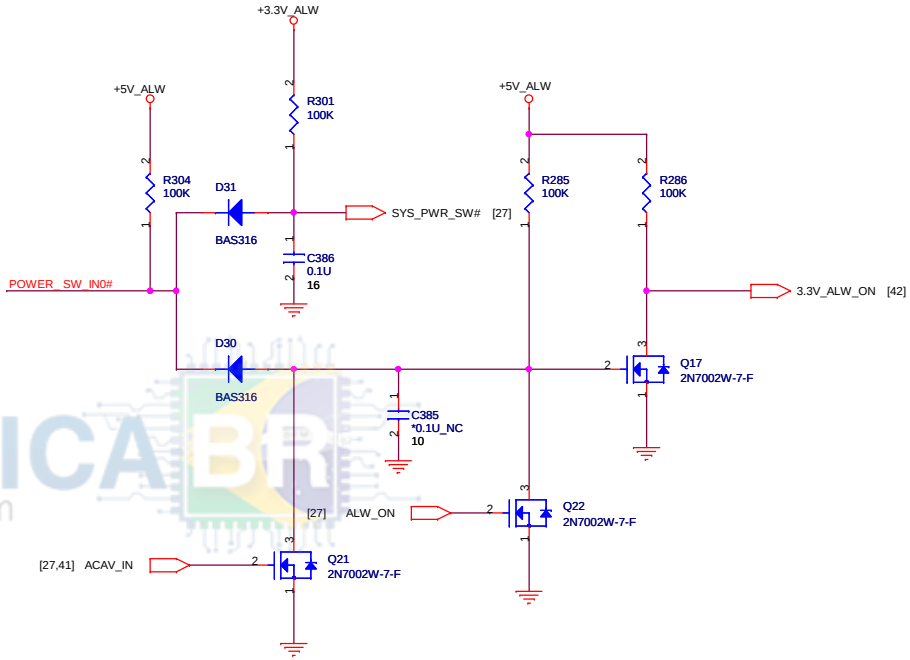
Power button Cable

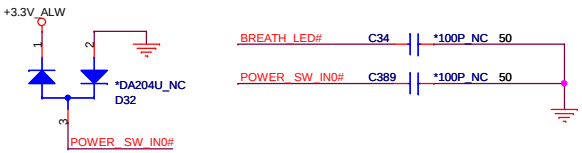


DFFC04FR014

PIN2,3 connect to POWER_ SW_IN0#

3VALW ON POWER LOGIC



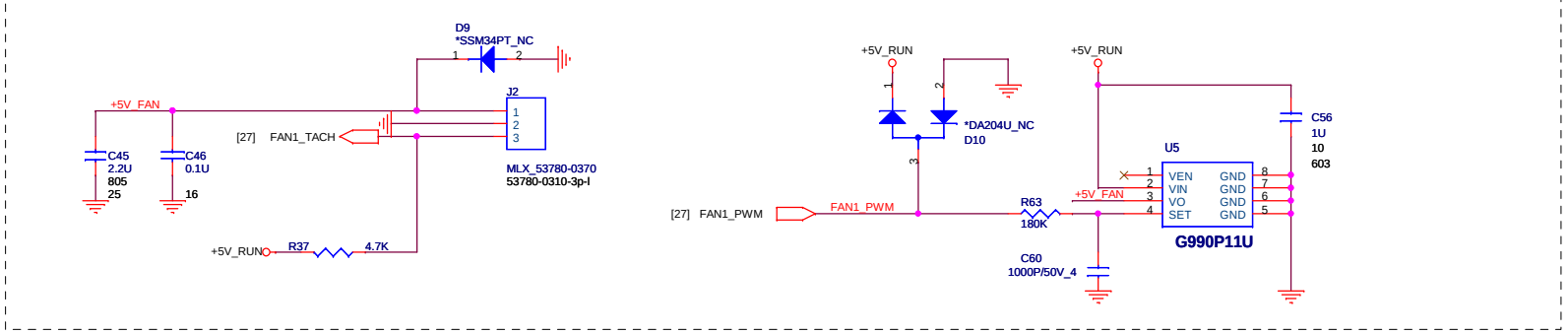


QUANTA COMPUTER

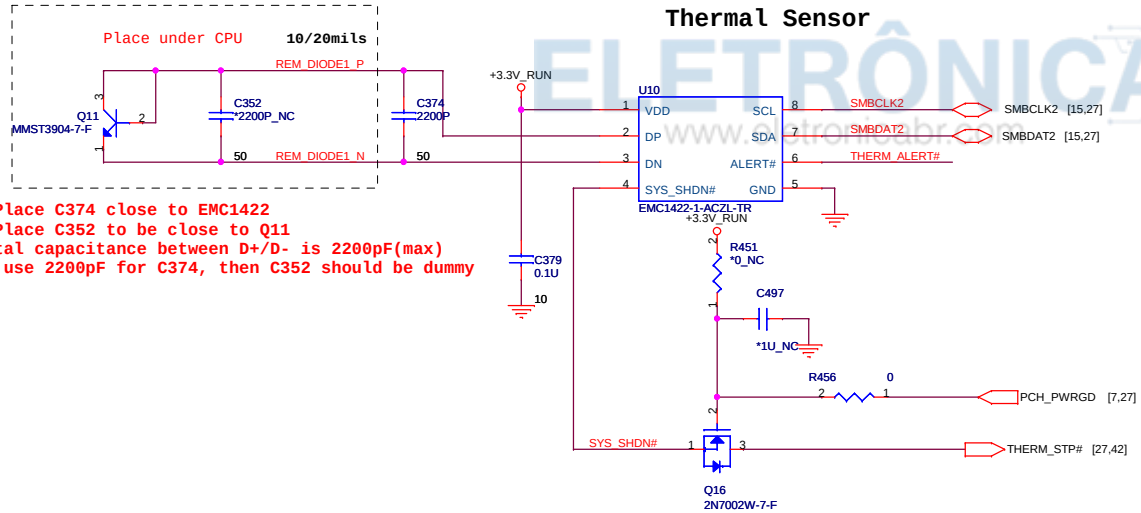
Title	SWITCH, KEYBOARD & LED&Touch Screen Module	
Size	Document Number UM3B/UM6B	Rev 1A
Date: Friday, October 02, 2009	Sheet 34 of 59	

FAN CONTROL

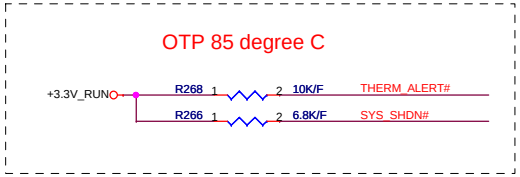
6/23 COPY FROM RM6



Thermal Sensor



1.Place C374 close to EMC1422
2.Place C352 to be close to Q11
Total capacitance between D+/D- is 2200pF(max)
if use 2200pF for C374, then C352 should be dummy



QUANTA COMPUTER

Title	FAN & THERMAL	
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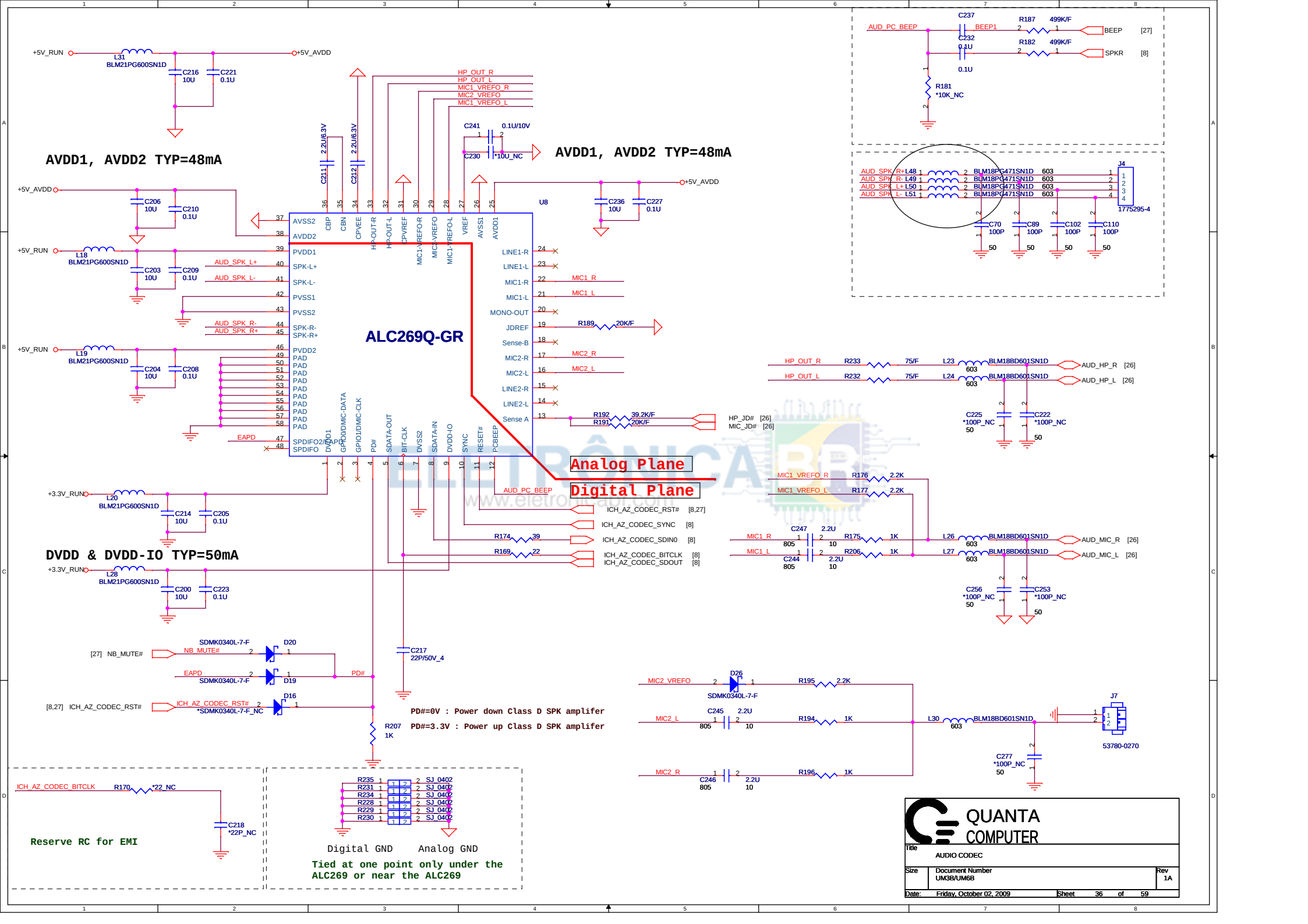
AVDD1, AVDD2 TYP=48mA
AVDD1, AVDD2 TYP=48mA
ALC269Q-GR
U8
Analog Plane
Digital Plane
DVDD & DVDD-IO TYP=50mA
PD#=0V : Power down Class D SPK amplifer
PD#=3.3V : Power up Class D SPK amplifer
Reserve RC for EMI
Digital GND
Analog GND
Tied at one point only under the ALC269 or near the ALC269
QUANTA COMPUTER
AUDIO CODEC
Document Number UM3B/UM6B
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Friday, October 02, 2009
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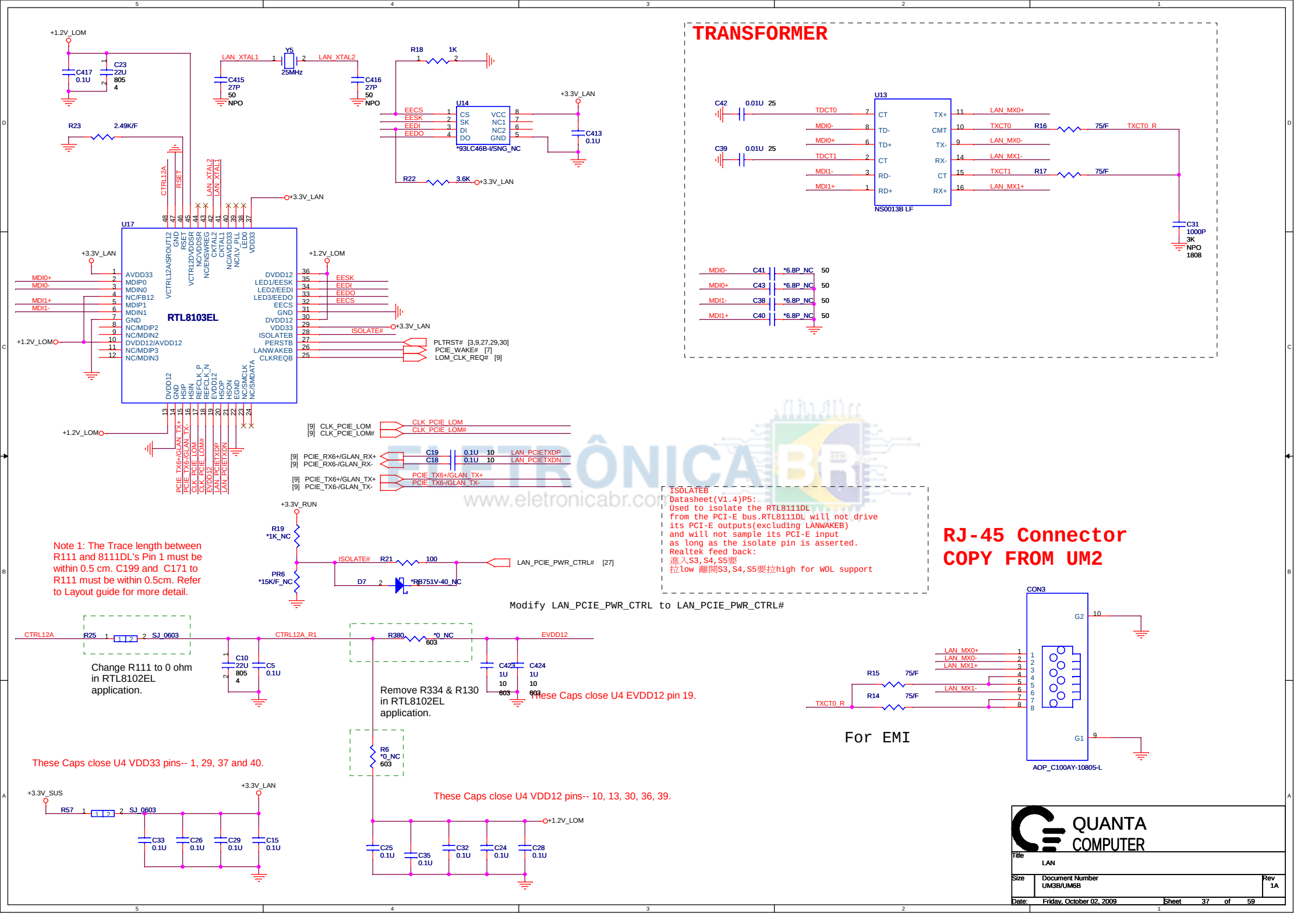
TRANSFORMER
RTL8103EL
U17
U13
U14
Y5
25MHz
NS0013B LF
*93LC46B-I/SNG_NC
Note 1: The Trace length between R111 and 8111DL's Pin 1 must be within 0.5 cm. C199 and C171 to R111 must be within 0.5cm. Refer to Layout guide for more detail.
ISOLATEB
Datasheet(V1.4)P5:
Used to isolate the RTL8111DL
from the PCI-E bus.RTL8111DL will not drive
its PCI-E outputs(excluding LANWAKEB)
and will not sample its PCI-E input
as long as the isolate pin is asserted.
Realtek feed back:
進入S3,S4,S5要
拉low 離開S3,S4,S5要拉high for WOL support
RJ-45 Connector
COPY FROM UM2
Modify LAN_PCIE_PWR_CTRL to LAN_PCIE_PWR_CTRL#
Change R111 to 0 ohm in RTL8102EL application.
Remove R334 & R130 in RTL8102EL application.
These Caps close U4 EVDD12 pin 19.
These Caps close U4 VDD33 pins-- 1, 29, 37 and 40.
These Caps close U4 VDD12 pins-- 10, 13, 30, 36, 39.
For EMI
CON3
AOP_C100AY-10805-L
QUANTA COMPUTER
Title LAN
Size Document Number UM3B/UM6B Rev 1A
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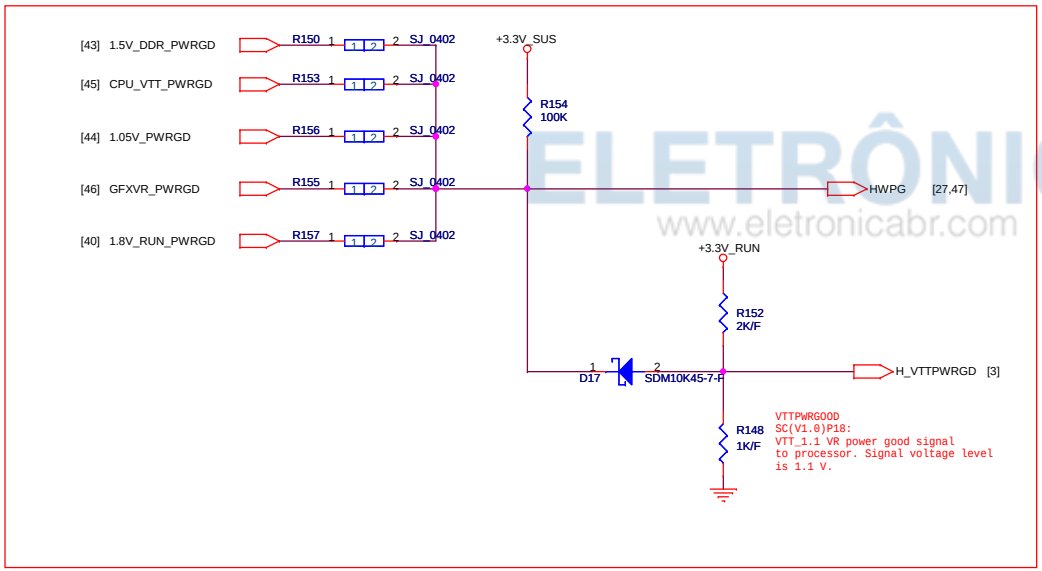
[27] RUN_ON_1 — R32 1 — 2 SJ_0402 — RUN_ON [40,43,44,45,48]



QUANTA COMPUTER

Title	System Reset Circuit	
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QUANTA COMPUTER

Title	Battery Selector	
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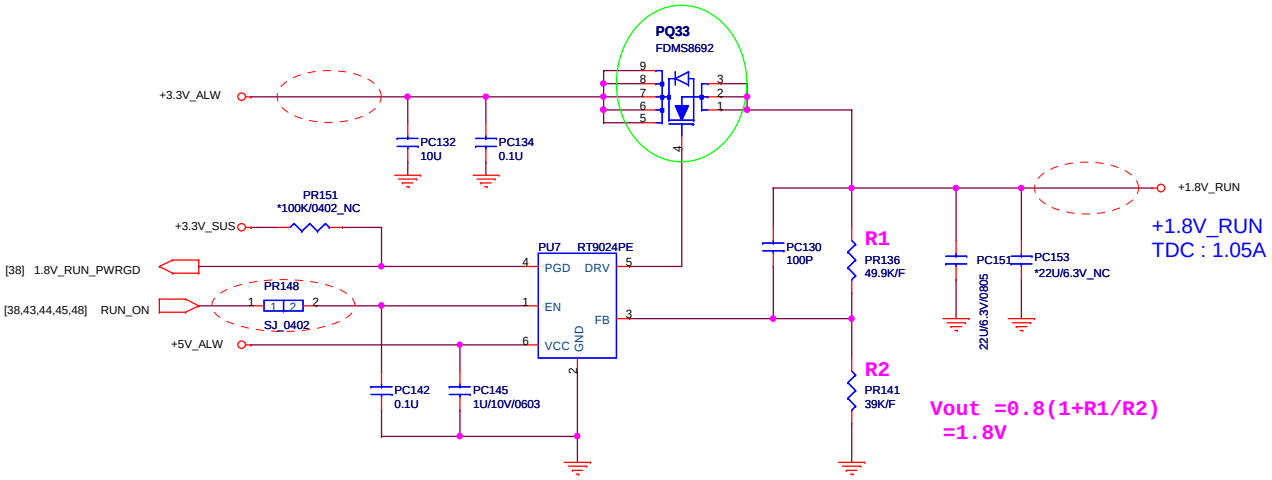

+1.8V_RUN for CPU and PCH 1.8V

09/08: remove PJP11 and PJP18, change PR148 from 0 ohm to shot jump

Title	+1.8V_RUN_GFX (RT9024PE) & +1.8V_RUN(RT9018B)	
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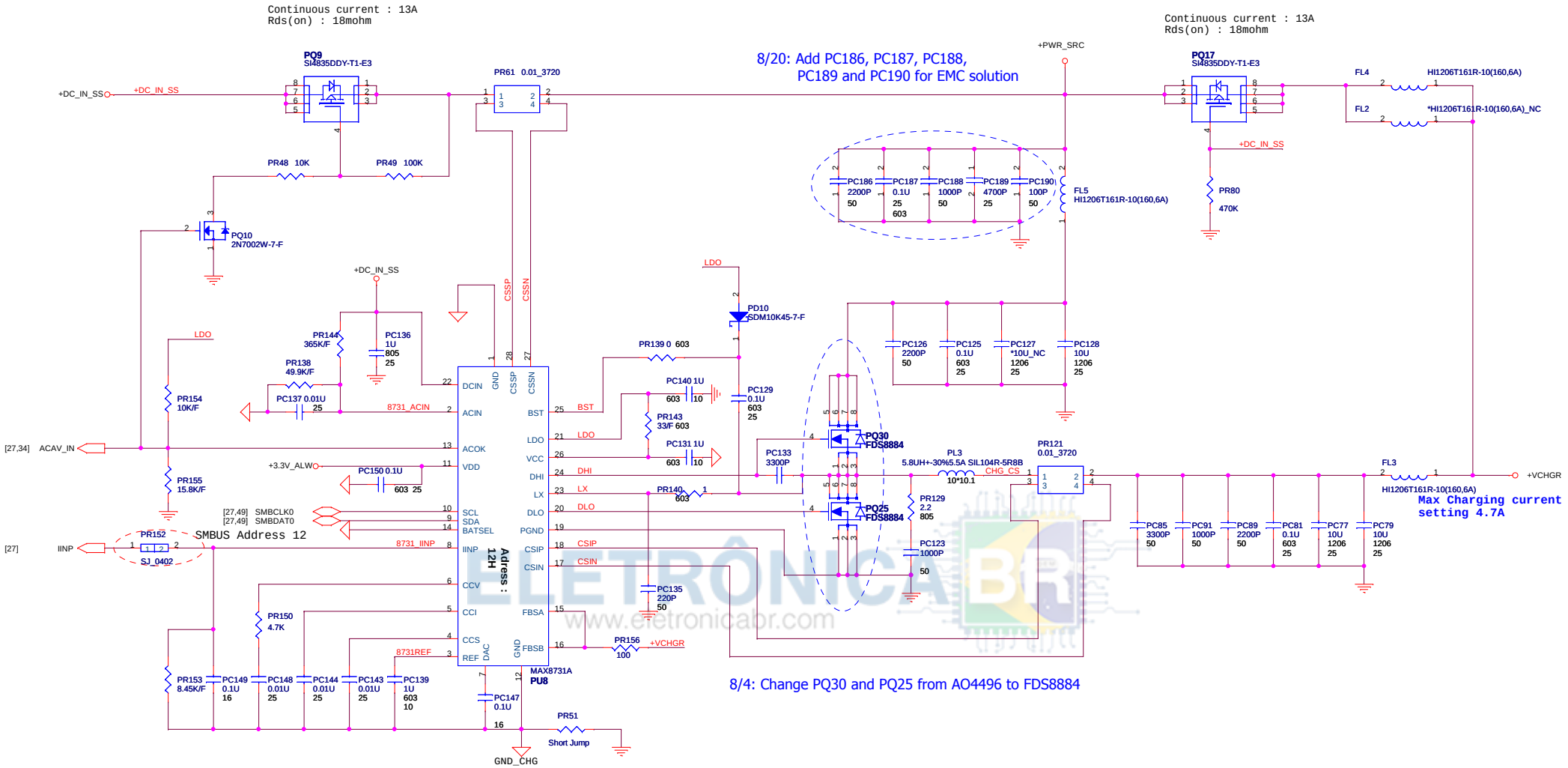

Title	Charger (MAX8731)
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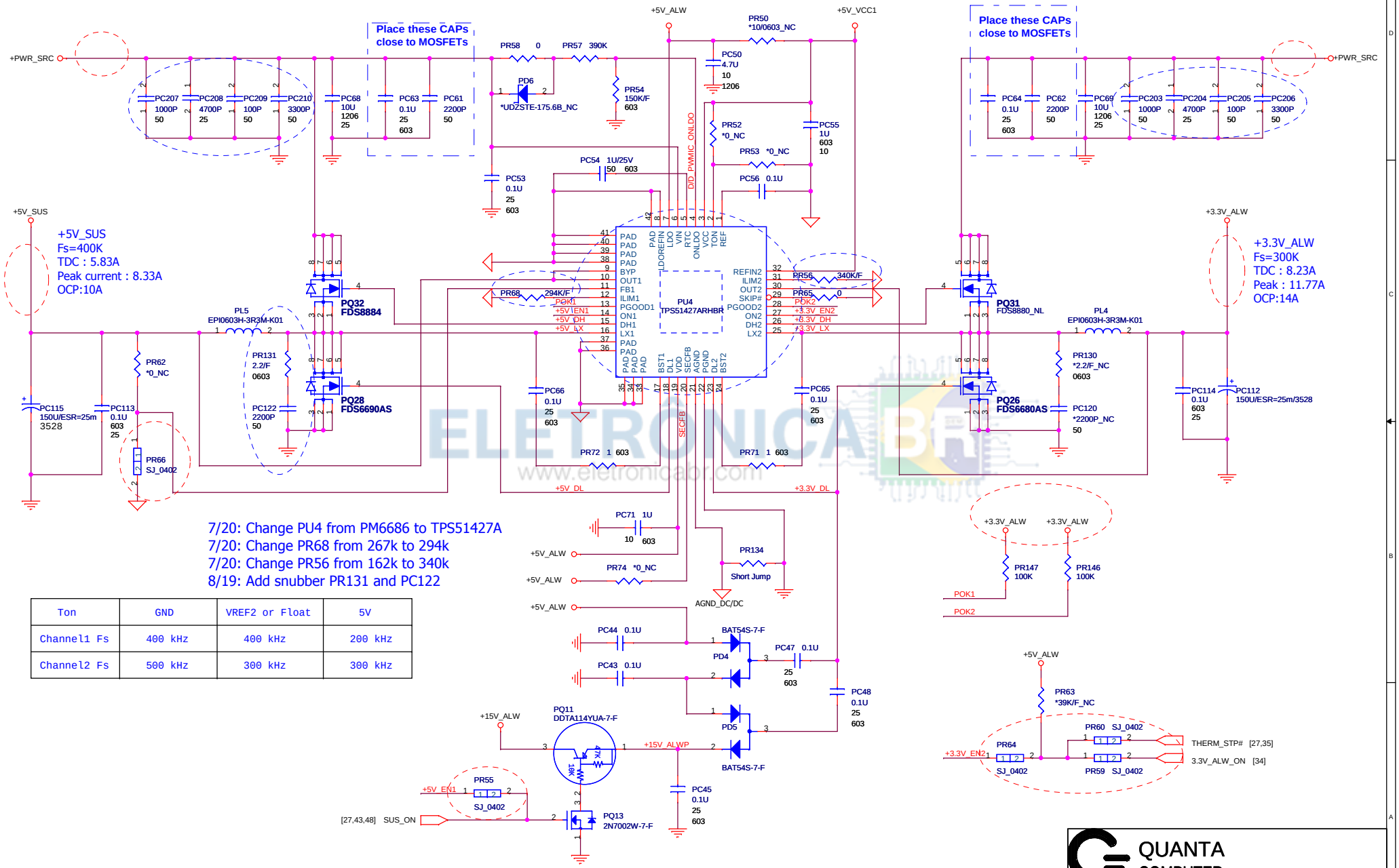
QUANTA COMPUTER

09/08: change PR59, PR60, PR64, PR66, PR55 from 0 ohm to shot jump
09/08: remove PJP8, PJP9, PJP12 and PJP15
8/20: Add PC207, PC208, PC209 and PC210
for EMC solution

8/20: Add PC203, PC204, PC205 and PC206
for EMC solution



7/20: Change PU4 from PM6686 to TPS51427A
7/20: Change PR68 from 267k to 294k
7/20: Change PR56 from 162k to 340k
8/19: Add snubber PR131 and PC122

Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	400 kHz	200 kHz
Channel2 Fs	500 kHz	300 kHz	300 kHz

QUANTA COMPUTER

Title	3.3V_ALW / 5V_ALW(TPS51427ARHBR)	
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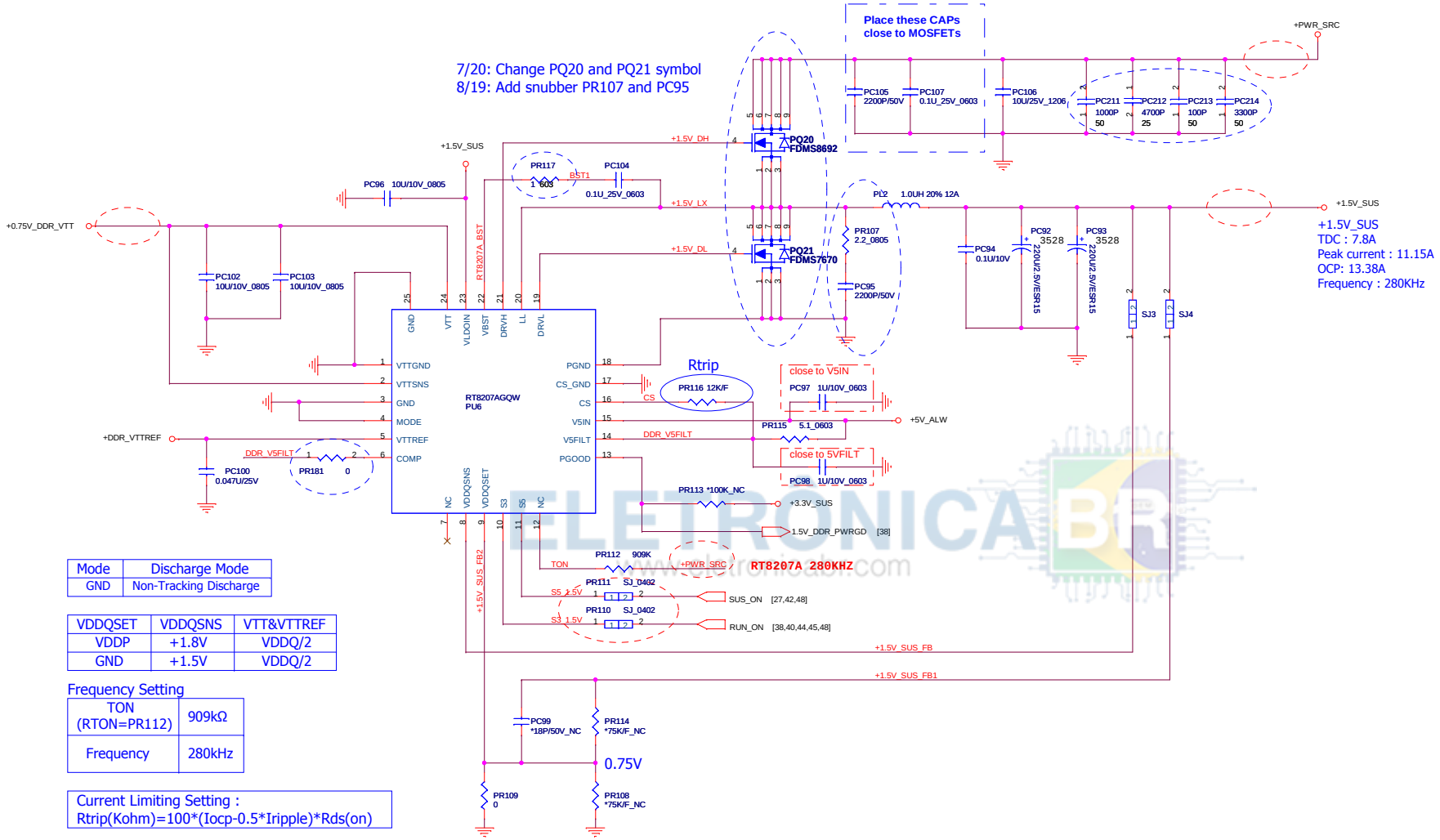
09/08: change PR110 and PR111 from 0 ohm to shot jump
09/08: remove PJP4, PJP5, PJP6 and PJP7

8/20: Add PC211, PC212, PC213 and PC214
for EMC solution

7/20: Change PQ20 and PQ21 symbol
8/19: Add snubber PR107 and PC95



Mode	Discharge Mode
GND	Non-Tracking Discharge

VDDQSET	VDDQSNS	VTT&VTTREF
VDDP	+1.8V	VDDQ/2
GND	+1.5V	VDDQ/2

Frequency Setting

TON (RTON=PR112)	909kΩ
Frequency	280kHz

Current Limiting Setting :
Rtrip(Kohm)=100*(Iocp-0.5*Iripple)*Rds(on)

QUANTA COMPUTER

Title	1.8VSUS & 0.9VTT (TPS51116)	
Size	Document Number UM3B/UM6B	Rev 3A
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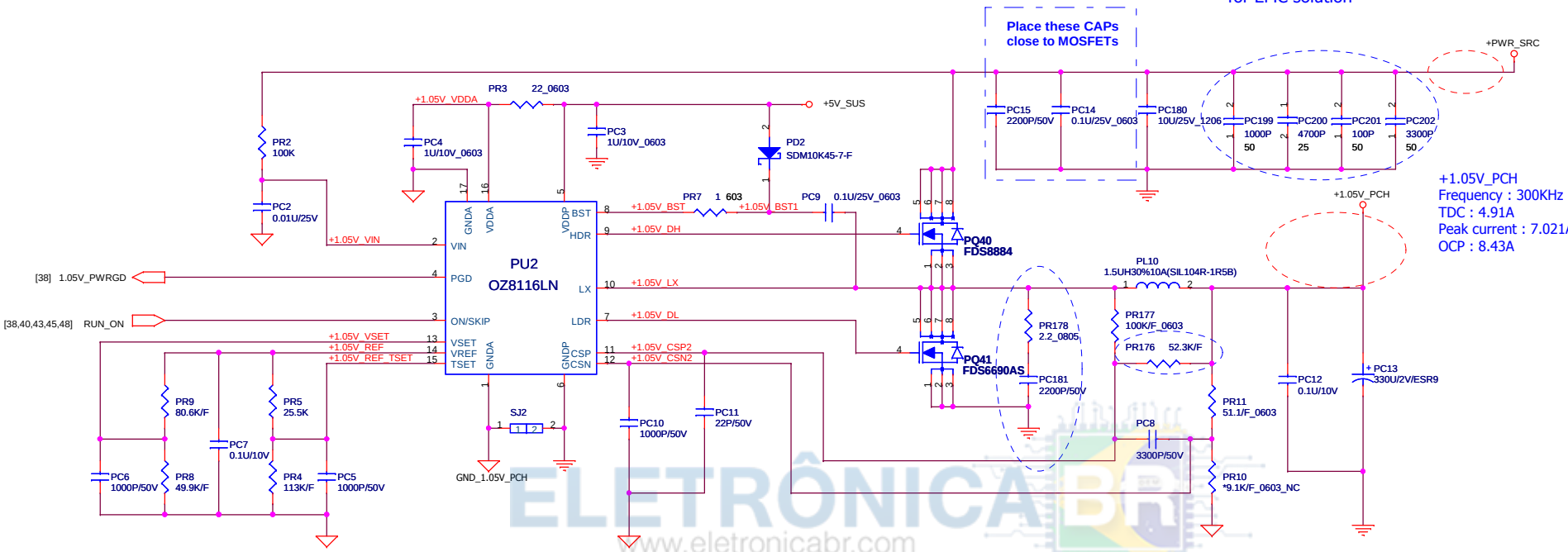
09/08: remove PJP21 and PJP22
8/20: Add PC199, PC200, PC201 and PC202
for EMC solution



7/20: Change PR176 from 47k to 52.3k
8/19: Add snubber PR178 and PC181
8/19: Remove PJP20

Title	<Title>	
Size: Custom	Document Number: UM3B/UM6B	Rev: 1A
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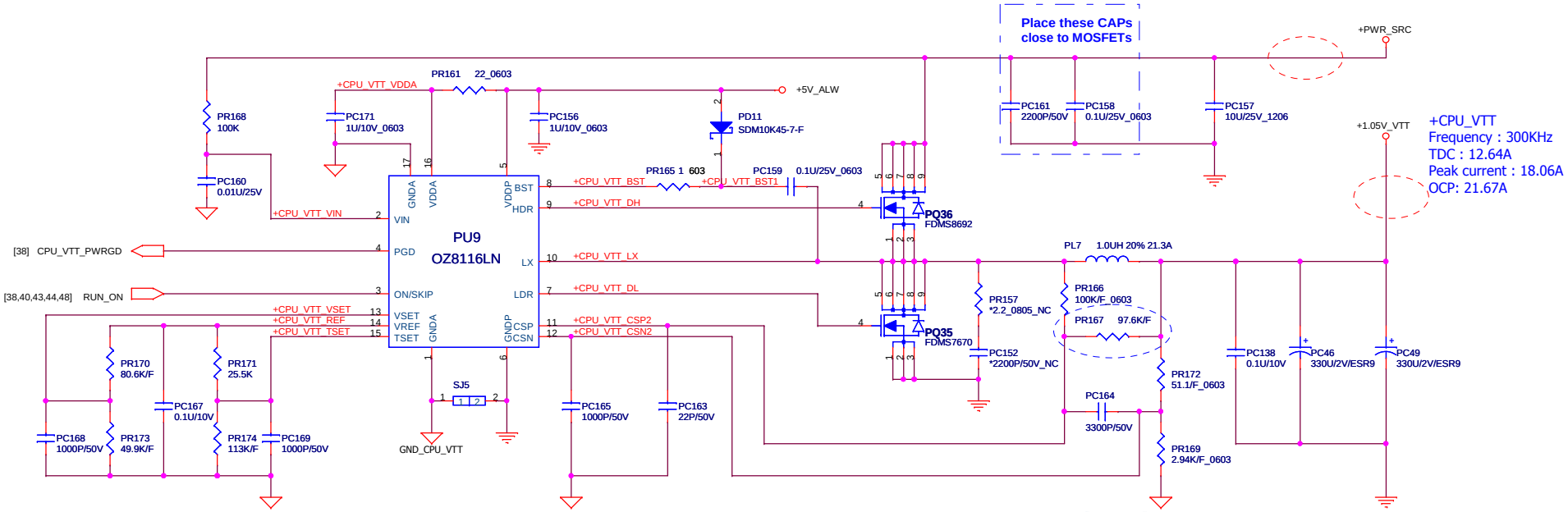

7/20: Change PR167 from 47k to 97.6k

09/08: remove PJP14, PJP17 and PJP19

Title	<Title>	
Size: Custom	Document Number: UM3B/UM6B	Rev: 1A
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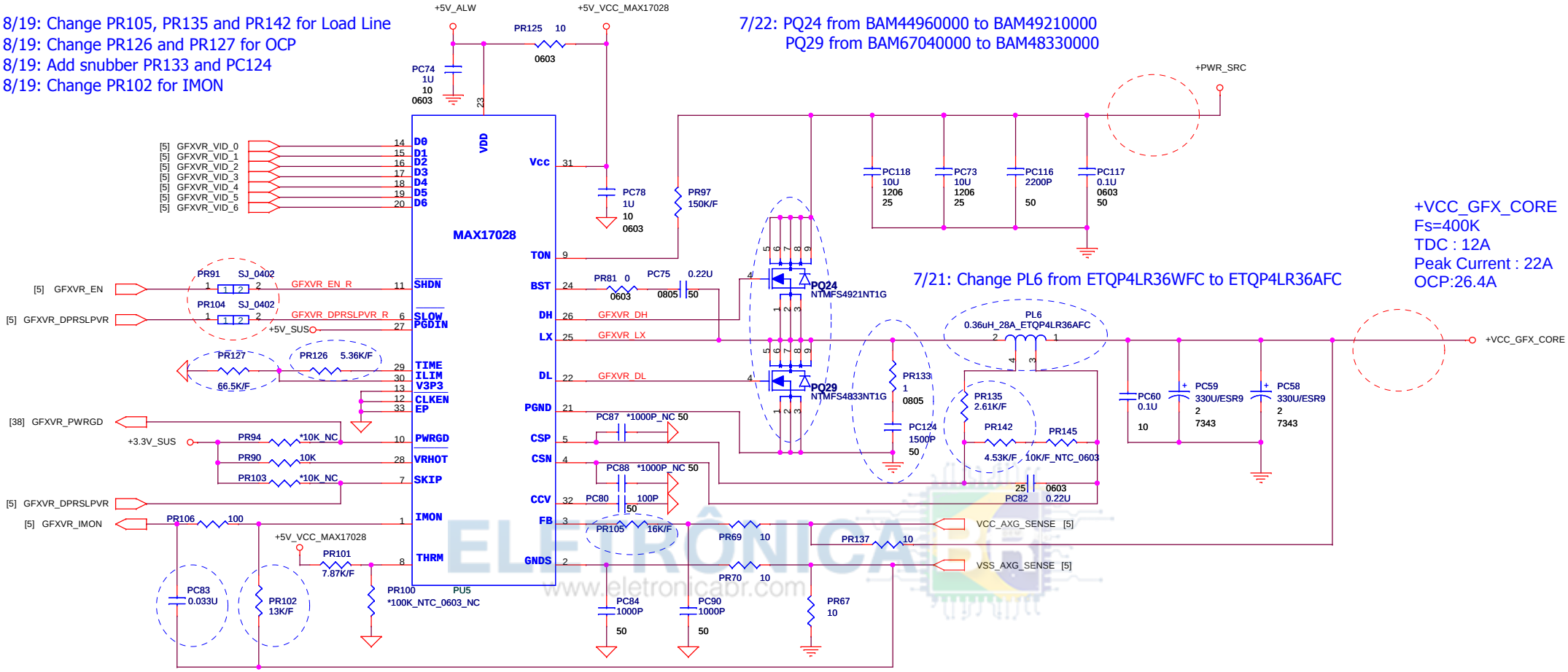
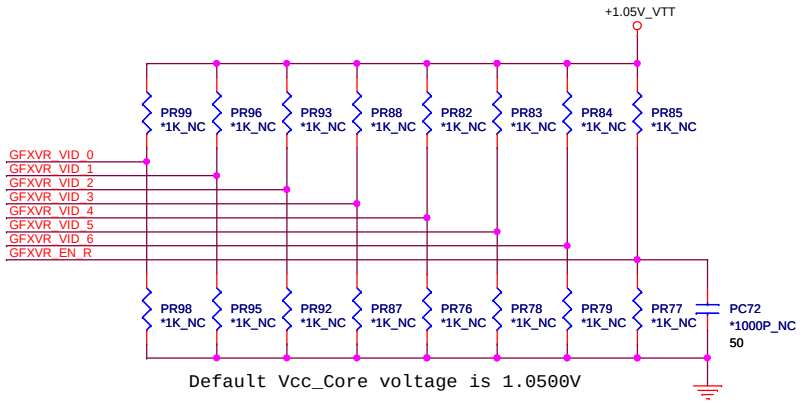
8/19: Change PR105, PR135 and PR142 for Load Line
8/19: Change PR126 and PR127 for OCP
8/19: Add snubber PR133 and PC124
8/19: Change PR102 for IMON

7/22: PQ24 from BAM44960000 to BAM49210000
PQ29 from BAM67040000 to BAM48330000

+VCC_GFX_CORE
Fs=400K
TDC : 12A
Peak Current : 22A
OCP:26.4A

7/21: Change PL6 from ETQP4LR36WFC to ETQP4LR36AFC





Default Vcc_Core voltage is 1.0500V

8/26: Change PC83 and PR102 for IMON
09/08: change PR91 and PR104 from 0 ohm to shot jump
09/08: remove PJP10, PJP13 and PJP16

QUANTA COMPUTER

Title	VGA DC/DC	
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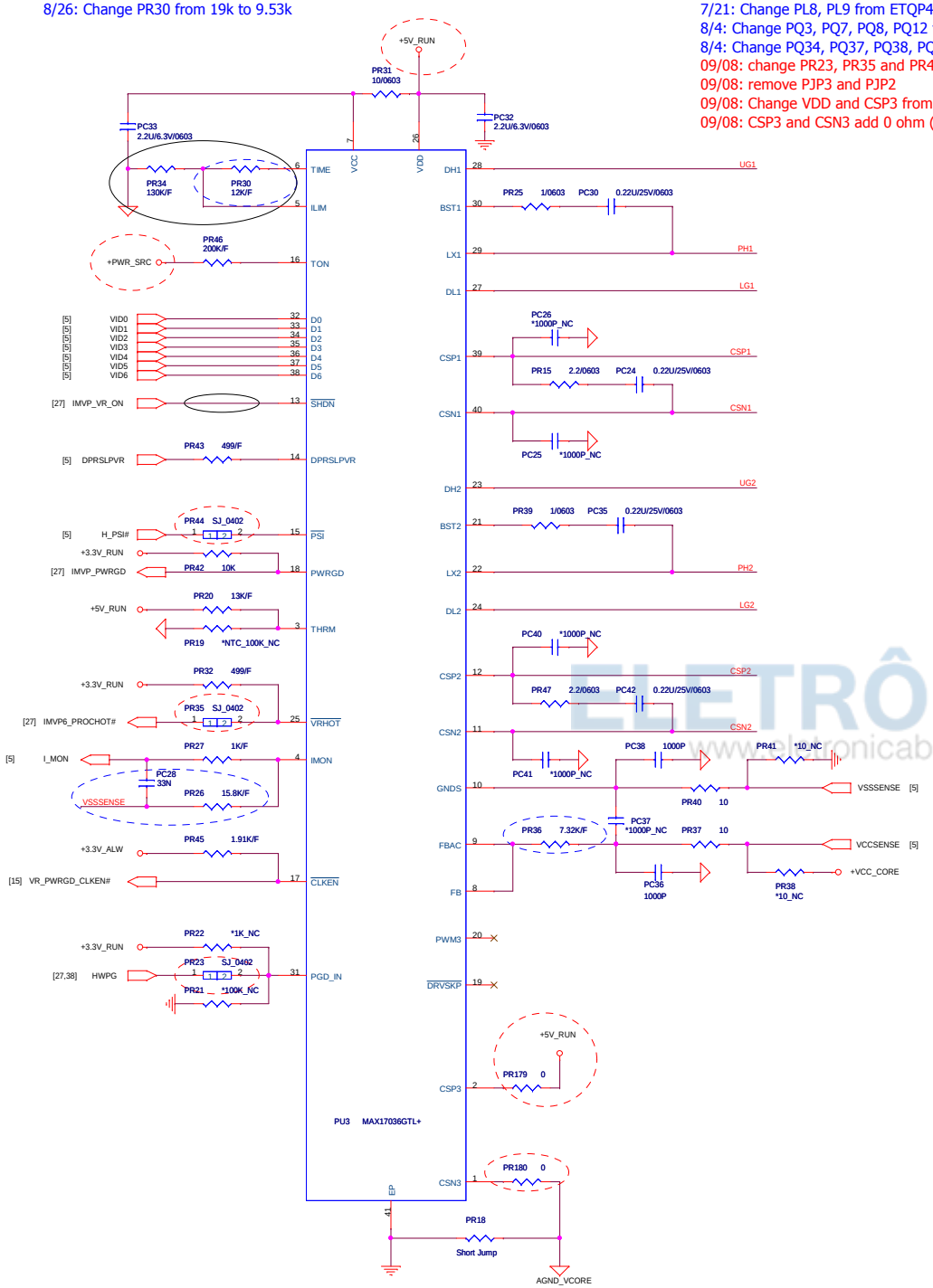
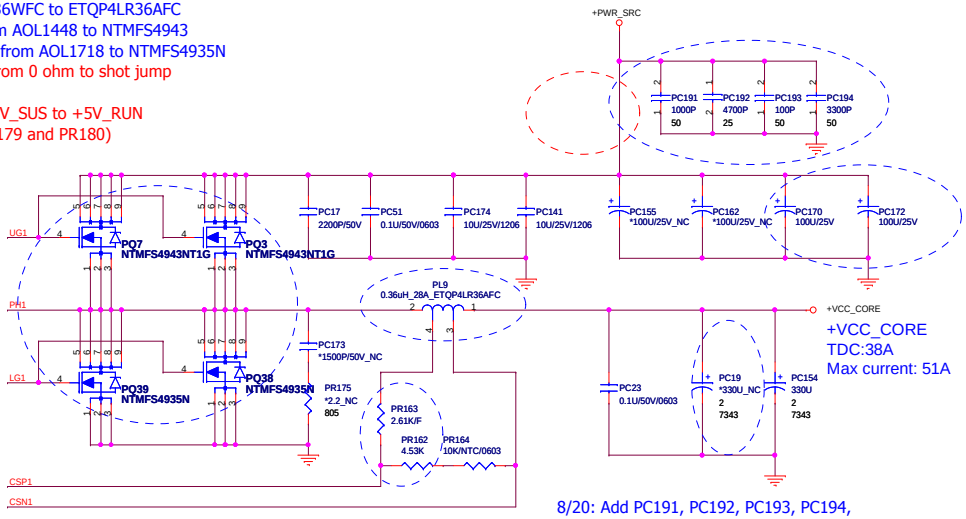
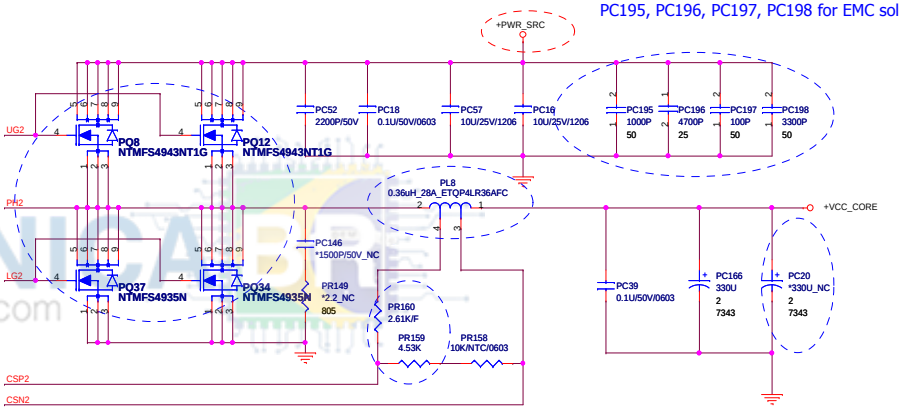
8/26: Change PR30 from 19k to 9.53k

7/21: Change PL8, PL9 from ETQP4LR36WFC to ETQP4LR36AFC
8/4: Change PQ3, PQ7, PQ8, PQ12 from AOL1448 to NTMFS4943
8/4: Change PQ34, PQ37, PQ38, PQ39 from AOL1718 to NTMFS4935N
09/08: change PR23, PR35 and PR44 from 0 ohm to shot jump
09/08: remove PJP3 and PJP2
09/08: Change VDD and CSP3 from +5V_SUS to +5V_RUN
09/08: CSP3 and CSN3 add 0 ohm (PR179 and PR180)





8/20: Add PC191, PC192, PC193, PC194,
PC195, PC196, PC197, PC198 for EMC solution



8/13: NC output cap PC19 and PC20

8/13: Change for Load Line and IMON regulator
change PR26 from 9.53k to 15.8k
change PR36 from 6.8k to 7.32k
change PR159, PR162 from 3.4k to 4.53k
change PR160, PR163 from 1.8k to 2.61k
change PC28 from 0.1uF to 33nF

Title	CPU core (MAX17036)	
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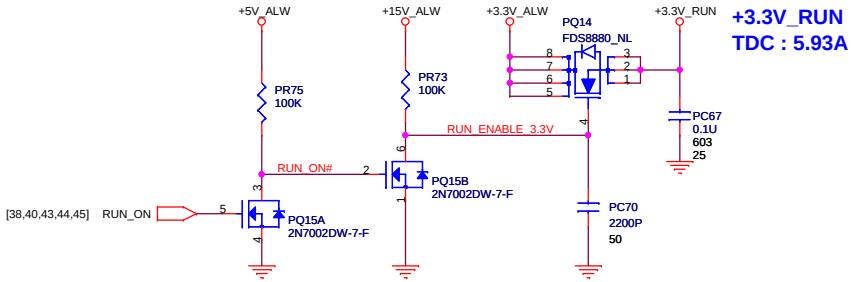
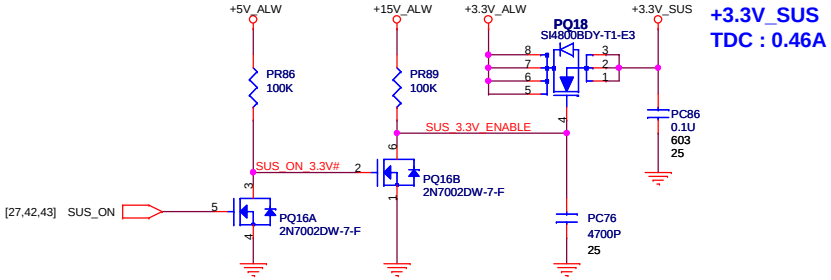
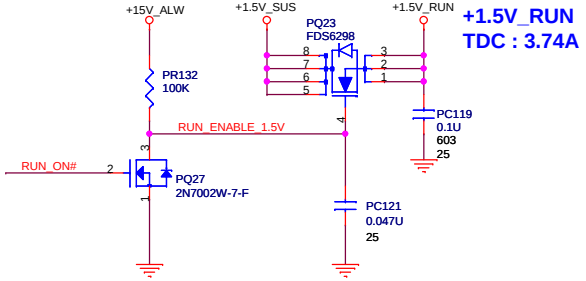


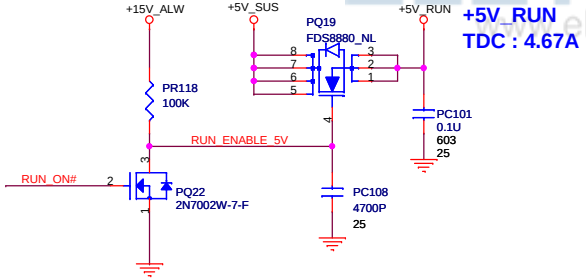
+3.3V_RUN
TDC : 5.93A



+3.3V_SUS
TDC : 0.46A



+1.5V_RUN
TDC : 3.74A



+5V_RUN
TDC : 4.67A

QUANTA COMPUTER

Title	RUN / SUS POWER SW	
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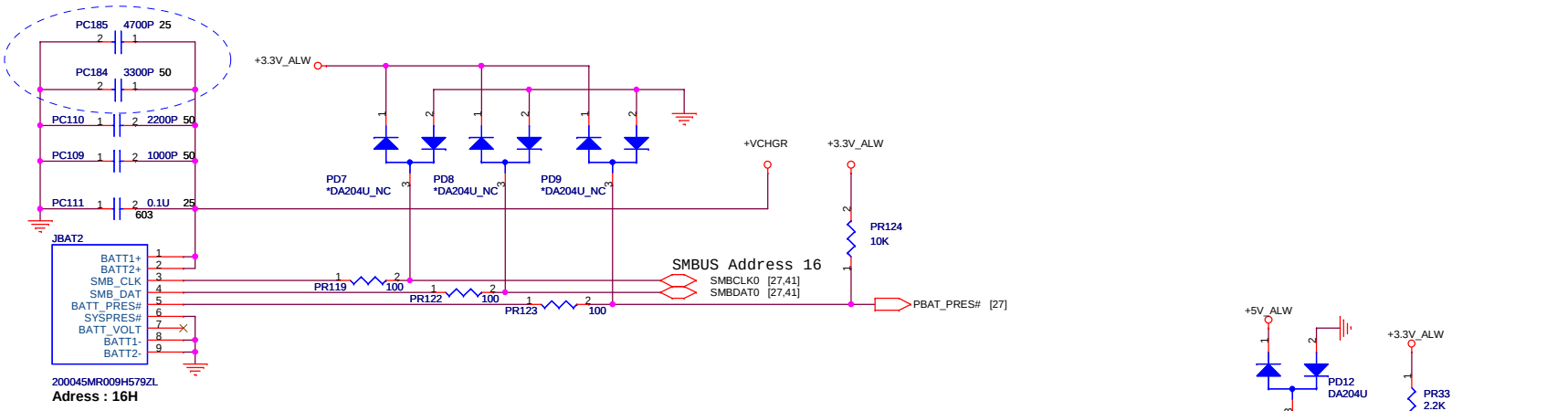
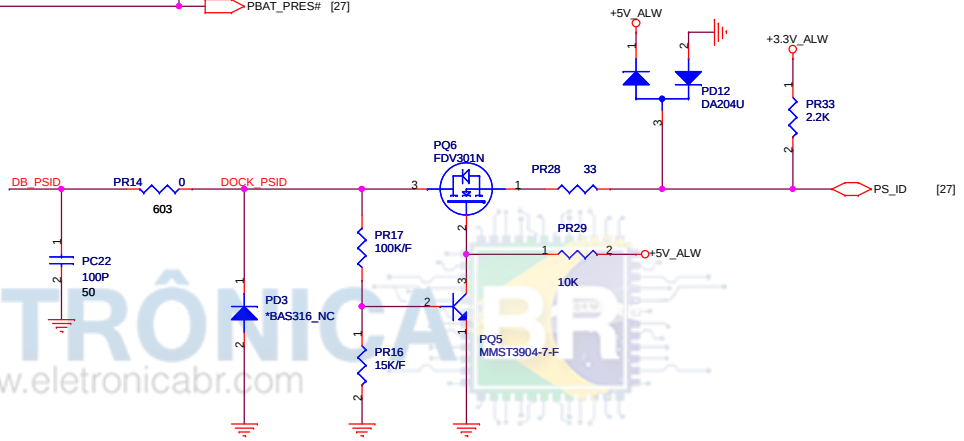
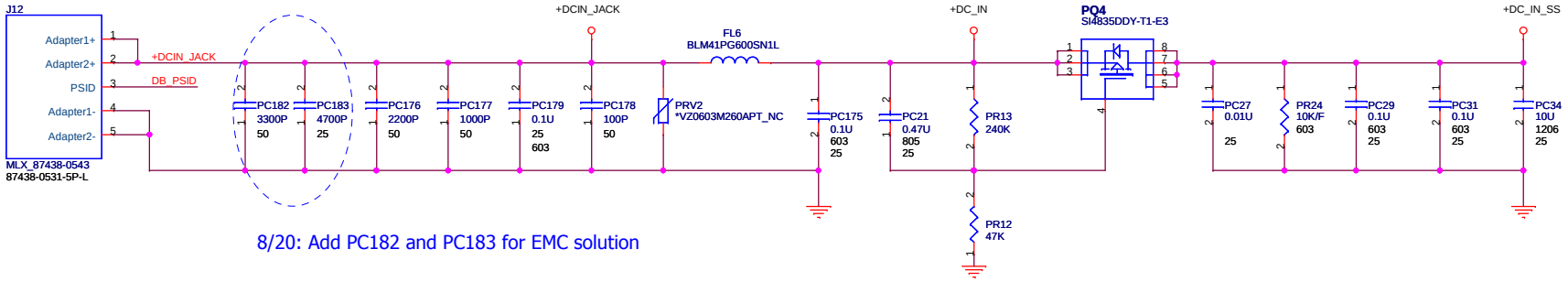
8/20: Add PC184 and PC185 for EMC solution





ZM1



8/20: Add PC182 and PC183 for EMC solution

QUANTA COMPUTER

Title	DCIN,BATT CONNECTOR	
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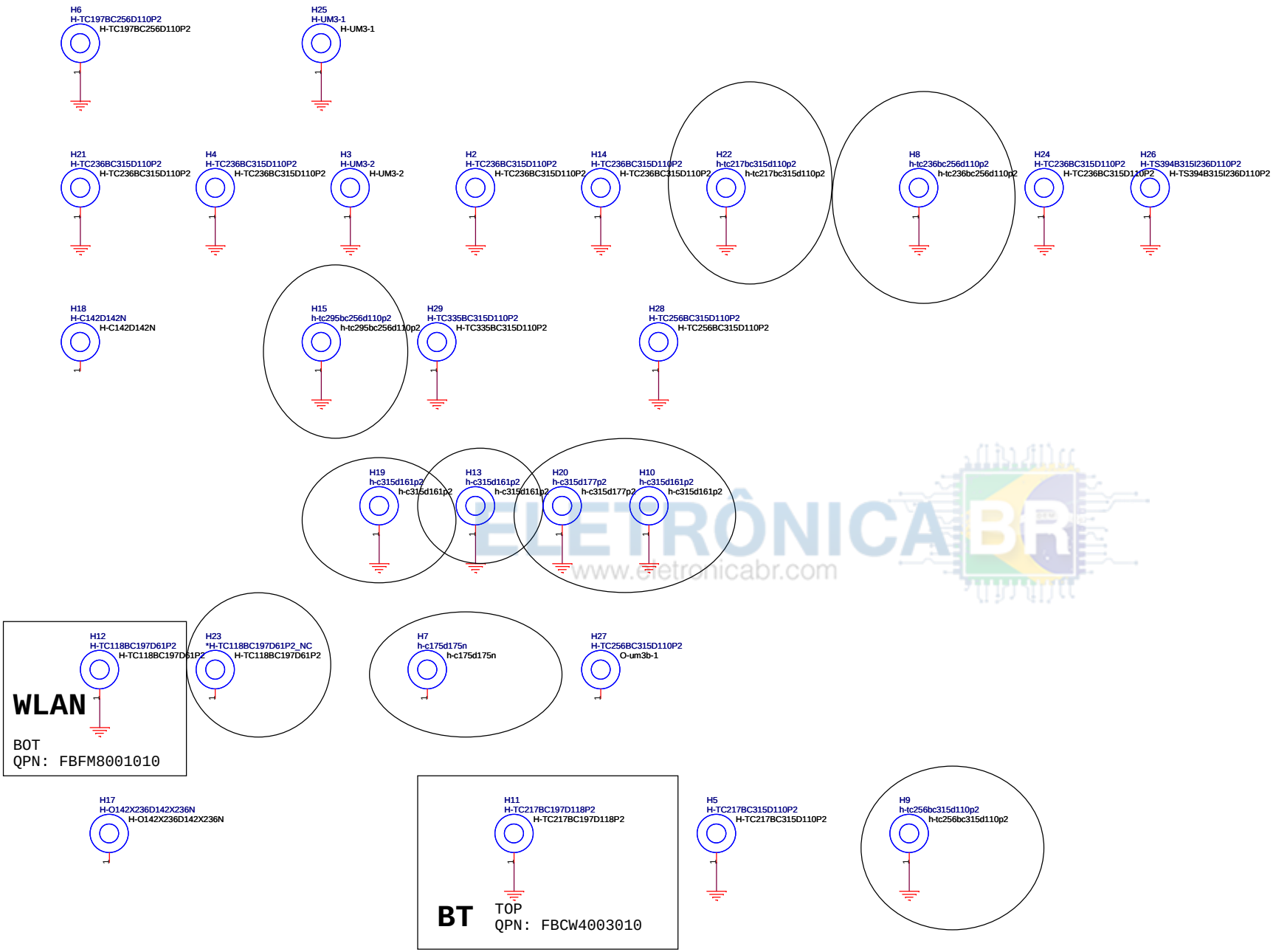

QUANTA COMPUTER

Title	SCREW PAD	
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Reserved for EMI.

QUANTA COMPUTER

Title	EMI CAP	
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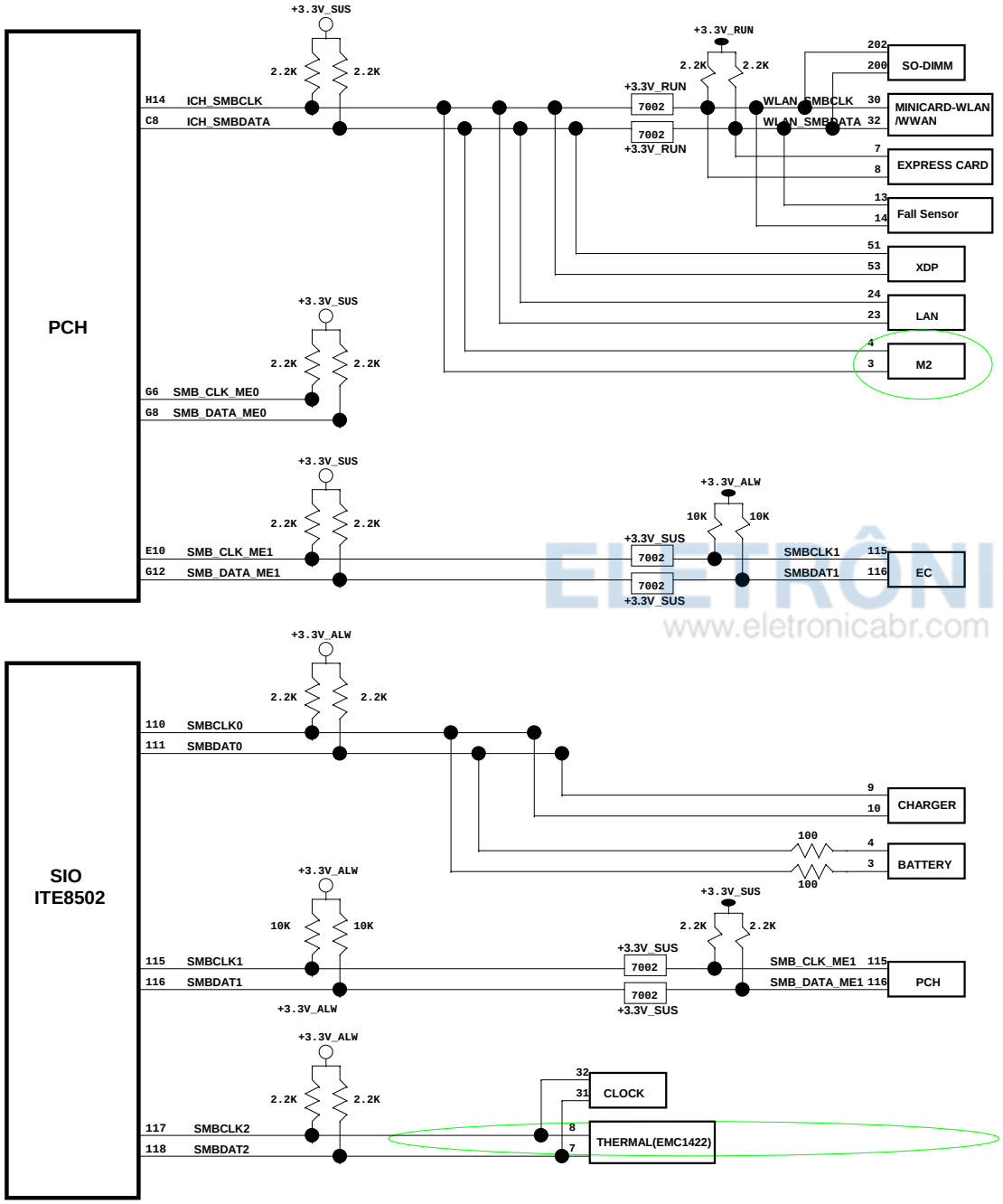

QUANTA COMPUTER

Title	SMBUS BLOCK	
Size	Document Number UMDS/UMGB	Rev 1A
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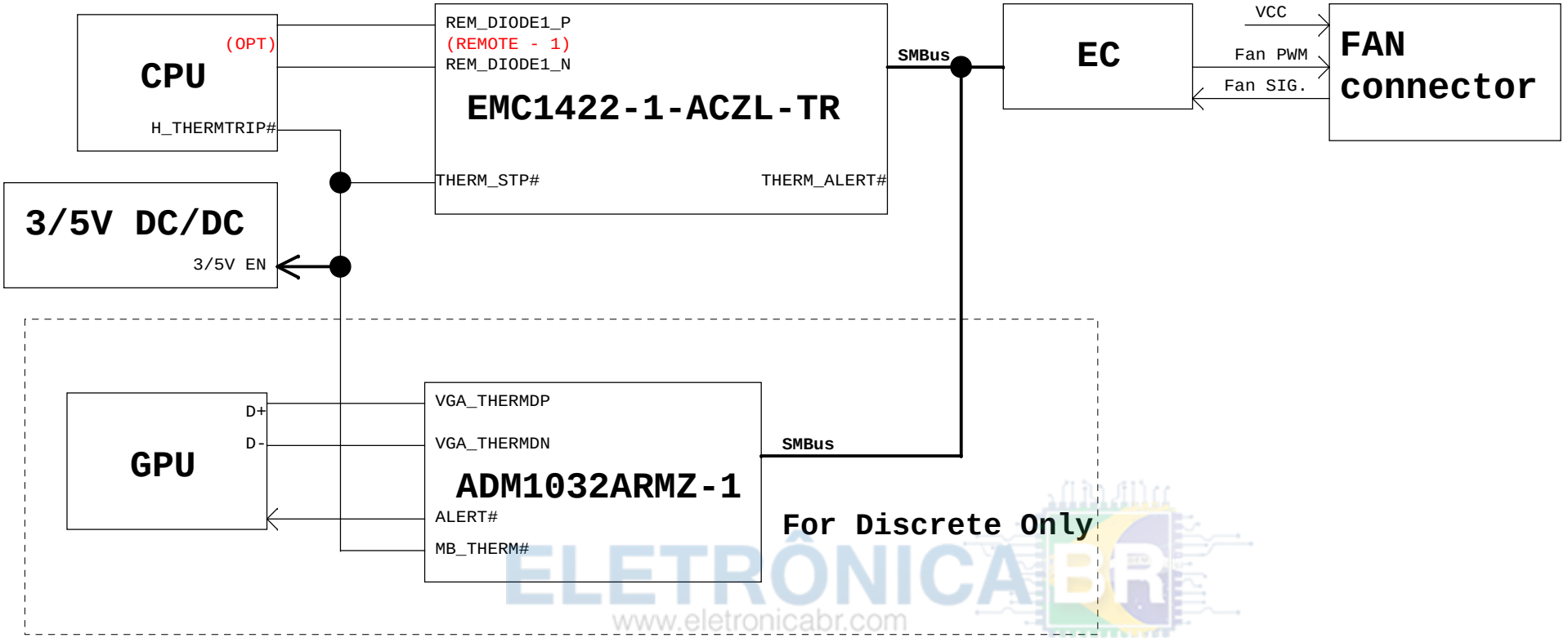

QUANTA COMPUTER

Title	Thermal Map	
Size	Document Number UM3B/UM6B	Rev 1A
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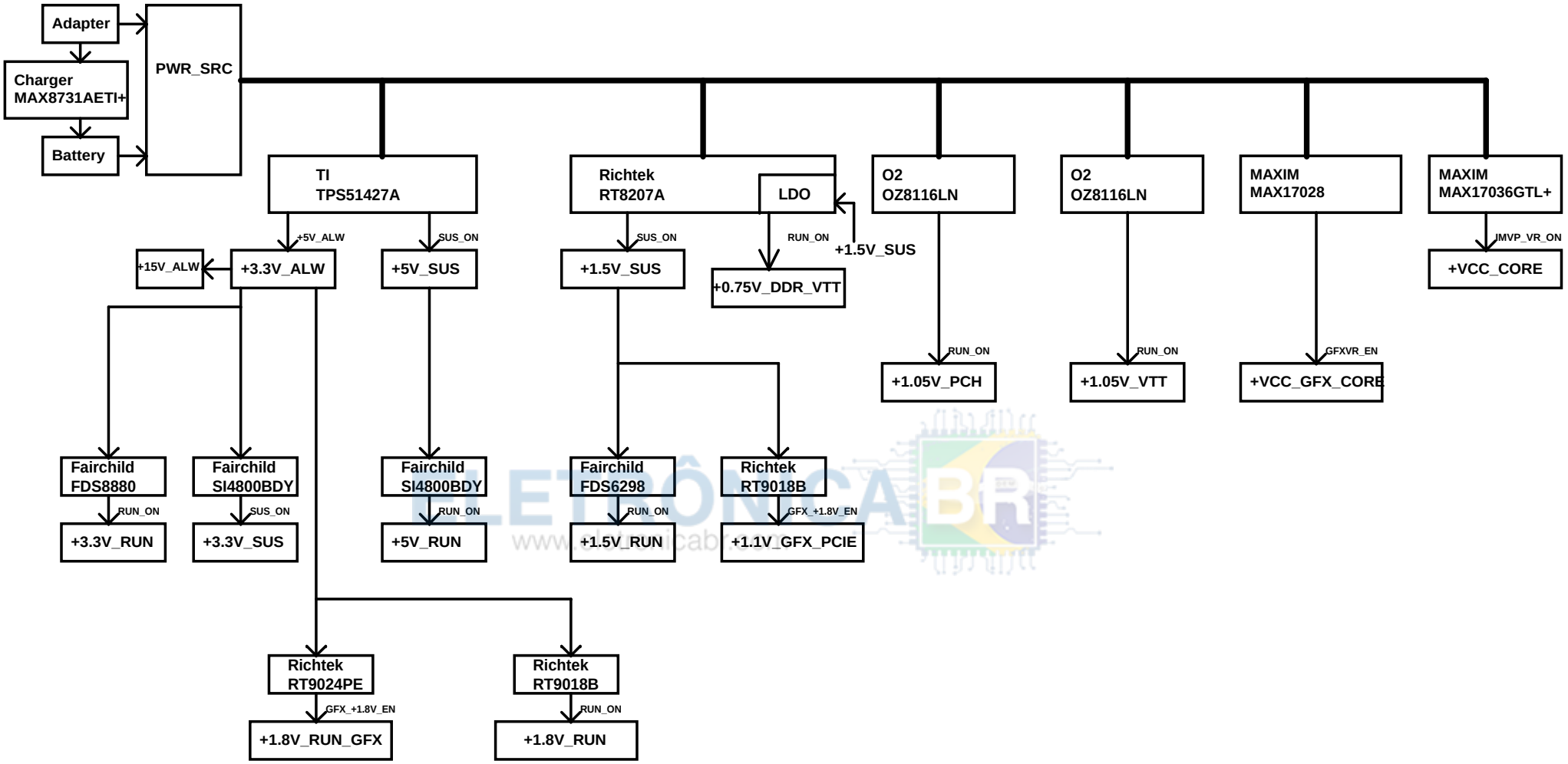
VER : 1A



QUANTA COMPUTER

Title	Schematic Block Diagram1	
Size	Document Number UM3B/UM6B	Rev 1A
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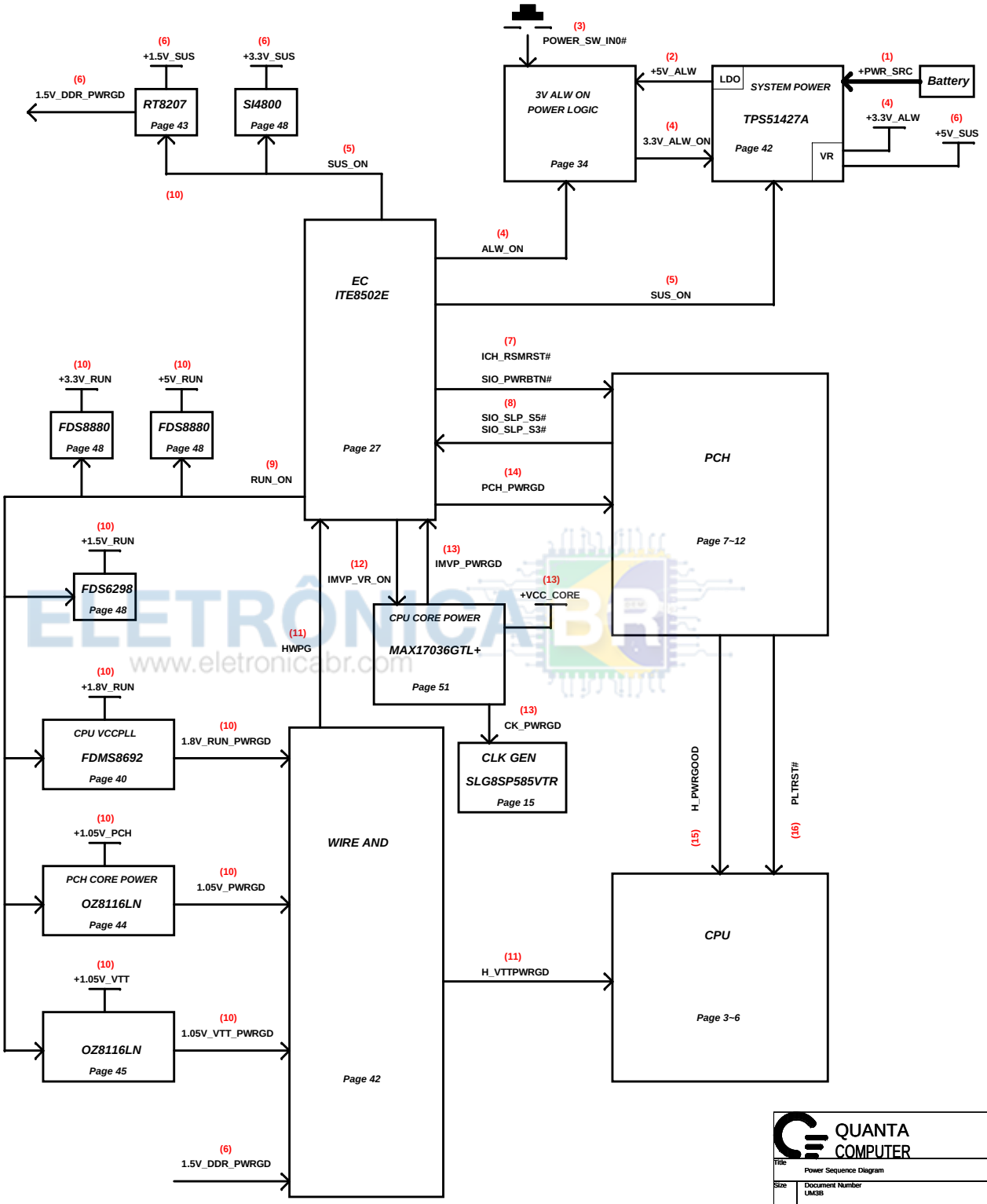
UM3 Power Design Block Diagram 2009/07/28



(1) +PWR_SRC
(2) +5V_ALW
(3) POWER_SW_IN0
(4) 3.3V_ALW_ON, +3.3V_ALW, ALW_ON
(5) SUS_ON
(6) +5V_SUS, +3.3V_SUS, +1.5V_SUS, 1.5V_DDR_PWRGD
(7) ICH_RSMRST#, SIO_PWRBTN#
(8) SIO_SLP_S5#, SIO_SLP_S4#, SIO_SLP_S3#
(9) RUN_ON
(10) +5V_RUN, +3.3V_RUN, +1.5V_RUN,+1.8V_RUN, +1.05V_VTT,+1.05V_PCH & PWRGD,+0.75V_RUN
(11) HWPG, H_VTTPWRGD
(12) IMVP_VR_ON
(13) +VCC_CORE, IMVP_PWRGD, CK_PWRGD
(14) PCH_PWRGD
(15) H_PWRGOOD
(16) PLTRST#

QUANTA COMPUTER

Title	Power Sequence Diagram	
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Title	SMBUS BLOCK	
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