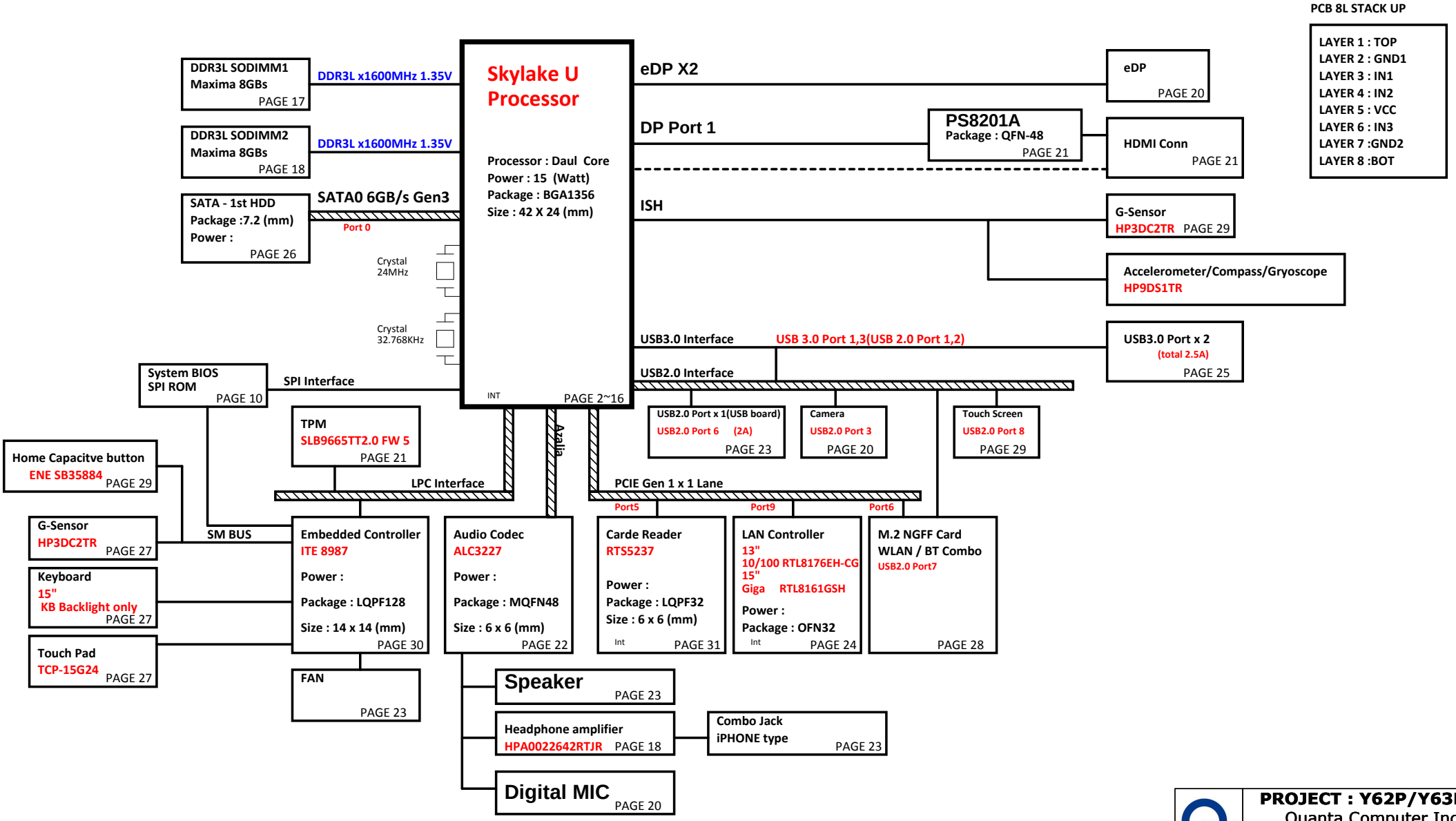
13"/15"
Intel Skylake ULT Platform Block Diagram



PROJECT : Y62P/Y63P
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

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+3V 4,10,11,12,13,14,15,16,17,18,20,21,22,23,24,25,26,27,29,30,31,37,39
+1.0V 4,6,16,30,36
+VCCIO 6,16,36
+VCCSTPLL 4,5,6,9,36,37

HDMI

21 IN_D2# → IN_D2# E55
21 IN_D2 → IN_D2 F55
21 IN_D1# → IN_D1# E58
21 IN_D1 → IN_D1 F58
21 IN_D0# → IN_D0# F53
21 IN_D0 → IN_D0 G53
21 IN_CLK# → IN_CLK# F56
21 IN_CLK → IN_CLK G56

U17A SKL_ULT ? **Need apply PN**

DDI1_TXN[0] DDI1_TXP[0] DDI1_TXN[1] DDI1_TXP[1] DDI1_TXN[2] DDI1_TXP[2] DDI1_TXN[3] DDI1_TXP[3]
DDI2_TXN[0] DDI2_TXP[0] DDI2_TXN[1] DDI2_TXP[1] DDI2_TXN[2] DDI2_TXP[2] DDI2_TXN[3] DDI2_TXP[3]
DDI
DISPLAY SIDEBANDS
EDP

EDP_TXN[0] C47 → INT_EDP_TXN0 → INT_EDP_TXN0 20
EDP_TXP[0] C46 → INT_EDP_TXP0 → INT_EDP_TXP0 20
EDP_TXN[1] D46 → INT_EDP_TXN1 → INT_EDP_TXN1 20
EDP_TXP[1] C45 → INT_EDP_TXP1 → INT_EDP_TXP1 20
EDP_TXN[2] A45
EDP_TXP[2] B45
EDP_TXN[3] A47
EDP_TXP[3] B47

EDP_AUXN E45 → INT_EDP_AUXN → INT_EDP_AUXN 20
EDP_AUXP F45 → INT_EDP_AUXP → INT_EDP_AUXP 20

EDP_DISP_UTIL B52 → TP107

DDI1_AUXN G50
DDI1_AUXP F50
DDI2_AUXN E48
DDI2_AUXP F48
DDI3_AUXN G46
DDI3_AUXP E46

GPP_E13/DDPB_HPD0 L9 → HDMI_HPD_CON → HDMI_HPD_CON 21
GPP_E14/DDPC_HPD1 L7
GPP_E15/DDPD_HPD2 L6
GPP_E16/DDPE_HPD3 N9
GPP_E17/EDP_HPD L10 → ULT_EDP_HPD → ULT_EDP_HPD 20

EDP_BKLTEN R12 → PCH_LVDS_BLON → PCH_LVDS_BLON 20
EDP_BKLTCTL R11 → PCH_DPST_PWM → PCH_DPST_PWM 20
EDP_VDDEN U13 → PCH_DISP_ON → PCH_DISP_ON 20

21 SDVO_CLK → L13 GPP_E18/DDPB_CTRLCLK
21 SDVO_DATA → L12 GPP_E19/DDPB_CTRLDATA

TP23 → DDPC_CTRLDATA → N7 GPP_E20/DDPC_CTRLCLK
N8 GPP_E21/DDPC_CTRLDATA

TP21 → DDPD_CTRLDATA → N11 GPP_E22/DDPD_CTRLCLK
N12 GPP_E23/DDPD_CTRLDATA

+VCCIO → R220 24.9/F_4 → EDP_RCOMP E52 EDP_RCOMP

SKL_ULT
REV = 1
1 OF 20
?

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Reserve EDP_HPD opposites circuit!

+3V
R30 10K_4
ULT_EDP_HPD
R51 100K_4

U17D SKL_ULT ? **Need apply PN**

30,32,37 H_PROCHOT# → R463 499/F_4 → 30 EC_PECI
30 PM_THRMTRIP#

TP117 → CATERR# → D63 CATERR#
EC_PECI A54 PECI
PROCHOT# C65 PROCHOT#
PM_THRMTRIP# C63 THERMTRIP#
A65 SKTOCC#

CPU MISC

16 XDP_BPM0 → C55 BPM#[0]
16 XDP_BPM1 → D55 BPM#[1]
B54 BPM#[2]
C56 BPM#[3]

TP94 → CPU_GP0 → A6 GPP_E3/CPU_GP0
TP92 → CPU_GP1 → A7 GPP_E7/CPU_GP1
TP55 → CPU_GP2 → BA5 GPP_B3/CPU_GP2
TP56 → CPU_GP3 → AY5 GPP_B4/CPU_GP3

R109 49.9/F_4 → PROC_POPIRCOMP AT16 PROC_POPIRCOMP
R108 49.9/F_4 → PCH_OPI_RCOMP AU16 PCH_OPIRCOMP
R273 49.9/F_4 → EDRAM_OPIO_RCOMP H66 OPCE_RCOMP
R272 49.9/F_4 → EOPIO_RCOMP H65 OPC_RCOMP

JTAG

PROC_TCK B61 → XDP_TCK0 → XDP_TCK0 16
PROC_TDI D60 → XDP_TDI_CPU → XDP_TDI_CPU 16
PROC_TDO A61 → XDP_TDO_CPU → XDP_TDO_CPU 16
PROC_TMS C60 → XDP_TMS_CPU → XDP_TMS_CPU 16
PROC_TRST# B59 → XDP_TRST#_CPU → XDP_TRST#_CPU 2,16

PCH_JTAG_TCK B56 → JTAG_TCK_PCH → JTAG_TCK_PCH 16
PCH_JTAG_TDI D59 → JTAG_TDI_PCH → JTAG_TDI_PCH 16
PCH_JTAG_TDO A56 → JTAG_TDO_PCH → JTAG_TDO_PCH 16
PCH_JTAG_TMS C59 → JTAG_TMS_PCH → JTAG_TMS_PCH 16
PCH_TRST# C61 → XDP_TRST#_CPU → XDP_TRST#_CPU 2,16
JTAGX A59 → JTAGX_PCH → JTAGX_PCH 16

SKL_ULT
REV = 1
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+VCCSTPLL
R470 *49.9/F_4 CATERR#

+1.0V
R335 *0_4/S
R326 *51_4 JTAGX_PCH
R322 51_4 JTAG_TMS_PCH
R329 51_4 JTAG_TDI_PCH
R327 51_4 JTAG_TDO_PCH
R328 51_4 JTAG_TCK_PCH

0612 Change R335 from 0 ohm to short pad

Close to Chipset

Close to EC

+VCCSTPLL
PM_THRMTRIP# R469 1K_4

Processor pull-up (CPU)
TO BE REPLACED WITH 1K OHMS FOR SKL .
470 OHM IS FOR I/P

PLACE NEAR CPU

+1.0V
XDP_TMS_CPU R336 *51_4
XDP_TDI_CPU R323 *51_4
XDP_TDO_CPU R324 *51_4

+1.0V
H_PROCHOT# R471 1K_4
XDP_TCK0 R325 51_4
XDP_TRST#_CPU R331 51_4

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Quanta Computer Inc.

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Custom	02 -- SKYPAKE 1/20(eDP/DDI)	1A
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SkyLake ULT Processor (DDR3L)

17 M_A_DQSN[7:0]
17 M_A_DQSP[7:0]
18 M_B_DQSN[7:0]
18 M_B_DQSP[7:0]
17 M_A_DQ[63:0]
18 M_B_DQ[63:0]

+1.35VSUS 6,17,18,34,36

Need apply PN

U17B — SKL_ULT — 2 OF 20

M_A_DQ0	AL71	DDR0_DQ[0]	
M_A_DQ1	AL68	DDR0_DQ[1]	
M_A_DQ2	AN68	DDR0_DQ[2]	
M_A_DQ3	AN69	DDR0_DQ[3]	
M_A_DQ4	AL70	DDR0_DQ[4]	
M_A_DQ5	AL69	DDR0_DQ[5]	
M_A_DQ6	AN70	DDR0_DQ[6]	
M_A_DQ7	AN71	DDR0_DQ[7]	
M_A_DQ8	AR70	DDR0_DQ[8]	
M_A_DQ9	AR68	DDR0_DQ[9]	
M_A_DQ10	AU71	DDR0_DQ[10]	
M_A_DQ11	AU68	DDR0_DQ[11]	
M_A_DQ12	AR71	DDR0_DQ[12]	
M_A_DQ13	AR69	DDR0_DQ[13]	
M_A_DQ14	AU70	DDR0_DQ[14]	
M_A_DQ15	AU69	DDR0_DQ[15]	
M_B_DQ0	AF65	DDR1_DQ[0]/DDR0_DQ[16]	
M_B_DQ1	AF64	DDR1_DQ[1]/DDR0_DQ[17]	
M_B_DQ2	AK65	DDR1_DQ[2]/DDR0_DQ[18]	
M_B_DQ3	AK64	DDR1_DQ[3]/DDR0_DQ[19]	
M_B_DQ4	AF66	DDR1_DQ[4]/DDR0_DQ[20]	
M_B_DQ5	AF67	DDR1_DQ[5]/DDR0_DQ[21]	
M_B_DQ6	AK67	DDR1_DQ[6]/DDR0_DQ[22]	
M_B_DQ7	AK66	DDR1_DQ[7]/DDR0_DQ[23]	
M_B_DQ8	AF70	DDR1_DQ[8]/DDR0_DQ[24]	
M_B_DQ9	AF68	DDR1_DQ[9]/DDR0_DQ[25]	
M_B_DQ10	AH71	DDR1_DQ[10]/DDR0_DQ[26]	
M_B_DQ11	AH68	DDR1_DQ[11]/DDR0_DQ[27]	
M_B_DQ12	AF71	DDR1_DQ[12]/DDR0_DQ[28]	
M_B_DQ13	AF69	DDR1_DQ[13]/DDR0_DQ[29]	
M_B_DQ14	AH70	DDR1_DQ[14]/DDR0_DQ[30]	
M_B_DQ15	AH69	DDR1_DQ[15]/DDR0_DQ[31]	
M_A_DQ16	BB65	DDR0_DQ[16]/DDR0_DQ[32]	
M_A_DQ17	AW65	DDR0_DQ[17]/DDR0_DQ[33]	
M_A_DQ18	AW63	DDR0_DQ[18]/DDR0_DQ[34]	
M_A_DQ19	AY63	DDR0_DQ[19]/DDR0_DQ[35]	
M_A_DQ20	BA65	DDR0_DQ[20]/DDR0_DQ[36]	
M_A_DQ21	AY65	DDR0_DQ[21]/DDR0_DQ[37]	
M_A_DQ22	BA63	DDR0_DQ[22]/DDR0_DQ[38]	
M_A_DQ23	BB63	DDR0_DQ[23]/DDR0_DQ[39]	
M_A_DQ24	BA61	DDR0_DQ[24]/DDR0_DQ[40]	
M_A_DQ25	AW61	DDR0_DQ[25]/DDR0_DQ[41]	
M_A_DQ26	BB59	DDR0_DQ[26]/DDR0_DQ[42]	
M_A_DQ27	AW59	DDR0_DQ[27]/DDR0_DQ[43]	
M_A_DQ28	BB61	DDR0_DQ[28]/DDR0_DQ[44]	
M_A_DQ29	AY61	DDR0_DQ[29]/DDR0_DQ[45]	
M_A_DQ30	BA59	DDR0_DQ[30]/DDR0_DQ[46]	
M_A_DQ31	AY59	DDR0_DQ[31]/DDR0_DQ[47]	
M_B_DQ16	AT66	DDR1_DQ[16]/DDR0_DQ[48]	
M_B_DQ17	AT65	DDR1_DQ[17]/DDR0_DQ[49]	
M_B_DQ18	AP65	DDR1_DQ[18]/DDR0_DQ[50]	
M_B_DQ19	AN65	DDR1_DQ[19]/DDR0_DQ[51]	
M_B_DQ20	AN66	DDR1_DQ[20]/DDR0_DQ[52]	
M_B_DQ21	AP66	DDR1_DQ[21]/DDR0_DQ[53]	
M_B_DQ22	AT65	DDR1_DQ[22]/DDR0_DQ[54]	
M_B_DQ23	AU65	DDR1_DQ[23]/DDR0_DQ[55]	
M_B_DQ24	AT61	DDR1_DQ[24]/DDR0_DQ[56]	
M_B_DQ25	AU61	DDR1_DQ[25]/DDR0_DQ[57]	
M_B_DQ26	AP60	DDR1_DQ[26]/DDR0_DQ[58]	
M_B_DQ27	AN60	DDR1_DQ[27]/DDR0_DQ[59]	
M_B_DQ28	AN61	DDR1_DQ[28]/DDR0_DQ[60]	
M_B_DQ29	AP61	DDR1_DQ[29]/DDR0_DQ[61]	
M_B_DQ30	AT60	DDR1_DQ[30]/DDR0_DQ[62]	
M_B_DQ31	AU60	DDR1_DQ[31]/DDR0_DQ[63]	

		DDR0_CKN[0]	
		DDR0_CKP[0]	
		DDR0_CKN[1]	
		DDR0_CKP[1]	
		DDR0_CKE[0]	
		DDR0_CKE[1]	
		DDR0_CKE[2]	
		DDR0_CKE[3]	
		DDR0_CS#[0]	
		DDR0_CS#[1]	
		DDR0_ODT[0]	
		DDR0_ODT[1]	
		DDR0_MA[5]/DDR0_CAA[0]/DDR0_MA[5]	
		DDR0_MA[9]/DDR0_CAA[1]/DDR0_MA[9]	
		DDR0_MA[6]/DDR0_CAA[2]/DDR0_MA[6]	
		DDR0_MA[8]/DDR0_CAA[3]/DDR0_MA[8]	
		DDR0_MA[7]/DDR0_CAA[4]/DDR0_MA[7]	
		DDR0_BA[2]/DDR0_CAA[5]/DDR0_BG[0]	
		DDR0_MA[12]/DDR0_CAA[6]/DDR0_MA[12]	
		DDR0_MA[11]/DDR0_CAA[7]/DDR0_MA[11]	
		DDR0_MA[15]/DDR0_CAA[8]/DDR0_ACT#	
		DDR0_MA[14]/DDR0_CAA[9]/DDR0_BG[1]	
		DDR0_MA[13]/DDR0_CAB[0]/DDR0_MA[13]	
		DDR0_CAS#/DDR0_CAB[1]/DDR0_MA[15]	
		DDR0_WE#/DDR0_CAB[2]/DDR0_MA[14]	
		DDR0_RAS#/DDR0_CAB[3]/DDR0_MA[16]	
		DDR0_BA[0]/DDR0_CAB[4]/DDR0_BA[0]	
		DDR0_MA[2]/DDR0_CAB[5]/DDR0_MA[2]	
		DDR0_BA[1]/DDR0_CAB[6]/DDR0_BA[1]	
		DDR0_MA[10]/DDR0_CAB[7]/DDR0_MA[10]	
		DDR0_MA[1]/DDR0_CAB[8]/DDR0_MA[1]	
		DDR0_MA[0]/DDR0_CAB[9]/DDR0_MA[0]	
		DDR0_MA[3]	
		DDR0_MA[4]	
		DDR0_DQSN[0]	
		DDR0_DQSP[0]	
		DDR0_DQSN[1]	
		DDR0_DQSP[1]	
		DDR1_DQSN[0]/DDR0_DQSN[2]	
		DDR1_DQSP[0]/DDR0_DQSP[2]	
		DDR1_DQSN[1]/DDR0_DQSN[3]	
		DDR1_DQSP[1]/DDR0_DQSP[3]	
		DDR0_DQSN[2]/DDR0_DQSN[4]	
		DDR0_DQSP[2]/DDR0_DQSP[4]	
		DDR0_DQSN[3]/DDR0_DQSN[5]	
		DDR0_DQSP[3]/DDR0_DQSP[5]	
		DDR1_DQSN[2]/DDR0_DQSN[6]	
		DDR1_DQSP[2]/DDR0_DQSP[6]	
		DDR1_DQSN[3]/DDR0_DQSN[7]	
		DDR1_DQSP[3]/DDR0_DQSP[7]	
		DDR0_ALERT#	
		DDR0_PAR	
		DDR_VREF_CA	
		DDR0_VREF_DQ	
		DDR1_VREF_DQ	
		DDR_VTT_CNTL	

NIL-DDR CH - A

	AU53	M_A_CLKN0	17
	AT53	M_A_CLKP0	17
	AU55	M_A_CLKN1	17
	AT55	M_A_CLKP1	17
	BA56		
	BB56	M_A_CKE0	17
	AW56	M_A_CKE1	17
	AY56		
	AU45		
	AU43	M_A_CS#0	17
	AT45	M_A_CS#1	17
	AT43	M_A_DIM0_ODT0	17
		M_A_DIM0_ODT1	17
BA51	M_A_A5	M_A_A5	17
BB54	M_A_A9	M_A_A9	17
BA52	M_A_A6	M_A_A6	17
AY52	M_A_A8	M_A_A8	17
AW52	M_A_A7	M_A_A7	17
AY55	M_A_BS#2	M_A_BS#2	17
AW54	M_A_A12	M_A_A12	17
BA54	M_A_A11	M_A_A11	17
BA55	M_A_A15	M_A_A15	17
AY54	M_A_A14	M_A_A14	17
AU46	M_A_A13	M_A_A13	17
AU48		M_A_CAS#	17
AT46		M_A_WE#	17
AU50		M_A_RAS#	17
AU52		M_A_BS#0	17
AY51	M_A_A2	M_A_A2	17
AT48		M_A_BS#1	17
AT50	M_A_A10	M_A_A10	17
BB50	M_A_A1	M_A_A1	17
AY50	M_A_A0	M_A_A0	17
BA50	M_A_A3	M_A_A3	17
BB52	M_A_A4	M_A_A4	17
AM70	M_A_DQSN0		
AM69	M_A_DQSP0		
AT69	M_A_DQSN1		
AT70	M_A_DQSP1		
AH66	M_B_DQSN0		
AH65	M_B_DQSP0		
AG69	M_B_DQSN1		
AG70	M_B_DQSP1		
BA64	M_A_DQSN2		
AY64	M_A_DQSP2		
AV60	M_A_DQSN3		
AA60	M_A_DQSP3		
AR66	M_B_DQSN2		
AR65	M_B_DQSP2		
AR61	M_B_DQSN3		
AR60	M_B_DQSP3		
AW50			
AT52	DDR0_PAR		
AY67	SM_VREF	SM_VREF	17
AY68	SMDDR_VREF_DQ0_M3	SMDDR_VREF_DQ0_M3	17
BA67	SMDDR_VREF_DQ1_M3	SMDDR_VREF_DQ1_M3	18
AW67	DDR_VTT_CNTL	DDR_VTT_CNTL	4,18

TP44

20mils width

SKL_ULT REV = 1

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Need apply PN

M_A_DQ32	AY39	DDR0_DQ[32]/DDR1_DQ[0]	
M_A_DQ33	AW39	DDR0_DQ[33]/DDR1_DQ[1]	
M_A_DQ34	AY37	DDR0_DQ[34]/DDR1_DQ[2]	
M_A_DQ35	AW37	DDR0_DQ[35]/DDR1_DQ[3]	
M_A_DQ36	BB39	DDR0_DQ[36]/DDR1_DQ[4]	
M_A_DQ37	BA39	DDR0_DQ[37]/DDR1_DQ[5]	
M_A_DQ38	BA37	DDR0_DQ[38]/DDR1_DQ[6]	
M_A_DQ39	BB37	DDR0_DQ[39]/DDR1_DQ[7]	
M_A_DQ40	AY35	DDR0_DQ[40]/DDR1_DQ[8]	
M_A_DQ41	AW35	DDR0_DQ[41]/DDR1_DQ[9]	
M_A_DQ42	AY33	DDR0_DQ[42]/DDR1_DQ[10]	
M_A_DQ43	AW33	DDR0_DQ[43]/DDR1_DQ[11]	
M_A_DQ44	BB35	DDR0_DQ[44]/DDR1_DQ[12]	
M_A_DQ45	BA35	DDR0_DQ[45]/DDR1_DQ[13]	
M_A_DQ46	BA33	DDR0_DQ[46]/DDR1_DQ[14]	
M_A_DQ47	BB33	DDR0_DQ[47]/DDR1_DQ[15]	
M_B_DQ32	AU40	DDR1_DQ[32]/DDR1_DQ[16]	
M_B_DQ33	AT40	DDR1_DQ[33]/DDR1_DQ[17]	
M_B_DQ34	AT37	DDR1_DQ[34]/DDR1_DQ[18]	
M_B_DQ35	AU37	DDR1_DQ[35]/DDR1_DQ[19]	
M_B_DQ36	AR40	DDR1_DQ[36]/DDR1_DQ[20]	
M_B_DQ37	AP40	DDR1_DQ[37]/DDR1_DQ[21]	
M_B_DQ38	AP37	DDR1_DQ[38]/DDR1_DQ[22]	
M_B_DQ39	AR37	DDR1_DQ[39]/DDR1_DQ[23]	
M_B_DQ40	AT33	DDR1_DQ[40]/DDR1_DQ[24]	
M_B_DQ41	AU33	DDR1_DQ[41]/DDR1_DQ[25]	
M_B_DQ42	AU30	DDR1_DQ[42]/DDR1_DQ[26]	
M_B_DQ43	AT30	DDR1_DQ[43]/DDR1_DQ[27]	
M_B_DQ44	AR33	DDR1_DQ[44]/DDR1_DQ[28]	
M_B_DQ45	AP33	DDR1_DQ[45]/DDR1_DQ[29]	
M_B_DQ46	AR30	DDR1_DQ[46]/DDR1_DQ[30]	
M_B_DQ47	AP30	DDR1_DQ[47]/DDR1_DQ[31]	
M_A_DQ48	AY31	DDR1_DQ[48]/DDR1_DQ[32]	
M_A_DQ49	AW31	DDR1_DQ[49]/DDR1_DQ[33]	
M_A_DQ50	AY29	DDR1_DQ[50]/DDR1_DQ[34]	
M_A_DQ51	AW29	DDR1_DQ[51]/DDR1_DQ[35]	
M_A_DQ52	BB31	DDR1_DQ[52]/DDR1_DQ[36]	
M_A_DQ53	BA31	DDR1_DQ[53]/DDR1_DQ[37]	
M_A_DQ54	BA29	DDR1_DQ[54]/DDR1_DQ[38]	
M_A_DQ55	BB29	DDR1_DQ[55]/DDR1_DQ[39]	
M_A_DQ56	AY27	DDR1_DQ[56]/DDR1_DQ[40]	
M_A_DQ57	AW27	DDR1_DQ[57]/DDR1_DQ[41]	
M_A_DQ58	AY25	DDR1_DQ[58]/DDR1_DQ[42]	
M_A_DQ59	AW25	DDR1_DQ[59]/DDR1_DQ[43]	
M_A_DQ60	BB27	DDR1_DQ[60]/DDR1_DQ[44]	
M_A_DQ61	BA27	DDR1_DQ[61]/DDR1_DQ[45]	
M_A_DQ62	BA25	DDR1_DQ[62]/DDR1_DQ[46]	
M_A_DQ63	BB25	DDR1_DQ[63]/DDR1_DQ[47]	
M_B_DQ48	AU27	DDR1_DQ[48]	
M_B_DQ49	AT27	DDR1_DQ[49]	
M_B_DQ50	AT25	DDR1_DQ[50]	
M_B_DQ51	AU25	DDR1_DQ[51]	
M_B_DQ52	AP27	DDR1_DQ[52]	
M_B_DQ53	AN27	DDR1_DQ[53]	
M_B_DQ54	AN25	DDR1_DQ[54]	
M_B_DQ55	AP25	DDR1_DQ[55]	
M_B_DQ56	AT22	DDR1_DQ[56]	
M_B_DQ57	AU22	DDR1_DQ[57]	
M_B_DQ58	AU21	DDR1_DQ[58]	
M_B_DQ59	AT21	DDR1_DQ[59]	
M_B_DQ60	AN22	DDR1_DQ[60]	
M_B_DQ61	AP22	DDR1_DQ[61]	
M_B_DQ62	AP21	DDR1_DQ[62]	
M_B_DQ63	AN21	DDR1_DQ[63]	

		DDR1_CKN[0]	
		DDR1_CKN[1]	
		DDR1_CKP[0]	
		DDR1_CKP[1]	
		DDR1_CKE[0]	
		DDR1_CKE[1]	
		DDR1_CKE[2]	
		DDR1_CKE[3]	
		DDR1_CS#[0]	
		DDR1_CS#[1]	
		DDR1_ODT[0]	
		DDR1_ODT[1]	
		DDR1_MA[5]/DDR1_CAA[0]/DDR1_MA[5]	
		DDR1_MA[9]/DDR1_CAA[1]/DDR1_MA[9]	
		DDR1_MA[6]/DDR1_CAA[2]/DDR1_MA[6]	
		DDR1_MA[8]/DDR1_CAA[3]/DDR1_MA[8]	
		DDR1_MA[7]/DDR1_CAA[4]/DDR1_MA[7]	
		DDR1_BA[2]/DDR1_CAA[5]/DDR1_BG[0]	
		DDR1_MA[12]/DDR1_CAA[6]/DDR1_MA[12]	
		DDR1_MA[11]/DDR1_CAA[7]/DDR1_MA[11]	
		DDR1_MA[15]/DDR1_CAA[8]/DDR1_ACT#	
		DDR1_MA[14]/DDR1_CAA[9]/DDR1_BG[1]	
		DDR1_MA[13]/DDR1_CAB[0]/DDR1_MA[13]	
		DDR1_CAS#/DDR1_CAB[1]/DDR1_MA[15]	
		DDR1_WE#/DDR1_CAB[2]/DDR1_MA[14]	
		DDR1_RAS#/DDR1_CAB[3]/DDR1_MA[16]	
		DDR1_BA[0]/DDR1_CAB[4]/DDR1_BA[0]	
		DDR1_MA[2]/DDR1_CAB[5]/DDR1_MA[2]	
		DDR1_BA[1]/DDR1_CAB[6]/DDR1_BA[1]	
		DDR1_MA[10]/DDR1_CAB[7]/DDR1_MA[10]	
		DDR1_MA[1]/DDR1_CAB[8]/DDR1_MA[1]	
		DDR1_MA[0]/DDR1_CAB[9]/DDR1_MA[0]	
		DDR1_MA[3]	
		DDR1_MA[4]	
		DDR0_DQSN[4]/DDR1_DQSN[0]	
		DDR0_DQSP[4]/DDR1_DQSP[0]	
		DDR0_DQSN[5]/DDR1_DQSN[1]	
		DDR0_DQSP[5]/DDR1_DQSP[1]	
		DDR1_DQSN[4]/DDR1_DQSN[2]	
		DDR1_DQSP[4]/DDR1_DQSP[2]	
		DDR1_DQSN[5]/DDR1_DQSN[3]	
		DDR1_DQSP[5]/DDR1_DQSP[3]	
		DDR0_DQSN[6]/DDR1_DQSN[4]	
		DDR0_DQSP[6]/DDR1_DQSP[4]	
		DDR0_DQSN[7]/DDR1_DQSN[5]	
		DDR0_DQSP[7]/DDR1_DQSP[5]	
		DDR1_DQSN[6]	
		DDR1_DQSP[6]	
		DDR1_DQSN[7]	
		DDR1_DQSP[7]	
		DDR1_ALERT#	
		DDR1_PAR	
		DRAM_RESET#	
		DDR_RCOMP[0]	
		DDR_RCOMP[1]	
		DDR_RCOMP[2]	

NIL-DDR CH - B

	AN45	M_B_CLKN0	18
	AN46	M_B_CLKN1	18
	AP45	M_B_CLKP0	18
	AP46	M_B_CLKP1	18
	AN56		
	AP55	M_B_CKE0	18
	AN55	M_B_CKE1	18
	AP53		
	BB42		
	AY42	M_B_CS#0	18
	BA42	M_B_CS#1	18
	AW42	M_B_DIM0_ODT0	18
		M_B_DIM0_ODT1	18
AY48	M_B_A5	M_B_A5	18
AP50	M_B_A9	M_B_A9	18
BA48	M_B_A6	M_B_A6	18
BB48	M_B_A8	M_B_A8	18
AP48	M_B_A7	M_B_A7	18
AP52		M_B_BS#2	18
AN50	M_B_A12	M_B_A12	18
AN48	M_B_A11	M_B_A11	18
AN53	M_B_A15	M_B_A15	18
AN52	M_B_A14	M_B_A14	18
BA43	M_B_A13	M_B_A13	18
AY43		M_B_CAS#	18
AY44		M_B_WE#	18
AW44		M_B_RAS#	18
BB44		M_B_BS#0	18
AY47	M_B_A2	M_B_A2	18
BA44		M_B_BS#1	18
AW46	M_B_A10	M_B_A10	18
AY46	M_B_A1	M_B_A1	18
BA46	M_B_A0	M_B_A0	18
BB46	M_B_A3	M_B_A3	18
BA47	M_B_A4	M_B_A4	18
BA38	M_A_DQSN4		
AY38	M_A_DQSP4		
AY34	M_A_DQSN5		
BA34	M_A_DQSP5		
AT38	M_B_DQSN4		
AR38	M_B_DQSP4		
AT32	M_B_DQSN5		
AR32	M_B_DQSP5		
BA30	M_A_DQSN6		
AY30	M_A_DQSP6		
AY26	M_A_DQSN7		
BA26	M_A_DQSP7		
AR25	M_B_DQSN6		
AR27	M_B_DQSP6		
AT22	M_B_DQSN7		
AR21	M_B_DQSP7		
AP43	DDR1_PAR		
AT13	SM_DRAMRST#		
AR18	SM_RCOMP_0	R164	121/F_4
AT18	SM_RCOMP_1	R158	80.6/F_4
AU18	SM_RCOMP_2	R154	100/F_4

TP42

+1.35VSUS

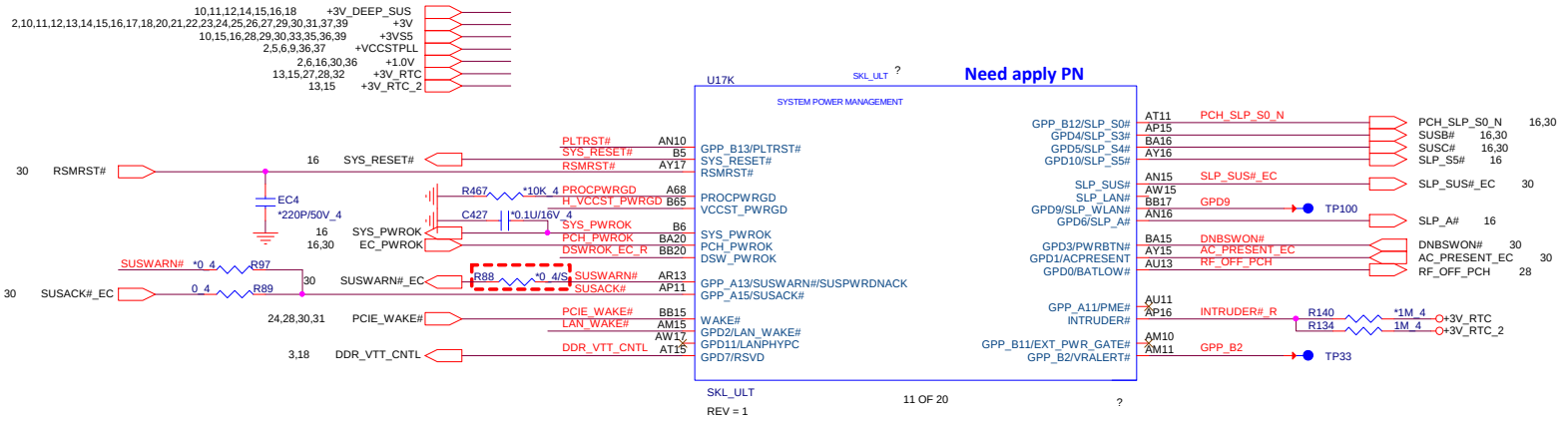
R293 470_4

DDR3_DRAMRST# 17,18

SKL_ULT REV = 1

PROJECT : Y62P/Y63P
Quanta Computer Inc.

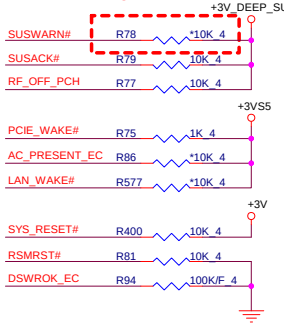
Size	Document Number	Rev
Custom	03 -- SKYPAKE 3/20(DDR3-A I/F)	1A
Date: Wednesday, July 22, 2015	Sheet 3 of 42	



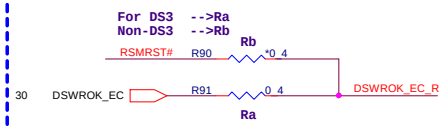
0612 Change R88 from 0 ohm to short pad

PCH Pull-high/low(CLG)

6/12 Change R78 from I to NI



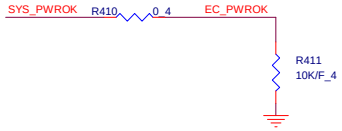
For DS3 Sequence

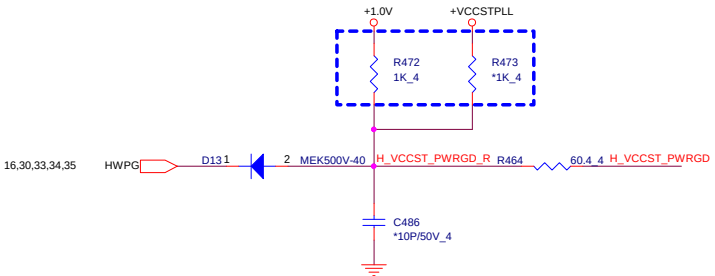


PLTRST#(CLG)

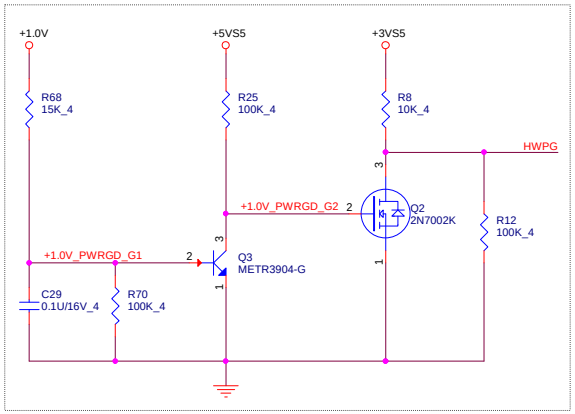
Check Q2010 Rise/Fall time less than 100ns

System PWR_OK(CLG)

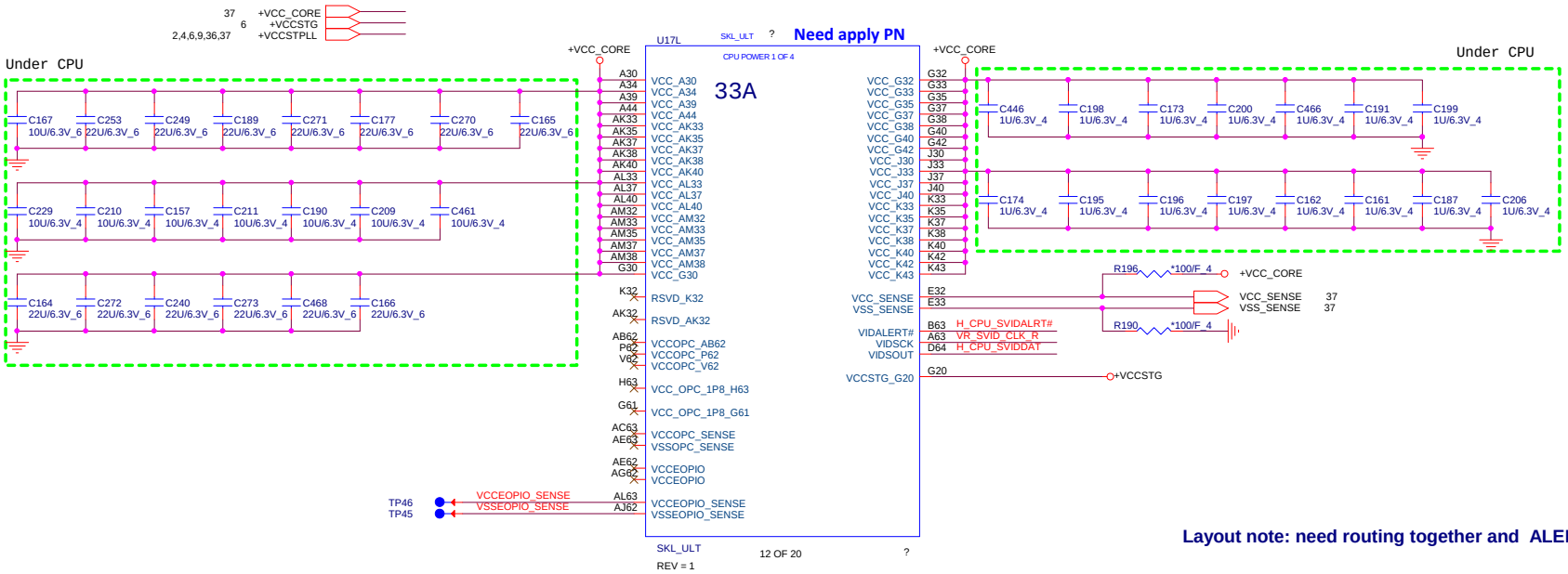


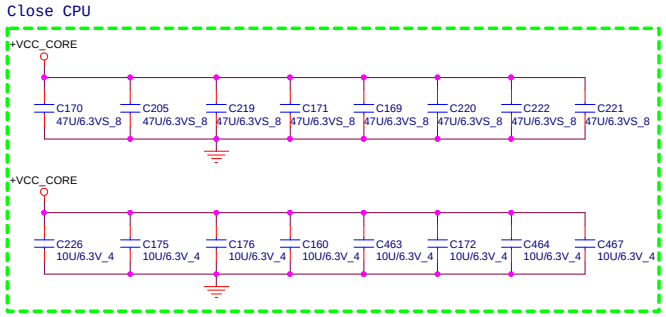


Close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"



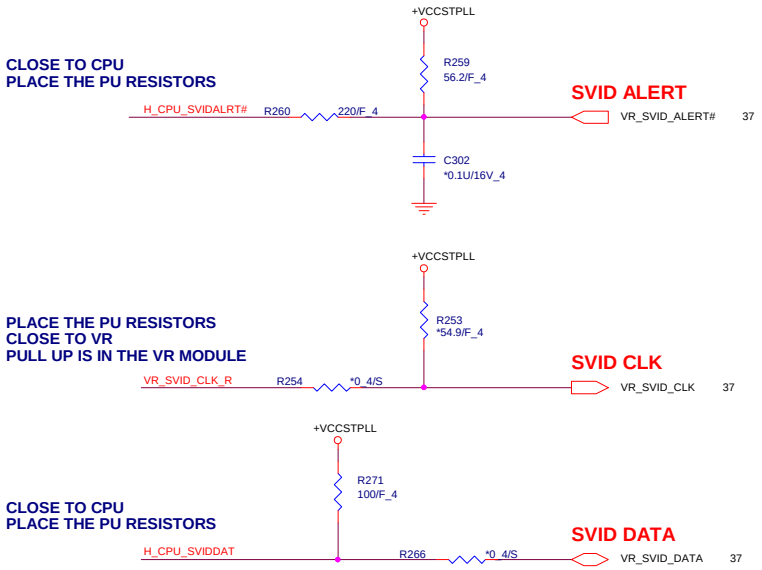
PROJECT : Y62P/Y63P Quanta Computer Inc.		
Size: Custom	Document Number: 04 -- SKYPAKE 5/20(Power Manger)	Rev: 1A
Date: Wednesday, July 22, 2015	Sheet 4 of 42	





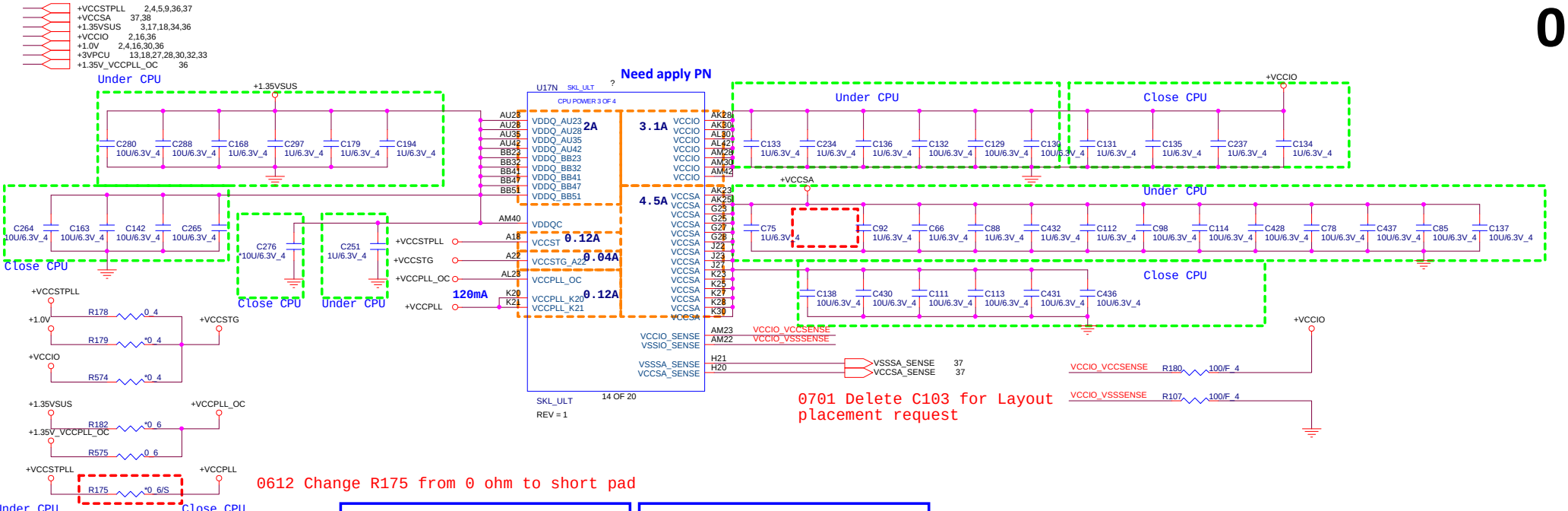
Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
$V_{CC_{GT}}$	Processor Graphics Power Rails	SVID
$V_{CC_{GTX}}$	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
$V_{CC_{SA}}$	System Agent Power Rail	SVID/Fixed (SKU dependent)
$V_{CC_{IO}}$	IO Power Rail	Fixed
$V_{CC_{ST}}$	Sustain Power Rail	Fixed
$V_{CC_{PLL}}$	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
$V_{CC_{OPC}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{OPC\_1P8}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{EOPIO}}$	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

Layout note: need routing together and ALERT need between CLK and DATA.

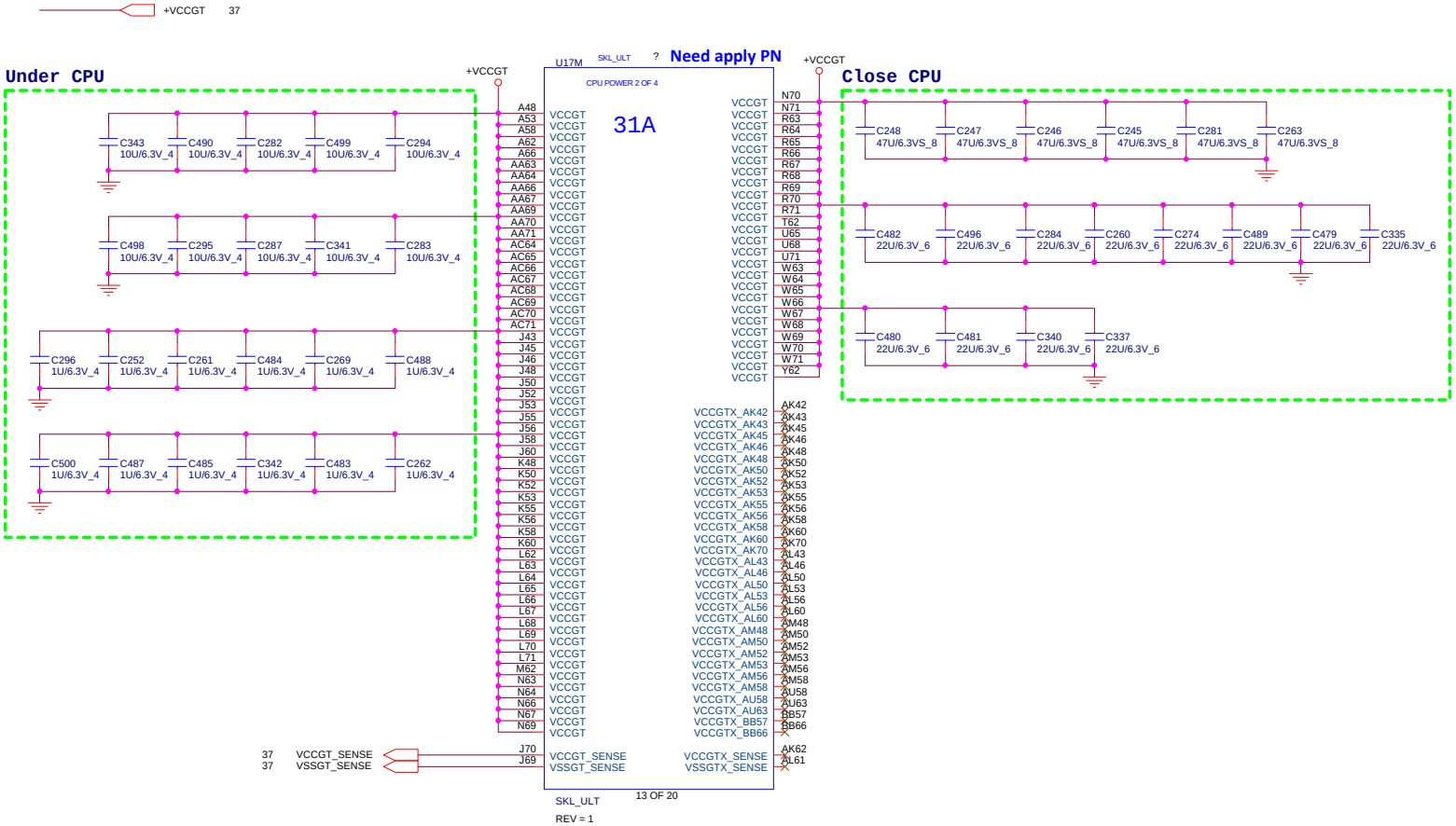


PROJECT : Y62P/Y63P
Quanta Computer Inc.

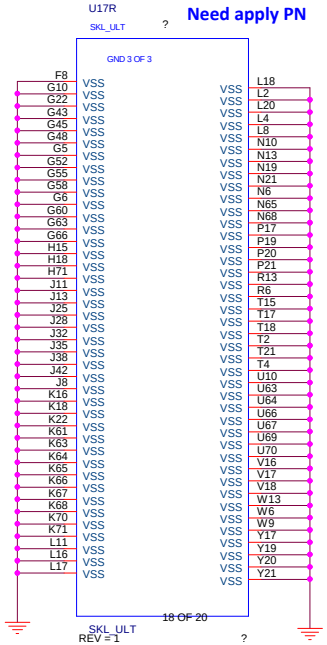
Size	Document Number	Rev
Custom	05 -- SKYPAKE 6/20 (POWER-1)	1A
Date: Wednesday, July 22, 2015	Sheet 5 of 42	

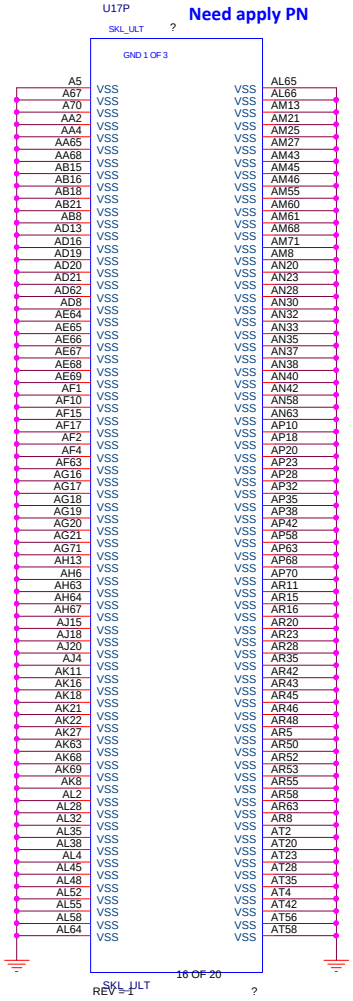


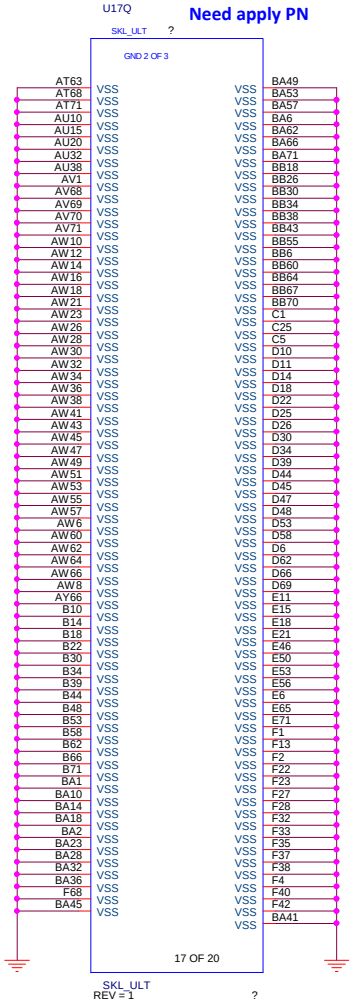
Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



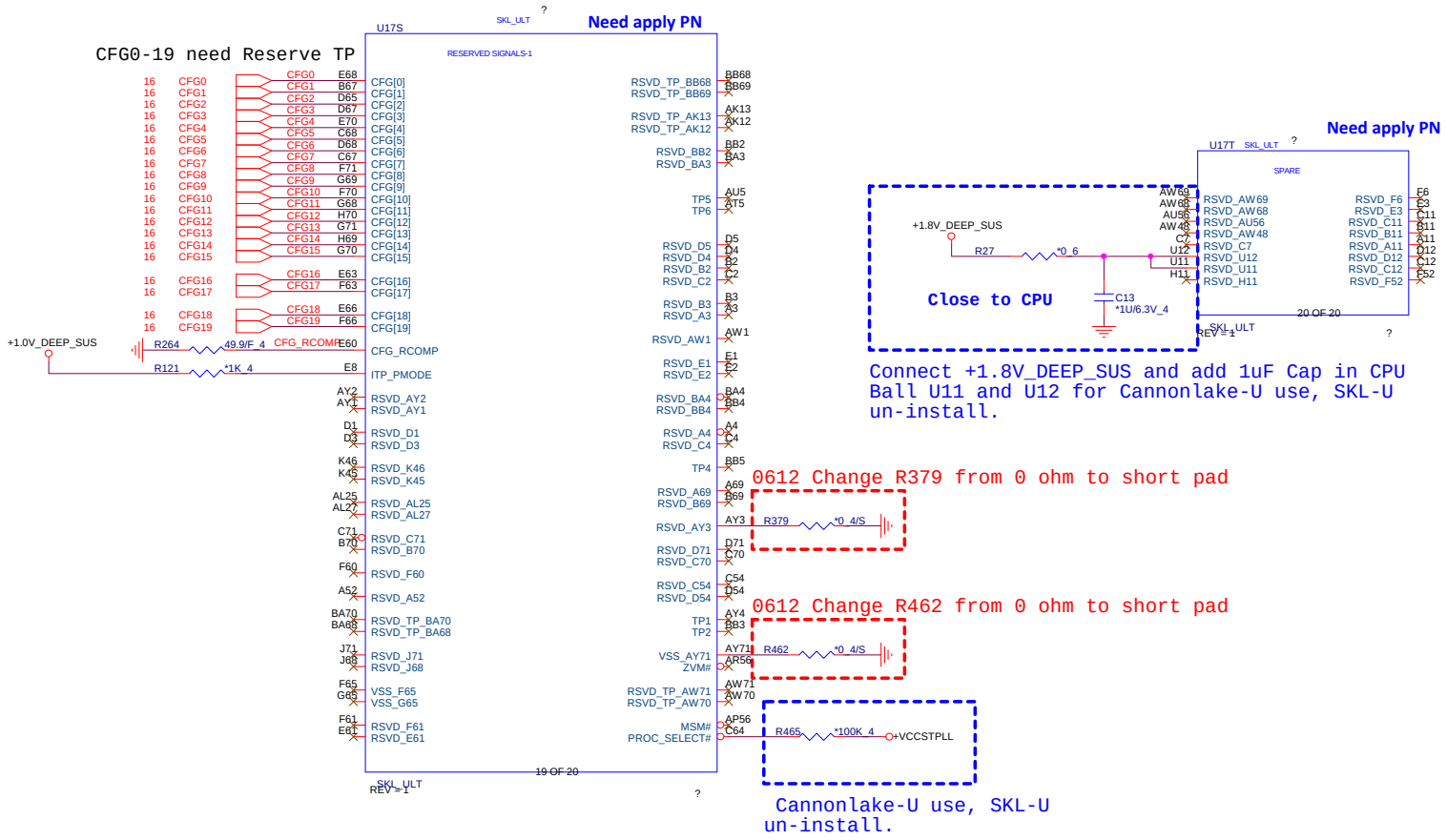




PROJECT : Y62P/Y63P
Quanta Computer Inc.

Size	Document Number	Rev
Custom	8 -- SKYPAKE 9/20 (GND-1)	1A
Date: Wednesday, July 22, 2015	Sheet 8 of 42	

+1.0V_DEEP_SUS 13,15,16,35,36
+VCCSTPLL 2,4,5,6,36,37



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physcial Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R466 *1K_4
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R468 1K_4

PROJECT : Y62P/Y63P
Quanta Computer Inc.

Size	Document Number	Rev
Custom	9 -- SKYPAKE 12/20 (RSV-1)	1A
Date: Wednesday, July 22, 2015	Sheet 9 of 42	

+3V_DEEP_SUS 4,11,12,14,15,16,18
+3V 2,4,11,12,13,14,15,16,17,18,20,21,22,23,24,25,26,27,29,30,31,37,39
+3VS5 4,15,16,28,29,30,33,35,36,39

Need apply PN

U17E

SKL_ULT

SPI - FLASH

PCH_SPI1_CLK AV2 SPI0_CLK
PCH_SPI1_SO AW3 SPI0_MISO
PCH_SPI1_SI AV3 SPI0_MOSI
PCH_SPI_IO2 AW2 SPI0_IO2
PCH_SPI_IO3 AU4 SPI0_IO3
PCH_SPI_CS0# AU3 SPI0_CS0#
AU2 SPI0_CS1#
AU1 SPI0_CS2#

SPI - TOUCH

TP83 SPI1_CLK M2 GPP_D1/SPI1_CLK
30 SIO_EXT_SMI# SIO_EXT_SMI# M3 GPP_D2/SPI1_MISO
30 PCI_SERR# PCI_SERR# J4 GPP_D3/SPI1_MOSI
SPI1_IO2 V1 GPP_D21/SPI1_IO2
TP87 SPI1_IO3 V2 GPP_D22/SPI1_IO3
TP64 SPI1_CS# M1 GPP_D0/SPI1_CS#
TP57

C LINK

G3 CL_CLK
G2 CL_DATA
G1 CL_RST#

30 EC_RCIN# AW13 GPP_A0/RCIN#
26,30 SERIRQ AY11 GPP_A6/SERIRQ

SKL_ULT
REV = 1

5 OF 20

SMBUS, SMLINK

GPP_C0/SMBCLK R7 SMB_PCH_CLK
GPP_C1/SMBDATA R8 SMB_PCH_DAT
GPP_C2/SMBALERT# R10 SML0ALERT# 11
GPP_C3/SML0CLK R9 SMB_ME0_CLK
GPP_C4/SML0DATA W2 SMB_ME0_DAT
GPP_C5/SML0ALERT# W1 SML1ALERT# 11
GPP_C6/SML1CLK W3 SMB_ME1_CLK
GPP_C7/SML1DATA V3 SMB_ME1_DAT
GPP_B23/SML1ALERT#/PCHHOT# AM7 GPP_B23 TP14

LPC

GPP_A1/LAD0/ESPI_IO0 AY13 LAD0 26,28,30
GPP_A2/LAD1/ESPI_IO1 BA13 LAD1 26,28,30
GPP_A3/LAD2/ESPI_IO2 BB13 LAD2 26,28,30
GPP_A4/LAD3/ESPI_IO3 AY12 LAD3 26,28,30
GPP_A5/LFRAME#/ESPI_CS# BA12 LFRAME# 26,28,30
GPP_A14/SUS_STAT#/ESPI_RESET# BA11

GPP_A9/CLKOUT_LPC0/ESPI_CLK AW9 CLK_PCI_EC_R R111 22/F_4 EC6 18P/50V_4 CLK_24M_KBC 30
GPP_A10/CLKOUT_LPC1 AY9 CLK_PCI_LPC_R R120 22/F_4 CLK_24M_DEBUG 28
GPP_A8/CLKRUN# AW11 CLKRUN# CLKRUN# 30
EC8 18P/50V_4 EMI(near PCH)
R115 22/F_4 CLK_PCI_TPM 26
EC7 *18P/50V_4 EMI(near PCH)

GPIO Pull UP

+3V
SERIRQ R44 10K_4
CLKRUN# R43 8.2K/F_4
SIO_EXT_SMI# R401 10K_4
EC_RCIN# R45 10K_4
PCI_SERR# R406 10K_4

+3V_DEEP_SUS
SMB_PCH_CLK R14 2.2K_4
SMB_PCH_DAT R13 2.2K_4
SMB_ME0_CLK R38 499/F_4
SMB_ME0_DAT R396 499/F_4
SMB_ME1_CLK R394 1K_4
SMB_ME1_DAT R393 1K_4
R405 10K_4
12,26 ACC_LED#

SMBus/Pull-up(CLG)

Q24 +3V
18,30 MBCLK2 SMB_ME1_CLK
18,30 MBDATA2 SMB_ME1_DAT
*2N7002DW

CPU heat pipe local thermal sensor
DDR thermal sensor
EC

Q1 +3V
+3V R24 4.7K_4
16,17,18,27 SMB_RUN_DAT SMB_PCH_DAT
+3V R16 4.7K_4
16,17,18,27 SMB_RUN_CLK SMB_PCH_CLK
2N7002KDW

Touch Pad
XDP
DDR3-L

PCH SPI ROM(CLG)

Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

4M SPI ROM Socket

30 PCH_SPI_CS0#_R
30 PCH_SPI1_CLK_R
30 PCH_SPI1_SI_R
30 PCH_SPI1_SO_R

U14
PCH_SPI_CS0#_R 1 CE# VDD 8 +3VSPI
PCH_SPI1_CLK_R 6 SCK
PCH_SPI1_SI_R 5 SI
PCH_SPI1_SO_R 2 SO HOLD# 7 HOLD#
BIOS_WP# 3 WP# VSS 4
*A25LQ32AM-F/Q
DFHS08FS023
91960-0084L-8P-SOCKET

U14 &U15 footprint 要重疊
Need place to TOP

TP5 PCH_SPI_CS0#_R
TP4 PCH_SPI1_CLK_R
TP2 PCH_SPI1_SI_R
TP1 PCH_SPI1_SO_R
TP3 BIOS_WP#
TP8 HOLD#

PCH SPI ROM(CLG)

0612 Change R10 from 0 ohm to short pad

+3VS5 R15 *0_4
+3V_DEEP_SUS R10 *0_4/S

PCH_SPI_CS0# R2 15/F_4 PCH_SPI_CS0#_R
PCH_SPI1_CLK R4 15/F_4 PCH_SPI1_CLK_R
PCH_SPI1_SI R3 15/F_4 PCH_SPI1_SI_R
PCH_SPI1_SO R1 15/F_4 PCH_SPI1_SO_R

U15
1 CE# VDD 8 +3VSPI
6 SCK
5 SI
2 SO HOLD# 7 HOLD#
3 WP# VSS 4
GD25B64BSIGR
AKE3EFP0N07

C1 22P/50V_4
C2 1U/10V_4 +3VSPI R6 1K/F_4
PCH_SPI_IO2 R5 15/F_4 BIOS_WP#
R9 1K/F_4
R7 15/F_4
C4 0.1U/16V_4
PCH_SPI_IO3

R1/R2/R3/R4/R5/R7 close to U15 pin

PROJECT : Y62P/Y63P
Quanta Computer Inc.

Size	Document Number	Rev
Custom	10 -- SKYPAKE 14/20(SPI/LPC/SMBUS)	1A
Date: Wednesday, July 22, 2015	Sheet 10of 42	

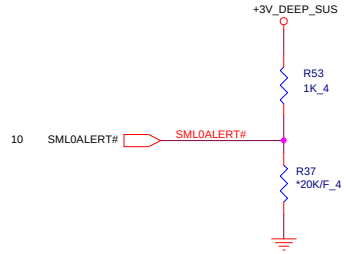
+3V_DEEP_SUS 4,10,12,14,15,16,18
+3V 2,4,10,12,13,14,15,16,17,18,20,21,22,23,24,25,26,27,29,30,31,37,39

Functional Strap Definitions

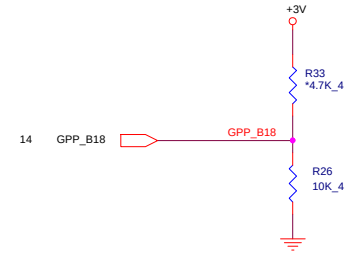
DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET

TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD

No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.



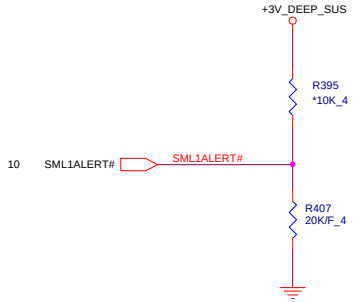
No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode
(PCH will disable the TCO
Timer system reboot feature).
This function is useful when running ITP/XDP.

No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.

Bit 10	Boot BIOS Destination
0	SPI
1	LPC



No Boot:
The signal has a weak internal pull-down.
0 = LPC Is selected for EC.
1 = eSPI Is selected for EC.

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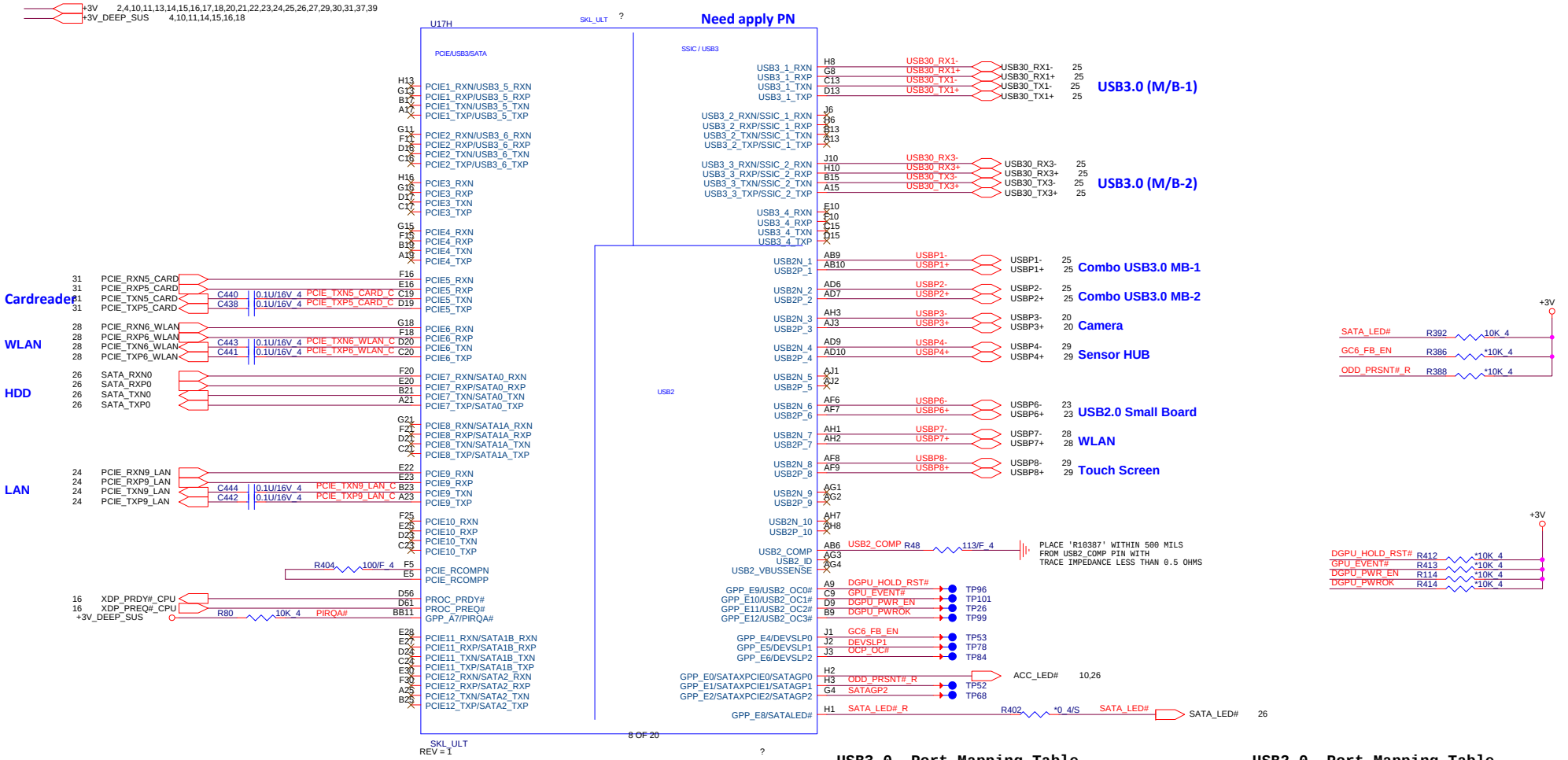

PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port1	Un-used	Port0	Un-used
Port2	Un-used	Port1	CardReader
Port3	Un-used	Port2	WLAN
Port4	Un-used	Port3	LAN
Port5	CardReader	Port4	Un-used
Port6	WLAN	Port5	Un-used
Port7	HDD		
Port8	Un-used		
Port9	LAN		
Port10	Un-used		

USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	USB3.0 MB-1
PORT-2	NC
PORT-3	USB3.0 MB-2
PORT-4	NC

USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	Cobime USB3.0 MB-1
PORT-2	Cobime USB3.0 MB-2
PORT-3	Camera
PORT-4	Sensor HUB
PORT-5	NC
PORT-6	USB2.0 Small Board
PORT-7	WLAN
PORT-8	Touch Screen
PORT-9	NC
PORT-10	NC

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+3V_RTC_2 4,15
+3V_RTC 4,15,27,28,32
+3V 2,4,10,11,12,14,15,16,17,18,20,21,22,23,24,25,26,27,29,30,31,37,39
+1.0V_DEEP_SUS 9,15,16,35,36

Need apply PN

U17J SKL_ULT ?

CLOCK SIGNALS

Cardreader
31 CLK_PCIE_CRN
31 CLK_PCIE_CRP
31 PCIE_CLKREQ_CR#

WLAN
28 CLK_PCIE_WLANN
28 CLK_PCIE_WLANP
28 PCIE_CLKREQ_WLAN#

LAN
24 CLK_PCIE_LANN
24 CLK_PCIE_LANP
24 PCIE_CLKREQ_LAN#

PCIE_CLKREQ0# D42 CLKOUT_PCIE_N0
C42 CLKOUT_PCIE_P0
AR10 GPP_B5/SRCCLKREQ0#
CLK_PCIE_CRN B42 CLKOUT_PCIE_N1
CLK_PCIE_CRP A42 CLKOUT_PCIE_P1
PCIE_CLKREQ_CR# AT7 GPP_B6/SRCCLKREQ1#
CLK_PCIE_WLANN D41 CLKOUT_PCIE_N2
CLK_PCIE_WLANP C41 CLKOUT_PCIE_P2
PCIE_CLKREQ_WLAN# AT8 GPP_B7/SRCCLKREQ2#
CLK_PCIE_LANN D40 CLKOUT_PCIE_N3
CLK_PCIE_LANP C40 CLKOUT_PCIE_P3
PCIE_CLKREQ_LAN# AT10 GPP_B8/SRCCLKREQ3#
B40 CLKOUT_PCIE_N4
A40 CLKOUT_PCIE_P4
PCIE_CLKREQ_VGA# AU8 GPP_B9/SRCCLKREQ4#
E40 CLKOUT_PCIE_N5
E39 CLKOUT_PCIE_P5
PCIE_CLKREQ5# AU7 GPP_B10/SRCCLKREQ5#

TBT

10 OF 20

SKL_ULT REV = 1

CLKOUT_ITPXDP_N F43 CK_XDP_N_R
CLKOUT_ITPXDP_P E43 CK_XDP_P_R
RP1 2 4 1 3 *0_4P2R_4
CK_XDP_N 16
CK_XDP_P 16

RP5002 install for XDP

GPD8/SUSCLK BA17 PCH_SUSCLK TP41
XTAL24_IN E37 XTAL24_IN
XTAL24_OUT E35 XTAL24_OUT
XCLK_BIASREF E42 XCLK_BIASREF
R444 2.7K/F_4
R445 *60.4/F_4
+1.0V_DEEP_SUS

Co-lay 60ohm 1% to GND for Cannonlake use

RTCX1 AM18 RTC_X1
RTCX2 AM20 RTC_X2 TP60
SRTCRST# AN18 SRTC_RST#
RTCRST# AM16 RTC_RST# RTC_RST# 16

CLK_REQ/Strap Pin(CLG)

+3V
PCIE_CLKREQ_VGA# R73 10K_4
PCIE_CLKREQ_WLAN# R93 10K_4
PCIE_CLKREQ_LAN# R104 10K_4
PCIE_CLKREQ_CR# R92 10K_4
PCIE_CLKREQ5# R82 10K_4
PCIE_CLKREQ0# R96 10K_4

Need apply PN

U17I SKL_ULT ?

CSI-2

CSI2_DN0 A36
CSI2_DP0 B36
CSI2_DN1 C36
CSI2_DP1 D36
CSI2_DN2 C35
CSI2_DP2 D35
CSI2_DN3 A35
CSI2_DP3 B35
CSI2_DN4 C31
CSI2_DP4 D31
CSI2_DN5 C32
CSI2_DP5 D32
CSI2_DN6 A33
CSI2_DP6 B33
CSI2_DN7 A32
CSI2_DP7 B32
CSI2_DN8 A29
CSI2_DP8 B29
CSI2_DN9 C28
CSI2_DP9 D28
CSI2_DN10 A27
CSI2_DP10 B27
CSI2_DN11 C27
CSI2_DP11 D27

CSI2_CLKN0 C37
CSI2_CLKP0 D37
CSI2_CLKN1 C32
CSI2_CLKP1 D32
CSI2_CLKN2 C29
CSI2_CLKP2 D29
CSI2_CLKN3 C26
CSI2_CLKP3 D26
CSI2_COMP E13
GPP_D4/FLASHTRIG B7 GPP_D4 TP95
R136 100/F_4

EMMC

GPP_F13/EMMC_DATA0 AP2 GPP_F13 TP77
GPP_F14/EMMC_DATA1 AP1 GPP_F14 TP67
GPP_F15/EMMC_DATA2 AP3 GPP_F15 TP86
GPP_F16/EMMC_DATA3 AN3 GPP_F16 TP75
GPP_F17/EMMC_DATA4 AN1 GPP_F17 TP66
GPP_F18/EMMC_DATA5 AN2 GPP_F18 TP80
GPP_F19/EMMC_DATA6 AM4 GPP_F19 TP85
GPP_F20/EMMC_DATA7 AM1 GPP_F20 TP59
GPP_F21/EMMC_RCLK AM2 EMMC_RCLK TP63
GPP_F22/EMMC_CLK AM3 EMMC_CLK TP73
GPP_F12/EMMC_CMD AP4 EMMC_CMD TP70
EMMC_RCOMP AT1 EMMC_RCOMP R380 200/F_4

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SKL_ULT REV = 1

RTC Clock 32.768KHz

C421 12P/50V_4
C422 12P/50V_4
Y2 32.768KHZ
R403 10M_4
RTC_X1
RTC_X2

RTC Circuitry(RTC)

30mils
RTC Power trace width 20mils.

+3V_RTC_2 R291 0_4
+3V_RTC R292 *0_4
J1 *SOLDERJUMPER-2
R278 20K/F_4
RTC_RST#
+3V_RTC_0
+3VPCU
D7 MEK500V-40
D6 MEK500V-40
R251 1K
+3V_RTC_1
R267 20K/F_4
SRTC_RST#
C310 1U/6.3V_4
C311 1U/6.3V_4
C306 1U/6.3V_4
CN20 RTC SOCKET
RTC_RST# R277 *0_6 SRTC_RST#
Q16 2N7002K
EC_RTC_RST
R298 10K_4

External Crystal and Green Clock

The 24 MHz (50 Ohm ESR) XTAL used for Skylake-U needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-U.

XTAL24_IN
XTAL24_OUT
R442 1M_4
C460 33P/50V_4
C453 33P/50V_4
24MHZ +-30PPM
Y3

0701 Delete TP102, TP103 for Layout placement request

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Skylake (GPIO)

+3V 2,4,10,11,12,13,15,16,17,18,20,21,22,23,24,25,26,27,29,30,31,37,39
+3V_DEEP_SUS 4,10,11,12,15,16,18

0629 Reserved R579 between +3V_DEEP_SUS and ISH_EMU_LID

+3V
ACCEL_INTA# R399 10K_4

+3V_DEEP_SUS
ISH_EMU_LID R579 *10K_4
BT_OFF R385 10K_4
PCH_TEMPALERT# R390 10K_4
SIO_EXT_SCI# R391 10K_4
UART2_TXD R398 *49.9K_4
UART2_RXD R397 *49.9K_4

0615 Change R397, R398 from I to NI

U17F — SKL_ULT ? — Need apply PN

LPSS
GPP_B15/GSPI0_CS# — TP31 GPP_B15 AN8
GPP_B16/GSPI0_CLK — TP15 GPP_B16 AP7
GPP_B17/GSPI0_MISO — TP13 GPP_B17 AP8
GPP_B18/GSPI0_MOSI — GPP_B18 AR7 — 11 GPP_B18
GPP_B19/GSPI1_CS# — TP16 GPP_B19 AM5
GPP_B20/GSPI1_CLK — TP11 GPP_B20 AN7
GPP_B21/GSPI1_MISO — TP12 GPP_B21 AP5
GPP_B22/GSPI1_MOSI — GSPI1_MOSI AN5 — 11 GSPI1_MOSI
GPP_C8/UART0_RXD — TP71 GPP_C8 AB1
GPP_C9/UART0_TXD — TP72 GPP_C9 AB2
GPP_C10/UART0_RTS# — TP90 GPP_C10 W4
GPP_C11/UART0_CTS# — TP82 GPP_C11 AB3
GPP_C20/UART2_RXD — UART2_RXD AD1 — 25 UART2_RXD
GPP_C21/UART2_TXD — UART2_TXD AD2 — 25 UART2_TXD
GPP_C22/UART2_RTS# — ACCEL_INTA# AD3 — 27 ACCEL_INTA#
GPP_C23/UART2_CTS# — SIO_EXT_SCI# AD4 — 30 SIO_EXT_SCI#
GPP_C16/I2C0_SDA — U7
GPP_C17/I2C0_SCL — U6
GPP_C18/I2C1_SDA — TP24 I2C1_SDA U8
GPP_C19/I2C1_SCL — TP29 I2C1_SCL U9
GPP_F4/I2C2_SDA — TP17 I2C2_SDA AH9
GPP_F5/I2C2_SCL — TP18 I2C2_SCL AH10
GPP_F6/I2C3_SDA — TP27 I2C3_SDA AH11
GPP_F7/I2C3_SCL — TP36 I2C3_SCL AH12
GPP_F8/I2C4_SDA — TP34 I2C4_SDA AF11
GPP_F9/I2C4_SCL — TP30 I2C4_SCL AF12

ISH
GPP_D9 — P2 GPP_D9 — TP69
GPP_D10 — P3 GPP_D10 — TP62
GPP_D11 — P4 GPP_D11 — TP61
GPP_D12 — P1 — BT_OFF — BT_OFF 28
GPP_D5/ISH_I2C0_SDA — M4 ISH_I2C0_SDA — ISH_I2C0_SDA 29
GPP_D6/ISH_I2C0_SCL — N3 ISH_I2C0_SCL — ISH_I2C0_SCL 29
GPP_D7/ISH_I2C1_SDA — N1 ISH_I2C1_SDA — TP76
GPP_D8/ISH_I2C1_SCL — N2 ISH_I2C1_SCL — TP51
GPP_F10/I2C5_SDA/ISH_I2C2_SDA — AD11 ISH_I2C2_SDA — TP39
GPP_F11/I2C5_SCL/ISH_I2C2_SCL — AD12 ISH_I2C2_SCL — TP38
GPP_D13/ISH_UART0_RXD/SML0BDATA/I2C4B_SDA — U1 PCH_TEMPALERT# — TP54
GPP_D14/ISH_UART0_TXD/SML0BCLK/I2C4B_SCL — U2 SML0BDATA — TP79
GPP_D15/ISH_UART0_RTS# — U3 SML0BCLK — TP88
GPP_D16/ISH_UART0_CTS#/SML0BALERT# — U4 SML0BALERT# — TP58
GPP_C12/UART1_RXD/ISH_UART1_RXD — AC1 UART1_RXD — TP65
GPP_C13/UART1_TXD/ISH_UART1_TXD — AC2 UART1_TXD — TP74
GPP_C14/UART1_RTS#/ISH_UART1_RTS# — AC3 UART1_RTS — TP81
GPP_C15/UART1_CTS#/ISH_UART1_CTS# — AB4 UART1_CTS — TP89
GPP_A18/ISH_GP0 — AY8 ISH_EMU_LID — D17 *MEK500V-40 — EMU_LID 20,30
GPP_A19/ISH_GP1 — BA8 — ISH_GYRO_DRDY 29
GPP_A20/ISH_GP2 — BB7 — ISH_GYRO_INT 29
GPP_A21/ISH_GP3 — BA7 — ISH_AE_INT 29
GPP_A22/ISH_GP4 — AY7 — ISH_ACC_INT 29
GPP_A23/ISH_GP5 — AW7 ISH_DISABLE KB — R389 *0_4 DISABLE KB — DISABLE KB 29,30
GPP_A12/BM_BUSY#/ISH_GP6 — AP13 — TP40

6 OF 20
SKL_ULT REV = 1

0629 Change Net name form ISH_COOL SENSE to ISH_EMU_LID
Delete R50
Add D17 between ISH_EMU_LID and EMU_LID

FOR ISH: Stuff R50, R389 (Default)

EMU_LID: Active Low
LID Open => High; LID Close =>Low
DISABLE KB: Active Low
Disable KB and TP => Output Low

FOR External Sensor HUB: Un Stuff D17, R389

FOR SKL 15" Stuff R5119, Unstuff R5118 (Default)
FOR SKL 13" Stuff R5118,Unstuff R5119

FOR ISH: Stuff R57, Un-stuff R34 (Default)
FOR External Sensor HUB: Stuff R34, Un-stuff R57

R61 *10K_4 BOARD_ID0 — R32 10K_4
R65 *10K_4 BOARD_ID1 — R31 10K_4
R64 *10K_4 BOARD_ID2 — R42 10K_4
R57 *10K_4 BOARD_ID3 — R34 10K_4
R58 10K_4 BOARD_ID4 — R35 *10K_4
R60 10K_4 BOARD_ID5 — R40 *10K_4
R63 *10K_4 BOARD_ID6 — R41 *10K_4
R59 *10K_4 BOARD_ID7 — R39 *10K_4
R55 *10K_4 BOARD_ID8 — R69 *10K_4
+3V_DEEP_SUS

Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
13" clamshell wo/TS	0	0	0	0	0	1
13" convertible w/TS	0	0	0	0	1	0
15" convertible w/TS+ Giga NIC	0	0	0	0	1	1
13" Sangria 2.0 (Y62M) w/TS+ w/eDP Panel	0	0	0	1	0	0
15" Spritzer 2.0 (Y63M) w/TS+ Giga NIC+ w/eDP Panel	0	0	0	1	0	1
13" Sangria 2.1 (SKL) w/TS+ w/eDP Panel	0	0	0	1	1	0
15" Spritzer 2.1 (SKL) w/TS+ Giga NIC+ w/eDP Panel+ISH	0	0	0	1	1	1
15" Spritzer 2.1 (SKL) w/TS+ Giga NIC+ w/eDP Panel+ESH	0	0	1	1	1	1
13" convertible w/TS (Y0H HSW Win10)	0	1	0	0	1	0

HDA Bus(CLG)

+3V_DEEP_SUS — R49 *1K_4 — ACZ_SYNC
22 ACZ_SYNC_AUDIO — R29 33_4 — ACZ_SYNC
22 ACZ_RST#_AUDIO — R417 33_4 — ACZ_RST#
22 ACZ_SDOUT_AUDIO — R46 33_4 — ACZ_SDOUT
22 BIT_CLK_AUDIO — R424 33_4 — ACZ_BCLK
C439 *10P/50V_4

U17G — SKL_ULT ? — Need apply PN

AUDIO
ACZ_SYNC — BA22 — HDA_SYNC/I2S0_SFRM
ACZ_BCLK — AY22 — HDA_BLK/I2S0_SCLK
ACZ_SDOUT — BB22 — HDA_SDO/I2S0_TXD
ACZ_SDIN0 — BA21 — HDA_SDI0/I2S0_RXD
ACZ_RST# — AY21 — HDA_SDI1/I2S1_RXD
AW22 — HDA_RST#/I2S1_SCLK
J5 — GPP_D23/I2S_MCLK
AY20 — I2S1_SFRM
AW20 — I2S1_TXD
11 ACZ_SDOUT
22 ACZ_SDIN0
TP25 SSP2_SFRM AK7 — GPP_F1/I2S2_SFRM
TP22 SSP2_SCLK AK6 — GPP_F0/I2S2_SCLK
TP19 SSP2_TXD AK9 — GPP_F2/I2S2_TXD
TP32 SSP2_RXD AK10 — GPP_F3/I2S2_RXD
TP28 GPP_D19 H5 — GPP_D19/DMIC_CLK0
TP93 GPP_D20 D7 — GPP_D20/DMIC_DATA0
TP98 GPP_D17 D8 — GPP_D17/DMIC_CLK1
TP97 GPP_D18 C8 — GPP_D18/DMIC_DATA1
11,22 ACZ_SPKR — ACZ_SPKR AW5 — GPP_B14/SPKR

SDIO/SDXC
GPP_G0/SD_CMD — AB11 BOARD_ID0
GPP_G1/SD_DATA0 — AB13 BOARD_ID1
GPP_G2/SD_DATA1 — AB12 BOARD_ID2
GPP_G3/SD_DATA2 — W12 BOARD_ID3
GPP_G4/SD_DATA3 — W11 BOARD_ID4
GPP_G5/SD_CD# — W10 BOARD_ID5
GPP_G6/SD_CLK — W8 BOARD_ID6
GPP_G7/SD_WP — W7 BOARD_ID7
GPP_A17/SD_PWR_EN#/ISH_GP7 — BA9 BOARD_ID8
GPP_A16/SD_1P8_SEL — BB9 GPP_A16 — GPP_A16 25
SD_RCOMP — AB7 — R62 200/F_4
GPP_F23 — AF13 GPP_F23 — TP20

7 OF 20
SKL_ULT REV = 1

BIOS need modify ISH_GP0 setting Internal PU 20K

* Please be noted ISH_GP[0:7] (Multiplexed with GPP_A12, GPPA_17, GPP_A[18:23]) are in PCH Primary Well Group A, when eSPI (Multiple xed withGPP_A[0:15]) is enable, VCCPGPPA should be supplied by 1.8V. That means the signaling level of all the Primary Well Group A signals including ISH_GP[0:7] will be 1.8V.

CN1
1 ISH_I2C0_SCL
2 ISH_I2C0_SDA
3 ISH_I2C1_SCL
4 ISH_I2C1_SDA
5
6 ISH_GYRO_DRDY
7 ISH_GYRO_INT
8 ISH_AE_INT
9 ISH_ACC_INT
10
11
12 ISH_DISABLE KB
13 TP6
14 TP7
15 TP10
16 TP9
17 +3V
18
*50501-0180N-001

Proposed location must be under the keyboard (TOP side)

0630 Delete Net ISH_COOL SENSE on CN1.11

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4,10,11,12,14,16,18 +3V_DEEP_SUS
9,13,16,35,36 +1.0V_DEEP_SUS
9,35 +1.8V_DEEP_SUS
4,13,27,28,32 +3V_RTC
4,10,16,28,29,30,33,35,36,39 +3VS5
4,13 +3V_RTC_2

U17O SKL_ULT

CPU POWER 4 OF 4

Need apply PN

PCH Internal VRM

C820 and C690 close to cpu less then 100 mils

0612 Change R168from 0 ohm to short pad

0612 Change R409, R139, R133, R151, R148, R163, R162, R408, R146, R156, R374, R17, R422, R165, R157, R152, R147, R146 from 0 ohm to short pad

20mils

for DS3

SKL_ULT
REV = 1

15 OF 20

+3V 2,4,10,11,12,13,14,15,17,18,20,21,22,23,24,25,26,27,29,30,31,37,39
+3V_DEEP_SUS 4,10,11,12,14,15,18
+1.0V 2,4,6,30,36
+1.0V_DEEP_SUS 9,13,15,35,36
+VCCIO 2,6,36

CPU XDP

CN12 — *Samtec BSH-030-01

12	XDP_PREQ#_CPU	3	OBSFN_A0	VCC_OBS_CD	44
12	XDP_PRDY#_CPU	5	OBSFN_A1	VCC_OBS_AB	43
9	CFG0	9	OBSDATA_A0	OBSFN_B0	21
9	CFG1	11	OBSDATA_A1	OBSFN_B1	23
9	CFG2	15	OBSDATA_A2	OBSFN_C0	4
9	CFG3	17	OBSDATA_A3	OBSFN_C1	6
9	CFG4	27	OBSDATA_B0	OBSDATA_C0	10
9	CFG5	29	OBSDATA_B1	OBSDATA_C1	12
9	CFG6	33	OBSDATA_B2	OBSDATA_C2	16
9	CFG7	35	OBSDATA_B3	OBSDATA_C3	18
16	ON/OFFBTN_KBC#	41	HOOK1	OBSFN_D0	22
		45	HOOK2	OBSFN_D1	24
13	CK_XDP_P	40	ITPCLK/HOOK4	OBSDATA_D0	28
13	CK_XDP_N	42	ITPCLK#/HOOK5	OBSDATA_D1	30
		48	DBR#/HOOK7	OBSDATA_D2	34
10,17,18,27	SMB_RUN_DAT	51	SDA	OBSDATA_D3	36
10,17,18,27	SMB_RUN_CLK	53	SCL	HOOK3	47
		52	TDO	TCK1	55
		54	TRSTN	PWRGOOD/HOOK0	39
		56	TDI	RESET#/HOOK6	46
		58	TMS	GND0	1
2	XDP_TCK0	57	TCK0	GND1	2
		60	GND17	GND2	7
		59	GND16	GND3	8
		50	GND15	GND4	13
		49	GND14	GND5	14
		38	GND13	GND6	19
		37	GND12	GND7	20
		32	GND11	GND8	25
		31	GND10	GND9	26

+1.0V_DEEP_SUS
TP116

XDP_BPM0 2
XDP_BPM1 2
CFG17 9
CFG16 9
CFG8 9
CFG9 9
CFG10 9
CFG11 9
CFG19 9
CFG18 9
CFG12 9
CFG13 9
CFG14 9
CFG15 9
EC_PWROK 4,30

R290 *1K_4
R289 *1K_4
CFG0 R339 *1K_4 PWR_DEBUG
R341 *0_4 SMB_RUN_DAT_XDP
R343 *0_4 SMB_RUN_CLK_XDP
XDP_DBRESET_N
XDP_TDO
XDP_TRST#
XDP_TDI
XDP_TMS
XDP_TCK0

0612 Change R290, R289, R339, R354, R340 from I to NI

0612 Change R341, R343 from I to NI

XDP_DBRESET_N R354 *1K_4 +3V
C346 *0.1U/16V_4

SYS_PWROK R338 *1K_4 +3V_DEEP_SUS
C344 *0.1U/16V_4

0612 Change C346, C344 from I to NI

+1.0V_DEEP_SUS
C345 0.1U/16V_4
C351 0.1U/16V_4

0612 Change R351 from I to NI

+VCCIO
R351 *150/F_4
PWR_DEBUG
R352 *10K_4

APS

+3V_DEEP_SUS
+3VS5

CN5 — *50501-0180N-001

SUSB#	4,16,30	+3VS5
SLP_S5#	4	
SUSC#	4,30	
SLP_A#	4	
RTC_RST#	13	
ON/OFFBTN_KBC#	16	
SYS_RESET#	4	
R110 *0_4 PCH_SLP_S0_N	4,30	
SUSB#	4,16,30	

+3V
C385 0.1U/16V_4

U12 — *SN74CBTLV3126RGYR

14	VCC			
XDP_TDO 2	1A	1B	3	XDP_TDO_CPU 2
1	1OE			
XDP_TDI 5	2A	2B	6	XDP_TDI_CPU 2
4	2OE			
XDP_TMS 9	3A	3B	8	XDP_TMS_CPU 2
10	3OE			
XDP_TRST# 12	4A	4B	11	XDP_TRST#_CPU 2
13	4OE			
		DPAD	15	
	GND		7	

4,30,33,34,35 HWPG

4 SYS_PWROK
SYS_PWROK

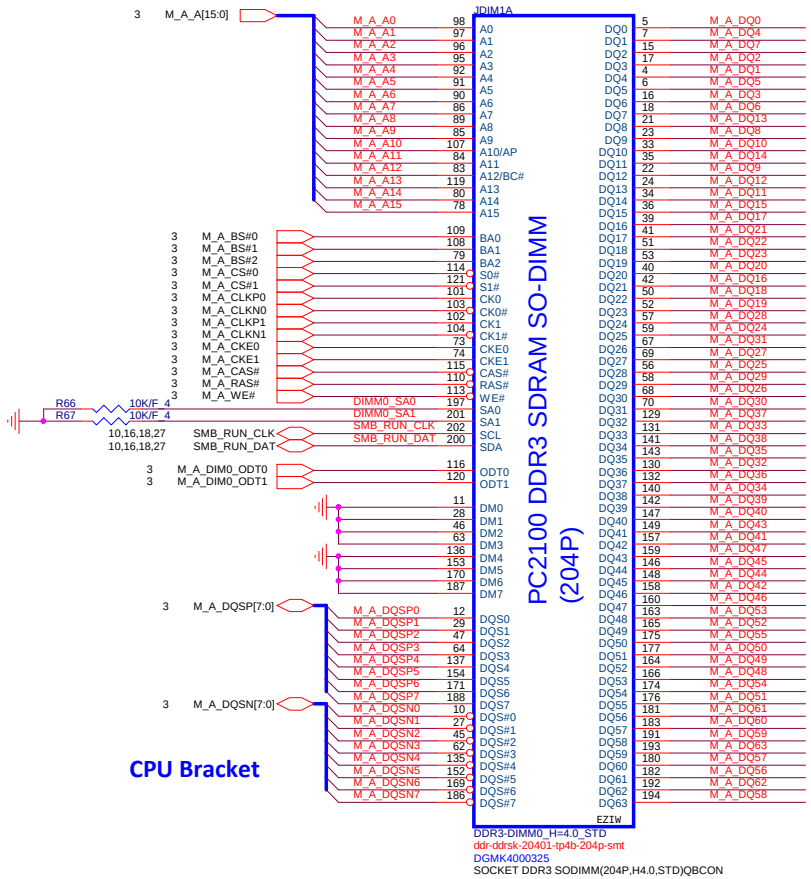
4,24,26,28,30,31 PLTRST#
R340 *1K_4 XDP_RST

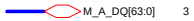
0612 Change R347 from I to NI

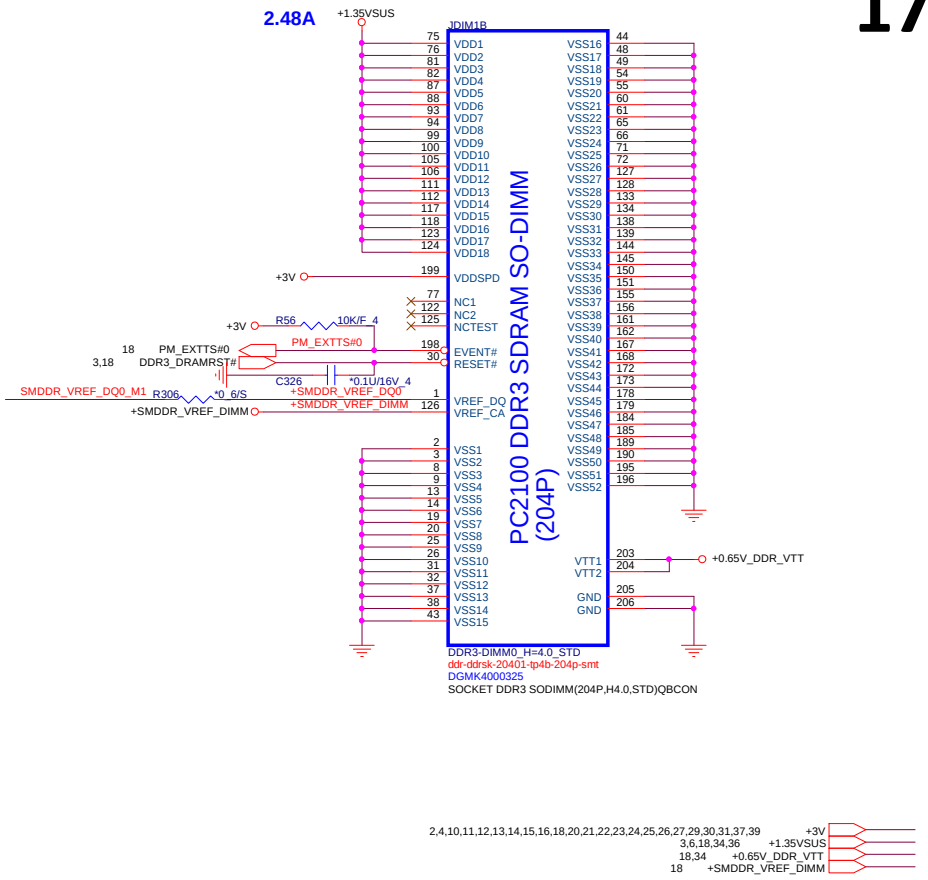
+1.0V
R347 *51_4 XDP_TDO
R345 *0_4 XDP_TCK0
2 JTAGX_PCH
2 JTAG_TMS_PCH XDP_TMS
2 JTAG_TDI_PCH XDP_TDI
2 JTAG_TDO_PCH XDP_TDO
R342 *0_4 XDP_TDI
R344 *0_4 XDP_TCK0
2 JTAG_TCK_PCH XDP_TCK1

PROJECT : Y62P/Y63P
Quanta Computer Inc.

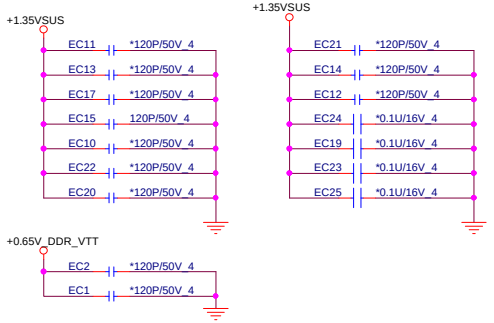
Size	Document Number	Rev
	16 -- HSW XDP & APS	1A
Date: Wednesday, July 22, 2015	Sheet 16 of 42	





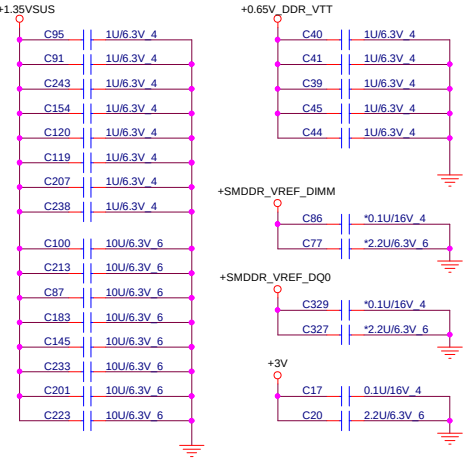


For EMI RESERVE

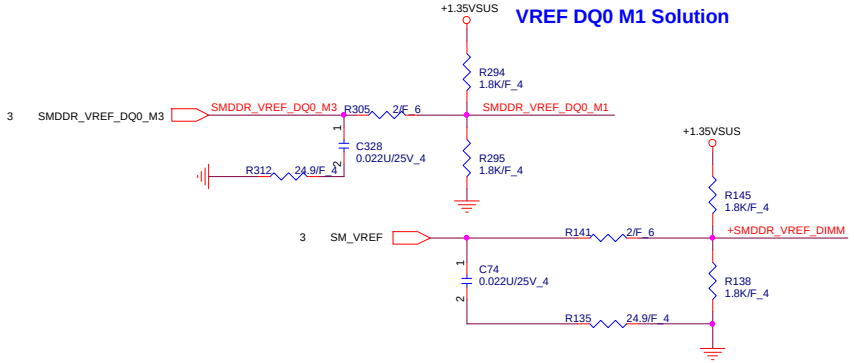


Place these Caps near So-Dimm0.

1uF/10uF 4pcs on each side of connector



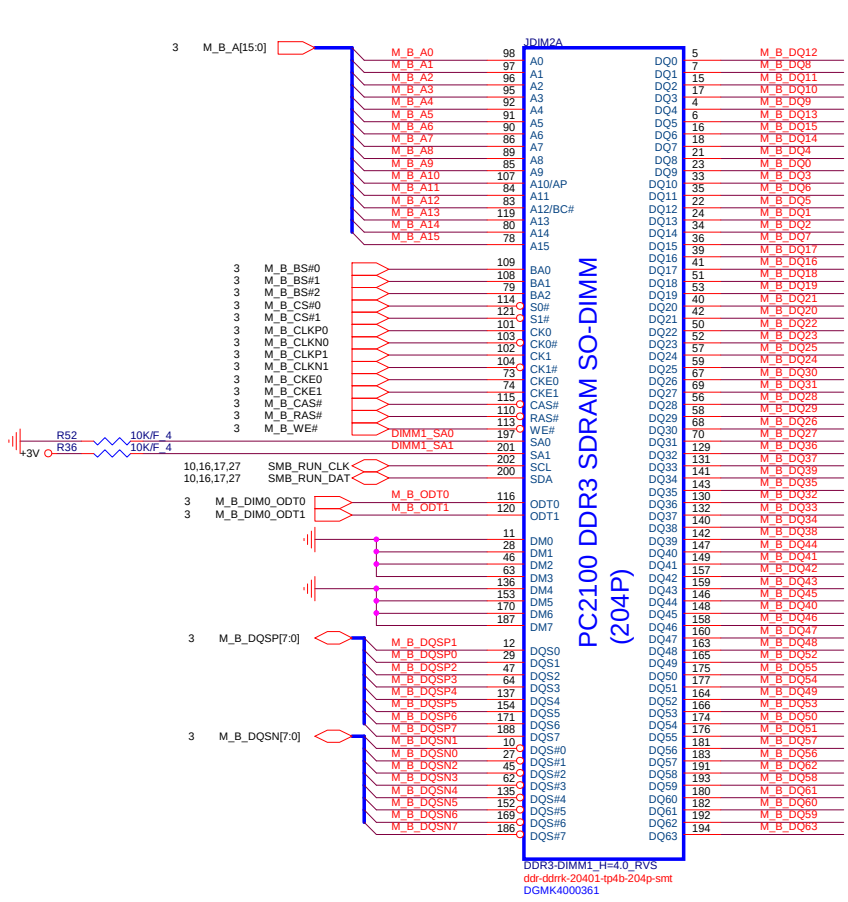
VREF DQ0 M1 Solution

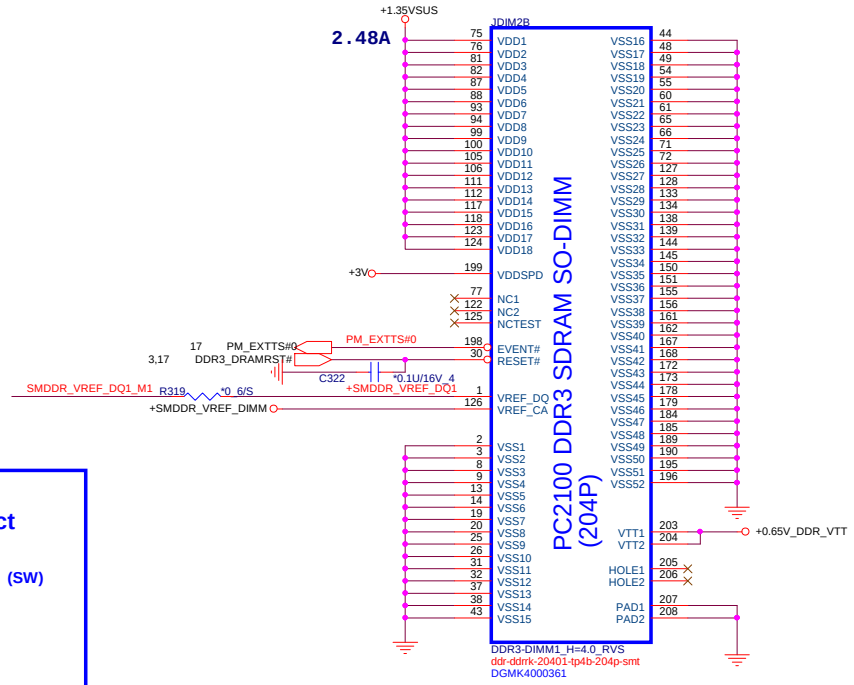


PROJECT : Y62P/Y63P

Quanta Computer Inc.

Size	Document Number	Rev
Custom	17 -- DDR3 DIMM0-STD(4.0H)	1A
Date: Wednesday, July 22, 2015	Sheet 17of 42	





DDR Thrm Protect

For 65 degree, 1.8v limit, (SW)

For 75 degree, 1.2v limit, (HW)

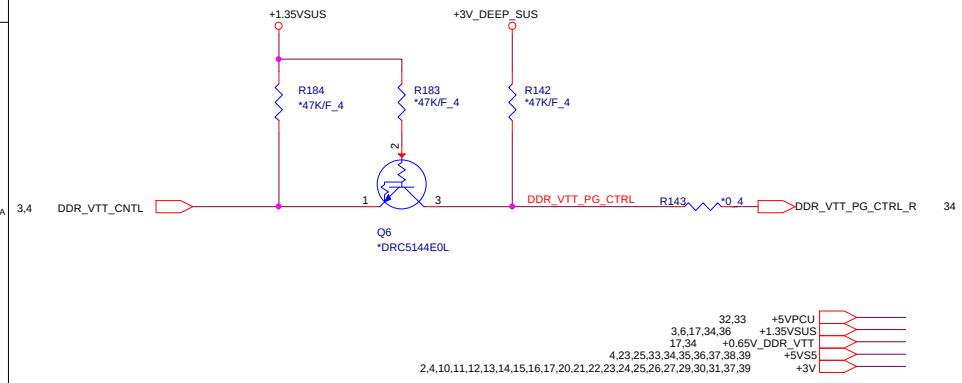
Close to U5010

Local Thermal Sensor

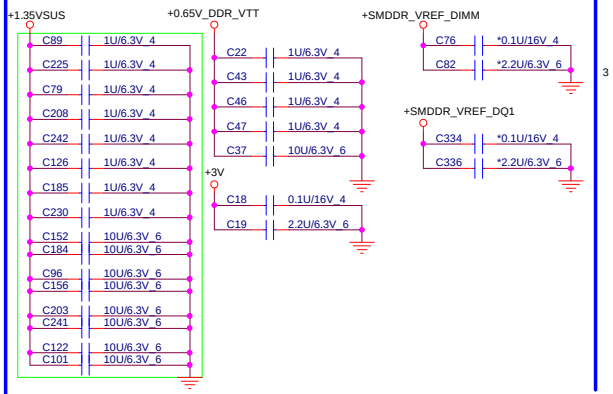
DDR3 Thermal Sensor

Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)

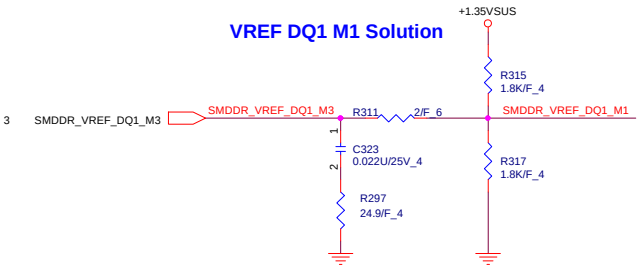
Co-lay for ODT
From Intel MOW, ODT directly connection to CPU



Place these Caps near So-Dimm1.
1uF/10uF 4pcs on each side of connector



VREF DQ1 M1 Solution



PROJECT : Y62P/Y63P
Quanta Computer Inc.

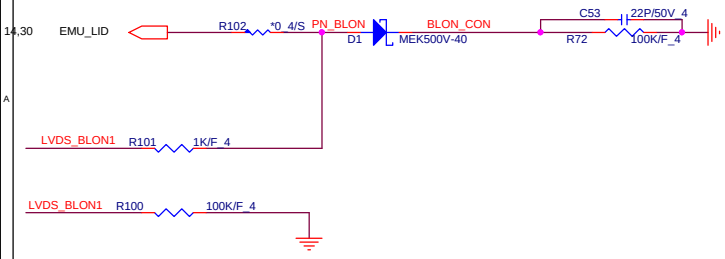
Size	Document Number	Rev
Custom	18 -- DDR3 DIMM1-RVS(4.0H)	1A
Date: Wednesday, July 22, 2015	Sheet 18of 42	

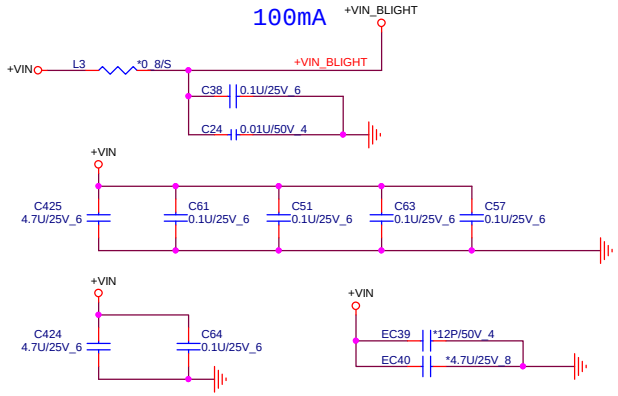
PROJECT : Y62P/Y63P
Quanta Computer Inc.

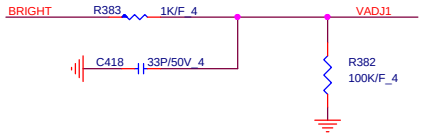
Size	Document Number	Rev
Custom	RTD2136	1A

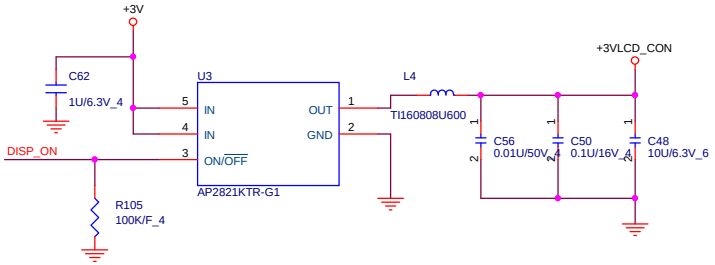
Date: Wednesday, July 22, 2015 | Sheet 19 of 42

LID Switch

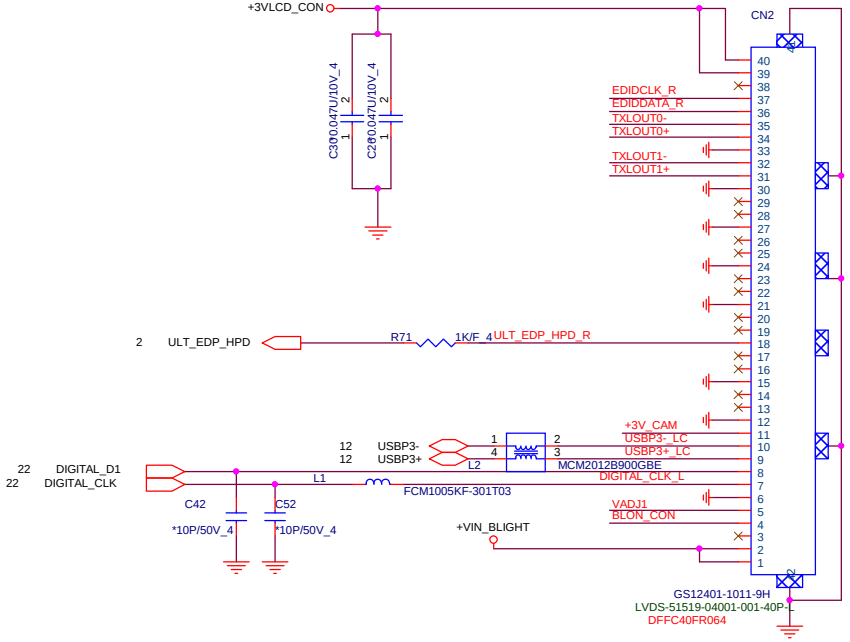


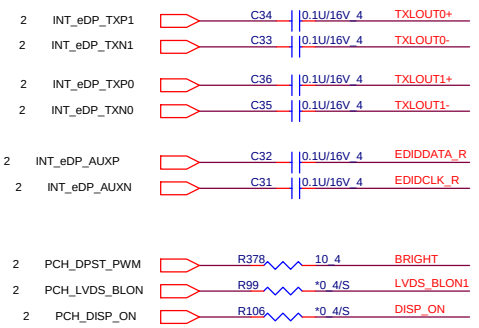


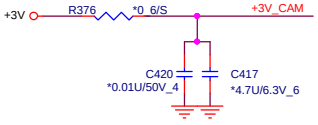


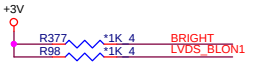


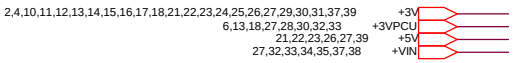
eDP Conn.





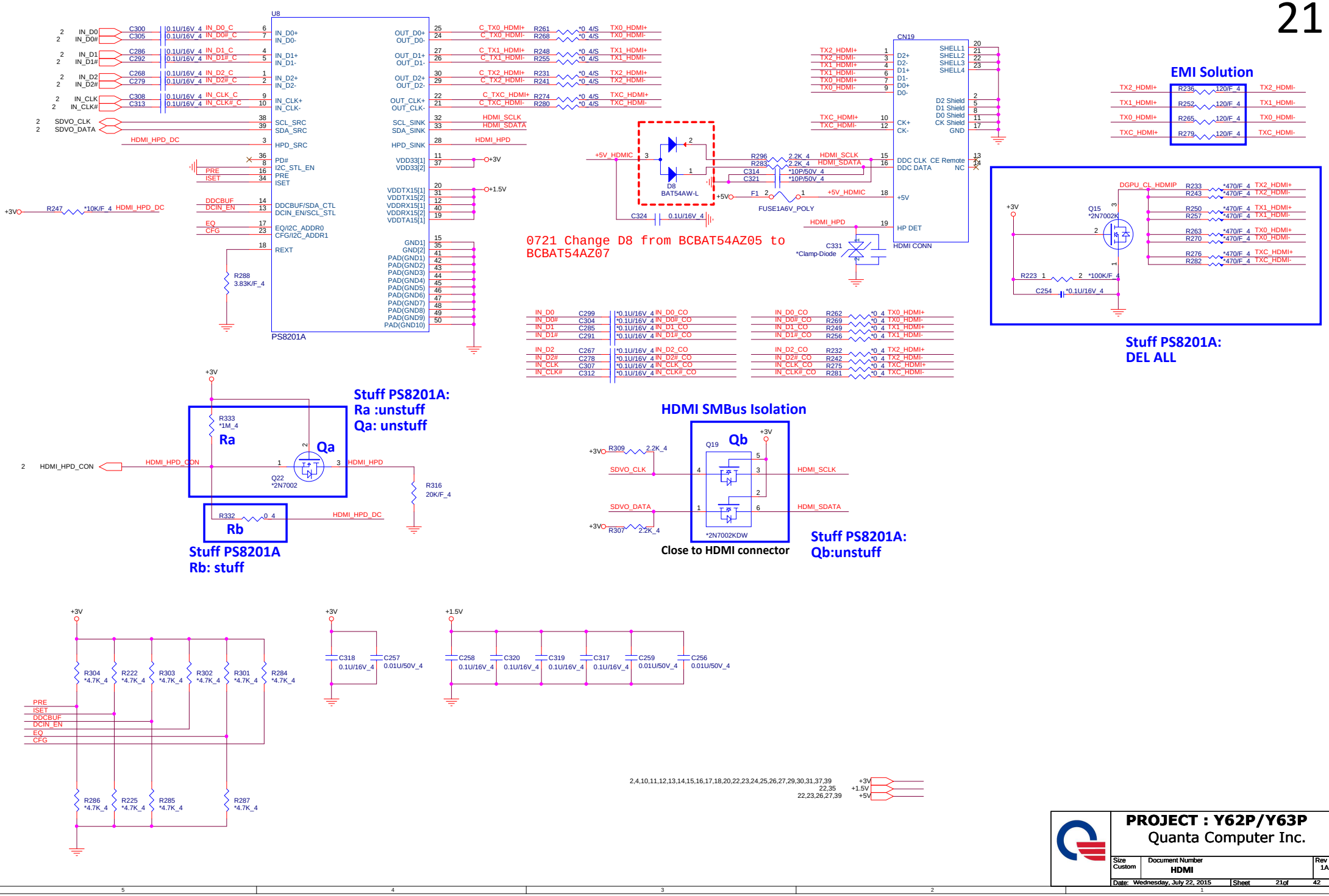






PROJECT : Y62P/Y63P
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID/CAM	1A
Date: Wednesday, July 22, 2015	Sheet 20 of 42	



PROJECT : Y62P/Y63P
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDMI	1A
Date: Wednesday, July 22, 2015	Sheet 21of 42	

Close to PIN1

Close to PIN26

Close to PIN40

Close to PIN27,39

Close to PIN28

Close to PIN7

Close to Pin 9

Close to Pin 34,35,36

Close to Pin 41

Close to Pin 46

Close to codec

Close to codec

Speaker 4 ohm: 40mils

Layout concern

TO Audio Jack MIC

check value

Check layout mount location

Close to CODEC

place to near U10013 or under U10013

TO Internal Speakers

Digital MIC

for intel HSW ULT

FOR EMI

>40mils trace

AGND SHIELD

Vset=1.242V

U22

ALC3227 x QFN48

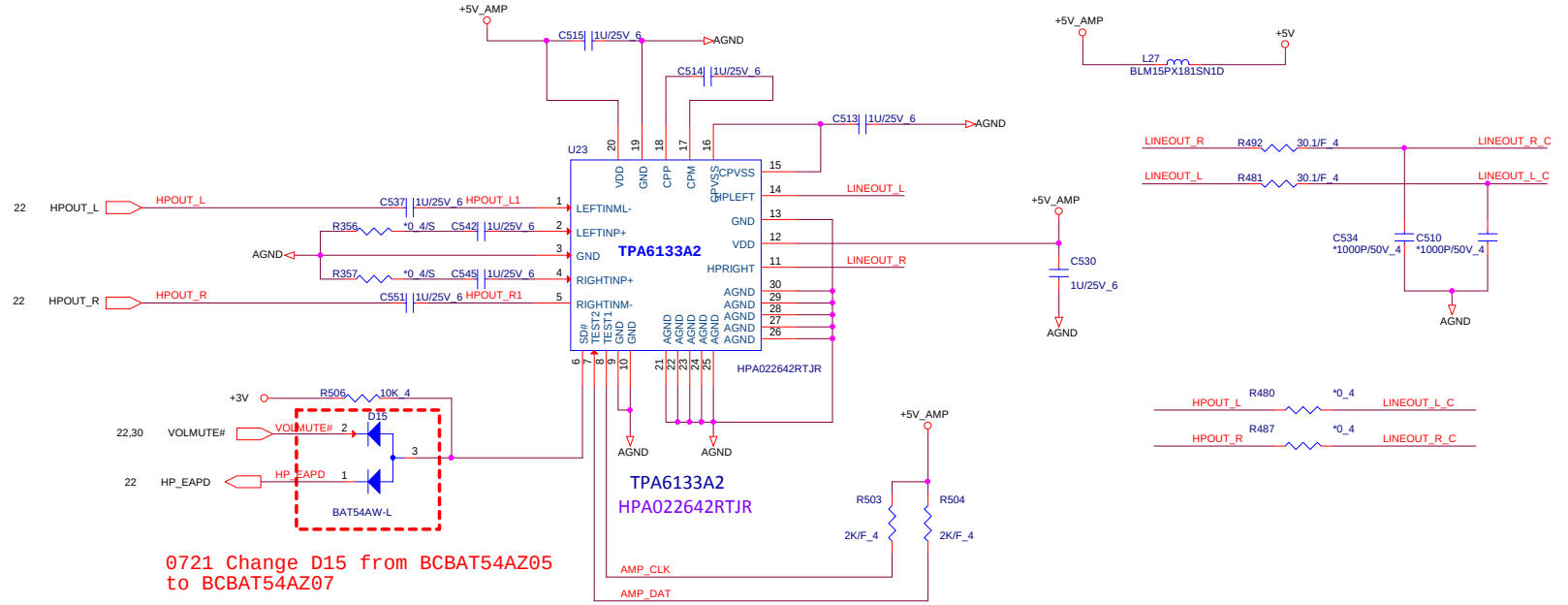
PROJECT : Y62P/Y63P

Quanta Computer Inc.

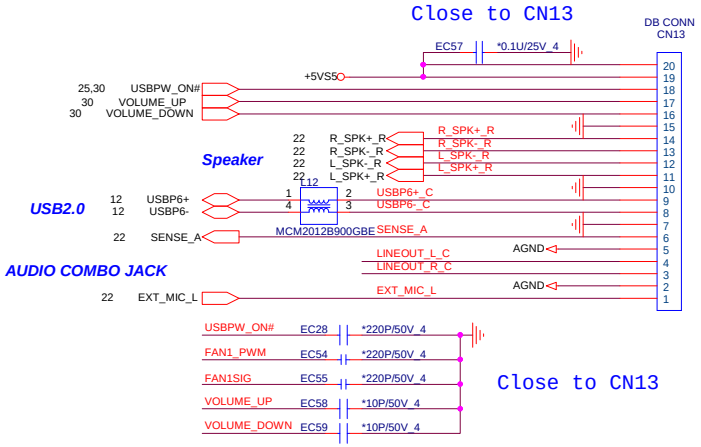
Size: Custom | Document Number: Azalia ALC 3227 | Rev: 1A

Date: Wednesday, July 22, 2015 | Sheet 22 of 42

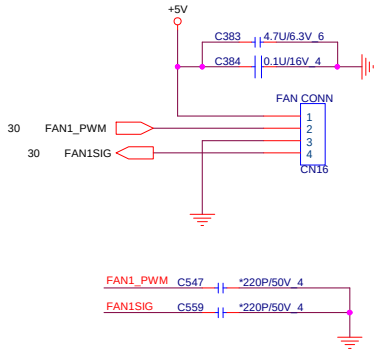
Head Phone out



Audio Board



FAN



2,4,10,11,12,13,14,15,16,17,18,20,21,22,24,25,26,27,29,30,31,37,39 +3V
21,22,26,27,39 +5V
4,25,33,34,35,36,37,38,39 +5VS5

PROJECT : Y62P/Y63P
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Audio/AMP HPA022642RTJR	1A
Date: Wednesday, July 22, 2015	Sheet 23 of 42	

For EMI 0 ~ 22 ohm

R208 10/F_4

LAN_XTAL1 — XTAL1

Y1 25MHZ +-10PPM

XTAL2

C232 10P/50V_4

C231 10P/50V_4

Trace<30 mil
Width > 60 mil

Power trace Layout 寬度> 60mil

>60mil

+1.05V_LAN_REGOUT

4.7UH,+-20%,650MA_1210 L21 La

>60mil

R206 *0_8

Cb C178 4.7U/6.3V_6

Ca C180 0.1U/16V_4

Cc C450 0.1U/16V_4

Cd C216 0.1U/16V_4

Ce C458 0.1U/16V_4

Cf C456 0.1U/16V_4

Cg C455 *1U/6.3V_4

C182 0.1U/16V_4

C447 *1U/6.3V_4 Cf

C181 *0.1U/16V_4

+1.05V_LAN

Close to Choke La
SWR mode need stuff Ca & Cb

Place Cg & C128 close to each VDD10 pin22

For GbE
* Place Cg close to each VDD10 pin-- 22 (reserve)

LED1:
FOR GIGA 8161: Stuff Ra, DEL Rb (Default)
FOR 10/100 8176: Stuff Rb,DEL Ra

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

+1.05V_LAN

R443 2.49K/F_4 LANRSET

+3V_LAN

LAN_AMBLED# TP43

Ra

R210 0_4 LAN_WLED#

Rb R209 *0_4

+3V

R441 1K_4

ISOLATEB

R440 15K/F_4

U6

RTL8176EH

Please add 9 GND VIAs connection with thermal PAD

MDI0+ MDI0- VDD10 MDI1+ MDI1- MDI2+ MDI2- VDD10

MDIP0 MDIN0 AVDD10(NC) MDIP1 MDIN1 MDIP2(NC) MDIN2(NC) AVDD10

REGOUT(NC) VDDREG(VDD33) DVDD10(NC) LANWAKEB ISOLATEB PERSTB HSON HSOP

+1.05V_LAN_REGOUT +3V_LAN +1.05V_LAN PCIE_WAKE# ISOLATEB PLTRST#

PCIE_RXN9_LAN_L PCIE_RXP9_LAN_L C127 C128 0.1U/16V_4 0.1U/16V_4

PCIE_RXN9_LAN PCIE_RXP9_LAN

RTL8161GSH-CG

MDI3+ MDI3-

CLK_PCIE_LANN CLK_PCIE_LANP PCIE_TXN9_LAN PCIE_TXP9_LAN

PCIE_CLKREQ_LAN# R167 *0_4/S LAN_CLKRQ

FOR GIGA: 8161GSH: AL008161004 (Default)
FOR 10/100: 8176EH: AL008176000

10/100 only

U16 *NS681684

MDI1-_1 MDI1+_1 LAN_MCT2 MDI0-_1 MDI0+_1 LAN_MCT1

TD+ TD- CT RD+ RD- CT

TX+ CMT TX- RX- CT RX+

MDI1- V_DAC MDI1+ MDI0+ V_DAC MDI0-

BOT: DB0LE6LAN00
FCE: DB0LE6LAN20

Reserve for Reltek FAE request.

+3V_LAN

+3VLANVCC

C117 C217 C214 C459 C116

0.1U/16V_4 0.1U/16V_4 *0.1U/16V_4 *4.7U/6.3V_6 *4.7U/6.3V_6

close to each VDD33 pin-- 11, 32

Place Cc and Cd close to each VDD33 pin-- 23

C202 4.7U/6.3V_6 Cc

C457 0.1U/16V_4 Cd

Remove For Not Using SWR mode

2,4,10,11,12,13,14,15,16,17,18,20,21,22,23,25,26,27,29,30,31,37,39

39 +3V +3VLANVCC

Giga only

Swap pin for Layout

U18 NS892407

MDI2+ MDI2- MDI3- MDI3+ MDI0+ MDI0- MDI1+ MDI1-

TD1+ TD1- TD2+ TD2- TD3+ TD3- TD4+ TD4-

MX1+ MX1- MX2+ MX2- MX3+ MX3- MX4+ MX4-

MDI2+_1 MDI2-_1 MDI3-_1 MDI3+_1 MDI0+_1 MDI0-_1 MDI1+_1 MDI1-_1

V_DAC V_DAC V_DAC V_DAC

TCT1 TCT2 TCT3 TCT4

MCT1 MCT2 MCT3 MCT4

LAN_MCT1 LAN_MCT2 LAN_MCT3 LAN_MCT4

R217 R155 R205 R204 75_4

C102 0.01U/50V_4

Stuff for Giga only

C433 10P/3KV_1808

BOT: DB0Z06LAN00
FCE: DB0LL1LAN00 (Default)

+3VLANVCC R161 330_4 C97 1000P/50V_4 LAN_AMBLED

+3VLANVCC R212 330_4 LAN_WLED C224 1000P/50V_4

LAN conn

RJ45 CN18

LAN_AMBLED LAN_AMBLED# (Amber)

LED_AMBER_P LED_AMBER_N

MDI3-_1 MDI3+_1 MDI1-_1 MDI2-_1 MDI2+_1 MDI1+_1 MDI0-_1 MDI0+_1

RX1- RX1+ RX0- TX1- TX1+ RX0+ TX0- TX0+

GND1 GND

LAN_WLED LAN_WLED# (White)

LED_WHITE_P LED_WHITE_N

R415 *0_6/S R450 *0_6/S

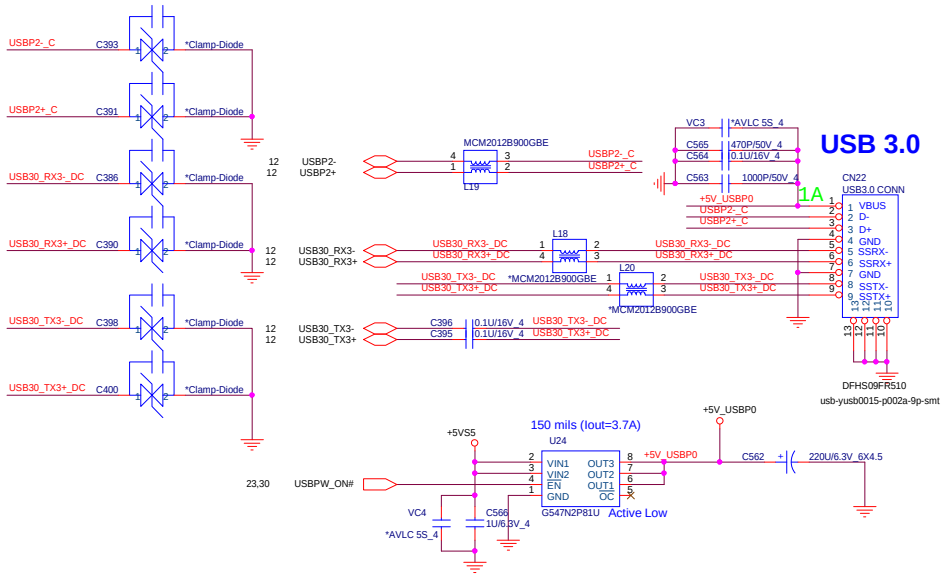
RJ45_CONN

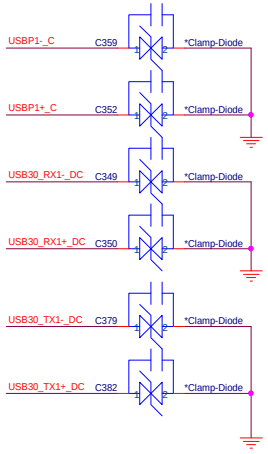
0721 Change CN18 from DFTJ12FR357 to DFTJ12FR396

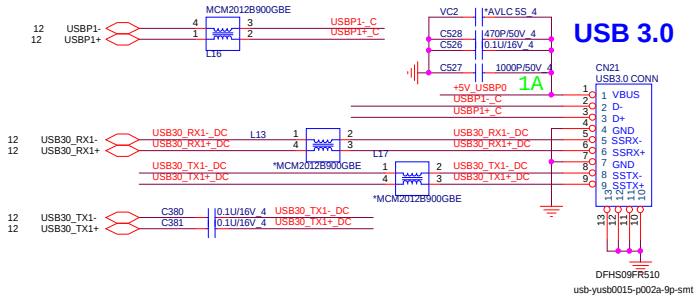
PROJECT : Y62P/Y63P
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTL 8161/RJ45	1A
Date: Wednesday, July 22, 2015	Sheet 24 of 42	

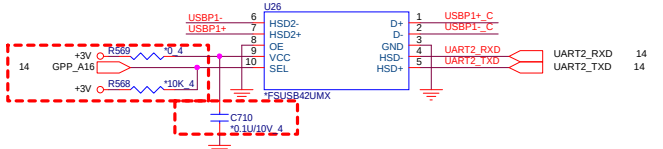
USB 2.0/3.0 Combo







UART for DEBUG



0612 Change R569, R568, C710 from I to NI

Place on BOT side under L16

+5VS5 4,23,33,34,35,36,37,38,39

+3V 2,4,10,11,12,13,14,15,16,17,18,20,21,22,23,24,26,27,29,30,31,37,39

PROJECT : Y62P/Y63P

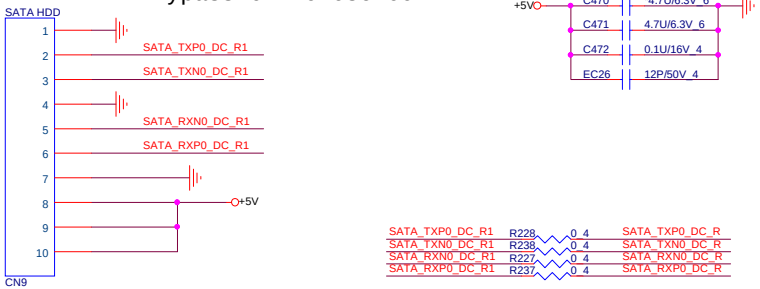
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB 3.0	1A

Date: Wednesday, July 22, 2015 Sheet 25 of 42

SATA HDD Connector(Cable type)

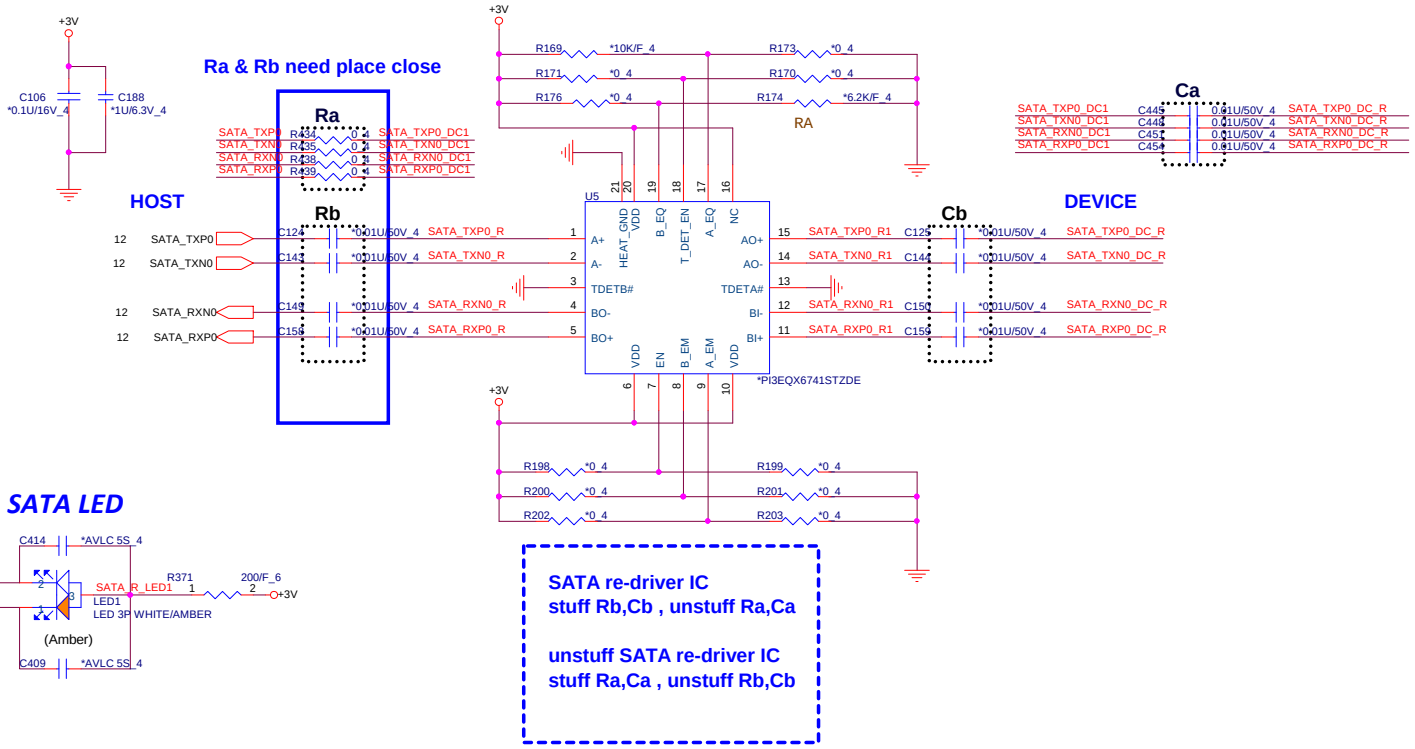
Bypass CAP close conn



LED1	PN	
Dual Color	BEWY0009ZA0	stuff R370, unstuff R573
Single Color	BEWH0046Z00	stuff R573, unstuff R370

SATA Re-driver

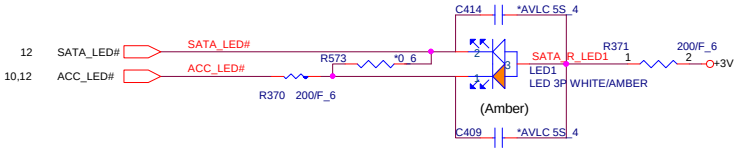
Ra & Rb need place close



SATA re-driver IC
stuff Rb,Cb , unstuff Ra,Ca

unstuff SATA re-driver IC
stuff Ra,Ca , unstuff Rb,Cb

SATA LED



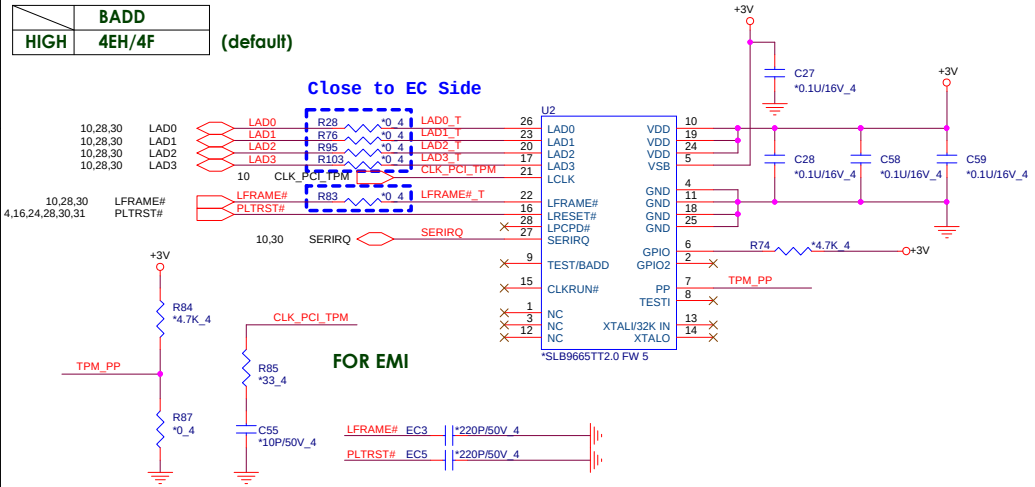
TPM (2.0)

Address

	BADD
HIGH	4EH/4F

(default)

Close to EC Side



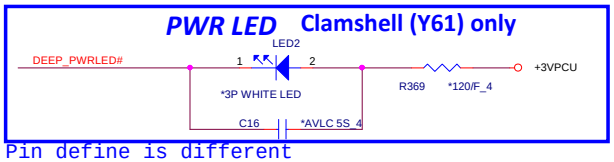
2,4,10,11,12,13,14,15,16,17,18,20,21,22,23,24,25,27,29,30,31,37,39 +3V
21,22,23,27,39 +5V

PROJECT : Y62P/Y63P
Quanta Computer Inc.

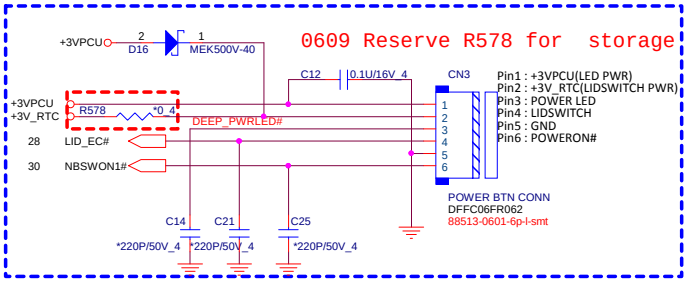
Size	Document Number	Rev
Custom	HDD/mSATA/FAN/LED	1A
Date: Wednesday, July 22, 2015	Sheet 26of 42	

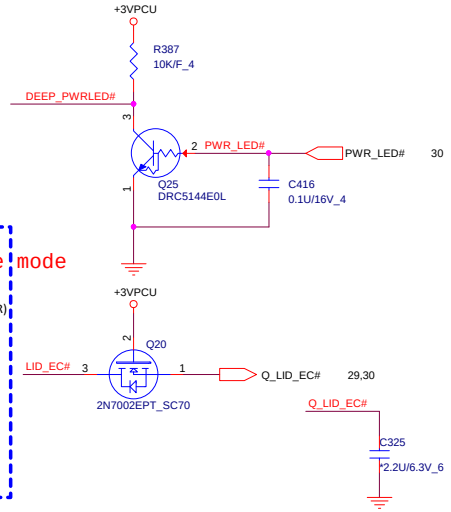
Power Botton Connector

PWR LED Clamshell (Y61) only

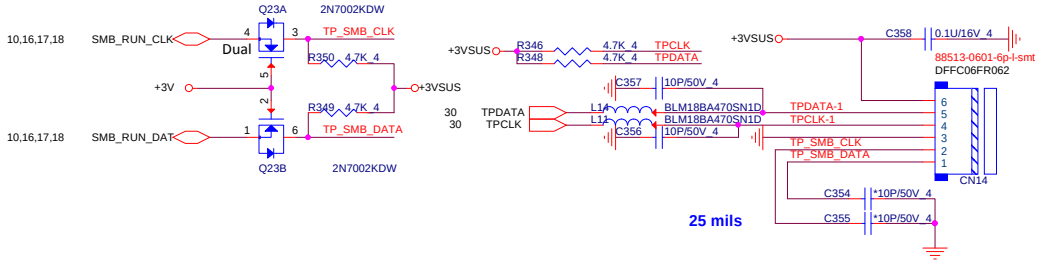


Pin define is different
Power Board does not shared with Y6x !!

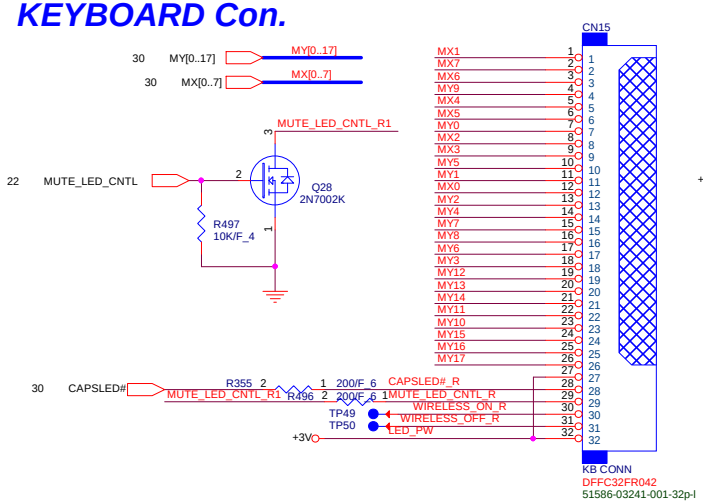




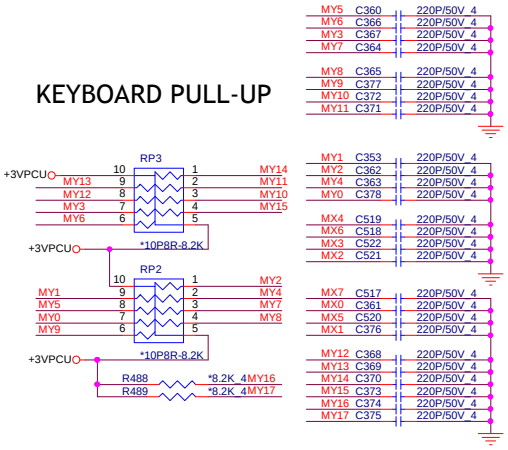
Touch Pad Connector



KEYBOARD Con.

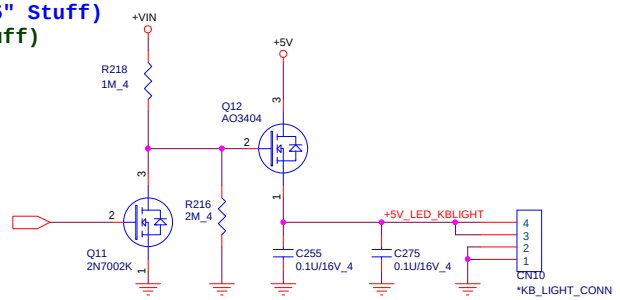


KEYBOARD PULL-UP

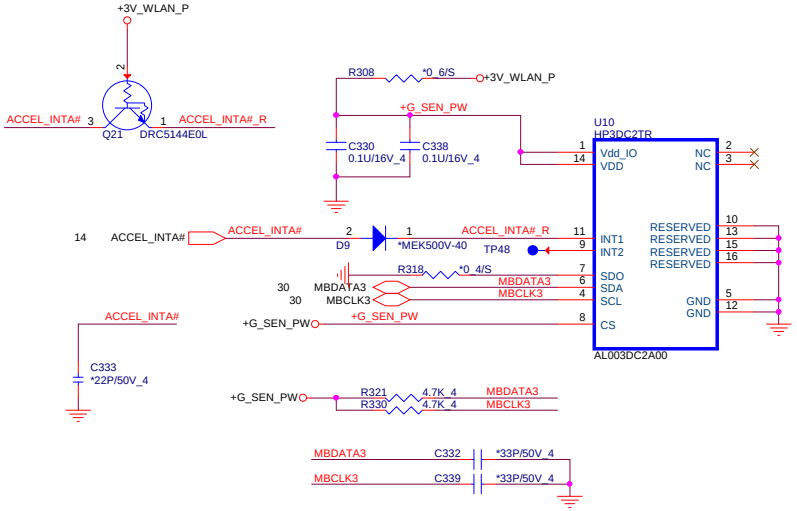


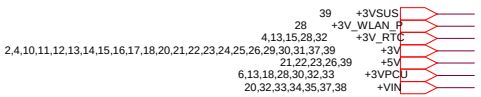
15" KB backlight only

(Default 15" Stuff)
(13" Un-Stuff)



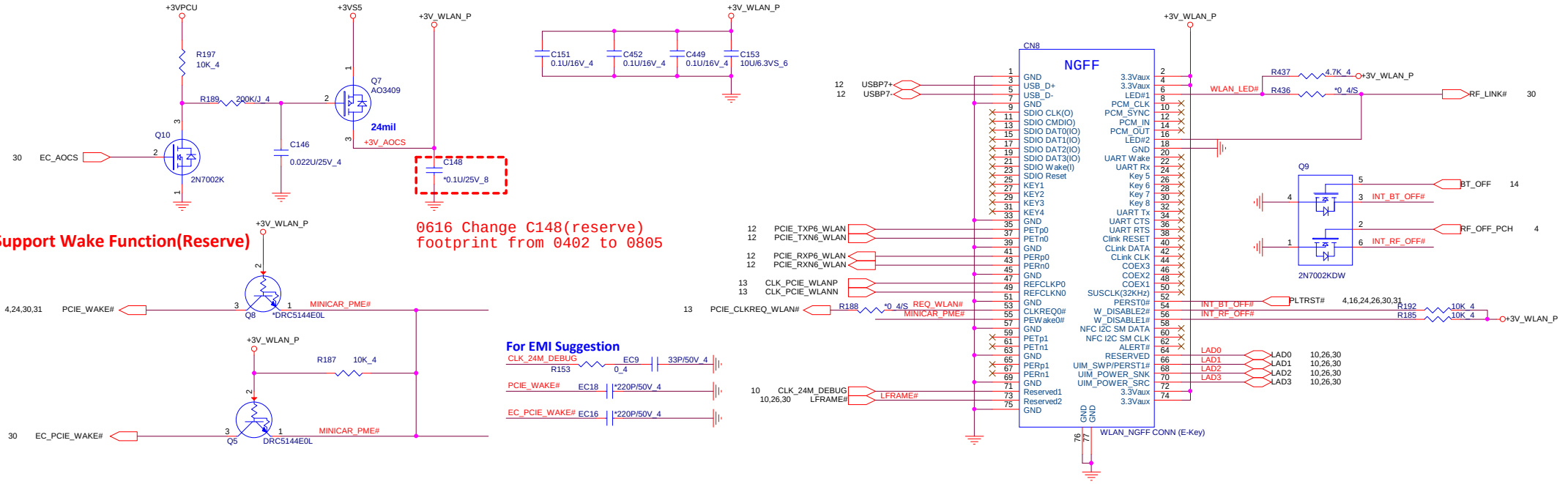
Accelerometer Sensor



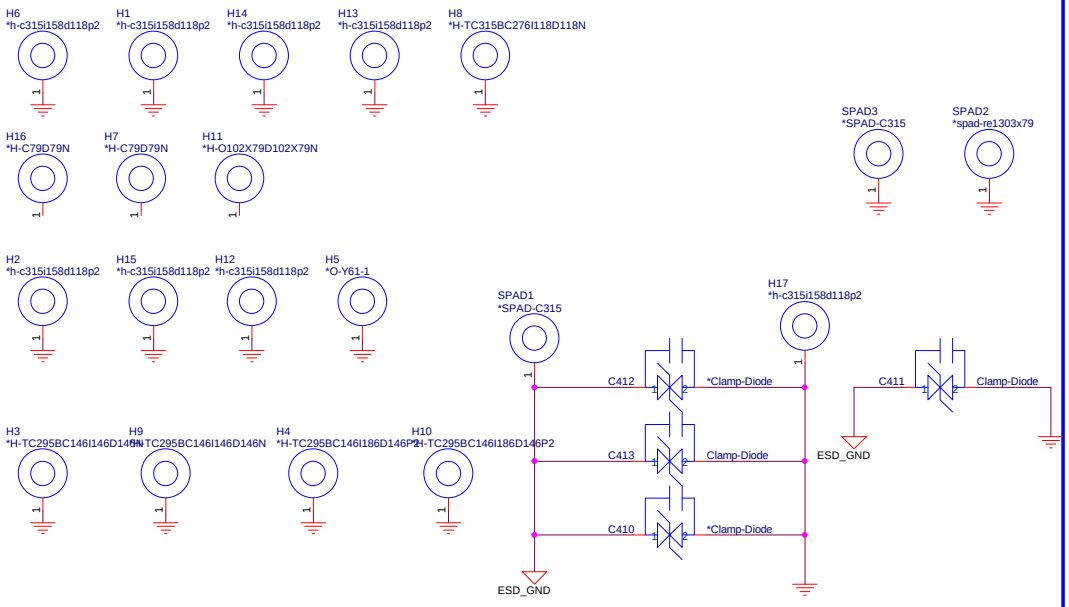


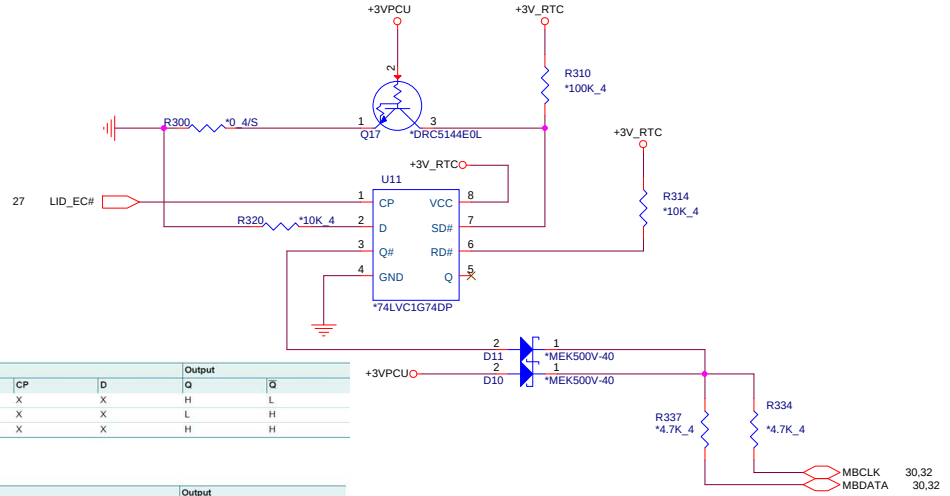
PROJECT : Y62P/Y63P Quanta Computer Inc.		
Size: Custom	Document Number: PB/TP/KB/FAN/EMI Cap	Rev: 1A
Date: Wednesday, July 22, 2015	Sheet 27 of 42	

Mini Card
WLAN/BT(Option)



Hole





Input				Output	
SD	RD	CP	D	Q	Q
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care.

Input				Output	
SD	RD	CP	D	Q_{n+1}	$\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

[1] H = HIGH voltage level;
L = LOW voltage level;
↑ = LOW-to-HIGH CP transition;
Q_{n+1} = state after the next LOW-to-HIGH CP transition.

4,10,15,16,29,30,33,35,36,39 +3VSS
27 +3V_WLAN_P
4,13,15,27,32 +3V_RTC
2,4,10,11,12,13,14,15,16,17,18,20,21,22,23,24,25,26,27,29,30,31,37,39 +3V
21,22,23,26,27,39 +5V
6,13,18,27,30,32,33 +3VPCU

PROJECT : Y62P/Y63P
Quanta Computer Inc.

Size	Document Number	Rev
Custom	WLAN/G-Sensor/G-CLK/TS	1A
Date: Wednesday, July 22, 2015	Sheet 28of 42	

2,4,10,11,12,13,14,15,16,17,18,20,21,22,23,24,25,26,27,30,31,37,39
4,10,15,16,28,30,33,35,36,39

+3V
+3VS5

FOR ISH: Stuff (Default)
FOR External Sensor HUB: Stuff

Note: Place all capacitors close to IT8350.

+3V
C476 0.1U/16V_4
C475 0.1U/16V_4
C469 0.1U/16V_4
C290 0.1U/16V_4
C250 0.1U/16V_4

20MIL

+3V R221 *0_6 AVCC
L9 BLM15PX181SN1D
C465 1000P/50V_4
C462 0.1U/16V_4
L23 BLM15PX181SN1D
IT8350_AGND

20MIL

20MIL +3V
10MIL (For PLL Power)
+3VPLL L10 BLM15PX181SN1D +3V
C316 0.1U/16V_4 AVCC

U19
IT8350E_LQFP-48

4 16 23 36 1 VSTBY VSTBY VSTBY VSTBY VSTBY
7 VSTBY(PLL)
33 AVCC

+3V
R461 100K/F_4 D12 MEK500V-40
WRST# 11 WRST#
C477 1U/10V_4

+3V
R455 1.5K_4
USBP4+

USB for Host

12 USBP4-
12 USBP4+
1 4 L24 2 3
USBP4- 37
USBP4+ 38
*MCM2012B900GBE
GPH5/ID5/DM
GPH6/ID6/DP

USB

SM BUS

SMCLK0/GPB3 47 SMCLK0 TP113
SMDAT0/GPB4 48 SMDAT0 TP114
SMCLK2/GPF6 2 SMCLK2
SMDAT2/GPF7 3 SMDAT2
SMCLK4/GPE0 13 SMCLK4_L
SMDAT4/GPE7 12 SMDAT4_L

Reserved SMBus channel 0 for debugging & updating FW
Reserved
SMbus channel 4 for connecting the Sensor (G-sensor)

FSPI

40 FSCE#/GPG3
41 FMOSI/GPG4
42 FMISO/GPG5
44 FSCK/GPG7

PWM

PWM0/GPA0 15
PWM1/GPA1 14
PWM4/SMCLK5/GPA4 17
PWM5/SMDAT5/GPA5 19
PWM6/SSCK/GPA6 18
Q_LID_EC# 15,30

0708 Add R580 between +3V and GPI5

Reserved TX/RX for debugging

UART

RXD/SIN0/GPB0 45 RXD TP111
TXD/SOUT0/GPB1 46 TXD TP112

if no use ADC function, please pull down to GND

A/D

ADC0/GPI0 27 GPI0
ADC1/SMINT0/GPI1 28 SMINT0
ADC2/SMINT1/GPI2 29 SMINT1
ADC3/SMINT2/GPI3 30 SMINT2
ADC4/SMINT3/GPI4 31 SMINT3
ADC5/GPI5 32 GPI5

SMINTx for sensor interrupt

+3V R580 10K_4 GPI5

GPI0 R451 4.7K_4
SMINT0 R452 *4.7K_4
SMINT1 R234 *4.7K_4
SMINT2 R235 *4.7K_4
SMINT3 R454 *4.7K_4
GPI5 R215 *4.7K_4

0708 Change R215 from I to NI

GPG2 can't floating

SSPI

SSCE0#/GPG2 39 GPIOG2
KSO17/SMISO/GPC5 25 GPIOC5
KSO16/SMOSI/GPC3 22 GPIOC3
TP104
TP106
R239 *100K/F_4
R224 100K/F_4

+3V R430 0_4 +3V_HOME
+3VS5 R425 *0_4

PWRSW 6 PWRSW/GPE4
TP110 KSI0 21 KSI0
TP109 KSI6 20 KSI6
TP108 KSI7 26 KSI7
TP107 GPG6 43 GPG6

GPIO

CLOCK

CK32KE/GPJ7 9 CK32KE
CK32K/GPJ6 8 CK32K
32.768KHZ_10 Y4
C474 22P/50V_4
C473 27P/50V_4

0708 Change C473 from 22P to 27P

External crystal is must be item when USB func. is used !

VSS 5 VSS 24 VSS 35 VCORE 10 AVSS 34
C478 0.1U/16V_4
IT8350_AGND

+3V R448 R431 R419 *10K_4
ACC_INT
AE_INT
GYRO_INT
R447 R429 R418 *10K_4

L22 *BLM18BA470SN1D/S
IT8350_AGND

12 USBP8-
12 USBP8+
1 4 L6 2 3
USBP8-
USBP8+
*MCM2012B900GBE

32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.

+3V
SMCLK0 R458 499/F_4
SMDAT0 R457 499/F_4
SMCLK2 R459 499/F_4
SMDAT2 R460 499/F_4

Close to CN3

14 ISH_GYRO_DRDY R426 *0_4 GYRO_DRDY
14 ISH_GYRO_INT R420 *0_4 GYRO_INT
14 ISH_AE_INT R432 *0_4 AE_INT
14 ISH_ACC_INT R449 *0_4 ACC_INT
DISABLE KB

0630 Delete R446 to COOL SENSE and GPI0

Close to CN3

SMINT0 R427 0_4 GYRO_DRDY
SMINT1 R421 0_4 GYRO_INT
SMINT2 R433 0_4 AE_INT
SMINT3 R453 0_4 ACC_INT

GPI5 R211 0_4 Close to U23
DISABLE KB 14,29,30

Accelerometer Sensor

Put it on MB side

+3V C315 10U/6.3V_6 C309 0.1U/16V_4
U9 HP3DC2TR
Vdd_IO 1
VDD 14
NC 2
NC 3
ACC_INT 11
INT1 9
INT2 7
SDO 6
SDA
SCL 4
CS 8
RESERVED 10
RESERVED 13
RESERVED 15
RESERVED 16
GND 5
GND 12
TP47
SMDAT4
SMCLK4

Close to U9

14 ISH_I2C0_SDA ISH_I2C0_SDA Q18A *2N7002KDW Dual SMDAT4
To ISH
14 ISH_I2C0_SCL ISH_I2C0_SCL Dual Q18B *2N7002KDW SMCLK4
R299 1K_4
R313 1K_4
+3V

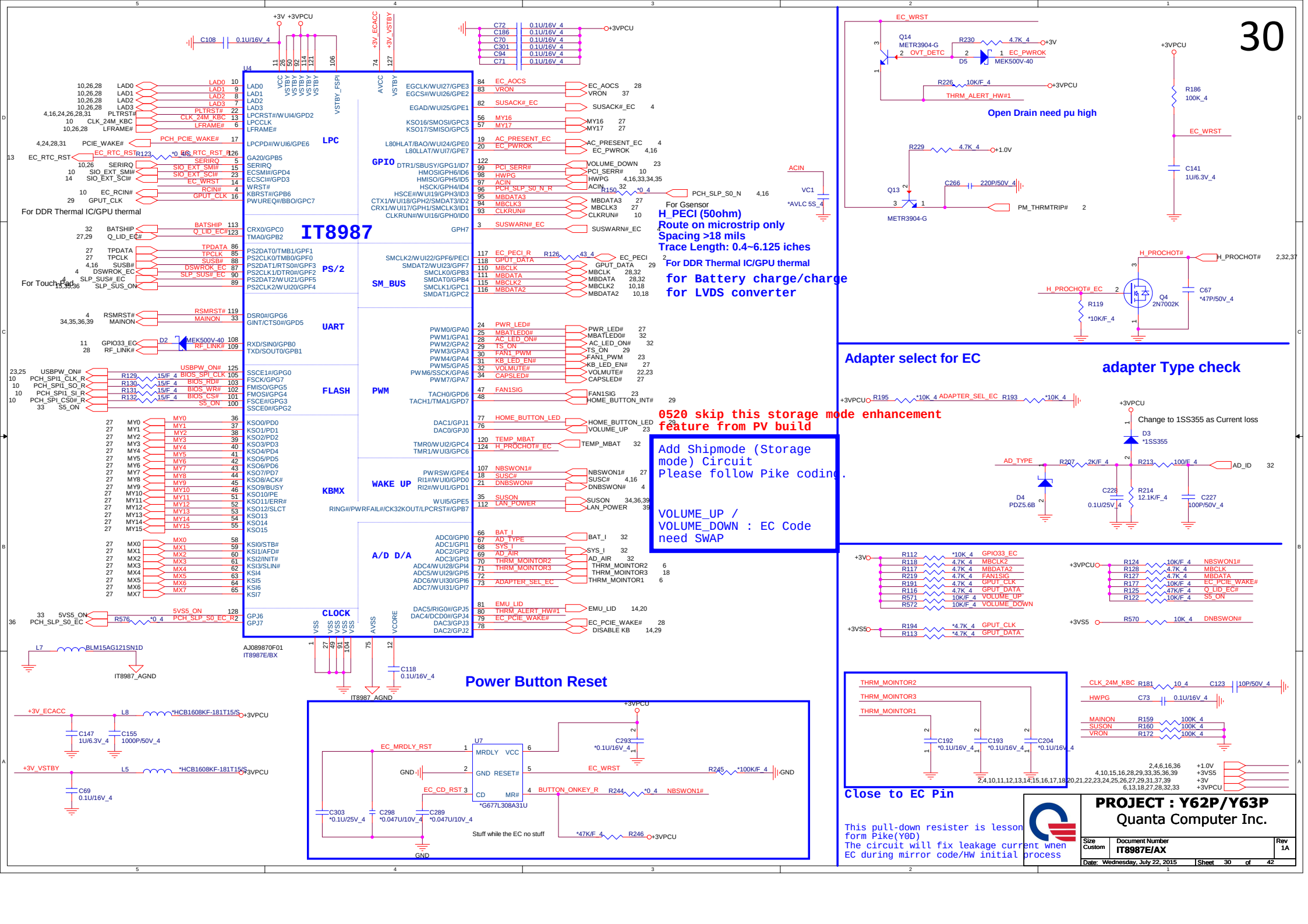
To Sensor Hub SMBUS

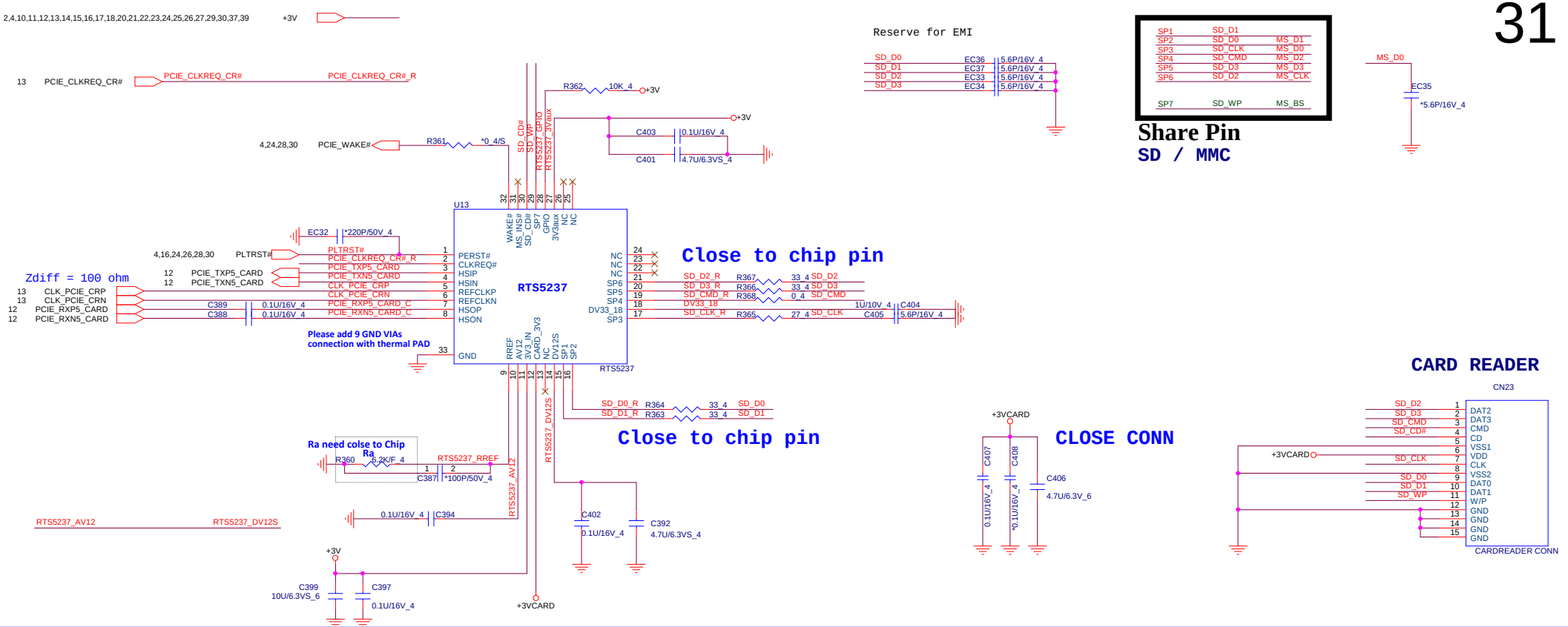
Close to U23

SMDAT4_L R240 0_4 SMDAT4
SMCLK4_L R258 0_4 SMCLK4

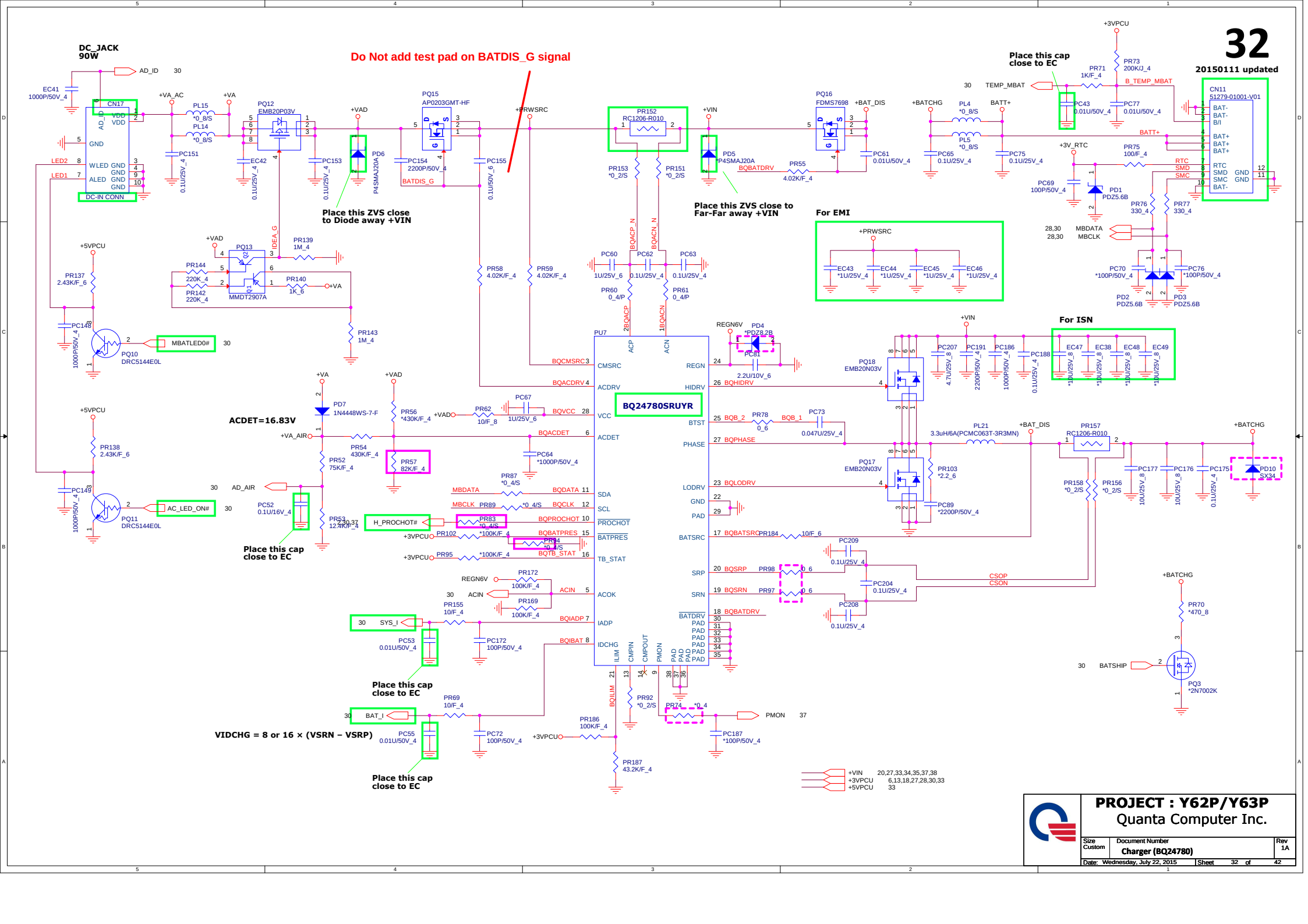
C99 0.1U/16V_4 SMD FPC 20P
+3V
30 GPUT_DATA
30 GPUT_CLK
SMDAT4
SMCLK4
+3V_HOME
30 TS_ON
TS_ON
R428 *0_4S
USBP8-
USBP8+
AE_INT
GYRO_DRDY
30 HOME_BUTTON_INT#
GYRO_INT
30 HOME_BUTTON_LED
R149 200/F_6
CN7

PROJECT : Y62P/Y63P		
Quanta Computer Inc.		
Size: Custom	Document Number: ITE8350/HP9DS0/HP3DC2	Rev: 1A
Date: Wednesday, July 22, 2015	Sheet 29 of 42	


IT8987
LPC
GPIO
PS/2
SM_BUS
UART
FLASH
PWM
KBMX
WAKE UP
A/D D/A
CLOCK
For DDR Thermal IC/GPU thermal
For Touch Pad
For Gsensor
H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 iches
for Battery charge/charge
for LVDS converter
0520 skip this storage mode enhancement
feature from PV build
Add Shipmode (Storage mode) Circuit
Please follow Pike coding.
VOLUME_UP /
VOLUME_DOWN : EC Code need SWAP
Open Drain need pu high
Adapter select for EC
adapter Type check
Change to 1SS355 as Current loss
Power Button Reset
Close to EC Pin
This pull-down resister is lesson form Pike(Y0D)
The circuit will fix leakage current when EC during mirror code/HW initial process
Stuff while the EC no stuff
AJ089870F01
IT8987E/BX
PROJECT : Y62P/Y63P
Quanta Computer Inc.
Size Custom
Document Number IT8987E/AX
Rev 1A
Date: Wednesday, July 22, 2015
Sheet 30 of 42



PROJECT : Y62P/Y63P Quanta Computer Inc.		
Size: Custom	Document Number: CR RTS5237 & HOLE	Rev: 1A
Date: Wednesday, July 22, 2015	Sheet 31 of 42	

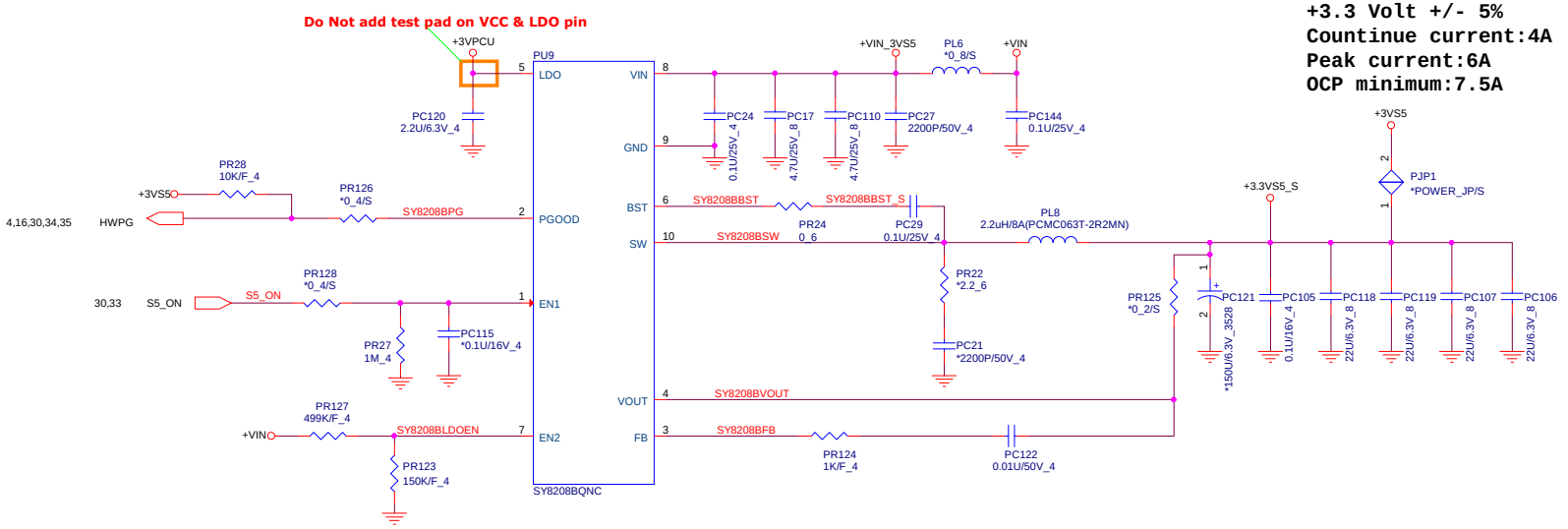

32
20150111 updated
DC_JACK
90W
Do Not add test pad on BATDIS_G signal
Place this cap close to EC
Place this ZVS close to Diode away +VIN
Place this ZVS close to Far-Far away +VIN
For EMI
For ISN
ACDET=16.83V
VIDCHG = 8 or 16 × (VSRN – VSRP)
BQ24780SRUYR
PROJECT : Y62P/Y63P
Quanta Computer Inc.
Charger (BQ24780)
Wednesday, July 22, 2015
Sheet 32 of 42

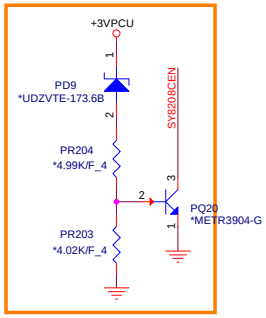
DC/DC +3VS5/+5VS5

+3VS5 4,10,15,16,28,29,30,35,36,39
+5VS5 4,23,25,34,35,36,37,38,39

Do Not add test pad on VCC & LDO pin

+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

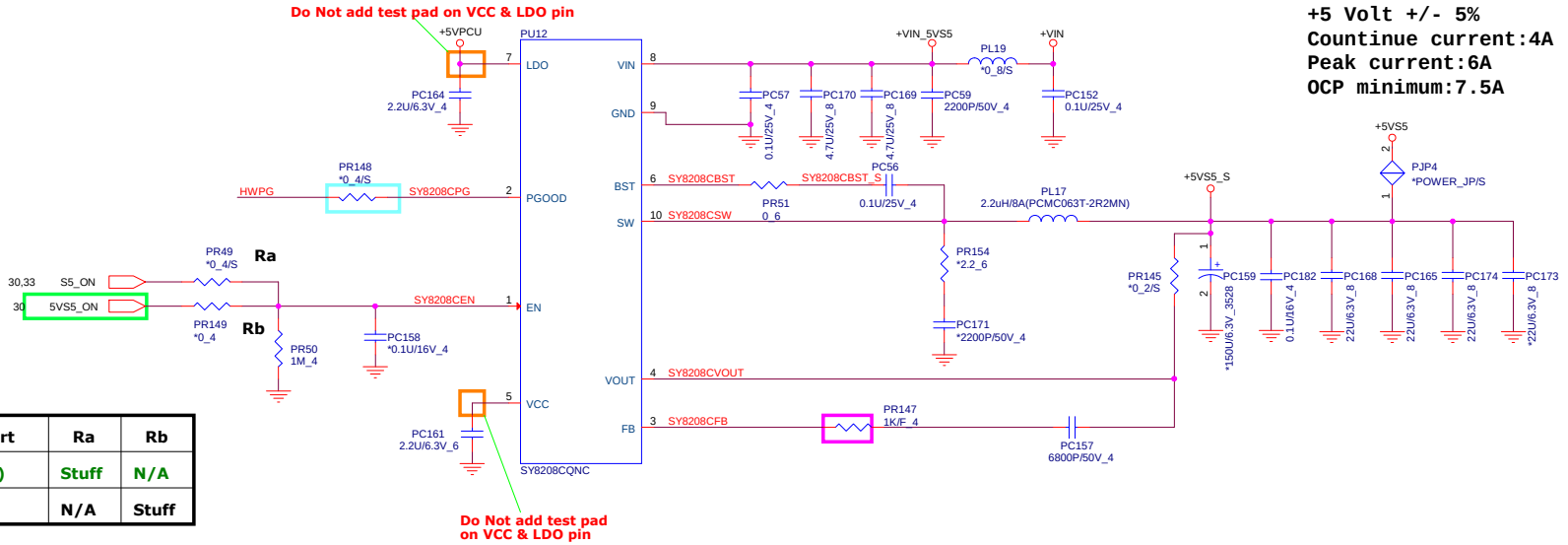




2014/12/17 updated

Do Not add test pad on VCC & LDO pin

+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

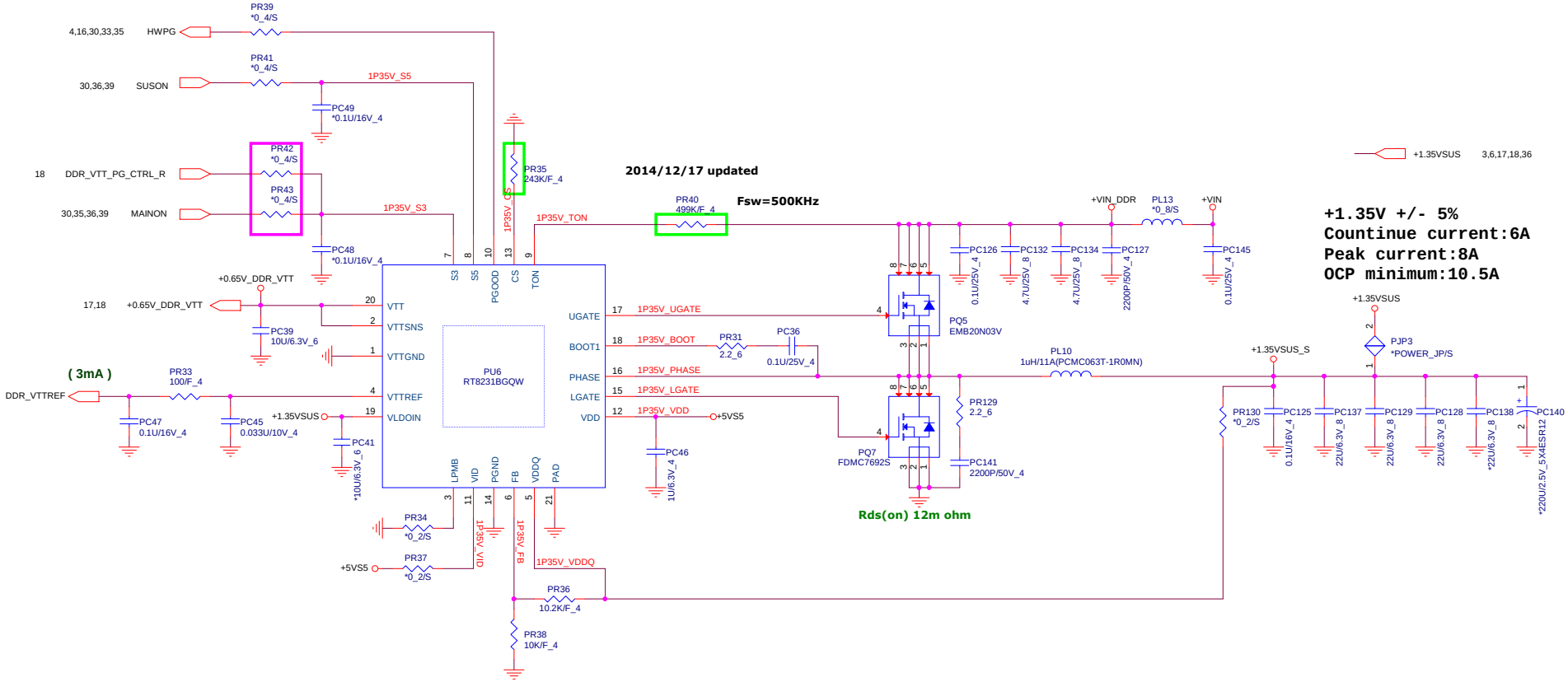


Do Not add test pad on VCC & LDO pin

USB charge support	Ra	Rb
Napa (No support)	Stuff	N/A
Whisky (Support)	N/A	Stuff

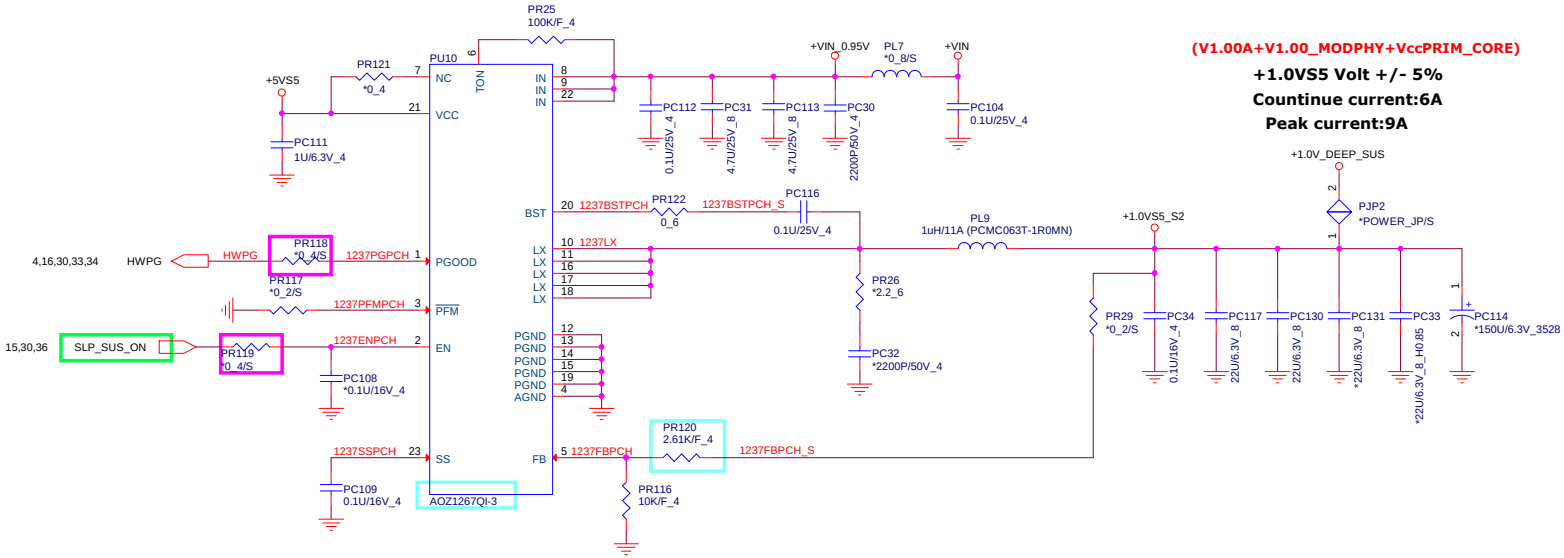
PROJECT : Y62P/Y63P
Quanta Computer Inc.

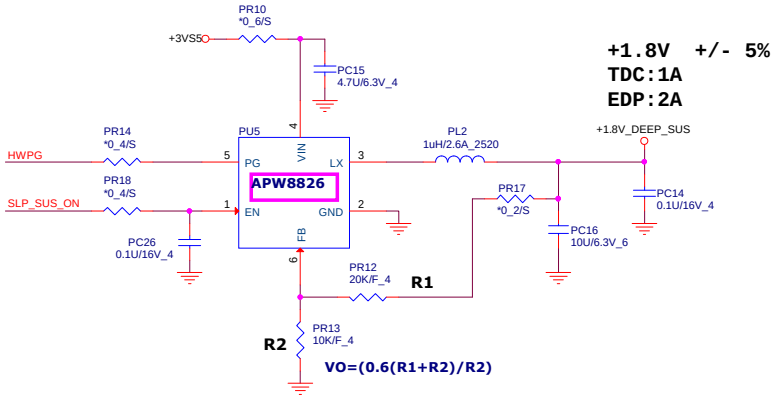
Size	Document Number	Rev
Custom	3/5VS5 (SY8208B/SY8208C)	1A
Date: Wednesday, July 22, 2015	Sheet 33 of 42	



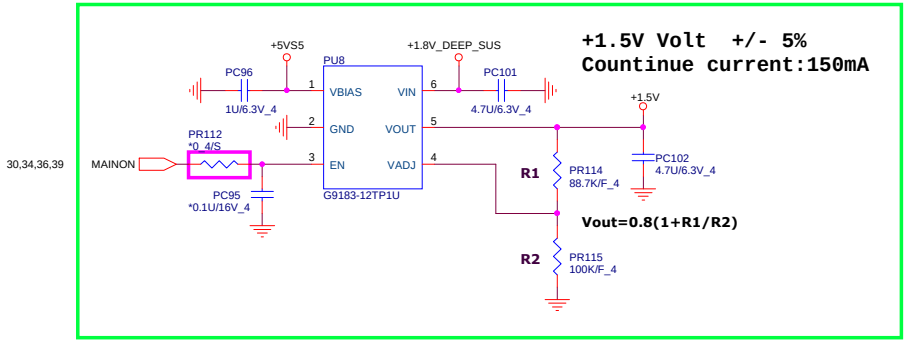
PROJECT : Y62P/Y63P	
Quanta Computer Inc.	
Size: Custom	Document Number: DDR3 (RT8231B)
Rev: 1A	
Date: Wednesday, July 22, 2015	Sheet 34 of 42

+VIN 20,27,32,33,34,37,38
+3VS5 4,10,15,16,28,29,30,33,36,39
+5VS5 4,23,25,33,34,36,37,38,39
+1.0V_DEEP_SUS 9,13,15,16,36
+1.8V_DEEP_SUS 9,15





20150111 updated



PROJECT : Y62P/Y63P
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.1VS5 (RT8228)/2.5V	1A
Date: Wednesday, July 22, 2015	Sheet 35 of 42	

+1.0V 2,4,6,16,30
+3VS5 4,10,15,16,28,29,30,33,35,39
+5VS5 4,23,25,33,34,35,37,38,39
+VCCIO 2,6,16
+VCCSTPLL 2,4,5,6,9,37
+1.0V_DEEP_SUS 9,13,15,16,35

20150107 updated

<= 65usec full load ready

TDC:0.16A

PR8 *0_4
PR7 *0_4
PR19 *47K/F_4
PR11 *0_6/S
PR21 *0_6/S
PC7 0.1U/16V_4
PC20 *1000P/50V_4
PC11 0.1U/16V_4
PC19 *10U/6.3V_6
PU3 MC74VHC1G08DFT2G
PQ1 *DMG3414U-7
PR23 *22_8
PR15 *1M_4
PR16 *2M_4
PQ2A *2N7002KDW
PQ2B *2N7002KDW

30,34,36,39 SUSON
15,30,35,36 SLP_SUS_ON
+VCCSTG_ON

If support Modern standby mode stuff Rb/Rc remove Ra

<= 65usec full load ready

TDC:0.04A

TDC:3A

Ra
Rb
Rc
Rd

PU2 AOZ1335DI
PC5 1U/6.3V_4
PC4 0.1U/16V_4
PC2 0.1U/16V_4
PC3 *10U/6.3V_6
PC1 *0.1U/16V_4
PR4 0_6
PR270 *0_6
PR3 *0_6/S
PR11173 0_4
PR6 0_4
PR11174 *0_4

20141229 updated

30,34,35,36,39 MAINON

Support Modern standby mode
1. Remove Ra/Rc & stuff Rb/Rd
2. stuff block C & D
3. Block E for option

Reserve for Modern StandBy

Block C

Block E for option

Modern StandBy

<= 65usec full load ready

TDC:0.26A

PR2 *0_4
PR11177 0_4
PR11176 0_4
PR1 *0_4
PC302 0.1U/16V_4
PR273 47K/F_4
PC295 *1000P/50V_4
PU1 MC74VHC1G08DFT2G
PQ40 DMG3414U-7
PC301 0.1U/16V_4
PR275 *0_6/S
PC294 0.1U/16V_4
PC296 *10U/6.3V_6
PR11175 *0_4
PR276 *22_8
PR274 *1M_4
PR272 *2M_4
PQ41A *2N7002KDW
PQ41B *2N7002KDW

30,34,35,36,39 MAINON
30,34,36,39 SUSON
15,30,35,36 SLP_SUS_ON
30,36 PCH_SLP_S0_EC

Block D

<= 65usec full load ready

TDC:0.12A

PR245 *47K/F_4
PC269 0.1U/16V_4
PC268 *1000P/50V_4
PQ34 *DMG3414U-7
PR246 *0_6/S
PC267 *0.1U/16V_4
PC270 *10U/6.3V_6
PR11172 *22_8
PR11170 *1M_4
PR11171 *2M_4
PQ58A *2N7002KDW
PQ58B *2N7002KDW

Reserve for Modern StandBy

PROJECT : Y62P/Y63P
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.0V/+VCCSTPLL	1A
Date: Wednesday, July 22, 2015	Sheet 36 of 42	

CPU CORE
TDC:25A
EDP:40A

VCCGT
TDC:22A
EDP:45A

Place close to VCORE Inductor

Place close to VCCSA Inductor

Place close to GT1 Inductor

place close to GT MOSFET

place close to VCORE MOSFET

program IccMax_2ph

DCR=0.48m ohm

DCR=0.48m ohm

For Acoustic

For Acoustic

For Acoustic

PU14 NCP81206

PQ14 FDMS7698

PQ9 FDMS0308AS

PQ8 FDMS0308AS

PQ19 FDMS3664S

PQ4 *FDMS3664S

PL16 0.15uH/40A(PCMB104T-R15MS0R487)

PL24 0.15uH/40A(PCMB104T-R15MS0R487)

PL18 *0_8/S

PL22 *0_8/S

+VCC_CORE

+VIN_VCC_CORE

+VIN

+VCCGT

+VIN_VCCGT

+VCCSTPLL

+VCCSA

+3V

+5VS5

VCC_SENSE
VSS_SENSE
VCCSA_SENSE
VSSSA_SENSE
VCCGT_SENSE
VSSGT_SENSE

VR_SVID_DATA
VR_SVID_ALERT#
VR_SVID_CLK
H_PROCHOT#

CSN_CORE
SWN_CORE
CSN_GT1
SWN_GT1

+3V 2,4,10,11,12,13,14,15,16,17,18,20,21,22,23,24,25,26,27,29,30,31,39
+VIN 20,27,32,33,34,35,38
+5VS5 4,23,25,33,34,35,36,38,39
+VCCSA 6,38
+VCCGT 7
+VCCSTPLL 2,4,5,6,9,36
+VCC_CORE 5

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Size	Document Number	Rev
Custom	CPU VR IC (NCP81206)	1A
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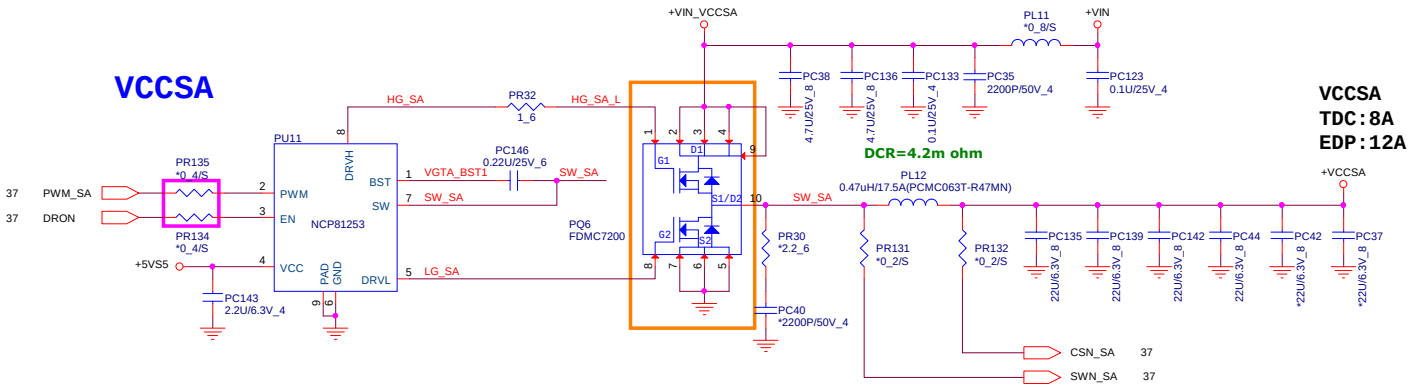
+VIN 20,27,32,33,34,35,37
+5VS5 4,23,25,33,34,35,36,37,39
+VCCSA 6,37



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Size: Custom	Document Number: +VCCSA (NCP81253)		Rev: 1A
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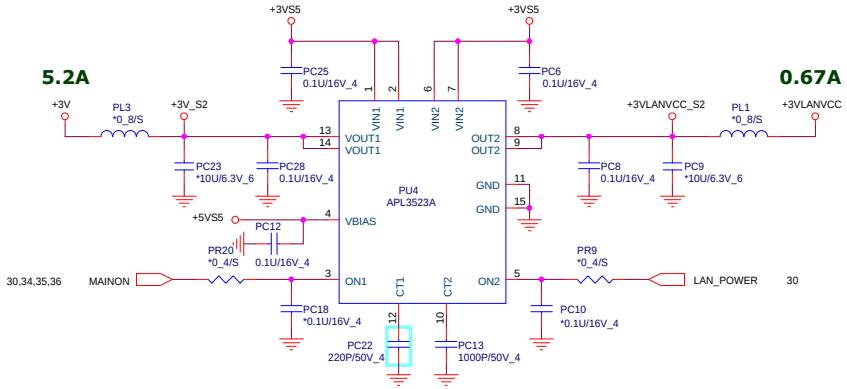

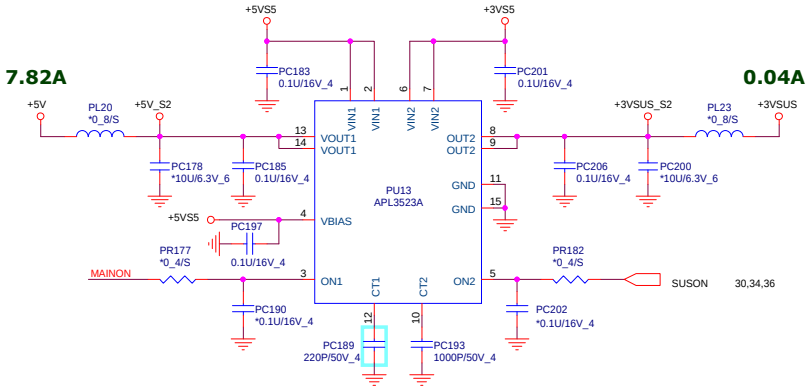

27 +3VSUS
2,4,10,11,12,13,14,15,16,17,18,20,21,22,23,24,25,26,27,29,30,31,37 +3V
21,22,23,26,27 +5V
4,10,15,16,28,29,30,33,35,36 +3VS5
4,23,25,33,34,35,36,37,38 +5VS5
24 +3VLANVCC

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Size	Document Number	Rev
Custom	Load switch IC (APL3523A)	1A

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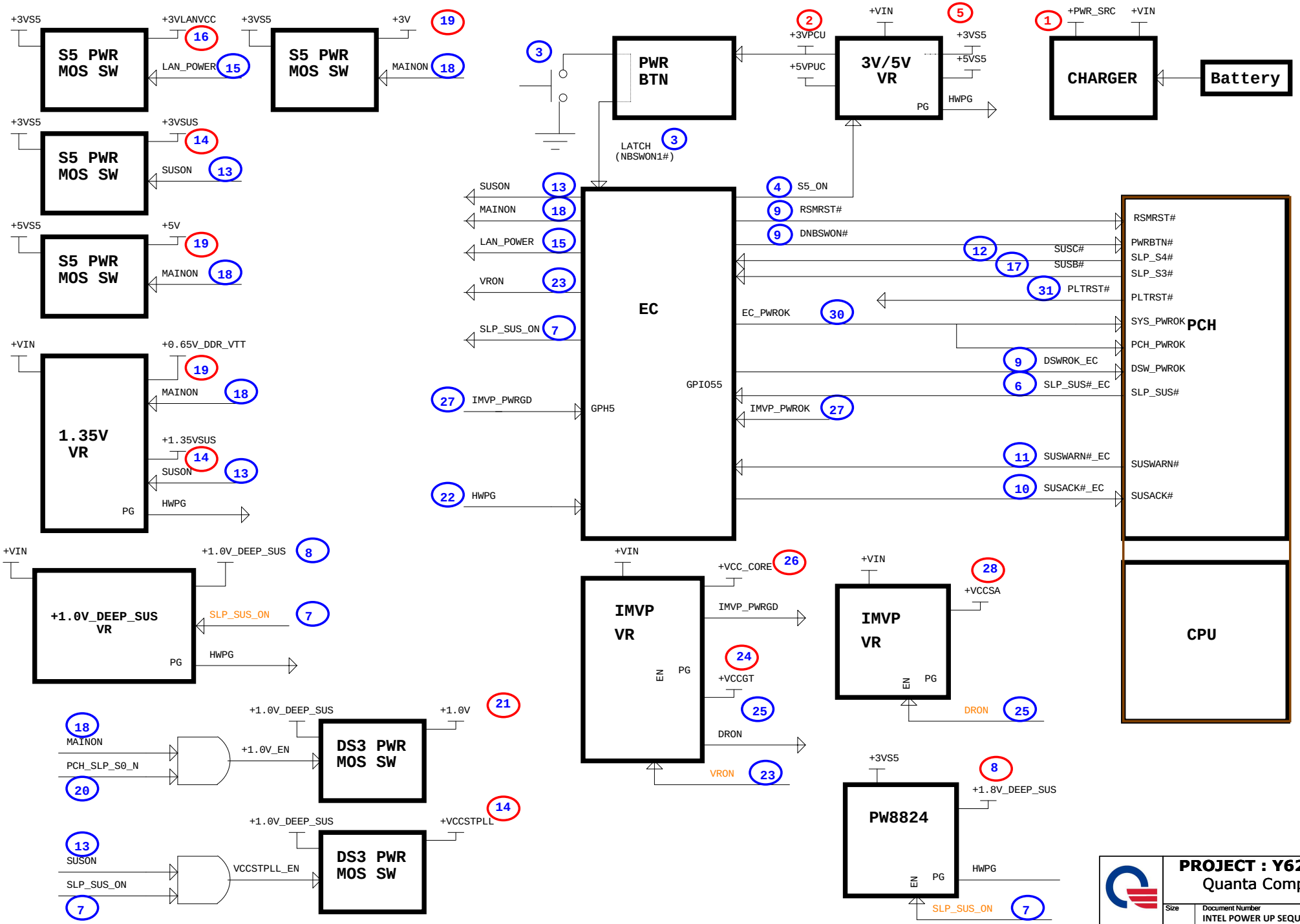

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Size	Document Number	Rev
	INTEL POWER UP SEQUENCE	1A

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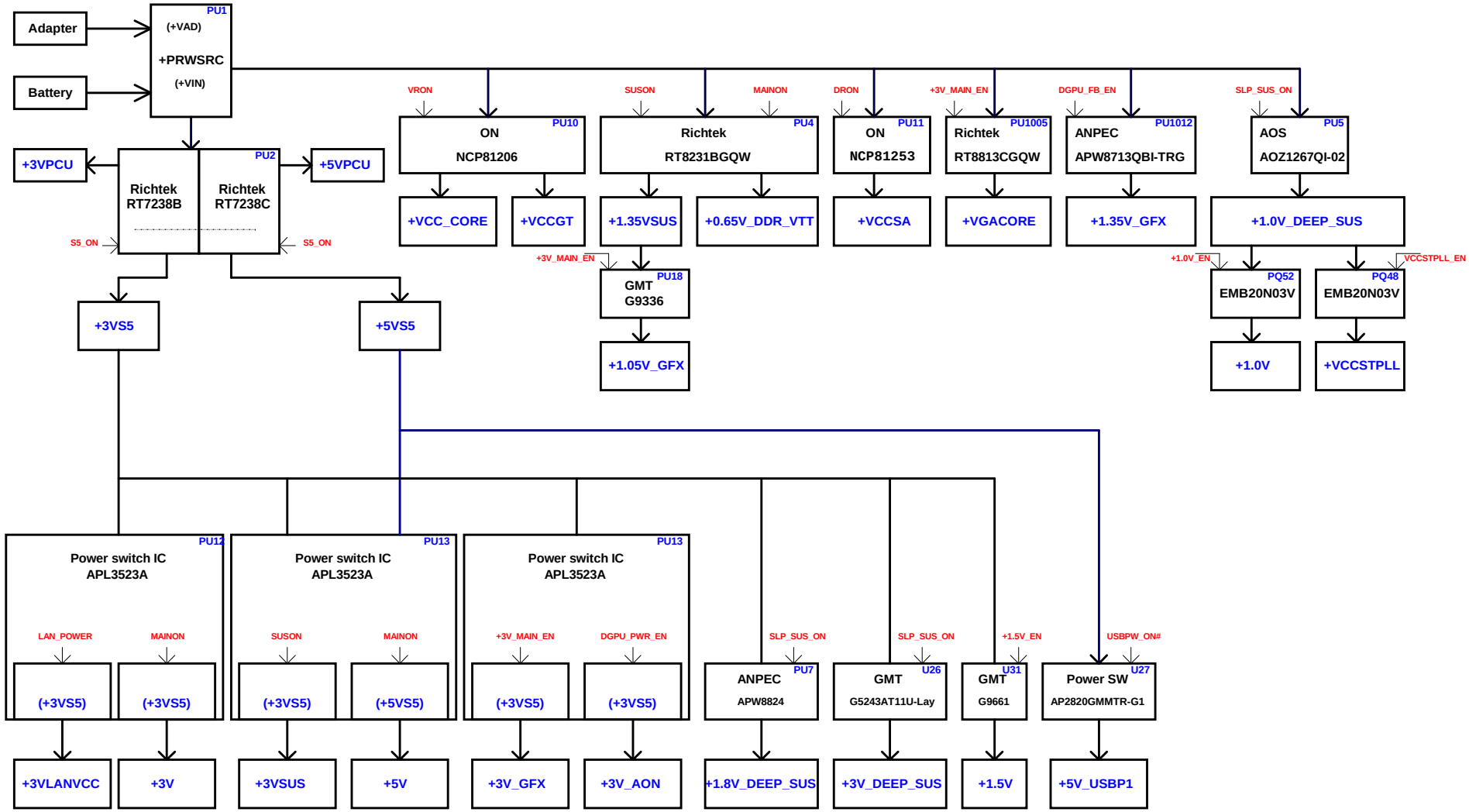

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Size	Document Number	Rev
	Power Block Diagram	1A
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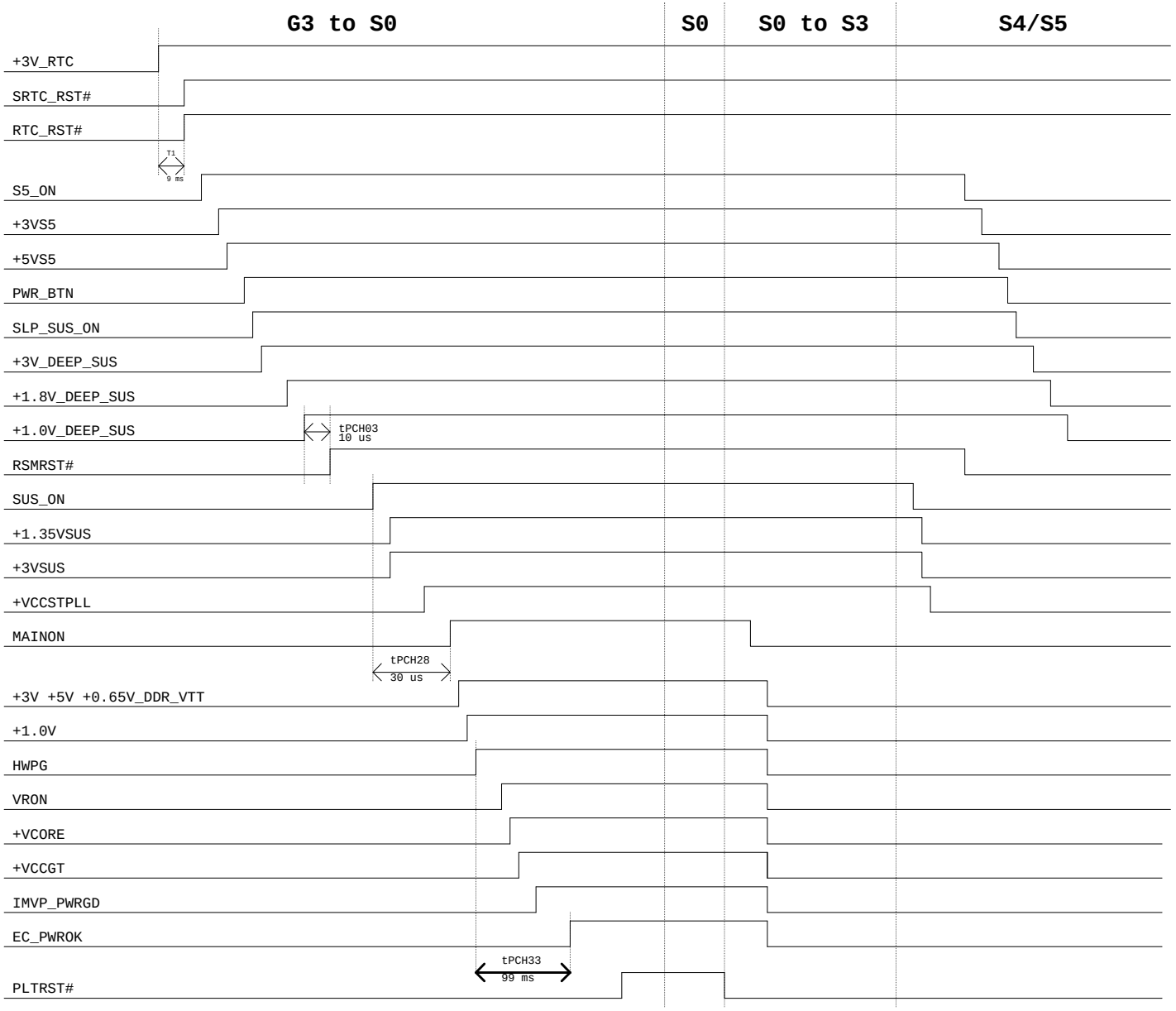

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Size	Document Number	Rev
	Intel POWER UP SEQUENCE	1A
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