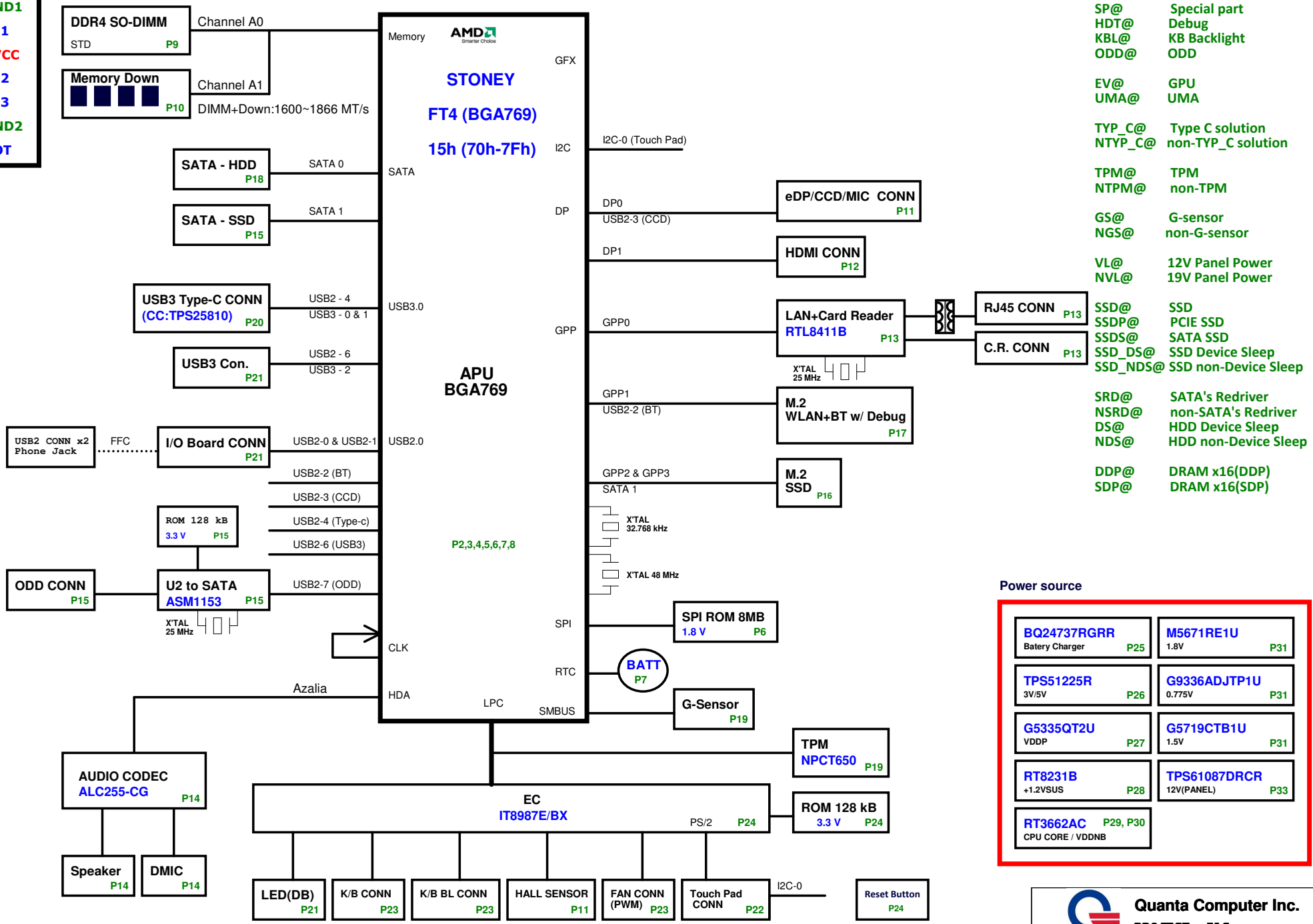
ZAS BLOCK DIAGRAM

01

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND1
- LAYER 3 : IN1
- LAYER 4 : SVCC
- LAYER 5 : IN2
- LAYER 6 : IN3
- LAYER 7 : GND2
- LAYER 8 : BOT



SP@ Special part
HDT@ Debug
KBL@ KB Backlight
ODD@ ODD

EV@ GPU
UMA@ UMA

TYP_C@ Type C solution
NTYP_C@ non-TYP_C solution

TPM@ TPM
NTPM@ non-TPM

GS@ G-sensor
NGS@ non-G-sensor

VL@ 12V Panel Power
NVL@ 19V Panel Power

SSD@ SSD
SSDP@ PCIE SSD
SSDS@ SATA SSD
SSD_DS@ SSD Device Sleep
SSD_NDS@ SSD non-Device Sleep

SRD@ SATA's Redriver
NSRD@ non-SATA's Redriver
DS@ HDD Device Sleep
NDS@ HDD non-Device Sleep

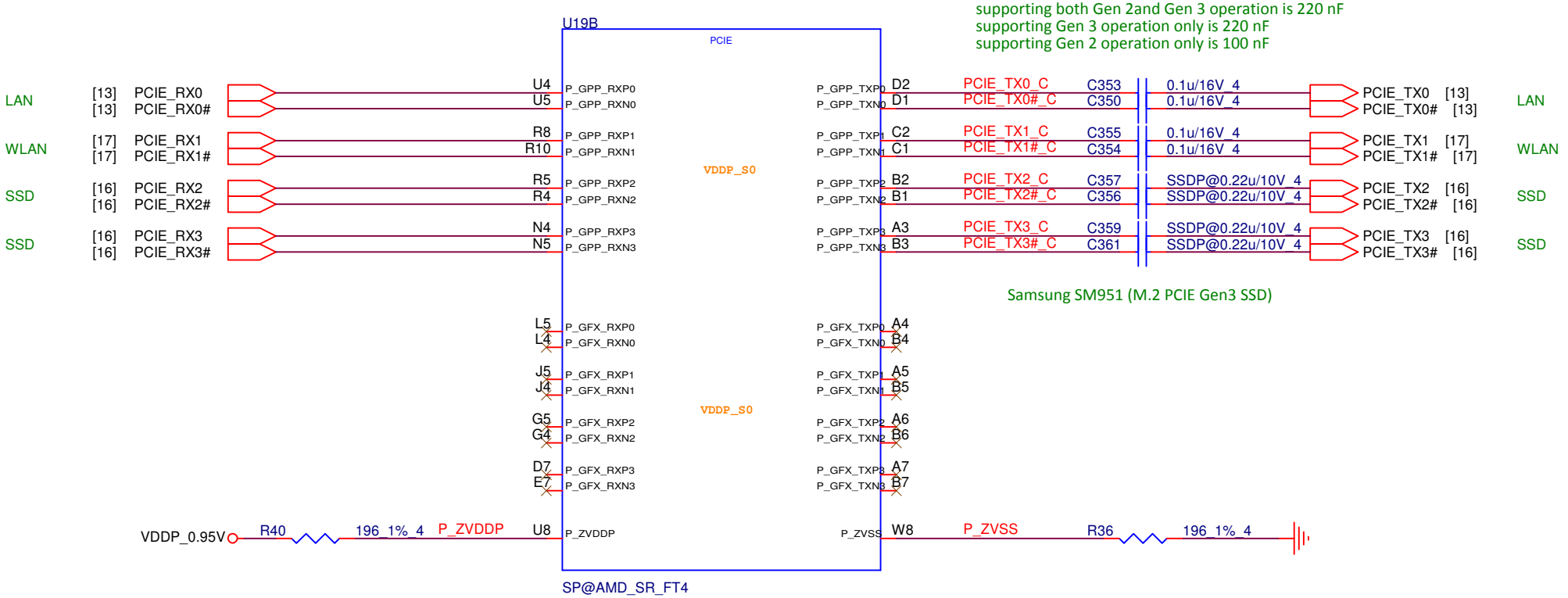
DDP@ DRAM x16(DDP)
SDP@ DRAM x16(SDP)

Power source

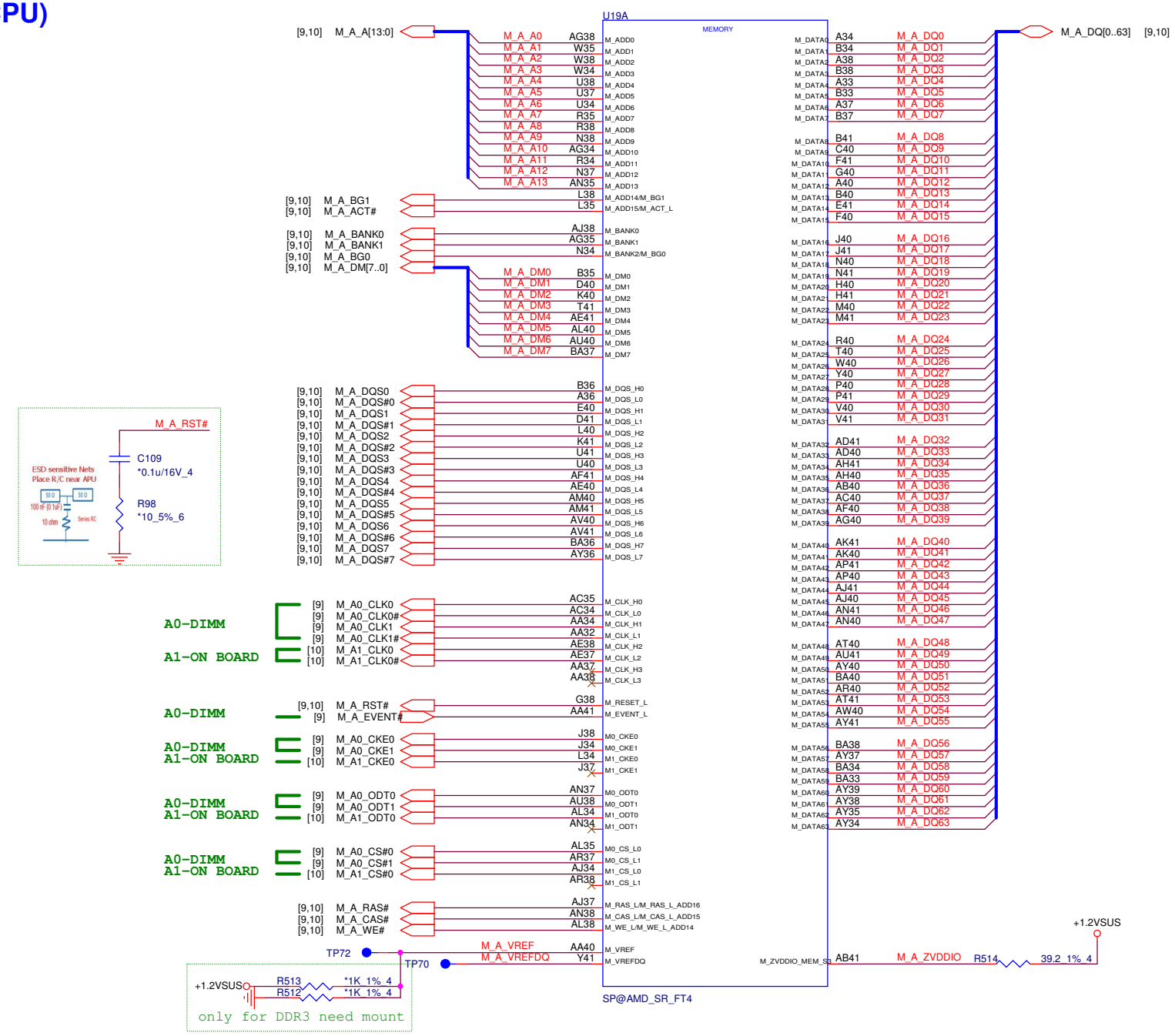
BQ24737RGRR Batery Charger P25	M5671RE1U 1.8V P31
TPS51225R 3V/5V P26	G9336ADJTP1U 0.775V P31
G5335QT2U VDDP P27	G5719CTB1U 1.5V P31
RT8231B +1.2VSUS P28	TPS61087DRCR 12V(PANEL) P33
RT3662AC P29, P30 CPU CORE / VDDNB	

Squirtle_SR SSID : 1192

Quanta Computer Inc.
PROJECT : ZAS
Size | Document Number: Block Diagram | Rev 1A
Date: Friday, March 24, 2017 Sheet 1 of 35

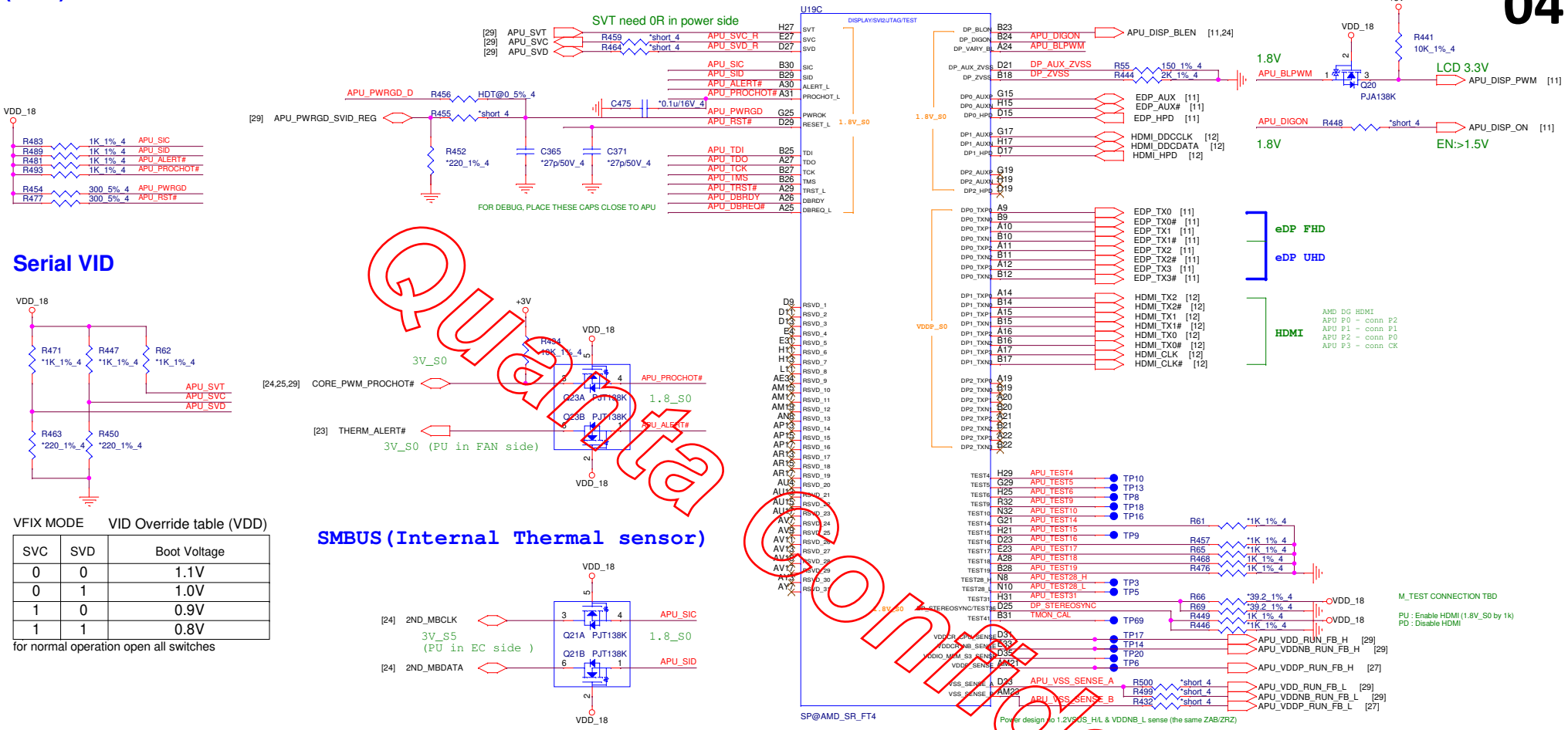


Quanta Computer Inc.		
PROJECT : ZAS		
Size	Document Number: FT4 PCIE I/F(1/7)	Rev: 1A
Date: Friday, March 24, 2017	Sheet 2 of 35	



Quanta Computer Inc.		
PROJECT : ZAS		
Size	Document Number: FT4 DDR4 I/F(2/7)	Rev: 1A
Date: Friday, March 24, 2017	Sheet 3 of 35	

(CPU)



Serial VID

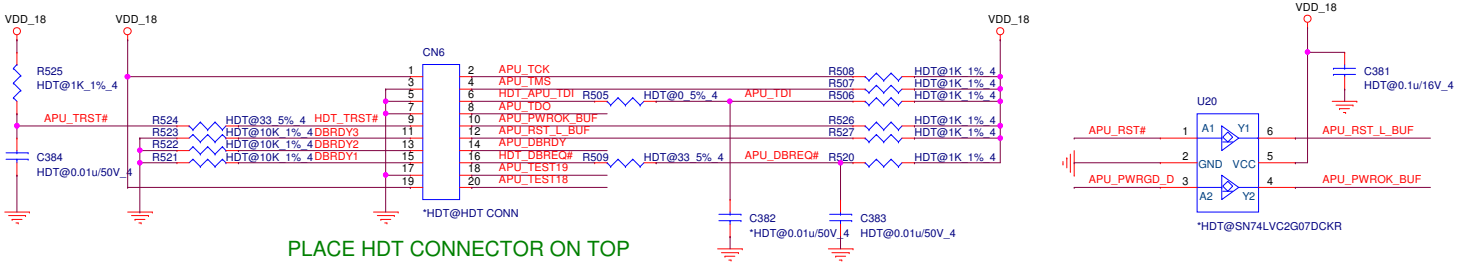
VFIX MODE VID Override table (VDD)

SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

for normal operation open all switches

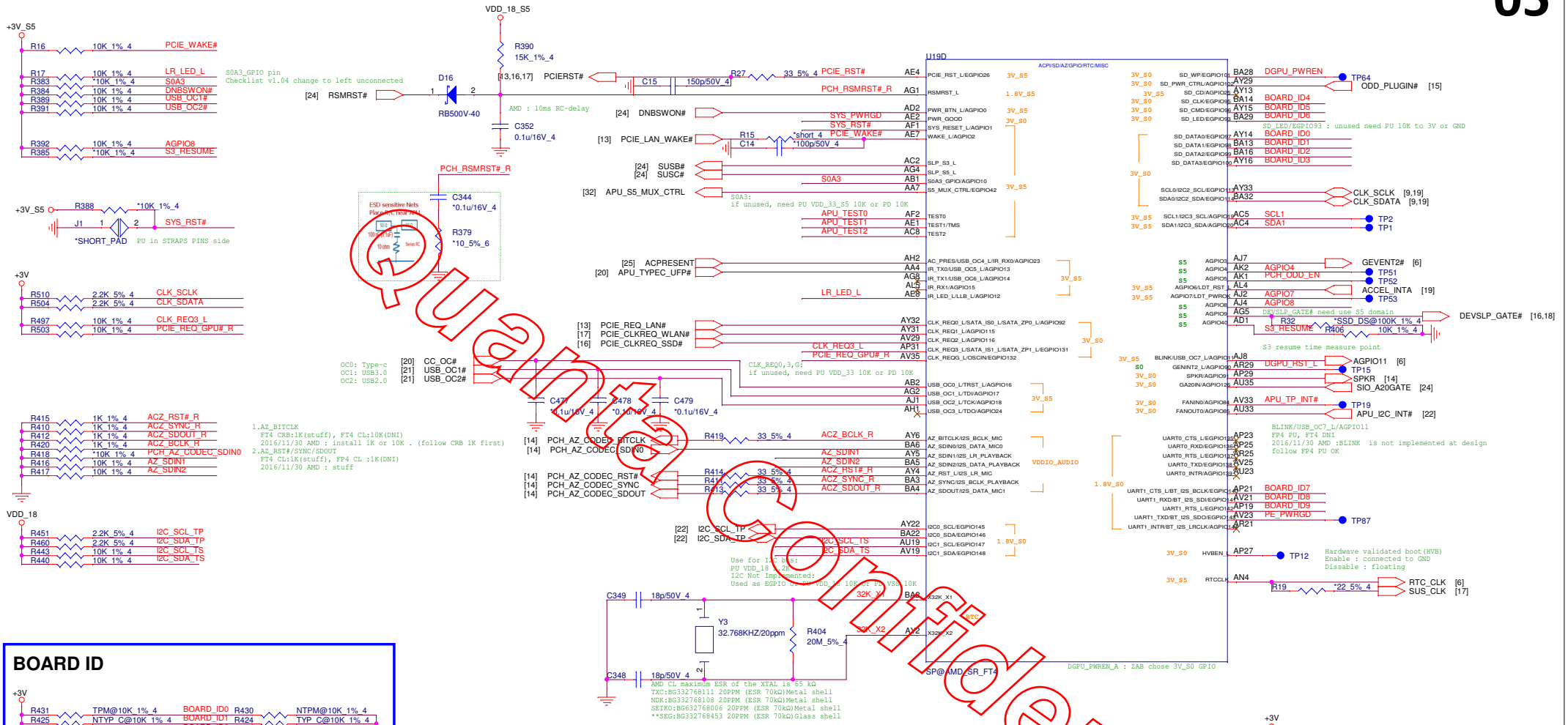
SMBUS(Internal Thermal sensor)

HDT(Hardware Debug Tool) Connector

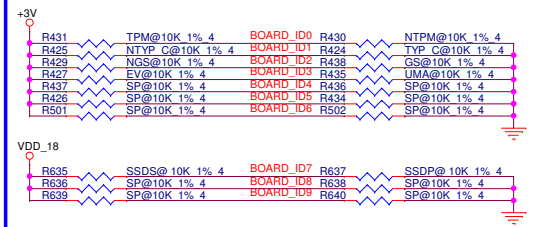


Quanta Computer Inc.
PROJECT : ZAS

Size	Document Number	Rev
	FT4 DISPLAY/MISC(3/7)	1A
Date: Friday, March 24, 2017	Sheet 4 of 35	



BOARD ID

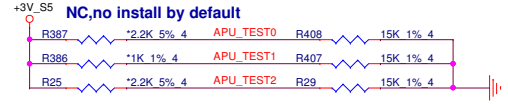


GPIO	High	Low
BOARD_ID0	dTPM	iTPM
BOARD_ID1	non-Type C	Type C
BOARD_ID2	non-G sensor	G sensor
BOARD_ID3	GPU	UMA
BOARD_ID4	Memory ID	Memory ID
BOARD_ID5	Memory ID	Memory ID
BOARD_ID6	Memory ID	Memory ID
BOARD_ID7	SATA SSD	PCIE SSD
BOARD_ID8	Reserve	Reserve
BOARD_ID9	Reserve	Reserve

Reserve:Default PD

Reserve:Default PD

Test mode setting (Follow AMD's suggestion)



TEST2	TEST1	TEST0	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	**Reserved**
0	1	X	**Reserved**
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	**Use on ATE only Yuba JTAG enabled**

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PROJECT : ZAS

Size	Document Number	Rev
	FT4 GPIO/AZ/I2C/UARTS/ACPI(4/7)	1A

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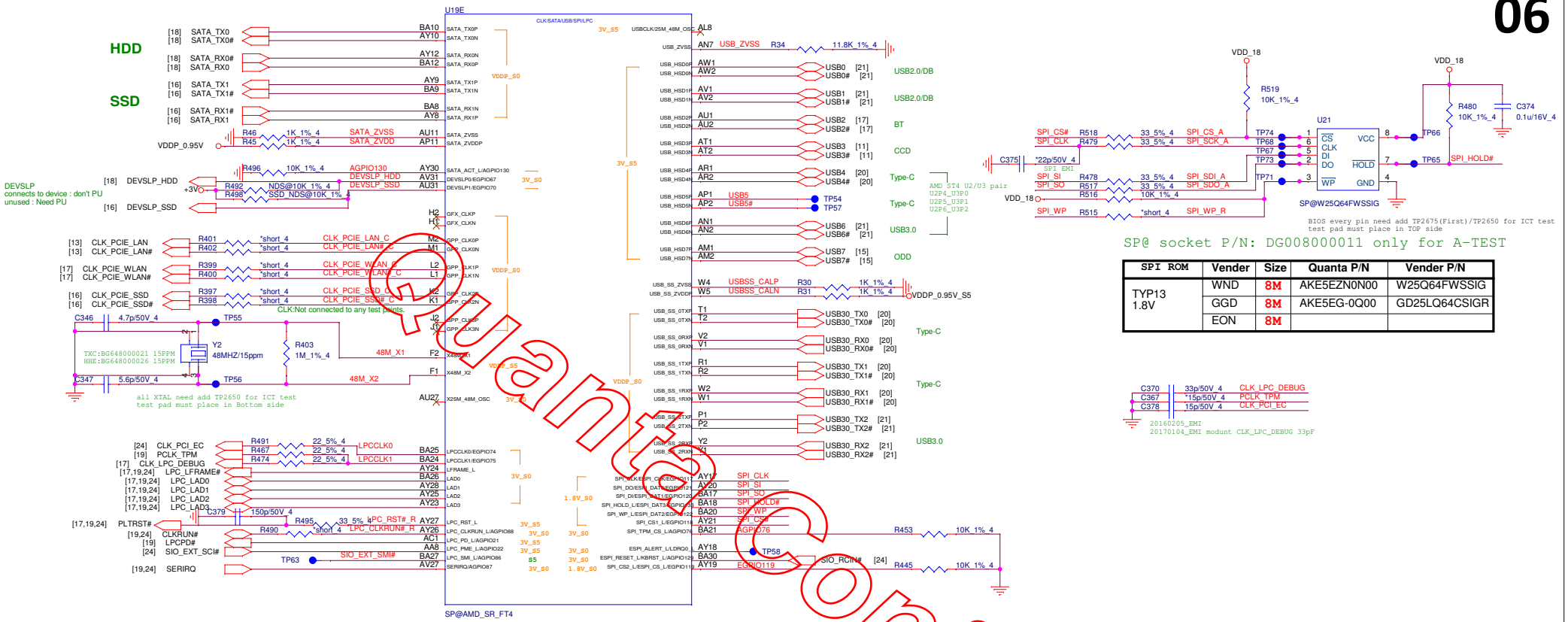
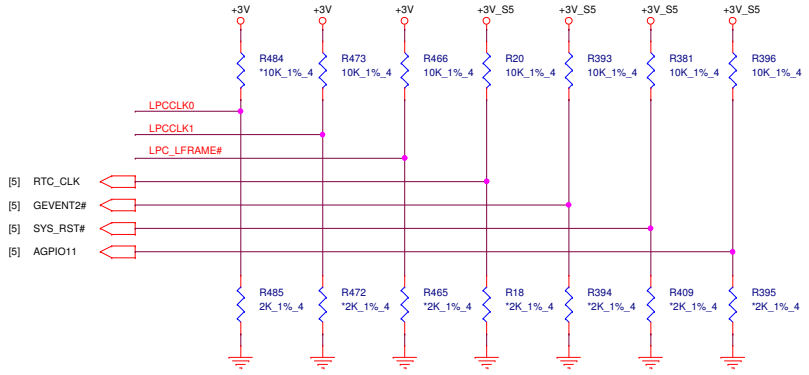


SPI ROM	Vender	Size	Quanta P/N	Vender P/N
TYP13 1.8V	WND	8M	AKE5EZN0N00	W25Q64FWSSIG
	GGD	8M	AKE5EG-0Q00	GD25LQ64CSIGR
	EON	8M		

STRAPS PINS



	LPC_CLK0	LPC_CLK1	LFRAME#	RTC_CLK	GEVENT2# (AGPIO3)		SYS_RST#	AGPIO11(BLINK)
					CZ-L	TYP13		
PU	BOOT Fail Timer ENABLE	Use 48Mhz crystal clock and generate both internal and external clocks DEFAULT	SPI ROM DEFAULT	Coin battery is on board. DEFAULT	1.8V SPI ROM	Enhanced Reset logic (for quicker S5 resume) DEFAULT	normal reset mode DEFAULT	LDT_RST#/LDT_PWRGD output to APU DEFAULT
PD	BOOT Fail Timer DISABLE DEFAULT	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	LPC ROM	Coin battery isn't on board.	3.3V SPI ROM DEFAULT	Default to traditional reset logic	short reset mode	LDT_RST#/LDT_PWRGD output to Pads

BLINK/USB_OC7_L/AGPIO11
FP4 PU, FT4 DNI
2016/11/30 AMD :BLINK is not implemented at design
follow FP4 PU OK

Quanta Computer Inc.
PROJECT : ZAS
Size | Document Number: FT4 SATA/USB/LPC/SPI/eSPI(5/7) | Rev 1A
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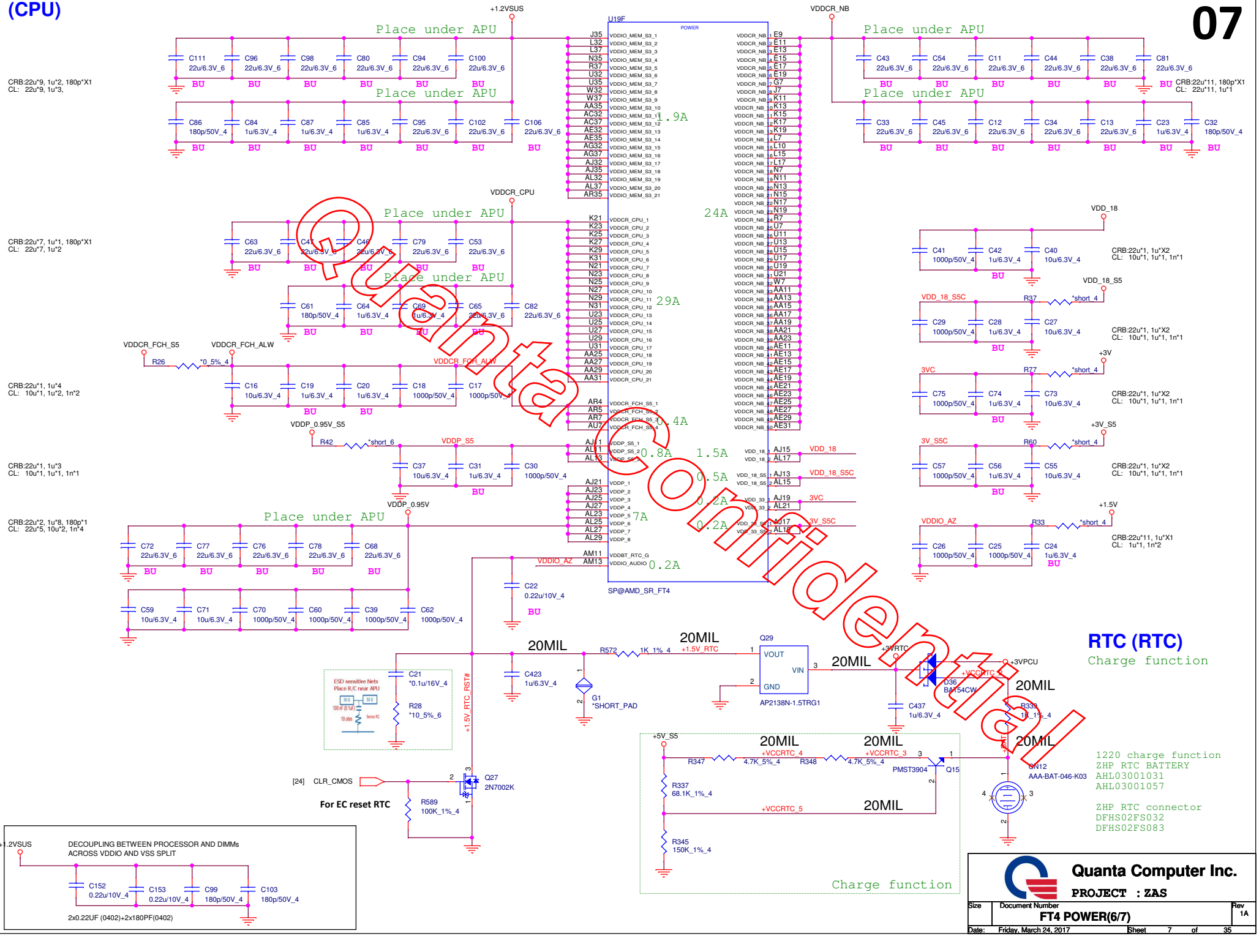
(CPU)



RTC (RTC)

Charge function

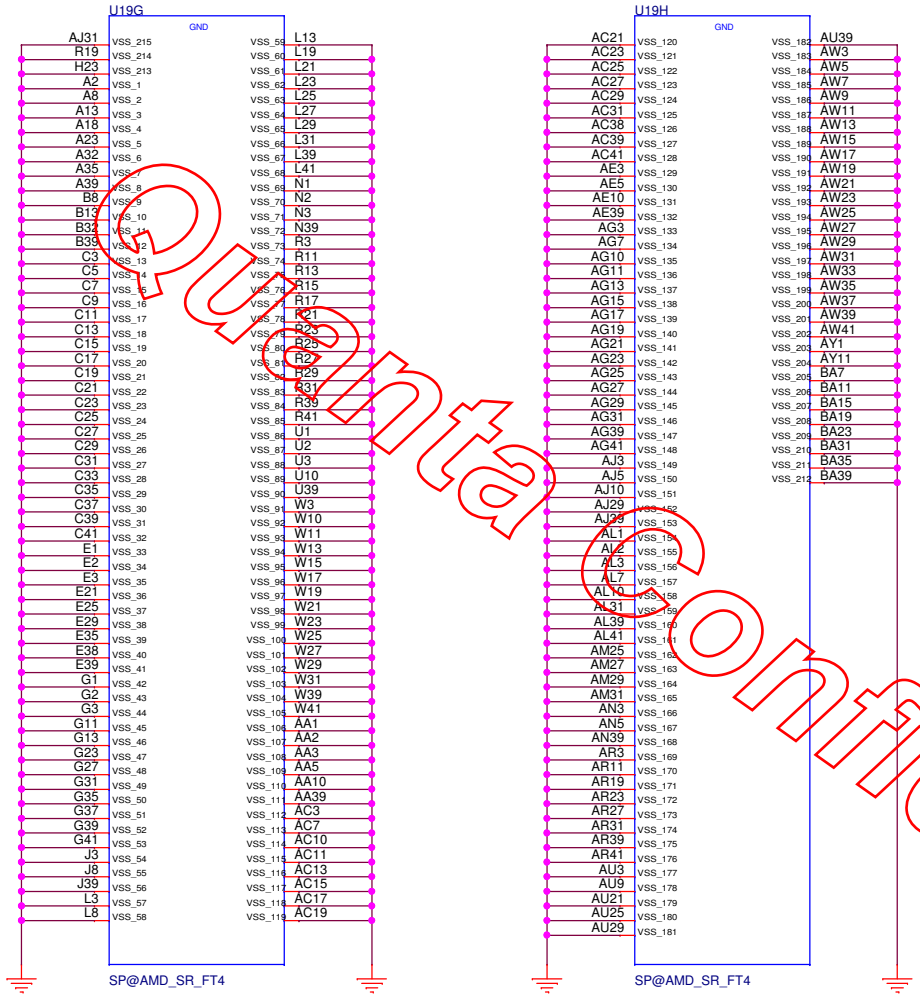
1220 charge function
ZHP RTC BATTERY
AHL03001031
AHL03001057

ZHP RTC connector
DFHS02FS032
DFHS02FS083

Quanta Computer Inc.

PROJECT : ZAS

Size	Document Number	Rev
	FT4 POWER(6/7)	1A
Date: Friday, March 24, 2017	Sheet 7 of 35	



Quanta Computer Inc.

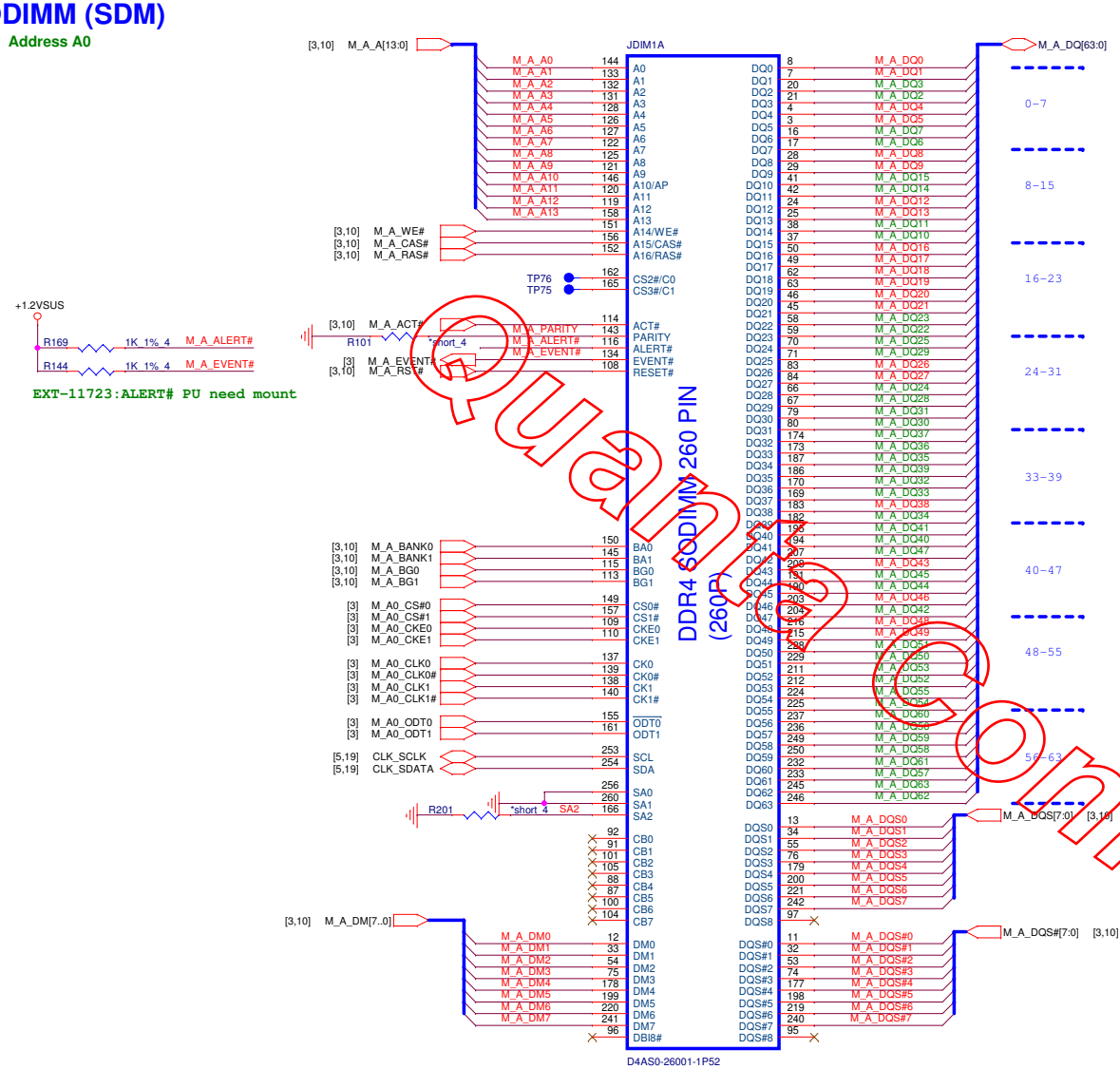
PROJECT : ZAS

Size	Document Number	Rev
	FT4 GND(7/7)	1A
Date: Friday, March 24, 2017	Sheet 8 of 35	

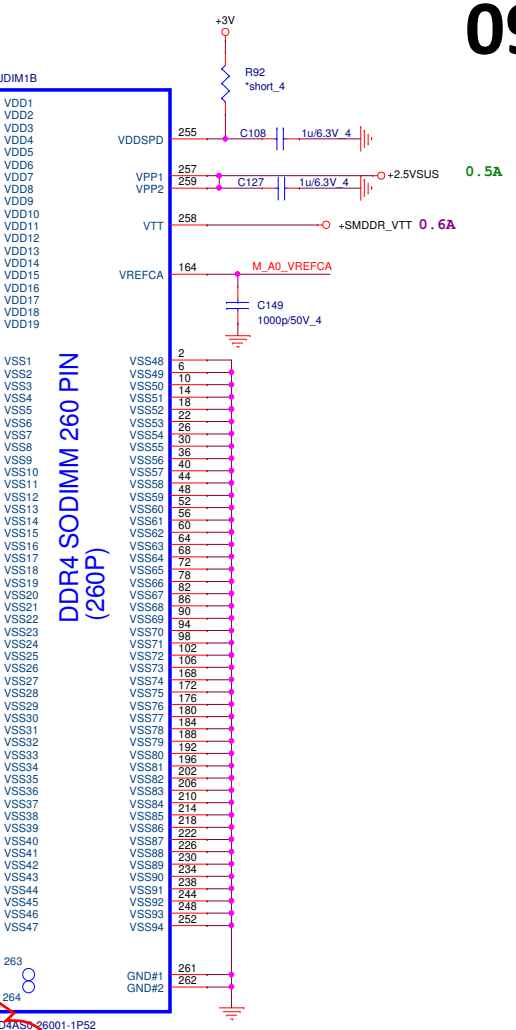
SODIMM (SDM)

09

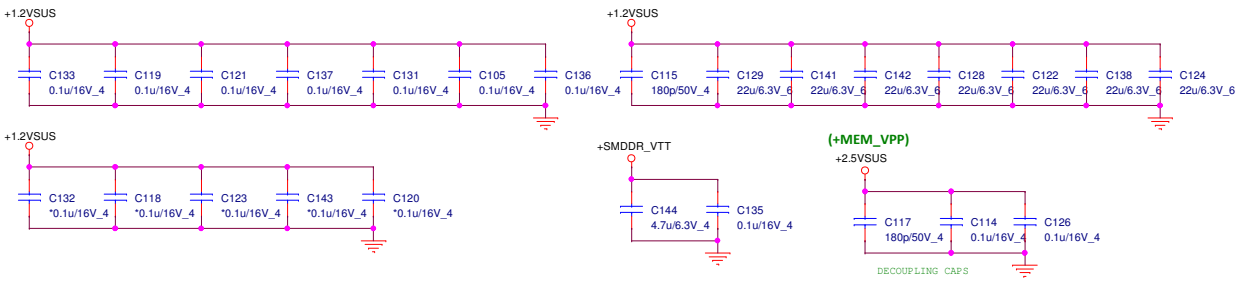
Address A0

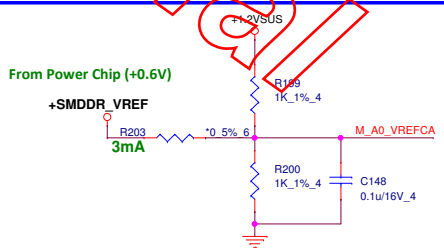


EXT-11723:ALERT# PU need mount



Place these Caps near So-Dimm A





Quanta Computer Inc.		
PROJECT : ZAS		
Size	Document Number: DDR4 DIMM CHA0 (STD)	Rev: 1A
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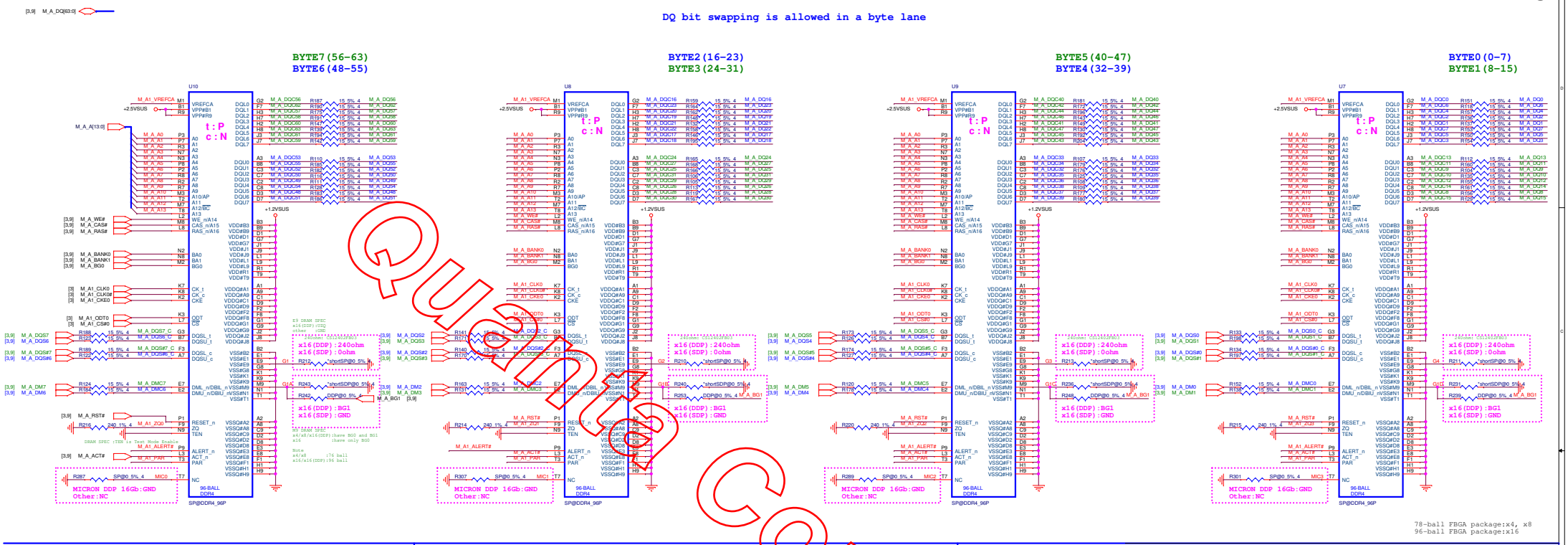
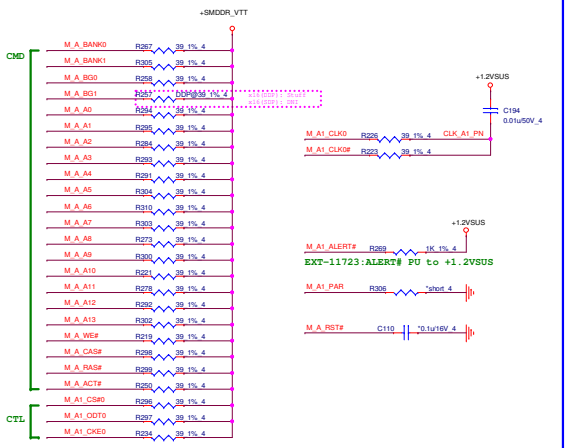
On board memory(OBM)

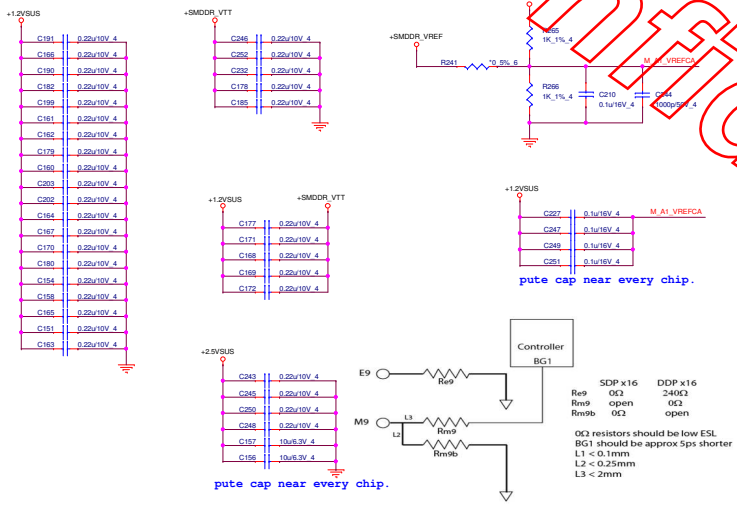
Address A2

15ohm Series resistor to DRAM Placed between DIMM and DRAM at a distance of <10mm from the DIMM.

DQ bit swapping is allowed in a byte lane





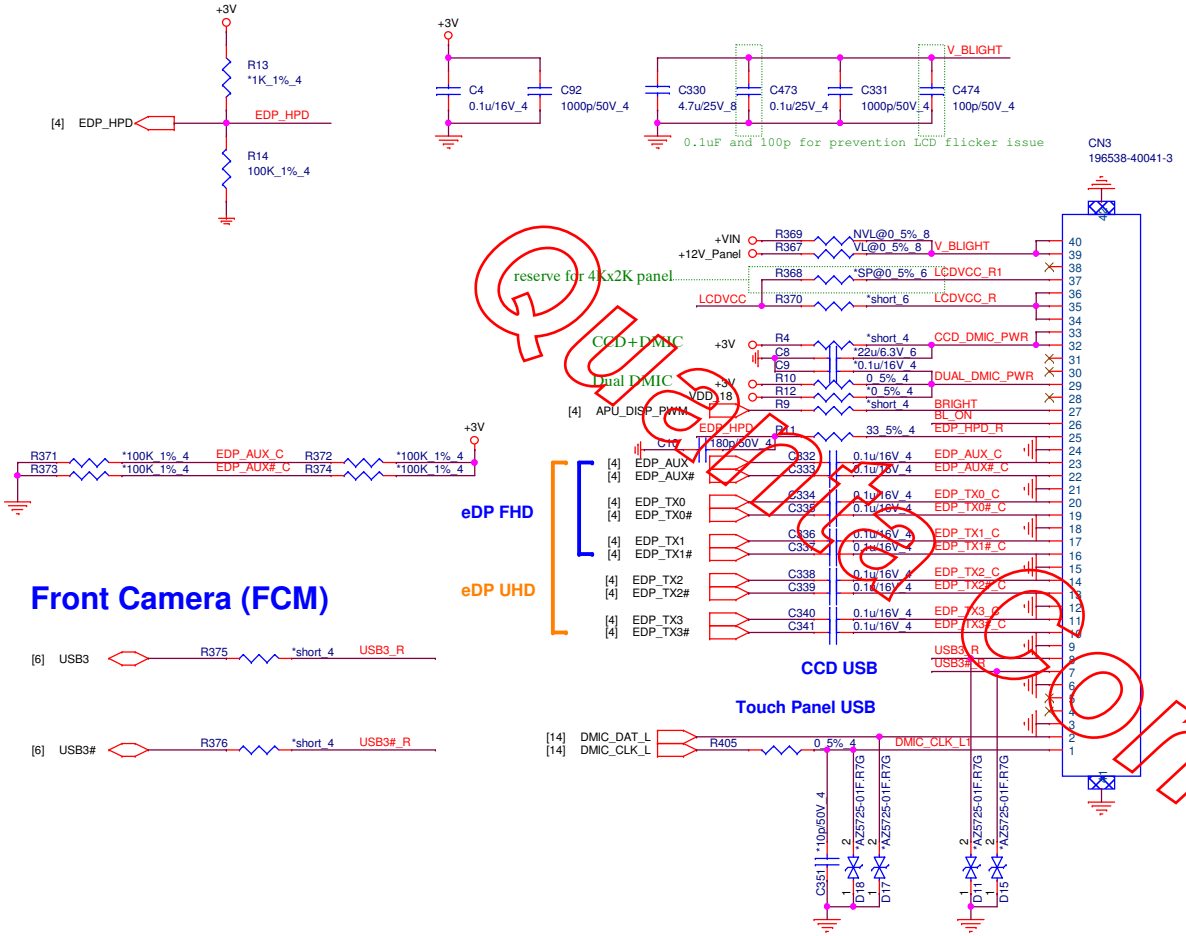


Memory ID

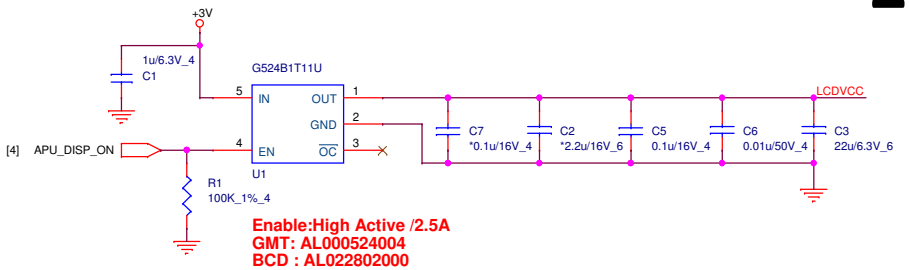
Vendor	Vendor P/N	STN B/S P/N	Size	Board 6	Board 5	Board 4
Hynix	H5AN8G6NAFR-UHC DDRIV 2400 8Gb x16(SDP)	AKD5QGSTW05 * 4	4GB	0	0	0
Samsung	K4A8G165WB-BCRC DDRIV 2400 8Gb x16(SDP)	AKD5QZ0T504 * 4	4GB	0	0	1
MICRON	MT40A512M16JY-083E DDRIV 2400 8Gb x16(SDP)	AKD5QGSTL18 * 4	4GB	0	1	0
				0	1	1
				1	0	0
				1	0	1
				1	1	0
Samsung	K4A8G165WB-BCPB DDRIV 2133 8Gb x16(SDP)	AKD5QG0T506 * 4	4GB	1	1	1

Quanta Computer Inc.
PROJECT : ZAS
Size: A3 | Document Number: DDR4 MEMORY DOWNx16 CHA1 | Rev
Date: Friday, March 24, 2017 | Sheet 10 of 35

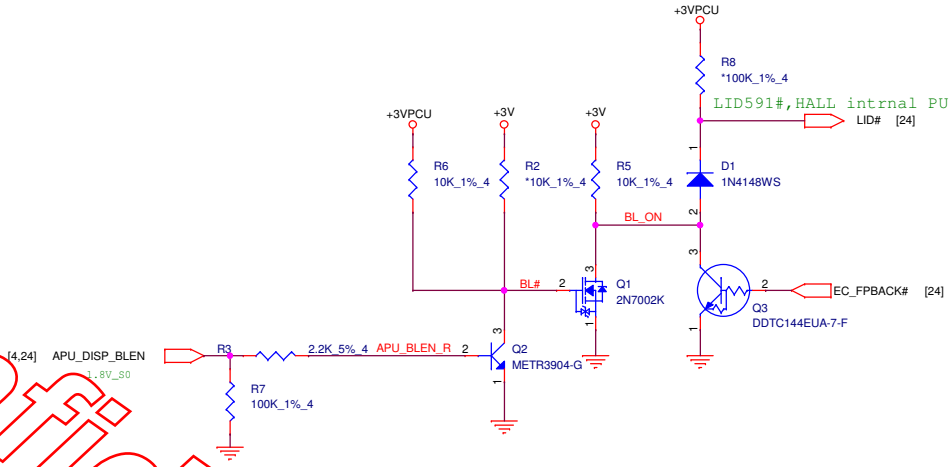
LCD (LDS)



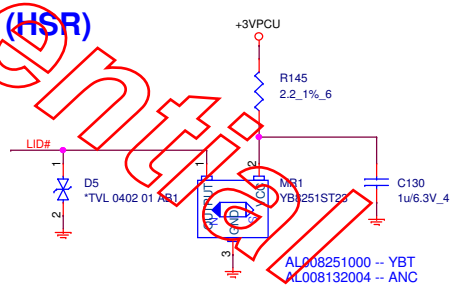
LCD Power (LDS)



Backlight Control (LDS)



Lid Switch (HSR)



Quanta Computer Inc.
PROJECT : ZAS

Size	Document Number	Rev
	eDP/Hall/CCD	1A
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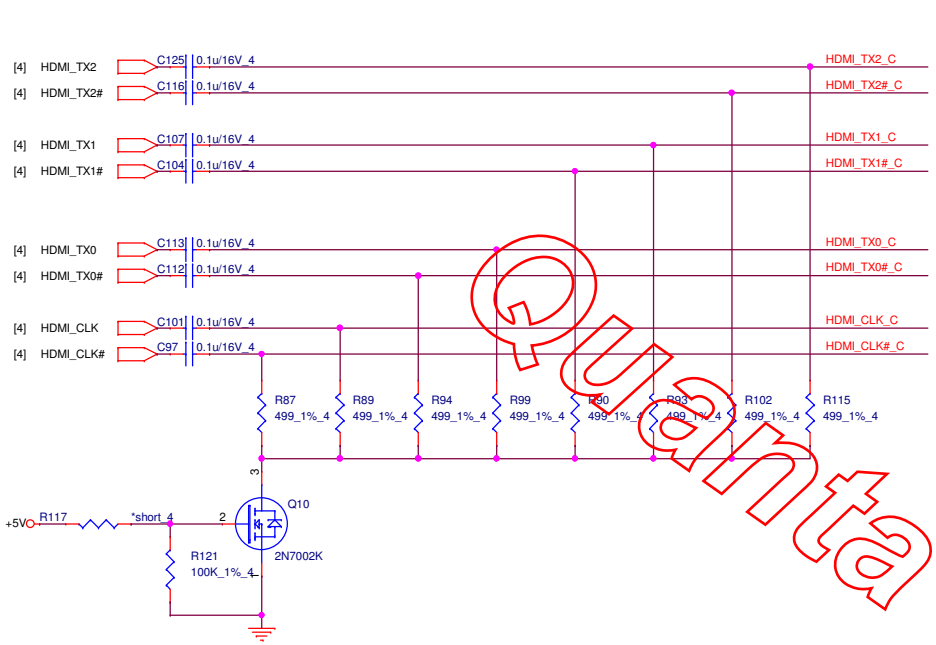
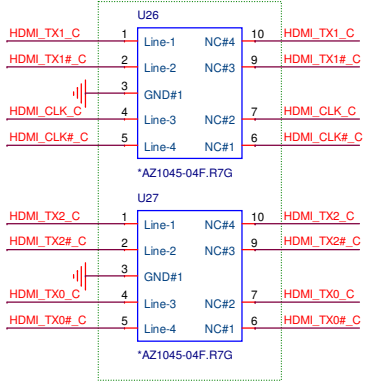
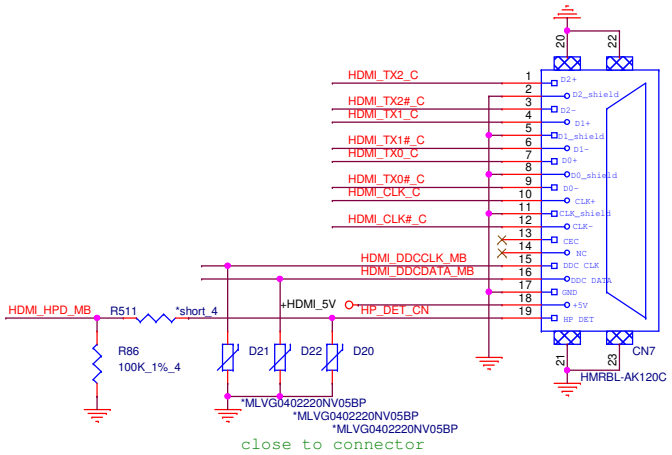
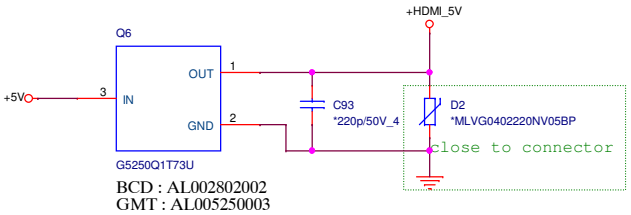
HDMI(HDM)



close to connector

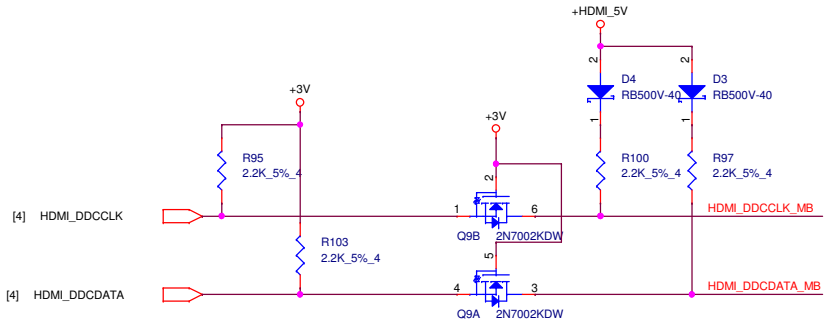




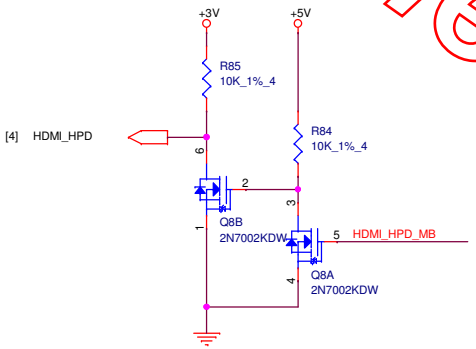


BCD : AL002802002
GMT : AL005250003

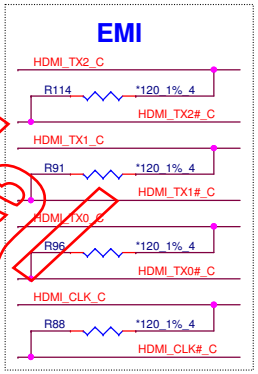
HDMI DDC (HDM)



HDMI-detect (HDM)



EMI



Quanta Computer Inc.
PROJECT : ZAS

Size	Document Number	Rev
	HDMI	1A
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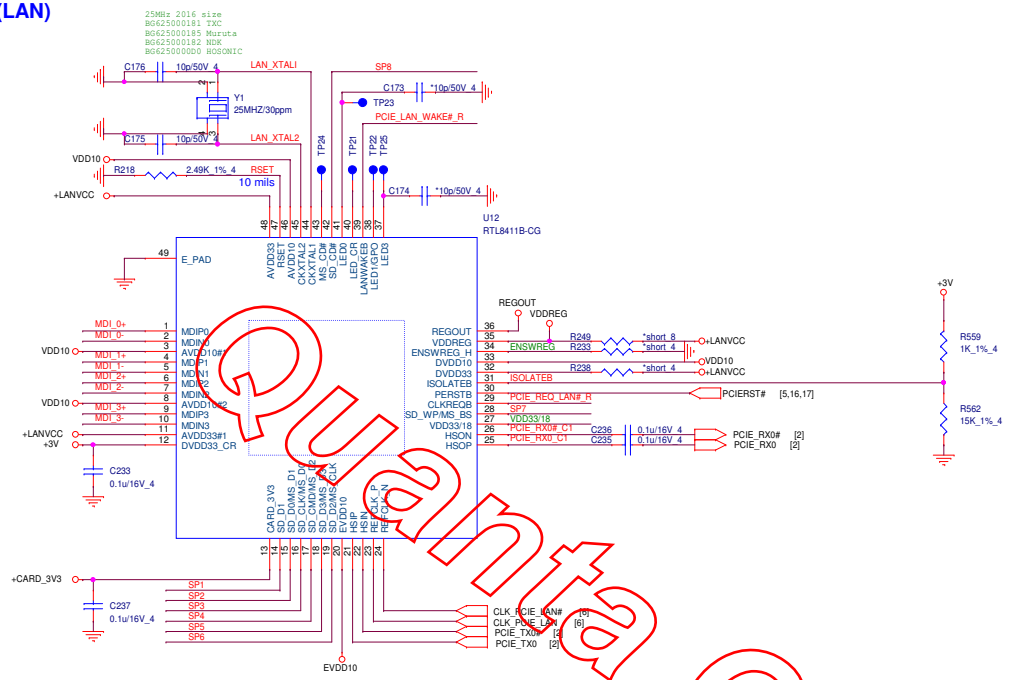
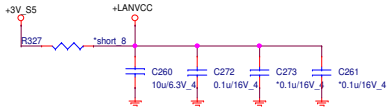
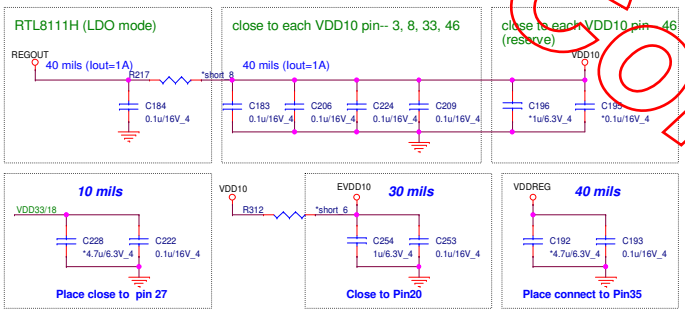
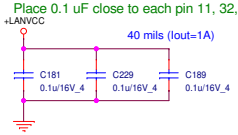
LAN & Card reader Combo (LAN)





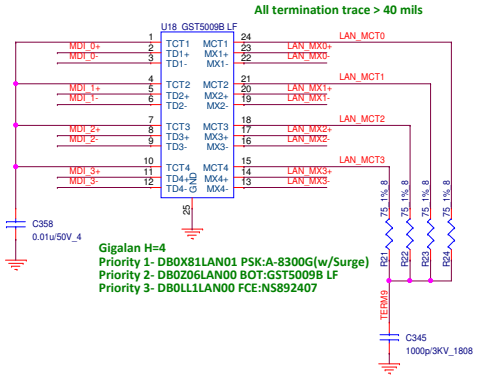


For RTL8111H
Place 0.1 uF close to each pin 11, 32,48



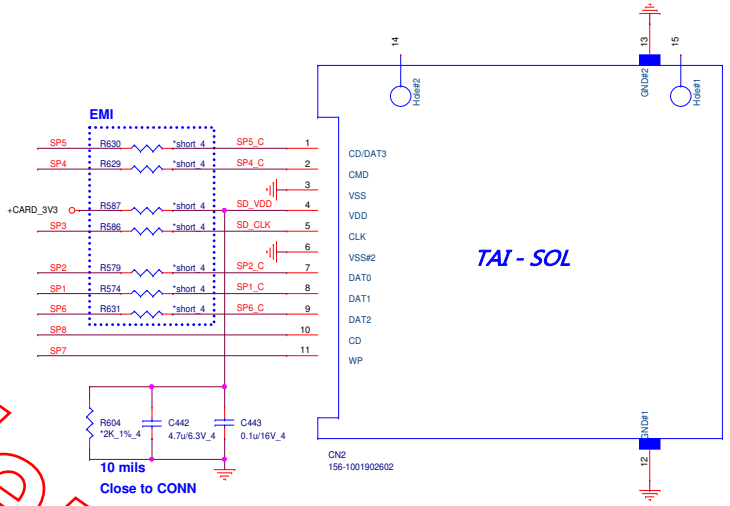
Tramsformer

All termination trace > 40 mils

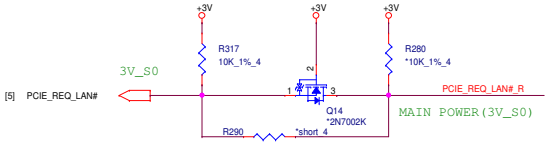


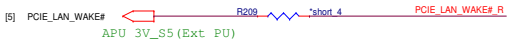
Gigalan H=4
Priority 1- DB0X81LAN01 PSK:A-8300G(w/Surge)
Priority 2- DB0Z06LAN00 BOT:GST5009B LF
Priority 3- DB0LL1LAN00 FCE:NS892407

Crad Reader Connector

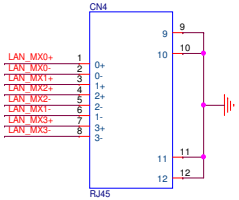


Leakage circuit

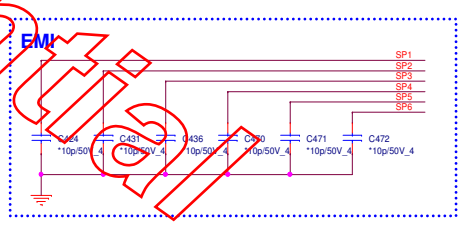




RJ45 Connector



EMI



Share Pin

SP1	SD_D1	
SP2	SD_D0	MS_D1
SP3	SD_CLK	MS_D0
SP4	SD_CMD	MS_D2
SP5	SD_D3	MS_D3
SP6	SD_D2	MS_CLK
SP7	SD_WP	MS_BS
SP8	SD_CD#	
SP9		MS_INS#

Quanta Computer Inc.
PROJECT : ZAS

Size	Document Number	Rev
	LAN-CR COMBO(RTL8411B)	1A
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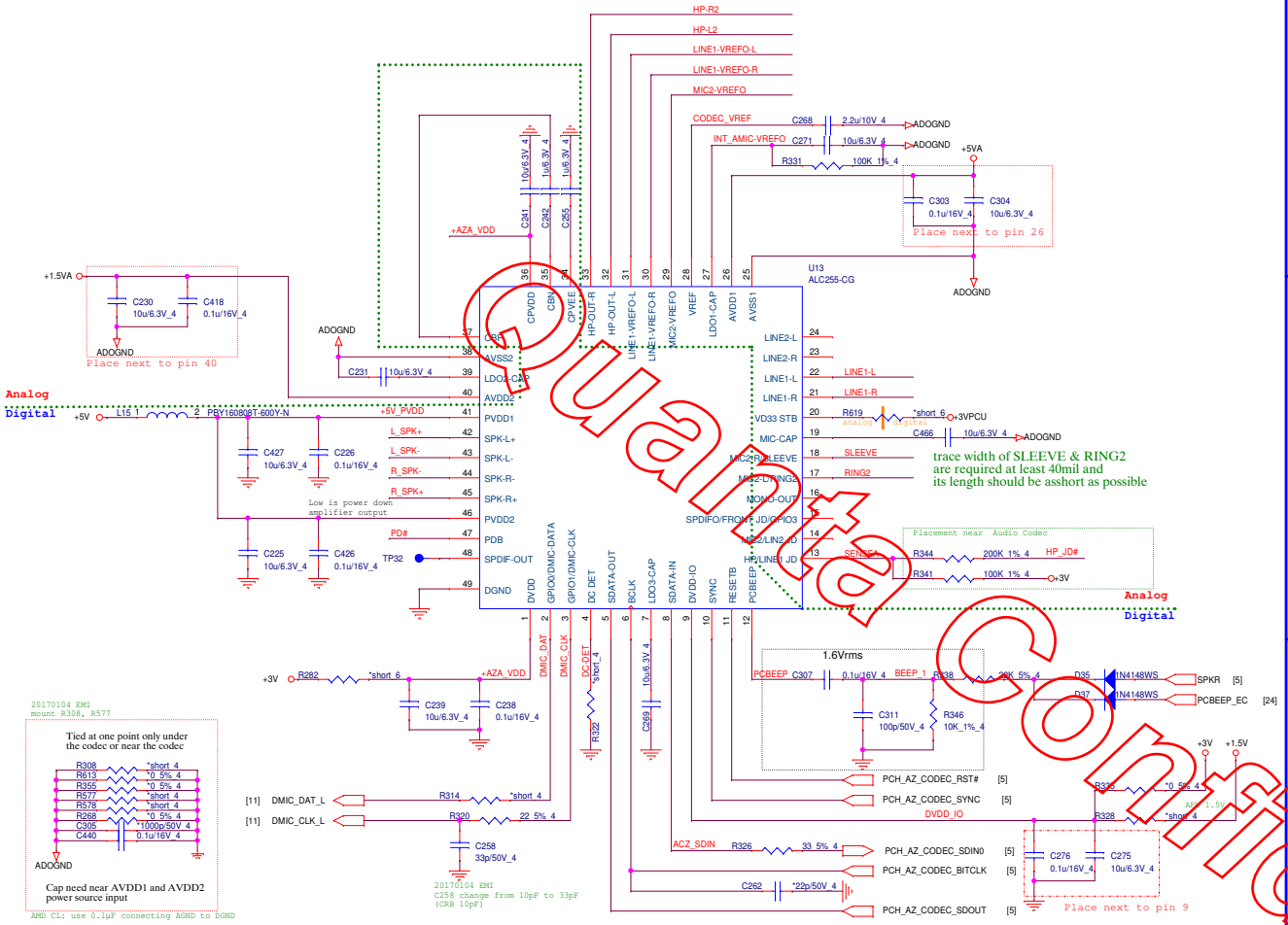
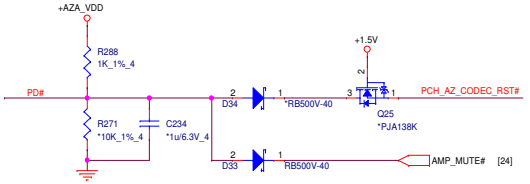
Codec(ADO)

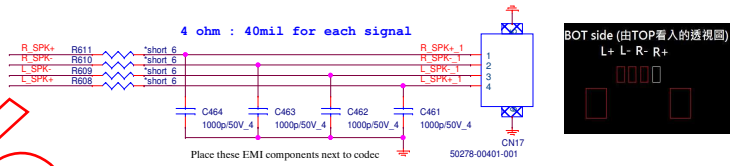


DC-DET circuit(ADO)

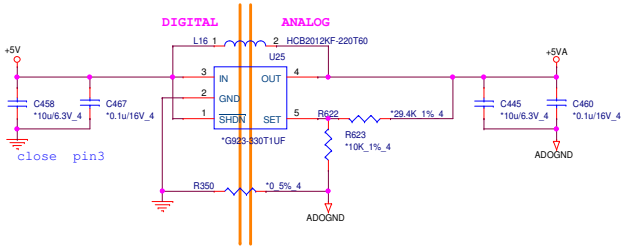
Mute(ADO)



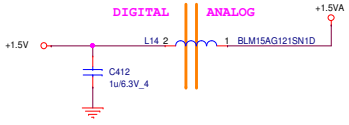
Internal Speaker(ADO)



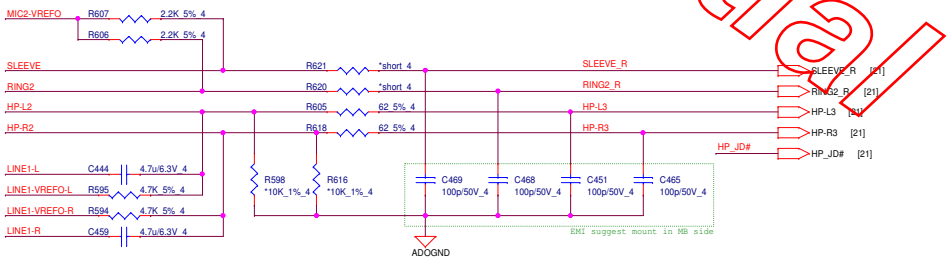
Codec PWR 5V(ADO)



Codec PWR 1.5V(ADO)



HEADPHONE/MIC/LINE combo (ADO)



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U2 to SATA (ODD)

GPIO7 (CLK_SEL1)	GPIO3 (CLK_SEL0)	
0	0	25MHz

GPIO6	SPI_EN#
0	Enable
1	Disable

Close to ASM1153

+1.2V_48: C421 ODD@0.1u/16V_4, C419 ODD@0.1u/16V_4, C409 ODD@0.1u/16V_4, C395 ODD@0.1u/16V_4, C400 ODD@0.1u/16V_4, C411 ODD@0.1u/16V_4

+3.3V_48: C392 ODD@0.1u/16V_4, C394 ODD@0.1u/16V_4, C420 ODD@0.1u/16V_4, C422 ODD@0.1u/16V_4, C406 ODD@0.1u/16V_4

Internal 1.2V voltage (Switching)
Close to ASM1153

+1.2V_48 > 40mIL → L13 ODD@4.7uH/1A_2X2 (use 1A choke, can't use beed) → PGND_48, VCC12O_48

C401 ODD@10u/6.3V_4

+3.3V_48 → R538 *shortODD@0_5%_4 → +1.2V_48

+3.3V_48 → R548 ODD@100K_1%_4 → RST_48 → C413 ODD@1u/6.3V_4

TP77, TP78

U23 ODD@ASM1153

Pin	Name
49	EPAD
48	LXI
47	PGND
46	VDD#3
45	HDDPC
44	GPIO1
43	GPIO0
42	TEST_EN
41	UART_TX
40	UART_RX
39	VCC#2
38	RST#
37	GPIO6
1	VCCIN
2	I2C_DATA
3	I2C_CLK
4	VCC#1
5	GPIO5
6	GPIO4
7	GPIO4
8	GPIO3
9	GPIO3
10	GPIO2
11	VBUS
12	VBUS_LDO
13	VCCO
14	VDDU#1
15	VCCU#1
16	UDP
17	UDM
18	REXT
19	VCCU#2
20	UTXN
21	UTXP
22	GNDA#1
23	URXN
24	URXP
25	VDDU#2
26	XO
27	XI
28	VCCTXL
29	VDDS
30	SRXP
31	SRXN
32	GNDA#2
33	STXN
34	STXP
35	VCCS
36	GPIO7
37	VDD#2

GPIO3_48 R530 ODD@4.7K_5%_4
GPIO7_48 R571 ODD@4.7K_5%_4
GPIO6_48 R561 ODD@4.7K_5%_4
UREXT_48 R541 ODD@12.1K_1%_4

This Cap
Power side closer to Pin 1
GND side closer to Pin47

PGND_48 C393 ODD@4.7u/6.3V_4

I2C_DATA_48, I2C_CLK_48, GPIO5_48, GPIO4_48, GPIO3_48, BUS_DET_48

+5V_48 R529 ODD@4.7K_5%_4

+1.2V_48 → +3.3V_48

C396 ODD@2.2u/10V_4

C391 ODD@4.7u/6.3V_4

ASM1153
Pin11 5V in, Pin12 3V out

+5V R528 ODD@0_5%_8 +5V_48

+3.3V_48 → +1.2V_48 → C402 ODD@0.1u/16V_4

USB7, USB7# [6] [6]

+3.3V_48 → +1.2V_48

GPIO7_48, STXP_48, STXN_48, SRXN_48, SRXP_48

ASM1153
TX connect connector TX
RX connect connector RX

XO_48, XI_48

C416 ODD@8.2p/50V_4

Y4 ODD@25MHZ/30ppm

25MHz 2016 size
BG625000181 TXC
BG625000185 Muruta
BG625000182 NDK
BG6250000D0 HOSONIC

SPI ROM

AKE35ZN0N00 (1 Mb)...EC
AKE37FN0N05 (4 Mb)...ODD

U22 ODD@W25X40CLSNIG

Pin	Name
1	CE#
2	SO
3	WP#
4	VSS
5	SI
6	SCK
7	HOLD#
8	VDD

GPIO4_48, I2C_DATA_48, +3.3V_48, I2C_CLK_48, GPIO5_48

+3.3V_48

ASM1153
Pin2 connect connector SO
Pin5 connect connector SI

C387 ODD@0.1u/16V_4

SATA ODD (ODD)

Cable type

ODD@132F18-100000-A2-R
CN15

Pin	Name
18	GND1
GND2	
EJ	
5V1	
5V2	
5V3	
5V4	
5V5	
5V6	
5V7	
DP	
GND3	
RXP	
RXN	
GND4	
TXN	
TXP	
1GND5	

R576 ODD@10K_1%_4 +3V → EC_ODD_EJ# [24]

+5V_ODD_R

1.5A 60mil

R569 *shortODD@0_5%_8 +5V_ODD

C429 ODD@0.01u/50V_4, C434 ODD@0.01u/50V_4, C433 *ODD@0.1u/16V_4, C430 *ODD@0.1u/16V_4, C425 ODD@10u/6.3V_4, C439 *ODD@100u/6.3V_12

C223 ODD@180p/50V_4

SATA_DP R263 ODD@33_5%_4 R255 ODD@10K_1%_4 +3V → ODD_PLUGIN# [5]

SRXP_48_C C452 ODD@0.01u/50V_4 SRXP_48
SRXN_48_C C453 ODD@0.01u/50V_4 SRXN_48

STXN_48_C C454 ODD@0.01u/50V_4 STXN_48
STXP_48_C C455 ODD@0.01u/50V_4 STXP_48

ODD POWER Control (reserve)

+5V 1.5A 60mil +5V_ODD

+15V to VIN → VIN → +3VPCU

R581 *shortODD@0_5%_8

Q30 *ODD@AO6402A

R281 *ODD@22_5%_8

R321 *ODD@100K_1%_4 R315 ODD@100K_1%_4

ODD_EN_Q MOD_EN_5V

+3.3V_48 → R547 *ODD@100K_1%_4

HDDPC_48 R542 *ODD@4.7K_5%_4 C408 *ODD@10u/6.3V_4

ODD_EN

Q13A *ODD@2N7002KDW Q13B *ODD@2N7002KDW

C259 *ODD@0.1u/16V_4

ODD_EN_Q Q26 *ODD@2N7002K

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	ASM1153/ODD	1A
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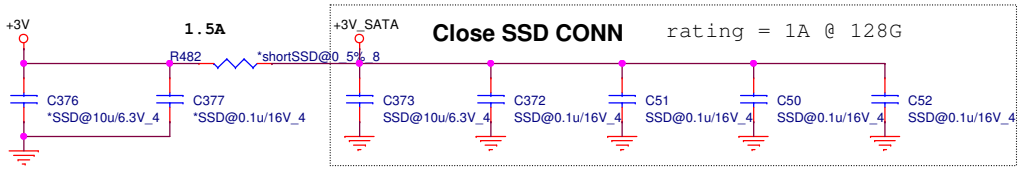
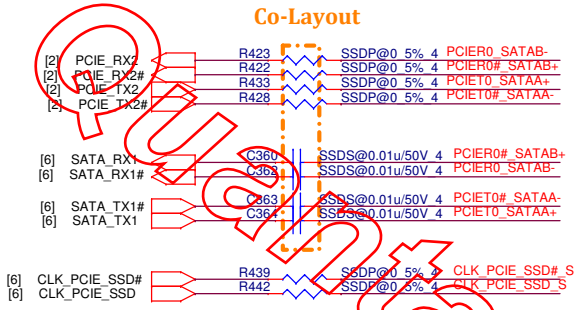
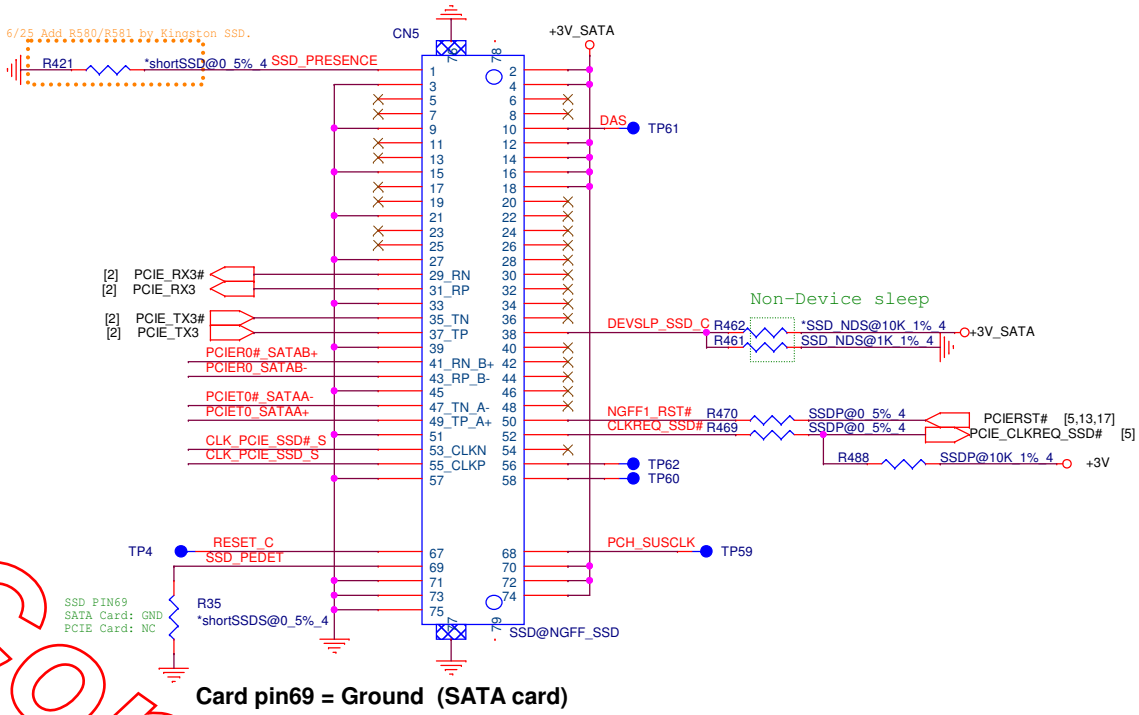
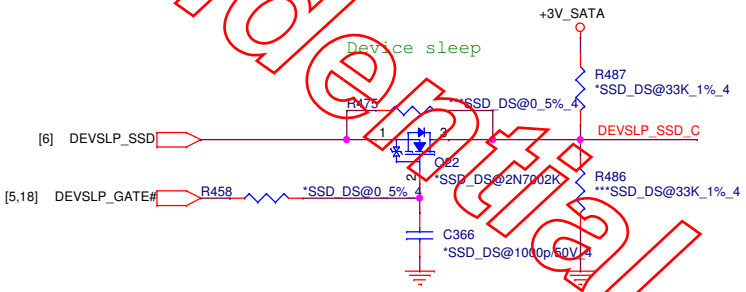
NGFF_M.2 SSD (NGF) M-KEY









pin	Type	Description
1	PRESENCE	This pin is grounded on the SSD. May be used by host to determine if slot is empty or populated
10	DAS#	Device Activity Signal
21	WWAN/SSDIND_N	This pin connect to Ground
38	Device Sleep Signal	If system didn't support DEVSLP, set DEVSLP Sleep Signal pin power high and keep (from power on), device will ignore. If system support DEVSLP, set DEVSLP Sleep Signal pin power low (from power on) device, device will support DEVSLP function. Device Sleep Signal H: SSD enter sleep model. Device Sleep Signal L: SSD exit sleep model.
53	REFCLKN	no connect on SSD
55	REFCLKP	no connect on SSD
56	MFG1	Manufacturing pin. Use determined by vendor. Must be a noconnect on the host board
58	MFG2	Manufacturing pin. Use determined by vendor. Must be a noconnect on the host board
68	SUSCLK	no connect on SSD
69	IFDET	This pin connect to Ground

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Size	Document Number	Rev
	M.2 SSD	1A
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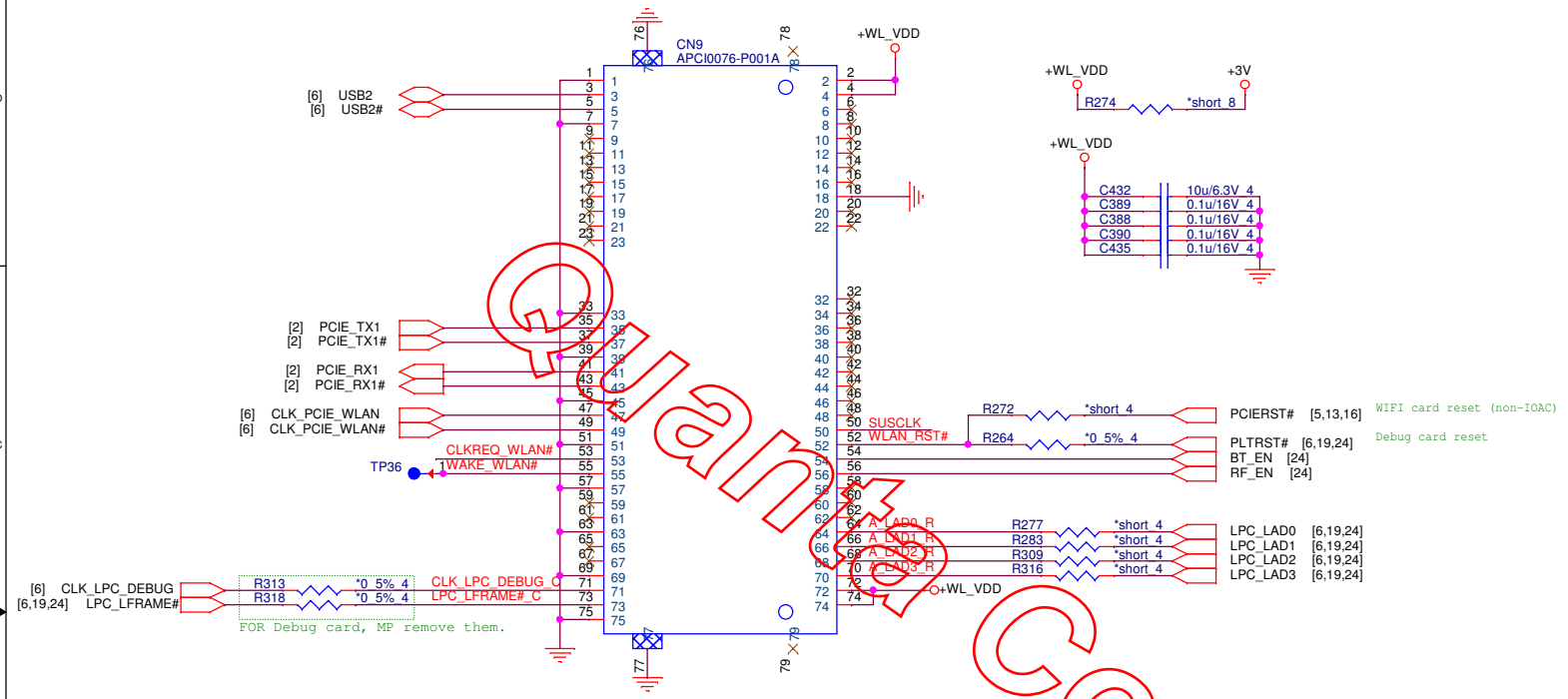
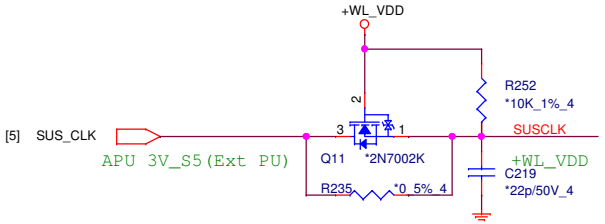
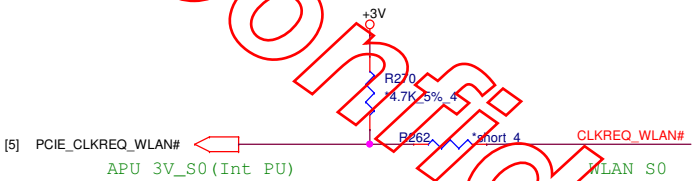
NGFF_M.2 WiFi & BT (NGF) E-KEY



Leakage circuit





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	NGFF(WiFi&BT combo)	1A
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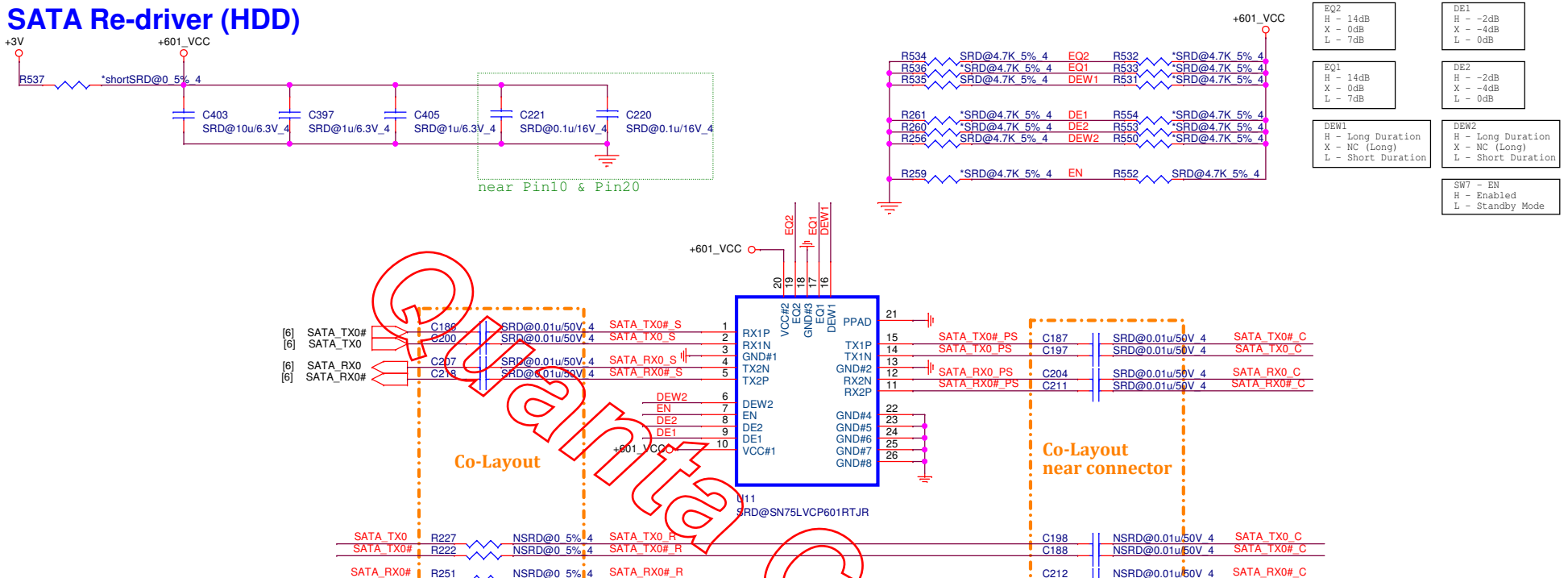
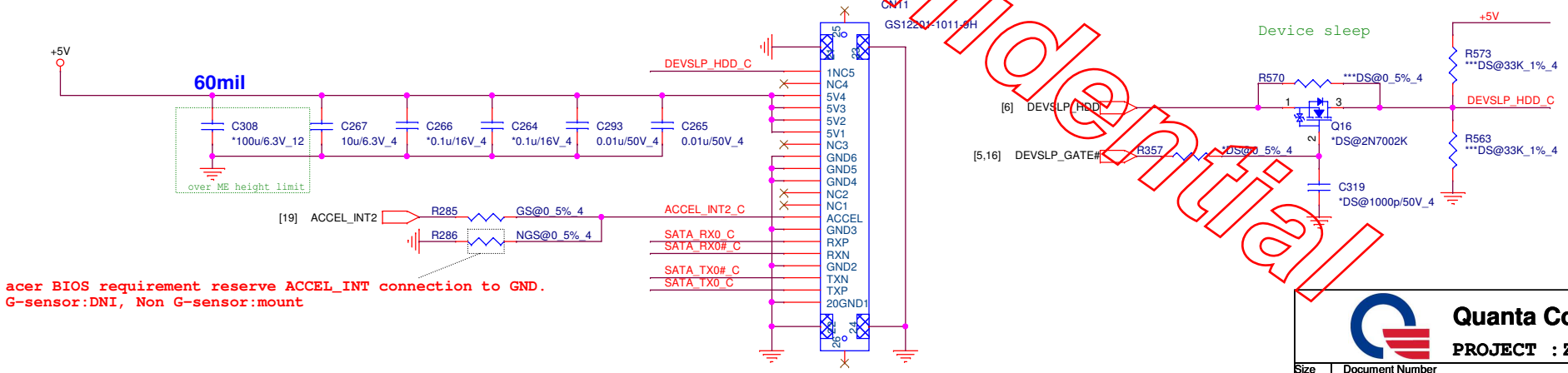
SATA Re-driver (HDD)



2.5" SATA HDD (HDD)

Cable type connector



acer BIOS requirement reserve ACCEL_INT connection to GND.
G-sensor:DNI, Non G-sensor:mount

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	HDD/REDRIVER	1A
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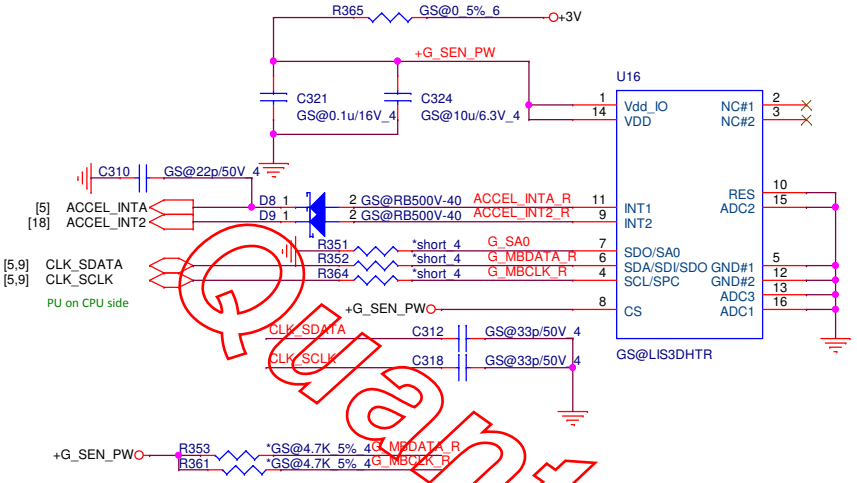
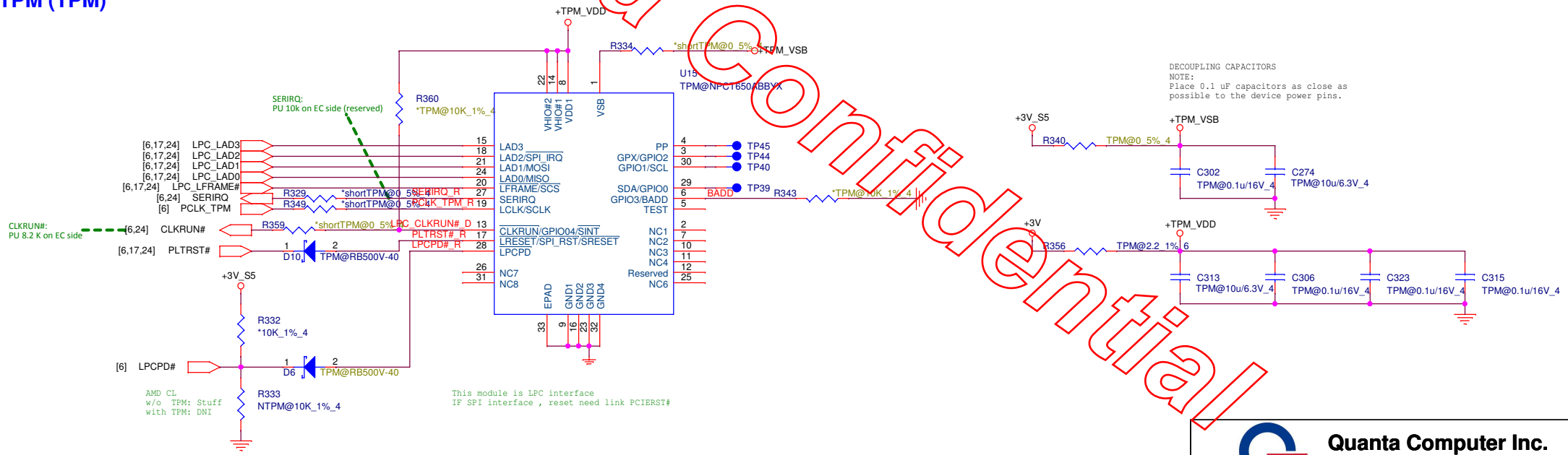
G-sensor (H3D)



TPM (TPM)



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	TPM (NPCT650)/G-sensor	1A
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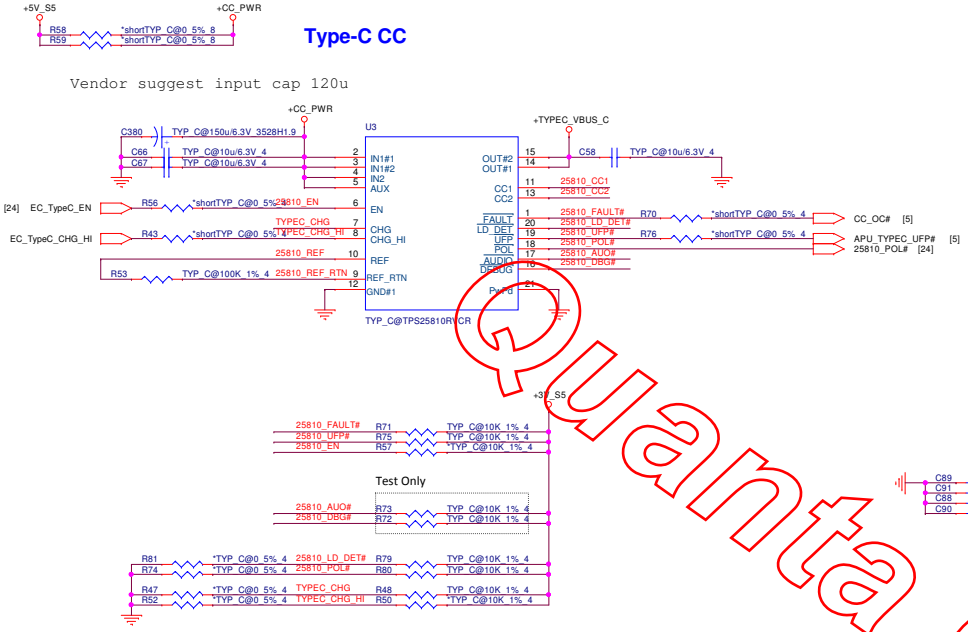
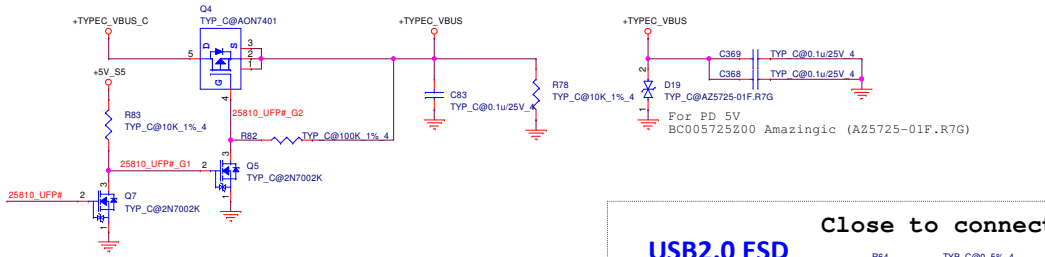
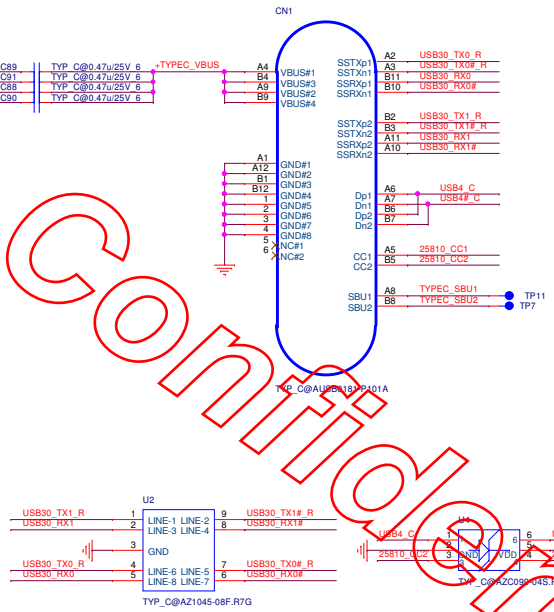
Type-C CC





CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A

TPS25810 Port	CC1	CC2	TPS25810 Response					
			OUT	VCONN On CC1 or CC2	POLb	UFPb	AUDIOb	DEBUGb
Nothing Attached	OPEN	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
UFP Connected	Rd	OPEN	IN1	NO	Hi-Z	LOW	Hi-Z	Hi-Z
UFP Connected	OPEN	Rd	IN1	NO	LOW	LOW	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	OPEN	Ra	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	Ra	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Rd	Ra	IN1	CC2	Hi-Z	LOW	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Ra	Rd	IN1	CC1	LOW	LOW	Hi-Z	Hi-Z
Debug Accessory Connected	Rd	Rd	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	LOW
Audio Adapter Accessory Connected	Ra	Ra	OPEN	NO	Hi-Z	Hi-Z	LOW	Hi-Z

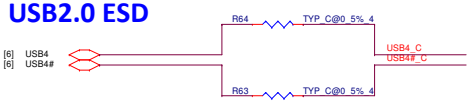


USE 5V TVS for U3
BC104508Z00 Amazingic
BC605S8QZ00 PANJIT
BC38109LZ00 INPAQ

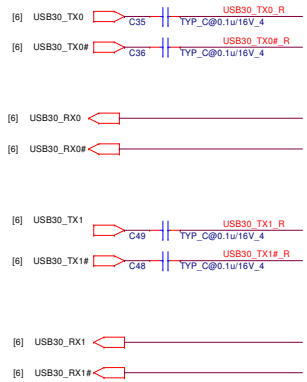
USE 4CH TVS for U2 CC
BC09904SZ00 Amazing
BCSRV05WZ01 PANJIT
BCST2304Z00 INPAQ

USB2.0 ESD

Close to connector



Type C1_HSIO_ ESD



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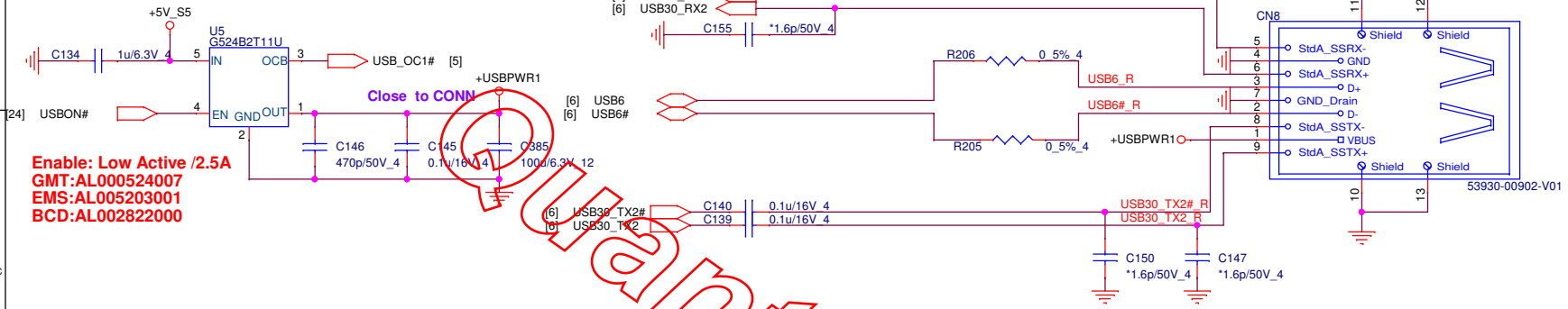
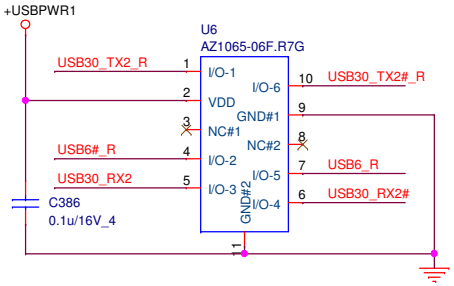
USB 3.0 Connector (UB3)

USB 3.0(5V) 6CH
BC106506000 Amazing(10KV)
BCD5326DZ00 willsemi(10KV)
BC12010LZ00 INPAQ(8KV_can't use)

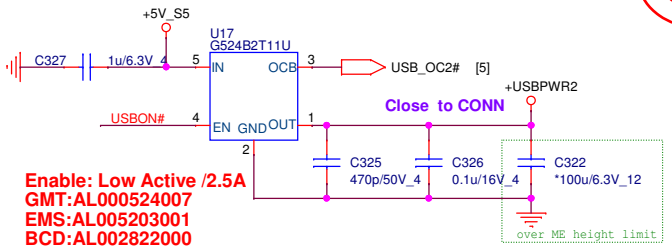
21

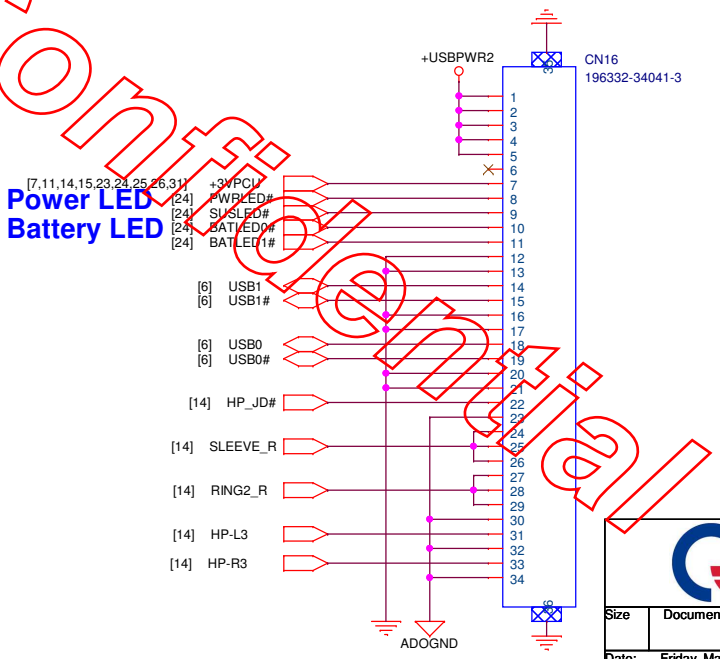




USB protection diodes for ESD.
as close as possible to USB connector pins.

DB USB2.0 (UB2)





Quanta Computer Inc.
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	USB3/USB2 DB	1A
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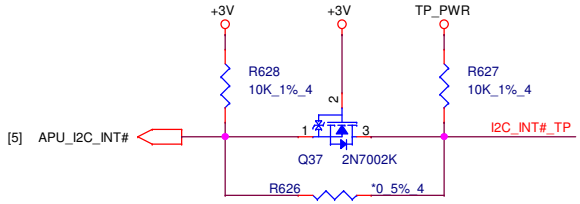
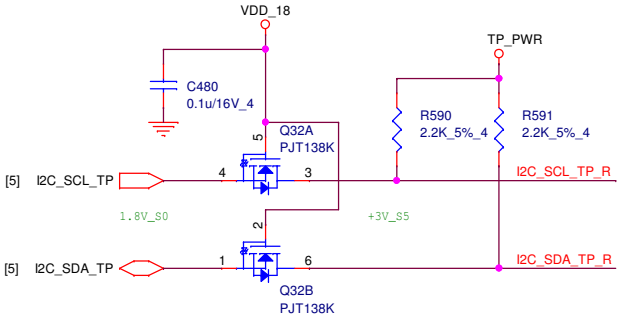
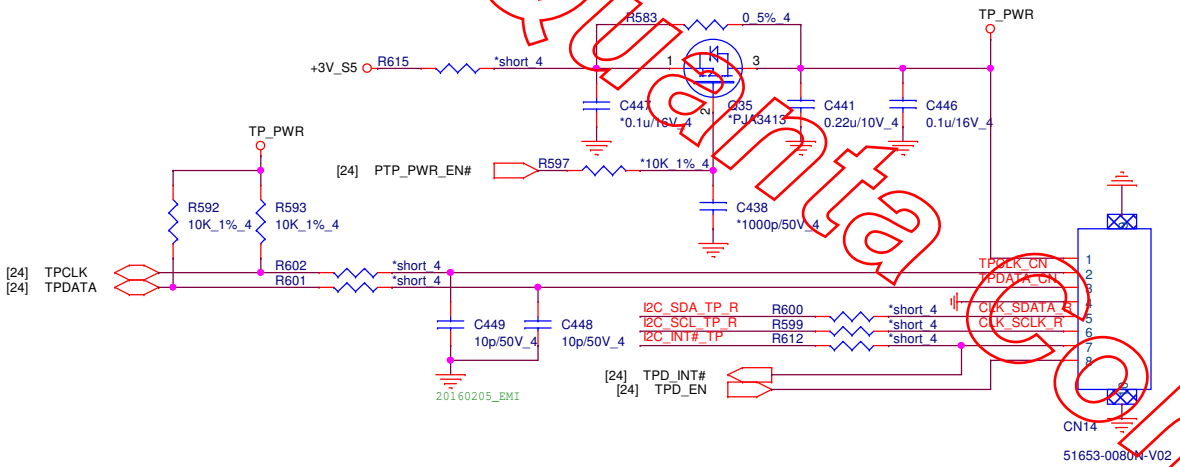
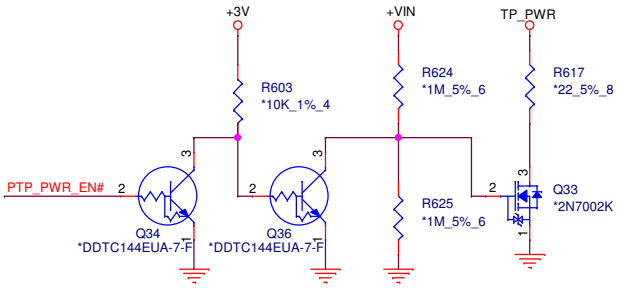
TOUCH PAD(TPD)



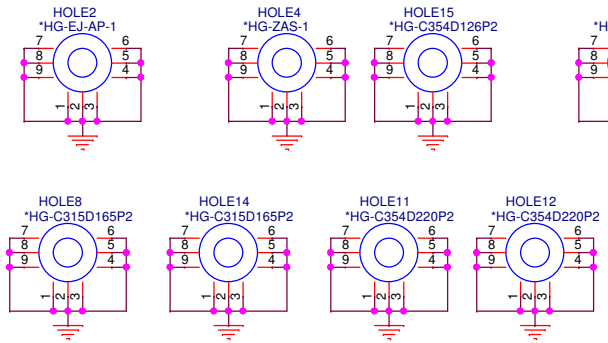


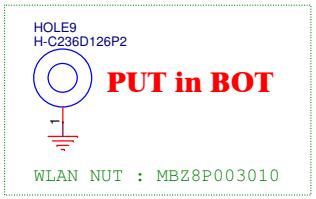


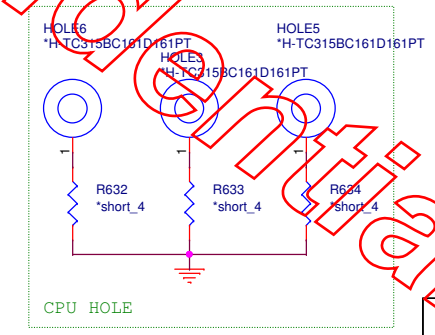
Discharge circuit

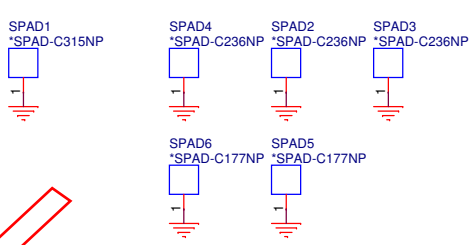


HOLE(OTH)









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	Touch Pad/HOLE	1A
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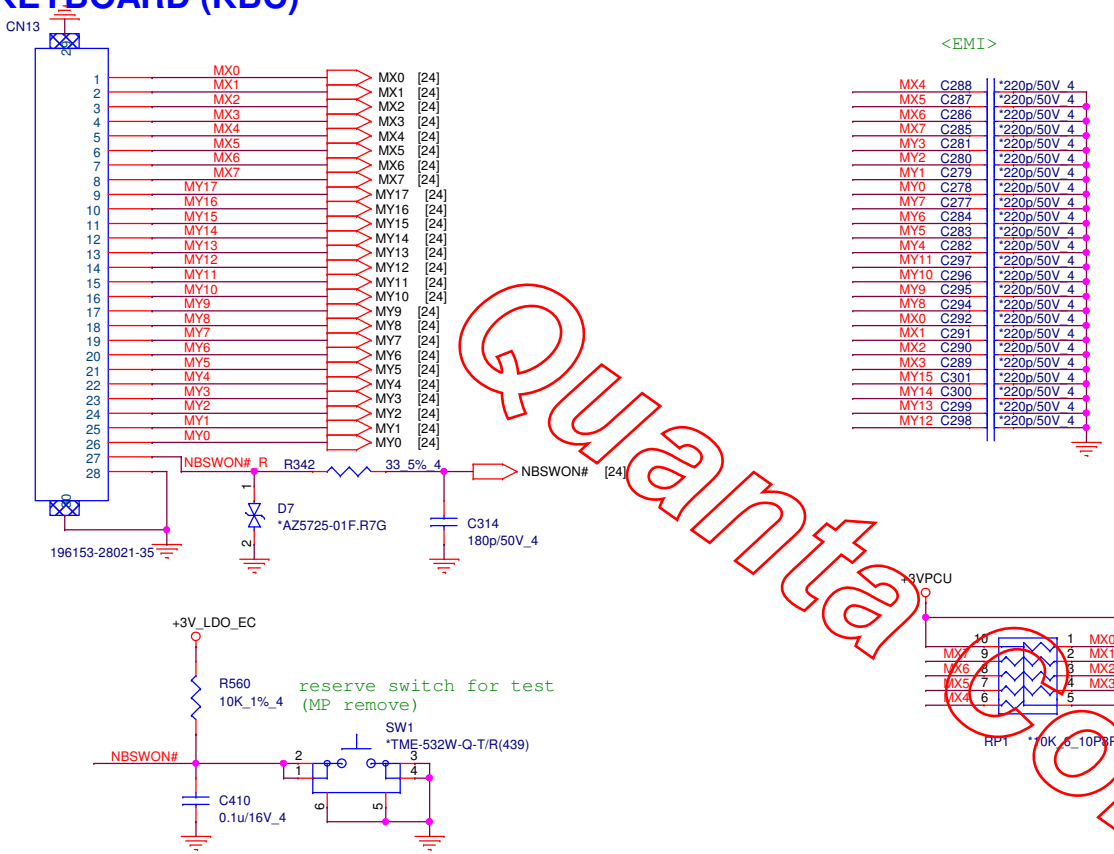
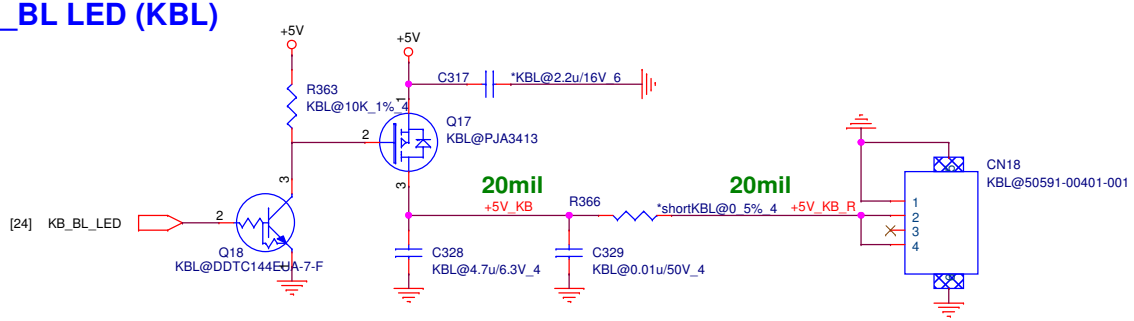
KEYBOARD (KBC)



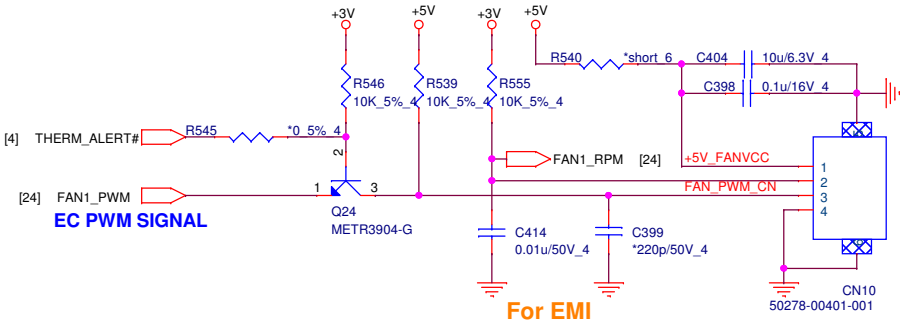
<EMI>

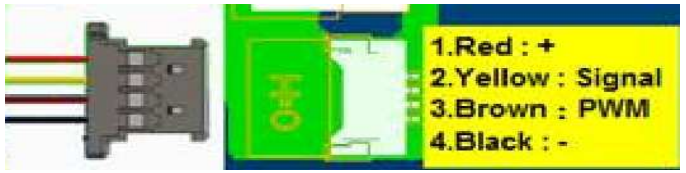
MX4	C288	*220p/50V_4
MX5	C287	*220p/50V_4
MX6	C286	*220p/50V_4
MX7	C285	*220p/50V_4
MY3	C281	*220p/50V_4
MY2	C280	*220p/50V_4
MY1	C279	*220p/50V_4
MY0	C278	*220p/50V_4
MY7	C277	*220p/50V_4
MY6	C284	*220p/50V_4
MY5	C283	*220p/50V_4
MY4	C282	*220p/50V_4
MY11	C297	*220p/50V_4
MY10	C296	*220p/50V_4
MY9	C295	*220p/50V_4
MY8	C294	*220p/50V_4
MX0	C292	*220p/50V_4
MX1	C291	*220p/50V_4
MX2	C290	*220p/50V_4
MX3	C289	*220p/50V_4
MY15	C301	*220p/50V_4
MY14	C300	*220p/50V_4
MY13	C299	*220p/50V_4
MY12	C298	*220p/50V_4

KB_BL LED (KBL)



CPU FAN CTRL(THM)



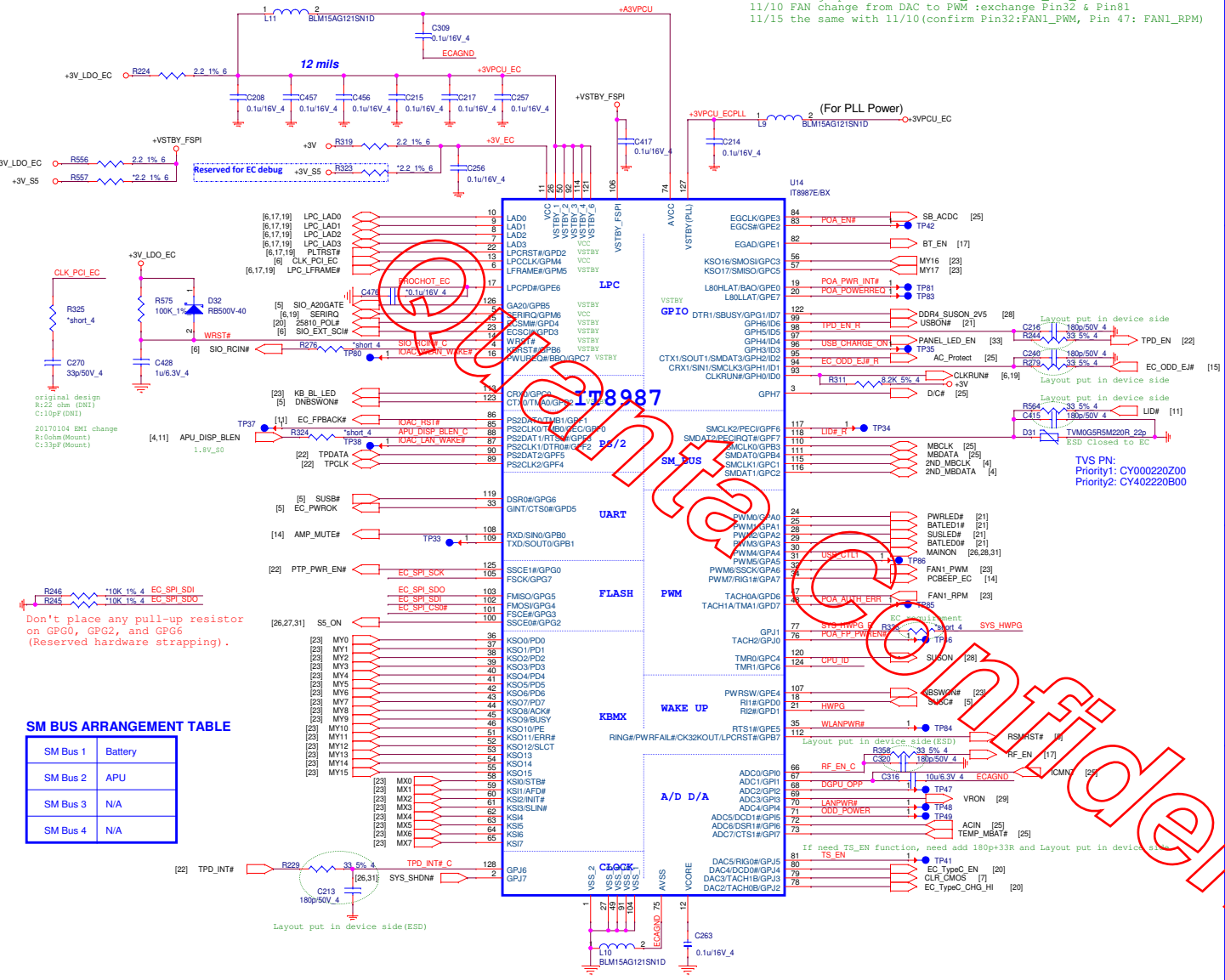


Stich cap

Quanta Computer Inc.		
PROJECT : ZAS		
Size	Document Number	Rev
	KB/FAN/Stich cap	1A
Date: Friday, March 24, 2017	Sheet 23 of 35	

EC(KBC)

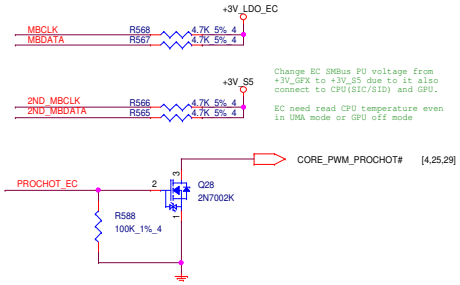
EC different with ZAB list
11/09 change pin 97 from USB-BC_ON to PANEL_LED_EN
11/10 FAN change from DAC to PWM :exchange Pin32 & Pin81
11/15 the same with 11/10(confirm Pin32:FAN1_PWM, Pin 47: FAN1_RPM)



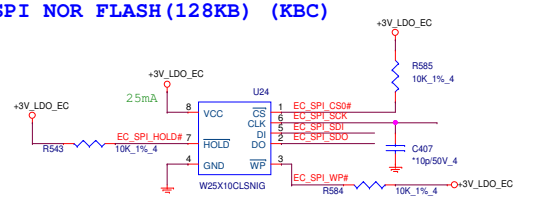
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	APU
SM Bus 3	N/A
SM Bus 4	N/A

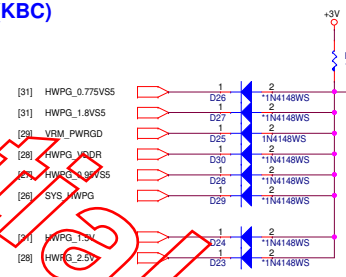
SM BUS PU(KBC)



SPI NOR FLASH(128KB) (KBC)

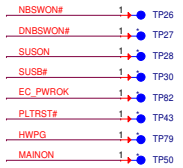


HWPG(KBC)



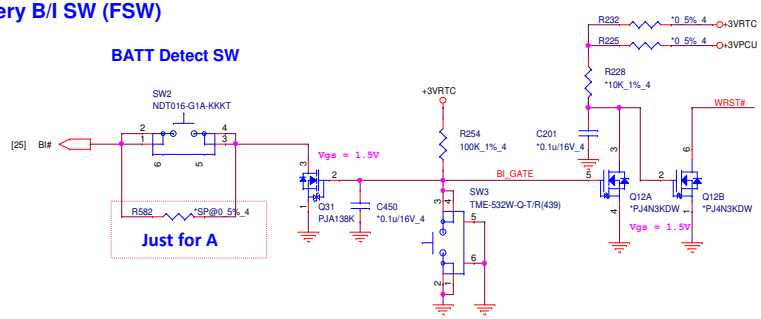
ZAS no GPU, no need this Circuit.

Power sequence

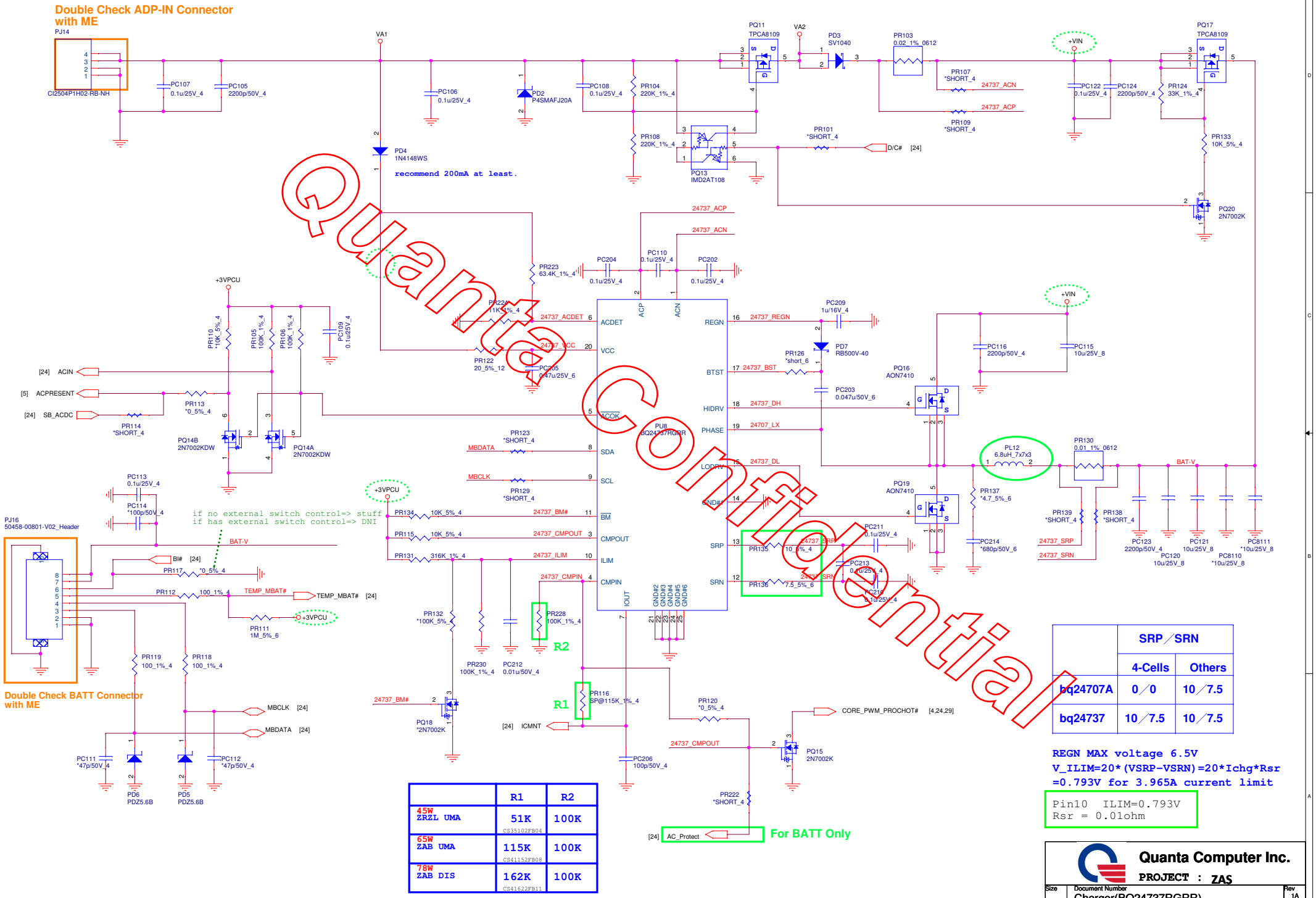


Battery B/I SW (FSW)

BATT Detect SW



Quanta Computer Inc. PROJECT : ZAS			
Size	Document Number		Rev
	EC (ITE8987E/BX)		1A
Date: Friday, March 24, 2017		Sheet 24 of 35	



	R1	R2
45W ZRZL UMA	51K CS35102FB04	100K
65W ZAB UMA	115K CS41152FB08	100K
78W ZAB DIS	162K CS41622FB11	100K

	SRP／SRN	
	4-Cells	Others
bq24707A	0／0	10／7.5
bq24737	10／7.5	10／7.5

REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit

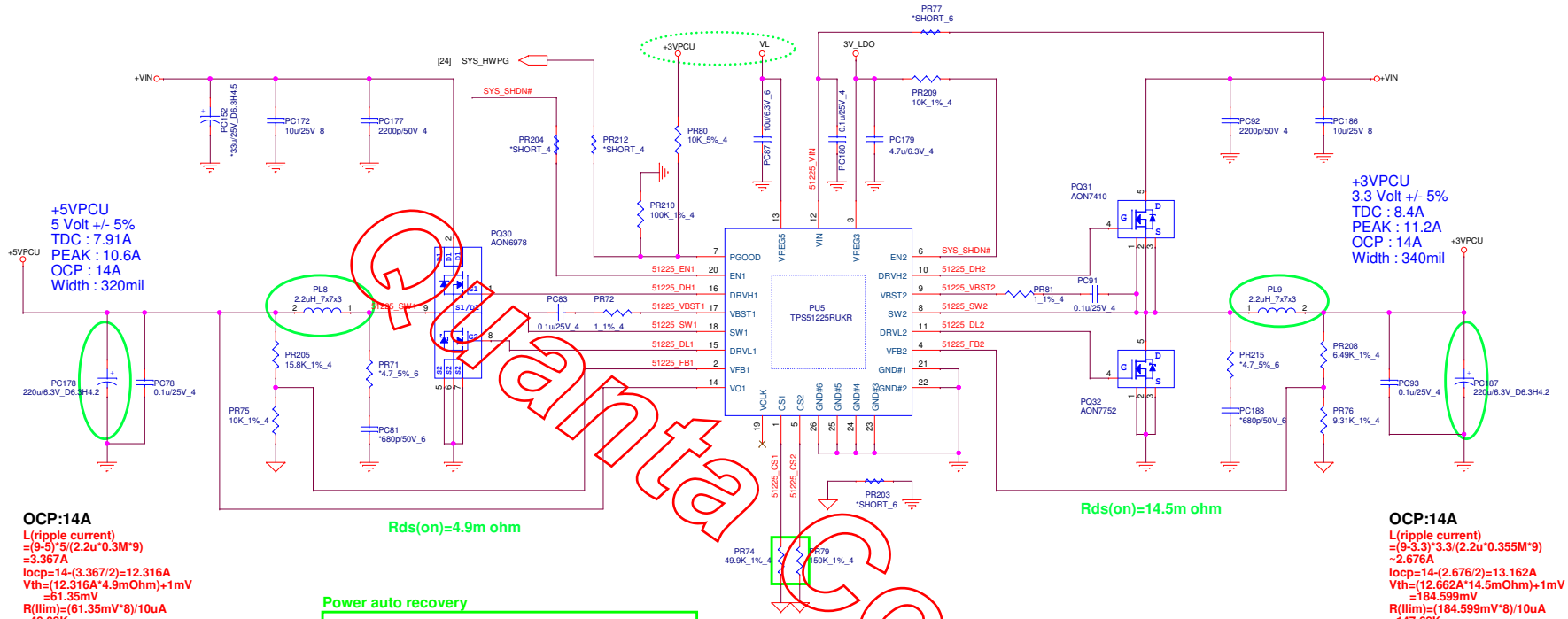
Pin10 ILIM=0.793V
Rsr = 0.01ohm

Quanta Computer Inc.
PROJECT : ZAS

Size	Document Number	Rev
	Charger(BQ24737RGRR)	1A
Date: Friday, March 24, 2017	Sheet 25 of 35	

3V_LDO no need Intersheet References, EE side connection with 3V_LDO_EC

+VIN [11,15,22,25,27,28,30,31,32,33] → VL [31]
+5VPCU [27,31]
+3VPCU [7,11,14,15,21,23,24,25,31] → SYS_SHDN# [24,31]



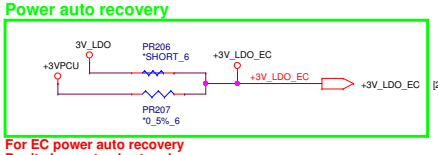
OCP:14A
L(ripple current)
=(9-5)*5/(2.2u*0.3M*9)
=3.367A
Iocp=14-(3.367/2)=12.316A
Vth=(12.316A*4.9mOhm)+1mV
=61.35mV
R(Ilim)=(61.35mV*8)/10uA
~49.08K

Rds(on)=4.9m ohm

Rds(on)=14.5m ohm

OCP:14A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.355M*9)
~2.676A
Iocp=14-(2.676/2)=13.162A
Vth=(12.662A*14.5mOhm)+1mV
=184.599mV
R(Ilim)=(184.599mV*8)/10uA
=147.68K

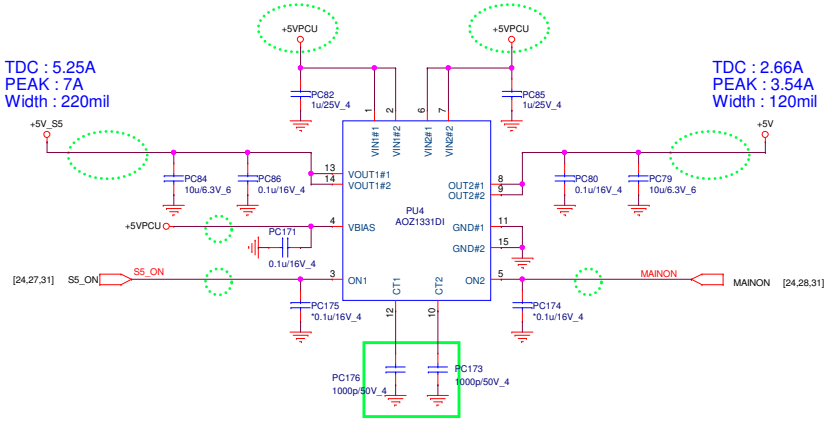
Power auto recovery



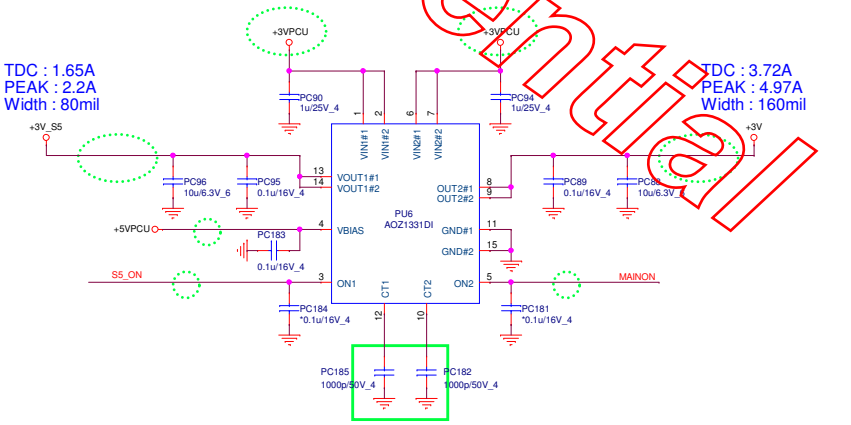
For EC power auto recovery
Don't change to short pad

+3V_LDO_EC
TDC : 100MA

+5V_S5 [7,20,21,28,29,32,33]
+5V [12,14,15,18,23,31]
→ +3V_S5 [5,6,7,13,19,20,22,24,28,32]
+3V [4,5,6,7,9,11,12,13,14,15,16,17,18,19,22,23,24,27,28,29,31]



Soft-Start



Soft-Start

Quanta Computer Inc.		
PROJECT : ZAS		
Size	Document Number: SYSTEM 5V/3V (TPS51225R)	Rev: 1A
Date: Friday, March 24, 2017	Sheet 26 of 35	

+VIN [11,15,22,25,26,28,30,31,32,33]
VDDP_0.95V_S5 [6,7,31]
VDDP_0.95V [2,6,7,31]
+5VPCU [26,31]
+3V [4,5,6,7,9,11,12,13,14,15,16,17,18,19,22,23,24,26,28,29,31]

Fsw=550KHz

PR199 73.2K_1%_4

PC74 *0.01u/50V_4

+VIN

G5335-TON-1

PU13 G5335QT2U

NC, TON, VCC, V+#1, V+#2, V+#3, V+#4

PC72 *0.1u/25V_4

PC71 2200p/50V_4

PC170 10u/25V_8

+5VPCU

PR59 10_5%_4

G5335-VCC-1

PC67 10u/6.3V_6

+3V

PR195 100K_1%_4

PR196 *SHORT_4

[24] HWPG_0.95VS5

G5335-PWRGD-1

PGOOD

+5VPCU

PR63 *0_5%_4

G5335-PFM-1

PFM

G5335-AGND-1

PR197 *SHORT_4

Pulse-Skipping mode

G5335-EN-1

EN

PR62 *SHORT_4

[24,26,31] S5_ON

G5335-SS-1

SS

PC168 *0.047u/16V_4

PC70 0.047u/16V_4

G5335-AGND-1

G5335-AGND-1

PR64 *SHORT_4

G5335-AGND-1

BST

G5335-BST-1

PR61 2.2_1%_6

PC66 0.1u/25V_4

LX#1, LX#2, LX#3, LX#4, LX#5, LX#6

G5335-LX-1

PL7 0.68uH_7x7x3

PR60 *4.7_5%_6

PC68 *680p/50V_6

PGND#1, PGND#2, PGND#3, PGND#4, PGND#5, AGND

G5335-AGND-1

FB

G5335-FB-1

VFB=0.8V

PC76 22u/6.3V_6

PC73 22u/6.3V_6

PC75 22u/6.3V_6

PC63 22u/6.3V_6

PC69 22u/6.3V_6

PC65 *22u/6.3V_6

PC64 *22u/6.3V_6

PC77 0.1u/16V_4

PR68 SP@0_5%_4

PC169 *1000p/50V_4

R1

PR65 3.83K_1%_4

PR198 20K_1%_4

R2

PR69 1_1%_4

VDDP_0.95V

APU_VDDP_RUN_FB_H [4]

APU_VDDP_RUN_FB_L [4]

PR67 *SHORT_4

PR66 *SHORT_4

G5335-AGND-1

Vo=0.8*(R1+R2)/R2
=0.95V

VDDP_0.95V_S5

[31] MAIND

MAIND

PQ29 AON6752

VDDP_0.95V

+0.95V
TDC : 5.25A
PEAK : 7A
Width : 220mil

VDDP_0.95V_S5
0.95 Volt +/- 5%
TDC : 6.15A
PEAK : 8.2A
Width : 260mil

AM9420AYN23AC 0.95V
AM9220AYN23AC 0.95V
AM9120AYN23AC 0.95V

AMD requirements (depends on OPN)
Refer to datasheet...SR: 55366 / BR:53557 / SR FT4:55367
1.05V: 2.49K ohm, CS22492FB22
0.95V: 0 ohm, CS00002JB38

Quanta Computer Inc.
PROJECT : ZAS

Size	Document Number	Rev
	VDDP_0.95V_S5 (G5335QT2U)	1A

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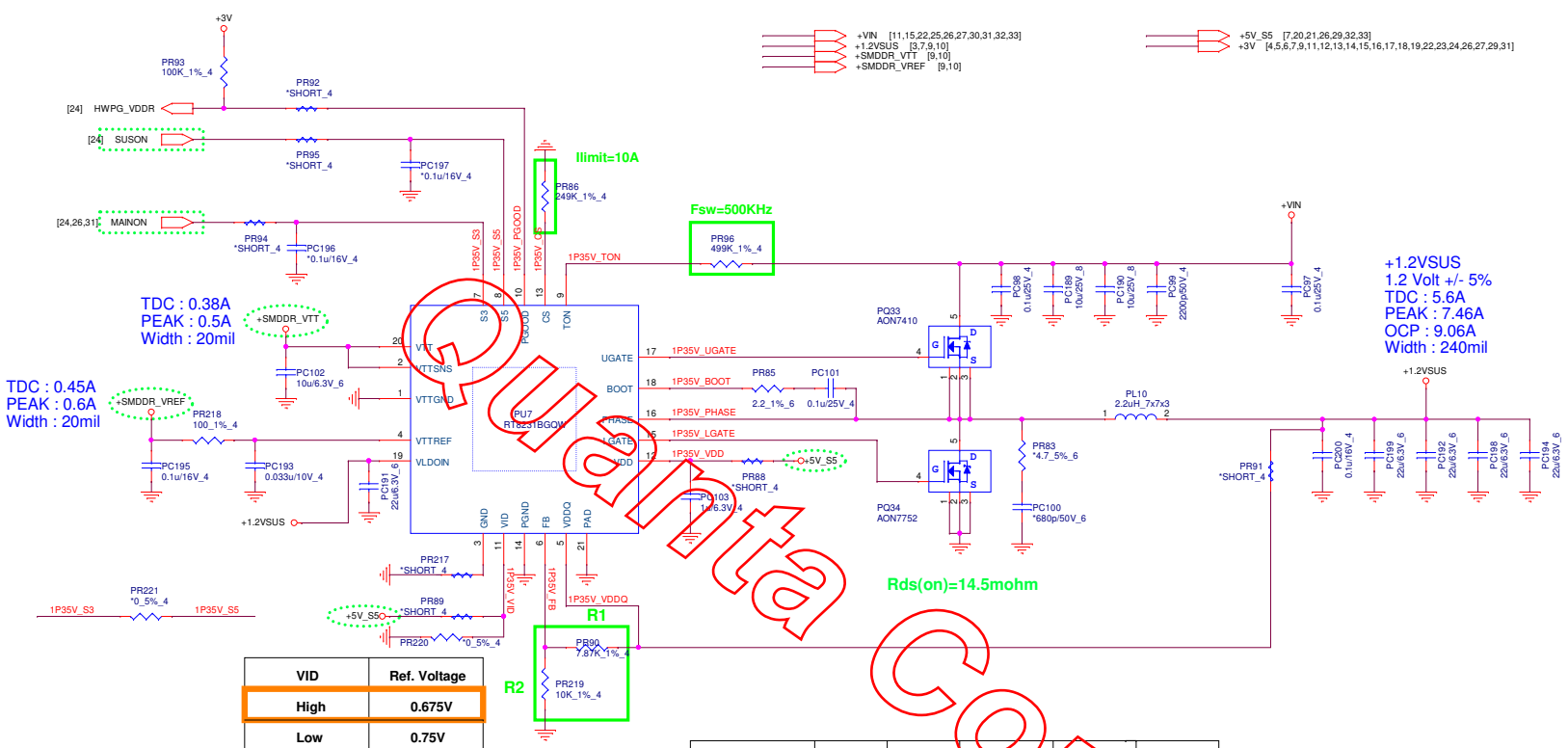


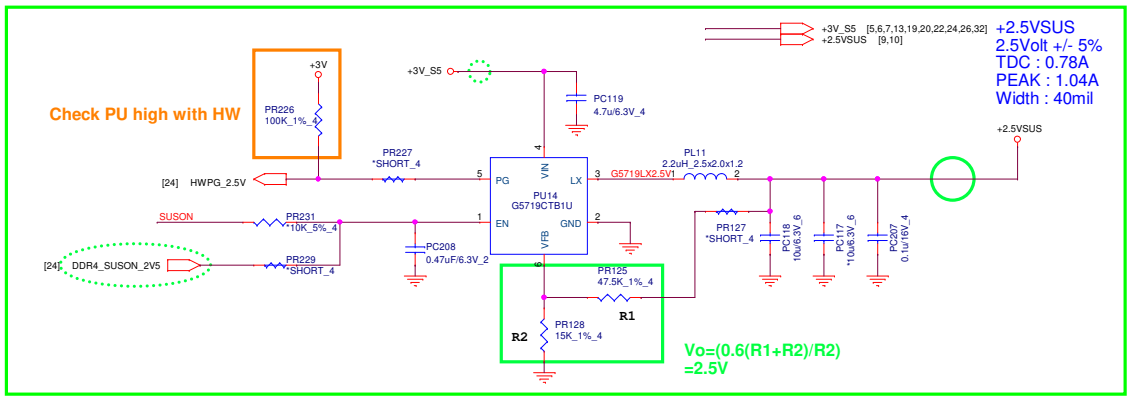
VID	Ref. Voltage
High	0.675V
Low	0.75V

OCP=10A
L ripple current
=(19-1.2)*1.2/(1u*500k*19)
=2.248A
Vtrip=10-(2.248/2)*14.5mohm
=128.702mV
Rlimit=128.702mV/5uA*10=257.4Kohm

DDR=1.2V
R1=7.87K/F_4
R2=10K/F_4

	S3	S5	VDDQ	VTTREF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

+2.5VSUS Power Rail For DDR4



Quanta Computer Inc.
PROJECT : ZAS

Size	Document Number	Rev
	DDR4_+1.2VSUS (RT8231BGQW)	1A

Date: Friday, March 24, 2017 Sheet 28 of 35

+VIN [11,15,22,25,26,27,28,30,31,32,33]
VDDCR_NB [7,30,32]
VDDCR_CPU [7,30]

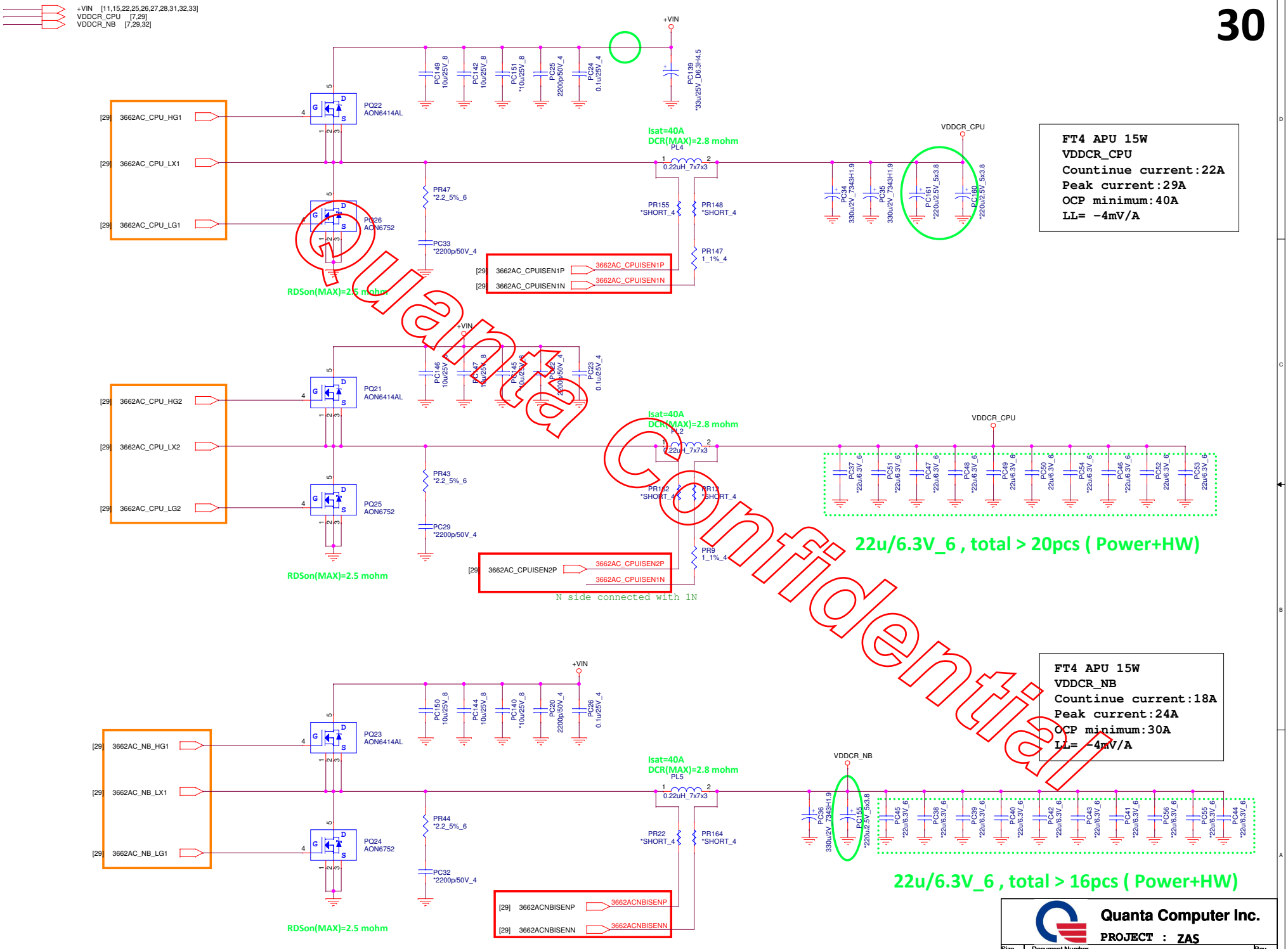
+5V_S5 [7,20,21,26,28,32,33]
VDD_18 [4,5,6,7,11,22,31]
+3V [4,5,6,7,9,11,12,13,14,15,16,17,18,19,22,23,24,26,27,28,31]

Vset1	874.6mV
Delta Vset1	1149mV
Vtsen	1.02V
Vtsen_NB	223mV

Quanta Computer Inc.
PROJECT : ZAS

Size	Document Number	Rev
	VGACORE(RT3662EB2)	1A

Date: Friday, March 24, 2017 Sheet 29 of 35



Quanta Computer Inc.
PROJECT : ZAS

Size	Document Number	Rev
	VGACORE(RT3662EB2)	1A
Date: Friday, March 24, 2017	Sheet 30 of 35	

+3VPCU [7,11,14,15,21,23,24,25,26]
VDD_18_S5 [5,7]
VDD_18 [4,5,6,7,11,22,29]
VDDP_0.95V_S5 [6,7,27]
VDDCR_FCH_S5 [7,32]
+1.5V [7,14]
+5VPCU [26,27]

VL [26]
+VIN [11,15,22,25,26,27,28,30,32,33]
+3V [4,5,6,7,9,11,12,13,14,15,16,17,18,19,22,23,24,26,27,28,29]
+5V [12,14,15,18,23,26]
VDDP_0.95V [2,6,7,27]

VDD_18_S5
1.8 Volt +/- 5%
TDC : 1.67A
PEAK : 2.23A
Width : 80mil

Vo=0.6*(R1+R2)/R2
=1.8V

TDC : 1.13A
PEAK : 1.5A
Width : 60mil

VDDCR_FCH_S5
0.775 Volt +/- 5%
TDC : 0.3A
PEAK : 0.4A
Width : 20mil

Vout = (1+Rg/Rh)*0.5
=0.78V

+1.5V
1.5Volt +/- 5%
TDC : 0.57A
PEAK : 0.76A
Width : 40mil

Vo=(0.6(R1+R2)/R2)
=1.5V

Thermal Protection

Need fine tune
for thermal protect point
Note placement position
TEMP=80'C

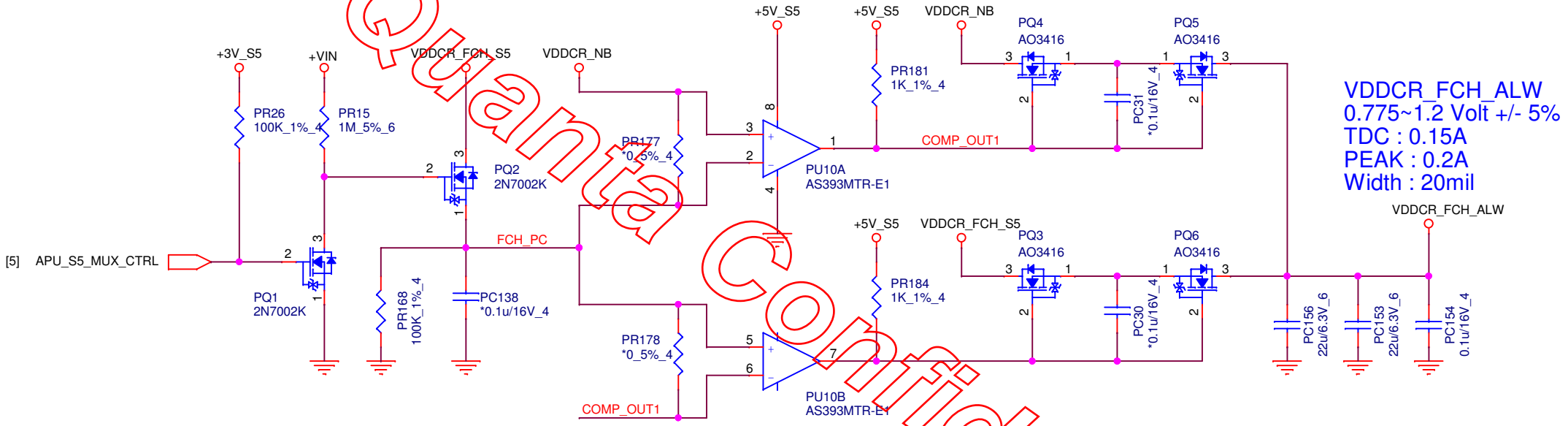
Rset(Kohm)=0.0012T*T-0.9308T+96.147
=25.69 K ohm

HYST=VCC for 10 degree Hys.
HYST=GND for 30 degree Hys.

Quanta Computer Inc.
PROJECT : ZAS

Size	Document Number	Rev
	+1.8V/+0.775V/+1.5V/Thermal	1A
Date: Friday, March 24, 2017	Sheet 31 of 35	

For Type 1 & 3



VDDCR_FCH_ALW
0.775~1.2 Volt +/- 5%
TDC : 0.15A
PEAK : 0.2A
Width : 20mil

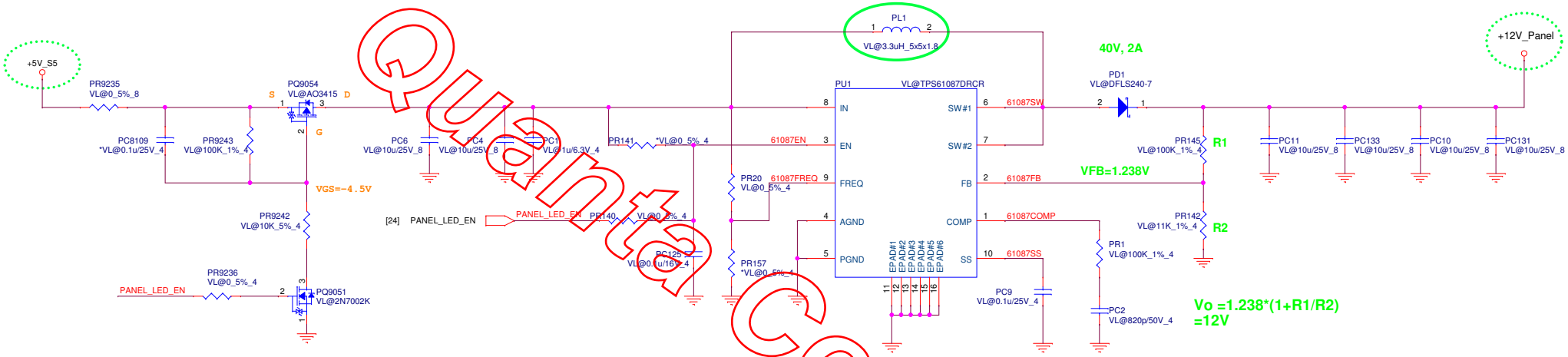
Quanta Computer Inc.
PROJECT : ZAS

Size	Document Number	Rev
	VDDCR_FCH_ALW	1A
Date: Friday, March 24, 2017	Sheet 32 of 35	

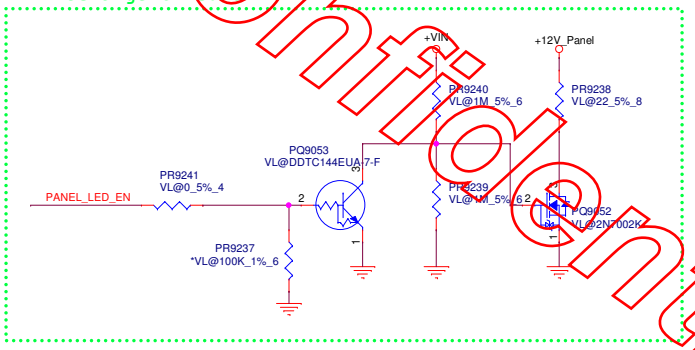
+5V_S5 [7,20,21,26,28,29,32]
+12V_Panel [11]

Panel Spec (TFT-LCD 14")
VLED : 6V~21V (Tpy:12.5V)
Power Consumption : 3W (MAX)

+12V_Panel
12.5 Volt +/- 5%
PEAK : 0.35A
Width : 20mil



BL Discharge Circuit



Quanta Computer Inc.		
PROJECT :		
Size	Document Number	Rev
	LED Panel (TPS61087)	1A
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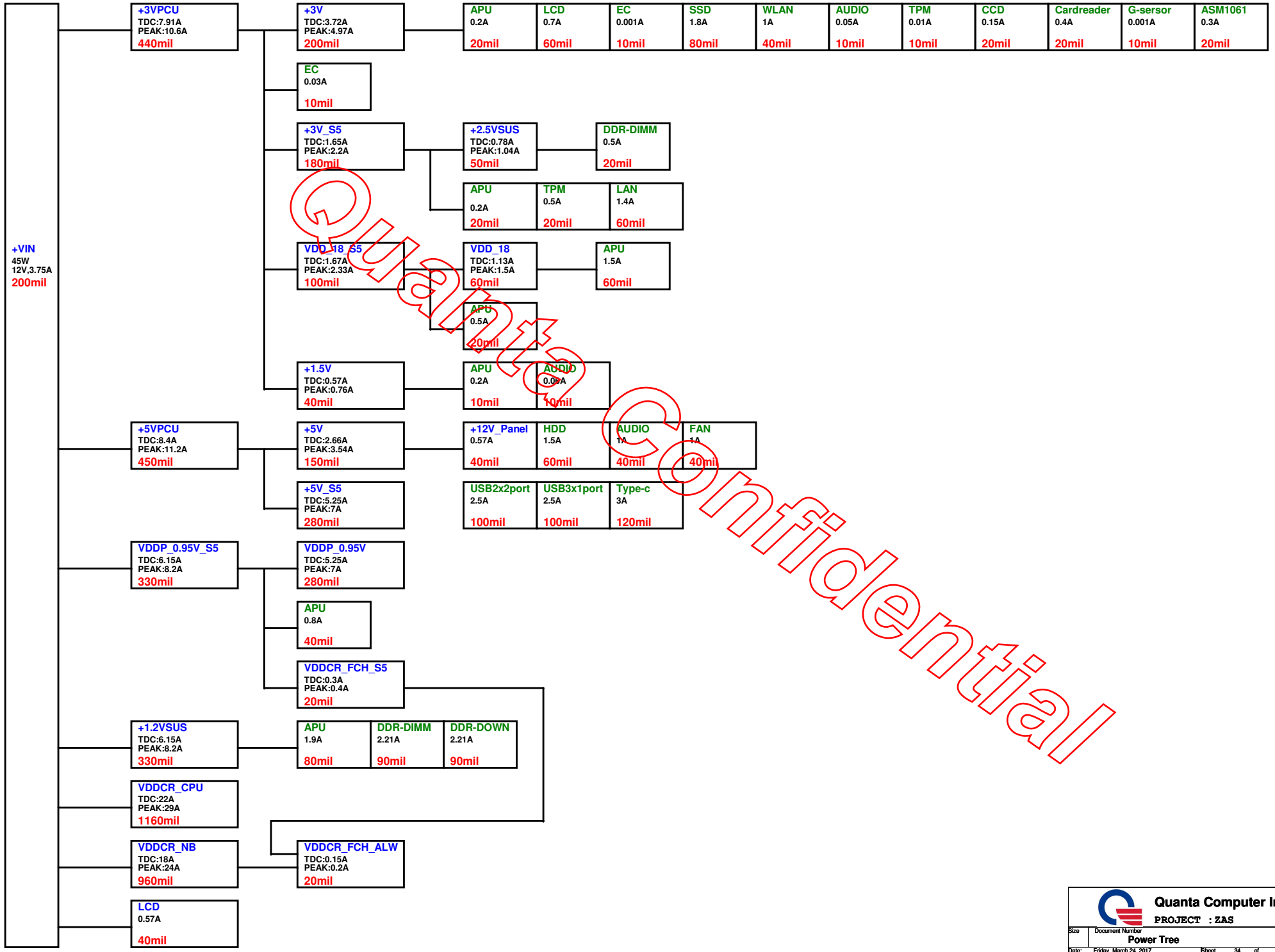
Power Tree



Quanta Computer Inc.
PROJECT : ZAS

Size	Document Number	Rev
	Power Tree	1A

Date: Friday, March 24, 2017 Sheet 34 of 35

MODEL	REV	Change List
ZAS M/B	A	First Release

Model / Page	ZAS M/B From	To
1		
2		
3		
4		
5		
6		
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41		

Quanta Computer Inc.

PROJECT : ZAS

Size	Document Number	Rev
	CHANGE LIST	1A

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