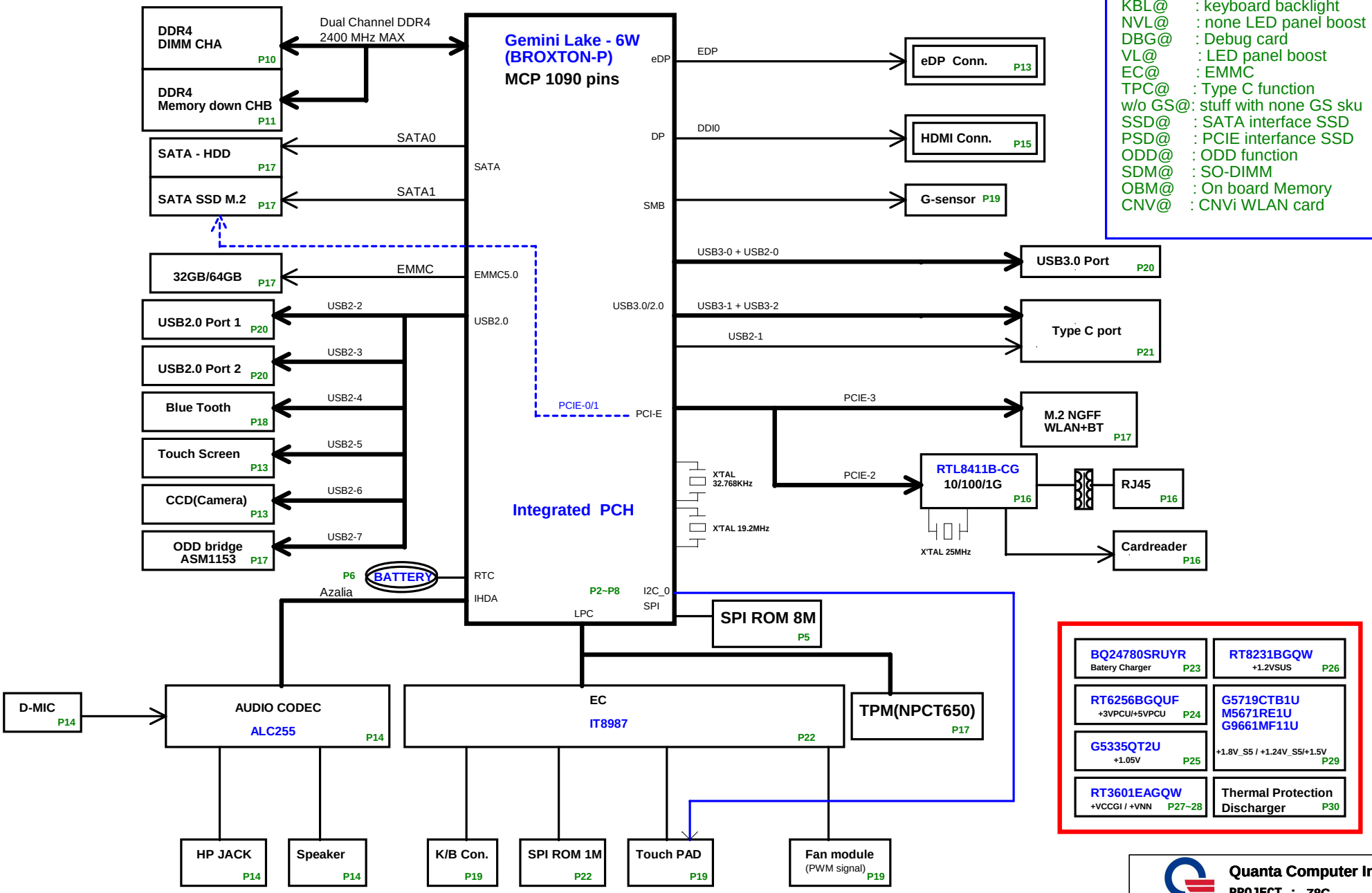
Z8G SYSTEM BLOCK DIAGRAM

BOM

TPM@ : TPM
GS@ : G-SENSOR
CB@ : Cloud book SKU
EJ@ : EJ sereies SKU
KBL@ : keyboard backlight
NVL@ : none LED panel boost
DBG@ : Debug card
VL@ : LED panel boost
EC@ : EMMC
TPC@ : Type C function
w/o GS@: stuff with none GS sku
SSD@ : SATA interface SSD
PSD@ : PCIE interfance SSD
ODD@ : ODD function
SDM@ : SO-DIMM
OBM@ : On board Memory
CNV@ : CNVi WLAN card



BQ24780SRUYR Batery Charger P23	RT8231BGQW +1.2VSUS P26
RT6256BGQUF +3VPCU/+5VPCU P24	G5719CTB1U M5671RE1U G9661MF11U
G5335QT2U +1.05V P25	+1.8V_S5 / +1.24V_S5/+1.5V P29
RT3601EAGQW +VCCGI / +VNN P27~28	Thermal Protection Discharger P30

Quanta Computer Inc.
PROJECT : Z8G
Size | Document Number | Rev 1A
Block Diagram
Date: Tuesday, December 26, 2017 | Sheet 1 of 35

GLK ULT (DDR4)

02

[7] +1.2VSUS_Q

[10] M_A_DQ[63:0]

[11] M_B_DQ[63:0]

U27A

DDR4_LP3_LP4

DDR0

1 OF 13

U27B

DDR4_LP3_LP4

DDR1

2 OF 13

Default no stuff

VREF trace must be at least 20 mils wide and space

R179 , R183 close to CPU

Trace length < 500 mils

Trace width = 15 mils

Trace spacing = 20 mils

colsed to CPU pin within 100 mils

C544 *1000p/50V_4

R583 *10_5%_4

C545 *1000p/50V_4

R584 *10_5%_4

DRAMRST-SODIMM

Trace length < 4500 mils, 50 ohm impendence

Trace spacing = 15 mils

CPU

SO-DIMM1

+1.2VSUS_Q

R187 1K_1%_4

MA_DRAMRST#

R178 *S_4

C144 *0.1u/16V_4

M_A_DRAMRST# [10]

Trace length < 4500 mils, 50 ohm impendence

Trace spacing = 15 mils

CPU

SO-DIMM2

+1.2VSUS_Q

R180 1K_1%_4

MB_DRAMRST#

R182 *S_4

C142 *0.1u/16V_4

M_B_DRAMRST# [11]

Quanta Computer Inc.

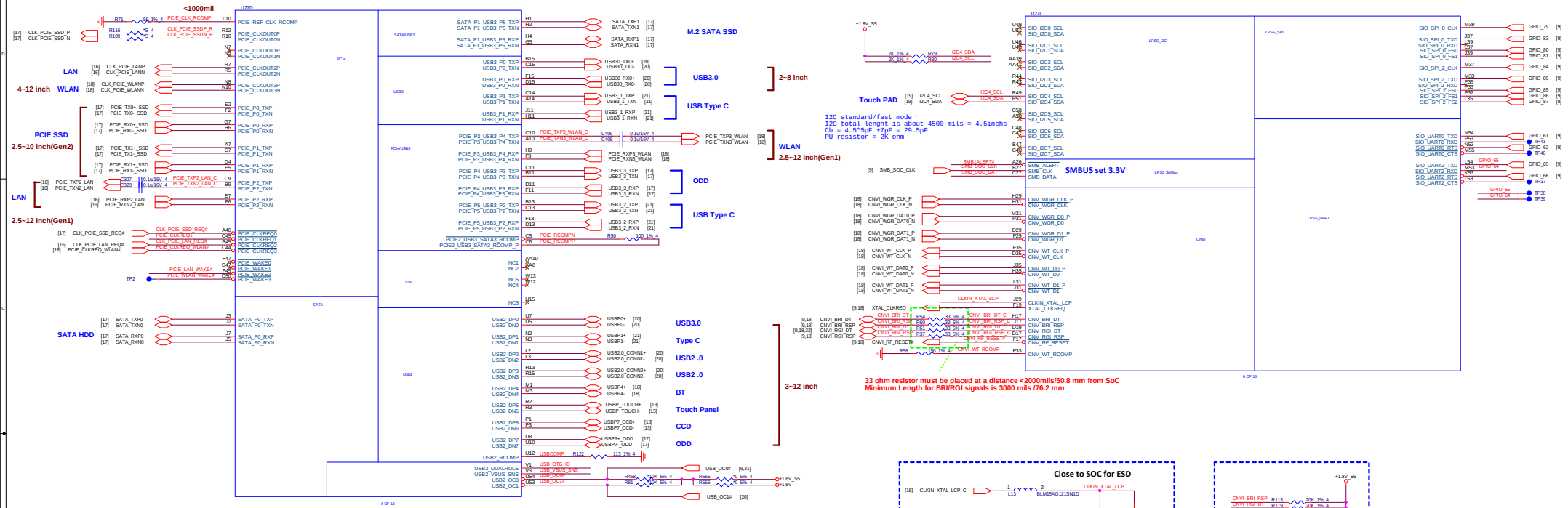
PROJECT : Z8G

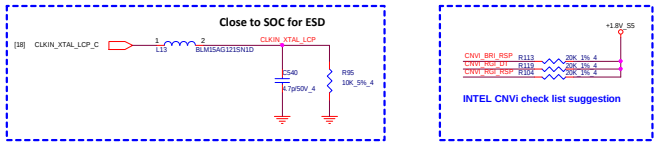
Size	Document Number	Rev
	GLK(MEMORY)	1A

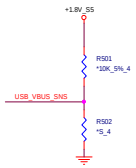
Date: Tuesday, December 26, 2017 Sheet 2 of 35

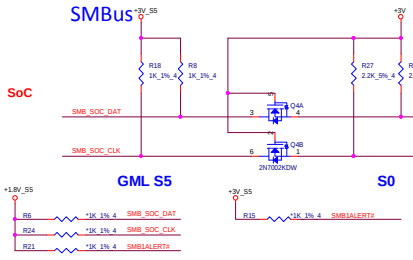
Gemini lake (SATA , ODD, CLK ,USB,PCIE)

03





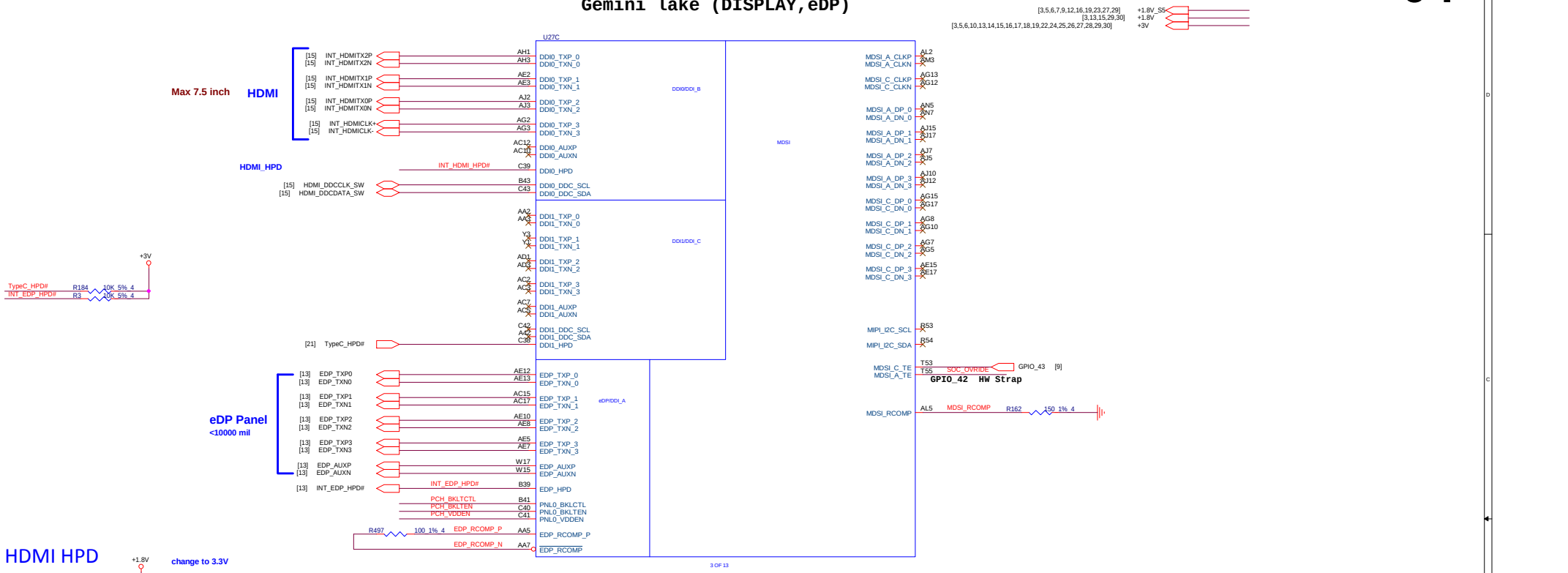




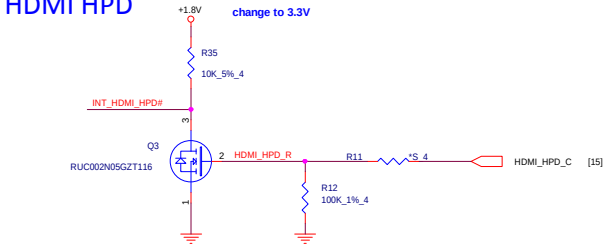
Quanta Computer Inc.			
PROJECT : Z8G			
Size	Document Number		Rev
	GLK(PCIE/USB/SATA/CNVI)		1A
Date: Tuesday, December 26, 2017	Sheet 3 of 35		

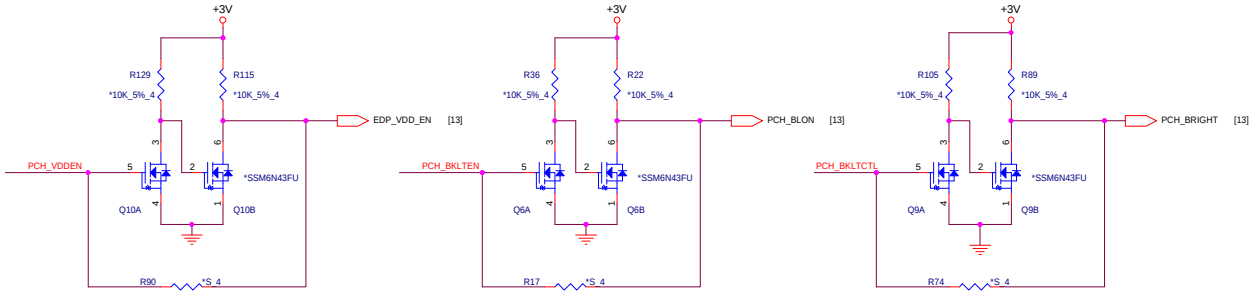
04

Gemini lake (DISPLAY,eDP)



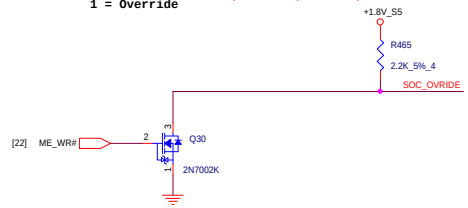
HDMI HPD





Override

Flash Descriptor Override (SOC_OVRIDE)
0 = Normal Override(Normal operation)
1 = Override



Quanta Computer Inc.		
PROJECT : Z8G		
Size	Document Number: GLK (HDMI/eDP)	Rev: 1A
Date: Tuesday, December 26, 2017	Sheet 4 of 35	

Gemini lake (EMMC/LPC/I2C/GPIO/HDA)

05

HDA

LPC set 3.3V

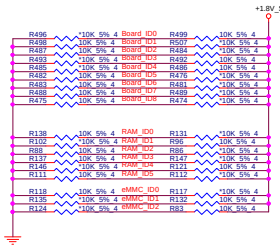
SPI is 1.8V

set to 3.3V

set to PU

BOARD ID SETTING

HW strap ID	Strap pin Description
Board_ID0	0 = w/o type C 1 = w/ type C
Board_ID1	0 = with EMMC 1 = without EMMC <HDD only>
Board_ID2	0 = M.2 SATA SSD 1 = M.2 PCIE SSD
Board_ID3	0 = none G sensor 1 = G sensor
Board_ID4	0 = none TPM 1 = TPM
Board_ID5	0 = With SATA Port 0 Connector 1 = Without SATA Port 0 Connector
Board_ID6	0 = With SATA Port 1 Connector 1 = Without SATA Port 1 Connector
Board_ID7	0 = EJ series 1 = Cloud book
Board_ID8	0 = UMA 1 = GPU
RAM_ID0	0 = With on board RAM 1 = Without on board RAM(SODIMM only)
RAM_ID1	0 = On board RAM 2GB 1 = On board RAM 4GB
RAM_ID2	(Reserved)



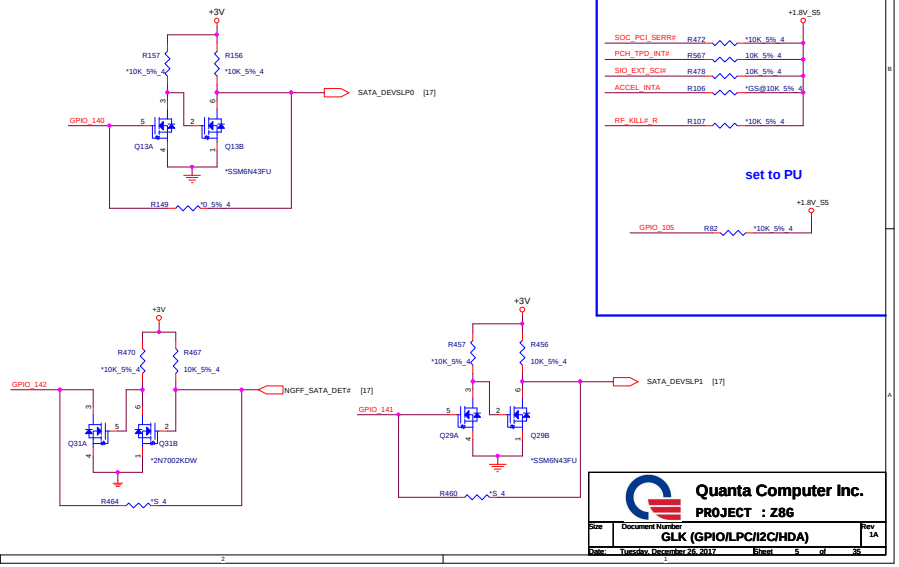
RAM_ID5	RAM_ID4	RAM_ID3	Vender
0	0	0	Miron-2GB
0	0	1	Hynix-2GB
0	1	0	Samsung-2GB
0	1	1	

eMMC_ID1	eMMC_ID0	eMMC_ID0	Vender
0	0	0	Samsung 32/64GB
0	0	1	Hynix 32/64GB
0	1	0	Kingston 32/64GB
0	1	1	Sandisk 32G/64G/128GB
1	1	1	Toshiba 128GB

Series resistance 33R is recommended for signals as per PDG Table 27-2

SP@ socket P/N: DFHS08FS023 only for A-TEST

SPI ROM	Vender	Size	Quanta P/N	Vender P/N
1.8V	WND	8M	AKE5EZN0N01	W25Q64FWSSIQ
	GGD	8M	AKE5EG-0Q01	GD25LB64CSIGR
	MAX	8M	AKE5EZN0Z01	MX25U6473FM2I-10G



Quanta Computer Inc.
PROJECT : Z8G
Size: Document Number: GLK (GPIO/LPC/I2C/HDA) Rev: 1A
Date: Tuesday, December 26, 2017 Sheet 5 of 35

Gemini lake (PMU/PMIC/RTC)

06

PMU set to 3.3V

RTC is 3.3V

PMU set 3.3V

1.8V

check list use 20k

EC reset RTC

RTC Circuitry (RTC)

RTC Clock 32.768KHz (CPU)

Trace width = 20 mils

Trace length < 1000 mils

+3V_RTC Trace width = 20 mils

20MIL

CH01006JB08 -> 10p
CH01506JB06 -> 15p
CH-6806TB01 -> 6.8p

ML1220 Coin type
AHL03001031 [VDE] 17mAH
AHL03001057 [DBV] 17mAH

colsed to CPU pin within 100 mils

colsed to CPU pin within 100 mils

colsed to CPU pin within 100 mils

Quanta Computer Inc.
PROJECT : Z8G

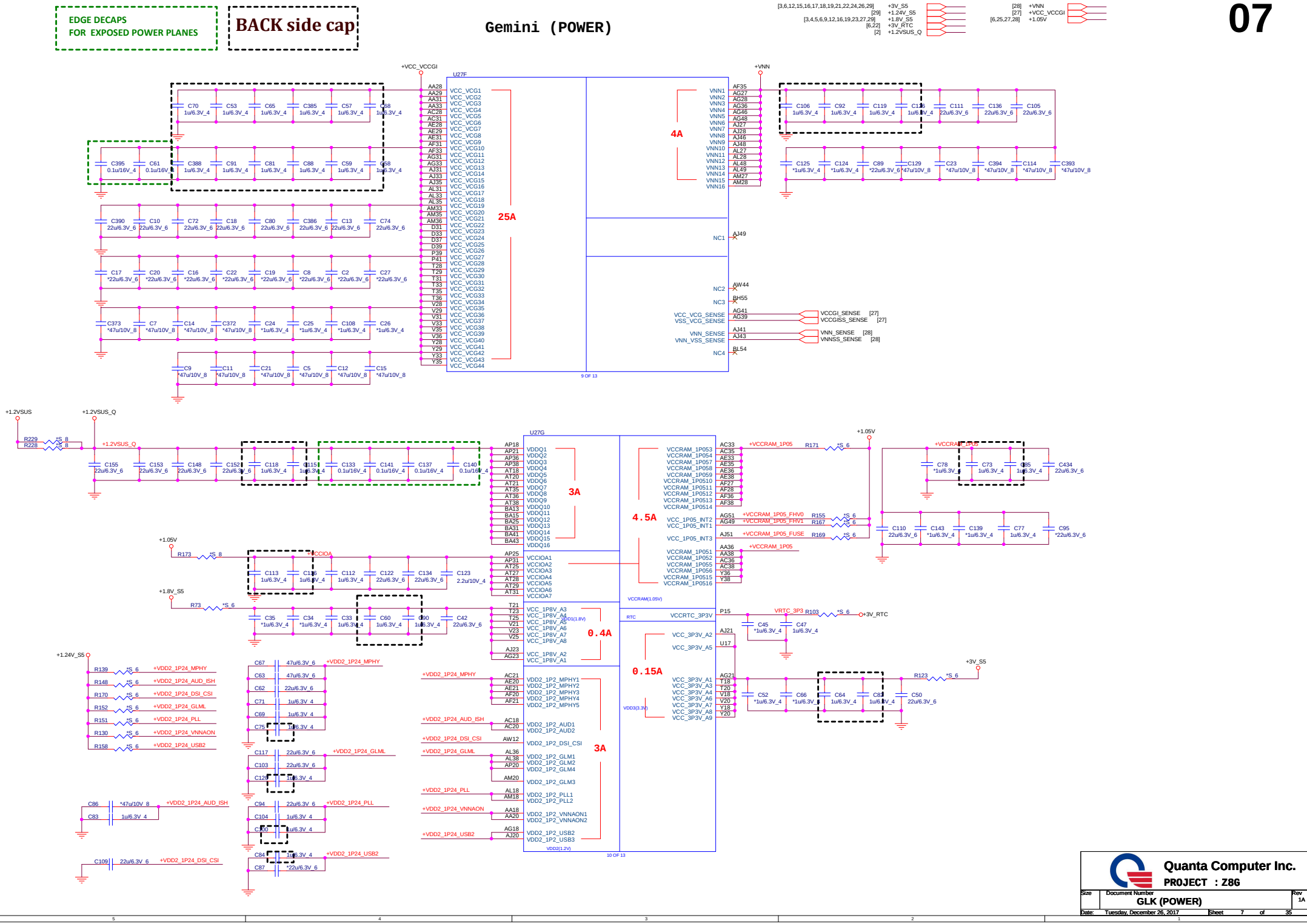
Size	Document Number	Rev
	GLK (PMU/PMIC/SMB/RTC)	1A
Date: Tuesday, December 26, 2017	Sheet 6 of 35	

EDGE DECAPS
FOR EXPOSED POWER PLANES

BACK side cap

Gemini (POWER)

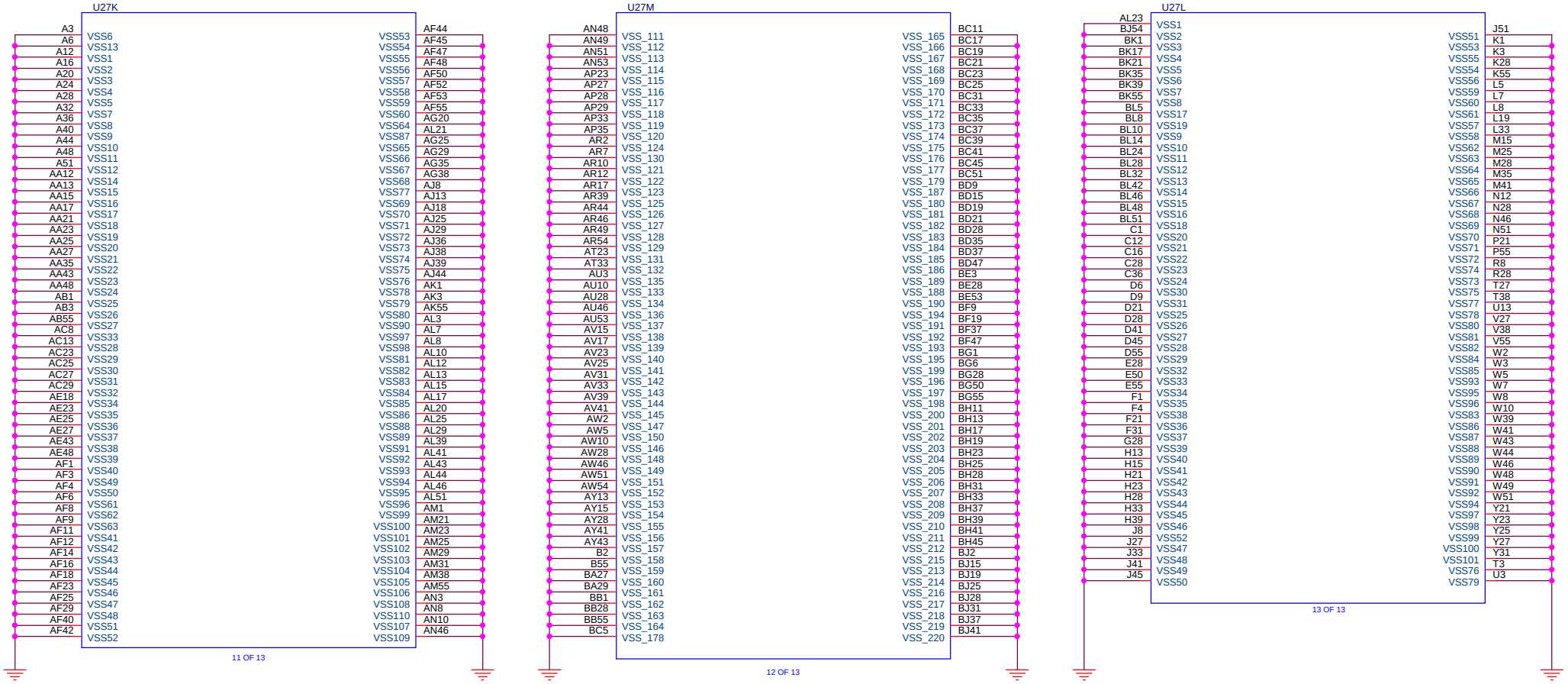
07



Quanta Computer Inc.	
PROJECT : Z8G	
Size	Document Number: GLK (POWER) — Rev: 1A
Date: Tuesday, December 26, 2017	Sheet 7 of 35

GLK ULT (GND)

08



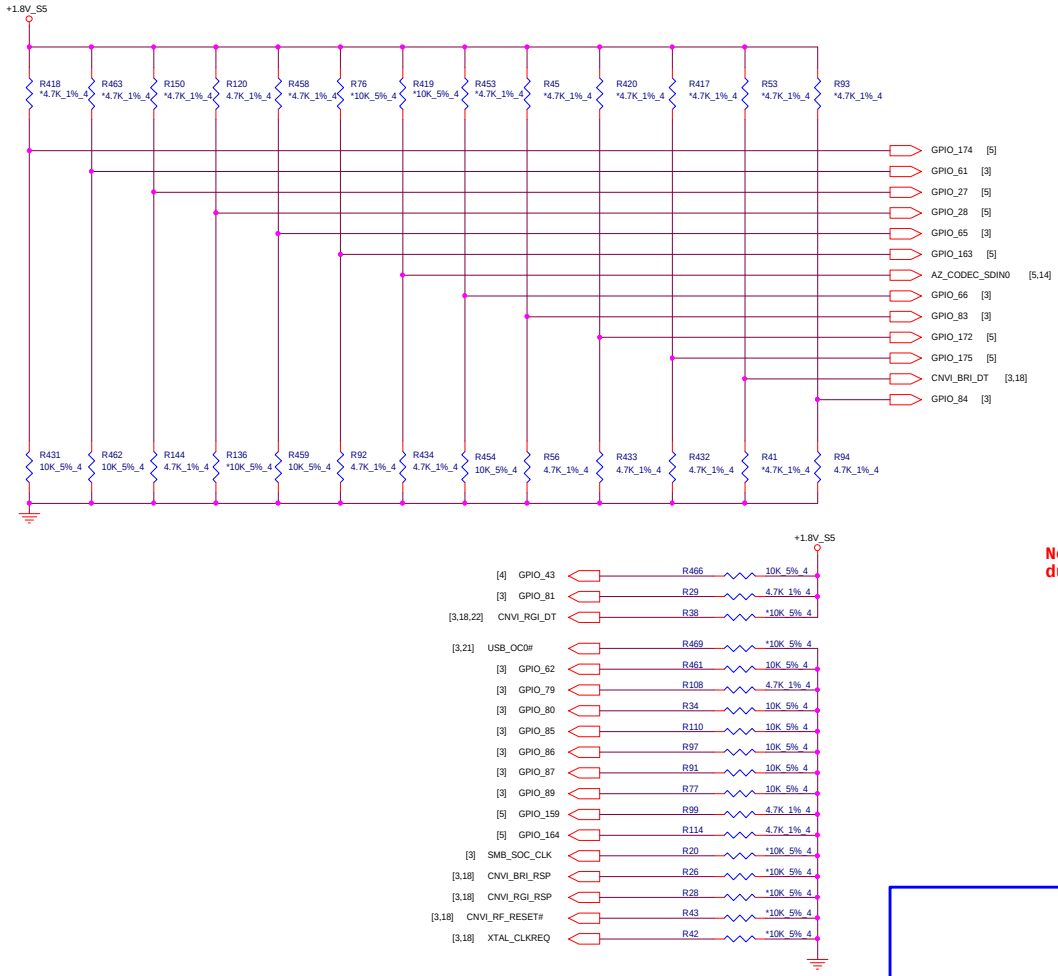
Quanta Computer Inc.

PROJECT : Z8G

Size	Document Number	Rev
	GLK (GND)	1A

Date: Tuesday, December 26, 2017 Sheet 8 of 35

HARDWARE STRAPS

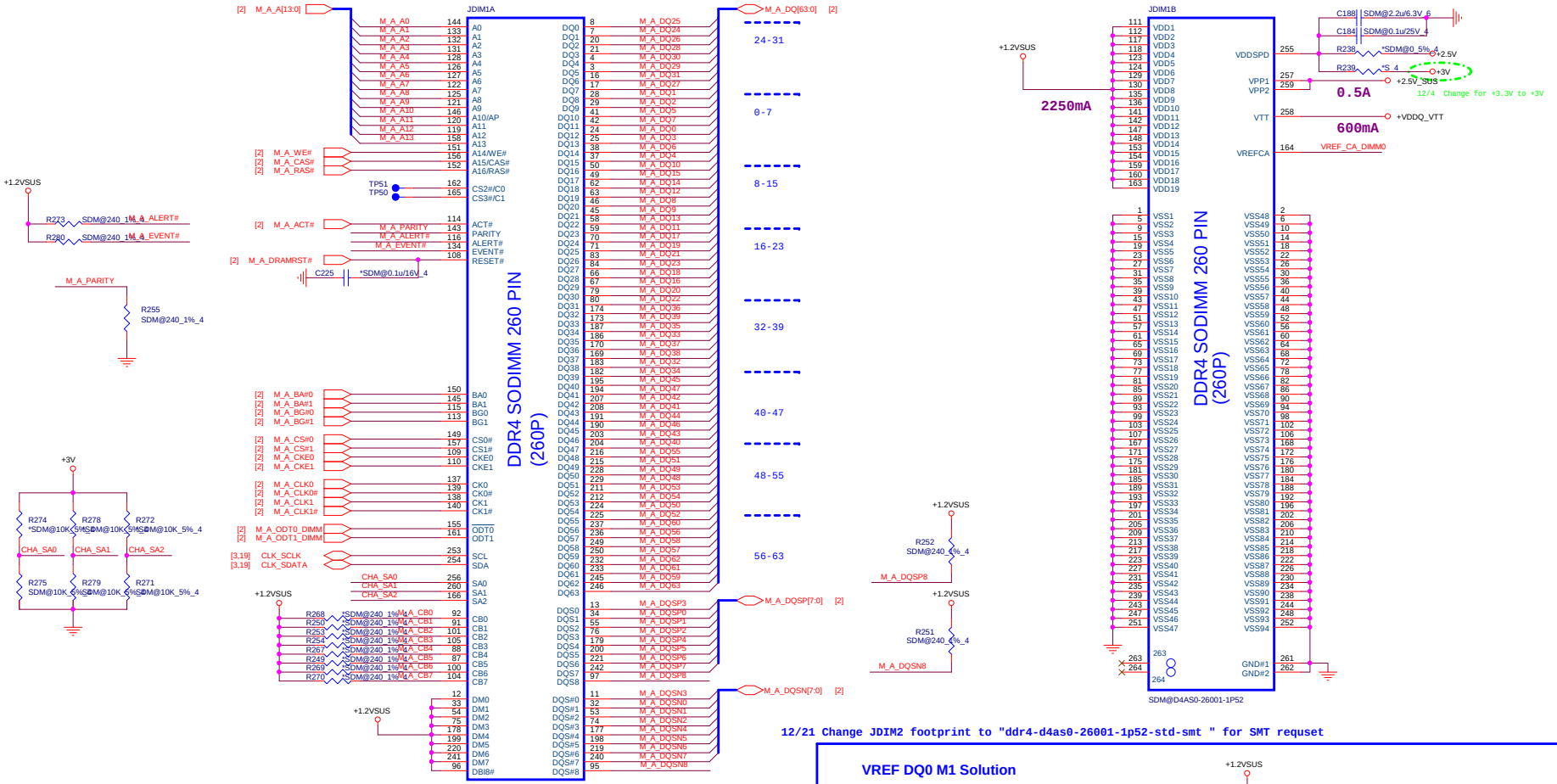


Note: If platform is using eMMC as boot device, then provide a pull down for this strap to disable SPI.

Note: The default for A0 will be eSPI due to a bug on LPC.

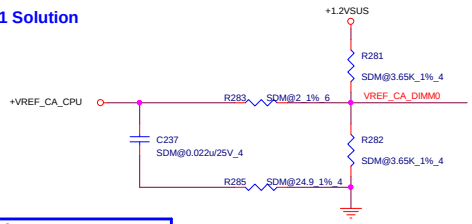
Hardware Strap	Strap Description	Value
GPIO_174	VDD2 1.24V vs.1.20V select 0 = 1.2V(default) 1 = 1.24V	1
GPIO_61	Enable CSE(TXE3.0) ROM Bypass 0 = Disable bypass 1 = Enable Bypass	0
GPIO_27	Allow eMMC as a boot source 0 = Disable 1 = Enable	0
GPIO_28	Allow SPI as a boot source 0 = Disable 1 = Enable	1
GPIO_65	Force DNX FW Load 0 = Do not force 1 = Force	0
GPIO_163	SMBus 1.8V/3.3V mode select 0=buffers set to 3.3V 1=buffers set to 1.8V	0
AZ_CODEC_SDIN0	PMU 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode	0
GPIO_66	LPC No Re-Boot 0 = Disable (default) 1 = Enable	0
GPIO_83	LPC 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode	0
		0
GPIO_172	SMbus No Re-Boot 0 = Disable (default) 1 = Enable	0
GPIO_42	Top swap override 0 = Disable 1 = Enable	0
GPIO_175	eSPI vs. LPC 0 = LPC mode (default) 1 = eSPI mode	0
CNVI_BRI_DT	eSPI Flash Sharing Mode: 0 = master attached flash sharing (MAFS; default) 1 = slave attached flash sharing (SAFS)	0
GPIO_84	Allow SPI as a boot source 0 = Enable (default) 1 = Disable	0

P/N and F/P



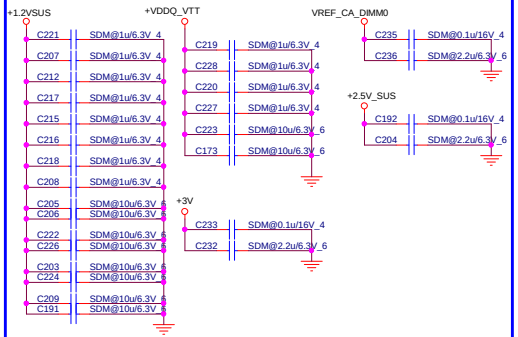
12/21 Change JDIM2 footprint to "ddr4-d4as0-26001-1p52-std-smt " for SMT requset

VREF DQ0 M1 Solution



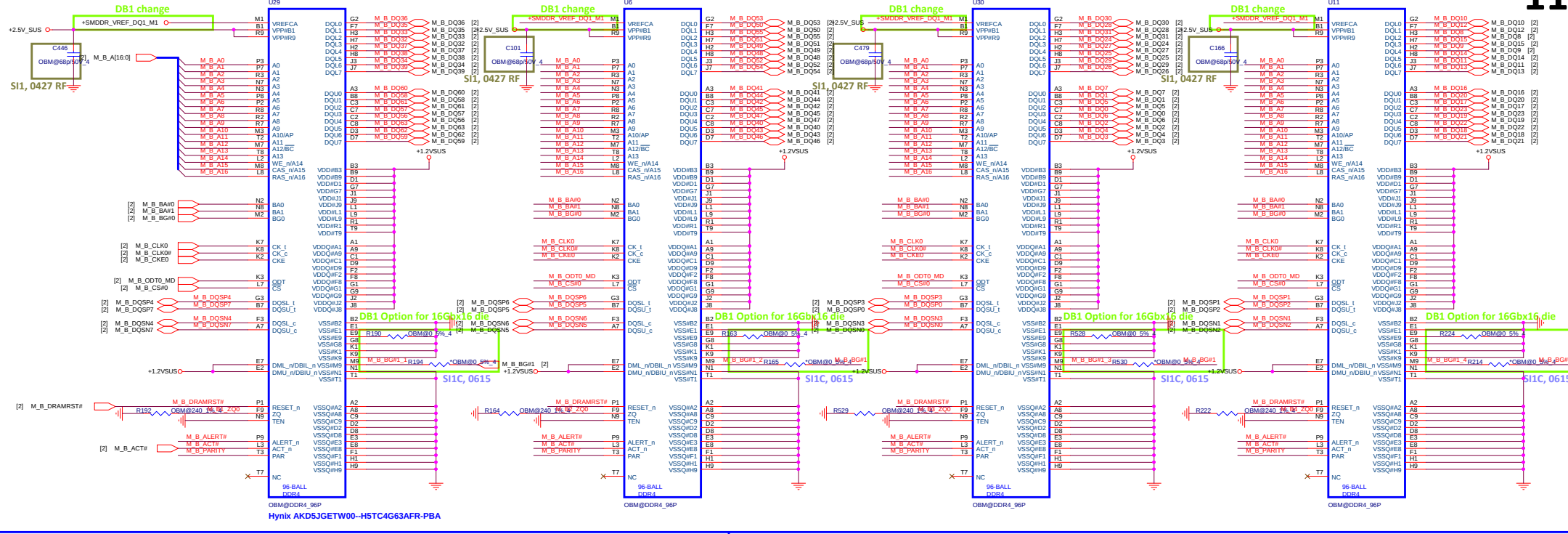
Place these Caps near So-Dimm1.

1uF/10uF 4pcs on each side of connector



[11,26] +2.5V_SUS
[7,11,26] +1.2VSUS
[11,26] +VDDQ_VTT
[2] +VREF_CA_CPU
[3,4,5,6,13,14,15,16,17,18,19,22,24,25,26,27,28,29,30] +3V

Quanta Computer Inc.		
PROJECT : Z8G		
Size	Document Number: DDR4 DIMM-STD 4H (CH. A)	Rev: 1A
Date: Tuesday, December 26, 2017	Sheet 10 of 35	



Vendor	P/N	Vendor P/N
MIC 16G	AKD5EG0TL00	MT40A1G16HBA-083E:A
Elpida		
SAMSUNG		

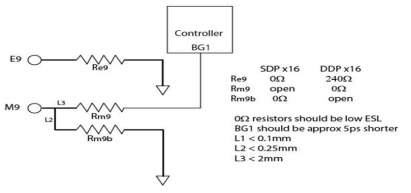
DB1 12/11, close memory

DB1 Option for 16Gbx16 die
Close DDR ball

DG 0.5 7/12, close T routing

DB1 12/11, close memory

Memory 8G & Memory 16G TABLE		
	Memory 8G	Memory 16G
R278	0Ω CS00002JB38	240Ω CS12402FB03
R279	0Ω CS00002JB38	240Ω CS12402FB03
R280	0Ω CS00002JB38	240Ω CS12402FB03
R281	0Ω CS00002JB38	240Ω CS12402FB03
R282	UNINSTAL	INSTAL
R283	UNINSTAL	INSTAL
R284	UNINSTAL	INSTAL
R285	UNINSTAL	INSTAL
R290	INSTAL	UNINSTAL
R291	INSTAL	UNINSTAL
R292	INSTAL	UNINSTAL
R293	INSTAL	UNINSTAL



Place these Caps near Channel B

1uF/10uF 4pcs on each side of connector

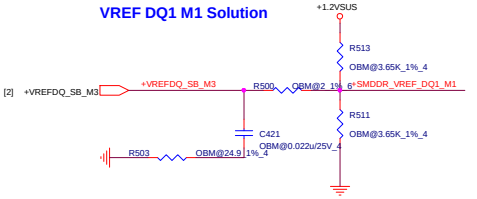
SI1, 0421 add

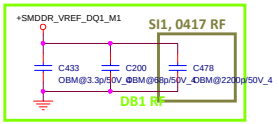
DB1 Intel

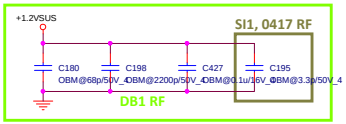
SI1B, 0603

DB1 Intel

VREF DQ1 M1 Solution







Quanta Computer Inc.		
PROJECT : Z8G		
Size	Document Number: DDR4 Memory Down (CH. B)	Rev 1A
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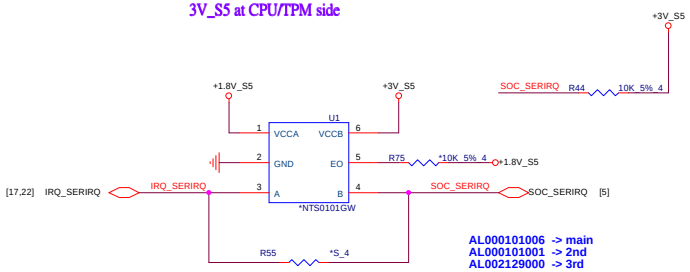
SERIRQ

SERIRQ is 1.8V_S5 at EC side but
3V_S5 at CPU/TPM side

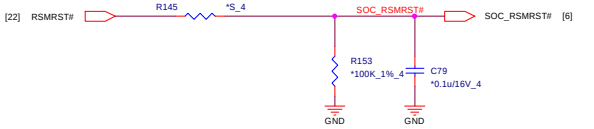


AL000101006 -> main
AL000101001 -> 2nd
AL002129000 -> 3rd

[3,6,7,15,16,17,18,19,21,22,24,26,29] +3V_S5
[3,4,5,6,7,16,19,23,27,29] +1.8V_S5
[3,4,5,6,10,13,14,15,16,17,18,19,22,24,25,26,27,28,29,30] +3V

RSMRST#

CPU IO is 3.3V



Quanta Computer Inc.
PROJECT : Z8G

Size	Document Number	Rev
	Level shift/Thermistor	1A
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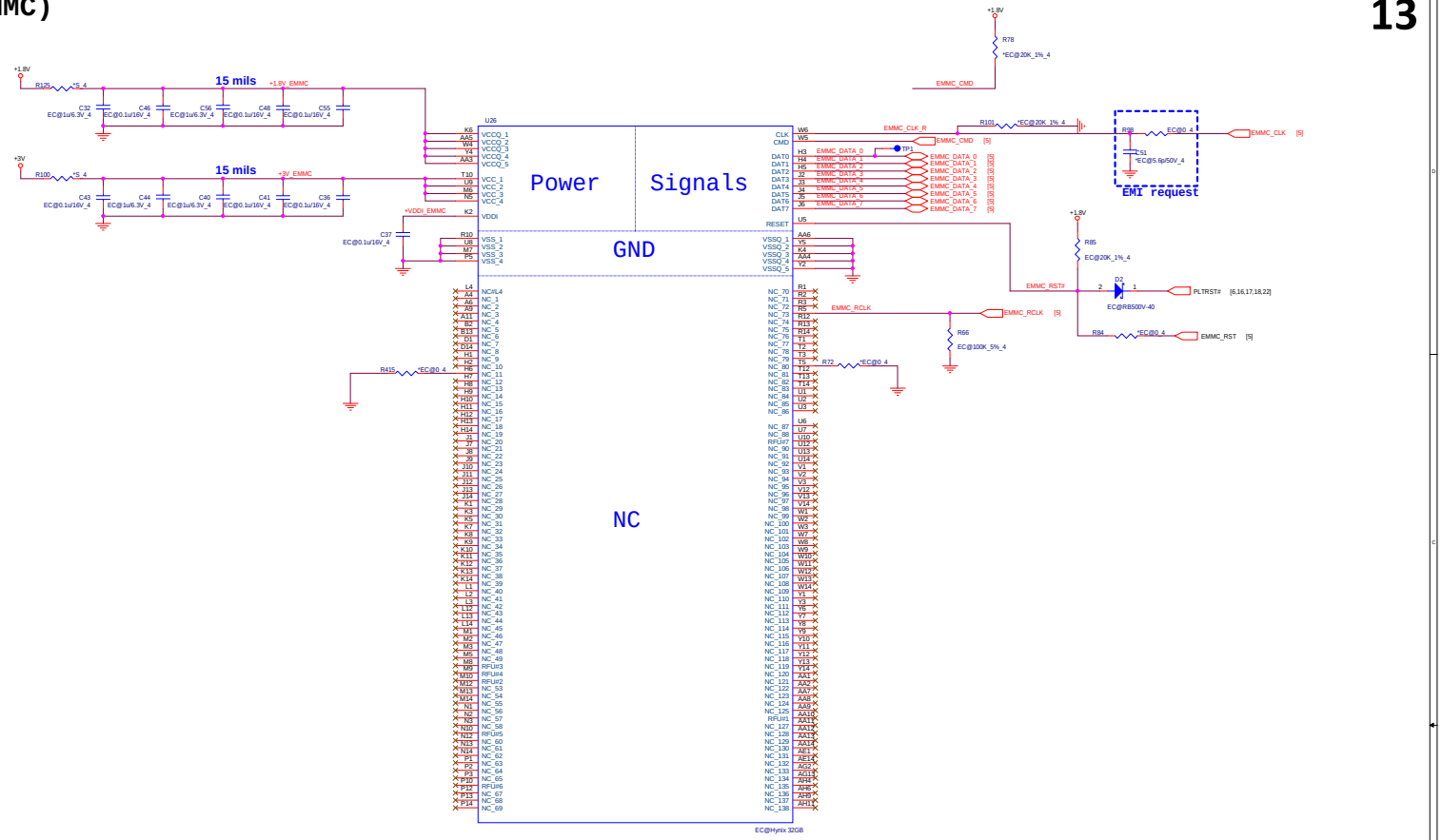
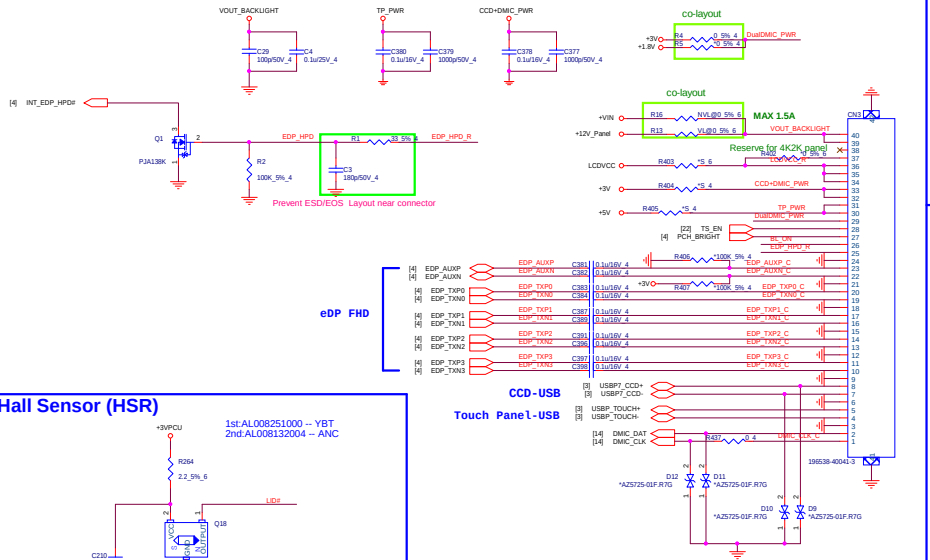
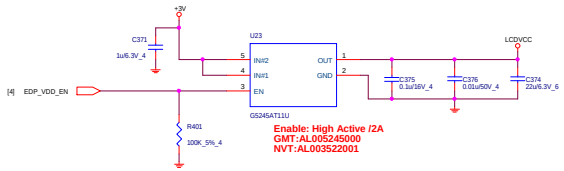
eMMC (MMC)



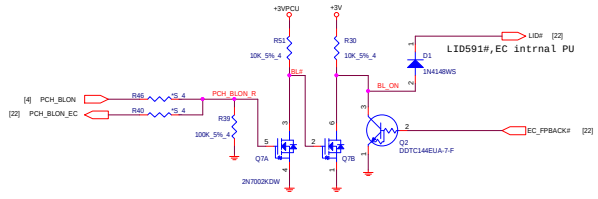
eDP CONNECTOR (LDS)



eDP Power (LDS)



eDP Backlight (LDS)



Hall Sensor (HSR)

Quanta Computer Inc.			
PROJECT : Z86			
Size	Document Number	eDP/ CCD/eMMC	Rev 1A
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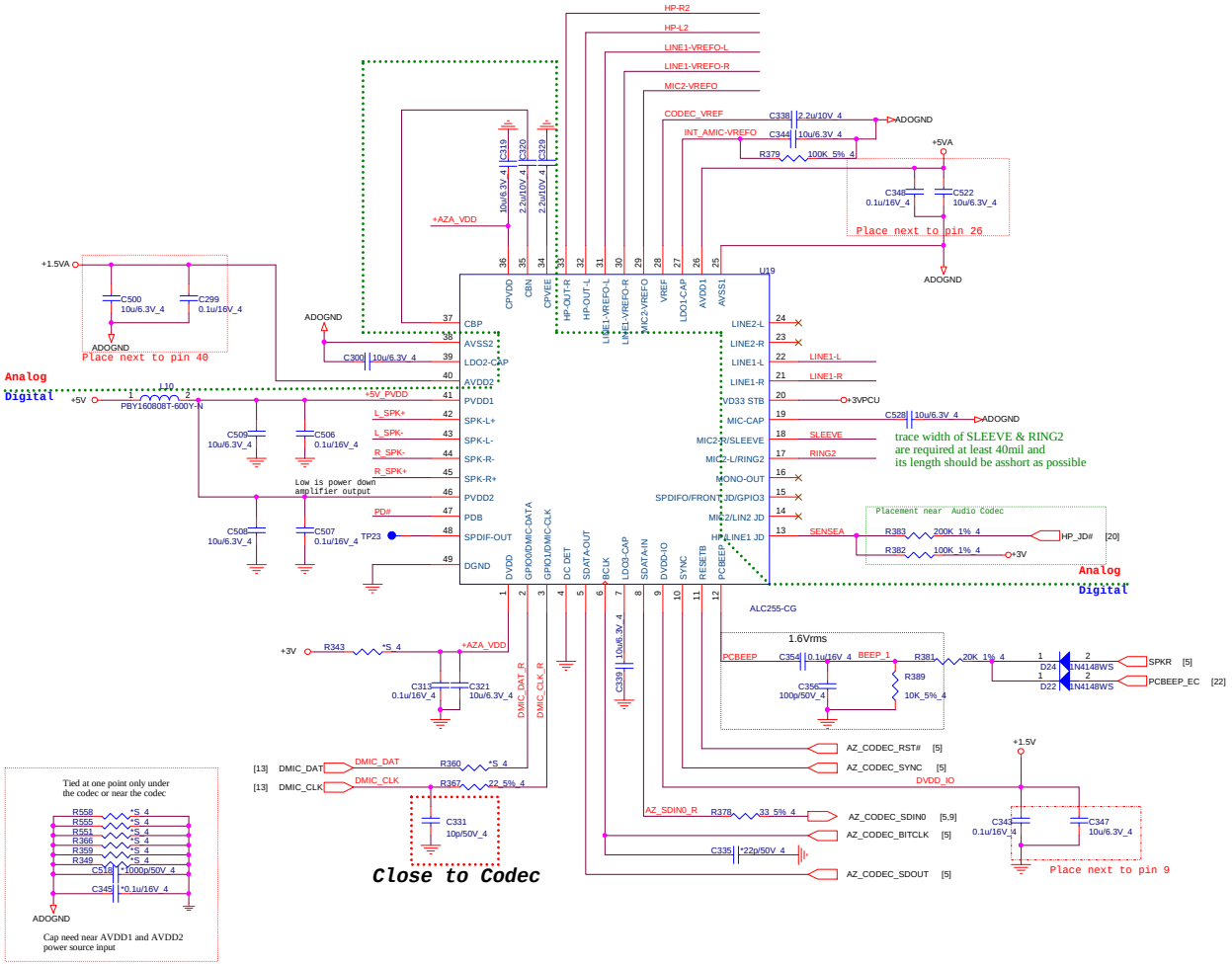
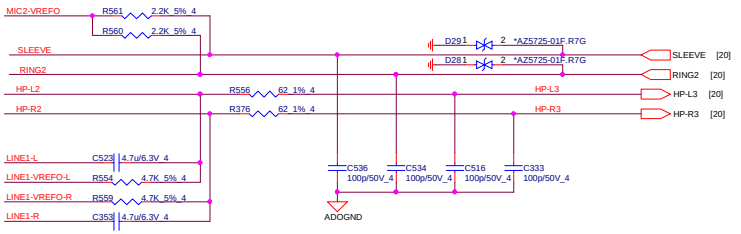
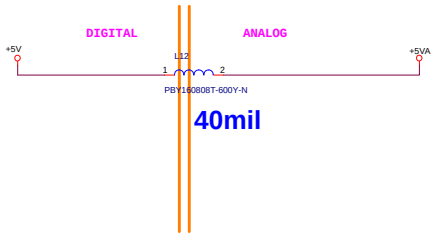
Codec(ADO)



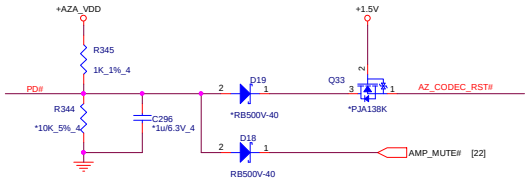
Universal Audio Jack HEADPHONE/MIC/LINE combo (ADO)



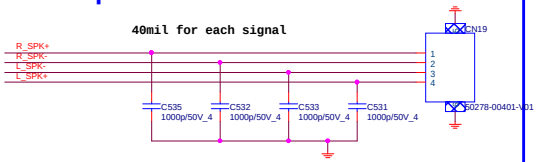
Codec PWR 5V(ADO)



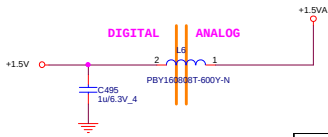
Mute(ADO)



Internal Speaker



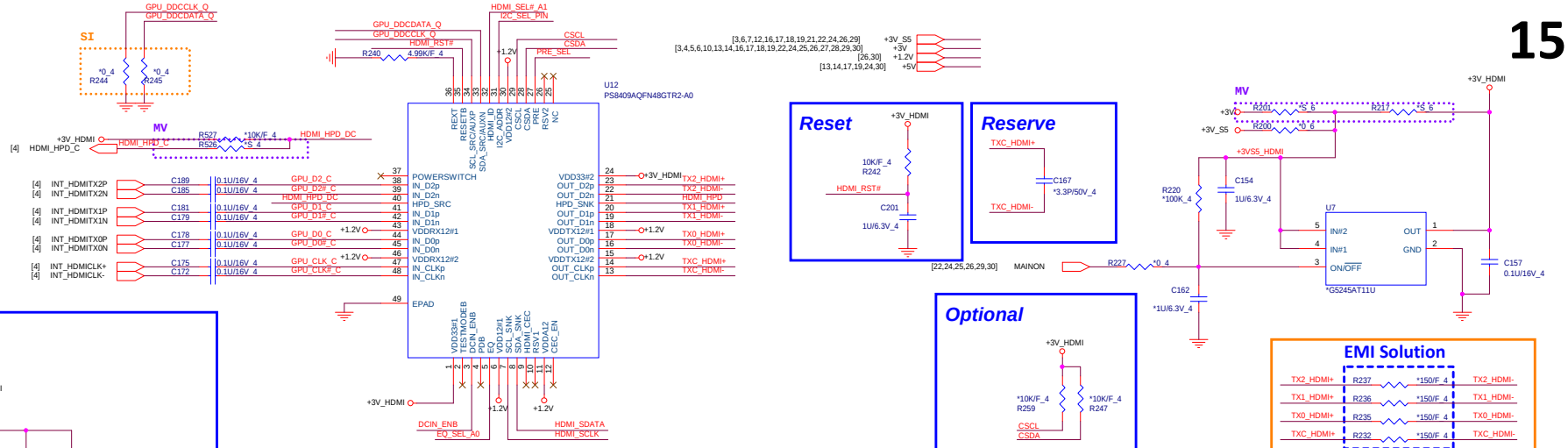
Codec PWR 1.5V(ADO)



Quanta Computer Inc.
PROJECT : Z86

Size	Document Number	Rev
	Audio Codec/HP/SPK/AMIC	1A
Date: Tuesday, December 26, 2017	Sheet 14 of 35	

From CPU



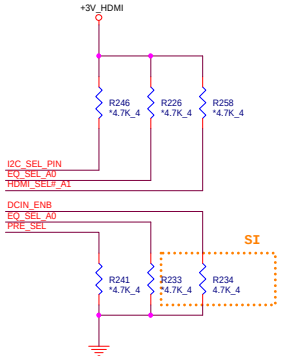
Reset

Reserve

Optional

EMI Solution

PS8409 strap pin



DCIN_ENB
DC coupling enable; Internal pull up, 3.3V I/O.
L: DC coupling input
H: Default,AC coupling input

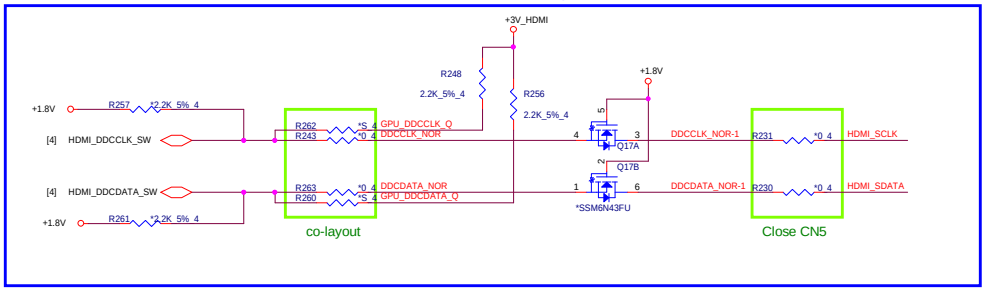
EQ_SEL_A0
Receiver equalization setting; Internal pull up , 3.3V I/O.
L: Compensaton for channel loss up to 13dB
H: Default , Compensation for channel loss up to 17dB
M: Compensation for channel loss up to 11dB

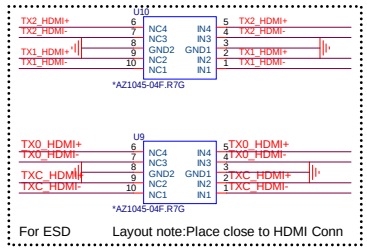
PRE_SEL
Output pre-emphasis setting; Internal pull up, 3.3V I/O.
L: Pre-emphasis =2.5dB
H: Default, No Pre-emphasis

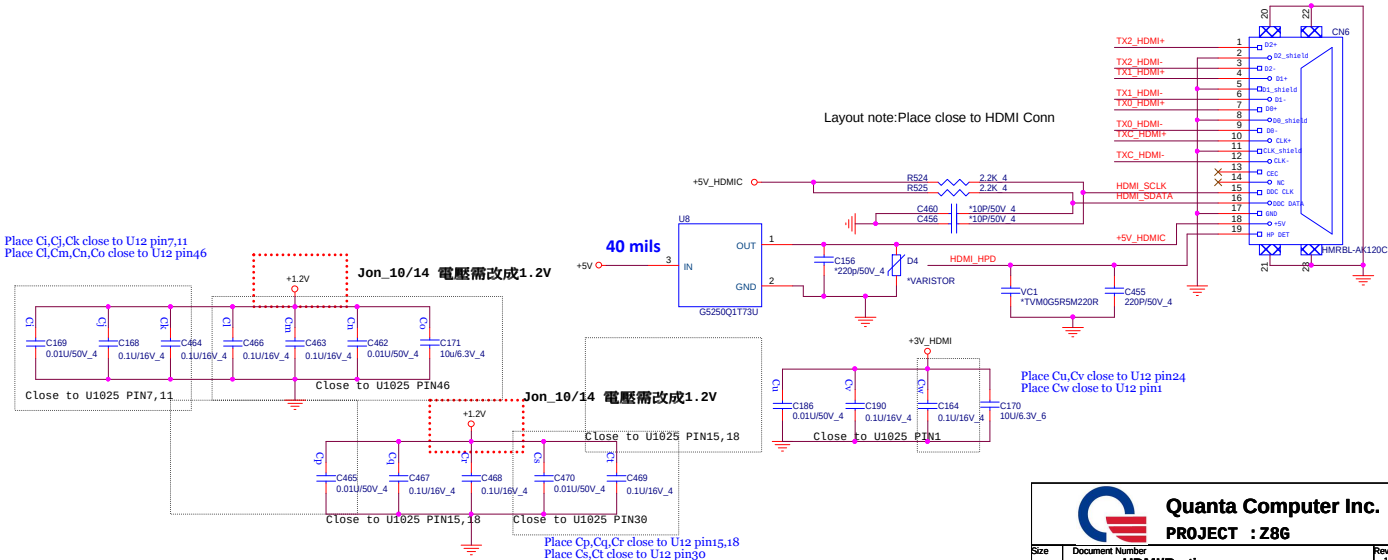
HDMI_SEL#_A1
HDMI_ID enable ; Internal pull down , 3.3V I/O.
L: Default, HDMI ID enable
H: HDMI ID disable

I2C_SEL_PIN
I2C Slave Address selection; Internal pull down, 3.3V I/O.
L: Default, Slave address 0x10-0x2F.
H: Alternative salve address 0x90-0x9F, 0xD0-0xDF.

Prevent current leakage when GPU is power off
add R12317/R1231 is for HMDI verify





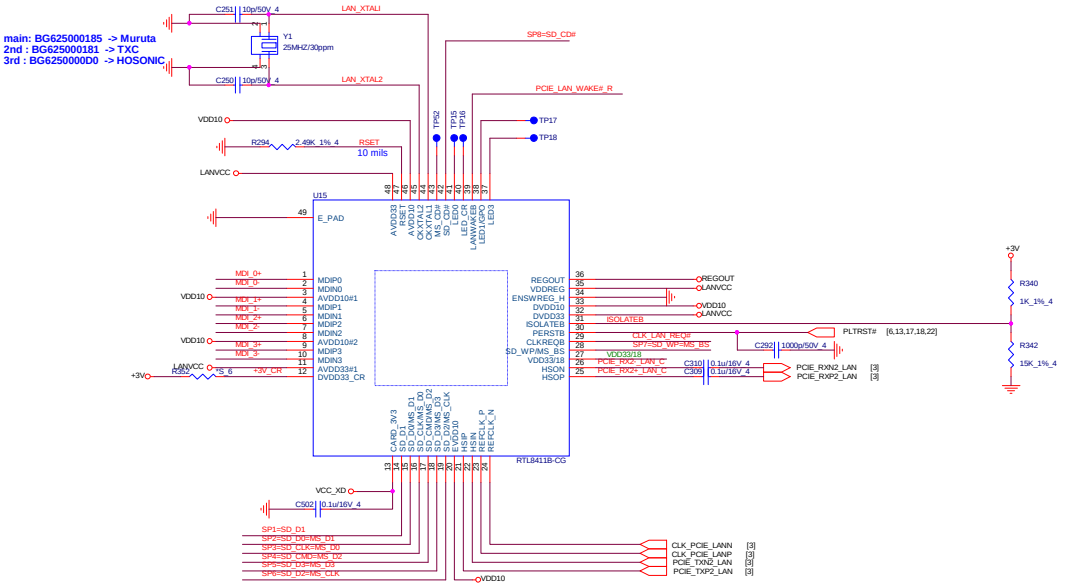


Quanta Computer Inc.
PROJECT : Z8G

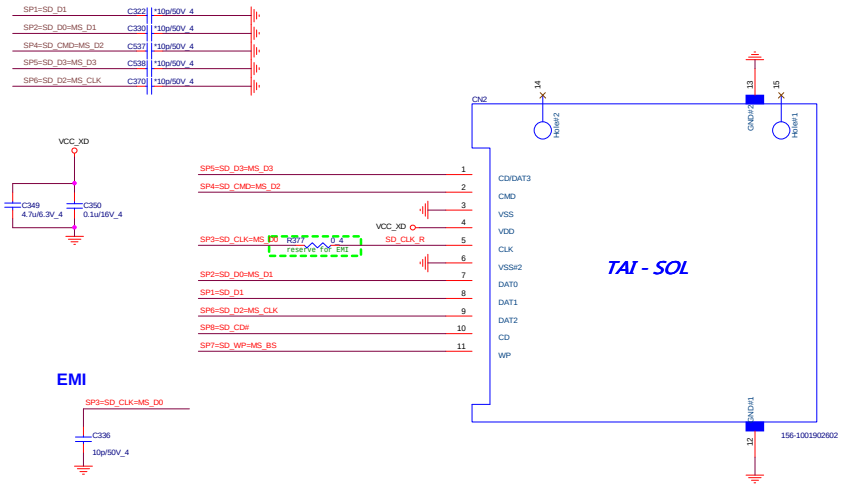
Size	Document Number	Rev
	HDMI/Re-timer	1A
Date: Tuesday, December 26, 2017	Sheet 15 of 35	

LAN & Card reader Combo (LAN)

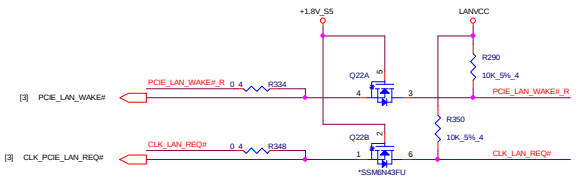
main: BG6250001B5 -> Muruta
2nd : BG6250001B1 -> TXC
3rd : BG6250000D0 -> HOSONIC

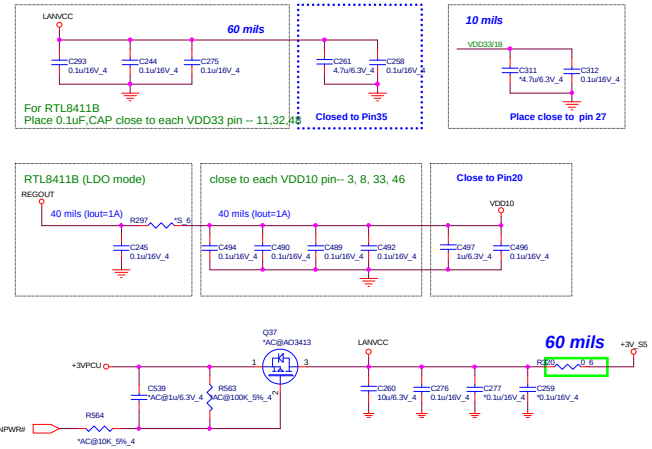


Card Reader (CRD)

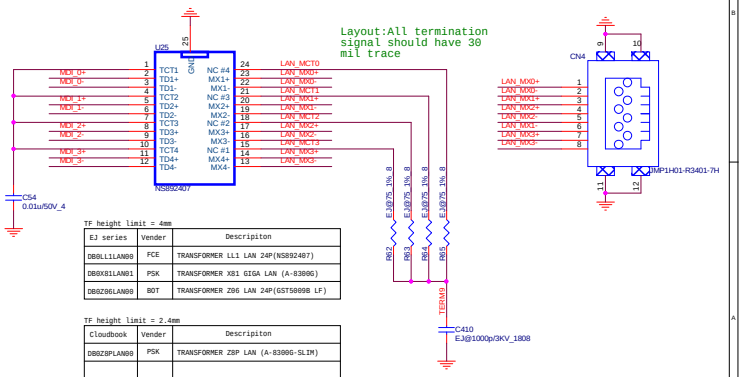


WAKE#/REQ# circuit(LAN)



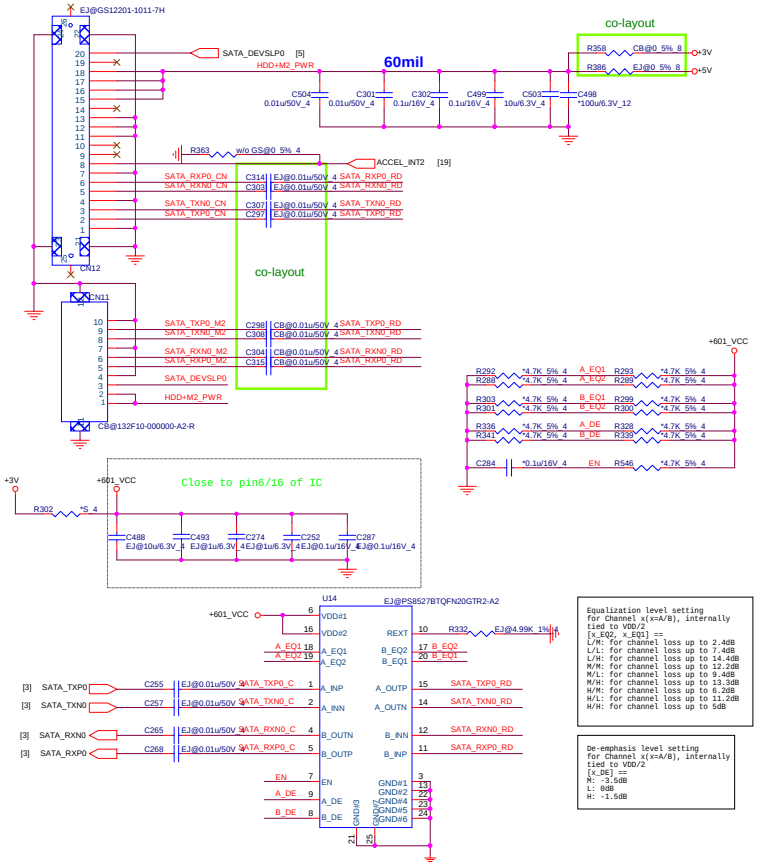


Tramsformer

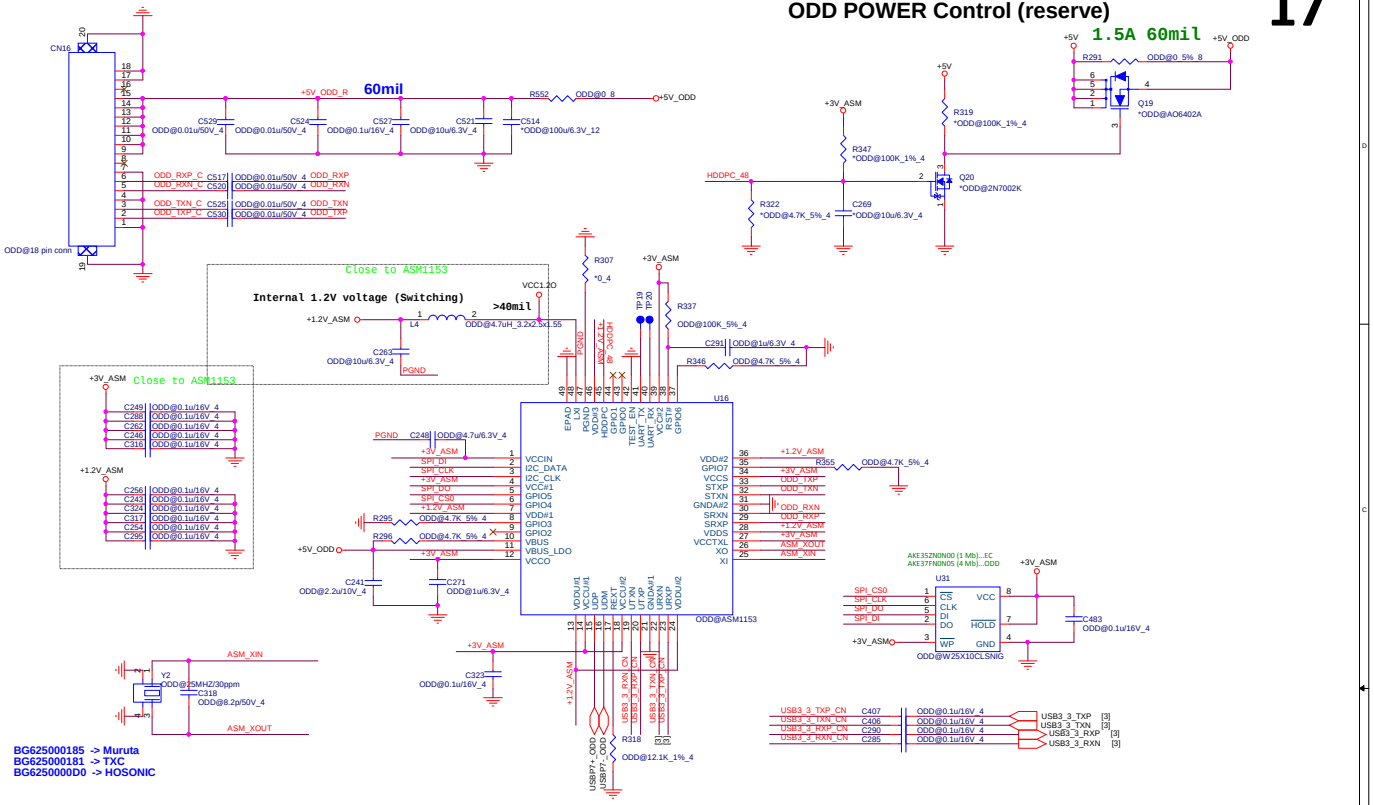


Quanta Computer Inc.
PROJECT : Z8G
Size | Document Number | Rev
LAN/CRD COMBO - RTL8411B | 1A
Date: Tuesday, December 26, 2017 | Sheet 16 of 35

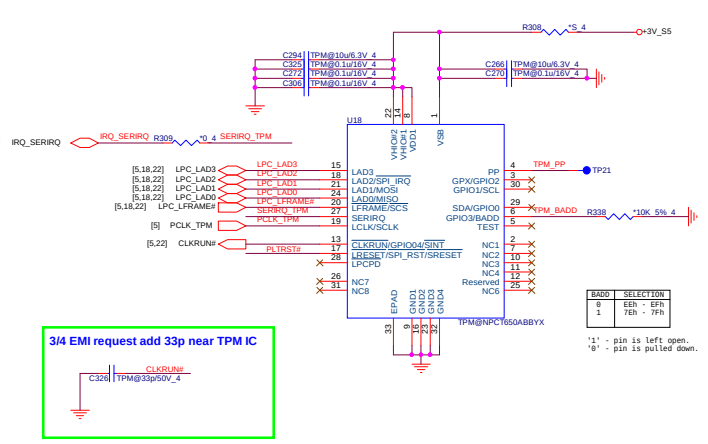
2.5" SATA HDD (HDD)



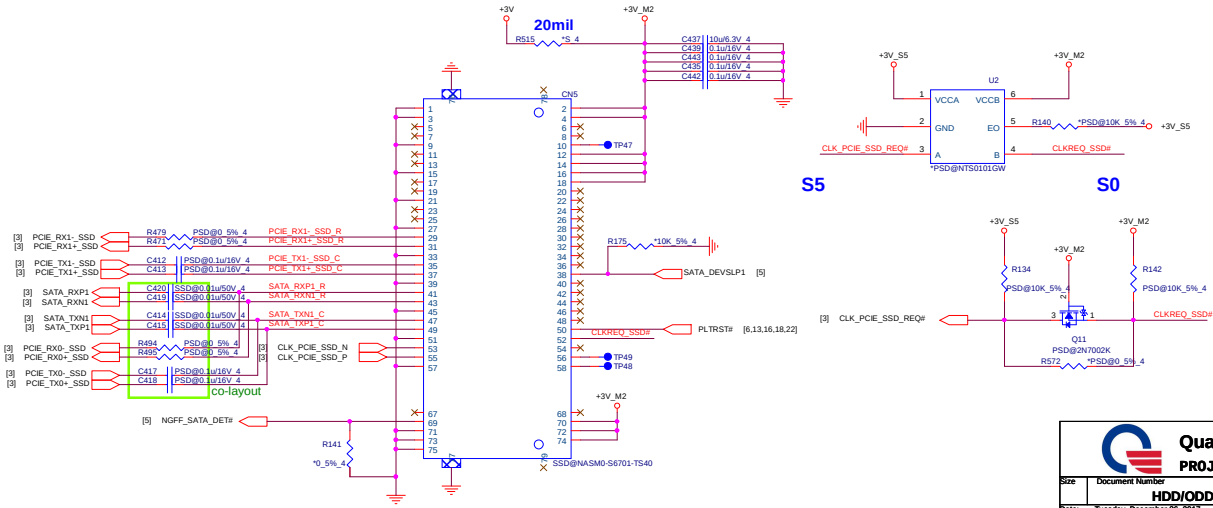
USB ODD Bridge (ODD)



TPM NPCT650 (TPM)



M.2 PCPIE & SATA SSD (NGF)

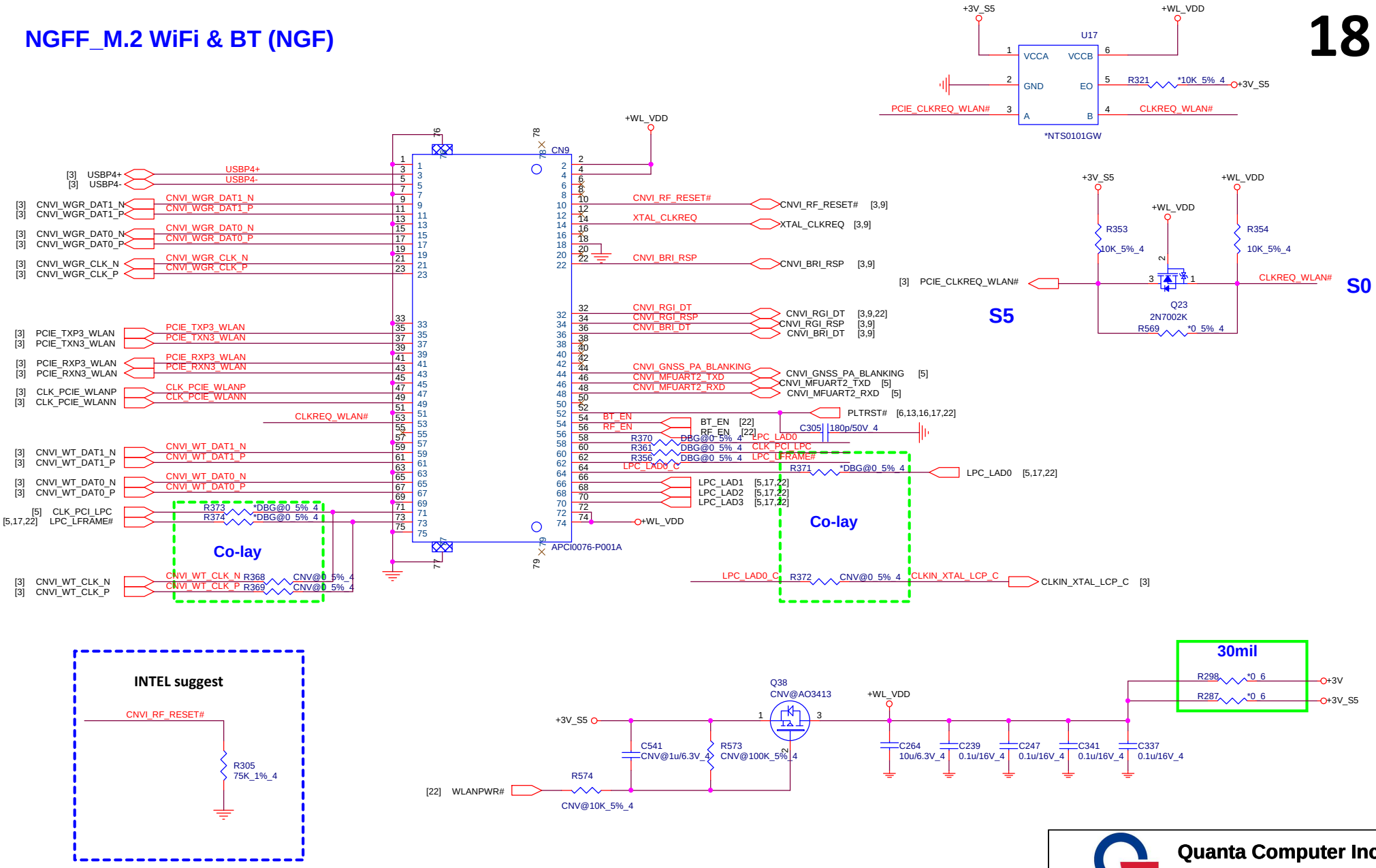


Quanta Computer Inc.
PROJECT : Z8G

Size	Document Number	Rev
	HDD/ODD/TPM NPCT650/Hole	1A

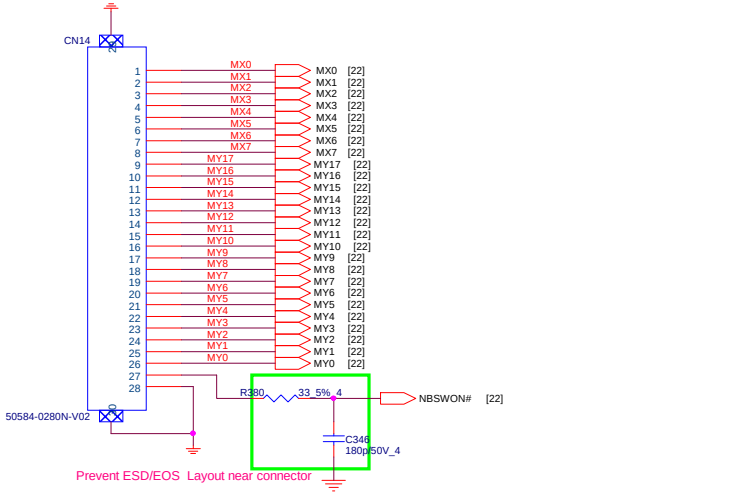
Date: Tuesday, December 26, 2017 Sheet 17 of 35

NGFF_M.2 WiFi & BT (NGF)



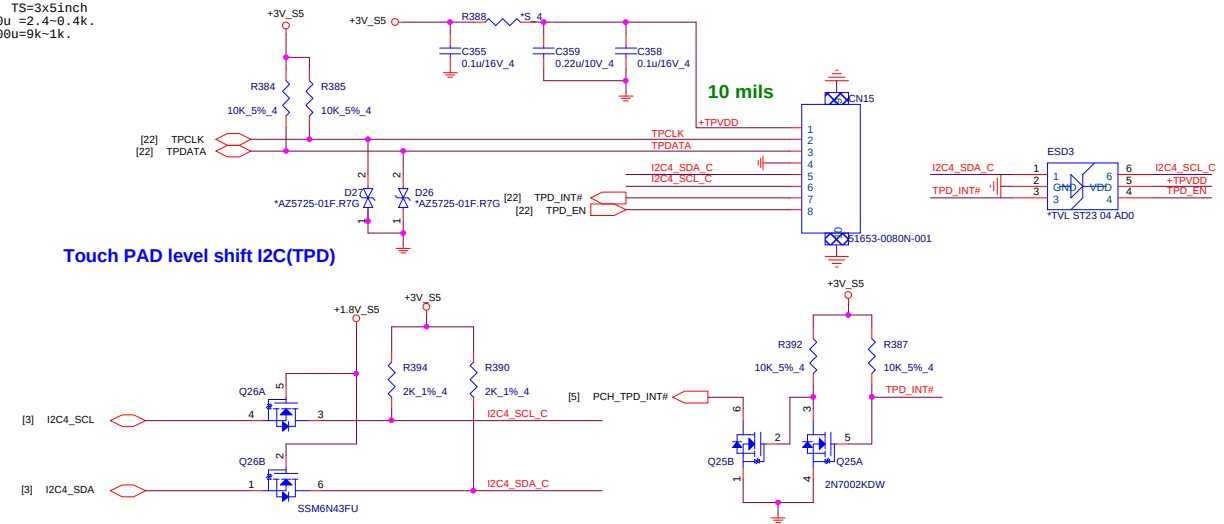
Quanta Computer Inc.		
PROJECT : Z8G		
Size	Document Number: NGFF WiFi & BT	Rev: 1A
Date: Tuesday, December 26, 2017	Sheet 18 of 35	

KEYBOARD (KBC)

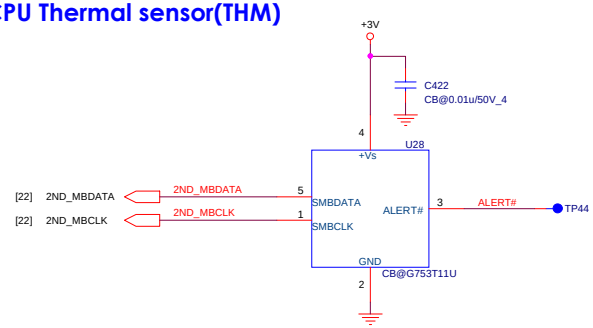


TOUCHPAD (TPD I2C/PS2 co-lay)

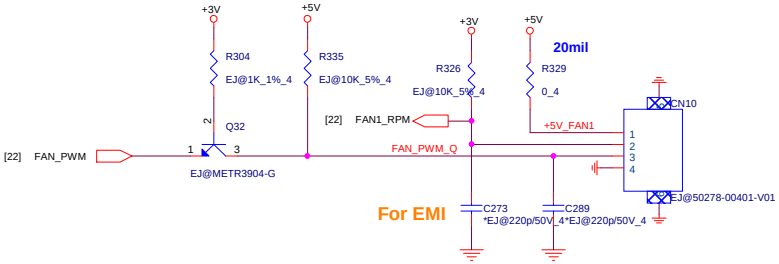
TPD->100kHz,TS=400Khz
Intel design guide suggestion
MCP PIN 10u.
Per inch 3u TS=3x5inch
400kHz10~100u =2.4~0.4k.
100Khz 10~100u=9k~1k.



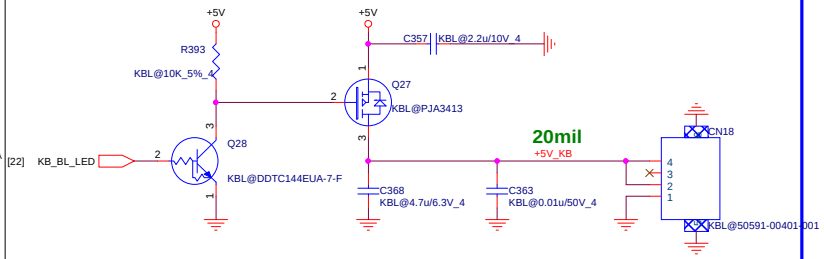
CPU Thermal sensor(THM)



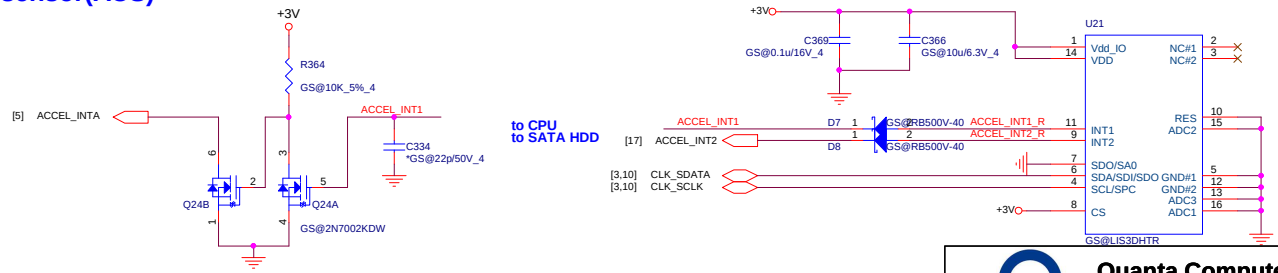
CPU FAN (THM)



Keyboard backlight (KBL)



G-sensor(ACS)

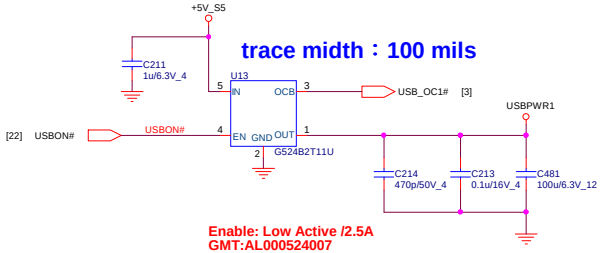


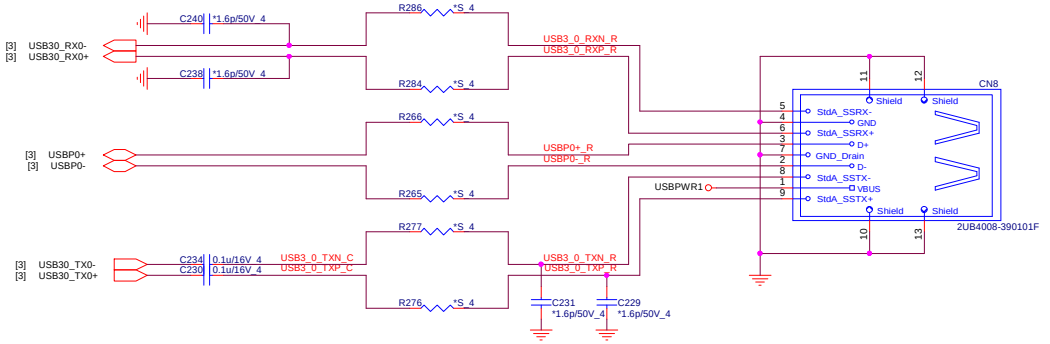
Quanta Computer Inc.
PROJECT : Z8G

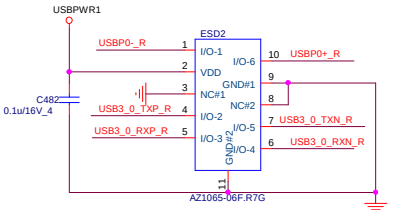
Size	Document Number	Rev
	KB/TP/FAN/G-sensor	1A

Date: Tuesday, December 26, 2017 Sheet 19 of 35

USB 3.0 (UB3)

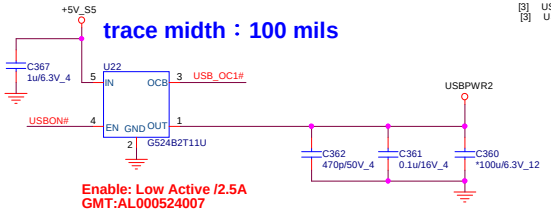


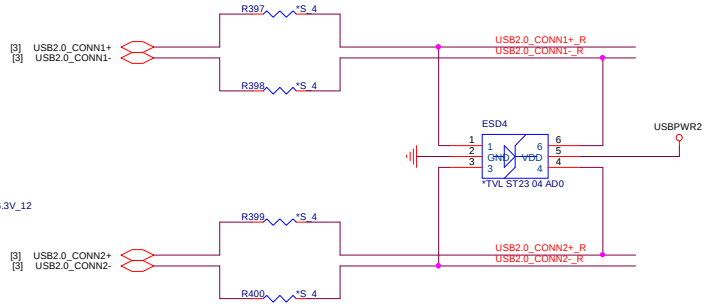




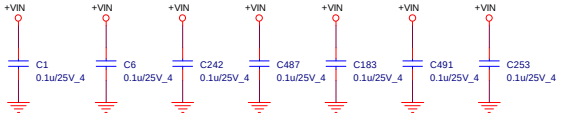
USB protection diodes for ESD.
as close as possible to USB connector pins.

USB 2.0 (UB2)

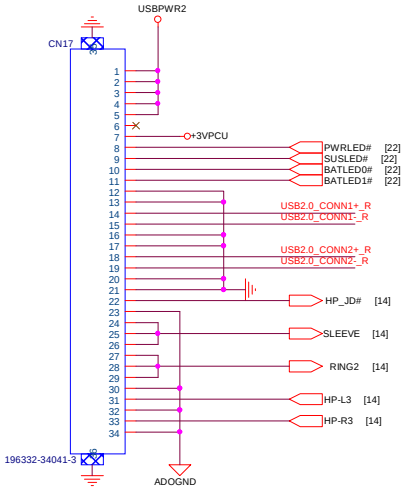




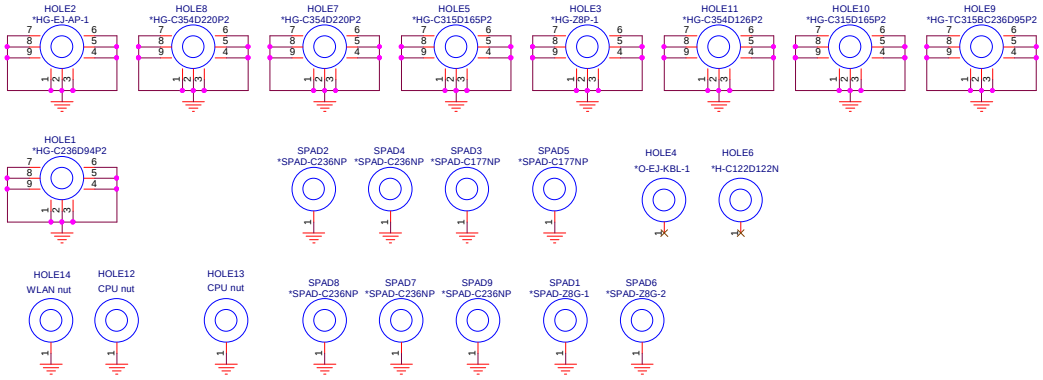
Stitch cap (EMC)



USB 2.0/LED/AUDIO JACK DB (UB2)



HOLE(OTH)



	P/N	Description
CPU Nut	MBZ8P001010	SMT NUT M2 H1.9 Z8P(MBZ8P001,3A)COPPER
WL M.2 Nut for CB	MBZ8P002010	SMT NUT M2 H0.45 Z8P(MBZ8P002,3A)COPPER
WL M.2 Nut for EJ	MBZ8P003010	SMT NUT M2 H2.45 Z8P(MBZ8P003,3A)COPPER

Quanta Computer Inc.
PROJECT : Z8G

Size	Document Number	Rev
	USB/CARDREADER/LED	1A
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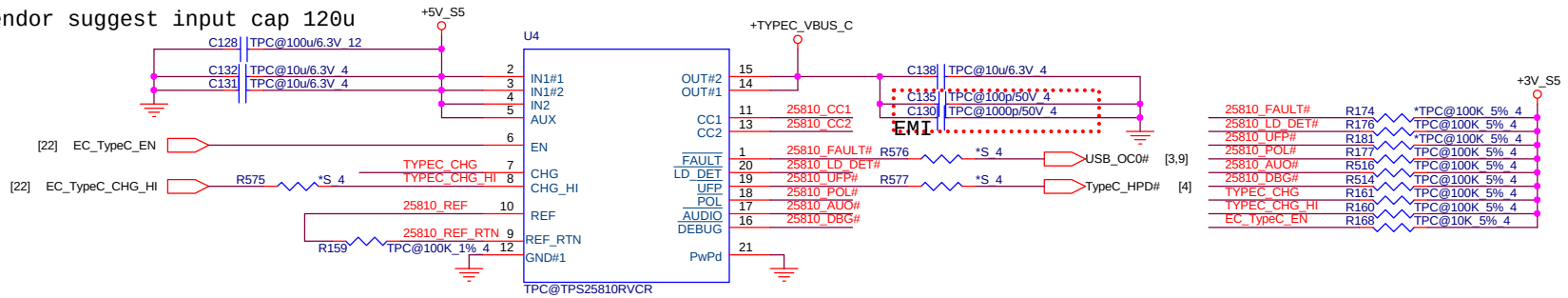
USB TYPE-C (UTC)

trace midth：150 mils

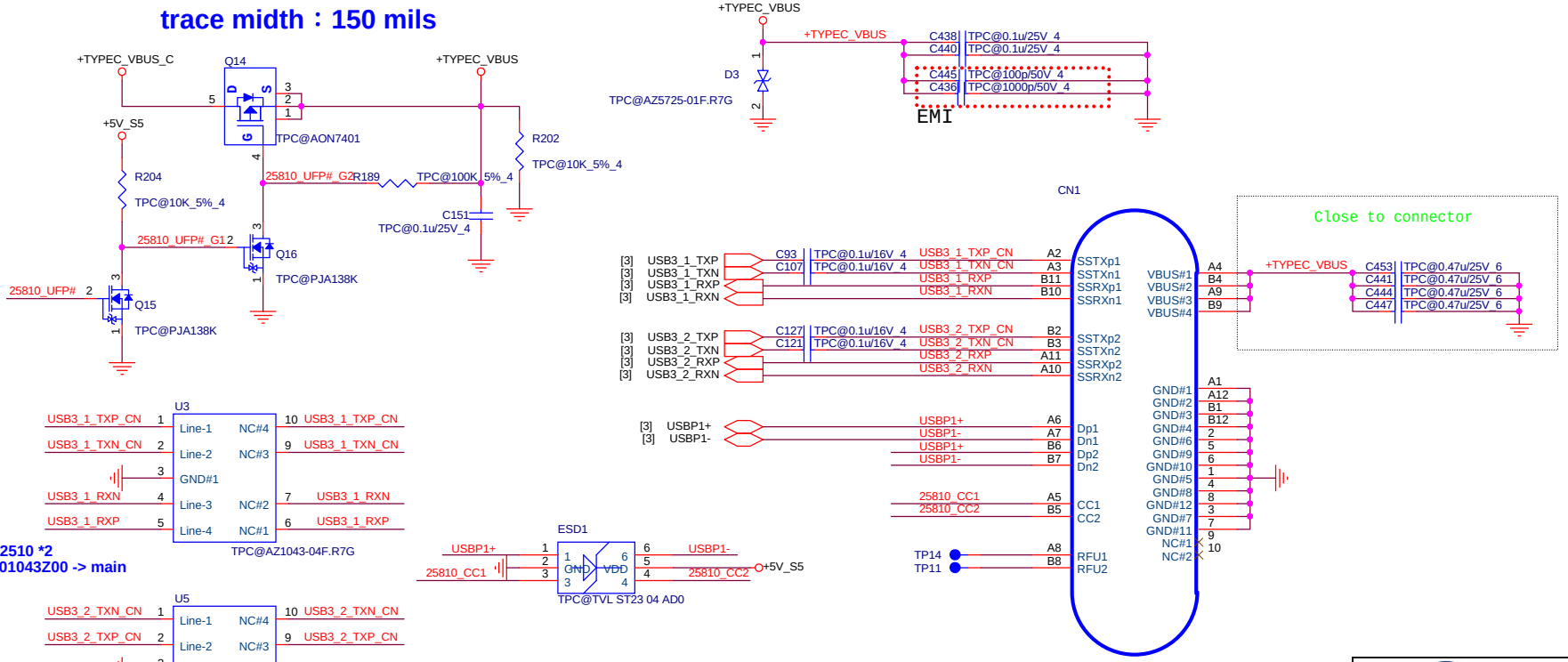
Vendor suggest input cap 120u



TPS25810 Port	CC1	CC2	TPS25810 Response					
			OUT	VCONN On CC1 or CC2	POLb	UFPb	AUDIOb	DEBUGb
Nothing Attached	OPEN	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
UFP Connected	Rd	OPEN	IN1	NO	Hi-Z	LOW	Hi-Z	Hi-Z
UFP Connected	OPEN	Rd	IN1	NO	LOW	LOW	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	OPEN	Ra	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	Ra	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Rd	Ra	IN1	CC2	Hi-Z	LOW	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Ra	Rd	IN1	CC1	LOW	LOW	Hi-Z	Hi-Z
Debug Accessory Connected	Rd	Rd	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	LOW
Audio Adapter Accessory Connected	Ra	Ra	OPEN	NO	Hi-Z	Hi-Z	LOW	Hi-Z

CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A

trace midth：150 mils



Quanta Computer Inc.

PROJECT ：Z8G

Size	Document Number	Rev
	USB_Type C_25810	1A
Date: Tuesday, December 26, 2017	Sheet 21 of 35	

EC(KBC)

+3VPCU_EC and +3V_RTC minimum trace width 12mils.

12 mils

(For PLL Power)

IT8987

LPC

GPIO

PS/2

SM_BUS

UART

FLASH

PWM

KBMX

WAKE UP

A/D D/A

CLOCK

Pin124 is a board ID for Cloud book (PD) , EC has internal PU for EJ series

Prevent ESD/EOS Layout near EC

Prevent ESD/EOS Layout near device

colsed to EC pin within 100 mils

Output for type-c Apling ridge
reset timming"Low " Active

SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	Thermal sensor
SM Bus 3	
SM Bus 4	

PU/PD (KBC)

Battery Disable (FSW)

Reserve power on switch for test (MP remove)

SPI ROM(KBC)

SPI ROM	Vender	Size	Quanta P/N	Vender P/N
3.3V	WND	128K	AKE35ZN0N00	W25X10CLSNIG
	GGD	128K	AKE5BY00000	GD25D10BTIGR
	MAX	128K	AKE35FN0Z02	MX25L1006EMI-10G

Power_Auto_Recovery

15 mils

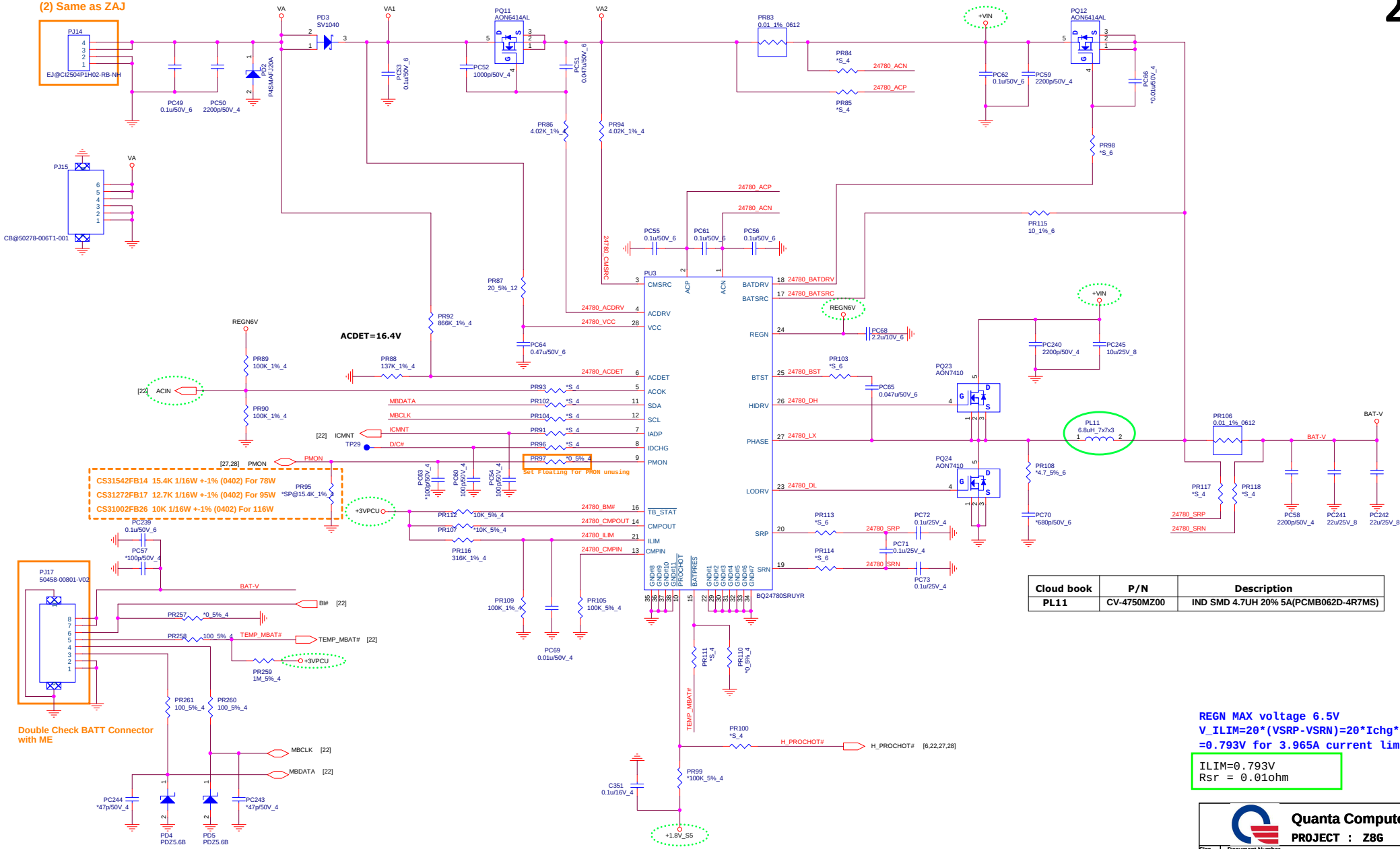
20 mils

HWPG(KBC)

Quanta Computer Inc.
PROJECT : Z8G
KBC IT8987E_BX
Rev 1A
Date: Tuesday, December 26, 2017 Sheet 22 of 35

(1) Double Check ADP-IN Connector with ME

(2) Same as ZAJ



Cloud book	P/N	Description
PL11	CV-4750MZ00	IND SMD 4.7UH 20% 5A(PCMB062D-4R7MS)

REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit

ILIM=0.793V
Rsr = 0.01ohm

Quanta Computer Inc.
PROJECT : Z8G

Size	Document Number	Rev
	Charger (BQ24780S)	1A

Date: Tuesday, December 26, 2017 Sheet 23 of 35

+VIN [13,20,23,25,26,27,28,30,31]
+3VPCU [6,13,14,16,20,22,23,29]
+5VPCU [25,29]
VL [30]

+5V [13,14,15,17,19,30]
+5V_S5 [6,20,21,26,27,28,31]
+3V [3,4,5,6,10,13,14,15,16,17,18,19,22,25,26,27,28,29,30]
+3V_S5 [3,6,7,12,15,16,17,18,19,21,22,26,29]

+3VPCU
3.3 Volt +/- 5%
TDC : 6A
Width : 240mil
FSW : 500KHZ

TDC : 1A
PEAK : 1.33A
Width : 40mil

TDC : 3.66A
PEAK : 4.89A
Width : 160mil

Soft-Start

+5VPCU
5 Volt +/- 5%
TDC : 8A
Width : 320mil
FSW : 750KHZ

TDC : 5.25A
PEAK : 7A
Width : 240mil

TDC : 4A
PEAK : 5.3A
Width : 160mil

Soft-Start

Power Auto Recovery

To Thermal Protection

LDO=3.3V/100mA

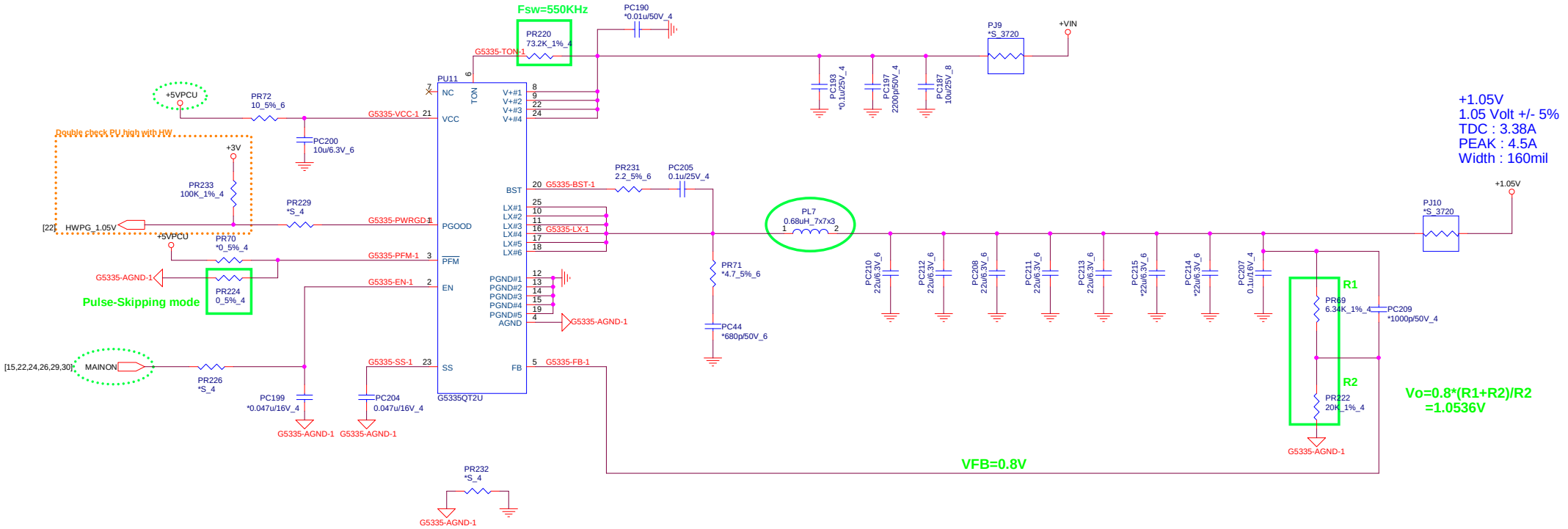
VCC=5V
(DON'T Connect to External Load)

LDO=5V/100mA

VCC=5V
(DON'T Connect to External Load)

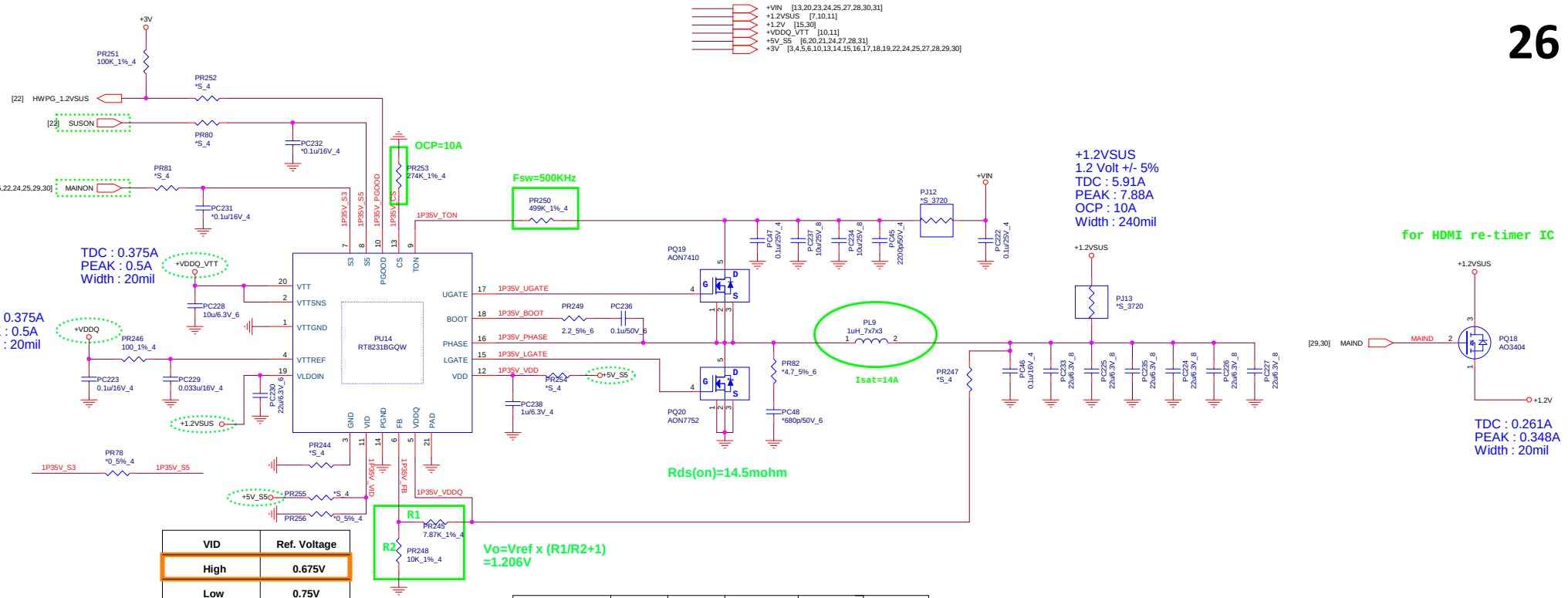
Quanta Computer Inc.			
PROJECT : Z8G			
Size	Document Number		Rev
	SYSTEM 5V/3V (RT6256B/RT6258C)		1A
Date: Tuesday, December 26, 2017	Sheet 24 of 35		

+VIN [13,20,23,24,26,27,28,30,31]
+1.05V [6,7,27,28]
+5VPCU [24,29]
+3V [3,4,5,6,10,13,14,15,16,17,18,19,22,24,26,27,28,29,30]



+1.05V
1.05 Volt +/- 5%
TDC : 3.38A
PEAK : 4.5A
Width : 160mil

Quanta Computer Inc.		
PROJECT : Z8G		
Size	Document Number: +1.05V (G5335QT2U)	Rev: 1A
Date: Tuesday, December 26, 2017	Sheet 25 of 35	



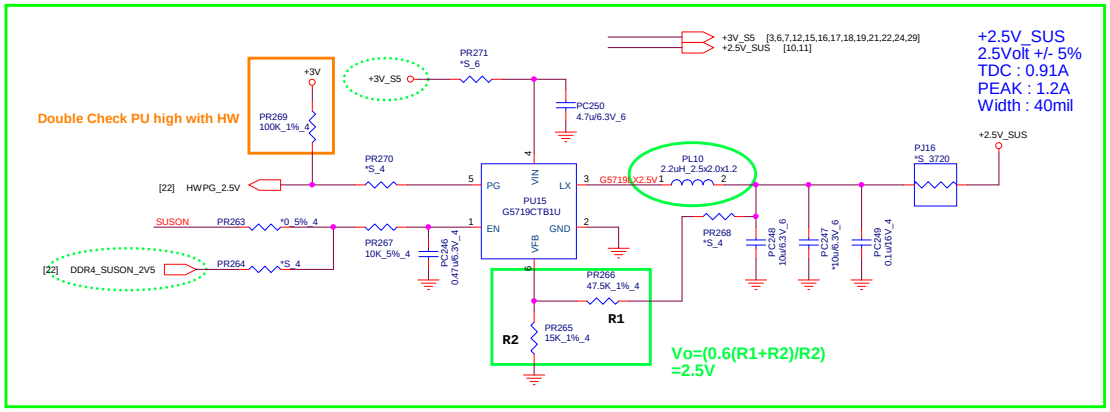
VID	Ref. Voltage
High	0.675V
Low	0.75V

OCP=10A
L ripple current
=(19-1.2)*1.2/(2.2u*500k*19)
=1.022A
Vtrip=10-(1.022/2)*14.5mohm
=137.59mV
Rlimit=137.59mV/5uA*10=275.18Kohm

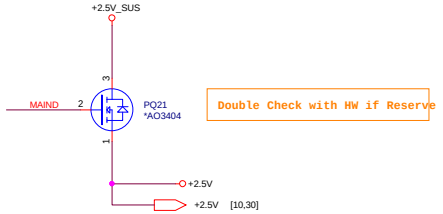
DDR=1.2V
R1=7.87K/F_4
R2=10K/F_4

	S3	S5	VDDQ	VTTREF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

+2.5VSUS Power Rail For DDR4

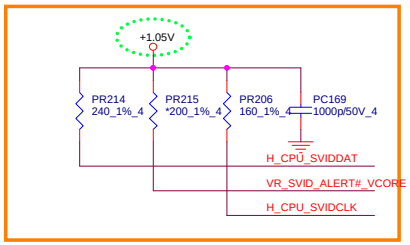


Reserve +2.5V for DDR4 VDDSPD



Quanta Computer Inc.		
PROJECT : Z8G		
Size	Document Number: DDR4 (RT8231BGQW)	Rev: 1A
Date: Tuesday, December 26, 2017	Sheet 26 of 35	

SVID_CLK : UP:160 ohm Series:95 ohm
SVID_ALERT : UP:68 ohm Series:220 ohm
SVID_DATA : UP:240 ohm Series:20 ohm



Check SVID PU UP R/Series R with HW

Cloud book	P/N	Description
PR165	CS18062FB29	RES CHIP 806 1/16W +-1%(0402)
PR22	CS21002FB24	RES CHIP 1K 1/16W +-1% (0402)
PC8	CH4472K9B00	CAP CHIP 0.47UF 10V(+-10%,X5R,0402)

+VIN [13,20,23,24,25,26,28,30,31]
+VCC_VCCGI [7]
+3V [3,4,5,6,10,13,14,15,16,17,18,19,22,24,25,26,28,29,30]
+5V_S5 [6,20,21,24,26,28,31]
+1.8V_S5 [3,4,5,6,7,9,12,16,19,23,29]
+1.05V [6,7,25,28]

Check EN Sequence with HW

PU7 RT3601EAGQW

Isat=45A
DCR=0.66m ohm

Imax=26A

Vref=0.6V

FSW=550KHZ

B=4250
PUT COLSE TO VCCGI HOT SPOT

Place close with VCORE Inductor B=3650

Total 20pcs 22u_0603 (with HW)

Vset1	1425mV
Delta Vset1	901mV
Vset2	675mV
Delta Vset2	49.8mV
Vset3	974mV
Delta Vset3	950mV
VTsen	448mV

+VCCGI

Icc Max：25A
Icc TDC：18A
Vboot：0V
OCP：35A
Fsw：550KHZ

VCCGI L/L :
R_DC_LL：6mV/A
R_AC_LL：6mV/A

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	+VCC_VCCGI (RT3601EAGQW)	1A

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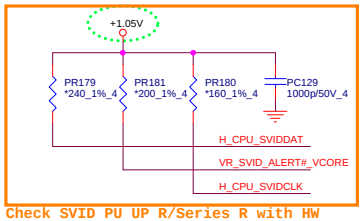
SVID_CLK : UP:160 ohm Series:95 ohm
SVID_ALERT : UP:68 ohm Series:220 ohm
SVID_DATA : UP:240 ohm Series:20 ohm

Cloud book	P/N	Description
PR123	CS14992FB24	RES CHIP 499 1/16W +-1%(0402)
PR4	CS11402FB19	RES CHIP 140 1/16W +-1%(0402)
PR5	CS12002FB25	RES CHIP 200 1/16W +-1%(0402)

+VIN [13,20,23,24,25,26,27,30,31]
+VNN [7]
+5V_S5 [6,20,21,24,26,27,31]
+1.05V [6,7,25,27]
+3V [3,4,5,6,10,13,14,15,16,17,18,19,22,24,25,26,27,29,30]



Check SVID PU UP R/Series R with HW

Check EN Sequence with HW

Vset1	124.9mV
Delta Vset1	899mV
Vset2	373.4mV
Delta Vset2	1.14V
Vset3	176mV
Delta Vset3	950mV
VTsen	548mV

+VNN

Icc Max：5.6A
Icc TDC：N/A
Vboot：1.05V
OCP：10A
Fsw：600KHZ

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	+VNN (RT3601EAGQW)	1A

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[6,13,14,16,20,22,23,24] +3VPCU
[3,4,5,6,7,9,12,16,19,23,27] +1.8V_S5
[7] +1.24V_S5
[3,4,13,15,30] +1.8V
[14] +1.5V

[3,6,7,12,15,16,17,18,19,21,22,24,26] +3V_S5
[24,25] +5VPCU
[3,4,5,6,10,13,14,15,16,17,18,19,22,24,25,26,27,28,30] +3V

+1.8V_S5
1.8Volt +/- 5%
TDC : 0.85A
PEAK : 1.13A
Width : 40mil

H cha _ pull up to 3 _

+3V_S5, +3VPCU
PR234 *S_6
PC220 4.7u/6.3V_4
PR238 100K_1%_4
PR239 *S_4
[22] HWPG_1.8V_S5
PU13 G5719CTB1U (PG, VIN, LX, EN, GND, VFB)
G5719LX_1.8V
PL8 2.2uH_2.5x2.0x1.2
[22,24,28] S5_ON
PR243 110K_1%_4
PC221 0.1u/16V_4
PR242 *S_4
PC218 10u/6.3V_6
PC217 *10u/6.3V_6
PC219 0.1u/16V_4
PJ11 *S_3720
+1.8V_S5
R1 PR241 30K_1%_4
R2 PR240 15K_1%_4

Check RC delay time with HW
(follow ZHP RC dealy time)

Vo=(0.6(R1+R2)/R2
=1.8V

[26,30] MAIND
MAIND
PQ7 AO3404
+1.8V_S5
+1.8V

TDC : 0.173A
PEAK : 0.23A
Width : 20mil

+1.24V_S5
1.24Volt +/- 5%
TDC : 1.875A
PEAK : 2.5A
Width : 80mil

h c Hi h u c with HW

+3V_S5
PR210 100K_1%_4
PR209 *S_4
[22] HWPG_1.24V_S5
5671PG_1.24V
+3VPCU
PJ4 *S_3720
PR54 10_5%_6
5671SVIN_1.24V
PC123 *2200p/50V_4
PR178 *2.2_5%_6
PU8 M5671RE1U (POK, VIN#1, VIN#2, VCC, GND, NC#1, SW#1, SW#2, NC#2, FB, EN)
PC150 0.01u/50V_4
PC141 10u/6.3V_6
PC156 1u/6.3V_4
5671LX_1.24V
PL5 1uH_7x7x3
5671NC_1.24V
PC160 *68p/50V_4
5671FB_1.24V
PC166 *22p/50V_4
5671EN_1.24V
PR211 *S_4
PC167 *0.1u/16V_4
PR207 *S_4
PC131 0.1u/25V_4
PC140 22u/6.3V_6
PJ7 *S_3720
+1.24V_S5
R1 PR213 10K_1%_4
R2 PR212 10K_1%_4
HWPG_1.8V_S5

Vo=0.6*(R1+R2)/R2
=1.24V

+1.5V
1.5Volt +/- 5%
TDC : 0.39A
PEAK : 0.52A
Width : 20mil

+3VPCU
PR230 *S_8
PC203 10u/6.3V_6
PC202 0.1u/50V_6
[15,22,24,25,26,30] MAINON
MAINON
PR228 *S_4
PR227 100K_5%_4
PC201 *0.1u/50V_6
PU12 G9661MF11U (VIN, NC, VO, VEN, VPP, POK, ADJ, GND#1, GND#2)
PR237 *S_8
+1.5V
+5VPCU
PR73 *S_4
PC206 1u/25V_4
[22] HWPG_1.5V
+3V
PR225 100K_5%_4
PC216 10u/6.3V_6
R1 PR236 30K_1%_4
R2 PR235 34K_1%_4

Vref=0.8V

Vo =0.8(1+R1/R2)
=1.506V

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	+1.8V_S5 / +1.24V_S5 / +1.5V	1A
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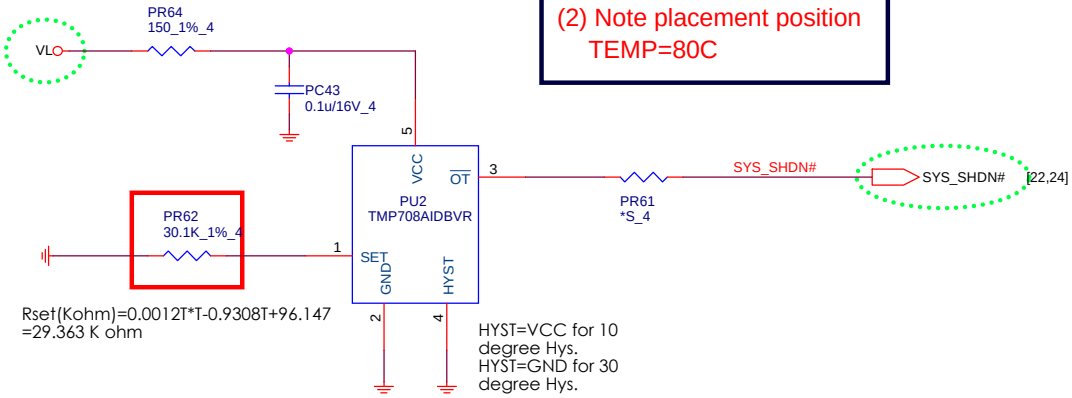
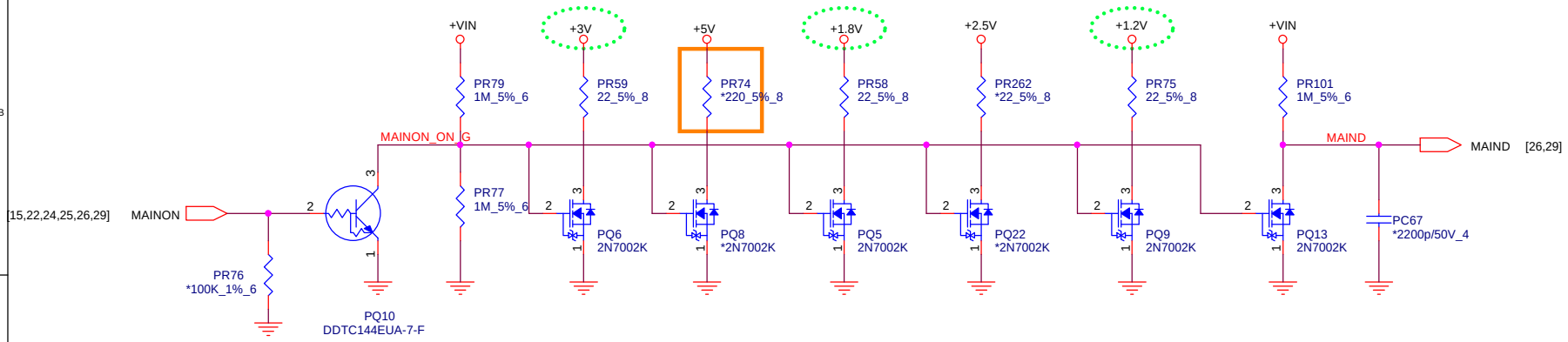
[24] VL
[13,20,23,24,25,26,27,28,31] +VIN
[3,4,5,6,10,13,14,15,16,17,18,19,22,24,25,26,27,28,29] +3V
[13,14,15,17,19,24] +5V
[3,4,13,15,29] +1.8V
[10,26] +2.5V

Thermal Protection

(1) Need fine tune for thermal protect point
(2) Note placement position TEMP=80C



+5V PU High R= 220 ohm for Bo-Bo sound issue.



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	Thermal / Discharge	1A
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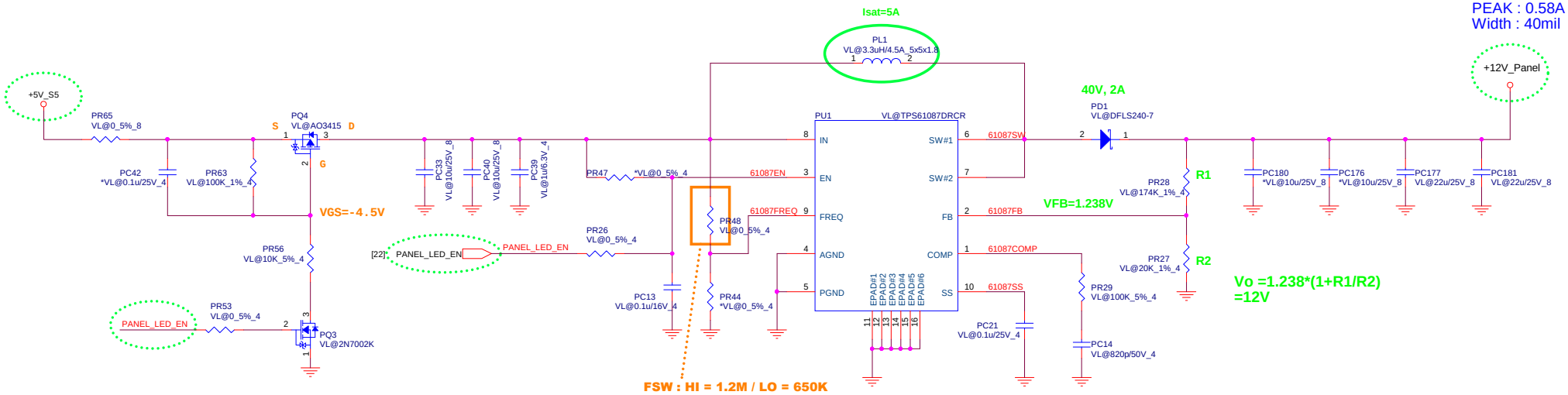
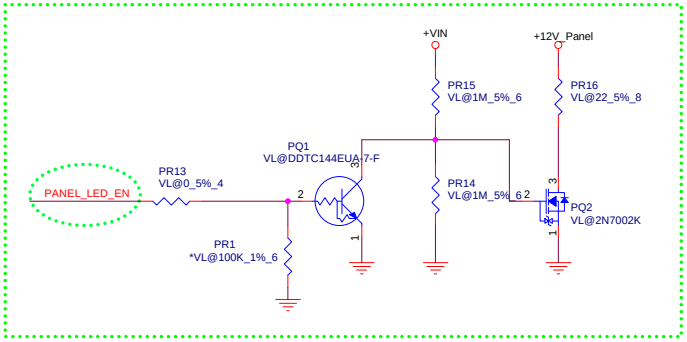
Panel Spec (TFT-LCD 17.3")
VLED : 6V~21V (Typ:12V)
Power Consumption : 7W (MAX)

+VIN [13,20,23,24,25,26,27,28,30]
+12V_Panel [13]
+5V_S5 [6,20,21,24,26,27,28]

+12V_Panel
12 Volt +/- 5%
PEAK : 0.58A
Width : 40mil



BL Discharge Circuit



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	LED Panel (TPS61087)	1A

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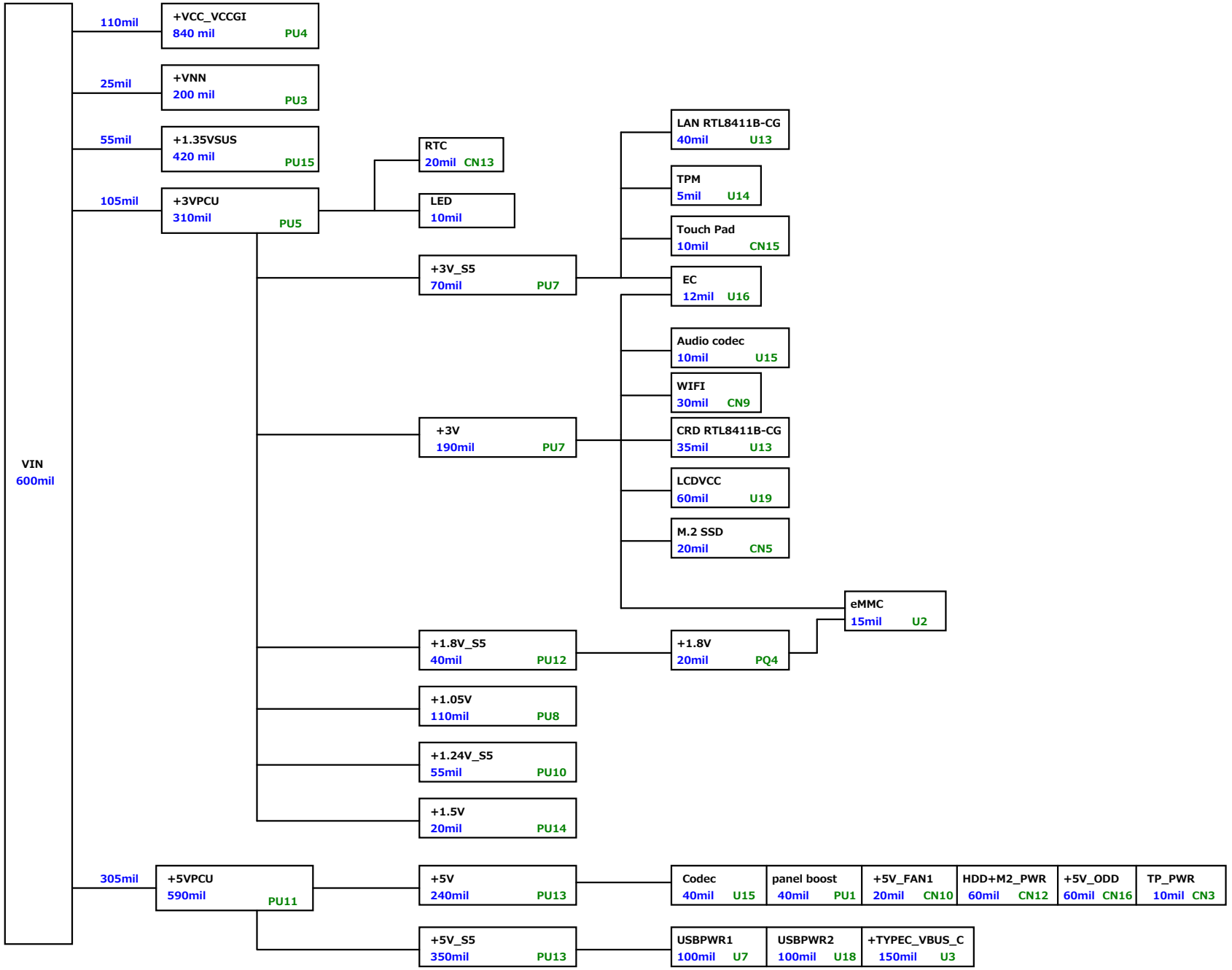
Gemini lake Power Tree



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POWER TREE
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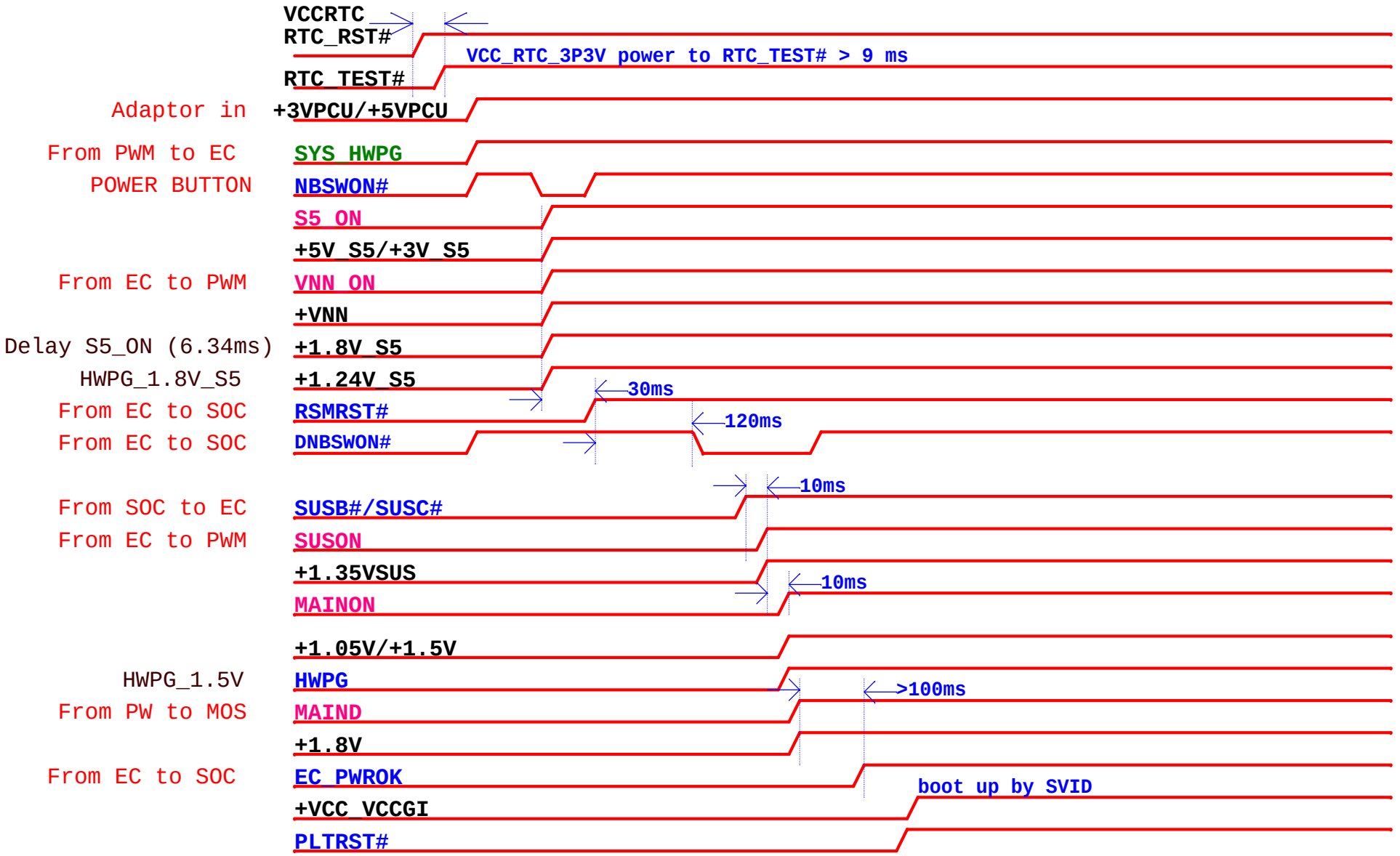

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