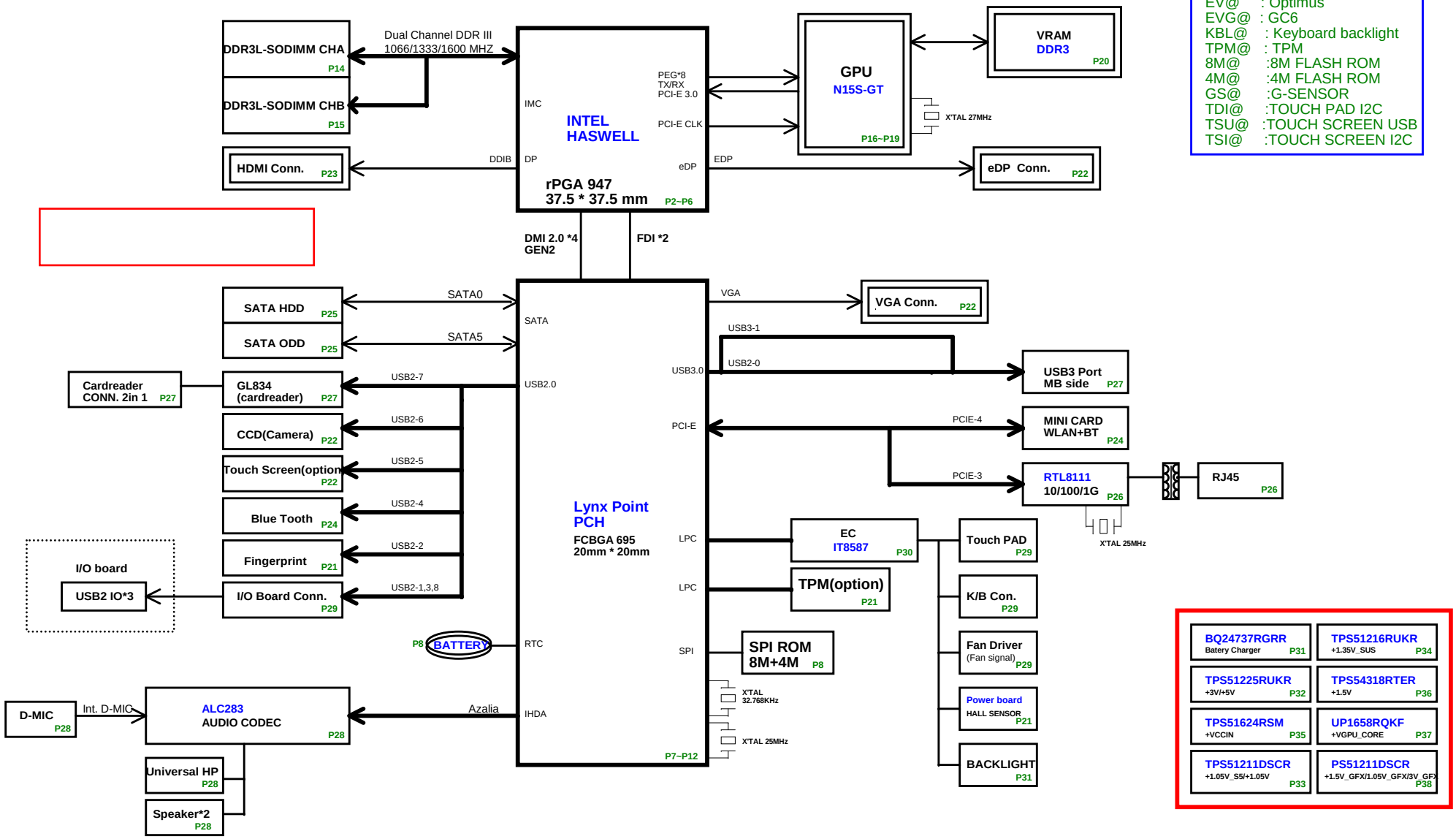
01

Z8B_GDDR3 HSW SV SYSTEM BLOCK DIAGRAM

BOM

IV@ : iGPU
EV@ : Optimus
EVG@ : GC6
KBL@ : Keyboard backlight
TPM@ : TPM
8M@ :8M FLASH ROM
4M@ :4M FLASH ROM
GS@ :G-SENSOR
TDI@ :TOUCH PAD I2C
TSU@ :TOUCH SCREEN USB
TSI@ :TOUCH SCREEN I2C

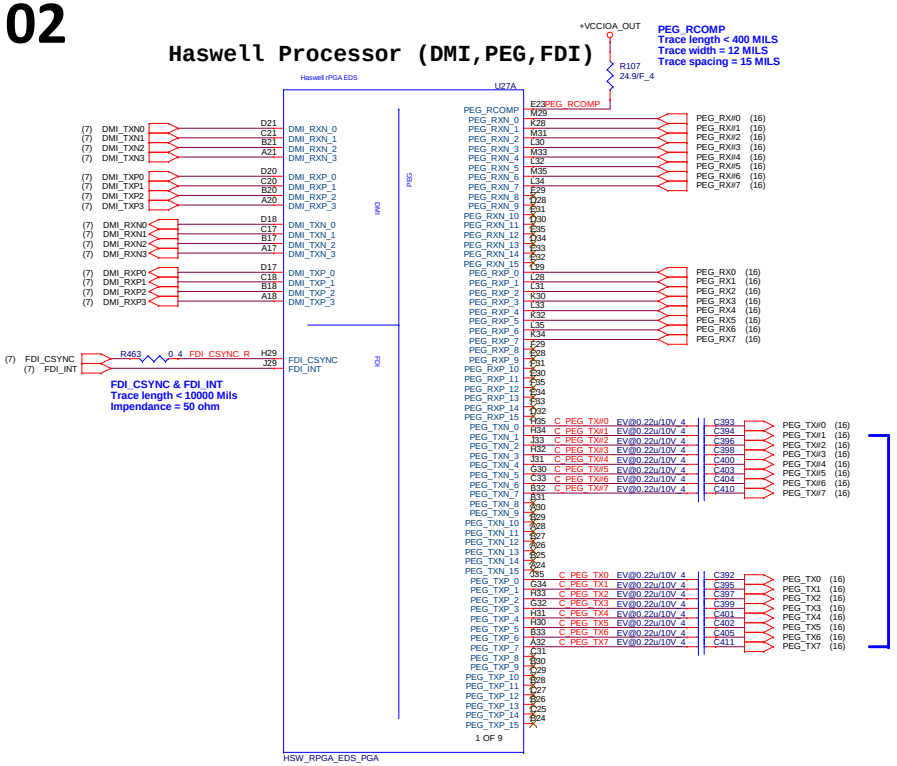


BQ24737RGRR Batery Charger P31	TPS51216RUKR +1.35V_SUS P34
TPS51225RUKR +3V/+5V P32	TPS54318RTER +1.5V P36
TPS51624RSM +VCCIN P35	UP1658RQKF +VGPU_CORE P37
TPS51211DSCR +1.05V_S5/+1.05V P33	PS51211DSCR +1.5V_GFX/1.05V_GFX/3V_GFX P38

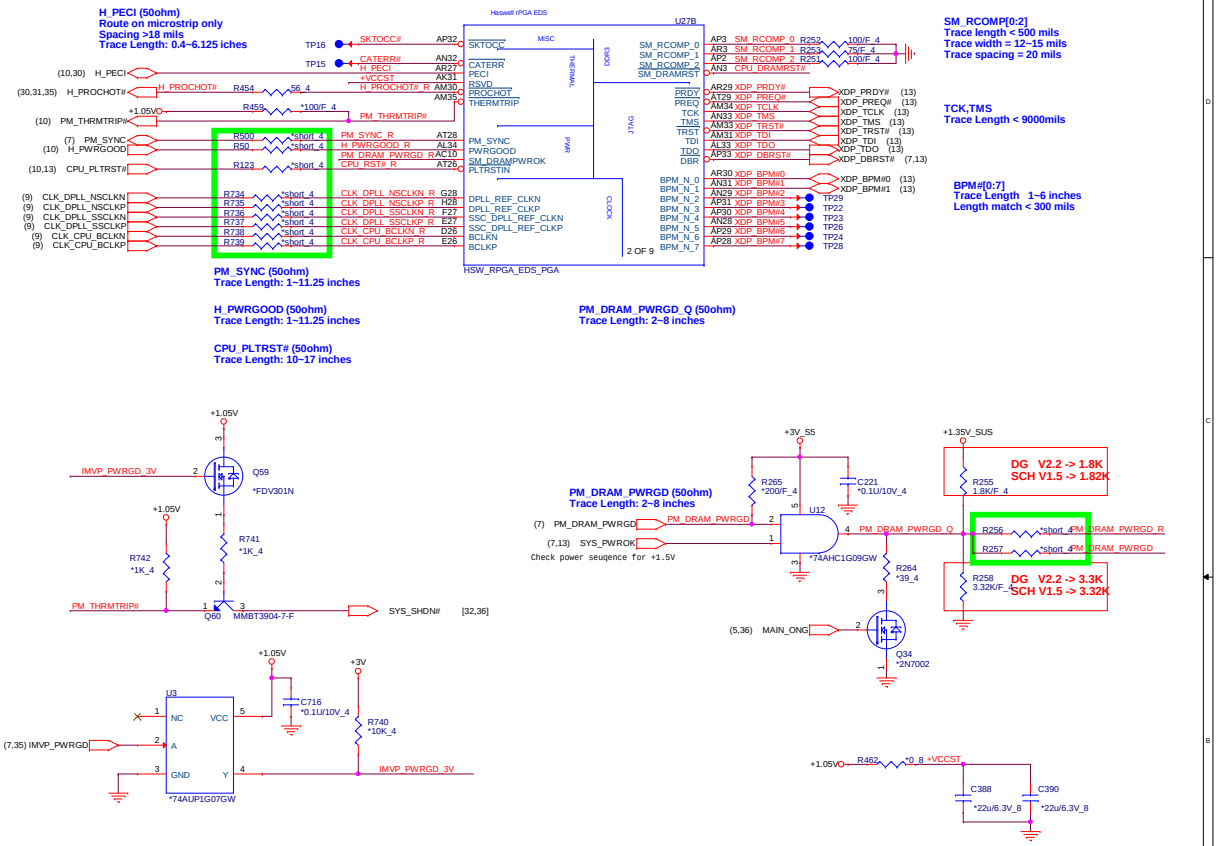
Quanta Computer Inc.
PROJECT : Z8B
Block Diagram
Size | Document Number | Rev 3A
Date: Friday, May 16, 2014 Sheet 1 of 44

02

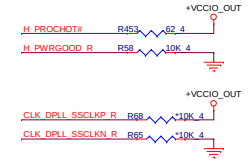
Haswell Processor (DMI,PEG,FDI)



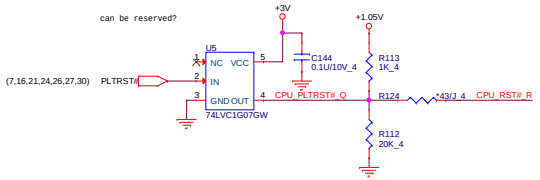
Haswell Processor (CLK,MISC,JTAG)



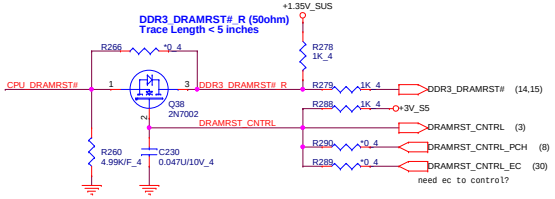
PU/PD of CPU



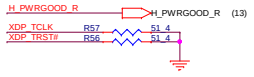
Reserved For buffer reset of PLTRSRIN#



SM_DRAMRST# Topology



XDP PU/PD

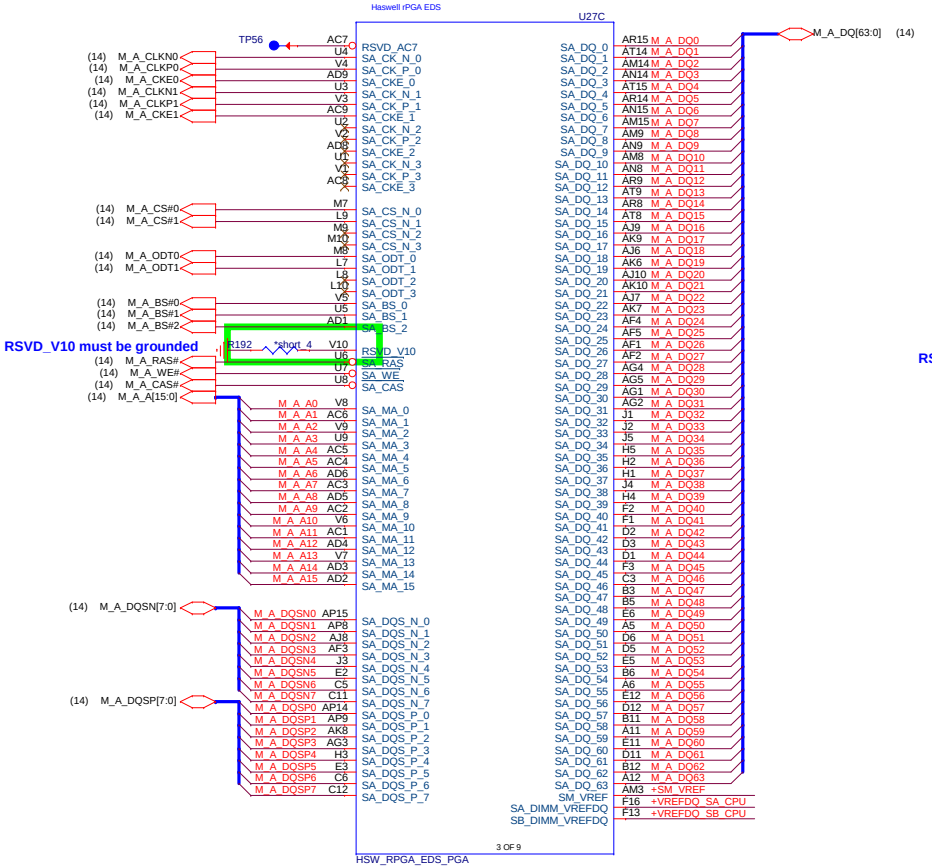


Quanta Computer Inc.
PROJECT : Z8B

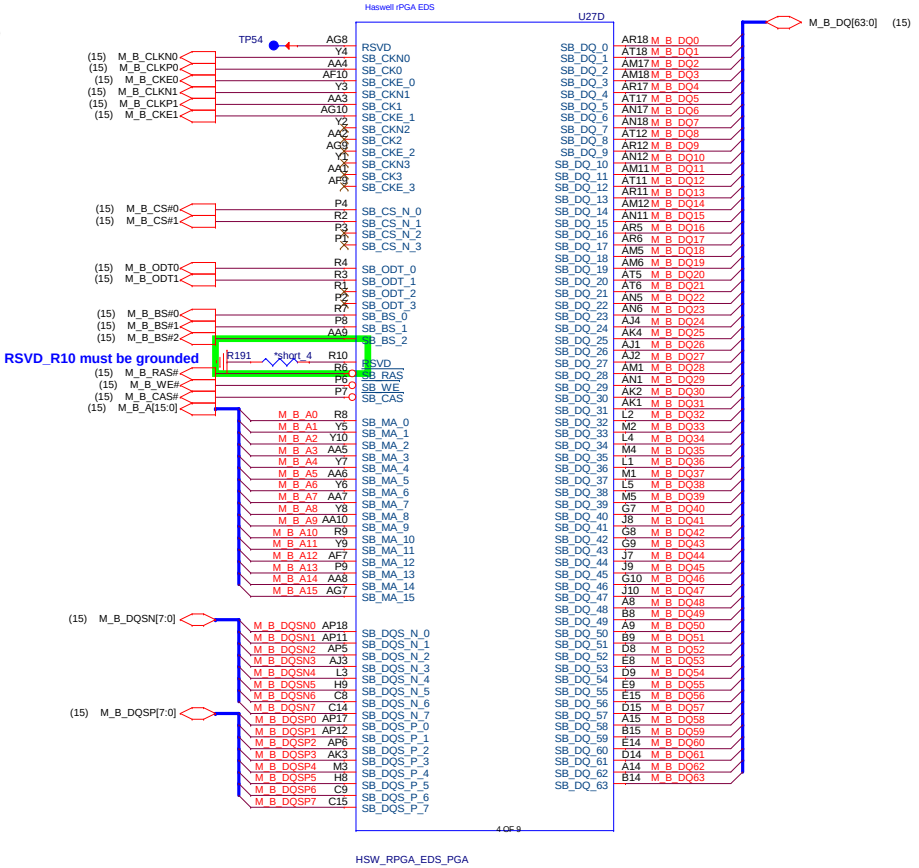
Size	Document Number	Rev
	Haswell 1/5 (PEG/DMI/FDI)	1A
Date: Monday, July 14, 2014	Sheet 2 of 44	

03

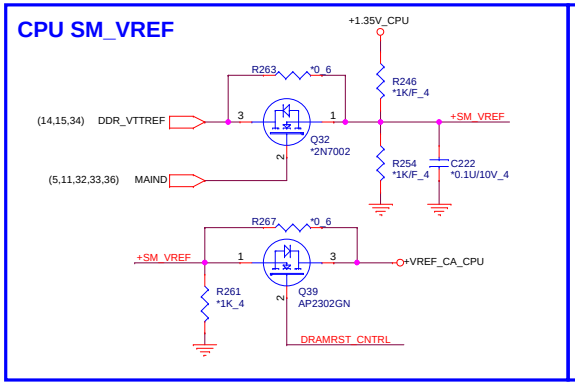
Haswell Processor (DDR3)



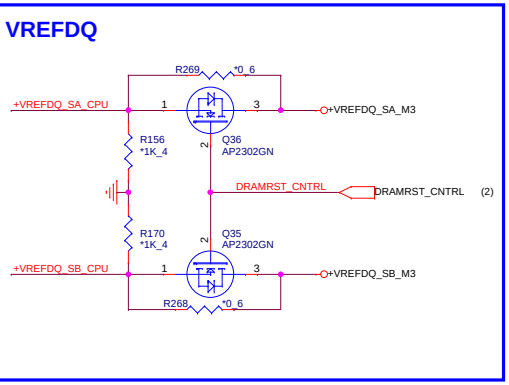
Haswell Processor (DDR3)



CPU SM_VREF



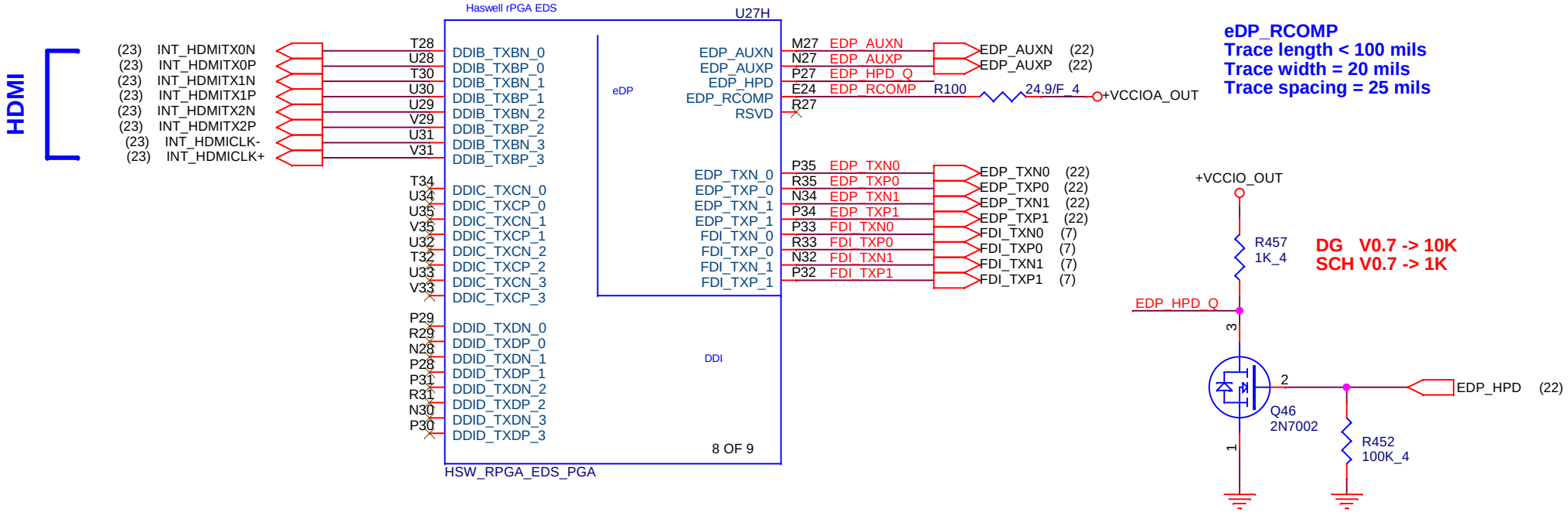
CPU VREFDQ



Quanta Computer Inc.		
PROJECT : Z8B		
Size	Document Number: Haswell 2/5 (DDR3 I/F)	Rev: 1A
Date: Friday, June 13, 2014	Sheet 3 of 44	

04

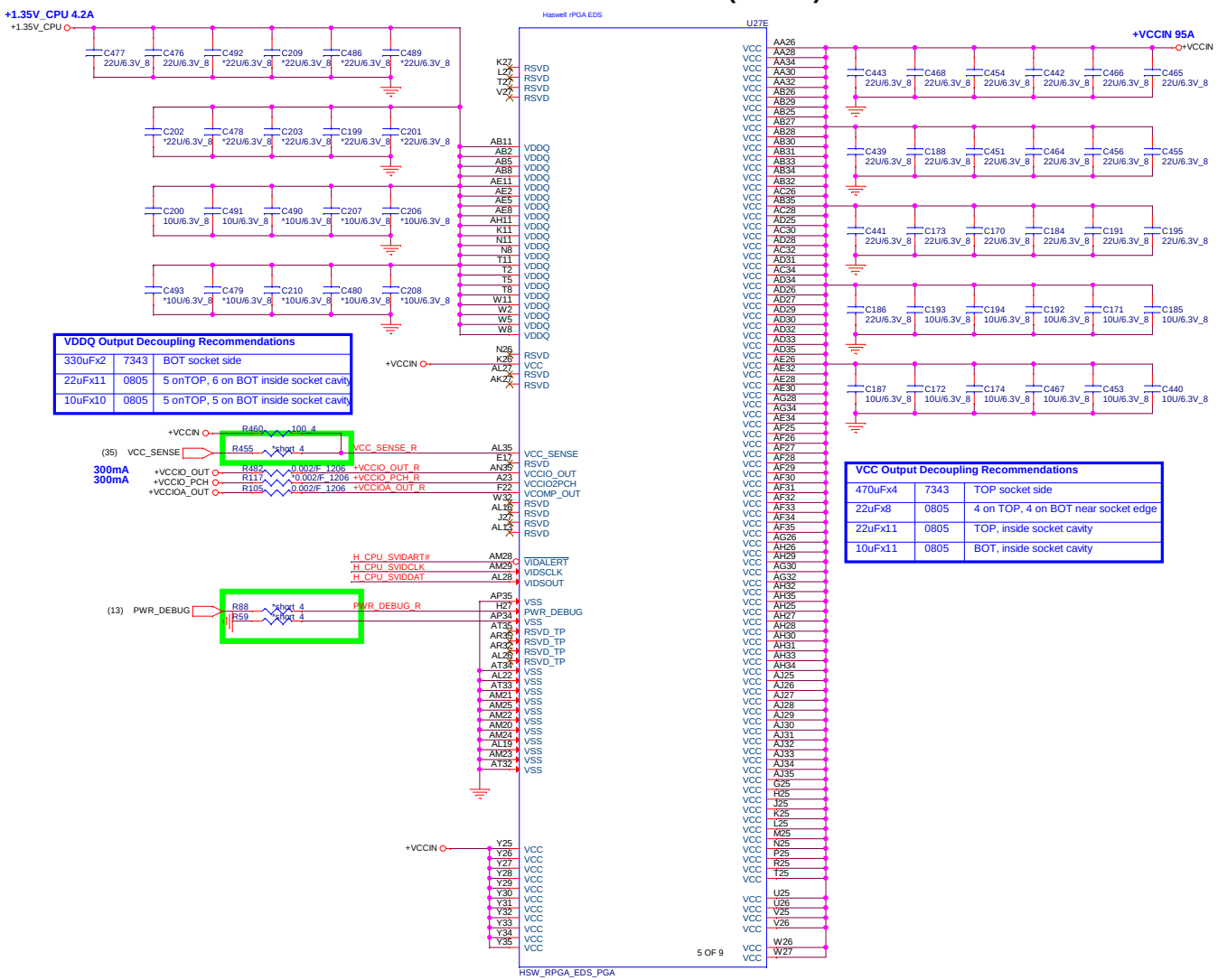
Haswell Processor (DDI,eDP,FDI)



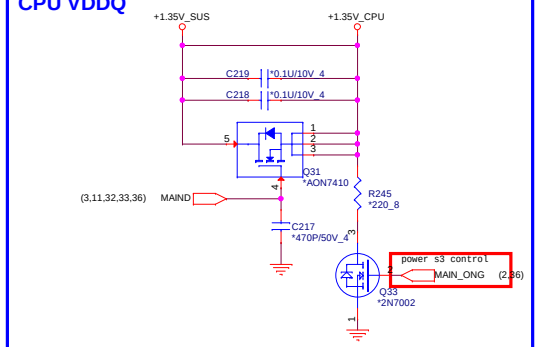
Quanta Computer Inc.		
PROJECT : Z8B		
Size	Document Number: Haswell 3/5 (DDI/eDP)	Rev: 1A
Date: Friday, June 13, 2014	Sheet 4 of 44	

05

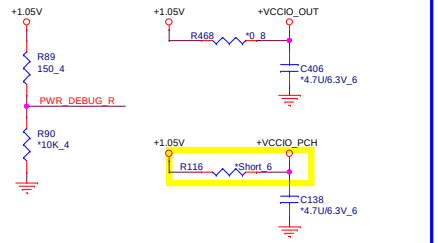
Haswell Processor (POWER)



CPU VDDQ

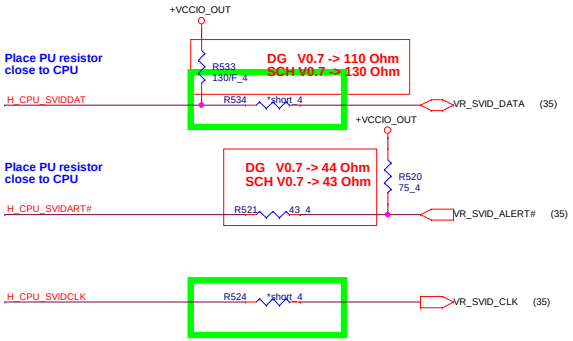


Power Test Propose



SVID

Layout note: need routing together and ALERT need between CLK and DATA.

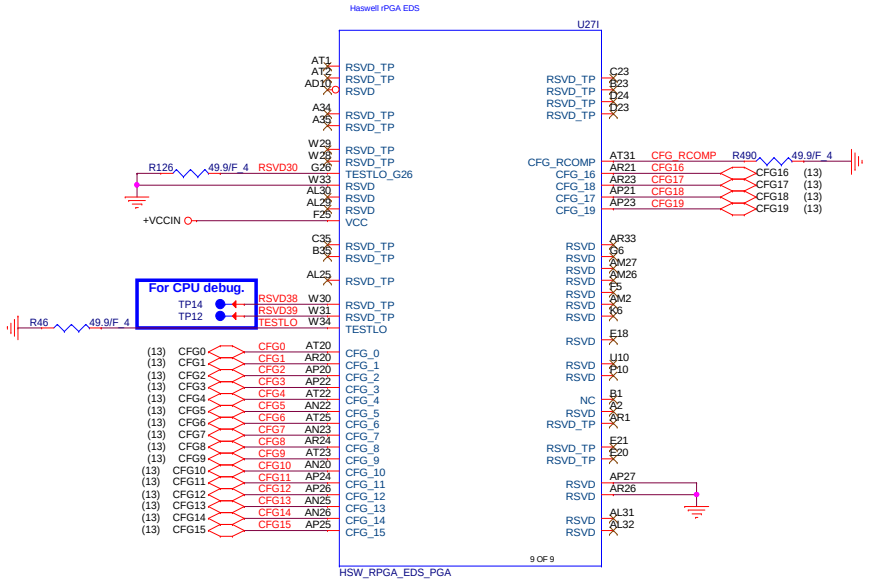


Quanta Computer Inc.	PROJECT : Z8B	
Size	Document Number: Haswell 4/5 (POWER)	Rev: 1A
Date: Monday, July 14, 2014	Sheet 5 of 44	

06

Haswell Processor (GND)

Haswell Processor (CFG,RSVD)



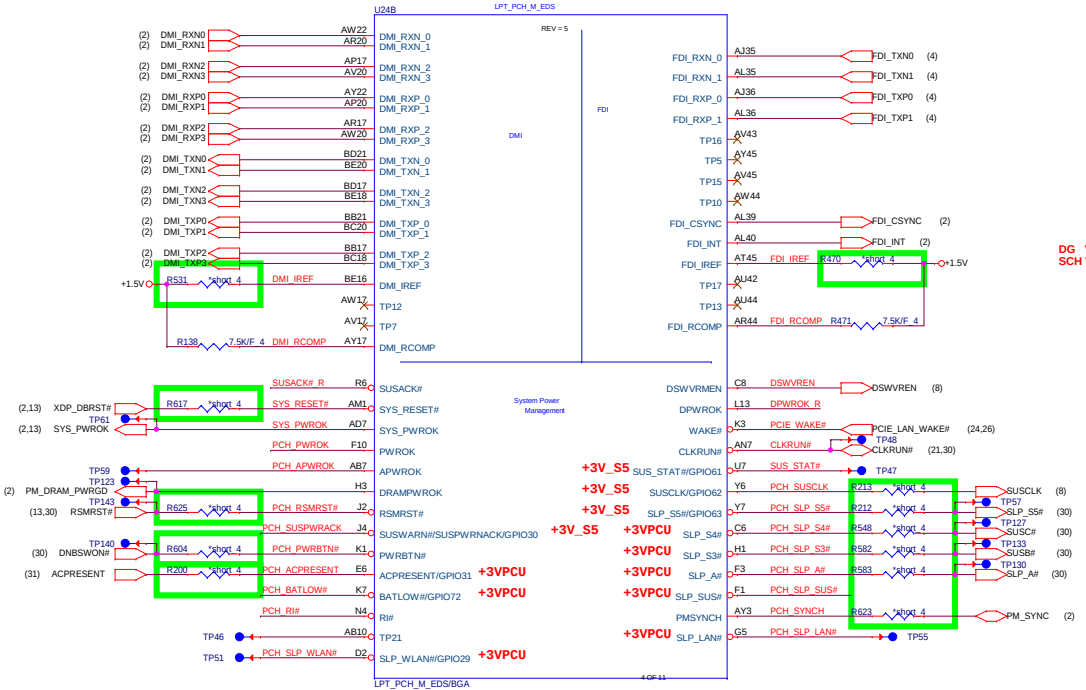
Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board.	
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed	CFG2 R147 *1K_4
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled	CFG4 R140 1K_4
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express	CFG6 R115 *1K_4 CFG5 R135 *1K_4
CFG[7]	PEG defer training	x1 = PEG train follow RESETB de-asseted x0 = PEG wait for BIOS fro training	CFG7 R131 *1K_4

Quanta Computer Inc.
PROJECT : Z8B

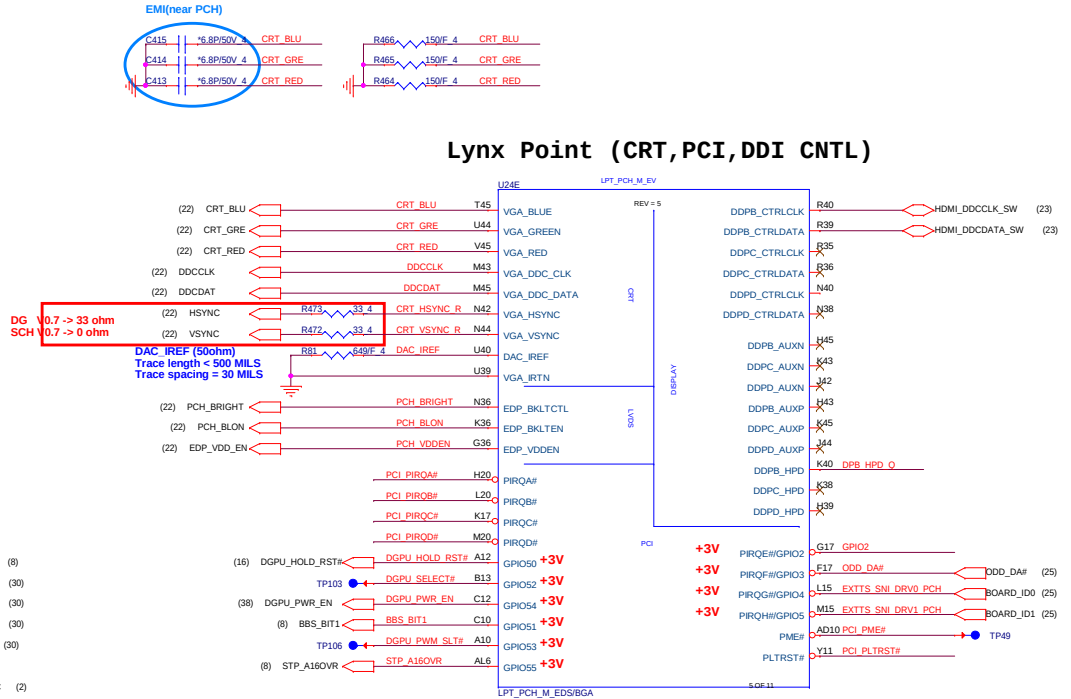
Size	Document Number	Rev
	Haswell 5/5 (CFG/GND)	1A
Date: Tuesday, June 10, 2014	Sheet 6 of 44	

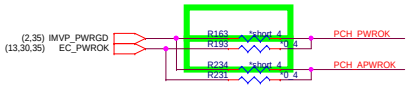
07

Lynx Point (DMI,FDI,PM)

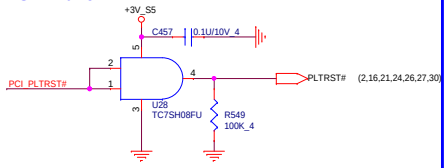


Lynx Point (CRT,PCI,DDI CNTL)

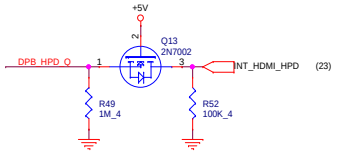




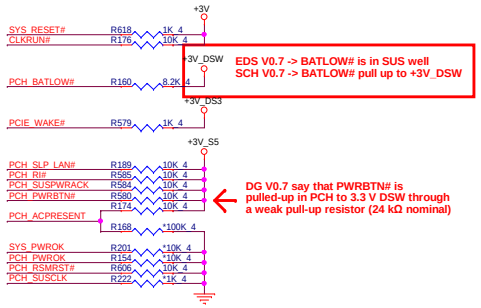
PLTRST# Buffer



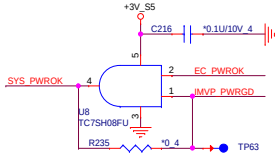
HDMI HPD



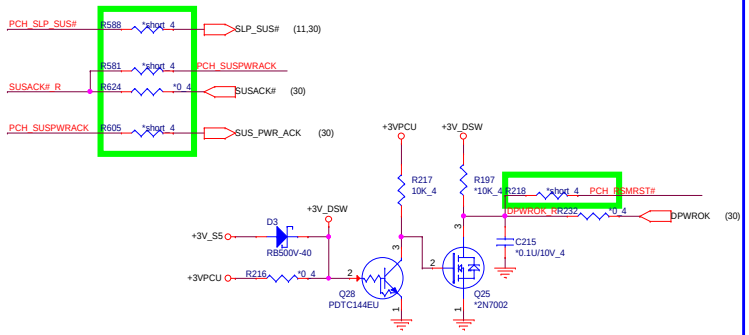
PCH PM PU/PD



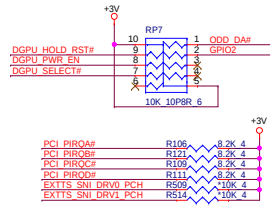
SYSPWOK



DSW Circuit



PCI PU

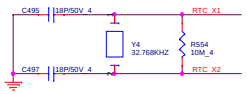


Quanta Computer Inc.
PROJECT : Z8B

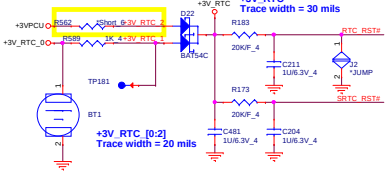
Size	Document Number	Rev
	LPT 1/6 (DMI/FDI/VGA)	1A
Date: Tuesday, July 01, 2014	Sheet 7 of 44	

08

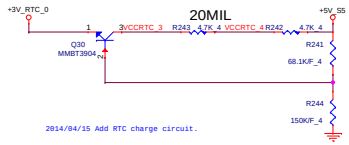
RTC Clock 32.768KHz (RTC)



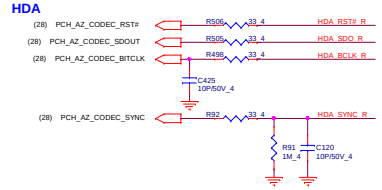
RTC Circuitry (RTC)



RTC charge circuit

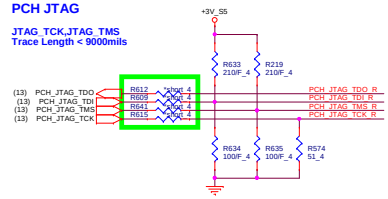


HDA

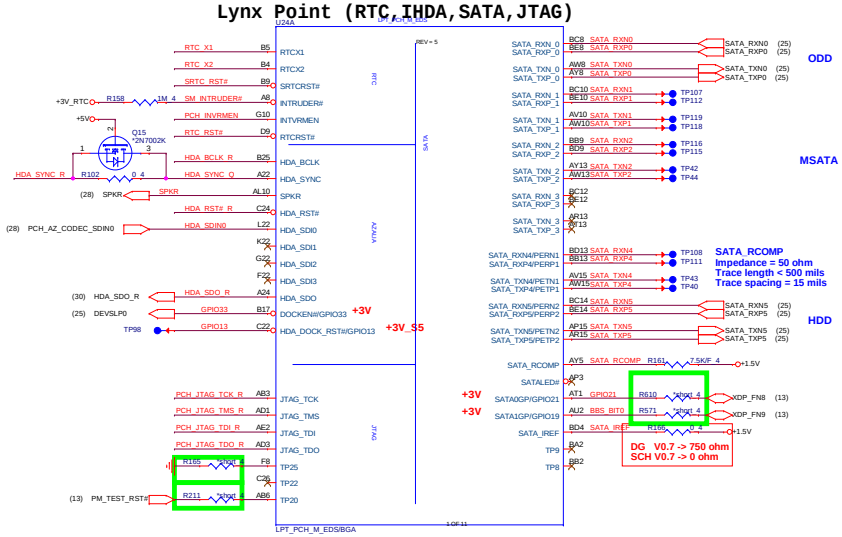


PCH JTAG

JTAG_TCK,JTAG_TMS
Trace Length < 9000mils



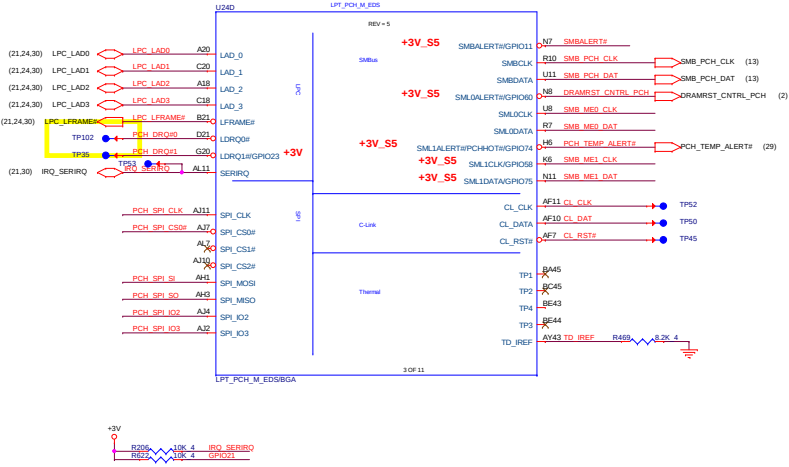
Lynx Point (RTC,IHDA,SATA,JTAG)



PCH STRAPING

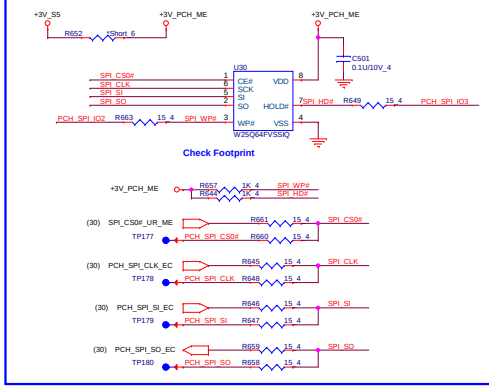
Pin Name	Usage	Sampled	Configuration	Circuitry
SPKR	No Reboot	PWROK	0 = Disable (Int PD) 1 = Enable	SPKR R209 *1K_4 +3V
GPIO62 / SUSCLK	PLL On-Die Voltage Regulator Enable	RSMRST#	0 = Disable 1 = Enable (Int PU)	(7) SUSCLK R221 *1K_4
GPIO55	Top-Block Swap Override	PWROK	0 = Top-Block Swap mode 1 = Default (Int PU)	(7) STP_A16OVR R167 *1K_4
INTVRMEN	Integrated VRM Enable	Always	0 = Disable 1 = Enable	PCH_INVRMEN R171 390K/F_4 +3V_RTC
GPIO51	Boot BIOS Strap bit 1	PWROK	Bit1 Bit0 1 0 Resevred 1 1 SPI 0 0 LPC	(7) BBS_BIT1 R146 *1K_4
SATA1GP/GPIO19	Boot BIOS Strap bit 0	PWROK		BBS_BIT0 R572 *1K_4
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	HDA_SDO_R R501 *1K_4 VCC_HDA_IO
GPIO36	RSVD	PWROK	Internal PD	(10) GPIO36 R596 *1K_4 +3V
SATA3GP/GPIO37	TLS Confidentiality	PWROK	0 = TLS no confidentiality (Int PD) 1 = TLS with confidentiality	(10) FDI_OVRVLTG R620 *1K_4 +3V
GPIO8	RSVD	RSMRST#	Internal PU	(10,22) GPIO8 R601 *1K_4
GPIO28	PLL on die VR enable	RSMRST#	0 = Disable 1 = Enable (Int PU)	(10) PLL_ODVR_EN R155 *1K_4
DSWVREN	On Die DSW VR Enable	Always	0 = Enable 1 = Disable Must be PU to VCCRTC	(7) DSWVREN R542 330K_4 R541 *330K_4 +3V_RTC

Lynx Point (LPC,SPI,SMBUS,C-LINK,THERMAL)

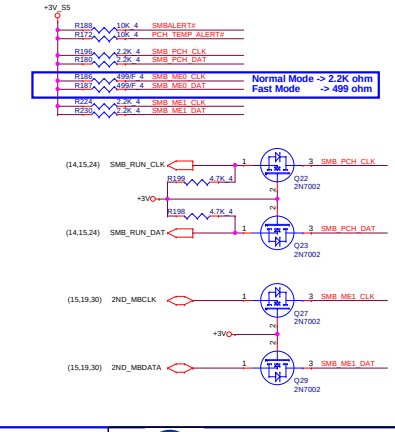


PCH Quad SPI ROM

Winbond 8MB AKE39ZP0N01



SMBus

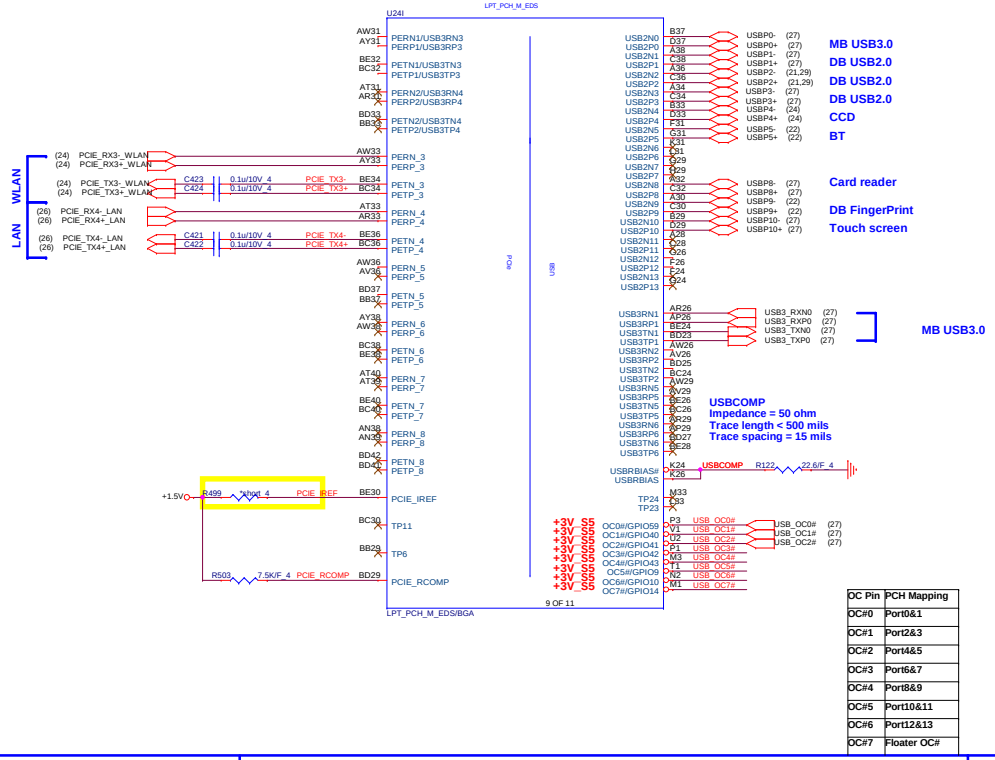


Quanta Computer Inc.
PROJECT : Z8B

Size	Document Number	Rev
	LPT 2/6 (SATA/HDA/SPI)	1A
Date: Saturday, July 12, 2014	Sheet 8 of 44	

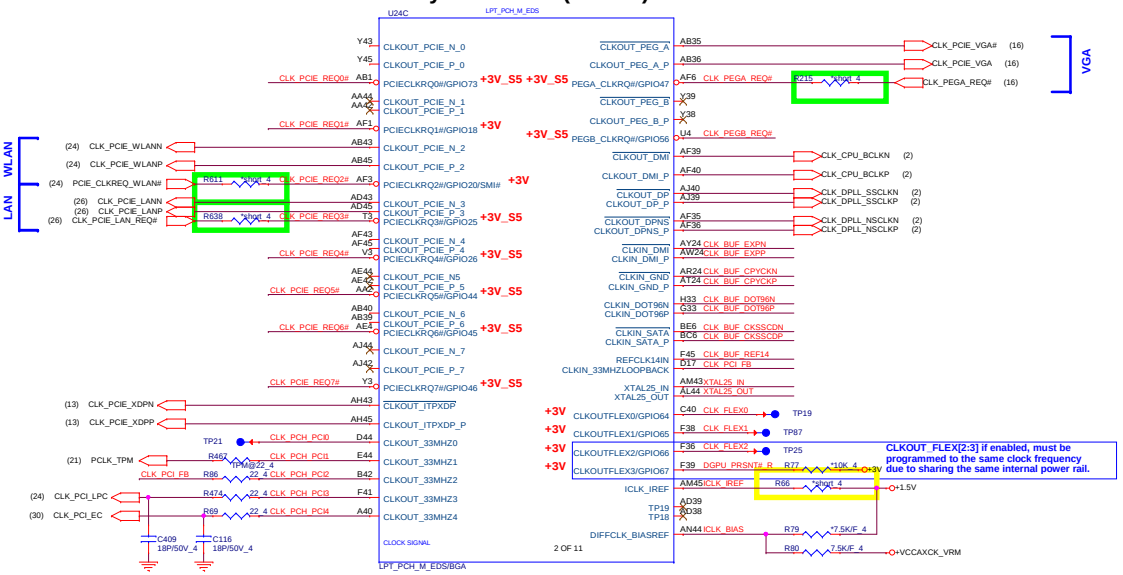
09

Lynx Point (PCIE,USB3.0,USB2.0)

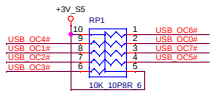


OC Pin	PCH Mapping
OC#0	Port0&1
OC#1	Port2&3
OC#2	Port4&5
OC#3	Port6&7
OC#4	Port8&9
OC#5	Port10&11
OC#6	Port12&13
OC#7	Floater OC#

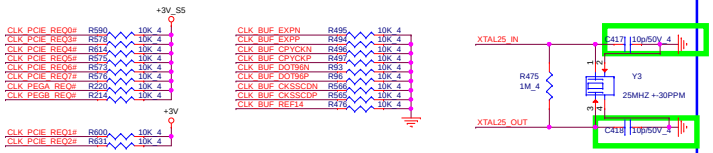
Lynx Point (CLOCK)



USB Overcurrent



PCH Intenal Clock



PCH XDP Signal

Routed by 50 ohm

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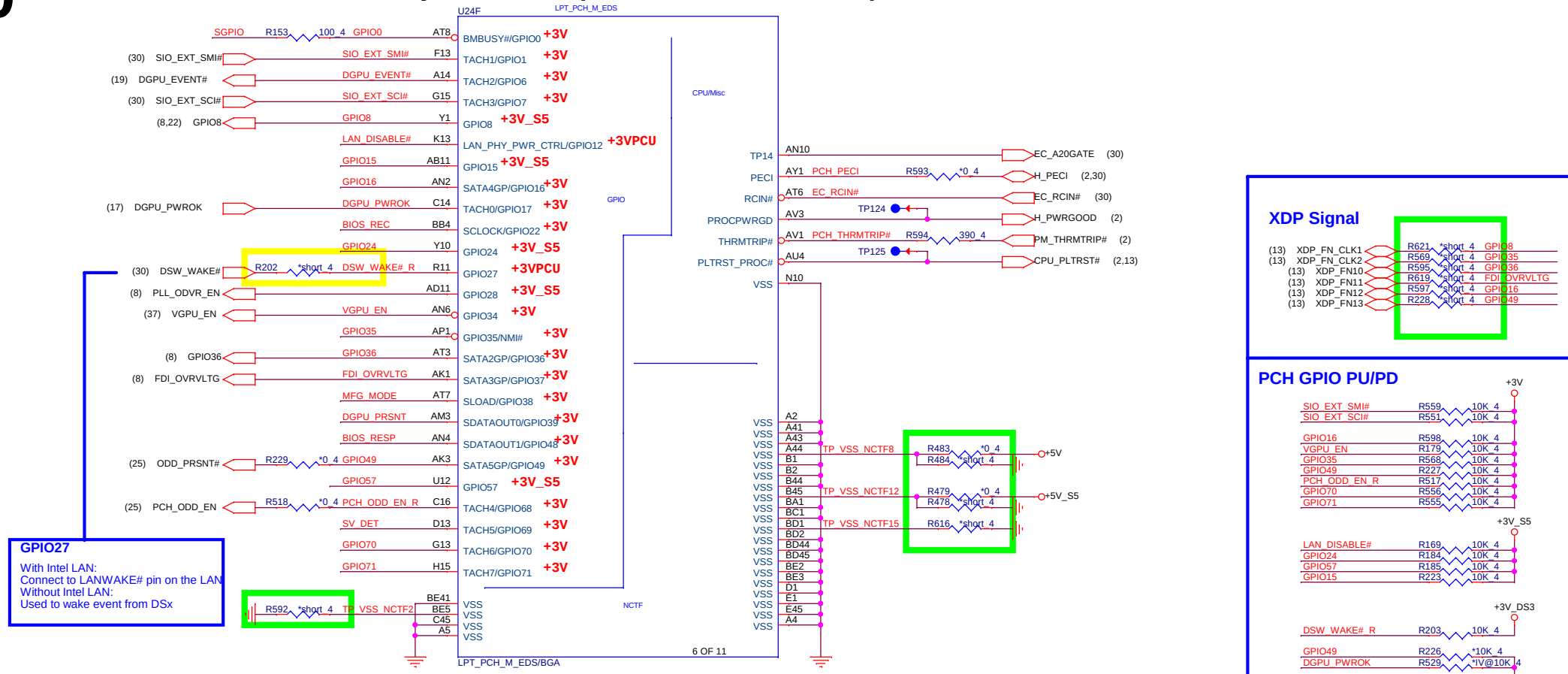
PROJECT : Z8B			
Size	Document Number		Rev
	LPT 3/6 (PCIE/USB/CLK)		1A
Date: Wednesday, July 09, 2014	Sheet 9	of 44	

10

Lynx Point (GPIO,CPU/MISC,NCTF)



GPIO27

With Intel LAN:
Connect to LANWAKE# pin on the LAN
Without Intel LAN:
Used to wake event from DSx

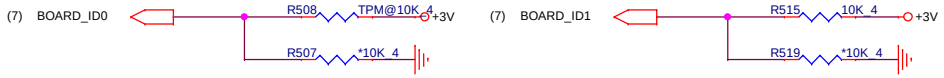
XDP Signal

PCH GPIO PU/PD

BOARD ID

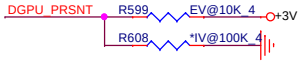
TPM exist or not 0 = No TPM
1 = TPM exist

Reserve: 0 = No xxx
1 = xxx exist

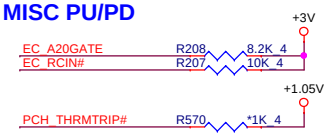


External Gfx Present

0 = Internal Gfx
1 = External Gfx

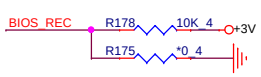


PCH MISC PU/PD



BIOS RECOVERY

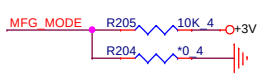
0 = Enable
1 = Disable



Swap GPIO

0 = SGPIO
1 = Default

MFG TEST



SV Detect

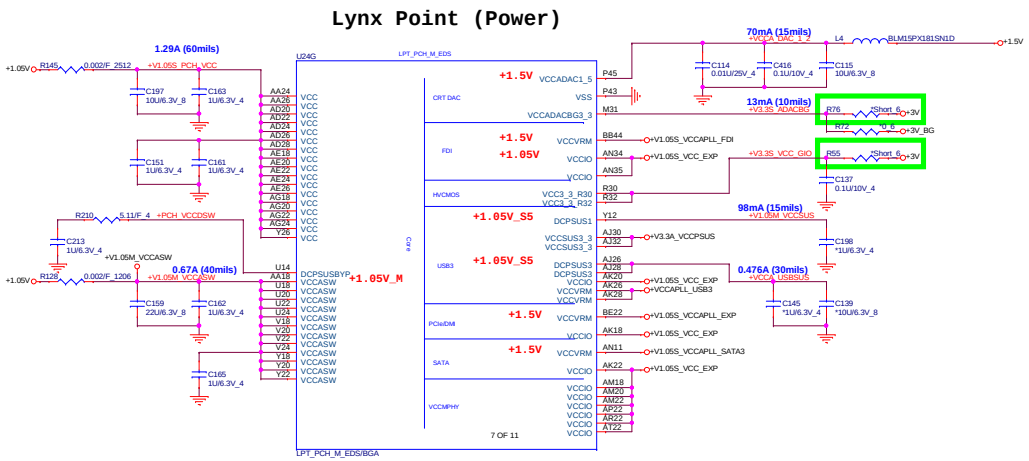
0 = SV Detect
1 = Default

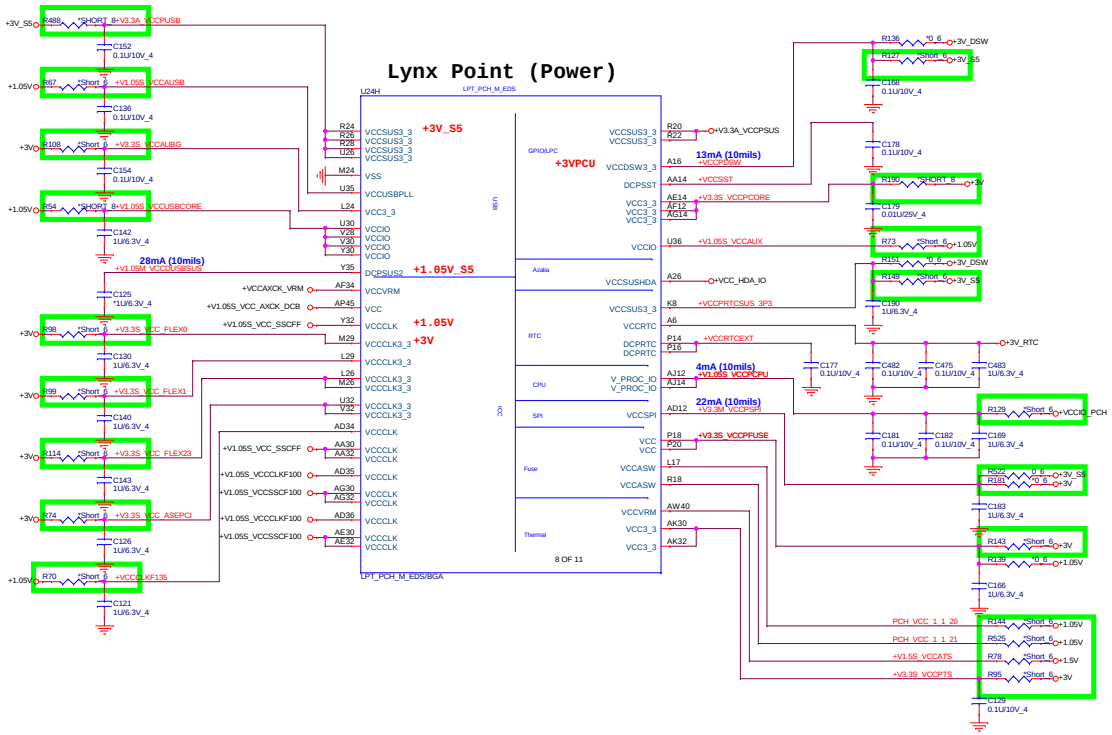
BIOS_RESP

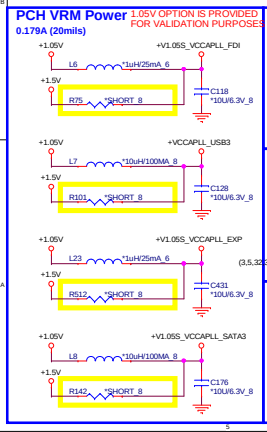
0 = BIOS RESP
1 = Default

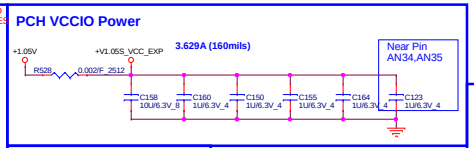
Quanta Computer Inc.
PROJECT : Z8B

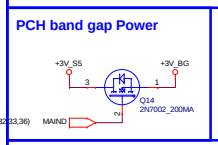
Size	Document Number	Rev
	LPT 4/6 (GPIO/MISC)	1A
Date: Wednesday, July 09, 2014	Sheet 10 of 44	

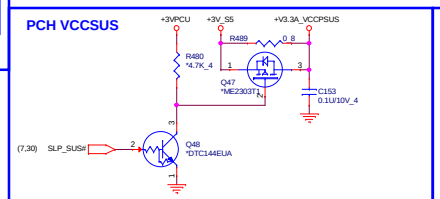


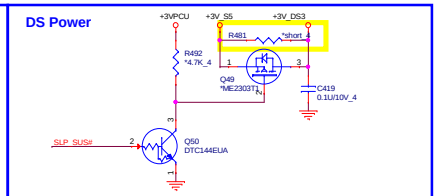


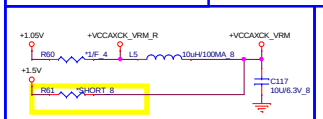


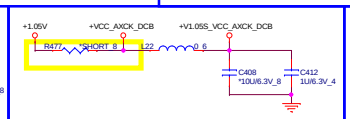


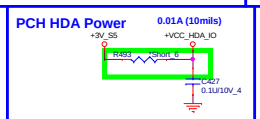


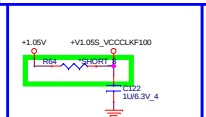


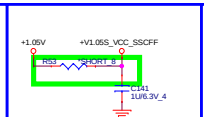


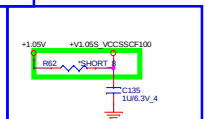










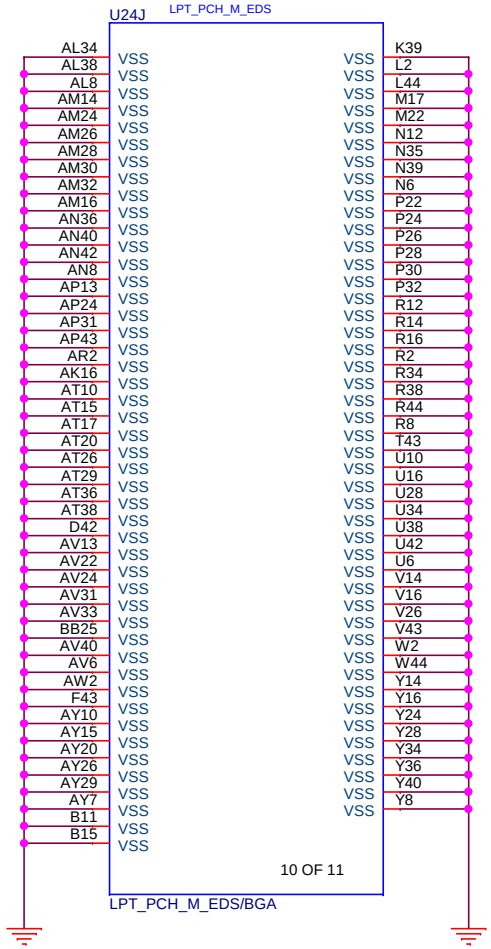


Quanta Computer Inc.
PROJECT : Z8B

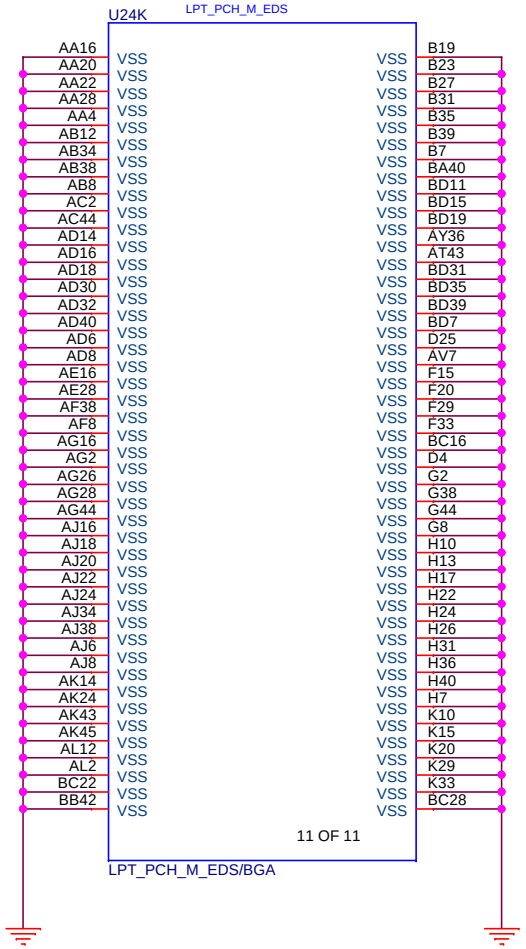
Size	Document Number	Rev
	LPT 5/6 (POWER)	1A
Date: Monday, July 14, 2014	Sheet 11 of 44	

12

Lynx Point (GND)



Lynx Point (GND)



Quanta Computer Inc.

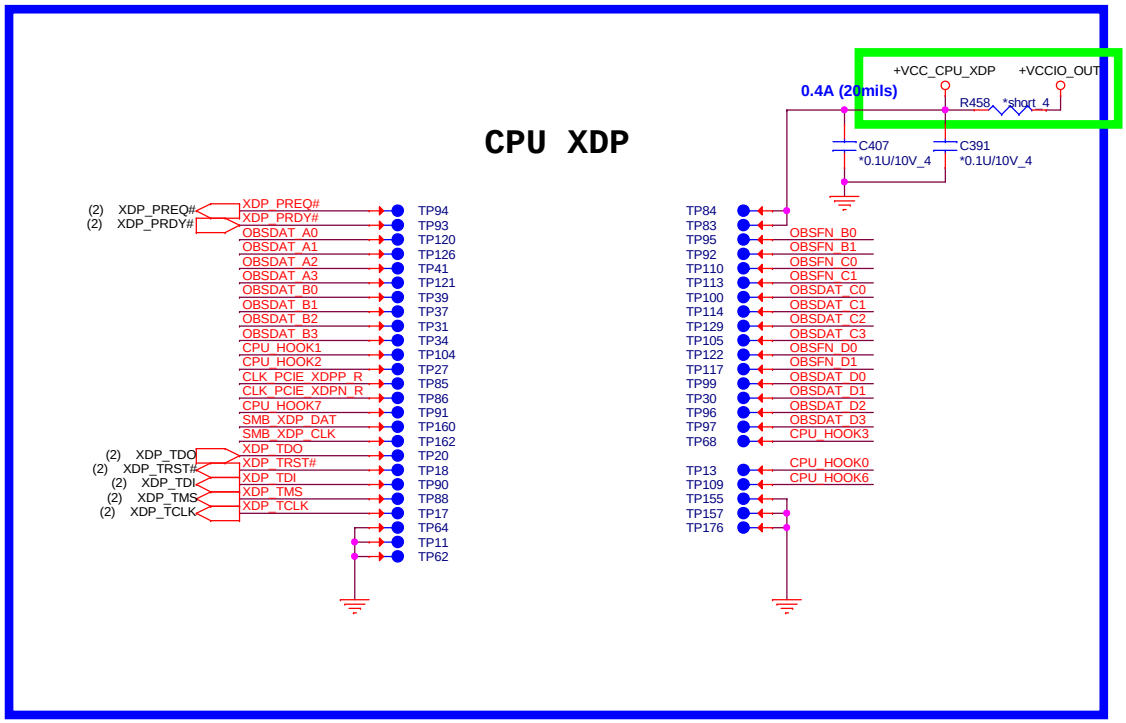
PROJECT : Z8B

Size	Document Number	Rev
	LPT 6/6 (GND)	1A

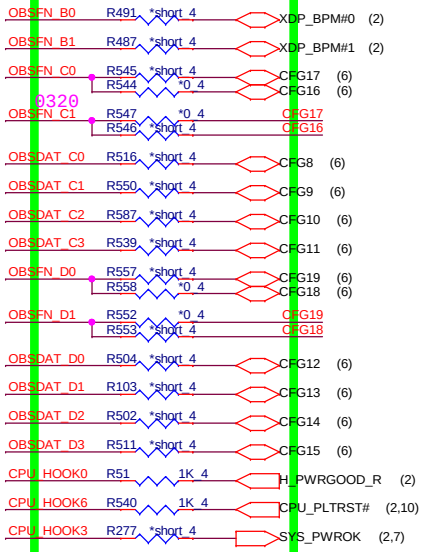
Date: Tuesday, May 13, 2014 Sheet 12 of 44

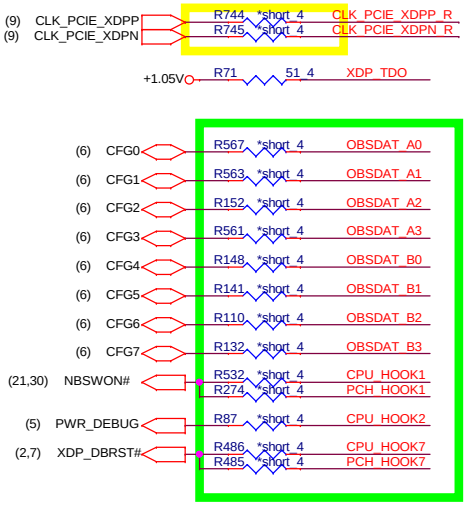
13

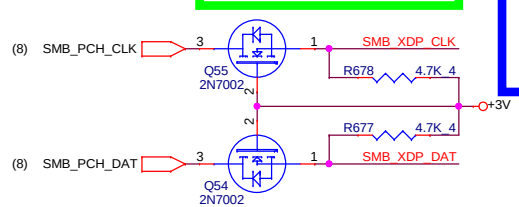
CPU XDP



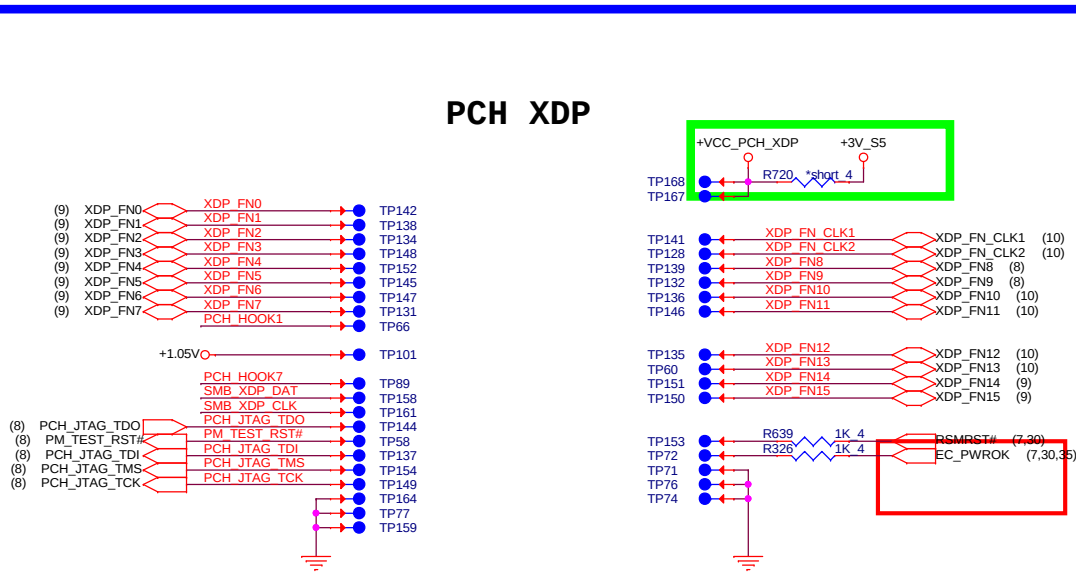
Stuff R1016, R1138
No stuff R1017, R1137

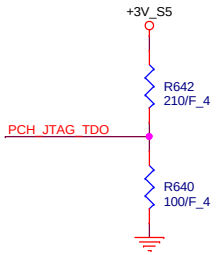






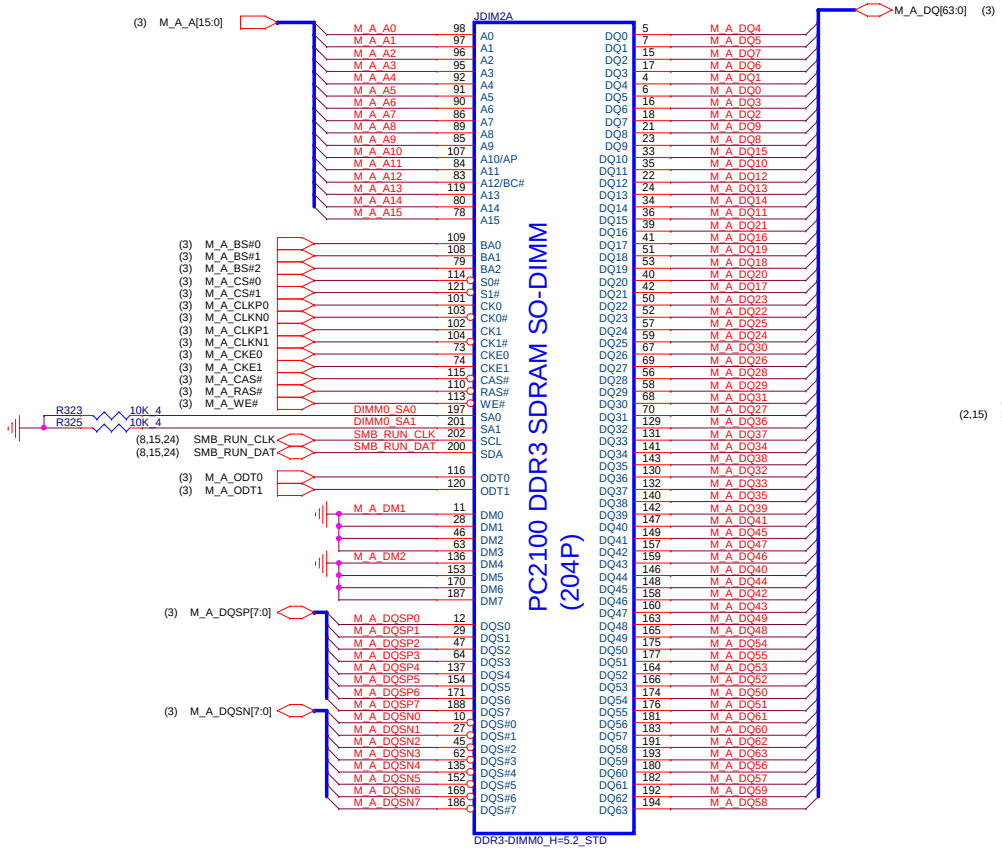
PCH XDP

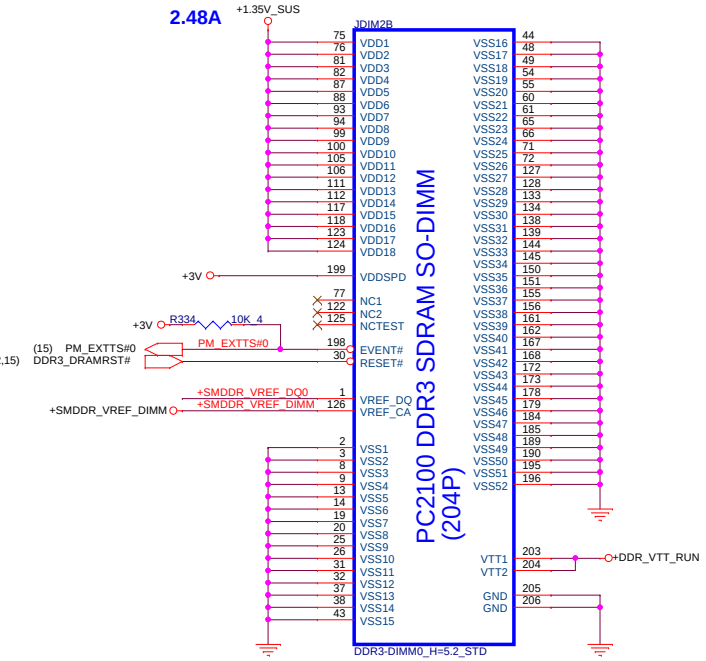




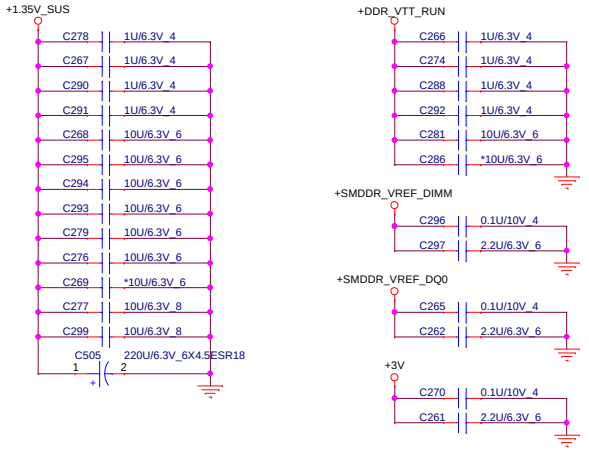
Quanta Computer Inc.		
PROJECT : Z8B		
Size	Document Number: CPU/PCH XDP	Rev: 1A
Date: Wednesday, July 09, 2014	Sheet 13 of 44	

14

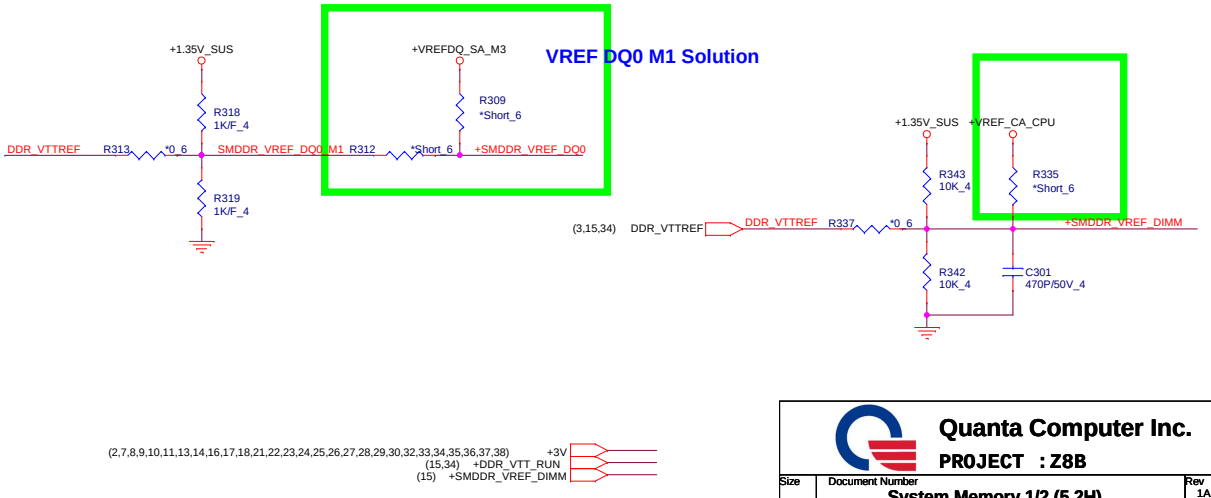




Place these Caps near So-Dimm0.

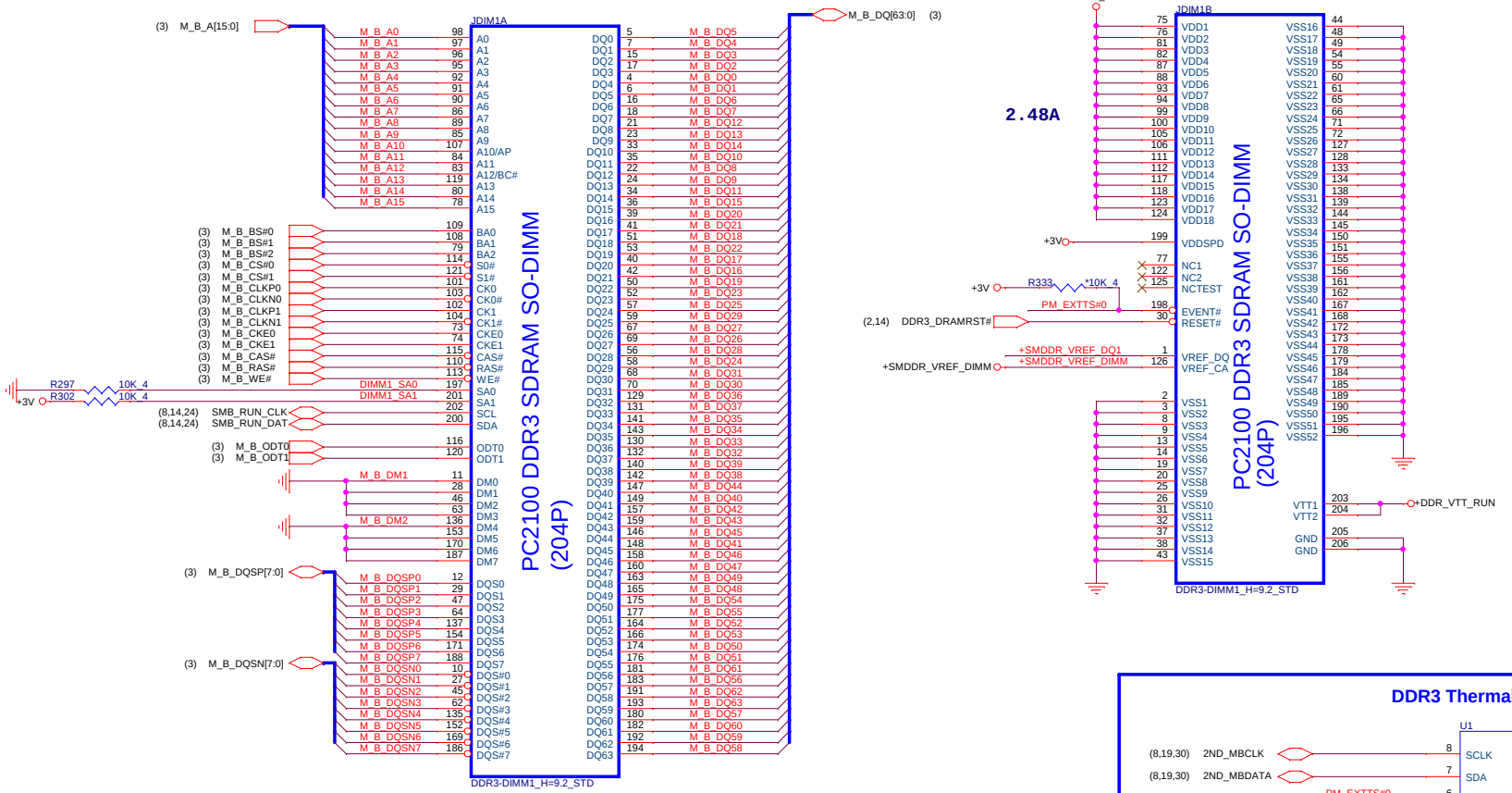


VREF DQ0 M1 Solution

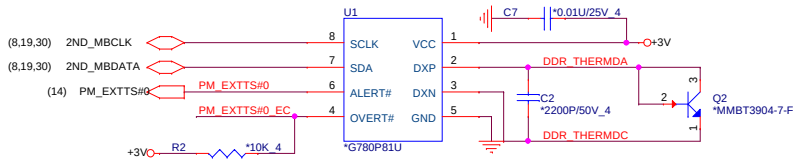


Quanta Computer Inc.
PROJECT : Z8B

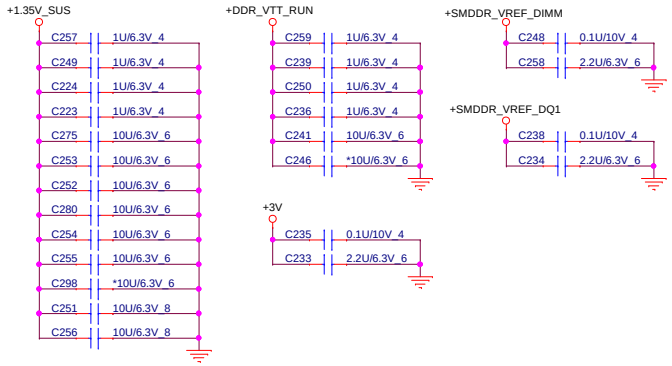
Size	Document Number	Rev
	System Memory 1/2 (5.2H)	1A
Date: Wednesday, July 09, 2014	Sheet 14 of 44	



DDR3 Thermal Sensor



Place these Caps near So-Dimm1.



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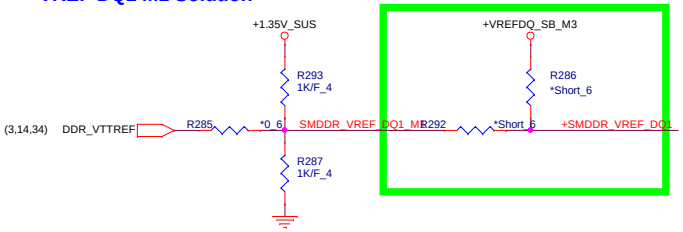
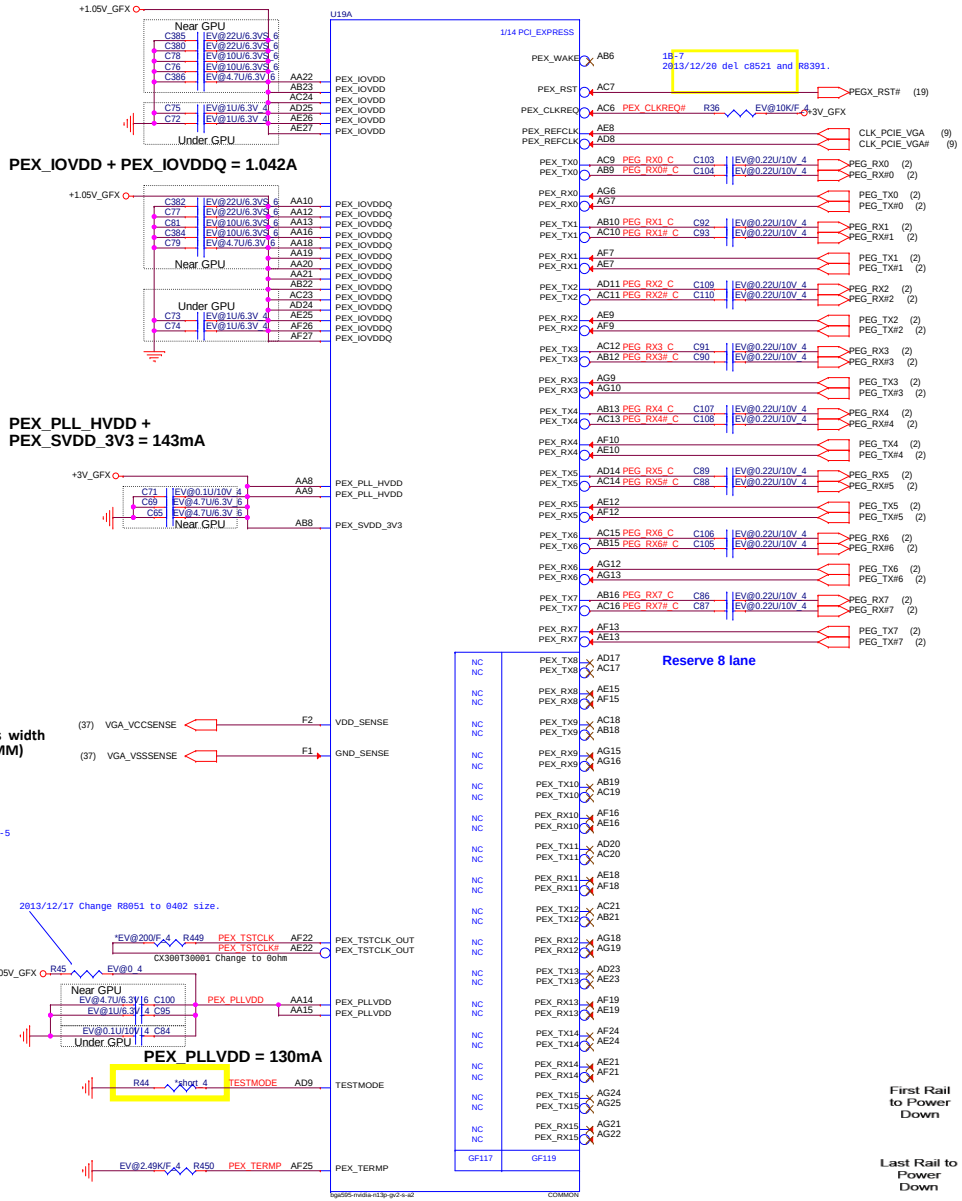
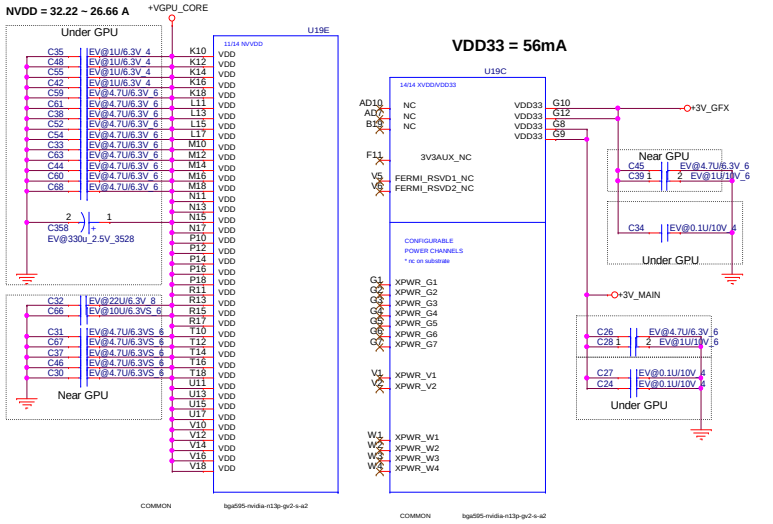
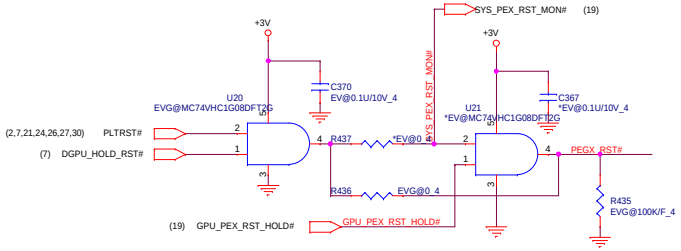


Quanta Computer Inc.			
PROJECT : Z8B			
Size	Document Number		Rev
	System Memory 2/2 (9.2H)		1A
Date: Wednesday, June 11, 2014		Sheet 15 of 44	

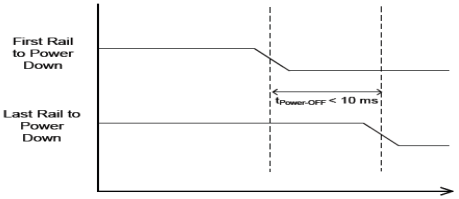
16

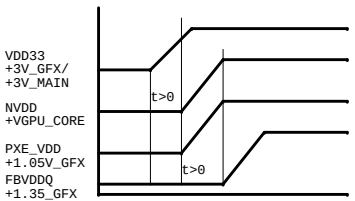






Power down sequence



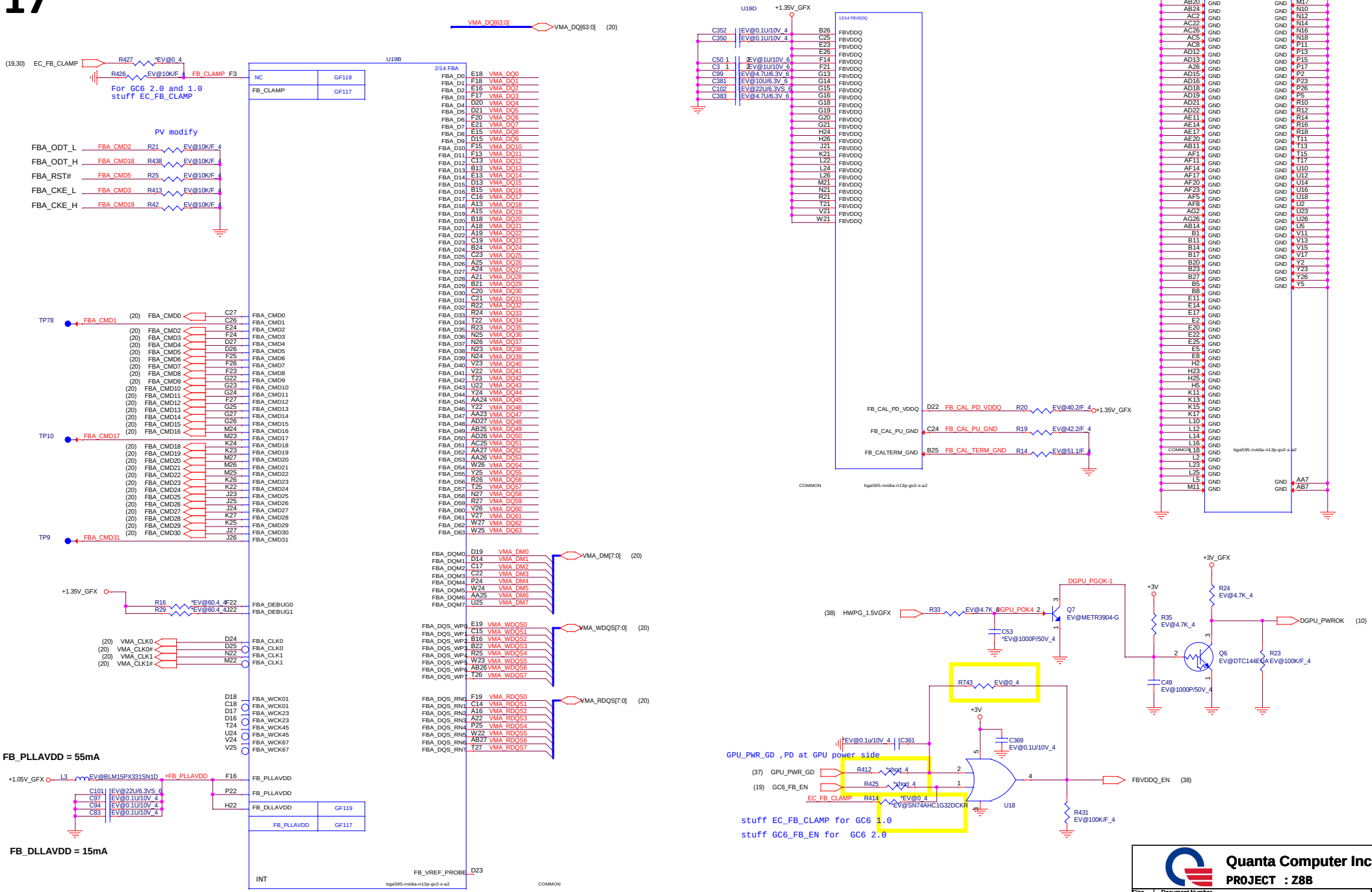


N15x Power on sequance

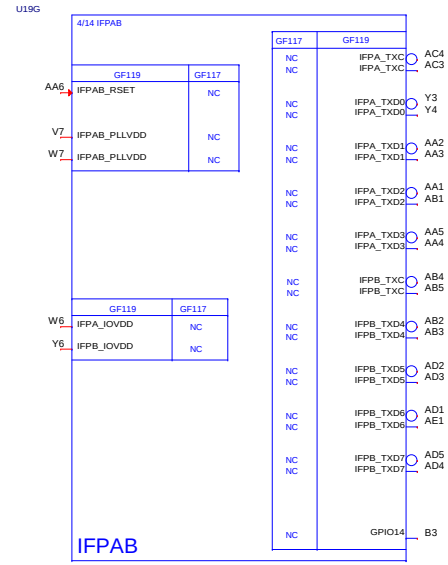
Quanta Computer Inc. PROJECT : Z8B			
Size	Document Number: N15S-GT (PCIE I/F) /NVDD		Rev: 1A
Date: Wednesday, July 09, 2014		Sheet 16 of 44	

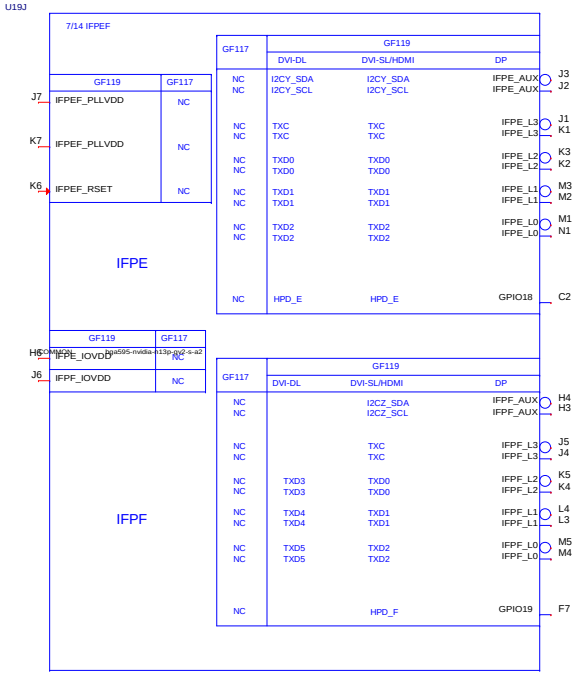
17

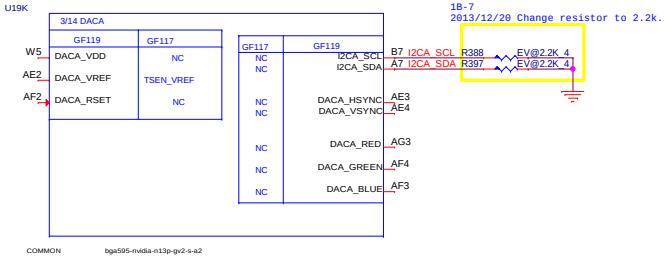
FBVDDQ + FBVDD = 3.116A

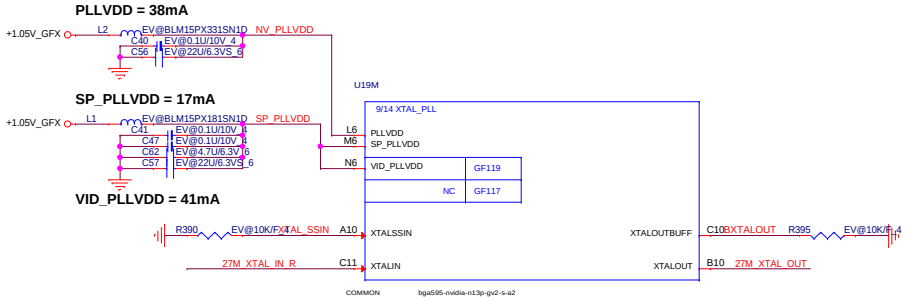


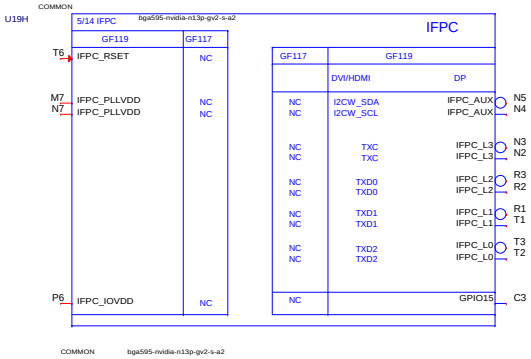
Quanta Computer Inc.			
PROJECT : Z8B			
Size	Document Number		Rev
	N15S-GT (MEMORY/GND)		1A
Date: Thursday, July 10, 2014		Sheet 17 of 44	

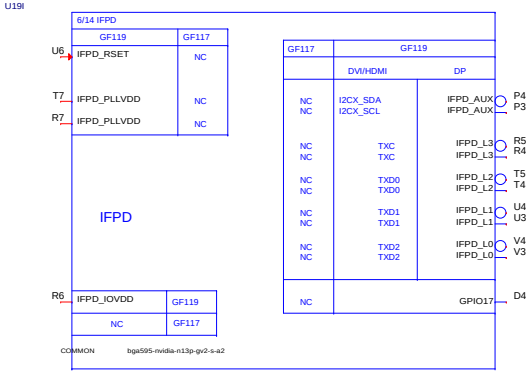


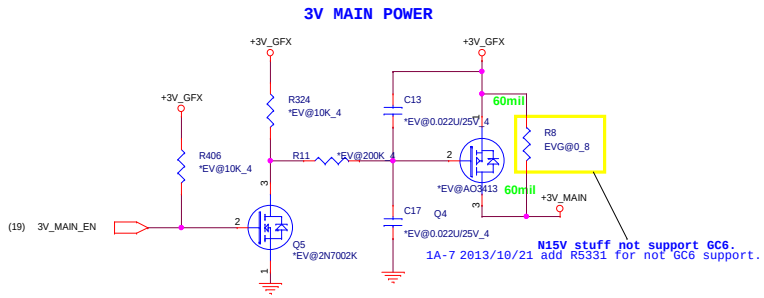


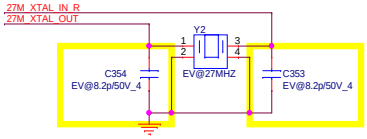


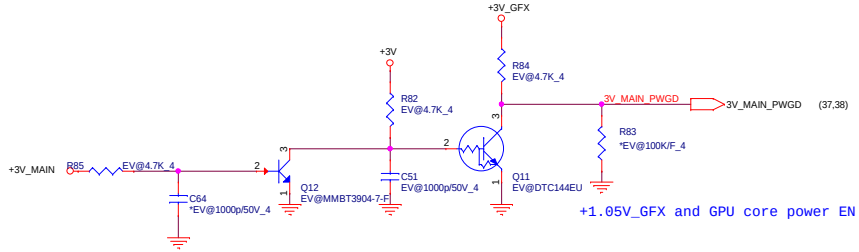










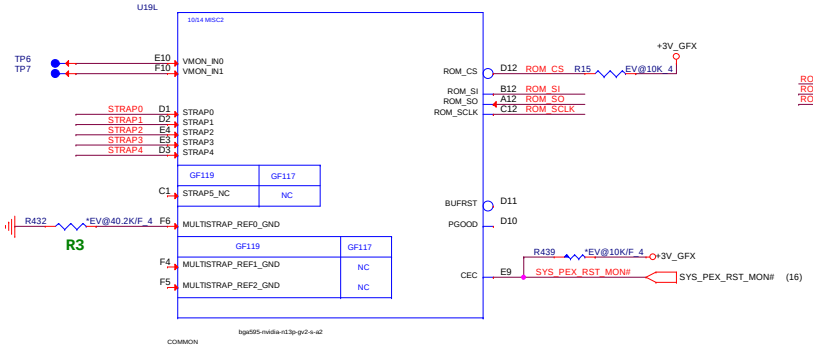


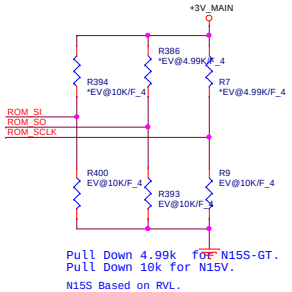
Quanta Computer Inc.
PROJECT : Z8B

Size	Document Number	Rev
	N15S-GT (DISPLAY)	1A
Date: Monday, July 14, 2014	Sheet 18 of 44	

For N15S-GT sku
N15S-GT device ID=0x0FE4
R3=40.3k pull down.
1.ROM_SCLK =4.99K pull down
2.ROM_SO = 4.99K pull down
3.ROM_SI= Memory strap setting
3.STRAP0 = 50k Pull pu.
4.Strap4~1 = reserve Pull pu
and Pull down

For N15V-GL-B and N15V-GM-B sku
Board_ID0=
H=N15V-GM,L=N15V-GL
Device ID=0x1140
R3= N.C.
1.ROM_SCLK =10K pull down.
2.ROM_SI= 10k pull down
3.ROM_SO= 10k pull down
4.Strap3~0 = RVL memory
binary mode setting.
5.Strap4 =10k pull down

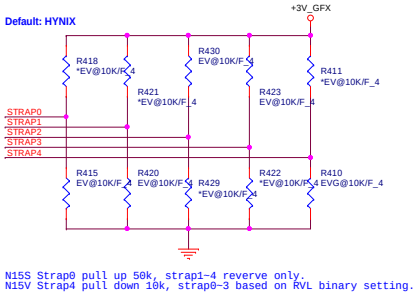




Pull Down 4.99k for N15S-GT.
Pull Down 10k for N15V.

N15S Based on RVL.
N15V pull down10k.

N15S-GT
STRAP1---> 50k PU
N15V-GMIGL
STRAP4---> 10k PD

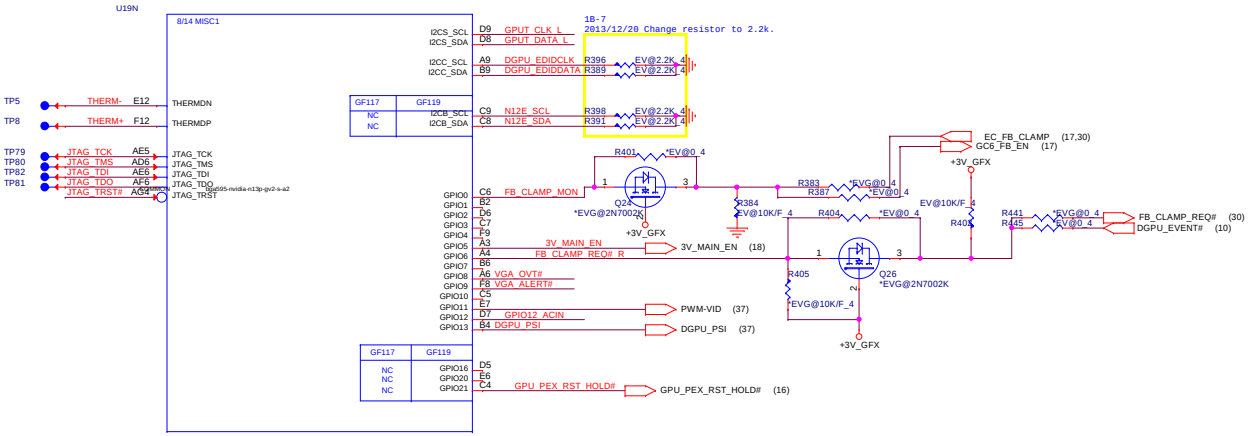


N15S Strap0 pull up 50k, strap1~4 reverve only.
N15V Strap4 pull down 10k, strap0~3 based on RVL binary setting.

Logical Strap Bit Mapping

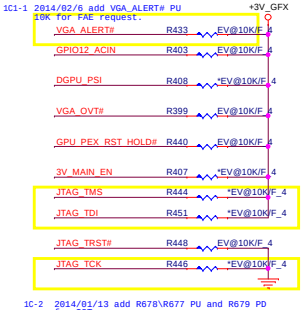
	PU-VDD	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

4.99k CS24992FB26
10k CS31002FB26
15k CS31502FB24
20k CS32002FB29
24.9k CS32492FB16
30.1k CS33012FB18
34.8k CS33482FB22
45.3k CS34532FB18



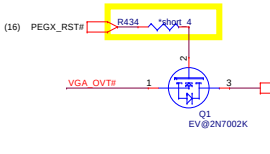
N15S -> GPIO0 un-stuff Q24 and EC_FB_CLAMP.
GPIO6 Un-stuff Q26\R70 and FB_CLAMP_REQ#.

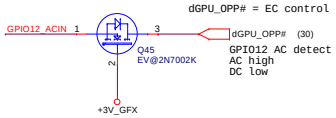
N15V -> GPIO0 stuff Q24 and EC_FB_CLAMP, un-stuff R75 GC6_FB_EN.
GPIO6 stuff Q26\R70 and FB_CLAMP_REQ#, un-stuff R76,FB_Clamp_req#.



GPIO ASSIGNMENTS

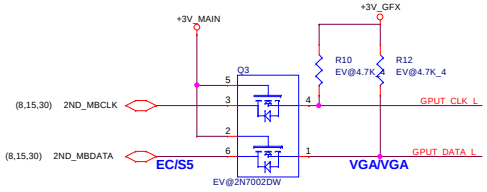
GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM VREF_CTL	MEMMORY VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding





dGPU_OPP# = EC control

GPIO12 AC detect
AC high
DC low



VRAM Configuration Table

ROM_SI	DESCRIPTION	Vendor	Vendor P/N	QCI P/N	STN P/N
0000	DDR3(L) 256MBx16x4, 64bit,1000MHz(	HYNIX	H5TC4G63AFR-11C	AKD5PGWTW05	AKD5PGWTW13
0010(0101)	DDR3(L) 256MBx16x4, 64bit, 1000MHz(900MHz)	SAMSUNG	K4W4G1646D-BC1A		
0110(1001)	DDR3(L) 128MBx16x4, 64bit,1000MHz(900MHz)	HYNIX	H5TC2G63FFR-11C		
0111(1010)	DDR3(L) 128MBx16x4, 64bit,1000MHz(900MHz)	MICRO	MT41J128M16JT-093G:K		
1000(1011)	DDR3(L) 128MBx16x4, 64bit,,1000MHz(900MHz)	SAMSUNG	K4W2G1646Q-BC1A		
1001(0100)	DDR3(L) 128MBx16x4, 64bit,1000MHz(900MHz)	MICRO	MT41J256M16HA-093G:E		

Strap [3:0]	DESCRIPTION	Vendor	Vendor P/N	QCI P/N		Note
0100	DDR3(L) 256MBx16x4, 64bit,1000MHz(900MHz)	HYNIX	H5TC4G63AFR-11C			
1100	DDR3(L) 128MBx16x4, 64bit,1000MHz(900MHz)	HYNIX	H5TC2G63FFR-11C			
0011	DDR3(L) 128MBx16x4, 64bit,1000MHz(900MHz)	MICRO	MT41J128M16JT-093G:K			
1101	DDR3(L) 128MBx16x4, 64bit,1000MHz(900MHz)	MICRO	MT41J256M16HA-093G:E			

Quanta Computer Inc.
PROJECT : Z8B

Size	Document Number	Rev
	N15S-GT (GPIO/STRAPS)	1A

Date: Wednesday, July 09, 2014 Sheet 19 of 44

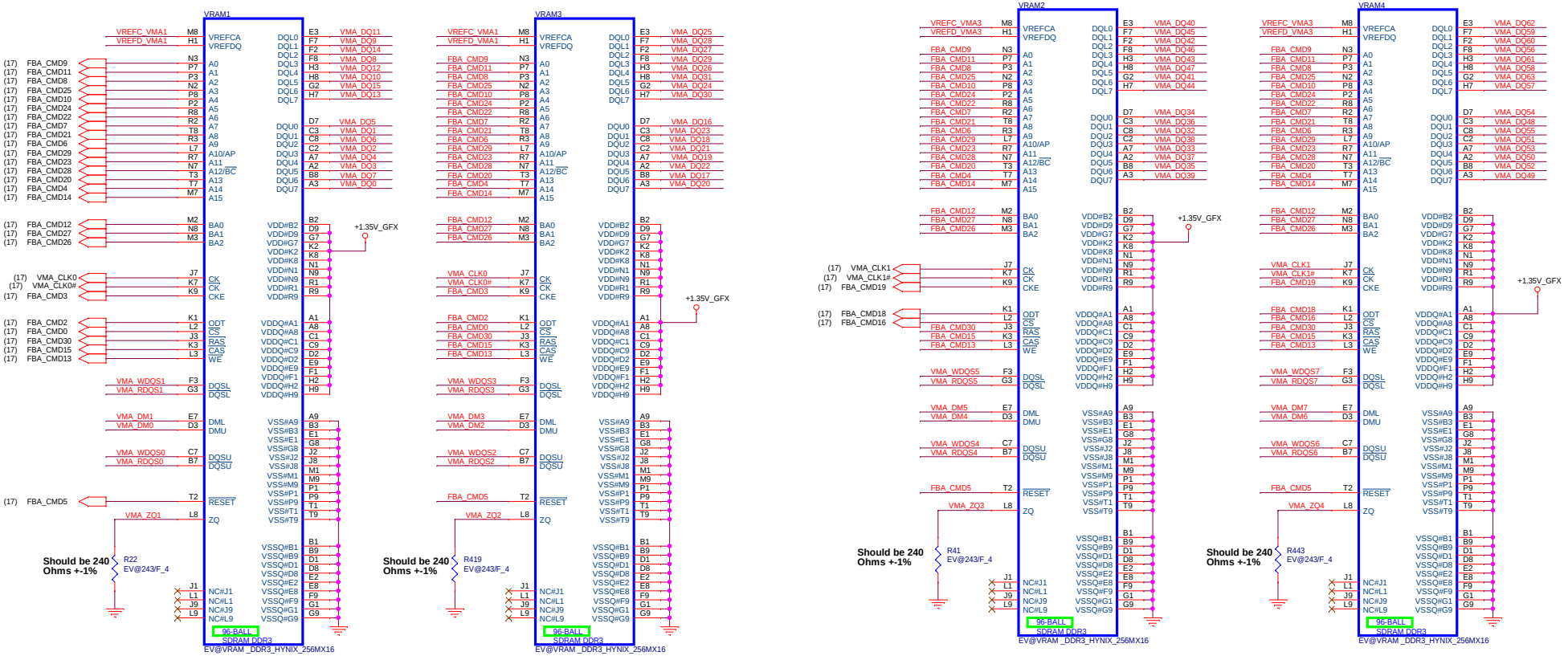
CHANNEL A: 256MB/512MB DDR3

(17) VMA_DQ[63..0]
(17) VMA_DM[7..0]
(17) VMA_WDQS[7..0]
(17) VMA_RDQS[7..0]

HYU 256Mx16, PN : AKD5PGWTW08---AKD5PGWTW07
HYU 128Mx16, PN : AKD5MZDTW03---AKD5MZDTW02

QBC TOP B/S

SAM 256Mx16, PN : AKD5PZDT501---AKD5PZDT500
SAM 128Mx16, PN : AKD5MGGT535---AKD5MGGT534



Quanta Computer Inc.
PROJECT : Z8B

Size	Document Number	Rev
	DGPU Memory (DDR3)	1A
Date: Tuesday, May 13, 2014	Sheet 20 of 44	

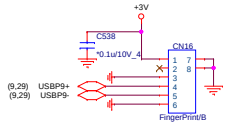
21

DP TO VGA

1A-1 2013/10/15 Change VGA ITE soltion to NXP.

1A-5 2013/10/18 Change VGA NXP soltion to ITE.

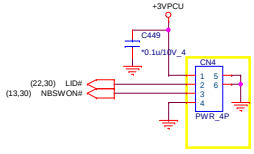
FingerPrint Conn



1A-7 2013/10/22 Change CN4 to 6pin.

1B-6 2013/12/18 Change CN5 USB port to port2.

Power Button/Conn

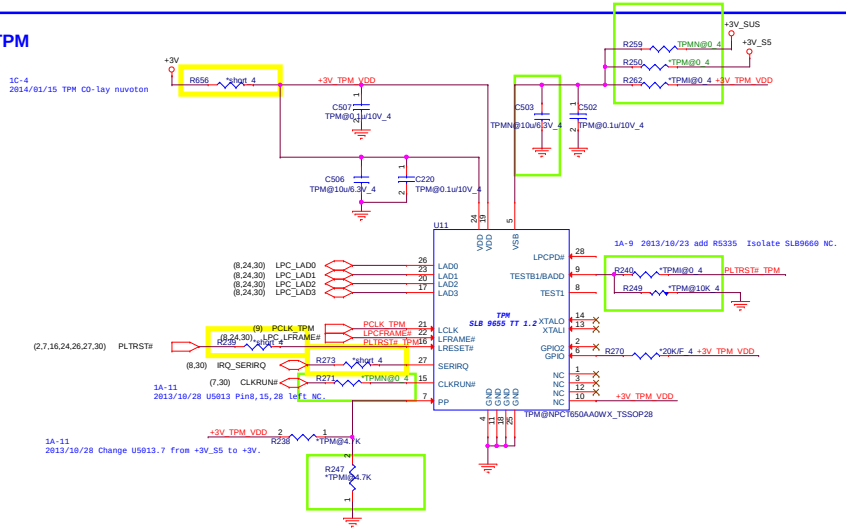


1A-1 2013/10/15 change to 6pin.

1B-2 2013/12/3 change to 4pin.

1B-3 2013/12/10 change CN6 footprint.

TPM



TPMI@-->for SLB9655 TPMN@-->for Nuvoton		
	SLB 9655	NPCT62x
R259	Un-stuff	stuff
C503	Un-stuff	stuff
R271	Un-stuff	stuff
R247	stuff	Un-stuff
R240	stuff	Un-stuff
R262	stuff	Un-stuff

Green CLK Gen

1B-4 2013/12/13 remove Green GLK U9

Quanta Computer Inc.		
PROJECT : Z8B		
Size	Document Number: ITE6513/TPM/FP/PB	Rev: 1A
Date: Wednesday, July 09, 2014	Sheet 21 of 44	

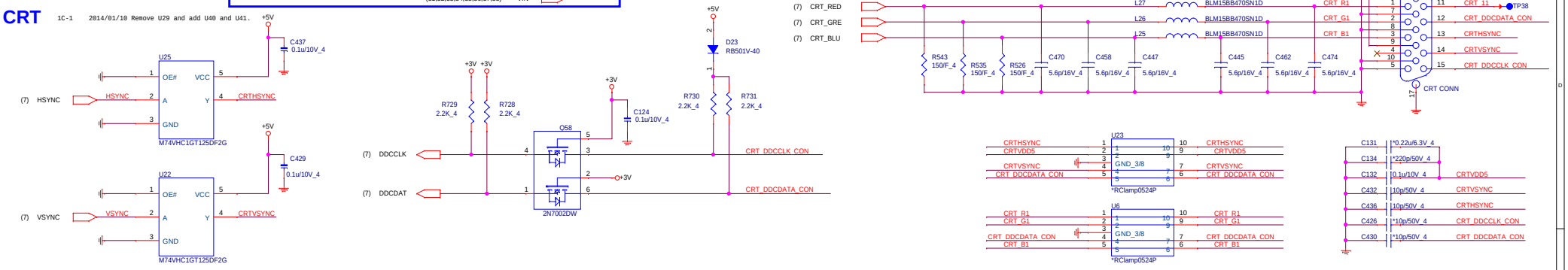
22

Power trace tracking

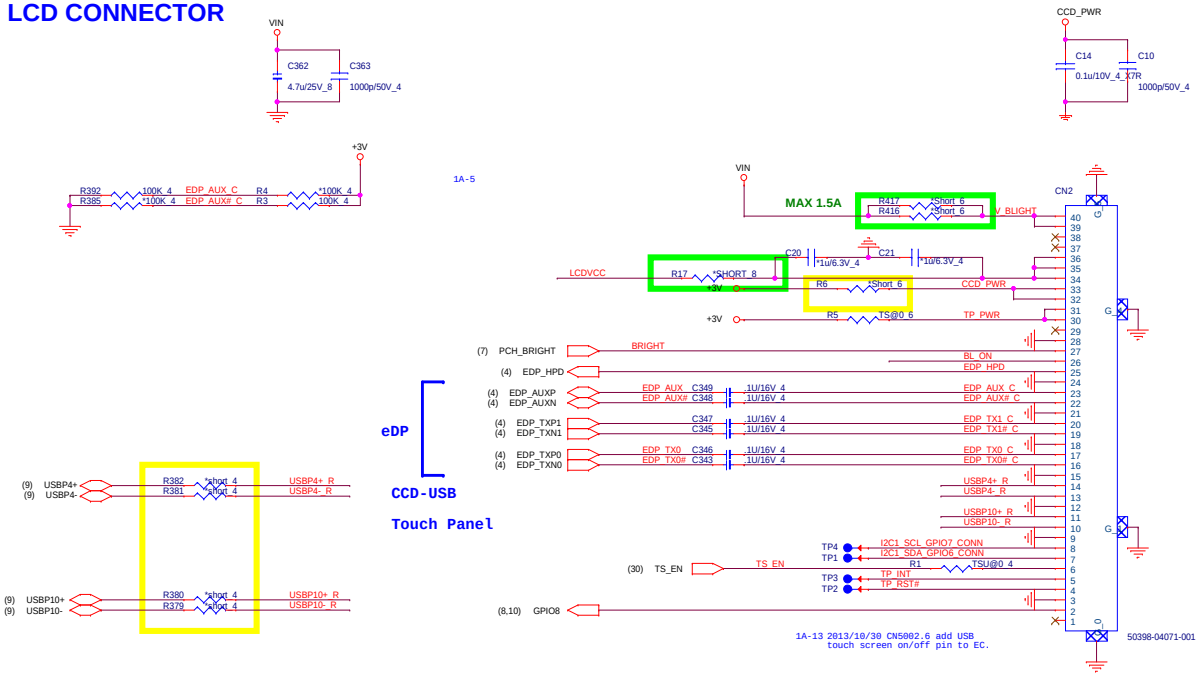
(2,7,8,9,10,11,13,14,15,16,17,18,21,23,24,25,26,27,28,29,30,32,33,34,35,36,37,38) +3V
(7,8,10,21,23,25,28,29,32,36) +5V
(7,8,11,21,25,27,28,29,30,31,32,36,37,38) +3VPCU
(31,32,33,34,35,36,37,38) VIN

CRT

1C-1 2014/01/10 Remove U29 and add U40 and U41.

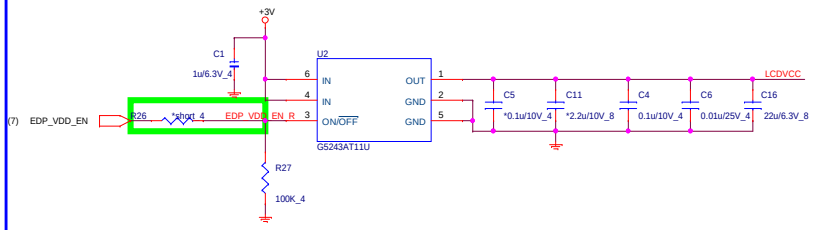


LCD CONNECTOR



1A-13 2013/10/30 CN5002_6 add USB touch screen on/off pin to EC.

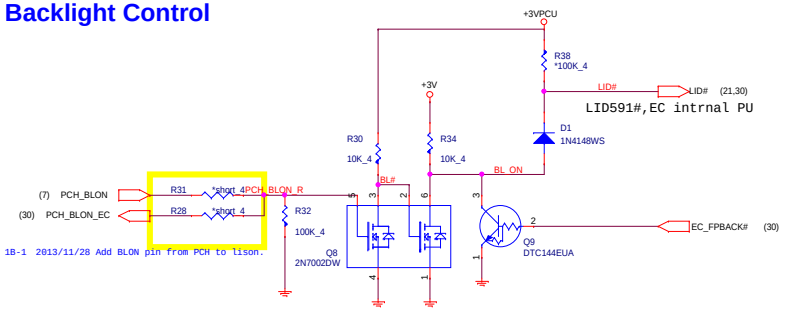
LCD Power



Touch screen level shift I2C(reserve)

TPD->100kHz,TS=400Khz
Intel design guide suggestion
MCP PIN 10u.
Per inch 3u TS=3x5inch
400kHz10~100u =2.4~0.4k.
100khz 10~100u=9k~1k.

Backlight Control



1B-1 2013/11/28 Add BLON pin from PCH to lison.

1B-3 2013/12/10 change Q3.3 from +3V to +3VPCU.

Quanta Computer Inc.
PROJECT : Z8B

Size	Document Number	Rev
	CRT/LVDS/CAMERA/LID	1A
Date: Monday, July 14, 2014	Sheet 22 of 44	

23

HDMI

From PCH

(4) INT_HDMITX2N
(4) INT_HDMITX2P
(4) INT_HDMITX1N
(4) INT_HDMITX1P
(4) INT_HDMITX0N
(4) INT_HDMITX0P
(4) INT_HDMICLK+
(4) INT_HDMICLK-

C521 0.1u/10V_4 INT_HDMITX2N_C
C522 0.1u/10V_4 INT_HDMITX2P_C
C519 0.1u/10V_4 INT_HDMITX1N_C
C520 0.1u/10V_4 INT_HDMITX1P_C
C523 0.1u/10V_4 INT_HDMITX0N_C
C525 0.1u/10V_4 INT_HDMITX0P_C
C518 0.1u/10V_4 INT_HDMICLK+_C
C517 0.1u/10V_4 INT_HDMICLK-_C

R674 R676 R321 R316 R307 R305 R314 R310
470_4

1B-1 20131108 Change +5V to +3V for DG.

+5V
R296 *100K/F_4
Q42 2N7002E

INT_HDMICLK+_C R301 *short_4 INT_HDMICLK+_CONN
INT_HDMICLK-_C R299 *short_4 INT_HDMICLK-_CONN

HDMI connector

CN9
INT_HDMITX0P_C
INT_HDMITX0N_C
INT_HDMITX1P_C
INT_HDMITX1N_C
INT_HDMITX2P_C
INT_HDMITX2N_C
INT_HDMICLK+_CONN
INT_HDMICLK-_CONN
HDMI_DDCCLK_MB
HDMI_DDCDATA_MB
HDMI_5V
HDMI_MB_HPD
HP_DET_CN
D2+ D2 Shield D2- D1+ D1 Shield D1- D0+ D0 Shield D0- CK+ CK Shield CK- CE Remote NC DDC CLK DDC DATA GND +5V HP DET
SHELL1 SHELL2 GND GND
HDMI connector

+5V Q40 IN OUT GND AP2331SA-7
C232 *220p/50V_4
D5 *AZ5125-01J
R280 *short_4
R284 20K_4

HDMI-detect

+3V R63 1M_4
(7) INT_HDMI_HPD
Q37 2N7002K
HDMI_MB_HPD

I2C

From PCH

(7) HDMI_DDCCLK_SW
(7) HDMI_DDCDATA_SW

+3V R47 2.2K_4
+5V D7 RB500V-40
R298 2.2K_4
Q43 2N7002K
HDMI_DDCCLK_MB

+3V R48 2.2K_4
+5V D4 RB500V-40
R294 2.2K_4
Q41 2N7002K
HDMI_DDCDATA_MB

EMI

INT_HDMITX2P_C R311 *120/F_4 INT_HDMITX2N_C
INT_HDMITX1P_C R306 *120/F_4 INT_HDMITX1N_C
INT_HDMITX0P_C R320 *120/F_4 INT_HDMITX0N_C
INT_HDMICLK+_C R675 *120/F_4 INT_HDMICLK-_C

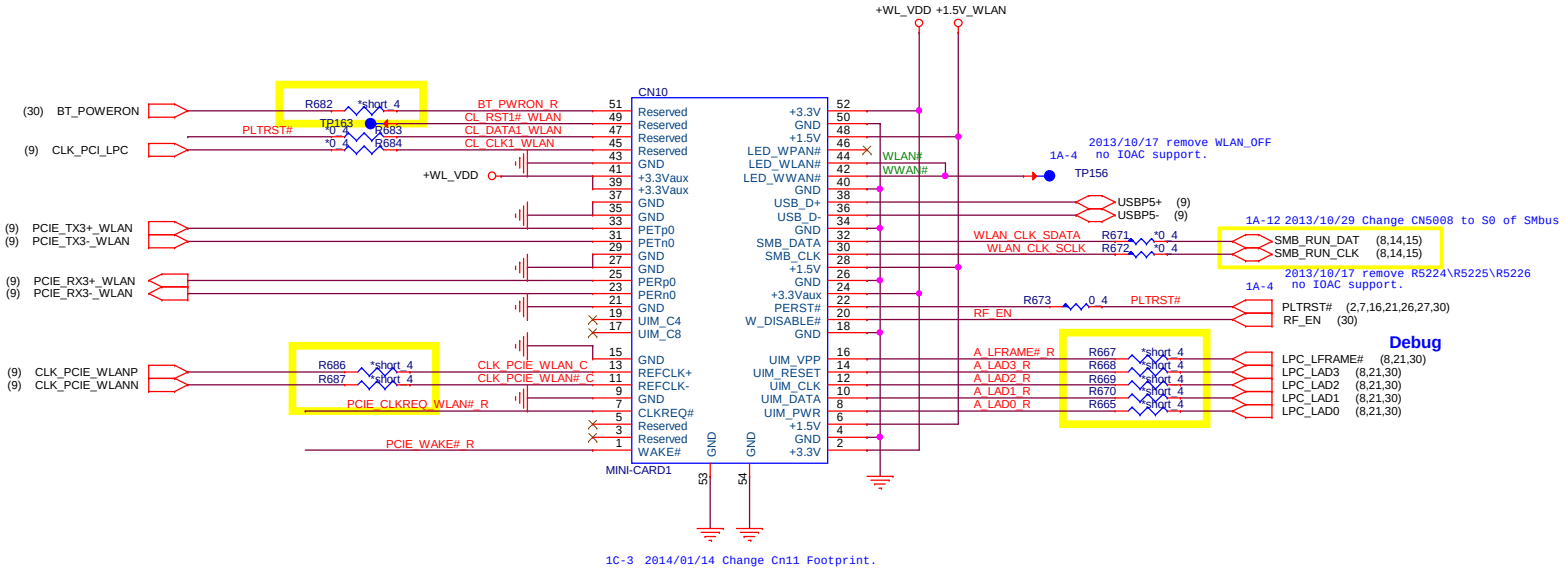
Power trace tracking

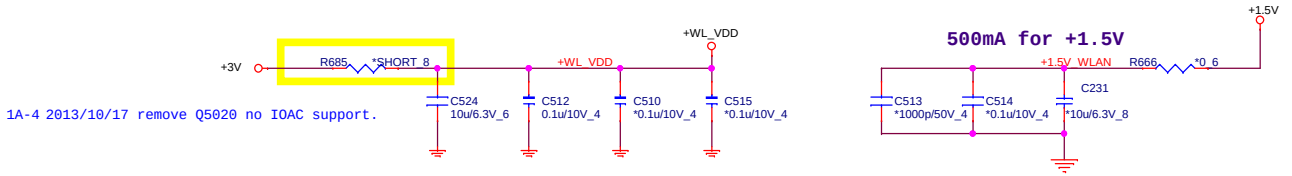
(2,7,8,9,10,11,13,14,15,16,17,18,21,22,24,25,26,27,28,29,30,32,33,34,35,36,37,38) +3V
(7,8,10,21,22,25,28,29,32,36) +5V

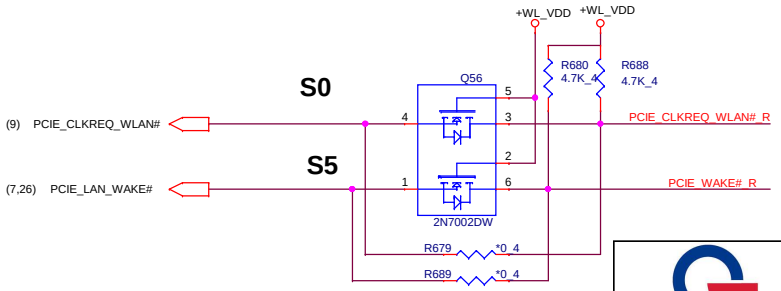
Quanta Computer Inc.
PROJECT : Z8B

Size	Document Number	Rev
	HDMI (PS8101)	1A
Date: Wednesday, July 09, 2014	Sheet 23 of 44	

24 Mini Card 1 (MNC)



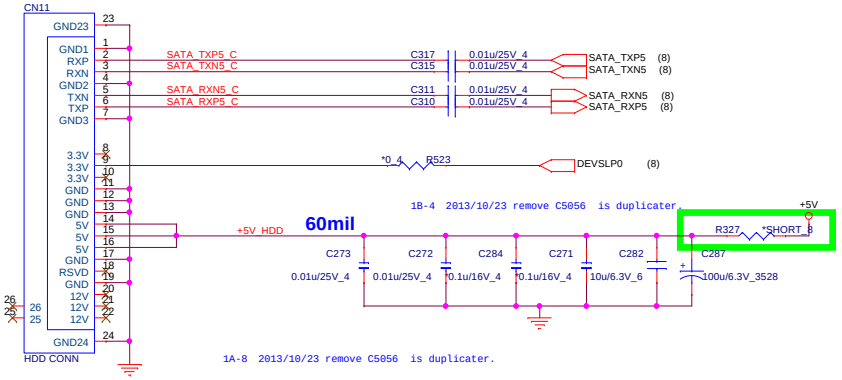




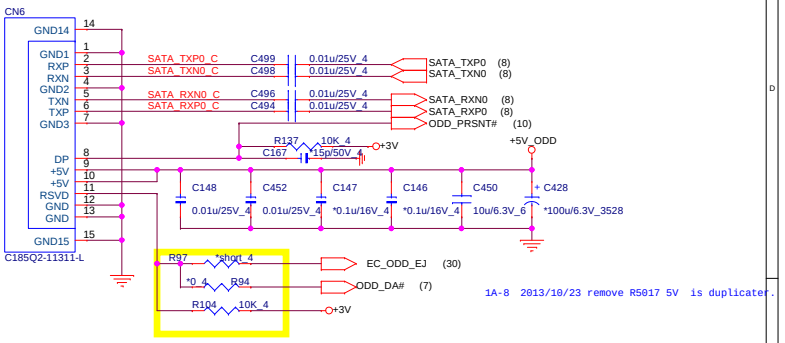
Quanta Computer Inc.
PROJECT : Z8B

Size	Document Number	Rev
	Mini-Card/WL/3G/SIM	1A
Date: Wednesday, July 09, 2014	Sheet 24 of 44	

25 2.5" SATA HDD (HDD)

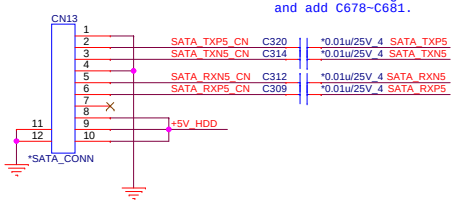


SATA ODD Connector



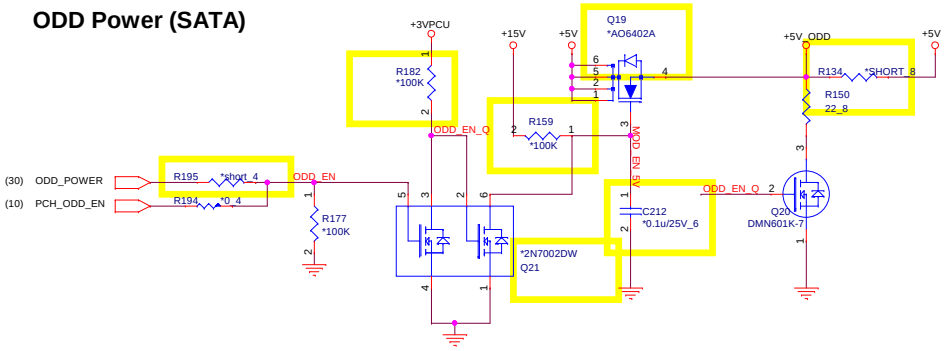
FFC Type SATA HDD CON

1C-2 2014/01/13 change CN14 sata net name and add C678~C681.



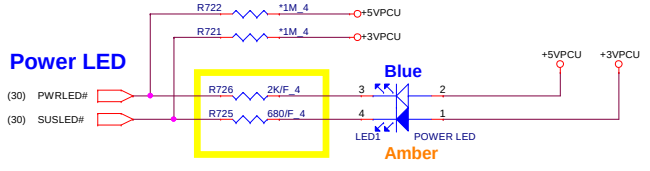
1B-3 2013/12/10 change Cn20 Pin define.

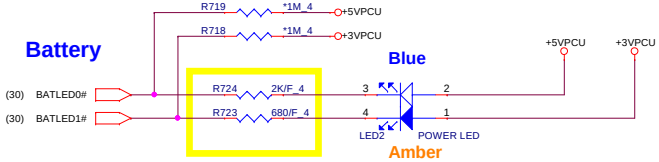
ODD Power (SATA)



POWER LED

1A-9 2013/10/17 Change power LED from +3VPCU to +3V_S5.
1A-10 2013/10/25 change LED from 3pin to 4pin. for acer request.
1A-11 2013/10/28 change LED from 4pin to 3pin. and power LED to +3VPCU.
1B-2 2013/12/03 change LED from 3pin to 4pin.
1C1-1 2014/02/06 change Blue LED power rail to +5VPCU.



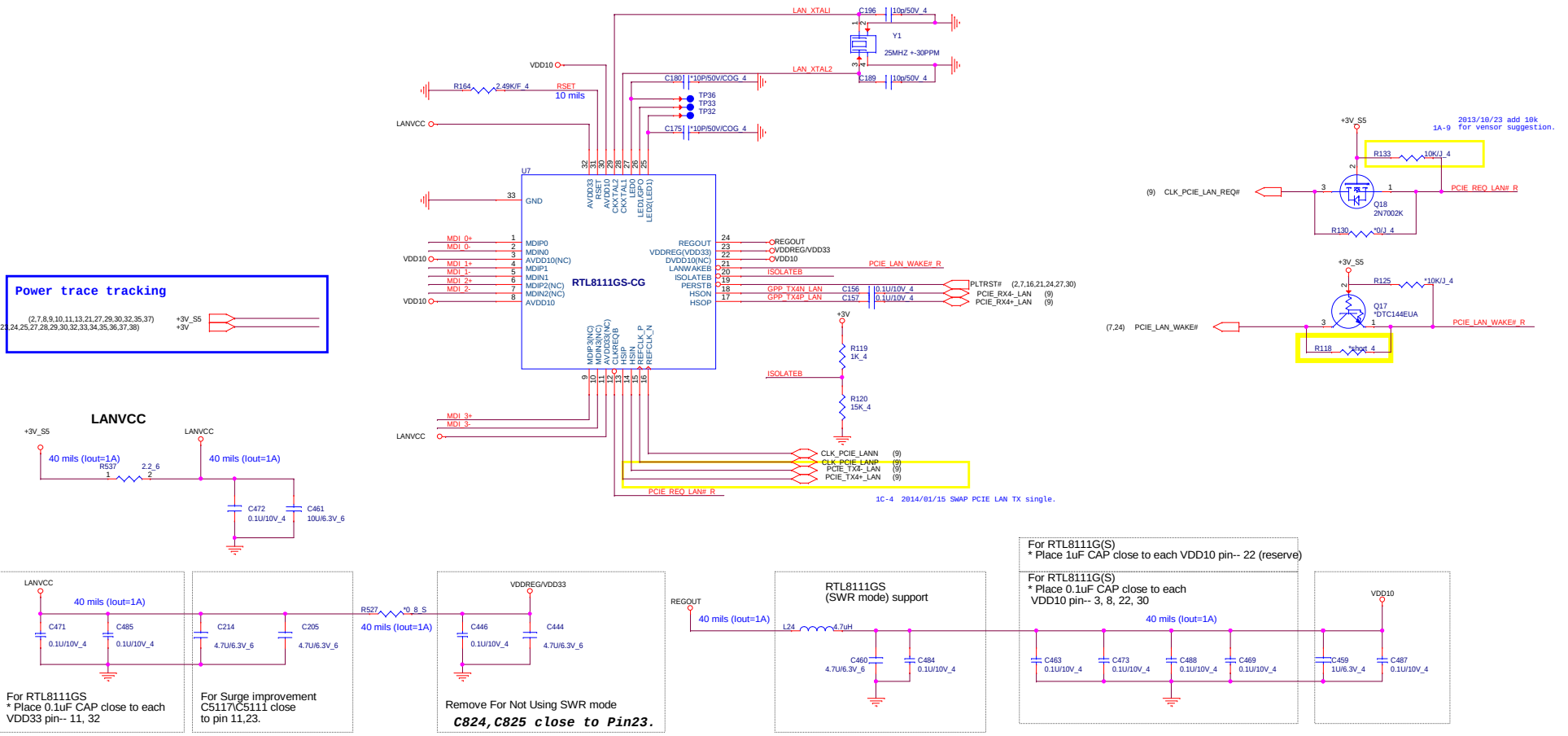


Quanta Computer Inc.
PROJECT : Z8B

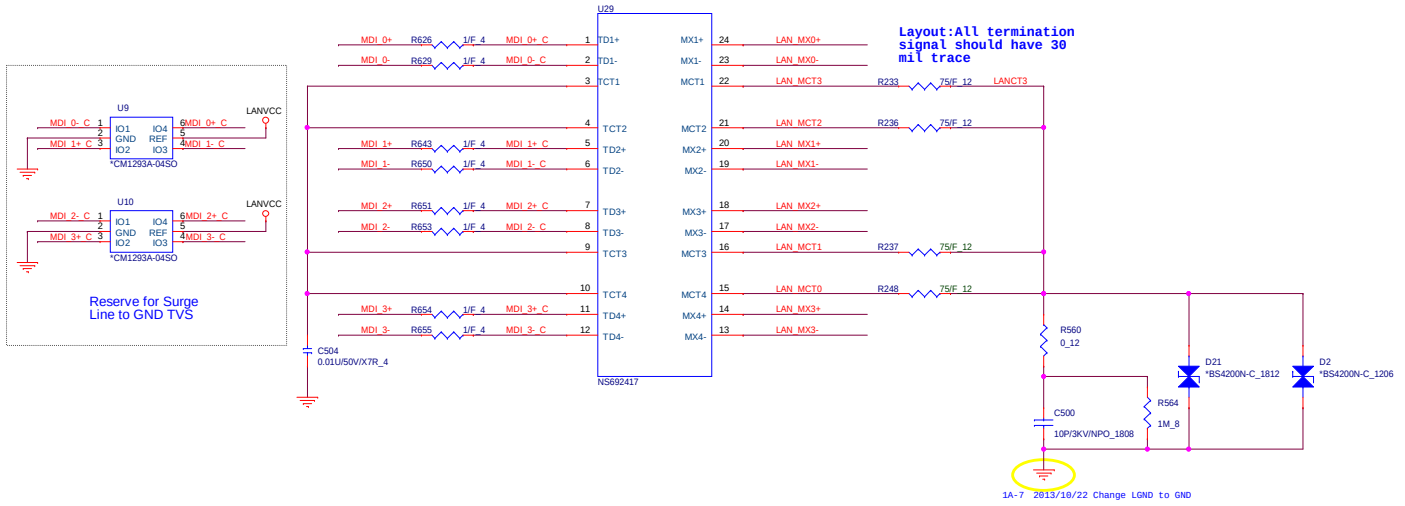
Size	Document Number	Rev
	SATA HDD/LED/SW	1A
Date: Monday, July 14, 2014	Sheet 25 of 44	

26

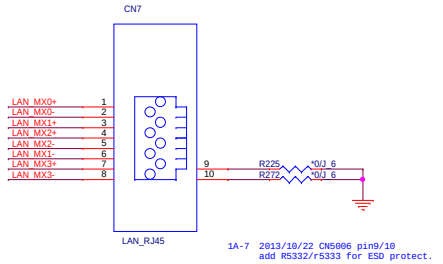
LAN



Tramsformer



RJ45 Connector



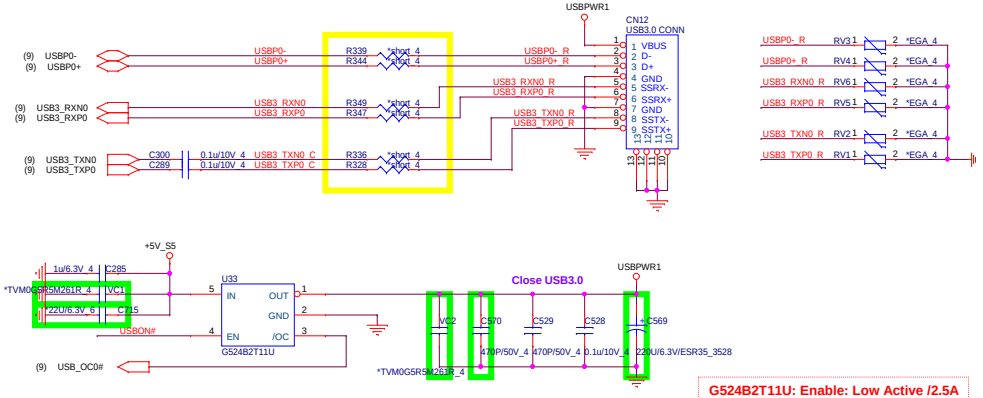
Quanta Computer Inc.
PROJECT : Z8B

Size	Document Number	Rev
	LAN (RTL8111GS)	1A
Date: Tuesday, July 15, 2014	Sheet 26 of 44	

27

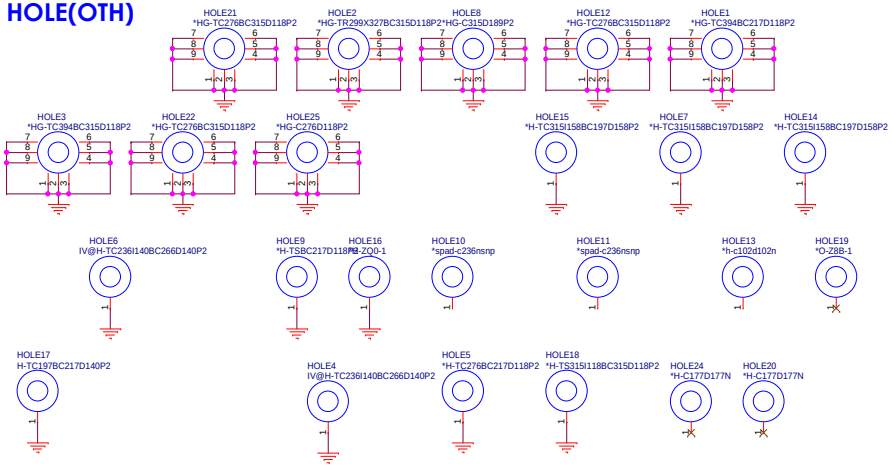
1B-6 2013/12/18 Change CN12 USB2.0 port to port0.

USB 3.0 Connector

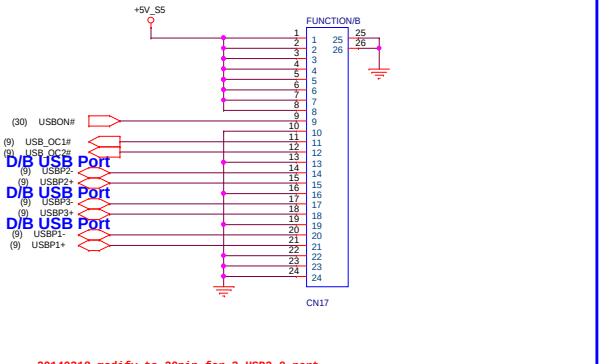


G524B2T11U: Enable: Low Active /2.5A

HOLE(OTH)

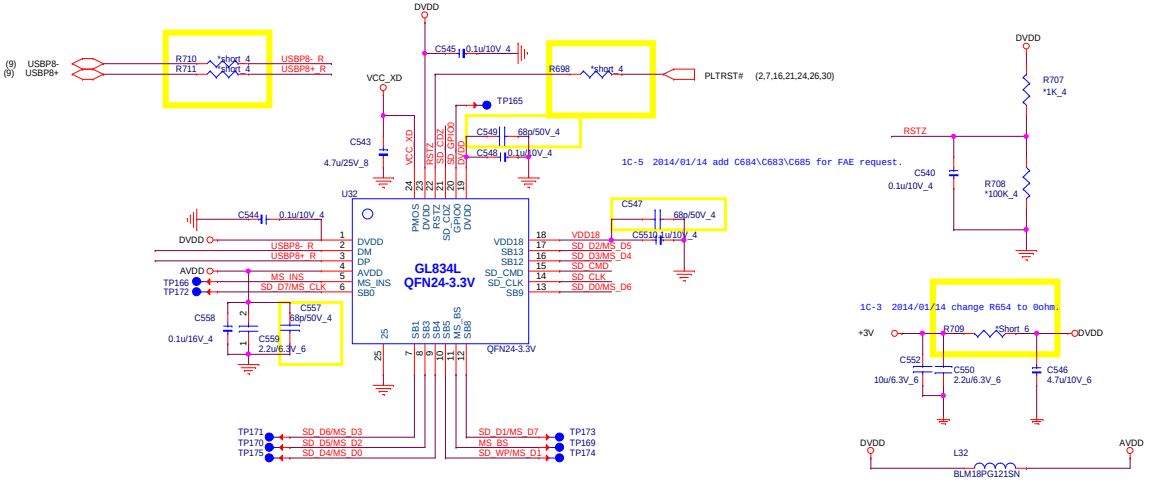


USB IO D/B

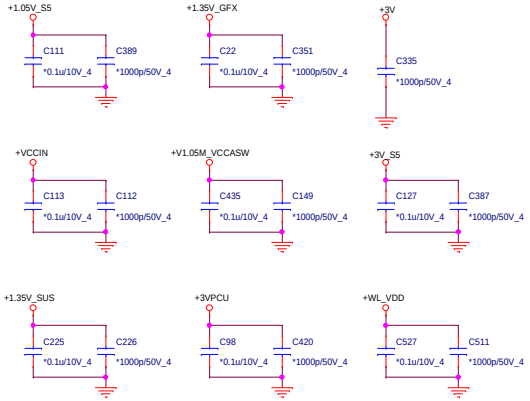


20140318 modify to 20pin for 3 USB2.0 port

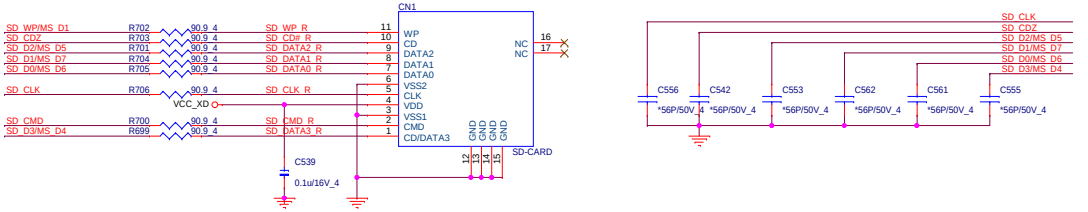
Card Reader and Connector



EMI

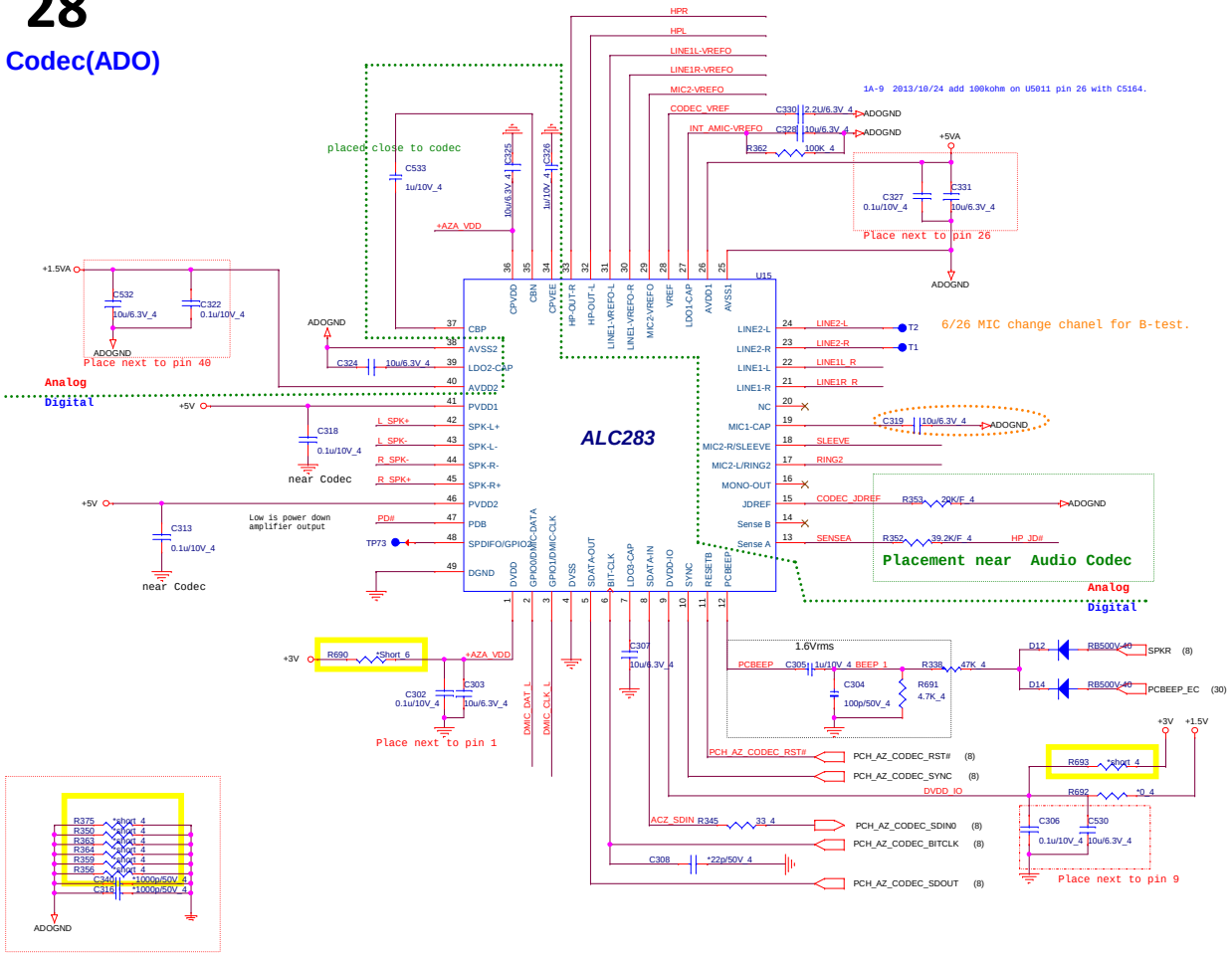


SD/MMC CARD READER (CRD)

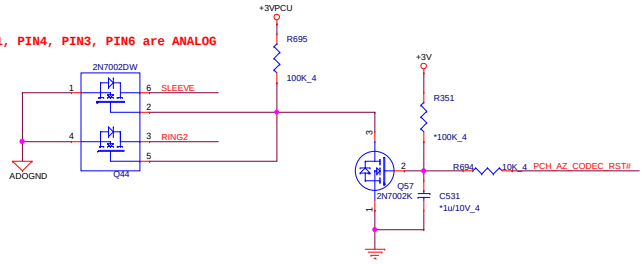


Quanta Computer Inc.		
PROJECT : Z8B		
Size	Document Number: USB Port/ DB	Rev: 1A
Date: Tuesday, July 15, 2014	Sheet 27 of 44	

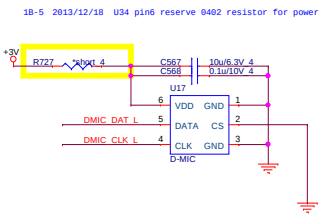
Codec(ADO)



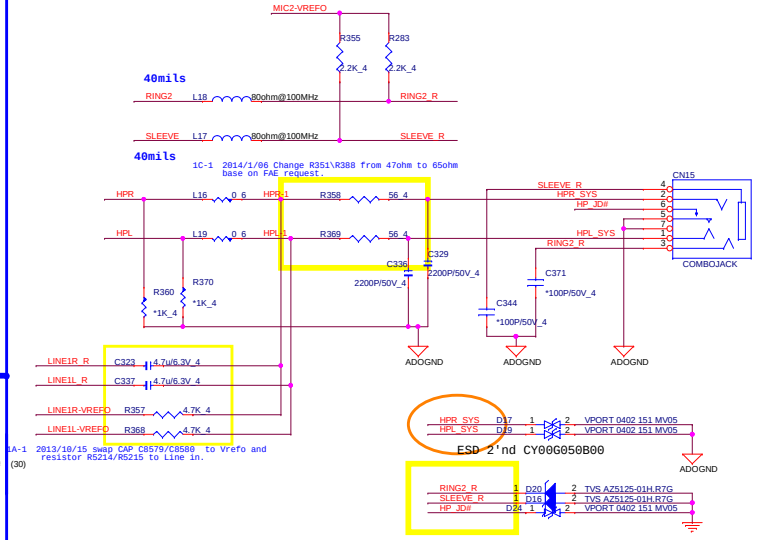
Grounding circuit(ADO)



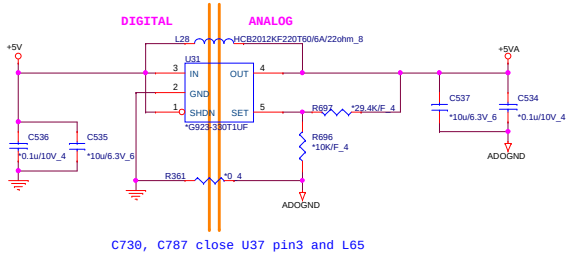
D-Mic



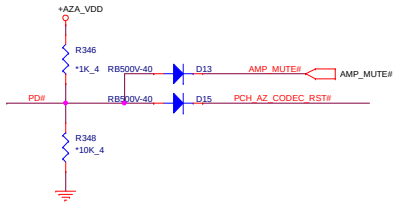
Universal Audio Jack



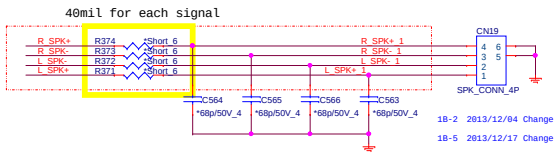
Codec PWR 5V(ADO)



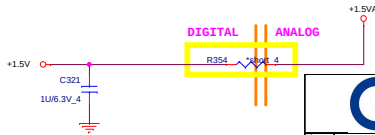
Mute(ADO)



Internal Speaker



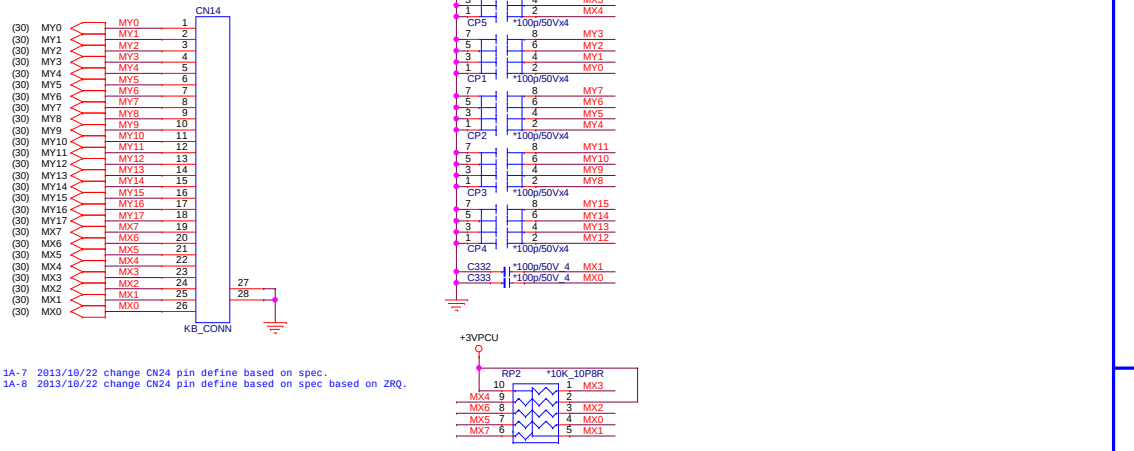
Codec PWR 3V/1.5V(ADO)



Quanta Computer Inc.		
PROJECT : Z8B		
Size	Document Number: ALC283/HP/SPK	Rev: 1A
Date: Tuesday, July 15, 2014	Sheet 28 of 44	

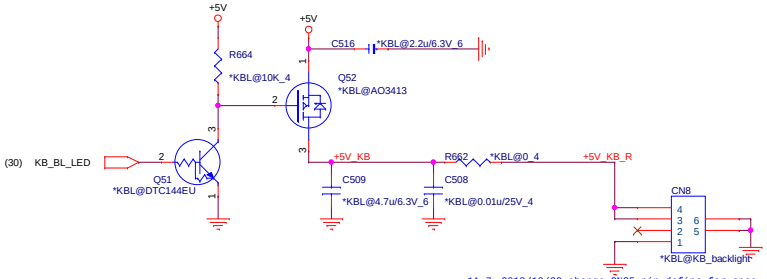
29

K/B (KBC)



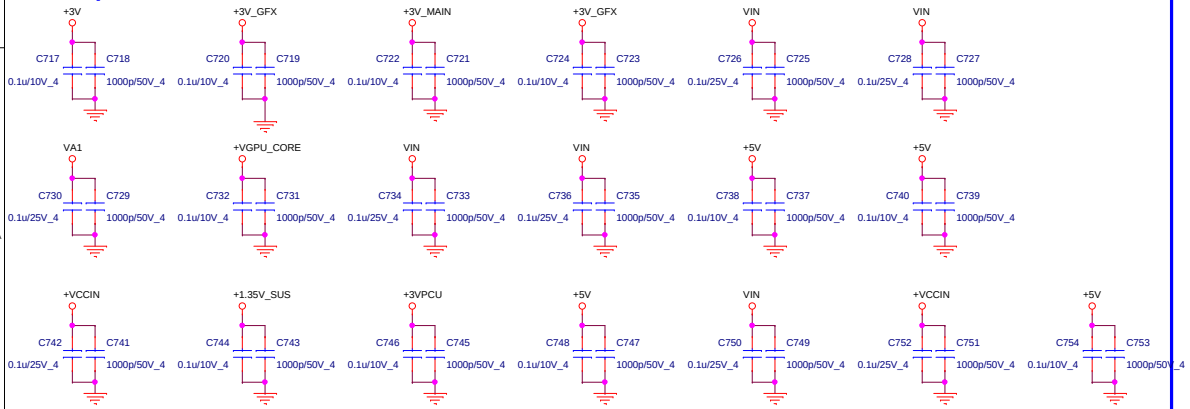
1A-7 2013/10/22 change CN24 pin define based on spec.
1A-8 2013/10/22 change CN24 pin define based on spec based on ZRQ.

KB_BL LED (KBC)



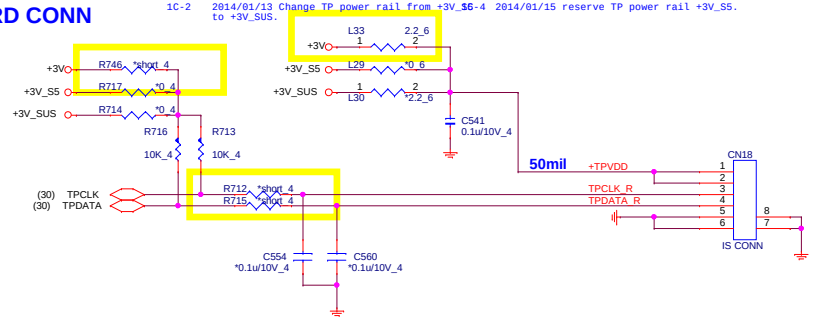
1A-7 2013/10/22 change CN25 pin define for spec.
1A-8 2013/10/23 change CN25 footprint.

EMI Cap



TOUCHPAD BOARD CONN

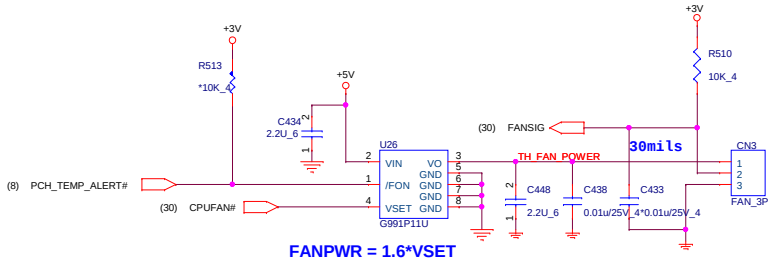
1C-2 2014/01/13 Change TP power rail from +3V_S5 to +3V_SUS.
1A-4 2014/01/15 reserve TP power rail +3V_S5.



TPD->100kHz,TS=400Khz
Intel design guide suggestion
MCP PIN 10u.
Per inch 3u TS=3x5inch
400kHz10~100u =2.4~0.4k.
100Khz 10~100u=9k~1k.

1A-5 2013/10/18 Change CN21 Pin8 for I2C/PS2 TPD idendify.
2013/10/29 Change CN21 power rail to S5 change Q42 direction and net name,
1A-12 reseve PS2 PU to +3V.

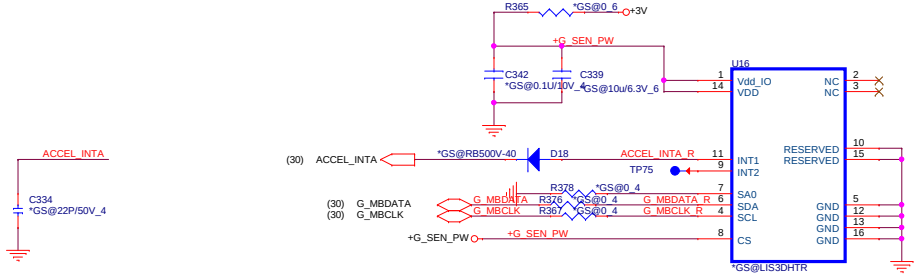
CPU FAN (THM)

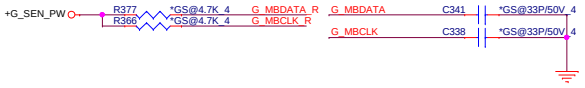


FANPWR = 1.6*VSET

1A-1 2013/10/15 change pin define and add pwm IC U17.
1A-11 2013/10/15 change U17 to G991P11U and PU U17 pin1.
1A-9 2013/10/24 Add alert on U17.1 for CPU themal tempture.

Accelerometer Sensor(reserve only)





Quanta Computer Inc.
PROJECT : Z8B

Size	Document Number	Rev
	KB/TP/FAN	1A

Date: Monday, July 14, 2014 Sheet 29 of 44

EC(KBC)

+3VPCU_EC and +3V_RTC minimum trace width 12mils.

12 mils

12 mils

(For PLL Power)

IT8587

IT8587E/FX

LPC

GPIO

SM BUS

PS/2

CIR

PWM

UART port

WAKE UP

EXTERNAL SERIAL FLASH

SPI ENABLE

KBMX

A/D D/A

CLOCK

1B-1 2013/11/28 Add BLON pin from PCH to lison.

2013/10/18 change U27.87 for Touch pad IO for I2C/PS2 solution switch.

1A-1 2013/10/15 del fan Pwm

2013/10/29 add U27.35 for touch pad on/off.

1A-12 2013/10/29 add U27.68 for touch pad interrupt.

1A-12 2013/10/29 Swap U27 pin2 and pin128.
1B-1 2013/11/27 connecto to GND of pin128.

Please do not place any pull-up resistor on GPG0, GPG2, and GPG6 (Reserved hardware strapping).

SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH/VGA
SM Bus 3	G-Snesor
SM Bus 4	

Add R732,R733

SM BUS PU(KBC)

HWPG(KBC)

For test only

*Power Switch

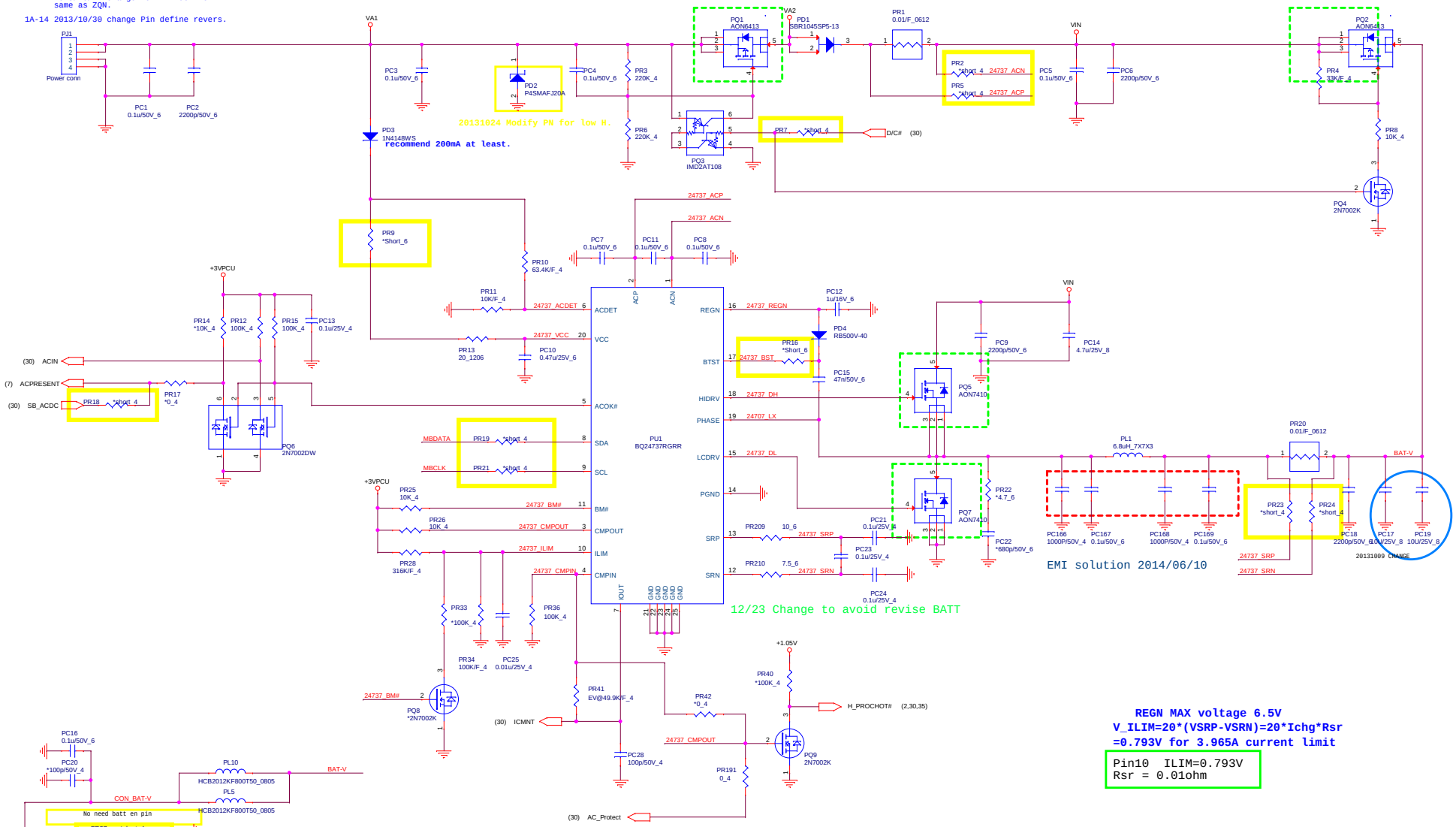
iRST

1A-4 2013/10/17 Del U22 becuse no support IOAC

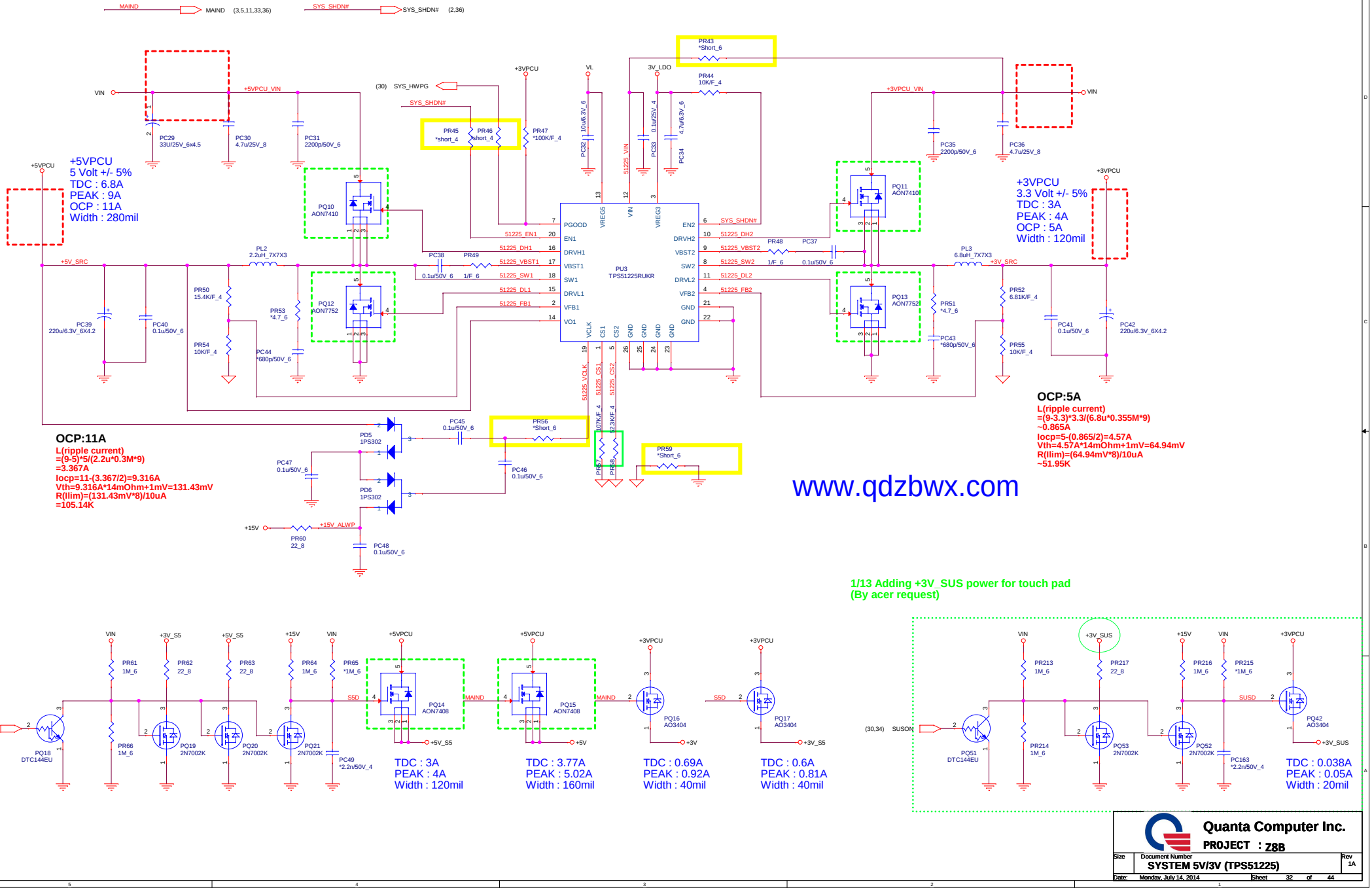
Quanta Computer Inc.
PROJECT : Z8B
Size | Document Number: KBC IT8587 | Rev: 1A
Date: Tuesday, June 10, 2014 | Sheet 30 of 44

1A-7 2013/10/22 change PJ1 Pin define same as ZQN.

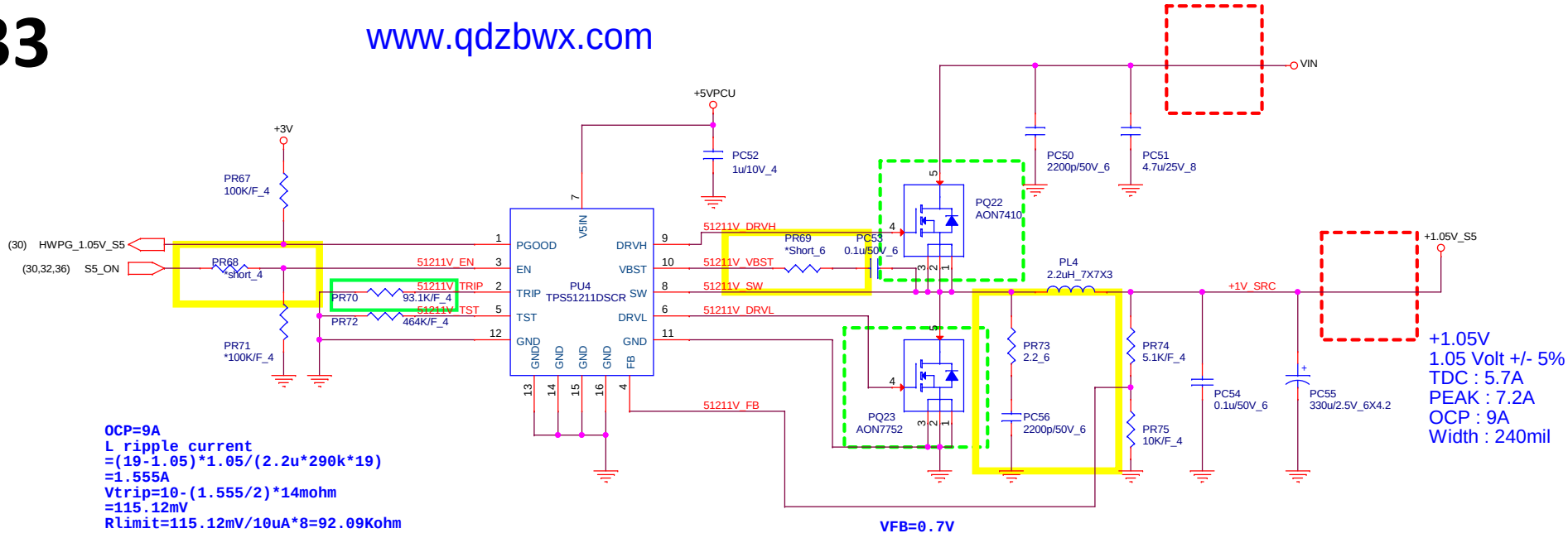
1A-14 2013/10/30 change Pin define revers.



Quanta Computer Inc.		
PROJECT : Z8B		
Size	Document Number: Charger(BQ24737RGRR)	Rev 1A
Date: Tuesday, July 15, 2014	Sheet 31 of 44	



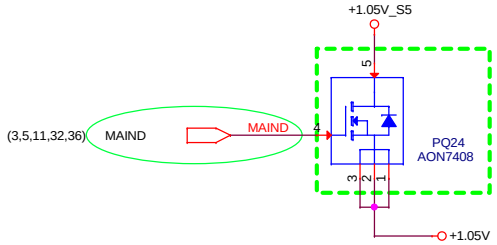
Quanta Computer Inc.			
PROJECT : Z8B			
Size	Document Number		Rev
	SYSTEM 5V/3V (TPS51225)		1A
Date: Monday, July 14, 2014		Sheet 32 of 44	



+1.05V
1.05 Volt +/- 5%
TDC : 5.7A
PEAK : 7.2A
OCP : 9A
Width : 240mil

OCP=9A
L ripple current
=(19-1.05)*1.05/(2.2u*290k*19)
=1.555A
Vtrip=10-(1.555/2)*14mohm
=115.12mV
Rlimit=115.12mV/10uA*8=92.09Kohm

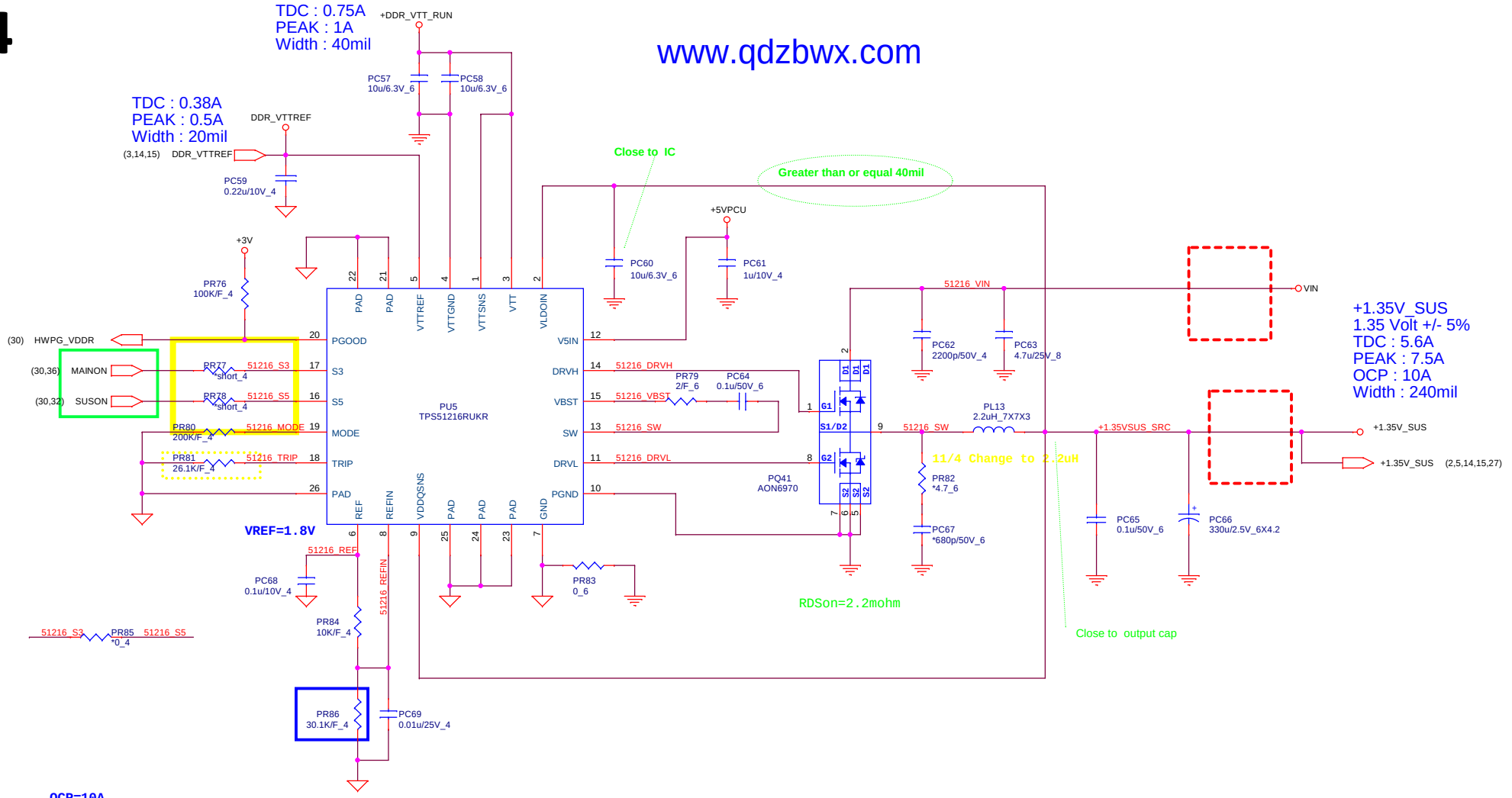
VFB=0.7V



1B-2 2013/12/03 change PQ24 to DFN 3x3 size

TDC : 2.4A
PEAK : 3.2A
Width : 100mil

Quanta Computer Inc. PROJECT : Z8B		
Size	Document Number: +1.05V_S5 (TPS51211)	Rev: 1A
Date: Monday, July 14, 2014	Sheet 33 of 44	



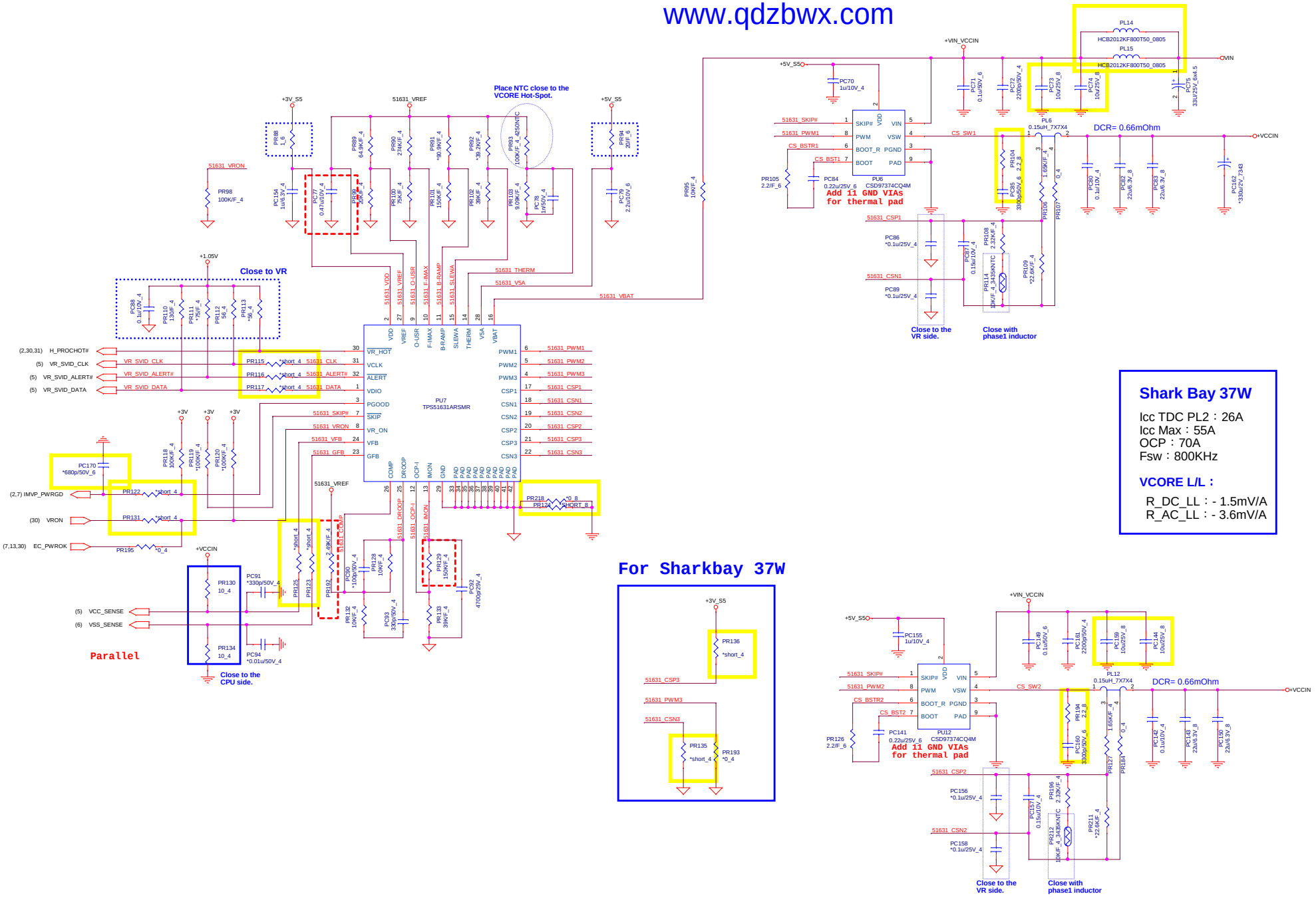
OCP=10A
L ripple current
=(19-1.35)*1.35/(2.2u*400k*19)
=1.425A
Vtrip=10-(1.425/2)*2.2mohm
=20.432mV
Rlimit=20.432mV/10uA*8=16.35Kohm

DDR=1.35V
PR84=10K/F_4
PR86=30.1K/F_4

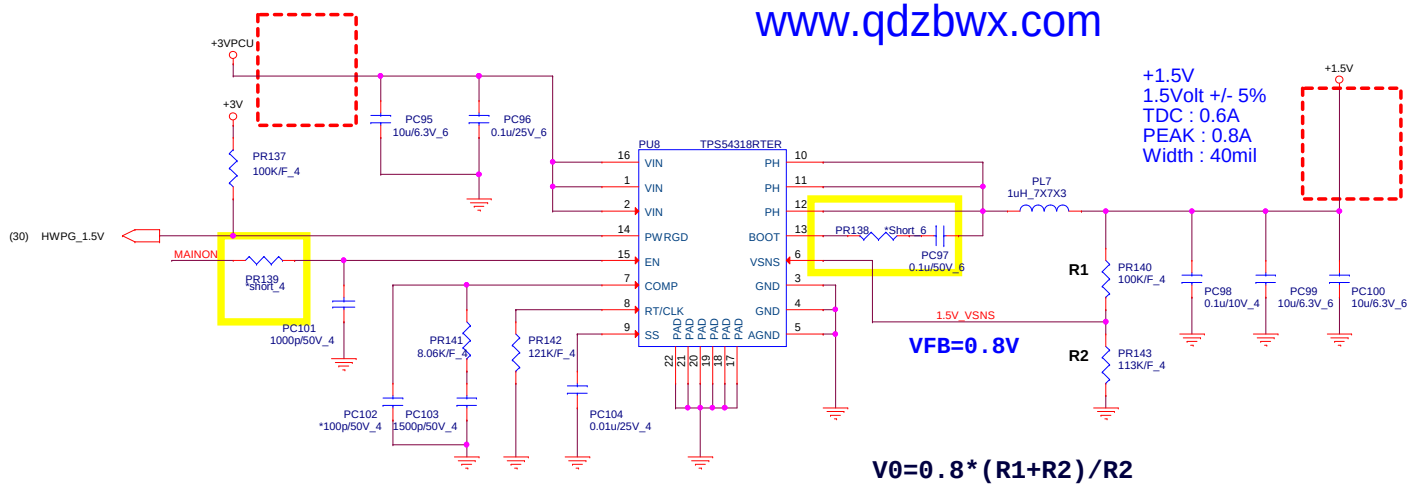
Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.
PROJECT : Z8B
Size | Document Number: DDR 1.35V(TPS51216) | Rev 1A
Date: Monday, July 14, 2014 | Sheet 34 of 44



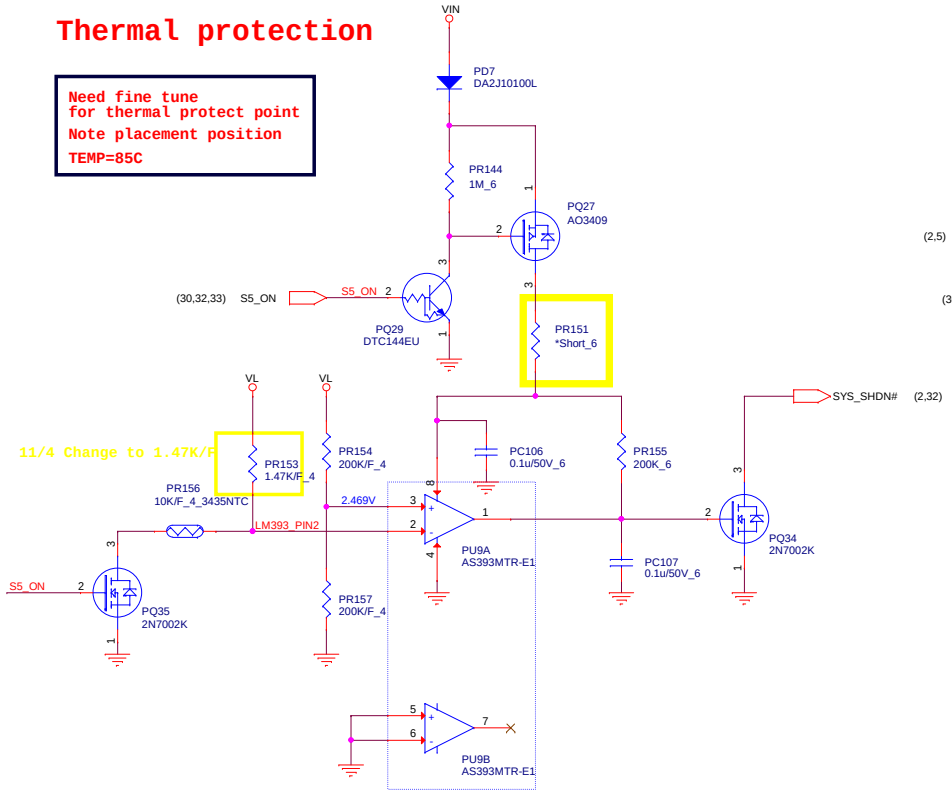
Quanta Computer Inc.	PROJECT : Z8B
Size	Document Number: +VCCIN(TPS51631) — Rev 1A
Date: Tuesday, July 15, 2014	Sheet 35 of 44

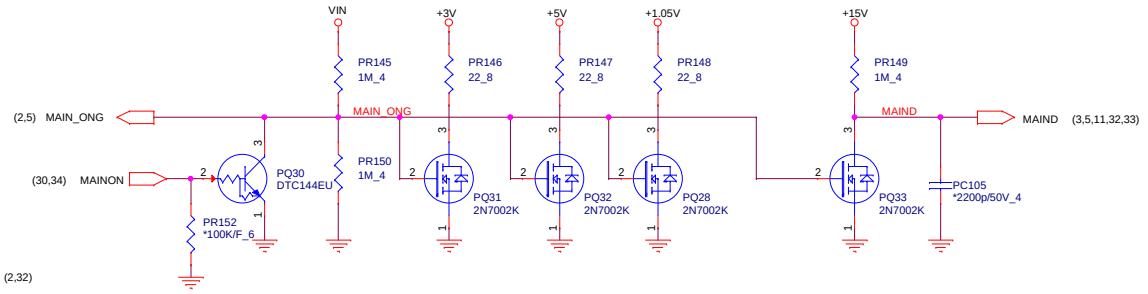


V0=0.8*(R1+R2)/R2

Thermal protection

Need fine tune
for thermal protect point
Note placement position
TEMP=85C

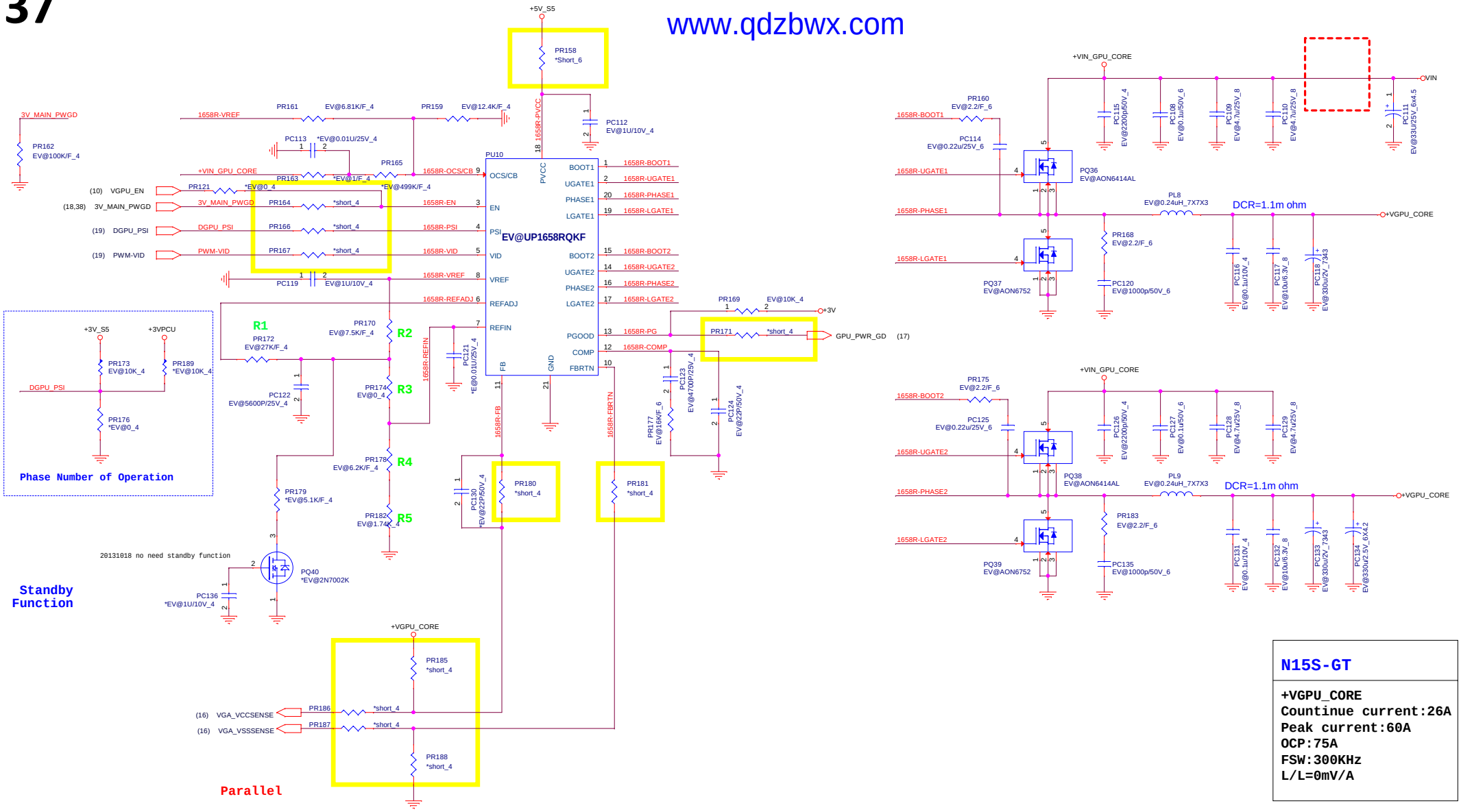




For EC control thermal protection (output 3.3V)

Quanta Computer Inc.
PROJECT : Z8B

Size	Document Number	Rev
	+1.5V/Thermal Protect	1A
Date: Monday, July 14, 2014	Sheet 36 of 44	



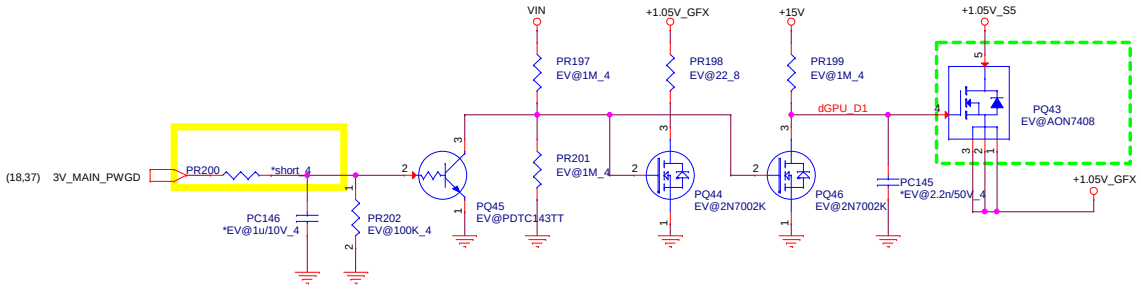
N15S-GT

+VGPU_CORE
Countinue current:26A
Peak current:60A
OCP:75A
FSW:300KHz
L/L=0mV/A

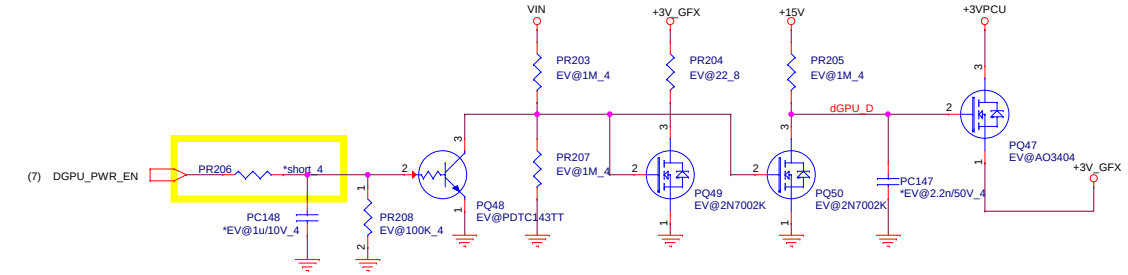
Quanta Computer Inc.
PROJECT : Z8B

Size	Document Number	Rev
	+VGPU_CORE(UP1642PQAG)	1A
Date: Monday, July 14, 2014	Sheet 37 of 44	

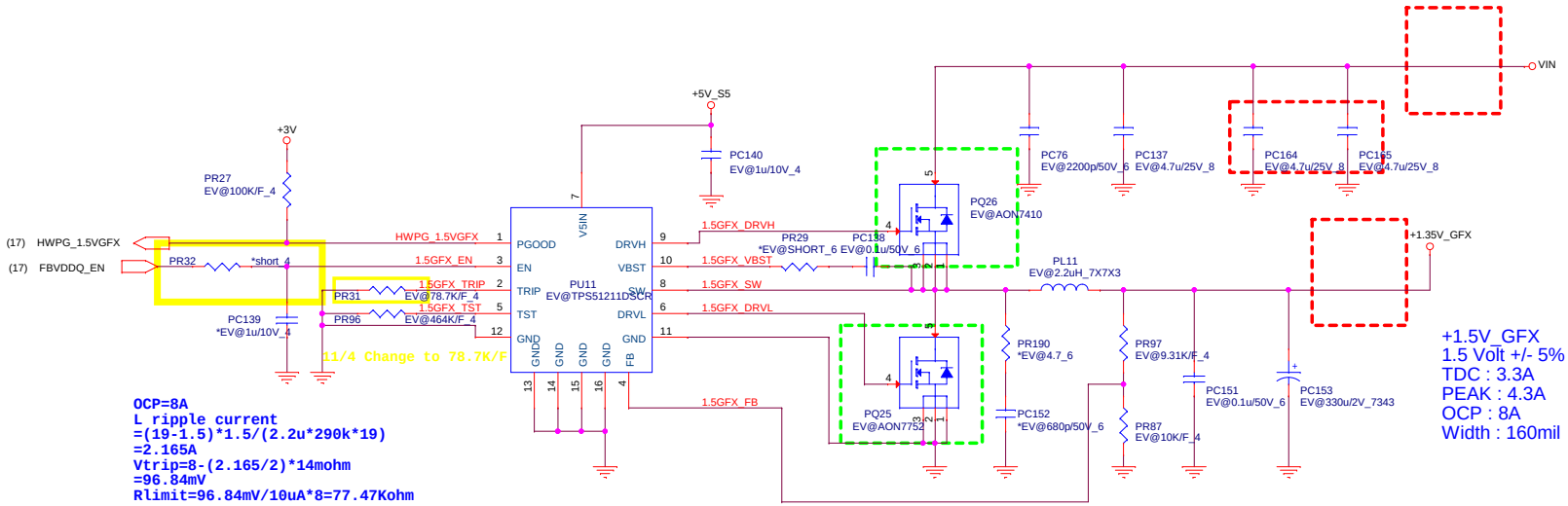
(16,17,18) +1.05V_GFX
(17,20,27) +1.35V_GFX
(16,17,18,19,30) +3V_GFX



+1.05V_GFX
TDC : 1.73A
PEAK : 2.3A
Width : 80mil



+3V_GFX
TDC : 0.17A
PEAK : 0.23A
Width : 20mil

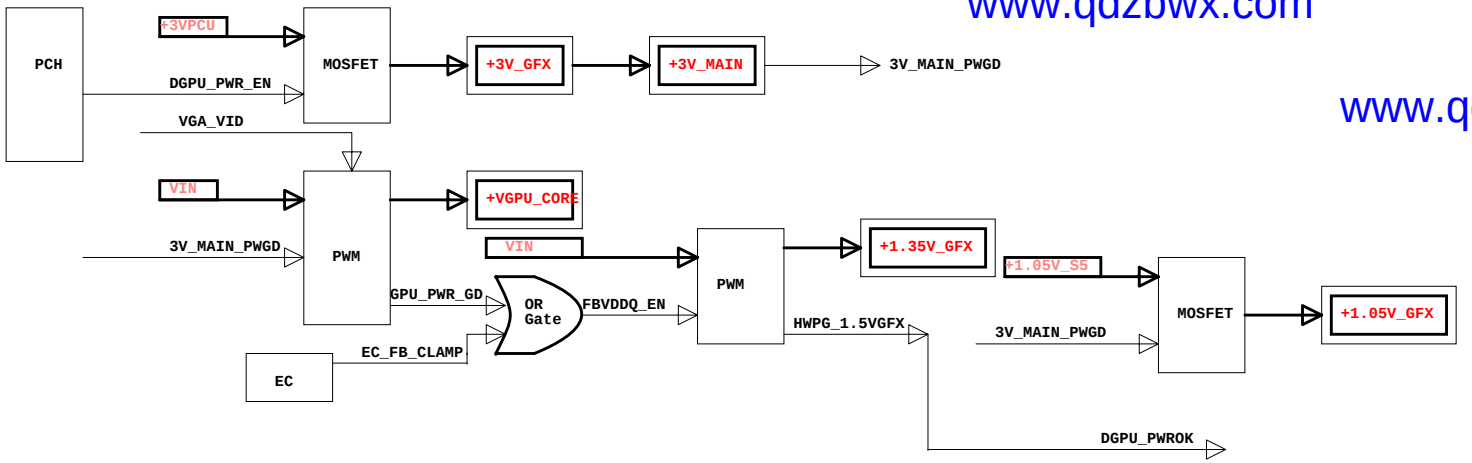


+1.5V_GFX
1.5 Volt +/- 5%
TDC : 3.3A
PEAK : 4.3A
OCP : 8A
Width : 160mil

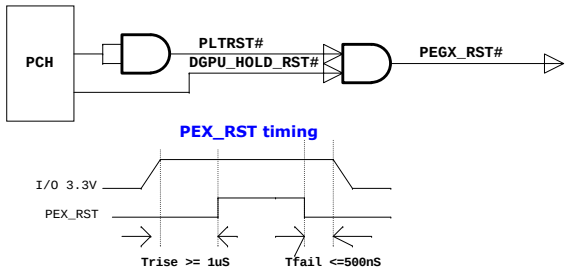
OCP=8A
L ripple current
=(19-1.5)*1.5/(2.2u*290k*19)
=2.165A
Vtrip=8-(2.165/2)*14mohm
=96.84mV
Rlimit=96.84mV/10uA*8=77.47Kohm

Quanta Computer Inc.		
PROJECT : Z8B		
Size	Document Number: +1.35V_GFX/+1.05V_GFX/+3V_GFX	Rev 1A
Date: Monday, July 14, 2014	Sheet 38 of 44	

39 VGA power up sequence



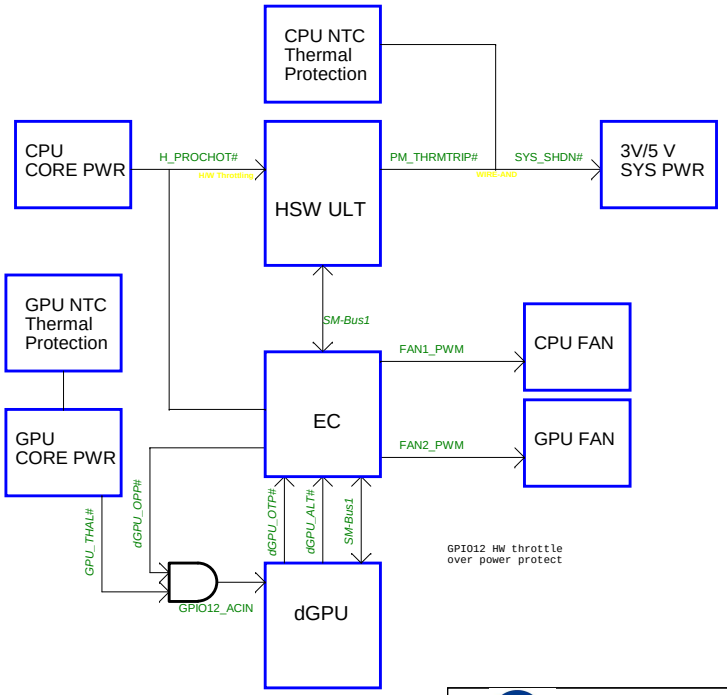
VGA Reset



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+3V_RTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	USB CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+1.05V_S5	+1.05V	PCH CORE VCCST POWER& External GPU POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/SPK/HDMI POWER/CRT	MAINON	S0
+3V		PCH/GPU/Peripheral component POWER	MAINON	S0
+1.35VSUS	+1.35V	CPU/SODIMM/MD POWER	SUSON	S0-S3
+DDR_VTT_RUN	+0.675V	SODIMM/MD Termination POWER	MAINON	
LCDVCC	+3.3V	LCD POWER	EDP_VDD_EN	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE VCCST POWER	MAINON	
+VCCIN	variation	CPU CORE POWER	VRON	S0
+VGPU_CORE	variation	External GPU POWER	VGPU_EN	
+3V_GFX	+3.3V	External GPU POWER	DGPU_PWR_EN	S0
+1.35V_GFX	+1.5V	External GPU POWER	FBVDDQ_EN	
+1.05V_GFX	+1.05V	External GPU POWER	3V_MAIN_PWGD	S0

Thermal Follow Chart

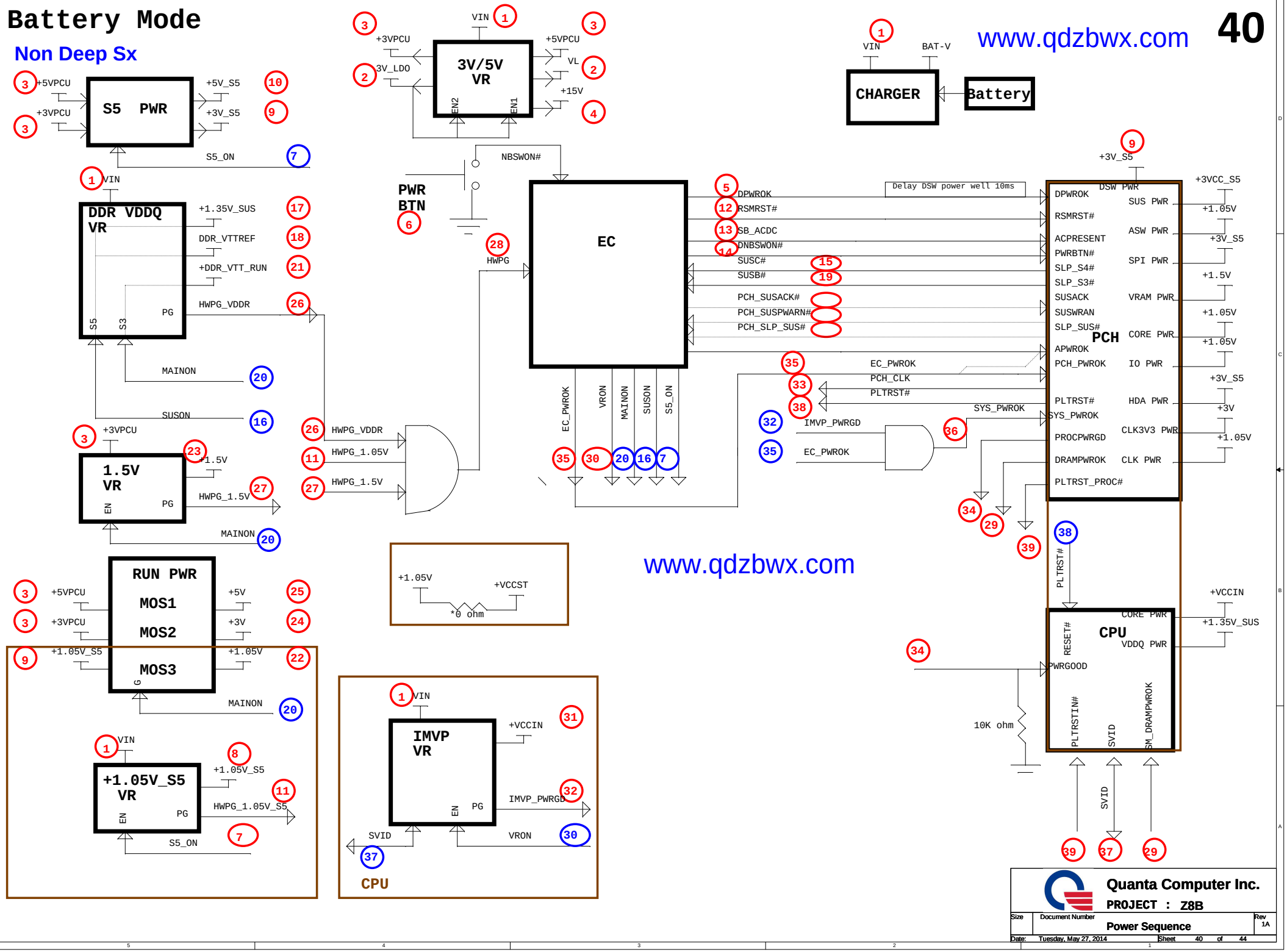


dGPU_OPP# EC notify HW throttle over power protect
dGPU_ALT# for ADPS circuit to infrom EC NV dGPU VPS Alert
dGPU_OTP# VGA thrmtrip# => inform EC over temperature protect

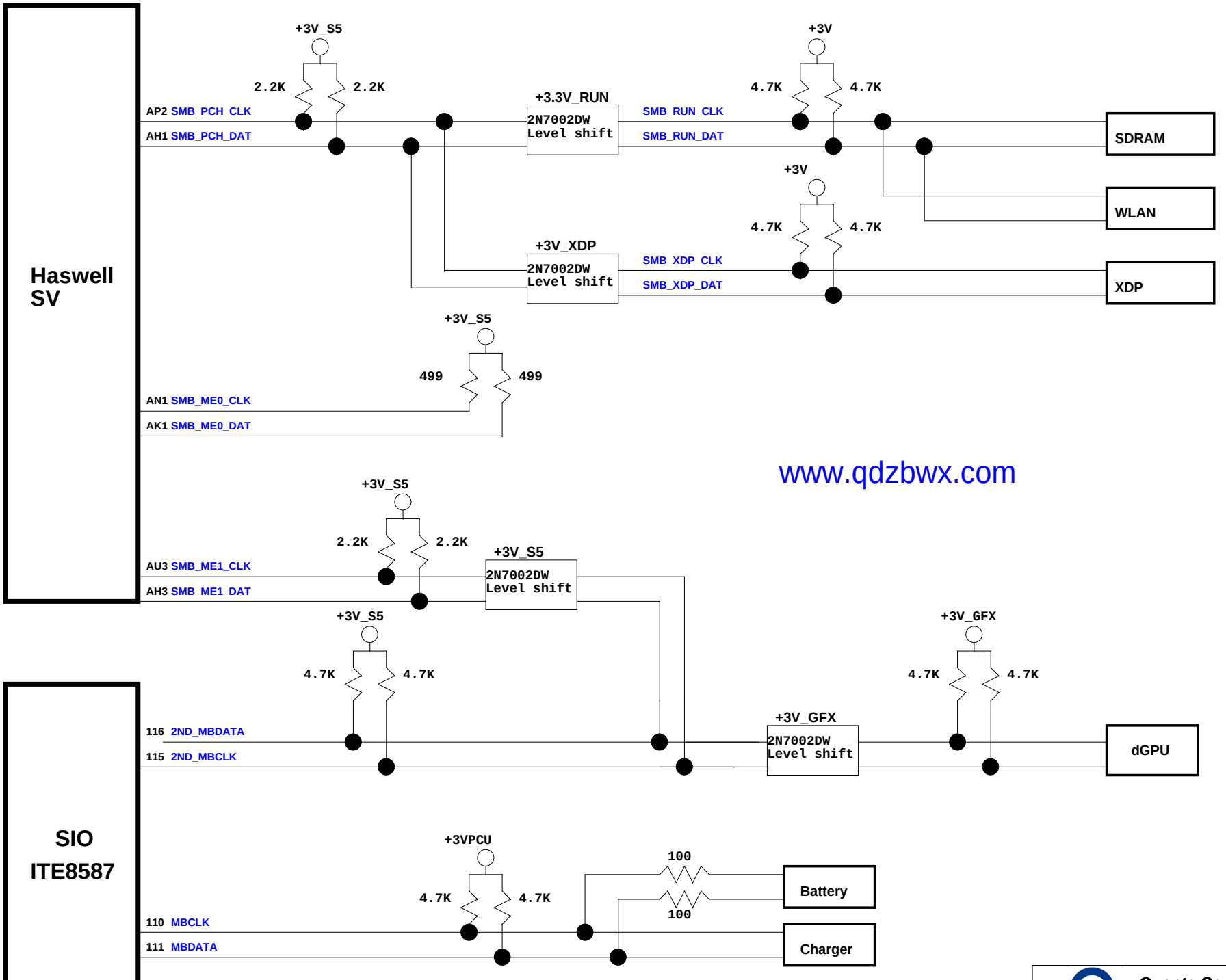
Quanta Computer Inc.
PROJECT : Z8B
Size | Document Number: PWR Status & GPU PWR CRL & THRM | Rev 1A
Date: Tuesday, June 10, 2014 | Sheet 39 of 44

Battery Mode

Non Deep Sx

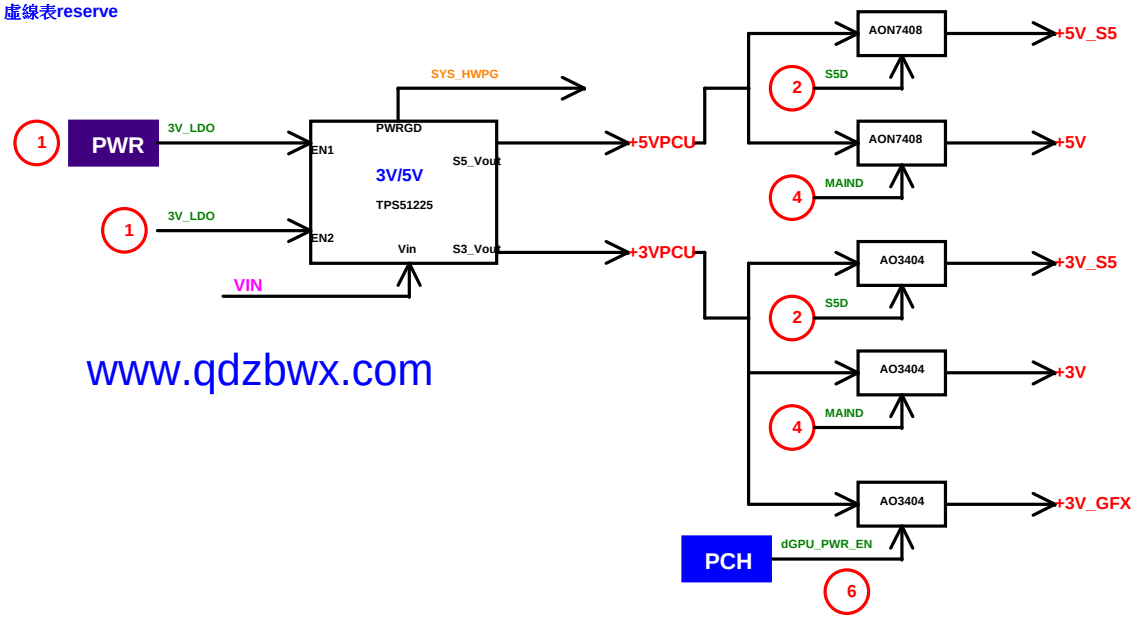


Quanta Computer Inc.			
PROJECT : Z8B			
Size	Document Number	Power Sequence	Rev 1A
Date: Tuesday, May 27, 2014	Sheet 40 of 44		



Quanta Computer Inc.
PROJECT : Z8B
Size | Document Number: SM Bus Map | Rev 1A
Date: Monday, May 26, 2014 Sheet 41 of 44

實線表defult
虛線表reserve



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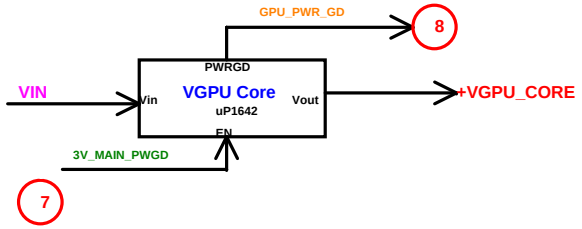

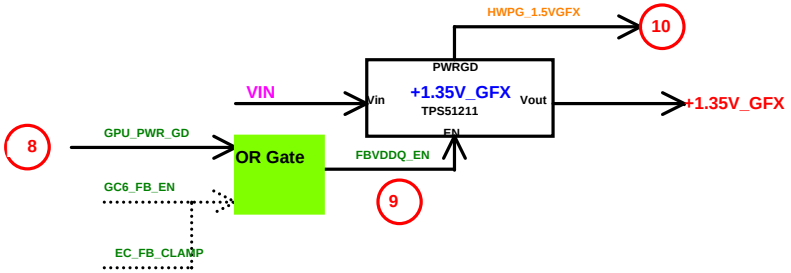

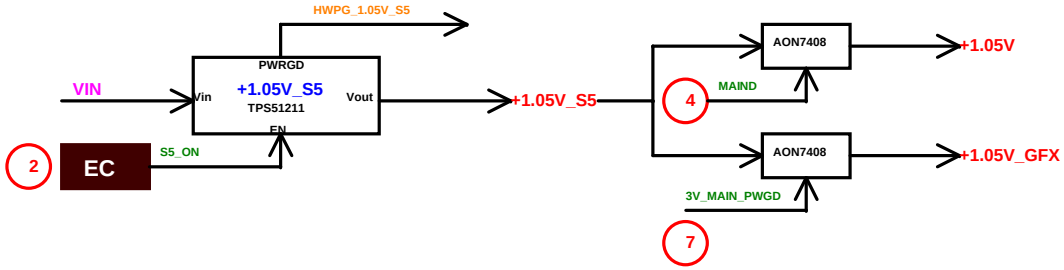

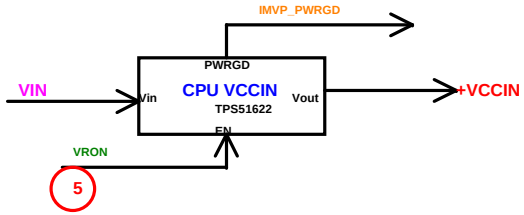

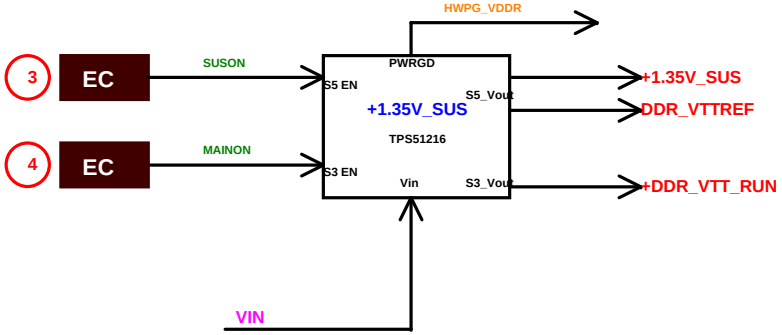

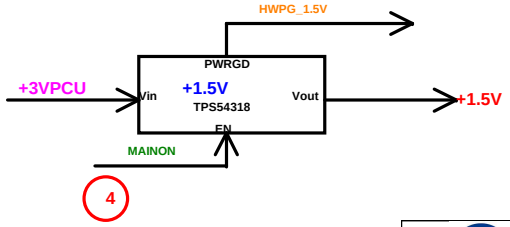

Quanta Computer Inc.
PROJECT : Z8B

Size	Document Number	Rev
	ULT PWR CONTROL	1A

Date: Wednesday, May 28, 2014 Sheet 42 of 44

Model	Version	CHANGE LIST
EA41	1B-1	1 Stuff PR130 and PR134 (2014_05_30)-->Add Vcore sensing Resistant 2 Un stuff PC156 and PC158 (2014_05_30)-->Remove Vcore PWM cap to balance 2 phase driving current 3 Stuff R649 and R663 (2014_05_30)-->Change for EEPROM QAUD MODE 4 Change R644 and R657 by CS21002JB34 (2014_05_30)-->Change for EEPROM QAUD MODE 5 Delete U3,U4,C119 and Add QSR,R729,R728,R730,R731,D23(2014_06_09)-->Change for CRT CCD level shift 6 Change Y3 from BG625000737 to BG625000081(2014_06_09)-->Change for Parts EOD issue 7 Change R255 change 1.82K to 1.8K(2014_06_09)-->Change for Parts EOD issue 8 Change C309,C310,C311,C312,C314,C315,C317,C320,C433,C438,C494,C496,C498,C499,C508 from CH31003KB11 to CH31004KB17-->Change for Parts EOD issue 9 Unstuff CP1,CP2,CP3,CP4,CP5,CP6,C332,C333 (2014_06_10)-->Cost saving 10 Add J2 (2014_06_10) 11 Unstuff Q33 (2014_06_10) -->Cost saving 12 stuff R308 (2014_06_10) -->solving Discrete issue 13 Add R732,R733 (2014_06_10) -->Discrete issue 14 Delete U14,C283 Add U33,C569,C570 Add Location VC1,VC2,C715,C570,C569(2014_06_10) -->Solving USB droop issue 15 Change R500,R50,R123,R256,R257,R192,R191,R455,R88,R59,R534,R524,R456,R531,R617,R625,R604,R200,R470,R213,R212,R548,R582,R583,R623,R218,R588,R581,R605,R163,R234 from Res 0 ohom 0402 to short pad-->Cost saving 16 Delete RP4,RP5,RP6 Add Location R734,R735,R736,R737,R738,R739 -->Cost Saving 17 Delete R522,R530-->Cost saving 18 Change Rs12,R649,R641,R615_R165,R211_R610,R571,R611,R638,R215,R591,R602,R577,R607,R603,R613,R627,R586,R632,R630,R592,R484,R478,R616,R621,R569,R595,R619,R597,R228, R567,R563,R152,R561,R148,R141,R110,R132,R532,R274,R87,R486,R485,R458, R720,R491,R487,R545,R546,R516,R550,R587,R539,R557,R553,R504,R103,R502,R511,R277 from Res 0 ohom 0402 to short pad(2014_06_11) 19 Change R76,R55,R67,R108,R98, R99,R114,R74,R70,R127,R73,R149,R129,R143,R144,R525,R78,R95,R493,R312,R309,R335,R292,R286 from Res 0 ohom 0603 to short pad(2014_06_11) 20 Change R488,R54,R190,R64,R53,R62from Res 0 ohom 0805 to short pad(2014_06_11) 21 Add PC166,PC167,PC168,PC169 for EMI solution 22 Delete JP11,JP12,JP13,JP6,JP4,JP10,JP7,JP14,JP5,JP3,JP9,JP2,JP1,JP8(2014_06_11) 23 Change PR192 from CS22742FB00 RES CHIP 2.74K 1/16W +-1%(0402) to CS22492FB22 RES CHIP 2.49K 1/16W +-1%(0402) (2014_06_11)-->Power require 24 Change PR129 from CS41692FB12 RES CHIP 169K 1/16W +-1%(0402)to CS41502FB18 RES CHIP 150K 1/16W +-1%(0402) (2014_06_11)-->Power require 25 Add PC164,PC165(2014_06_11) 26 Change R171 from CS43902JB10 to CS43902FB00(2014_06_11) 27 Change PC77 from CH43302KB14 to CH4472K9B00 (2014_06_11) 28 Change CN19 from DFHD04MR155 to DFHD04MR296 for SMT issue(2014_06_11) 29 Change CN16 from DFFC06FR058 to DFFC06FR127 by ME request(2014_06_11) 30 Change CN17 from DFFC20FR043 to DFFC24FR039 by ME request(2014_06_11) 31 Stuff C503(2014_06_12) 32 Unstuff R262 Stuff R259(2014_06_12) 33 Stuff R240(2014_06_12) 34 Stuff R271(2014_06_12) 35 UnStuff R247(2014_06_12) 36 Change U11from AL009655K01 to AL000650K00(2014_06_12) 37 Unstuff R683,R684(2014_06_12) 38 Delete R181 ,Add R522(2014_06_12) 39 Delete Hole23(2014_06_12) 40 Unstuffl RV1,RV2,RV3,RV4,RV5,RV6, L13,L14,L15 stuff R339,R344,R349,R347,R336,R328(2014_06_12) 41 Hole4,Hole6 change from H-TC163I140BC236D140P2 to H-TC236I140BC276D140P2(2014_06_12) 42 Unstuff R271 (2014_06_12) 43 Unstuff L11 and stuff R301, R299(2014_06_12) 44 Unstuff L31 and stuff R710, R711(2014_06_12) 45 Change R26,R280from Res 0 ohom 0402 to short pad(2014_06_12) 46 Change R416,R417,R6 from Res 0 ohom 0603 to short pad(2014_06_12) 47 Change R17,R327 from Res 0 ohom 0805 to short pad(2014_06_12) 48 Change U32 from AL000834003 to AL000834004(20140613)-->SD Card issue 49 Change C417,C418 from CH01806JB07(CAP CHIP 18P 50V(+-5% C0G 0402)) to CH01006JB08(CAP CHIP 10P 50V(+-5%,C0G,0402))(2014_06_13)-->Y3 EOD issue 50 Change L4 from CX000181016 to CXSPX181000(20140613)-->EOD issue 51 Change D22 from BCBAT54C204 to BCBAT54CF13(20140613)-->EOD issue 52 Change Q28 ,Q48,Q50 from BA001440Z87 to BA001440013(20140613)--> EOD issue 53 Change Q13,Q14,Q22,Q23,Q25,Q27,Q29,Q32,Q33,Q34,Q38,Q46,Q54,Q55, from BAM70020001 to BAM70020002(20140613)--> EOD issue 54 Change D4,D7 from BCRB501VZ16 to BCRB500VZ29(20140613)-->EOD issue
	1C-1	1 Add thermal-trip schematic Add Location U3,Q59,Q60,C716,R740,R741,R742(20140701) 2 Delete PJP1 for Assembly issue(20140701) 3 Add R743 for cost down(20140701) 4 Add TP177,TP178,TP179,TP180 for SMT test(20140701) 5 Add TP181 for SMT test(20140701) 6 Add C717,C718,C719,C720,C721,C722,C723,C724,C725,C726,C727,C728,C729,C730,C731,C732,C733,C734,C735,C736,C737,C738,C739,C740,C741,C742,C743,C744,C745,C746,C747,C748,C749,C750,C751,C752,C753,C754 for EMI filter(20140701) 7 Add PR41 CS34992FB10 RES CHIP 49.9K 1/16W +-1%(0402) (20140704) 8 Add PR36 CS41002JB20 RES CHIP 100K 1/16W 5%(0402) (20140704) 9 Add PR26 CS31002JB28 RES CHIP 10K 1/16W 5%(0402) (20140704) 10 Add PR191 CS00002JB38 RESISTOR CHIP 0 1/16W +-5%(0402) (20140704) 11 Add PQ9 BAM70020002 TRANSISTOR MOS 2N7002K(60V,300MA)SOT-23 (20140704) 12 PC29,PC75,PC111 change from CC63304M202 to CC63304M203 for material prepare issue 13 C52,PC82,PC83 change from CH6221M9A02 to CH6221M9A00 for material prepare issue 14 Change R499,R202,R44,R412,R425,R434,R239,R273,R656,R28,R31,R682,R686,R687,R665,R667,R668,R669,R670,R97,R195,R118,R693,R375,R350,R363,R364,R359,R356,R727,R354 from Res 0 ohm 0402 to short pad 15 Change R116, R562,R709,R690,R371,R372,R373,R374 from Res 0 ohom 0603 to short pad 16 Change R75,R101,R512,R142,R61,R477,R685 from Res 0 ohom 0805 to short pad 17 Delete PR3 Add R744,R745 18 Delete L21,L20 Change R379,R380,R381,R382 from RES 0 ohm 0402 to short pad(2014_07_09) 19 Delete L11 Change R299,R301 from RES 0 ohm 0402 to short pad(2014_07_09) 20 Delete L11 Change R299,R301 from RES 0 ohm 0402 to short pad(2014_07_09) 21 Delete L13,L14,L15 Change R339,R344,R349,R347,R336,R328 from RES 0 ohm 0402 to short pad(2014_07_09) 22 Delete L31 Change R710,R711 from RES 0 ohm 0402 to short pad(2014_07_09) 23 Change R724,R726 from RES 220 0402 1% to RES CHIP 2K 1% R725,R723 from RES 220 0402 1% to RES CHIP 680 1% (2014_07_09) 24 ADD PR7 RES2.2 1/2W+-5%(0603) PC56 CAP 2200P(2014_07_09) 25 Stuff R742 and un stuff U18 (2014_07_09) 26 Change Hole 9 footprint from H-T5BC217D11BP2 to H-Z8B-1 (2014.07.11) 27 Change CN1 footprint from sdcard-pidat4-09g8n1nn4h0-11p to sdcard-5-251301001000-6-11p-smt(2014.07.11) 28 Change TP102 footprint from TP2675 to TP2050 (2014_07_12) 29 Change Net: SLEEVE_R, RING2_R connection from ADOGND to DGND (2014_07_12) 30 Add Net: HP_JD# connection to DGND (2014_07_12) 31 Unstuff L30 and R714, L33 and R746 conect to +3V (2014_07_12) 32 Add PR218 (2014_07_12) 33 Add Location PC170 (2014_07_14) 34 Change C353,C354 from CAP CHIP 10P 50V to CAP CHIP 8.2P 50V(2014_07_14) 35 Unstuff Q21, R182, R159, Q19, C212 and change R134 from 0805 0 ohm to short pad(2014_07_14) 36 Add PL14 and PL15 for reducing Vin noise(2014_07_14) 37 Change PR124 from RES CHIP 0 ohm 0805 to short pad (2014_07_14) 38 Change R481,R608,R712,R715,PR7,PR2,PR5,PR18,PR19,PR21,PR191,PR37,PR23,PR24,PR45,PR46,PR68,PR115,PR116,PR117,PR122,PR131,PR123,PR125,PR135,PR136,R139,PR164,PR166,PR167,PR185,PR186,PR187,PR188,PR180,PR181,PR171,PR200,PR206,PR32 from Res 0 ohm 0402 to short pad(2014_07_14)

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Quanta Computer Inc.
PROJECT : Z8B

Size: B | Document Number: Change list-1 | Rev: 1A

Date: Tuesday, July 15, 2014 | Sheet 38 of 45

Model	Version	CHANGE LIST
EA41	1C-1	39 Change R481,R698,R712,R715,PR7,PR2,PR5,PR18,PR19,PR21,PR191,PR37,PR23,PR24,PR45,PR46,PR68,PR115,PR116,PR117,PR122,PR131,PR123,PR125,PR135,PR136,R139,PR164,PR166,PR167,PR185,PR186,PR187,PR188,PR180,PR181,PR171,PR200,PR206,PR32 from Res 0 ohm 0402 to short pad(2014_07_14) 40 Change R6,PR9,PR16,PR43,PR59,PR56,PR69,PR77,PR78,R138,PR151,PR158 from Res 0 ohm 0603 to short pad(2014_07_14) 41 Change PR104,PR194 from 0603,2.2ohm to 0805/2.2ohm(2014_07_14) 42 Change PC85,PC160 from 0603,1000pF to 0603/3300pF(2014_07_14) 43 Change PC73, PC74, PC144, PC159??cap from 4.7uF/25V/0805 to 10uF/25V/0805(2014_07_14) 44 Change R358,R369??from 64.9/1%/0402 to 56/1%/0402 (2014_07_14) 45 Delete PCB1 46 Change TVS Diode at D16 and D20(fromCY402M04B02 to CS1250120D)(2014_07_15)

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PROJECT : Z8B
Size: A4 | Document Number: Change list-1 | Rev: 1A
Date: Tuesday, July 15, 2014 | Sheet 36 of 45