

LV530 KBL/ SKL Schematics

Kabylake-U

U22 / U2+3e / U42

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceramic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

DY	DUMMY
DY-EMC	Follow EMC team request (SDV DY)
EMC-TVS	SDV : ASM FVT&SIT : By SKU (SKU1 DY / SKU2 ASM)
EMC-TEST	For EMC team SDV test (SDV : ASM)
23e	U2+3e only
U42	U42 only
NON-U42	U22 or U2+3e
UMA	UMA only
PX	Discrete only

<Variant Name>

緯創資通

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Title

COVER PAGE

Size

Document Number

Rev

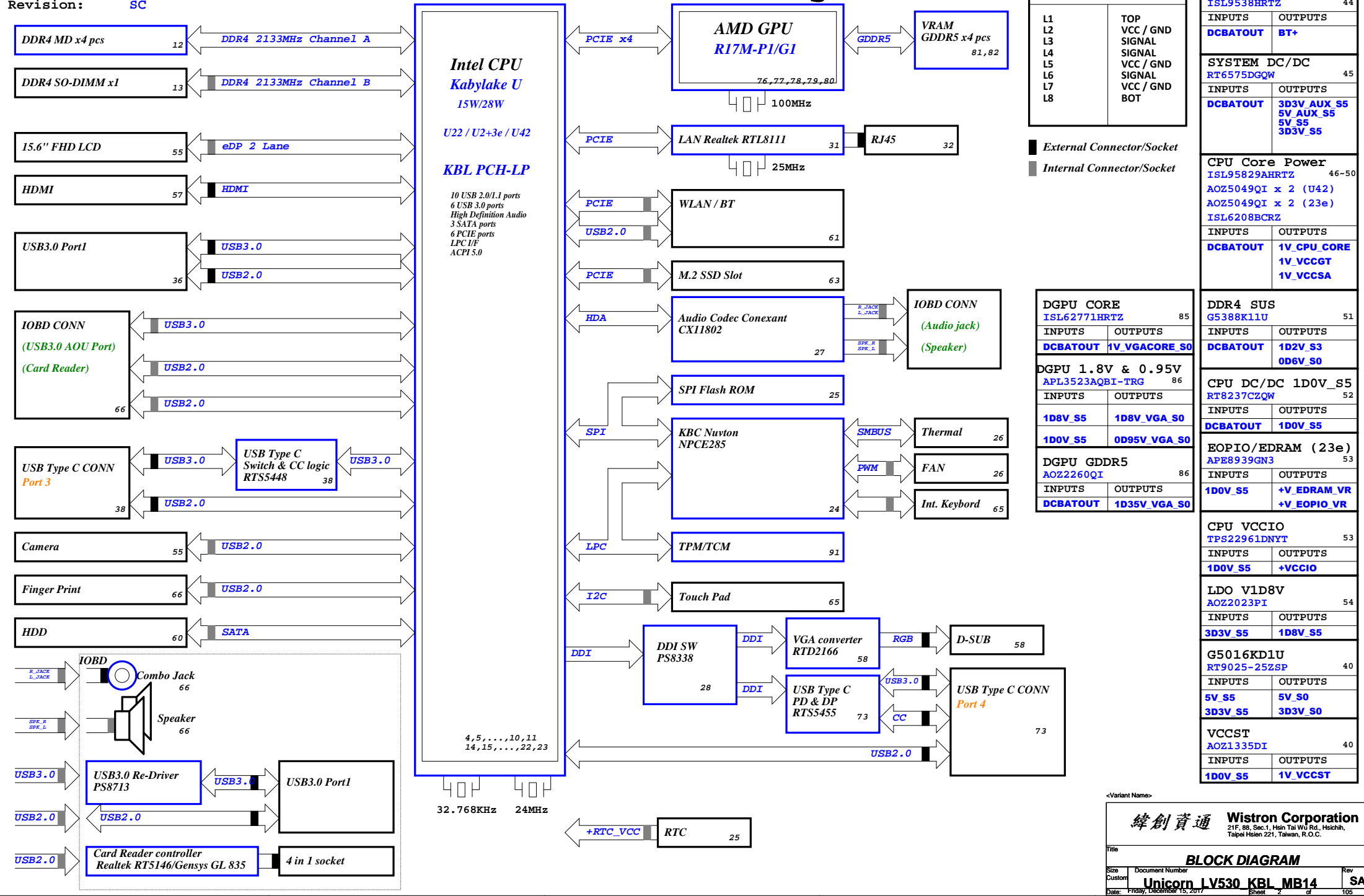
SA

Unicorn LV530 KBL MB14

Date: Friday, December 15, 2017

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LV315 KBL-U Block Diagram



PCB LAYER	
L1	TOP
L2	VCC / GND
L3	SIGNAL
L4	SIGNAL
L5	VCC / GND
L6	SIGNAL
L7	VCC / GND
L8	BOT

External Connector/Socket

Internal Connector/Socket

CHARGER	
ISL9538HRTZ 44	
INPUTS	OUTPUTS
DCBATOUT	BT+
SYSTEM DC/DC	
RT6575DGQW 45	
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5
CPU Core Power	
ISL95829AHRTZ 46~50	
AOZ5049QI x 2 (U42) AOZ5049QI x 2 (23e) ISL6208BCRZ	
INPUTS	OUTPUTS
DCBATOUT	1V_CPU_CORE 1V_VCCGT 1V_VCCSA
DDR4 SUS	
G5388K11U 51	
INPUTS	OUTPUTS
DCBATOUT	1D2V_S3 0D6V_S0
CPU DC/DC 1D0V_S5	
RT8237CZQW 52	
INPUTS	OUTPUTS
DCBATOUT	1D0V_S5
EOPIO/EDRAM (23e)	
APE8939GN3 53	
INPUTS	OUTPUTS
1D0V_S5	+V_EDRAM_VR +V_EOPIO_VR
CPU VCCIO	
TPS22961DNYT 53	
INPUTS	OUTPUTS
1D0V_S5	+VCCIO
LDO V1D8V	
AOZ2023P1 54	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5
G5016KD1U	
RT9025-25ZSP 40	
INPUTS	OUTPUTS
5V_S5	5V_S0
3D3V_S5	3D3V_S0
VCCST	
AOZ1335DI 40	
INPUTS	OUTPUTS
1D0V_S5	1V_VCCST

DGPU CORE	
ISL62771HRTZ 85	
INPUTS	OUTPUTS
DCBATOUT	1V_VGACORE_S0
DGPU 1.8V & 0.95V	
APL3523AQBI-TRG 86	
INPUTS	OUTPUTS
1D8V_S5	1D8V_VGA_S0
1D0V_S5	0D95V_VGA_S0
DGPU GDDR5	
AOZ2260QI 86	
INPUTS	OUTPUTS
DCBATOUT	1D35V_VGA_S0

<Variant Name>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title BLOCK DIAGRAM	
Size Custom	Document Number
Date: Friday, December 15, 2017	Unicorn LV530 KBL_MB14
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Main Func = CPU

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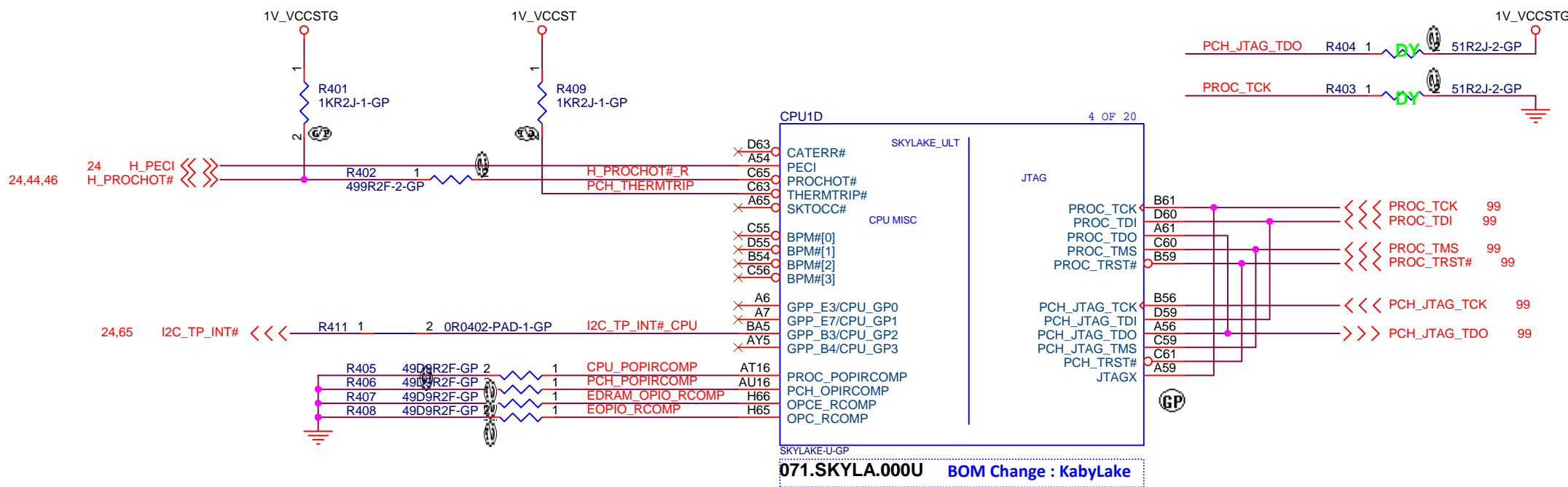
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Document Number
Unicorn LV530 KBL MB 1A

Rev
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Title

CPU (JTAG/CPU SIDE BAND)

Size
A4

Document Number

Unicorn LV530_KBL_MB14

Rev
SA

Date: Friday, December 15, 2017

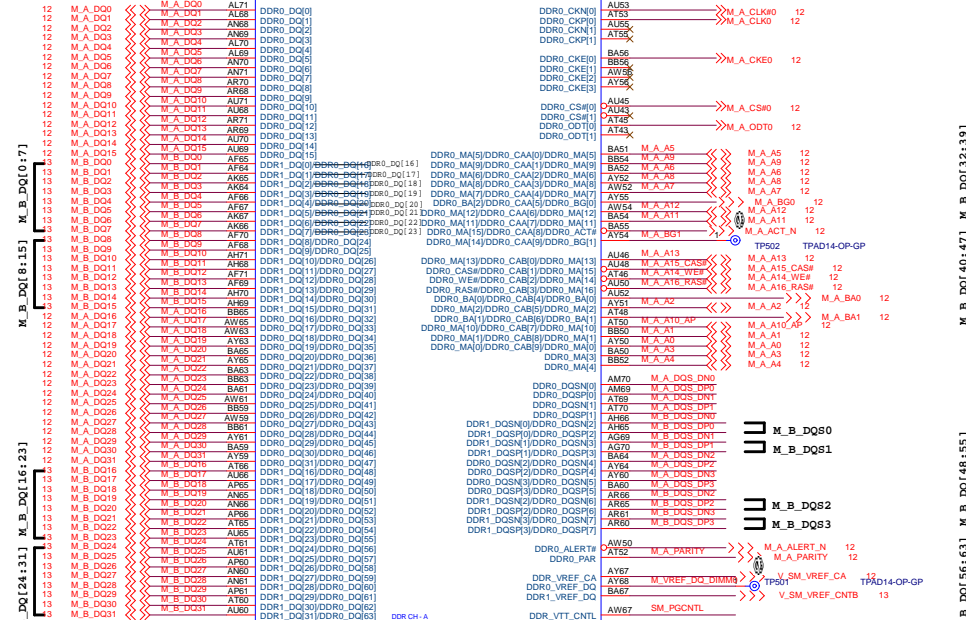
Sheet 4 of 105

M_A_BG1, M_VREF_DQ_DIMM0
Reserve Testpoint only

CPUHB

SKYLAKE_UJT

2 OF 25



071.SKYLA.000U BOM Change : KabyLake

Q01 DIMM0, 800-7-GP 84.05067.031

12V2V_S3 303V_S0 AFTPD01

SM_PGNTL S D

Q01 DIMM0, 800-7-GP 84.05067.031

12V2V_S3 303V_S0 AFTPD01

SM_PGNTL S D

Q01 DIMM0, 800-7-GP 84.05067.031

12V2V_S3 303V_S0 AFTPD01

SM_PGNTL S D

Q01 DIMM0, 800-7-GP 84.05067.031

12V2V_S3 303V_S0 AFTPD01

SM_PGNTL S D

Q01 DIMM0, 800-7-GP 84.05067.031

12V2V_S3 303V_S0 AFTPD01

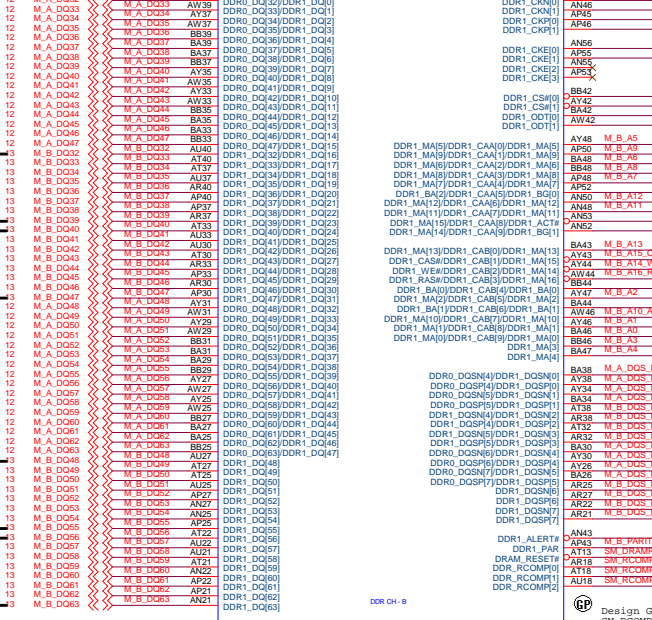
SM_PGNTL S D

Q01 DIMM0, 800-7-GP 84.05067.031

CPUIC

SKYLAKE_UJT

3 OF 25



071.SKYLA.000U BOM Change : KabyLake

Q01 DIMM0, 800-7-GP 84.05067.031

12V2V_S3 303V_S0 AFTPD01

SM_PGNTL S D

Q01 DIMM0, 800-7-GP 84.05067.031

12V2V_S3 303V_S0 AFTPD01

SM_PGNTL S D

Q01 DIMM0, 800-7-GP 84.05067.031

12V2V_S3 303V_S0 AFTPD01

SM_PGNTL S D

Q01 DIMM0, 800-7-GP 84.05067.031

12V2V_S3 303V_S0 AFTPD01

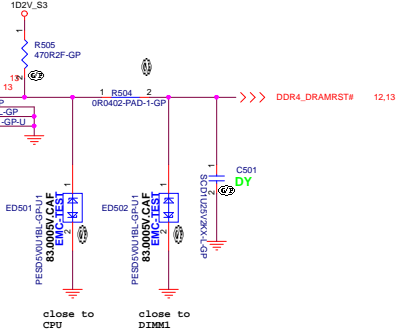
SM_PGNTL S D

Q01 DIMM0, 800-7-GP 84.05067.031

12V2V_S3 303V_S0 AFTPD01

SM_PGNTL S D

Q01 DIMM0, 800-7-GP 84.05067.031



close to CPU

close to DIMM1

Q01 DIMM0, 800-7-GP 84.05067.031

12V2V_S3 303V_S0 AFTPD01

SM_PGNTL S D

Q01 DIMM0, 800-7-GP 84.05067.031

12V2V_S3 303V_S0 AFTPD01

SM_PGNTL S D

Q01 DIMM0, 800-7-GP 84.05067.031

12V2V_S3 303V_S0 AFTPD01

SM_PGNTL S D

Q01 DIMM0, 800-7-GP 84.05067.031

12V2V_S3 303V_S0 AFTPD01

SM_PGNTL S D

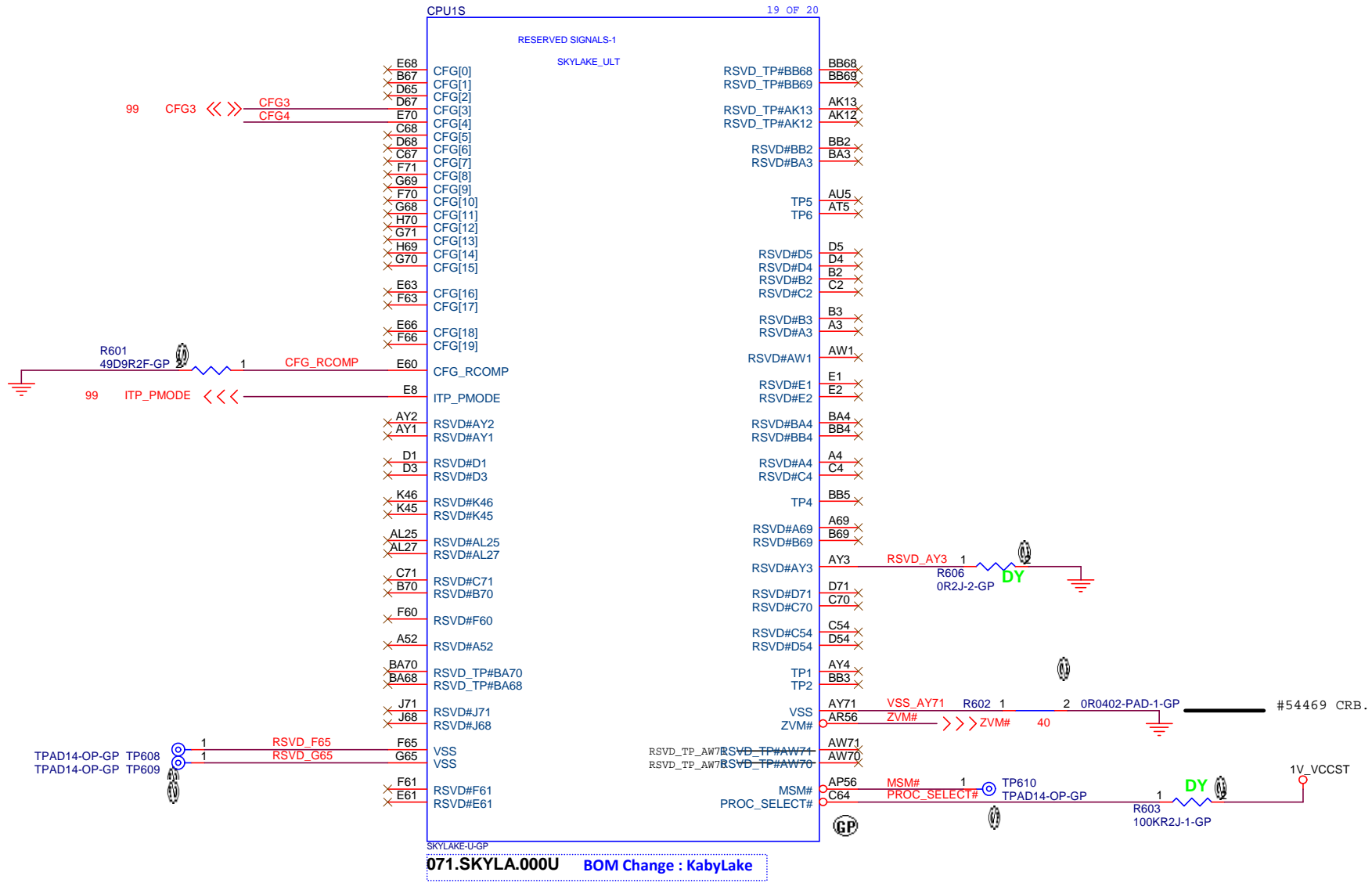
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CPUR (DDR)
Unicorn LV530_KBL_MB14

Rev SA

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Main Func = CPU



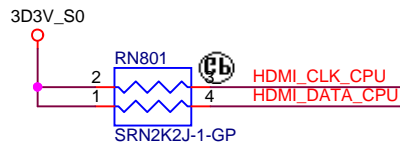
071.SKYLA.000U BOM Change : KabyLake

[559100]
CFG[3]: Reserved configuration lane.
CFG[4]: eDP enable:
1 = Disabled.
0 = Enabled.

<Variant Name>

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Title CPU (CFG)		
Size Custom	Document Number Unicorn_LV530_KBL_MB14	Rev SA
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Main Func = CPU



HDMI

20170413

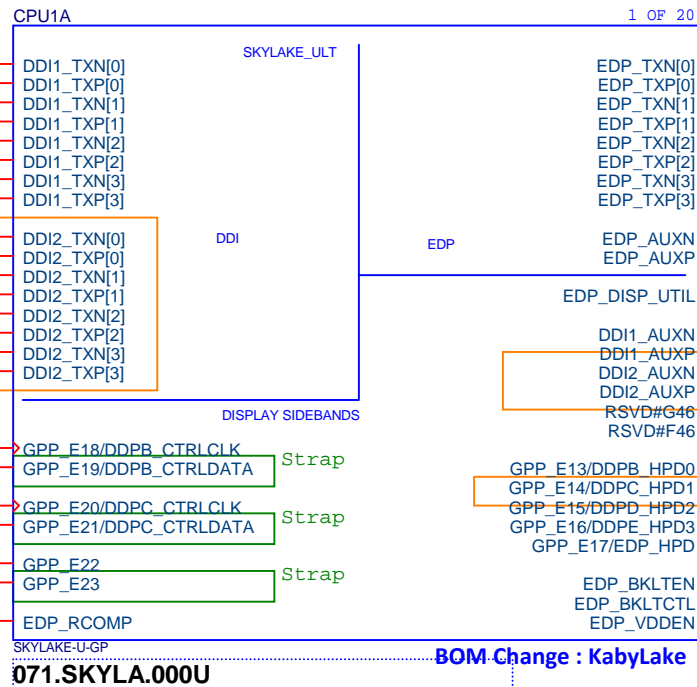
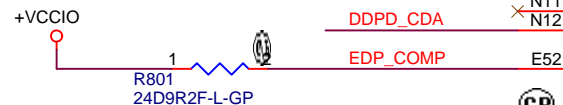
different with BOHO

DDI Switch Type C PD, DSUB



HDMI

DDI Switch



BOM Change : KabyLake

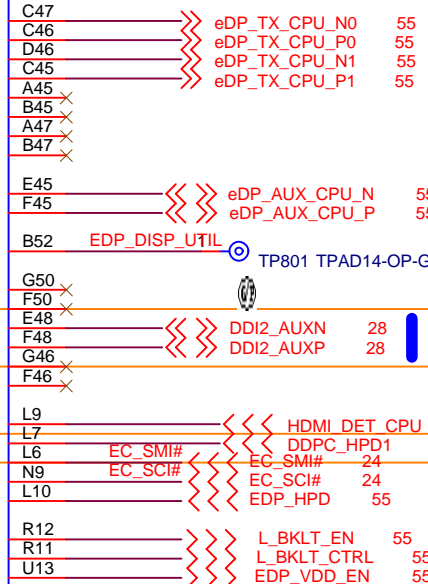
071.SKYLA.000U

[561280] eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	5 mils	25 mils	24.9 Ω \pm 1%	Max = 600 mils

[561280] DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k \pm 5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k \pm 5% resistor	NC

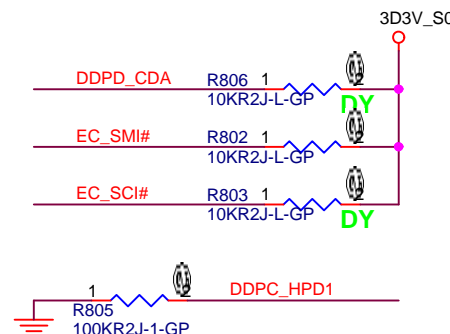


20170413

different with BOHO

DDI Switch Type C PD, DSUB

DDI Switch Type C PD, DSUB



<Variant Name>

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Title		
CPU (DDI/EDP)		
Size A4	Document Number	Rev
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Main Func = CPU

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<Variant Name>

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Title

CPU (RESERVED)

Size
A4

Document Number

Unicorn LV530 KBL MB GA

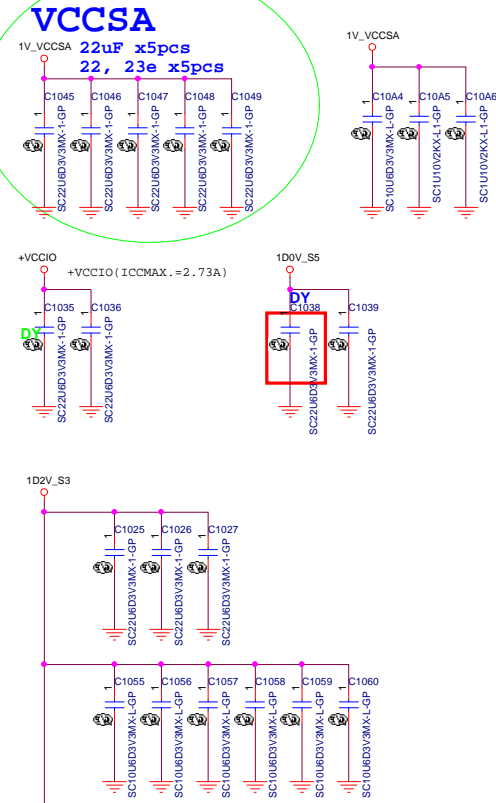
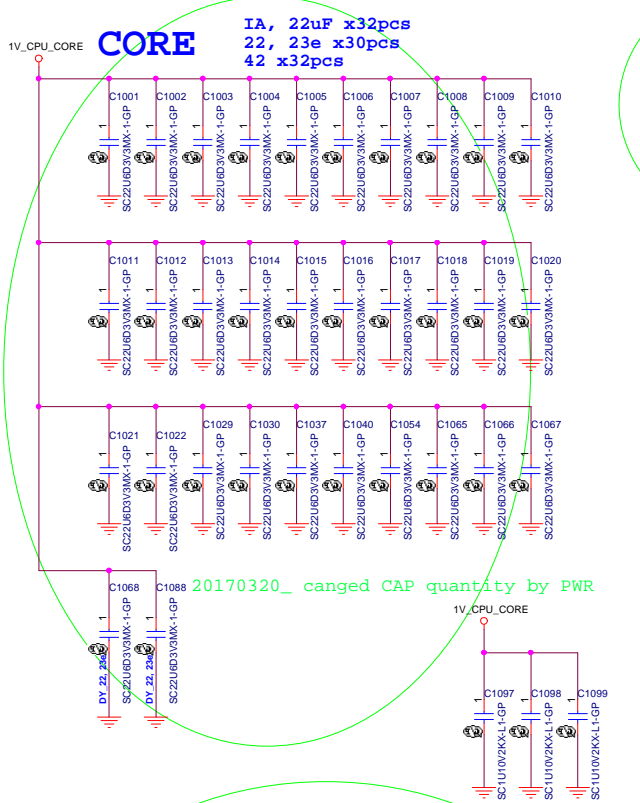
Rev

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Main Func = CPU

20170320_ changed CAP quantity by PWR



GT:

U-Line_22/23e

U-line 22/23e 15W/28W
IccMax current-10ms max[A] = 64 A

22uF	PCS	Cap
Suggestion	32	330uF*1 (U22)
Suggestion	32	330uF*2 (U23e)
OPP	26	330uF*1 (U22)

U-Line_42

U-line 22/42 15W/28W
IccMax current-10ms max[A] = 32 A

22uF	PCS	Cap
Suggestion	26	330uF*1

IA:

U-Line_22/23e

U-line 22/23e 15W/28W
IccMax current-10ms max = 32 A

22uF	PCS	Cap
Suggestion	30	330uF*1
OPP	22	330uF*1

U-Line_42

U-line 42
IccMax current-10ms max = 64 A

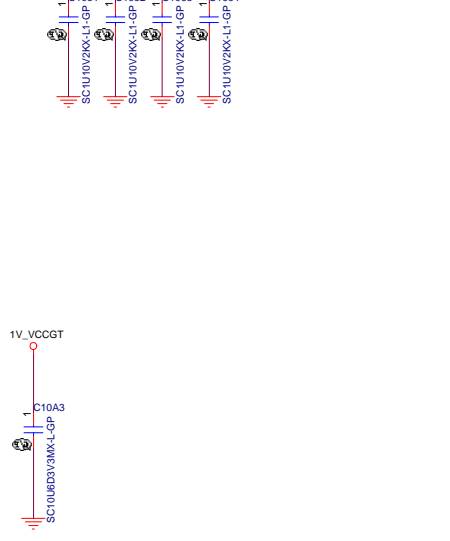
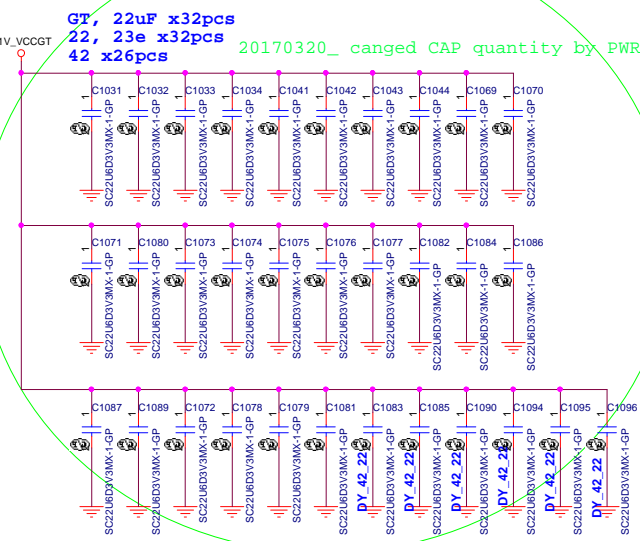
22uF	PCS	Cap
Suggestion	32	330uF*2

VCCSA:

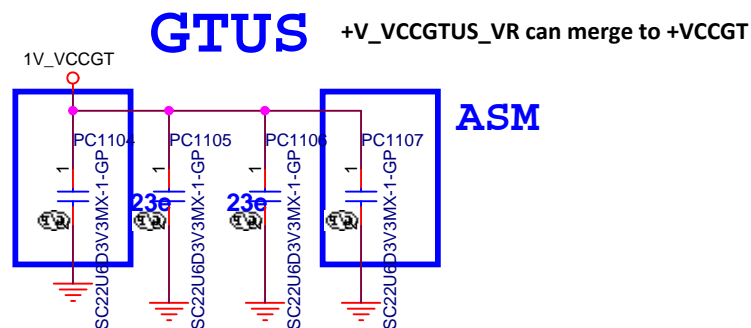
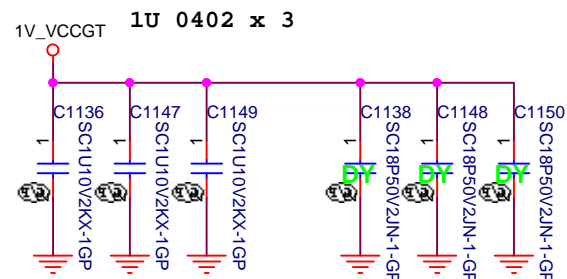
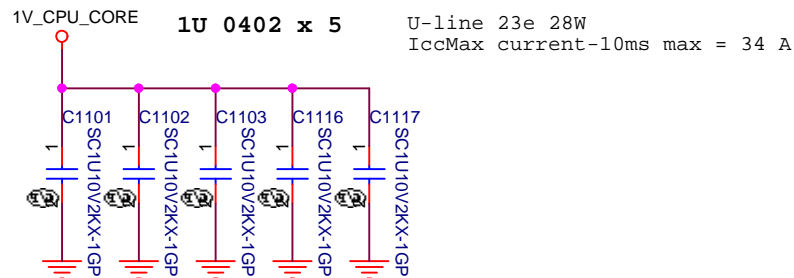
U-Line

U-line 22/23e 15W/28W
IccMax current-10ms max[A] = 5.1 A

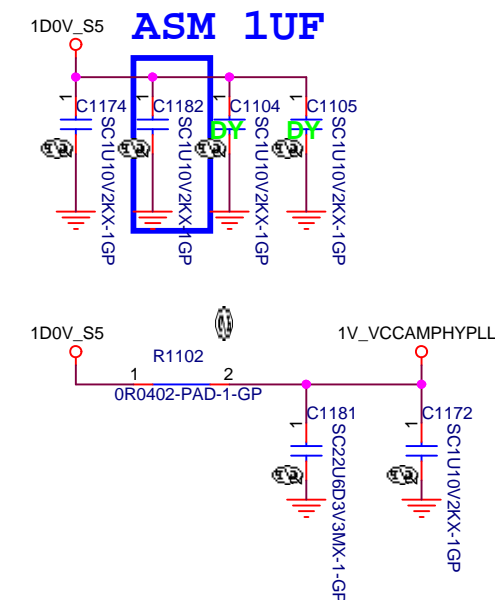
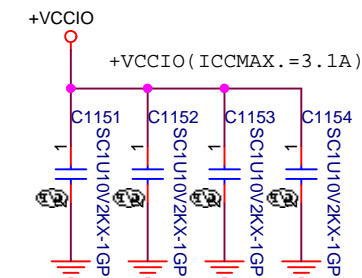
22uF	PCS
Suggestion	5
OPP	5



Main Func = CPU

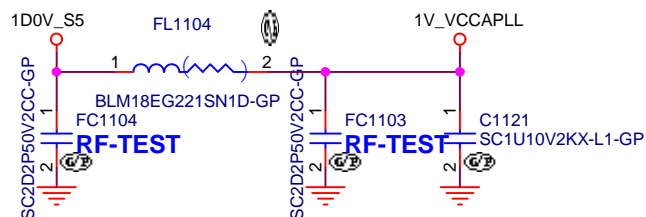
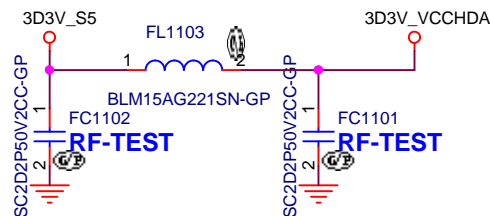


VCCIO



PCH DERIVED RAILS

VCCPGPPA(ICCMAX.=0.05A)

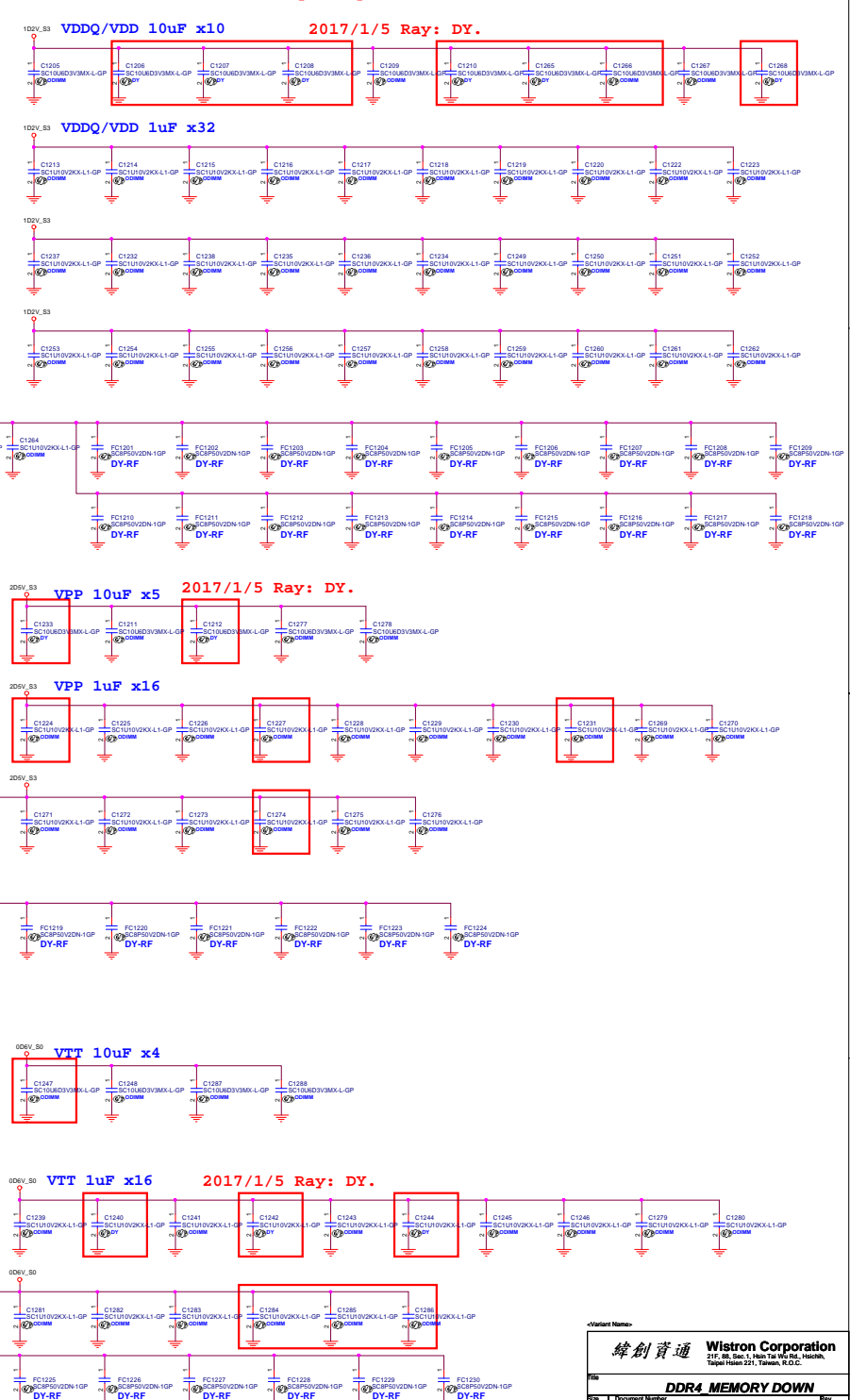


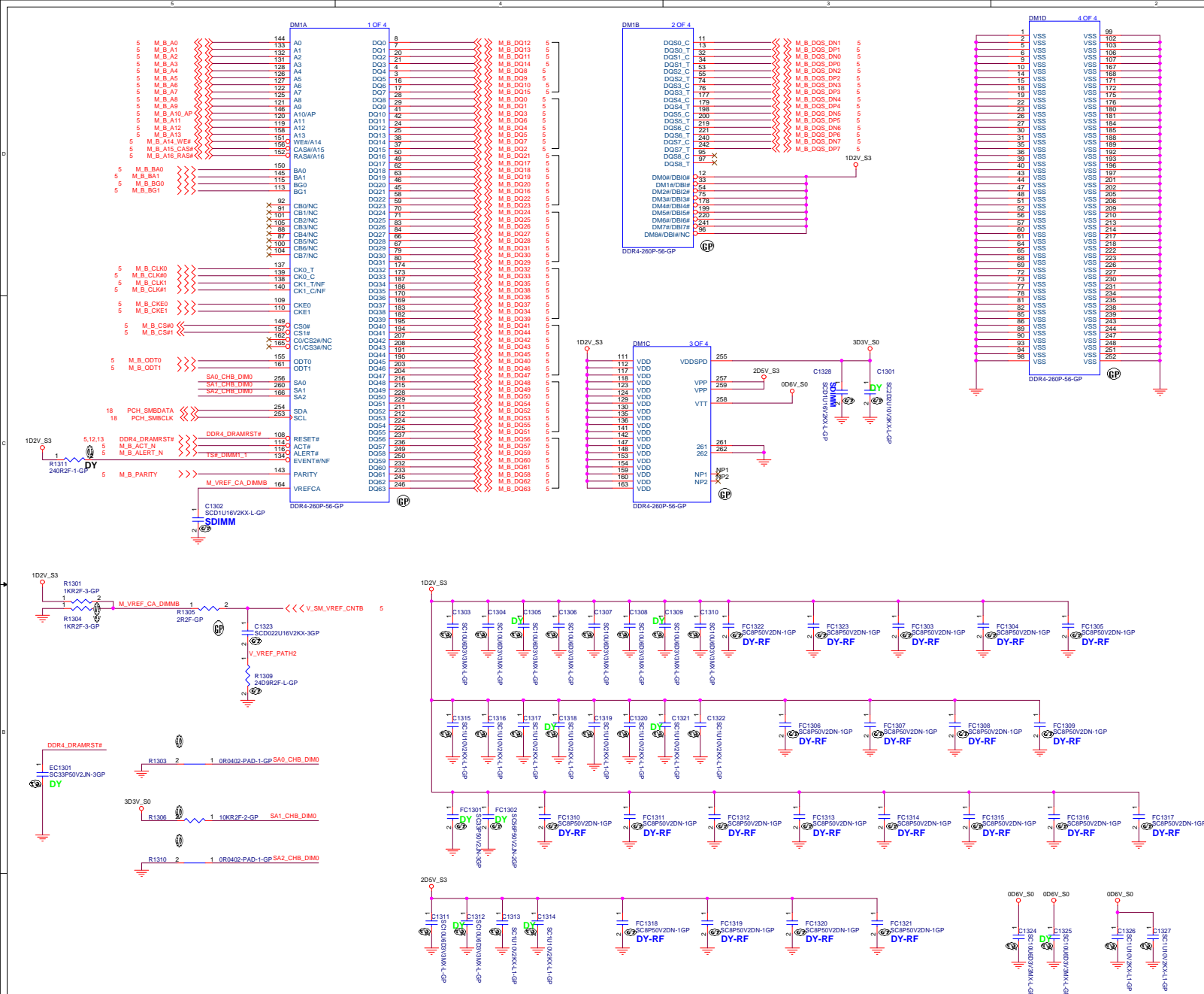
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Title		
CPU (POWER CAP2)		
Size	Document Number	Rev
A4	Unicorn_LV530_KBL_MB14	SA
Date: Friday, December 15, 2017		
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DDR4 On Board RAM Power Decouple Cap





12/09 Ray
Need to check property

[561280] 4.23.6 KBL-U DDR4 SODIMM Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x μ F (size)
DDR4 SODIMM 1DPC	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10 μ F (0603)
		4 near each side of the DIMM connector close to VDD pins	16x 1 μ F (0402)
		1 placeholder	1x 330 μ F (7343)
	VTT	Place these caps on the VTT plane close to SODIMM	1x 10 μ F (0805)
		Placeholder	1x 10 μ F (0805)
		Place these caps on the VTT plane close to SODIMM	4x 1 μ F (0402)
	VPP	DRAM Side	2x 10 μ F (0603)
		DRAM Side	2x 1 μ F (0402)
	VDDSPD	Place close to DIMM	1x 0.1 μ F (0402)
		Place close to DIMM	1x 2.2 μ F (0402)

Variant Name

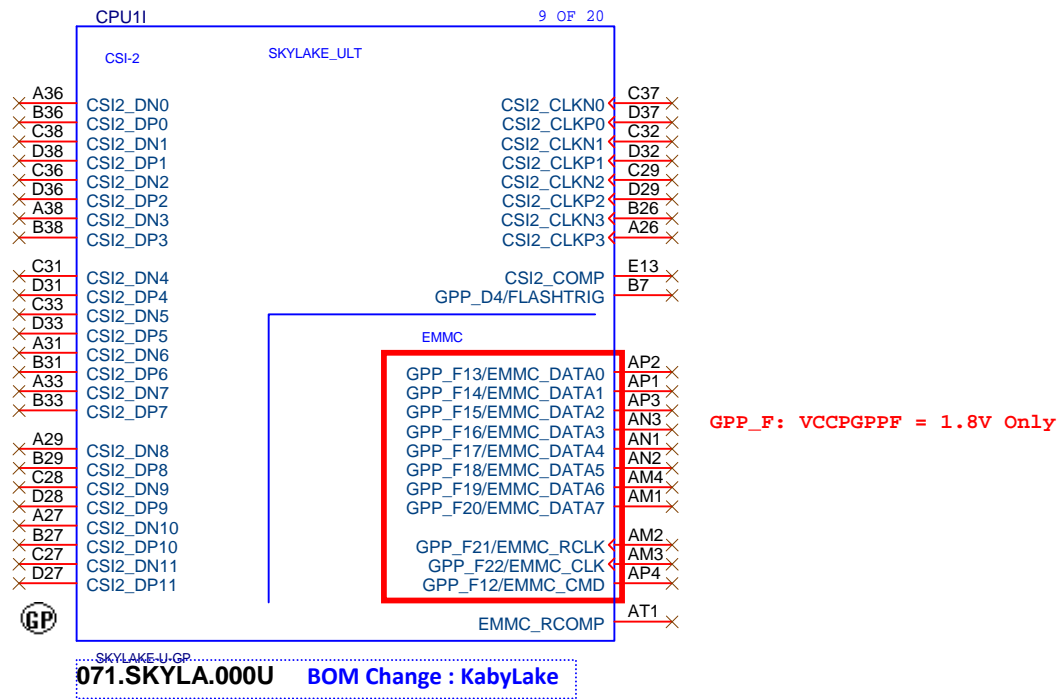
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Title: DDR4 SODIMM			
Size: A2	Document Number: Unicorn LV530 KBL MB	Rev: 1.0	
Date: Friday, December 15, 2017	Sheet: 13	of 106	

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Title <div>RESERVED</div>		
Size <div>A4</div>	Document Number <div>Unicorn LV530 KBL MB 1A</div>	Rev <div>1A</div>
Date <div>Friday, December 15, 2017</div>		Sheet <div>14</div> of <div>105</div>

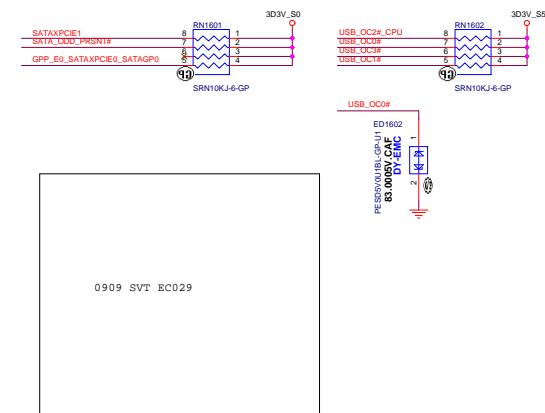
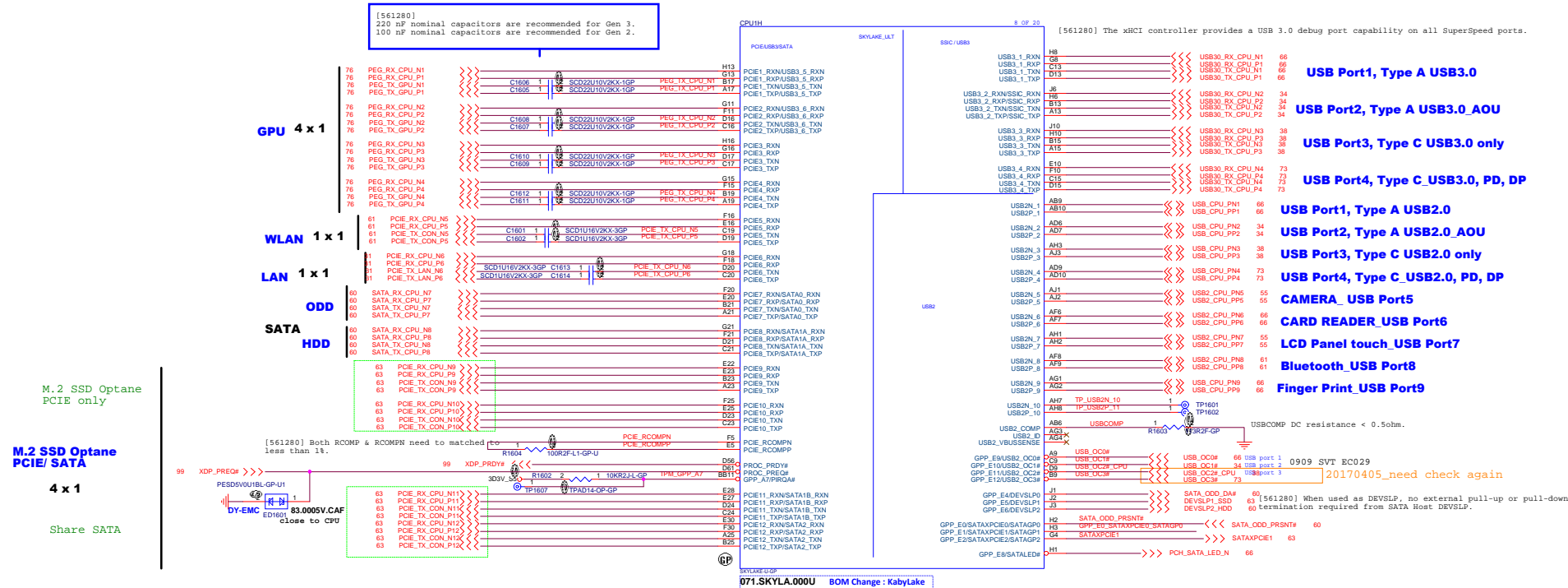
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Title					
CPU (CSI2/EMMC)					
Size	Document Number				Rev
A4	Unicorn LV530 KBL MB GA				1A
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Main Func = PCH

**PCIE Table**

Port	PCIe Device	Share BUS
1	GPU L0	
2	GPU L1	
3	GPU L2	
4	GPU L3	
5	M.2 SSD	
6	M.2 SSD	
7	M.2 SSD	SATA0
8	M.2 SSD	SATA1A
9	LAN	
10	WLAN	
11	ODD	SATA1B
12	HDD	SATA2

SATA Table

Pair	SATA Device	Share BUS
0	ODD	PCIE7
1A	HDD	PCIE8
1B	M.2 SSD	PCIE11
2	M.2 SSD	PCIE12

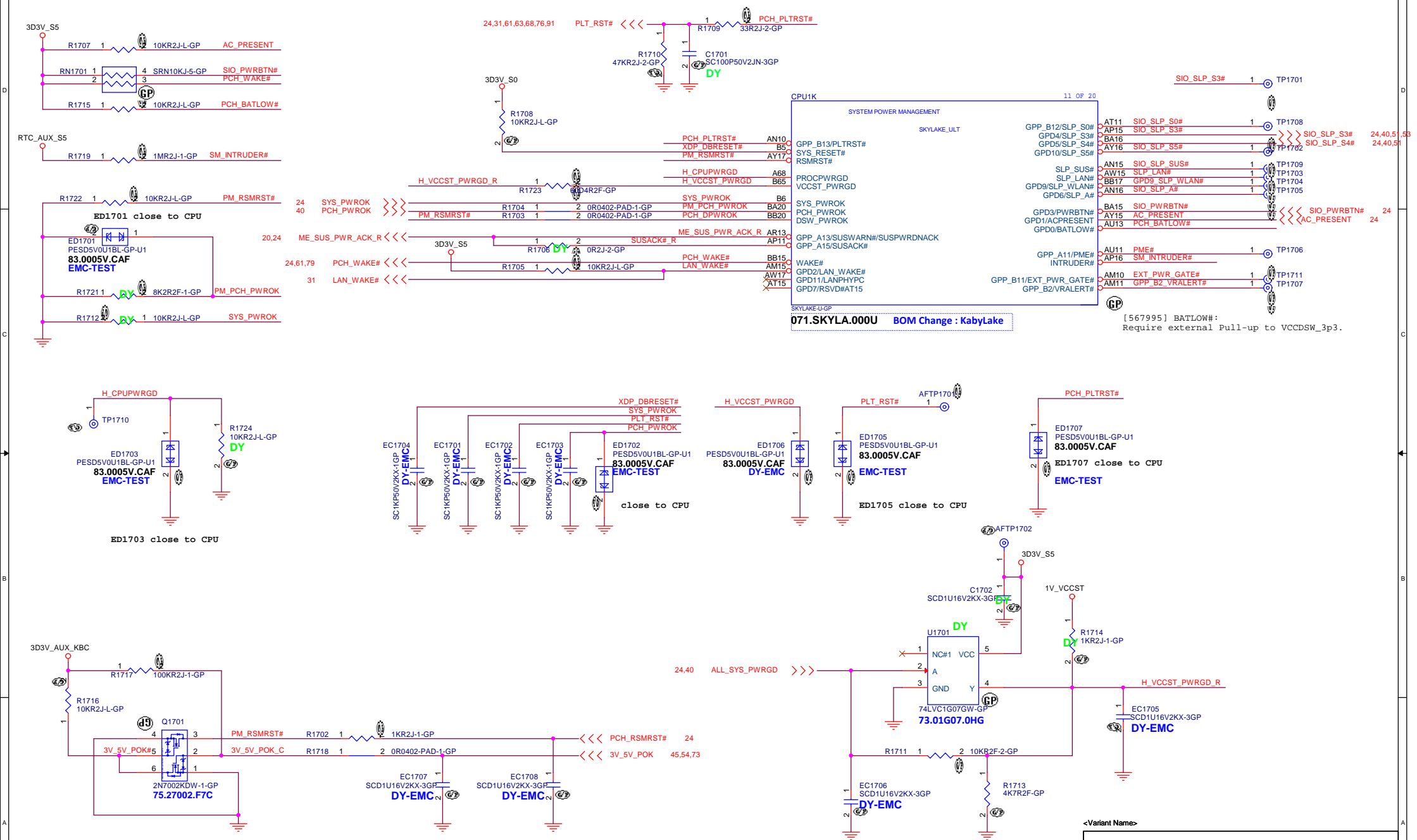
USB 3.0 Table

Pair	USB3.0 Device	Share BUS
1	USB3.0 port1 (Type A USB3.0)	
2	USB3.0 port2 (Type A USB3.0_AOU)	
3	USB Port3, Type C USB3.0 only	
4	USB Port4, Type C_USB3.0, PD, DP	
5	N/A	PCIE1 (GPU)
6	N/A	PCIE2 (GPU)

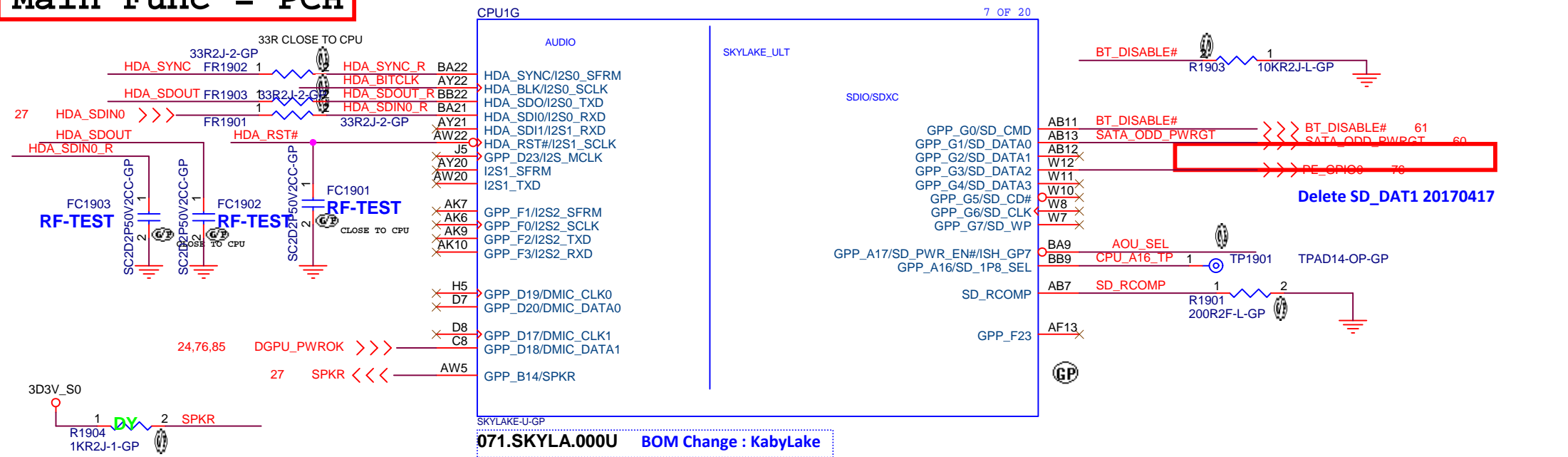
USB 2.0 Table

Pair	USB2.0 Device
1	USB Port1, Type A USB2.0
2	USB Port2, Type A USB2.0_AOU
3	USB Port3, Type C USB2.0 only
4	USB Port4, Type C_USB2.0, PD, DP
5	CAMERA_USB Port5
6	CARD READER_USB Port6
7	LCD Panel touch_USB Port7
8	Bluetooth_USB Port8
9	Finger Print_USB Port9
10	Ultrabay_USB Port10

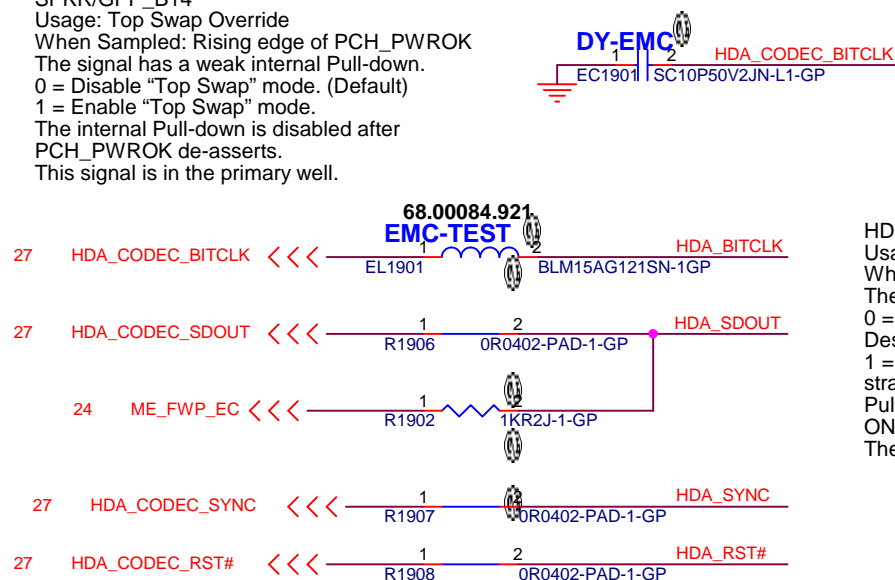
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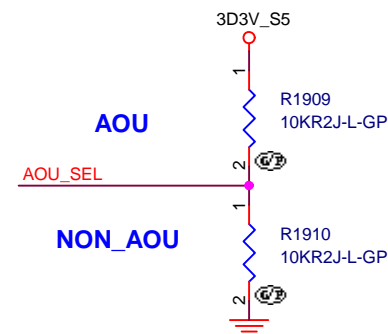
Main Func = PCH



SPKR/GPP_B14
Usage: Top Swap Override
When Sampled: Rising edge of PCH_PWROK
The signal has a weak internal Pull-down.
0 = Disable "Top Swap" mode. (Default)
1 = Enable "Top Swap" mode.
The internal Pull-down is disabled after
PCH_PWROK de-asserts.
This signal is in the primary well.



HDA_SDO_I2S_TXD0
Usage: Flash Descriptor Security Override
When Sampled: Rising edge of PCH_PWROK
The signal has a weak internal Pull-down.
0 = Enable security measures defined in the Flash Descriptor. (Default)
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY.
The internal Pull-down is disabled after PCH_PWROK de-asserts.



<Variant Name>

緯創資通 **Wistron Corporation**
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Title	Author	Year	Journal	Volume	Issue	Page
1. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	1-15
2. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	16-30
3. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	31-45
4. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	46-60
5. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	61-75
6. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	76-90
7. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	91-105
8. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	106-120
9. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	121-135
10. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	136-150

CPU (HDA/SDIO/SDXC)

Size

Document Number

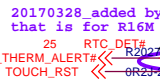
Unicorn LV530 KBL MB14

Rev

SA

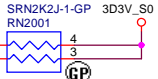
Date: Friday, December 15, 2017

Sheet 19 of 105

[illegible]

20170328_added by
that is for R16M

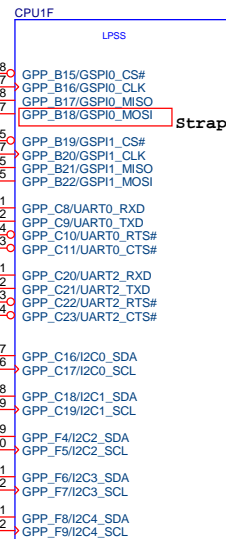
25 RTC_DET#
THERM_ALERT#<<< R2027
TOUCH_RST <<< 0R2J2



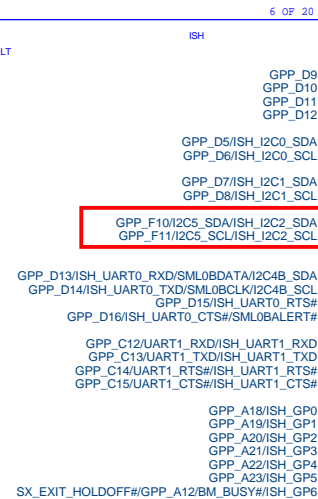
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65  I2C_TP_DATA  <<>> I2C_TP_DATA
66  I2C_TP_CLK  <<>> I2C_TP_CLK

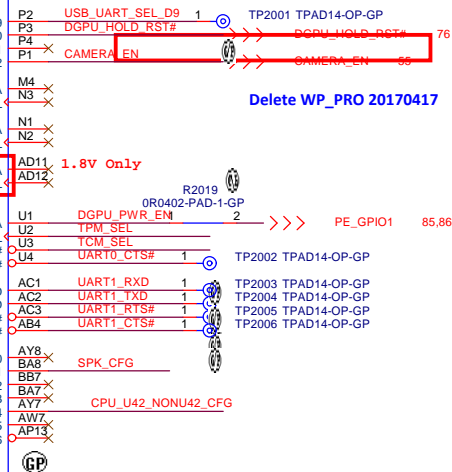
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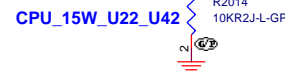
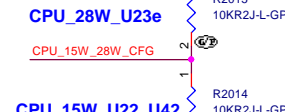
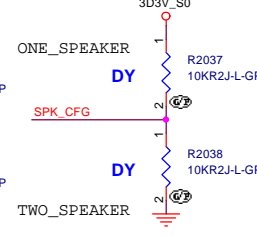
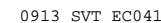
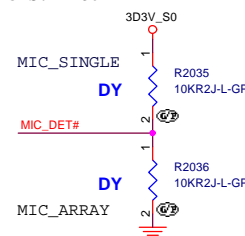
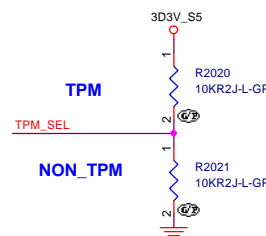
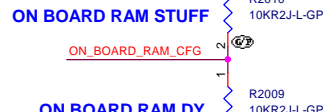
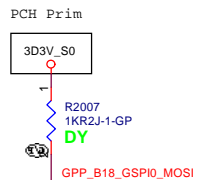
BOM Change : KabyLake



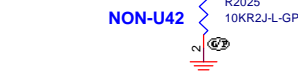
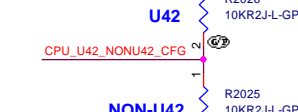
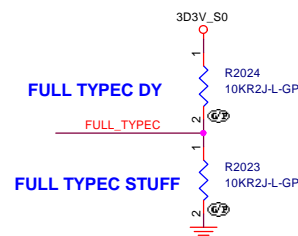
AD11 1.8V Only



GPIO0_MOSI/GPP_B18
Usage: No Reboot
When Sampled: Rising edge of PCH_PWROK
The signal has a weak internal Pull-down.
0 = Disable "No Reboot" mode. (Default)
1 = Enable "No Reboot" mode (PCH will disable the
TCO Timer system reboot feature). This function is useful when running ITP/XDP.
The internal Pull-down is disabled after PCH_PWROK de-asserts.



20170405_need check again

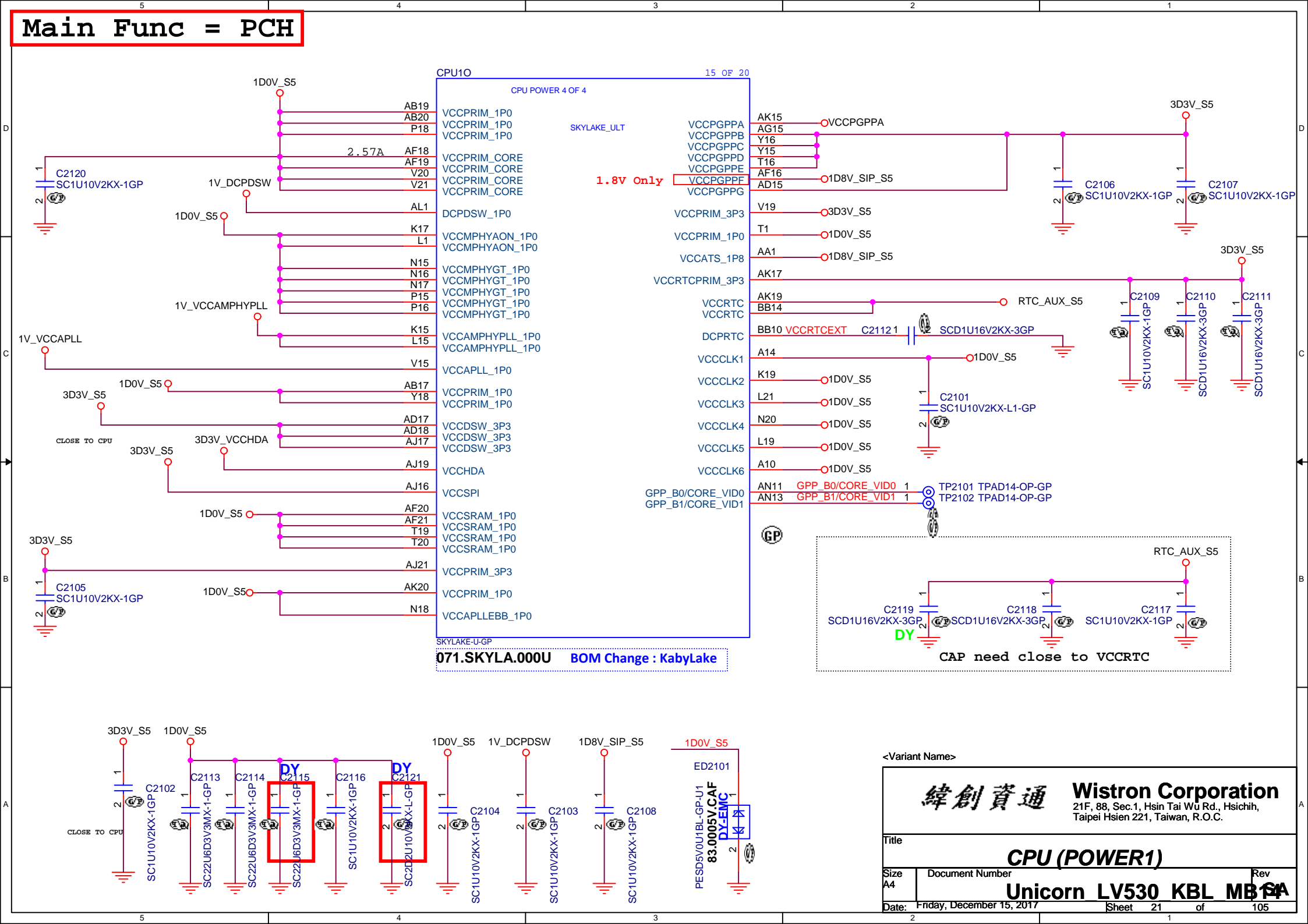


<Variant Names>

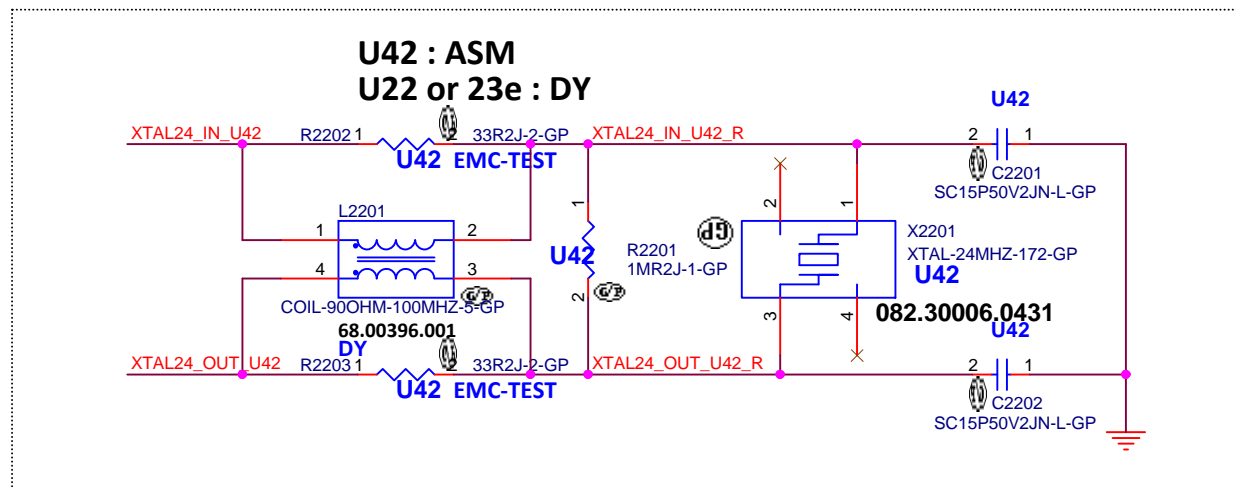
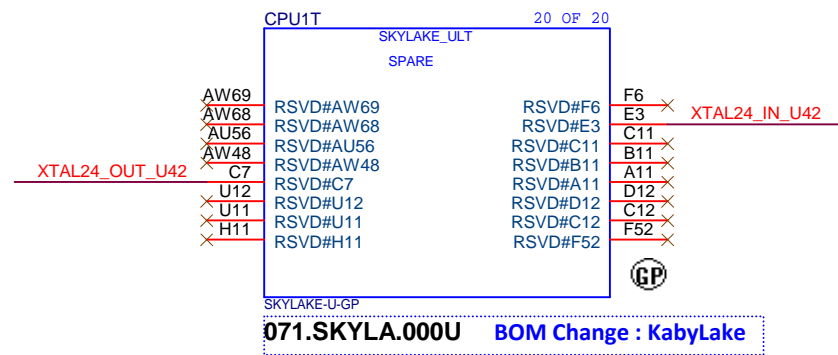
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
CPU (LPSS/UART/ISH)			
Size A3	Document Number		Rev
Unicorn LV530 KBL MB18A			
Date:	Friday, December 15, 2017	Sheet 20 of	105

Main Func = PCH



Main Func = PCH



<Variant Name>

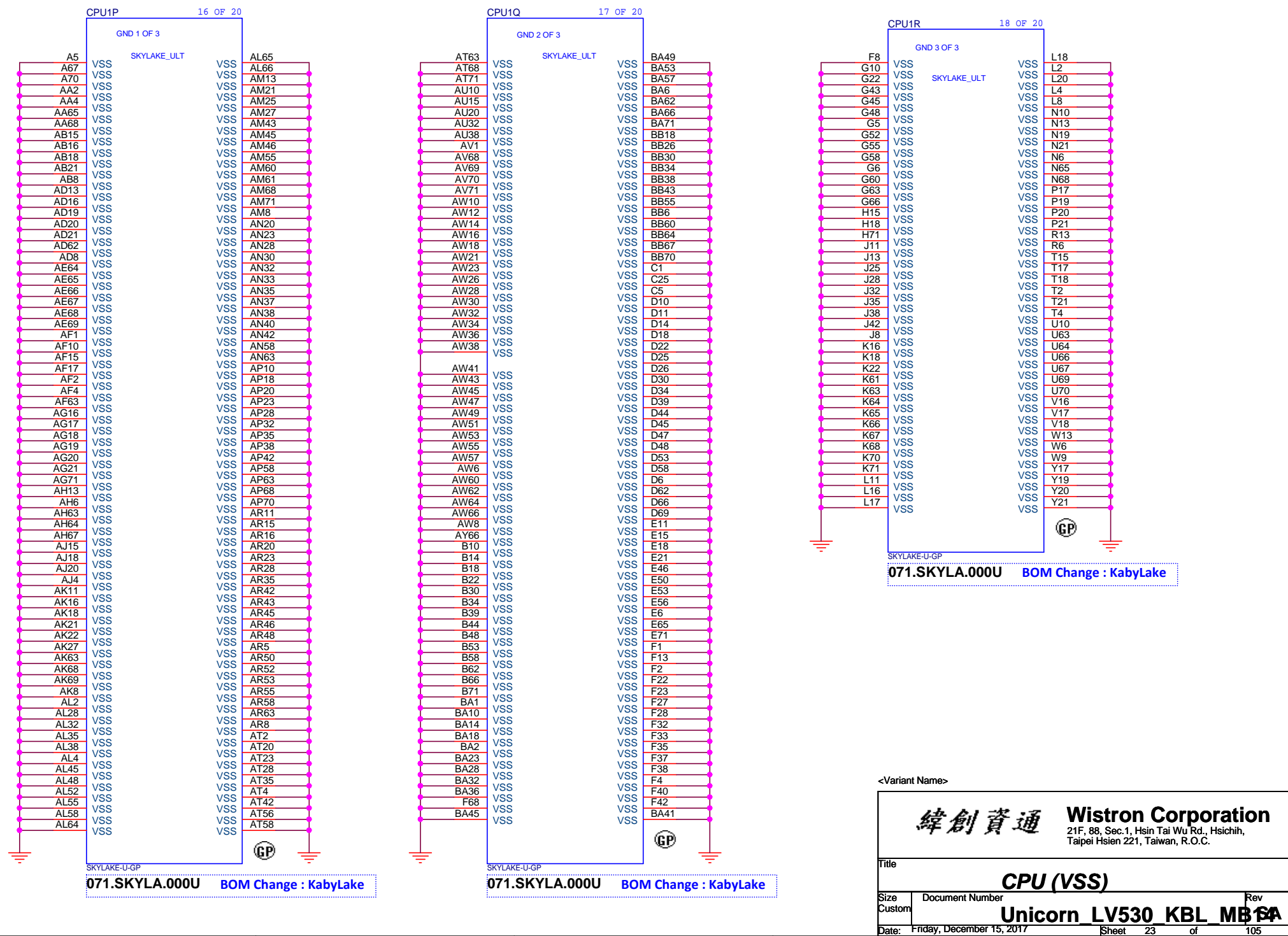
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
CPU (RSVD)

Size A4 Document Number Unicorn LV530 KBL MB GA Rev

Date: Friday, December 15, 2017 Sheet 22 of 105

Main Func = PCH



<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (VSS)

Size Custom

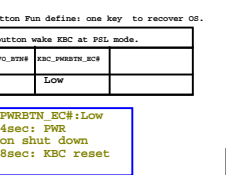
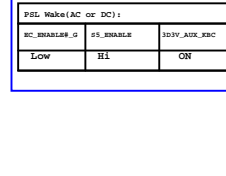
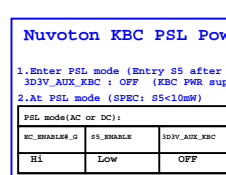
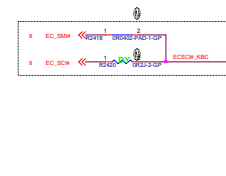
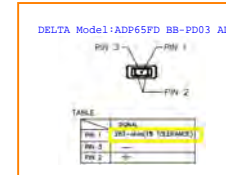
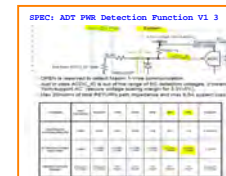
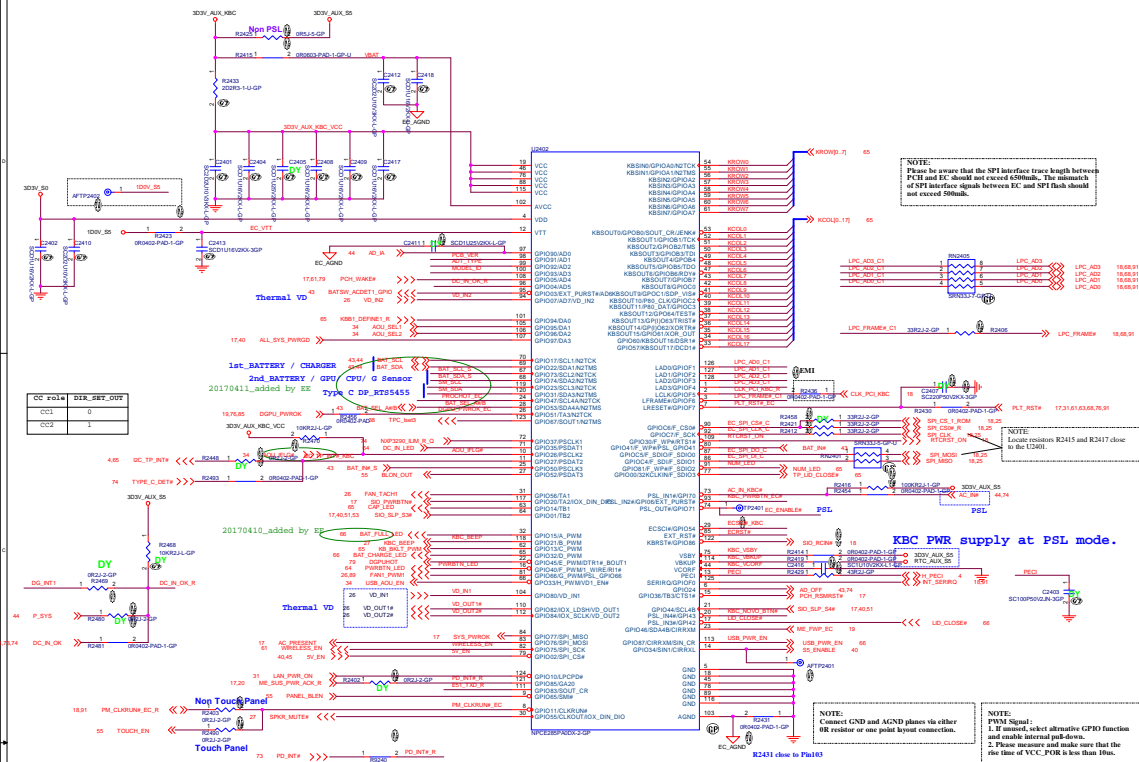
Document Number

Rev

Unicorn LV530 KBL MB 6A

Date: Friday, December 15, 2017

Sheet 23 of 105



Model ID BOM Ctrl

PCB VERSION	ADP(PWR)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
ES1_KBL	100.0K	100.0K	64.18025.1.0L	3.0V
ES3_KBL	100.0K	100.0K	64.28025.1.0L	2.75V
V30_KBL	100.0K	100.0K	64.18025.1.0L	2.40V
V30_KBL	100.0K	100.0K	64.27025.1.0L	2.34V
NA	100.0K	100.0K	64.28025.1.0L	2.8V
V10-KBL	100.0K	100.0K	64.28025.1.0L	1.8V
NA	100.0K	100.0K	64.28025.1.0L	1.84V

PCB VERSION

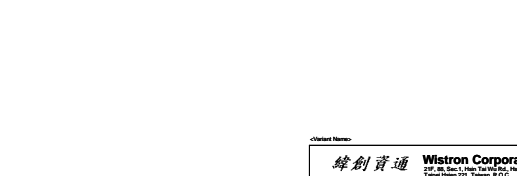
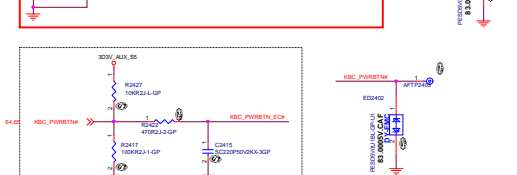
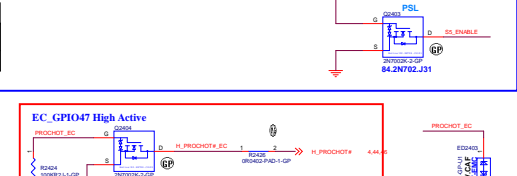
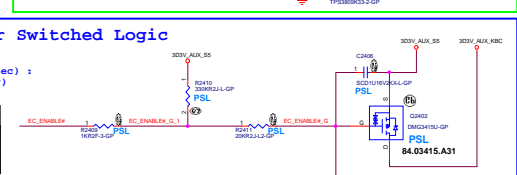
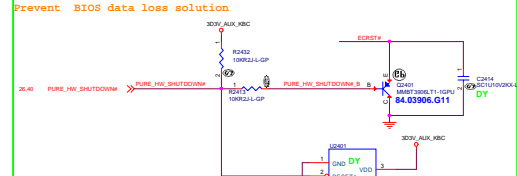
PCB VERSION	ADP(PWR)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
NA	100.0K	100.0K	20.0K	2.75V
NC	100.0K	100.0K	33.0K	2.40V
ND	100.0K	100.0K	47.0K	2.34V
-1M	100.0K	100.0K	64.9K	2.8V
PTV BC051	2	100.0K	100.0K	1.65V
-3M	100.0K	100.0K	133.0K	1.41V
-4	100.0K	100.0K	174.0K	1.30V

DELTA Model:ADP65FD BB-PD03 ADP

45W 65W
High: 45W / Low 65W
DISCRETE#
High: UMA / Low: Discrete

ADP internal Resis 287ohm
3.3*287/1037=0.91V (65W)

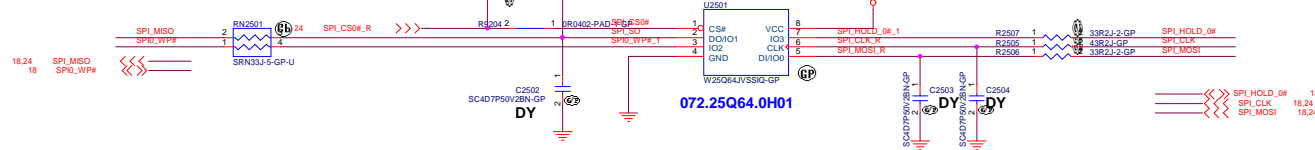
AC Adapter: ADT_TYPE System Power Limit
130W 1.45V < ID < 2.105V 90W
90W 1.172V < ID < 1.618V 90W
65W 0.690V < ID < 1.154V 65W
45W 0.234V < ID < 0.660V 45W



SSID = Flash.ROM

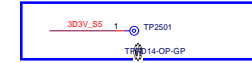
SPI ROM Equal length need to less than 500mil

1ST	MXIC	8MB	072.25647.000D
2ND	WINBOND	W25Q64JVSSIQ	8MB 072.25Q64.0H01
3RD	GIGA DEVICE	8MB	072.25B64.0C01

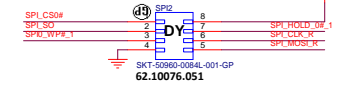


16MB SOIC8
WINBOND W25Q128FVSIQ/ 72.25128.0E1
WINBOND W25Q128FVSIQ/ 072.25128.0AC1
MACRONIX MX25L12873FM2I-10G/ 72.12873.001
MACRONIX MX25L12873FM2I-10G/ 072.25128.0B11

Test point

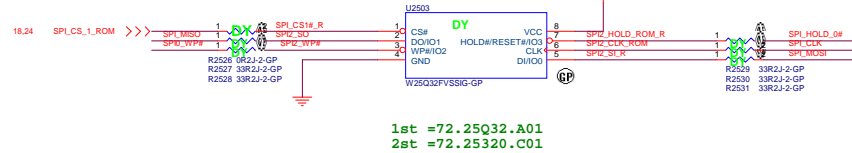


SPI ROM Socket (SPI2)



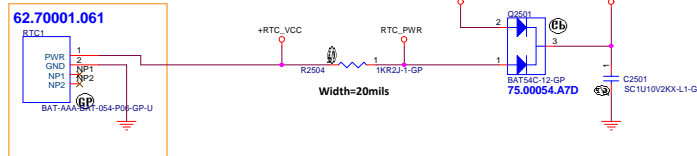
Co-Layout Design on U2501

SPI FLASH ROM 4M byte



SSID = RBATT

20170320_need check pin define with ME



Test point

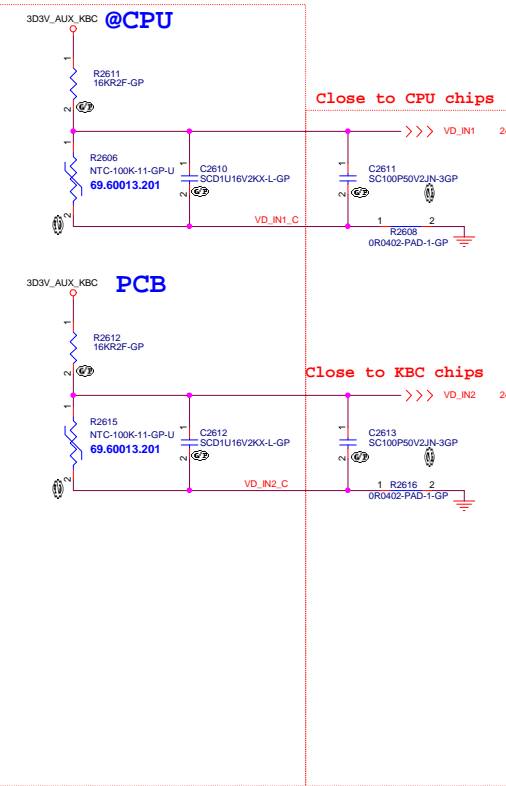


High Detect
Need to Check whether to PD in PCH Side

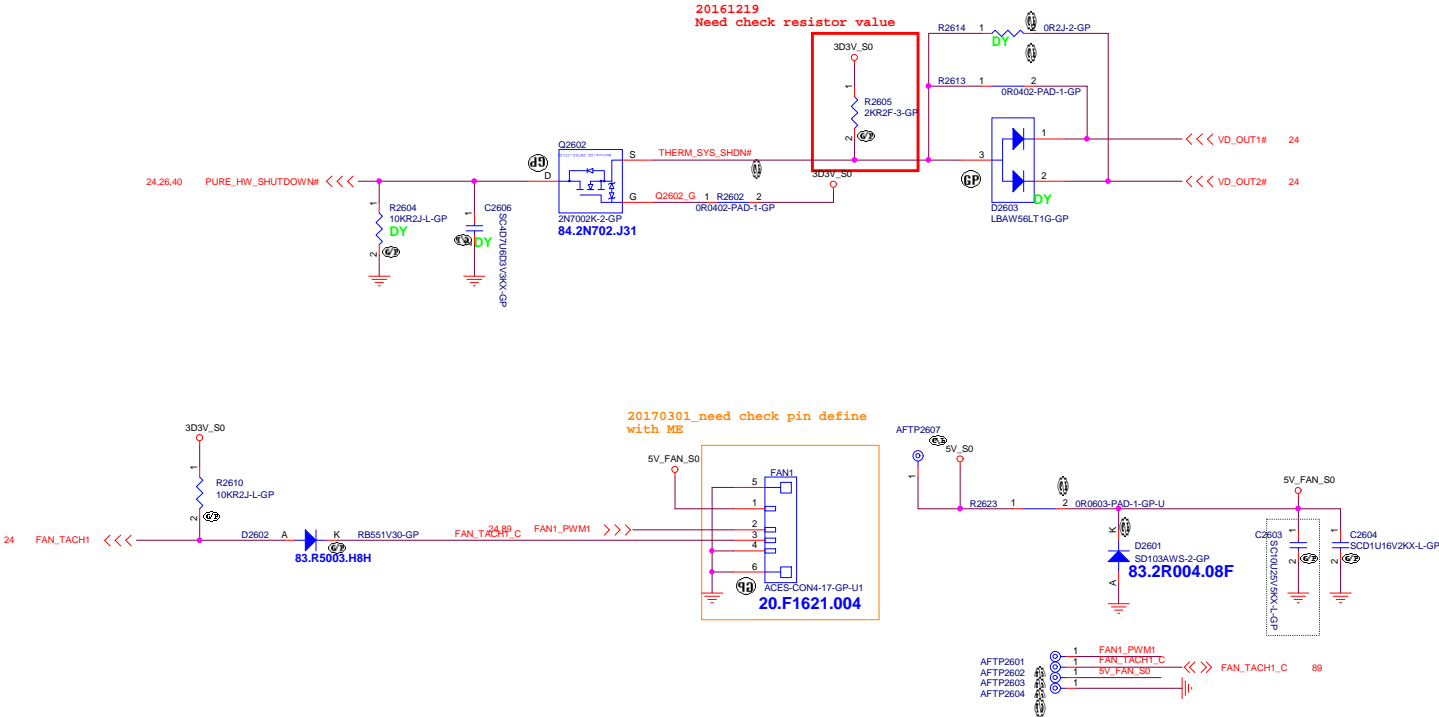
Variant Name

Main Func = Thermal Sensor

Close to Thermal sensor

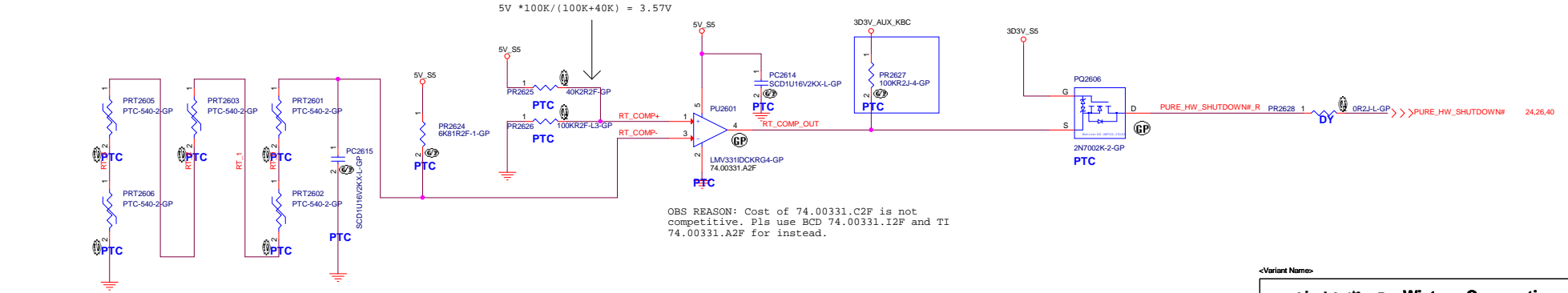


20161219
Need check resistor value



PURE_HW_SHUTDOWN# logic table

signal name	Sys. Temp < Ref. Temp	Sys. Temp > Ref. Temp
RT_COMP_OUT	High	Low
PURE_HW_SHUTDOWN#	High	Low



OBS REASON: Cost of 74.00331.C2F is not competitive. Pls use BCD 74.00331.I2F and TI 74.00331.A2F for instead.

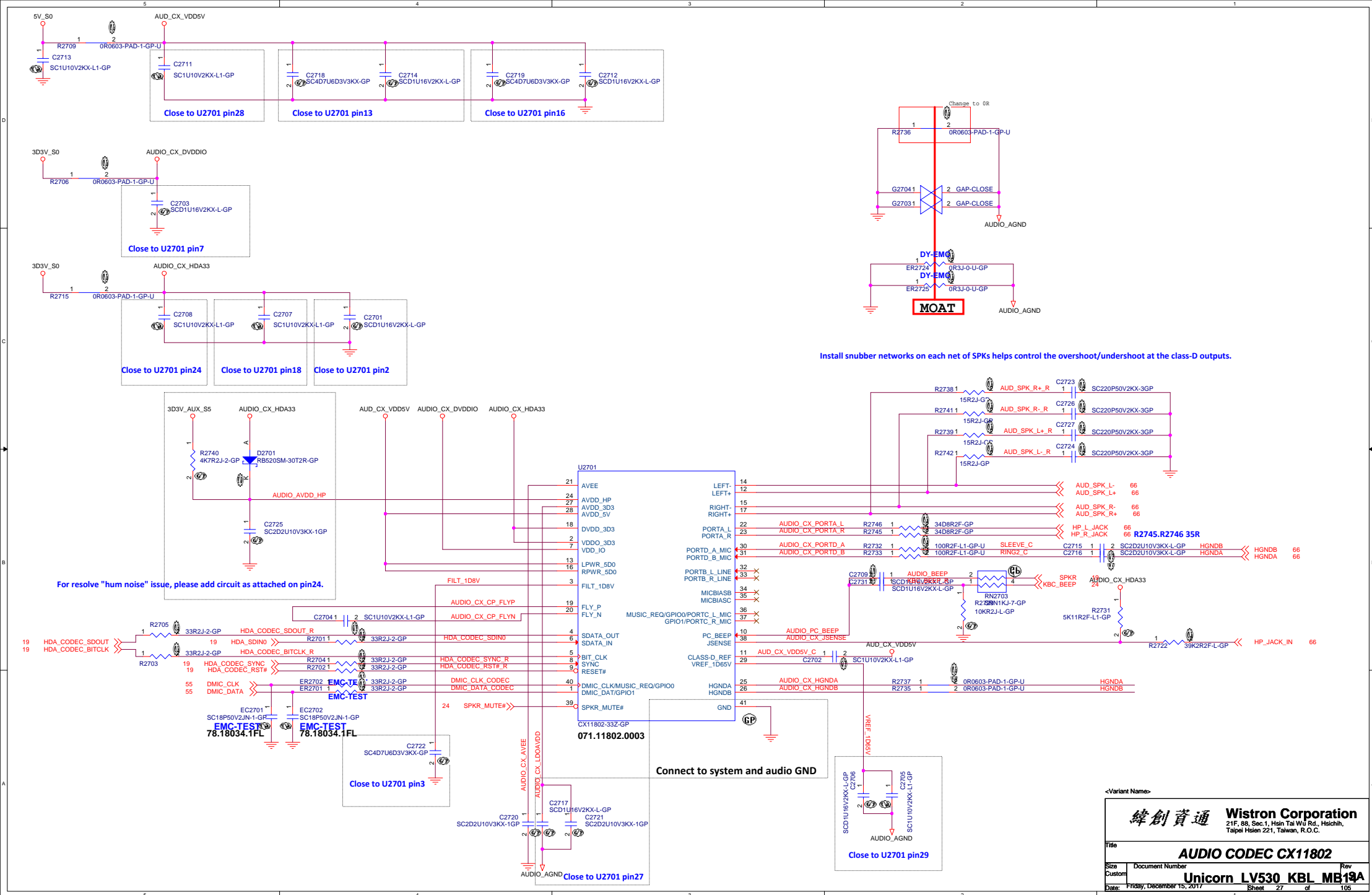


TABLE : Automatic Switching Mode (CFG0 = H)

SW (DDI_PRIORITY2)

L Port 1 has higher priority when both ports are plugged
H Port 2 has higher priority when both ports are plugged

For Automatic Switching Mode (CFG0 = H):

SW = L: Port1 has higher priority when both ports are plugged (default)

SW = H: Port2 has higher priority when both ports are plugged

Overwritten by I2C register in I2C Control Mode

Port 2 first

Layout note: extend the length to
6 inch for DP traces of PS8338B input

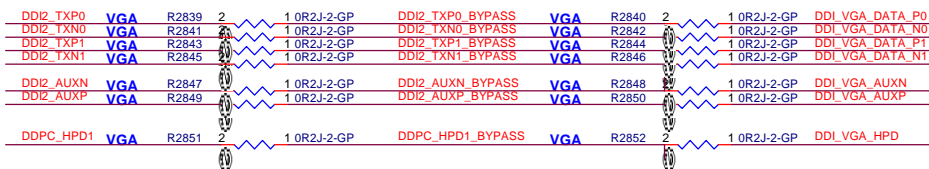
CPU side
DDI2 IO

TPAD14-OP-GP
TPAD14-OP-GP
TP2802 1 IN_DDC_SCL
TP2803 1 IN_DDC_SDA

20170301_need check with vendor

CPU side

Bypass DDI SW



Closed to
Type C DP Controller

to VGA DSUB

to Type C DP

20170301_need check with vendor

to Type C DP

to VGA DSUB

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

DDI Switch

Size

Document Number

Rev

A3

Unicorn LV530 KBL MB13A

Date:

Friday, December 15, 2017

Sheet

28

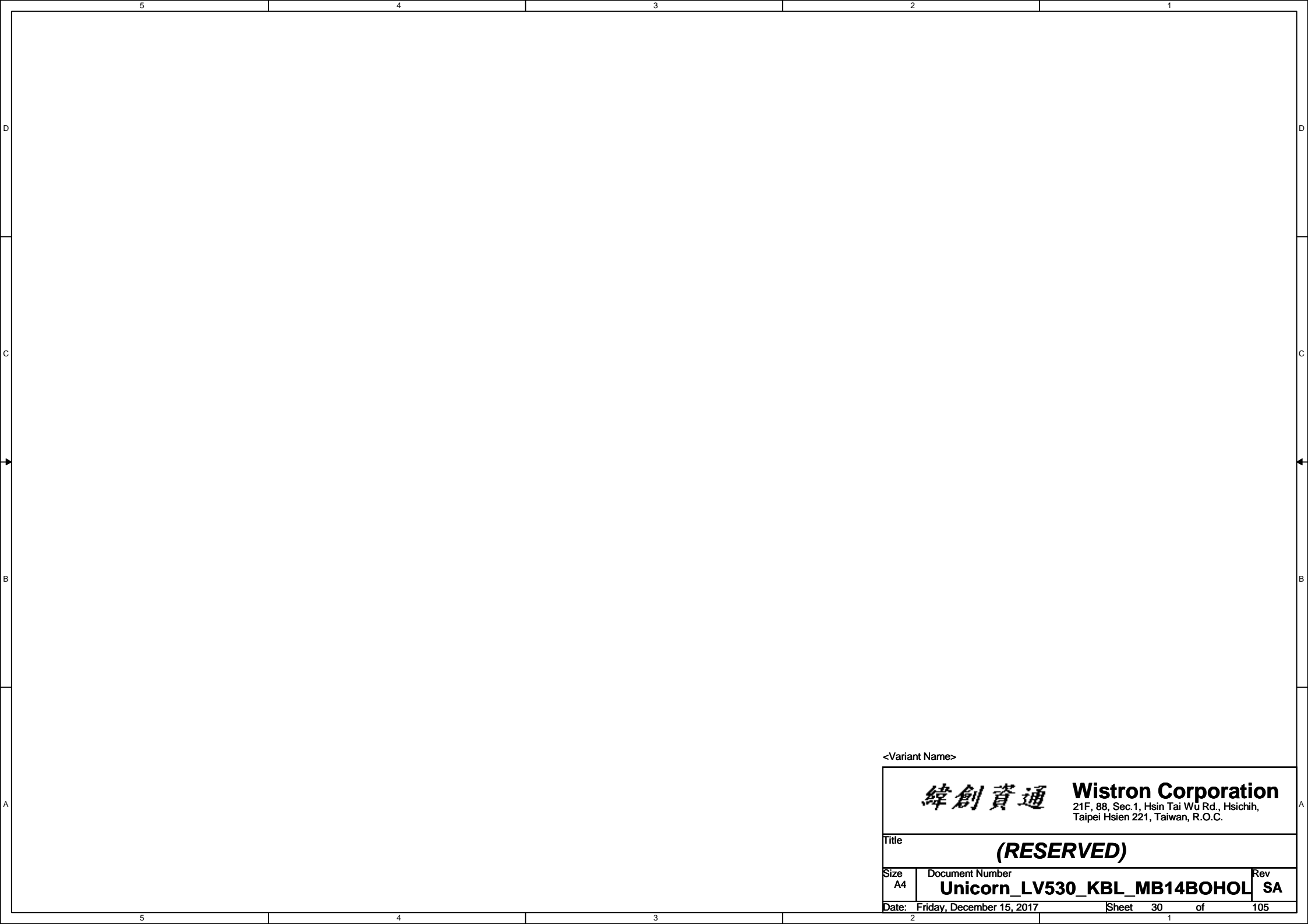
of

105

INTERNAL STEREO SPEAKERS

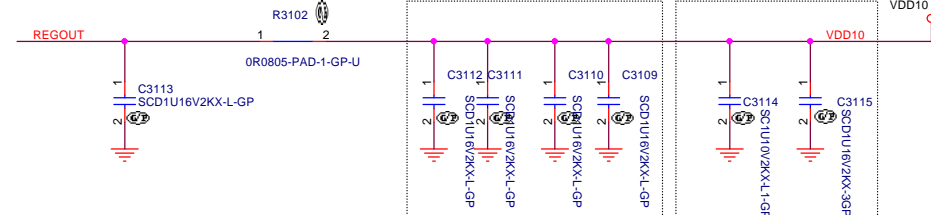
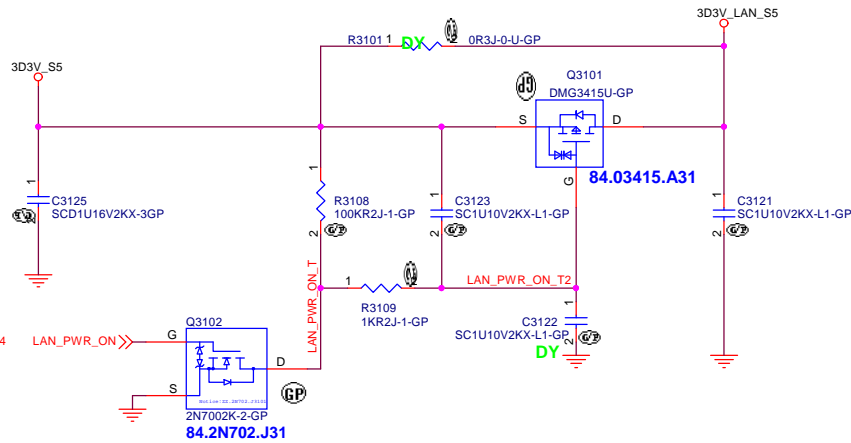
MOVE TO SMALL BOARD

<Variant Name>		
<div>緯創資通Wistron Corporation21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
AUDIO SPEAKER		
Size	Document Number	Rev
A3	Unicorn LV530 KBL MB13A	13A
Date: Friday, December 15, 2017	Sheet 29	of 105



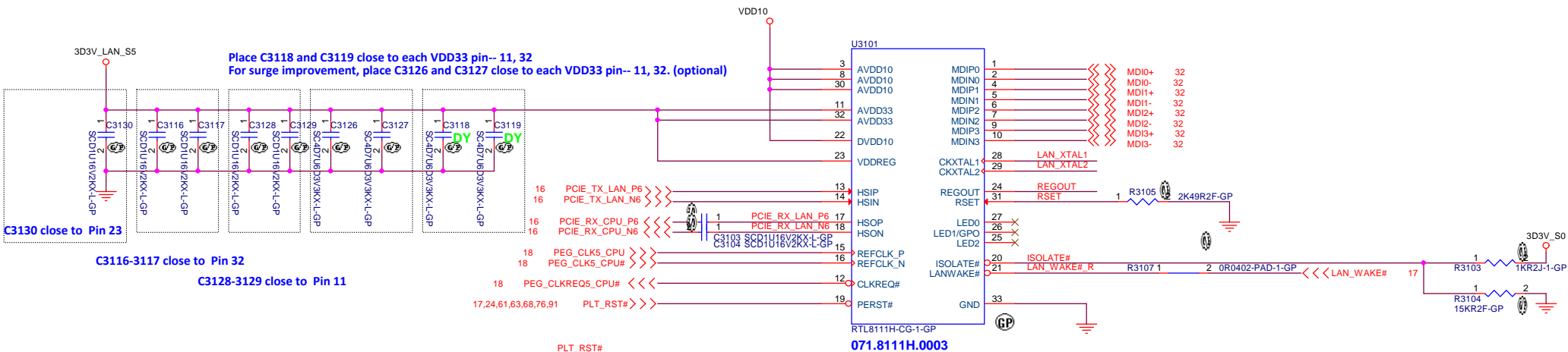
<Variant Name>

<div>緯創資通</div>		<div>Wistron Corporation</div>	
		<div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
<div>Title</div> <div>(RESERVED)</div>			
<div>Size</div> <div>A4</div>	<div>Document Number</div> <div>Unicorn_LV530_KBL_MB14BOHOL</div>		<div>Rev</div> <div>SA</div>
<div>Date:</div> <div>Friday, December 15, 2017</div>	<div>Sheet</div> <div>30</div>	<div>of</div> <div>105</div>	

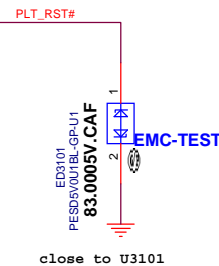
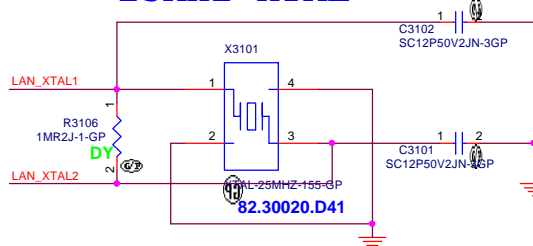


For RTL8111G(S)/ RTL8111GUS/ RTL8106EUS
 *Place C3109 to C3112 close to each VDD10 pin-- 3, 8, 22, 30

For RTL8111G(S)/ RTL8111GUS/ RTL8106EUS
 *Place C3114 and C3115 close to each VDD10 pin-- 22 (Reserved)

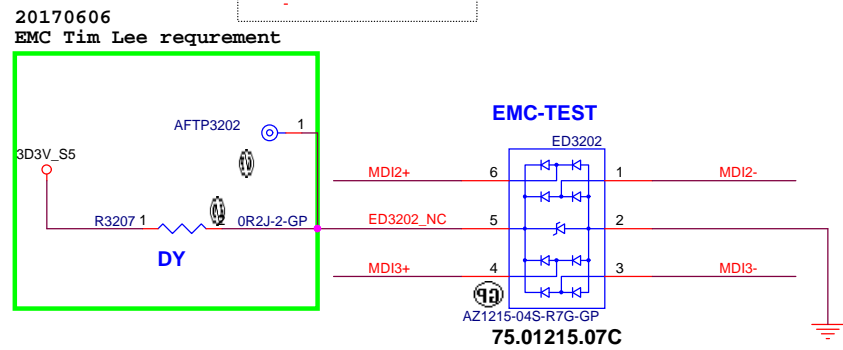
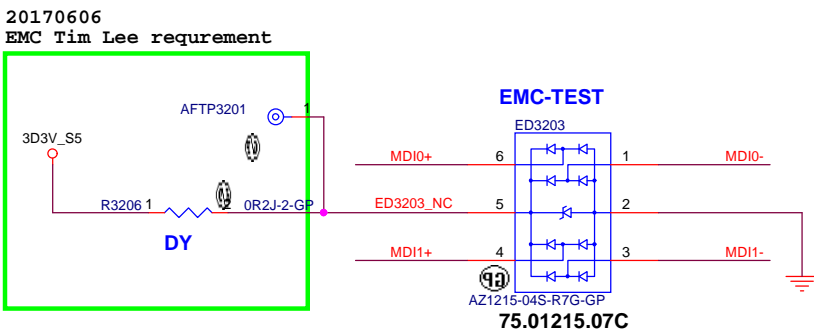
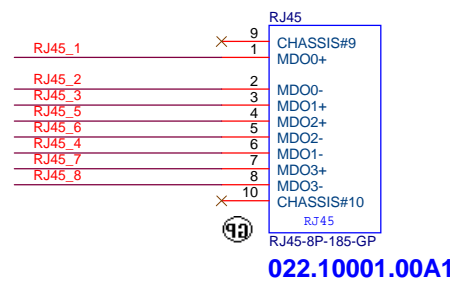
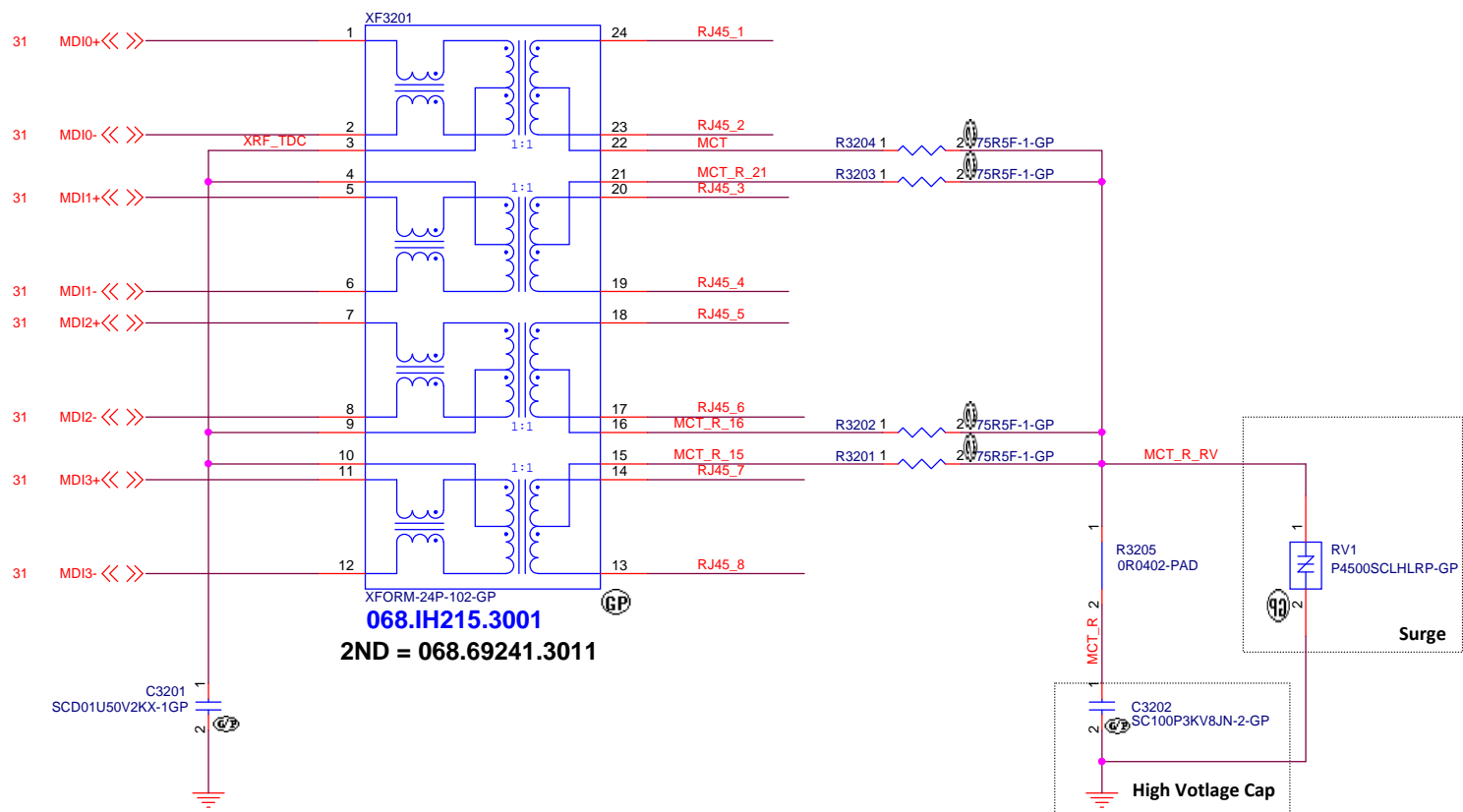


25MHz XTAL



10/100M/1000M Lan Transformer

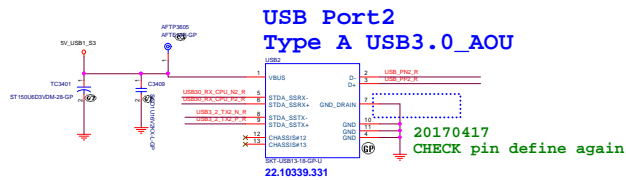
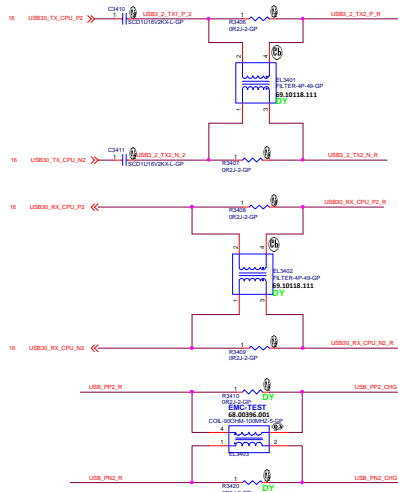
LAN Connector



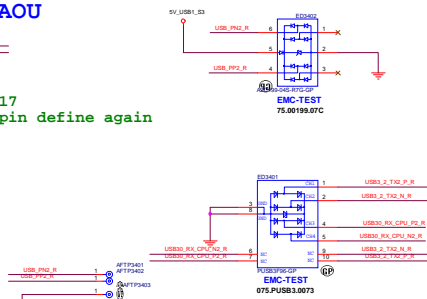
<Variant Name>

Title	
RJ45	
Size	Document Number
Custom	Unicorn LV530 KBL MB13A
Date:	Friday, December 15, 2017
Sheet	32 of 105

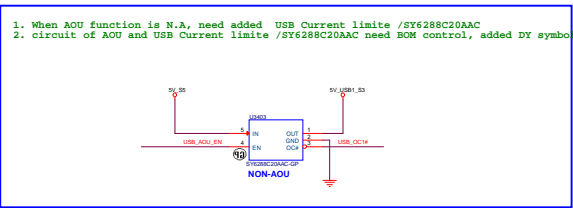
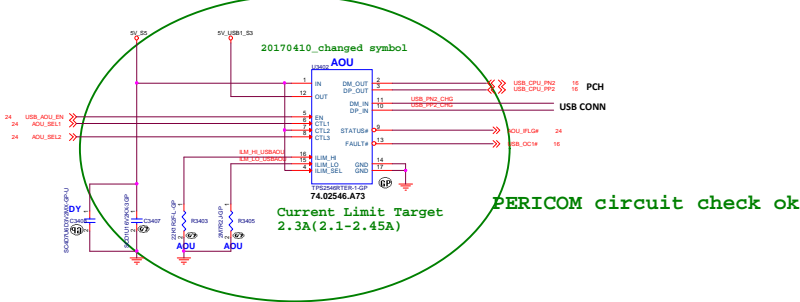
needReserve USB2.0 by pas AOU



USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	St-dA_SSRX-
6	St-dA_SSRX+
7	GND
8	St-dA_SSTX-
9	St-dA_SSTX+



AOU
1ST,
TI, 74.02546.A73
IC PWR SW TPS2546RTER QFN 16P(REV 1.1)
2ND
PERICOM, 074.52546.0A73
IC PWR SW PI5USB2546ZHEX TQFN 16P REV.X



RESERVED

<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB30 RE-DRIVER

Size

A3

Document Number

Unicorn_LV530_KBL_MB13A

Rev

13A

Date: Friday, December 15, 2017

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<Variant Name>	
<div>緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipin Hsien 221, Taiwan, R.O.C.</div>	
File	
(RESERVED)	
Size	Document Number
A2	Unicorn LV530 KBL MB 6A
Date: Friday, December 15, 2017	Sheet 36 of 105

5	4	3	2	1
D				
C				
B				
A				

<Variant Name>

<div>緯創資通</div>		<div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title			
TYPEC USB3.1-1			
Size	Document Number		Rev
A4	Unicorn LV530 KBL MB		1A
Date:	Friday, December 15, 2017	Sheet 37 of	105

[illegible]075.PUSB3.0073
USB_TypeC_EMC-TEST

20170302
check with vendor

[illegible]

20170322
update by EE

Over-current protection

$$I_{\text{LIM}} \text{ (A)} = 6800 / R_{\text{SET}} \text{ } (\Omega)$$

R3835/ 2.15K>>3.16A
R3835/ 2.15K + R3836/ 5.1K >> 0.94A

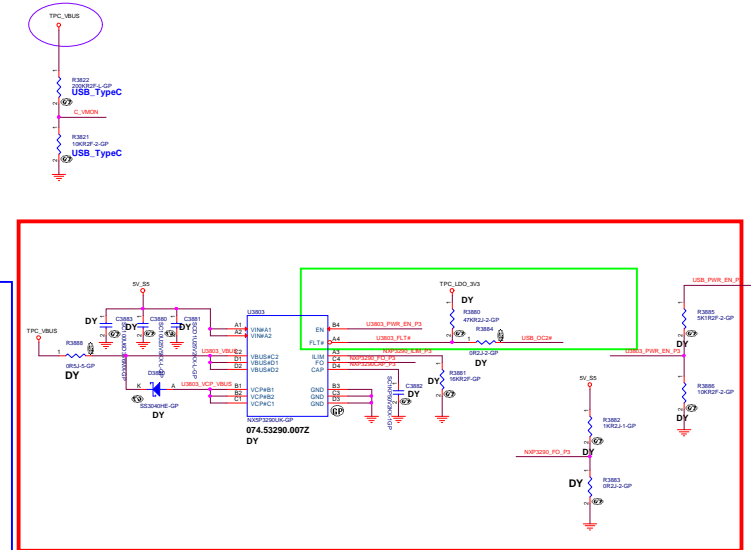
Diagram illustrating the USB TypeC connector configuration. The diagram shows the following connections:

- R16** (Green): Connected to **RX3DS** and **MCR224-GP**.
- R17** (Green): Connected to **RX3DS** and **USB_P2WR_EN_P3**.
- R18** (Green): Connected to **RX3DS** and **USB_TypeC**.
- 5V_5S** (Red): Supply voltage pin.
- Ground** (Red): Ground connection.

Additional text in the diagram:

- 20170302** (Orange)
- check with vendor** (Orange)
- High active** (Blue)

High active

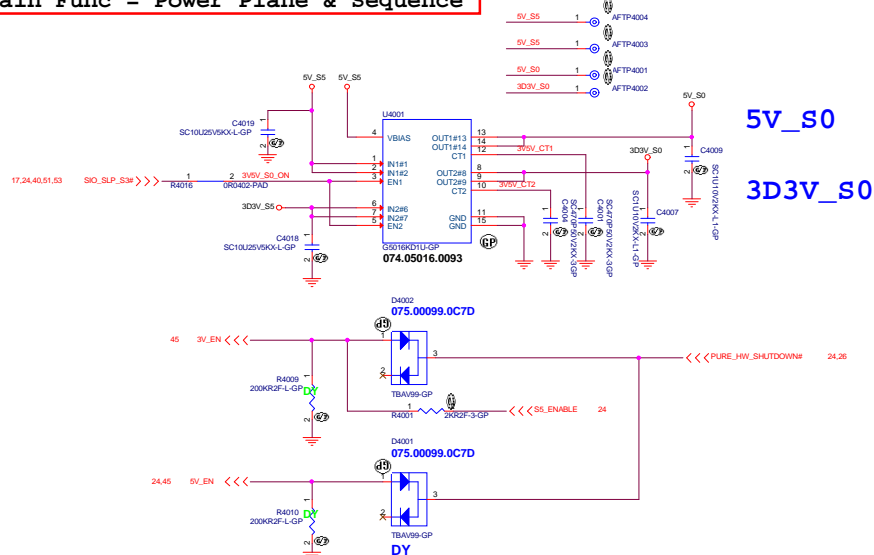
[illegible]

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

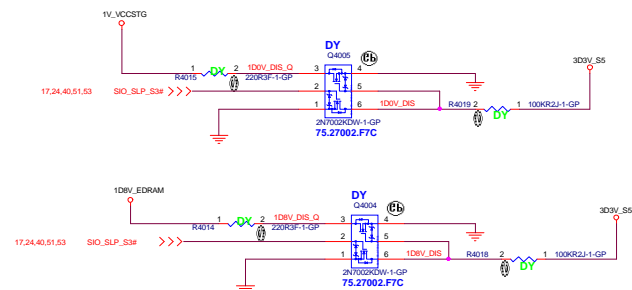
<Variant Name>

<Title>		緯創資通		Wistron Corporation	
				21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title					
Size	Document Number				Rev
A	Unicorn_LV530_KBL_MB14BOH01SA				1
Date:	Friday, December 15, 2017			Sheet 39 of	105

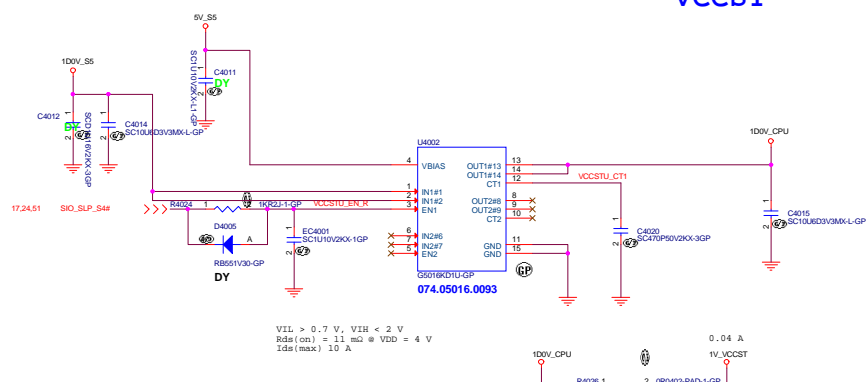
Main Func = Power Plane & Sequence



Discharge circuit



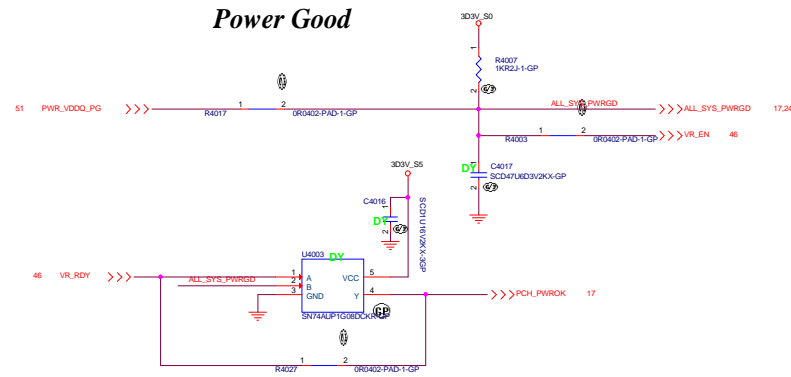
VCCST



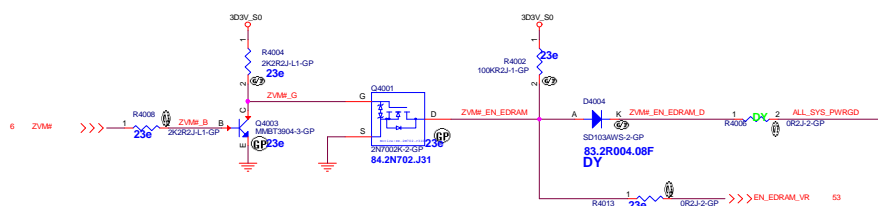
VIL > 0.7 V, VIH < 2 V
Rds(on) = 11 mΩ @ VDD = 4 V
Ids(max) 10 A

0.04 A

Power Good

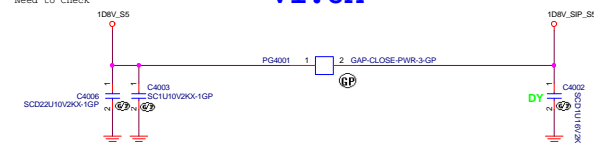


GT3 Low Power Circuit (ZVM)

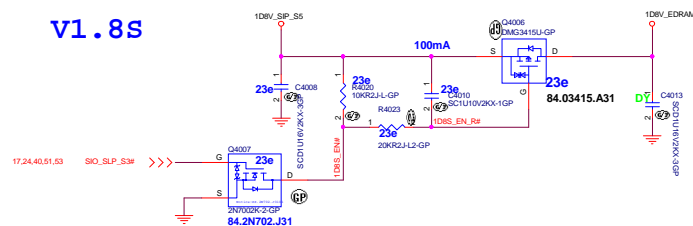


V1.8A

Need to Check



v1.8s



561280 KBL UY PDG Rev2.0 Notes:
On power up sequence, VCCOPC_p8 must never ramp up after VCCOPC/VCCOPIO under any circumstance.
There are no ramp down requirements between VCCOPC_p8 and VCCOPC/VCCOPIO.
Platform must guarantee VCCOPC/VCCOPIO rails do not start ramping back up for any reason while VCCOPC_p8 is ramping down or OFF.

<Variant Name>

緯創資通 Wistron Corporation 21F, 8F, Sec. 1, Hsin Tai Hsi Road, Hsinshui, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
POWER PLAN EN/SEQUE	
Size	Rev
Customs	Document Number
Unicorn LV530 KBL MB150HOL	
Date: Friday, December 10, 2017	Sheet 40 of 105

D

D

C

C

B

B

A

A

<Variant Name>

Title

<Title>

Size

A

Document Number

<Doc>

Rev

<RevCode>

Date:

Friday, December 15, 2017

Sheet

41

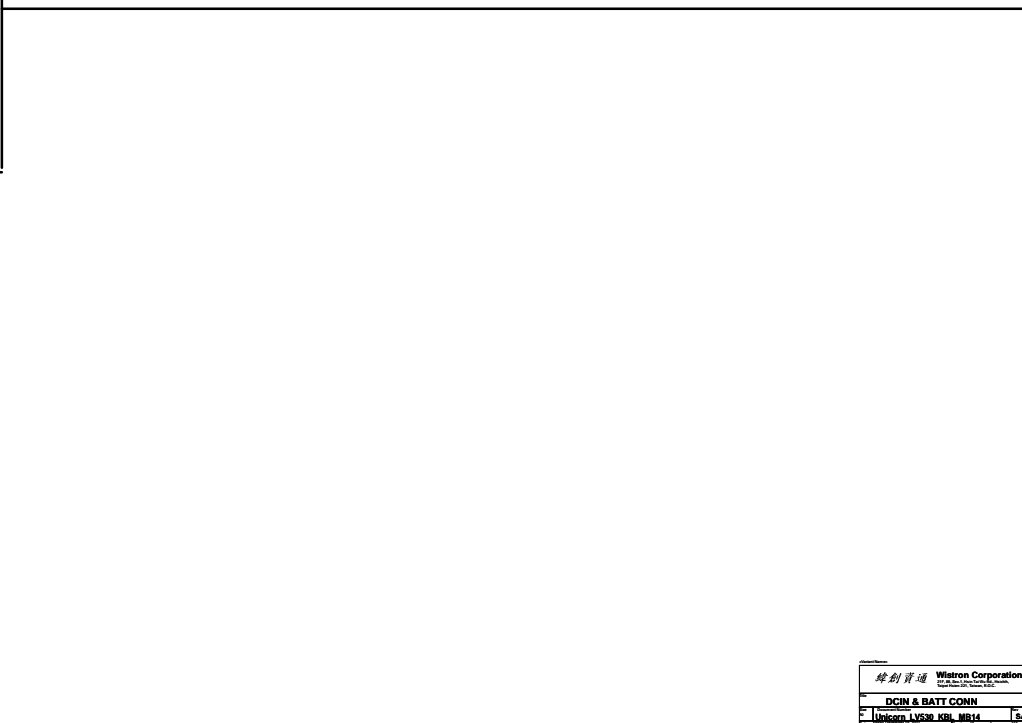
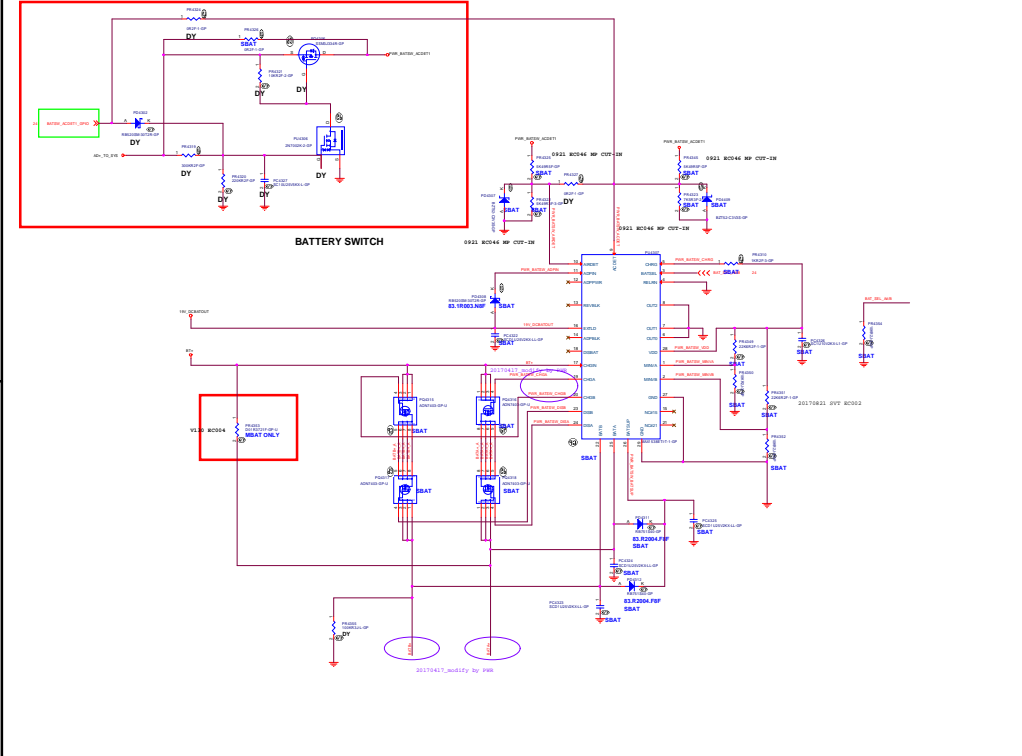
of

105

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<Variant Name>

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
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RESERVED		
Size	Document Number	Rev
A4	Unicorn LV530 KBL MB	1A
Date:	Friday, December 15, 2017	Sheet 42 of 105

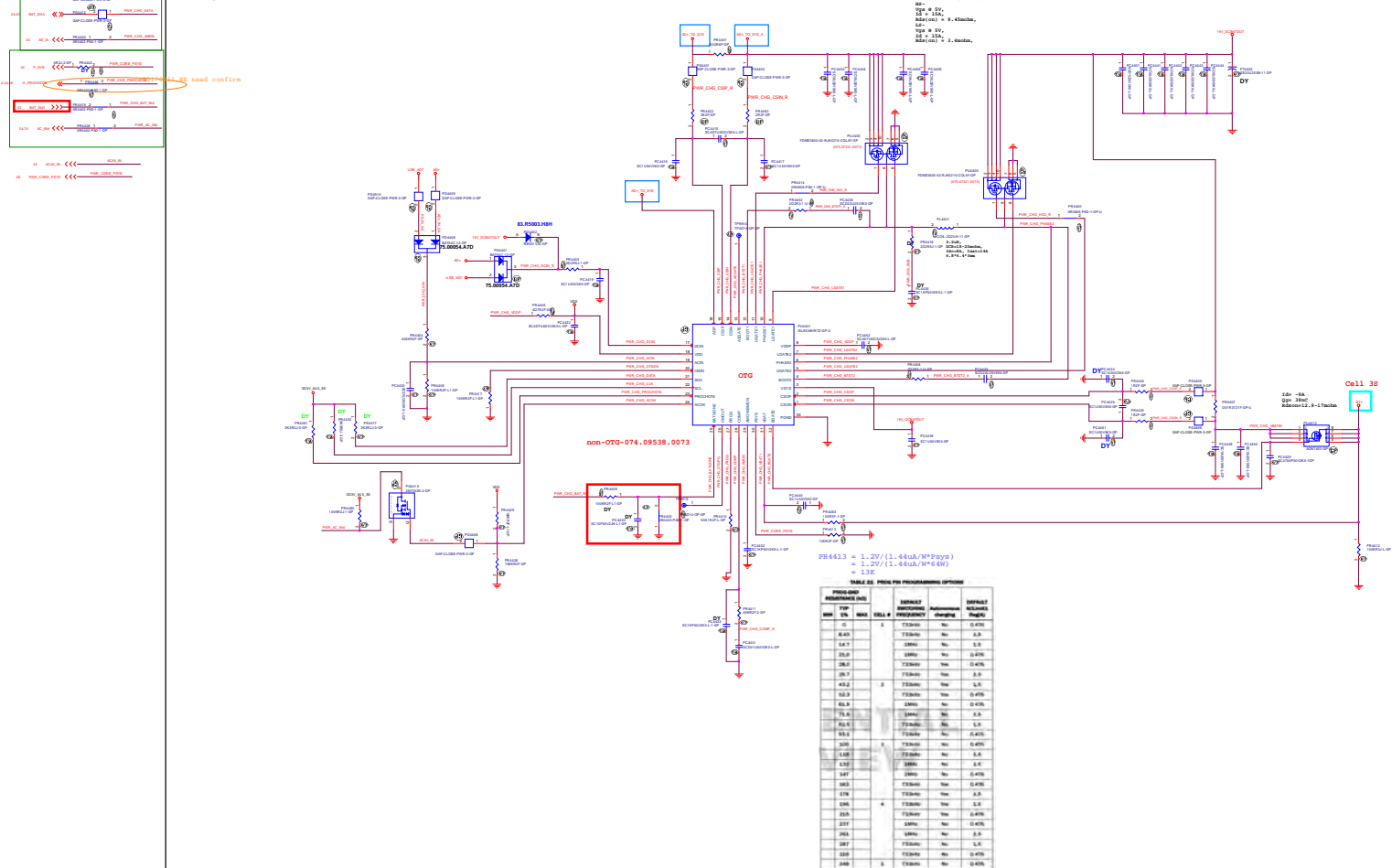


Main Func = Charger

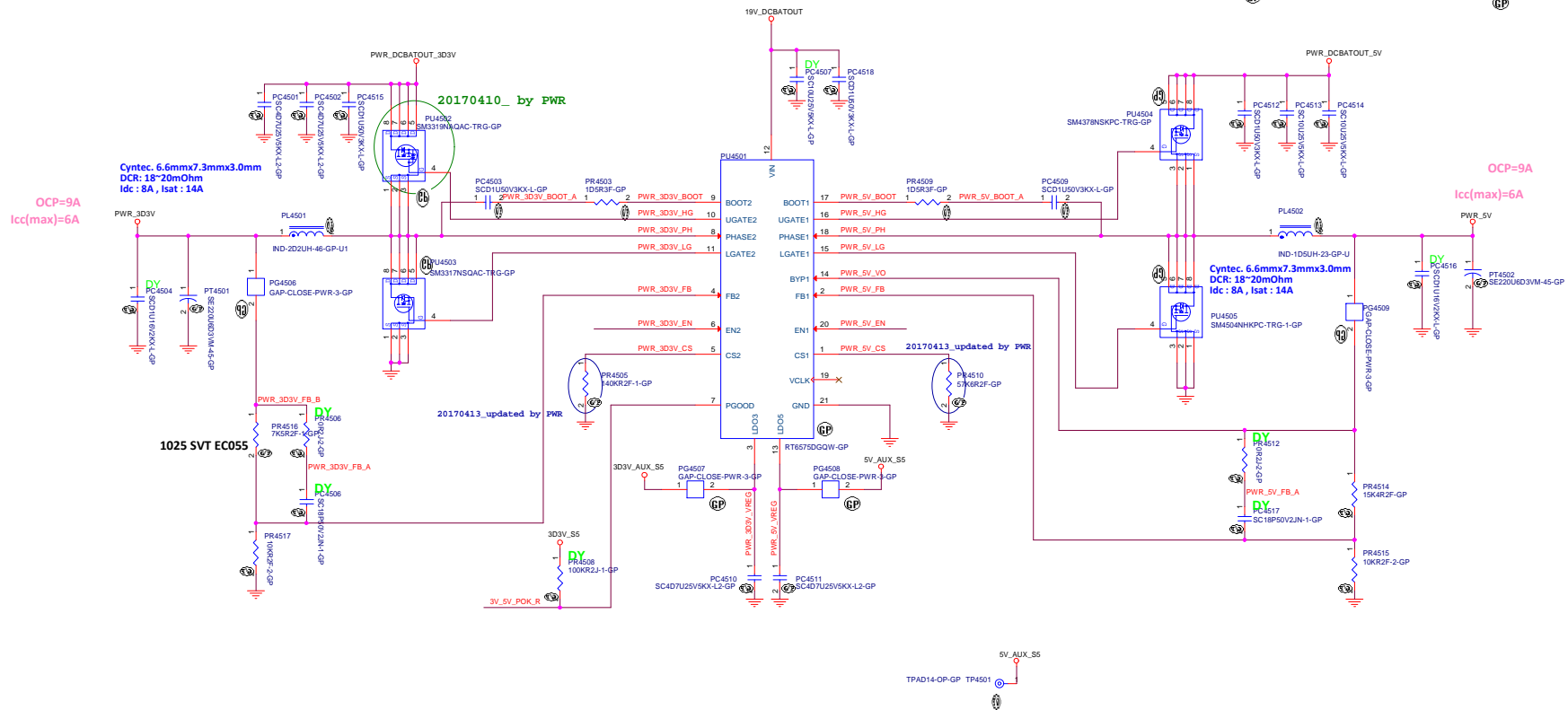
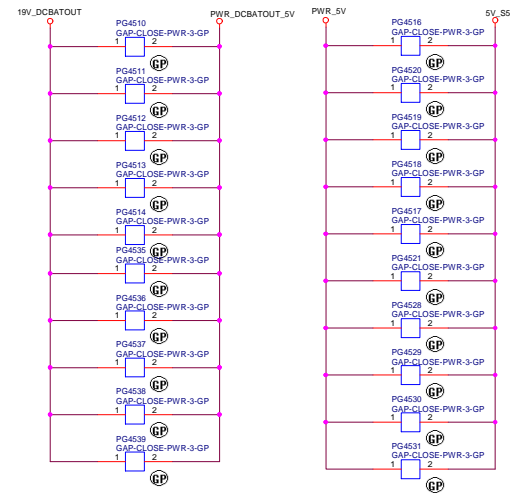
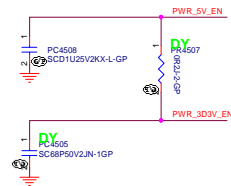
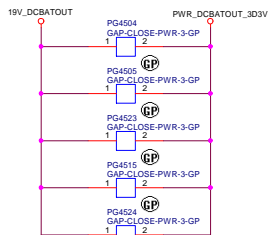
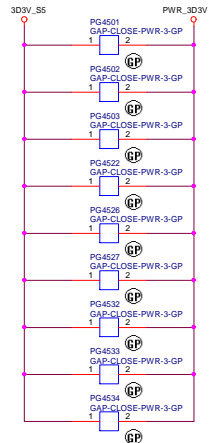
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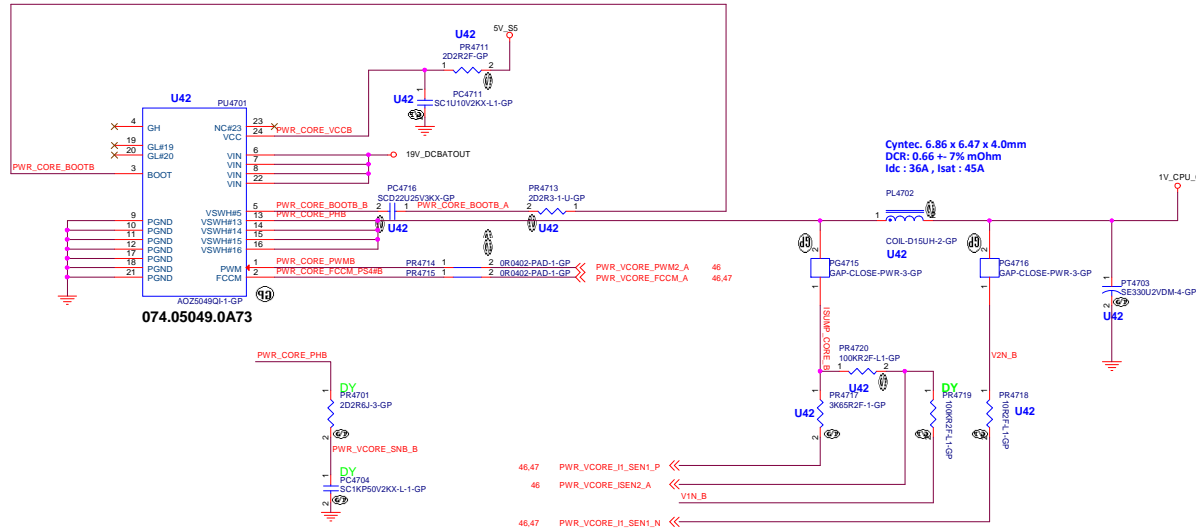
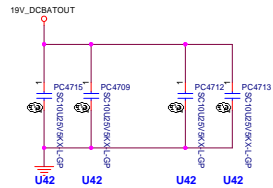
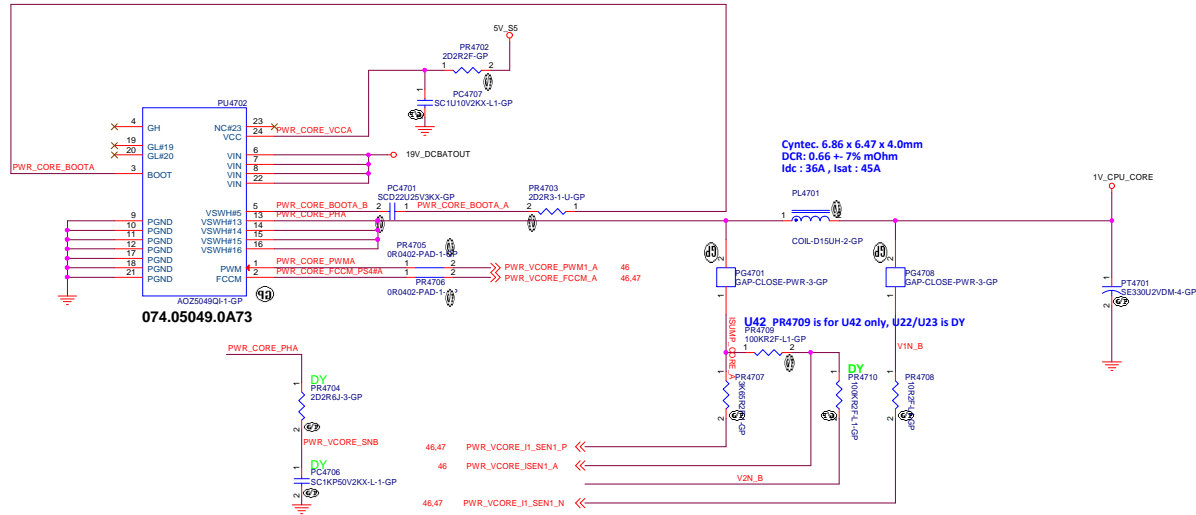
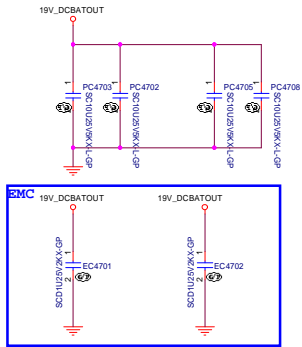
75.87333.071 CSD87330
ME-
Vgs @ 5V,
Id = 15A,
Rds(on) = 9.45mohm,
LE-
Vgs @ 5V,
Id = 15A,
Rds(on) = 3.6mohm,

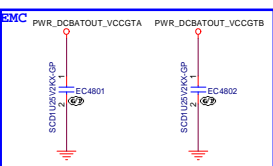
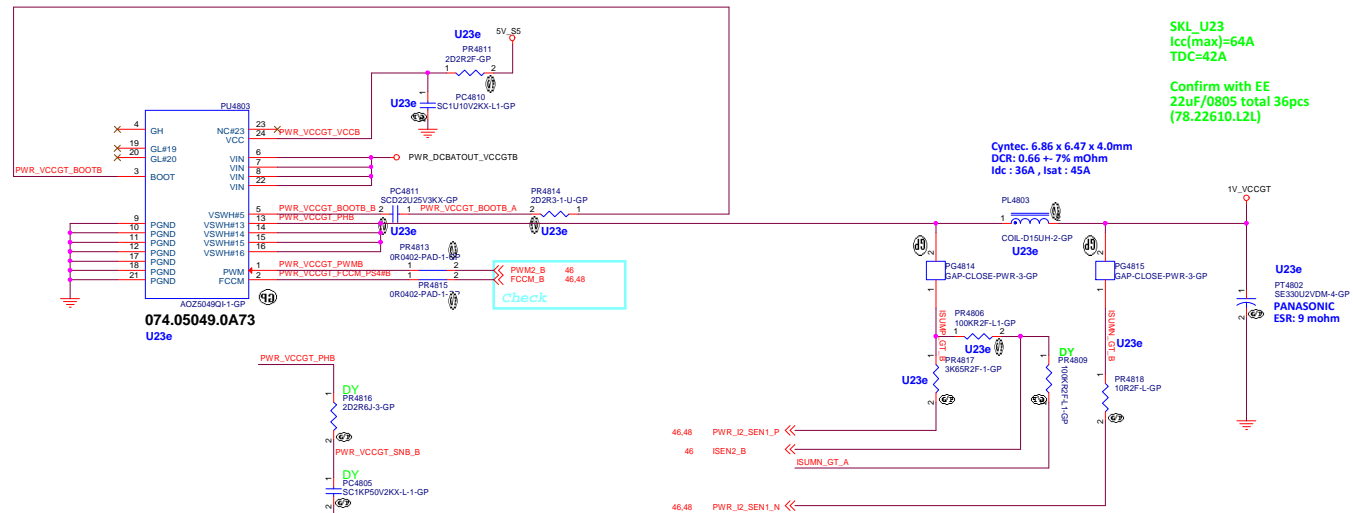
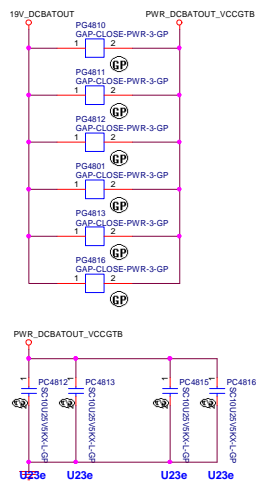
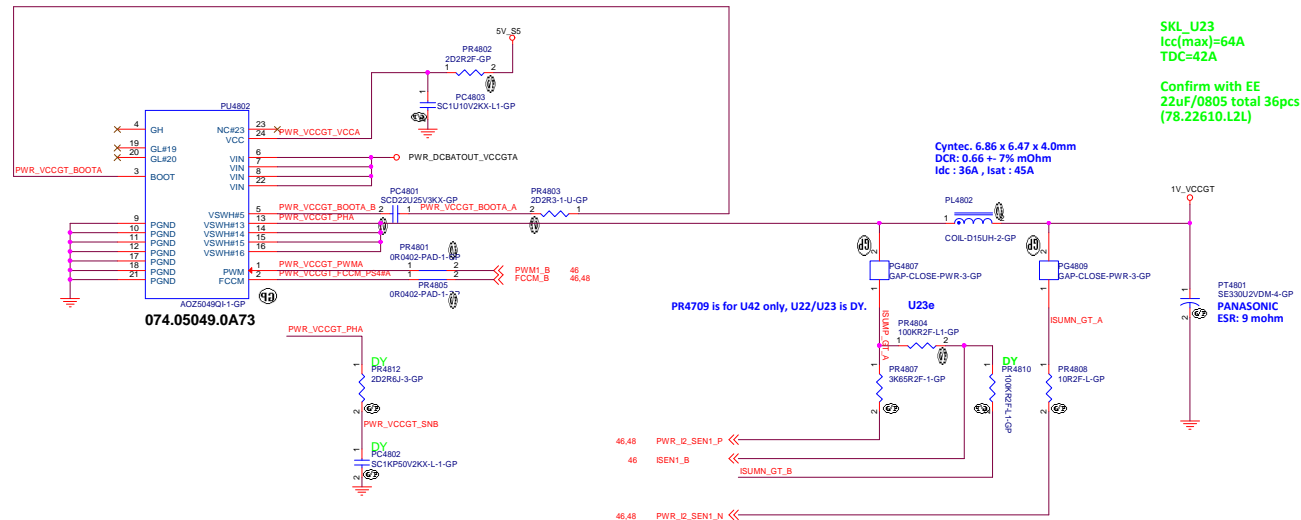
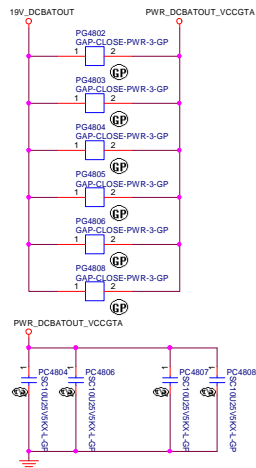
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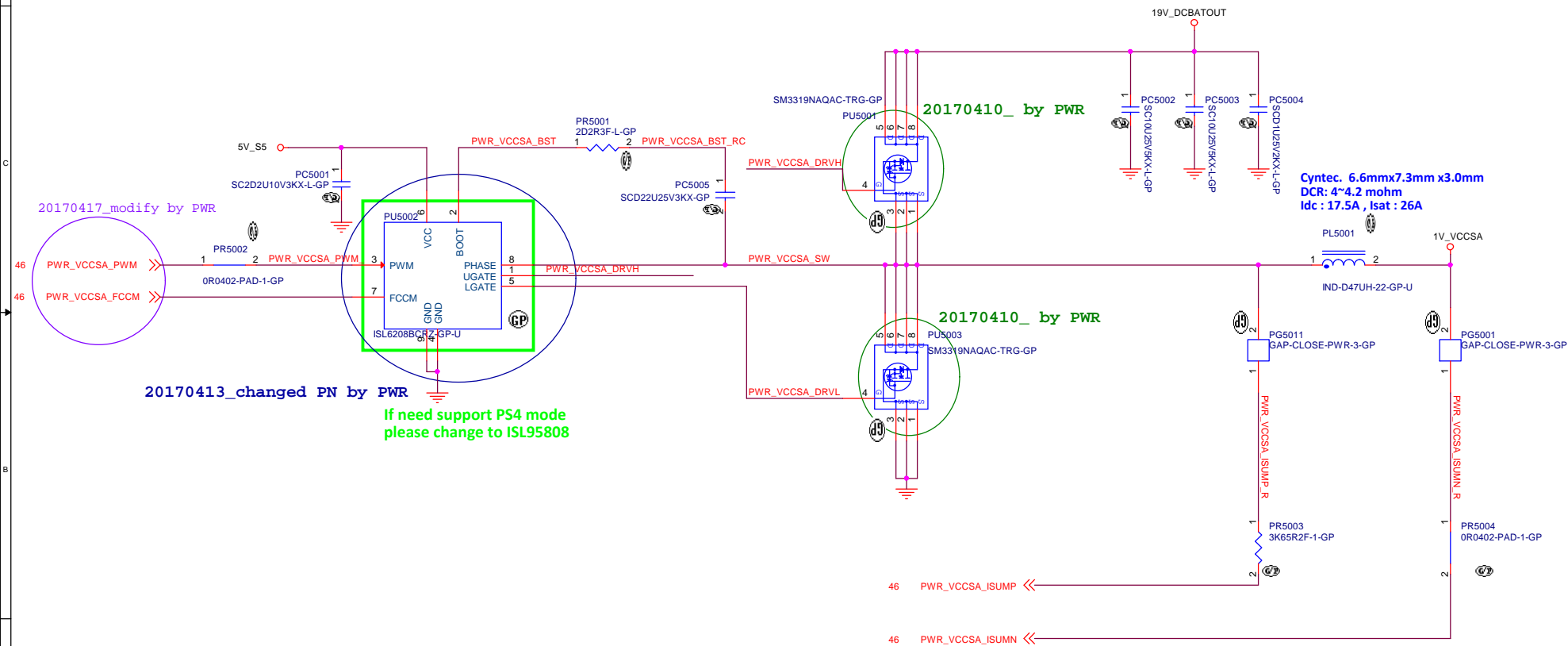
 Wistron Corporation 21/F, Sec. 1, Xinyi Center, No. 11, Sec. 4, Roosevelt Rd., Taipei 106, Taiwan, R.O.C.	
CHARGER(SI 9238HRT7)	
Part Number:	Unicorn LV530 KBL MB1500





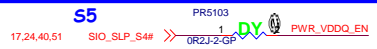


Main Func = CPU_CORE

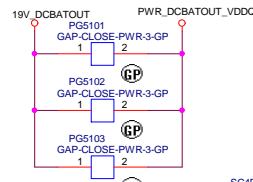
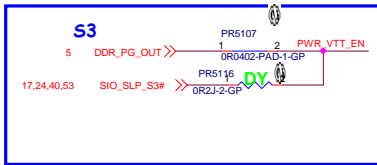


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S5

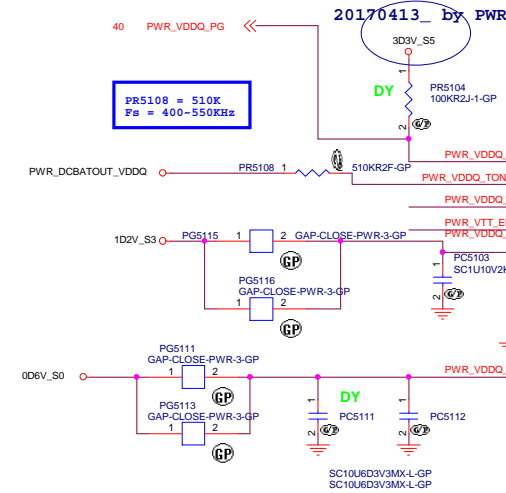


S3

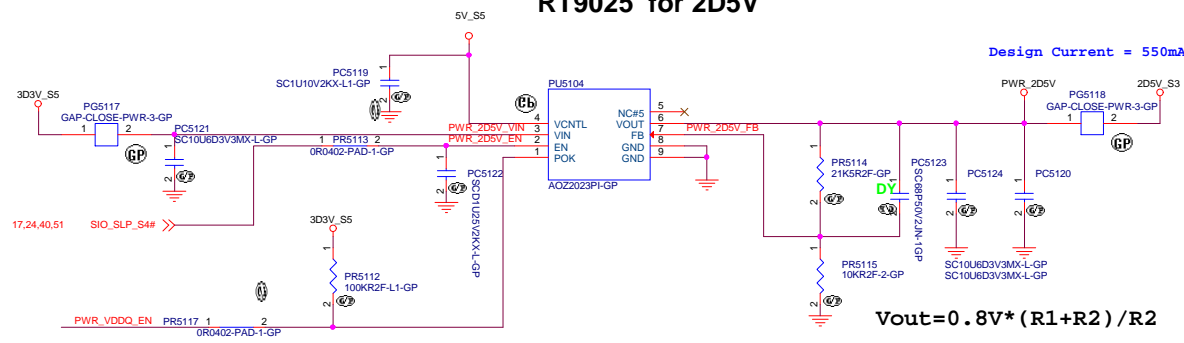


40

PR5108 = 510K
Fs = 400-550KHz



RT9025 for 2D5V



$$V_{out} = 0.8V * (R1 + R2) / R2$$

Design Current = 550mA

TDC : 8A

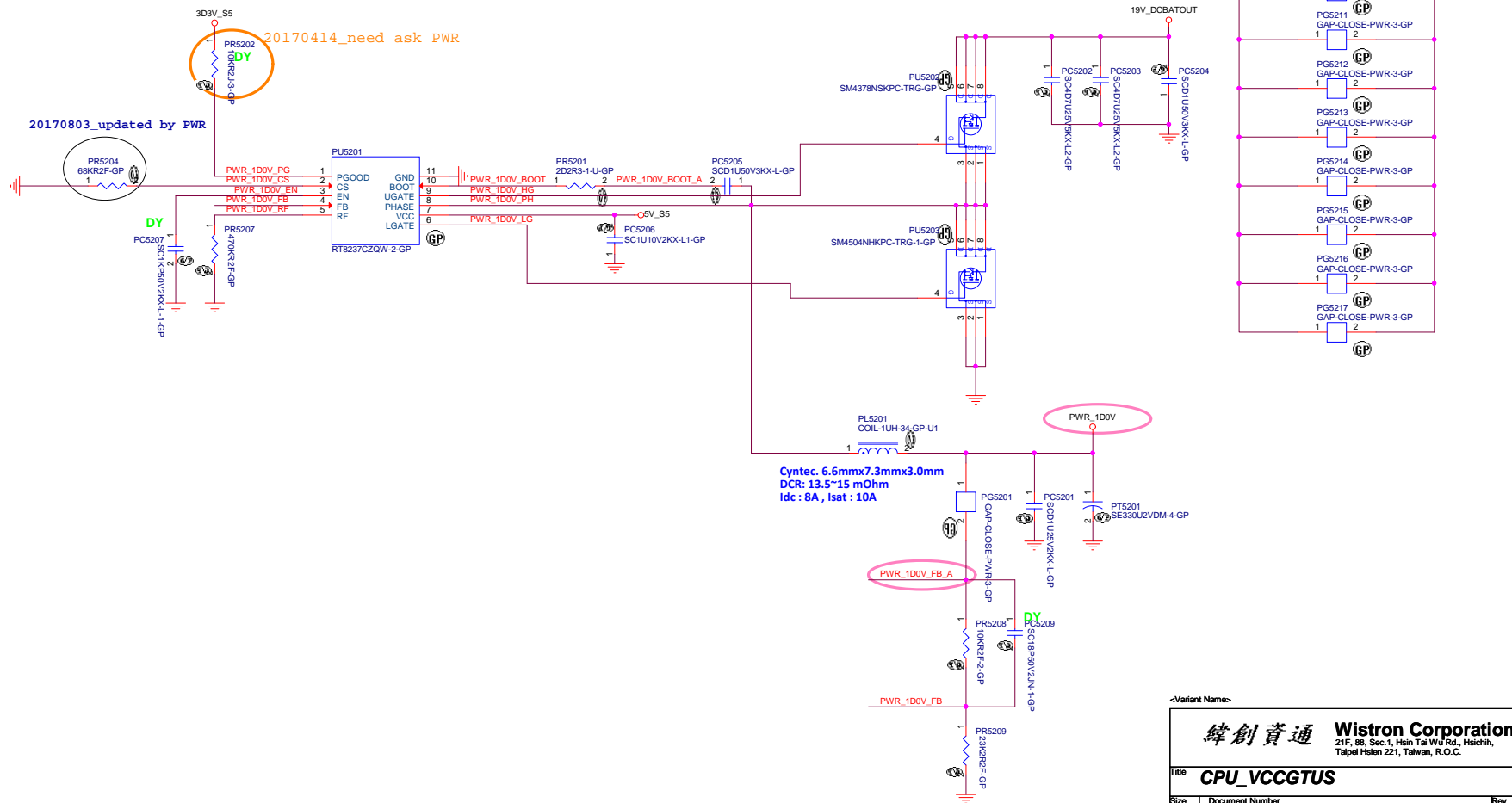
Cynotec, 7 x 7 x 3.0 mm
DCR: 9m~10mOhm
Idc : 11 A, Isat : 22A

$$V_{out} = 0.75 * (1 + R1/R2) = 1.2$$

BOM1

緯創資通 Wistron Corporation	
21F, 8B, Sec.1, Hsin Tai Wu Rd., Heichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title G5388_VDDQ	
Size Custom	Document Number
Unicorn LV530 KBL MB14A	
Date: Friday, December 15, 2017	Sheet 51 of 105

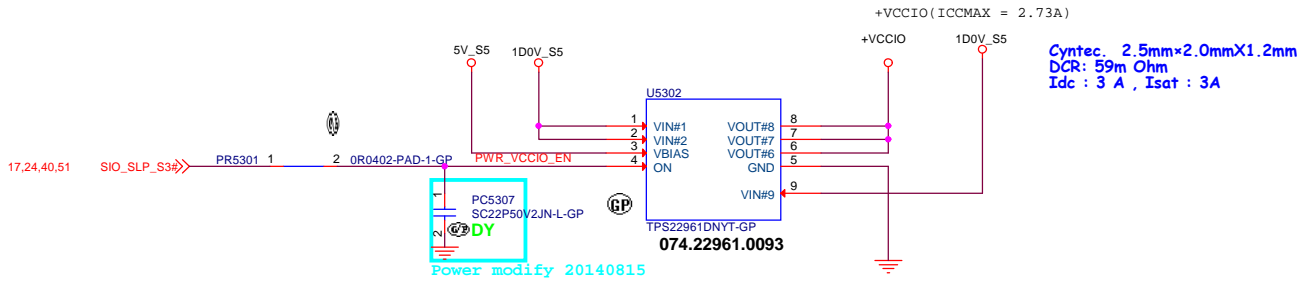
OFFPAGE



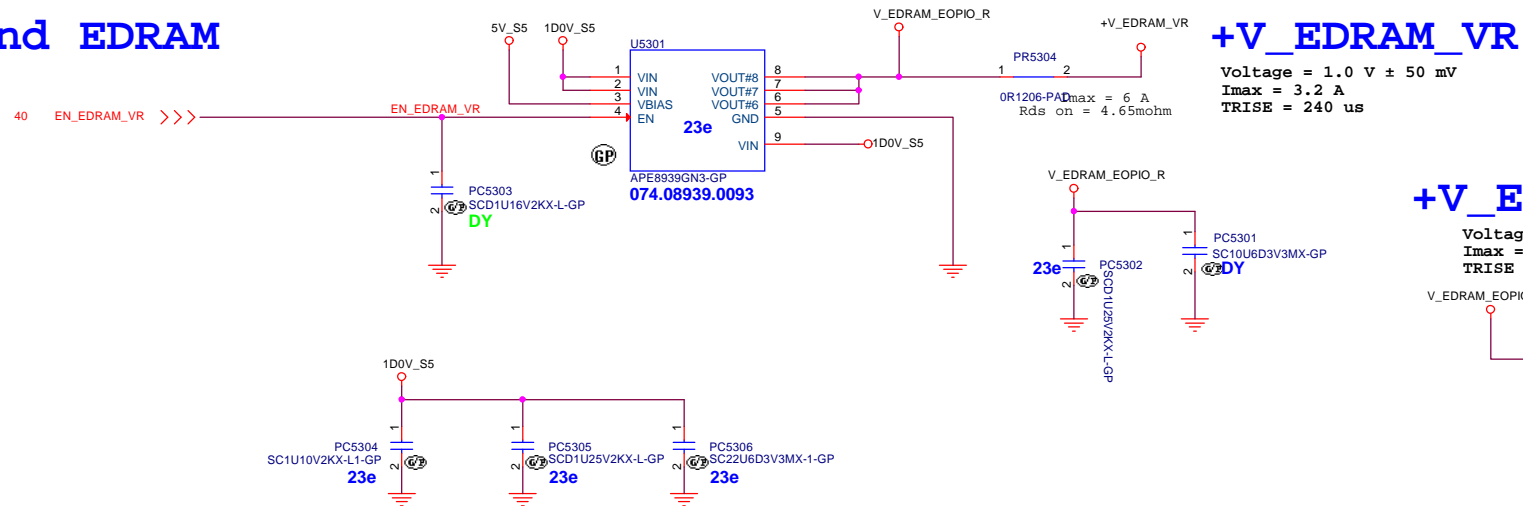
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Title	
CPU_VCCGTUS	
Size	Rev
Customer	Document Number
<div style="display: flex; justify-content: space-between; align-items: center;"> <div> <p>Unicorn LV530 KBL MB15A</p> </div> </div>	
Date:	Sheet
Friday, December 15, 2017	52 of 105

Main Func = 1D0V

VCCIO



EOPIO and EDRAM



+V_EOPIO_VR

Voltage = 1.0 V \pm 50 mV
Imax = 2.8 A
TRISE = 240 us

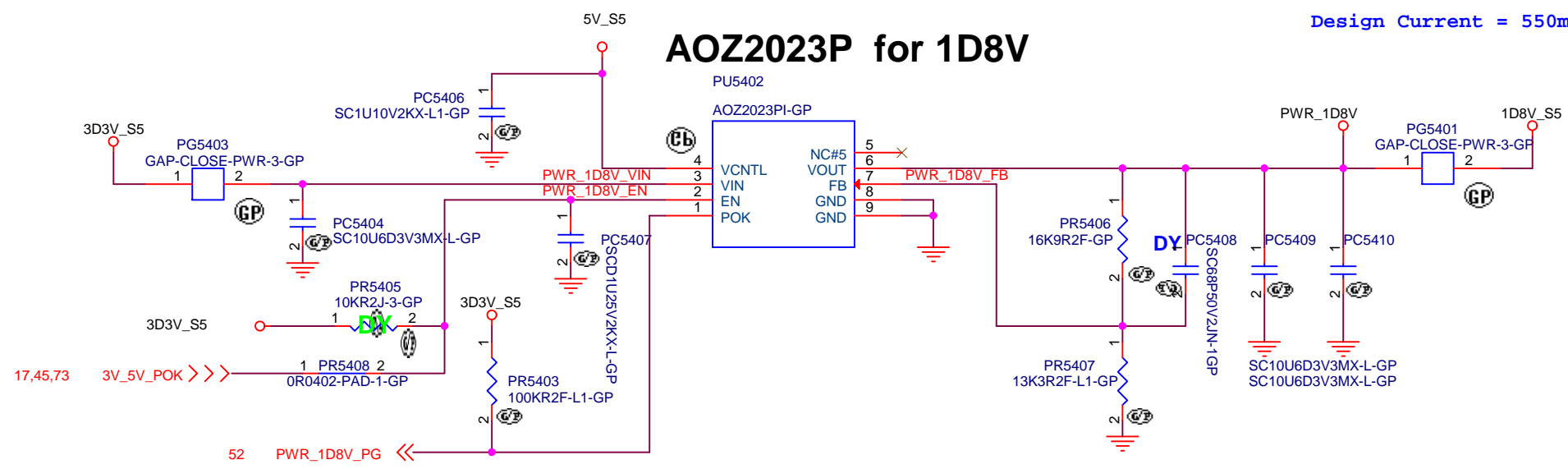


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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
TPS2296 VCCIO&VCCPRIM			
Size	Document Number	Rev	
A3	Unicorn_LV530_KBL_MB14	SA	
Date:	Friday, December 15, 2017	Sheet 53 of	105

Main Func = 1D8V



$$V_{out} = 0.8V * (R1 + R2) / R2$$

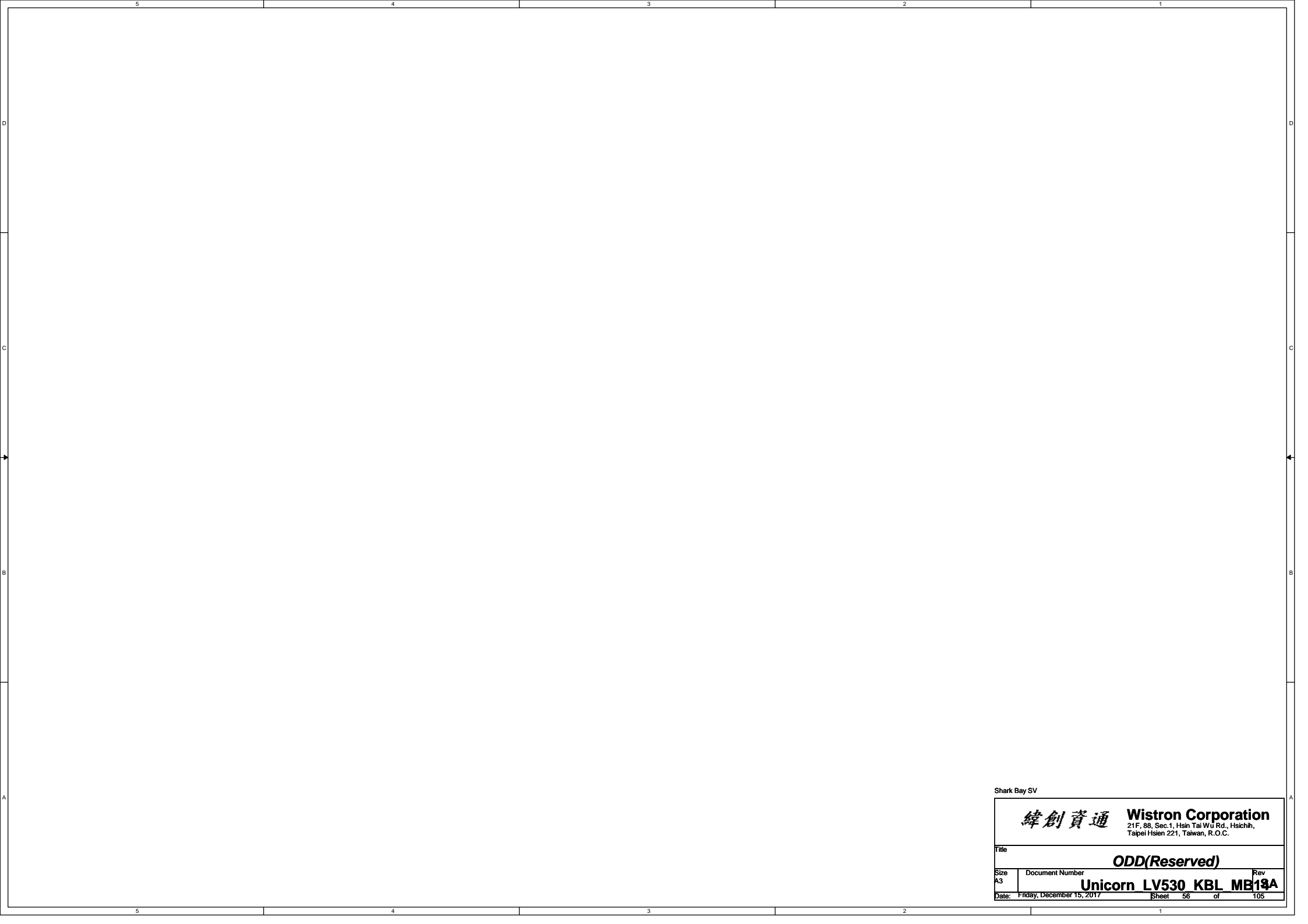
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.					
Title					
RT9025 1D8V					
Size	Document Number				Rev
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Date:	Friday, December 15, 2017		Sheet	54	of 105

need check pin define

need check pin define





Shark Bay SV

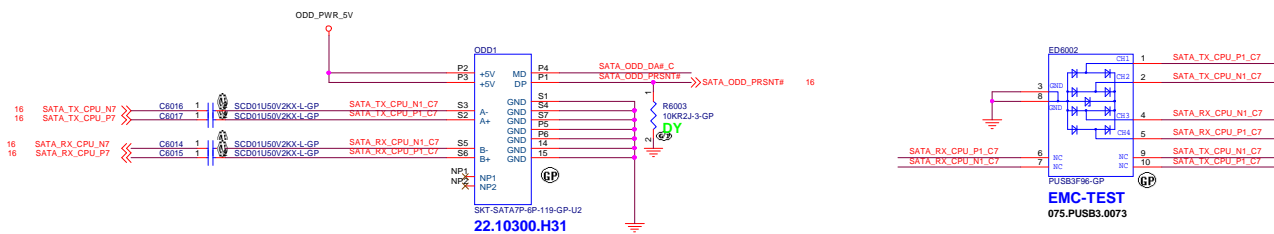
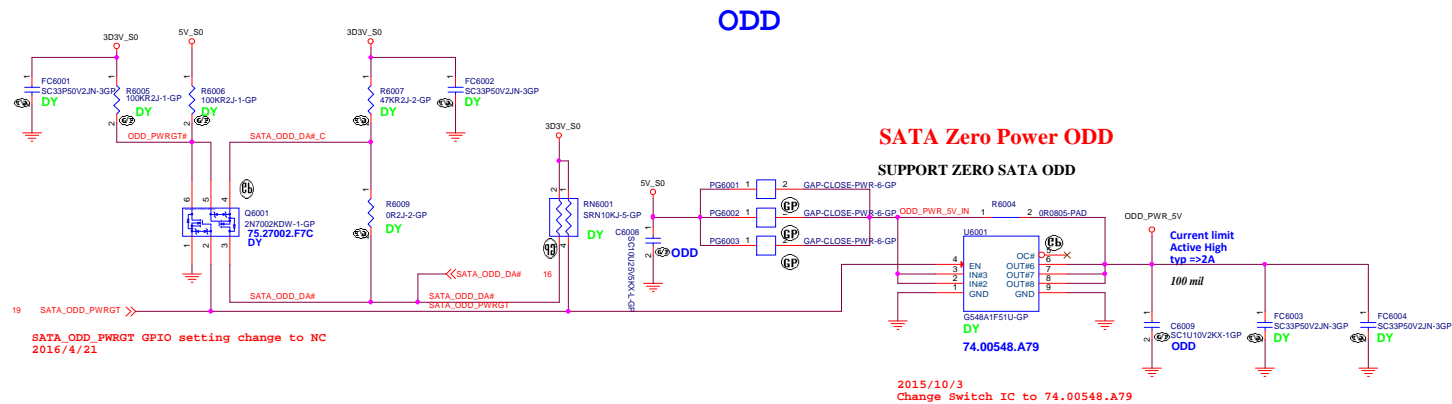
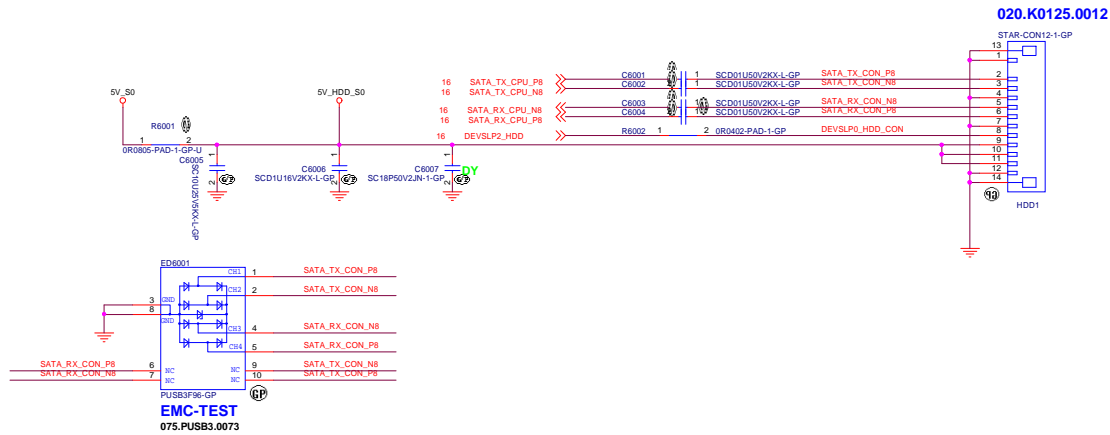
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
ODD(Reserved)			
Size	Document Number		Rev
A3	Unicorn LV530 KBL MB13A		13A
Date:	Friday, December 15, 2017	Sheet 56 of 105	

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BOM1

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
RESERVED		
Size	Document Number	Rev
A4	Unicorn LV530 KBL MB	1A
Date:	Friday, December 15, 2017	Sheet 59 of 105

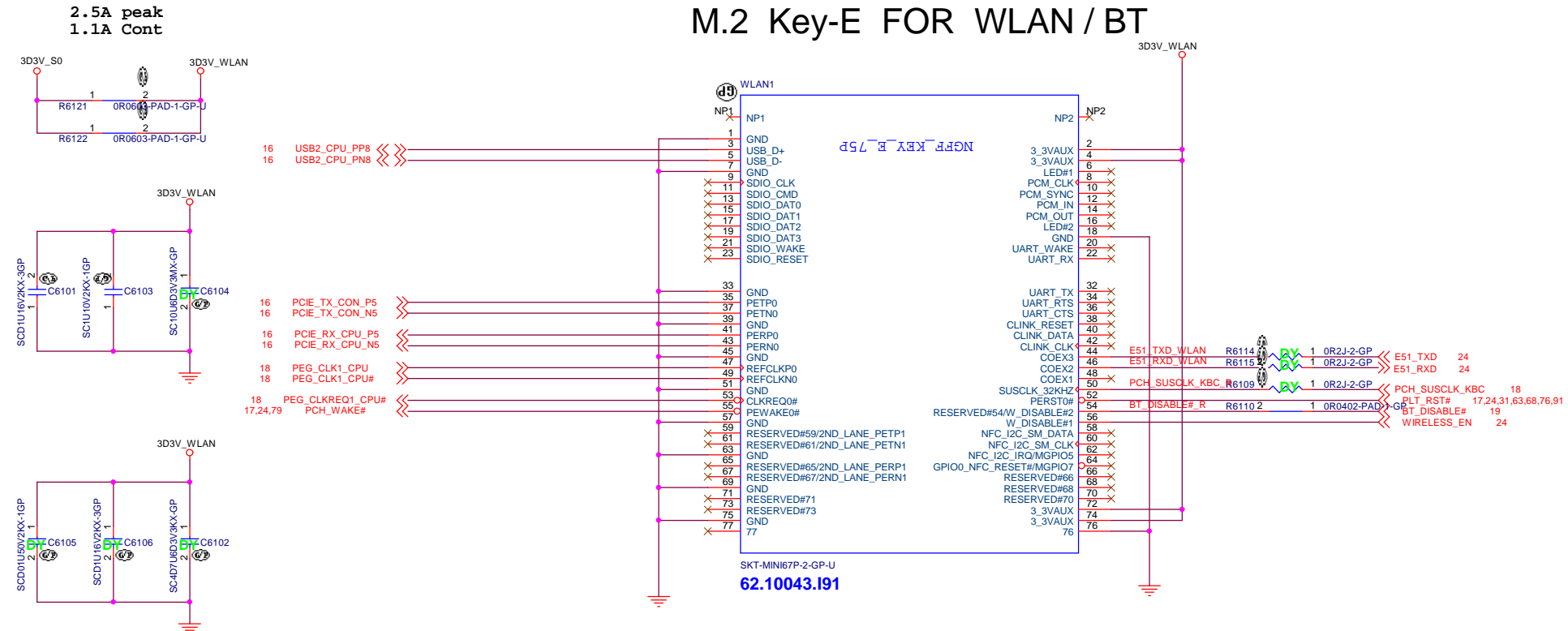
HDD 20170427
Cnchange pin define follow LV315ST(NC) but pn 1 different



BOM1

Main Func = WLAN

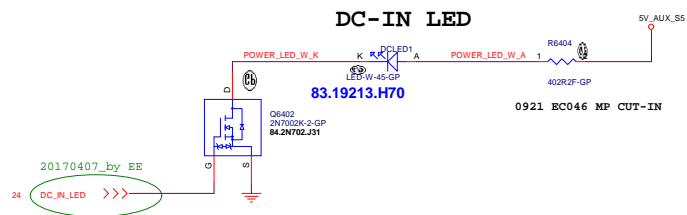
M.2 Key-E FOR WLAN / BT



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BOM1

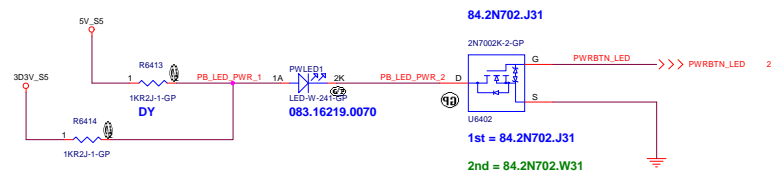
<div>緯創資通</div>		<div>Wistron Corporation</div>	
		<div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
<div>Title</div>			
<div>RESERVED</div>			
<div>Size</div>	<div>Document Number</div>		<div>Rev</div>
<div>A4</div>	<div>Unicorn LV530 KBL MB 6A</div>		<div>1A</div>
<div>Date: Friday, December 15, 2017</div>		<div>Sheet</div>	<div>62 of 105</div>



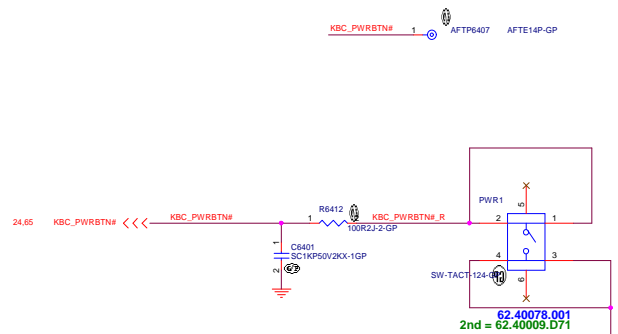
Test point



POWER BTN LED



KBC_PWRBTN#



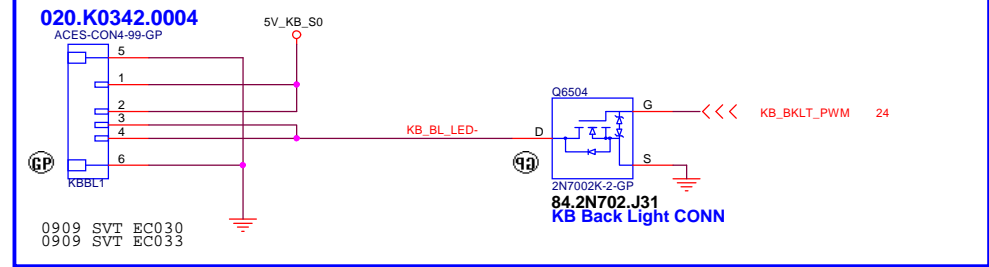
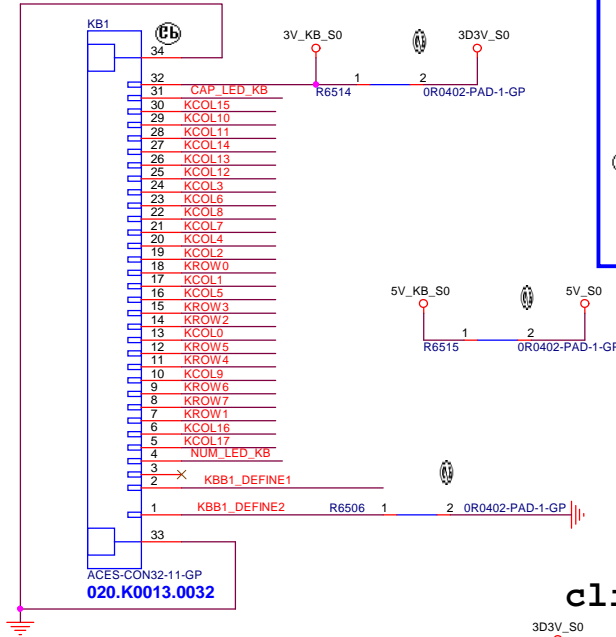
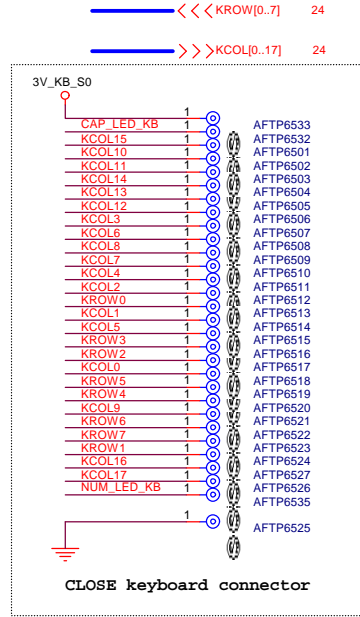
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緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
LED / POWER BUTTON			
Size	Document Number		Rev
A2	Unicorn LV530 KBL MB14		SA
Date	Friday, December 15, 2017	Sheet 64 of	105

SSID = Touch.Pad

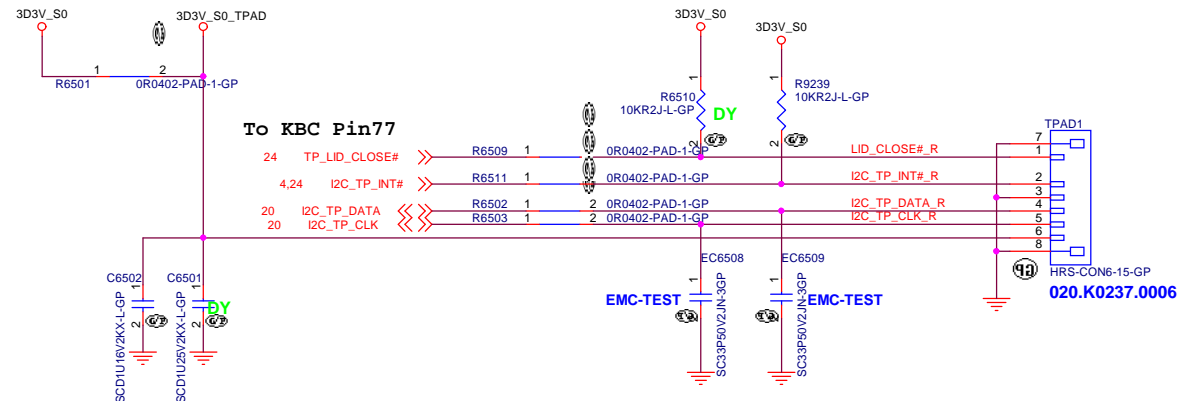
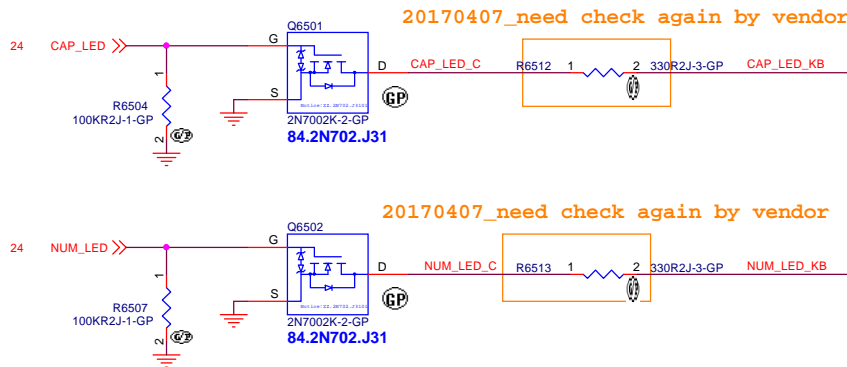
20170427_pin deifne check by Dennis

KB_LED

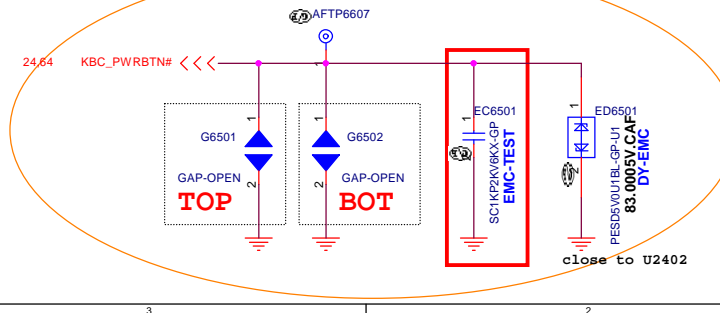


click pad

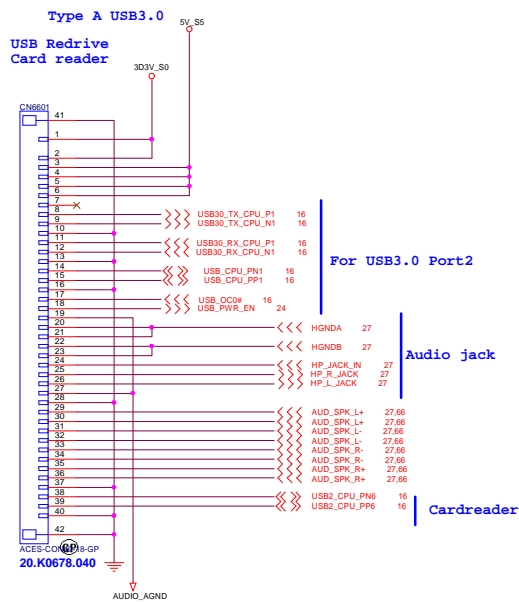
20170421
Cnhange pin define by Dennis



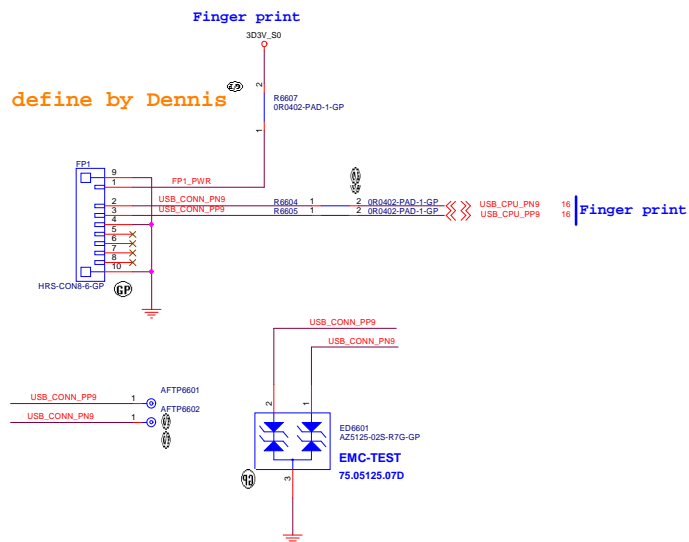
20170412_ WKS test by LB720



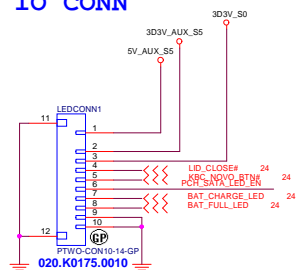
IO CONN



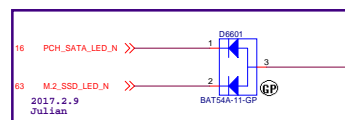
20170421
Change pin define by Dennis



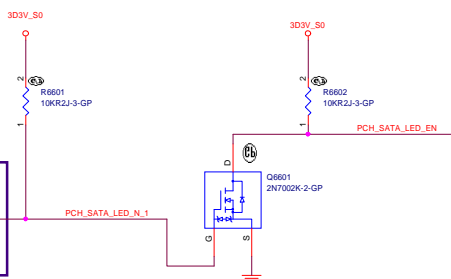
LED IO CONN



www.teknisi-indonesia.com



LOW:ENABLE, LED ON
HIGH:DISABLE,LED OFF



BOM1		緯創資通 Wistron Corporation 21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsuehshin, Taipei Hsien 221, Taiwan, R.O.C.	
File		LEDIO_IO BOARD CONN	
Size	Document Number	Rev	
A2	Unicorn LV530_KBL_MB14	SA	
Date:	Friday, December 16, 2017	Sheet	66 of 105

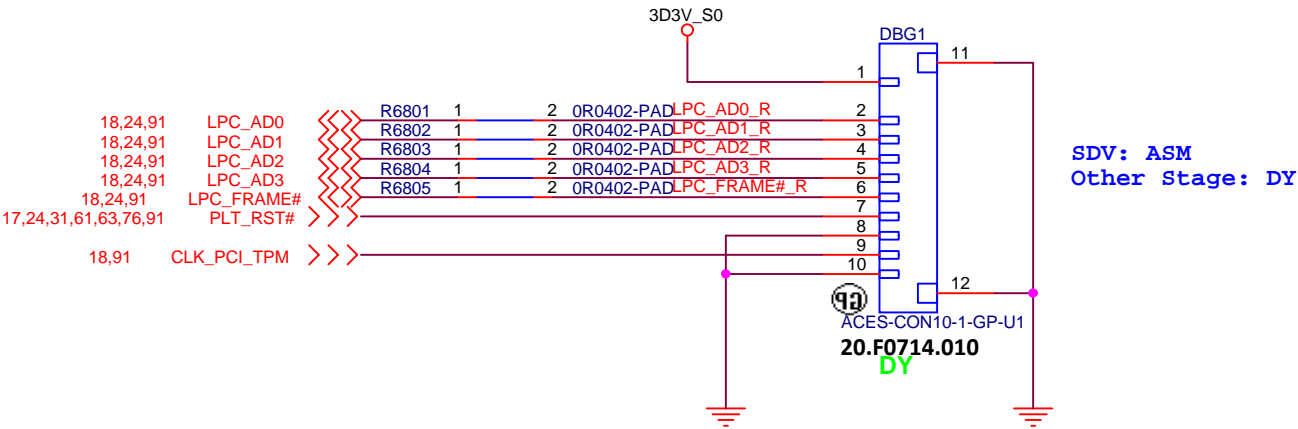
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BOM1

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
RESERVED		
Size	Document Number	Rev
A4	Unicorn LV530 KBL MB	1A
Date:	Friday, December 15, 2017	Sheet 67 of 105

Main Func = Debug

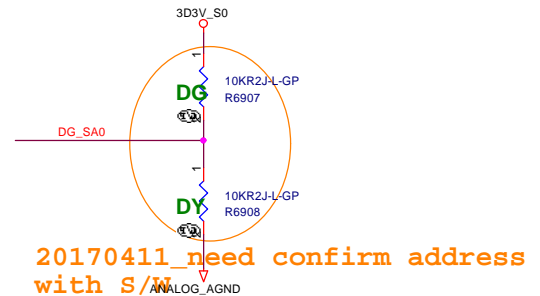
Debug Connector



BOM1

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
DEBUG CONN			
Size	Document Number	Rev	
A4	Unicorn LV530 KBL MB14	SA	
Date:	Friday, December 15, 2017	Sheet	68 of 105

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1st:ST/ LIS3DETR, 74.00003.BB0
(cannot be used, bit not enough)
2nd:KX124-1051, 074.01051.00B0
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BOM1

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
RESERVED		
Size	Document Number	Rev
A4	Unicorn LV530 KBL MB	1A
Date:	Friday, December 15, 2017	Sheet 70 of 105

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BOM1

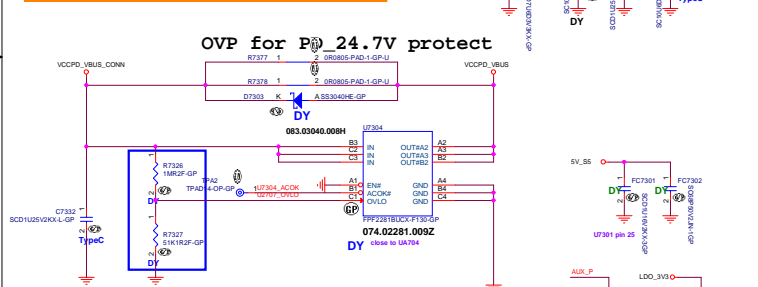
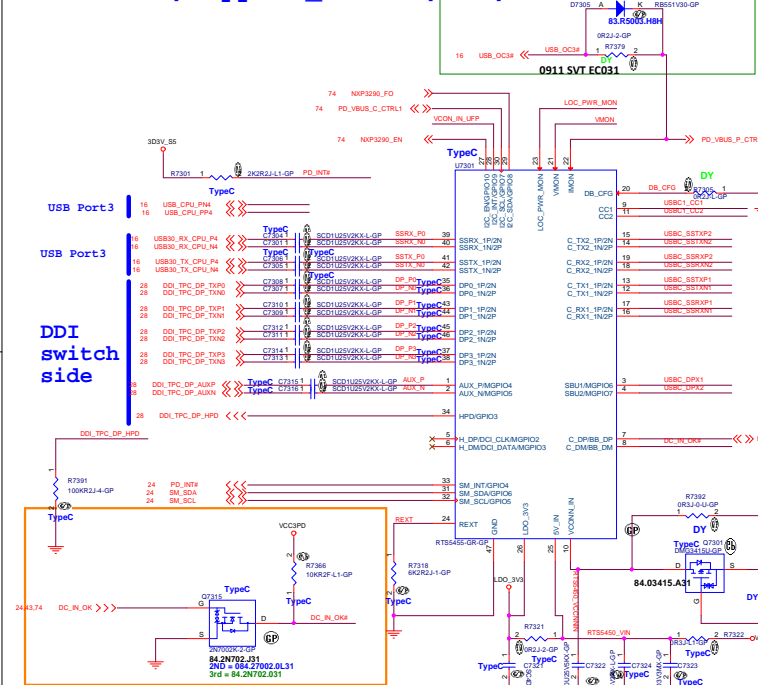
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
RESERVED		
Size	Document Number	Rev
A4	Unicorn LV530 KBL MB	1A
Date:	Friday, December 15, 2017	Sheet 71 of 105

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BOM1

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
RESERVED		
Size	Document Number	Rev
A4	Unicorn LV530 KBL MB	1A
Date:	Friday, December 15, 2017	Sheet 72 of 105

USB Port4, Type C_USB3.0, PD, DP 20170405, need check again TypeC

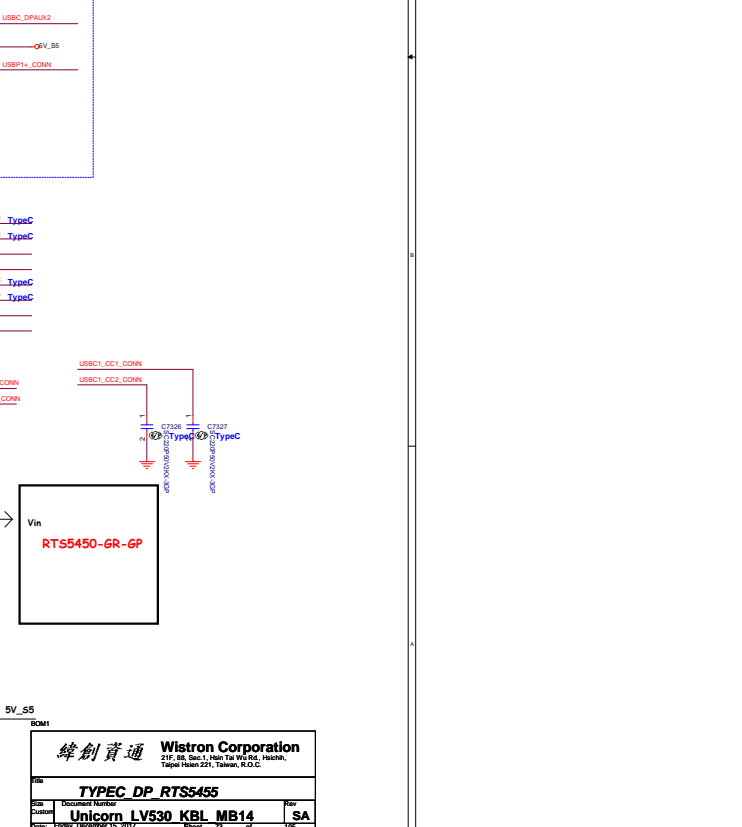
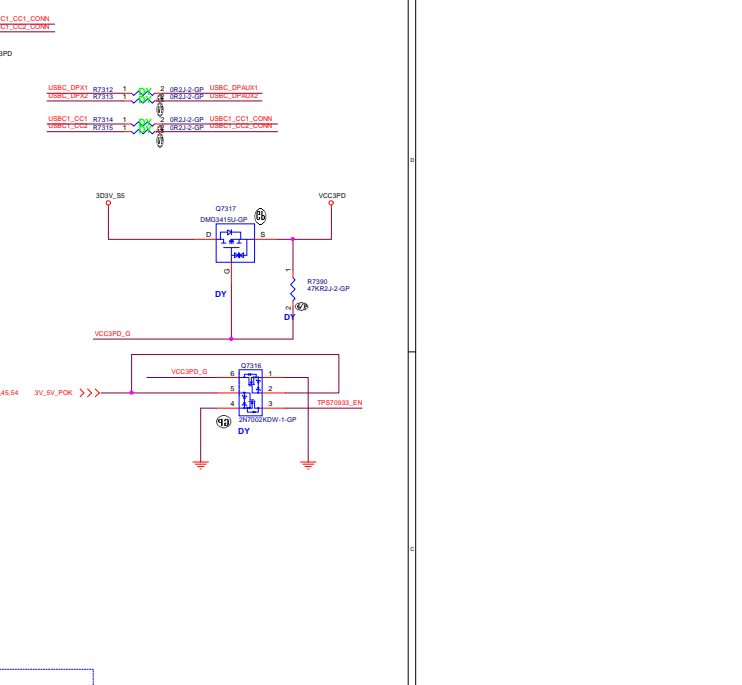
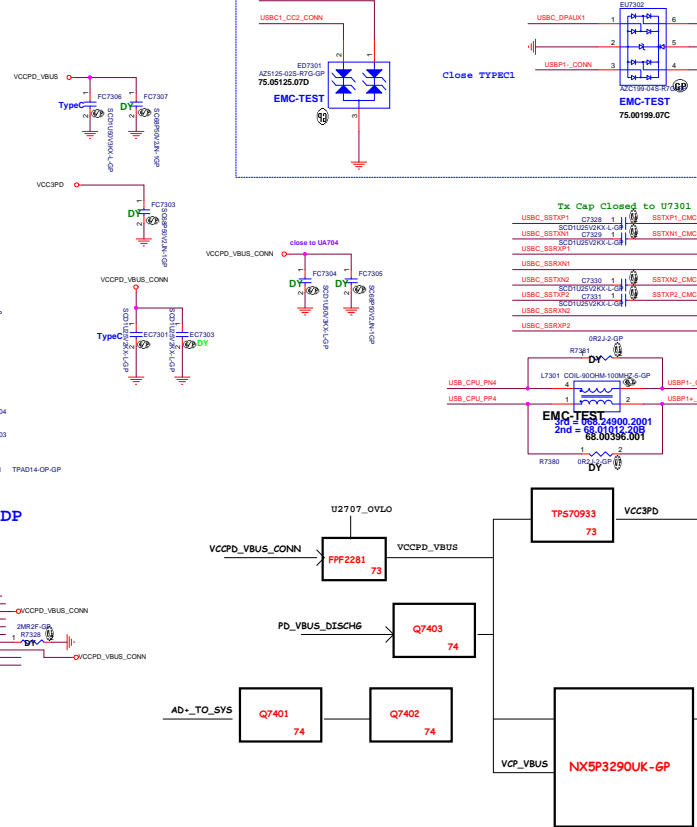
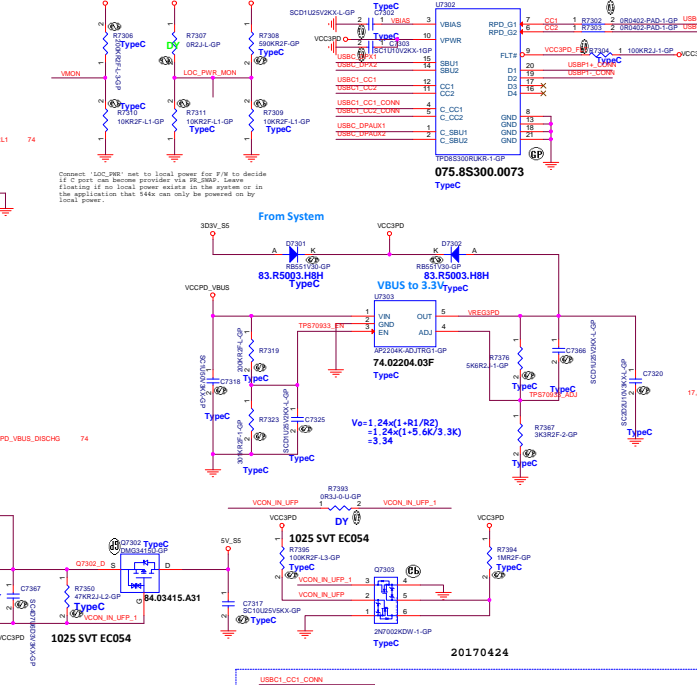
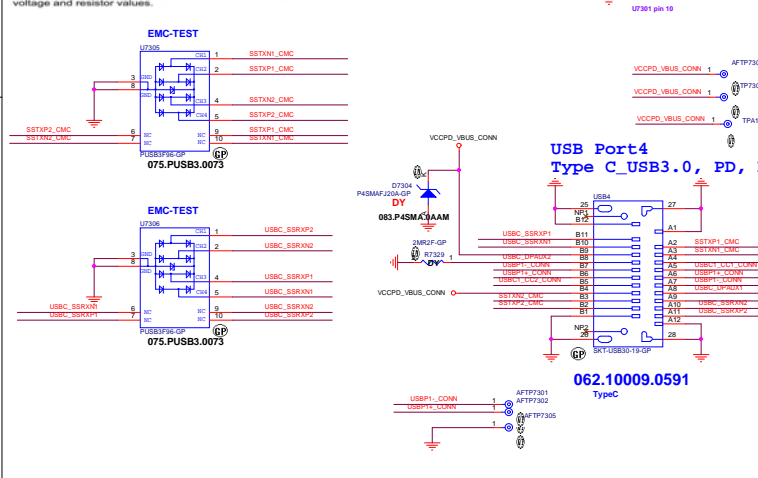


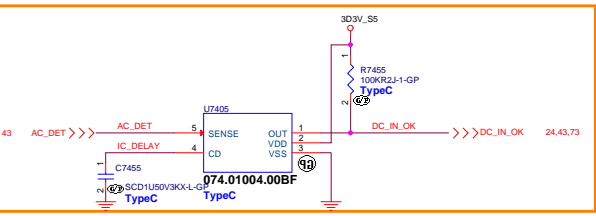
Over-Voltage Lockout (OVLO) Calculation

OVLO can be set externally and override default OVP. By connecting an external resistor-driver to the OVP pin, Equation (1) can produce the desired trip

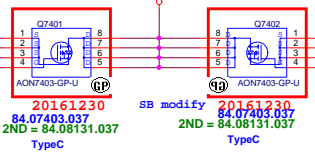
$$V_{IN_OVLO} = V_{OVLO_TH} \times [1 + R1/R2]$$

Recommended minimum R1 = 1 M Ω .

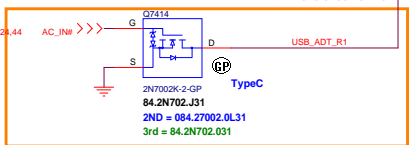




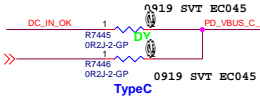
USB PD (Consumer: 20V 3.25A, Provider: 5V 2A)
To System



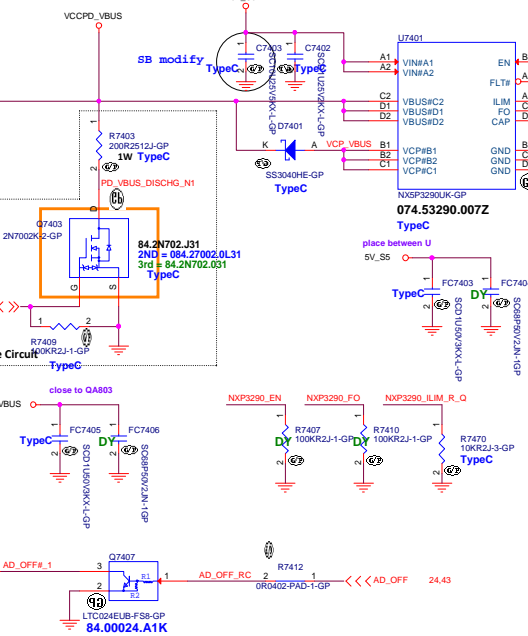
VBUS_C_CTRL = 0 (Consumer Path ON)
VBUS_C_CTRL = 1 (Consumer Path OFF)



Battery charger will turn off QA802 without any adapter in

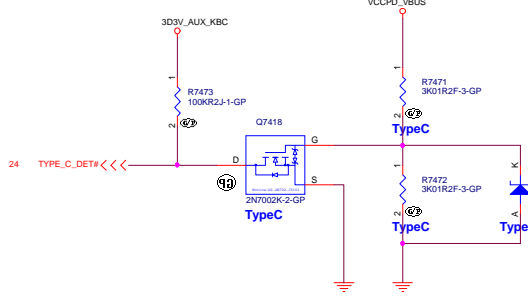


19V Power source type	Control Pin				PMOS Location	Status	Remark
	Net name	Status	Net name	Status			
Normal adapter Only	DC_IN_OK	High	PD_VBUS_C_CTRL1	High	Q7401	OFF	Control by DC_IN_OK
					Q7402	OFF	Control by PD_VBUS_C_CTRL1
					PU4302	ON	Control by DC_IN_OK or ACAV_IN
Type-C adapter Only	DC_IN_OK	Low	PD_VBUS_C_CTRL1	Low	Q7401	ON	Control by BGATE
					PU4302	OFF	
					PU4412	OFF	
Normal adapter + Type-C	DC_IN_OK	High	PD_VBUS_C_CTRL1	High	Q7401	OFF	
					Q7402	OFF	
					PU4302	ON	
Battery Only	DC_IN_OK	Low	PD_VBUS_C_CTRL1	High	Q7401	OFF	
					Q7402	OFF	
					PU4302	OFF	
					PU4412	ON	Battery to 19V_DCBATOUT



1. AC: 15W/ 3A, 系統功耗不足降
至4.5W/ 0.9A
2.DC: 4.5W/ 0.9A

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _{over current} I _{protection current}	V _{IN} = 4.75 ± 0.5 V, T _{amb} = +40 °C to +85 °C					
	See Figure 15					
	R _{DS(on)} = 140 mΩ		350	400	405	mA
	R _{DS(on)} = 100 mΩ		480	500	625	mA
	R _{DS(on)} = 33 mΩ		915	931	1137	mA
	R _{DS(on)} = 24.5 mΩ		1505	1670	1780	mA
I _{SD} = 18 mA	R _{DS(on)} = 20 mΩ		2024	2220	2584	mA
	R _{DS(on)} = 20 mΩ		2490	2640	2820	mA
	R _{DS(on)} = 18 mΩ		3190	3300	3531	mA
LIM limited to VIN			168	210	270	mA

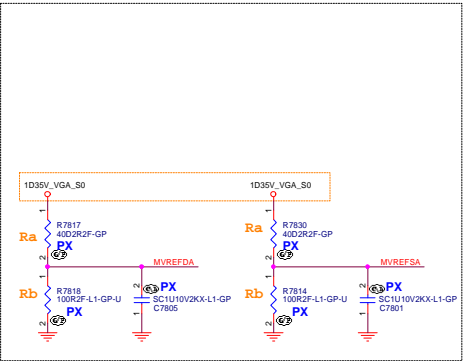


BOM1

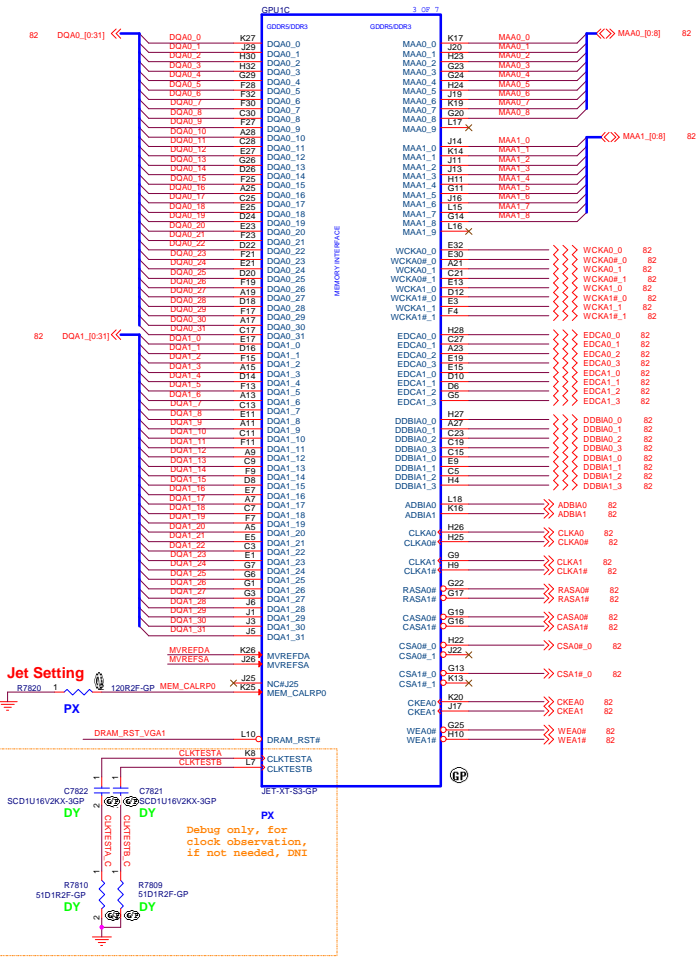
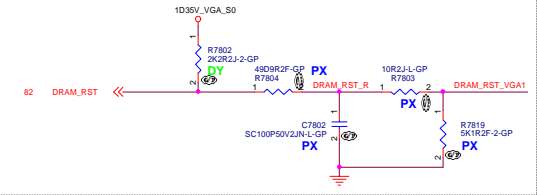
緯創資通 Wistron Corporation	
21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title TYPEC PD Controller	
Size Custom	Document Number Unicorm LV530_KBL_MB14
Date: 2018.05.15.2017	Rev SA



Please MVREF drivers and Caps close to ASIC



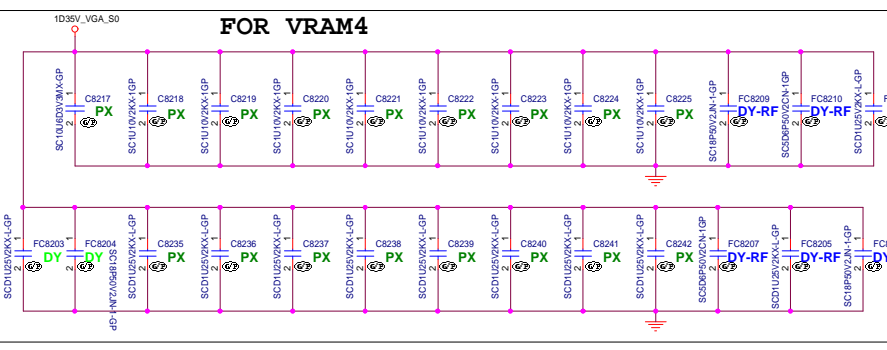
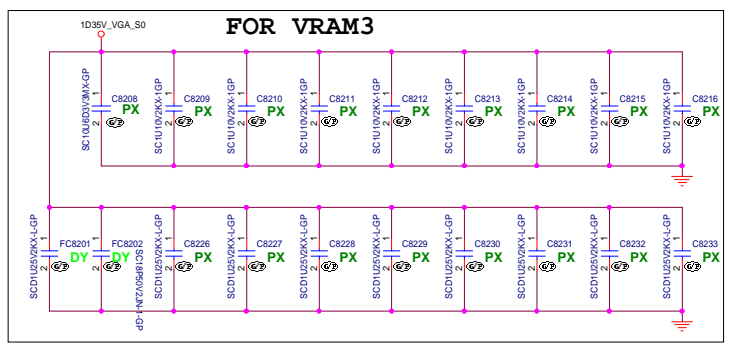
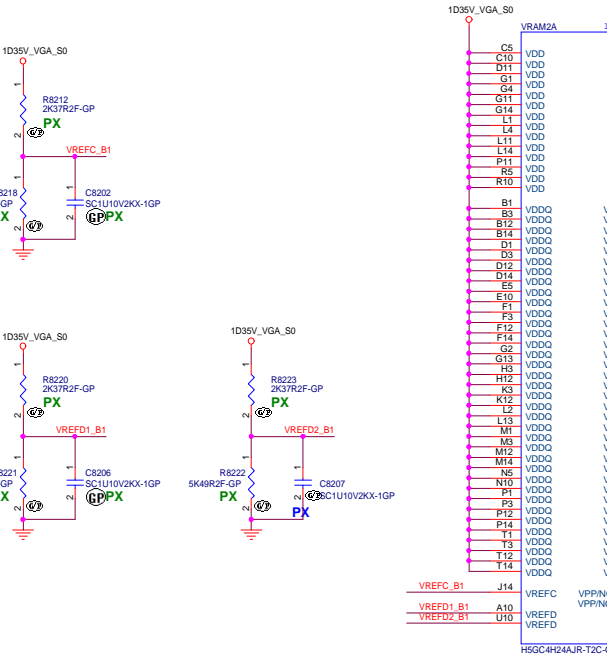
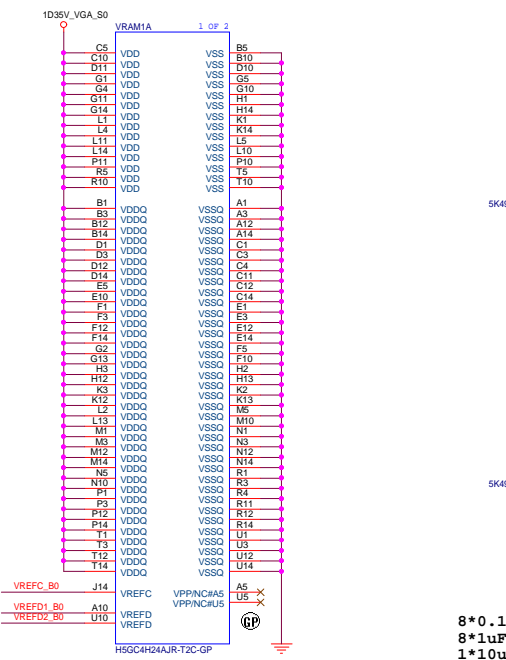
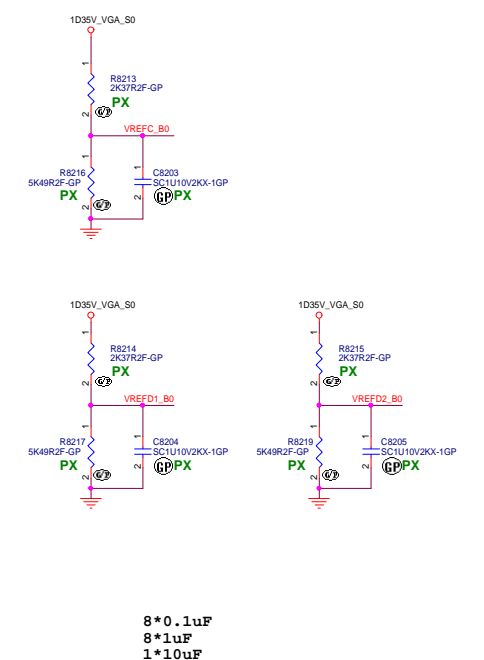
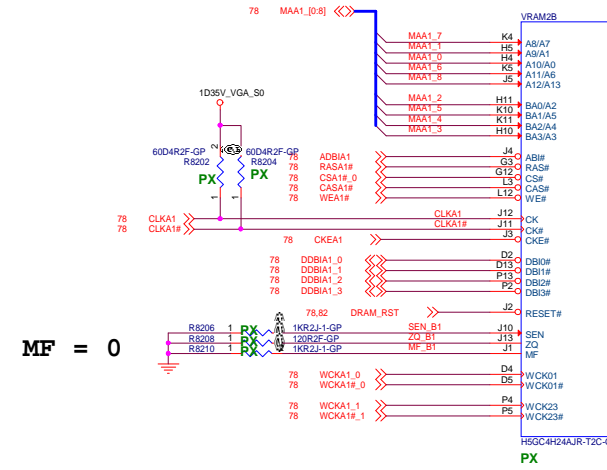
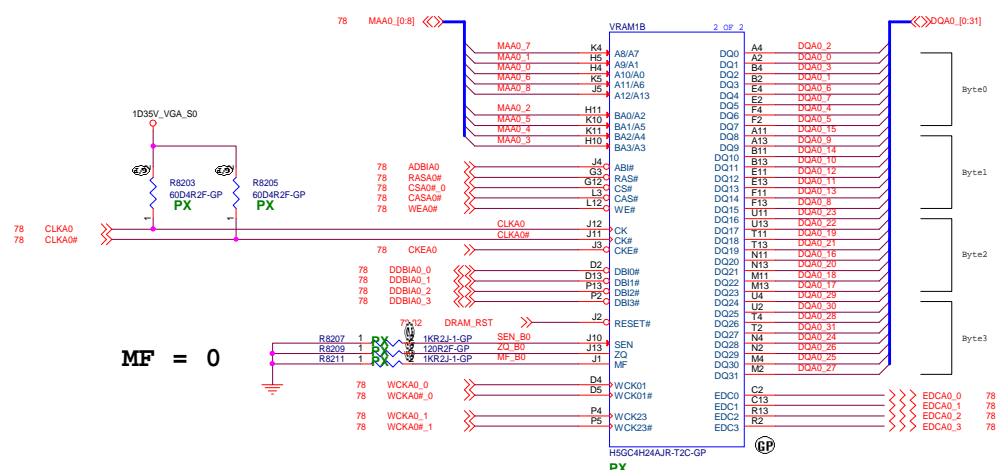
Place all these componets very close to GPU (within 25mm) and keep all componets close to each other
This basic topology should be used for DDR3/GDDR5



	5	4	3	2	1
D					
C					
B					
A					

BOM1

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Title			
GPU VRAM1.2 (1/4)			
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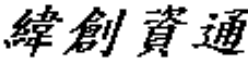
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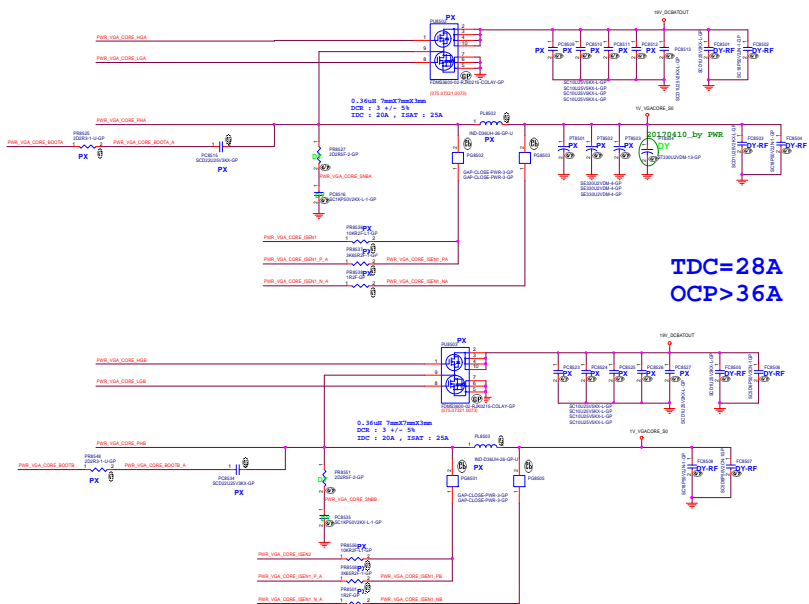
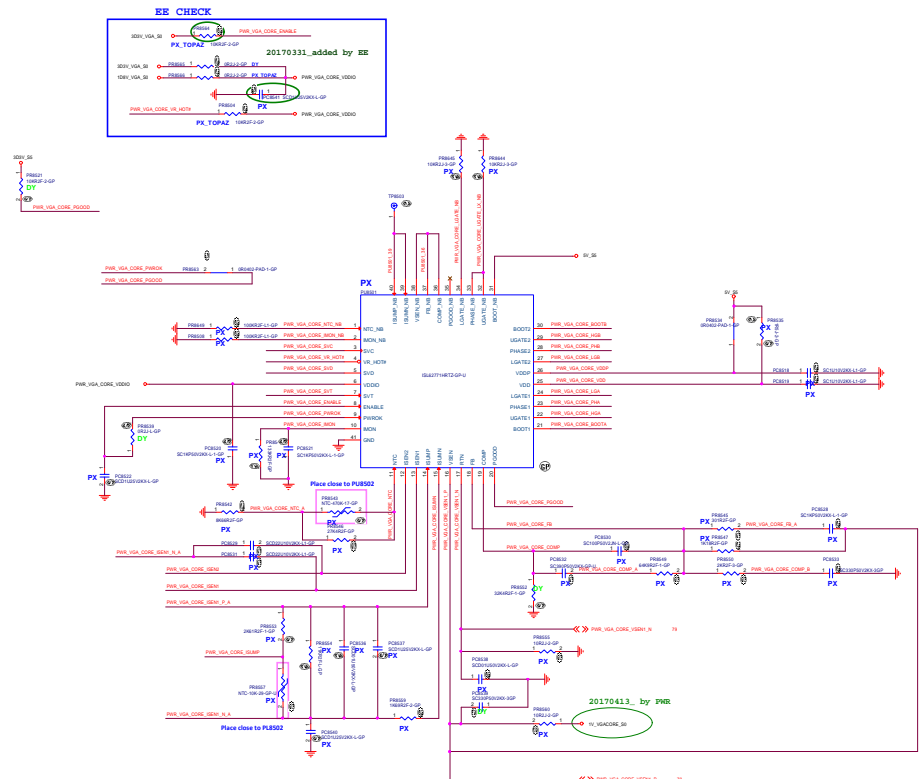
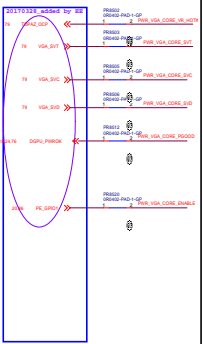
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BOM1

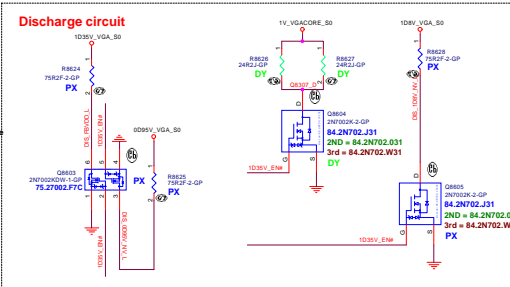
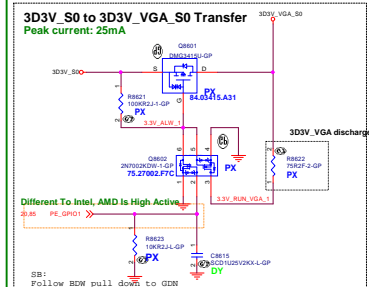
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GPU VRAM7,8 (4/4)			
Size A	Document Number		Rev
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EE CHECK



TDC=28A
OCP>36A

20151106 need Add MOS to Control 1D35V_EN# IN SB version



GPU PWR Sequencing
3D3V_VGAS0

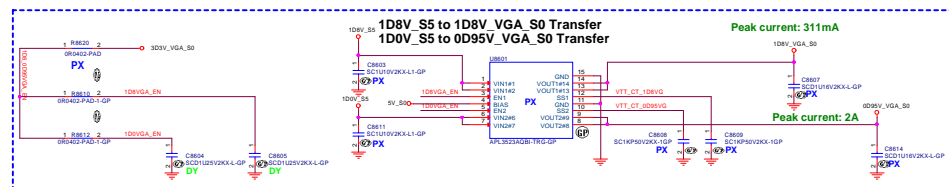
=> 0D95V VGA S0/1D8V VGA S0

=> 1D35V VGA S0

All the ASIC supplies must reach their respective nominal voltages within **20ms** of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50mV/us.

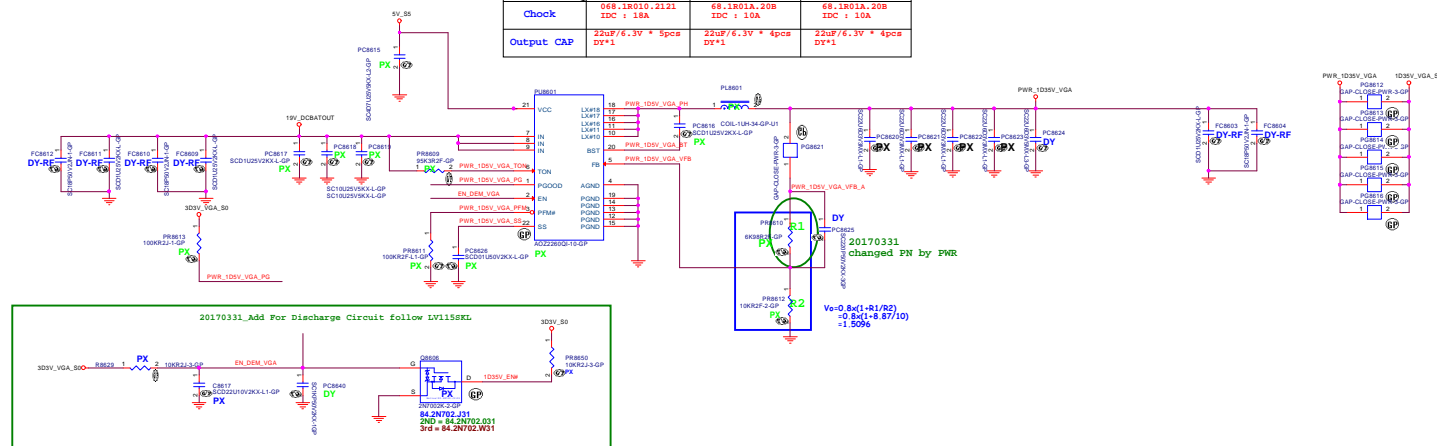
It is recommended that the 3.3V rail ramp up first.

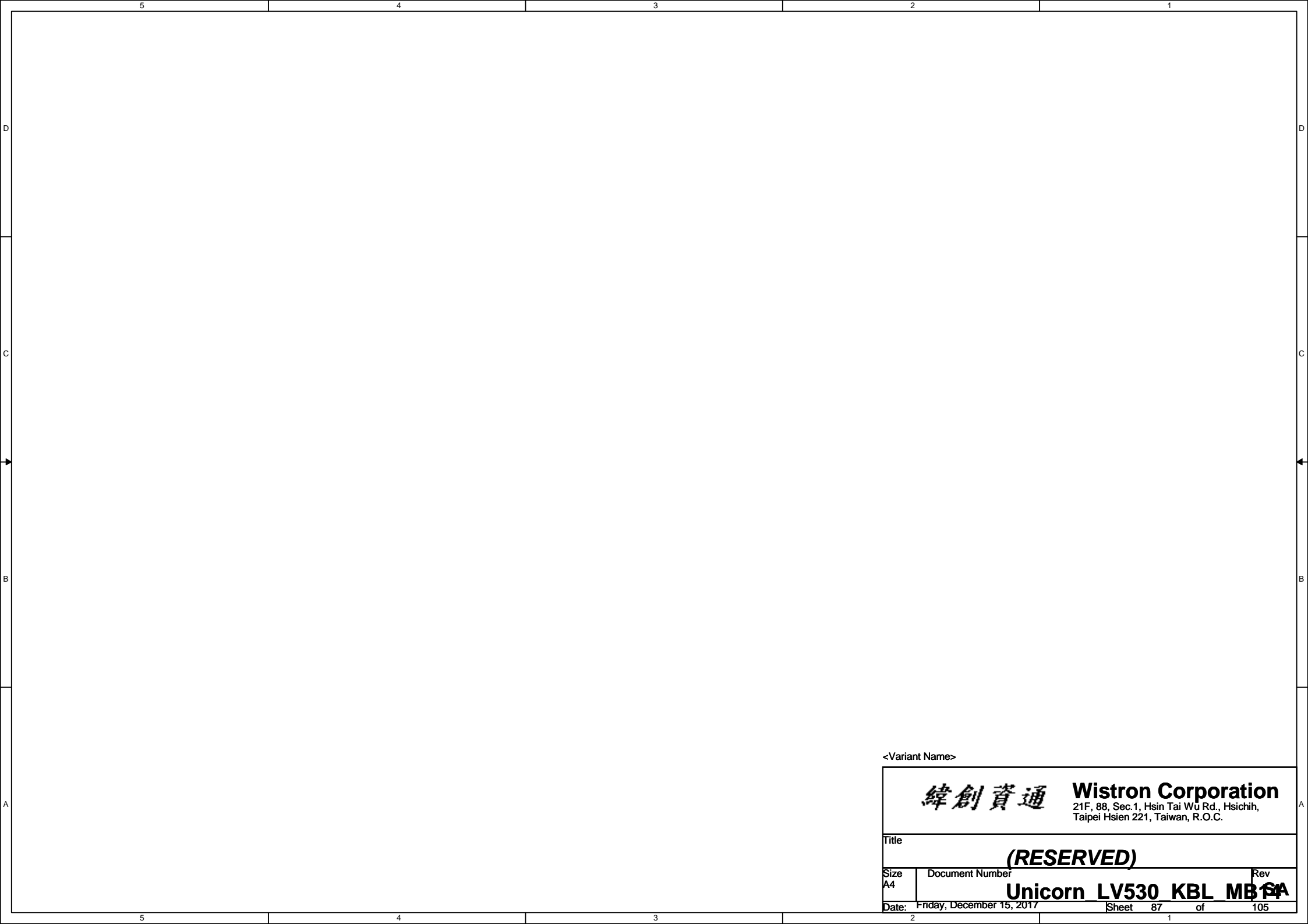
It is recommended that the 0.95V rail reach at least 90% of its normal value no later than 2ms from the start of VDDC ramping up.



EE need to confirm 20170208
EE confirm 20170413

IC COM	A0Z2262(10A)	A0Z2261(8A)	A0Z2260(6A)
Check	06B.1R010.2121 IDC : 18A	68.1R01A.20B IDC : 10A	68.1R01A.20B IDC : 10A
Output CAP	22uF/6.3V * 5pcs DY*1	22uF/6.3V * 4pcs DY*1	22uF/6.3V * 4pcs DY*1





<Variant Name>

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Document Number

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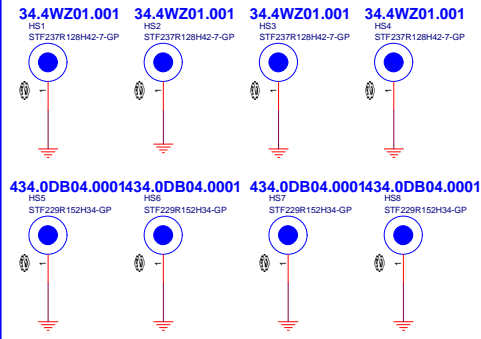
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EMI Clip

EMI Clip

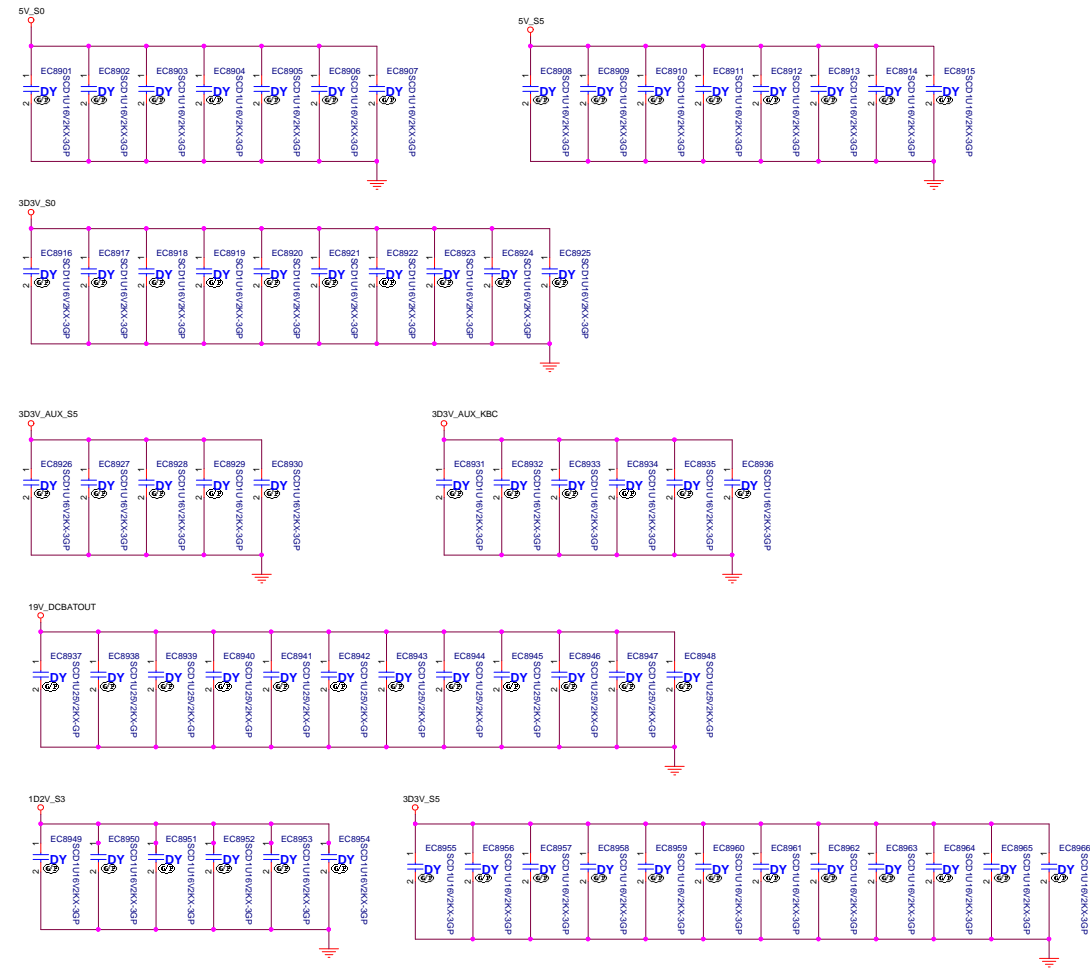
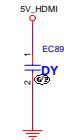
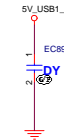
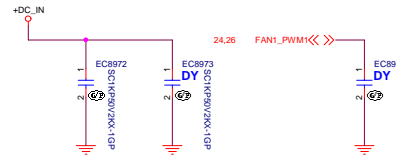
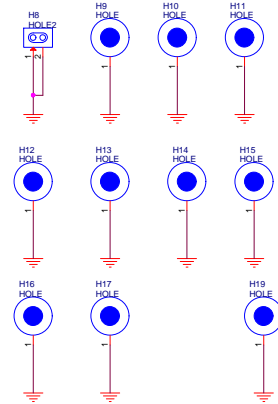
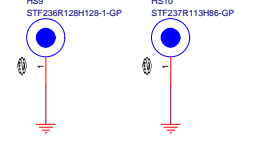
34.4GD01.101 will change to 434.0DB04.0001 by ME request
Waiting for symbol



ZZ.00PAD.EX1 ZZ.00PAD.EJ1 ZZ.00PAD.FN1



34.4LO45.001 434.07K0E.0001



BOM1

緯創資通 Wistron Corporation
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Taipai Hsien 221, Taiwan, R.O.C.

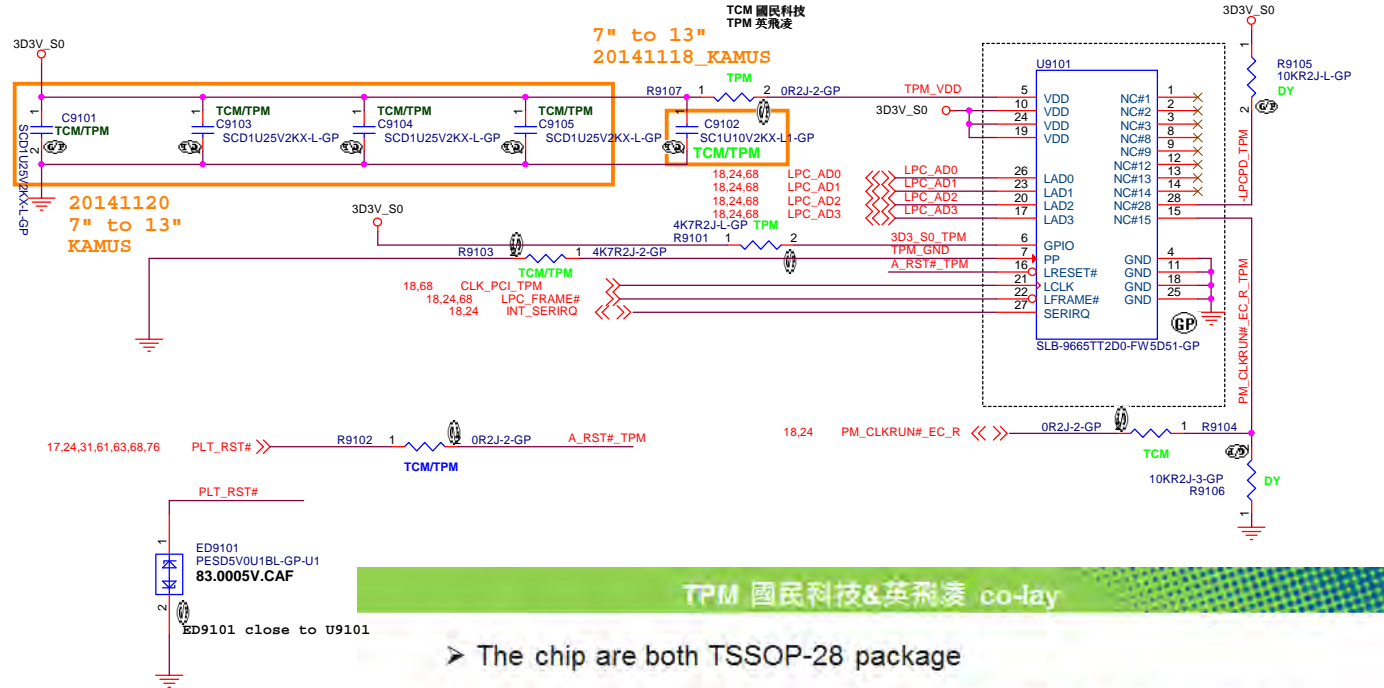
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Priority, 12/26/2008 15, 2017
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UNUSED PARTS/EMI Capacitors
Unicorn LV530 KBL MB64

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BOM1

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➤ The chip are both TSSOP-28 package

Pin define	國民	英飛凌	Remark	Pin define	國民	英飛凌	Remark
1	NC	NC		15	CLRUN#	NC	0ohm
2	NC	NC		16	LRESET#	LRESET#	
3	NC	NC		17	LAD3	LAD3	
4	GND	GND		18	GND	GND	
5	NC	VDD	0ohm	19	VDD	VDD	
6	NC	GPIO	0ohm	20	LAD2	LAD2	
7	NC	PP	0ohm	21	LCLK	LCLK	33ohm for 國民
8	NC	NC		22	LFRAME#	LFRAME#	
9	NC	NC		23	LAD1	LAD1	
10	VDD	VDD		24	VDD	VDD	
11	GND	GND		25	GND	GND	
12	NC	NC		26	LAD0	LAD0	
13	NC	NC		27	SIRQ	SERIRQ	
14	NC	NC		28	LPCLD#	NC	0ohm

Czrrizo/Carrizo-Lite + Exo Pro

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091_TPM

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A3

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D

D

C

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B

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A

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Rev

Unicorn LV530 KBL MB14

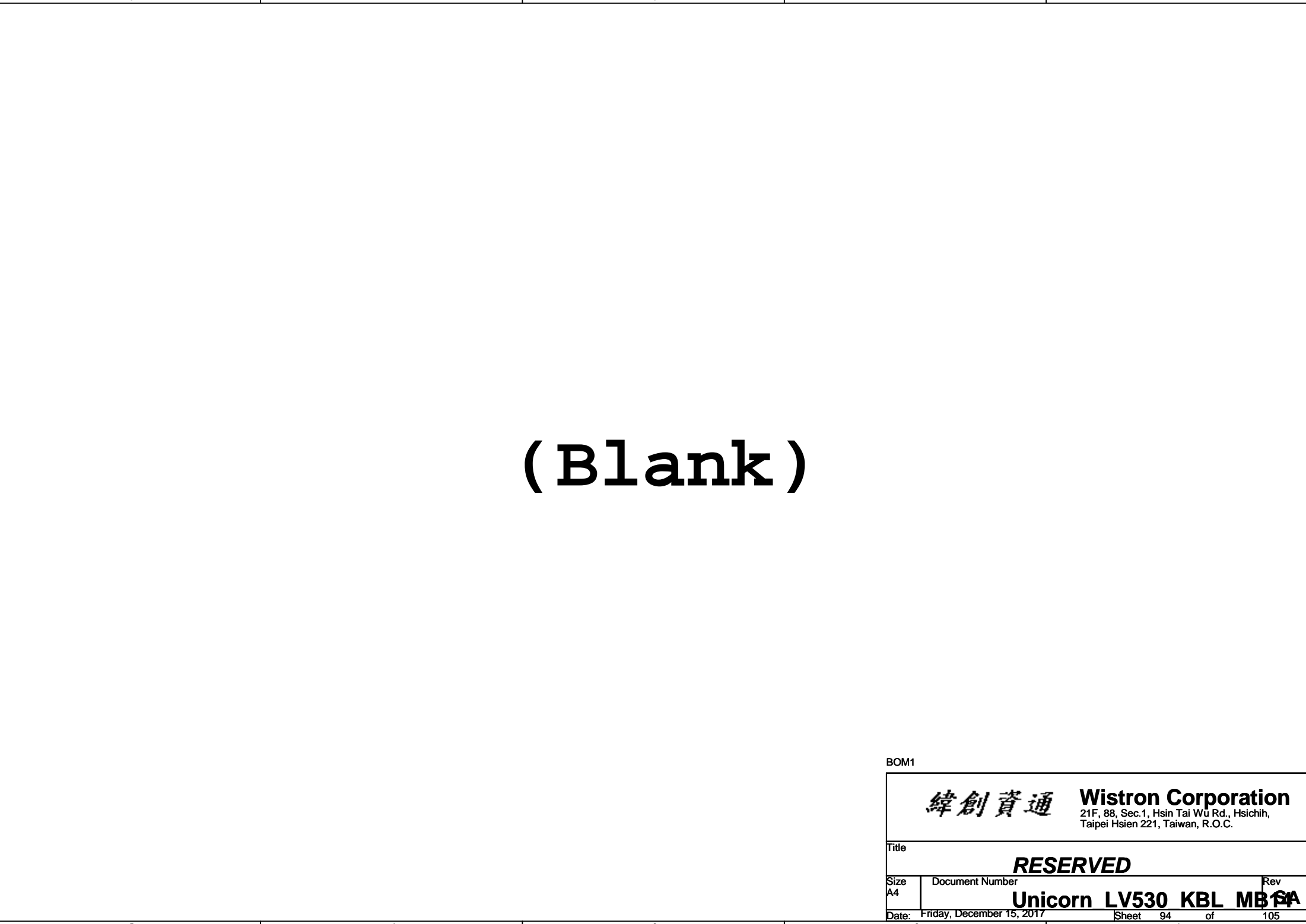
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BOM1

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BOM1

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BOM1

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<Variant Name>

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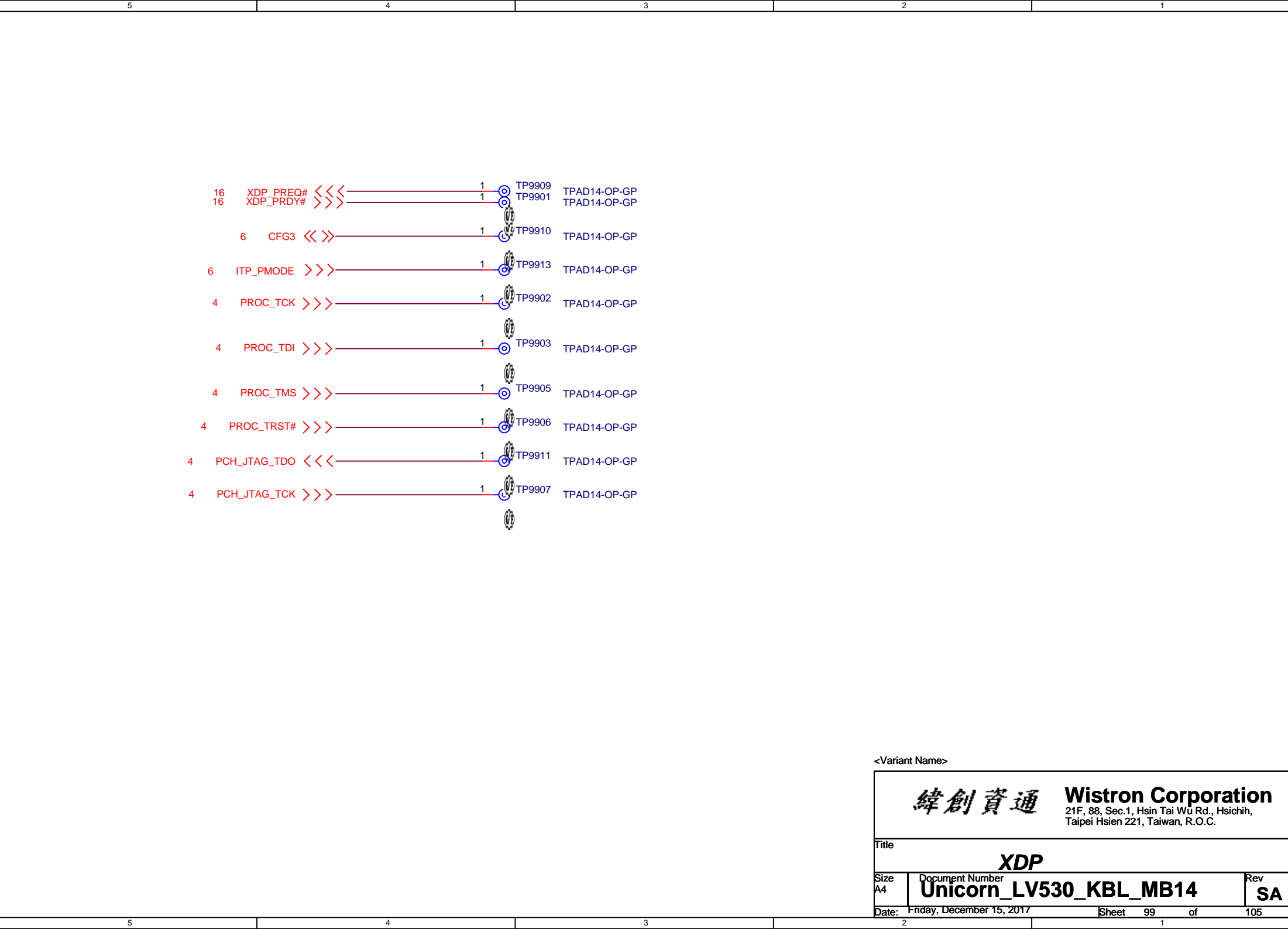
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XDP		
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D				D
C				C
B				B
A				A

<Variant Name>

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Title

TABLE OF CONTENT

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D				D
C				C
B				B
A				A

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CHANGE HISTORY

Size A4	Document Number Unicorn LV530 KBL MB 1A	Rev 1A
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Figure 41-5. KBL R U Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform] (Sheet 1 of 2)

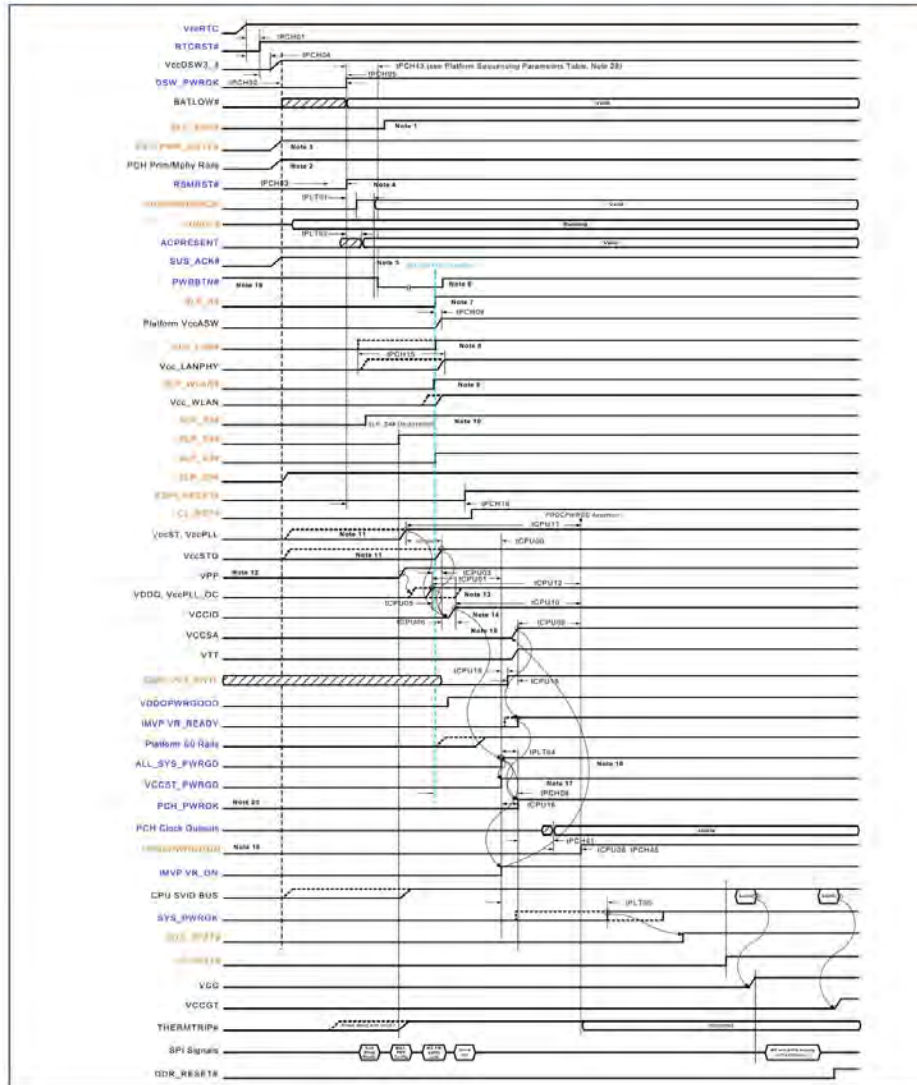


Figure 41-5. KBL R U Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform] (Sheet 2 of 2)

Notes:

1. SLP_SUS# is ignored in Non-DSx systems
2. Refer Rail-to-Rail Power Sequencing Requirement section for details on PCH prime rail-to-rail power and power down dependencies
3. EXT_PWR_GATE# has been de-featured. This pin, in native mode, will never be driven low
4. For a non-DeepSx system DSW_PWRGD and RSMRST# go high at the same time (connected on board)
5. For a non-DeepSx system SUS_ACK# will rise with prime voltage rail powering the VCCPGPPA power pin due to weak internal pull-up.
6. Minimum duration of PWRBTN# assertion = 16mS. PWRBTN# can assert before or after RSMRST#
7. On first exit from G3, SLP_A# de-asserts with SLP_S3# de-assertion
8. High for WoL=1, Low for WoL=0. SLP_LAN# may rise before, but no later than SLP_A#
9. On first exit from G3, SLP_WLAN# de-asserts with SLP_S3# de-assertion
10. Delay between SLP_S5#, SLP_S4#, and SLP_S3# exaggerated for drawing purposes. If the system EC is driving these signals in ESP1 mode if the, the minimum delay between SLP_S3#, SLP_S4#, and SLP_S5# is not guaranteed
11. VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization. VCCST, VCCSTG may also remain powered in S4 and S5 for debug purposes. Refer to Chapter 42, "Platform Debug and Test Hooks" for more details. VCCSTG should only ramp up equal to or after VCCST.
12. Only required with LPDDR3 and DDR4 memory configurations
13. VDDQ must ramp after VPP on DDR4 and LPDDR3 based systems, thus VDDQ may ramp up after SLP_S3# de-assertion due to VR ramp timing and configuration
14. VCCIO, VCCSA must ramp after VccST, VccSTG, and VDDQ have completed their ramps. If VCCSTG and VCCIO supplies are merged together as a single supply, VCCSA must ramp after VccST, VCCSTG/VCCIO, and VDDQ have completed their ramps
15. IMVP_VR_ON is recommended to be triggered by ALL_SYS_PWRGD in order to help minimize boot latency.
16. ALL_SYS_PWRGD is assumed to logically AND together the pwrgood signals for the major system power rails
17. VCCST_PWRGD can assert before or equal to PCH_PWRGD, but must never lag it. It is recommended that both VCCST_PWRGD and PCH_PWRGD include ALL_SYS_PWRGD in their generation. This ensures during failure events, both signals de-assert at the same time
18. PROCPWRGD is used only for power sequence debug and is not required to be connected to anything on the platform.
19. When "Power Button" is the trigger for wake or sleep event for the system
20. The Platform should ensure that PCH_PWRGD does not glitch when RSMRST# is de-asserted

Additional Notes:

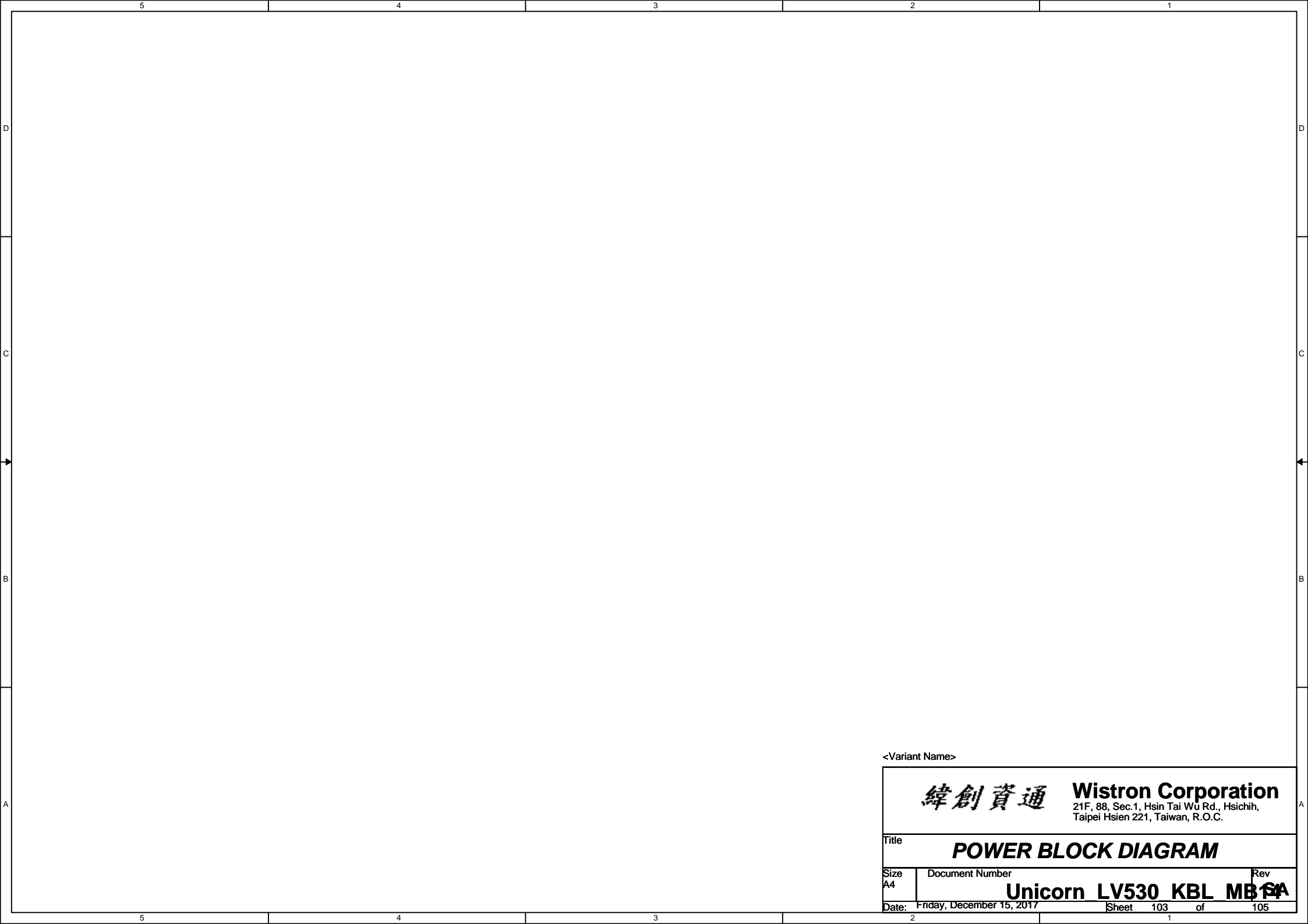
The state of the SLP_A# and SUSPWRDNACK signals are used by the EC to determine if PCH requires the suspend-well to stay powered.

• SUSPWRDNACK

- Platform not supporting M3 - EC must keep SUS Rails powered ON if: SUSPWRDNACK is de-asserted **OR** System state is S3. Else, EC has an option to do whatever it wants with the SUS Rails
- Platform supporting M3 - EC must keep SUS Rails powered ON if: SUSPWRDNACK is de-asserted **OR** System state is S3 **OR** SLP_A# is de-asserted **OR** it is the first 200ms after SUS Rails power has been applied. Else, EC has an option to do whatever it wants with the SUS Rails

- Primary rails and Deep Sx Rails should **never** be active while VccRTC rail is inactive.

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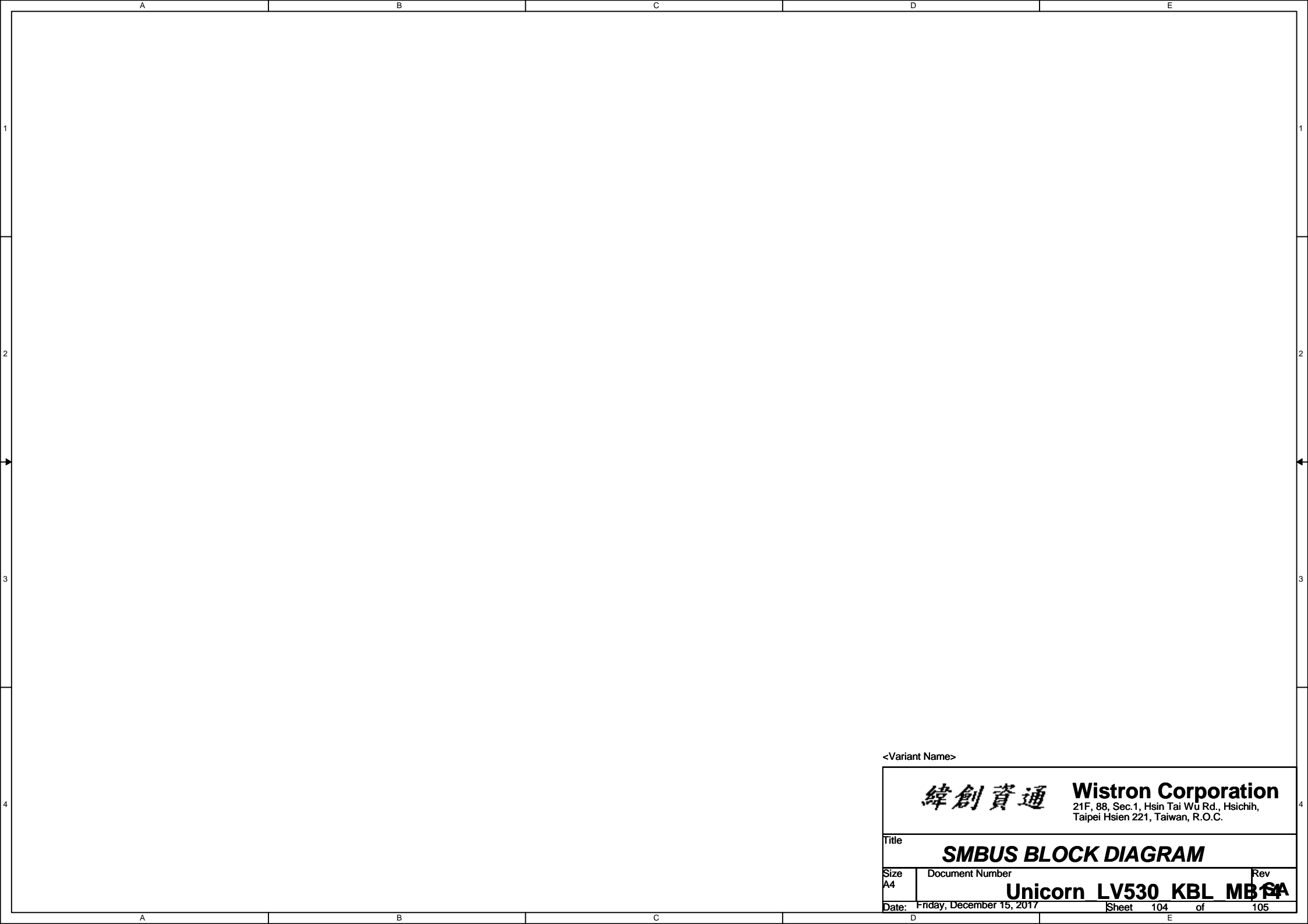
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POWER BLOCK DIAGRAM

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Title

SMBUS BLOCK DIAGRAM

Size
A4

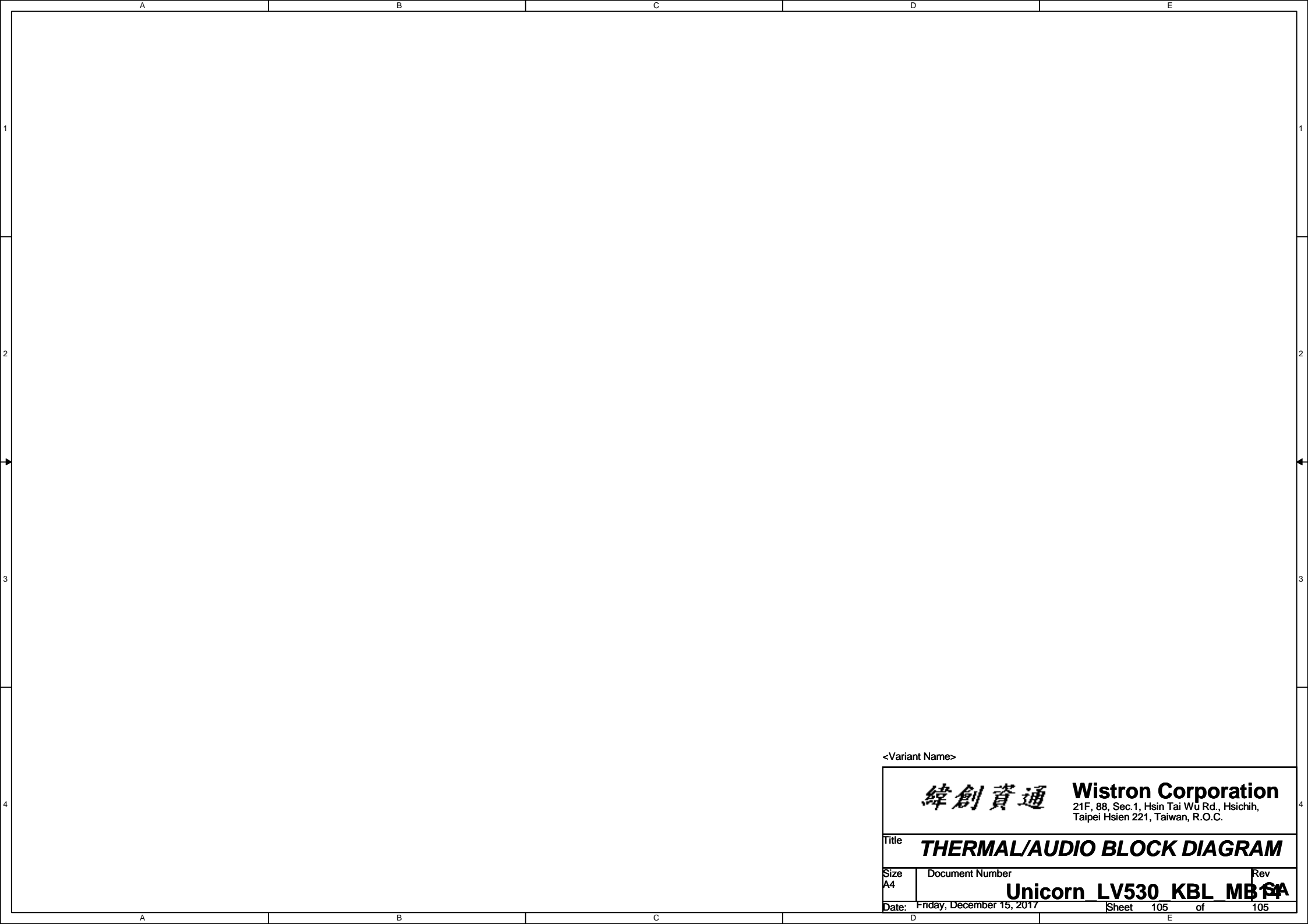
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Title **THERMAL/AUDIO BLOCK DIAGRAM**

Size
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