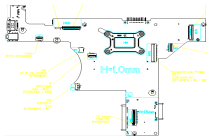
R05 UMA BLOCK DIAGRAM

PCB STACK UP

8L UMA

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : SVCC
- LAYER 5 : IN2
- LAYER 6 : IN3
- LAYER 7 : GND
- LAYER 8 : BOT



R05-HR MB PCB (rev B)

Label

Label

DDRIII-SODIMM0 H=4.0mm PAGE 17

DDRIII-SODIMM1 H=4.0mm PAGE 18

DDRIII 1333 MT/s

DDRIII 1333 MT/s

CPU
Sandy Bridge 35W
BGA 1023 SV
PAGE 4~8

FAN & THERMAL
SMSC1422
PG 34

- +VCHGR PAGE 38
- +3.3V_ALW/+5V_ALW PAGE 39
- +1.5V_SUS/+0.75V_DDR_VTT PAGE 40
- +VCCSA_CORE PAGE 41
- +1.05V_PCH/+1.8V_RUN PAGE 42
- +VCC_CORE/+VCC_GFX_CORE PAGE 43

FDI LINK 2.7GT /s

DMI LINK 5GT /s

Mobile Intel Series 6 Chipset

PCH

HM67
Couger Point

FCBGA 989
25 mm X 25 mm

PAGE 9~15

SINGLE CHANNEL LVDS → **LCD CONN** PAGE 20

HDMI Bus → **HDMI CONN** PAGE 21

DISPLAY PORT C → **Mini DP CONN** PAGE 19

SATA -HDD PAGE 27 — SATA0 600MB /S

SATA -ODD PAGE 27 — SATA1 300MB /S

Camera PAGE 20

USB2.0 PAGE 16

USB2.0

USB2.0

CardReader SD/MS/MMC PAGE 36

IO Board

WLAN/BT PAGE 23

PCI-E

LAN/RJ45 Atheros AR8152 PAGE 29

25MHz

USB3.0 Controller PAGE 25

USB3.0 Ports x2 PAGE 26

RJ45 CONN PAGE 29

IO Board

IHDA

Keyboard Conn. PAGE 32

Touch Pad PAGE 32

LPC

KBC ITE 8518 PAGE 30

PWM FAN PAGE 34

SPI ROM 4Mbit PAGE 31

SPI

SPI ROM 32Mbit PAGE 31

25MHz

32.768KHz

Audio Codec CX20671 PAGE 28

IO Board

Speaker PAGE 28

Audio Combo Jack X1 PAGE 28

Quanta Computer Inc.

PROJECT : R05

Size	Document Number	Rev
	BLOCK DIAGRAM	2A

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power / State					
S0					
S1					
S3					
S4/S5 AC					
S4/S5 DC Only					
AC/DC No Exist					

Quanta Computer Inc.

PROJECT : R05

Size	Document Number	Rev
	Power Rails	2A

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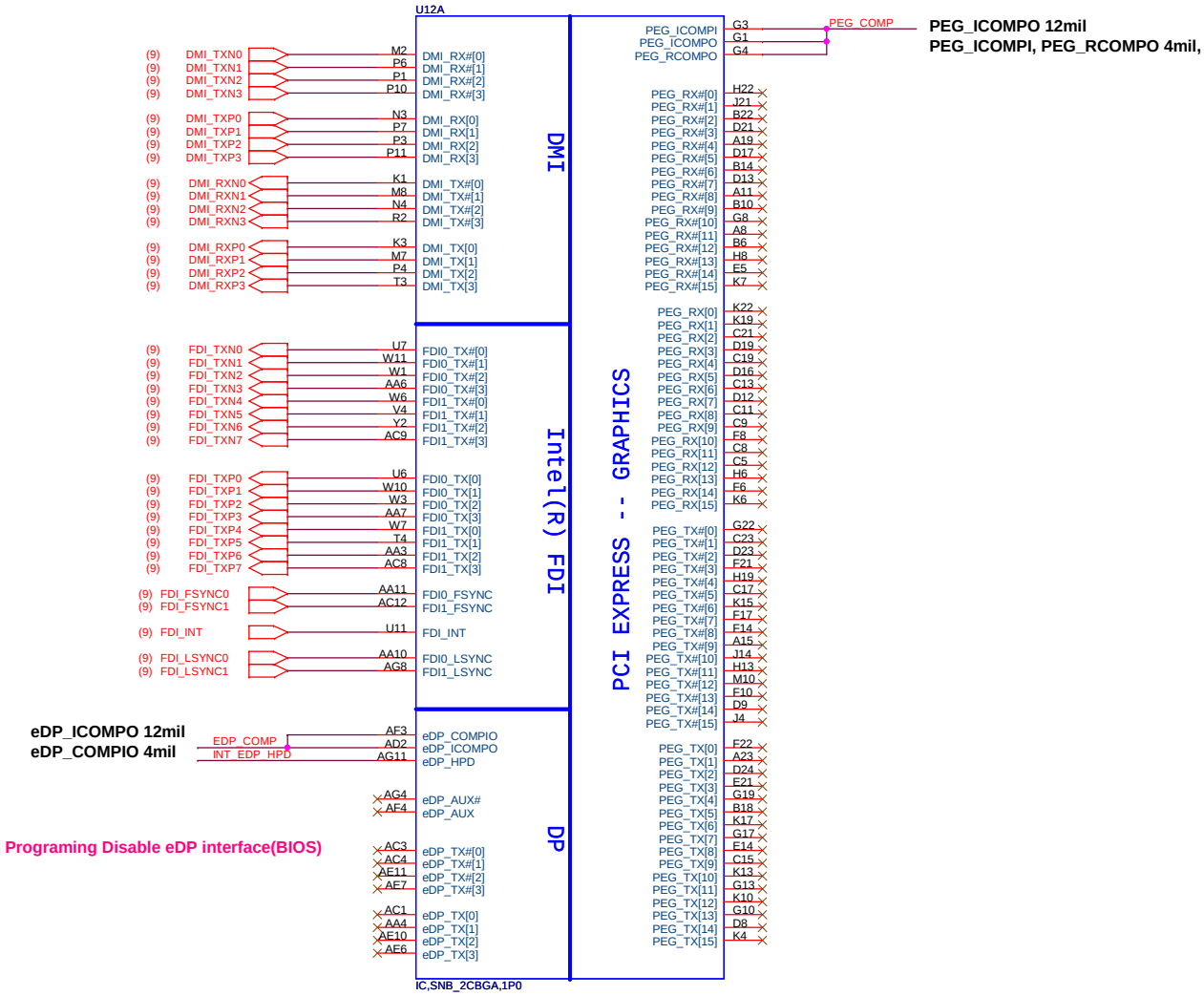
Quanta Computer Inc.

PROJECT : R05

Size	Document Number	Rev
	CLOCK GEN (9LRS3197)	2A

Date: Wednesday, June 22, 2011 Sheet 3 of 51

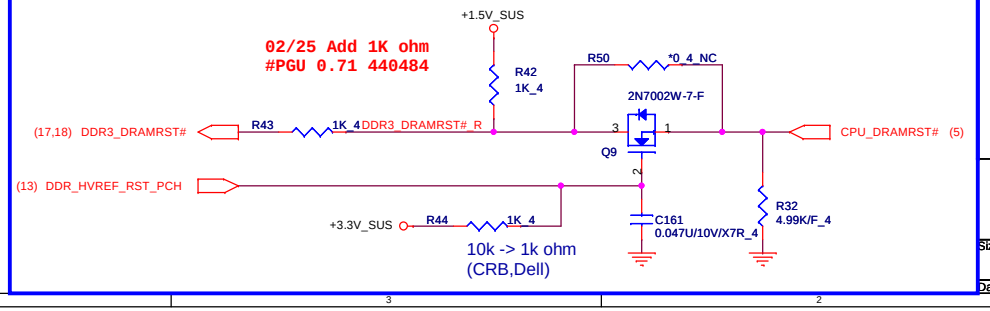
Sandy Bridge Processor (DMI,PEG,FDI)



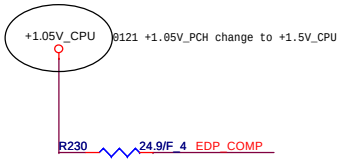
PEG_ICOMPO 12mil
PEG_ICOMPI, PEG_RCOMPO 4mil,

eDP_ICOMPO 12mil
eDP_COMPIO 4mil

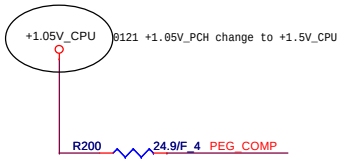
Programing Disable eDP interface(BIOS)



DP & PEG Compensation



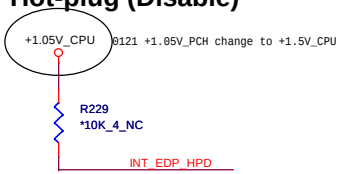
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms



PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms

PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

eDP Hot-plug (Disable)



CAD Note: Place PU resistor within 2 inches of CPU

HPD PU/PD resistor values based on CRB and different to DG

Quanta Computer Inc.
PROJECT : R05

Size	Document Number	Rev
	Sandy Bridge 1/5	2A
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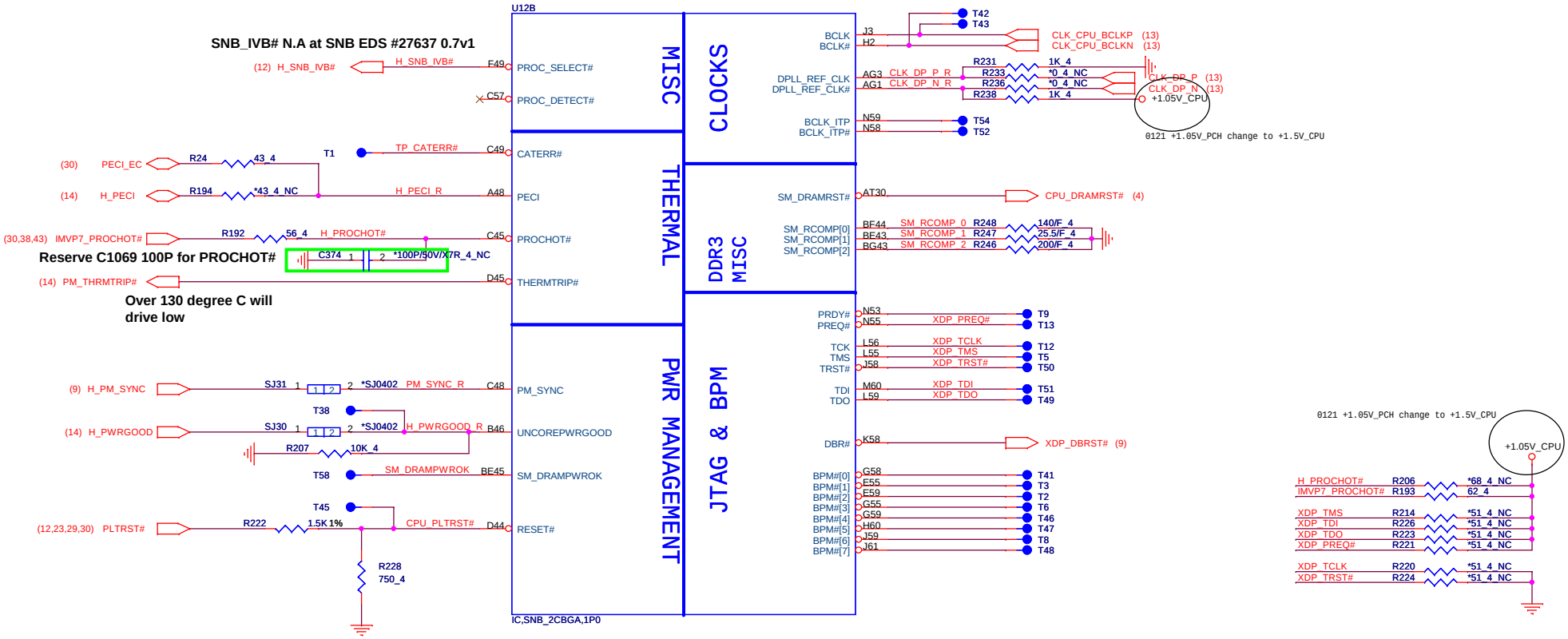
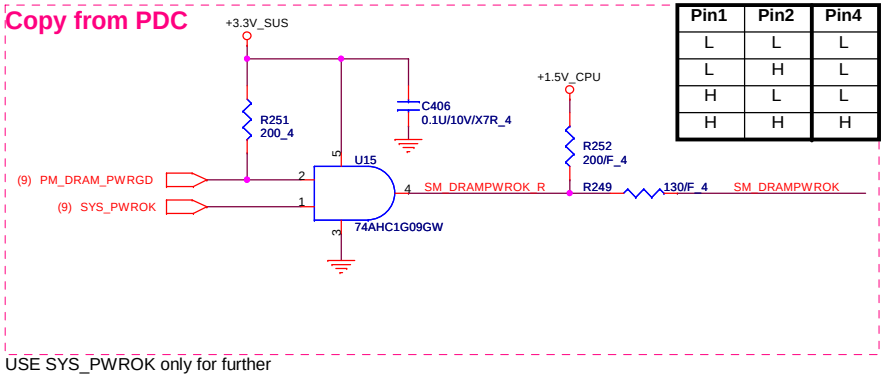
Sandy Bridge Processor (CLK,MISC,JTAG)

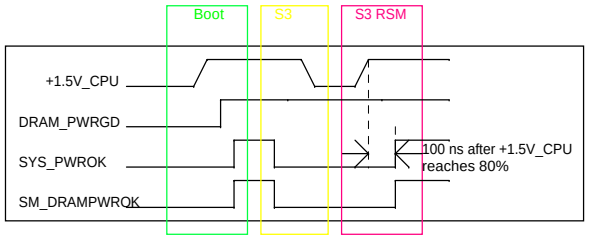


Change OD part same with PDC

Copy from PDC



Pin1	Pin2	Pin4
L	L	L
L	H	L
H	L	L
H	H	H

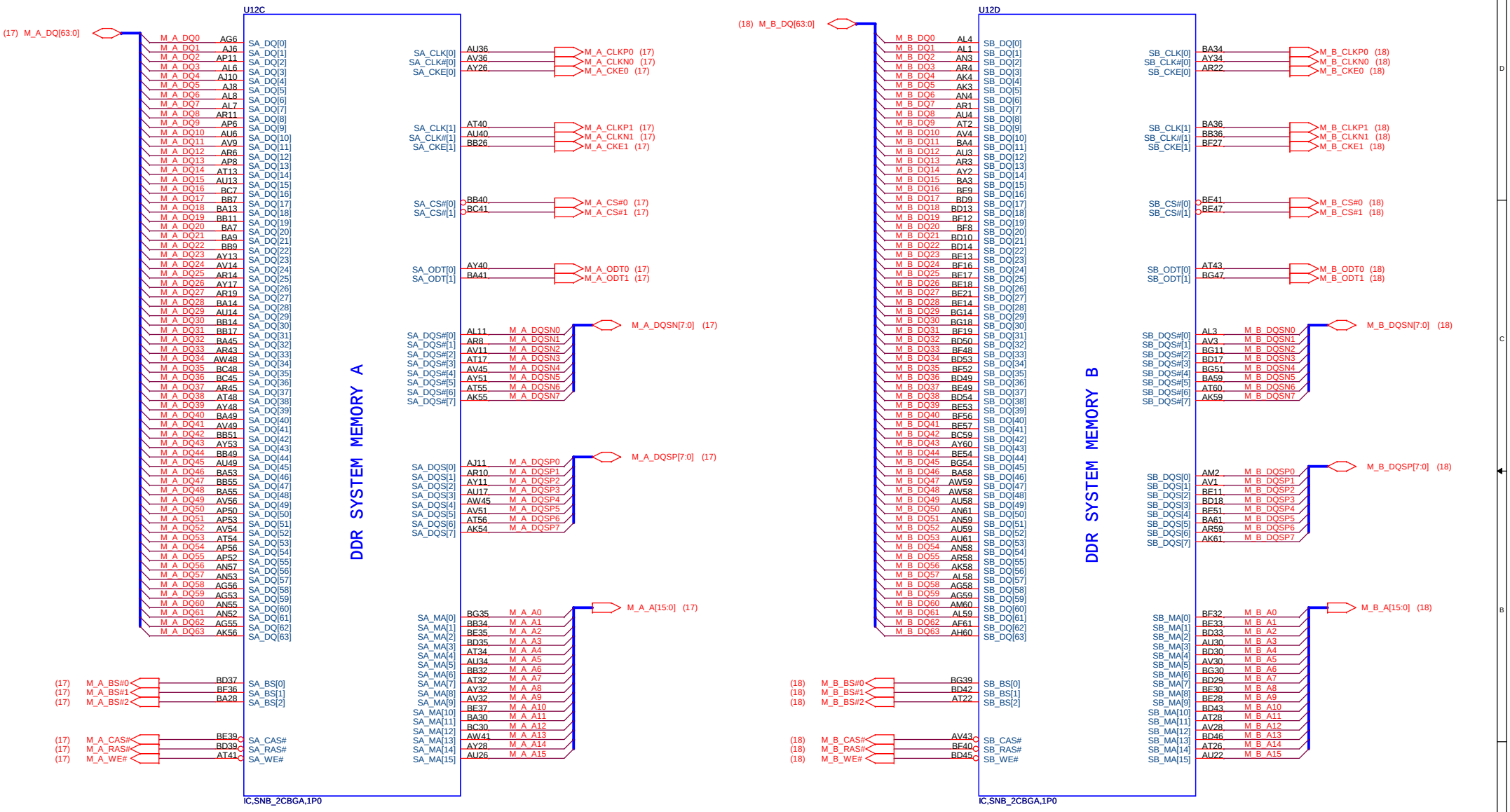


USE SYS_PWROK only for further test without change part

Quanta Computer Inc.
PROJECT : R05

Size	Document Number	Rev
	Sandy Bridge 2/5	2A
Date: Wednesday, June 22, 2011	Sheet 5 of 51	

Sandy Bridge Processor (DDR3)



Quanta Computer Inc.

PROJECT : R05

Size	Document Number	Rev
	Sandy Bridge 3/5	2A

Date: Wednesday, June 22, 2011 Sheet 6 of 51

Sandy Bridge Processor (POWER)

330uF locate power side

CPU Core Power

SNB:55A

8.5A

+VCC_CORE

+1.05V_CPU

U12F

CORE SUPPLY

PEG AND DDR

POWER

QUIET RAILS

SVID

SENSE LINES

Follow PDDG_0.9

IC,SNB_2CBGA,1P0

54.9 ohm has no 5%

Sandy Bridge Processor (GRAPHIC POWER)

U12G

22A

+VCC_GFX_CORE

GRAPHICS

POWER

DDR3 - 1.5V RAILS

SENSE LINES

1.8V RAIL

QUIET RAILS

SA RAIL

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

SM_VREF

+VDDR_REF_CPU

SNB:4A

Add C1084 to 1U

5A

Q12 PDMS7670

PT

(9) PS_S3CNTRL_S

C131 *4700P/25V/X7R_4_NC

4/26 Intel

01/28 R186 R187 NC

Add PR182 PR 181 to 10 ohm

(43) VCC_AXG_SENSE

(43) VSS_AXG_SENSE

VAXG_SENSE

VSSAXG_SENSE

3A

+1.8V_RUN

SNB:6A

+VCCSA_CORE

VCCSA_SENSE

SNB_IVB# N.A at SNB EDS #27637 0.7v1

VCCSA_VID0

VCCSA_VID1

IC,SNB_2CBGA,1P0

If +1.5V_CPU will be implemented, have to change the two divided resistor as 100-ohm 1%

5/16 0ohm to short jump

+3.3V_RUN

H_VTTVID1 (42)

VCCIO_SEL

VCCSENSE (43)

VSSSENSE (43)

VCCIO_SENSE (42)

VSSIO_SENSE (42)

Add PR183, PR184 for power solution 1/13

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK

SVID DATA

Place resistor R204 close to CPU

SVID ALERT

Place resistor R190 close to CPU

H_CPU_SVIDCLK

VR_SVID_CLK (43)

H_CPU_SVIDDAT

VR_SVID_DATA (43)

H_CPU_SVIDALRT#

VR_SVID_ALERT# (43)

Quanta Computer Inc.

PROJECT : R05

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	Sandy Bridge 4/5	2A
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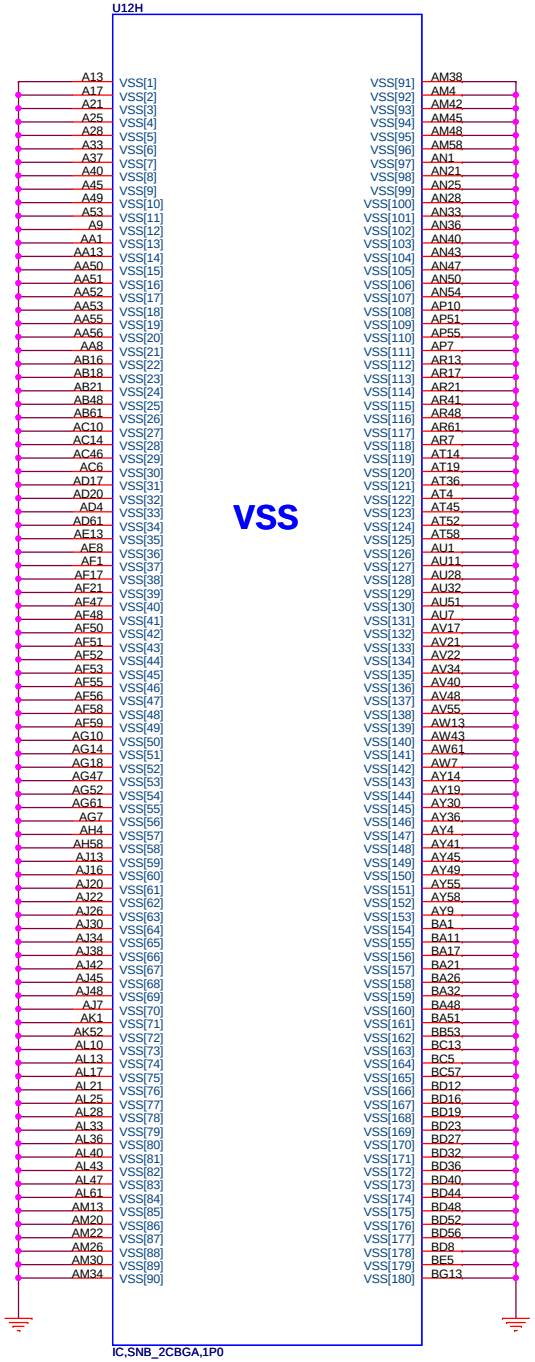
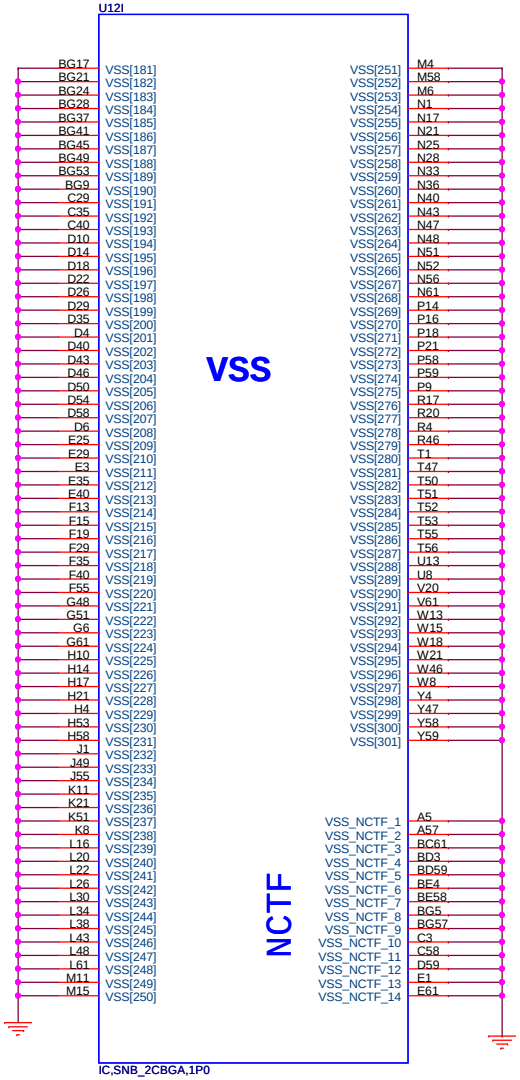
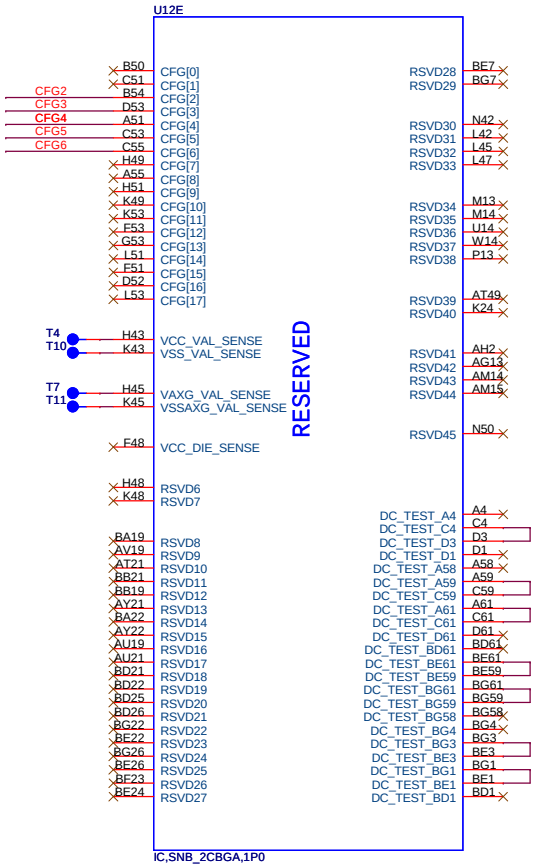
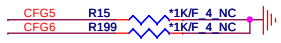
Sandy Bridge Processor (GND)





Sandy Bridge Processor (RESERVED, CFG)





CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed
CFG3 (PCI-E Static x4 Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP

Quanta Computer Inc.
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	Sandy Bridge 5/5	2A
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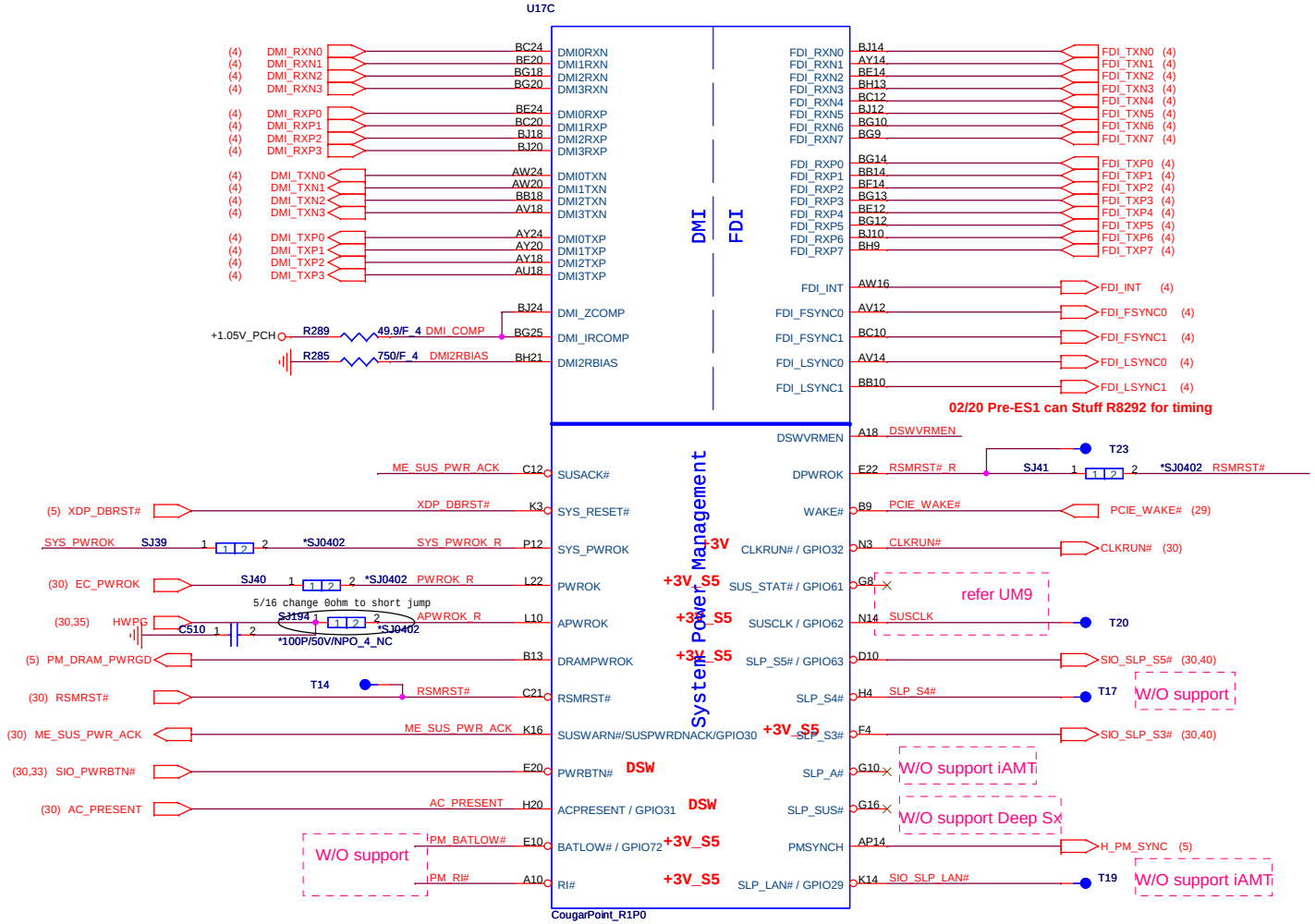
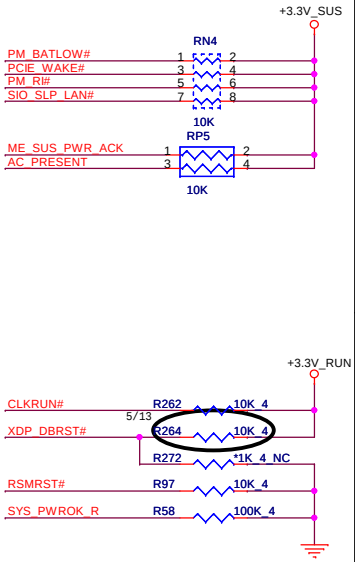
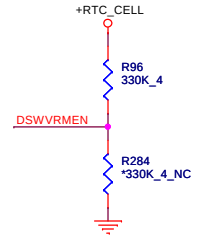
Cougar Point (DMI,FDI,PM)



PCH Pull-high/low(CLG)

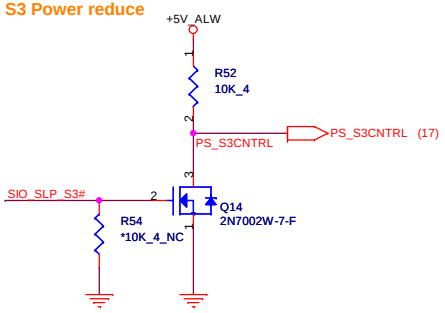


Pull-up to VccRTC (Intel,Tinna)
Even no support Deep Sx?(Intel,Yes)



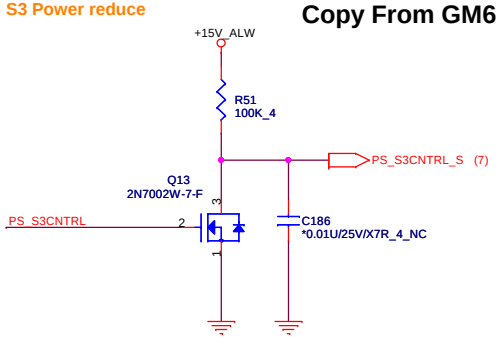
On Die DSW VR Enable
High = Enable (Default)
Low = Disable

S3 Power reduce

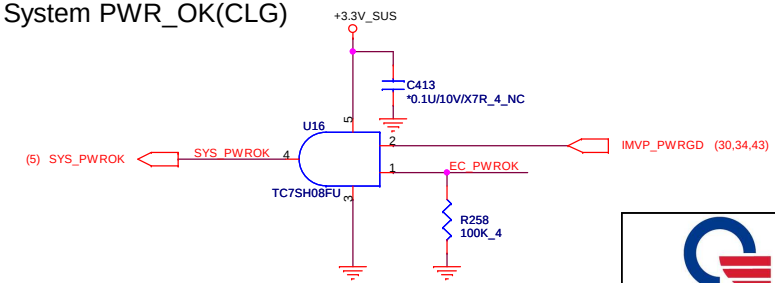


S3 Power reduce

Copy From GM6



System PWR_OK(CLG)



Quanta Computer Inc.

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	Cougar Point 1/7	2A
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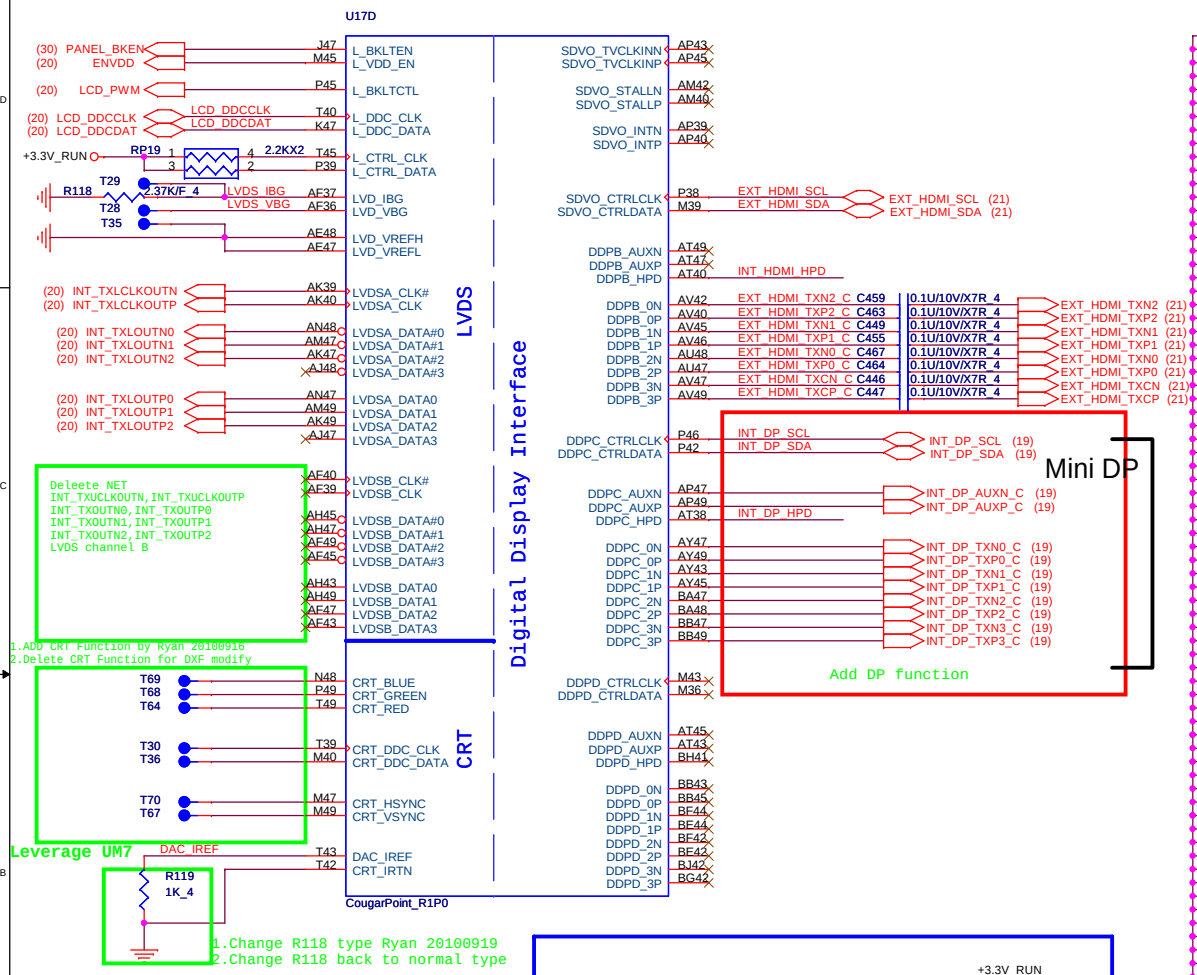
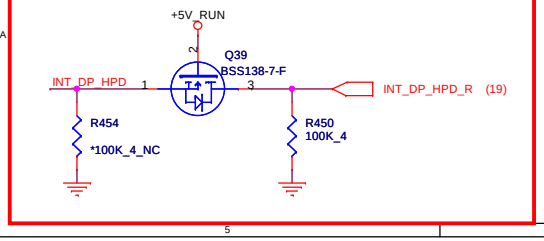
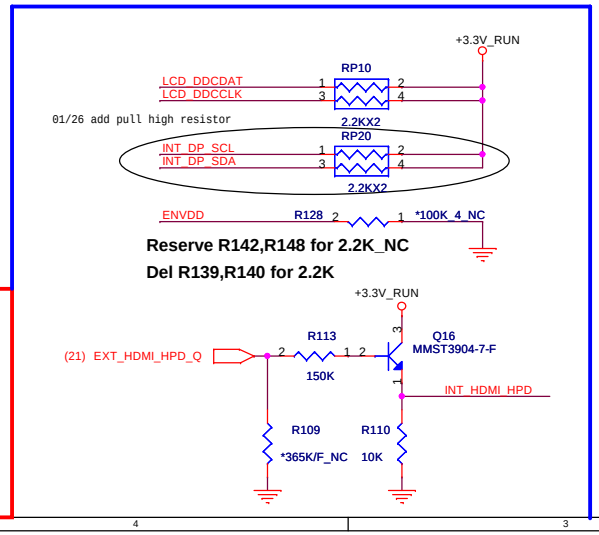
Cougar Point (LVDS,DDI)



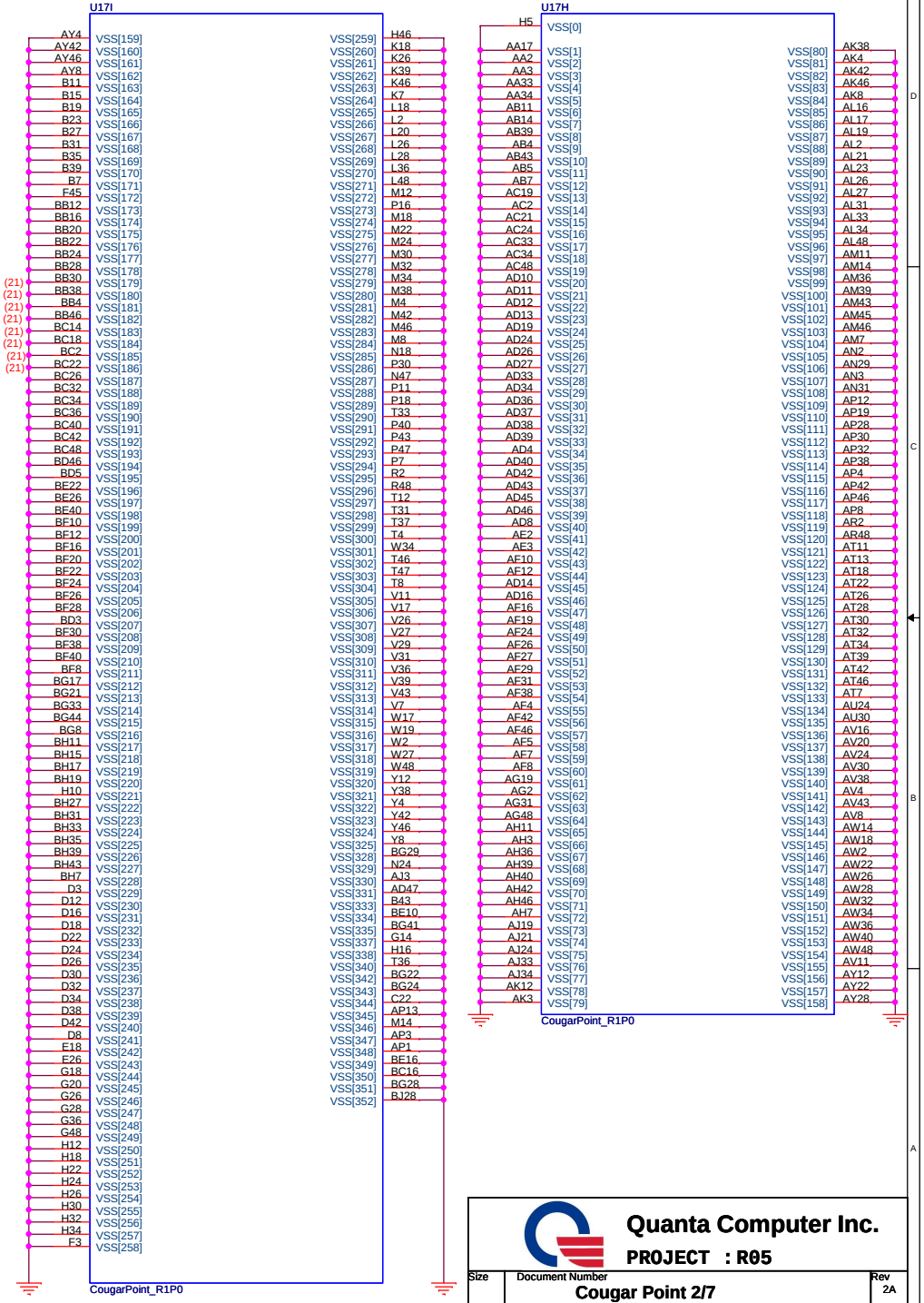




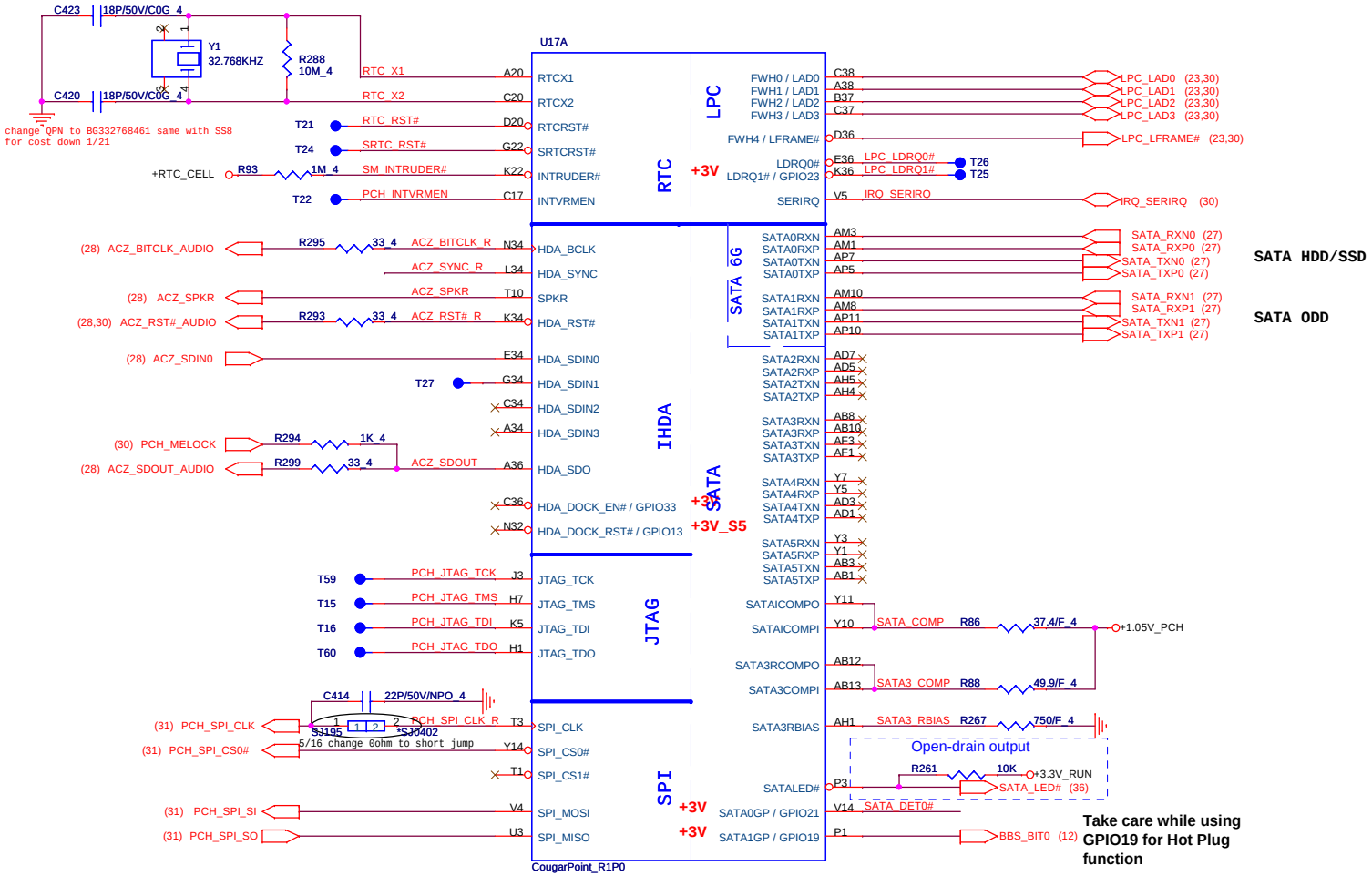
1.ADD CRT Function by Ryan 20100916
2.Delete CRT Function for DXF modify

Leverage UM7

Cougar Point (GND)



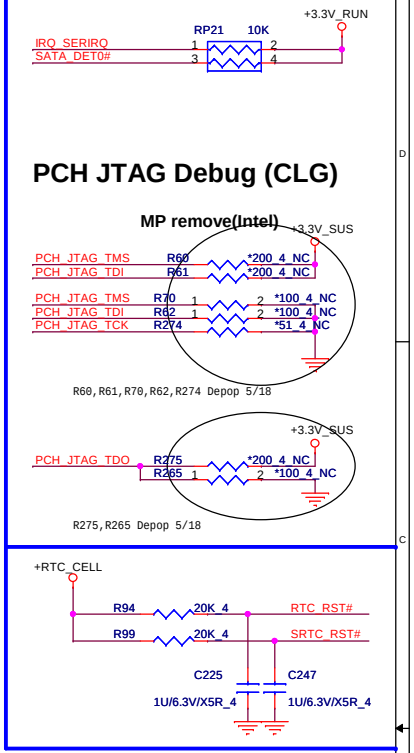
Cougar Point (HDA,JTAG,SATA)



SATA HDD/SSD

SATA ODD

Take care while using GPIO19 for Hot Plug function



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3.3V_RUN R76 *1K_4_NC ACZ_SPKR
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	+3.3V_SUS R297 *1K_4_NC ACZ_SDOUT
Del 0510			**Remove SPI_MOSI from PCH strapping, HR_C/L_v0.91**	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	**Should be always pull-up**	+RTC_CELL R91 330K_4 PCH_INTVRMEN
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V	(28) ACZ_SYNC_AUDIO R300 33_4 ACZ_SYNC_R 1K_4 R305 +3.3V_SUS

Quanta Computer Inc.
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	Cougar Point 3/7	2A
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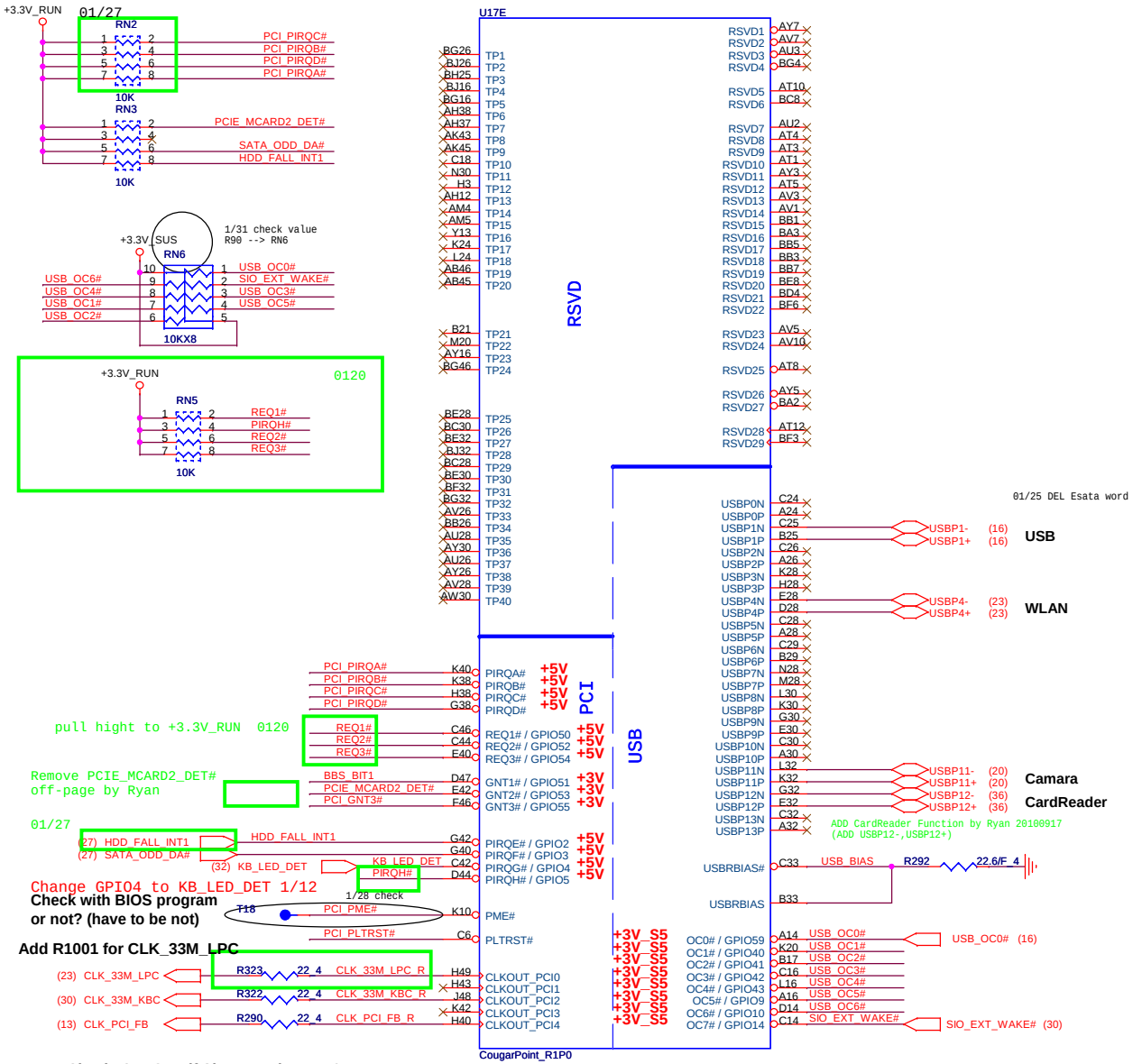
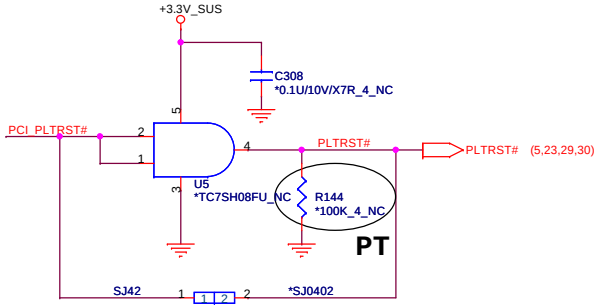
Cougar Point-M (PCI,USB,NVRAM)

change RN2 footprint to "8P4R-0402-SMT"
from 8P4R 1/12

PCI/USBOC# Pull-up(CLG)



PLTRST#(CLG)



Pin Name	Strap description	Sampled	Configuration
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
	R325 *1K_4_NC PCI_GNT3#		Defined in EDS (Intel)
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	Bit 0 / Bit 1 / Boot Location 1 / 1 / SPI * 0 / 0 / LPC
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	
	BBS_BIT1 R324 *1K_4_NC (11) BBS_BIT0 R270 *1K_4_NC		Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]
DF_TVS	DMI and FDI Tx/Rx Termination Voltage	PWROK	weak pull-down 20kohm
	R67 2.2K +1.8V_RUN R74 1K_4 DF_TVS (14) H_SNB_IVB# (5)		CheckList_1.5 p72; HR_v1.5 p476

Quanta Computer Inc.
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Size	Document Number	Rev
	Cougar Point 4/7	2A
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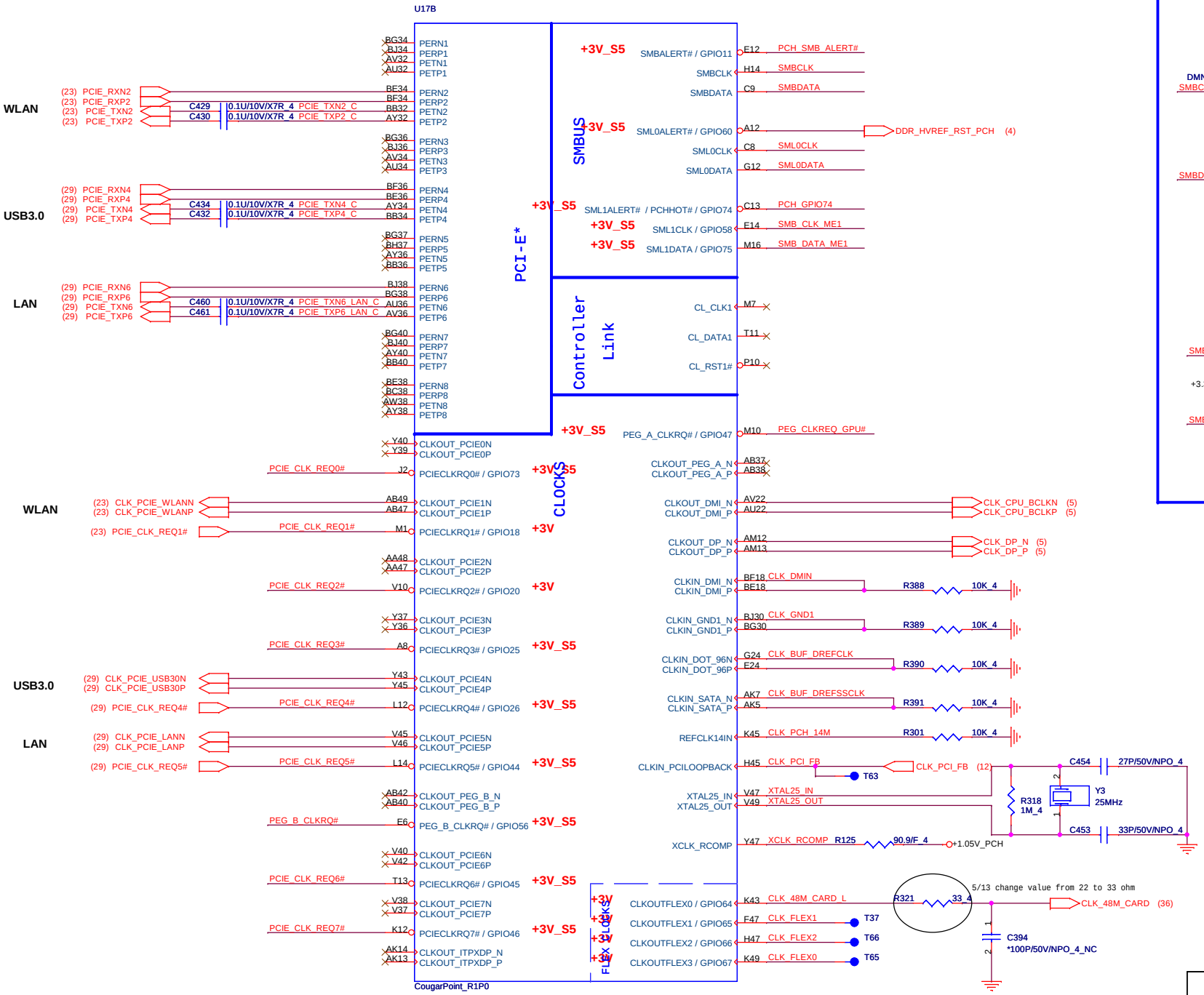
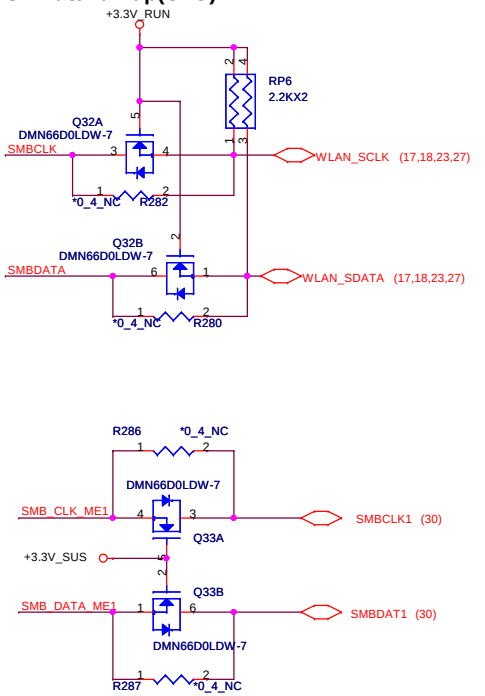
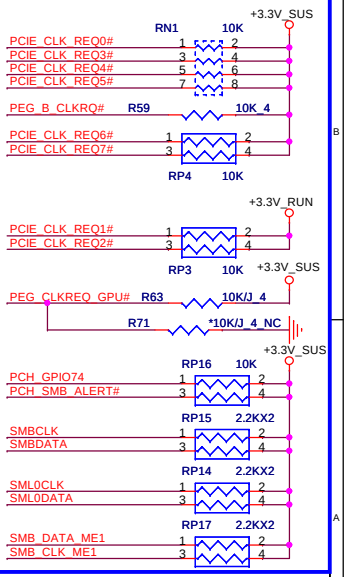
Cougar Point-M (PCI-E,SMBUS,CLK)



SMBus/Pull-up(CLG)



CLK_REQ/Strap Pin(CLG)



Quanta Computer Inc.

PROJECT : R05

Size	Document Number	Rev
	Cougar Point 5/7	2A
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Cougar Point (GPIO,VSS_NCTF,RSVD)

Pin Name	Strap description	Sampled	Configuration
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)

R55 *1K_4_NC PLL_ODVR_EN

Delete NET USB_MCARD2_DET# WWAN Function by Ryan 20100917
GPIO34/STP_PCI#

ADD ODD Function by Ryan

U17F

GPIO

S_GPIO	T7	BMBUSY# / GPIO0	+3V	+3V	TACH4 / GPIO68	C40
(30) SIO_EXT_SMI#	A42	TACH1 / GPIO1	+3V	+3V	TACH5 / GPIO69	B41
PCH_GPIO6	H36	TACH2 / GPIO6	+3V	+3V	TACH6 / GPIO70	C41
(30) SIO_EXT_SCI#	E38	TACH3 / GPIO7	+3V	+3V	TACH7 / GPIO71	A40
(29) SMIB	C10	GPIO8	+3V_S5			
LAN_PHY_PWR_CTRL	C4	LAN_PHY_PWR_CTRL / GPIO12		+3V_S5		
HOST_ALERT#1	G2	GPIO15	+3V_S5			
PCH_GPIO16	U2	SATA4GP / GPIO16	+3V			
	D40	TACH0 / GPIO17	+3V			
GPIO22	T5	SCLOCK / GPIO22	+3V			
(23) PCIE_MCARD1_DET#	E8	GPIO24 / MEM_LED	+3V_S5			
ROUSH_PAID_TS_DET#	E16	GPIO27	DSW			
PLL_ODVR_EN	P8	GPIO28	+3V_S5			
USB_MCARD2_DET#	K1	STP_PCI# / GPIO34	+3V			
(23) USB_MCARD1_DET#	K4	GPIO35	+3V			
CAMERA_CBL_DET#	V8	SATA2GP / GPIO36	+3V			
FDI_OVRVLTG	M5	SATA3GP / GPIO37	+3V			
(23) WLAN_RADIO_DIS#	N2	SLOAD / GPIO38	+3V			
(23) BT_RADIO_DIS#	M3	SDATAOUT0 / GPIO39	+3V			
(27) HDD_FALL_INT2	V13	SDATAOUT1 / GPIO48	+3V			
(30) CRIT_TEMP_REP#	V3	SATA5GP / GPIO49	+3V			
GPIO57	D6	GPIO57	+3V_S5			

CPU/MISC

A20GATE	P4	SIO_A20GATE	SIO_A20GATE (30)
PECI	AU16		H_PECI (5)
RCIN#	P5	SIO_RCIN#	SIO_RCIN# (30)
PROCPWRGD	AY11		H_PWRGOOD (5)
THRMTRIP#	AY10	PCH_THRMTRIP# R82 390_4	PM_THRMTRIP# (5)
INIT3_3V#	T14		
DF_TVS	AY1		DF_TVS (12)
TS_VSS1	AH8		
TS_VSS2	AK11		
TS_VSS3	AH10		
TS_VSS4	AK10		
NC_1	P37		

NCTF

VSS_NCTF_1	A4	VSS_NCTF_15	BG2
VSS_NCTF_2	A44	VSS_NCTF_16	BG48
VSS_NCTF_3	A45	VSS_NCTF_17	BH3
VSS_NCTF_4	A46	VSS_NCTF_18	BH47
VSS_NCTF_5	A5	VSS_NCTF_19	BJ4
VSS_NCTF_6	A6	VSS_NCTF_20	BJ44
VSS_NCTF_7	B3	VSS_NCTF_21	BJ45
VSS_NCTF_8	B47	VSS_NCTF_22	BJ46
VSS_NCTF_9	BD1	VSS_NCTF_23	BJ5
VSS_NCTF_10	BD49	VSS_NCTF_24	BJ6
VSS_NCTF_11	BE1	VSS_NCTF_25	C2
VSS_NCTF_12	BE49	VSS_NCTF_26	C48
VSS_NCTF_13	BF1	VSS_NCTF_27	D1
VSS_NCTF_14	BF49	VSS_NCTF_28	D49
		VSS_NCTF_29	E1
		VSS_NCTF_30	E49
		VSS_NCTF_31	F1
		VSS_NCTF_32	F49

CougarPoint_R1P0

Add 10k Ohom pull-up to 3.3V_RUN

Remove off-page by Ryan 20100921

01/27

Delete R373 WWAN Function by Ryan

Add 10k Ohom pull-up to 3.3V_RUN

GPIO Pull-up/Pull-down(CLG)

Yes

+3.3V_SUS

LAN_PHY_PWR_CTRL	R277	10K_4
GPIO57	R69	10K_4

+3.3V_RUN

SIO_EXT_SMI#	R315	10K_4
SIO_EXT_SCI#	R308	10K_4
CRIT_TEMP_REP#	R268	10K_4
SIO_A20GATE	R65	10K_4
SIO_RCIN#	R75	10K_4
HDD_FALL_INT2	R66	*10K_4_NC
USB_MCARD2_DET#	R273	10K_4
USB_MCARD1_DET#	R278	10K_4
BT_RADIO_DIS#	R263	10K_4
S_GPIO	R105	10K_4
PCH_GPIO16	R260	10K_4
PCIE_MCARD1_DET#	R68	10K_4
WLAN_RADIO_DIS#	R271	10K_4
PCH_GPIO6	R107	10K_4
PCH_GPIO69	R312	10K_4
PCH_GPIO70	R311	10K_4
PCH_GPIO71	R306	10K_4
ROUSH_PAID_TS_DET#	R89	10K_4
SMIB	R281	*10K_4_NC
GPIO22	R56	10K_4

Depop R281 5/18

+3.3V_RUN R64 *1K/F_4_NC FDI_OVRVLTG R72 100K_4

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

Change GPIO36 from pull-up 3.3V_RUN to pull-low for CAMERA_CBL_DET#

+3.3V_RUN R73 200K_4 CAMERA_CBL_DET#

Change GPIO36 from pull-low 3.3V_RUN to pull-up 3.3V_RUN for CAMERA_CBL_DET#

Change R106 from CS42002JB14 to CS42002FB04

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

Reserve (PDC)

+3.3V_SUS

HOST_ALERT#1 R276 1K_4

Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

MFG-TEST

del 0527

Quanta Computer Inc.

PROJECT : R05

Size	Document Number	Rev
	Cougar Point 6/7	2A
Date: Wednesday, June 22, 2011	Sheet 14 of 51	

COUGAR POINT (POWER)

Cougar Point (POWER)

VccCORE =1.14A(50mils)

need 1206?

VccADAC =1mA(8mils)

VCCDSW3_3 tie to 3.3V_SUS, when don't support Deep SX CP_v1.0 p88

VccALVDS=1mA (8mils)

VccTX_LVDS=60mA (10mils)

C159:CH6221M9A03->CH6221M9A01

need Indutor?

Vcc3_3 = 0.266A (15mils)

Change CH6101M9905 to CH61001KA94

VccIO =2.925 A(120mils)

Near to AN16, AP21, AN33

VccVRM(1.5V) =0.16 A(10mils)

VccDMI =0.042 A(10mils)

VccDMI = 80mA (10mils)

VccCLKDMI = 20mA (8mils)

VCCPNAND = 190 mA(15mils)

VCCSPI = 20mA(8mils)

01/26 power rail for VCCIO

VCCVRM: 1.8V (Destop) 07/20 del for Pre-ES1
1.5V (Mobile)

*Short Jump_150

change SJ21 to Jump150 / 3720package 1/12

VccASW =1.01A (50mils)

VccDSW3_3= 3mA(8mil)

80mA(10mils)

80mA(10mils)

VCCDIFFCLKN= 55mA(18mils,PDDG)

VCCSSC= 95mA(10mils)

01/26 power rail for VCCIO

1mA(8mils)

VCCRTC<1mA(8mils)

VCCSUS3_3 = 119mA (15mils)

VCC5REFSUS=1mA(8mil)

V5REF= 1mA(8mil)

VCCSUS3_3 = 119mA (15mils)

VCCPCORE = 28mA(10mils)

C278:CH5102K9B06 ->CH5101K9B01

C197:CH5102K9B06->CH5101K9B01

VCCVRM= 114mA(15mils)

C481:CH6101M9905->CH61001KA94

change +1.05V_VCCEPW to +1.05V_PCH 1/12

VCCSUSHDA= 10mA(8mils)

C145:CH6221M9A03->CH6221M9A01

C106:CH6221M9A03->CH6221M9A01

C247:CH5102K9B06->CH5101K9B01

Quanta Computer Inc.
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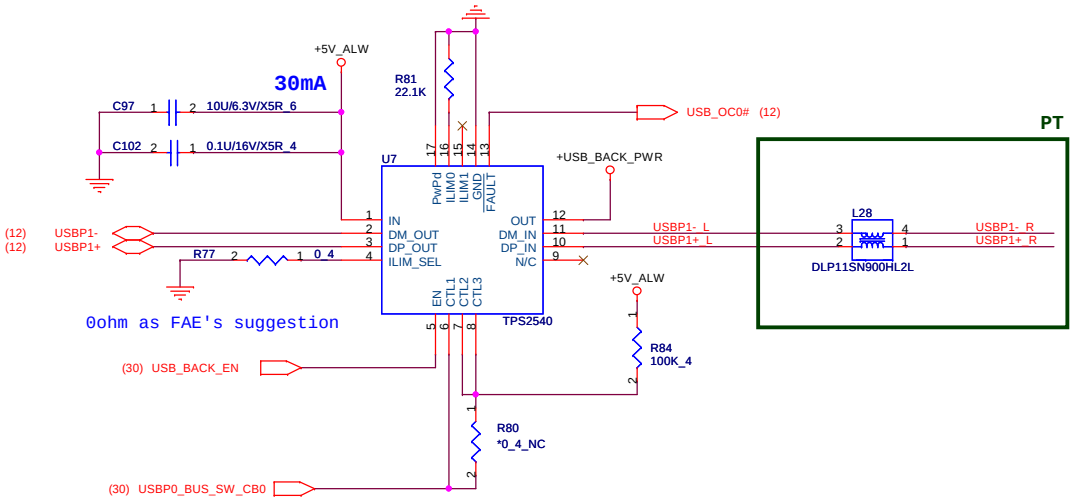
Size	Document Number	Rev
	Cougar Point 7/7	2A
Date: Wednesday, June 22, 2011	Sheet 15 of 51	

USB Conn + Power share

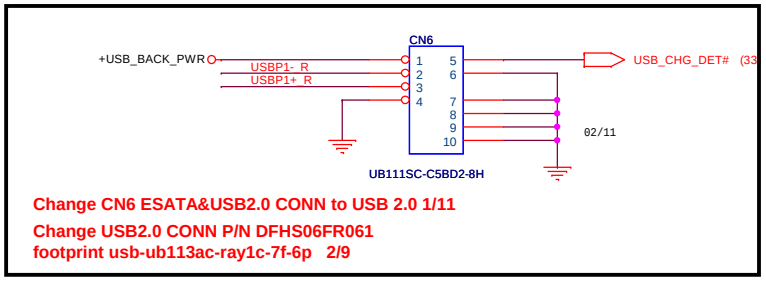
S3/S5 USB charging circuit



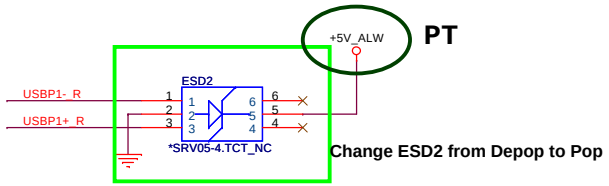
USBP0_BUS_SW_CB0	Mode
Low	DCP, Auto-detect
High	CDP, BC Spec 1.1

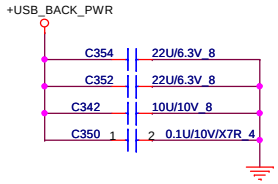
	R81	mA	
OC limitation	100k ohm	480	
	22.1k ohm	2171	Applied Now

1/31 ADD OFFPAGE PORT



Change footprint for ME request





Quanta Computer Inc.			
PROJECT : R05			
Size	Document Number		Rev
	PUSB / ESATA		2A
Date: Wednesday, June 22, 2011	Sheet 16 of 51		

H=8.0mm,RVS

SO-DIMMA SPD Address is 0XA0
SO-DIMMA TS Address is 0X30

Still Support? (Yes)

Change R205,R257 to RP1014 by Ryan

JDIM1A

PC2100 DDR3 SDRAM SO-DIMM (204P)

DGMK4000005
ddr-ddrrk-20401-tp4b-204p-ruv

S3 Power reduce

+0.75V_DDR_VTT
R253 22_4
Q28 2N7002W-7-F
PS_S3CNTRL (9)

JDIM1B

PC2100 DDR3 SDRAM SO-DIMM (204P)

DGMK4000005
ddr-ddrrk-20401-tp4b-204p-ruv

Change JDIM1A,JDIMB P/Q to DGMK4000005

C531,C530,C529,C528,C527,C526:
CH6101M9A07->CH61001KA94

Change C357 CH6101M9A07 to CH61001KA94
C356,C358:CH6101M9A07->CH61001KA94

Place these Caps near So-Dimm0.

Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%

11/6

M1 VREF

change C331 PN CH4102KB93 to CH4102K1B03

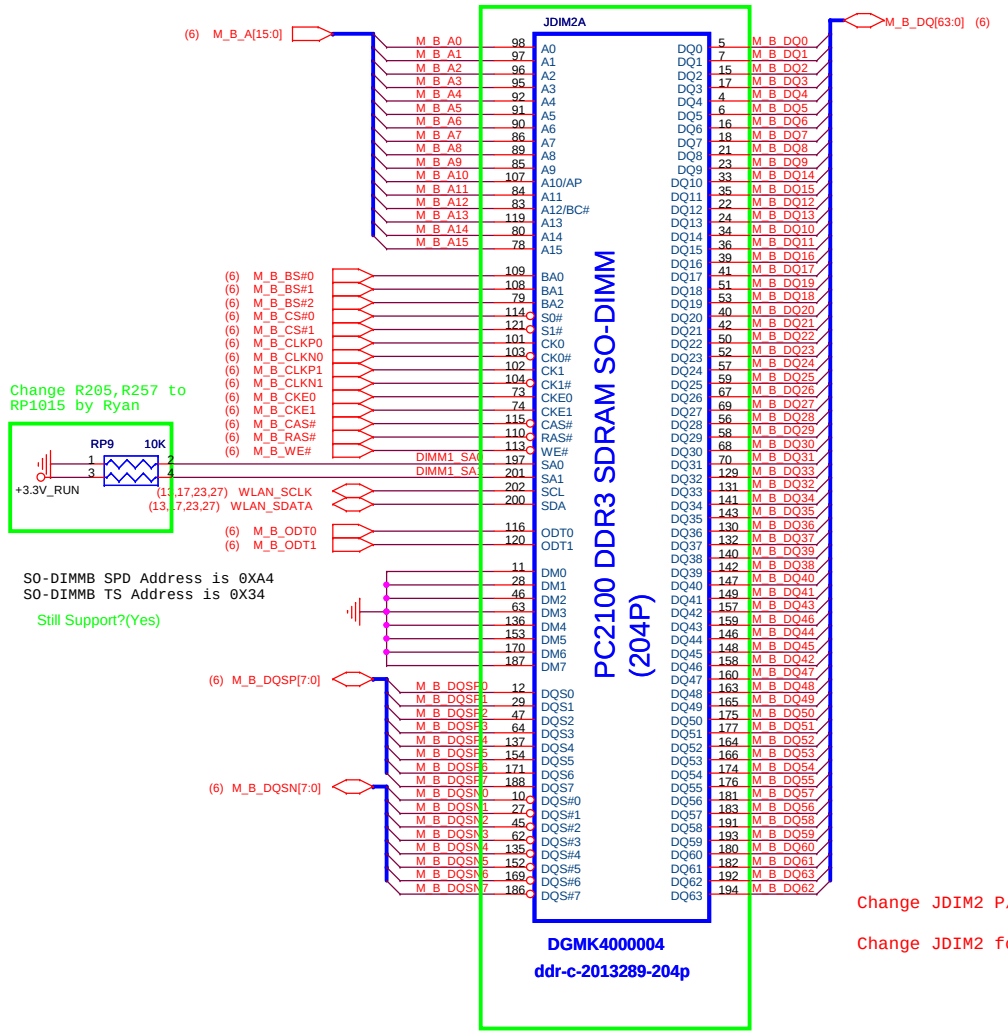
change C380 PN CH4102KB93 to CH4102K1B03

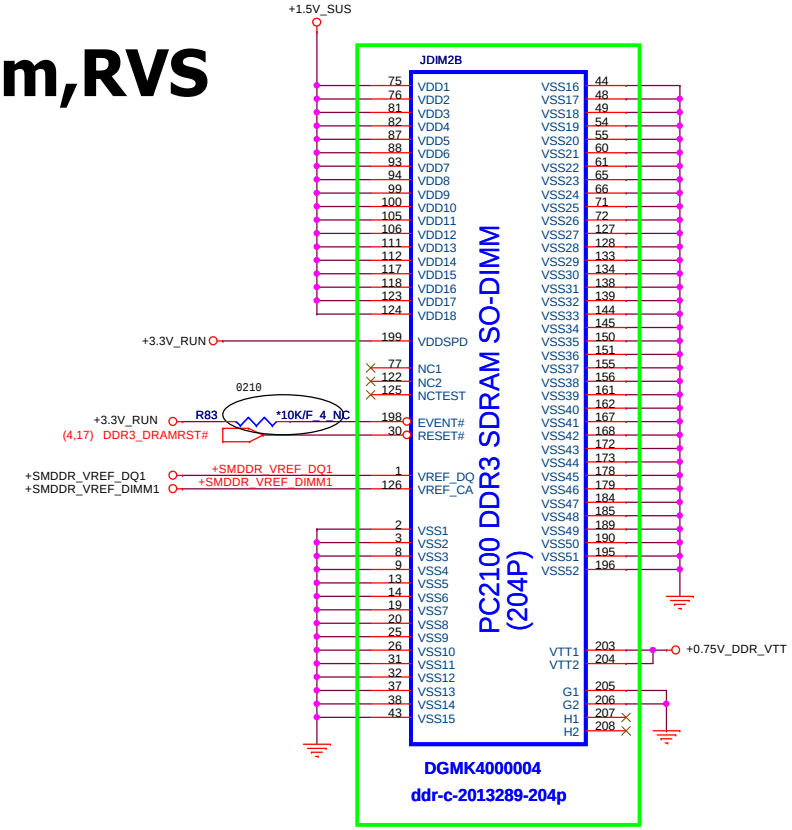
Quanta Computer Inc.
PROJECT : R05

Size	Document Number	Rev
	DDR3 DIMM-0	2A

Date: Wednesday, June 22, 2011 Sheet 17 of 51

H=4.0mm,RVS





Change JDIM2 P/N to DGMK4000004 from DGMK4000005 1/17

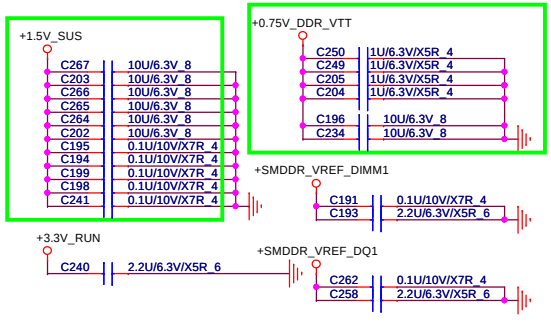
Change JDIM2 footprint to ddr-c-2013289-204p from ddr-ddrrk-20401-tp4b-204p-ruv 1/17

C374:CH61001ME96->CH61001KA94
C370:CH6101M9A07->CH61001KA94
C368,C373,C364,C366:
CH6101M9A07->CH61001KA94

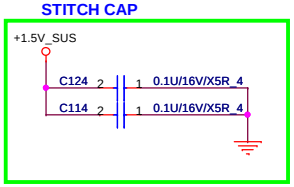
Change C365 CH6101M9A07 to CH61001KA94
C369,C372:CH6101M9A07->CH61001KA94

Place these Caps near So-Dimm1.

Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%



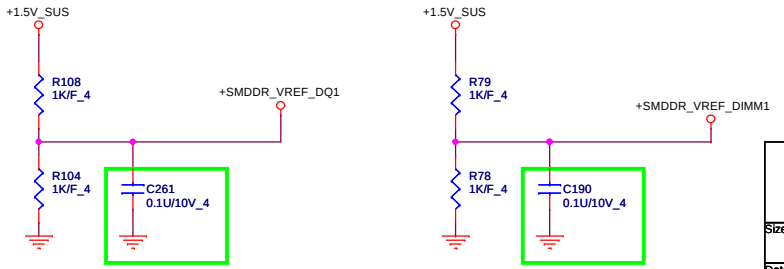
2/15 FOR SATA SIGNAL CROSS MOAT STITCH CAP



change C410 PN CH4102KB93 to CH4102K1B03

change C380 PN CH4102KB93 to CH4102K1B03

M1 VREF



Quanta Computer Inc.
PROJECT : R05

Size	Document Number	Rev
	DDR3 DIMM-1	2A
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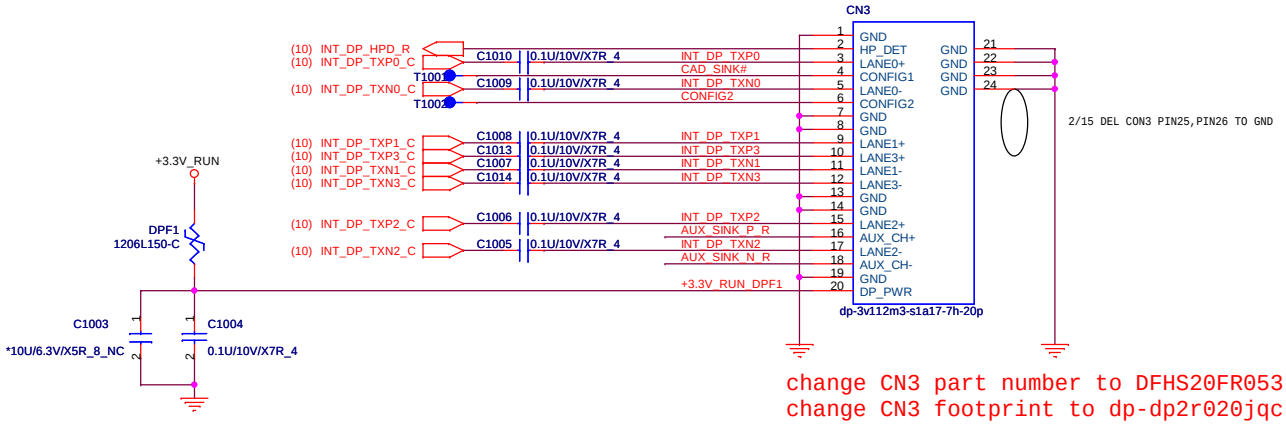
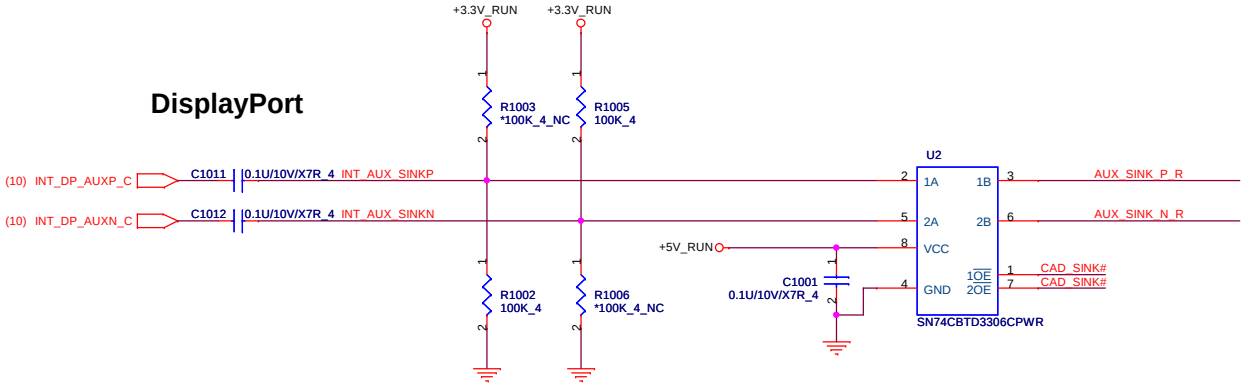
MINI DISPLAY PORT CONNECTOR

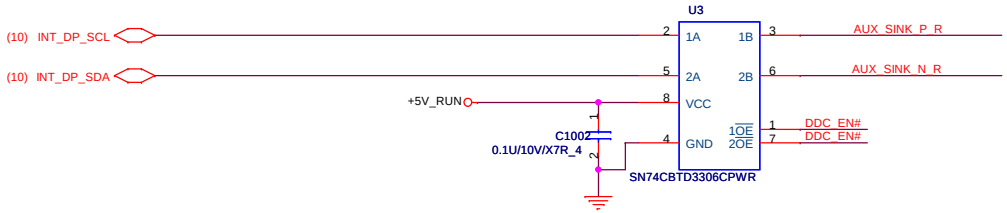


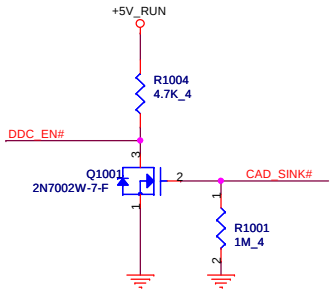
change CN3 part number to DFHS20FR053 from DFHS20FR093 1/11
change CN3 footprint to dp-dp2r020jqc-cp-20p-v-smt
from dp-3v112m3-s1a17-7h-20p 1/11

DisplayPort

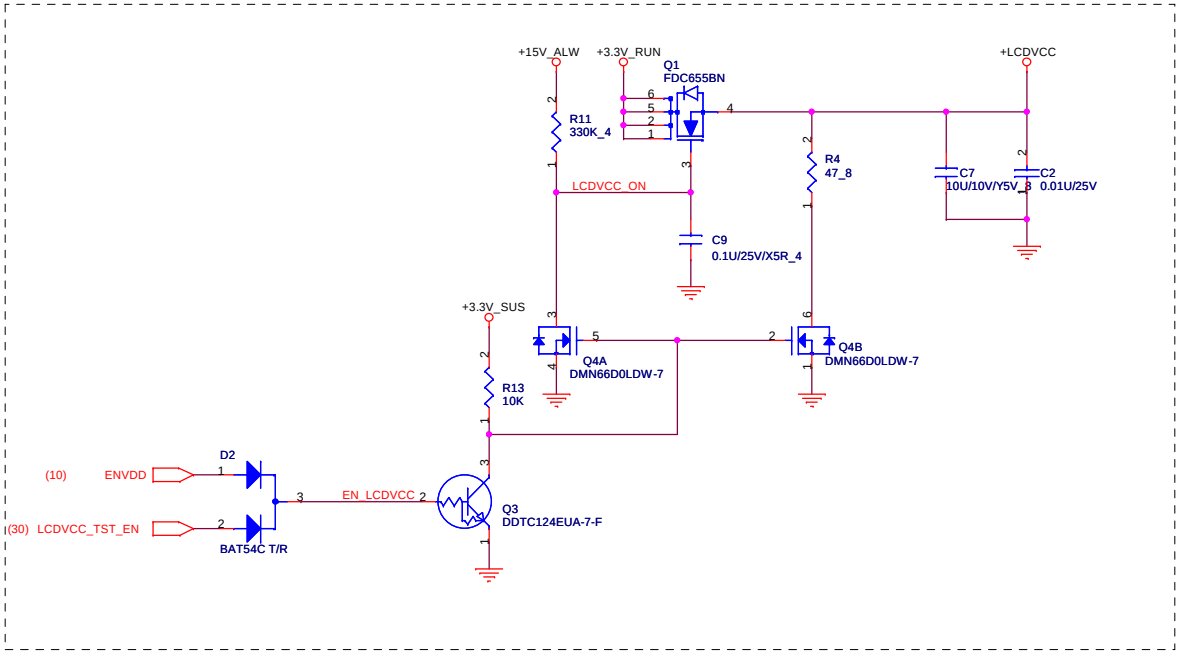


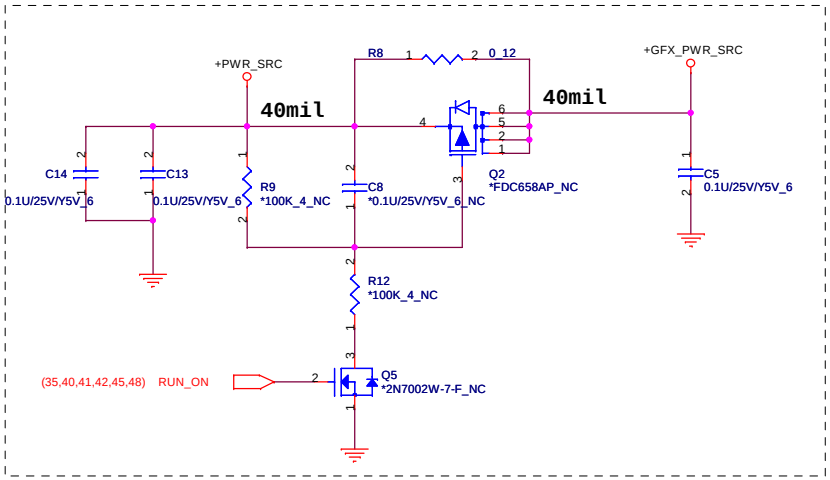
HDMI

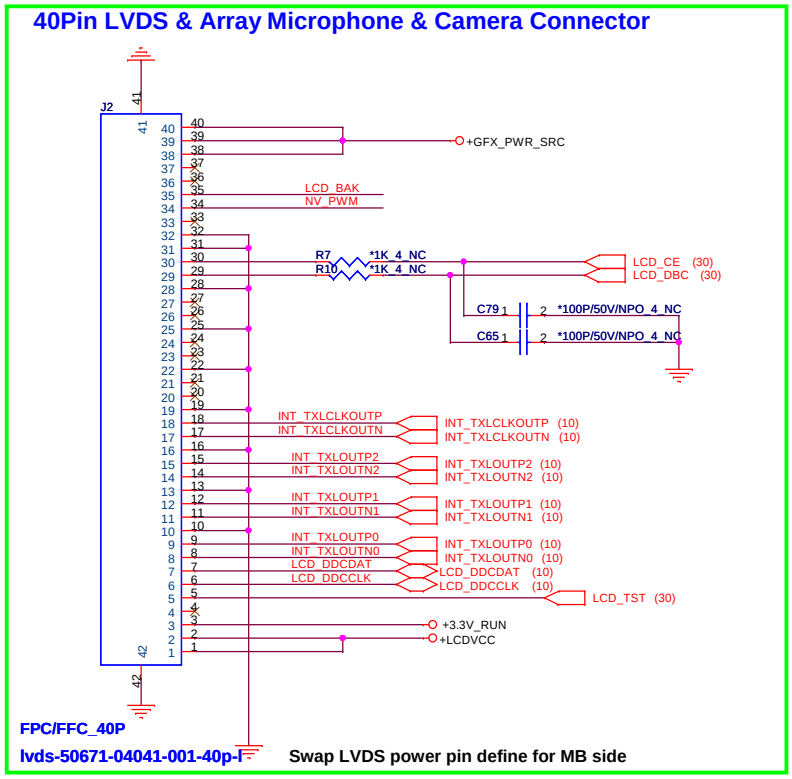


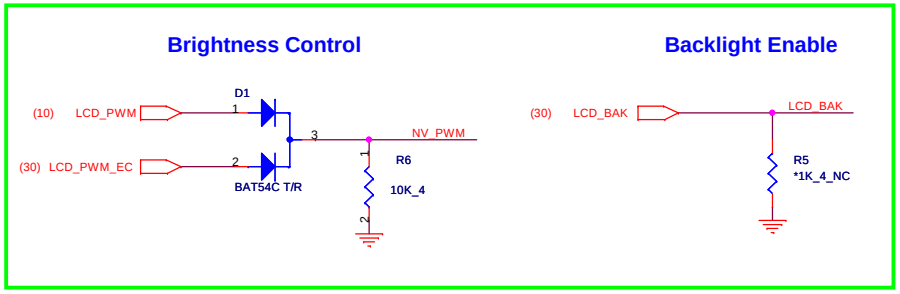


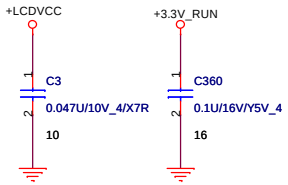
Quanta Computer Inc.		
PROJECT : R05		
Size	Document Number: MINI DP CONN	Rev: 2A
Date: Wednesday, June 22, 2011	Sheet 19 of 51	









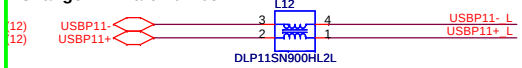


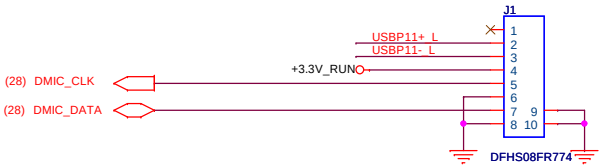
TO CCD CONNECTOR

Change L12 from Depop to Pop

Change R180;R181 from Pop to Depop 5/13

Change L12 Part Number





Quanta Computer Inc.

PROJECT : R05

Size	Document Number	Rev
	LVDS CONN	2A
Date: Wednesday, June 22, 2011	Sheet 20 of 51	

HDMI

Depop L26,L27,L30,L31 & short two point

(10) EXT_HDMI_TXN2
(10) EXT_HDMI_TXP2
L26 *EXC24CG900U_NC
HDMI_TXDN2_RL
HDMI_TXDP2_RL

(10) EXT_HDMI_TXN1
(10) EXT_HDMI_TXP1
L27 *EXC24CG900U_NC
HDMI_TXDN1_RL
HDMI_TXDP1_RL

(10) EXT_HDMI_TXN0
(10) EXT_HDMI_TXP0
L30 *EXC24CG900U_NC
HDMI_TXDN0_RL
HDMI_TXDP0_RL

(10) EXT_HDMI_TXCN
(10) EXT_HDMI_TXCP
L31 *EXC24CG900U_NC
HDMI_TXCN_RL
HDMI_TXCP_RL

+3.3V_RUN
RP18 4.7KX2
(10) EXT_HDMI_SCL
(10) EXT_HDMI_SDA
Q19 FDV301N
Q34 FDV301N

Add D30 & R1037 for QT 0615
+5V_RUN
D30 RB500V-40
R1037 *0_4_NC
RP8 2.2KX2

HDMI_TXDP2_RL
HDMI_TXDN2_RL
HDMI_TXDP1_RL
HDMI_TXDN1_RL
HDMI_TXDP0_RL
HDMI_TXDN0_RL
HDMI_TXCP_RL
HDMI_TXCN_RL
HDMI_CLK
HDMI_DAT
+5V_RUN_HDMIF1

CN4 Connector-HDMI
SHELL1 D2+ D2 Shield D2- D1+ D1 Shield D1- D0+ D0 Shield D0- CK+ CK Shield CK- CE Remote NC DDC CLK DDC DATA GND 5V HP DET SHELL2

5/13 change footprint F3_2X1_65-2_8
+5V_RUN
HDMIF1 1206L110THYR
C439 *0.1U/10V/X7R_4_NC

(10) EXT_HDMI_HPD_Q
SJ22 *SJ0402
HDMI_HPD_R
C280 0.1U/10V/X7R_4

R336 680/F HDMI_TXDP2_RL
R334 680/F HDMI_TXDN2_RL
R328 680/F HDMI_TXDP1_RL
R320 680/F HDMI_TXDN1_RL
R339 680/F HDMI_TXDP0_RL
R342 680/F HDMI_TXDN0_RL
R317 680/F HDMI_TXCP_RL
R314 680/F HDMI_TXCN_RL

+3.3V_RUN
Q20 2N7002W-7-F

Quanta Computer Inc.
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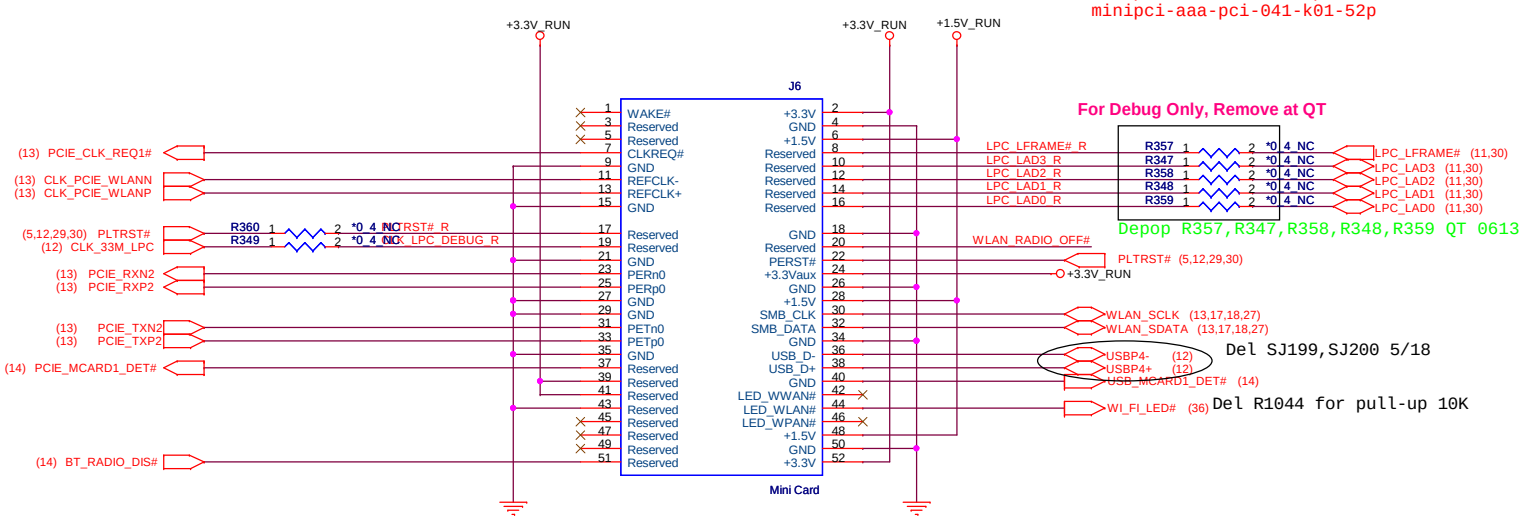
Size	Document Number	Rev
	HDMI CONN	2A
Date: Wednesday, June 22, 2011	Sheet 21 of 51	

1.Deltet MINI DP Function by Ryan 20100916
2.Add MINI DP Function
3.Deltet MINI DP Function

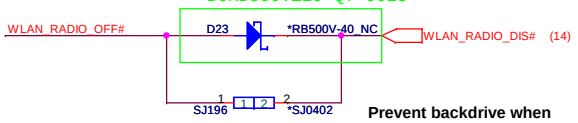
MiniCard WLAN connector

1/17 Change J6 footprint to
minipci-80052-1021-52p-ldv-v from
minipci-aaa-pci-041-k01-52p



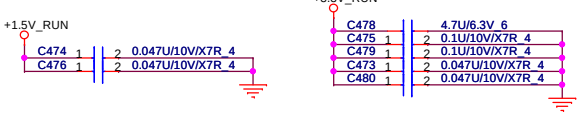
Support for WoW

change D23 PN to
BCRB500VZ29 QT 0615



Prevent backdrive when WoW is enabled.

Place caps close to connector.



Quanta Computer Inc.

PROJECT : R05

Size	Document Number	Rev
	MINI-PCI (WLAN/WPAN)	2A
Date: Wednesday, June 22, 2011	Sheet 23 of 51	

Deltet WWAN Function by Ryan 20100916

Quanta Computer Inc.

PROJECT : R05

Size	Document Number	Rev
	CCD CONNECTOR	2A

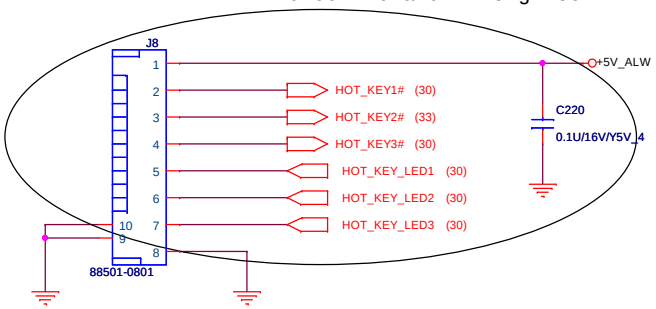
Date: Wednesday, June 22, 2011 Sheet 24 of 51

USB3.0 schematic Remove to IO Board

HotKey CONN

Add HotKey CONN

Check EC and ME engineer



Quanta Computer Inc.

PROJECT : R05

Size	Document Number	Rev
	NEC USB 3.0	2A

Date: Wednesday, June 22, 2011 Sheet 25 of 51

USB3.0 CONN schematic Remove to IO Board

Quanta Computer Inc.

PROJECT : R05

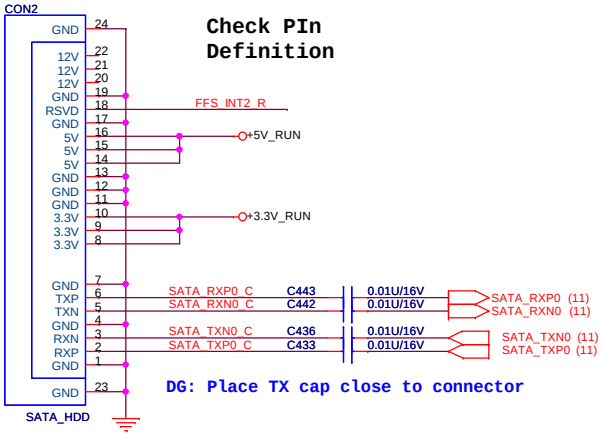
Size	Document Number	Rev
	USB 3.0 CONN	2A

Date: Wednesday, June 22, 2011 Sheet 26 of 51

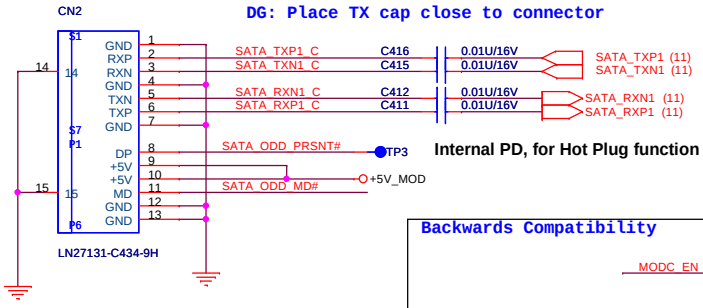
Change CON1001 from DFHS22FR085 to DFHS22FR178

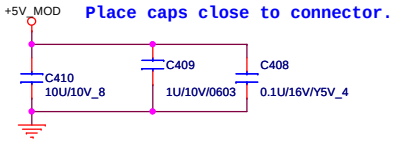
Change CON1001 footprint from sata-c166p5-12205-l-22p-r to sata-sat-22hd0b-22p-l-v

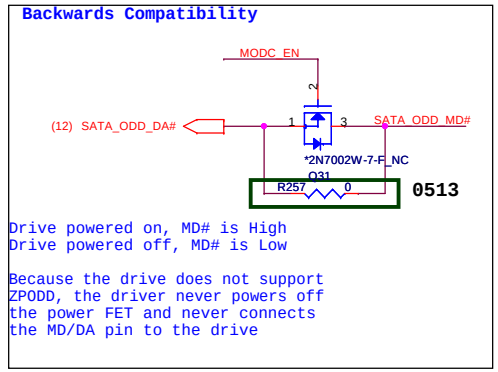
SATA Connector UM8

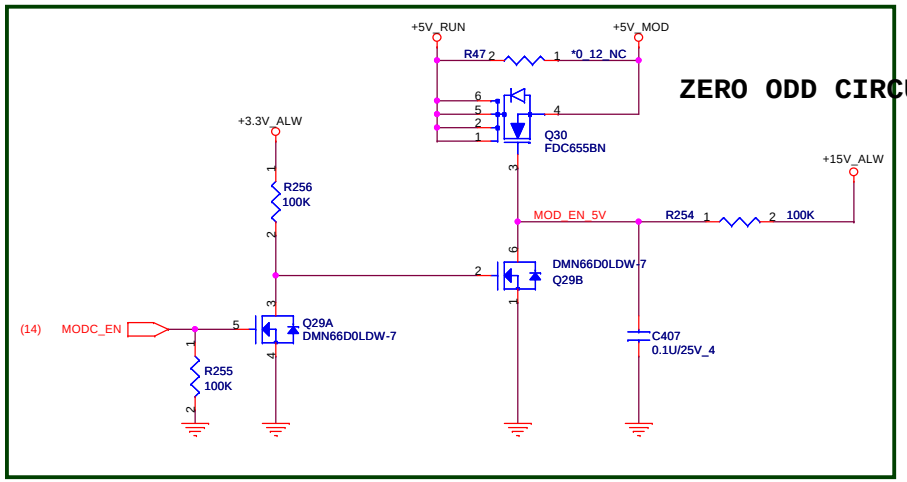


ODD Connector

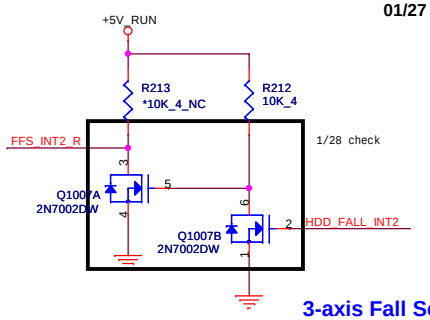




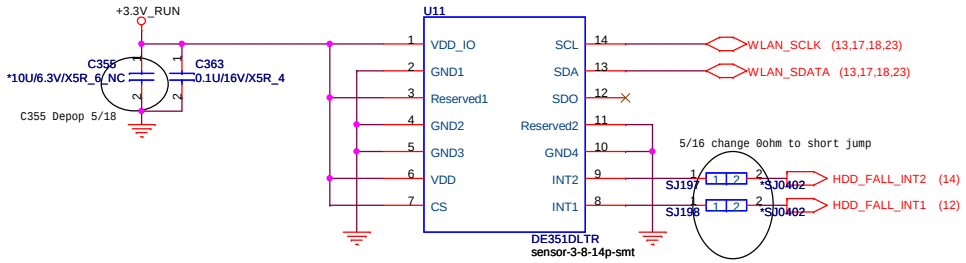




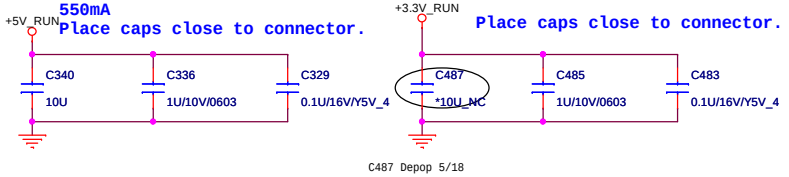
01/27 ADD FALL SENSON CIRCUIT



3-axis Fall Sensor (HDD data protector)



Change CON2 HDD CONN form DFHS22FR178 to DFHS22FR129



Quanta Computer Inc.

PROJECT : R05

Size	Document Number	Rev
	SATA HDD/ODD	2A

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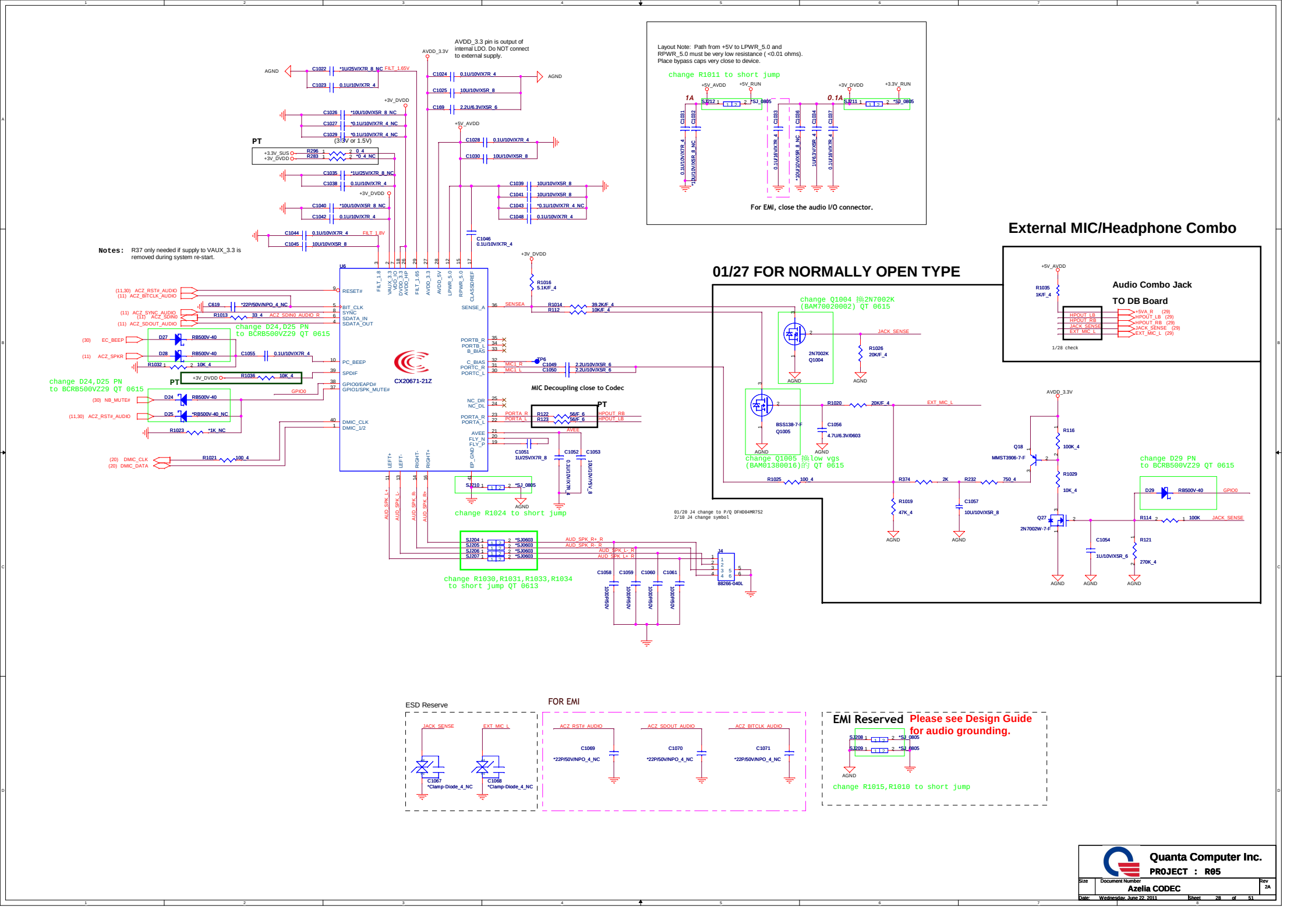
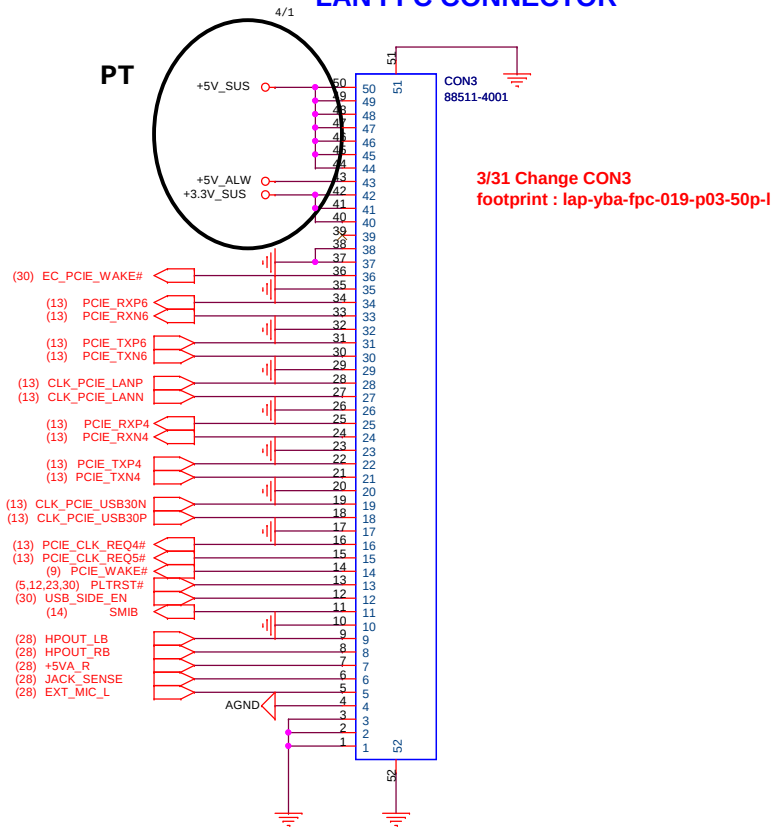

AVDD_3.3 pin is output of internal LDO. Do NOT connect to external supply.
Layout Note: Path from +5V to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms). Place bypass caps very close to device.
change R1011 to short jump
For EMI, close the audio I/O connector.
External MIC/Headphone Combo
Audio Combo Jack
TO DB Board
01/27 FOR NORMALLY OPEN TYPE
Notes: R37 only needed if supply to VAUX_3.3 is removed during system re-start.
change D24,D25 PN to BCRB500VZ29 QT 0615
CX20671-21Z
MIC Decoupling close to Codec
change Q1004 換2N7002K (BAM70020002) QT 0615
change Q1005 換low vgs (BAM01380016)的 QT 0615
change D29 PN to BCRB500VZ29 QT 0615
change R1024 to short jump
change R1030,R1031,R1033,R1034 to short jump QT 0613
01/20 J4 change to P/Q DFHD04MR752
2/10 J4 change symbol
ESD Reserve
FOR EMI
EMI Reserved
Please see Design Guide for audio grounding.
change R1015,R1010 to short jump
Quanta Computer Inc.
PROJECT : R05
Azelia CODEC
Wednesday, June 22, 2011

LAN (AR8151B) schematic remove to DB

LAN FFC CONNECTOR



3/31 Change CON3
footprint : lap-yba-fpc-019-p03-50p-l

Quanta Computer Inc.
PROJECT : R05

Size	Document Number	Rev
	FFC CONN	2A
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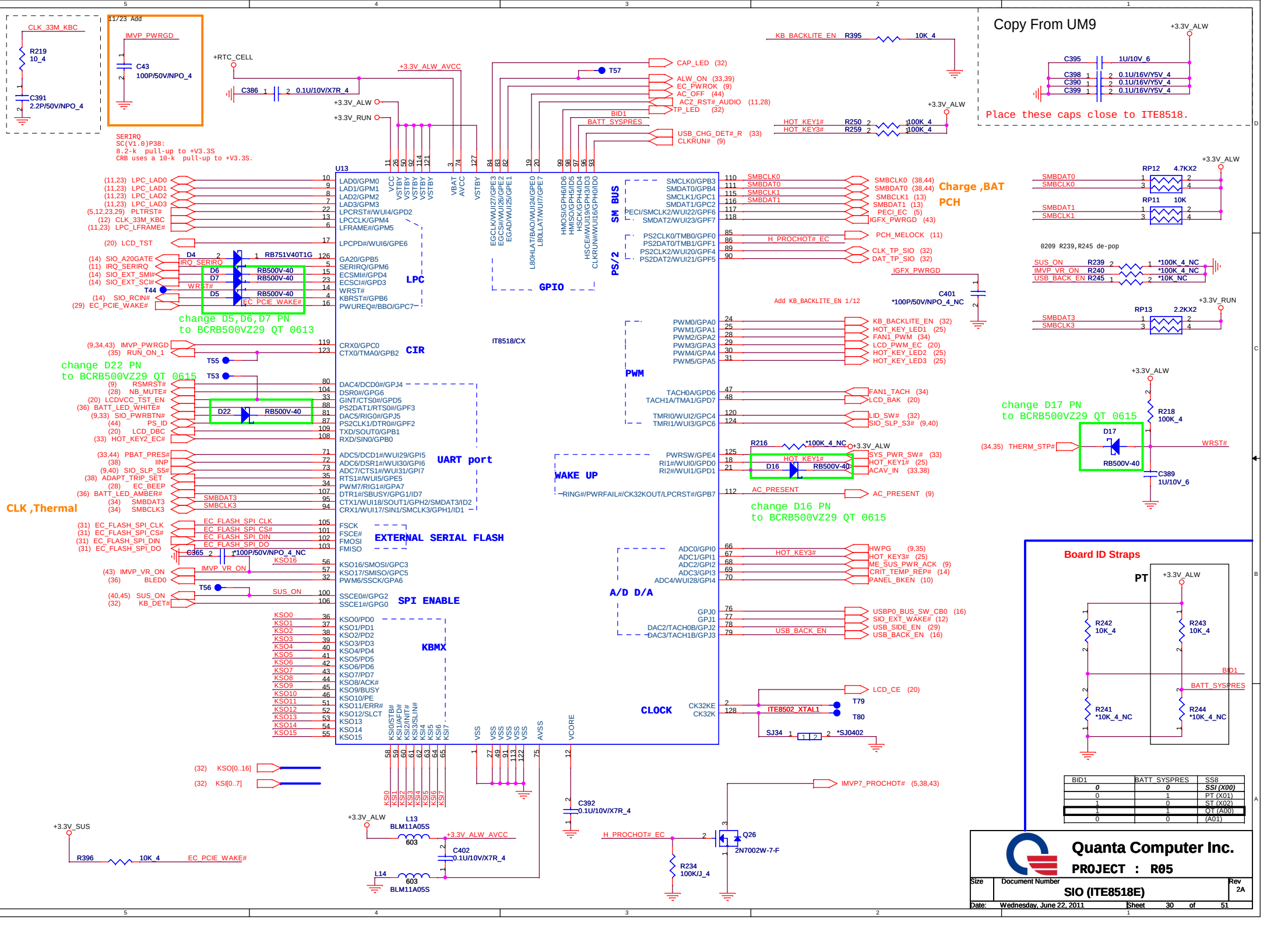
Copy From UM9
Place these caps close to ITE8518.
change D5,D6,D7 PN to BCRB500VZ29 QT 0613
change D22 PN to BCRB500VZ29 QT 0615
change D16 PN to BCRB500VZ29 QT 0615
change D17 PN to BCRB500VZ29 QT 0615
Add KB_BACKLITE_EN 1/12
0209 R239,R245 de-pop
SERIRQ
SC(V1.0)P38:
8.2-k pull-up to +V3.3S
CRB uses a 10-k pull-up to +V3.3S.
U13
IT8518/CX
LPC
CIR
GPIO
SM BUS
PS/2
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
A/D D/A
CLOCK
Charge ,BAT
PCH
CLK ,Thermal
Board ID Straps
PT
Quanta Computer Inc.
PROJECT : R05
SIO (ITE8518E)
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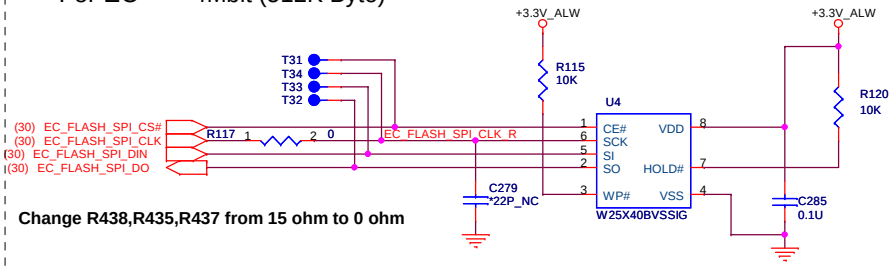
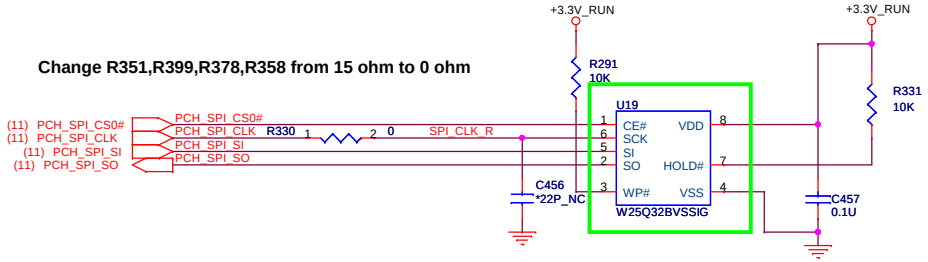
For EC 4Mbit (512K Byte)



Change R438,R435,R437 from 15 ohm to 0 ohm

For PCH 32Mbit (4M Byte)

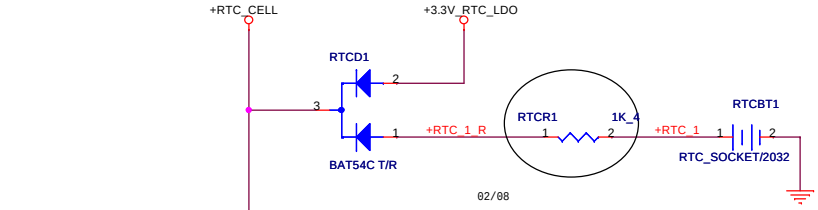


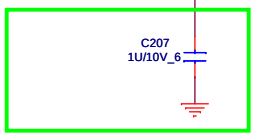
Change R351,R399,R378,R358 from 15 ohm to 0 ohm

Change U21 from AKE39FP0Z02 to AKE391P0N00

01/25 change to QPN: DFHS02FS033

RTC BATTERY





C1042:CH5101K9B01->CH5102Z3919

Change RTCBT1 DFHD02MS784->DFHS02FS033

02/09 Change RTCBT1 DFHS02FS033->DFHS02FS027

2/16 coin battary P/N AHL03003002

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PROJECT : R05		
Size	Document Number: FLASH / RTC	Rev: 2A
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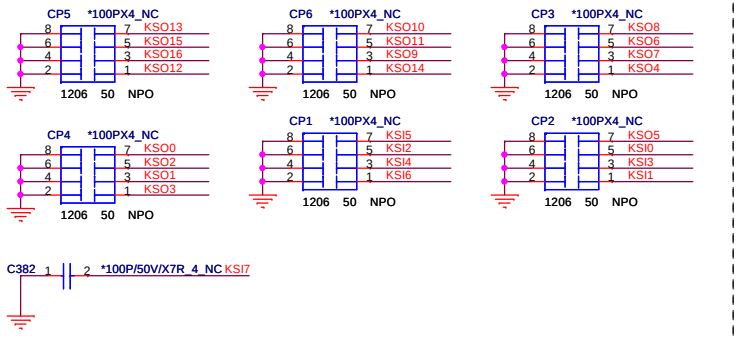
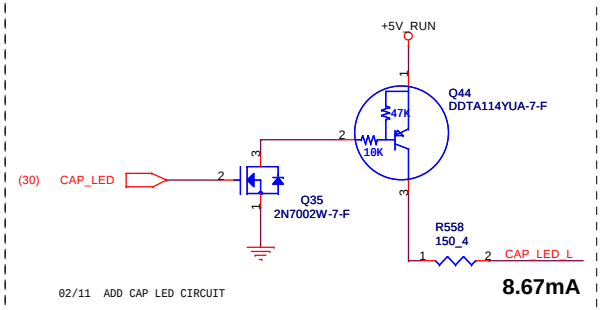
KEYBOARD CONNECTOR

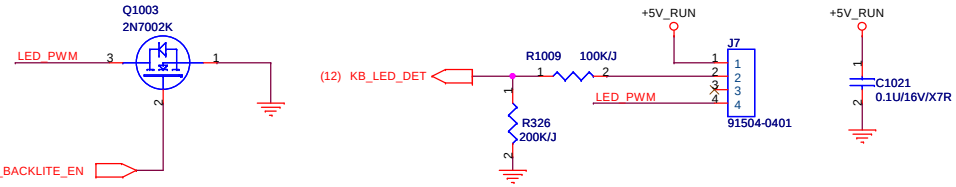
03/30 Change CP1,CP2,CP3,CP4,CP5,CP6,C382 from Pop to Depop



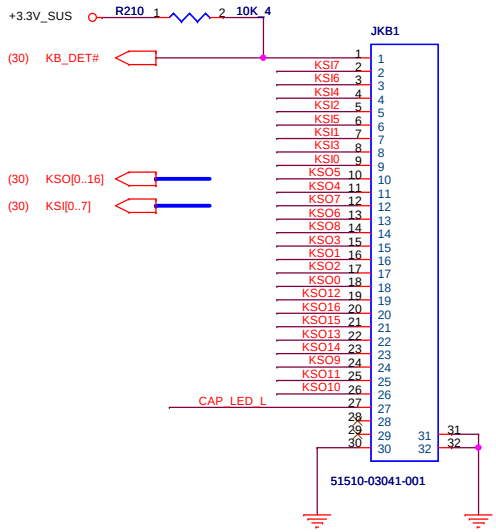


Add KB_BACKLITE_EN 1/11

Key board illumination **From GM6C**



KEYBOARD CONNECTOR



Change CON6 PN DFFC32FR005 to DFFC30FR058

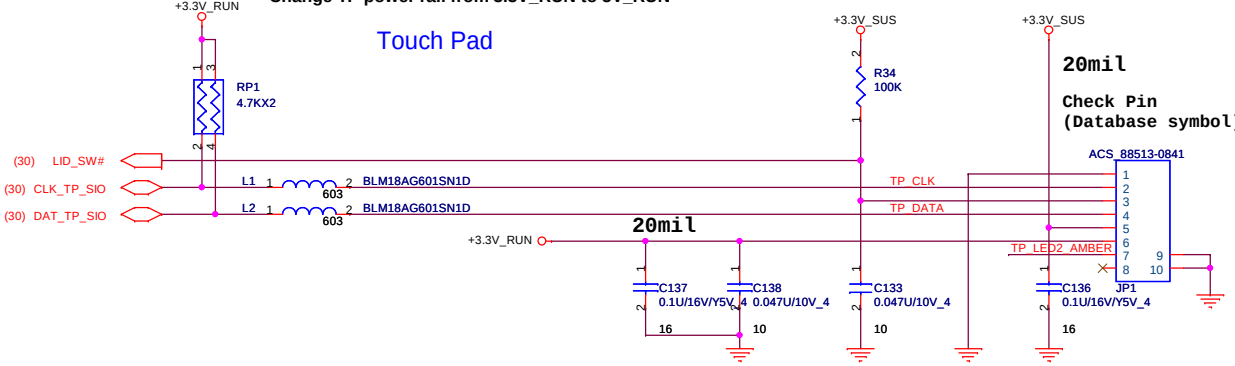
From GM7

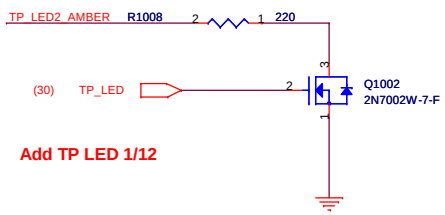
Change TP power rail from 5V_RUN to 3.3V_RUN

Change TP power rail from 3.3V_RUN to 5V_RUN

Change JP2 DFFC06FR012->DFFC12FR011(CIS SYMBOL ERROR)

Touch Pad





Add TP LED 1/12

02/10 change JP1 symbol

Change JP2 from DFFC12FR011 to DFFC06FR022

Change TP footprint from 88502-06XX-6P-L-NB1 to 88502-06XX-6P-L-SMT

Change JP1 footprint to 88513-0801-8p-l
from 88502-06XX-6P-L-SMT 1/11

Change JP1 part number to DFFC08FR016
from DFFC06FR022 1/11

Quanta Computer Inc.

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Size	Document Number	Rev
	TP / KB	2A
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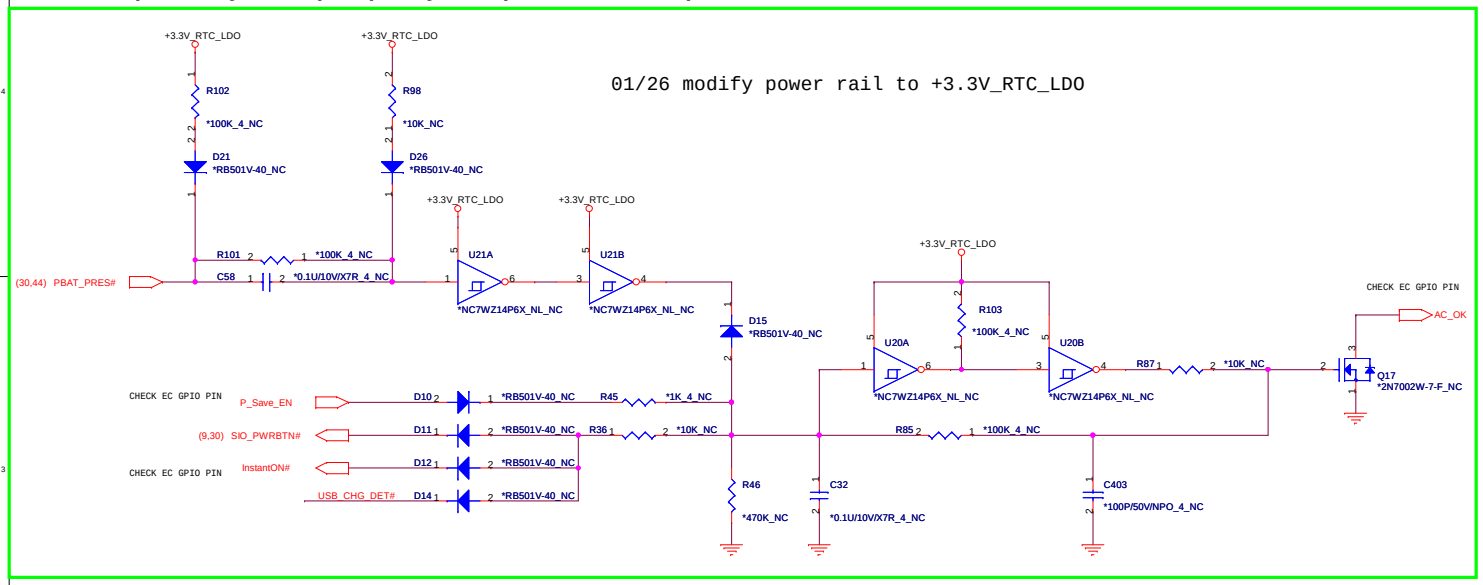
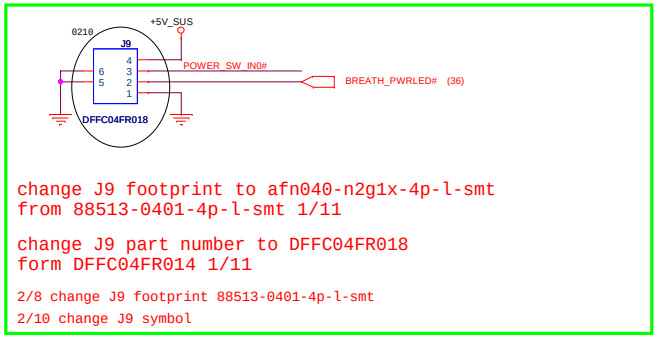
01/25 Deep standby mode (Temporary name) is to reduce S5 power when AC is inserted

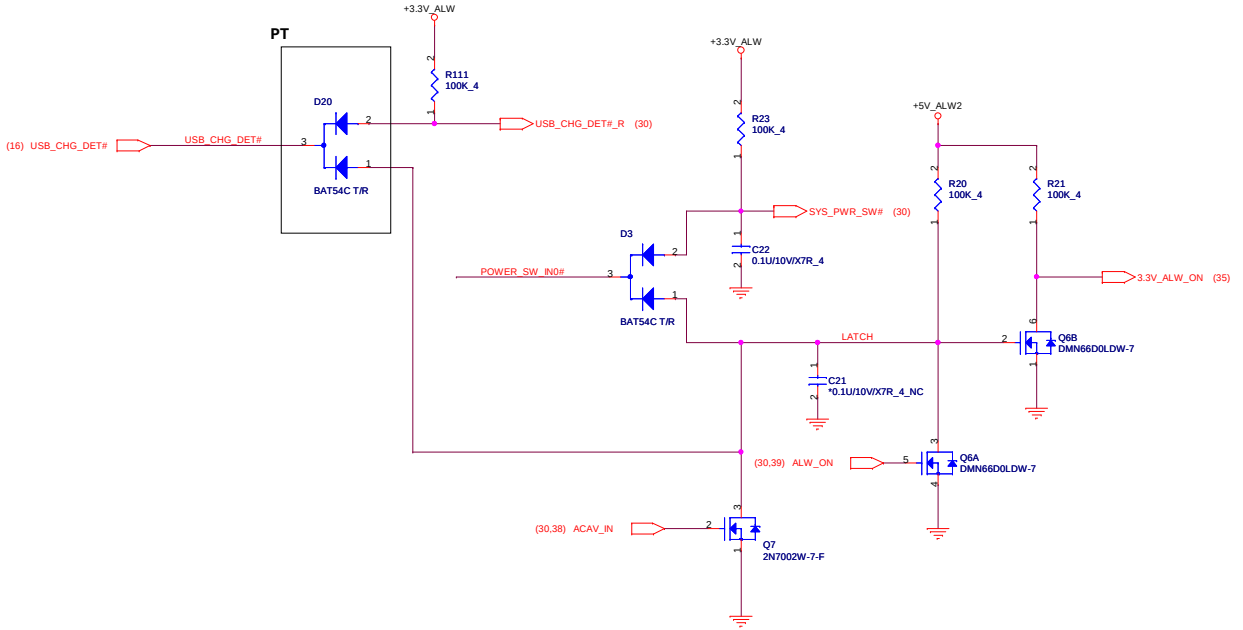


Power button Board

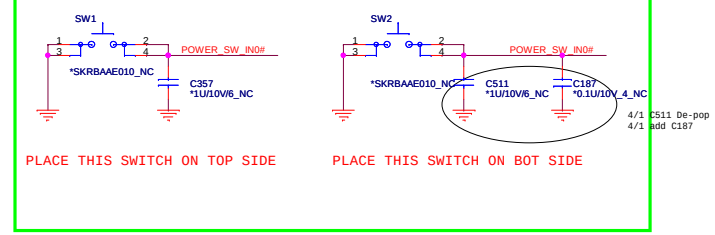
Add PWR Board CONN

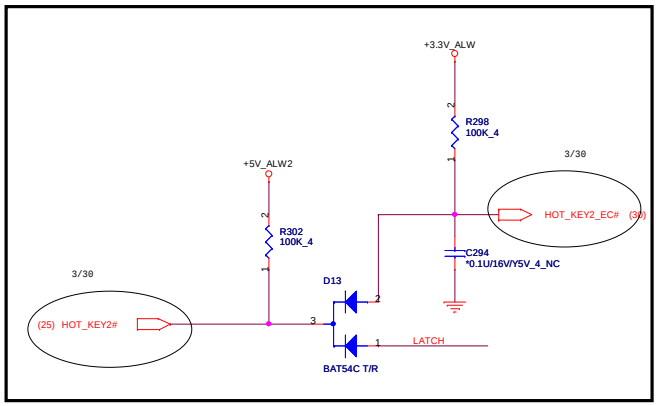


3VALW ON POWER LOGIC



Debug PWR SW





Quanta Computer Inc.		
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Size	Document Number	Rev
	PWR SW/LED	2A
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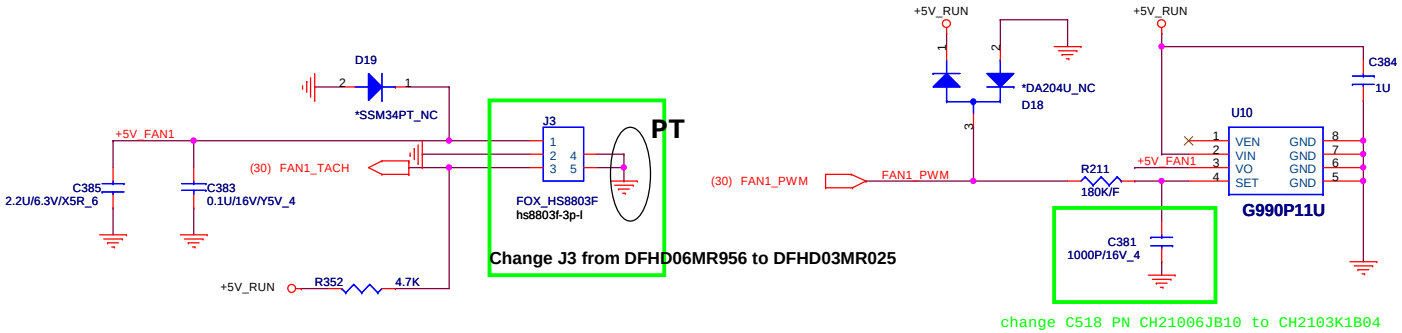
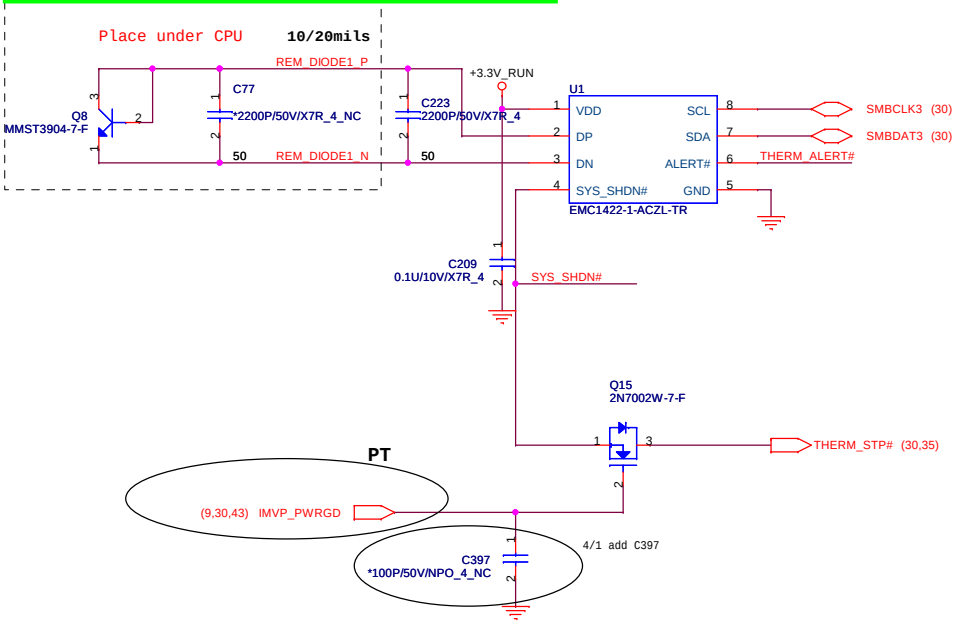
FAN CONN



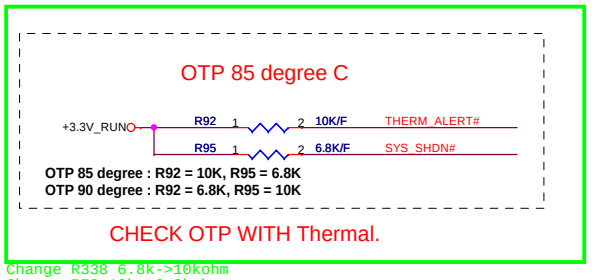
change C518 PN CH21006JB10 to CH2103K1B04

THERMAL IC

1.Place C223 close to EMC1422-U1
2.Place C77 to be close to Q8
Total capacitance between D+/D- is 2200pF(max)
if use 2200pF for C223, then C77 should be dummy



SYS_SHD# / ALERT#	4.7K	6.8K	10K	15K	22K	33K
4.7K	77'C	83'C	89'C	95'C	101'C	107'C
6.8K	78'C	84'C	90'C	96'C	102'C	108'C
10K	79'C	85'C	91'C	97'C	103'C	109'C
15K	80'C	86'C	92'C	98'C	104'C	110'C
22K	81'C	87'C	93'C	99'C	105'C	111'C
33K	82'C	88'C	94'C	100'C	106'C	112'C



Change R338 6.8k->10kohm
Change R78 10k->6.8kohm

Quanta Computer Inc.
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Size	Document Number	Rev
	FAN & THERMAL	2A

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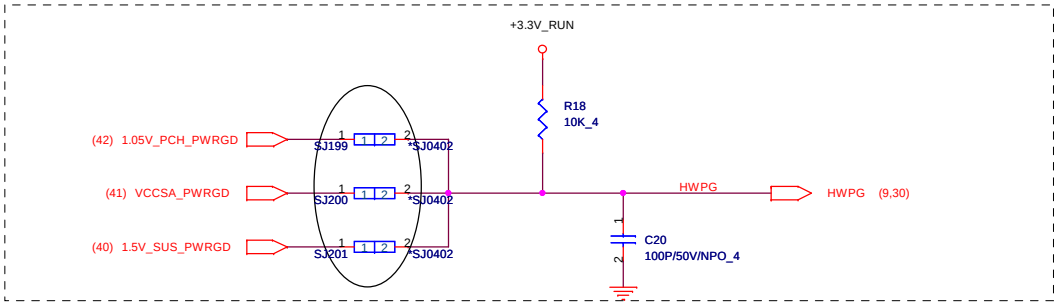
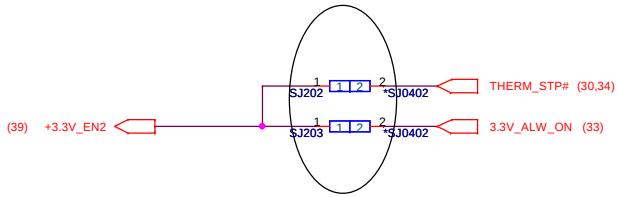
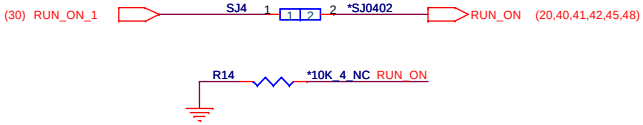
Change to +3.3V_RUN or confirm with EC do not latch HWPG before RUN_ON sending



R387,R364,R17 change to short jump 5/18



R19,R22 change to short jump 5/18



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PROJECT : R05		
Size	Document Number: System Reset Circuit	Rev: 2A
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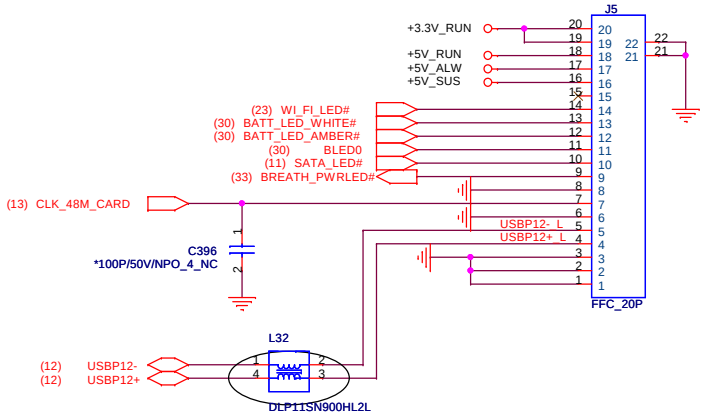
Card Reader schematic Remove to IO Board

CR Board CONN



Add R1037,R1038 for EMI request
change R1037,R1038 to short jump 5/18
change short jump to choke 5/19

Quanta Computer Inc.
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Size	Document Number	Rev
	CardReader	2A

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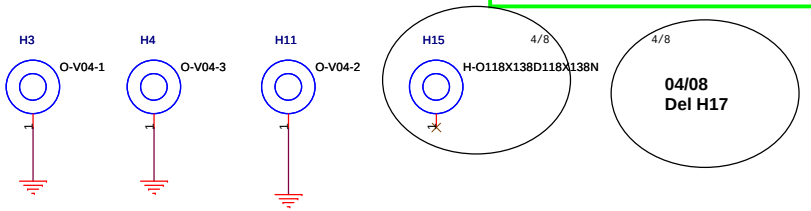
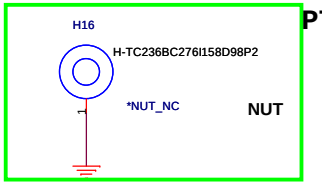
H15、H18　封裝更新為 from H-C276D94P2 to H-TC276BC374I158D118P2
H2 、H6　封裝更新為 from H-TC276BC374I158D118P2 to H-TC355BC276I158D118P2
H5　　封裝更新為 from H-TC276BC374I158D118P2 to H-TC276BC355I158D118P2



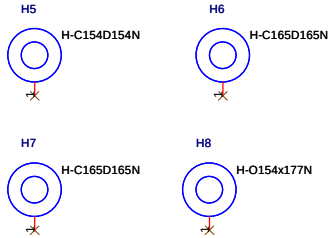


PT

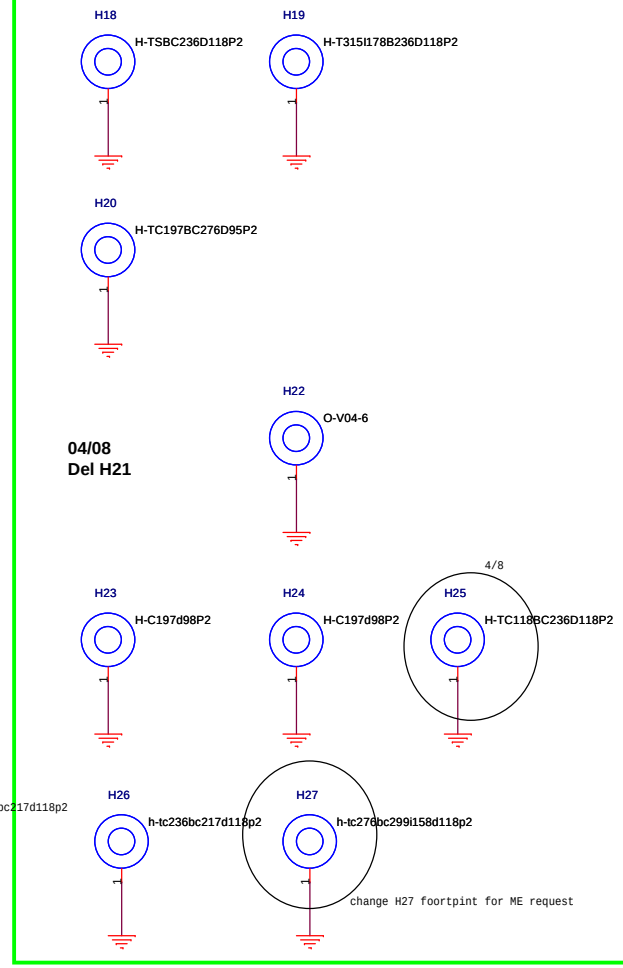
02/08
Del H2 H9 H1 H10 H14 H12　 H13 H28

02/14
Del H12

02/11
DEL H5,H6.H7.H8 contact to GND



01/26 for layout house 煜元



Quanta Computer Inc.
PROJECT : R05

Size	Document Number	Rev
	SCREW PAD	2A
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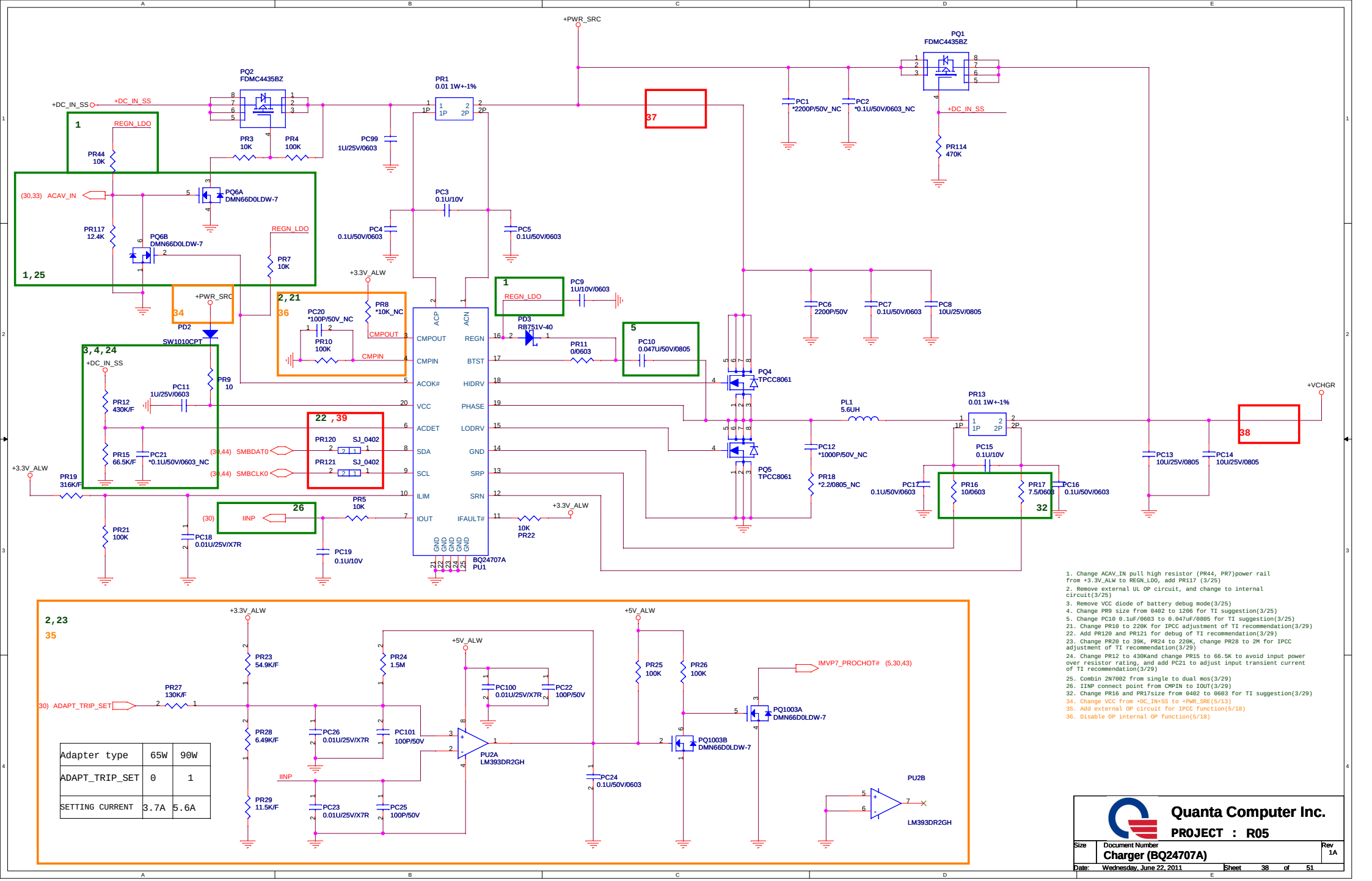

Adapter type	65W	90W
ADAPT_TRIP_SET	0	1
SETTING CURRENT	3.7A	5.6A

1. Change ACAV_IN pull high resistor (PR44, PR7)power rail from +3.3V_ALW to REGN_LDO, add PR117 (3/25)
2. Remove external UL OP circuit, and change to internal circuit(3/25)
3. Remove VCC diode of battery debug mode(3/25)
4. Change PR9 size from 0402 to 1206 for TI suggestion(3/25)
5. Change PC10 0.1uF/0603 to 0.047uF/0805 for TI suggestion(3/25)
21. Change PR10 to 220K for IPCC adjustment of TI recommendation(3/29)
22. Add PR120 and PR121 for debug of TI recommendation(3/29)
23. Change PR20 to 30K, PR24 to 220K, change PR28 to 2M for IPCC adjustment of TI recommendation(3/29)
24. Change PR12 to 430Kand change PR15 to 66.5K to avoid input power over resistor rating, and add PC21 to adjust input transient current of TI recommendation(3/29)
25. Combin 2N7002 from single to dual mos(3/29)
26. IINP connect point from CMPIN to IOUT(3/29)
32. Change PR16 and PR17size from 0402 to 0603 for TI suggestion(3/29)
34. Change VCC from +DC_IN+SS to +PWR_SRE(5/13)
35. Add external OP circuit for IPCC function(5/18)
36. Disable OP internal OP function(5/18)

Quanta Computer Inc.
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Size	Document Number	Rev
	Charger (BQ24707A)	1A

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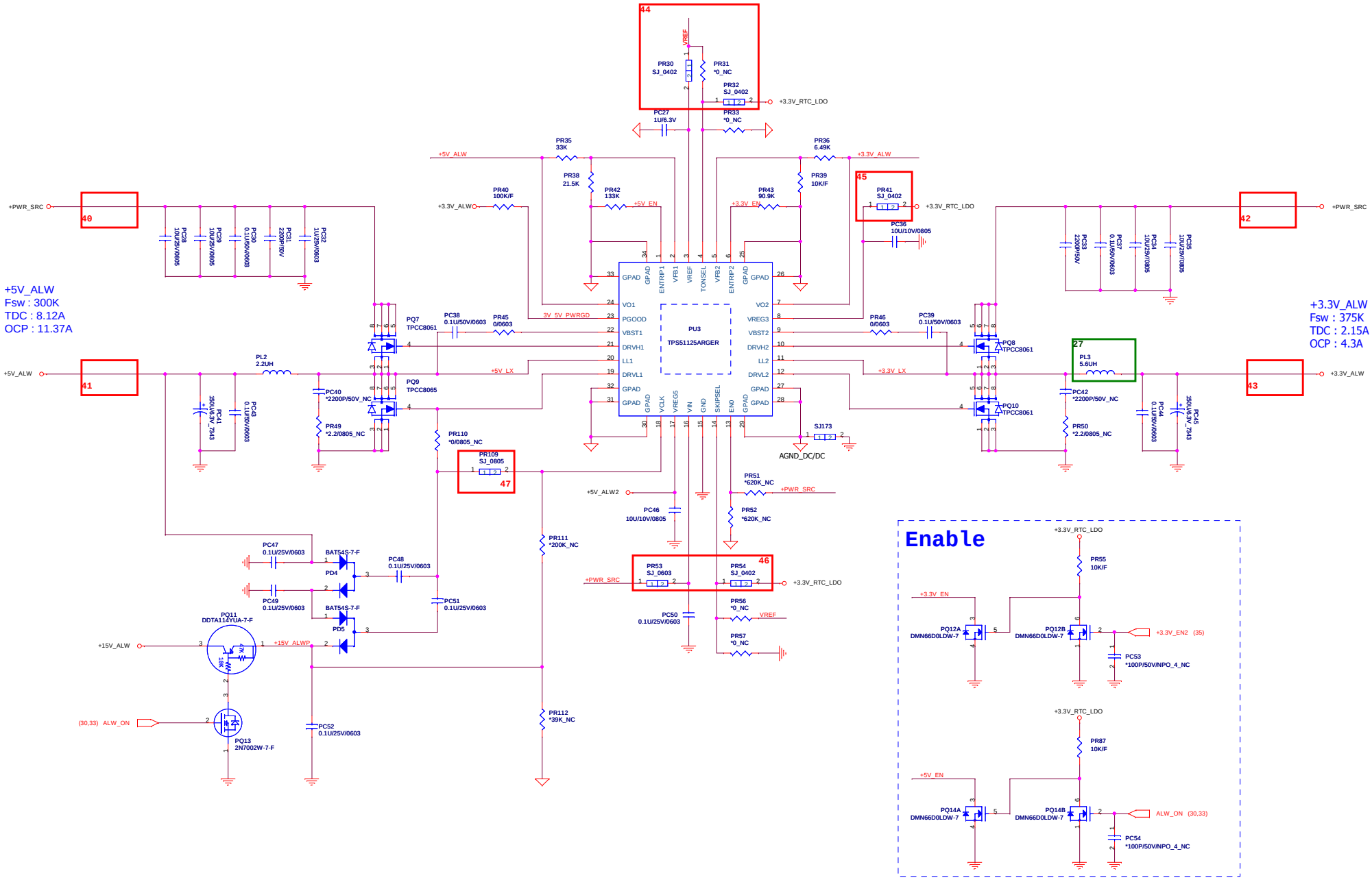
+5V_ALW
Fsw : 300K
TDC : 8.12A
OCP : 11.37A
+3.3V_ALW
Fsw : 375K
TDC : 2.15A
OCP : 4.3A
PU3
TPS51125ARGER
AGND_DC/DC
Enable
+3.3V_EN2 (35)
ALW_ON (30,33)
27. Change PL3 to 5.6uH to reduce ripple current(3/29)
Quanta Computer Inc.
PROJECT : R05
3.3V_ALW/5V_ALW(TPS51125ARGER)
Wednesday, June 22, 2011
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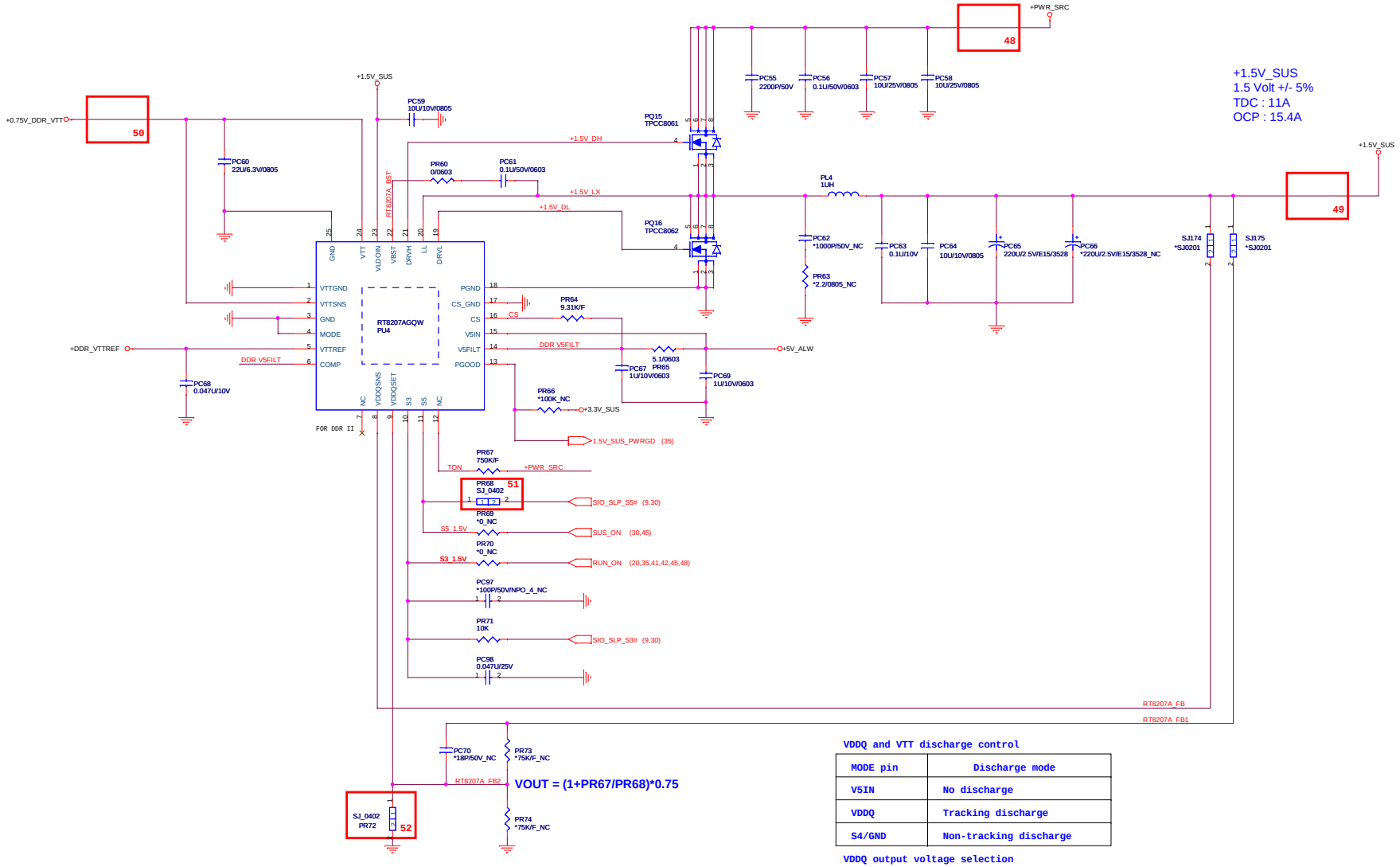

VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

VDDQ output voltage selection

VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

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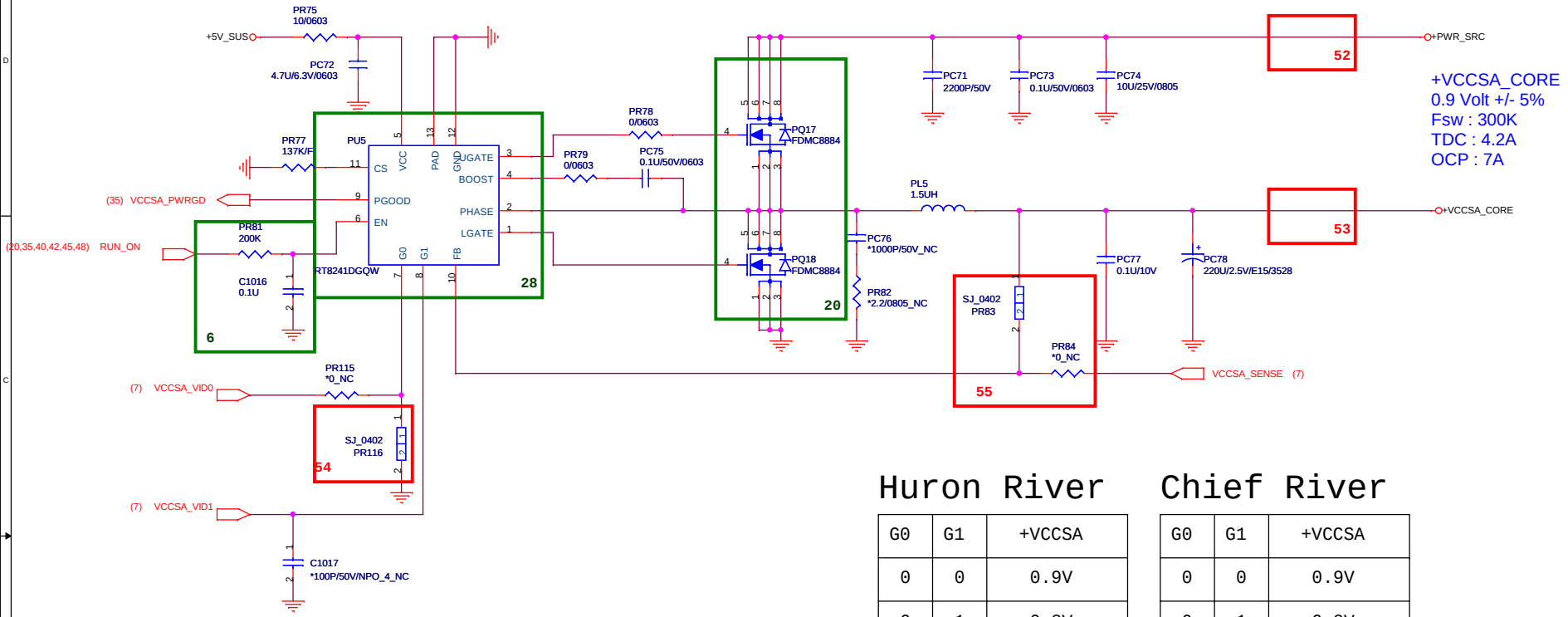

+VCCSA_CORE
0.9 Volt +/- 5%
Fsw : 300K
TDC : 4.2A
OCP : 7A

Huron River

G0	G1	+VCCSA
0	0	0.9V
0	1	0.8V

Chief River

G0	G1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

6. Change for EE sequence adjustment(3/25)
7. Change FB route from CPU side to PWM side(3/25)
20. Change H/S and L/S from TPCC8061 to FDMC8884(3/25)
28. change PU5 footprint to wqfn12-2x2-4-13p-SMT(3/29)

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	VCCSA_CORE(RT8241DGQW)	1A

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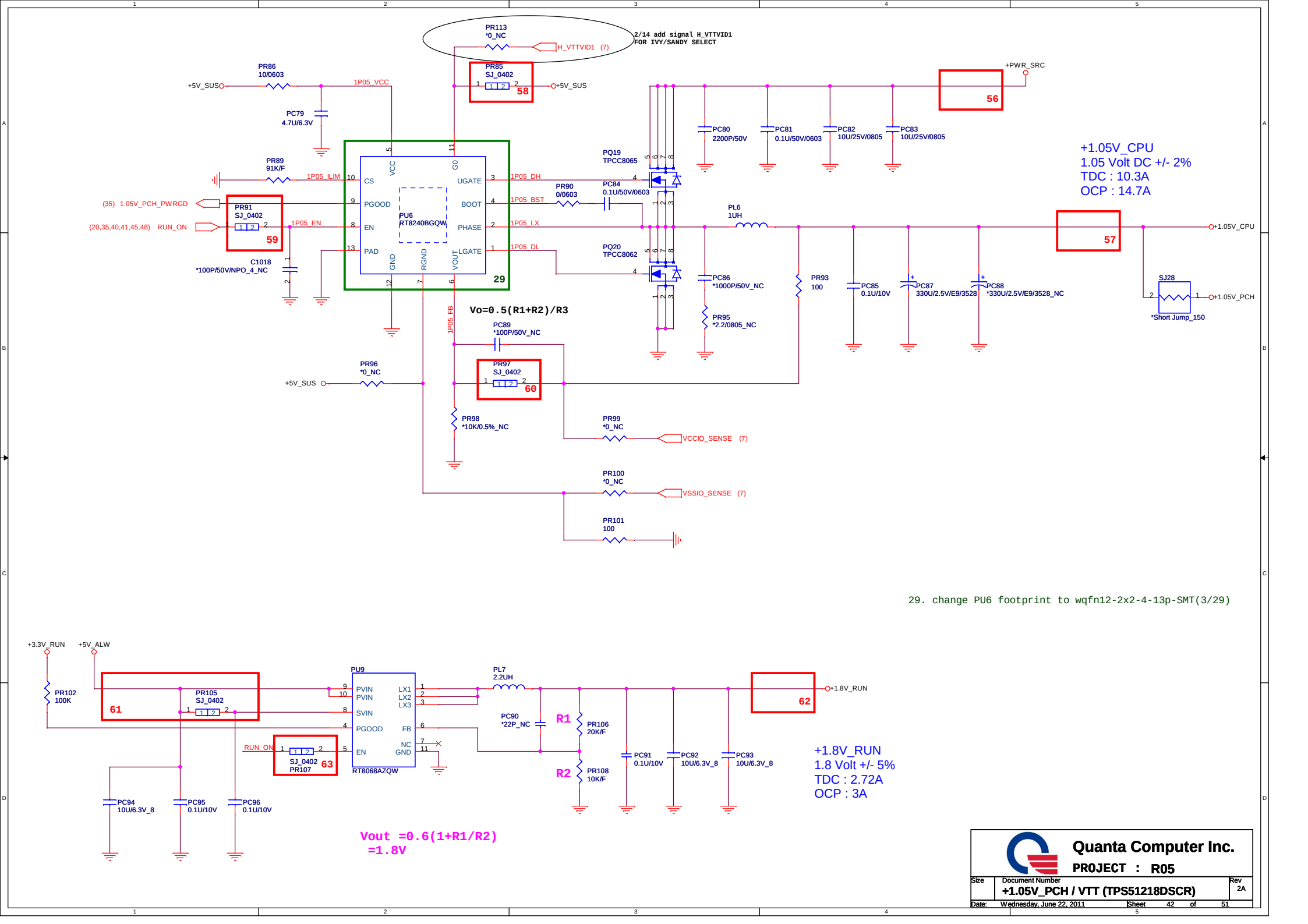
PR113
*0_NC
H_VTTVID1 (7)
2/14 add signal H_VTTVID1
FOR IVY/SANDY SELECT
PR86
10/0603
+5V_SUS
1P05_VCC
PR85
SJ_0402
58
+5V_SUS
+PWR_SRC
56
PC79
4.7U/6.3V
PC80
2200P/50V
PC81
0.1U/50V/0603
PC82
10U/25V/0805
PC83
10U/25V/0805
PR89
91K/F
1P05_ILIM
PU6
RT8240BGQW
VCC
G0
CS
UGATE
PGOOD
BOOT
EN
PHASE
PAD
LGATE
GND
RGND
VOUT
29
PQ19
TPCC8065
1P05_DH
PR90
0/0603
PC84
0.1U/50V/0603
1P05_BST
1P05_LX
PQ20
TPCC8062
1P05_DL
(35) 1.05V_PCH_PWRGD
(20,35,40,41,45,48) RUN_ON
PR91
SJ_0402
59
1P05_EN
C1018
*100P/50V/NPO_4_NC
PL6
1UH
PC86
*1000P/50V_NC
PR95
*2.2/0805_NC
PR93
100
PC85
0.1U/10V
PC87
330U/2.5V/E9/3528
PC88
*330U/2.5V/E9/3528_NC
57
+1.05V_CPU
SJ28
*Short Jump_150
+1.05V_PCH
+1.05V_CPU
1.05 Volt DC +/- 2%
TDC : 10.3A
OCP : 14.7A
Vo=0.5(R1+R2)/R3
1P05_FB
PC89
*100P/50V_NC
PR96
*0_NC
+5V_SUS
PR97
SJ_0402
60
PR98
*10K/0.5%_NC
PR99
*0_NC
VCCIO_SENSE (7)
PR100
*0_NC
VSSIO_SENSE (7)
PR101
100
29. change PU6 footprint to wqfn12-2x2-4-13p-SMT(3/29)
+3.3V_RUN
+5V_ALW
PR102
100K
PR105
SJ_0402
61
PU9
PVIN
PVIN
SVIN
PGOOD
EN
LX1
LX2
LX3
FB
NC
GND
RT8068AZQW
PL7
2.2UH
62
+1.8V_RUN
PC90
*22P_NC
R1
PR106
20K/F
R2
PR108
10K/F
PC91
0.1U/10V
PC92
10U/6.3V_8
PC93
10U/6.3V_8
RUN_ON
SJ_0402
PR107
63
PC94
10U/6.3V_8
PC95
0.1U/10V
PC96
0.1U/10V
+1.8V_RUN
1.8 Volt +/- 5%
TDC : 2.72A
OCP : 3A
Vout =0.6(1+R1/R2)
=1.8V
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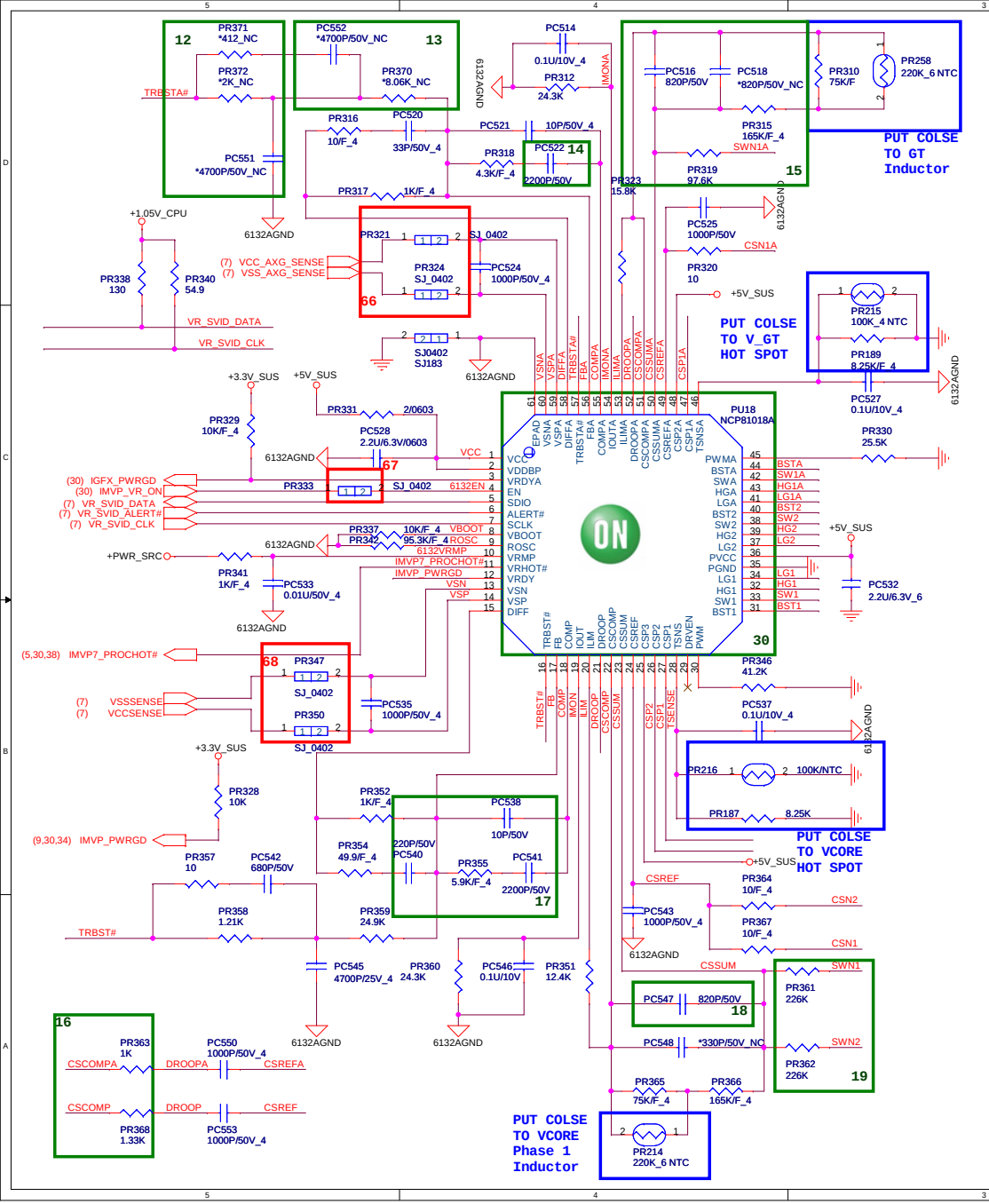
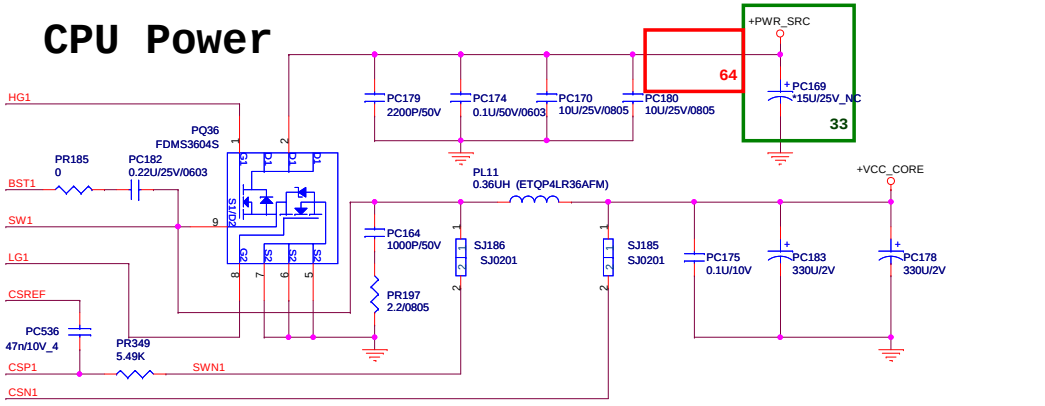
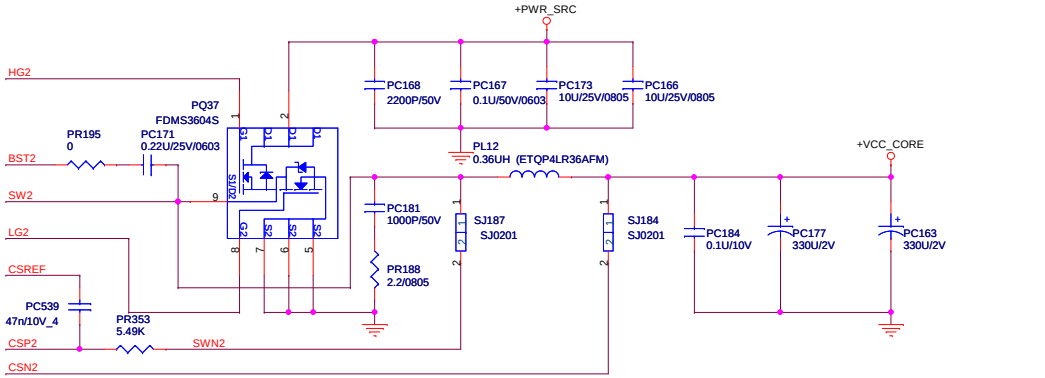
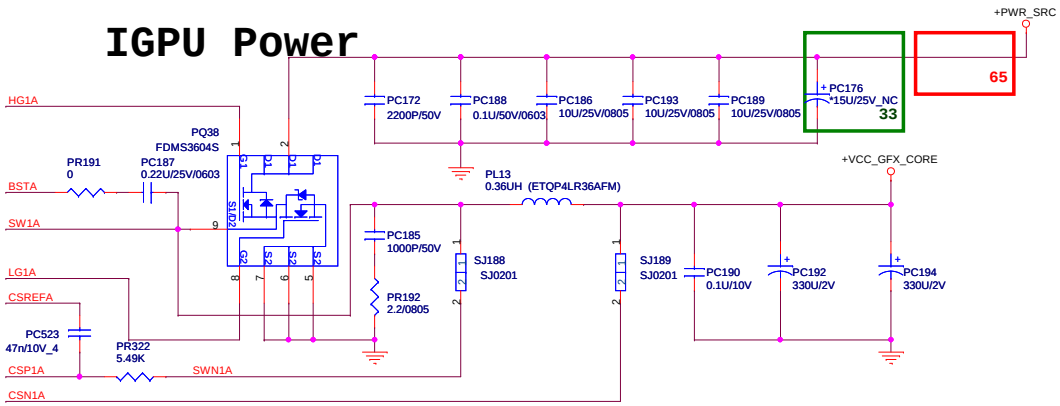


CPU Power





IGPU Power



12~19. For load line and transient adjustment

30. change PU18 P/N to NCP6132A and
change footprint to qfn60-7x7-4-61p-smt(3/29)

33. Pop 15U/25V AL cap for acoustic test.(3/29)

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	CPU_CORE (NCP6132A)	1A
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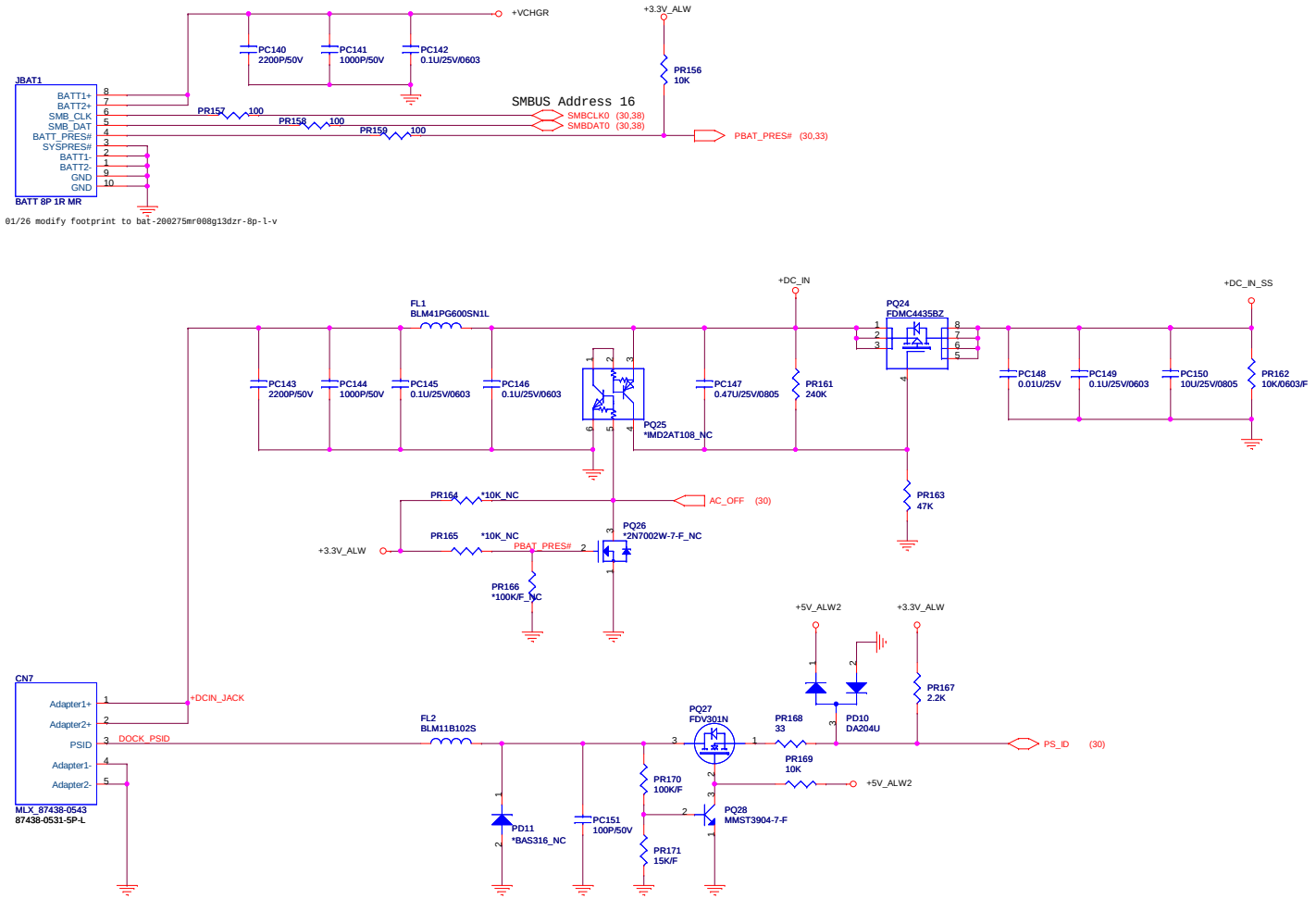

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Size	Document Number: DCIN.BATT CONNECTOR	Rev: 2A
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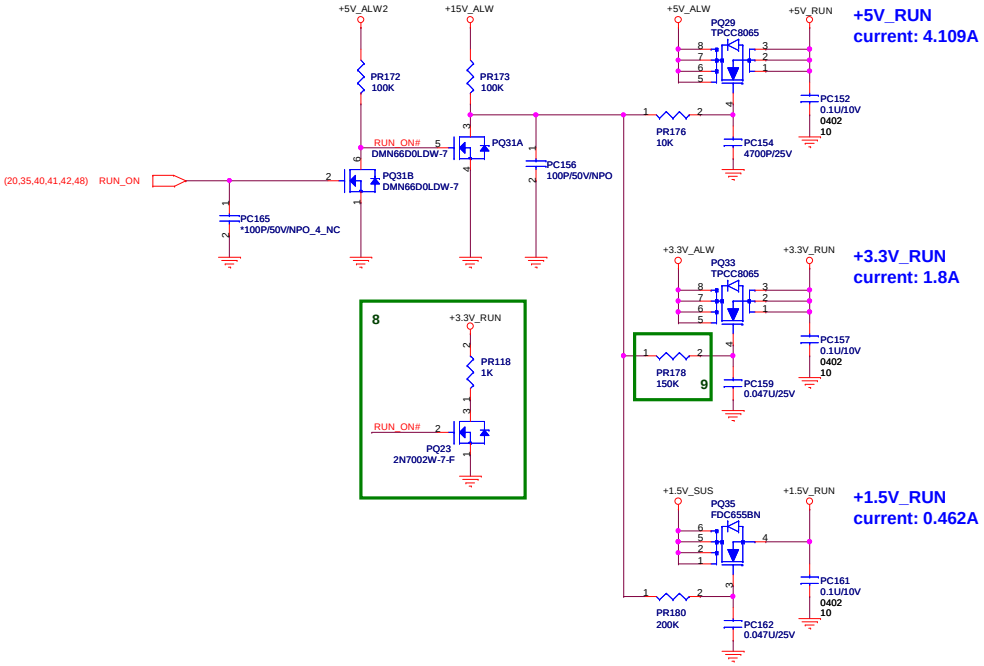

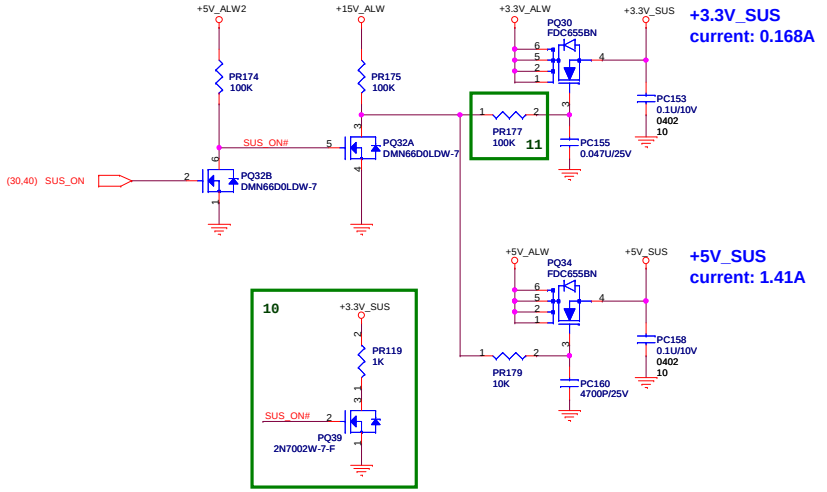

8.9.10.11. Change for EE sequence adjustment(3/25)

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	DA0SS7MBCA0	1A
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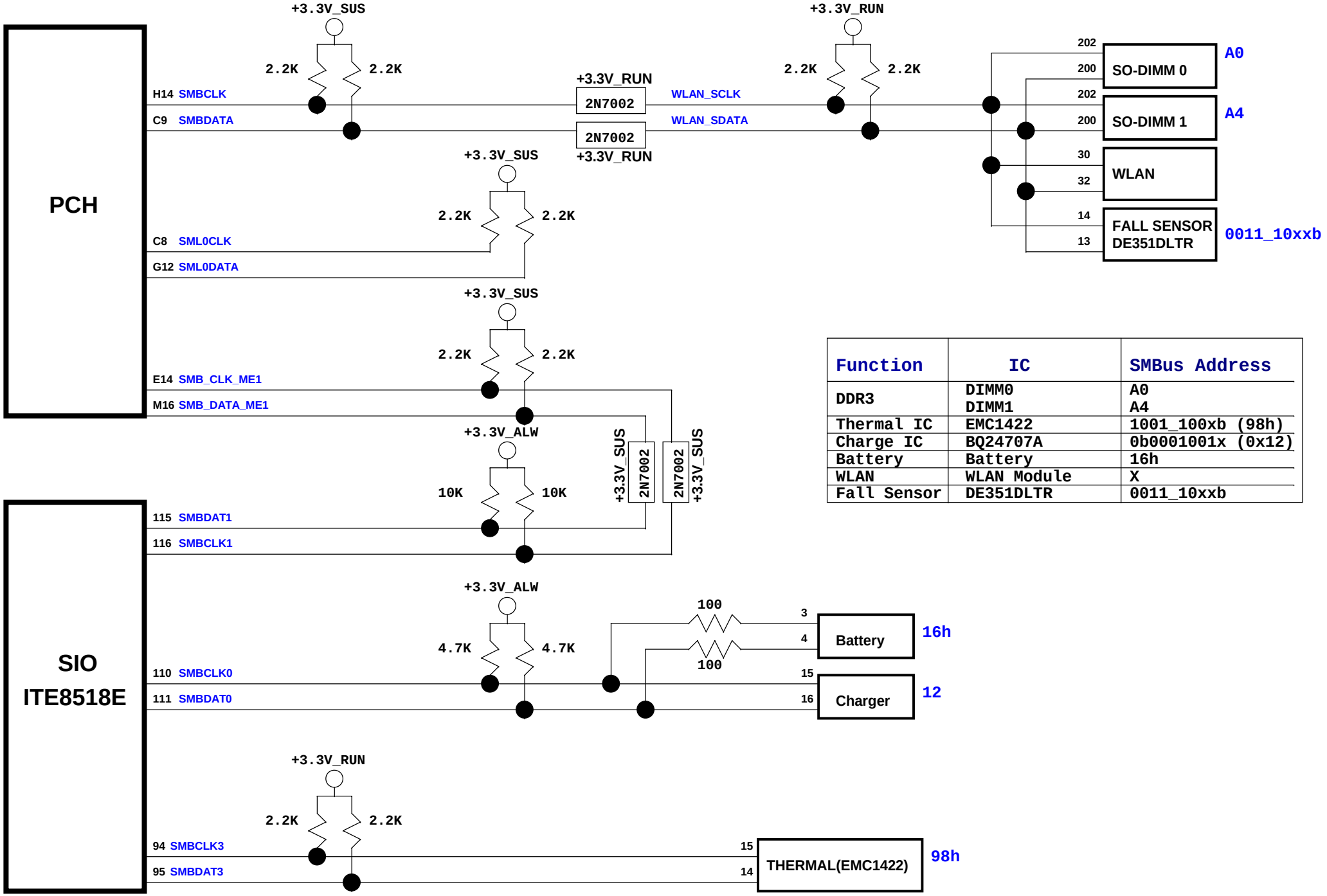

Function	IC	SMBus Address
DDR3	DIMM0 DIMM1	A0 A4
Thermal IC	EMC1422	1001_100xb (98h)
Charge IC	BQ24707A	0b0001001x (0x12)
Battery	Battery	16h
WLAN	WLAN Module	X
Fall Sensor	DE351DLTR	0011_10xxb

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	SMBUS	2A

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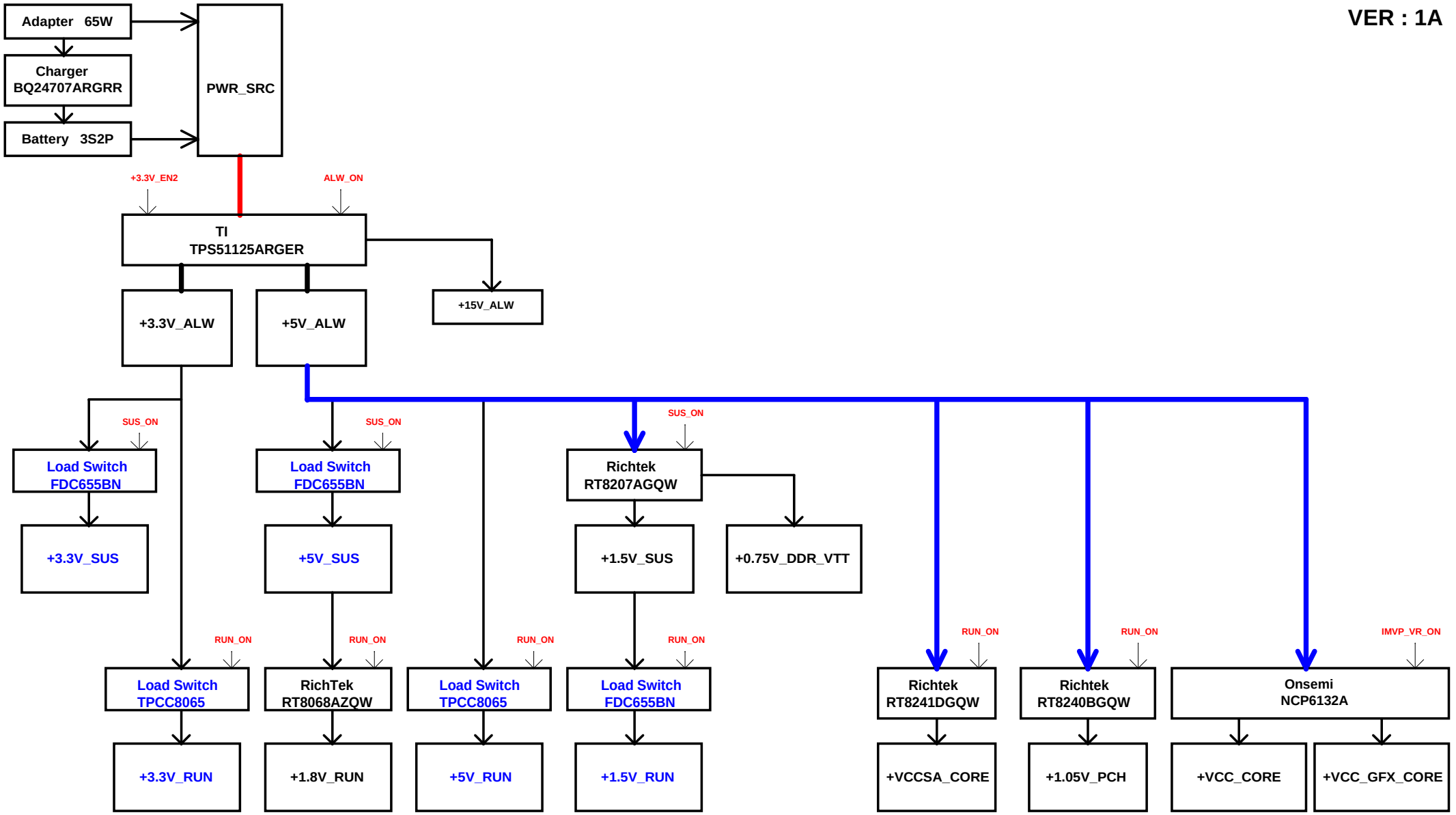

Quanta Computer Inc.

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	Power Block Diagram	2A

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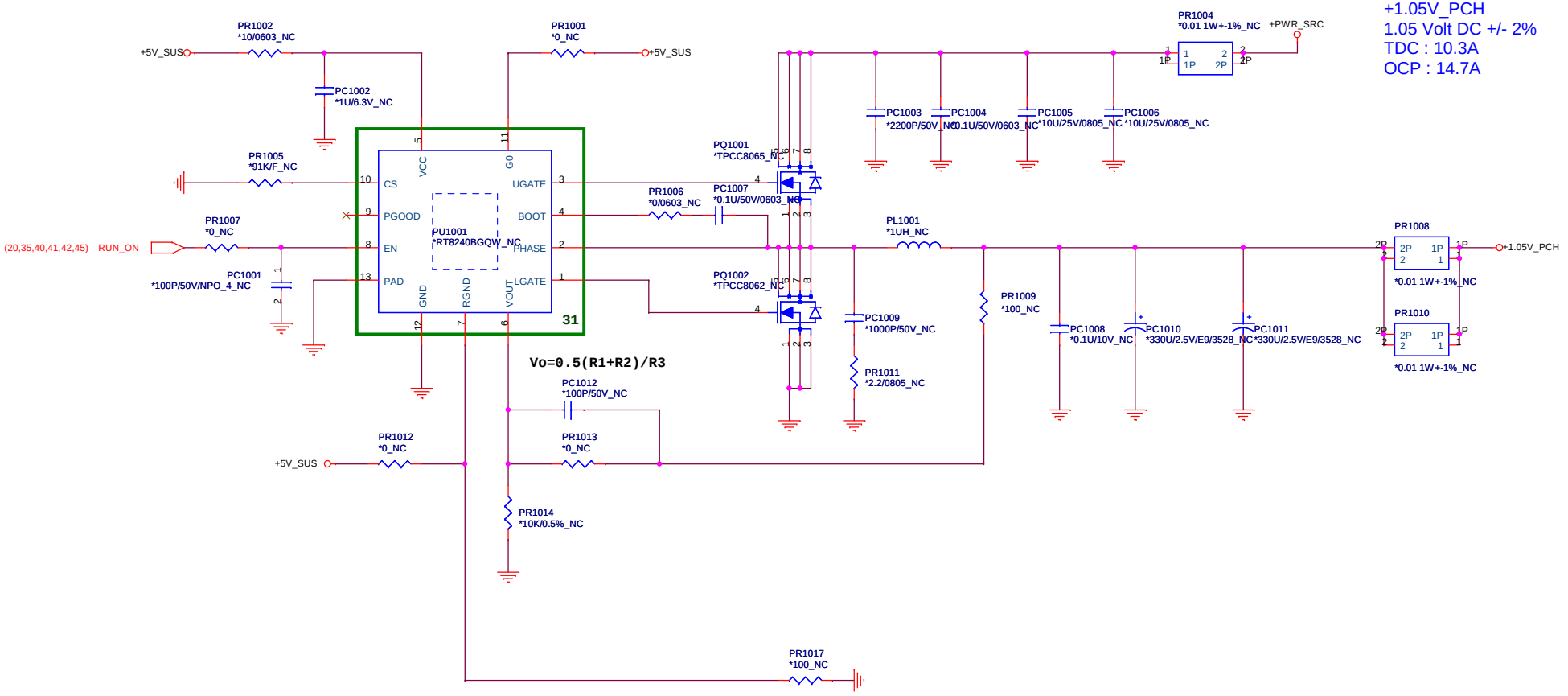

31. change PU6 footprint to wqfn12-2x2-4-13p-SMT(3/29)

Reserve for Ivy bridge

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