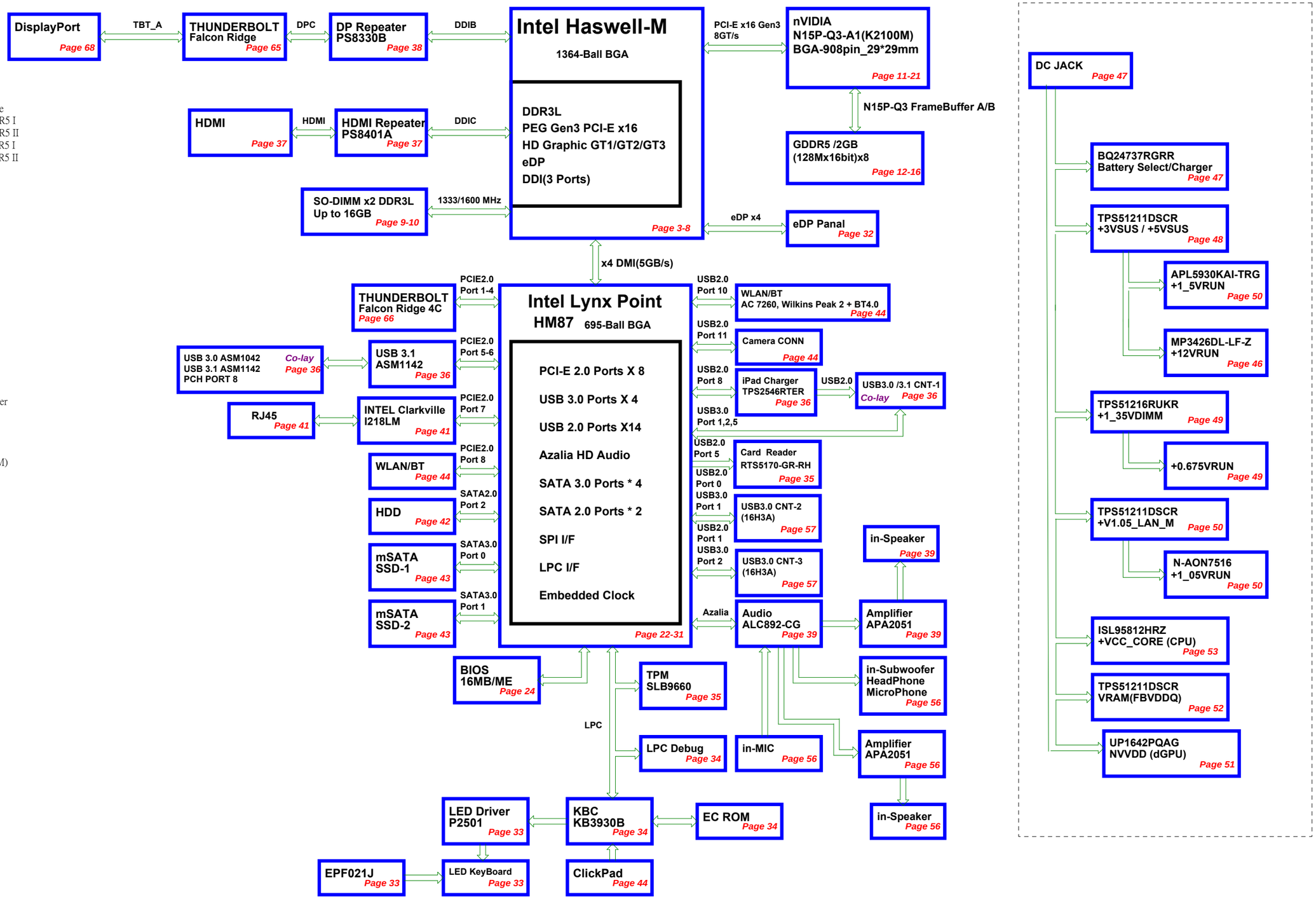
MS-16H3 Ver:0A

Wednesday, June 25, 2014

Shark Bay Mobile



msi	MICRO-STAR INT'L CO.,LTD.		
Title	Block Diagram		
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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

Voltage	Description	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
+5VALW	5.0V always on power rail	PWR_SRC
+3VALW	3.3V always on power rail	PWR_SRC
+5VSUS	5.0V power rail	SUS_ON
+3VSUS	3.3V power rail	SUS_ON
+1_35VDIMM	1.35V DDR3L power rail (off in S4-S5)	DIMM_ON
+0_675VRUN	0.675V DDR3L Termination voltage (off in S3-S5)	PM_SLP_S3#
+5VRUN	5.0V switched power rail (off in S3-S5)	RUN_ON
+3VRUN	3.3V switched power rail (off in S3-S5 / M0)	RUN_ON
+1_5VRUN	1.5V switched power rail (off in S3-S5)	RUN_ON
+VCC_CORE	1.8V Core Voltage for Processor	EC_ALLSYSPG
+1_05VRUN	1.05V rail for Processor	RUN_ON
NVVDD	V Core Voltage for nVIDIA dGPU	NVVDD_EN
+3V3_NV	3.3V PEX power rail (off in Optimus OFF)	DGPU_PWR_EN#
FBVDDQ	1.35V FB / GDDR5 power rail (off in Optimus OFF)	FBVDDQ_ON
PEX_VDD	1.05V PLL power rail (off in Optimus OFF)	NVVDD_EN

POWER STATES

SIGNAL / STATE	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALW	+*VSUS	+*VRUN	Clocks
S0(Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3(Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Note : WHEN AC MODE , System turn on and +V*SUS always keep high

Net Naming Conventions

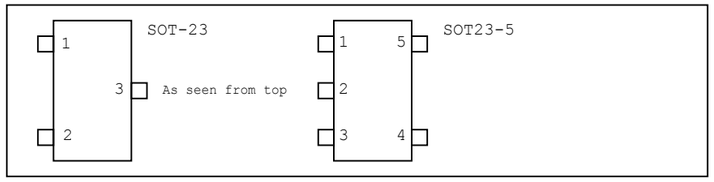
Suffix

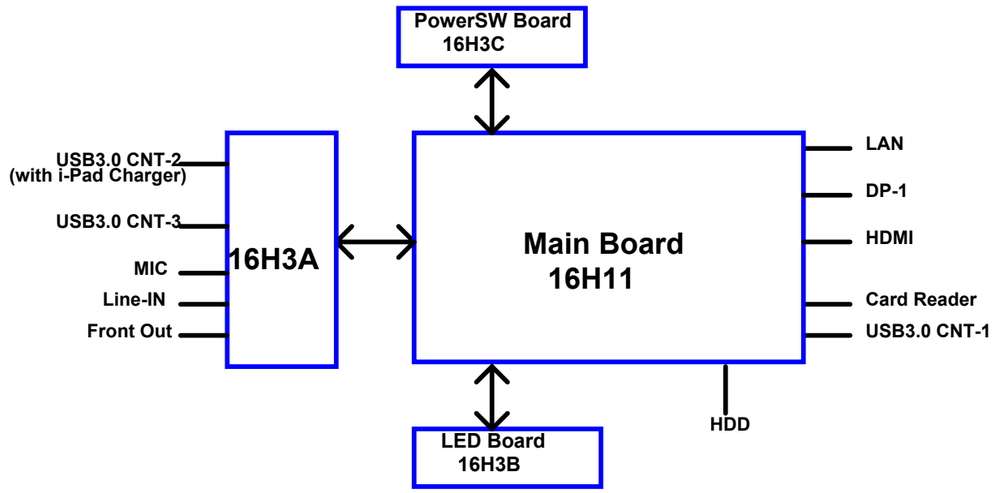
\# = Active Low Signal

Prefix

H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)
FB = DGPU VRAM
VIAxxx = Like Test Point, but using VIA.

PCB Footprints





msi MICRO-STAR INT'L CO.,LTD.			
Title: Platform			
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Haswell (DMI,PEG,FDI)

PEG_RCOMP
Width:12 mils
Spacing:15 mils
Length:400 mils

U1A — HASWELL_BGA_E

25 DMI_TXN0	AB2	DMI_RXN0	DMI
25 DMI_TXN1	AB3	DMI_RXN1	
25 DMI_TXN2	AC3	DMI_RXN2	
25 DMI_TXN3	AC1	DMI_RXN3	
25 DMI_TXP0	AB1	DMI_RXP0	
25 DMI_TXP1	AB4	DMI_RXP1	
25 DMI_TXP2	AC4	DMI_RXP2	
25 DMI_TXP3	AC2	DMI_RXP3	
25 DMI_RXN0	AF2	DMI_TXN0	
25 DMI_RXN1	AF4	DMI_TXN1	
25 DMI_RXN2	AG4	DMI_TXN2	
25 DMI_RXN3	AG2	DMI_TXN3	
25 DMI_RXP0	AF1	DMI_TXP0	
25 DMI_RXP1	AF3	DMI_TXP1	
25 DMI_RXP2	AG3	DMI_TXP2	
25 DMI_RXP3	AG1	DMI_TXP3	
25 FDI_CSYNC	F11	FDI_CSYNC	FDI
25 FDI_INT	F12	DISP_INT	

PEG_RCOMP	AH6	PEG_COMP R252 24.9R1%0402	+VCCIOA_OUT
PEG_RXN0	E10	PEG_RXN0	11
PEG_RXN1	C10	PEG_RXN1	11
PEG_RXN2	B10	PEG_RXN2	11
PEG_RXN3	E9	PEG_RXN3	11
PEG_RXN4	D9	PEG_RXN4	11
PEG_RXN5	B9	PEG_RXN5	11
PEG_RXN6	L5	PEG_RXN6	11
PEG_RXN7	L2	PEG_RXN7	11
PEG_RXN8	M4	PEG_RXN8	11
PEG_RXN9	L4	PEG_RXN9	11
PEG_RXN10	M2	PEG_RXN10	11
PEG_RXN11	V5	PEG_RXN11	11
PEG_RXN12	V4	PEG_RXN12	11
PEG_RXN13	V1	PEG_RXN13	11
PEG_RXN14	Y3	PEG_RXN14	11
PEG_RXN15	Y2	PEG_RXN15	11
PEG_RXP0	F10	PEG_RXP0	11
PEG_RXP1	D10	PEG_RXP1	11
PEG_RXP2	A10	PEG_RXP2	11
PEG_RXP3	F9	PEG_RXP3	11
PEG_RXP4	C9	PEG_RXP4	11
PEG_RXP5	A9	PEG_RXP5	11
PEG_RXP6	M5	PEG_RXP6	11
PEG_RXP7	L1	PEG_RXP7	11
PEG_RXP8	M3	PEG_RXP8	11
PEG_RXP9	L3	PEG_RXP9	11
PEG_RXP10	M1	PEG_RXP10	11
PEG_RXP11	Y5	PEG_RXP11	11
PEG_RXP12	V3	PEG_RXP12	11
PEG_RXP13	V2	PEG_RXP13	11
PEG_RXP14	Y4	PEG_RXP14	11
PEG_RXP15	Y1	PEG_RXP15	11
PEG_TXN0	B6	PEG_TXN0	11
PEG_TXN1	C5	PEG_TXN1	11
PEG_TXN2	E6	PEG_TXN2	11
PEG_TXN3	D4	PEG_TXN3	11
PEG_TXN4	G4	PEG_TXN4	11
PEG_TXN5	E3	PEG_TXN5	11
PEG_TXN6	J5	PEG_TXN6	11
PEG_TXN7	G3	PEG_TXN7	11
PEG_TXN8	J3	PEG_TXN8	11
PEG_TXN9	J2	PEG_TXN9	11
PEG_TXN10	T6	PEG_TXN10	11
PEG_TXN11	R6	PEG_TXN11	11
PEG_TXN12	R2	PEG_TXN12	11
PEG_TXN13	R4	PEG_TXN13	11
PEG_TXN14	T4	PEG_TXN14	11
PEG_TXN15	T1	PEG_TXN15	11
PEG_TXP0	C6	PEG_TXP0	11
PEG_TXP1	B5	PEG_TXP1	11
PEG_TXP2	D6	PEG_TXP2	11
PEG_TXP3	E4	PEG_TXP3	11
PEG_TXP4	G5	PEG_TXP4	11
PEG_TXP5	E2	PEG_TXP5	11
PEG_TXP6	J6	PEG_TXP6	11
PEG_TXP7	G2	PEG_TXP7	11
PEG_TXP8	J4	PEG_TXP8	11
PEG_TXP9	J1	PEG_TXP9	11
PEG_TXP10	T5	PEG_TXP10	11
PEG_TXP11	R5	PEG_TXP11	11
PEG_TXP12	R1	PEG_TXP12	11
PEG_TXP13	R3	PEG_TXP13	11
PEG_TXP14	T3	PEG_TXP14	11
PEG_TXP15	T2	PEG_TXP15	11

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Haswell (CLK,MISC,JTAG)

SM_RCOMP_0/1/2 : 15/20/25/15/20/25
SM_RCOMP_0/1/2 Length max: 500mil

U1B — HASWELL_BGA_E

C51	PROC_DETECT	MISC	
VIA_H_CATERR#	G50 CATERR	THERMAL	
34 H_PECI	G51 PECI		
H_PROCHOT# R	E50 PROCHOT		
27 H_THRMTRIP#	D53 THERMTRIP		
25 H_PM_SYNC	D52 PM_SYNC	PWR	
27 H_CPUPWRGD	F50 PWRGOOD		
PM_DRAM_PWRGD_R	AP48 SM_DRAMPWROK		
27 PCH_PLTRST_CPU	L54 PLTRSTIN		
23 CLK_DPN	AC6 DPLL_REF_CLKN	CLOCK	
23 CLK_DPP	AE6 DPLL_REF_CLKP		
23 CLK_DP_SSCN	V6 SSC_DPLL_REF_CLKN		
23 CLK_DP_SSCP	Y6 SSC_DPLL_REF_CLKP		
23 CLK_EXP#	AB6 BCLKN		
23 CLK_EXP	AA6 BCLKP		
SM_RCOMP0	BB51 SM_RCOMP0_JNC R277 100R1%0402 GND	DDR3	
SM_RCOMP1	BB53 SM_RCOMP1_JNC R269 75R1%0402		
SM_RCOMP2	BB52 SM_RCOMP2_JNC R276 100R1%0402		
SM_DRAMRST	BE51 CPUDRAMRST#		
PRDY	N53	JTAG	
PREQ	N52 VIA_XDP_PREQ#		
TCK	N54 XDP_TCLK		
TMS	M51 VIA_XDP_TMS		
TRST	M53 XDP_TRST#		
TDI	N49 VIA_XDP_TDI		
TDO	M49 VIA_XDP_TDO		
DBR	F53 VIA_XDP_DBRESET#		
BPM#0	R51		
BPM#1	R50		
BPM#2	P49		
BPM#3	N50		
BPM#4	P49		
BPM#5	P53		
BPM#6	U51		
BPM#7	P51		

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R237 10KR1%0402 — GND

H_CPUPWRGD EC14 X_C15p50N0402 GND

EC Sink current 2 mA

+VCCIO_OUT — R236 681R1%0402

34 EC_PROCHOT# — R235 56R0402 — H_PROCHOT# R

53 IMVP_PROCHOT# — 1 — 2 — JNC7 X_0402

47P close PWM

+1_35VDIMM — Not Support Deep S3

R22 1.8K1%0402

1.35V

25 PM_DRAM_PWRGD — R20 0R1%0402 — PM_DRAM_PWRGD_R

R21 3.3KR1%0402 — GND

1K on CRB , 0R on DG

R,C Close SO-DIMM

9,10 DDR3_DRAMRST# — R29 0R1%0402 CPUDRAMRST#

EC1 X_C0.1u50X70402 — GND

p.11 479493_479493_SharkBay_HSW_ext_rev2.0.pdf
Processor JTAG (TDI, TDO, TMS, TRST#, TCK) signals, PREQ# and PRDY# signals signals have adequate internal bias resistances to support the removal of the external pull up and pull down on the board when debug is no longer needed.

XDP_TCLK R17 51R1%0402

XDP_TRST# R18 51R1%0402 — GND

MICRO-STAR INT'L CO.,LTD.

Title: CPU-1 (Host Bus)

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Haswell (DDR3L)

SODIMM#A

U1C — HASWELL_BGA_E

9 M_A_DQ[63:0]

M_A_DQ0	AH54	SA_DQ0
M_A_DQ1	AH52	SA_DQ1
M_A_DQ2	AK51	SA_DQ2
M_A_DQ3	AK54	SA_DQ3
M_A_DQ4	AH53	SA_DQ4
M_A_DQ5	AH51	SA_DQ5
M_A_DQ6	AK52	SA_DQ6
M_A_DQ7	AK53	SA_DQ7
M_A_DQ8	AN54	SA_DQ8
M_A_DQ9	AN52	SA_DQ9
M_A_DQ10	AR51	SA_DQ10
M_A_DQ11	AR53	SA_DQ11
M_A_DQ12	AN53	SA_DQ12
M_A_DQ13	AN51	SA_DQ13
M_A_DQ14	AR52	SA_DQ14
M_A_DQ15	AR54	SA_DQ15
M_A_DQ16	AV52	SA_DQ16
M_A_DQ17	AV53	SA_DQ17
M_A_DQ18	AY52	SA_DQ18
M_A_DQ19	AY51	SA_DQ19
M_A_DQ20	AV51	SA_DQ20
M_A_DQ21	AV54	SA_DQ21
M_A_DQ22	AY54	SA_DQ22
M_A_DQ23	AY53	SA_DQ23
M_A_DQ24	AY47	SA_DQ24
M_A_DQ25	AY49	SA_DQ25
M_A_DQ26	BA47	SA_DQ26
M_A_DQ27	BA45	SA_DQ27
M_A_DQ28	AY45	SA_DQ28
M_A_DQ29	AY43	SA_DQ29
M_A_DQ30	BA49	SA_DQ30
M_A_DQ31	BA43	SA_DQ31
M_A_DQ32	BF14	SA_DQ32
M_A_DQ33	BC14	SA_DQ33
M_A_DQ34	BC11	SA_DQ34
M_A_DQ35	BF11	SA_DQ35
M_A_DQ36	BE14	SA_DQ36
M_A_DQ37	BD14	SA_DQ37
M_A_DQ38	BD11	SA_DQ38
M_A_DQ39	BE11	SA_DQ39
M_A_DQ40	BC9	SA_DQ40
M_A_DQ41	BE9	SA_DQ41
M_A_DQ42	BE6	SA_DQ42
M_A_DQ43	BC6	SA_DQ43
M_A_DQ44	BD9	SA_DQ44
M_A_DQ45	BF9	SA_DQ45
M_A_DQ46	BE5	SA_DQ46
M_A_DQ47	BD6	SA_DQ47
M_A_DQ48	BB4	SA_DQ48
M_A_DQ49	BC2	SA_DQ49
M_A_DQ50	AW3	SA_DQ50
M_A_DQ51	AW2	SA_DQ51
M_A_DQ52	BB3	SA_DQ52
M_A_DQ53	BB2	SA_DQ53
M_A_DQ54	AW4	SA_DQ54
M_A_DQ55	AW1	SA_DQ55
M_A_DQ56	AU3	SA_DQ56
M_A_DQ57	AU1	SA_DQ57
M_A_DQ58	AR1	SA_DQ58
M_A_DQ59	AR4	SA_DQ59
M_A_DQ60	AU2	SA_DQ60
M_A_DQ61	AU4	SA_DQ61
M_A_DQ62	AR2	SA_DQ62
M_A_DQ63	AR3	SA_DQ63

9,10 DIMM_SM_VREF	AM6	SM_VREF
9 M_VREF_DQ_DIMMA	AR6	SA_DIMM_VREFDQ
10 M_VREF_DQ_DIMMB	AN6	SB_DIMM_VREFDQ
	BC53	RSVD

RSVD	BD31	
SA_CKN0	BE25	M_A_CLK_DDR#0 9
SA_CK0	BE25	M_A_CLK_DDR0 9
SA_CKE0	BE34	M_A_CKE0 9
SA_CKN1	BD25	M_A_CLK_DDR#1 9
SA_CK1	BC25	M_A_CLK_DDR1 9
SA_CKE1	BE34	M_A_CKE1 9
SA_CKN2	BE23	
SA_CK2	BF23	
SA_CKE2	BC34	
SA_CKN3	BD23	
SA_CK3	BC23	
SA_CKE3	BD34	
SA_CS#0	BE16	M_A_CS#0 9
SA_CS#1	BC17	M_A_CS#1 9
SA_CS#2	BE17	
SA_CS#3	BD16	
SA_ODT0	BC16	M_A_ODT0 9
SA_ODT1	BE16	M_A_ODT1 9
SA_ODT2	BF17	
SA_ODT3	BD17	
SA_BS0	BC20	M_A_BS0 9
SA_BS1	BD21	M_A_BS1 9
SA_BS2	BD32	M_A_BS2 9
VSS	BC21	GND
SA_RAS	BE20	M_A_RAS# 9
SA_WE	BE21	M_A_WE# 9
SA_CAS	BE21	M_A_CAS# 9
SA_MA0	BD28	M_A_A0
SA_MA1	BD27	M_A_A1
SA_MA2	BE28	M_A_A2
SA_MA3	BE28	M_A_A3
SA_MA4	BF32	M_A_A4
SA_MA5	BC27	M_A_A5
SA_MA6	BF27	M_A_A6
SA_MA7	BC28	M_A_A7
SA_MA8	BE27	M_A_A8
SA_MA9	BC32	M_A_A9
SA_MA10	BD20	M_A_A10
SA_MA11	BE31	M_A_A11
SA_MA12	BC31	M_A_A12
SA_MA13	BE20	M_A_A13
SA_MA14	BE32	M_A_A14
SA_MA15	BE31	M_A_A15
SA_DQSN0	AJ52	M_A_DQS#0
SA_DQSN1	AP53	M_A_DQS#1
SA_DQSN2	AW52	M_A_DQS#2
SA_DQSN3	AY46	M_A_DQS#3
SA_DQSN4	BD12	M_A_DQS#4
SA_DQSN5	BE7	M_A_DQS#5
SA_DQSN6	BA3	M_A_DQS#6
SA_DQSN7	AT2	M_A_DQS#7
RSVD	AW39	
SA_DQS0	AJ53	M_A_DQS0
SA_DQS1	AP52	M_A_DQS1
SA_DQS2	AW53	M_A_DQS2
SA_DQS3	BA46	M_A_DQS3
SA_DQS4	BE12	M_A_DQS4
SA_DQS5	BD7	M_A_DQS5
SA_DQS6	BA2	M_A_DQS6
SA_DQS7	AT3	M_A_DQS7
RSVD	AW40	
RSVD	BA40	
RSVD	AY40	
RSVD	BA39	
RSVD	AY39	
RSVD	AV40	
RSVD	AU40	
RSVD	AV39	
RSVD	AU39	

M_A_A[15:0] 9

M_A_DQS#[7:0] 9

M_A_DQS[7:0] 9

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SODIMM#B

U1D — HASWELL_BGA_E

10 M_B_DQ[63:0]

M_B_DQ0	AC54	SB_DQ0
M_B_DQ1	AC52	SB_DQ1
M_B_DQ2	AE51	SB_DQ2
M_B_DQ3	AE54	SB_DQ3
M_B_DQ4	AC53	SB_DQ4
M_B_DQ5	AC51	SB_DQ5
M_B_DQ6	AE52	SB_DQ6
M_B_DQ7	AE53	SB_DQ7
M_B_DQ8	AU47	SB_DQ8
M_B_DQ9	AU49	SB_DQ9
M_B_DQ10	AV43	SB_DQ10
M_B_DQ11	AV45	SB_DQ11
M_B_DQ12	AU43	SB_DQ12
M_B_DQ13	AU45	SB_DQ13
M_B_DQ14	AV47	SB_DQ14
M_B_DQ15	AV49	SB_DQ15
M_B_DQ16	BC49	SB_DQ16
M_B_DQ17	BE49	SB_DQ17
M_B_DQ18	BD47	SB_DQ18
M_B_DQ19	BC47	SB_DQ19
M_B_DQ20	BD49	SB_DQ20
M_B_DQ21	BD50	SB_DQ21
M_B_DQ22	BE47	SB_DQ22
M_B_DQ23	BF47	SB_DQ23
M_B_DQ24	BE44	SB_DQ24
M_B_DQ25	BD44	SB_DQ25
M_B_DQ26	BC42	SB_DQ26
M_B_DQ27	BE42	SB_DQ27
M_B_DQ28	BE44	SB_DQ28
M_B_DQ29	BC44	SB_DQ29
M_B_DQ30	BD42	SB_DQ30
M_B_DQ31	BE42	SB_DQ31
M_B_DQ32	BA16	SB_DQ32
M_B_DQ33	AU16	SB_DQ33
M_B_DQ34	BA15	SB_DQ34
M_B_DQ35	AV15	SB_DQ35
M_B_DQ36	AY16	SB_DQ36
M_B_DQ37	AV16	SB_DQ37
M_B_DQ38	AY15	SB_DQ38
M_B_DQ39	AU15	SB_DQ39
M_B_DQ40	AU12	SB_DQ40
M_B_DQ41	AY12	SB_DQ41
M_B_DQ42	BA10	SB_DQ42
M_B_DQ43	AU10	SB_DQ43
M_B_DQ44	AV12	SB_DQ44
M_B_DQ45	BA12	SB_DQ45
M_B_DQ46	AY10	SB_DQ46
M_B_DQ47	AV10	SB_DQ47
M_B_DQ48	AU8	SB_DQ48
M_B_DQ49	BA8	SB_DQ49
M_B_DQ50	AV6	SB_DQ50
M_B_DQ51	BA6	SB_DQ51
M_B_DQ52	AV8	SB_DQ52
M_B_DQ53	AY8	SB_DQ53
M_B_DQ54	AU6	SB_DQ54
M_B_DQ55	AY6	SB_DQ55
M_B_DQ56	AM2	SB_DQ56
M_B_DQ57	AM3	SB_DQ57
M_B_DQ58	AK1	SB_DQ58
M_B_DQ59	AK4	SB_DQ59
M_B_DQ60	AM1	SB_DQ60
M_B_DQ61	AM4	SB_DQ61
M_B_DQ62	AK2	SB_DQ62
M_B_DQ63	AK3	SB_DQ63

RSVD	AY36	
SB_CKN0	AW27	M_B_CLK_DDR#0 10
SB_CK0	AV27	M_B_CLK_DDR0 10
SB_CKE0	AU36	M_B_CKE0 10
SB_CKN1	AW26	M_B_CLK_DDR#1 10
SB_CK1	AV26	M_B_CLK_DDR1 10
SB_CKE1	AU35	M_B_CKE1 10
SB_CKN2	BA26	
SB_CK2	AY26	
SB_CKE2	AV35	
SB_CKN3	BA27	
SB_CK3	AY27	
SB_CKE3	AV36	
SB_CS#0	BA20	M_B_CS#0 10
SB_CS#1	AY19	M_B_CS#1 10
SB_CS#2	AU19	
SB_CS#3	AW20	
SB_ODT0	AY20	M_B_ODT0 10
SB_ODT1	BA19	M_B_ODT1 10
SB_ODT2	AV19	
SB_ODT3	AW19	
SB_BS0	AY23	M_B_BS0 10
SB_BS1	BA23	M_B_BS1 10
SB_BS2	BA36	M_B_BS2 10
VSS	AU30	GND
SB_RAS	AV23	M_B_RAS# 10
SB_WE	AW23	M_B_WE# 10
SB_CAS	AV20	M_B_CAS# 10
SB_MA0	BA30	M_B_A0
SB_MA1	AW30	M_B_A1
SB_MA2	AY30	M_B_A2
SB_MA3	AV30	M_B_A3
SB_MA4	AW32	M_B_A4
SB_MA5	AY32	M_B_A5
SB_MA6	AT30	M_B_A6
SB_MA7	AV32	M_B_A7
SB_MA8	BA32	M_B_A8
SB_MA9	AU32	M_B_A9
SB_MA10	AU23	M_B_A10
SB_MA11	AY35	M_B_A11
SB_MA12	AW35	M_B_A12
SB_MA13	AU20	M_B_A13
SB_MA14	AW36	M_B_A14
SB_MA15	BA35	M_B_A15
SB_DQSN0	AD52	M_B_DQS#0
SB_DQSN1	AU46	M_B_DQS#1
SB_DQSN2	BD48	M_B_DQS#2
SB_DQSN3	BD43	M_B_DQS#3
SB_DQSN4	AW16	M_B_DQS#4
SB_DQSN5	AW10	M_B_DQS#5
SB_DQSN6	AW8	M_B_DQS#6
SB_DQSN7	AL2	M_B_DQS#7
RSVD	BE38	
SB_DQS0	AD53	M_B_DQS0
SB_DQS1	AV46	M_B_DQS1
SB_DQS2	BE48	M_B_DQS2
SB_DQS3	BE43	M_B_DQS3
SB_DQS4	AW15	M_B_DQS4
SB_DQS5	AW12	M_B_DQS5
SB_DQS6	AW6	M_B_DQS6
SB_DQS7	AL3	M_B_DQS7
RSVD	BD38	
RSVD	BF39	
RSVD	BE39	
RSVD	BF37	
RSVD	BE37	
RSVD	BD39	
RSVD	BC39	
RSVD	BC37	
RSVD	BD37	

M_B_A[15:0] 10

M_B_DQS#[7:0] 10

M_B_DQS[7:0] 10

4 OF 12

MICRO-STAR INT'L CO.,LTD.

Title: CPU-2 (DDR3L)

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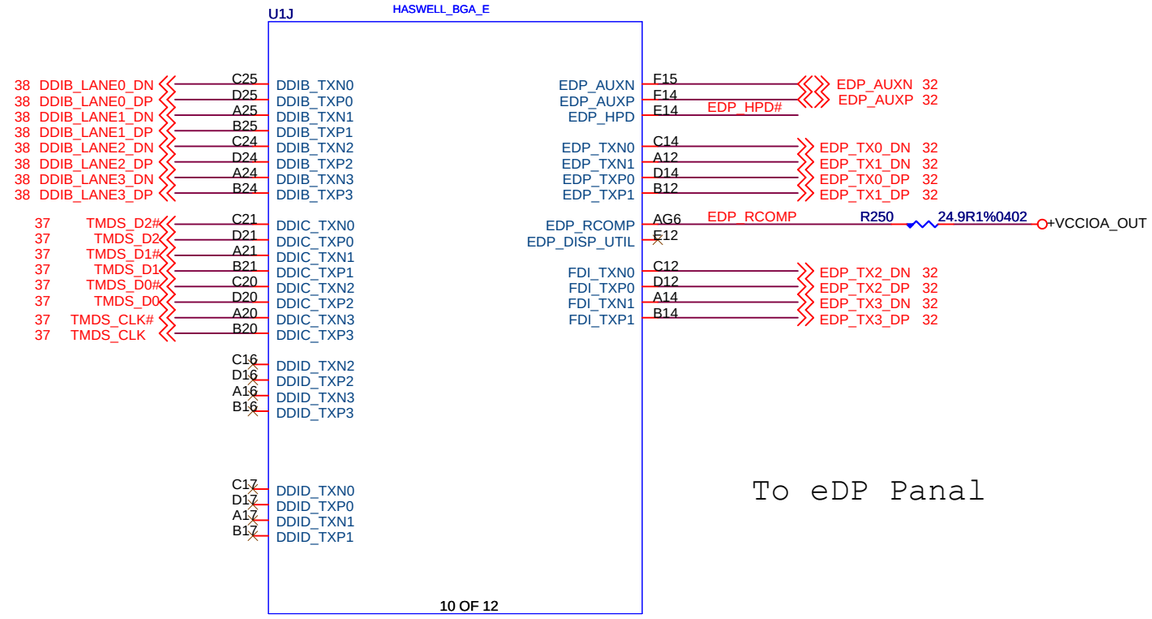
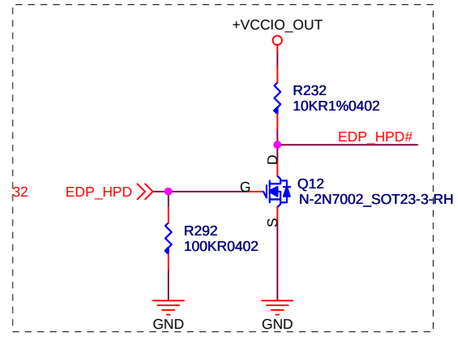
Display/Reserved

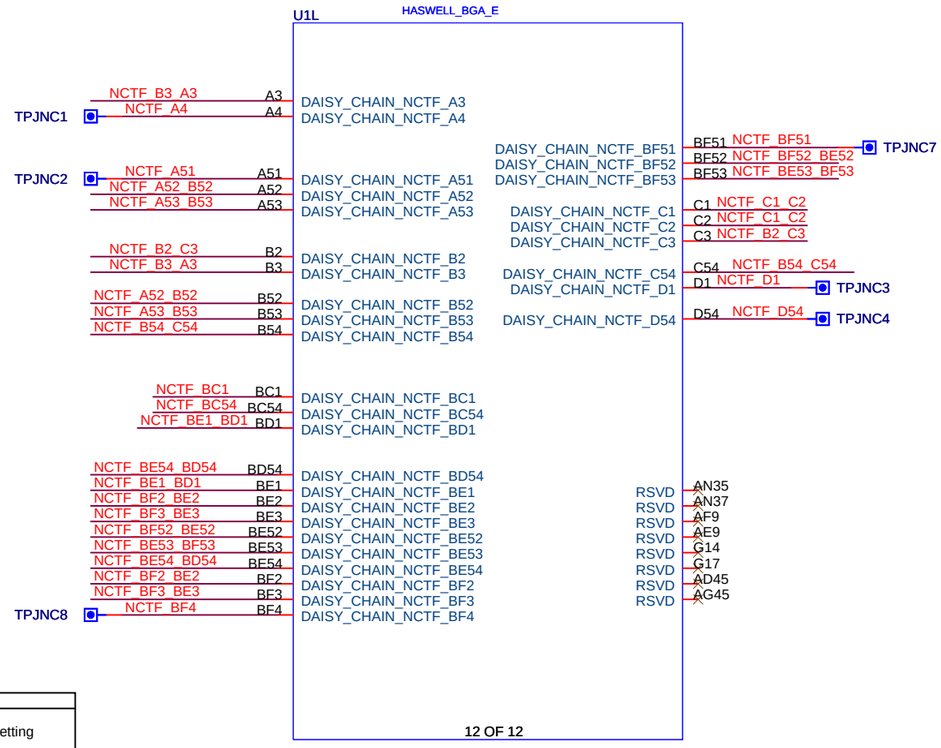
DP

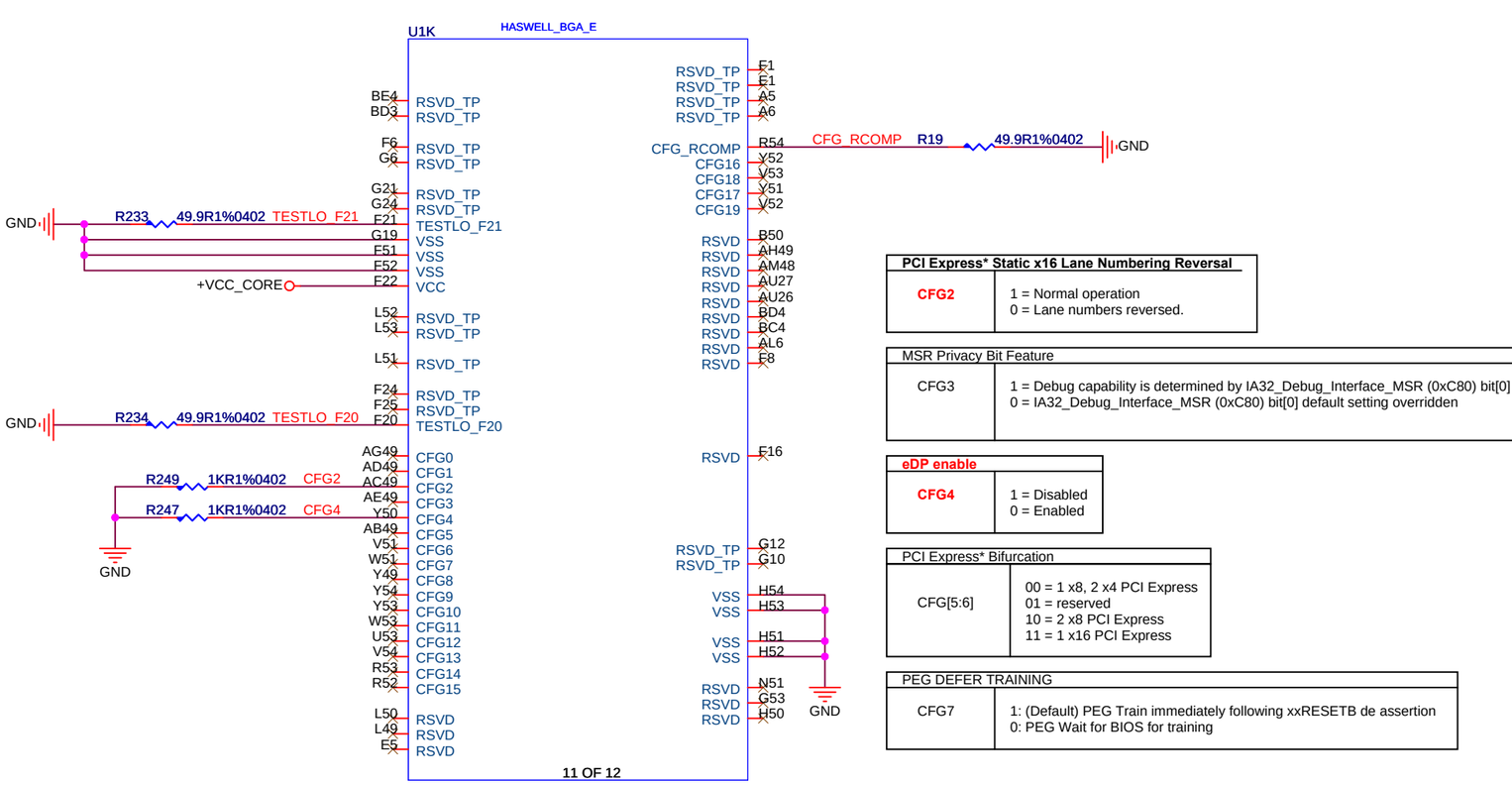
HDMI



To eDP Panal







PCI Express* Static x16 Lane Numbering Reversal	
CFG2	1 = Normal operation 0 = Lane numbers reversed.

MSR Privacy Bit Feature	
CFG3	1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden

eDP enable	
CFG4	1 = Disabled 0 = Enabled

PCI Express* Bifurcation	
CFG[5:6]	00 = 1 x8, 2 x4 PCI Express 01 = reserved 10 = 2 x8 PCI Express 11 = 1 x16 PCI Express

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

MICRO-STAR INT'L CO.,LTD.

Title: CPU-3 (Display/Reserved)

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Haswell (POWER)

22uF x 20 /0603
C11-2267313-T04

+VCC_CORE

C17 C22u6.3X0603
C22 C22u6.3X0603
C299 C22u6.3X0603
C253 C22u6.3X0603
C16 C22u6.3X0603
C254 C22u6.3X0603
C265 C22u6.3X0603
C21 C22u6.3X0603
C15 C22u6.3X0603
C20 C22u6.3X0603
C298 C22u6.3X0603
C266 C22u6.3X0603
C256 C22u6.3X0603
C269 C22u6.3X0603
C270 C22u6.3X0603
C252 C22u6.3X0603
C264 C22u6.3X0603
C263 C22u6.3X0603
C262 C22u6.3X0603
C255 C22u6.3X0603

GND

10uF x 4 /0603
C11-1067333-Y01

+VCC_CORE

C23 C10u6.3X5-HF
C19 C10u6.3X5-HF
C24 C10u6.3X5-HF
C18 C10u6.3X5-HF

GND

	Haswell	Boardwell
R231	No Stuff	Stuff
C284	No Stuff	Stuff
C271	No Stuff	Stuff
R12	No Stuff	Stuff
R11	No Stuff	Stuff

2014.2.20 Modify for Haswell CPU

+VCC_CORE

95A

HASWELL_BGA_E

U1E

VCC: B43 B45 B46 B48 C27 C28 C31 C32 C34 C36 C38 C39 C42 C43 C45 C46 C48 D27 D28 D31 D32 D34 D36 D38 D39 D42 D43 D45 D46 D48 E27 E28 E31 E32 E34 E36 E38 E39 E42 E43 E45 E46 E48 F27 F28 F31 F32 F34 F36 F38 F39 F42 F43 F45 F46 F48 G27 G29 G31 G32 G34 G36 G38 G39 G42 G43 G45 G46 G48 H11 H12 H13 H14 H16 H17 H18 H19 H20 H21 H23 H24 H25 H26 H27 H29

RSVD: J17 J21 J26 J31

4.2 A

VDDQ: AR29 AR31 AR33 AT13 AT19 AT23 AT27 AT32 AT36 AV37 AW22 AW25 AW29 AW33 AY18 BB21 BB22 BB26 BB27 BB30 BB31 BB34 BB36 BD22 BD26 BD30 BD33 BE18 BE22 BE26 BE30 BE33

+1_35VDIMM

PEC20 C330u2SO

C391 C1u25X0402
C389 C1u25X0402
C392 C1u25X0402
C436 C10u6.3X5-HF
C440 C10u6.3X5-HF
C437 C10u6.3X5-HF

GND

1u*3 / 0402
10u*3 / 0603

+VCC_CORE

RSVD: AN31 L6 M6 AN22 AN18

	Haswell	Boardwell
R229	No Stuff	Stuff

R217
100R1%0402

VCC_SENSE: C50
VCCSENSE 53

RSVD: AH9 D51

VCCIO_OUT: F17
FC_F17: F17
FC_F17 R229 X_0R1%0402 1_05V_AJ12

VCOMP_OUT: AK6
+VCCIO_OUT

300 mA

+VCCIO_OUT

C286
C4.7u10X0603

GND

2014.2.20 Modify for Haswell CPU

RSVD: AN33 W9 J12 AR49

VIDALERT: J53
VIDSCLK: J52
VIDSOUT: J50

VR_SVID_ALERT# R
R13 43R0402
VR_SVID_CLK
VR_SVID_DATA

+VCCIO_OUT
R14
75R1%0402
VR_SVID_ALERT# 53

+VCCIO_OUT
R211
54.9R1%0402
VR_SVID_CLK 53

+VCCIO_OUT
R16
130R1%0402

+VCCIO_OUT
R207
130R1%0402
VR_SVID_DATA 53

Close to CPU

Close to IMVP

VSS: B51

PWR_DEBUG: F19
PWR_DEBUG#
PJNC26

VSS: E52 V49

RSVD_TP: U49 AM49 W49

VIA_IVR_ERROR
VIA_IST_TRIGGER

VSS: V50 AN49 AJ49 AG50 AK49 AJ50 AP49 AB50 AP50 AD50 AM50

If XDP not implemented, then Route Processor PWR_DEBUG as a test point. This Test point must be clearly labeled

VCC: A36 A38 A39 A42 A43 A45 A46 A48 AA46 AA47 AA8 AA9

+VCC_CORE

5 OF 12

1_05V_AJ12

CPU_FC_PWR R231 X_0R1%0402

C284 X_C0.1u50X70402
C271 X_C22u6.3X0603

GND GND

25,34 EC_PCH_PWROK
R12 X_6.04KR1%0402
CPU_FC_PWR
CPU_FC_PWROK
D5 D3
FC_D5 FC_D3

R11 X_2.67KR1%0402

GND

Resever For BDW H 2-chips

CLK and DATA Misatch 2000mils
SVID total Length not over 6"

Title	CPU-4 (Power)
Size	
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Rev	1.0
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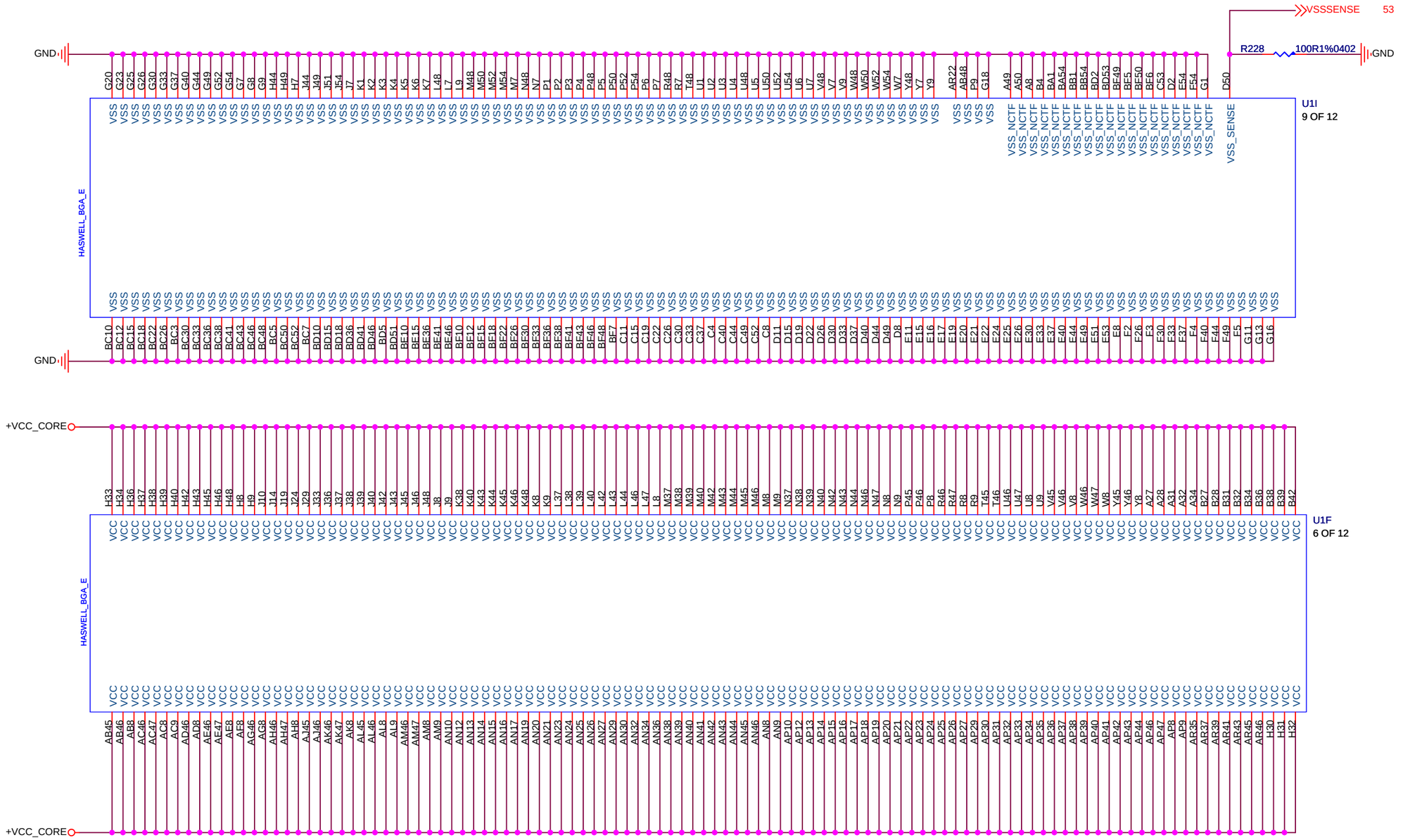
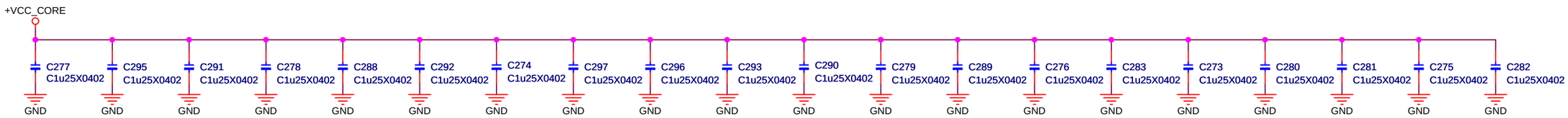
MICRO-STAR INT'L CO.,LTD.

Haswell (Power & GND)





MICRO-STAR INT'L CO.,LTD.

Title: CPU-6 (Power & GND)

Size | Document Number: MS-16H3 | Rev: 1.0

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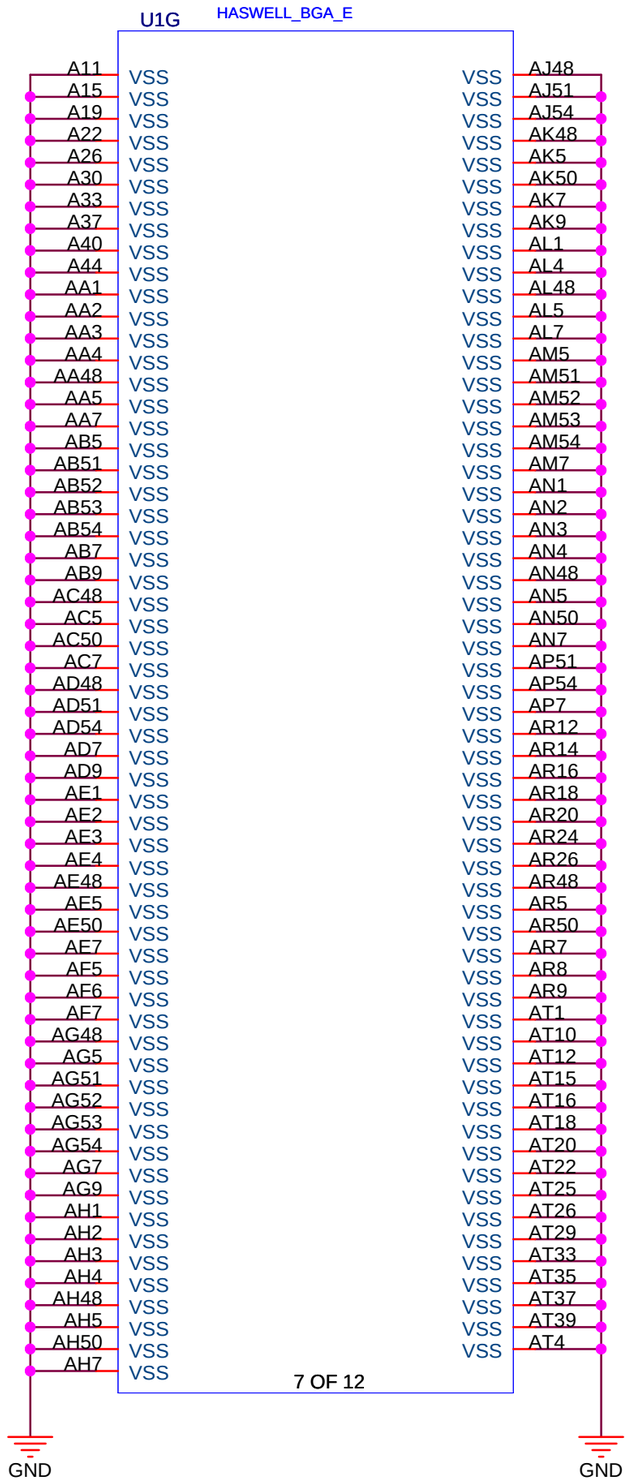
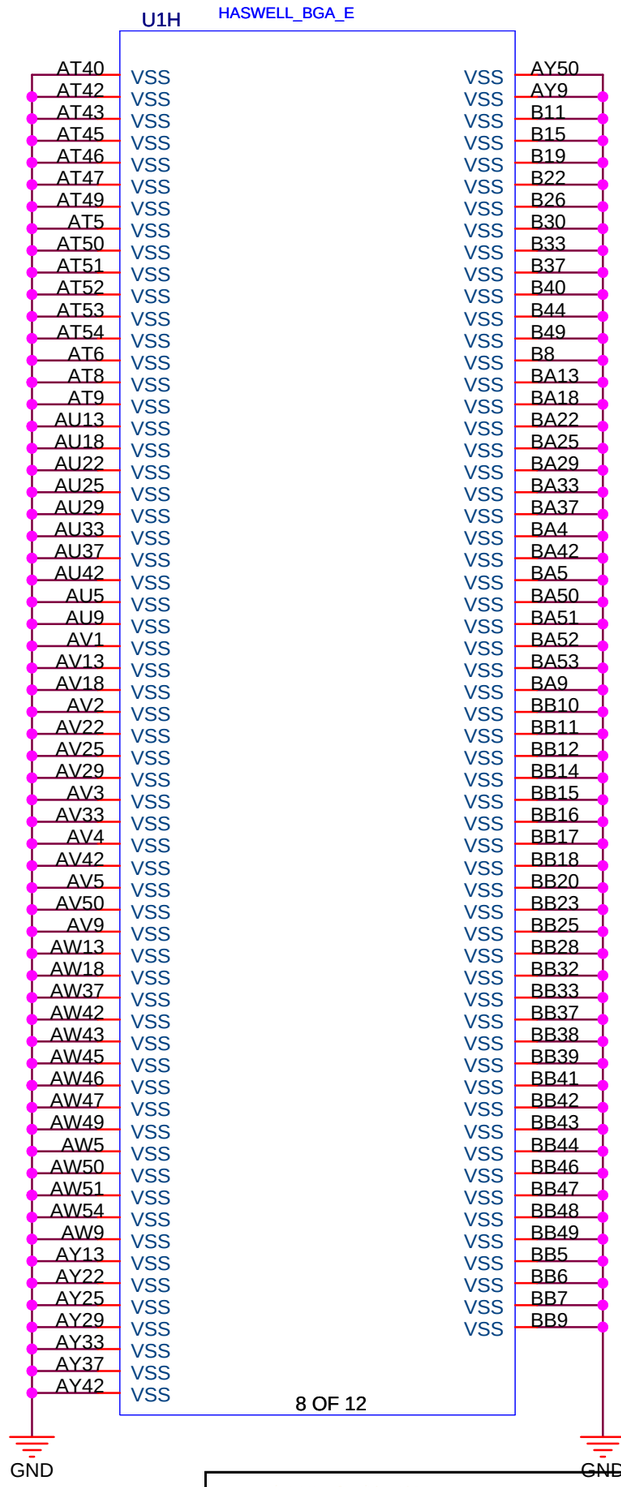
Haswell (GND)





MICRO-STAR INT'L CO.,LTD.		
Title: CPU-5 (GND)		
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SODIMM#A

SOCKET2A

4 M_A_DQ[63:0]

M_A_DQ0	5	DQ0	
M_A_DQ1	7	DQ1	
M_A_DQ2	15	DQ2	
M_A_DQ3	17	DQ3	
M_A_DQ4	4	DQ4	
M_A_DQ5	6	DQ5	
M_A_DQ6	16	DQ6	
M_A_DQ7	18	DQ7	
M_A_DQ8	21	DQ8	
M_A_DQ9	23	DQ9	
M_A_DQ10	33	DQ10	
M_A_DQ11	35	DQ11	
M_A_DQ12	22	DQ12	
M_A_DQ13	24	DQ13	
M_A_DQ14	34	DQ14	
M_A_DQ15	36	DQ15	
M_A_DQ16	39	DQ16	
M_A_DQ17	41	DQ17	
M_A_DQ18	51	DQ18	
M_A_DQ19	53	DQ19	
M_A_DQ20	40	DQ20	
M_A_DQ21	42	DQ21	
M_A_DQ22	50	DQ22	
M_A_DQ23	52	DQ23	
M_A_DQ24	57	DQ24	
M_A_DQ25	59	DQ25	
M_A_DQ26	67	DQ26	
M_A_DQ27	69	DQ27	
M_A_DQ28	56	DQ28	
M_A_DQ29	58	DQ29	
M_A_DQ30	68	DQ30	
M_A_DQ31	70	DQ31	
M_A_DQ32	129	DQ32	
M_A_DQ33	131	DQ33	
M_A_DQ34	141	DQ34	
M_A_DQ35	143	DQ35	
M_A_DQ36	130	DQ36	
M_A_DQ37	132	DQ37	
M_A_DQ38	140	DQ38	
M_A_DQ39	142	DQ39	
M_A_DQ40	147	DQ40	
M_A_DQ41	149	DQ41	
M_A_DQ42	157	DQ42	
M_A_DQ43	159	DQ43	
M_A_DQ44	146	DQ44	
M_A_DQ45	148	DQ45	
M_A_DQ46	158	DQ46	
M_A_DQ47	160	DQ47	
M_A_DQ48	163	DQ48	
M_A_DQ49	165	DQ49	
M_A_DQ50	175	DQ50	
M_A_DQ51	177	DQ51	
M_A_DQ52	164	DQ52	
M_A_DQ53	166	DQ53	
M_A_DQ54	174	DQ54	
M_A_DQ55	176	DQ55	
M_A_DQ56	181	DQ56	
M_A_DQ57	183	DQ57	
M_A_DQ58	191	DQ58	
M_A_DQ59	193	DQ59	
M_A_DQ60	180	DQ60	
M_A_DQ61	182	DQ61	
M_A_DQ62	192	DQ62	
M_A_DQ63	194	DQ63	

A0	98	M_A_A0	
A1	97	M_A_A1	
A2	96	M_A_A2	
A3	95	M_A_A3	
A4	92	M_A_A4	
A5	91	M_A_A5	
A6	90	M_A_A6	
A7	86	M_A_A7	
A8	89	M_A_A8	
A9	85	M_A_A9	
A10/AP	107	M_A_A10	
A11	84	M_A_A11	
A12/BC#	83	M_A_A12	
A13	119	M_A_A13	
A14	80	M_A_A14	
A15	78	M_A_A15	

M_A_A[15:0] 4

BA0	109	M_A_BS0 4
BA1	108	M_A_BS1 4
BA2	79	M_A_BS2 4
S0#	114	M_A_CS#0 4
S1#	121	M_A_CS#1 4
CK0	101	M_A_CLK_DDR0 4
CK0#	103	M_A_CLK_DDR#0 4
CK1	102	M_A_CLK_DDR1 4
CK1#	104	M_A_CLK_DDR#1 4
CKE0	73	M_A_CKE0 4
CKE1	74	M_A_CKE1 4
CAS#	115	M_A_CAS# 4
RAS#	110	M_A_RAS# 4
WE#	113	M_A_WE# 4
SA0	197	SA0_DIM0
SA1	201	SA1_DIM0
SCL	202	SMB_CLK_DIMM 10,24
SDA	200	SMB_DATA_DIMM 10,24
ODT0	116	M_A_ODT0 4
ODT1	120	M_A_ODT1 4
DM0	11	
DM1	28	
DM2	46	
DM3	63	
DM4	136	
DM5	153	
DM6	170	
DM7	187	

DQS0	12	M_A_DQS0
DQS1	29	M_A_DQS1
DQS2	47	M_A_DQS2
DQS3	64	M_A_DQS3
DQS4	137	M_A_DQS4
DQS5	154	M_A_DQS5
DQS6	171	M_A_DQS6
DQS7	188	M_A_DQS7
DQS#0	10	M_A_DQS#0
DQS#1	27	M_A_DQS#1
DQS#2	45	M_A_DQS#2
DQS#3	62	M_A_DQS#3
DQS#4	135	M_A_DQS#4
DQS#5	152	M_A_DQS#5
DQS#6	169	M_A_DQS#6
DQS#7	186	M_A_DQS#7

M_A_DQS[7:0] 4

M_A_DQS#[7:0] 4

DDR3SODIMM-204PS_BLACK-HF-33

N13-2041170-L41

M1(used for S3)
M3(used for S0),maybe to over-ride
Active when soft-start

+1_35VDIMM

C607 C1u25X0402 — GND
C584 C1u25X0402 — GND
C585 C1u25X0402 — GND
C609 C1u25X0402 — GND

+1_35VDIMM

C588 C10u6.3X5-HF — GND
C613 C10u6.3X5-HF — GND
C614 C10u6.3X5-HF — GND
C587 C10u6.3X5-HF — GND

SA0_DIM0 — 1 — JNC12 — 2 — X_0402 — GND

SA1_DIM0 — 1 — JNC13 — 2 — X_0402 — GND

+1_35VDIMM

SOCKET2B

75	VDD	VSS	44
76	VDD	VSS	48
81	VDD	VSS	49
82	VDD	VSS	54
87	VDD	VSS	55
88	VDD	VSS	60
93	VDD	VSS	61
94	VDD	VSS	65
99	VDD	VSS	66
100	VDD	VSS	71
105	VDD	VSS	72
106	VDD	VSS	127
111	VDD	VSS	128
112	VDD	VSS	133
117	VDD	VSS	134
118	VDD	VSS	138
123	VDD	VSS	139
124	VDD	VSS	144
		VSS	145
199	VDDSPD	VSS	150
		VSS	151
77	NC1	VSS	155
122	NC2	VSS	156
125	NCTEST	VSS	161
		VSS	162
198	EVENT#	VSS	167
30	RESET#	VSS	168
		VSS	172
		VSS	173
1	VREF_DQ	VSS	178
126	VREF_CA	VSS	179
		VSS	184
		VSS	185
2	VSS	VSS	189
3	VSS	VSS	190
8	VSS	VSS	195
9	VSS	VSS	196
13	VSS		
14	VSS	MEC1	MEC1
19	VSS		
20	VSS	MEC2	MEC2
25	VSS	VTT	203
26	VSS	VTT	204
31	VSS		
32	VSS	205	205
37	VSS	206	206
38	VSS		
43	VSS		

+3VRUN

C504 C0.1u50X70402
C490 C2.2u6.3X0402

3,10 DDR3_DRAMRST#

M_VREF_DQ_DIMM0_R

C591 C0.1u50X70402
C583 C2.2u6.3X0402

M_VREF_CA_DIMM0

C620 C0.1u50X70402
C605 C2.2u6.3X0402

+0_675VRUN

C549 C1u25X0603
C491 C1u25X0603

DDR3SODIMM-204PS_BLACK-HF-33

N13-2041170-L41

+1_35VDIMM

R379 1KR1%0402
M_VREF_DQ_DIMM0_R R377 2R1%0402 DQ_A R364 X_0R1%0402 M_VREF_DQ_DIMMA 4
R385 1KR1%0402
GND

Close to DIMM

C561 C0.022u10X0402 GC
R363 24.9R1%0402
GND

+1_35VDIMM

R436 1KR1%0402
M_VREF_CA_DIMM0 R430 2R1%0402 CA_A R431 X_0R1%0402 DIMM_SM_VREF 4,10
R435 1KR1%0402
GND

Close to DIMM

C611 C0.022u10X0402 GC
R439 24.9R1%0402
GND

Vref DQ & CA

MICRO-STAR INT'L CO.,LTD.

Title: DDR3L SODIMM 0

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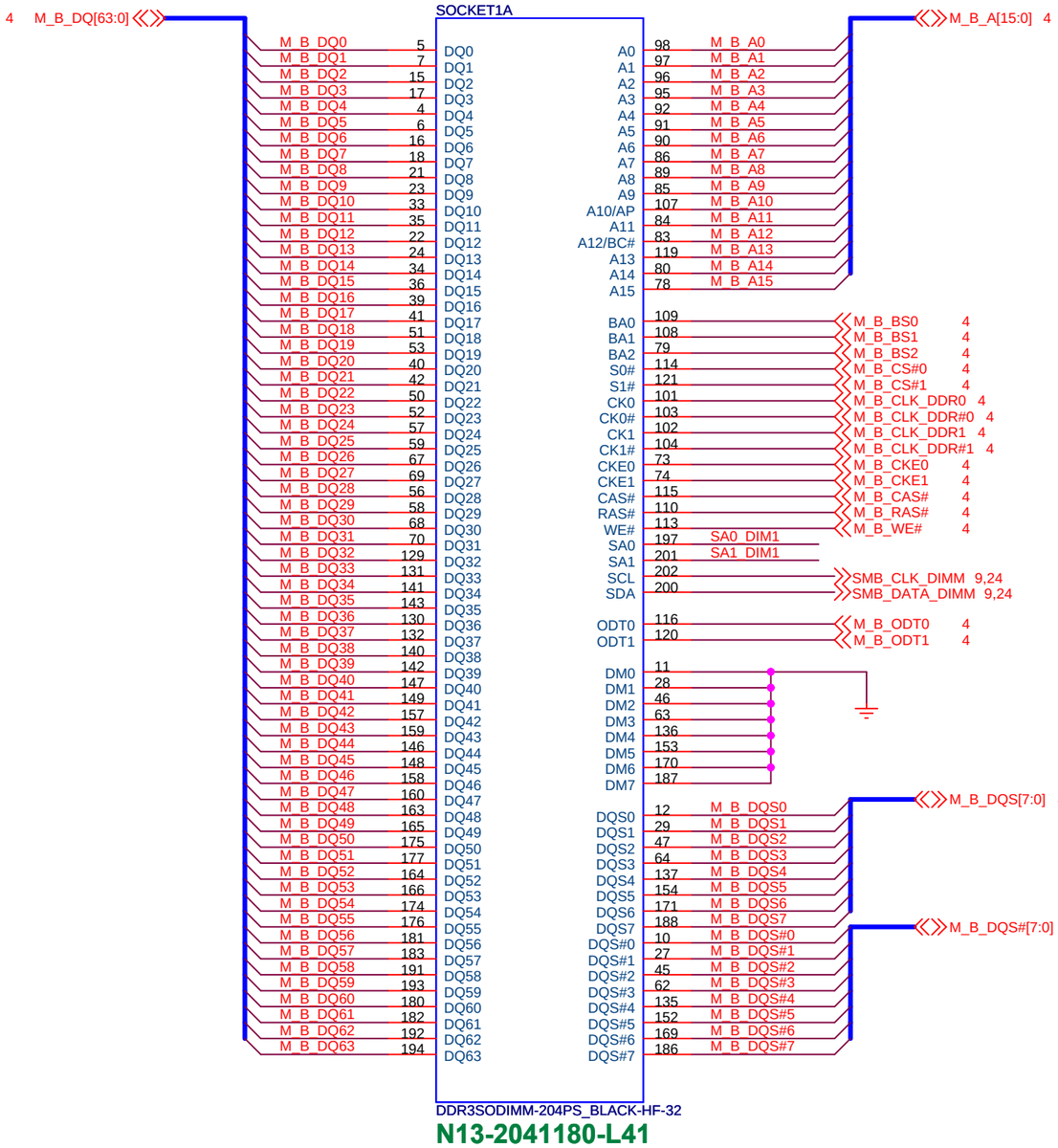
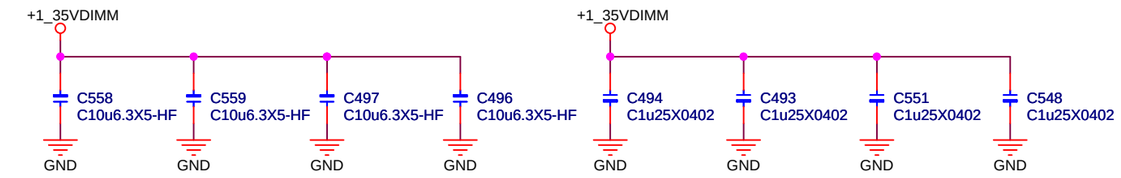
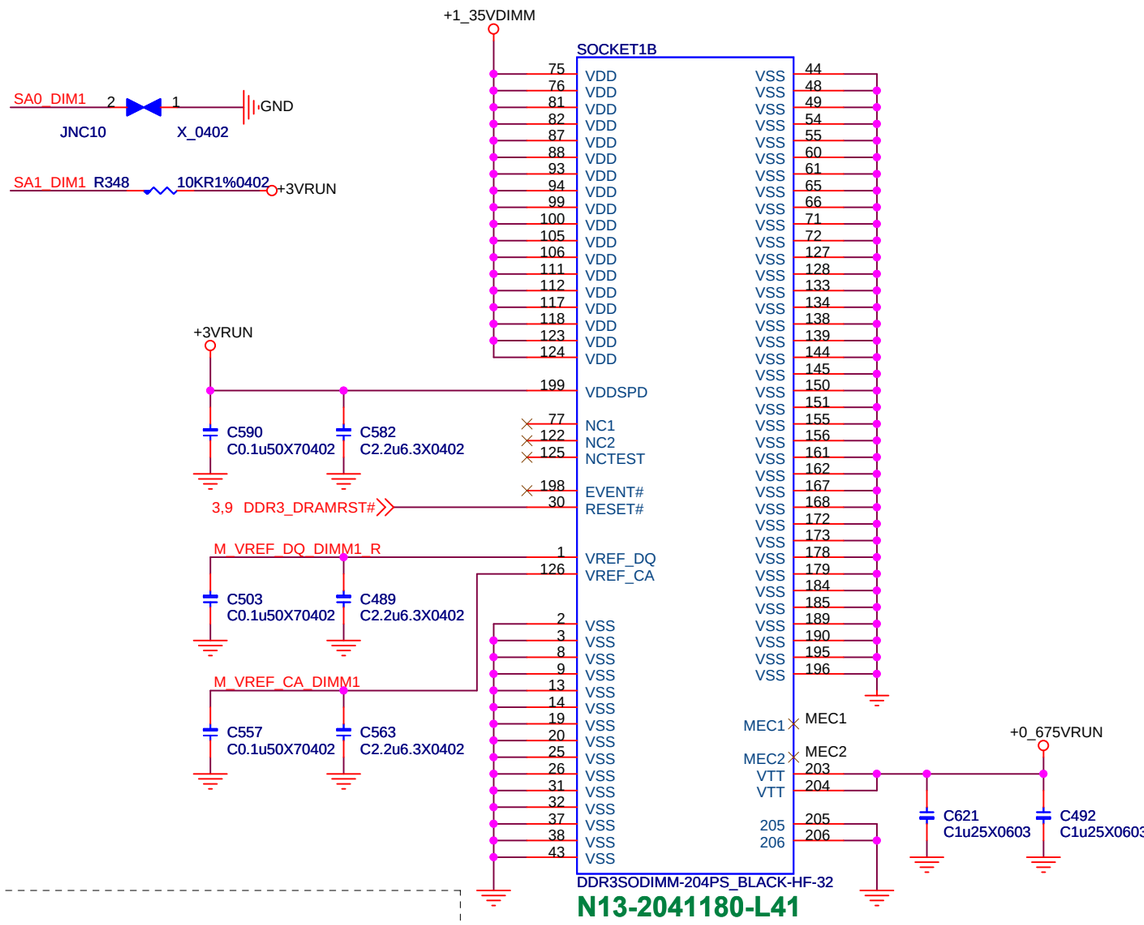
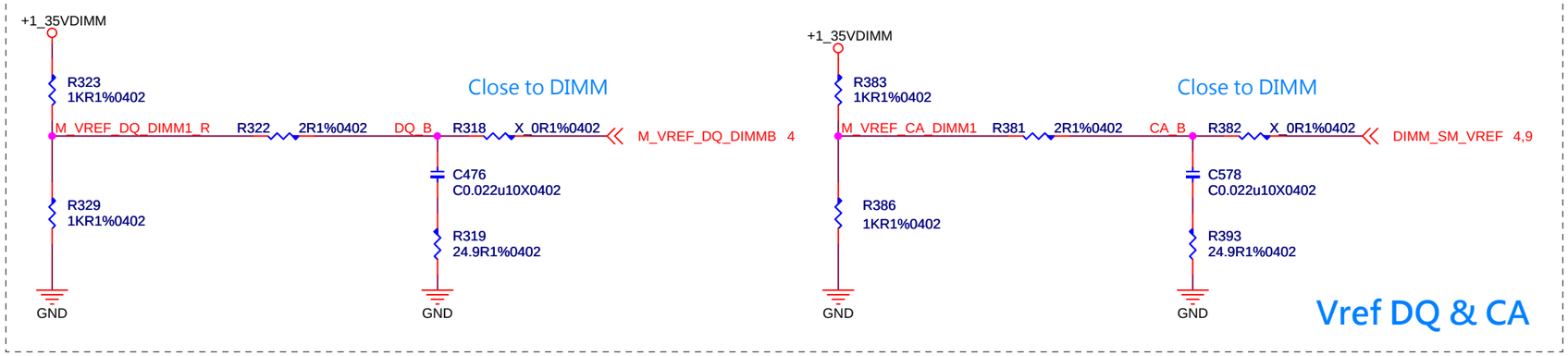
SODIMM#B









MICRO-STAR INT'L CO.,LTD.		
Title: DDR3L SODIMM 1		
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GPU CLK REQ#

18,20,27,34,52 DGPU_PWRGD

PEX_CLKREQ#

Q3 X_N-2N7002_SOT23-3-RH

Q4 N-2N7002_SOT23-3-RH

GPU_CLKREQ# 23

G5-N15P-GT-A2

X_N15P-GT-A2-RH

B03-0N15P25-N08

G5A

BGA908 COMMON

2014.2.6 不上件
2014.3.3 改上件

1/17 PCI_EXPRESS

GK107/GF108 GK208/GF117

+3V3_NV

26 PCIE_RST#

R51 X_10KR0402

R27 100KR0402

TPJNC29

PCIE_RST#

PEX_CLKREQ#

PEX_WAKE AJ11 — NC

PEX_RST AJ12

PEX_CLKREQ AK12

PEX_REFCLK AL13

PEX_REFCLK AK13

23 GFX_REFCLK
23 GFX_REFCLK#

3 PEG_RXP15	C396	C0.22u16X0402-HF	PEG_C_TXP15	AK14	PEX_TX0
3 PEG_RXN15	C403	C0.22u16X0402-HF	PEG_C_TXN15	AJ14	PEX_TX0
3 PEG_TXP15	C62	C0.22u16X0402-HF	PEG_C_RXP15	AN12	PEX_RX0
3 PEG_TXN15	C61	C0.22u16X0402-HF	PEG_C_RXN15	AM12	PEX_RX0
3 PEG_RXP14	C390	C0.22u16X0402-HF	PEG_C_TXP14	AH14	PEX_TX1
3 PEG_RXN14	C394	C0.22u16X0402-HF	PEG_C_TXN14	AG14	PEX_TX1
3 PEG_TXP14	C60	C0.22u16X0402-HF	PEG_C_RXP14	AN14	PEX_RX1
3 PEG_TXN14	C59	C0.22u16X0402-HF	PEG_C_RXN14	AM14	PEX_RX1
3 PEG_RXP13	C382	C0.22u16X0402-HF	PEG_C_TXP13	AK15	PEX_TX2
3 PEG_RXN13	C388	C0.22u16X0402-HF	PEG_C_TXN13	AJ15	PEX_TX2
3 PEG_TXP13	C58	C0.22u16X0402-HF	PEG_C_RXP13	AP14	PEX_RX2
3 PEG_TXN13	C57	C0.22u16X0402-HF	PEG_C_RXN13	AP15	PEX_RX2
3 PEG_RXP12	C370	C0.22u16X0402-HF	PEG_C_TXP12	AL16	PEX_TX3
3 PEG_RXN12	C381	C0.22u16X0402-HF	PEG_C_TXN12	AK16	PEX_TX3
3 PEG_TXP12	C56	C0.22u16X0402-HF	PEG_C_RXP12	AN15	PEX_RX3
3 PEG_TXN12	C55	C0.22u16X0402-HF	PEG_C_RXN12	AM15	PEX_RX3
3 PEG_RXP11	C368	C0.22u16X0402-HF	PEG_C_TXP11	AK17	PEX_TX4
3 PEG_RXN11	C359	C0.22u16X0402-HF	PEG_C_TXN11	AJ17	PEX_TX4
3 PEG_TXP11	C54	C0.22u16X0402-HF	PEG_C_RXP11	AN17	PEX_RX4
3 PEG_TXN11	C53	C0.22u16X0402-HF	PEG_C_RXN11	AM17	PEX_RX4
3 PEG_RXP10	C352	C0.22u16X0402-HF	PEG_C_TXP10	AH17	PEX_TX5
3 PEG_RXN10	C358	C0.22u16X0402-HF	PEG_C_TXN10	AG17	PEX_TX5
3 PEG_TXP10	C52	C0.22u16X0402-HF	PEG_C_RXP10	AP17	PEX_RX5
3 PEG_TXN10	C51	C0.22u16X0402-HF	PEG_C_RXN10	AP18	PEX_RX5
3 PEG_RXP9	C350	C0.22u16X0402-HF	PEG_C_TXP9	AK18	PEX_TX6
3 PEG_RXN9	C347	C0.22u16X0402-HF	PEG_C_TXN9	AJ18	PEX_TX6
3 PEG_TXP9	C50	C0.22u16X0402-HF	PEG_C_RXP9	AN18	PEX_RX6
3 PEG_TXN9	C49	C0.22u16X0402-HF	PEG_C_RXN9	AM18	PEX_RX6
3 PEG_RXP8	C341	C0.22u16X0402-HF	PEG_C_TXP8	AL19	PEX_TX7
3 PEG_RXN8	C344	C0.22u16X0402-HF	PEG_C_TXN8	AK19	PEX_TX7
3 PEG_TXP8	C48	C0.22u16X0402-HF	PEG_C_RXP8	AN20	PEX_RX7
3 PEG_TXN8	C47	C0.22u16X0402-HF	PEG_C_RXN8	AM20	PEX_RX7
3 PEG_RXP7	C340	C0.22u16X0402-HF	PEG_C_TXP7	AK20	PEX_TX8
3 PEG_RXN7	C329	C0.22u16X0402-HF	PEG_C_TXN7	AJ20	PEX_TX8
3 PEG_TXP7	C46	C0.22u16X0402-HF	PEG_C_RXP7	AP20	PEX_RX8
3 PEG_TXN7	C44	C0.22u16X0402-HF	PEG_C_RXN7	AP21	PEX_RX8
3 PEG_RXP6	C324	C0.22u16X0402-HF	PEG_C_TXP6	AH20	PEX_TX9
3 PEG_RXN6	C323	C0.22u16X0402-HF	PEG_C_TXN6	AG20	PEX_TX9
3 PEG_TXP6	C43	C0.22u16X0402-HF	PEG_C_RXP6	AN21	PEX_RX9
3 PEG_TXN6	C42	C0.22u16X0402-HF	PEG_C_RXN6	AM21	PEX_RX9
3 PEG_RXP5	C319	C0.22u16X0402-HF	PEG_C_TXP5	AK21	PEX_TX10
3 PEG_RXN5	C318	C0.22u16X0402-HF	PEG_C_TXN5	AJ21	PEX_TX10
3 PEG_TXP5	C41	C0.22u16X0402-HF	PEG_C_RXP5	AN23	PEX_RX10
3 PEG_TXN5	C40	C0.22u16X0402-HF	PEG_C_RXN5	AM23	PEX_RX10
3 PEG_RXP4	C315	C0.22u16X0402-HF	PEG_C_TXP4	AL22	PEX_TX11
3 PEG_RXN4	C317	C0.22u16X0402-HF	PEG_C_TXN4	AK22	PEX_TX11
3 PEG_TXP4	C39	C0.22u16X0402-HF	PEG_C_RXP4	AP23	PEX_RX11
3 PEG_TXN4	C38	C0.22u16X0402-HF	PEG_C_RXN4	AP24	PEX_RX11
3 PEG_RXP3	C312	C0.22u16X0402-HF	PEG_C_TXP3	AK23	PEX_TX12
3 PEG_RXN3	C308	C0.22u16X0402-HF	PEG_C_TXN3	AJ23	PEX_TX12
3 PEG_TXP3	C37	C0.22u16X0402-HF	PEG_C_RXP3	AN24	PEX_RX12
3 PEG_TXN3	C36	C0.22u16X0402-HF	PEG_C_RXN3	AM24	PEX_RX12
3 PEG_RXP2	C305	C0.22u16X0402-HF	PEG_C_TXP2	AH23	PEX_TX13
3 PEG_RXN2	C307	C0.22u16X0402-HF	PEG_C_TXN2	AG23	PEX_TX13
3 PEG_TXP2	C35	C0.22u16X0402-HF	PEG_C_RXP2	AN26	PEX_RX13
3 PEG_TXN2	C34	C0.22u16X0402-HF	PEG_C_RXN2	AM26	PEX_RX13
3 PEG_RXP1	C304	C0.22u16X0402-HF	PEG_C_TXP1	AK24	PEX_TX14
3 PEG_RXN1	C302	C0.22u16X0402-HF	PEG_C_TXN1	AJ24	PEX_TX14
3 PEG_TXP1	C33	C0.22u16X0402-HF	PEG_C_RXP1	AP26	PEX_RX14
3 PEG_TXN1	C32	C0.22u16X0402-HF	PEG_C_RXN1	AP27	PEX_RX14
3 PEG_RXP0	C301	C0.22u16X0402-HF	PEG_C_TXP0	AL25	PEX_TX15
3 PEG_RXN0	C300	C0.22u16X0402-HF	PEG_C_TXN0	AK25	PEX_TX15
3 PEG_TXP0	C31	C0.22u16X0402-HF	PEG_C_RXP0	AN27	PEX_RX15
3 PEG_TXN0	C29	C0.22u16X0402-HF	PEG_C_RXN0	AM27	PEX_RX15

PEX LANES 8 TO 15 NC FOR GF117/GK208

PEX_IOVDD AG19, AG21, AG22, AG24, AH21, AH25

PEX_IOVDDQ AG13, AG15, AG16, AG18, AG25, AH15, AH18, AH26, AH27, AJ27, AK27, AL27, AM28, AN28

Under GPU / Near GPU

3.3A

PEX_VDD 1.05V

Under GPU: C400 C1u6.3X60402-RH; C316 C1u6.3X60402-RH; C311 C1u6.3X60402-RH; C346 C1u6.3X60402-RH

Near GPU: C78 C4.7u6.3X6; C70 C10u6.3X7R_0805; C75 C10u6.3X7R_0805; C453 C22u6.3X60805-HF; C451 C22u6.3X60805-HF; C397 C4.7u6.3X6; C444 C10u6.3X7R_0805; C69 C10u6.3X7R_0805; C76 C22u6.3X60805-HF; C63 C22u6.3X60805-HF

2014.03.13 Modify

1x 0.1u under GPU;
2x 4.7u near GPU;

GF108 / NC — GK208/GK107/GF117 — PEX_PLL_HVDD AH12 — PEX_SVDD_3V3 AG12

Near GPU

0.21A

+3V3_NV

C426 C0.1u10X0402

C424 C4.7u6.3X6

Near GPU

+3V3_NV

C415 C4.7u6.3X6

Under GPU

PEX_VDD

C80 C1u6.3X60402-RH

2014.03.13 Change

2014.03.13 remove

GPU to R < 10000mils — R to PWM < 2000mils

VDD_SENSE L4 — NVVDD_SENSE_GPU 51

GND_SENSE L5 — NVVDD_GND_SENSE_GPU 51

GPU to R < 10000mils — R to PWM < 2000 mils

2014.03.13 remove

Near PWM

3V3AUX_NC P8

PEX_TSTCLK_OUT AJ26 — PEX_TSTCLK_OUT R244 X_200R1%0402 — PEX_TSTCLK_OUT# AK26

PEX_PLLVDD AG26 0.15A

Under GPU: C456 C0.1u10X0402

Near GPU: C454 C4.7u6.3X6

PEX_VDD

TESTMODE AK11 GPU_TESTMODE R260 10KR1%0402

PEX_TERMP AP29 PEX_TERMP R15 2.49KR1%0402

MICRO-STAR INT'L CO.,LTD.

Title: N15P-Q3_PCIE Host

Size: — Document Number: MS-16H3 — Rev: 1.0

Date: Wednesday, June 25, 2014 — Sheet 11 of 69

G5B

BGA908 COMMON

2/17 FBA

13	FBA_D0	L28	FBA_D0
13	FBA_D1	M29	FBA_D1
13	FBA_D2	L29	FBA_D2
13	FBA_D3	M28	FBA_D3
13	FBA_D4	N31	FBA_D4
13	FBA_D5	P29	FBA_D5
13	FBA_D6	R29	FBA_D6
13	FBA_D7	P28	FBA_D7
13	FBA_D8	J28	FBA_D8
13	FBA_D9	H29	FBA_D9
13	FBA_D10	J29	FBA_D10
13	FBA_D11	H28	FBA_D11
13	FBA_D12	G29	FBA_D12
13	FBA_D13	E31	FBA_D13
13	FBA_D14	E32	FBA_D14
13	FBA_D15	F30	FBA_D15
13	FBA_D16	C34	FBA_D16
13	FBA_D17	D32	FBA_D17
13	FBA_D18	B33	FBA_D18
13	FBA_D19	C33	FBA_D19
13	FBA_D20	E33	FBA_D20
13	FBA_D21	F32	FBA_D21
13	FBA_D22	H33	FBA_D22
13	FBA_D23	H32	FBA_D23
13	FBA_D24	P34	FBA_D24
13	FBA_D25	P32	FBA_D25
13	FBA_D26	P31	FBA_D26
13	FBA_D27	P33	FBA_D27
13	FBA_D28	L31	FBA_D28
13	FBA_D29	L34	FBA_D29
13	FBA_D30	L32	FBA_D30
13	FBA_D31	L33	FBA_D31
14	FBA_D32	AG28	FBA_D32
14	FBA_D33	AF29	FBA_D33
14	FBA_D34	AG29	FBA_D34
14	FBA_D35	AE28	FBA_D35
14	FBA_D36	AD30	FBA_D36
14	FBA_D37	AD29	FBA_D37
14	FBA_D38	AC29	FBA_D38
14	FBA_D39	AD28	FBA_D39
14	FBA_D40	AJ29	FBA_D40
14	FBA_D41	AK29	FBA_D41
14	FBA_D42	AJ30	FBA_D42
14	FBA_D43	AK28	FBA_D43
14	FBA_D44	AM29	FBA_D44
14	FBA_D45	AM31	FBA_D45
14	FBA_D46	AN29	FBA_D46
14	FBA_D47	AM30	FBA_D47
14	FBA_D48	AN31	FBA_D48
14	FBA_D49	AN32	FBA_D49
14	FBA_D50	AP30	FBA_D50
14	FBA_D51	AP32	FBA_D51
14	FBA_D52	AM33	FBA_D52
14	FBA_D53	AL31	FBA_D53
14	FBA_D54	AK33	FBA_D54
14	FBA_D55	AK32	FBA_D55
14	FBA_D56	AD34	FBA_D56
14	FBA_D57	AD32	FBA_D57
14	FBA_D58	AC30	FBA_D58
14	FBA_D59	AD33	FBA_D59
14	FBA_D60	AF31	FBA_D60
14	FBA_D61	AG34	FBA_D61
14	FBA_D62	AG32	FBA_D62
14	FBA_D63	AG33	FBA_D63

13	FBA_DBI0	P30	FBA_DQM0
13	FBA_DBI1	E31	FBA_DQM1
13	FBA_DBI2	F34	FBA_DQM2
13	FBA_DBI3	M32	FBA_DQM3
14	FBA_DBI4	AD31	FBA_DQM4
14	FBA_DBI5	AL29	FBA_DQM5
14	FBA_DBI6	AM32	FBA_DQM6
14	FBA_DBI7	AE34	FBA_DQM7

13	FBA_EDC0	M31	FBA_DQS_WP0
13	FBA_EDC1	G31	FBA_DQS_WP1
13	FBA_EDC2	E33	FBA_DQS_WP2
13	FBA_EDC3	M33	FBA_DQS_WP3
14	FBA_EDC4	AE31	FBA_DQS_WP4
14	FBA_EDC5	AK30	FBA_DQS_WP5
14	FBA_EDC6	AN33	FBA_DQS_WP6
14	FBA_EDC7	AF33	FBA_DQS_WP7

M30	FBA_DQS_RN0	
H30	FBA_DQS_RN1	
E34	FBA_DQS_RN2	
M34	FBA_DQS_RN3	
AF30	FBA_DQS_RN4	
AK31	FBA_DQS_RN5	
AM34	FBA_DQS_RN6	
AF32	FBA_DQS_RN7	

NC
NC
GF117/GK208
GK107/GF108

THE FBA_WCKBxx PINS ARE USED ONLY ON GK107 THEY ARE NC FOR GK208/GF108 /GF117

FB_CLAMP E1 — FB_CLAMP 18,20,34

R47 10KR0402

FB_DLL_AVDD K27 — FB_DLL_AVDD — 50mA — L4 30L5A-10-RH — PEX_VDD

Under GPU: C310 C0.1u10X0402_

Near GPU: C268 C22u6.3X60805-HF

2014.03.13 Stuff

2014.03.17 Change to BEAD,300hm,25%,0603,5000mA,0.010hm

FBA_CMD0	U30	FBA_CMD0	13
FBA_CMD1	T31	FBA_CMD1	13
FBA_CMD2	U29	FBA_CMD2	13
FBA_CMD3	R34	FBA_CMD3	13
FBA_CMD4	R33	FBA_CMD4	13
FBA_CMD5	U32	FBA_CMD5	13
FBA_CMD6	U33	FBA_CMD6	13
FBA_CMD7	U28	FBA_CMD7	13
FBA_CMD8	V28	FBA_CMD8	13
FBA_CMD9	V29	FBA_CMD9	13
FBA_CMD10	V30	FBA_CMD10	13
FBA_CMD11	U34	FBA_CMD11	13
FBA_CMD12	U31	FBA_CMD12	13
FBA_CMD13	V34	FBA_CMD13	13
FBA_CMD14	V33	FBA_CMD14	13
FBA_CMD15	Y32	FBA_CMD15	13
FBA_CMD16	AA31	FBA_CMD16	14
FBA_CMD17	AA29	FBA_CMD17	14
FBA_CMD18	AA28	FBA_CMD18	14
FBA_CMD19	AC34	FBA_CMD19	14
FBA_CMD20	AC33	FBA_CMD20	14
FBA_CMD21	AA32	FBA_CMD21	14
FBA_CMD22	AA33	FBA_CMD22	14
FBA_CMD23	Y28	FBA_CMD23	14
FBA_CMD24	Y29	FBA_CMD24	14
FBA_CMD25	W31	FBA_CMD25	14
FBA_CMD26	Y30	FBA_CMD26	14
FBA_CMD27	AA34	FBA_CMD27	14
FBA_CMD28	Y31	FBA_CMD28	14
FBA_CMD29	Y34	FBA_CMD29	14
FBA_CMD30	Y33	FBA_CMD30	14
FBA_CMD31	V31	FBA_CMD31	14

GDDR5 CMD Mapping Table

<0..31>	<32..63>	MEMORY
12	28	RAS*
15	31	CAS*
5	21	WE*
0	16	CS*
8	24	ABI*
10	26	A0_A10
11	27	A1_A9
2	18	A2_BA0
1	17	A3_BA3
3	19	A4_BA2
4	20	A5_BA1
7	23	A6_A11
6	22	A7_A8
9	25	A12_RFU
14	30	CKE*
13	29	RESET*

FBA_CMD_RFU0 R32 — TPJNC27

FBA_CMD_RFU1 AC32 — TPJNC28

FBVDDQ

FBA_DEBUG0 R28 — FBA_DEBUG0 R239 X_60.4R1%0402

FBA_DEBUG1 AC28 — FBA_DEBUG1 R240 X_60.4R1%0402

For debug purposes only,no-stuffed. ---Dragon 9/10

FBA_CLK0	R30	FBA_CLK0	13
FBA_CLK0	R31	FBA_CLK0#	13
FBA_CLK1	AB31	FBA_CLK1	14
FBA_CLK1	AC31	FBA_CLK1#	14

FBA_WCK01	K31	FBA_WCK01	13
FBA_WCK01	L30	FBA_WCK01#	13
FBA_WCK23	H34	FBA_WCK23	13
FBA_WCK23	J34	FBA_WCK23#	13
FBA_WCK45	AG30	FBA_WCK45	14
FBA_WCK45	AG31	FBA_WCK45#	14
FBA_WCK67	AJ34	FBA_WCK67	14
FBA_WCK67	AK34	FBA_WCK67#	14

FBA_WCKB01	J30	
FBA_WCKB01	J31	
FBA_WCKB23	J32	
FBA_WCKB23	J33	
FBA_WCKB45	AH31	
FBA_WCKB45	AJ31	
FBA_WCKB67	AJ32	
FBA_WCKB67	AJ33	

FBVDDQ

R246 X_1.3KR1%0402

R245 X_1.3KR1%0402

C328 X_C0.01u25X0402

H26 FB_VREF

FBA_PLL_AVDD J27 — 120mA — FA_PLLAVDD — L5 X_30L5A-10-RH — PEX_VDD — For N14P

L6 30L5A-10-RH — +3V3_NV — For N14E-GL

Under GPU: C378 C0.1u10X0402

Near GPU: C322 X_C1u10X7 C267 C22u6.3X60805-HF

2014.03.13 Modify

2014.03.17 Change to BEAD,300hm,25%,0603,5000mA,0.010hm

FBA CKE H FBA_CMD30

FBA CKE L FBA_CMD14

RN8 8P4R-10KR0402

FBA RST H FBA_CMD29

FBA RST L FBA_CMD13

FBVDDQ

G5C

BGA908 COMMON

3/17 FBB

ALL PINS NC FOR GF117/GK208

15	FBB_D0	G9	FBB_D0
15	FBB_D1	E9	FBB_D1
15	FBB_D2	G8	FBB_D2
15	FBB_D3	F9	FBB_D3
15	FBB_D4	E11	FBB_D4
15	FBB_D5	G11	FBB_D5
15	FBB_D6	E12	FBB_D6
15	FBB_D7	G12	FBB_D7
15	FBB_D8	G6	FBB_D8
15	FBB_D9	F5	FBB_D9
15	FBB_D10	E6	FBB_D10
15	FBB_D11	F6	FBB_D11
15	FBB_D12	F4	FBB_D12
15	FBB_D13	G4	FBB_D13
15	FBB_D14	E2	FBB_D14
15	FBB_D15	F3	FBB_D15
15	FBB_D16	C2	FBB_D16
15	FBB_D17	D4	FBB_D17
15	FBB_D18	D3	FBB_D18
15	FBB_D19	C1	FBB_D19
15	FBB_D20	B3	FBB_D20
15	FBB_D21	C4	FBB_D21
15	FBB_D22	B5	FBB_D22
15	FBB_D23	C5	FBB_D23
15	FBB_D24	A11	FBB_D24
15	FBB_D25	C11	FBB_D25
15	FBB_D26	D11	FBB_D26
15	FBB_D27	B11	FBB_D27
15	FBB_D28	D8	FBB_D28
15	FBB_D29	A8	FBB_D29
15	FBB_D30	C8	FBB_D30
15	FBB_D31	B8	FBB_D31
16	FBB_D32	F24	FBB_D32
16	FBB_D33	G23	FBB_D33
16	FBB_D34	E24	FBB_D34
16	FBB_D35	G24	FBB_D35
16	FBB_D36	D21	FBB_D36
16	FBB_D37	E21	FBB_D37
16	FBB_D38	G21	FBB_D38
16	FBB_D39	F21	FBB_D39
16	FBB_D40	G27	FBB_D40
16	FBB_D41	D27	FBB_D41
16	FBB_D42	G26	FBB_D42
16	FBB_D43	E27	FBB_D43
16	FBB_D44	E29	FBB_D44
16	FBB_D45	F29	FBB_D45
16	FBB_D46	E30	FBB_D46
16	FBB_D47	D30	FBB_D47
16	FBB_D48	A32	FBB_D48
16	FBB_D49	C31	FBB_D49
16	FBB_D50	C32	FBB_D50
16	FBB_D51	B32	FBB_D51
16	FBB_D52	D29	FBB_D52
16	FBB_D53	A29	FBB_D53
16	FBB_D54	C29	FBB_D54
16	FBB_D55	B29	FBB_D55
16	FBB_D56	B21	FBB_D56
16	FBB_D57	C23	FBB_D57
16	FBB_D58	A21	FBB_D58
16	FBB_D59	C21	FBB_D59
16	FBB_D60	B24	FBB_D60
16	FBB_D61	C24	FBB_D61
16	FBB_D62	B26	FBB_D62
16	FBB_D63	C26	FBB_D63

15	FBB_DBI0	E11	FBB_DQM0
15	FBB_DBI1	E3	FBB_DQM1
15	FBB_DBI2	A3	FBB_DQM2
15	FBB_DBI3	C9	FBB_DQM3
16	FBB_DBI4	F23	FBB_DQM4
16	FBB_DBI5	E27	FBB_DQM5
16	FBB_DBI6	C30	FBB_DQM6
16	FBB_DBI7	A24	FBB_DQM7

15	FBB_EDC0	D10	FBB_DQS_WP0
15	FBB_EDC1	D5	FBB_DQS_WP1
15	FBB_EDC2	C3	FBB_DQS_WP2
15	FBB_EDC3	B9	FBB_DQS_WP3
16	FBB_EDC4	E23	FBB_DQS_WP4
16	FBB_EDC5	E28	FBB_DQS_WP5
16	FBB_EDC6	B30	FBB_DQS_WP6
16	FBB_EDC7	A23	FBB_DQS_WP7

D9	FBB_DQS_RN0	
E4	FBB_DQS_RN1	
B2	FBB_DQS_RN2	
A9	FBB_DQS_RN3	
D22	FBB_DQS_RN4	
D28	FBB_DQS_RN5	
A30	FBB_DQS_RN6	
B23	FBB_DQS_RN7	

THE FBB_WCKBxx PINS ARE USED ONLY ON GK107 THEY ARE NC FOR GF108

NC GF108 — FBB_PLL_AVDD H17 — GK107

FBB_CMD0	D13	FBB_CMD0	15
FBB_CMD1	E14	FBB_CMD1	15
FBB_CMD2	F14	FBB_CMD2	15
FBB_CMD3	A12	FBB_CMD3	15
FBB_CMD4	B12	FBB_CMD4	15
FBB_CMD5	C14	FBB_CMD5	15
FBB_CMD6	B14	FBB_CMD6	15
FBB_CMD7	G15	FBB_CMD7	15
FBB_CMD8	F15	FBB_CMD8	15
FBB_CMD9	E15	FBB_CMD9	15
FBB_CMD10	D15	FBB_CMD10	15
FBB_CMD11	A14	FBB_CMD11	15
FBB_CMD12	D14	FBB_CMD12	15
FBB_CMD13	A15	FBB_CMD13	15
FBB_CMD14	B15	FBB_CMD14	15
FBB_CMD15	C17	FBB_CMD15	15
FBB_CMD16	D18	FBB_CMD16	16
FBB_CMD17	E18	FBB_CMD17	16
FBB_CMD18	F18	FBB_CMD18	16
FBB_CMD19	A20	FBB_CMD19	16
FBB_CMD20	B20	FBB_CMD20	16
FBB_CMD21	C18	FBB_CMD21	16
FBB_CMD22	B18	FBB_CMD22	16
FBB_CMD23	G18	FBB_CMD23	16
FBB_CMD24	G17	FBB_CMD24	16
FBB_CMD25	F17	FBB_CMD25	16
FBB_CMD26	D16	FBB_CMD26	16
FBB_CMD27	A18	FBB_CMD27	16
FBB_CMD28	D17	FBB_CMD28	16
FBB_CMD29	A17	FBB_CMD29	16
FBB_CMD30	B17	FBB_CMD30	16
FBB_CMD31	E17	FBB_CMD31	16

FBB_CMD_RFU0 C12

FBB_CMD_RFU1 C20

FBVDDQ

FBB_DEBUG0 G14 — FBB_DEBUG0 R255 X_60.4R1%0402

FBB_DEBUG1 G20 — FBB_DEBUG1 R251 X_60.4R1%0402

For debug purposes only,no-stuffed. ---Dragon 9/10

FBB_CLK0	D12	FBB_CLK0	15
FBB_CLK0	E12	FBB_CLK0#	15
FBB_CLK1	E20	FBB_CLK1	16
FBB_CLK1	F20	FBB_CLK1#	16

FBB_WCK01	F8	FBB_WCK01	15
FBB_WCK01	E8	FBB_WCK01#	15
FBB_WCK23	A5	FBB_WCK23	15
FBB_WCK23	A6	FBB_WCK23#	15
FBB_WCK45	D24	FBB_WCK45	16
FBB_WCK45	D25	FBB_WCK45#	16
FBB_WCK67	B27	FBB_WCK67	16
FBB_WCK67	C27	FBB_WCK67#	16

FBB_WCKB01	D6	
FBB_WCKB01	D7	
FBB_WCKB23	C6	
FBB_WCKB23	B6	
FBB_WCKB45	F26	
FBB_WCKB45	E26	
FBB_WCKB67	A26	
FBB_WCKB67	A27	

FBVDDQ

120mA — FA_PLLAVDD

C330

Under GPU: C0.1u10X0402

FBB CKE H FBB_CMD30

FBB CKE L FBB_CMD14

RN9 8P4R-10KR0402

FBB RST H FBB_CMD29

FBB RST L FBB_CMD13

FBVDDQ

MICRO-STAR INT'L CO.,LTD.

Title: N15P-Q3_MEM Interface

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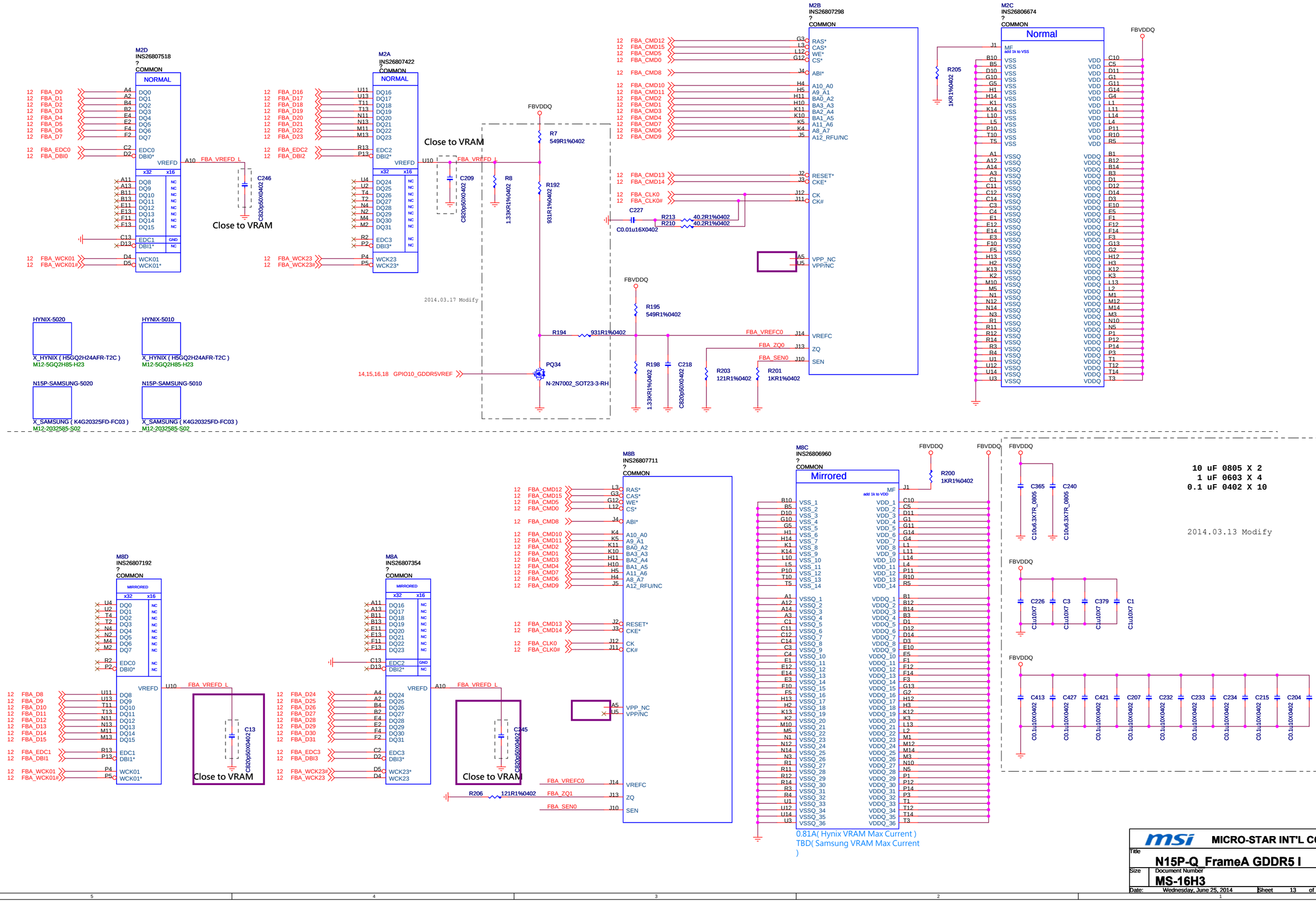
M2D
INS26807518
?
COMMON
NORMAL
M2A
INS26807422
?
COMMON
NORMAL
M2B
INS26807298
?
COMMON
M2C
INS26806674
?
COMMON
Normal
FBVDDQ
Close to VRAM
C246
C820p50X0402
C209
R7
549R1%0402
R192
931R1%0402
R8
1.33KR1%0402
R194
931R1%0402
R195
549R1%0402
R198
1.33KR1%0402
C218
C820p50X0402
R203
121R1%0402
R201
1KR1%0402
R205
1KR1%0402
C227
C0.01u16X0402
R213
40.2R1%0402
R210
40.2R1%0402
PQ34
N-2N7002_SOT23-3-RH
14,15,16,18 GPIO10_GDDR5VREF
FBA_VREFD_L
FBA_VREFC0
FBA_ZQ0
FBA_SEN0
2014.03.17 Modify
HYNIX-5020
X_HYNIX (H5GQ2H24AFR-T2C)
M12-5GQ2H85-H23
HYNIX-5010
X_HYNIX (H5GQ2H24AFR-T2C)
M12-5GQ2H85-H23
N15P-SAMSUNG-5020
X_SAMSUNG (K4G20325FD-FC03)
M12-2032585-S02
N15P-SAMSUNG-5010
X_SAMSUNG (K4G20325FD-FC03)
M12-2032585-S02
M8D
INS26807192
?
COMMON
MIRRORED
M8A
INS26807354
?
COMMON
MIRRORED
M8B
INS26807711
?
COMMON
M8C
INS26806960
?
COMMON
Mirrored
R206
121R1%0402
R200
1KR1%0402
10 uF 0805 X 2
1 uF 0603 X 4
0.1 uF 0402 X 10
2014.03.13 Modify
0.81A(Hynix VRAM Max Current)
TBD(Samsung VRAM Max Current)
MICRO-STAR INT'L CO.,LTD.
Title
N15P-Q FrameA GDDR5 I
Size
Document Number
MS-16H3
Rev
1.0
Date: Wednesday, June 25, 2014
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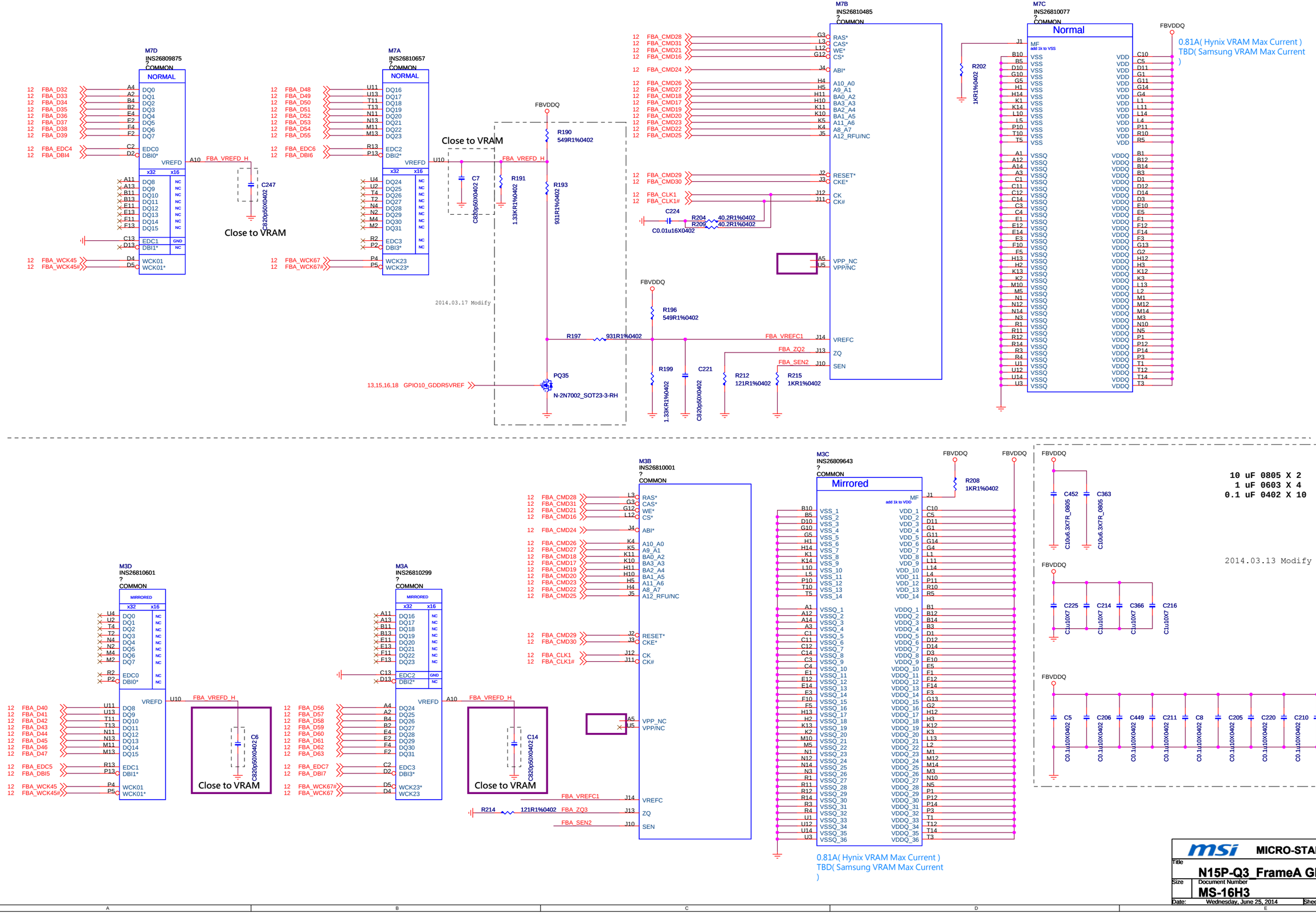

MICRO-STAR INT'L CO.,LTD.	
Title	N15P-Q3_FrameA GDDR5 II
Size	Document Number: MS-16H3 — Rev: 1.0
Date:	Wednesday, June 25, 2014 — Sheet 14 of 69

M5D
INS26812648
?
COMMON
NORMAL
x32 x16
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7
EDC0 DBI0*
VREFD
DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15
EDC1 DBI1*
WCK01 WCK01*
FBB_D0 FBB_D1 FBB_D2 FBB_D3 FBB_D4 FBB_D5 FBB_D6 FBB_D7
FBB_EDC0 FBB_DBI0
FBB_WCK01 FBB_WCK01#
A10 FBB_VREFD_L
C65 C820p50X0402
Close to VRAM

M5A
INS26813536
?
COMMON
NORMAL
x32 x16
DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23
EDC2 DBI2*
VREFD
DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31
EDC3 DBI3*
WCK23 WCK23*
FBB_D16 FBB_D17 FBB_D18 FBB_D19 FBB_D20 FBB_D21 FBB_D22 FBB_D23
FBB_EDC2 FBB_DBI2
FBB_WCK23 FBB_WCK23#
U10 FBB_VREFD_L
C431 C820p50X0402
R287 1.33KR1%0402
Close to VRAM

FBVDDQ
R289 549R1%0402
R290 931R1%0402
R299 931R1%0402
PQ37 N-2N7002_SOT23-3-RH
13,14,16,18 GPIO10_GDDR5VREF
R291 549R1%0402
R293 1.33KR1%0402
C446 C820p50X0402
R298 121R1%0402
R297 1KR1%0402

M5B
INS26812542
?
COMMON
RAS* CAS* WE* CS*
ABI*
A10_A0 A9_A1 BA0_A2 BA3_A3 BA2_A4 BA1_A5 A11_A6 A8_A7 A12_RFU/NC
RESET* CKE*
CK CK#
VPP_NC VPP/NC
VREFC
ZQ
SEN
FBB_CMD12 FBB_CMD15 FBB_CMD5 FBB_CMD0
FBB_CMD8
FBB_CMD10 FBB_CMD11 FBB_CMD2 FBB_CMD1 FBB_CMD3 FBB_CMD4 FBB_CMD7 FBB_CMD6 FBB_CMD9
FBB_CMD13 FBB_CMD14
FBB_CLK0 FBB_CLK0#
C447 C0.01u16X0402
R294 40.2R1%0402
R295 40.2R1%0402
FBB_VREFC0
FBB_ZQ0
FBB_SEN0

M5C
INS26812744
?
COMMON
Normal
MF
add 1k to VSS
R253 1KR1%0402
VSS VSSQ VDD VDDQ
FBVDDQ
0.81A(Hynix VRAM Max Current)
TBD(Samsung VRAM Max Current)

2014.03.17 Modify

M10D
INS26813032
?
COMMON
MIRRORED
x32 x16
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7
EDC0 DBI0*
VREFD
DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15
EDC1 DBI1*
WCK01 WCK01*
FBB_D8 FBB_D9 FBB_D10 FBB_D11 FBB_D12 FBB_D13 FBB_D14 FBB_D15
FBB_EDC1 FBB_DBI1
FBB_WCK01 FBB_WCK01#
U10 FBB_VREFD_L
C66 C820p50X0402
Close to VRAM

M10A
INS26813470
?
COMMON
MIRRORED
x32 x16
DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23
EDC2 DBI2*
VREFD
DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31
EDC3 DBI3*
WCK23* WCK23
FBB_D24 FBB_D25 FBB_D26 FBB_D27 FBB_D28 FBB_D29 FBB_D30 FBB_D31
FBB_EDC3 FBB_DBI3
FBB_WCK23# FBB_WCK23
A10 FBB_VREFD_L
C433 C820p50X0402
Close to VRAM
R296 121R1%0402
FBB_ZQ1

M10B
INS26812976
?
COMMON
RAS* CAS* WE* CS*
ABI*
A10_A0 A9_A1 BA0_A2 BA3_A3 BA2_A4 BA1_A5 A11_A6 A8_A7 A12_RFU/NC
RESET* CKE*
CK CK#
VPP_NC VPP/NC
VREFC
ZQ
SEN
FBB_CMD12 FBB_CMD15 FBB_CMD5 FBB_CMD0
FBB_CMD8
FBB_CMD10 FBB_CMD11 FBB_CMD2 FBB_CMD1 FBB_CMD3 FBB_CMD4 FBB_CMD7 FBB_CMD6 FBB_CMD9
FBB_CMD13 FBB_CMD14
FBB_CLK0 FBB_CLK0#
FBB_VREFC0
FBB_ZQ0
FBB_SEN0

M10C
INS26813158
?
COMMON
Mirrored
MF
add 1k to VDD
R254 1KR1%0402
VSS_1 VSS_2 VSS_3 VSS_4 VSS_5 VSS_6 VSS_7 VSS_8 VSS_9 VSS_10 VSS_11 VSS_12 VSS_13 VSS_14
VSSQ_1 VSSQ_2 VSSQ_3 VSSQ_4 VSSQ_5 VSSQ_6 VSSQ_7 VSSQ_8 VSSQ_9 VSSQ_10 VSSQ_11 VSSQ_12 VSSQ_13 VSSQ_14 VSSQ_15 VSSQ_16 VSSQ_17 VSSQ_18 VSSQ_19 VSSQ_20 VSSQ_21 VSSQ_22 VSSQ_23 VSSQ_24 VSSQ_25 VSSQ_26 VSSQ_27 VSSQ_28 VSSQ_29 VSSQ_30 VSSQ_31 VSSQ_32 VSSQ_33 VSSQ_34 VSSQ_35 VSSQ_36
VDD_1 VDD_2 VDD_3 VDD_4 VDD_5 VDD_6 VDD_7 VDD_8 VDD_9 VDD_10 VDD_11 VDD_12 VDD_13 VDD_14
VDDQ_1 VDDQ_2 VDDQ_3 VDDQ_4 VDDQ_5 VDDQ_6 VDDQ_7 VDDQ_8 VDDQ_9 VDDQ_10 VDDQ_11 VDDQ_12 VDDQ_13 VDDQ_14 VDDQ_15 VDDQ_16 VDDQ_17 VDDQ_18 VDDQ_19 VDDQ_20 VDDQ_21 VDDQ_22 VDDQ_23 VDDQ_24 VDDQ_25 VDDQ_26 VDDQ_27 VDDQ_28 VDDQ_29 VDDQ_30 VDDQ_31 VDDQ_32 VDDQ_33 VDDQ_34 VDDQ_35 VDDQ_36
FBVDDQ
0.81A(Hynix VRAM Max Current)
TBD(Samsung VRAM Max Current)

FBVDDQ
C223 C10u6.3X7R_0805
C229 C10u6.3X7R_0805
FBVDDQ
C383 C1u10X7
C212 C1u10X7
C213 C1u10X7
C219 C1u10X7
FBVDDQ
C448 C0.1u10X0402
C9 C0.1u10X0402
C4 C0.1u10X0402
C208 C0.1u10X0402
C238 C0.1u10X0402
C259 C0.1u10X0402
C217 C0.1u10X0402
C450 C0.1u10X0402
C376 C0.1u10X0402
C242 C0.1u10X0402

10 uF 0805 X 2
1 uF 0603 X 4
0.1 uF 0402 X 10

2014.03.13 Modify

MICRO-STAR INT'L CO.,LTD.
Title: N15P-Q3_FrameC GDDR5 I
Size: Document Number: MS-16H3
Rev: 1.0
Date: Wednesday, June 25, 2014
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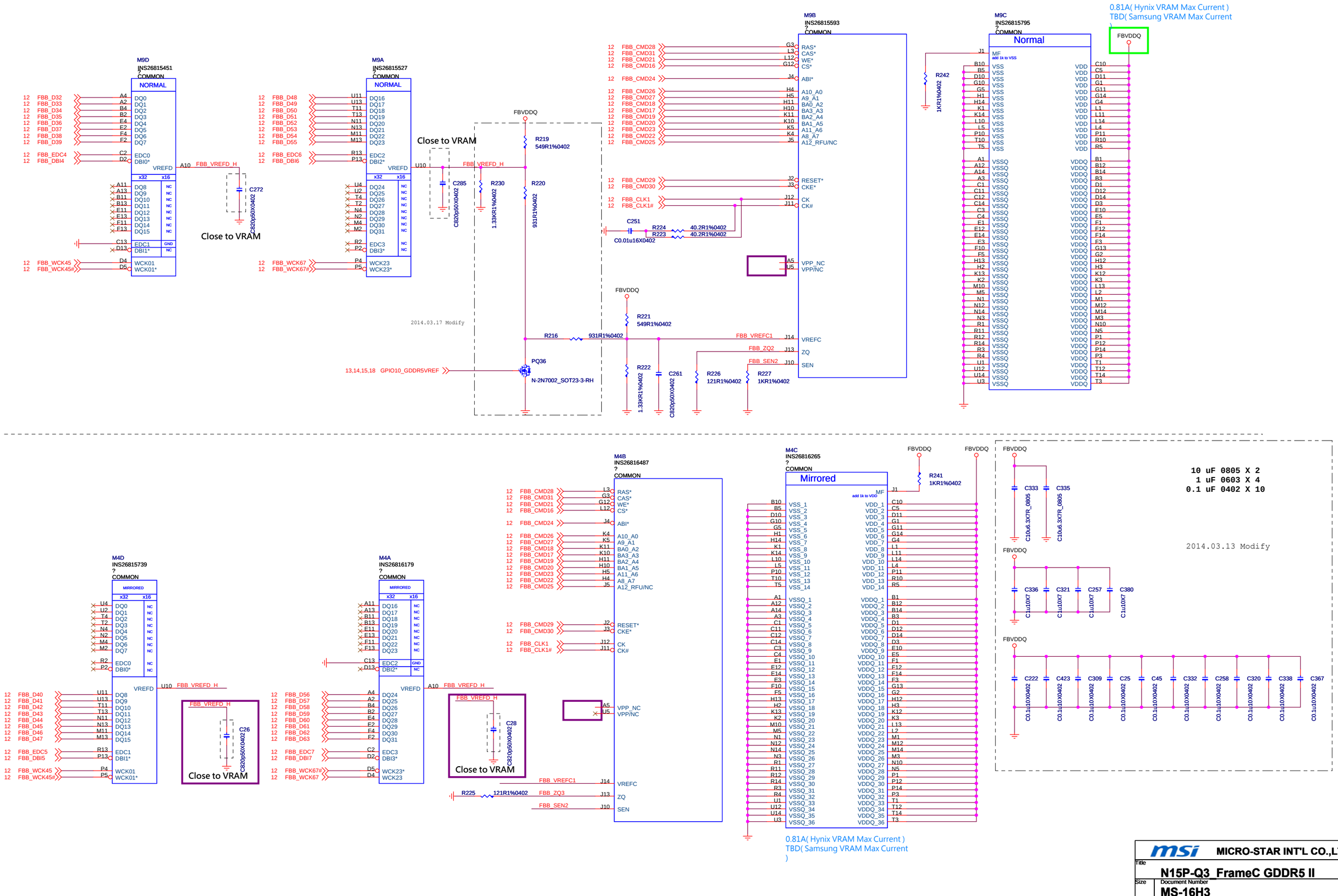

MICRO-STAR INT'L CO.,LTD.			
Title	N15P-Q3_FrameC GDDR5 II		
Size	Document Number MS-16H3		Rev 1.0
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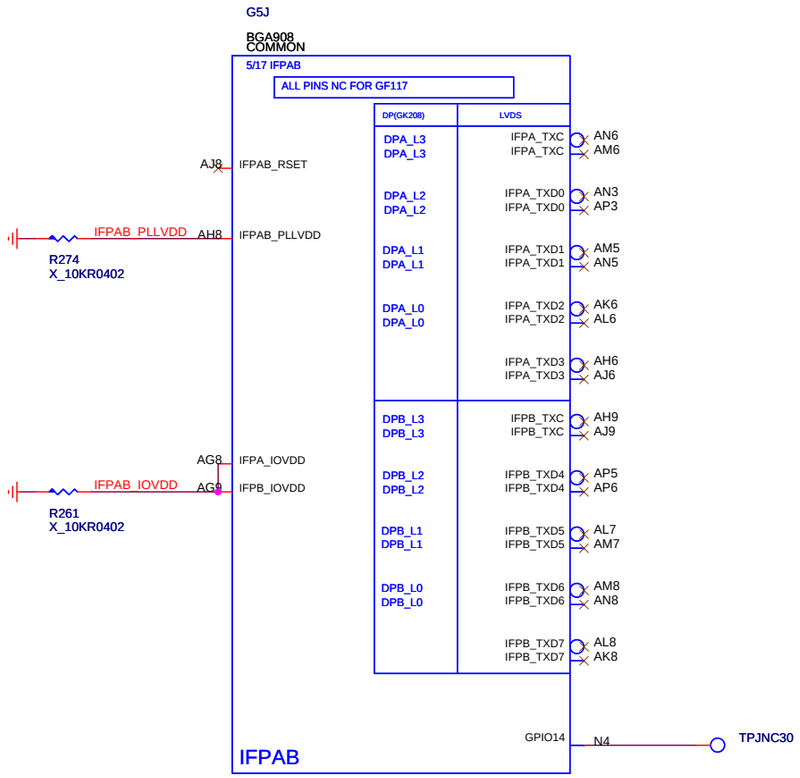
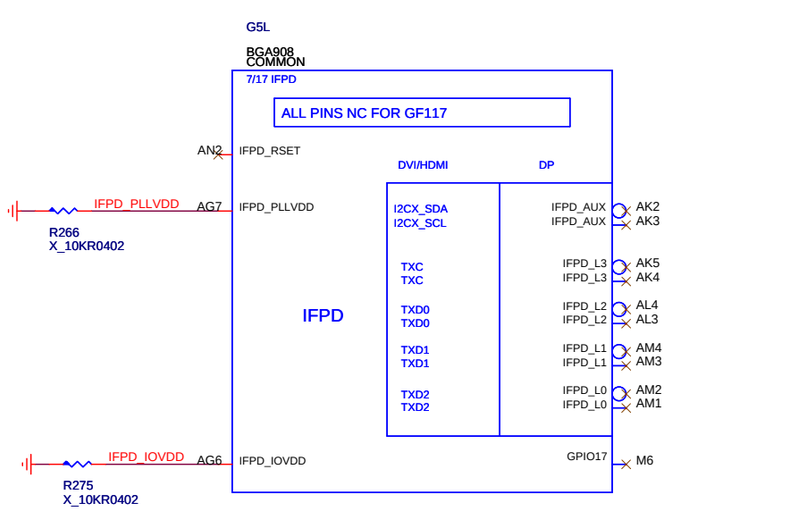
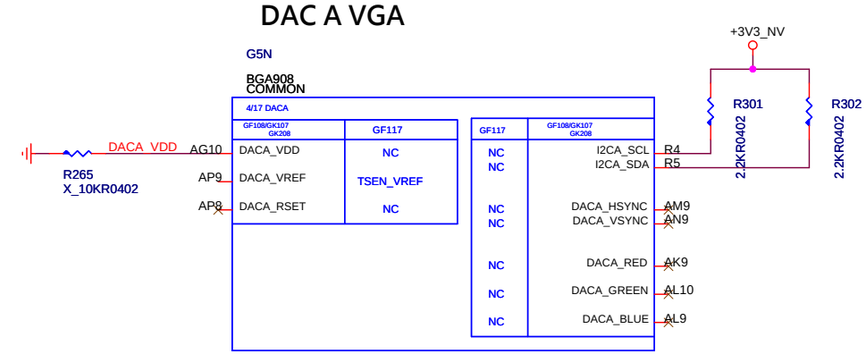
IFP A/B LVDSDual Link



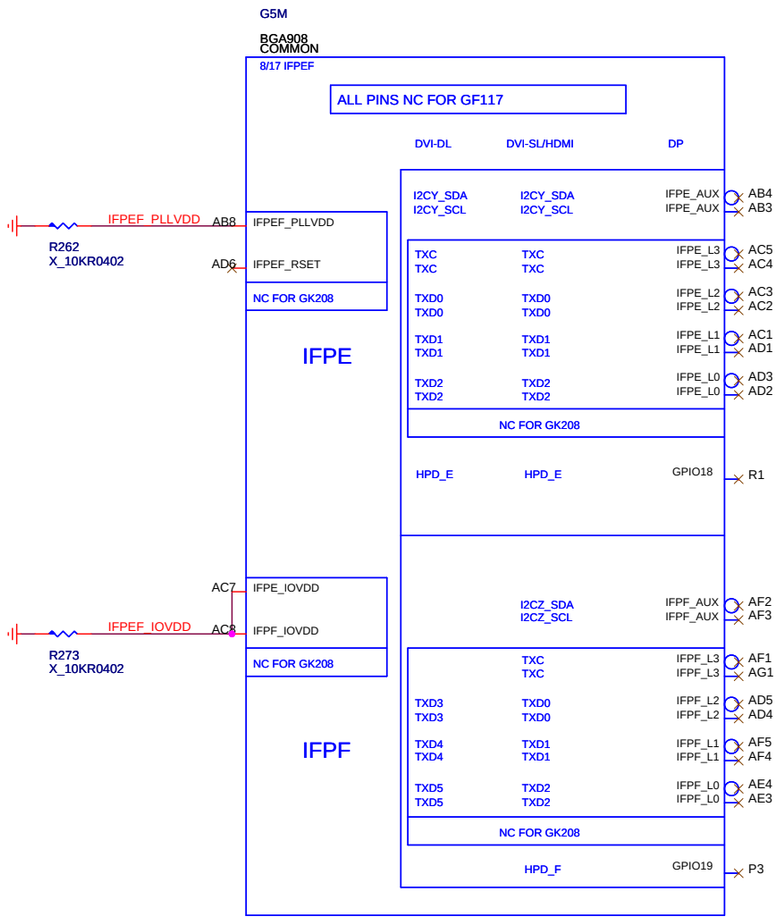
IFP D Dual Mode DP



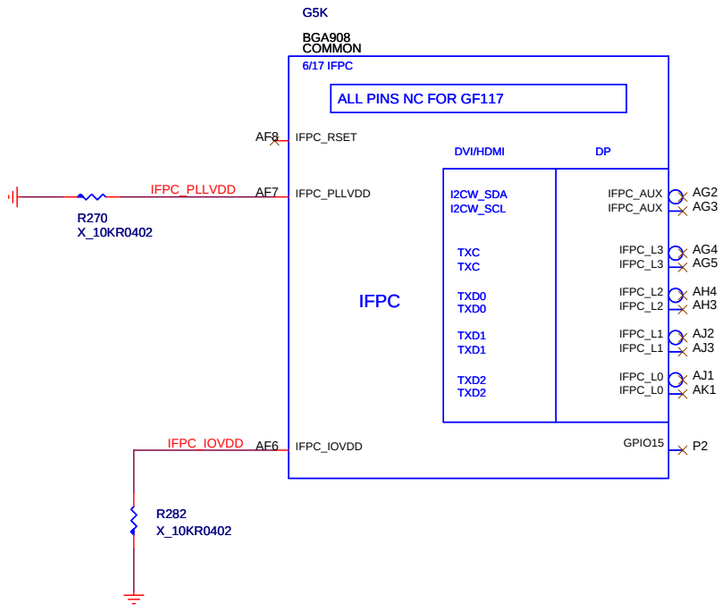
DAC A VGA



IFP E/F Dual Link TMDS DVI-I



IFP C Native HDMI OR DP



MSI	MICRO-STAR INT'L CO.,LTD.	
Title	N15P-Q3_Display Interface	
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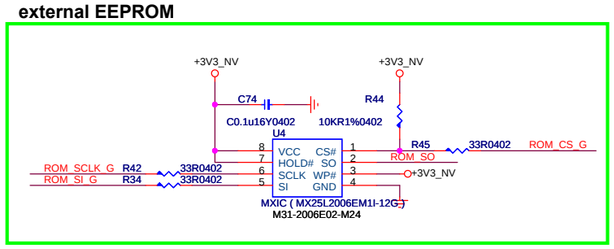
external EEPROM



Item	Location	N15P-Q3
Strap Mode	R3365	MULTISTRAP_REF_GND,40.2K PD to GND
Device ID		0x11FC
Package		GB4-128
Memory Type		GDDR5
ROM_SI	R3175	0x4, Hynix 2G, 24.9kohm PD
	R3175	0x7, Samsung 2G, 45kohm PD
ROM_SO	R3193	0x8, 5kohm pull up
ROM_SCLK	R3179	0x1110,35kohm PU(with ROM)
Strap0	R3170	45kohm pull up
Strap1	R3180	5kohm pull down
Strap2	R3171	DID,0x1100, 24.9kohm PU
Strap3	R3188	0x0 for Optimus, 5kohm pull down
Strap4	R3183	0x0111, 45kohm pull down

R170-N15P-GT
X_49.9KR1%0402
R11-4992T12-W08

+3V3_NV
G5P
BGA908 COMMON
12/17 MISC2
R48 X_20KR1%0402
R280 X_45.3KR1%0402
R267 24.9KR1%0402
R256 X_20KR1%0402
R272 45.3KR1%0402
STRAP0 J2 STRAP0
STRAP1 J7 STRAP1
STRAP2 J6 STRAP2
STRAP3 J5 STRAP3
STRAP4 J3 STRAP4
NC NC
GK107/GF117 GK208 GF108
R35 45.3KR1%0402
R268 4.99KR1%0402
R278 X_20KR1%0402
R263 4.99KR1%0402
R283 X_20KR1%0402
2014.03.13 Change to 4.99K 1%
J1 MULTI_STRAP_REF0_GND
R36 40.2KR1%0402
ROM_CS H6 ROM_CS_G
ROM_SI H5 ROM_SI_G
ROM_SO H7 ROM_SO
ROM_SCLK H4 ROM_SCLK_G
BUFRST L2
CEC L3
CEC IS NC FOR GK107/GK208/GF117
+3V3_NV
R288 X_5.1KR1%0402
R258 4.99KR1%0402
R307 34.8KR1%0402
2014.03.13 Change to 4.99K 1%
R175-N15P-GT
X_4.99KR1%0402
R11-4991T12-W08
R279 24.9KR1%0402
R264 X_5.1KR1%0402
R300 X_34.8KR1%0402
R177-N15P-GT
X_4.99KR1%0402
R11-4991T12-W08
2014.03.14 Change to 24.9K 1% for Hynix H5GC2H24BFR-T2C memory

BOM Option :
Hynix VRAM : R279 24.9K P/N R11-2492T12-W08
Samsung VRAM : R279 45.3K P/N R11-4532T12-W08

R171-N14P
X_24.9KR1%0402
R11-2492T12-W08
R175-HYNIX
X_34.8KR1%0402
R11-3482T12-W08
R165-N15P-GT
X_10KR0402
R11-0103012-W08

78mA
PEX_VDD
BEAD-30Ohm-N15P-GT
X_30L5A-10-RH
L02-3008043-M26
2014.03.13 Change to 30 Ohm Bead
L8
30L5A-10-RH
Routing 16mil wide.
C428 C22u4X6-HF
C420 C0.1u10X0402

112mA
PEX_VDD
L7
180L230mA-300-RH
2014.03.13 Stuff
C439 C22u6.3X6080S-HF
2014.03.13 Add
C435 C4.7u6.3X6
C432 C0.1u10X0402
C429 C0.1u10X0402

G5O
BGA908 COMMON
11/17 XTAL_PLL
GPU_PLLVDD AD8 PLLVDD
AE8 SP_PLLVDD
GPU_SP_PLLVDD AD7 VID_PLLVDD
NC
GK208/GK107 GF108 GF117
H1 XTAL_SSIN
H3 XTAL_IN
XTAL_OUTBUFF J4
XTAL_OUT H2
R33 10KR1%0402
R286 10KR1%0402
Y1 27MHz
XTALIN 1 2 XTALOUT
C71 C18p50N0402
C72 C18p50N0402
2014.03.13 Change to 18pF

34 SMB_CLK_EC
34 SMB_DATA_EC
Q2
D2 G2 S2
D1 G1 S1
NN-2N7002DW-7-F_SOT363-6-RH
I2CS_SCL
I2CS_SDA
C79 C0.1u10X0402
DGPU_PWRGD 11,20,27,34,52
Add 0.1U CAP for DGPU_PWRGD glitch. ---Dragon 12/19

+3V3_NV
2014.03.13 Change to 10k Ohm
RN1 8P4R-2.2KR0402-HF
R304 10KR0402
R303 10KR0402
R50 100KR0402
R38 100KR0402
R162-N15P-GT
X_10KR0402
R11-0103012-W08
R163-N15P-GT
X_100KR0402
R11-0104042-W08

G5Q
BGA908 COMMON
10/19 MISC1
I2CS_SCL T4 I2CS_SCL
I2CS_SDA T3 I2CS_SDA
I2CC_SCL R2 I2CC_SCL_G
I2CC_SDA R3 I2CC_SDA_G
I2CB_SCL R7 I2CB_SCL_G
I2CB_SDA R6 I2CB_SDA_G
NC NC
GF117 GK107/GF108 GK208
K4 THERMDN
K3 THERMDP
The FB_CLAMP signal holds the GPU frame-buffer in self-refresh,even when the GPU core power rails are off. ---N14X DG
TPJNC5
TPJNC6
JTAG_TCK AM10 JTAG_TCK
JTAG_TMS AP11 JTAG_TMS
JTAG_TDI AM11 JTAG_TDI
JTAG_TDO AP12 JTAG_TDO
JTAG_TRST# AN11 JTAG_TRST
R24 10KR1%0402
JTAG_TCK
JTAG_TDI
R25 10KR1%0402
R23 10KR1%0402
GPIO0 P6
GPIO1 M3
GPIO2 L6
GPIO3 P5
GPIO4 R7
GPIO5 L7
GPIO6 M7
GPIO7 N8
GPIO8 M1
GPIO9 M2
GPIO10 L1
GPIO11 M5
GPIO12 N3
GPIO13 M4
GPIO16 R8
GPIO20 R4
GPIO21 R1
X_0R0402 R309
FB_CLAMP 12,20,34
20140319 add for no GC6
GK208 OVERT
FB_CLMP_TGL_REQ# 34
GPIO8_THERM_SHDWN_N
GFX_ALERT#
GPIO10_GDDR5VREF 13,14,15,16
GPIO11_GPUVID 51
GPIO13_NVVDD_PSI# 51
2014.03.13 Change net name
GPU_ACIN_OK
R37 100KR0402
R39 10KR1%0402
R46 X_0R1%0402
R53 0R1%0402
+3V3_NV
GPU_ACIN 47
GPU_ACIN1 34
GPIO12:
AC MODE : HIGH
DC MODE : LOW
GPIO16 NC NC GPIO16
GPIO20 NC NC NC
GPIO8 NC NC NC
GK208 GF117 GK107 GF108
Stuff R163&PQ10 for performance issue. ---Dragon 12/19
+3V3_NV
R49 10KR0402
2014.03.13 Change net name GPIO13_NVVDD_PSI#
10K pull up to enable two phase.
----N14X DG.

Pin Name	Normal function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	FB_CLAMP_MON	I	FB Clamp monitor	
GPIO1	NC	O		
GPIO2	NC	O		
GPIO3	NC	O		
GPIO4	NC	O		
GPIO5	NC	O		
GPIO6	FB_CLAMP_TGL_REQ	O	FB Clamp toggle request	
GPIO7	NC	O		
GPIO8	OVERT	I	Thermal Over Temperature	100K pull-up
GPIO9	ALERT	I/O	Active Low Thermal Alert	100K pull-up
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	PWM_VID	O	GPU Core VDD PWM control signal	
GPIO12	PWR_LEVEL	I	AC power detect	100K pull-up
GPIO13	SPI	O	Phase Shedding	10K pull-up
GPIO14	NC	I		
GPIO15	NC	I		
GPIO16	NC	O		
GPIO17	NC	I		
GPIO18	NC	I		
GPIO19	NC	I		
NC	NC			

MICRO-STAR INT'L CO.,LTD.

Title: N15P-Q3_Thermal & GPIO

Size: | Document Number: MS-16H3 | Rev: 1.0

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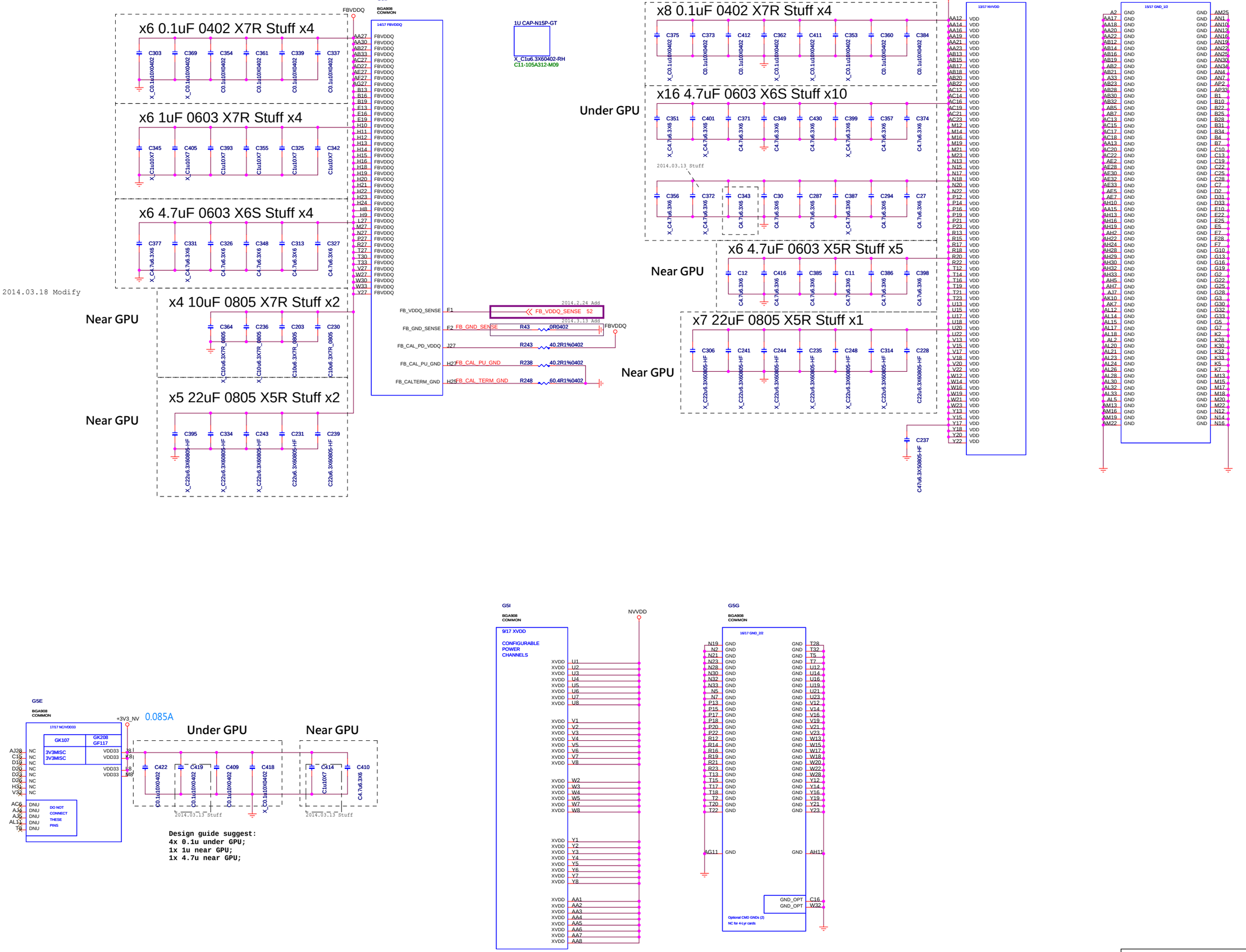


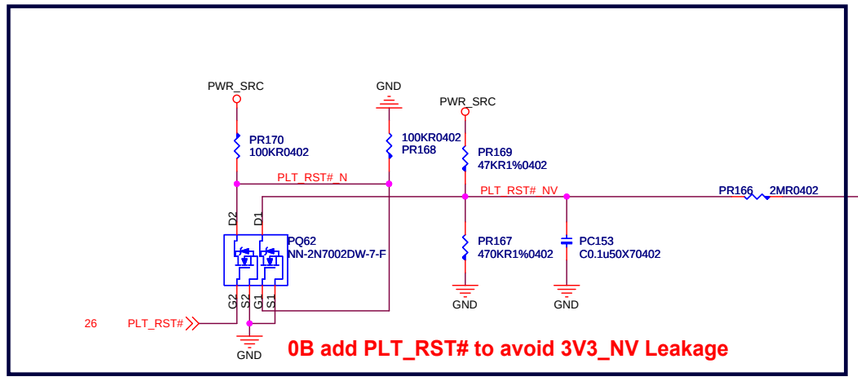
MICRO-STAR INT'L CO.,LTD.

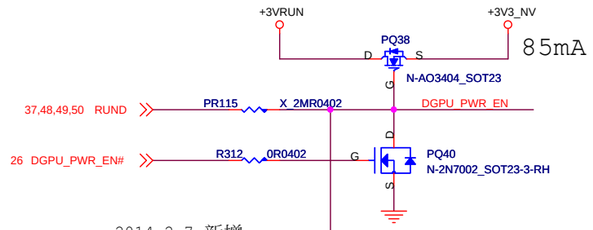
Title: N15P-Q3 Power & GND

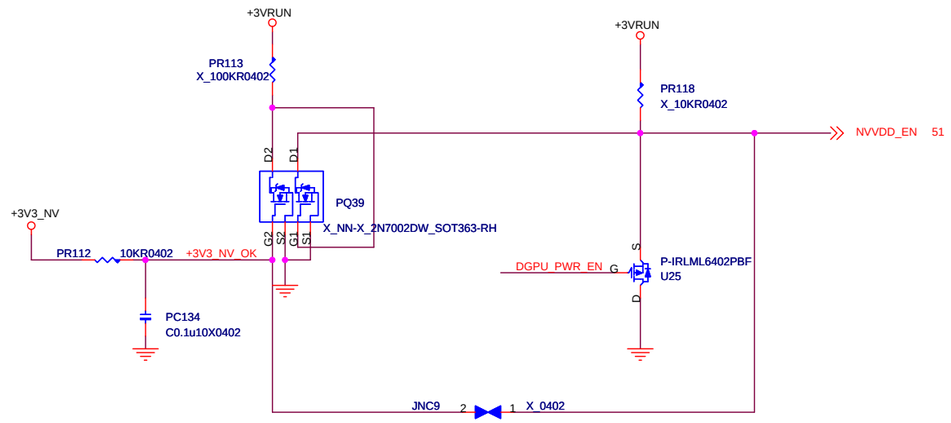
Size: | Document Number: MS-16H3 | Rev: 1.0

Date: Wednesday, June 25, 2014 | Sheet 19 of 69

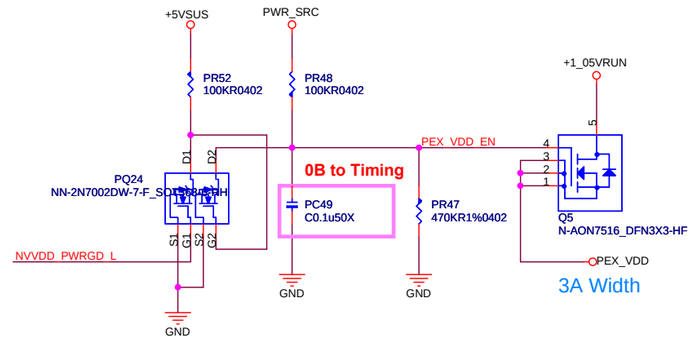
DGPU_Power Control

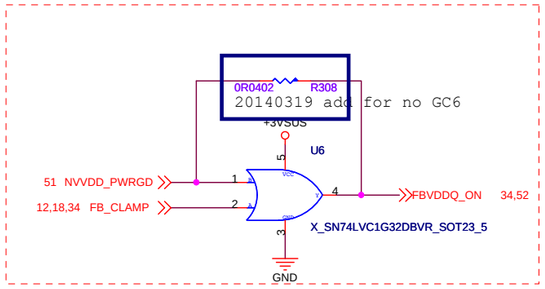


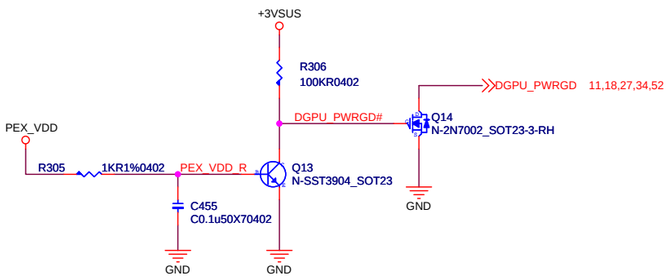




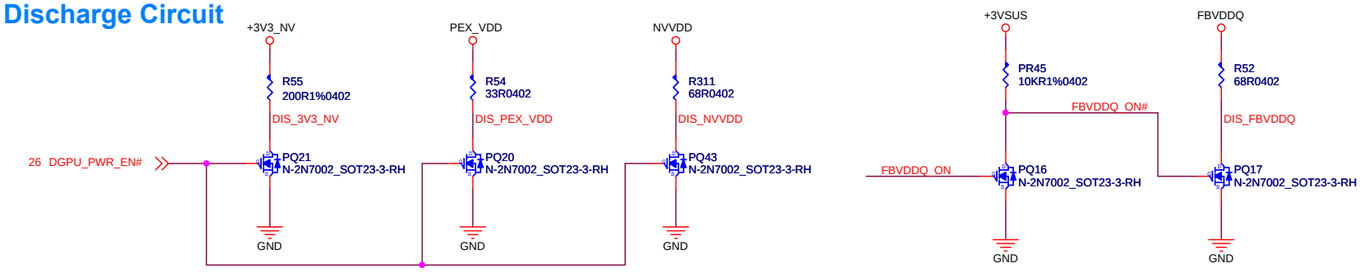
PEX_VDD

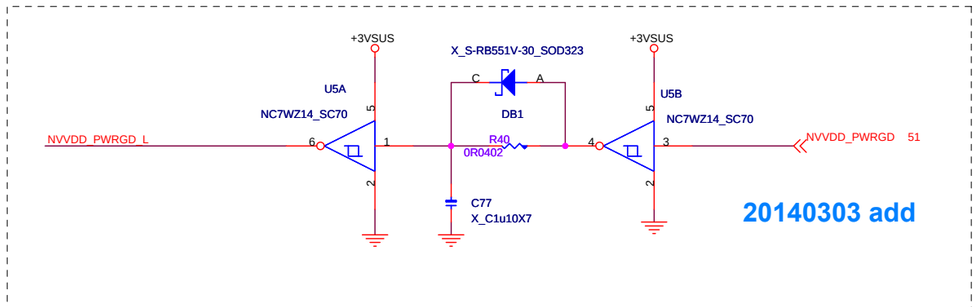






Discharge Circuit





MICRO-STAR INT'L CO.,LTD.			
Title: N15P-Q3_Power Control			
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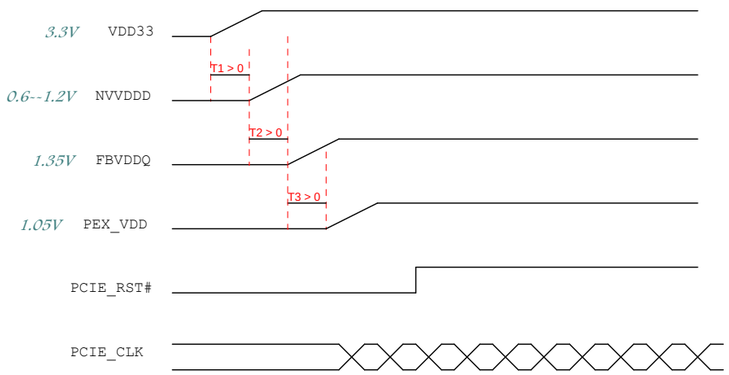
GPU POWER ON SEQUENCE



NOTES: The ramp time for any rail must be more than 40 us.
The total time for all rails to ramp up should be within 6ms.
A power rail has to ramp up to 90% before the next rail in sequence can start ramping up.
No signal should be applied to the GPU before the power rails are fully ramped

NOTES: For optimus system, VDD33 usually drops down earlier than NVVDD and FBVDDQ.

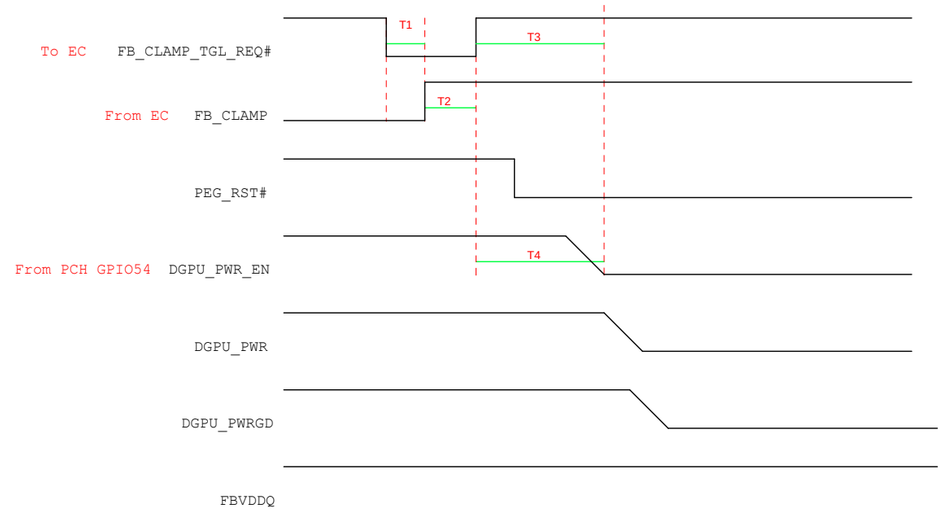
NOTES: All rails must be powered off within 10 ms from the first rail powering off.

GC6 TIMING

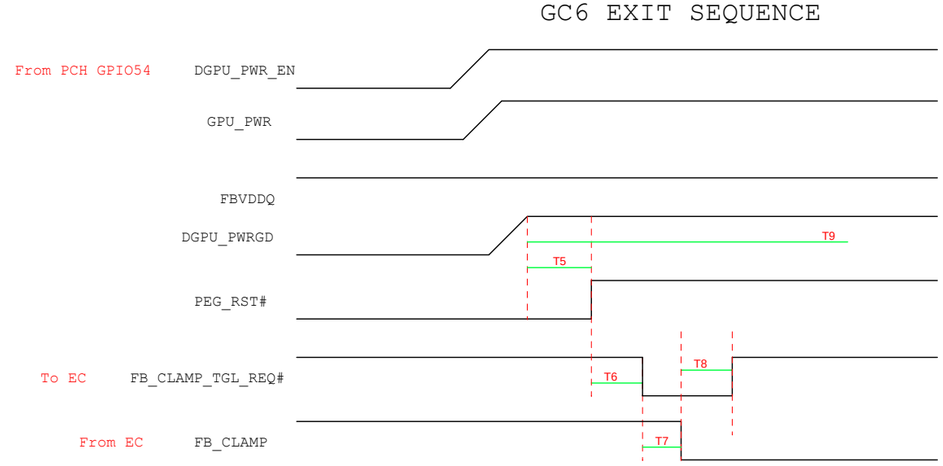
	Min	Max	Unit	Description
T1	0	10	mS	GPU asserts toggle request to GB_CLAMP assertion
T2	0	1	mS	Assertion of FB_CLAMP to de-assertion of toggle request
T3	0	10	mS	De-assertion of toggle request to GPU PWR_EN=0
T4	0.01	1	mS	PEX reset assertion to GPU PWR_EN de-assertion
T5	0.1	5	mS	GPU power stable to de-assertion of PEX reset
T6	3.3		mS	De-assertion of PEX reset to toggle request assertion
T7	0	1	mS	Assertion of toggle request to de-assertion of FB_CLAMP
T8	0	1	mS	De-assertion of FB_CLAMP to de-assertion of toggle request
T9	TBD	TBD	mS	GPU power enable to GPU ready for normal operatioon

Notes: *System designers should minimize T1,T3,T4,T5,T6,and T7 to increase the time spent in GC6.
This increased GC6 residency will improve both power savings and user experience.
**If10 ms expirs for T1, the GPU will de-assert FB_CLAMP_TGL_REQ# and abort the GC6 entry procedure.
FB_CLAMP should never assert outside an FB_CLAMP_TGL_REQ# handshake.

GC6 ENTRY SEQUENCE(NOT support)



GC6 EXIT SEQUENCE



MICRO-STAR INT'L CO.,LTD.

Title	N15P-Q3_Power Sequence	
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Date: Wednesday, June 25, 2014	Sheet 21 of 69	

Lynx Point (HDA/JTAG/SATA)

SKU	High Speed SATA I/O Ports					
	SATA-0	SATA-1	SATA-2	SATA-3	SATA-4	SATA-5
HM87	GEN3	GEN3	GEN2	GEN2	GEN3	GEN3
HM86	GEN2	N/A	GEN2	N/A	GEN3	GEN3

+3VALW
D5
S-BAT54C_SOT23
RTCVCC
R72 20KR1%0402
C577 C1u25X0402
C98 C1u25X0402
EC13 X_C15p50N0402
R415 1KR1%0402
CON1
R71 20KR1%0402
C97 C1u25X0402
R74 1MR1%0402
RTC_P3
BAT1
BCR1220H2.8AM1KB
D06-0105001-K26
BH1X2#S-1.25PITCH_BLACK
N32-10200Q0-A81
SWAP

Y4
Main source: D04-0305500-S35
2nd source: D04-0305400-T16

2014.2.17 Changed

C586 C15p50N0402
Y7
32.768KHZ12.5p_S-RH-21
D04-0305500-S35
OSC_3_2X1_5_1
C595 C15p50N0402
R395 10MR1%0402
RTCX1_JNC
RTCX2_JNC
SRTCRST#
SM_INTRUDER#
RTCVCC R376 330KR0402
PCH_INTVRMEN
RTCRST#
34 RTCRST#

U7A
LPT_PCH_M_EDS

B5	RTCX1	RTC
B4	RTCX2	
B9	SRTCRST#	
A8	INTRUDER#	
G10	INTVRMEN	
D9	RTCRST#	
B25	HDA_BCLK	AZALIA
A22	HDA_SYNC	
AL10	SPKR	
C24	HDA_RST#	
L22	HDA_SDI0	
K22	HDA_SDI1	
G22	HDA_SDI2	
F22	HDA_SDI3	
A24	HDA_SDO	
B17	DOCKEN#/GPIO33	
C22	HDA_DOCK_RST#/GPIO13	
AB3	JTAG_TCK	JTAG
AD1	JTAG_TMS	
AE2	JTAG_TDI	
AD3	JTAG_TDO	
F8	TP25	
C26	TP22	
AB6	TP20	

HDA_BIT_CLK_PCH_R
HDA_SYNC_PCH_R
39 HDA_SPKR
HDA_RST#_PCH_R
39 CODEC_HDA_SDIN0
HDA_SDOUT_PCH_R

39 CODEC_HDA_BIT_CLK
39 CODEC_HDA_SDOUT
39 CODEC_HDA_RST#
39 CODEC_HDA_SYNC
RN2
8P4R-33R0402
EC5 X_C10p50N0402
EC8 X_C10p50N0402
EC9 X_C10p50N0402
EC10 X_C10p50N0402
34 FLASH_SECURITY
R66 1KR1%0402

Flash Descriptor Security Protect	
HDA_SDO	Low = Enable High = Disable

SATA_RXN_0	BC8	SATA0RXN 43
SATA_RXP_0	BE8	SATA0RXP 43
SATA_TXN_0	AW8	SATA0TXN 43
SATA_TXP_0	AY8	SATA0TXP 43
SATA_RXN_1	BC10	SATA1RXN 43
SATA_RXP_1	BE10	SATA1RXP 43
SATA_TXN_1	AV10	SATA1TXN 43
SATA_TXP_1	AW10	SATA1TXP 43
SATA_RXN_2	BB9	SATA4RXN 42
SATA_RXP_2	BD9	SATA4RXP 42
SATA_TXN_2	AY13	SATA4TXN 42
SATA_TXP_2	AW13	SATA4TXP 42
SATA_RXN_3	BC12	
SATA_RXP_3	BE12	
SATA_TXN_3	AR13	
SATA_TXP_3	AT13	
SATA_RXN4/PERN1	BD13	
SATA_RXP4/PERP1	BB13	
SATA_TXN4/PETN1	AV15	
SATA_TXP4/PETP1	AW15	
SATA_RXN5/PERN2	BC14	
SATA_RXP5/PERP2	BE14	
SATA_TXN5/PETN2	AP15	
SATA_TXP5/PETP2	AR15	
SATA_RCOMP	AY5	SATAICOMP R384 7.5KR1%0402 +1_5VRUN
SATALED#	AP3	LEDHDD# 40
SATA0GP/GPIO21	AT1	SATA0GP R94 10KR1%0402 +3VRUN / R85 10KR1%0402
SATA1GP/GPIO19	AU2	BBS_BIT0 R82 10KR1%0402 +3VRUN
SATA_IREF	BD4	+1_5VRUN
TP9	BA2	
TP8	BB2	

SATA

m-SATA SSD
m-SATA SSD
SATA GEN3
HDD
SATA GEN2

1 OF 11

SPK	The Signal has a weak internal pull-down Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Panther Point will disable the TCO Timer system reboot feature)

MICRO-STAR INT'L CO.,LTD.

Title: PCH-1 (HDA/JTAG/SATA)

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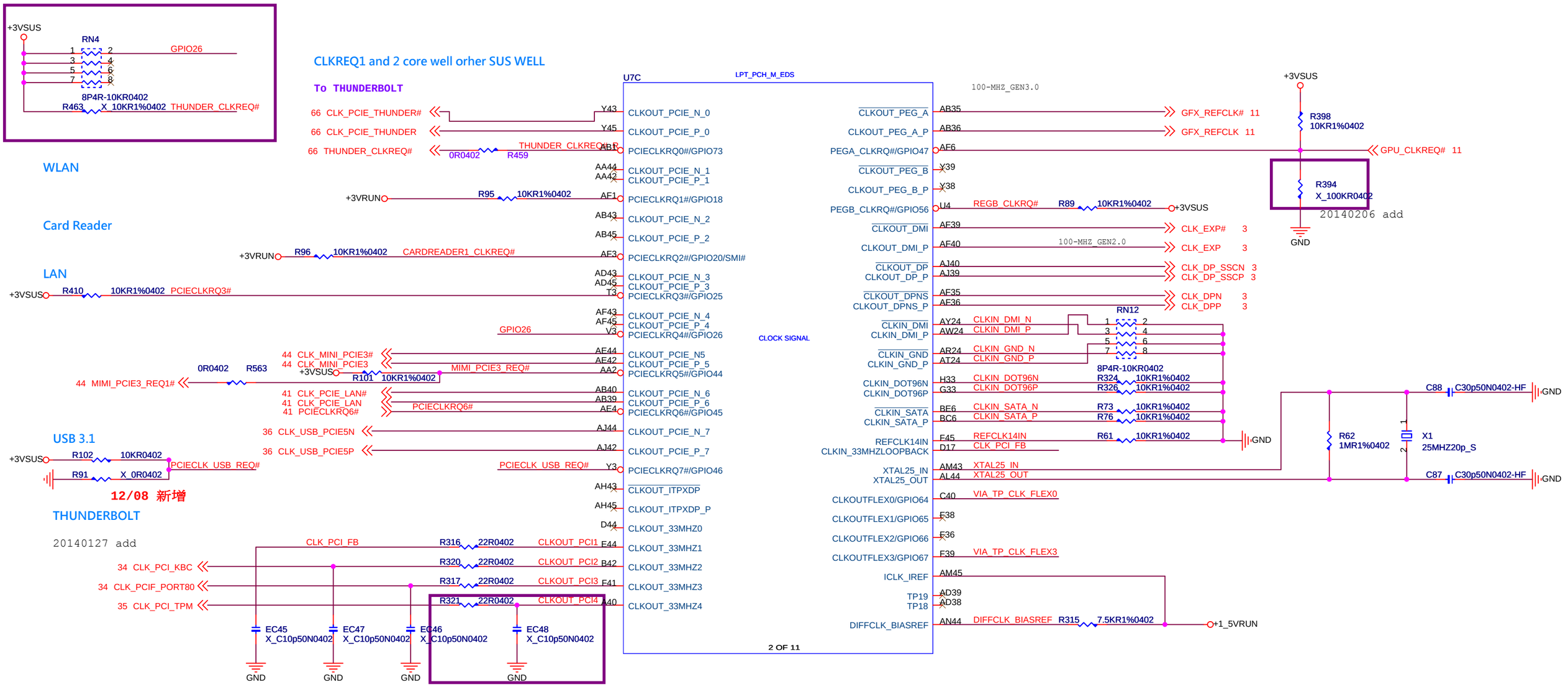
Lynx Point (Clock)

PCIe devices or addin cards that do NOT support CLKREQ# functionality should not route this signal to PCH.
Intel recommends terminating PCIECLKRQx# pin on PCH with 10 kΩ ±10% external pull-up resistor instead of No Connect.
Only PCIECLKRQ[2:1]# on PCH are core well powered. All other PCIECLKRQx# are suspend well powered.



2014.2.17 Add

The CLKREQ# function can be disabled via intel management engine FW .Please refer to INTEL ME FW Bring up guide for configuring/disabling CLKREQ#

MICRO-STAR INT'L CO.,LTD.

Title: PCH-2 (CLK)

Size | Document Number: MS-16H3 | Rev: 1.0

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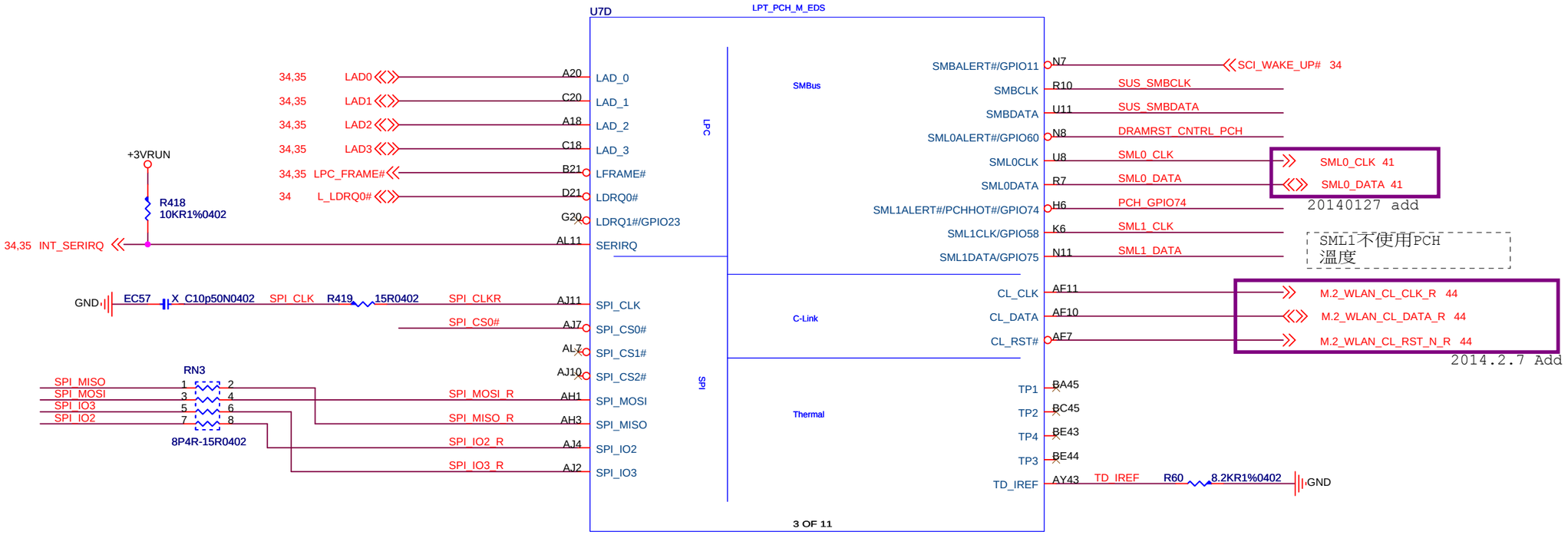
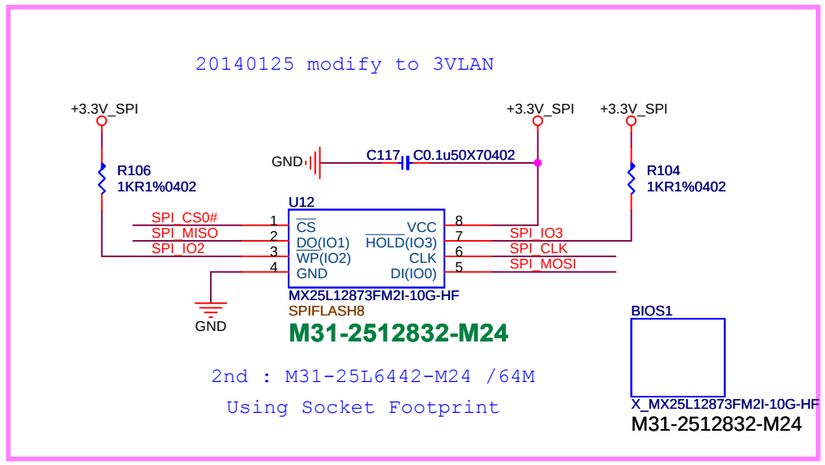
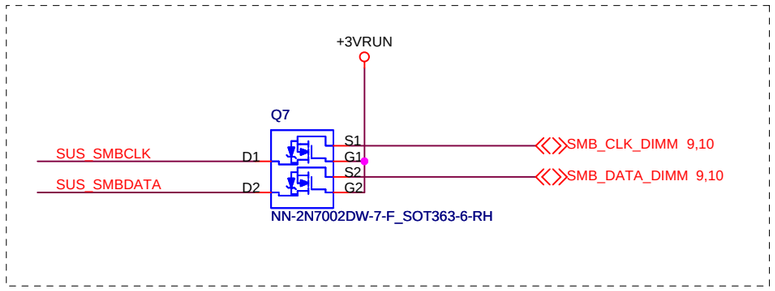
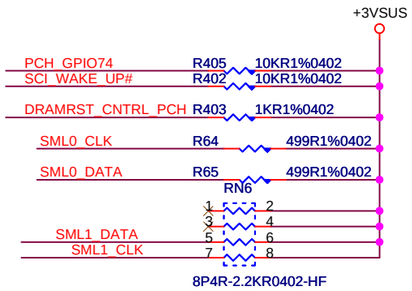
Lynx Point (LPC,SMBUS)

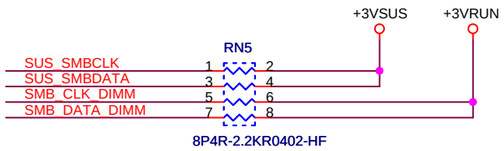


20140310 0A先上socket,N14-0080030-L06
顆粒,M31-25Q6402-E17
(0A Footprint共用SPIFLASH8 is Socket footprint)









MICRO-STAR INT'L CO.,LTD.		
Title: PCH-3 (LPC,SMBUS)		
Size	Document Number: MS-16H3	Rev: 1.0
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Lynx Point (DMI,FDI)

20140127 add

+3VSUS

SLP_LAN# R420 X_10KR0402
SUSPWRACK R406 10KR1%0402
AC_PRESENT R407 10KR1%0402
PM_RI# R401 10KR1%0402
PM_BATLOW# R404 8.2KR1%0402
PCIE_WAKE# R87 10KR1%0402

+3VRUN

PM_CLKRUN# R416 8.2KR1%0402
PM_SYSRST# R92 10KR1%0402

U7B — LPT_PCH_M_EDS

DMI

3 DMI_RXN0 — AW22 DMI_RXN_0
3 DMI_RXN1 — AR20 DMI_RXN_1
3 DMI_RXN2 — AP17 DMI_RXN_2
3 DMI_RXN3 — AV20 DMI_RXN_3
3 DMI_RXP0 — AY22 DMI_RXP_0
3 DMI_RXP1 — AP20 DMI_RXP_1
3 DMI_RXP2 — AR17 DMI_RXP_2
3 DMI_RXP3 — AW20 DMI_RXP_3
3 DMI_TXN0 — BD21 DMI_TXN_0
3 DMI_TXN1 — BE20 DMI_TXN_1
3 DMI_TXN2 — BD17 DMI_TXN_2
3 DMI_TXN3 — BE18 DMI_TXN_3
3 DMI_TXP0 — BB21 DMI_TXP_0
3 DMI_TXP1 — BC20 DMI_TXP_1
3 DMI_TXP2 — BB17 DMI_TXP_2
3 DMI_TXP3 — BC18 DMI_TXP_3

+1_5VRUN

BE16 DMI_IREF
AW17 TP12
AV17 TP7
R358 7.5KR1%0402 DMI_COMP_R — AY17 DMI_RCOMP

FDI

FDI_RXN_0 AJ35
FDI_RXN_1 AL35
FDI_RXP_0 AJ36
FDI_RXP_1 AL36
TP16 AV43
TP5 AY45
TP15 AV45
TP10 AW44
FDI_CSYNC AL39 — FDI_CSYNC 3
FDI_INT AL40 — FDI_INT 3
FDI_IREF AT45
TP17 AU42
TP13 AU44
FDI_RCOMP AR44

2014.3.2 NON AMT
non-AMT R793 stuff
ANT
R793 unstuff

EC_PCH_PWROK — R412 0R0402 — 45 PM_MPWROK
R411 10KR1%0402 — GND

EC delay 99ms

20140306 modify

VIA_SUSACK# — R6 SUSACK#
34 PM_SYSRST# — PM_SYSRST# — AM1 SYS_RESET#
SYS_PWROK — AD7 SYS_PWROK
F10 PWROK
AB7 APWROK
3 PM_DRAM_PWRGD — H3 DRAMPWROK
34 RSMRST# — J2 RSMRST#
34 SUSPWRACK — J4 SUSWARN#/SUSPWRNACK/GPIO30
34 PM_PWRBTN# — K1 PWRBTN#
34 AC_PRESENT — E6 ACPRESENT/GPIO31
PM_BATLOW# — K7 BATLOW#/GPIO72
PM_RI# — N4 RI#
AB10 TP21
44 SLP_WLAN# — D2 SLP_WLAN#/GPIO29

4 OF 11

System Power Management

DSWVRMEN C8 — DSWVRMEN — R77 330KR0402 — RTCVCC
DPWROK L13 — RSMRST#
WAKE# K3 — PCIE_WAKE# — PCIE_WAKE# 36,41,44,64
CLKRUN# AN7 — PM_CLKRUN# — R417 X_0R1%0402 — EC_CLKRUN# 34
SUS_STAT#/GPIO61 U7
SUSCLK/GPIO62 Y6 — SUSCLK — R409 22R0402 — EC_SUSCLK 34
SLP_S5#/GPIO63 Y7 — VIA_PM_SLP_S5# 34,64 — R408 X_22R0402 — WLAN_SUSCLK 44
SLP_S4# C6 — PM_SLP_S4# 34,49
SLP_S3# H1 — PM_SLP_S3# 34,49,64

unstuff 0B

SLP_A# F3 — SLP_M# 34,45
SLP_SUS# F1

20140127 add

PMSYNCH AY3 — H_PM_SYNC 3
SLP_LAN# G5 — SLP_LAN# 41,50

20140127 add

APWROK
not supporting Intel AMT , it can be connected to PWROK
GPIO31 : If not used,require pull up +3VSUS
DSWVRMEN - On Die DSW VR Enable HIGH : Enable internal 1.05V regulator LOW : Disable
DPWROK Without deep s4/s5 support tied together with RSMRST#

+3VSUS — C608 C0.1u50X70402 — GND

53 CPU_PWROK — 1
6,34 EC_PCH_PWROK — 2
U32 NC7S08P5X_SC70 — 4 SYS_PWROK
EC55 X_C15p50N0402 — GND
EC56 X_C15p50N0402 — GND

GPIO Setting : Ref 486708_LPT_EDS Section2.18

PLL ON DIE VR_ENABLE	
GPIO62	Internal pull high (Enable)
	Low: Disable

MICRO-STAR INT'L CO.,LTD.

Title: **PCH-4 (DMI,FDI)**

Size | Document Number: **MS-16H3** | Rev: **1.0**

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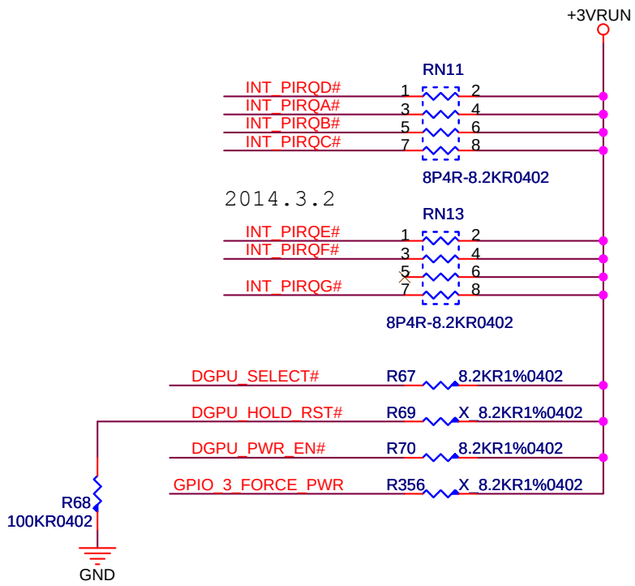
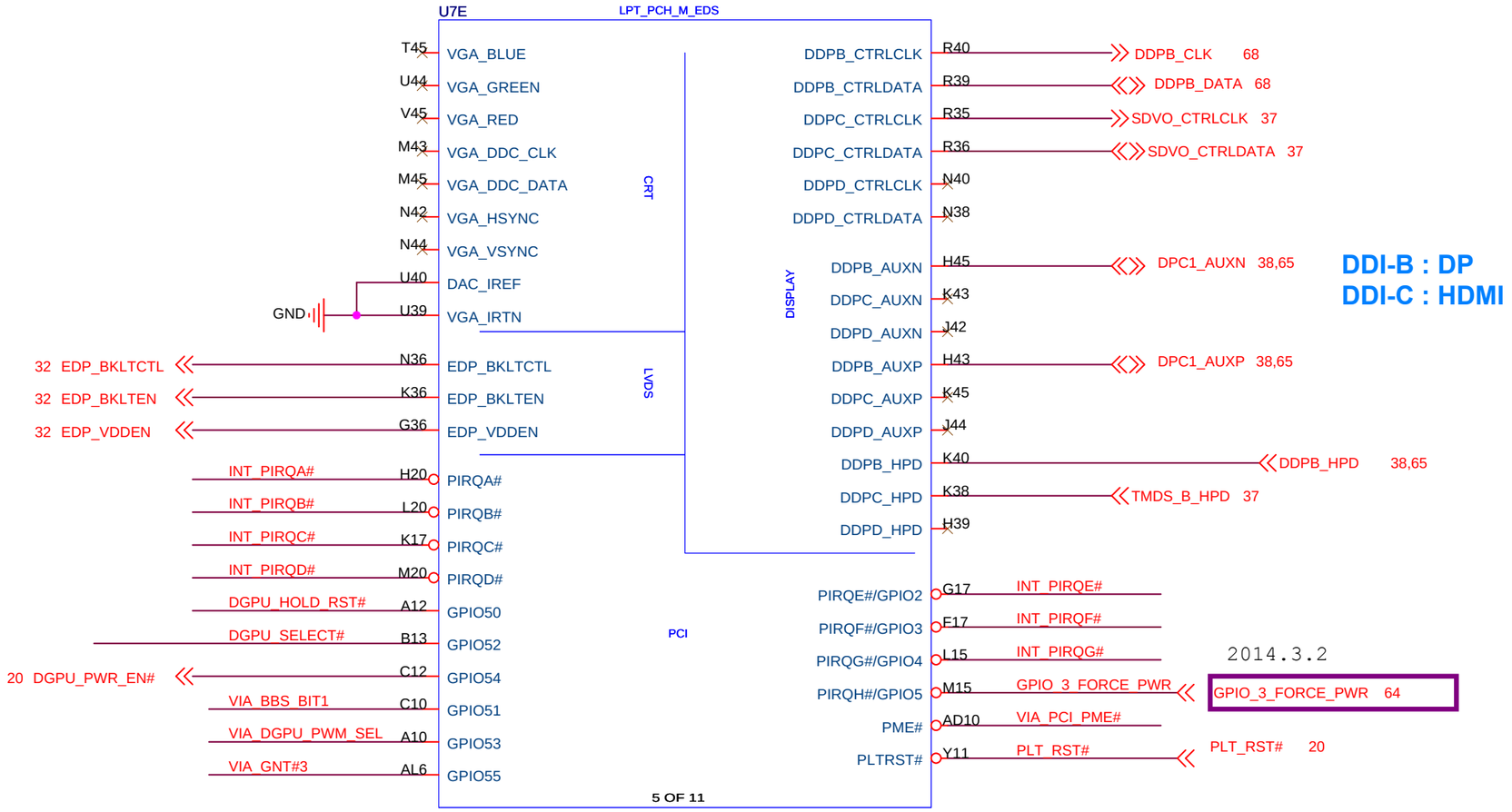
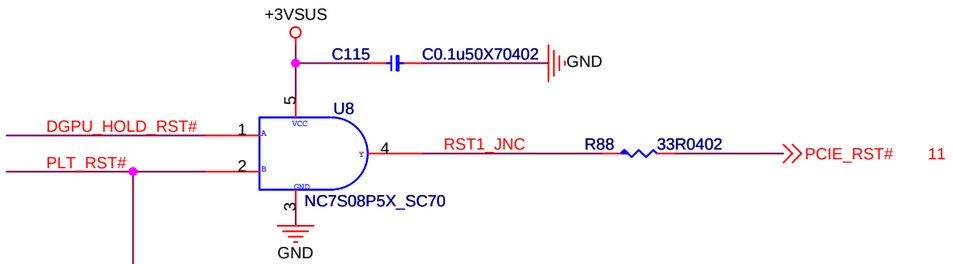
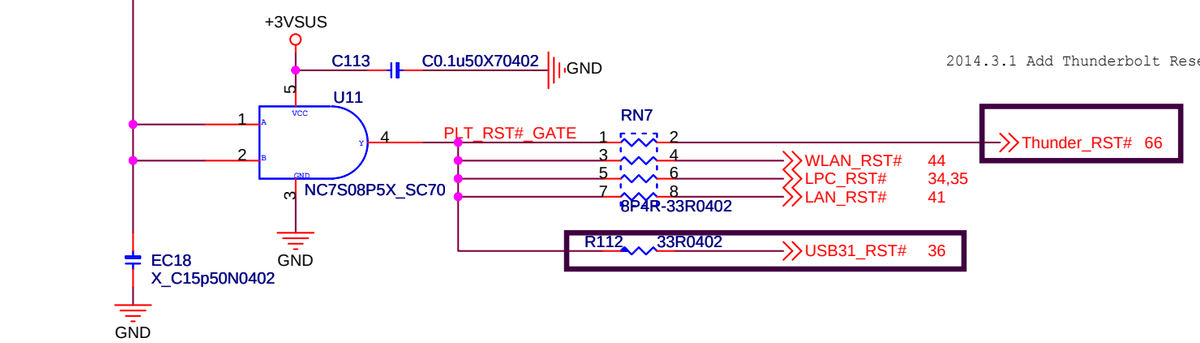
Lynx Point (PCI,DDI)









Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	N/A
1	1	SPI

21p

MICRO-STAR INT'L CO.,LTD.

Title: PCH-5 (PCI,DDI)

Size | Document Number: MS-16H3 | Rev: 1.0

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Lynx Point (GPIO,MISC)

GPIO Setting : Ref 486708_LPT_EDS Section2.24

PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable)
	Low: Disable

公板100R empty

U7F LPT_PCH_M_EDS

GPIO

CPU/Misc

NCTF

6 OF 11

+3VRUN R374 10KR1%0402 PCH_GPIO0 — AT8 BMBUSY#/GPIO0

34 KBSMI# — F13 TACH1/GPIO1

For USB 3.1 20140218 add

36 USBSMI# — A14 TACH2/GPIO6

34 KBSCI# — G15 TACH3/GPIO7

VIA_ICC_EN# — Y1 GPIO8

20140127 add

41 LAN_DISABLE# — K13 LAN_PHY_PWR_CTRL/GPIO12

64 GPIO_5_PLUG_EVENT — AB11 GPIO15

VIA_JTAG_SATA4GP — AN2 SATA4GP/GPIO16

DGPU_PWRGD — R366 100KR0402 — GND

11,18,20,34,52 DGPU_PWRGD — C14 TACH0/GPIO17

+3VRUN R378 10KR1%0402 BIOS_REC — BB4 SCLOCK/GPIO22

VIA_HOST_ALERT#2 — Y10 GPIO24

+3VSUS R400 10KR1%0402 PCH_GPIO_27 — R11 GPIO27

AD11 GPIO28

41,44 PCH_GPIO_27

VIA_STP_PCI# — AN6 GPIO34

20140206 add

VIA_EDID_SELECT# — AP1 GPIO35/NMI#

VIA_PCH_GPIO36 — AT3 SATA2GP/GPIO36

VIA_PCH_GPIO37 — AK1 SATA3GP/GPIO37

+3VRUN R368 10KR1%0402 MFG_MODE — AT7 SLOAD/GPIO38

VIA_CRB_SV_DET — AM3 SDATAOUT0/GPIO39

+3VRUN R93 10KR1%0402 TEST_SET_UP — AN4 SDATAOUT1/GPIO48

VIA_GPIO49 — AK3 SATA5GP/GPIO49

+3VSUS R90 X_10KR1%0402 GPIO57 — U12 GPIO57

C16 TACH4/GPIO68

D13 TACH5/GPIO69

G13 TACH6/GPIO70

H15 TACH7/GPIO71

BE41 BE5 C45 A5 — VSS — GND

TP14 AN10 — H_A20GATE 34

PECI AY1 VIA_PECI

RCIN# AT6 — KBRST# 34

PROCPWRGD AV3 — H_CPUPWRGD 3

THRMTRIP# AV1 PCH_THRMTRIP#_R R80 390R0402 — H_THRMTRIP# 3

PLTRST_PROC# AU4 — PCH_PLTRST_CPU 3

VSS N10

+1_05VRUN 2014.2.20 remove for Haswell

R81 X_1KR1%0402

	Haswell	Boardwell
R81	No Stuff	Stuff
R80	Stuff 390R	Stuff value need to confirm

VSS A2 A41 A43 A44 B1 B2 B44 B45 BA1 BC1 BD1 BD2 BD44 BD45 BE2 BE3 D1 E1 E45 A4 — GND

PCH_THRMTRIP#_R — EC15 X_C15p50N0402 — GND

MICRO-STAR INT'L CO.,LTD.

Title: PCH-6 (GPIO,MISC)

Size | Document Number: MS-16H3 | Rev: 1.0

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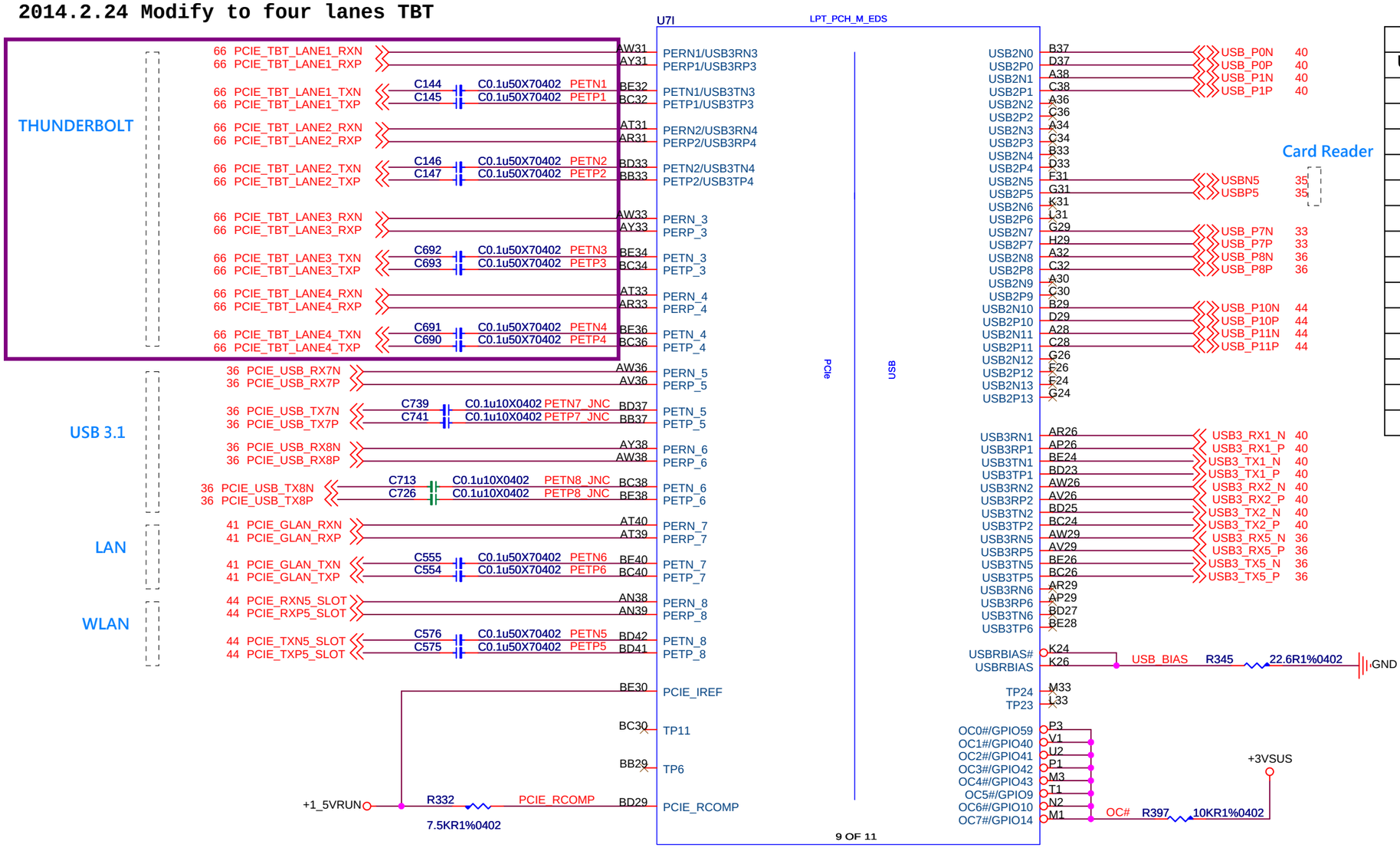
Lynx Point (PCIE,USB)

Intel Lynx Point ECHI USB(2.0) debug transport 需接Port1 or Port9

2014.2.24 Modify to four lanes TBT



USB			
USB 2.0	**USB 3.0**	**Device**	**Note**
0	1	USB 3.0 Port 1	**16H3A**
1	2	USB 3.0 Port 2	**16H3A**
2			
3			NC
4			NC
5			NC
6			NC
7		EPF021	3 色KBC
8	3	USB 3.0 Port 5	**16H31**
9	4	USB 3.0 Port 6	**no use**
10		WLAN	
11		WebCam	
12		SECOND DISPLAY	
13			NC

HM86 沒USB3.0 PORT 5,6

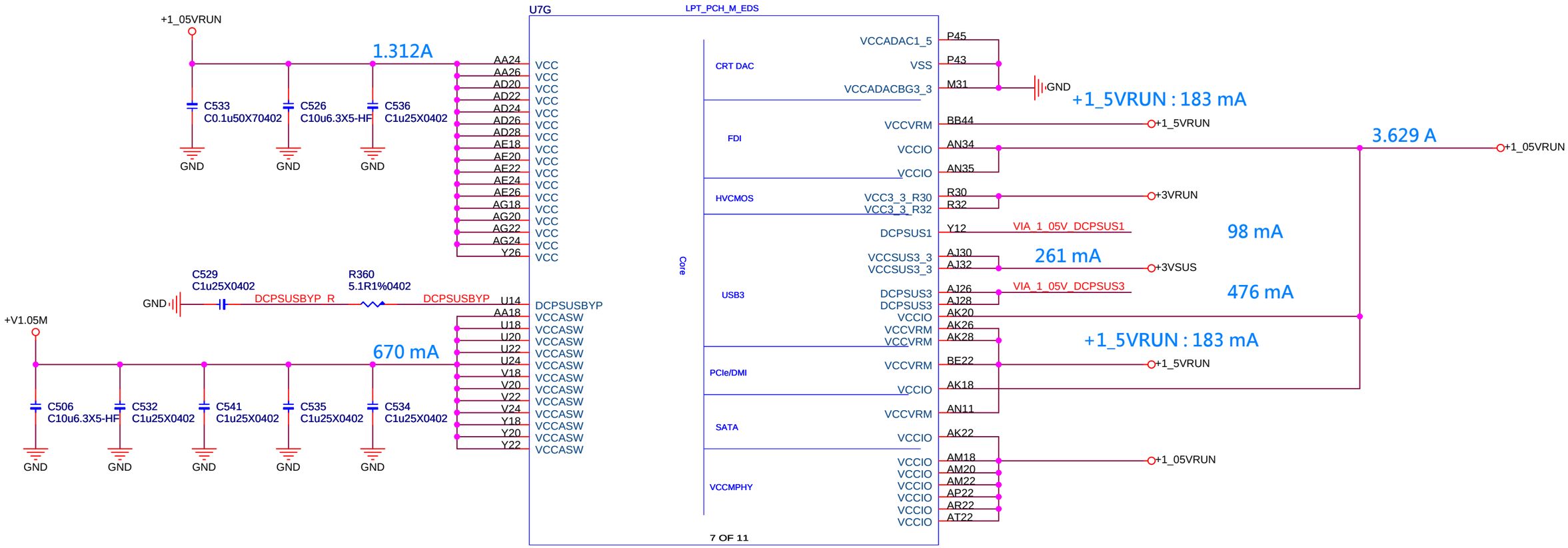
MICRO-STAR INT'L CO.,LTD.

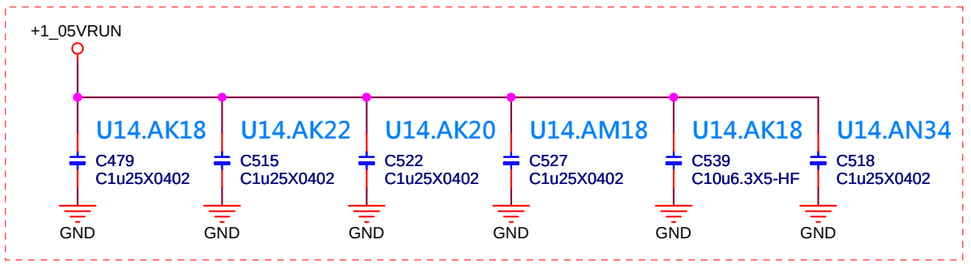
Title: PCH-7 (PCIE,USB)

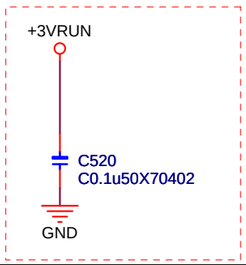
Size | Document Number: MS-16H3 | Rev: 1.0

Date: Wednesday, June 25, 2014 | Sheet 28 of 69

Lynx Point (Power)







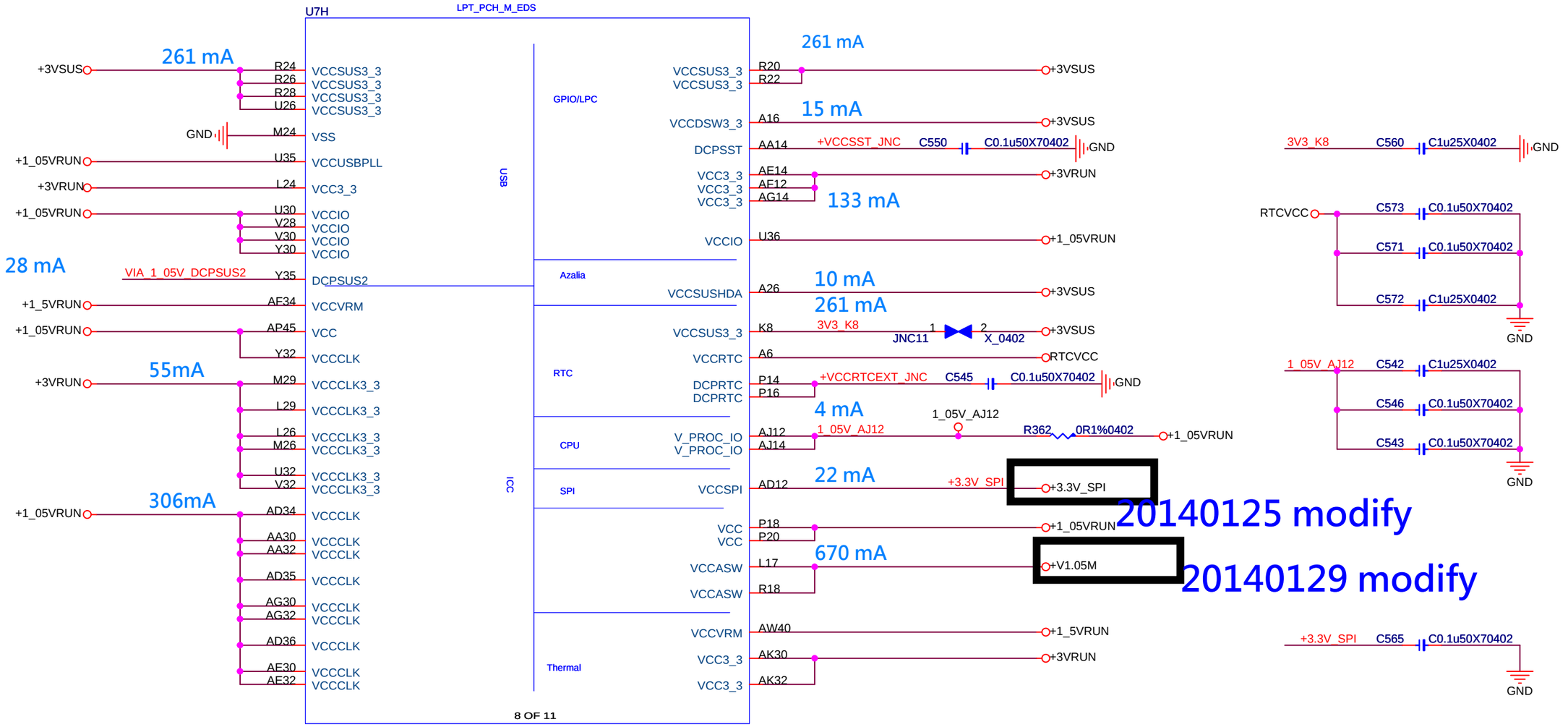
MICRO-STAR INT'L CO.,LTD.

Title: PCH-8 (Power)

Size | Document Number: MS-16H3 | Rev: 1.0

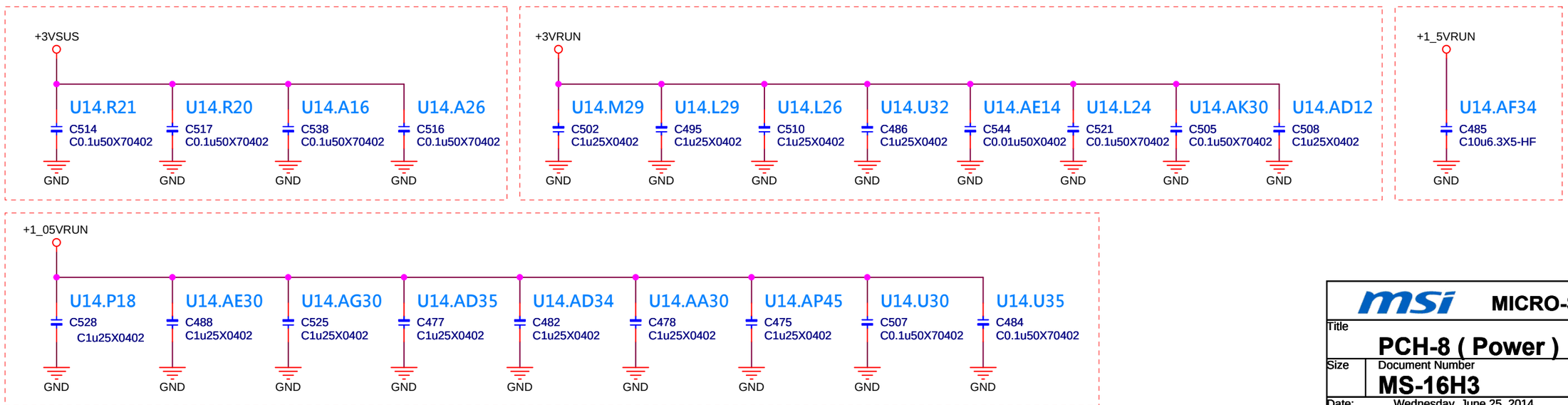
Date: Wednesday, June 25, 2014 | Sheet 29 of 69

Lynx Point (Power)



20140125 modify

20140129 modify



MICRO-STAR INT'L CO.,LTD.

Title: PCH-8 (Power)

Size | Document Number: MS-16H3 | Rev: 1.0

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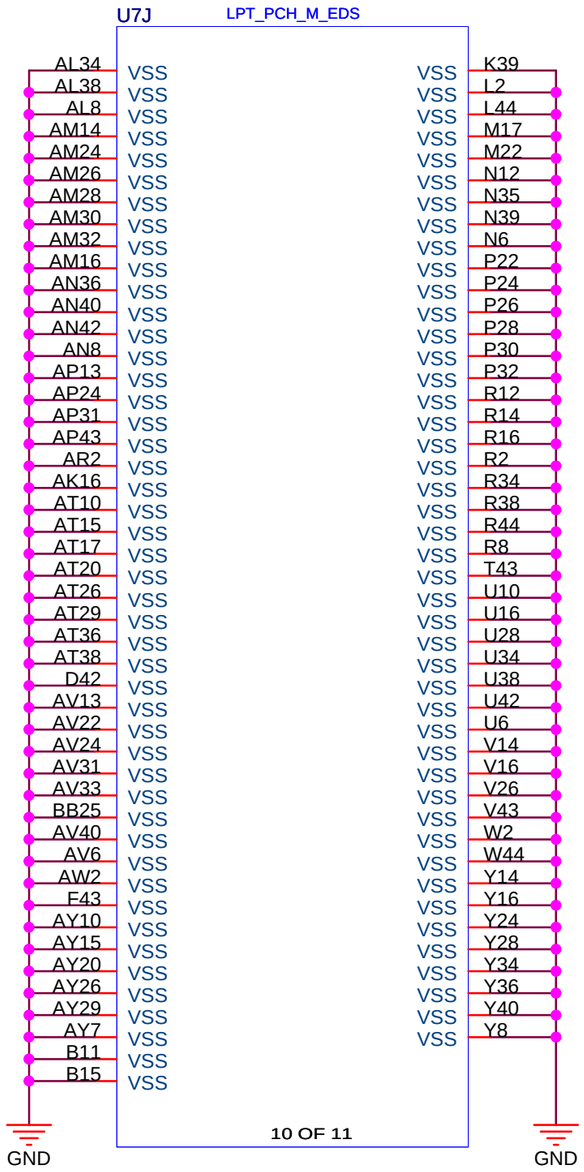
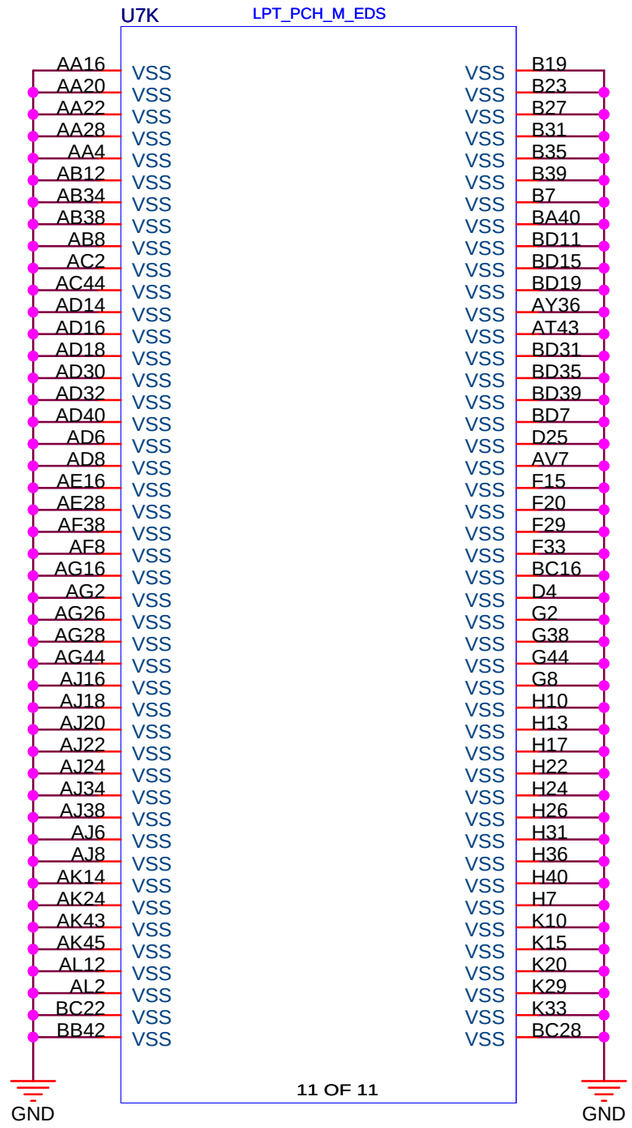
Lynx Point (GND)





MICRO-STAR INT'L CO.,LTD.		
Title: PCH-8 (GND)		
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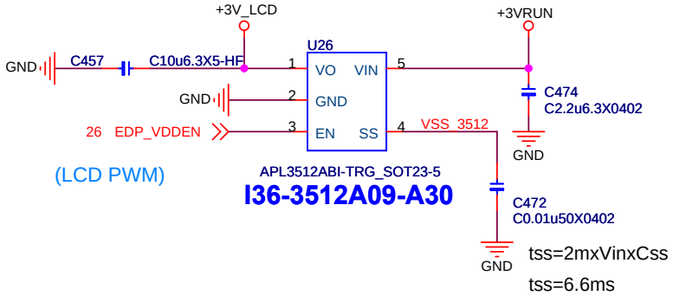
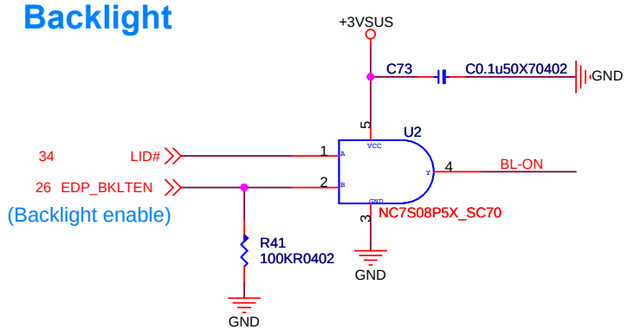
Date: Wednesday, June 25, 2014	Sheet 31 of 69	

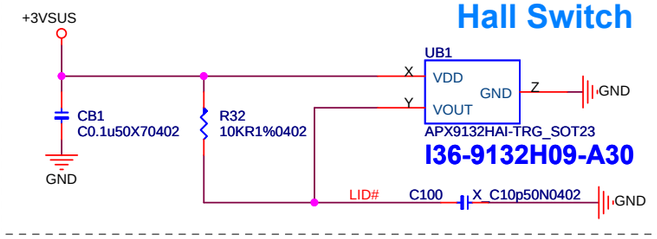
Pannel Device Logic Power



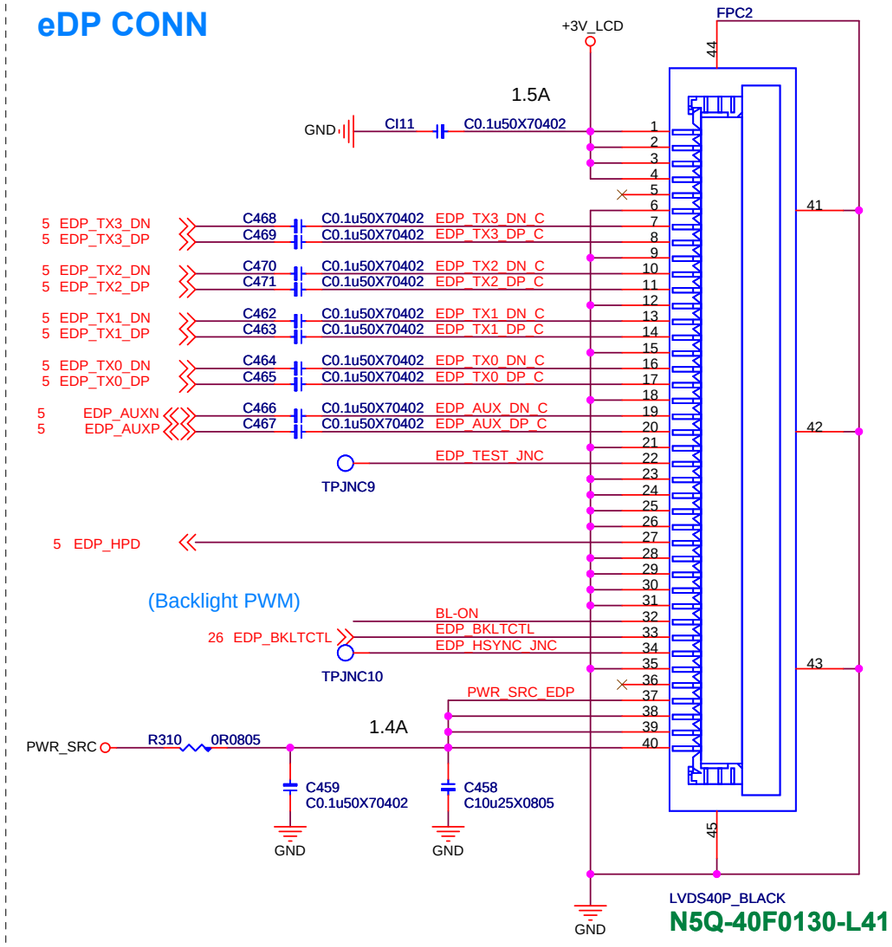
Backlight



Hall Switch

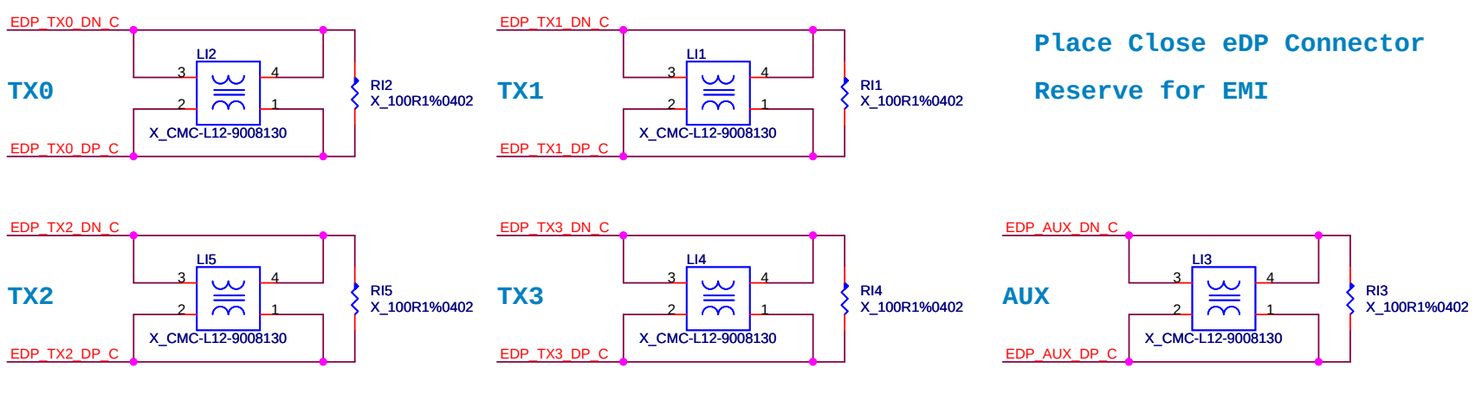


eDP CONN



LCD Module Pin Define

Pin No	Symbol	Description
1	WP	EEPROM Write Protect(Keep open)
2	H_GND	High Speed Ground(0V)
3	eDP_Rx_3N	Complement Signal Link Lane 3
4	eDP_Rx_3P	True Signal Link Lane 3
5	H_GND	High Speed Ground(0V)
6	eDP_Rx_2N	Complement Signal Link Lane 2
7	eDP_Rx_2P	True Signal Link Lane 2
8	H_GND	H_GND
9	eDP_Rx_1N	Complement Signal Link Lane 1
10	eDP_Rx_1P	True Signal Link Lane 1
11	H_GND	H_GND
12	eDP_Rx_0N	Complement Signal Link Lane 0
13	eDP_Rx_0P	True Signal Link Lane 0
14	H_GND	H_GND
15	eDP_AUX_CH_P	True Signal Aux Channel
16	eDP_AUX_CH_N	Complement Signal Aux Channel
17	H_GND	H_GND
18	LCD_VCC	LCD logic and driver power
19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	TEST	LCD Test Port
23	LCD_GND	LCD logic and driver ground(0V)
24	LCD_GND	LCD logic and driver ground(0V)
25	LCD_GND	LCD logic and driver ground(0V)
26	LCD_GND	LCD logic and driver ground(0V)
27	eDP_HPD	HPD signal pin
28	BL_GND	Backlight ground(0V)
29	BL_GND	Backlight ground(0V)
30	BL_GND	Backlight ground(0V)
31	BL_GND	Backlight ground(0V)
32	BL_ENABLE	Backlight enable
33	BL_PWM_DIM	System PWM signal input
34	SDA	I2C-bus Data
35	SCL	I2C-bus Clock
36	BL_PWR	Backlight power (5~21V)
37	BL_PWR	Backlight power (5~21V)
38	BL_PWR	Backlight power (5~21V)
39	BL_PWR	Backlight power (5~21V)
40	HSYNC	HSYNC output from Tcon



MICRO-STAR INT'L CO.,LTD.

Title: eDP switch & Conn/CAM/Lid

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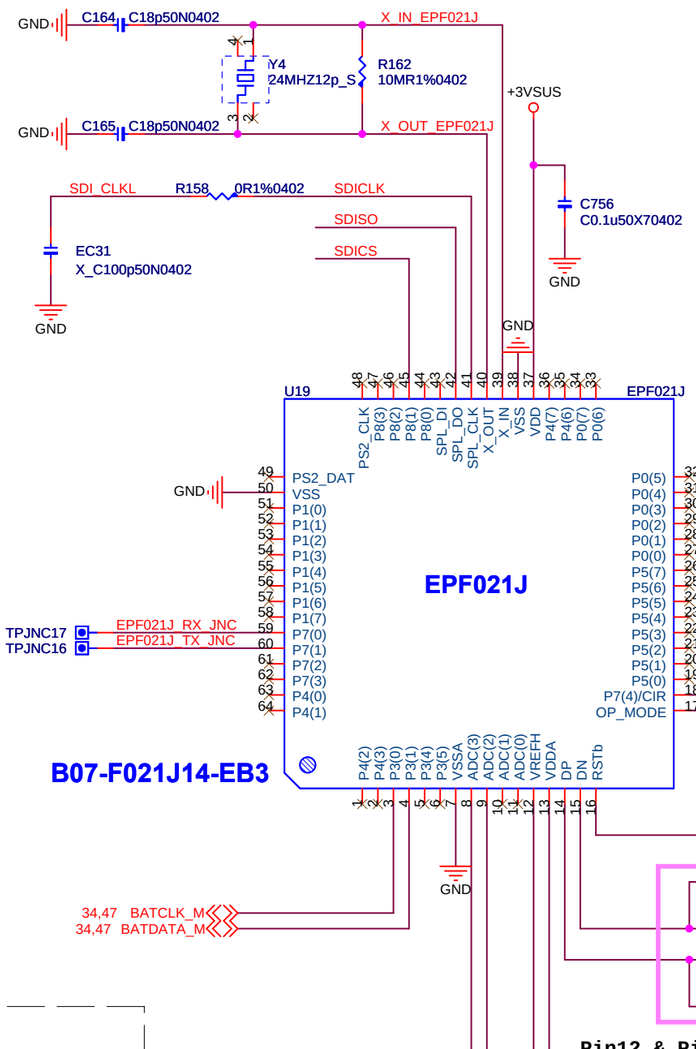
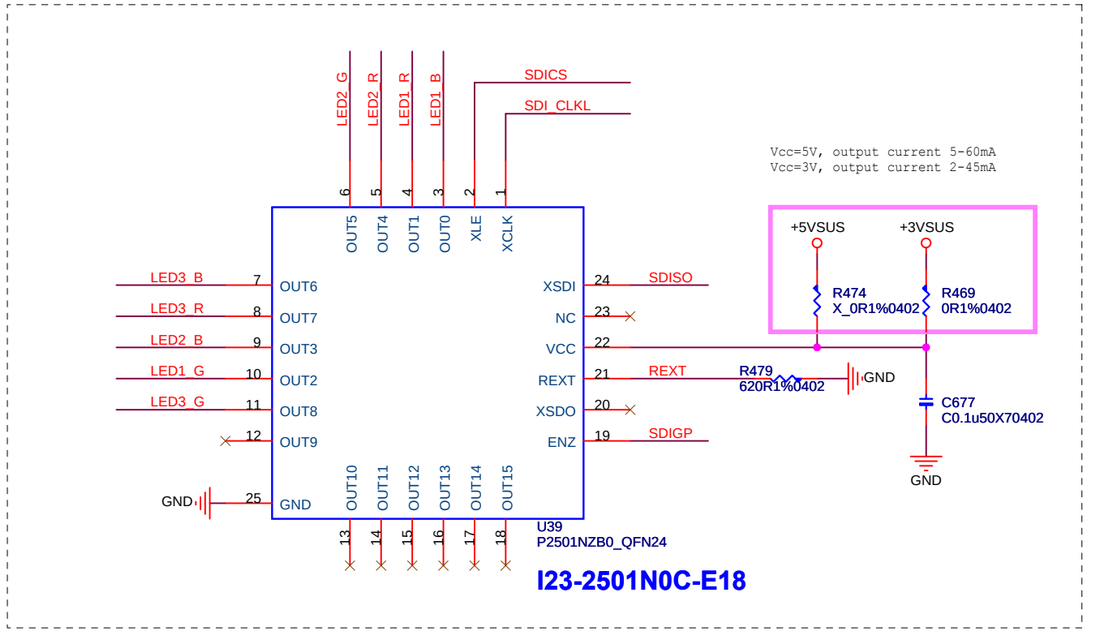
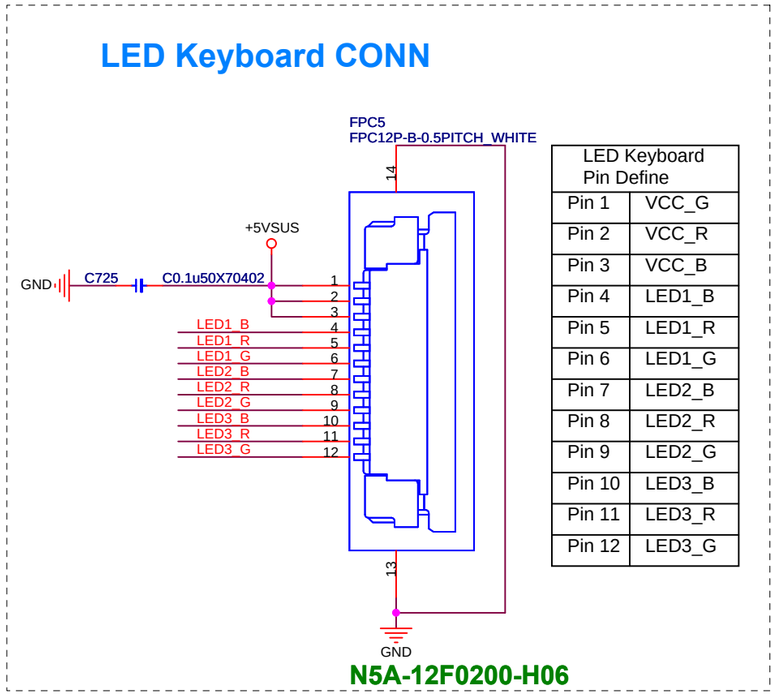
LED 8051 Controller

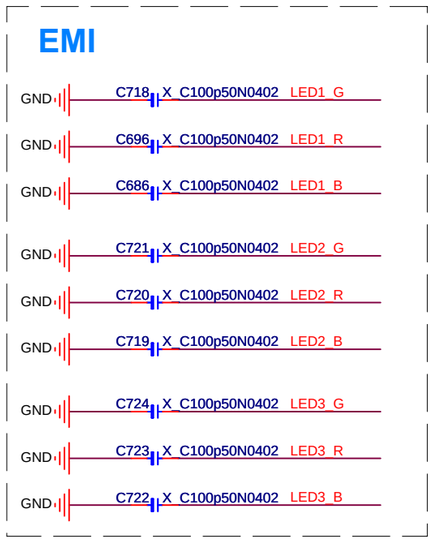






LED Keyboard Pin Define	
Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G

EMI



MICRO-STAR INT'L CO.,LTD.

Title: LED Driver IC/LED_8051

Size	Document Number	Rev
	MS-16H3	1.0

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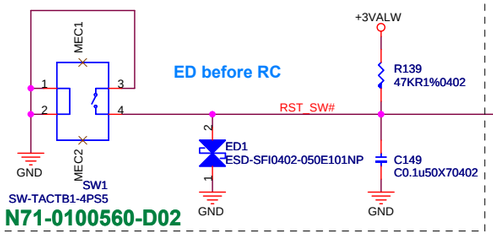
KBC(KB3930QFB1)

Hardware Reset

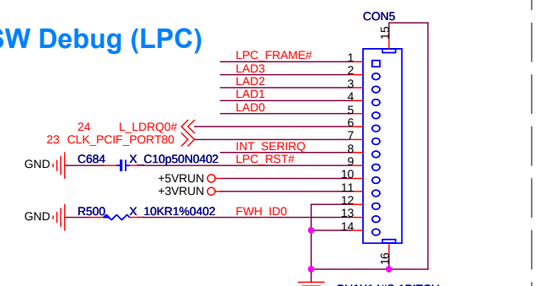


N71-0100560-D02

RC and R Close SW

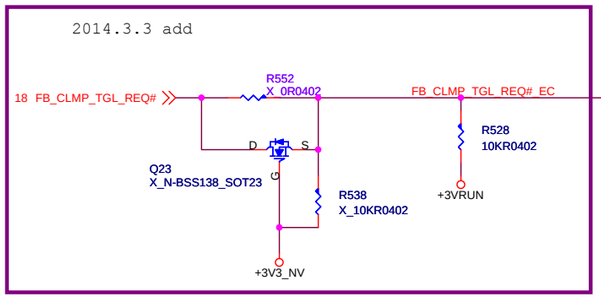
R140 33R0402 EC_RST#

SW Debug (LPC)



N32-1140130-H06

2014.3.3 add



U17

LPC I/F

24,35 INT_SERIRQ	3	SERIRQ
24,35 LPC_FRAME#	4	LFARAME#
23 CLK_PCI_KBC	12	PCICLK
25 EC_CLKRUN#	38	CLKRUN#/GPIO1D
24,35 LAD0	10	LAD0
24,35 LAD1	8	LAD1
24,35 LAD2	7	LAD2
24,35 LAD3	5	LAD3

POWER/GROUND

	9	VCC
	22	VCC
	33	VCC
	96	VCC
	111	VCC
	125	VCC
EC_AVCC	67	AVCC
	69	AGND
	11	GND
	24	GND
	35	GND
	94	GND
	113	GND

RST / GA20

	37	ECRST#
27 KBRST#	2	KBRST#
27 KBSCI#	20	SCI#/GPIO0E
27 H_A20GATE	1	GA20
26,35 LPC_RST#	13	PCIRST#

FAN&PWM

40 UMA_ON#	21	PWM0/GPIO0F
47 AC_CTL	23	PWM1/GPIO10
	25	GPIO11/PWM2
22 FLASH_SECURITY	34	GPIO19/PWM3
40 FAN1_PWM0	26	FANPWM0/GPIO12
43 FAN1_PWM1	27	FANPWM1/GPIO13
40 CPUFAN_FB	28	FANFB0/GPIO14
43 GPUFAN_FB	29	FANFB1/GPIO15

SMBUS

	78	SDA0/GPIO45
	77	SCL0/GPIO44
	80	SDA1/GPIO47
	79	SCL1/GPIO46

AD/DA

	68	DA0/GPO3C
	70	DA1/GPO3D
	71	DA2/GPO3E
	72	DA3/GPO3F
	63	AD0/GPI38
MB_ID	64	AD1/GPI39
	65	AD2/GPI3A
	66	AD3/GPI3B
	75	AD4/GPI42
	76	AD5/GPI43

SDI

	97	GPXIOA00/SDICS#
	98	GPXIOA01/SDICLK
	99	GPXIOA02/SDIMOSI

IKB

KBOUT0	39	KSO0/GPIO20/TP_TEST
KBOUT1	40	KSO1/GPIO21/TP_PLL
KBOUT2	41	KSO2/GPIO22/TP_ANA_TEST
KBOUT3	42	KSO3/GPIO23/TP_ISP
KBOUT4	43	KSO4/GPIO24
KBOUT5	44	KSO5/GPIO25
KBOUT6	45	KSO6/GPIO26
KBOUT7	46	KSO7/GPIO27
KBOUT8	47	KSO8/GPIO28
KBOUT9	48	KSO9/GPIO29
KBOUT10	49	KSO10/GPIO2A
KBOUT11	50	KSO11/GPIO2B
KBOUT12	51	KSO12/GPIO2C
KBOUT13	52	KSO13/GPIO2D
KBOUT14	53	KSO14/GPIO2E
KBOUT15	54	KSO15/GPIO2F/E51_RXD(ISP)
KBOUT16	81	KSO16/GPIO48
KBOUT17	82	KSO17/GPIO49
KBIN0	55	KSI0/GPIO30/E51TXD(ISP)
KBIN1	56	KSI1/GPIO31
KBIN2	57	KSI2/GPIO32
KBIN3	58	KSI3/GPIO33
KBIN4	59	KSI4/GPIO34/EDI_CS
KBIN5	60	KSI5/GPIO35/EDI_CLK
KBIN6	61	KSI6/GPIO3/EDI_DIN
KBIN7	62	KSI7/GPIO37/EDI_DO

ESB

39,40 EC_MUTE#	17	GPIO0B/ESB_CLK
47 BAT_BM#	18	GPIO0C/ESB_DAT_O/ESB_DAT_I

CIR

	73	GPIO40/CIR_RX/AD6
39 EAPD	74	GPIO41/CIR_RLC_TX/AD7
12,18,20 FB_CLAMP	16	GPIO0A/RLC_RX2
	19	GPIO0D/RLC_TX2

SPI FLASH

EC_RD#	119	MISO
EC_WR#	120	MOSI
EC_SPI_CLK	126	SPICLK/GPIO58
EC_CS#	128	SPICS#

PS2 I/F

44 TP_CLK	87	PSCLK2/GPIO4E
44 TP_DATA	88	PSDAT2/GPIO4F
36 CTL2_EC	85	PSCLK1/GPIO4C
36 CTL3_EC	86	PSDAT1/GPIO4D
3 EC_PROCHOT#	83	PSCLK0/GPIO4A/P80CLK
36,40 USB_ENABLE	84	PSDAT0/GPIO4B/P80DAT

UART

TPJNC15	30	E51TXD/GPIO16
TPJNC14	31	E51RXD/GPIO17

LED

		GPIO1A/NUMLED#
		E51TMR1/GPIO53/CAPSLED#
		E51INT0/GPIO55/SCROLED#

KB3930QFB1

B02-0393024-E18

GPIO / LED nets

	6	GPIO04
	14	GPIO07/i_clk_8051
	15	GPIO08/i_clk_peri
	32	GPIO18
	89	GPIO50
	90	E51CS#/GPIO52
	92	E51TMR0/GPIO54/WDT_LED#
	95	E51INT1/GPIO56
	121	GPIO57/XCLK32K
	127	GPIO59/TEST_CLKSPICLKI
	36	GPIO1A/NUMLED#
	91	E51TMR1/GPIO53/CAPSLED#
SCROLED# JNC	93	E51INT0/GPIO55/SCROLED#

	100	GPXIOA03
	101	GPXIOA04
	102	GPXIOA05
	103	GPXIOA06
	104	GPXIOA07
	105	GPXIOA08
	106	GPXIOA09
	107	GPXIOA10
	108	GPXIOA11
	109	GPXIOD0
	110	GPXIOD1
	112	GPXIOD2
EC_ALLSYSPG	114	GPXIOD3
	115	GPXIOD4
	116	GPXIOD5
	117	GPXIOD6
	118	GPXIOD7/PECI

Clock / misc

25 EC_SUSCLK	122	EC_XIN
	123	EC_XOUT
	124	V18R

R168 0R1%0402 · R167 X_10MR1%0402 · Y5 X_32.768KHZ12.5p · EC_XOUT_JNC · V18R · C748 C4.7u10X0603 · R169 680KR0402 · ER2 X_22R0402 · SUSCLK_RC · C175 X_C22p50N0402 · C170 X_C18p50N0402 · C171 X_C18p50N0402

POWER/GROUND

+3VALW · C761 C0.1u50X70402 · C169 C0.1u50X70402 · L2 80L700mA-150 · C151 C0.1u50X70402 · C150 C10u6.3X5-HF · C156 C0.1u50X70402 · C752 C0.1u50X70402 · C152 C0.1u50X70402 · +3VALW · GND

SMBUS

BATDATA_M	33,47
BATCLK_M	33,47
SMB_DATA_EC	18
SMB_CLK_EC	18

AD/DA

EPF021_RST	33
EPF021_OPMODE	33
DGPU_ON#	40
CTL1_EC	36
FBVDDQ_ON	20,52
ADP_ICC	47
SUSPWRACK	25
AC_OK#	47
BAT_IN#	47

SDI

AC_PRESENT	25
SUS_ON	46,48
RSMRST#	25

GPIO / LED nets

DIMM_ON	49
RUN_ON	46,48,50
EC_PCH_PWROK	6,25
BATLOW_N	64
WLAN_PWRON	44
LED_ACPI#	40
LED_CHARGE#	40
LED_BATLOW#	40
LED_BLUETOOTH#	40
SUSPWROK	48
PM_SLP_S4#	25,49
PM_SLP_S3#	25,49,64
PWR_SW#	40
SCI_WAKE_UP#	24
LID#	32
H_PECI	3

R535 43R0402 · H_PECI_R · C751 X_C47p50N0402

2014.3.2 DELETE, then add it.

Pin 105-108 8mA-16mA Sink

GPU_ACIN1	18
DGPU_PWRGD	11,18,20,27,52
KBSMI#	27
BATT_OFF	47
LED_WLAN#	40
PM_PWRBTN#	25
BT_PWR_ON	44
CAMERA_ON#	44

2014.2.7 新增

Pin 92 16mA-20mA Sink

LED_NUM#	40
LED_CAP#	40

Pin 39,91 16mA-20mA Sink

TPJNC18

Keyboard conn

CON6 FPC26P-B-1PITCH_BLACK

KBOUT17	26
KBOUT16	25
KBIN0	24
KBIN1	23
KBIN2	22
KBIN3	21
KBIN4	20
KBIN5	19
KBIN6	18
KBIN7	17
KBOUT15	16
KBOUT14	15
KBOUT13	14
KBOUT12	13
KBOUT11	12
KBOUT10	11
KBOUT9	10
KBOUT8	9
KBOUT7	8
KBOUT6	7
KBOUT5	6
KBOUT4	5
KBOUT3	4
KBOUT2	3
KBOUT1	2
KBOUT0	1

N5A-26F0340-H06

CNI4 · CNI3 · CNI1 · CNI2 — 8P4C-100p50N0402

KBOUT17 CI14 C100p50N0402 · KBOUT16 CI13 C100p50N0402

MB_ID

+3VALW · PR70 X_100KR0402 · MB_ID · R141 10KR1%0402

MB_ID=1=AMT

MB_ID=0=non-AMT

FLASH/ME DEBUG MODE STRAP

20140311 add

25,64 VIA_PM_SLP_S5#	TPJNC32
22 RTCRST#	TPJNC11
25 PM_PWRBTN#	TPJNC19
25 PM_SYSRST#	TPJNC12

FOR APS TOOL

APS1 · 25,45 SLP_M# · 25,49,64 PM_SLP_S3# · 25,49 PM_SLP_S4# · +3VALW · +3VSUS · +3VSUS · X_H2X3M_BLACK-RH

MP remove

ROM

+3VALW · C158 C0.1u50X70402 · R172 2.2KR1%0402 · WP#_EC_ROM · R173 10KR1%0402 · U20 · SPI_HOLD# · EC_SPICLK · EC_WR# · EC_CS# · EC_RD# · MX25L512EMI-10G

M31-2551222-M24

EC_SPI_CLK · ER1 22R0402 · EC_SPICLK · EC32 C22p50N0402

ALLSYSPG

+3VRUN · R542 10KR1%0402

	non AMT	AMT
R527	No_Stuff	Stuff
R2	Stuff	No_Stuff
	Stuff	No_Stuff
	No_Stuff	Stuff
	No_Stuff	Stuff

50 +1_5VRUN_PWRGD · JNC15 · X_0402

45 +1_05VRUN_PWRGD · R527 X_0R1%0402

3/2 AMT

49 +1_35VDIMM_PWRGD · JNC14 · X_0402 · EC_ALLSYSPG 53

50 +1_05V_PWRGD · X_R2 0R1%0402

3/2 non AMT

PU/PD

+3VALW · BATCLK_M R145 2.2KR1%0402 · BATDATA_M R146 2.2KR1%0402

+3VRUN · SMB_CLK_EC R149 2.2KR1%0402 · SMB_DATA_EC R151 2.2KR1%0402

KBRST#, H_A20GATE

KBRST# R159 X_100KR0402

RSMRST# R84 10KR1%0402

Title	KBC(KB3930QFB1)
Size	Document Number: MS-16H3
Rev	1.0
Date:	Wednesday, June 25, 2014
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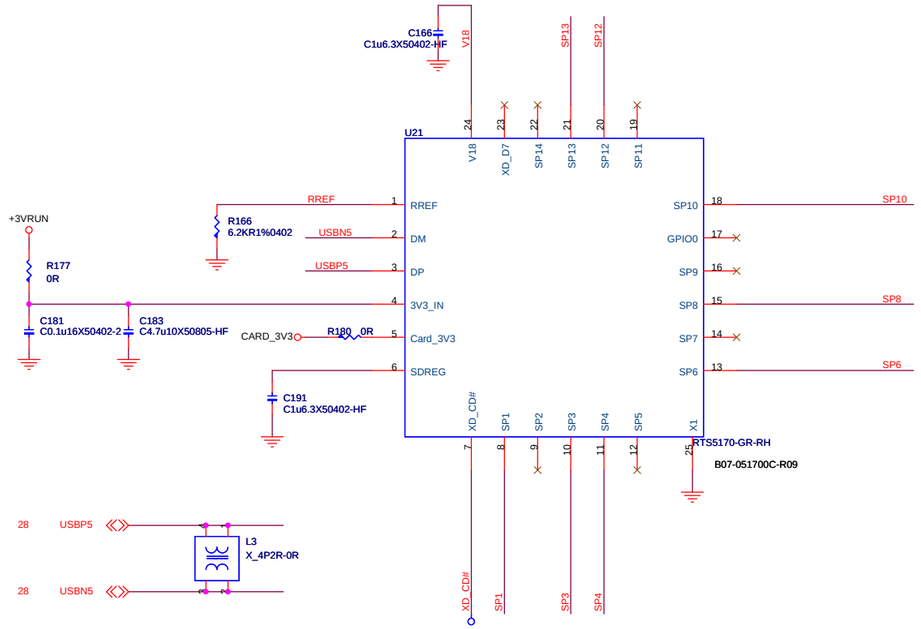
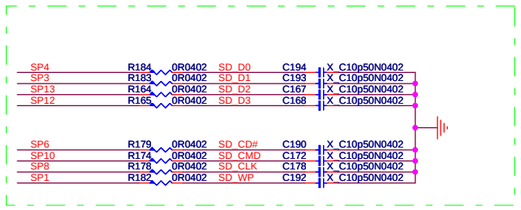
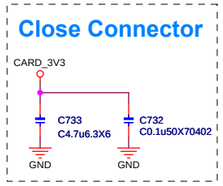
MICRO-STAR INT'L CO.,LTD.

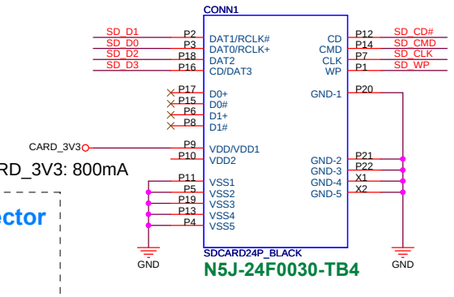
CARD READER_RTS5170





For EMI and Close to RTS5170



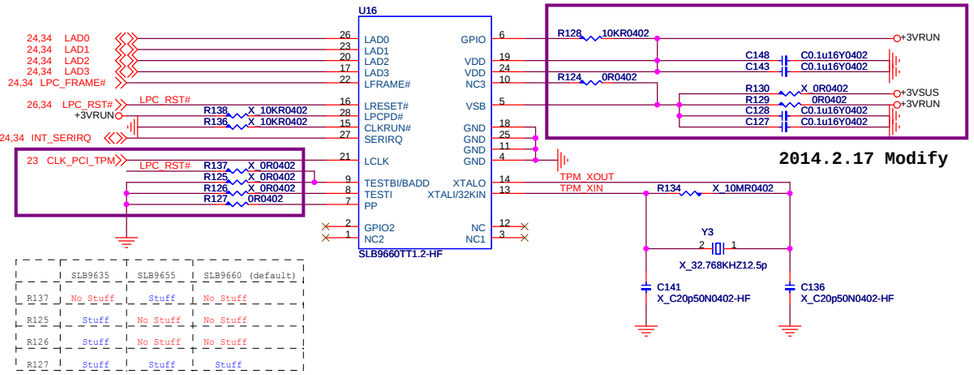


CARD_3V3: 800mA

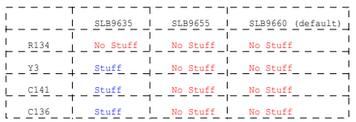
Pin#	Name	I/O Type	Description
1	RREF	I	Connect external resistor (6.2K ± 1%) to reference ground
2	DM	I/O	USB D- signal
3	DP	I/O	USB D+ signal
4	3V3_IN	I	3.3V power input
5	CARD_3V3	O	3.3V power for all cards
6	SDREG	O	Internal regulator for SD card. An external capacitor should be connected
7	XD_CD#	I	xD Card Detect (xD_CD#)
8	SP1	I/O	xD Ready Signal (xD_RDY), SD Write Protect (SD WP) and MS Clock (MS_CLK)
9	SP2	I/O	xD RE# and MS Card Detect (MS_INS#)
10	SP3	I/O	xD CE# and SD Data 1 (SD_DAT1)
11	SP4	I/O	xD_CLE, SD Data 0 (SD_DAT0) and MS Data 7 (MS_D7)
12	SP5	I/O	xD ALE, SD Data 7 (SD_DAT7) and MS Data 3 (MS_D3)
13	SP6	I/O	xD_WE# and SD Card Detect (SD_CD#)
14	SP7	I/O	xD Write Protect (xD_WP), SD_Data 6 (SD_DAT6) and MS Data 6 (MS_D6)
15	SP8	I/O	xD Data 0 (xD_D0), SD Clock (SD_CLK) and MS Data 2 (MS_D2)
16	SP9	I/O	xD Data 1 (xD_D1), SD Data 5 (SD_D5) and MS Data 0 (MS_D0)
17	GPIO0	I/O	General purpose input/output with interrupt ability
18	SP10	I/O	xD Data 2 (xD_D2) and SD command signal (SD_CMD)
19	SP11	I/O	xD Data 3 (xD_D3), SD Data 4 (SD_DAT4) and MS Data 4 (MS_D4)
20	SP12	I/O	xD Data 4 (xD_D4), SD Data 3 (SD_DAT3) and MS Data 1 (MS_D1)
21	SP13	I/O	xD Data 5 (xD_D5), SD Data 2 (SD_DAT2) and MS Data 5 (MS_D5)
22	SP14	I/O	xD Data 6 (xD_D6) and MS BS
23	XD_D7	I/O	xD Data 7 (xD_D7)
24	V18	O	Regulated supply voltage (1.8V ±10%) from internal 3.3V to 1.8V regulator; supplies internal digital circuits. An external capacitance should be connected

TPM

2014.2.17 Modify



2014.2.17 Modify



MICRO-STAR INT'L CO.,LTD.

Title: Card Reader & TPM

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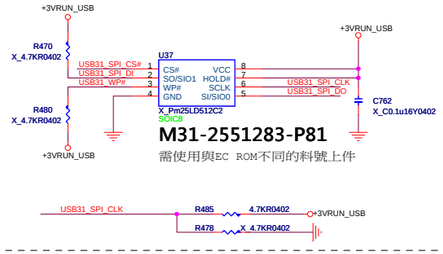
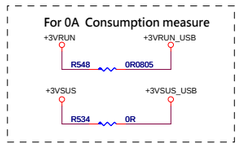
USB 3.0 / iCharger

USB3.0 CNT-1
USB3.0 Port-5
USB2.0 Port-8

SPI ROM For FW (stuff first)

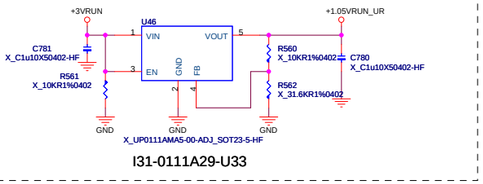


For 0A Consumption measure

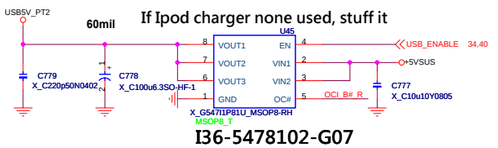


PCIE to USB 3.1

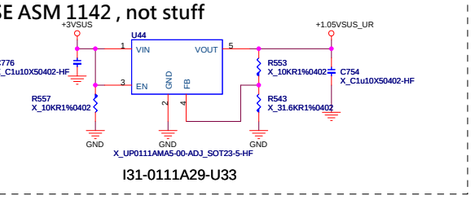
20140505add



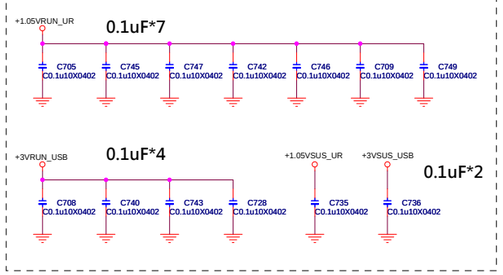
If Ipod charger none used, stuff it



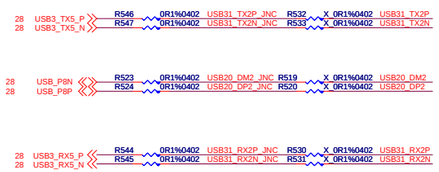
20140312 add forASM1042 If USE ASM 1142 , not stuff



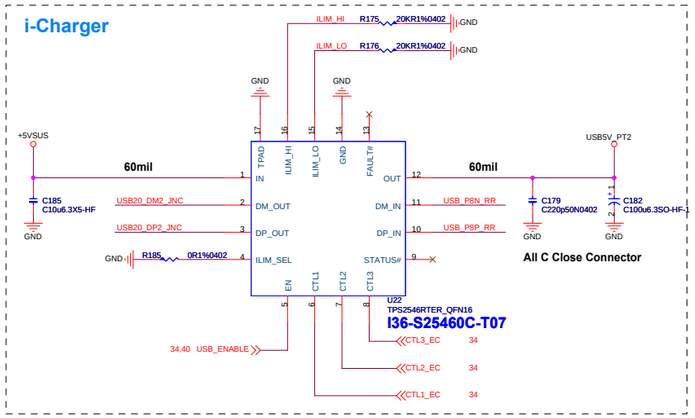
0.1uF*7 / 0.1uF*4 / 0.1uF*2



USB 3.1 Port 1



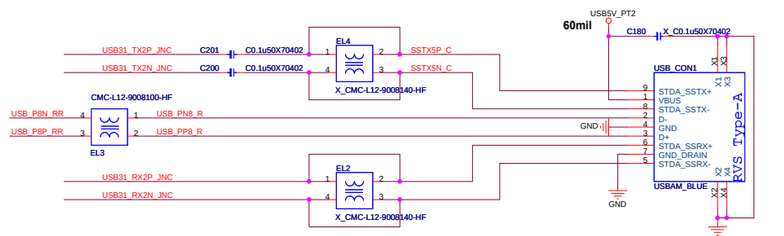
i-Charger



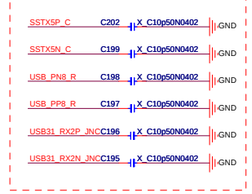
USB3.0 CNT-1

USB3.0 Port-6
USB2.0 Port-9

USB 3.0 / iCharger



EMI



MICRO-STAR INT'L CO.,LTD.		
Title: USB 3.0 / iCharger		
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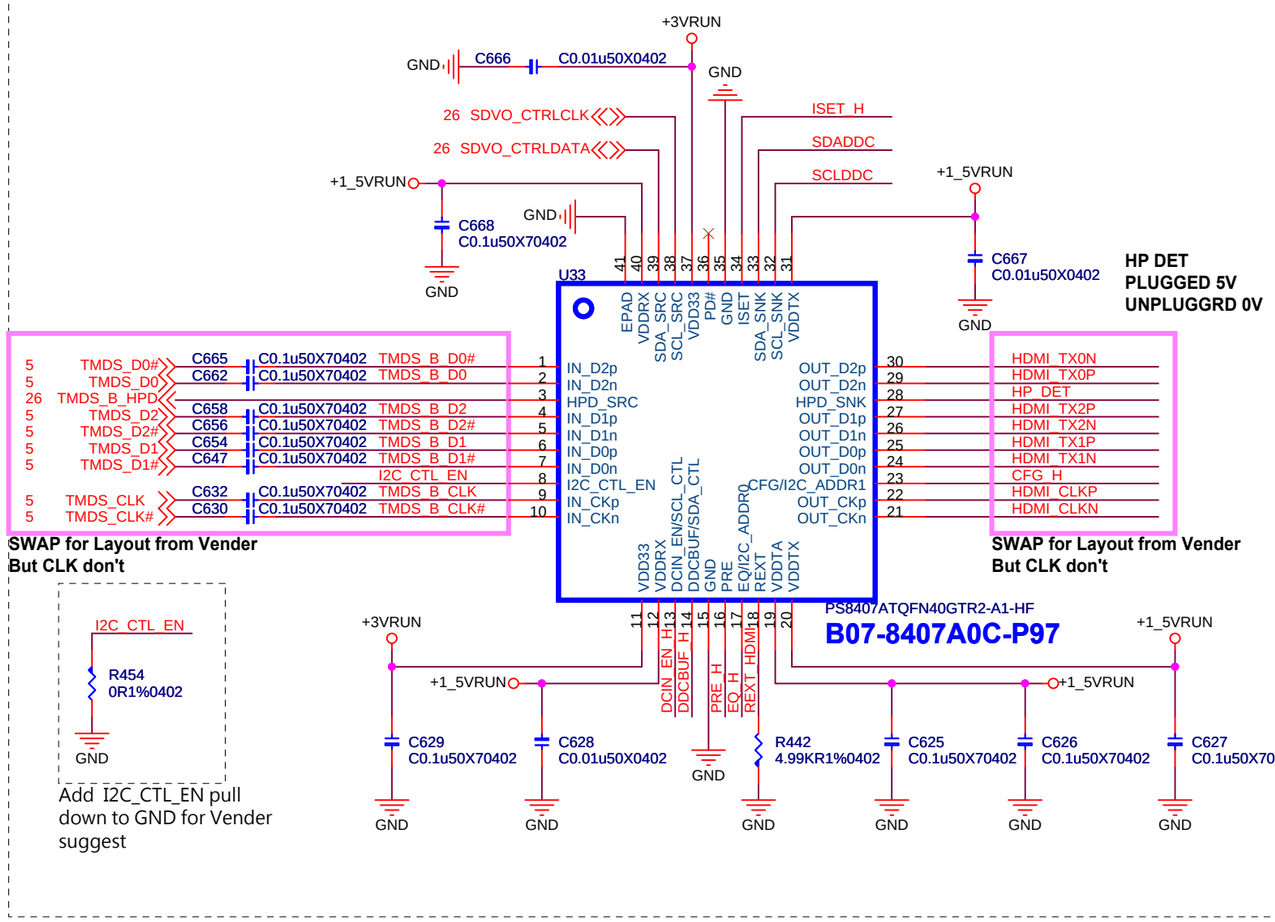
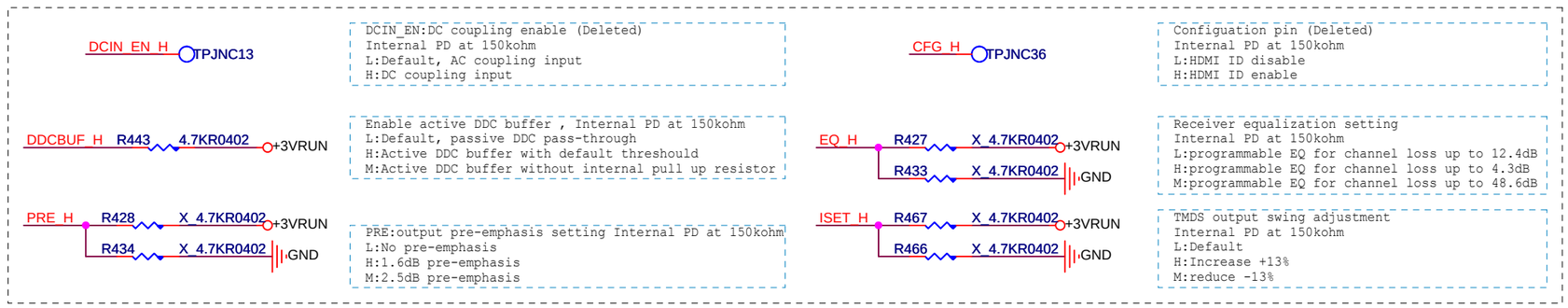
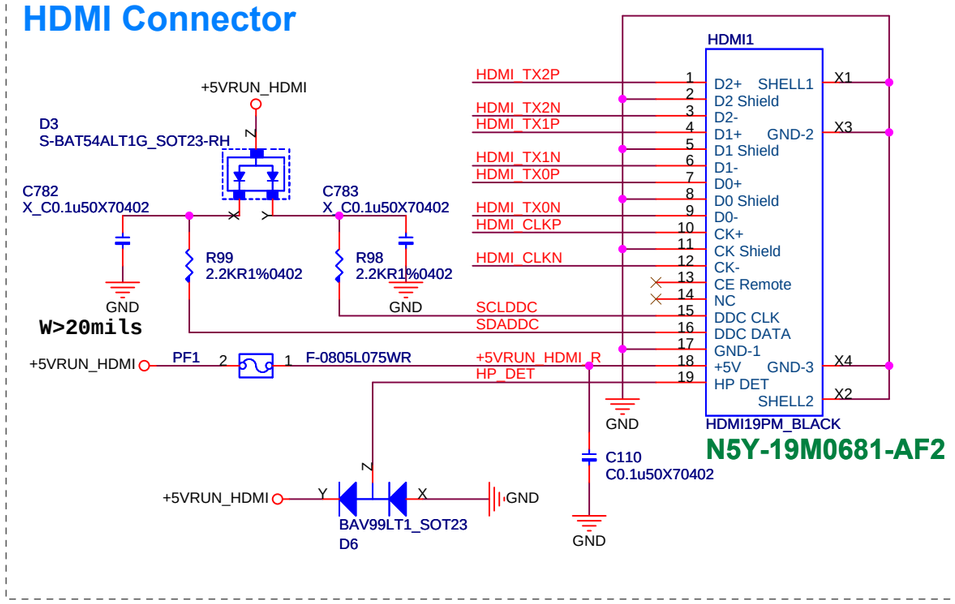
HDMI Repeater





ADDR1 (CFG)	ADDR0 (EQ)	I2C control bus address (Internal pull down at ~150kΩ, 3.3V I/O)
0	0	0x4C / 4D (default)
0	1	0x5C / 5D
1	0	0xCC / CD
1	1	0xEC / ED

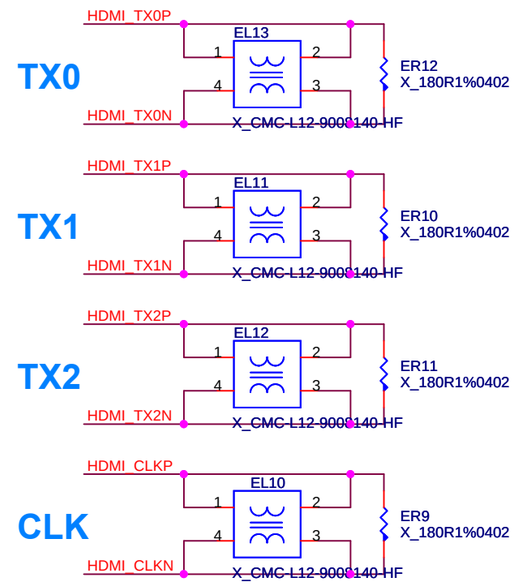
HDMI Connector



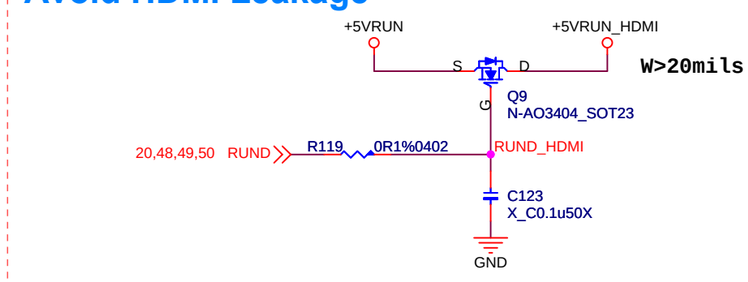
An HDMI Source shall have +5V Power signal over-current protection of no more than 0.5A.

HPD_SNK Internal PD 150kohm

EMI Close Connector



Avoid HDMI Leakage



MICRO-STAR INT'L CO.,LTD.		
Title: HDMI Repeater		
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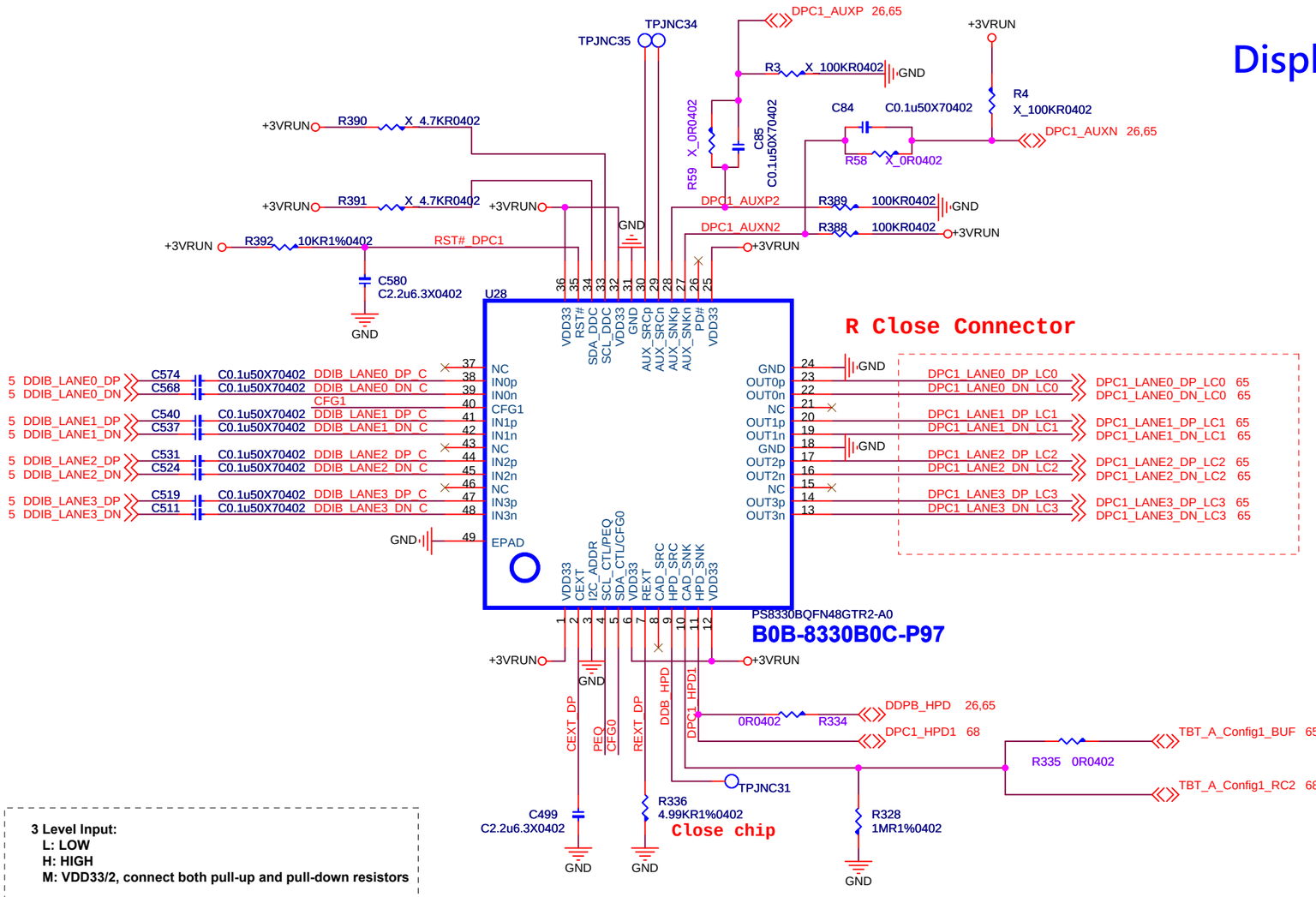
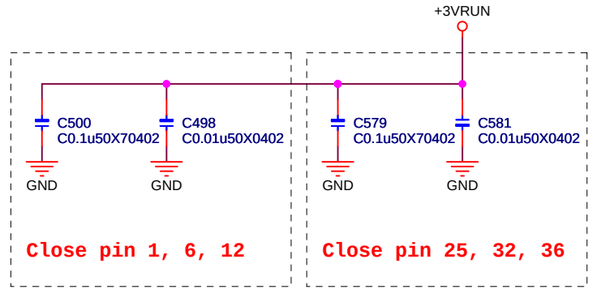
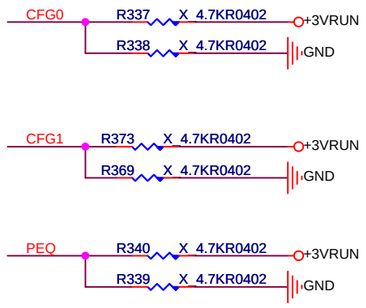
Display Port



R Close Connector



3 Level Input:
L: LOW
H: HIGH
M: VDD33/2, connect both pull-up and pull-down resistors



Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150k Ohm, 3.3V I/O.
L: default, automatic EQ enable & AUX interception enable
H: automatic EQ disable & AUX interception enable
M: automatic EQ disable & AUX interception disable, no pre-emphasis, 600mVpp swing

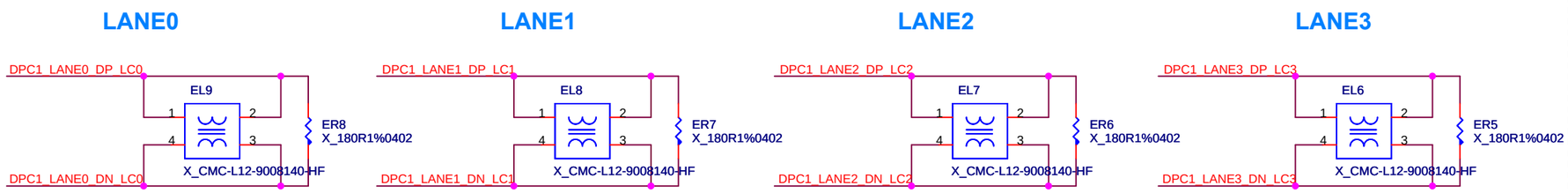
Configuration pin for auto test and input offset cancellation, 3.3V IO, internal pull up at ~150K Ohm
H: default, auto test disable & input offset cancellation enable
L: auto test enable & input offset cancellation enable
M: auto test disable & input offset cancellation disable

Programmable input equalization levels; Internal pull down at ~150k Ohm, 3.3V I/O.
L: default, LEQ, compensate channel loss up to 12dB @ HBR2
H: HEQ, compensate channel loss up to 15dB @ HBR2
M: LLEQ, compensate channel loss up to 5dB @ HBR2

CAD_SNK Have internal Pull down 1Mohm.

HPD_SNK Have internal Pull down 150kohm.
No problem with Leakage from DP device
The DP_PWR and RETURN pins of the box-to-box connectors must support the maximum current rating of 500mA.

EMI Close Connector



MICRO-STAR INT'L CO.,LTD.		
Title: DP witch Repeater		
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Audio CODEC/Audio AMP

L11 X_0R
JNC4 X_93519
C689 C0.1u50X70402
C139 C0.1u50X70402
C661 C0.1u50X70402
C660 C0.1u50X70402
EC20 X_C0.1u50X70402
EC21 X_C0.1u50X70402
GND AGND

CODEC_HDA_SDIN0
EC59 C10p50N0402
GND
EMI(RADIATION SOLUTION)

DVDD
Close Codec
+3VSUS
C650 C10u6.3X5-HF
C675 C0.1u50X70402
GND GND

Close Pin25
Close Pin38
CODEC_LDOOUT
C685 C10u6.3X5-HF
C682 C0.1u50X70402
C641 C10u6.3X5-HF
C648 C0.1u50X70402
AGND

AVDD5V
+5VSUS
1A
L10 180L1.5A-90
C671 C0.1u50X70402
C669 C10u6.3X5-HF
AGND AGND
AVDD5V

U34
DVDD 1
DVDD-IO 9
LDO-OUT1 25
LDO-OUT2 38

GND C643 X_C10p50N0402 34 EAPD 47 EAPD/SPDIFI
40 SPDIFO R457 10R1%0402 SPDIFO_R 48 SPDIF-OUT
22 CODEC_HDA_SDOUT 5 SDATA-OUT
22 CODEC_HDA_SDIN0 R471 33R0402 HD_SDIN 8 SDATA-IN
22 CODEC_HDA_SYNC 10 SYNC
22 CODEC_HDA_RST# 11 RESET#
22 CODEC_HDA_BIT_CLK 6 BCLK

REGREF
GND C663 C10u6.3X5-HF PDM_CLK 2 GPIO0/DMIC-CLK/SPDIF-OUT2
REGREF 3 REGREF
40 FRONT_JD R499 5.1KR1%0402 SENSEA 13 SENSE A
40 MIC_JD R498 20KR1%0402 34 SENSE B
MIC-VREFO-R 32 MIC1-VREFO-R
30 MIC2-VREFO
MIC-VREFO-L 28 MIC1-VREFO-L
VREF_ALC898 37 PIN37-VREFO
AVDD5V 29 LDO-IN
Close Codec 31 LINE2-VREFO
Close Codec AGND C673 C10u6.3X5-HF 27 VREF
AGND R458 20KR1%0402 JDREF 33 SENSE C
40 JDREF
22 HDA_SPKR R489 47KR1%0402 PC_BEEP_A C681 C1u25X0402 PC_BEEP 12 BEEP
R490 4.7KR0402
C680 C0.1u50X70402
GND GND
PDM_DATA 4 GPIO1/DMIC-DATA
7 DVSS
26 AVSS
42 AVSS
GND AGND
ALC892-CG
B05-LC89214-R09

FRONT-R 36 FRONT_OUT_R C657 C10u6.3X5-HF FRONT_OUTR 40
FRONT-L 35 FRONT_OUT_L C659 C10u6.3X5-HF FRONT_OUTL 40
SURR-R 41 BACK_SPK_R_F C646 C0.47u10X0402 BACK_SPK_R 40
SURR-L 39 BACK_SPK_L_F C649 C0.47u10X0402 BACK_SPK_L 40
CENTER 43
LFE 44
SIDE-R 46 HP_R_ADC_R C644 C1u25X0402 HP_R_ADC 33
SIDE-L 45 HP_L_ADC_R C645 C1u25X0402 HP_L_ADC 33
LINE1-R 24
LINE1-L 23
LINE2-R 15 FRONT_SPK_R_F C695 C0.47u10X0402 FRONT_SPK_R
LINE2-L 14 FRONT_SPK_L_F C694 C0.47u10X0402 FRONT_SPK_L
MIC1-R 22 MIC_R C700 C4.7u10X0603 MIC_R_C R502 75R1%0402
MIC1-L 21 MIC_L C699 C4.7u10X0603 MIC_L_C R507 75R1%0402
R497 2.2KR1%0402 MIC-VREFO-R
MIC_IN_R 40
MIC_IN_L 40
R508 2.2KR1%0402 MIC-VREFO-L
MIC2-R 17
MIC2-L 16
CD-R 20
CD-GND 19
CD-L 18

APA2051 Pin23: Gain Setting
Speaker Spec: 2.0W(Normal), 2.5W (Max)
Vo=(2*4)^0.5=2.828
dB-20LOG(Vo/Vi)
Gain: 2.828Vrms/1.2Vrms=2.36
7dB =~ 20LOG 2.36
7dB : Setting Pin23 on 3.1V
(R103:13Kohm, R106:22Kohm)

For 6dB When Using 1.5W (Normal)
(R103:10Kohm, R106:15Kohm)

AMP

+5VSUS
R109 100KR0402
+5VSUS
R103 10KR1%0402
6DB/1.5W
AGND C122 C1u25X0402 BIAS_AMP 22 BIAS
SET_AMP AGND 24 /AMP_EN
23 SET
AGND R122 0R1%0402 HP_EN 21 HP EN
3 NC
CP+_AMP 9 CP+
C138 C2.2u6.3X0402
CP-_AMP 11 CP-
28 INR_H
2 INL_H
Q8 NN-2N7002DW-7-F_SOT363-6-RH
D1 D2 S1 G1 S2 G2
34,40 EC_MUTE#
R114 15KR1%0402
AGND AGND
FRONT_SPK_R 27 INR_A
FRONT_SPK_L 1 INL_A
U14
ROUT+ 19 OUT_R+
ROUT- 18 OUT_R#
LOUT+ 5 OUT_L+
LOUT- 6 OUT_L#
HVDD 15 HVDD_AMP
VDD 25
GND 26 AGND
PVDD 17
PVDD 7
CVDD 8
PGND 20
PGND 4
CGND 10 AGND
VSS 12 VSS_AMP C140 C1u25X0402 AGND
NC 14
HP_R 13
HP_L 16
GND-PAD 29 AGND
R135 0R1%0402 +3VSUS
C135 C0.1u50X70402 AGND
C636 C10u6.3X5-HF AGND
C142 C1u25X0402 AGND
C137 C0.1u50X70402 AGND
C121 C0.1u50X70402 AGND
+5V_AMP
+5VSUS
L9 180L1.5A-90
50mil
APA2051QBI-TRG_TQFN28
I71-020510C-A30

EMI Close Codec

Internal Mic

R464 33R0402 PDM_CLK_CONN PDM_CLK_CONN 44
R468 0R1%0402 PDM_DATA_CONN PDM_DATA_CONN 44
PDM_CLK
PDM_DATA
EC58 X_C22p50N0402
C670 X_C22p50N0402
GND GND

Internal Speaker Conn

OUT_L# ER13 0R1%0402 OUT_L#_R
OUT_L+ ER14 0R1%0402 OUT_L+_R
OUT_R+ ER15 0R1%0402 OUT_R+_R
OUT_R# ER16 0R1%0402 OUT_R#_R
CON7
C711 X_C680p50X70402
C714 X_C680p50X70402
C727 X_C680p50X70402
C730 X_C680p50X70402
GND GND GND GND GND
BH1X4#S-1.25PITCH_WHITE
N32-1040AV0-H06

MSI MICRO-STAR INT'L CO.,LTD.
Title: Audio CODEC/Audio AMP
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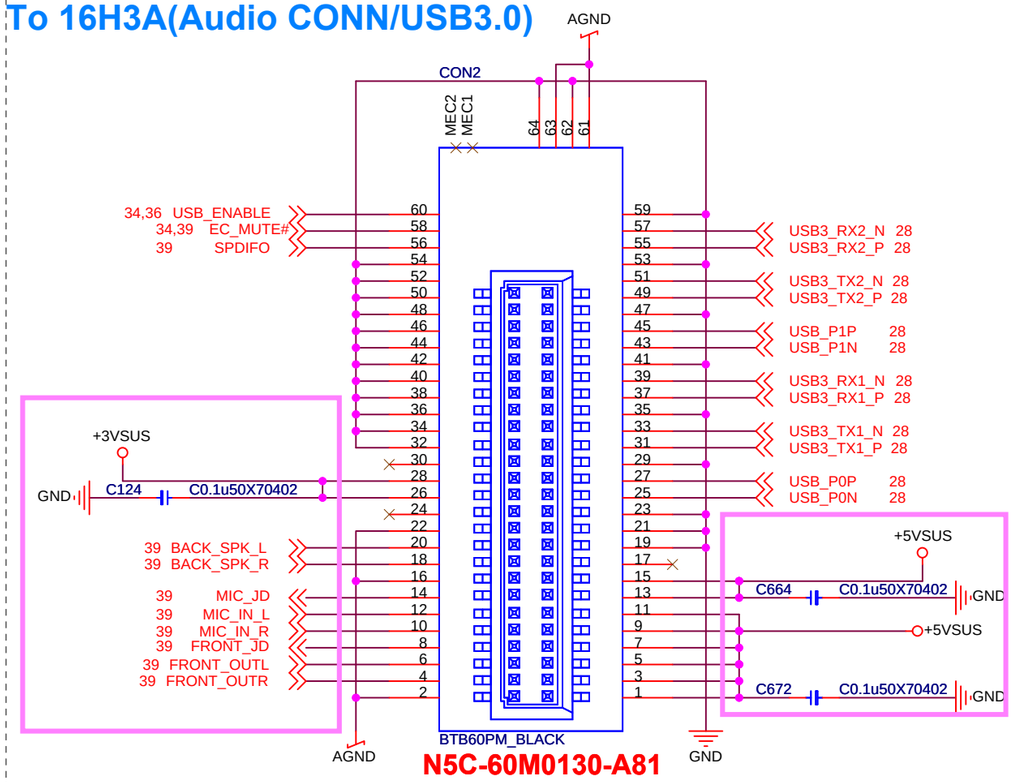
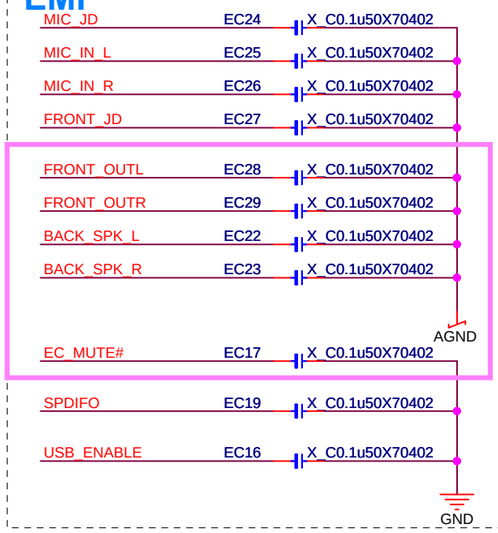
CPU FAN/BTB CONN

To 16H3A(Audio CONN/USB3.0)

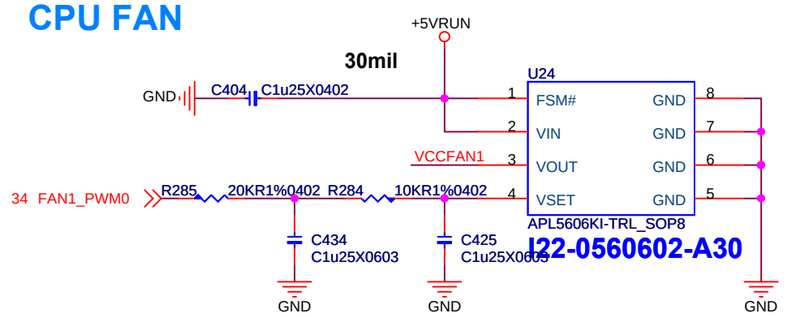


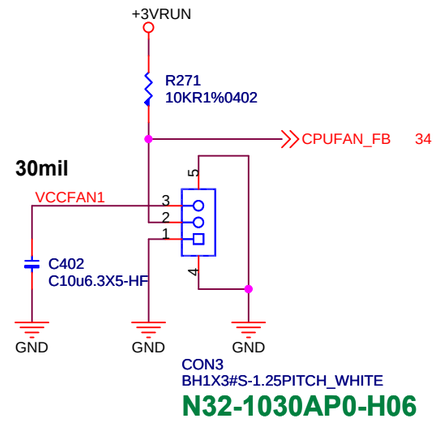
EMI



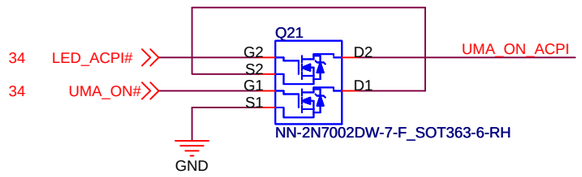
EMI

CPU FAN

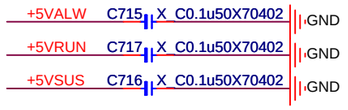


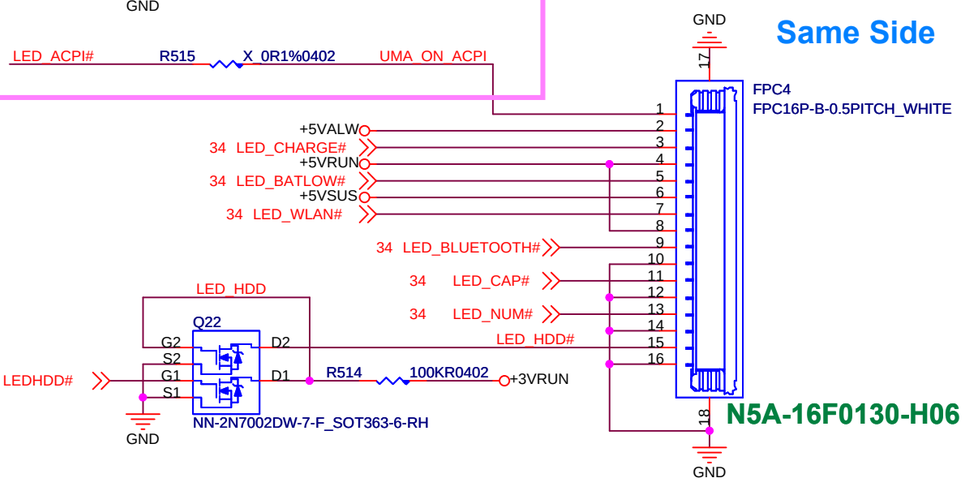


S3 Breath
S0 No active

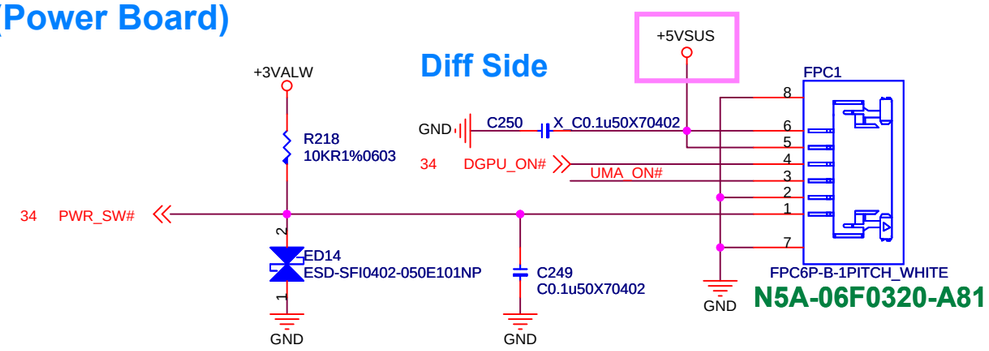


To 16H3B(LED Board)





To 16H3C (Power Board)



MICRO-STAR INT'L CO.,LTD.		
Title: CPU FAN/BTB CONN		
Size	Document Number: MS-16H3	Rev: 1.0
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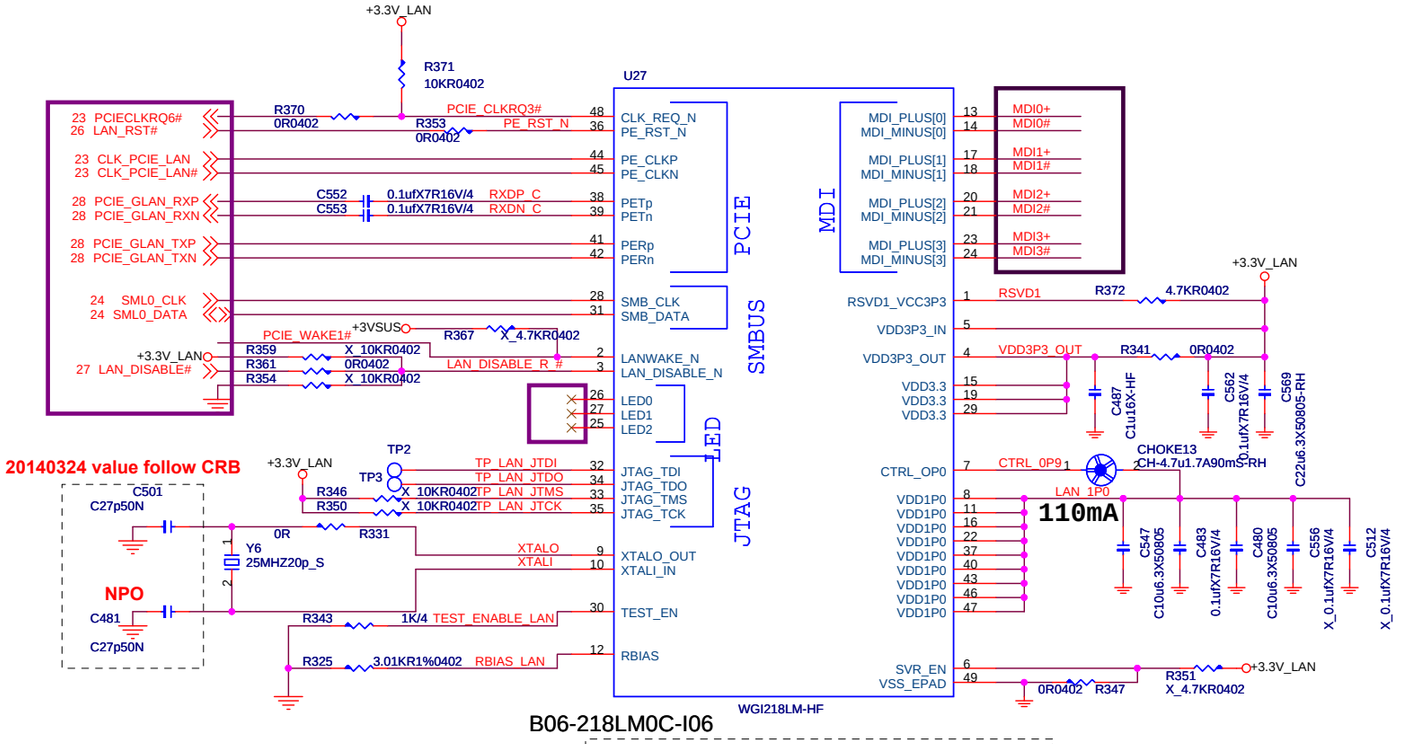
INTEL Clarkville LAN(I218LM)



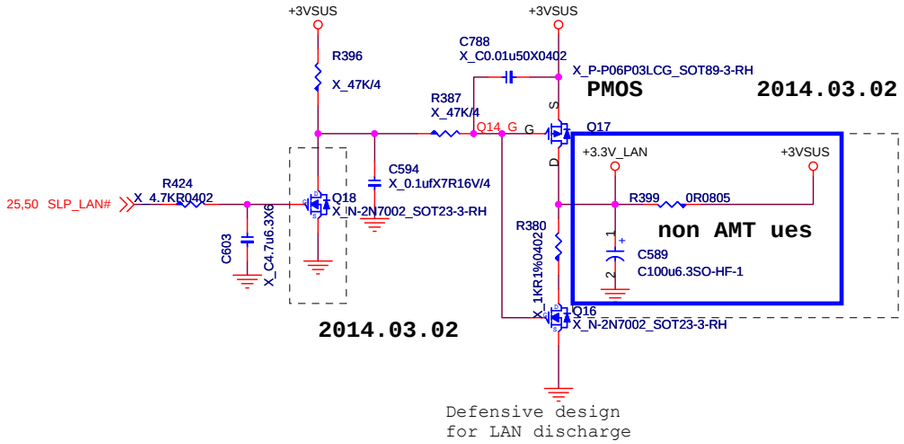
B06-218LM0C-I06

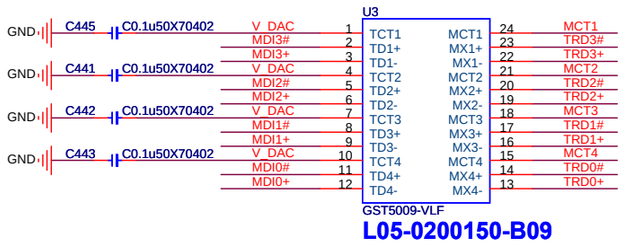
PCIE_WAKE1# R83 0R1%0402 PCIE_WAKE# 25,36,44,64

PCIE_WAKE1# R421 X_0R1%0402 PCH_GPIO_27 27,44

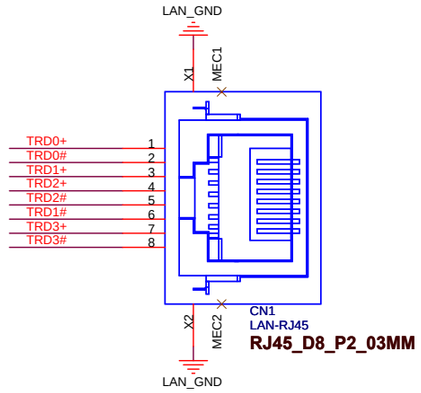
Note that the PHY SMBus address is 0xC8
and default MAC SMBus address is 0xE0.

+3.3V_LAN
(132mA)



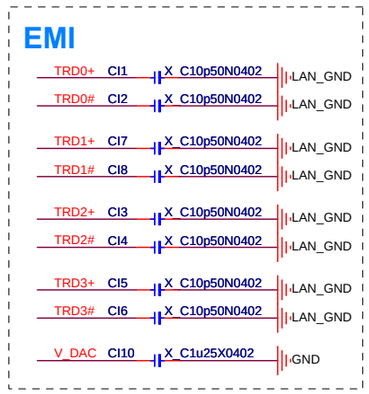


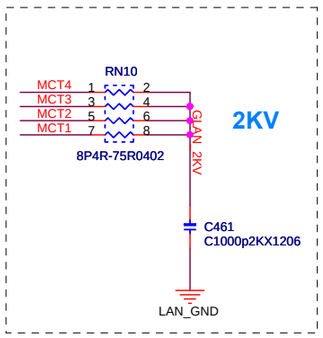
L05-0200150-B09

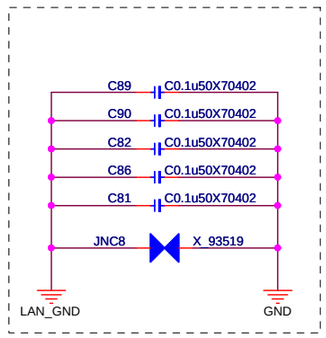


RJ45_D8_P2_03MM

N55-08F0691-AF2







MICRO-STAR INT'L CO.,LTD.			
Title: INTEL Clarkville LAN (I218LM)			
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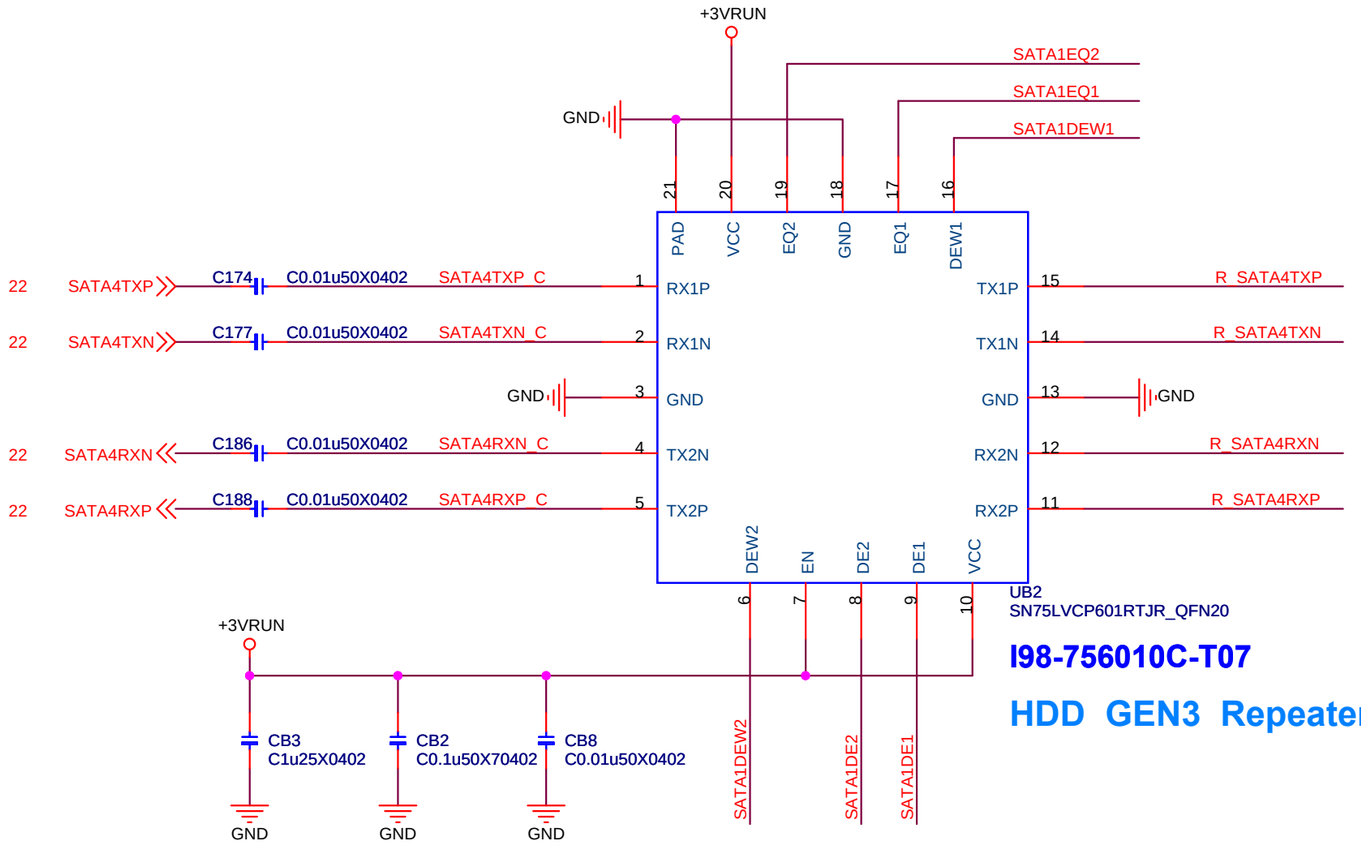
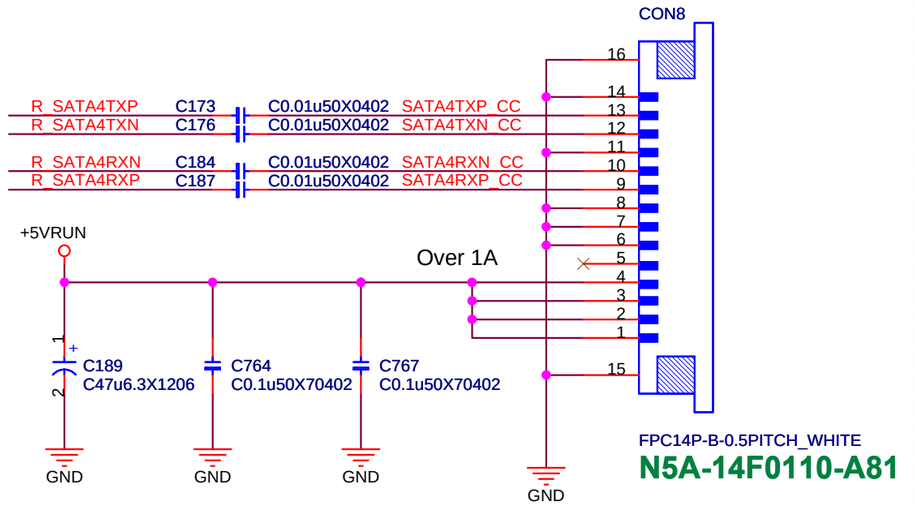
HDD (With Repeater)

+3VRUN:80mA



BTB Connecter



SATA1EQ1 R550 X_10KR1%0402 +3VRUN
SATA1EQ2 R551 X_10KR1%0402 +3VRUN
SATA1DE1 TPJNC20
SATA1DE2 TPJNC21
SATA1DEW1 R549 0R1%0402 GND
SATA1DEW2 R181 0R1%0402 GND

TI SN75LVCP601RTJR HW Setting

DE1/DE2	CH1/CH2De-Emphasis dB (at 6Gbps)	EQ1/EQ2	CH1/CH2Equalization dB (at 6Gbps)
NC (***default***)	–4	NC (***default***)	0
0	0	0	7
1	–2	1	14

DEW1/DEW2	Device Function → DE Width for CH1/CH2
0	De-emphasis pulse duration, short (recommended setting when link operates at SATA 1.5/3/6 Gbps)
1 (***default***)	De-emphasis pulse duration, long (recommended setting when link operates at SATA 1.5/3 Gbps speed only)

MICRO-STAR INT'L CO.,LTD.

Title: HDD With Repeater

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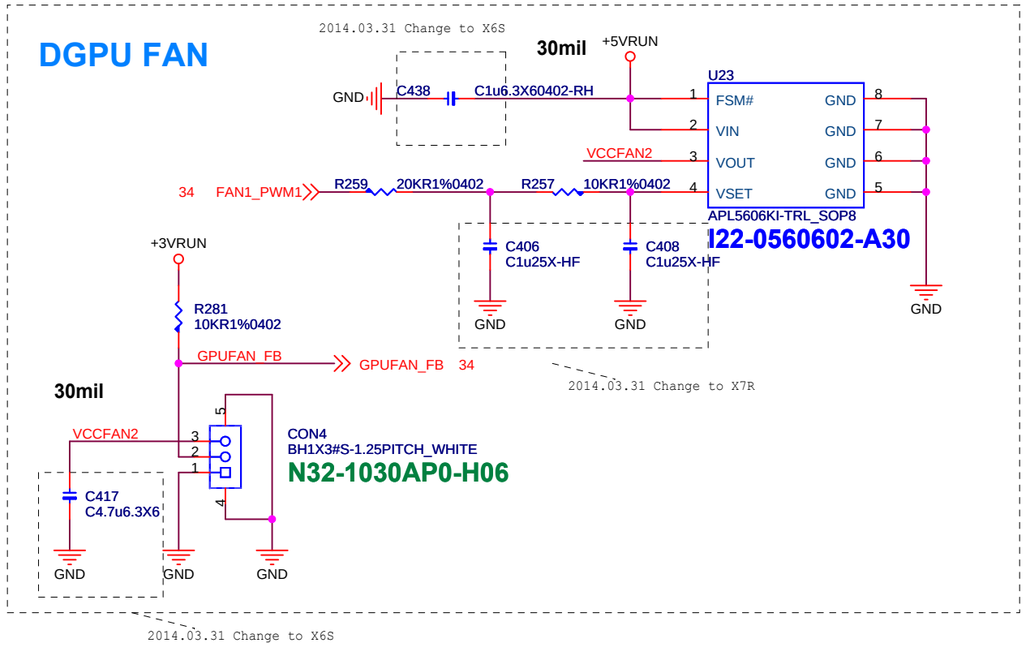
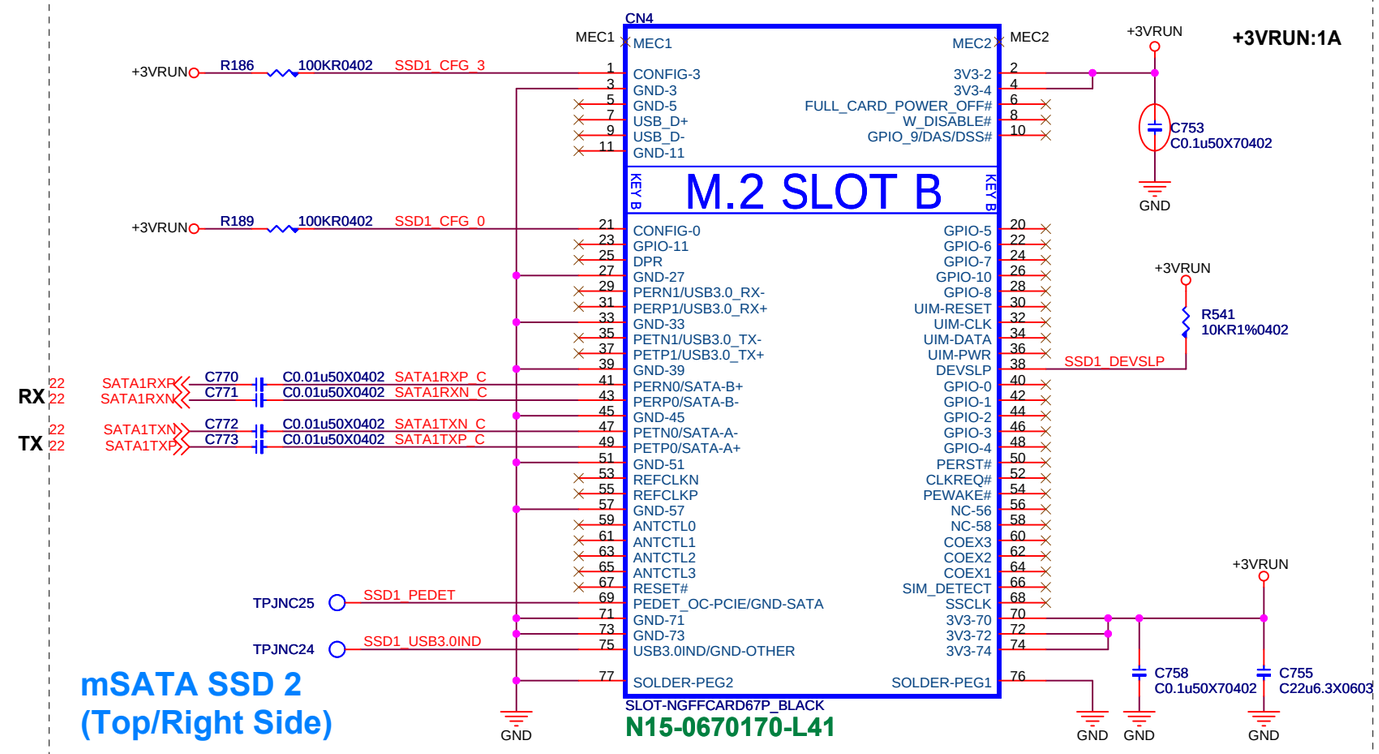
SSD/ DGPU FAN

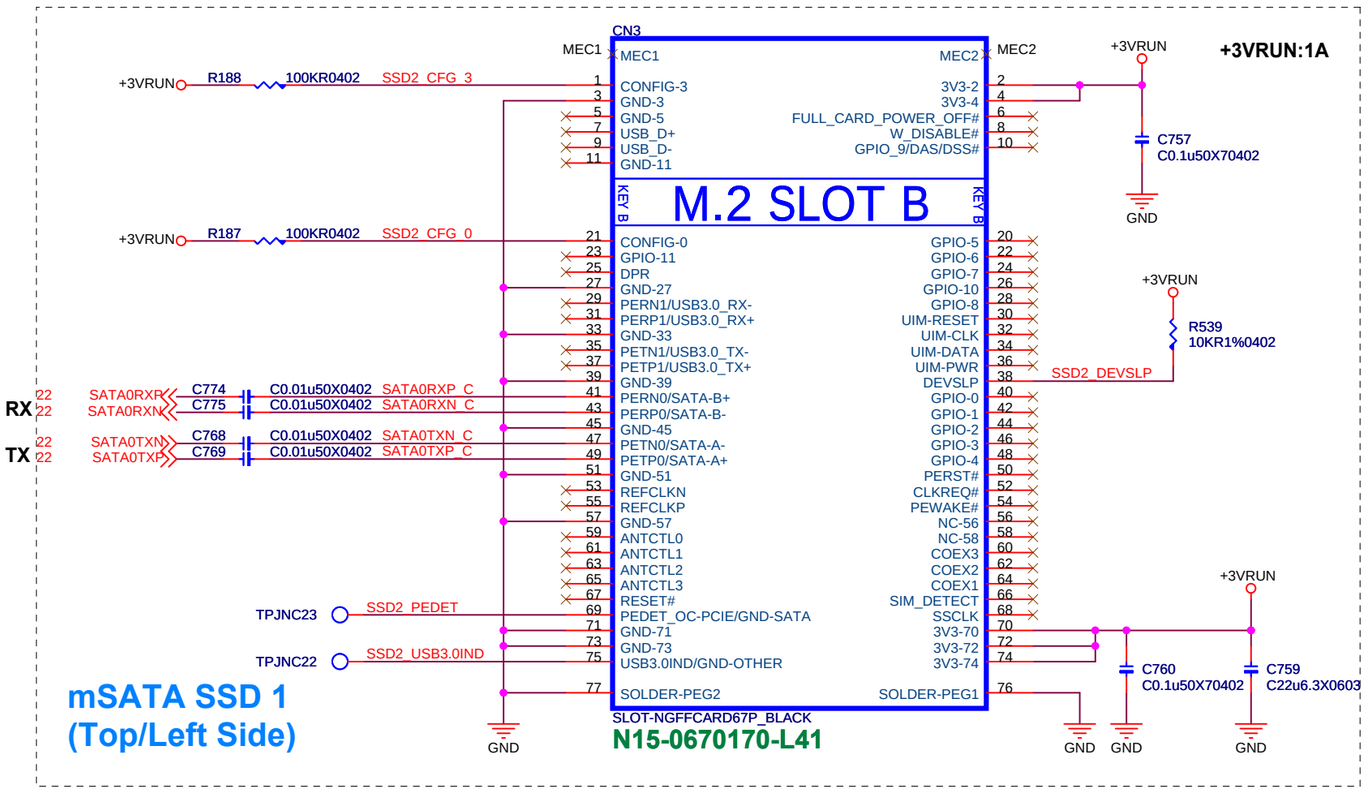
DGPU FAN



mSATA SSD 2 (Top/Right Side)



mSATA SSD 1 (Top/Left Side)



40	NC	No Connect
41	SATA-B+/PERn0	Host receiver differential signal pair
42	NC	No Connect
43	SATA-B-/PERp0	Host receiver differential signal pair
44	NC	No Connect
45	GND	Ground
46	NC	No Connect
47	SATA-A-/PETn0	Host Transmitter differential signal pair
48	NC	No Connect
49	SATA-A+/PETp0	Host transmitter differential signal pair

MICRO-STAR INT'L CO.,LTD.

Title: SSD/ DGPU FAN

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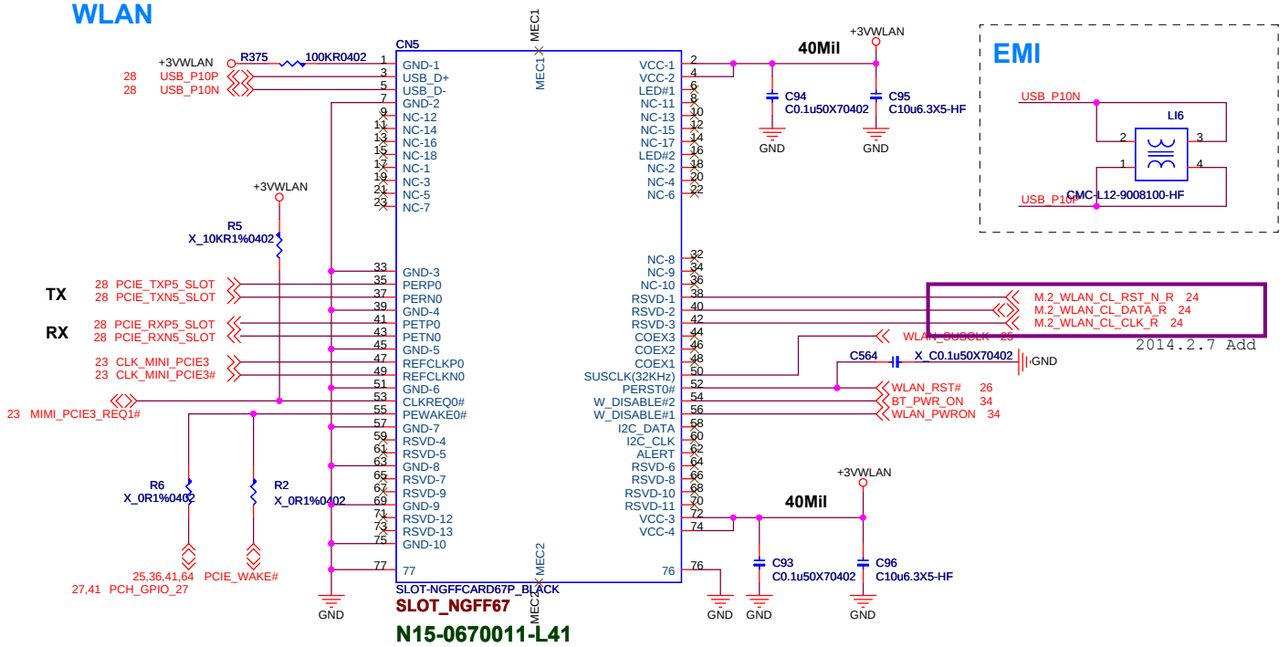
WLAN /Camera/ClickPad/FP

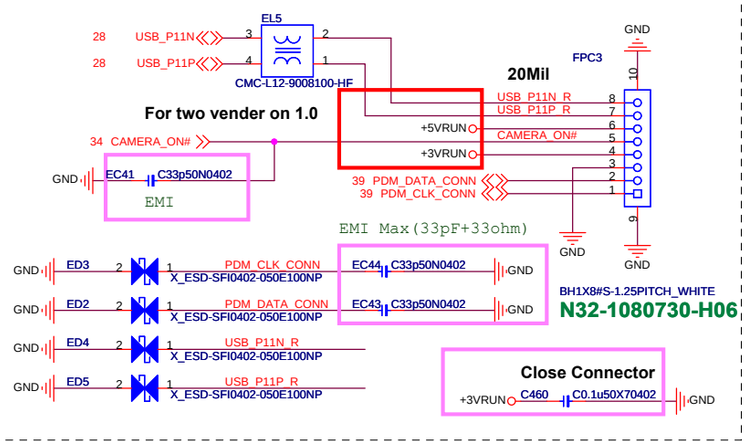
WLAN



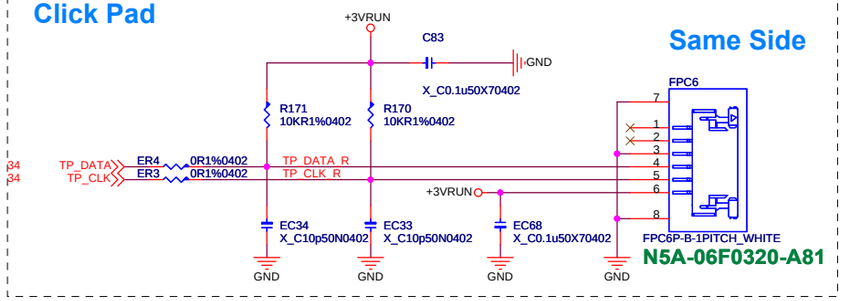
EMI

Pin 1	GND		
Pin 3	USB_D+	Pin 2	3.3V
Pin 5	USB_D-	Pin 4	3.3V
Pin 7	GND	Pin 6	LED1#
Pin 9	Module Key	Pin 8	Module Key
Pin 11	Module Key	Pin 10	Module Key
Pin 13	Module Key	Pin 12	Module Key
Pin 15	Module Key	Pin 14	Module Key
Pin 17	N/C	Pin 16	LED2#
Pin 19	N/C	Pin 18	GND
Pin 21	N/C	Pin 20	N/C
Pin 23	N/C	Pin 22	N/C
Pin 25	Module Key	Pin 24	Module Key
Pin 27	Module Key	Pin 26	Module Key
Pin 29	Module Key	Pin 28	Module Key
Pin 31	Module Key	Pin 30	Module Key
Pin 33	GND	Pin 32	N/C
Pin 35	PERP0	Pin 34	N/C
Pin 37	PERN0	Pin 36	N/C
Pin 39	GND	Pin 38	Clink Reset (I 3.3V)
Pin 41	PETP0	Pin 40	N/C
Pin 43	PETN0	Pin 42	N/C
Pin 45	GND	Pin 44	N/C
Pin 47	REFCLKP0	Pin 46	N/C
Pin 49	REFCLKN0	Pin 48	N/C
Pin 51	GND	Pin 50	N/C (SUSCLK (32kHz) for DSx)
Pin 53	CLKREQ0#	Pin 52	PERST0#
Pin 55	PEWAKE0#	Pin 54	BT_EN (W_DISABLE2#)
Pin 57	GND	Pin 56	WLAN_EN(W_DISABLE2#)
Pin 59	N/C	Pin 58	N/C
Pin 61	N/C	Pin 60	N/C
Pin 63	GND	Pin 62	N/C
Pin 65	N/C	Pin 64	Resever
Pin 67	N/C	Pin 66	N/C
Pin 69	GND	Pin 68	N/C
Pin 71	N/C	Pin 70	N/C
Pin 73	N/C	Pin 72	3.3V
Pin 75	GND	Pin 74	3.3V

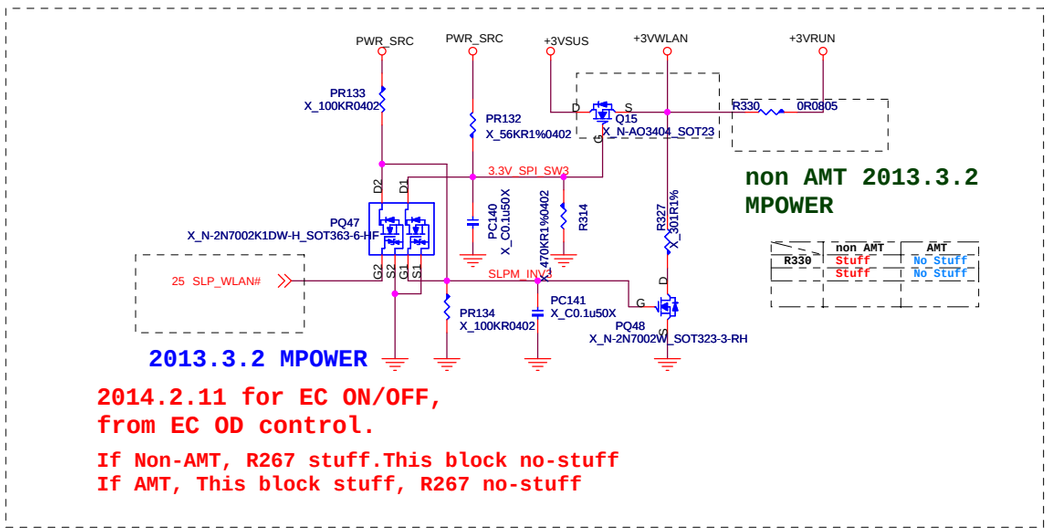
CAMERA



Click Pad



Same Side



R330	non AMT	AMT
	Stuff	No Stuff
	Stuff	No Stuff

MICRO-STAR INT'L CO.,LTD.

Title: WLAN /Camera/ClickPad/FP

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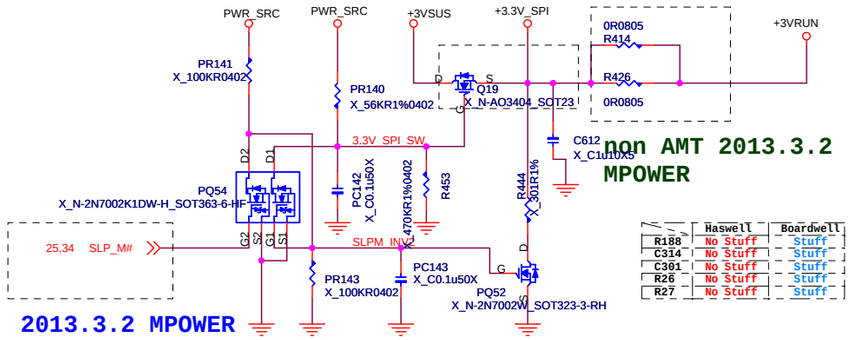
+3.3V_SPI

2A in 2013.3.2 MPOWER



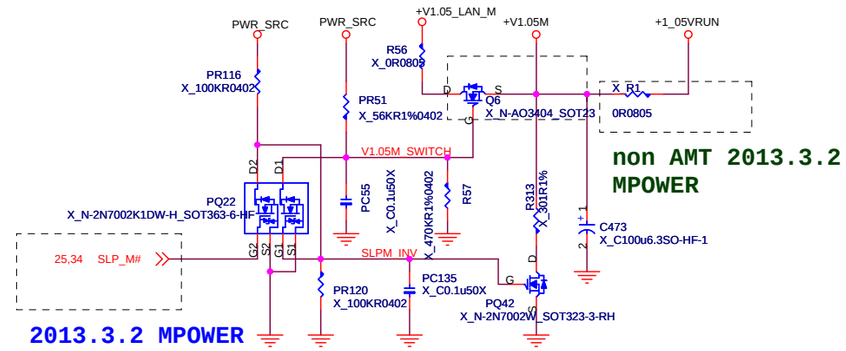
non AMT 2013.3.2 MPOWER

	Haswell	Boardwell
R188	No Stuff	Stuff
C314	No Stuff	Stuff
C301	No Stuff	Stuff
R26	No Stuff	Stuff
R27	No Stuff	Stuff

2013.3.2 MPOWER

+V1.05M

+V1.05M 2A in 2013.3.2 MPOWER



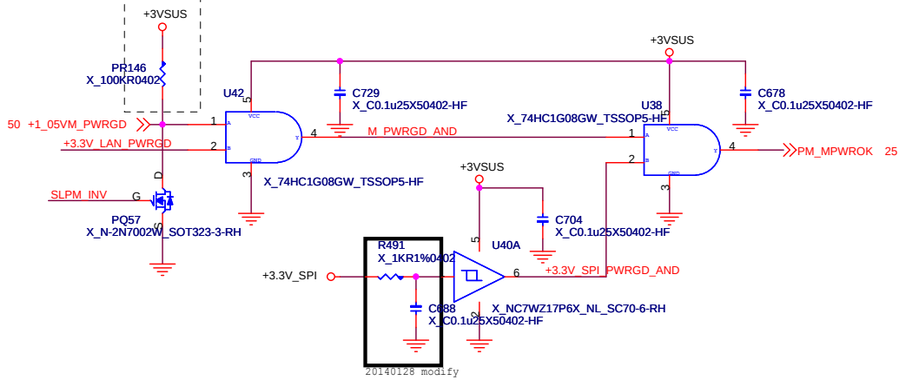
non AMT 2013.3.2 MPOWER

2013.3.2 MPOWER

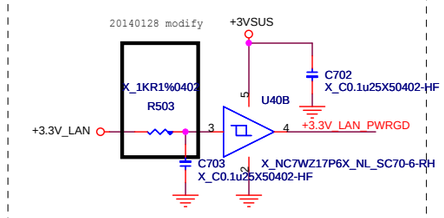
請靠近 PCH

2013.3.2 for AMT

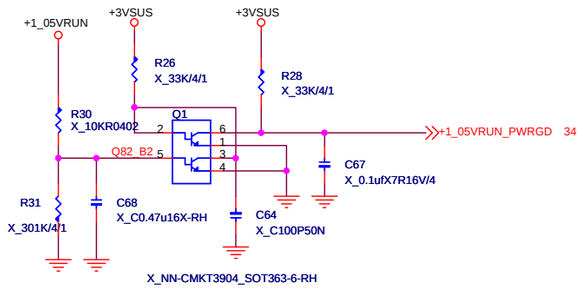
AMT PWRGD



+3.3V_LAN_PWRGD



+1_05VRUN_PWRGD, AMT used



MICRO-STAR INT'L CO.,LTD.

Title: M-POWER

Size: | Document Number: MS-16H3 | Rev: 1.0

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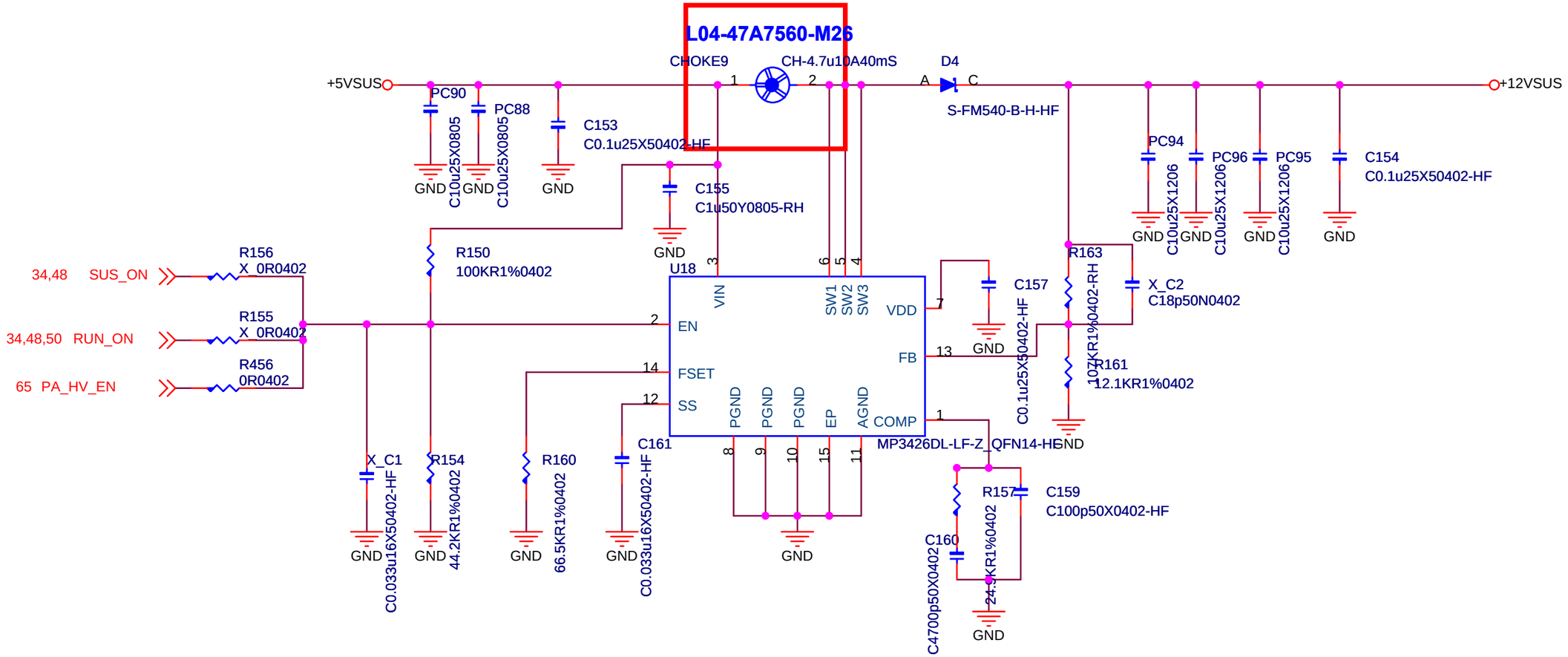
TBT Power 5V Boost 12V 1A



MICRO-STAR INT'L CO.,LTD.		
Title: Thunderbolt Power		
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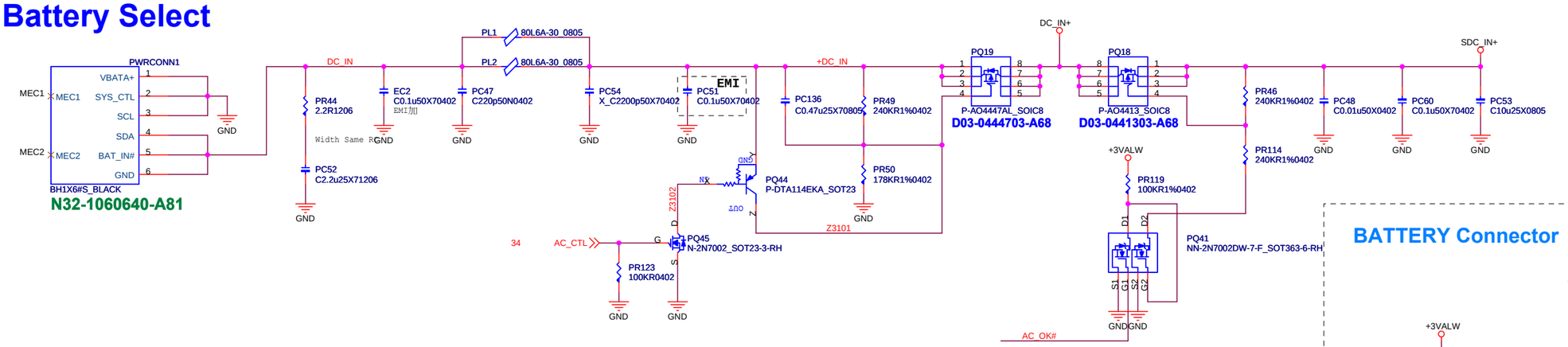
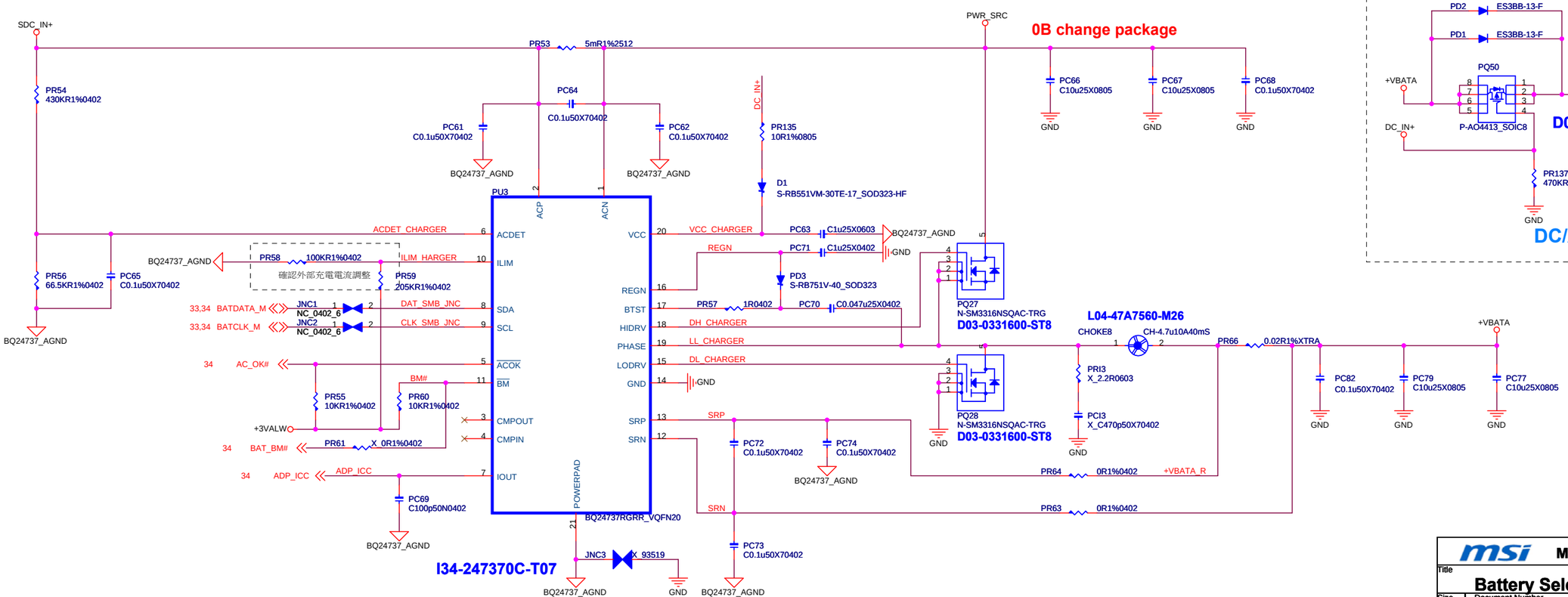
Battery Select/Charger

Battery Select



Battery Charger



MSI	MICRO-STAR INT'L CO.,LTD.		
Title	Battery Select/Charger		
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System Power

OCP 13A
MAX 10A

+3VSUS

PWR_SRC
Close to high side Mosfet
PC110 C10u25X0805
PC102 C0.1u50X70402
PC108 C2200p50X70402
GND

PQ31 D03-0331600-ST8
N-SM3316NSQAC-TRG
PR163 2.2R0603
PC149 C0.1u50X
L04-47A7620-M26
CHOKE12 CH-4.7u13A15.0mS
+3VSUS
PEC12 C220u6.3SO
PC100 C10u25X0805
PQ32 N-SM3317NSQAC-TRG D03-0331700-ST8
PRI5 X_2.2R0603
PCI5 X_C2200p50X70402
PR155 6.8KR1%0402
3.35V
PR157 10KR1%0402

PQ29 D03-0331600-ST8
JNC5 X_0402 RUND
+3VRUN
N-SM3316NSQAC-TRG
+3VRUN

PWR_SRC
0B change PN
PC97 C1u25X70805
34,46 SUS_ON
PR162 100KR0402
SUSPWROK
SUSPWROK 34
PR160 10KR1%0402 +3VALW

PU9 **I32-512250C-T07**
TPS51225CRUKR_QFN20
VBST2 DRVH2 SW2 DRVL2 VFB2 GPAD
VBST1 DRVH1 SW1 DRVL1 VO1 VFB1
EN2 EN1 VIN PGOOD CS2 CS1 VERG3 VREG5 VCLK
DH2 LL2 DL2 3V_FB
DH1 LL1 DL1 5V_FB
PR156 115KR1%0402-RH
PR161 100KR1%0402
PC147 C1u25X0603 **+3VALW**
PC151 C1u25X0603 **+5VALW**

PWR_SRC
Close to high side Mosfet
PC109 C2200p50X70402
PC112 C10u25X0805
PC111 C10u25X0805
GND

PQ30 D03-0331600-ST8
N-SM3316NSQAC-TRG
PC150 C0.1u50X
PR165 2.2R0603
L04-47A7620-M26
CHOKE11 CH-4.7u13A15.0mS
PCI6 X_C2200p50X70402
PR164 X_2.2R0603
PQ33 N-SM3317NSQAC-TRG D03-0331700-ST8
PR159 15KR1%0402
PR158 10KR1%0402
PC152 C10u25X0805
PEC13 C220u6.3SO
+5VSUS

OCP 13A
MAX 10A

+5VSUS

PQ61 N-SM3316NSQAC-TRG D03-0331600-ST8
RUND
+5VRUN
+5VRUN

PWR_SRC
PR147 100KR0402
RUN_ON_R
PR154 47KR1%0402
RUND 20,37,49,50
PQ59 NN-2N7002DW-7-F_SOT363-6-RH
PR153 470KR1%0402
PC146 C0.1u50X70402
34,46,50 RUN_ON
PR151 100KR0402
PC144 C0.1u50X70402

MICRO-STAR INT'L CO.,LTD.			
Title: System Power			
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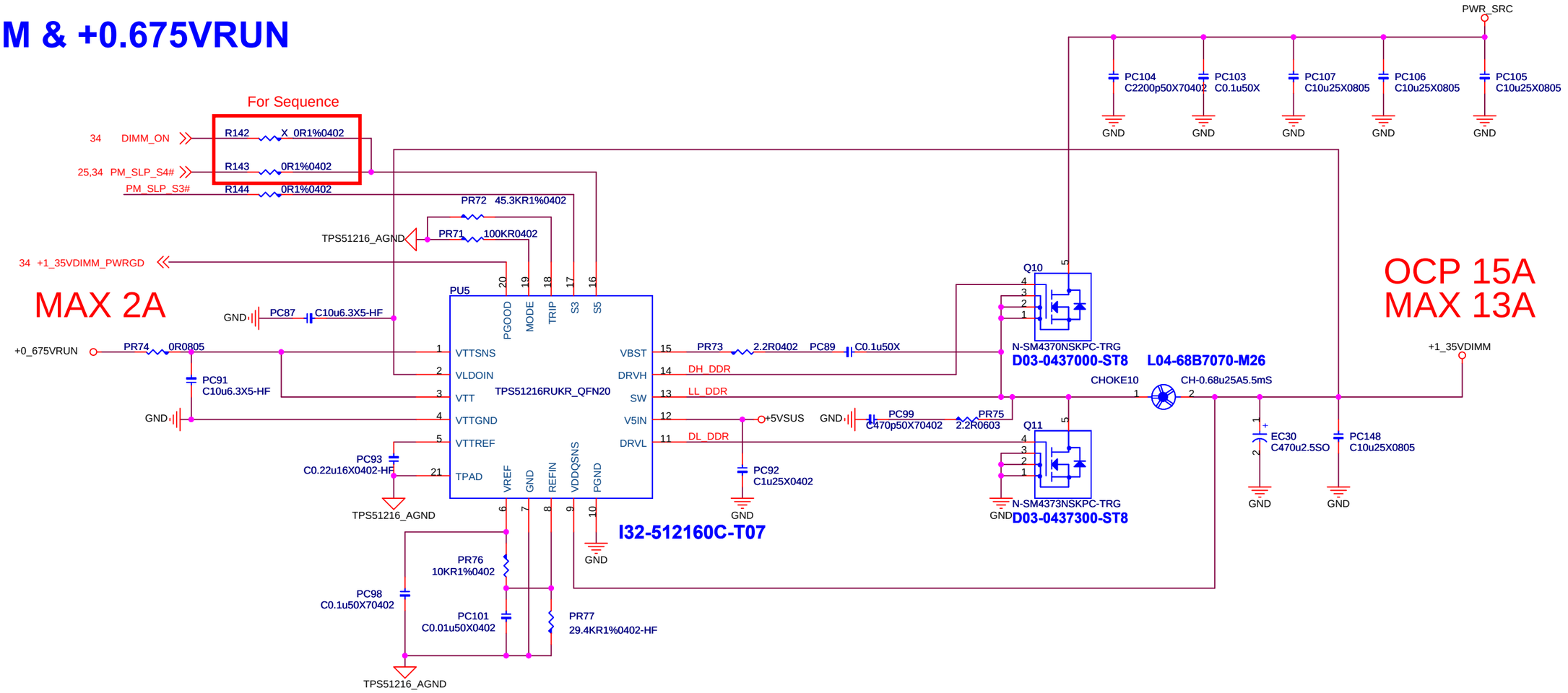
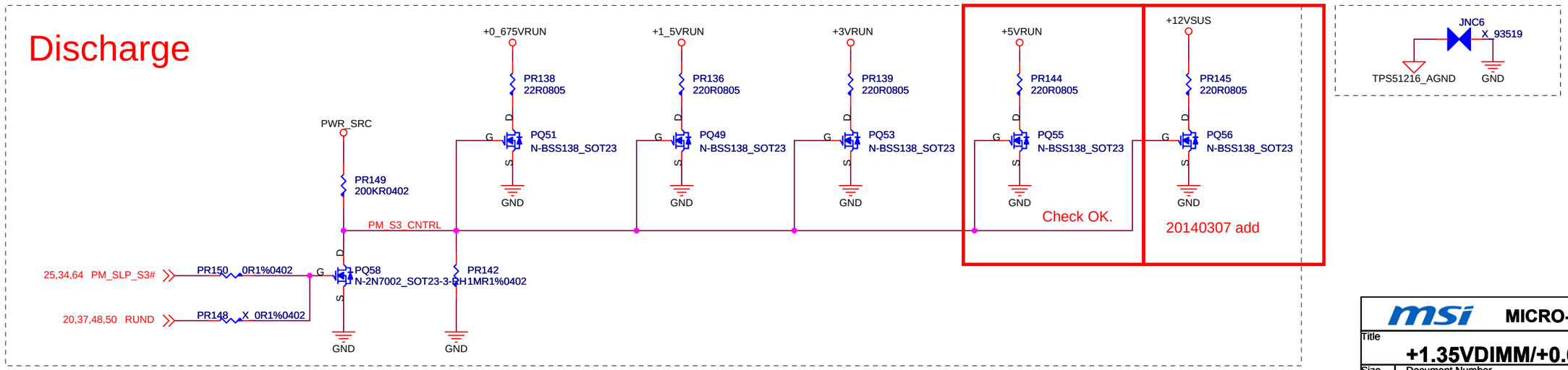
+1.35VDIMM/+0.675VRUN

+1.35VDIMM & +0.675VRUN





MICRO-STAR INT'L CO.,LTD.		
Title: +1.35VDIMM/+0.675VRUN		
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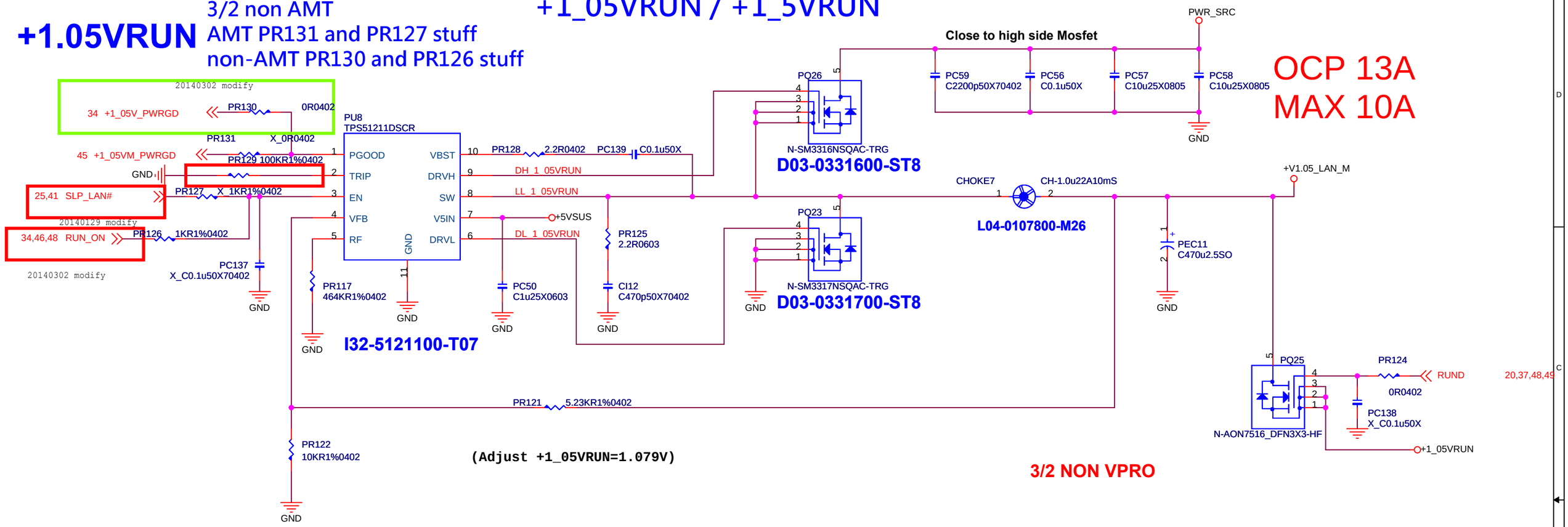
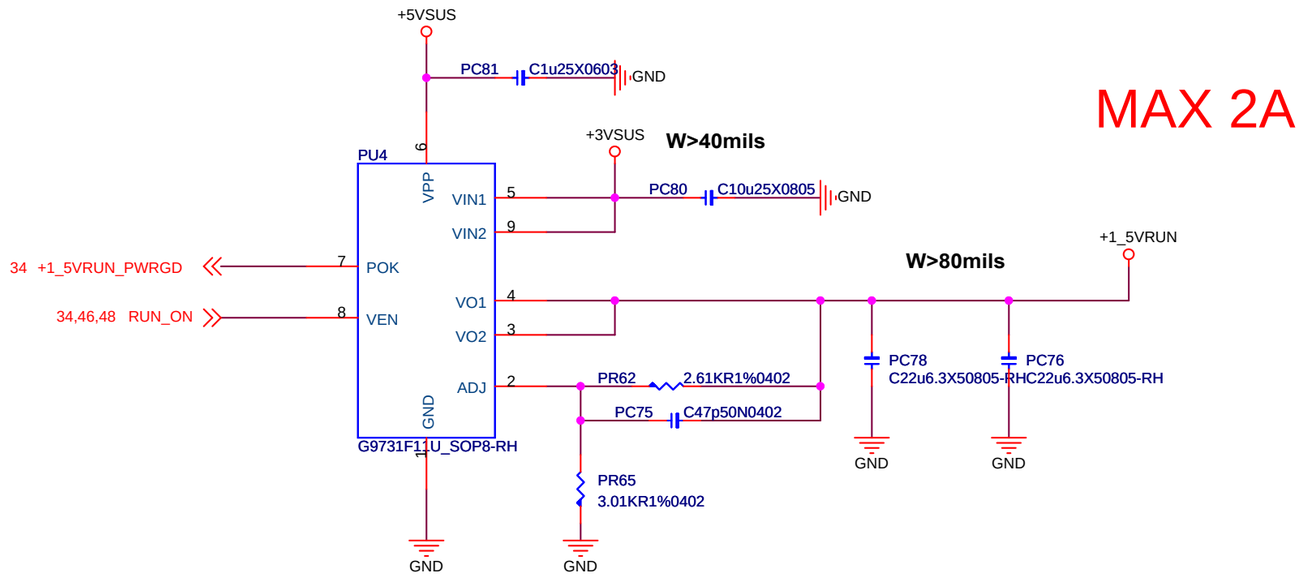
+1.05VRUN

3/2 non AMT
AMT PR131 and PR127 stuff
non-AMT PR130 and PR126 stuff

+1_05VRUN / +1_5VRUN



+1.5VRUN



MICRO-STAR INT'L CO.,LTD.		
Title: +1_05VRUN / +1_5VRUN		
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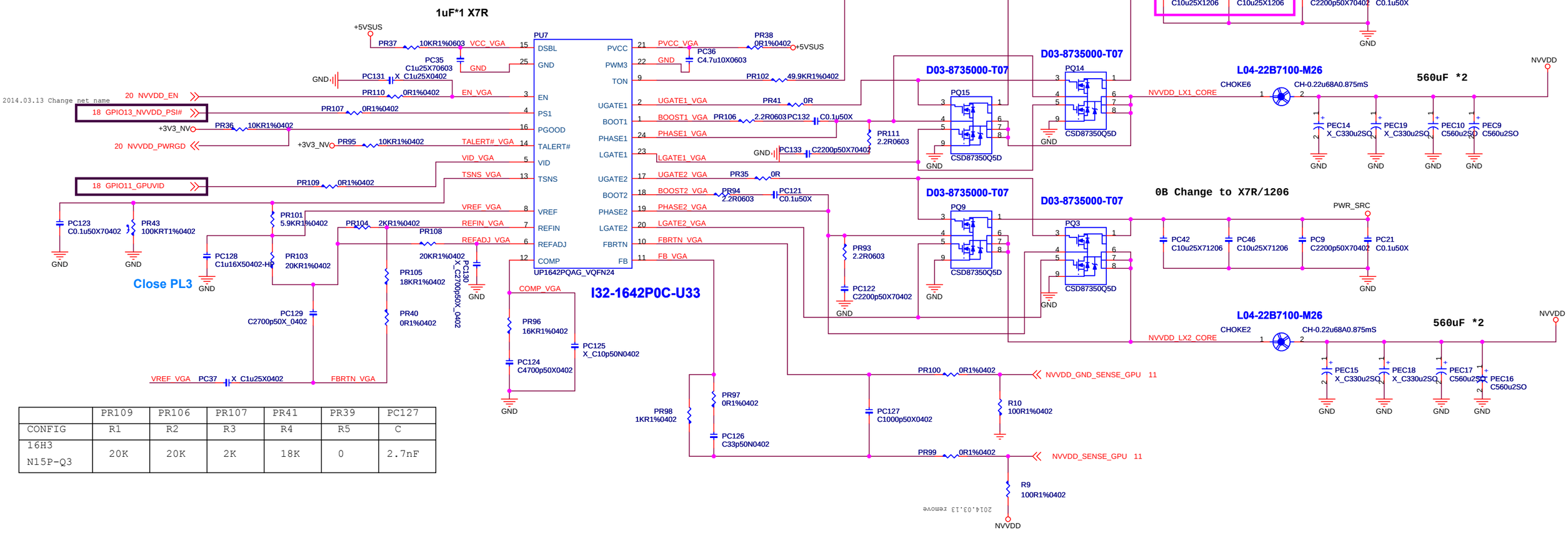
DGPU POWER NVVDD

DGPU POWER / UP1642PQAG

CONFIG B
VBoot:0.9V
Vmin:0.6V / Vmax:1.2V

EDP-Peak 57A
EDP-MAX 49A
EDP-Con 37A



	PR109	PR106	PR107	PR41	PR39	PC127
CONFIG	R1	R2	R3	R4	R5	C
16H3 N15P-Q3	20K	20K	2K	18K	0	2.7nF

MICRO-STAR INT'L CO.,LTD.

Title: DGPU POWER NVVDD

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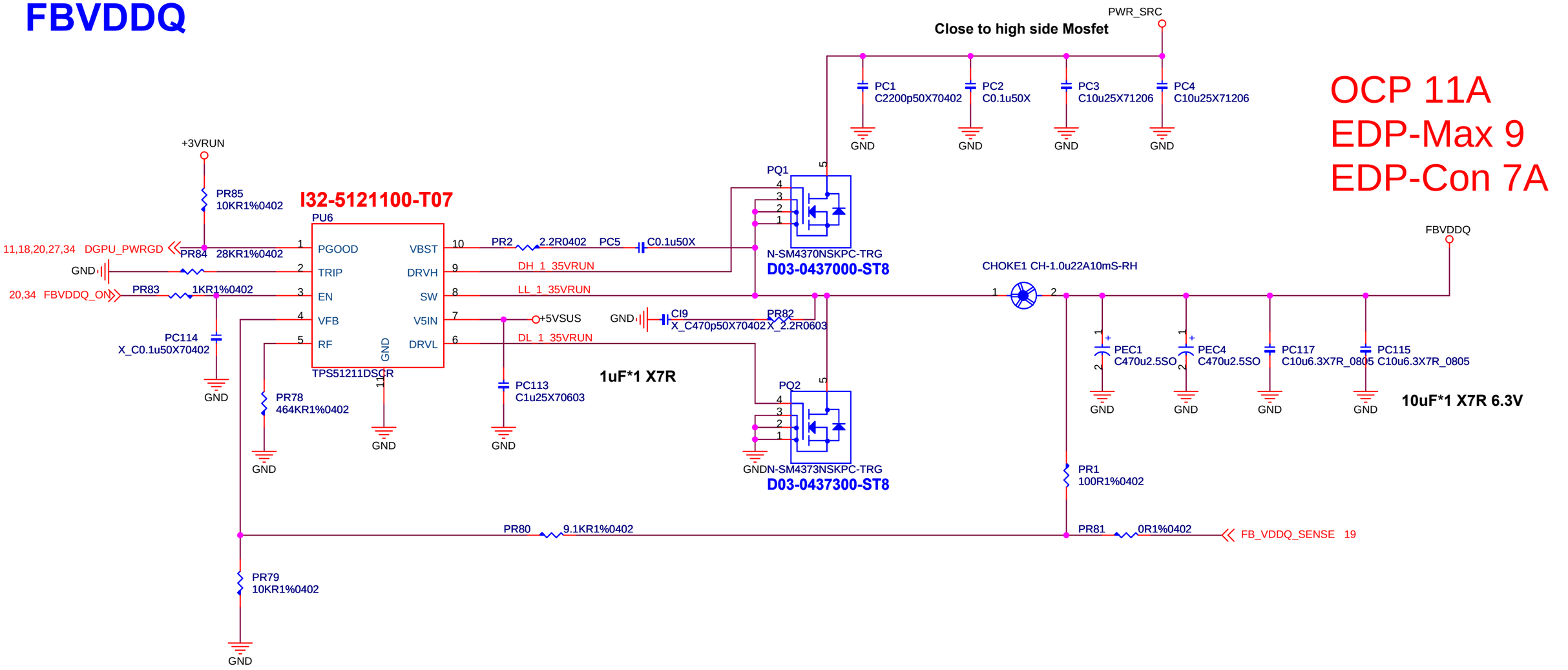
DGPU POWER FBVDDQ

FBVDDQ



MICRO-STAR INT'L CO.,LTD.			
Title: DGPU POWER FBVDDQ			
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CPU Core Power(ISL95812HRZ)

CPU Power (+VCC_CORE)

MAX 95A
TDC 27A

ALERT#走SDA&SCLK中間，間距18mil

PU1 ISL95812HRZ-T_QFN32

+5VSUS PR4 1R0402 +V95812 PC12 C2.2u10X0603
PWR_SRC PR3 0R1%0402 PC11 C0.22u25X70603
+5VSUS PR5 1R0402 PC14 C2.2u10X0603

+3VSUS PR30 1.91KR1%0402
6 VR_SVID_ALERT# 6 VR_SVID_DATA 6 VR_SVID_CLK → ALERT# SDA SCLK
25 CPU_PWROK 34 EC_ALLSYSPG → PGOOD VR_ON
3 IMVP_PROCHOT# → VR_HOT#
PC31 X_C0.1u50X70402
PR33 2.2KR1%0402 PC28 C3300p50X70402
PC29 C82p50N0402 → COMP
PC32 X_C330p16N0402 PR34 X_3KR1%0402
PC30 C100p50N0402 PR32 910R1%0402 → FB
PR27 2.7KR1%0402 FB_CPU
PR91 0R1%0402 PR88 8.06KR1%0402 → SLOPE
C10 C47p50N0402

6 VCCSENSE → PC120 X_C1000p50X0402 → RTN
7 VSSSENSE → PR89 10R1%0402 PC118 C0.01u50X0402

IMON_CPU → IMON
PROG1_CPU → PROG1
PROG2_CPU → PROG2
PROG3_CPU → PROG3
THERMAL PAD
NTC_CPU → NTC

PC27 C560p50N0402
PR31 80.6KR1%0402
PR23 21KR1%0402
PR16 49.9KR1%0402
PR20 34KR1%0402

PR90 3.83KR1%0402
PR92 27.4KR1%0402
PRT1 470KRT3%0402 靠近一項限MOS

VDDP PR87 0R1%0402 PC116 C0.22u16X0402-HF
BOOT1 PRI4 2.2R0603 PCI4 C470p50X70402
UGATE1 PHASE1 LGATE1

PQ6 PQ5 PQ4 N-SM4370NSKPC-TRG D03-0437000-ST8
PQ5 PQ4 N-SM4373NSKPC-TRG D03-0437300-ST8

PC23 C10u25X1206 PC10 C10u25X1206 PC13 C0.1u50X70402 PC17 C2200p50X70402
PEC3 C100u35EL

L04-22B7100-M26 CHOKE3 CH-0.22u68A0.875mS
VSUM+ PR11 3.65KR1%0402
ISEN1 PR10 10KR1%0402
PR12 X_10KR1%0402 V2N
PC22 C0.22u16X0402-HF PR14 X_10KR1%0402 V3N
VSUM- PR15 10R1%0402 V1N
PEC6 C330u2SO PEC5 C330u2SO
+VCC_CORE

0B change PN

BOOT2 PR13 0R1%0402 PC20 C0.22u16X0402-HF
UGATE2 PHASE2 LGATE2
PRI1 2.2R0603 PCI1 C470p50X70402
PQ10 PQ8 PQ7 N-SM4370NSKPC-TRG D03-0437000-ST8
PQ8 PQ7 N-SM4373NSKPC-TRG D03-0437300-ST8

PC25 C0.1u50X70402 PC34 C10u25X1206 PC33 C10u25X1206 PC119 C2200p50X70402
PEC2 C100u35EL

L04-22B7100-M26 CHOKE4 CH-0.22u68A0.875mS
VSUM+ PR18 3.65KR1%0402
ISEN2 PR17 10KR1%0402
PR19 X_10KR1%0402 V1N
PC24 C0.22u16X0402-HF PR21 X_10KR1%0402 V3N
VSUM- PR22 10R1%0402 V2N
PEC7 C330u2SO
+VCC_CORE

PWM3 → PWM3
ISEN1 ISEN2 ISEN3 → ISEN1 ISEN2 ISEN3
please help me rename
0B change PN
PR86 6.8MR0603

ISUNP ISUMN → VSUM+ VSUM-
PC19 X_C470p50X0402 PR6 X_1.5KR1%0402
PC15 C0.33u16X5
PC18 X_C0.22u16X0402-HF
PR7 11KR1%0402
PR8 453R1%0402
PR9 2.61KR1%0402
PRT2 10KRT0603 靠近一項限Chock
PC16 C0.1u50X70402

0B change PN

PU2 ISL6208BCRZ_QFN8
V_DRIVER → FCCM
GND → GND
PHASE3 → PHASE
LGATE → LGATE
PWM → PWM3
BOOT → PR42 0R1%0402 PC39 C0.22u16X0402-HF
UGATE → UGATE
VCC → V_DRIVER PR39 0R1%0402 +5VSUS
PC38 C2.2u10X0603 GND
THERMAL PAD
I33-062081C-I11

PQ13 N-SM4370NSKPC-TRG D03-0437000-ST8
PC41 C0.1u50X70402 PC40 C2200p50X70402 PC44 C10u25X71206 PC43 C10u25X71206

0B Change to X7R/1206

PRI2 2.2R0603 PCI2 C470p50X70402
PQ11 PQ12 N-SM4373NSKPC-TRG D03-0437300-ST8

L04-22B7100-M26 CHOKE5 CH-0.22u68A0.875mS
VSUM+ PR29 3.65KR1%0402
ISEN3 PR28 10KR1%0402
PR24 X_10KR1%0402 V1N
PC26 C0.22u16X0402-HF PR26 X_10KR1%0402 V2N
VSUM- PR25 10R1%0402 V3N
PEC8 C330u2SO
+VCC_CORE

I32-958120C-I11

MICRO-STAR INT'L CO.,LTD.	
Title	CPU Power (ISL95812HRZ)
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Date: Wednesday, June 25, 2014	Sheet 53 of 69

EMI/ Impedence

Impedence Connector No PN

40 ohm

J29 — 2 L1_6.5mil_40_Ohm; 1 GND2 — X_H1X2M_BLACK
J21 — 2 L3_5mil_40_Ohm; 1 GND2_GND4 — X_H1X2M_BLACK
J14 — 2 L10_5mil_40_Ohm; 1 GND9_GND11 — X_H1X2M_BLACK

45 ohm

J31 — 2 L1_5.5mil_45_Ohm; 1 GND2 — X_H1X2M_BLACK
J28 — 2 L3_4mil_45_Ohm; 1 GND2_GND4 — X_H1X2M_BLACK
J4 — 2 L5_4mil_45_Ohm; 1 GND4_GND6 — X_H1X2M_BLACK
J20 — 2 L10_4mil_45_Ohm; 1 GND9_GND11 — X_H1X2M_BLACK
J9 — 2 L12_5.5mil_45_Ohm; 1 GND11 — X_H1X2M_BLACK

50 ohm

J30 — 2 L1_4mil_50_Ohm; 1 GND2 — X_H1X2M_BLACK
J27 — 2 L3_3mil_50_Ohm; 1 GND2_GND4 — X_H1X2M_BLACK
J12 — 2 L5_3mil_50_Ohm; 1 GND4_GND6 — X_H1X2M_BLACK
J13 — 2 L10_3mil_50_Ohm; 1 GND9_GND11 — X_H1X2M_BLACK
J1 — 2 L12_4mil_50_Ohm; 1 GND11 — X_H1X2M_BLACK

80 ohm

J35 — L1_DIFF_4.5/4/4.5_80ohm+ / L1_DIFF_4.5/4/4.5_80ohm- — X_H1X4_BLACK — GND2
J25 — L3_DIFF_4.5/7/4.5_80ohm+ / L3_DIFF_4.5/7/4.5_80ohm- — X_H1X4_BLACK — GND2_GND4
J10 — L5_DIFF_4.5/7/4.5_80ohm+ / L5_DIFF_4.5/7/4.5_80ohm- — X_H1X4_BLACK — GND4_GND6
J16 — L10_DIFF_4.5/7/4.5_80ohm+ / L10_DIFF_4.5/7/4.5_80ohm- — X_H1X4_BLACK — GND9_GND11
J2 — L12_DIFF_4.5/4/4.5_80ohm+ / L12_DIFF_4.5/4/4.5_80ohm- — X_H1X4_BLACK — GND11

85 ohm

J36 — L1_DIFF_4.5/4.5/4.5_85ohm+ / L1_DIFF_4.5/4.5/4.5_85ohm- — X_H1X4_BLACK — GND2
J26 — L3_DIFF_4/6.5/4_85ohm+ / L3_DIFF_4/6.5/4_85ohm- — X_H1X4_BLACK — GND2_GND4
J11 — L5_DIFF_4/6.5/4_85ohm+ / L5_DIFF_4/6.5/4_85ohm- — X_H1X4_BLACK — GND4_GND6
J18 — L10_DIFF_4/6.5/4_85ohm+ / L10_DIFF_4/6.5/4_85ohm- — X_H1X4_BLACK — GND9_GND11
J7 — L12_DIFF_4.5/4.5/4.5_85ohm+ / L12_DIFF_4.5/4.5/4.5_85ohm- — X_H1X4_BLACK — GND11

88 ohm

J34 — L1_DIFF_4.5/6/4.5_88ohm+ / L1_DIFF_4.5/6/4.5_88ohm- — X_H1X4_BLACK — GND2
J23 — L3_DIFF_3.5/4.5/3.5_88ohm+ / L3_DIFF_3.5/4.5/3.5_88ohm- — X_H1X4_BLACK — GND2_GND4
J17 — L10_DIFF_3.5/4.5/3.5_88ohm+ / L10_DIFF_3.5/4.5/3.5_88ohm- — X_H1X4_BLACK — GND9_GND11

90 ohm

J33 — L1_DIFF_4/6/4_90ohm+ / L1_DIFF_4/6/4_90ohm- — X_H1X4_BLACK — GND2
J24 — L3_DIFF_3.5/5.5/3.5_90ohm+ / L3_DIFF_3.5/5.5/3.5_90ohm- — X_H1X4_BLACK — GND2_GND4
J8 — L5_DIFF_3.5/5.5/3.5_90ohm+ / L5_DIFF_3.5/5.5/3.5_90ohm- — X_H1X4_BLACK — GND4_GND6
J15 — L10_DIFF_3.5/5.5/3.5_90ohm+ / L10_DIFF_3.5/5.5/3.5_90ohm- — X_H1X4_BLACK — GND9_GND11
J5 — L12_DIFF_4/6/4_90ohm+ / L12_DIFF_4/6/4_90ohm- — X_H1X4_BLACK — GND11

100 ohm

J32 — L1_DIFF_3.5/7.5/3.5_100ohm+ / L1_DIFF_3.5/7.5/3.5_100ohm- — X_H1X4_BLACK — GND2
J22 — L3_DIFF_3/10/3_100ohm+ / L3_DIFF_3/10/3_100ohm- — X_H1X4_BLACK — GND2_GND4
J6 — L5_DIFF_3/10/3_100ohm+ / L5_DIFF_3/10/3_100ohm- — X_H1X4_BLACK — GND4_GND6
J19 — L10_DIFF_3/10/3_100ohm+ / L10_DIFF_3/10/3_100ohm- — X_H1X4_BLACK — GND9_GND11
J3 — L12_DIFF_3.5/7.5/3.5_100ohm+ / L12_DIFF_3.5/7.5/3.5_100ohm- — X_H1X4_BLACK — GND11

+3VRUN: EC69 X_C0.1u50X70402 → GND
+1_35VDIMM: EC40 X_C0.1u50X70402, EC63 X_C0.1u50X70402, EC62 X_C0.1u50X70402 → GND
+3VSUS: EC66 C0.1u50X70402, EC54 X_C0.1u50X70402 → GND
+5VSUS: EC70 X_C0.1u50X70402, EC65 X_C0.1u50X70402, EC67 X_C0.1u50X70402, EC61 X_C0.1u50X70402, EC60 X_C0.1u50X70402 → GND

EMI

PWR_SRC — 0B stuff
RFI
EC35 C0.1u50X70402
EC38 C0.1u50X70402
EC51 C0.1u50X70402
EC42 C0.1u50X70402
EC50 C0.1u50X70402
EC7 X_C0.1u50X70402
EC12 X_C0.1u50X70402
RFI
EC6 C1000p50X0402
EC11 C0.1u50X70402
EC4 C0.1u50X70402
EC3 C0.1u50X70402
→ GND

+VBATA: EC52 C0.1u50X70402, EC64 C0.1u50X70402 — RFI → GND
NVVDD: EC36 X_C0.1u50X70402, EC37 X_C0.1u50X70402, EC39 X_C0.1u50X70402 → GND
+1_05VRUN: EC49 X_C0.1u50X70402 → GND
+0_675VRUN: EC53 X_C0.1u50X70402 → GND

PWR_SRC: C784 C0.1u10X0402, C785 C0.1u10X0402 → GNDGND
+VBATA: C787 C0.1u10X0402 → GND
+3VRUN: C786 C0.1u10X0402 → GND
0507 add for RF

J49, J48, J45, J41, J43, J44, J42, J46 — E21-5801010-RH → GND
0507 add for RF clamp

MICRO-STAR INT'L CO.,LTD.			
Title: EMI/ Impedence			
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CPU/GPU Holes

MCPU4
H_R200D150
GND

MCPU2
H_R200D150
GND

MCPU3
H_R200D150
GND

MCPU1
H_R200D150
GND

MGPU2
H_R276D169_PB
GND

MGPU4
H_R276D169_PB
GND

MGPU1
H_R276D169_PB
GND

MGPU3
H_R276D169_PB
GND

EMI

SPRING3
X_MECHCU,2.5*5.5*0.1mm

SPRING2
X_E2M-7213211-RH
GND
E2M-7213211-CA7

GND
E2M-2142011-CA7

SPRING1
X_E23-1029060-RH
GND
E23-1029060-CA7

SPRING4
X_E2M-7213211-RH
GND
E2M-7213211-CA7

RUBBER1
E2Y-6H20712-Y40
RUBBER

RUBBER2
E2Y-6H21312-Y40
RUBBER

RUBBER3
E2Y-6H21312-Y40
RUBBER

BRACKET1
307-6H20111-C22
CPU_BRACKET

BRACKET2
307-6H20111-C22
CPU_BRACKET

BRACKET3
307-6H20211-C22
GPU_BRACKET

MYLAR1
E2P-6H22111-Y42
MYLAR

MYLAR2
E2P-6H23111-Y42
MYLAR

MYLAR3
E2P-6H22711-Y42
MYLAR

PCB1
PF0-16H3110-H73
PF0-16H3110-H73
Hannstar: PF0-16H2110-H73
TRIPOD: PF0-16H2110-T53

FM4 1
FM3 1
FM2 1
FM1 1
FM8 1
FM6 1
FM7 1
FM5 1

M1
X_H_R197D118_PT_V3
H_R197D118_PT_V3
GND

M6
X_H_R197D118_PT_V3
H_R197D118_PT_V3
GND

MYLAR4
E2P-6G13911-Y42
MYLAR

MYLAR5
E2P-6H30111-Y42
MYLAR

MYLAR6
E2P-6H30211-Y42
MYLAR

UME1
HDMI Lable
HDMI ROYALTY
Y01-RHDMI03-000

UME2
BIOS Lable
BIOS_LABEL
G51-LA01678-A09

For MP

Fan Hole

MH4
H_R197D91
X_ME_ SCREW HOLE
GND

SSD Stand off

MH2
H_R220D146_PTB
E2B-16H2020
GND

MH1
H_R220D146_PTB
E2B-16H2020
GND

MH3
NPTH157
X_NPTH157

MYLAR7
E2Y-X043611-CA7
Gaste

MICRO-STAR INT'L CO.,LTD.

Title: Screw/ME		
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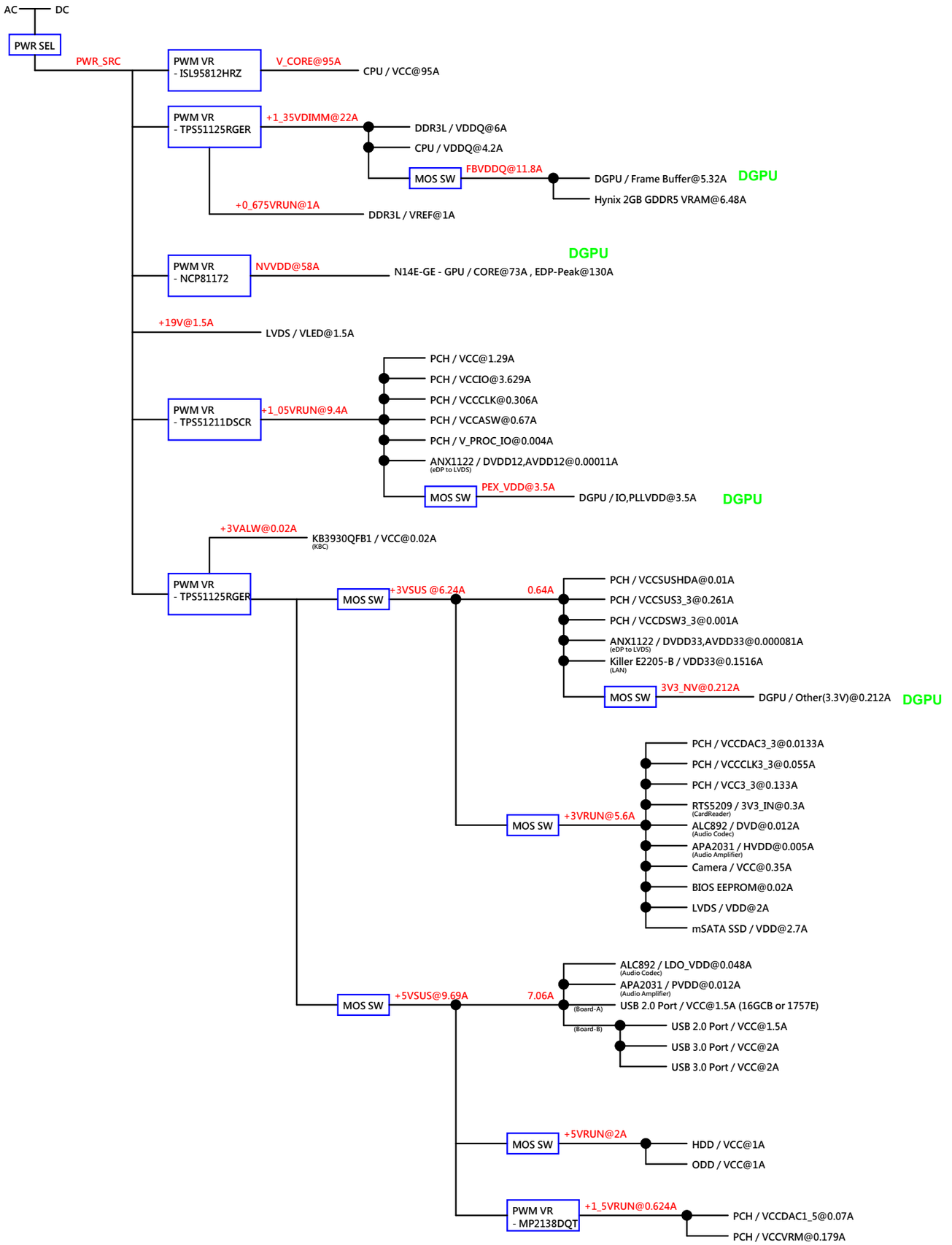
MS-16H2 Power Delivery Chart



msi	MICRO-STAR INT'L CO.,LTD.	
Title	Power Delivery Map	
Size	Document Number	Rev
	MS-16H3	1.0
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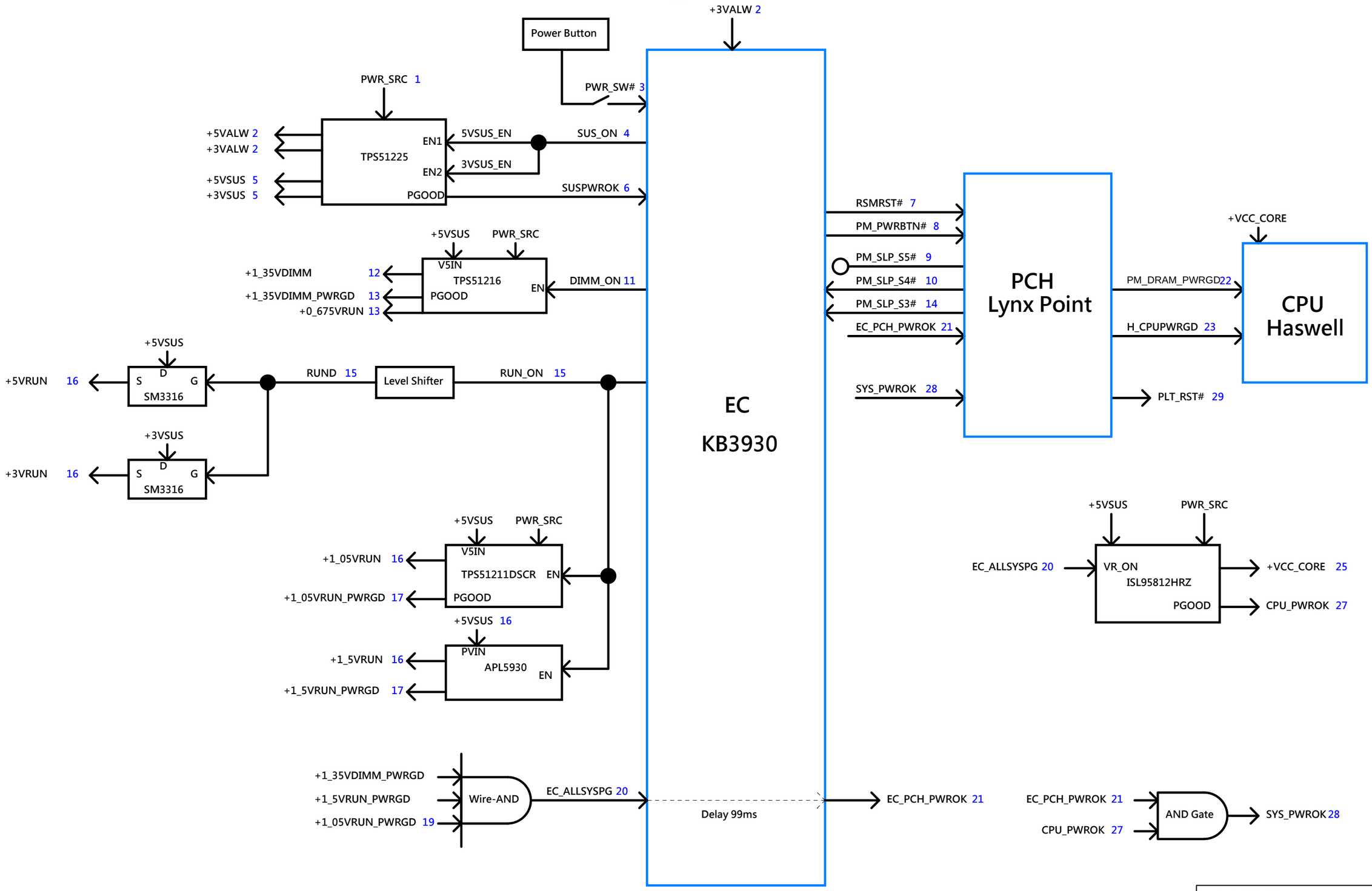
MS-16H2 Power on Block Diagram



msi MICRO-STAR INT'L CO.,LTD.			
Title: Power on Block Diagram			
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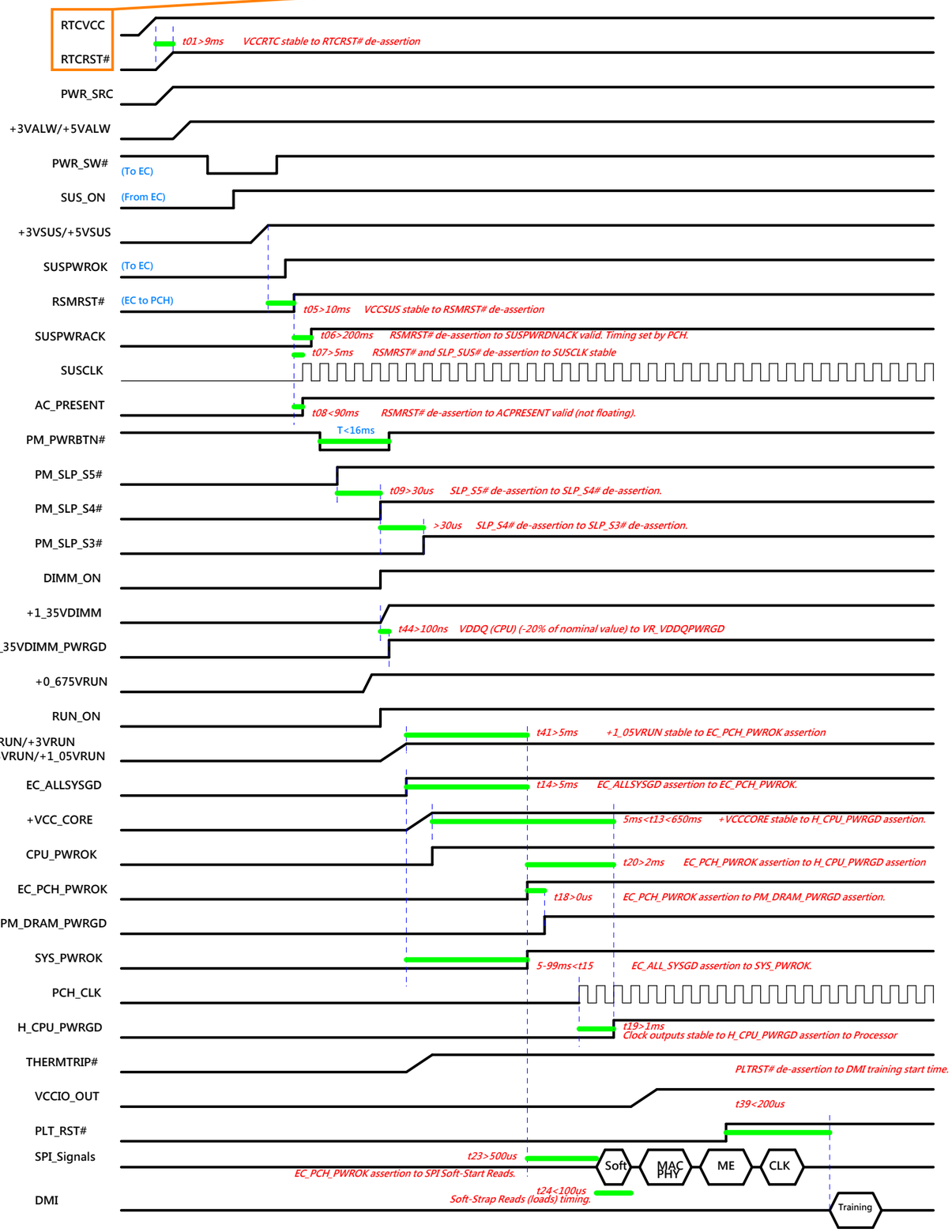
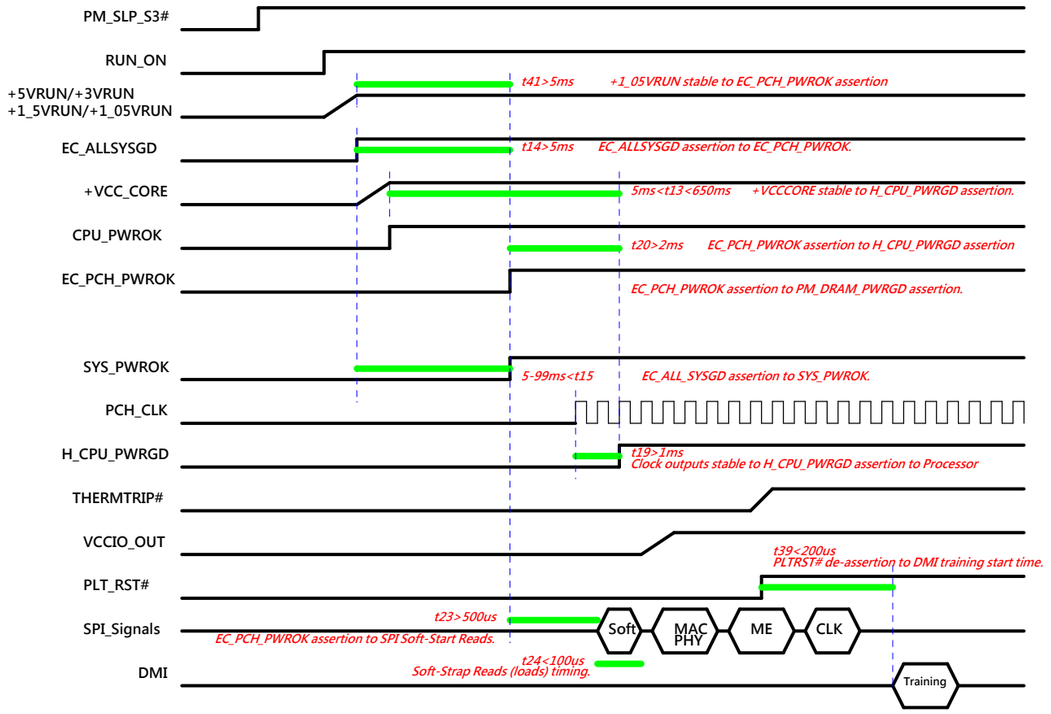
Power on Sequence

G3 -> S0



S3-> S0



MICRO-STAR INT'L CO.,LTD.

Title: Power on Sequence

Size | Document Number: MS-16H3 | Rev: 1.0

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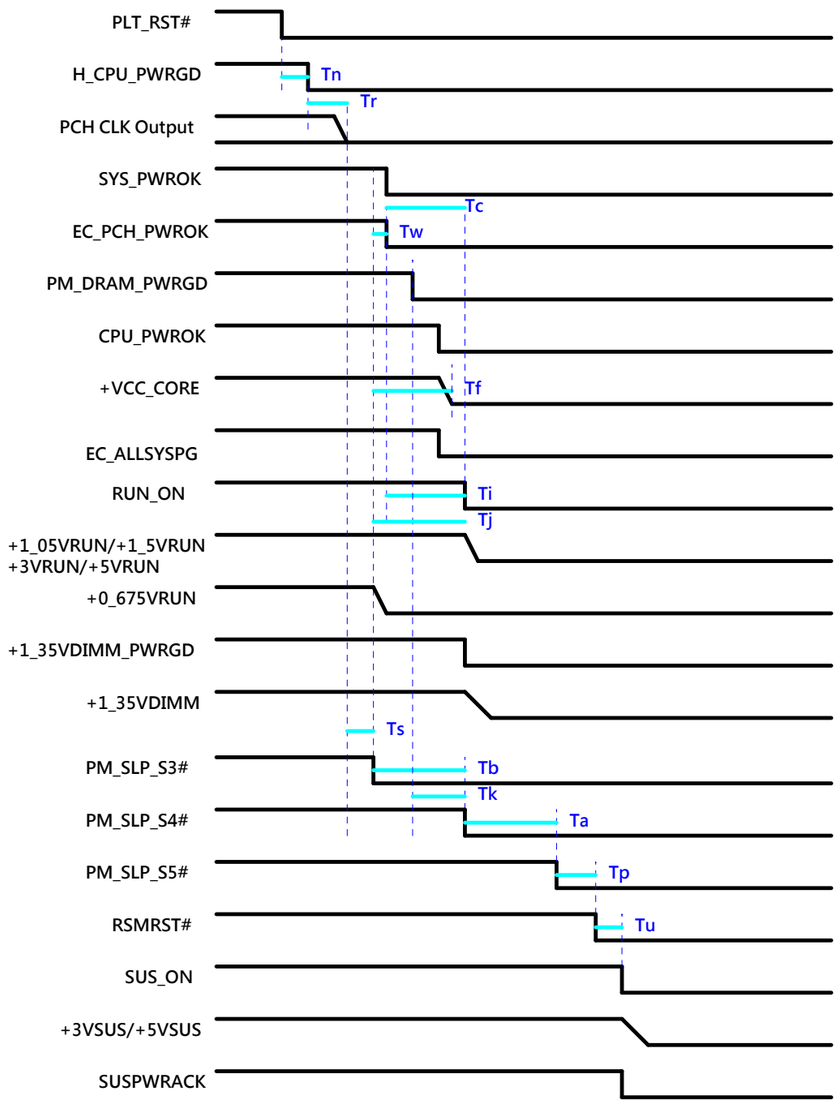
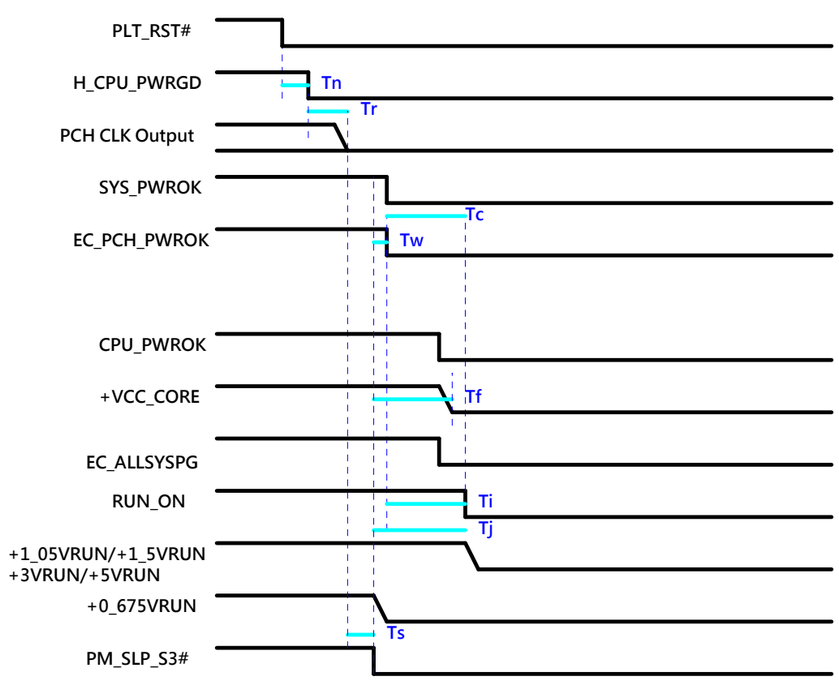
Power down Sequence

S0 -> G3



	MIN	MAX	Units	Description
Ta	30		us	SLP_S4# assertion to SLP_S5# assertion.
Tb	30		us	SLP_S3# assertion to SLP_S4# assertion.
Tc	40		ns	APWROK de-assertion to VCCASW/VCCSPI rails falling.
Tf		500	ms	SLP_S3# assertion to VCCIN(CPU) rail completely off.
Ti	40		ns	PWROK de-assertion to VCCCore (PCH) rail falling (-5% of nominal value).
Tj	5		us	SLP_S3# assertion to VCCCore (PCH) rails falling (-5% of nominal value).
Tk	-100		ns	DRAMPWROK de-assertion to SLP_S4# assertion
Tn	30		us	PLTRST# assertion to CPUPWRGOOD de-assertion.
Tp	500		us	Last SLP_Sx# or SLP_A# assertion to RSMRST# assertion
Tr	10		us	CPUPWRGOOD de-assertion to PCH clock outputs turning off.
Ts	1		us	PCH Clock outputs turning OFF to SLP_S3# assertion.
Tu	40		ns	RSMRST# assertion to VCCSUS rails falling (-5% of nominal value).
Tw	0		ms	SLP_S3# assertion to PWROK de-assertion.

S0 -> S3

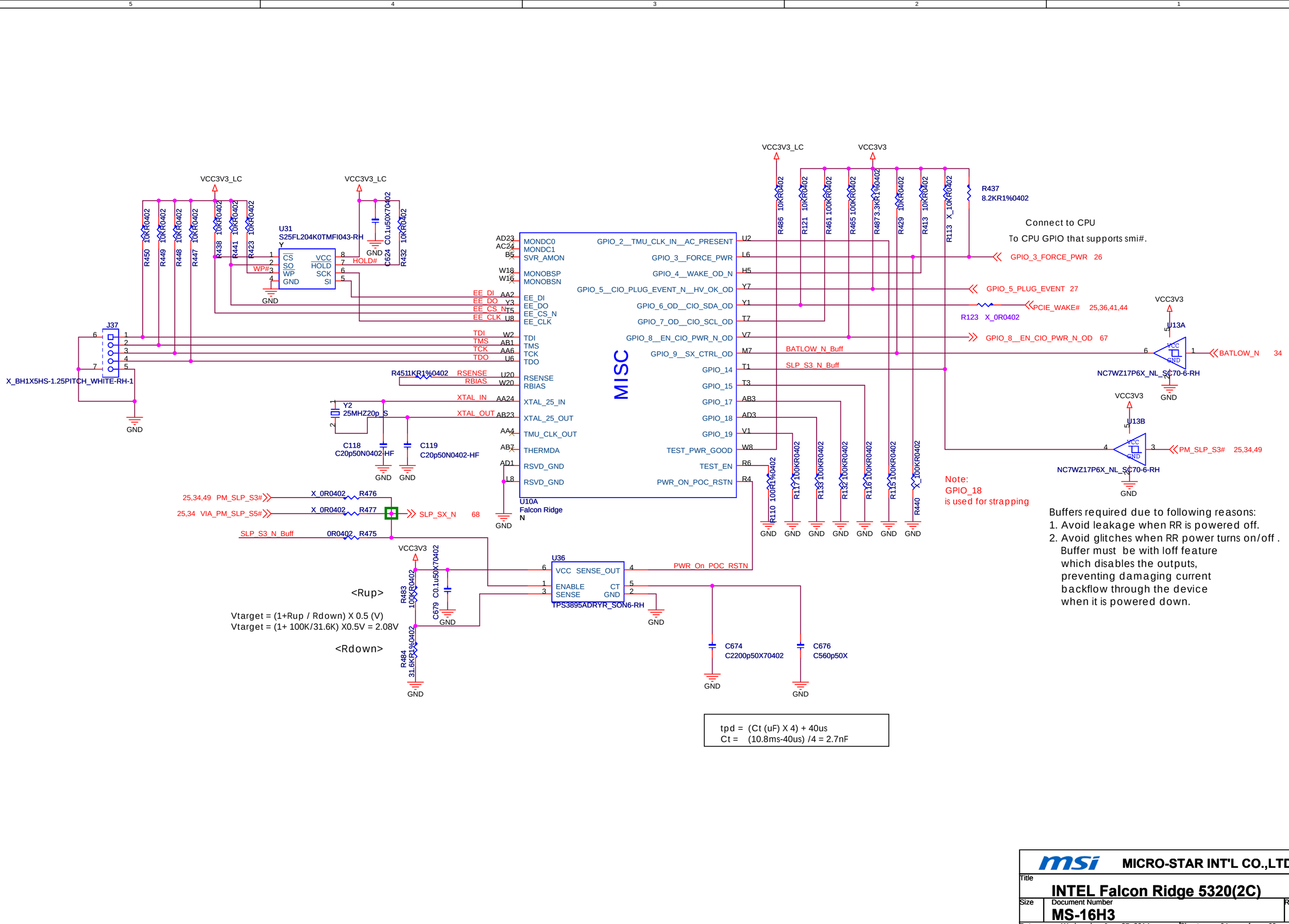


MICRO-STAR INT'L CO.,LTD.

Title: Power down Sequence

Size | Document Number: MS-16H3 | Rev: 1.0

Date: Wednesday, June 25, 2014 | Sheet 63 of 69



MICRO-STAR INT'L CO.,LTD.		
Title: INTEL Falcon Ridge 5320(2C)		
Size	Document Number: MS-16H3	Rev: 1.0
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Route Thunderbolt and PA traces
as 85 Ohm control impedance.
Match inside lane 2 mil
Match between lanes N/A
0.8"<Thunderbolt lenght <2 "

Route DPSINKS traces
as 90 Ohm control impedance.
Match inside lane 5 mil
Match between lanes 10 mil
Max lenght 7.2"

VCC3V3

R107 10KR0402

CIO

DPSRC Port A
PA_DPSRC_3_P
PA_DPSRC_3_N
PA_DPSRC_1_P
PA_DPSRC_1_N
PA_AUX_P
PA_AUX_N
PA_DPSRC_HPD

PORT0
PA_CIO0_TX_P__DPSRC_0_P
PA_CIO0_TX_N__DPSRC_0_N
PA_CIO0_RX_P
PA_CIO0_RX_N
PA_CONFIG1__CIO_0_LSEO
PA_CONFIG2__CIO_0_LSOE

PORT1
PA_CIO1_TX_P__DPSRC_2_P
PA_CIO1_TX_N__DPSRC_2_N
PA_CIO1_RX_P
PA_CIO1_RX_N
PA_LSTX__CIO_1_LSEO
PA_LSRX__CIO_1_LSOE

GPIO_0__PA_HV_EN__BYP0
GPIO_10__PA_CIO_SEL__BYP1
GPIO_12__PA_DP_PWRDN__BYP2

DPSRC Port B
PB_DPSRC_3_P
PB_DPSRC_3_N
PB_DPSRC_1_P
PB_DPSRC_1_N
PB_AUX_P
PB_AUX_N
PB_DPSRC_HPD

PORT2
PB_CIO2_TX_P__DPSRC_0_P
PB_CIO2_TX_N__DPSRC_0_N
PB_CIO2_RX_P
PB_CIO2_RX_N
PB_CONFIG1__CIO_2_LSEO
PB_CONFIG2__CIO_2_LSOE

PORT3
PB_CIO3_TX_P__DPSRC_2_P
PB_CIO3_TX_N__DPSRC_2_N
PB_CIO3_RX_P
PB_CIO3_RX_N
PB_LSTX__CIO_3_LSEO
PB_LSRX__CIO_3_LSOE

GPIO_1__PB_HV_EN__BYP0
GPIO_11__PB_CIO_SEL__BYP1
GPIO_13__PB_DP_PWRDN__BYP2

U10E
Falcon Ridge
N

DP

Sink Port 0
DPSNK0_3_P E14
DPSNK0_3_N D13
DPSNK0_2_P E16
DPSNK0_2_N D15
DPSNK0_1_P E18
DPSNK0_1_N D17
DPSNK0_0_P E20
DPSNK0_0_N D19
DPSNK0_AUX_P G4
DPSNK0_AUX_N G2
DPSNK0_HPD AB5

Sink Port 1
DPSNK1_3_P E6
DPSNK1_3_N D5
DPSNK1_2_P E8
DPSNK1_2_N D7
DPSNK1_1_P E10
DPSNK1_1_N D9
DPSNK1_0_P E12
DPSNK1_0_N D11
DPSNK1_AUX_P H3
DPSNK1_AUX_N H1
DPSNK1_HPD U4

Source Port
DPSRC_3_P A14
DPSRC_3_N B15
DPSRC_2_P A12
DPSRC_2_N B13
DPSRC_1_P A10
DPSRC_1_N B11
DPSRC_0_P A8
DPSRC_0_N B9
DPSRC_AUX_P J4
DPSRC_AUX_N J2
DPSRC_HPD_OD AC2

C601 C0.1u50X70402 DPC1_LANE3_DP_LC3 38
C602 C0.1u50X70402 DPC1_LANE3_DN_LC3 38
C599 C0.1u50X70402 DPC1_LANE2_DP_LC2 38
C600 C0.1u50X70402 DPC1_LANE2_DN_LC2 38
C592 C0.1u50X70402 DPC1_LANE1_DP_LC1 38
C593 C0.1u50X70402 DPC1_LANE1_DN_LC1 38
C596 C0.1u50X70402 DPC1_LANE0_DP_LC0 38
C597 C0.1u50X70402 DPC1_LANE0_DN_LC0 38
C109 C0.1u50X70402 DPC1_AUXP 26,38
C111 C0.1u50X70402 DPC1_AUXN 26,38

DDPB_HPD 26,38

3/2 add

R488 10KR0402
R120 10KR0402
R131 10KR0402

GND

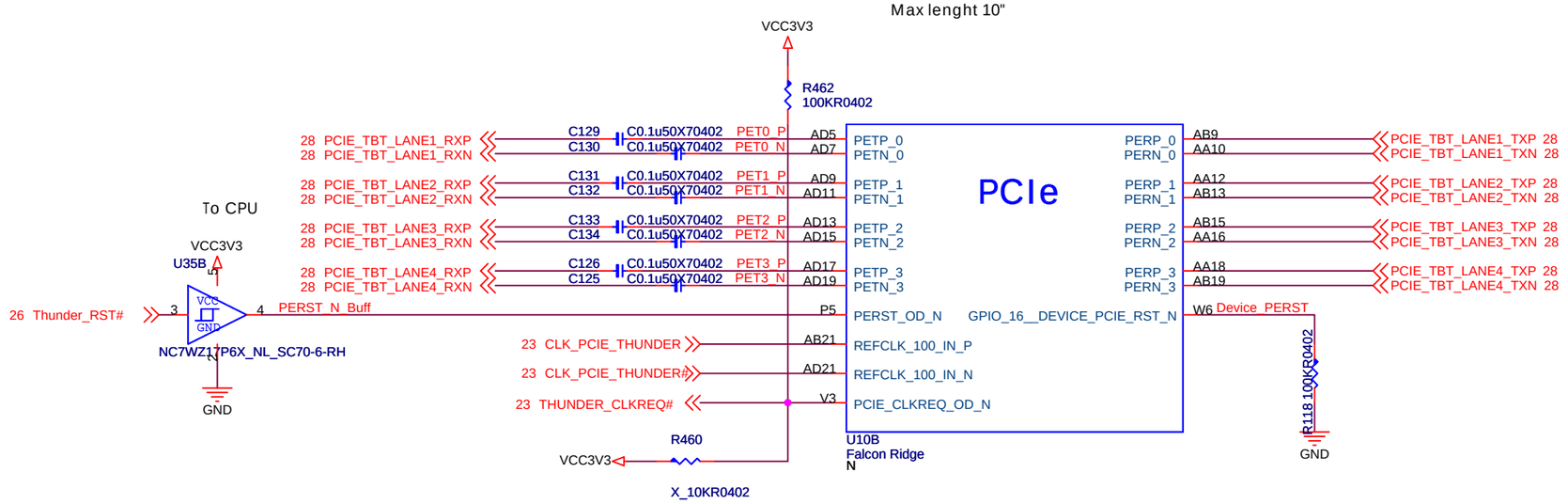
68 DP_TBTPA_ML3_P C105 C0.22u16X0402-HF DP_TBTPA_ML3_C_P A18
68 DP_TBTPA_ML3_N C106 C0.22u16X0402-HF DP_TBTPA_ML3_C_N B19
68 DP_TBTPA_ML1_P C104 C0.22u16X0402-HF DP_TBTPA_ML1_C_P A16
68 DP_TBTPA_ML1_N C103 C0.22u16X0402-HF DP_TBTPA_ML1_C_N B17
68 DP_TBTPA_AUX_P C112 C0.1u50X70402 DP_TBTPA_AUX_C_P L4
68 DP_TBTPA_AUX_N C116 C0.1u50X70402 DP_TBTPA_AUX_C_N L2
68 DP_TBTPA_HPD M3
68 TBT_A_R2D_0_P C101 C0.22u16X0402-HF TBT_A_R2D_C_0_P G24
68 TBT_A_R2D_0_N C102 C0.22u16X0402-HF TBT_A_R2D_C_0_N E24
68 TBT_A_D2R_0_P C513 C0.47u10X0402 TBT_A_D2R_C_0_P G22
68 TBT_A_D2R_0_N C523 C0.47u10X0402 TBT_A_D2R_C_0_N E22
38,68 TBT_A_Config1_BUF P1
68 TBT_A_Config2_BUF K5
68 TBT_A_R2D_1_P C107 C0.22u16X0402-HF TBT_A_R2D_C_1_P L24
68 TBT_A_R2D_1_N C108 C0.22u16X0402-HF TBT_A_R2D_C_1_N J24
68 TBT_A_D2R_1_P C567 C0.47u10X0402 TBT_A_D2R_C_1_P L22
68 TBT_A_D2R_1_N C566 C0.47u10X0402 TBT_A_D2R_C_1_N J22
68 TBT_A_LSTX N8
68 TBT_A_LSRX J6
46 PA_HV_EN R8
68 PA_CIO_SEL N2
68 PA_DP_PWRDN P3

R455 10KR1%0402
R108 100KR0402

R452100KR0402 PB_DPSRC_HPD N6
R422 100KR0402 TBT_B_Config1 D3
R105 100KR0402 TBT_B_Config2 M1
R445 100KR0402 PB_LSTX M5
R446 100KR0402 PB_LSRX P7
R97 100KR0402 PB_HV_EN F1
R111 100KR0402 PB_CIO_SEL R2
R425 100KR0402 PB_DP_PWRDN F3

DP_SINK0_3_P
DP_SINK0_3_N
DP_SINK0_2_P
DP_SINK0_2_N
DP_SINK0_1_P
DP_SINK0_1_N
DP_SINK0_0_P
DP_SINK0_0_N
DP_SINK0_AUX_P
DP_SINK0_AUX_N
DP_SNK1_HPD
DP_SCR_HPD

Route PCIe traces
as 85 Ohm control impedance
Match inside lanes 5mil
Match between lanes N/A
Max lenght 10"



X_10KR0402

Buffer required due to following reasons:
1. Avoid leakage when RR is powered off.
2. Avoid glitches when RR power turns on/off .
   Buffer must be with Ioff feature
   which disables the outputs,
   preventing damaging current
   backflow through the device
   when it is powered down.

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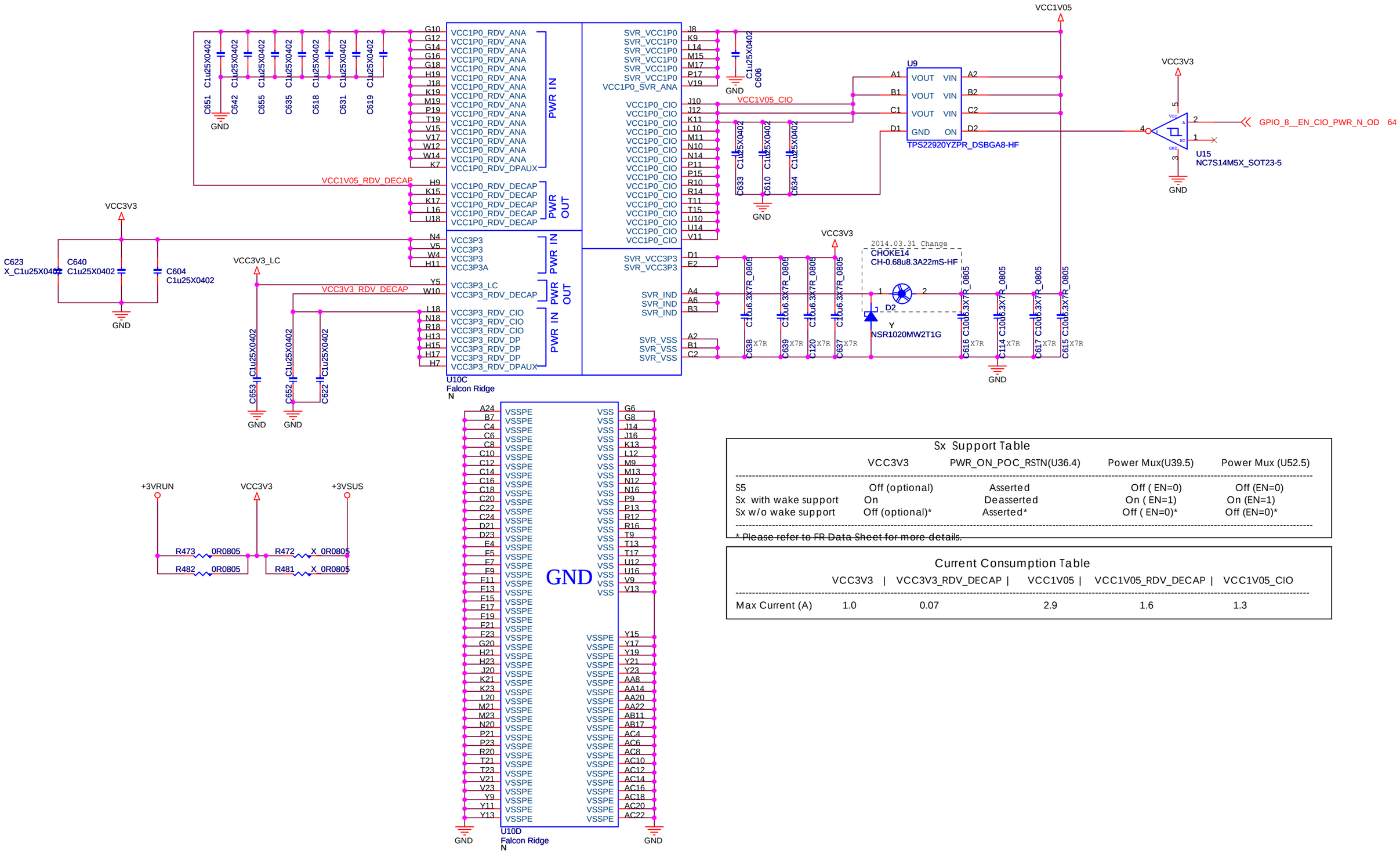

Sx Support Table

	VCC3V3	PWR_ON_POC_RSTN(U36.4)	Power Mux(U39.5)	Power Mux (U52.5)
S5	Off (optional)	Asserted	Off (EN=0)	Off (EN=0)
Sx with wake support	On	Deasserted	On (EN=1)	On (EN=1)
Sx w/o wake support	Off (optional)*	Asserted*	Off (EN=0)*	Off (EN=0)*

* Please refer to FR Data Sheet for more details.

Current Consumption Table

	VCC3V3	VCC3V3_RDV_DECAP	VCC1V05	VCC1V05_RDV_DECAP	VCC1V05_CIO
Max Current (A)	1.0	0.07	2.9	1.6	1.3

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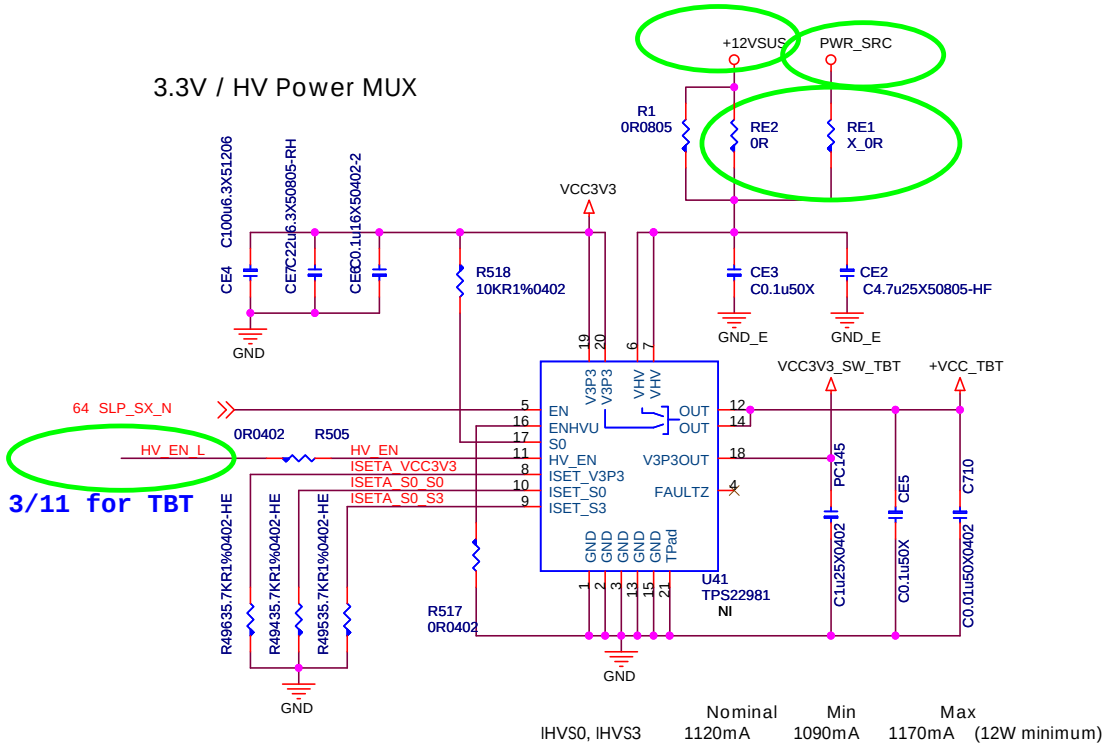
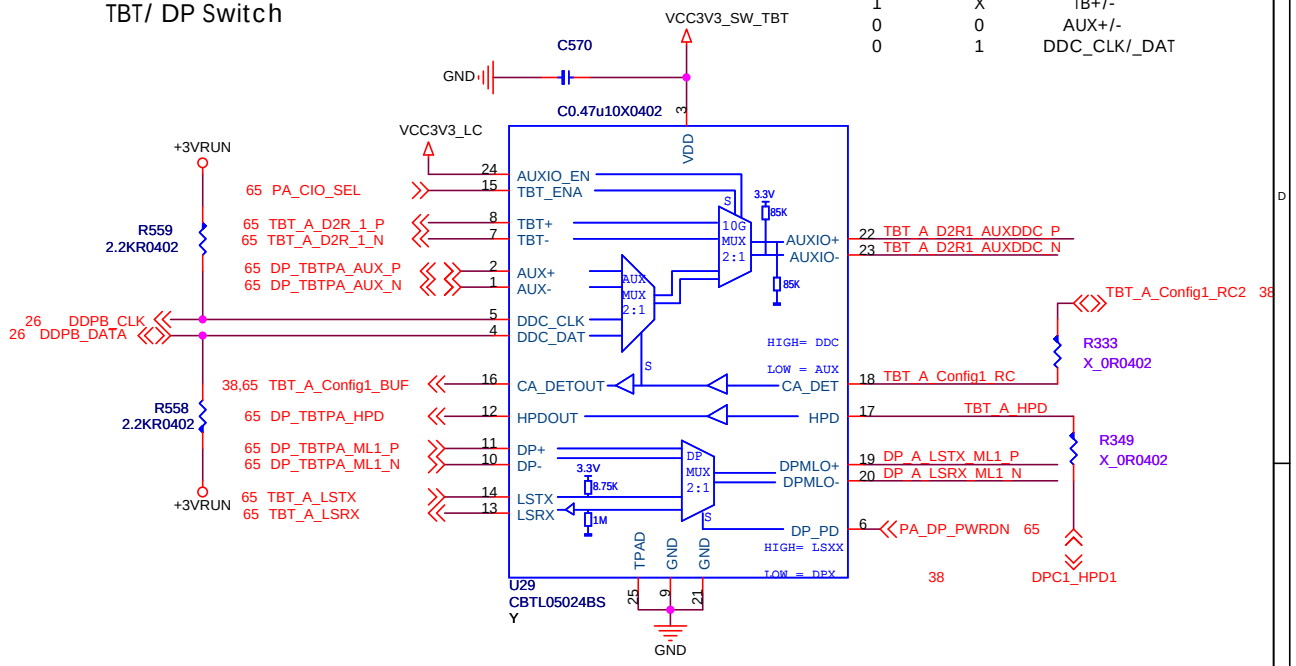
3.3V / HV Power MUX



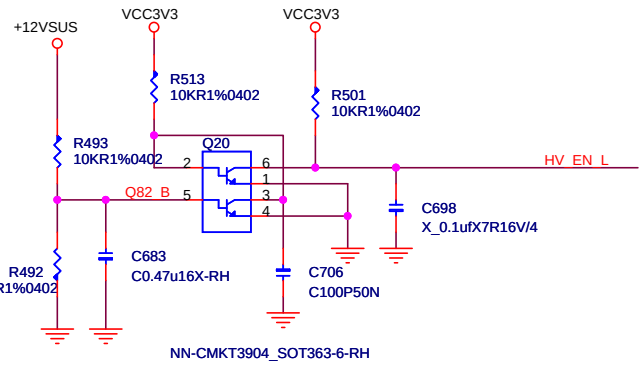
	Nominal	Min	Max	
IHVS0, IHVS3	1120mA	1090mA	1170mA	(12W minimum)

TBT/ DP Switch

TBT_ENA	CA_DET	AUXIO+/-
1	X	TB+/-
0	0	AUX+/-
0	1	DDC_CLK/_DAT

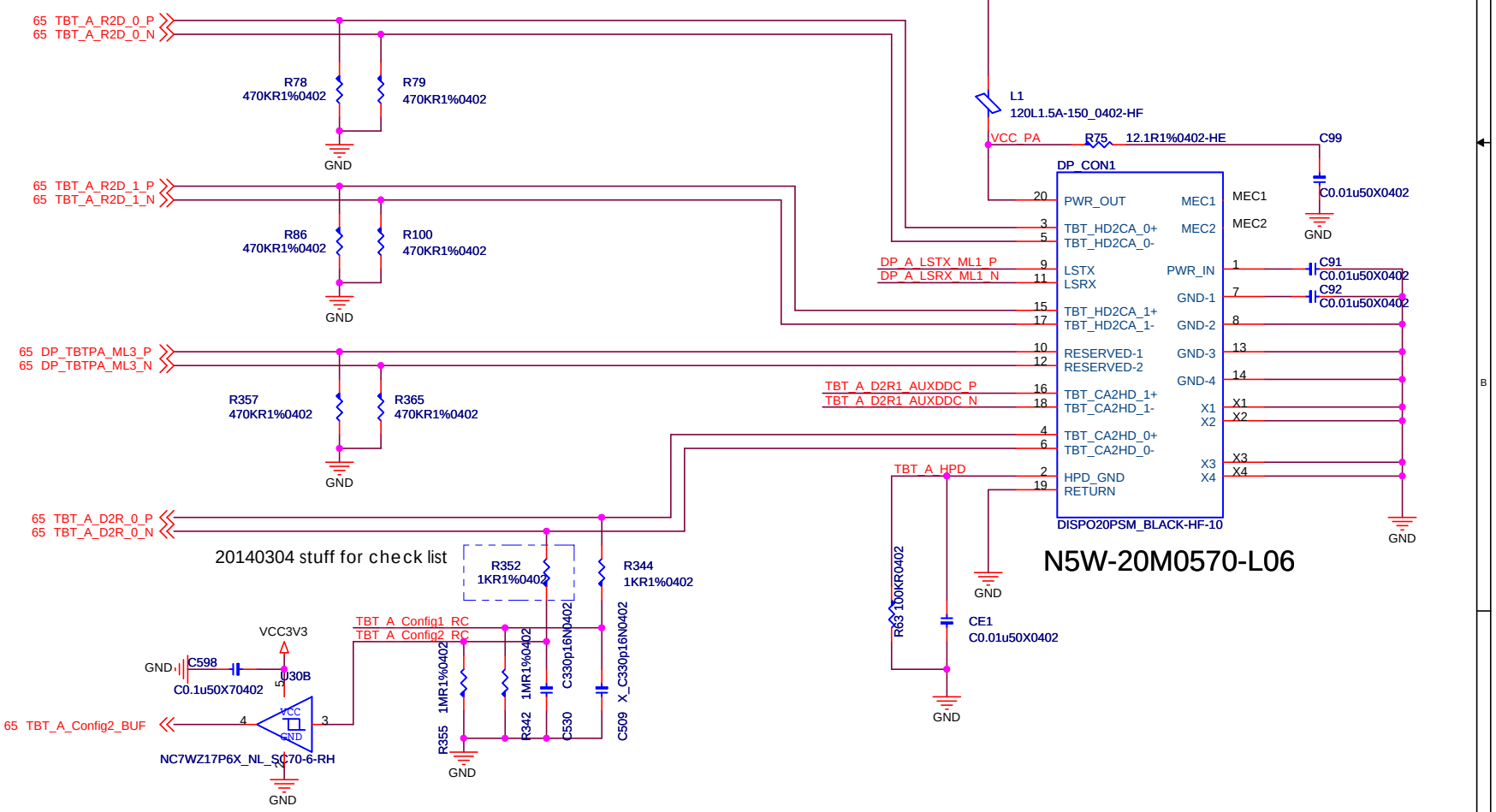


3/11 for TBT



Power mux will be
on when VCC12V0 >=4.5V and
off when VCC12V0 <=3.4V
Vbe=770mV@Ic=10mA -->
4.5X2.05K/(10K+2.05K) = 0.766V

Note:
If generating the 12v from a supply
different than 3.3v - resistors values of
R52 and R53 should be different
Example: If VCC12V0 is boosted from 5V,
the R52 is 10K ohm and R53 is 1K ohm



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History

0A: Hardware part

01.RB4 , RB6 RB5 , RB7 , RB9 , RB10 470R change to 680R
02. Modify WLAN CLKREQ SCH , add R101
03. R440 unstuff , R437 stuff
04. Add TBT DDC Pull-high 2.2K , R558 and R559
05. RA2 and RA6 unstuff
06. Add U46 sch for ASM1042 1.05VRUN
07. Modify HDMI SCH , D3 change to D01-BAT5429-D07 ,add C782 and C783
08. CPU change part number for each item.
09. Samsung VRAM EOL , change to Hynix
10. Add C785 and C784 for PWR_SCR
11. Add C786 for 3VRUN
12. Add C787 for VBATA
13. R396 change connect to 3VSUS
14. rename 3V3_NV to +3V3_NV
15. Swap RTC pin
16. change EL3 , ELA5 , ELA2 and LI6 PN to L12-9008100-I05
17. R30 change to 10k and C67 , C68 unstuff for EC_ALLSYSPG sequency
18. Revese Q6, Q15, Q19 DS pin for power on sequence
19. C594 unstuff
20. R40 change to 0ohm and C77 unstuff
21. Add eight RF clamp
22. remove F1
23. R387 change to 47K
24. Add PQ62 sch for DGPU power control
25. EC59 stuff
26. ASM 1042 SCH unstuff

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