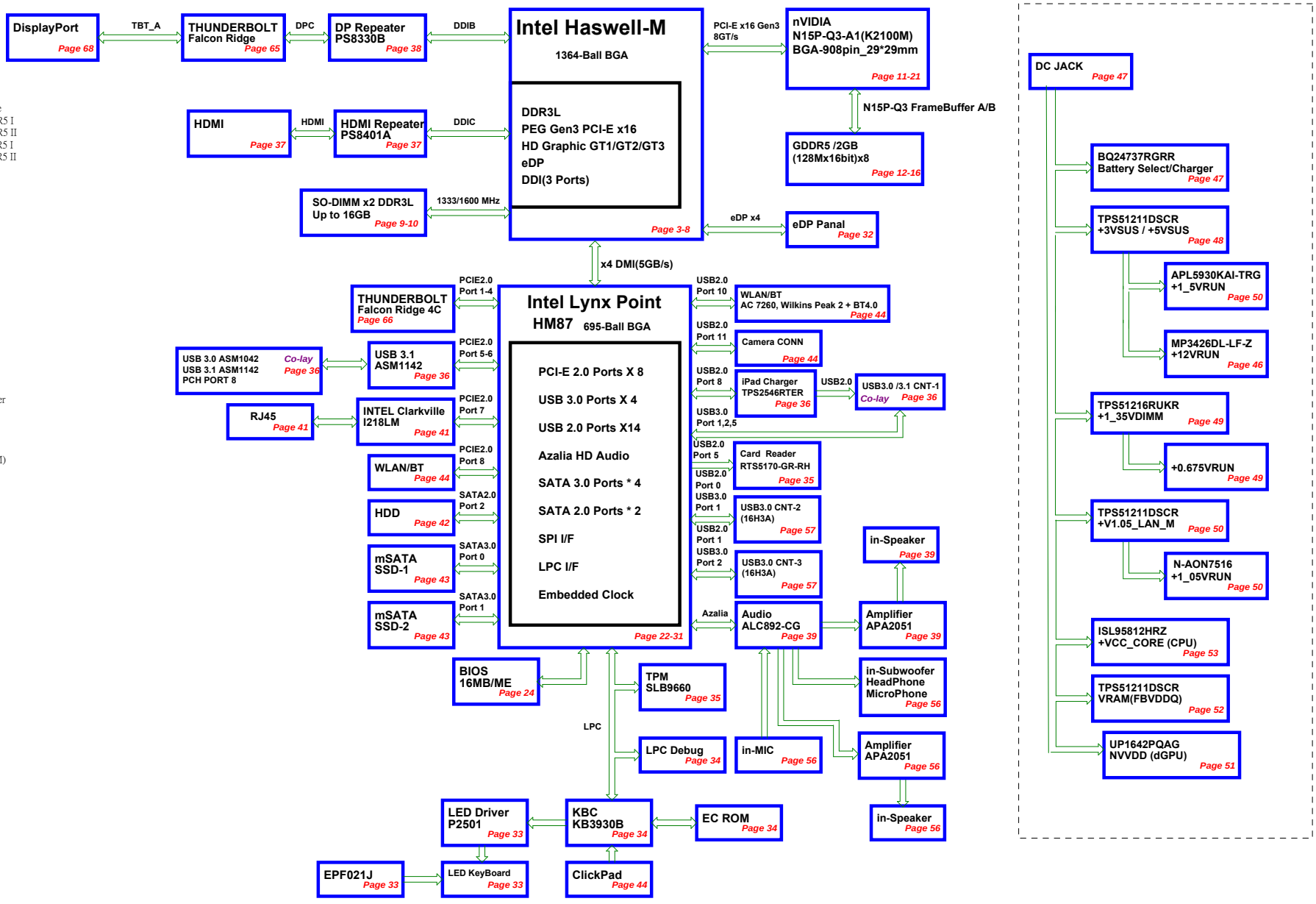
MS-16H3 Ver:0A

Tuesday, May 20, 2014

Shark Bay Mobile



msi	MICRO-STAR INT'L CO.,LTD.		
Title	Block Diagram		
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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

Voltage	Description	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
+5VALW	5.0V always on power rail	PWR_SRC
+3VALW	3.3V always on power rail	PWR_SRC
+5VSUS	5.0V power rail	SUS_ON
+3VSUS	3.3V power rail	SUS_ON
+1_35VDIMM	1.35V DDR3L power rail (off in S4-S5)	DIMM_ON
+0_675VRUN	0.675V DDR3L Termination voltage (off in S3-S5)	PM_SLP_S3#
+5VRUN	5.0V switched power rail (off in S3-S5)	RUN_ON
+3VRUN	3.3V switched power rail (off in S3-S5 / M0)	RUN_ON
+1_5VRUN	1.5V switched power rail (off in S3-S5)	RUN_ON
+VCC_CORE	1.8V Core Voltage for Processor	EC_ALLSYSPG
+1_05VRUN	1.05V rail for Processor	RUN_ON
NVVDD	V Core Voltage for nVIDIA dGPU	NVVDD_EN
+3V3_NV	3.3V PEX power rail (off in Optimus OFF)	DGPU_PWR_EN#
FBVDDQ	1.35V FB / GDDR5 power rail (off in Optimus OFF)	FBVDDQ_ON
PEX_VDD	1.05V PLL power rail (off in Optimus OFF)	NVVDD_EN

POWER STATES

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALW	+*VSUS	+*VRUN	Clocks
S0(Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3(Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Note : WHEN AC MODE , System turn on and +V*SUS always keep high

Net Naming Conventions

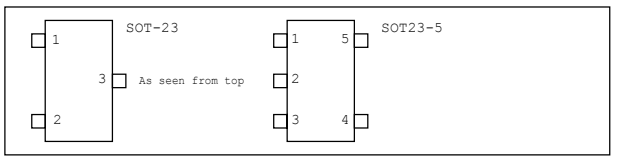
Suffix

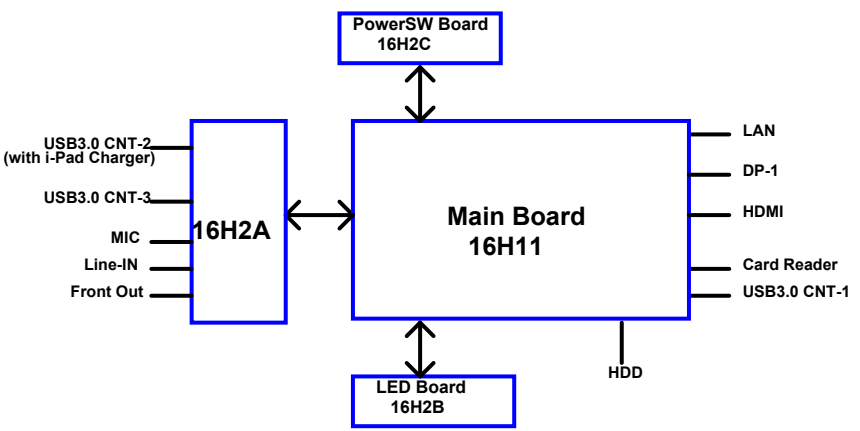
```
#  =  Active Low Signal
```

Prefix

```
H  =  Host
M  =  DDR Memory
TP =  Test Point (does not connect anywhere else)
FB = DGPU VRAM
VIAxxx =  Like Test Point, but using VIA.
```

PCB Footprints





MICRO-STAR INT'L CO.,LTD.

Title: Platform

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Haswell (DMI,PEG,FDI)

PEG_RCOMP
Width:12 mils
Spacing:15 mils
Length:400 mils

U1A HASWELL_BGA_E

DMI_TXN0 25 AB2 DMI_RXN0
DMI_TXN1 25 AB3 DMI_RXN1
DMI_TXN2 25 AC3 DMI_RXN2
DMI_TXN3 25 AC1 DMI_RXN3

DMI_TXP0 25 AB1 DMI_RXP0
DMI_TXP1 25 AB4 DMI_RXP1
DMI_TXP2 25 AC4 DMI_RXP2
DMI_TXP3 25 AC2 DMI_RXP3

DMI_RXN0 25 AF2 DMI_TXN0
DMI_RXN1 25 AF4 DMI_TXN1
DMI_RXN2 25 AG4 DMI_TXN2
DMI_RXN3 25 AG2 DMI_TXN3

DMI_RXP0 25 AF1 DMI_TXP0
DMI_RXP1 25 AE3 DMI_TXP1
DMI_RXP2 25 AG3 DMI_TXP2
DMI_RXP3 25 AG1 DMI_TXP3

DMI

FDI_CSYNC 25 F11 FDI_CSYNC
FDI_INT 25 F12 DISP_INT

FDI

PEG

AH6 PEG_COMP R252 24.9R1%0402 +VCCIOA_OUT

PEG_RCOMP			
PEG_RXN0	E10	PEG_RXN0	11
PEG_RXN1	C10	PEG_RXN1	11
PEG_RXN2	B10	PEG_RXN2	11
PEG_RXN3	F9	PEG_RXN3	11
PEG_RXN4	D9	PEG_RXN4	11
PEG_RXN5	B9	PEG_RXN5	11
PEG_RXN6	L5	PEG_RXN6	11
PEG_RXN7	L2	PEG_RXN7	11
PEG_RXN8	M4	PEG_RXN8	11
PEG_RXN9	L4	PEG_RXN9	11
PEG_RXN10	M2	PEG_RXN10	11
PEG_RXN11	V5	PEG_RXN11	11
PEG_RXN12	V4	PEG_RXN12	11
PEG_RXN13	V1	PEG_RXN13	11
PEG_RXN14	Y3	PEG_RXN14	11
PEG_RXN15	Y2	PEG_RXN15	11
PEG_RXP0	F10	PEG_RXP0	11
PEG_RXP1	D10	PEG_RXP1	11
PEG_RXP2	A10	PEG_RXP2	11
PEG_RXP3	F9	PEG_RXP3	11
PEG_RXP4	C9	PEG_RXP4	11
PEG_RXP5	A9	PEG_RXP5	11
PEG_RXP6	M5	PEG_RXP6	11
PEG_RXP7	L1	PEG_RXP7	11
PEG_RXP8	M3	PEG_RXP8	11
PEG_RXP9	L3	PEG_RXP9	11
PEG_RXP10	M1	PEG_RXP10	11
PEG_RXP11	Y5	PEG_RXP11	11
PEG_RXP12	V3	PEG_RXP12	11
PEG_RXP13	V2	PEG_RXP13	11
PEG_RXP14	Y4	PEG_RXP14	11
PEG_RXP15	Y1	PEG_RXP15	11
PEG_TXN0	B6	PEG_TXN0	11
PEG_TXN1	C5	PEG_TXN1	11
PEG_TXN2	E6	PEG_TXN2	11
PEG_TXN3	D4	PEG_TXN3	11
PEG_TXN4	G4	PEG_TXN4	11
PEG_TXN5	E3	PEG_TXN5	11
PEG_TXN6	J5	PEG_TXN6	11
PEG_TXN7	G3	PEG_TXN7	11
PEG_TXN8	J3	PEG_TXN8	11
PEG_TXN9	J2	PEG_TXN9	11
PEG_TXN10	T6	PEG_TXN10	11
PEG_TXN11	R6	PEG_TXN11	11
PEG_TXN12	R2	PEG_TXN12	11
PEG_TXN13	R4	PEG_TXN13	11
PEG_TXN14	T4	PEG_TXN14	11
PEG_TXN15	T1	PEG_TXN15	11
PEG_TXP0	C6	PEG_TXP0	11
PEG_TXP1	B5	PEG_TXP1	11
PEG_TXP2	D6	PEG_TXP2	11
PEG_TXP3	E4	PEG_TXP3	11
PEG_TXP4	G5	PEG_TXP4	11
PEG_TXP5	E2	PEG_TXP5	11
PEG_TXP6	J6	PEG_TXP6	11
PEG_TXP7	G2	PEG_TXP7	11
PEG_TXP8	J4	PEG_TXP8	11
PEG_TXP9	J1	PEG_TXP9	11
PEG_TXP10	T5	PEG_TXP10	11
PEG_TXP11	R5	PEG_TXP11	11
PEG_TXP12	R1	PEG_TXP12	11
PEG_TXP13	R3	PEG_TXP13	11
PEG_TXP14	T3	PEG_TXP14	11
PEG_TXP15	T2	PEG_TXP15	11

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Haswell (CLK,MISC,JTAG)

SM_RCOMP_0/1/2 : 15/20/25/15/20/25
SM_RCOMP_0/1/2 Length max: 500mil

U1B HASWELL_BGA_E

MISC
C51 PROC_DETECT
VIA_H_CATERR# G50 CATERR
34 H_PECI G51 PECI
H_PROCHOT# R E50 PROCHOT
27 H_THRMTRIP# D53 THERMTRIP
THERMAL

27 H_CPUPWRGD D52 PM_SYNC
F50 PWRGOOD
PM_DRAM_PWRGD_R AP48 SM_DRAMPWROK
27 PCH_PLTRST_CPU L54 PLTRSTIN
PWR

25 H_PM_SYNC

R237 10KR1%0402 GND

CLK_DPN 23 AC6 DPLL_REF_CLKN
CLK_DPP 23 AE6 DPLL_REF_CLKP
CLK_DP_SSCN 23 V6 SSC_DPLL_REF_CLKN
CLK_DP_SSCP 23 Y6 SSC_DPLL_REF_CLKP
CLK_EXP# 23 AB6 BCLKN
CLK_EXP 23 AA6 BCLKP
CLOCK

DDR3
SM_RCOMP0 BB51 SM_RCOMP0_JNC R277 100R1%0402 GND
SM_RCOMP1 BB53 SM_RCOMP1_JNC R269 75R1%0402
SM_RCOMP2 BB52 SM_RCOMP2_JNC R276 100R1%0402
SM_DRAMRST BE51 CPUDRAMRST#

JTAG
PRDY N53
PREQ N52 VIA_XDP_PREQ#
TCK N54 XDP_TCLK
TMS M51 VIA_XDP_TMS
TRST M53 XDP_TRST#
TDI N49 VIA_XDP_TDI
TDO M49 VIA_XDP_TDO
DBR F53 VIA_XDP_DBRESET#

BPM#0 R51
BPM#1 R50
BPM#2 P49
BPM#3 N50
BPM#4 R49
BPM#5 P53
BPM#6 U51
BPM#7 P51

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H_CPUPWRGD EC14 X_C15p50N0402 GND

p.11 479493_479493_SharkBay_HSW_ext_rev2.0.pdf
Processor JTAG (TDI, TDO, TMS, TRST#, TCK) signals, PREQ# and PRDY# signals signals have adequate internal bias resistances to support the removal of the external pull up and pull down on the board when debug is no longer needed.

XDP_TCLK R17 51R1%0402
XDP_TRST# R18 51R1%0402
GND

EC Sink current 2 mA

+VCCIO_OUT
R236 681R1%0402
34 EC_PROCHOT# R235 56R0402 H_PROCHOT# R
53 IMVP_PROCHOT# 1 2 JNC7 X_0402

47P close PWM

+1_35VDIMM
Not Support Deep S3
R22 1.8K1%0402
1.35V
25 PM_DRAM_PWRGD R20 0R1%0402 PM_DRAM_PWRGD_R
R21 3.3KR1%0402
GND

1K on CRB , 0R on DG

R,C Close SO-DIMM
9,10 DDR3_DRAMRST# R29 0R1%0402 CPUDRAMRST#
EC1 X_C0.1u50X70402
GND

MICRO-STAR INT'L CO.,LTD.

Title: CPU-1 (Host Bus)

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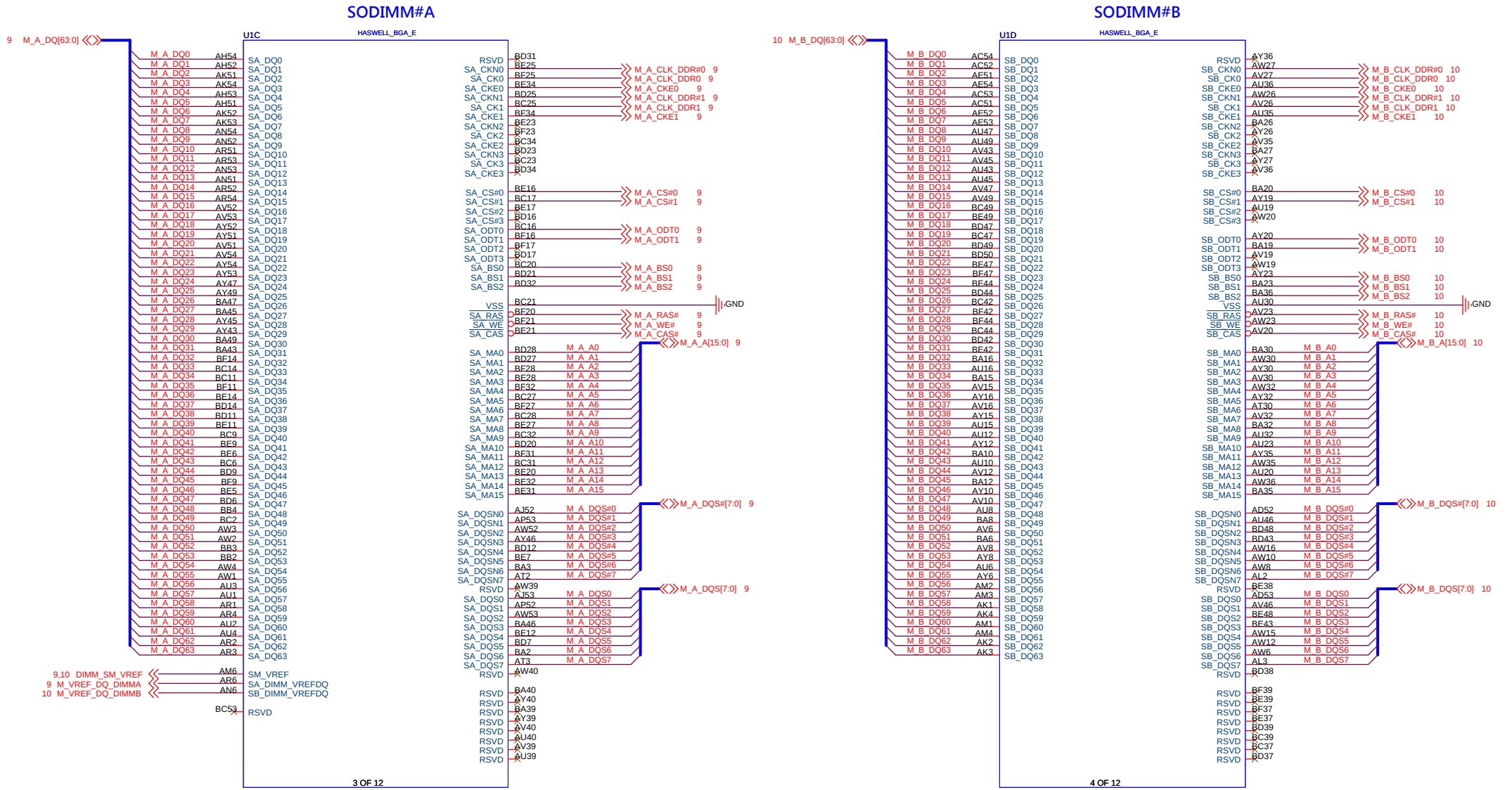
Haswell (DDR3L)



MICRO-STAR INT'L CO.,LTD.		
Title: CPU-2 (DDR3L)		
Size	Document Number: MS-16H3	Rev: 0B
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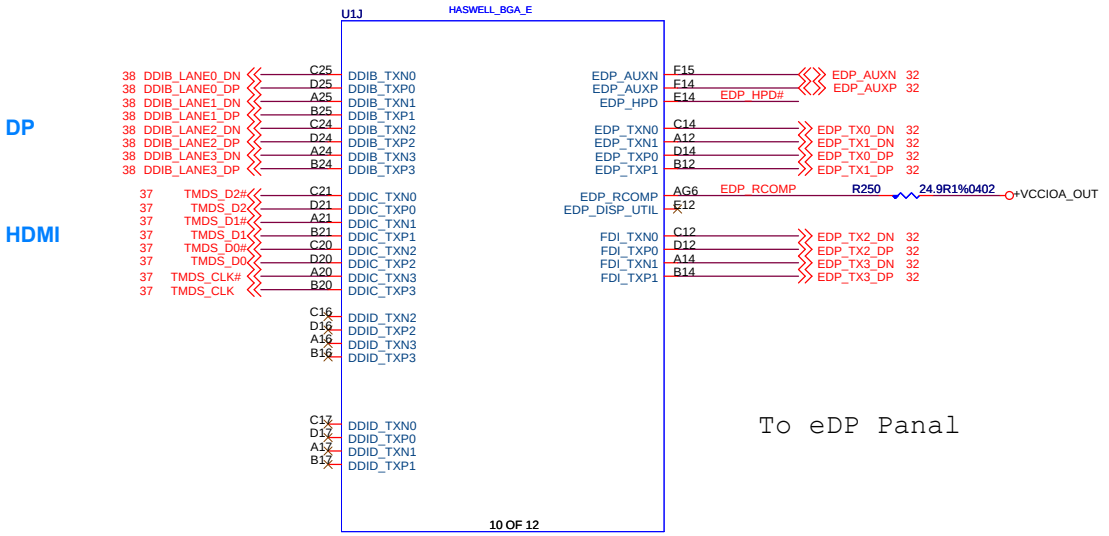
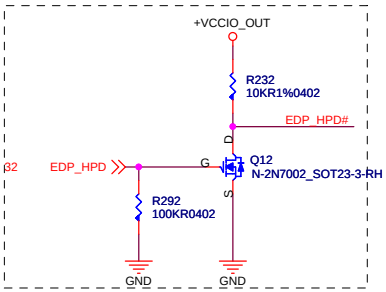
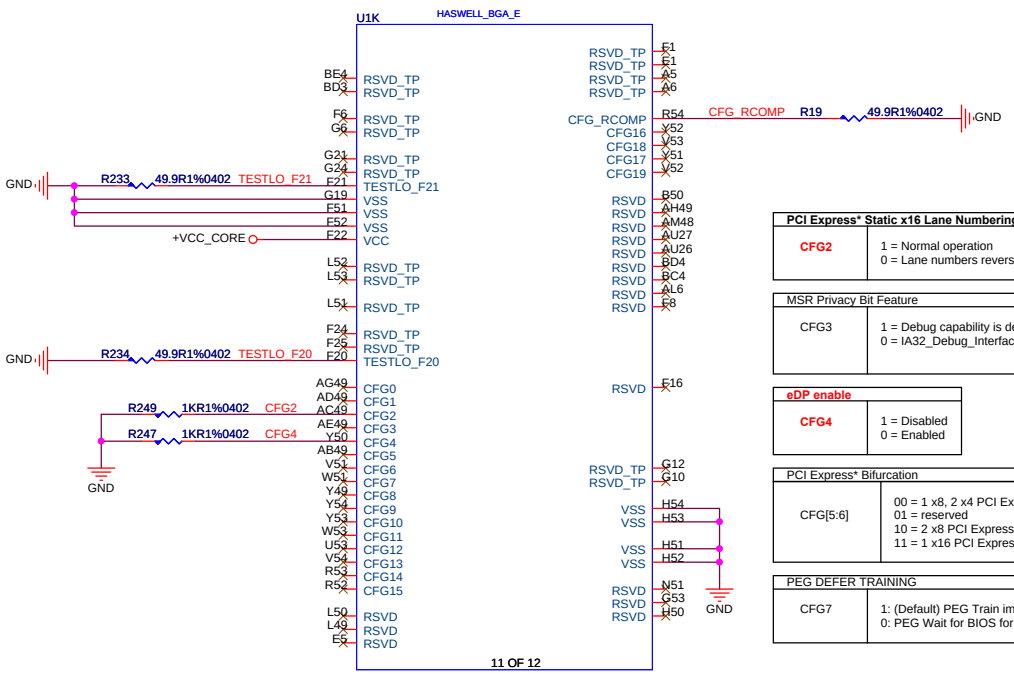
Display/Reserved







PCI Express* Static x16 Lane Numbering Reversal	
CFG2	1 = Normal operation 0 = Lane numbers reversed.

MSR Privacy Bit Feature	
CFG3	1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden

eDP enable	
CFG4	1 = Disabled 0 = Enabled

PCI Express* Bifurcation	
CFG[5:6]	00 = 1 x8, 2 x4 PCI Express 01 = reserved 10 = 2 x8 PCI Express 11 = 1 x16 PCI Express

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

MICRO-STAR INT'L CO.,LTD.

Title: CPU-3 (Display/Reserved)

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Haswell (POWER)

22uF x 20 /0603
C11-2267313-T04

+VCC_CORE
C17 C22u6.3X0603
C22 C22u6.3X0603
C299 C22u6.3X0603
C253 C22u6.3X0603
C16 C22u6.3X0603
C254 C22u6.3X0603
C265 C22u6.3X0603
C21 C22u6.3X0603
C15 C22u6.3X0603
C20 C22u6.3X0603
C298 C22u6.3X0603
C266 C22u6.3X0603
C256 C22u6.3X0603
C269 C22u6.3X0603
C270 C22u6.3X0603
C252 C22u6.3X0603
C264 C22u6.3X0603
C263 C22u6.3X0603
C262 C22u6.3X0603
C255 C22u6.3X0603
GND

10uF x 4 /0603
C11-1067333-Y01

+VCC_CORE
C23 C10u6.3X5-HF
C19 C10u6.3X5-HF
C24 C10u6.3X5-HF
C18 C10u6.3X5-HF
GND

	Haswell	Boardwell
R231	No Stuff	Stuff
C284	No Stuff	Stuff
C271	No Stuff	Stuff
R12	No Stuff	Stuff
R11	No Stuff	Stuff

2014.2.20 Modify for Haswell CPU

95A

+VCC_CORE

HASWELL_BGA_E

U1E

B43 B45 B46 B48 C27 C28 C31 C32 C34 C36 C38 C39 C42 C43 C45 C46 C48 D27 D28 D31 D32 D34 D36 D38 D39 D42 D43 D45 D46 D48 E27 E28 E31 E32 E34 E36 E38 E39 E42 E43 E45 E46 E48 F27 F28 F31 F32 F34 F36 F38 F39 F42 F43 F45 F46 F48 G27 G29 G31 G32 G34 G36 G38 G39 G42 G43 G45 G46 G48 H11 H12 H13 H14 H16 H17 H18 H19 H20 H21 H23 H24 H25 H26 H27 H29 — VCC

RSVD J17 J21 J26 J31

4.2 A

VDDQ AR29 AR31 AR33 AT13 AT19 AT23 AT27 AT32 AT36 AV37 AW22 AW25 AW29 AW33 AY18 BB21 BB22 BB26 BB27 BB30 BB31 BB34 BB36 BD22 BD26 BD30 BD33 BE18 BE22 BE26 BE30 BE33

+1_35VDIMM

PEC20 C330u2SO

C391 C1u25X0402
C389 C1u25X0402
C392 C1u25X0402
C436 C10u6.3X5-HF
C440 C10u6.3X5-HF
C437 C10u6.3X5-HF

GND

1u*3 / 0402
10u*3 / 0603

+VCC_CORE

	Haswell	Boardwell
R229	No Stuff	Stuff

RSVD AN31 L6 VCC M6 VCC AN22 RSVD AN18 RSVD

R217 100R1%0402

VCC_SENSE C50 — VCCSENSE 53

RSVD AH9

VCCIO_OUT D51

FC_F17 F17 — R229 X_0R1%0402 — 1_05V_AJ12

VCOMP_OUT AK6 — +VCCIOA_OUT

RSVD AN33 W9 J12 AR49

300 mA

2014.2.20 Modify for Haswell CPU

+VCCIO_OUT

C286 C4.7u10X0603

GND

CLK and DATA Misatch 2000mils
SVID total Length not over 6"

VIDALERT J53 — VR_SVID_ALERT# R — R13 43R0402 — VR_SVID_ALERT# 53

VIDSCLK J52 — VR_SVID_CLK — VR_SVID_CLK 53

VIDSOUT J50 — VR_SVID_DATA — VR_SVID_DATA 53

+VCCIO_OUT
R14 75R1%0402
R16 130R1%0402
Close to CPU

+VCCIO_OUT
R211 54.9R1%0402
R207 130R1%0402
Close to IMVP

VSS B51 E52 V49 U49 W49 V50 AN49 AJ49 AG50 AK49 AJ50 AP49 AB50 AP50 AD50 AM50

PWR_DEBUG F19 — PWR_DEBUG# — PJNC26

RSVD_TP AM49 — VIA_IVR_ERROR

RSVD_TP — VIA_IST_TRIGGER

If XDP not implemented, then Route Processor PWR_DEBUG as a test point. This Test point must be clearly labeled

VCC A36 A38 A39 A42 A43 A45 A46 A48 AA46 AA47 AA8 AA9 — +VCC_CORE

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1_05V_AJ12

CPU_FC_PWR R231 X_0R1%0402

C284 X_C0.1u50X70402
C271 X_C22u6.3X0603
GND

25,34 EC_PCH_PWROK — R12 X_6.04KR1%0402 — CPU_FC_PWR — CPU_FC_PWROK — D5 D3 — FC_D5 FC_D3

R11 X_2.67KR1%0402

GND

Resever For BDW H 2-chips

Title	CPU-4 (Power)
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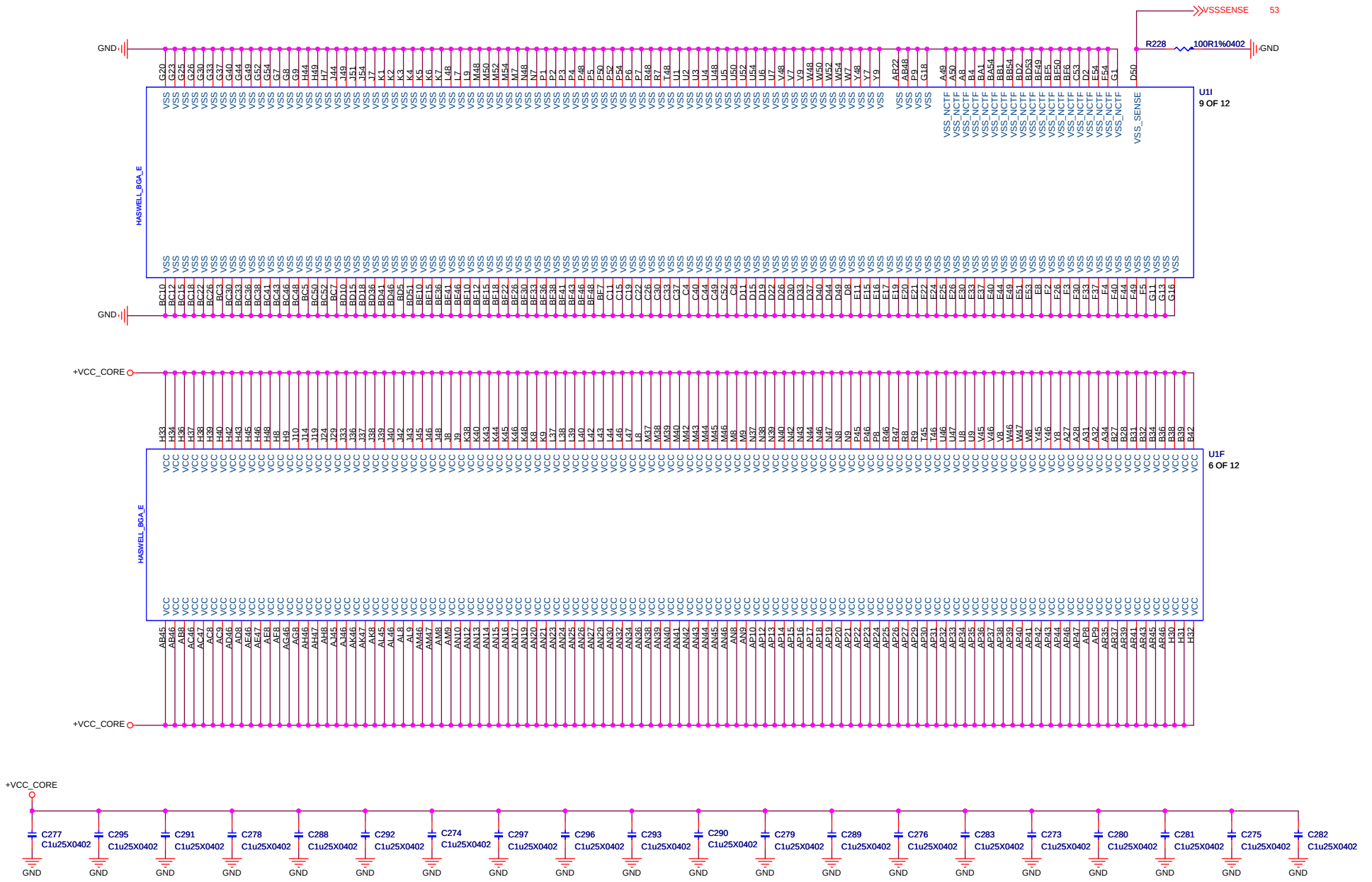
Haswell (Power & GND)



MICRO-STAR INT'L CO.,LTD.

Title	CPU-6 (Power & GND)	
Size	Document Number MS-16H3	Rev 0B
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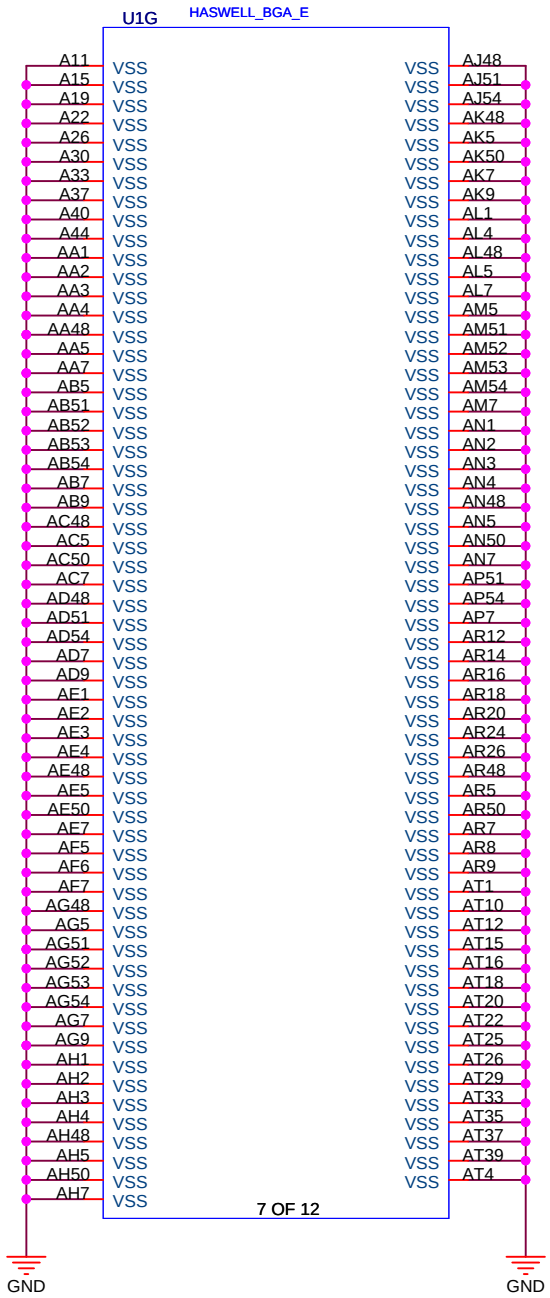
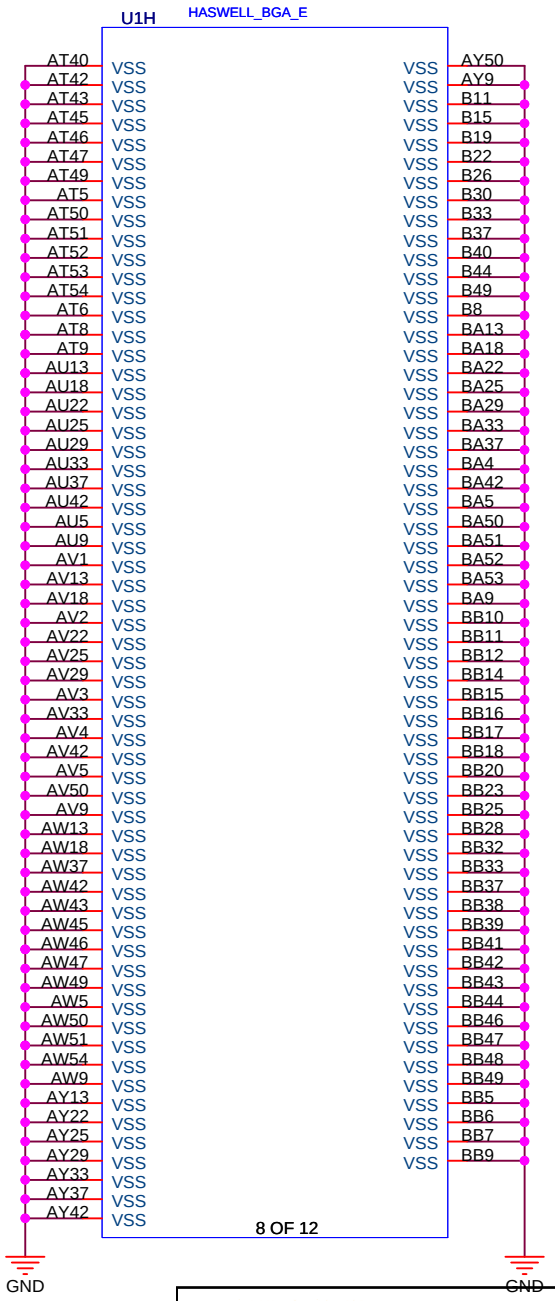
Haswell (GND)





MICRO-STAR INT'L CO.,LTD.		
Title: CPU-5 (GND)		
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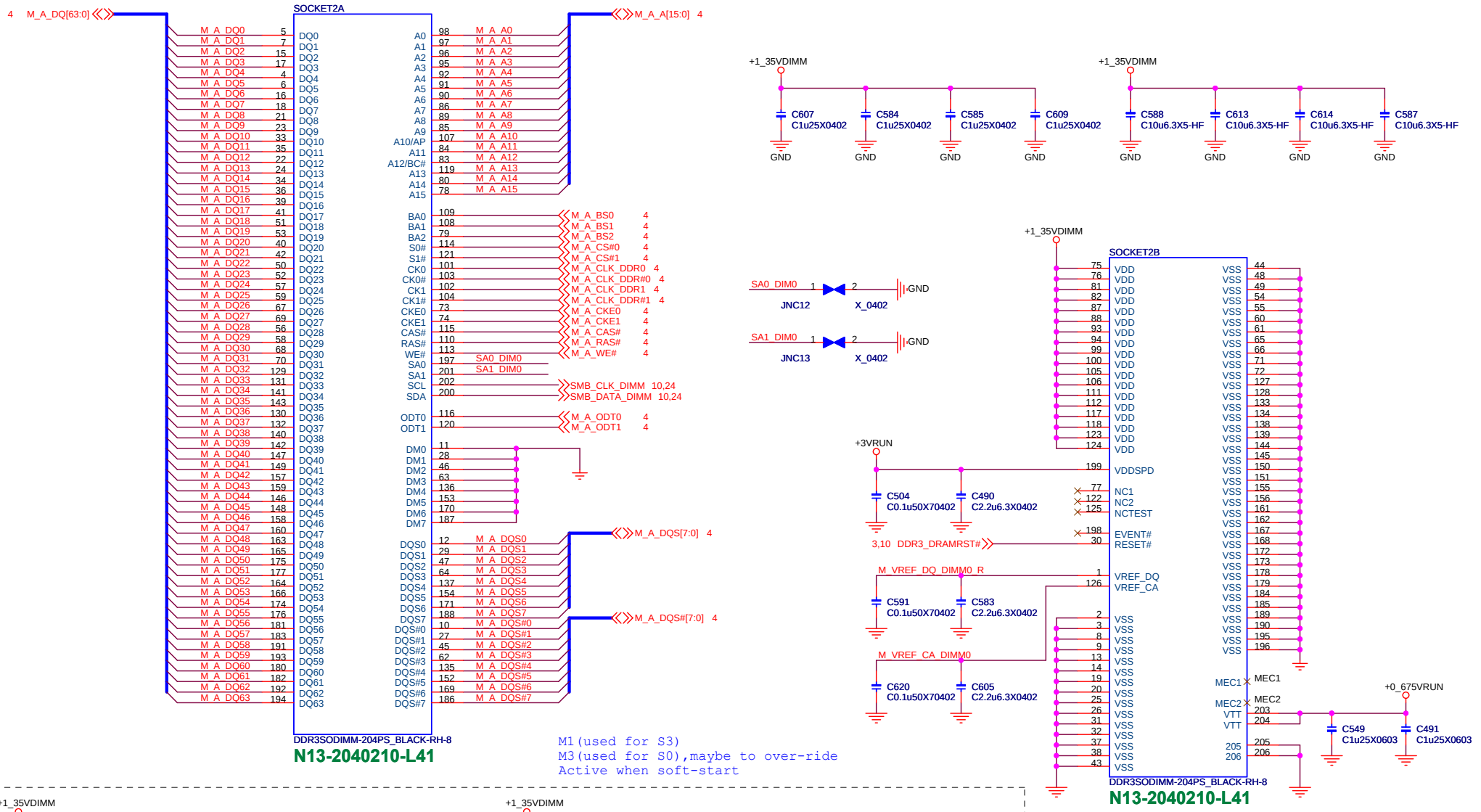
SODIMM#A



MICRO-STAR INT'L CO.,LTD.		
Title: DDR3L SODIMM 0		
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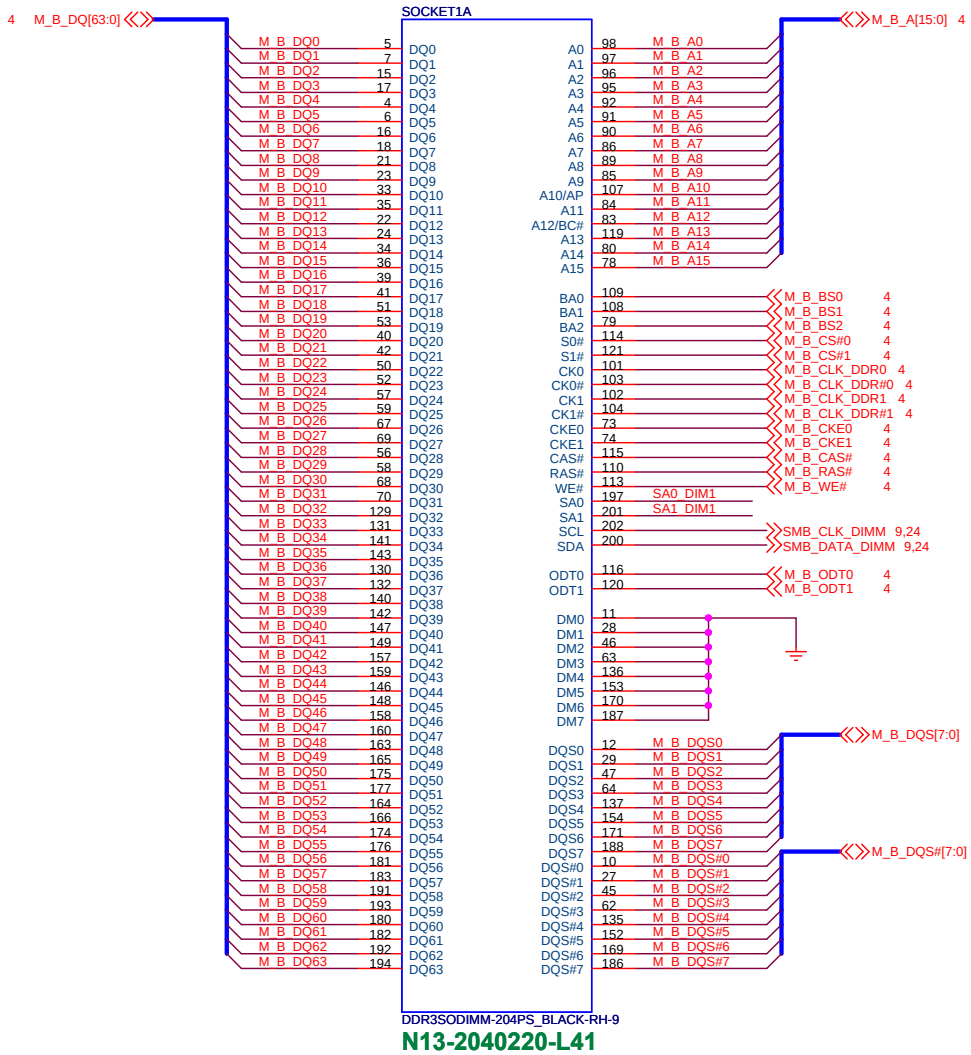
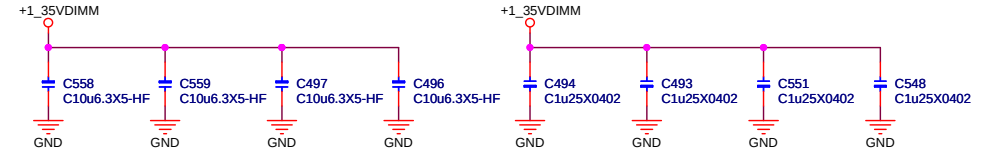
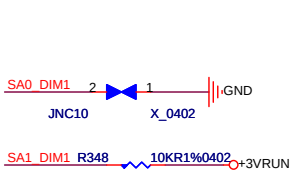
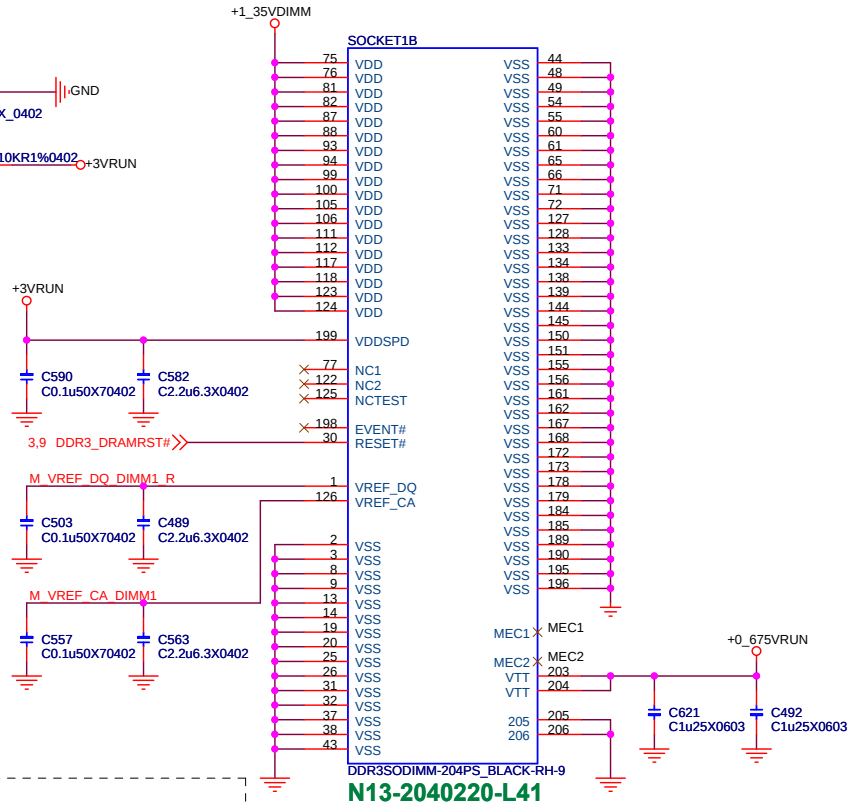
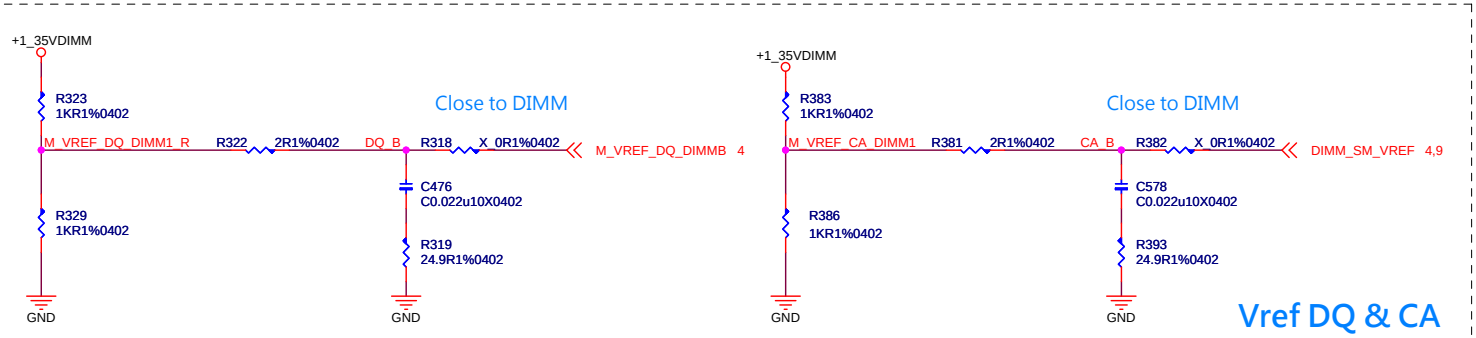
SODIMM#B











MICRO-STAR INT'L CO.,LTD.

Title: DDR3L SODIMM 1

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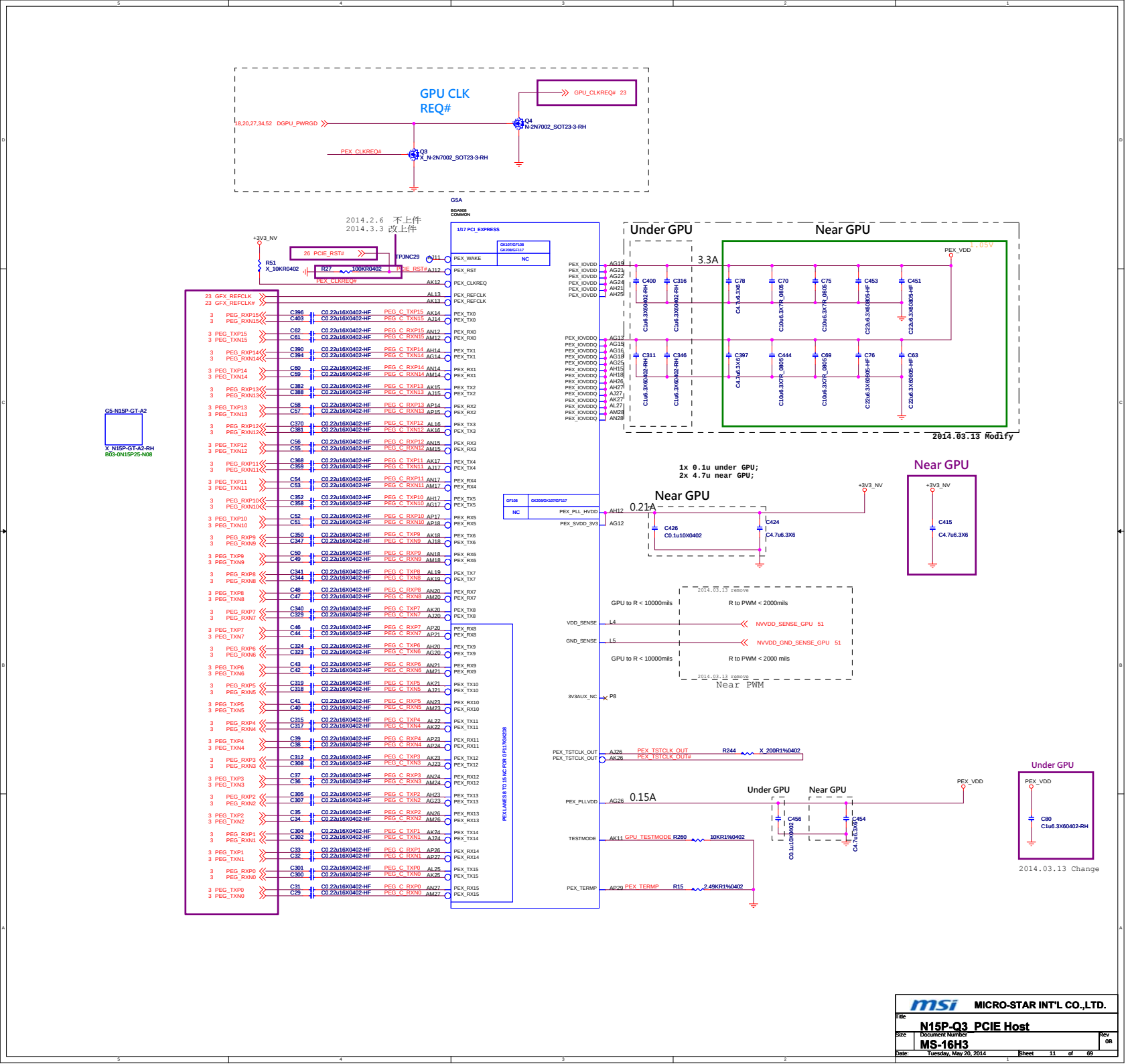

MSI	MICRO-STAR INT'L CO.,LTD.
Title	N15P-Q3 PCIE Host
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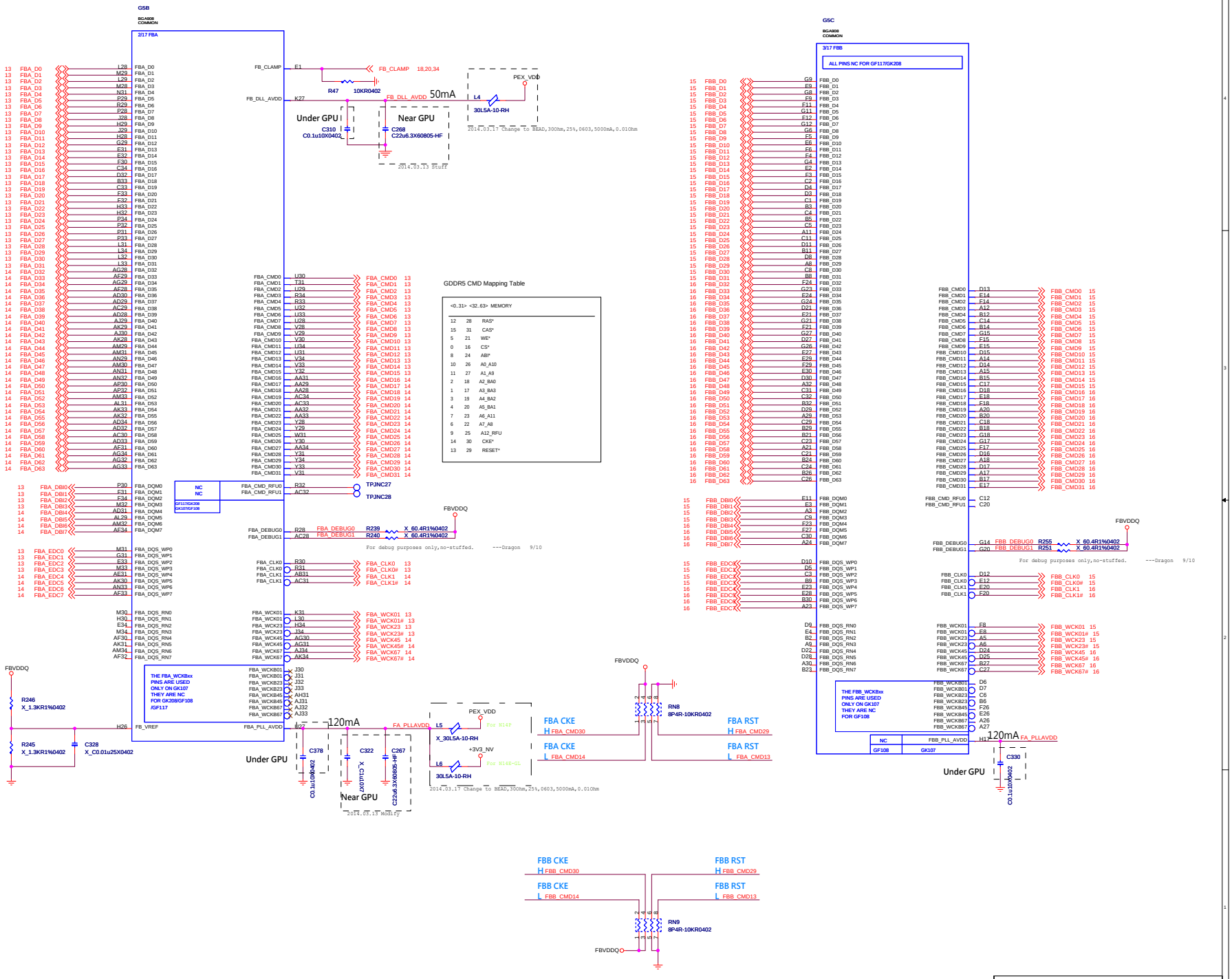

MICRO-STAR INT'L CO.,LTD.		
Title: N15P-Q3 MEM Interface		
Size	Document Number: MS-16H3	Rev: 0B
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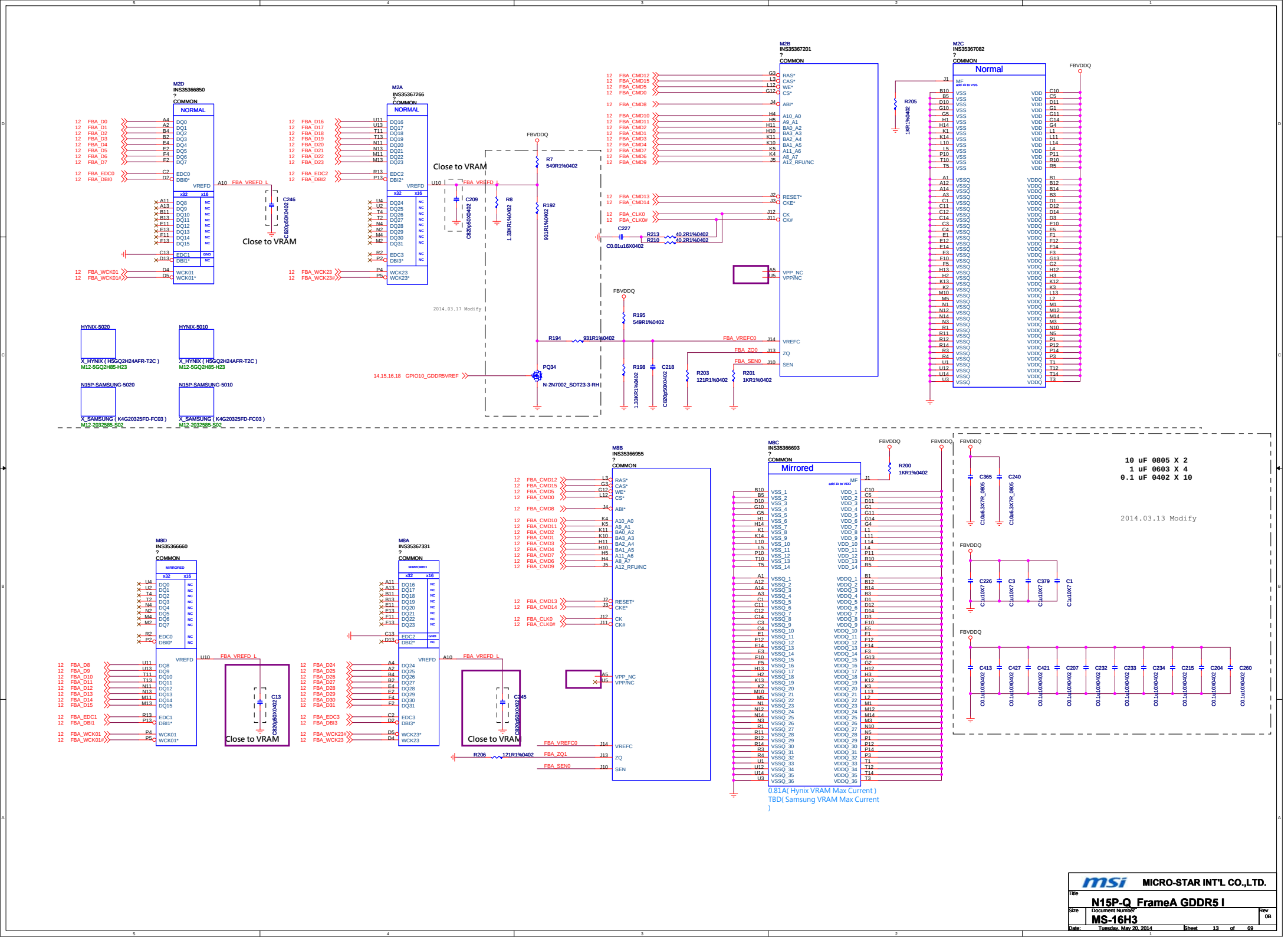
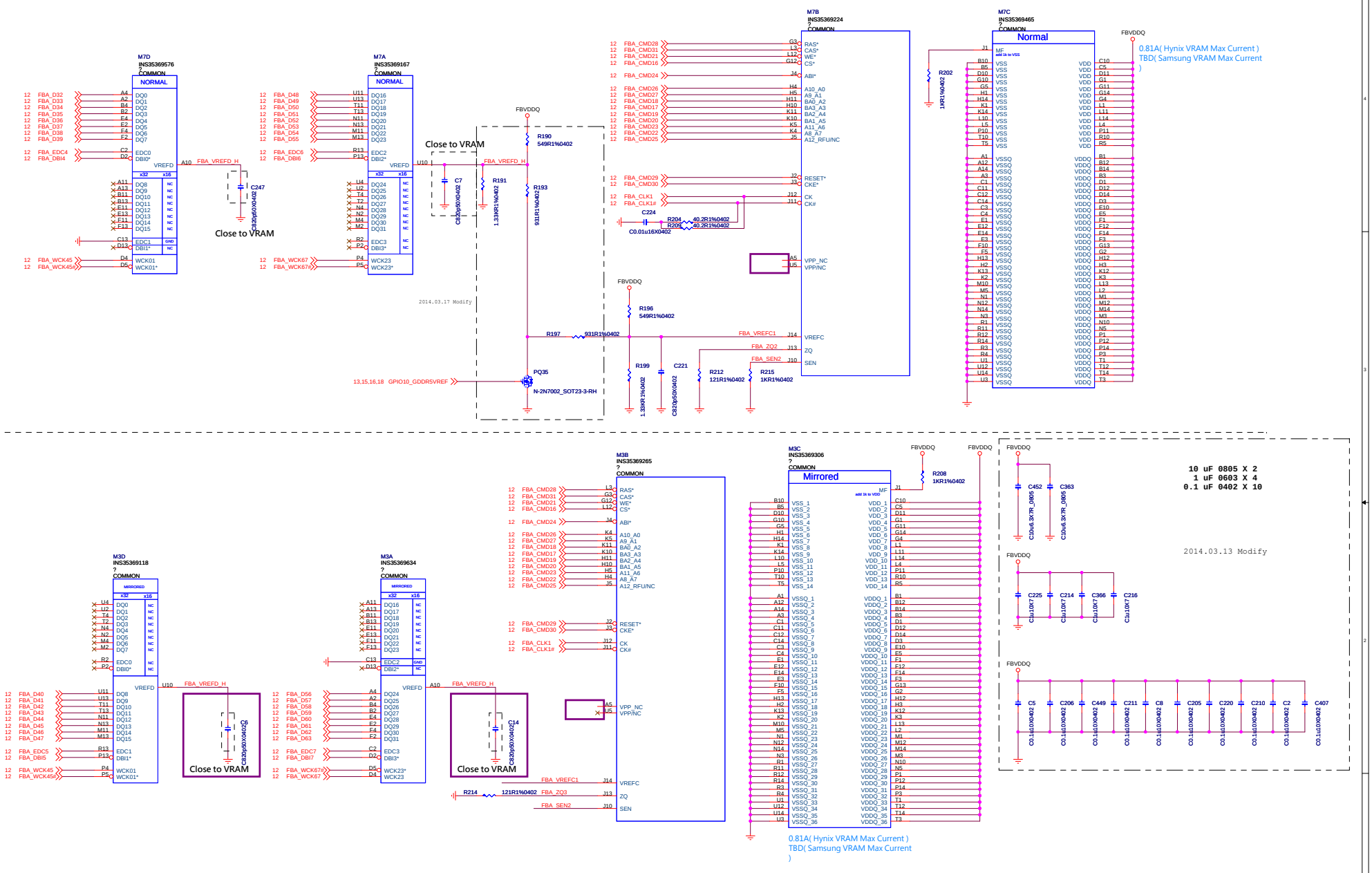
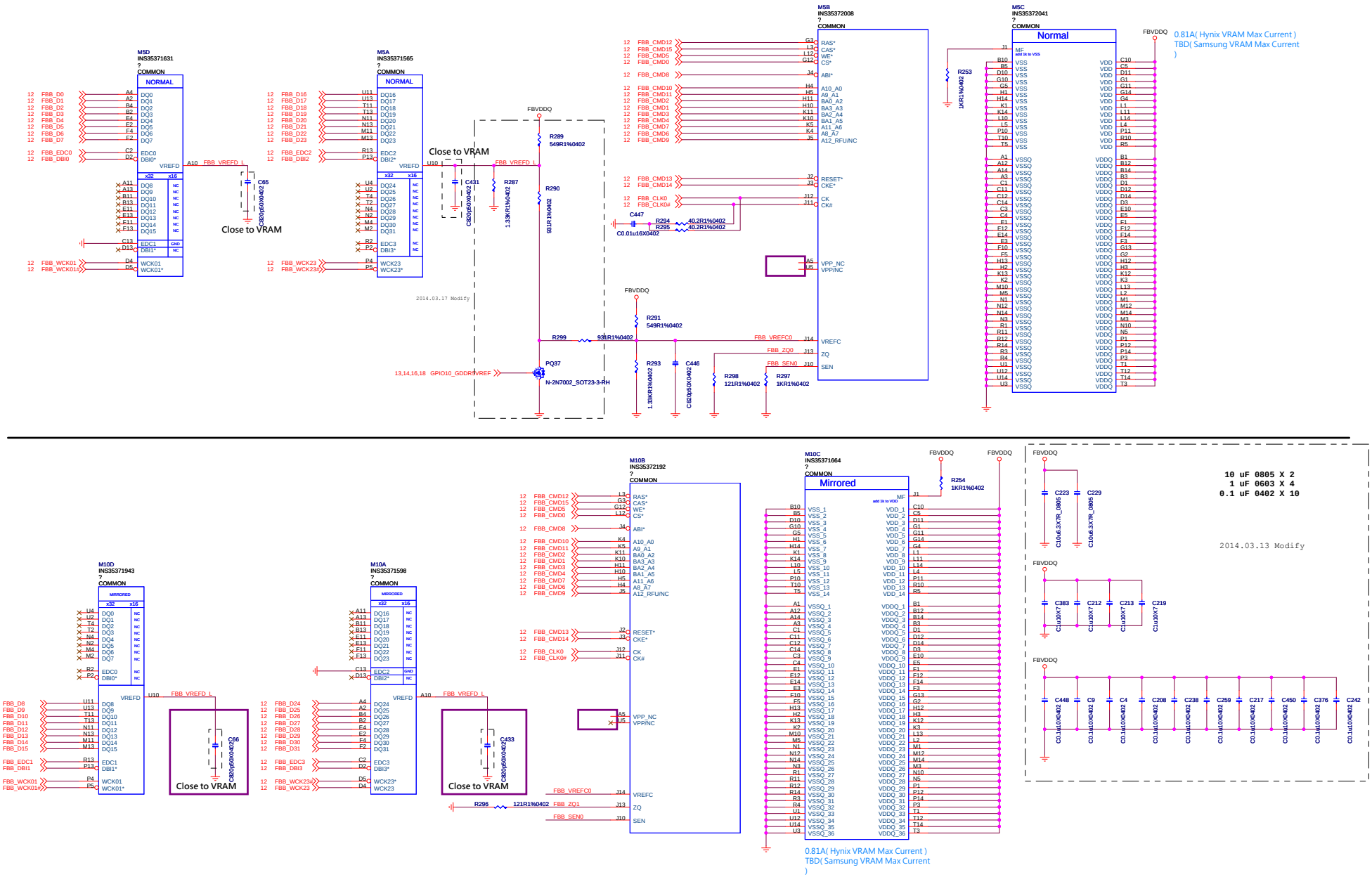


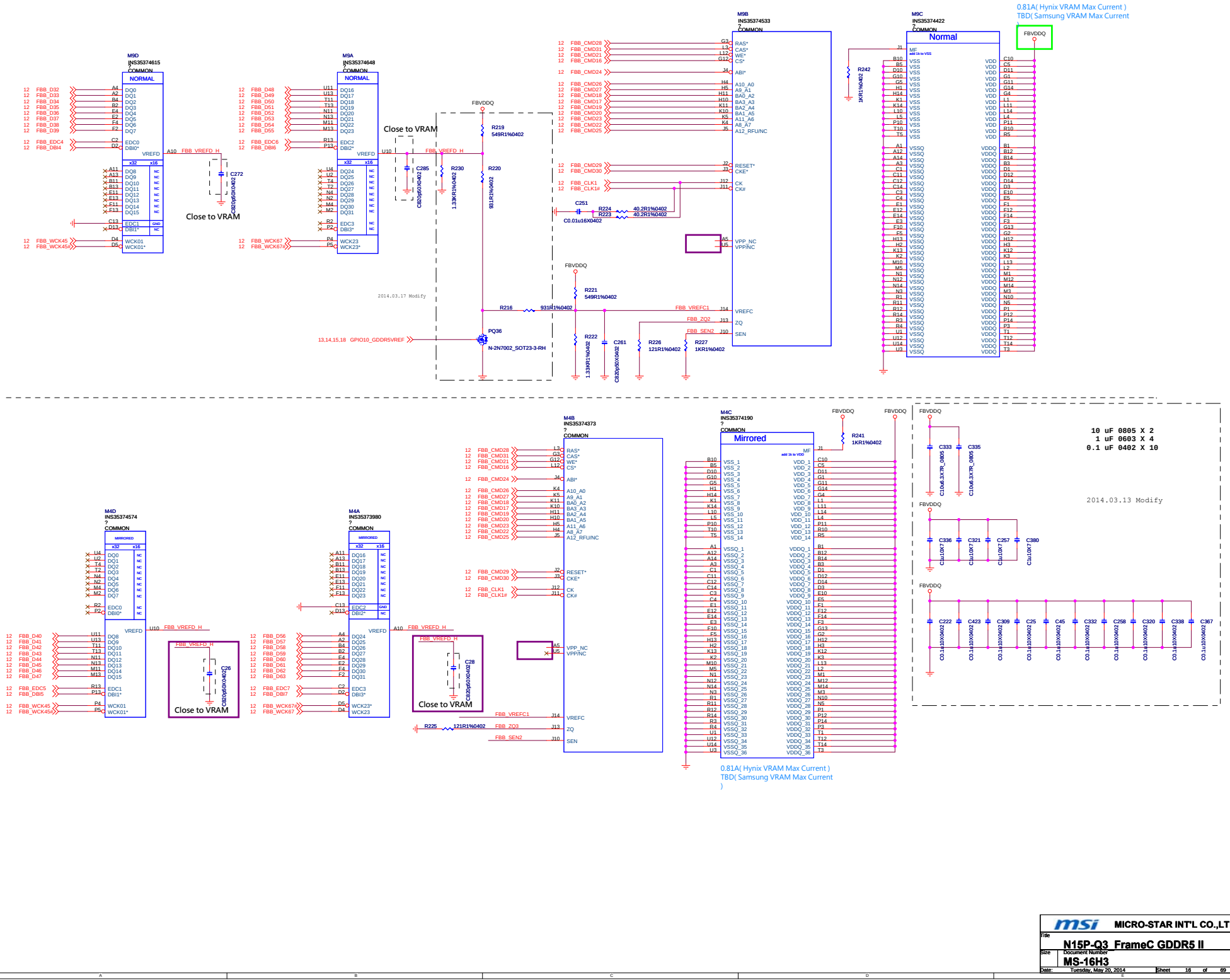
MICRO-STAR INT'L CO.,LTD.			
Title	N15P-Q FrameA GDDR5 I		
Size	Document Number		Rev
	MS-16H3		0B
Date:	Tuesday, May 20, 2014	Sheet 13 of 69	



MICRO-STAR INT'L CO.,LTD.			
Title: N15P-Q3_FrameA GDDR5 II			
Size	Document Number: MS-16H3		Rev: 0B
Date: Tuesday, May 20, 2014		Sheet 14 of 69	



msi	MICRO-STAR INT'L CO.,LTD.		
Title	N15P-Q3_FrameC GDDR5 I		
Size	Document Number MS-16H3		Rev 0B
Date: Tuesday, May 20, 2014		Sheet 15 of 69	


0.81A(Hynix VRAM Max Current)
TBD(Samsung VRAM Max Current
M9D
INS35374615
COMMON
NORMAL
M9A
INS35374648
COMMON
NORMAL
M9B
INS35374533
COMMON
M9C
INS35374422
COMMON
Normal
FBVDDQ
Close to VRAM
Close to VRAM
R219
549R1%0402
R220
931R1%0402
R230
1.33KR1%0402
C285
C820p50X0402
C272
C820p50X0402
C251
C0.01u16X0402
R224
40.2R1%0402
R223
40.2R1%0402
R242
1KR1%0402
FBVDDQ
R221
549R1%0402
R216
931R1%0402
R222
1.33KR1%0402
C261
C820p50X0402
R226
121R1%0402
R227
1KR1%0402
PQ36
N-2N7002_SOT23-3-RH
2014.03.17 Modify
M4D
INS35374574
COMMON
M4A
INS35373980
COMMON
M4B
INS35374373
COMMON
M4C
INS35374190
COMMON
Mirrored
R241
1KR1%0402
FBVDDQ
10 uF 0805 X 2
1 uF 0603 X 4
0.1 uF 0402 X 10
2014.03.13 Modify
0.81A(Hynix VRAM Max Current)
TBD(Samsung VRAM Max Current
)
R225
121R1%0402
MICRO-STAR INT'L CO.,LTD.
Title
N15P-Q3 FrameC GDDR5 II
Size
Document Number
MS-16H3
Rev
0B
Date: Tuesday, May 20, 2014
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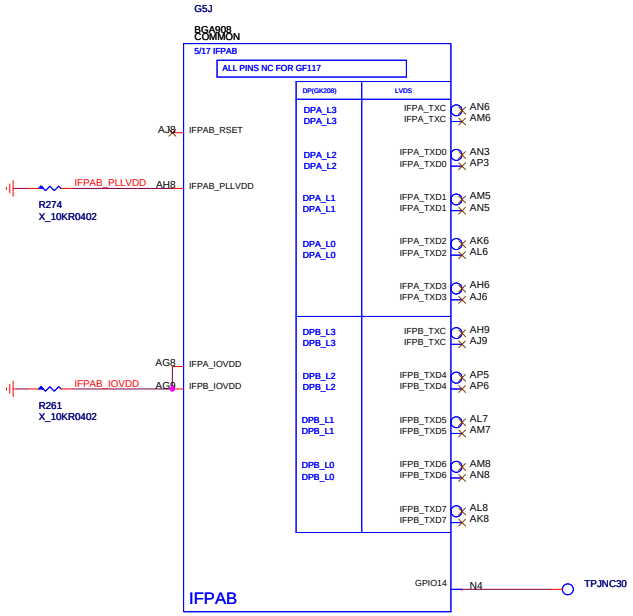
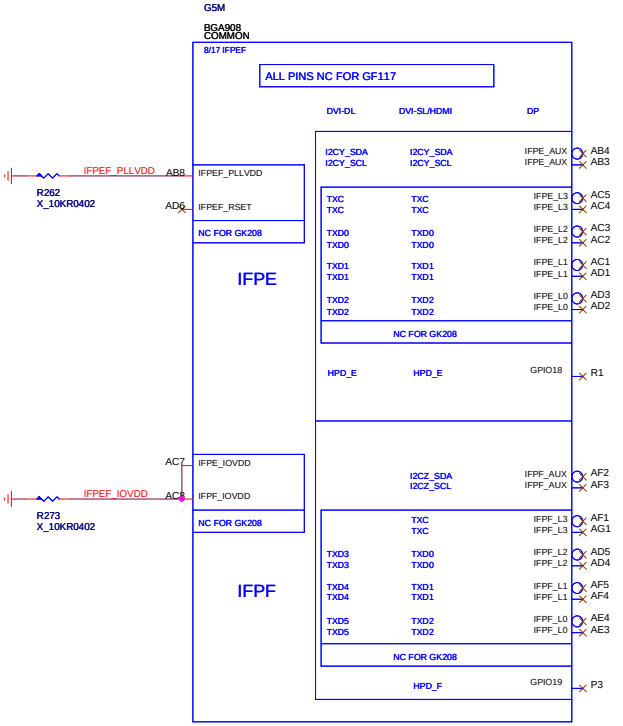
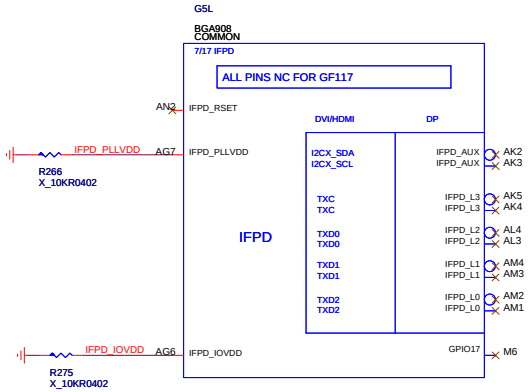
IFP A/B LVDSDual Link



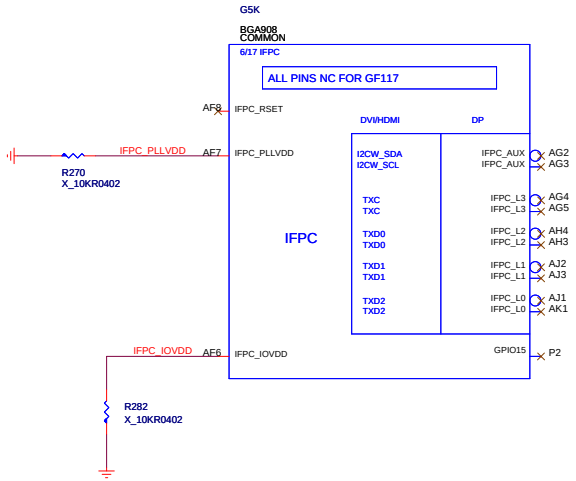
IFP E/F Dual Link TMDS DVI-I



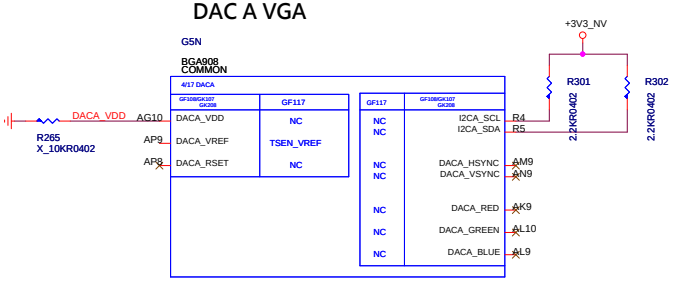
IFP D Dual Mode DP



IFP C Native HDMI OR DP

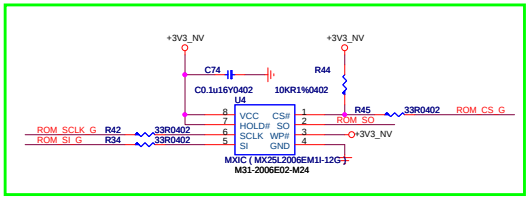


DAC A VGA

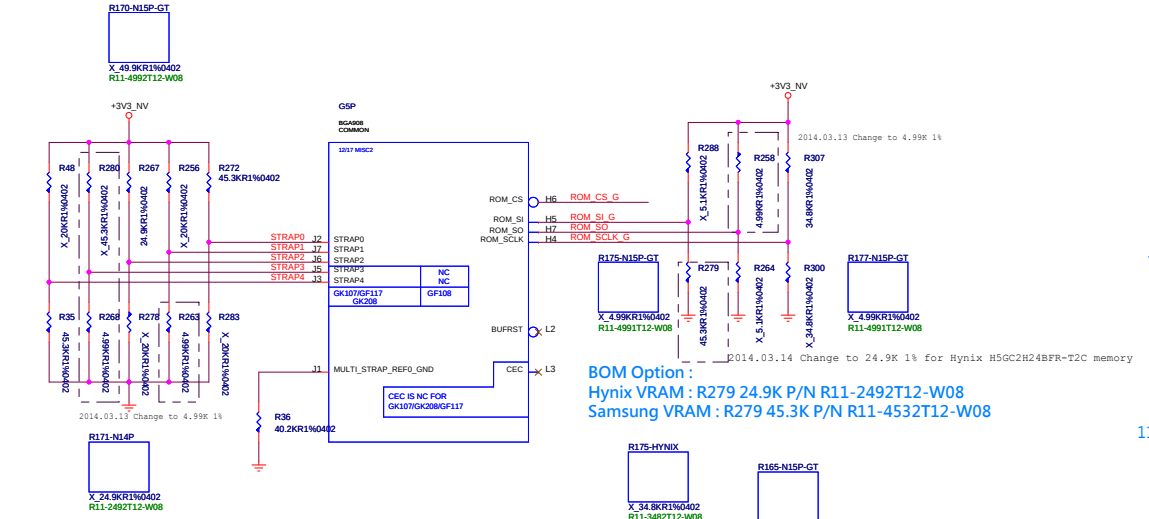


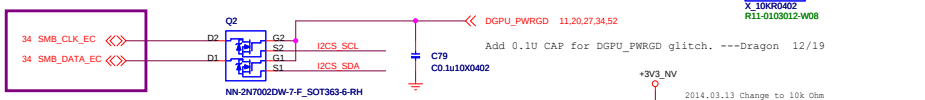
MICRO-STAR INT'L CO.,LTD.			
Title: N15P-Q3_Display Interface			
Size	Document Number: MS-16H3		Rev: 0B
Date: Tuesday, May 20, 2014	Sheet 17 of 69		

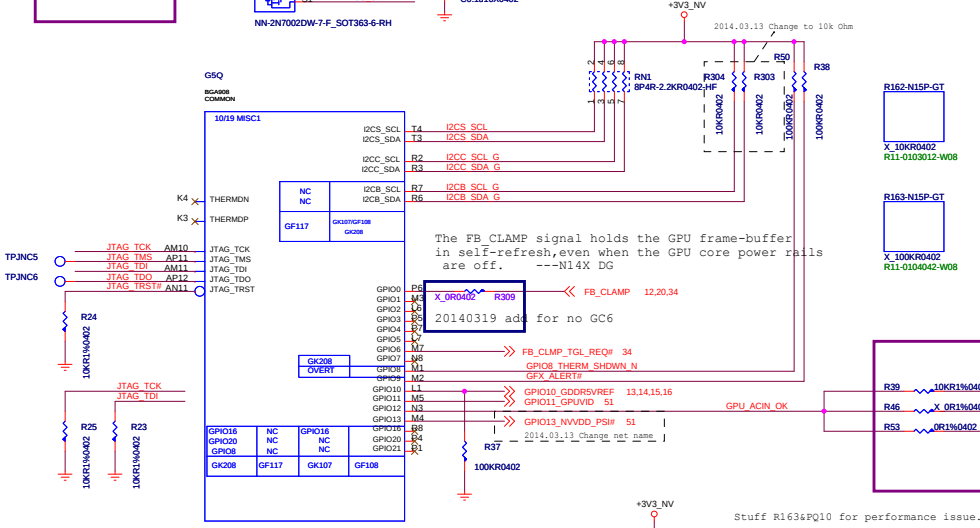
external EEPROM

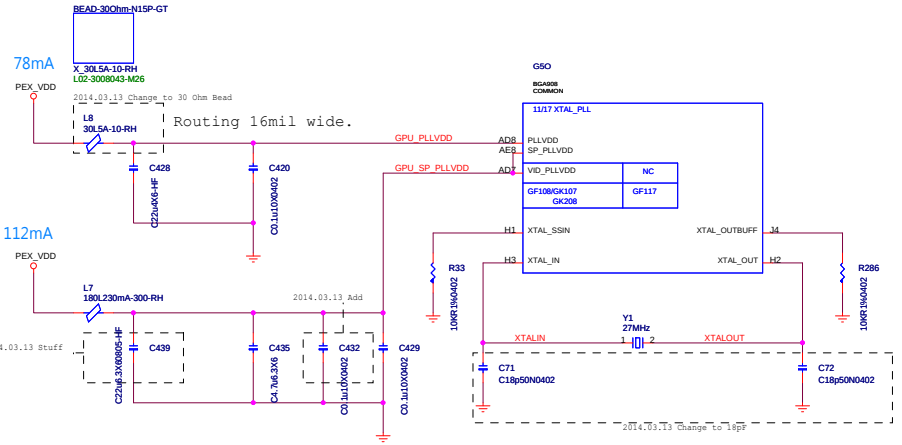


Item	Location	N15P-Q3
Strap Mode	R3365	MULTISTRAP_REF_GND,40.2K PD to GND
Device ID		0x11FC
Package		GB4-128
Memory Type		GDDR5
ROM_SI	R3175	0x4, Hynix 2G, 24.9kohm PD
	R3175	0x7, Samsung 2G, 45kohm PD
ROM_SO	R3193	0x8, 5kohm pull up
ROM_SCLK	R3179	0x1110,35kohm PU(with ROM)
Strap0	R3170	45kohm pull up
Strap1	R3180	5kohm pull down
Strap2	R3171	DID,0x1100, 24.9kohm PU
Strap3	R3188	0x0 for Optimus, 5kohm pull down
Strap4	R3183	0x0111, 45kohm pull down









Pin Name	Normal function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	FB_CLAMP_MON	I	FB Clamp monitor	
GPIO1	NC	O		
GPIO2	NC	O		
GPIO3	NC	O		
GPIO4	NC	O		
GPIO5	NC	O		
GPIO6	FB_CLAMP_TGL_REQ	O	FB Clamp toggle request	
GPIO7	NC	O		
GPIO8	OVERT	I	Thermal Over Temperature	100K pull-up
GPIO9	ALERT	I/O	Active Low Thermal Alert	100K pull-up
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	PWM_VID	O	GPU Core VDD PWM control signal	
GPIO12	PWR_LEVEL	I	AC power detect	100K pull-up
GPIO13	SPI	O	Phase Shedding	10K pull-up
GPIO14	NC	I		
GPIO15	NC	I		
GPIO16	NC	O		
GPIO17	NC	I		
GPIO18	NC	I		
GPIO19	NC	I		
NC	NC			

MICRO-STAR INT'L CO.,LTD.

Title: N15P-Q3 Thermal & GPIO

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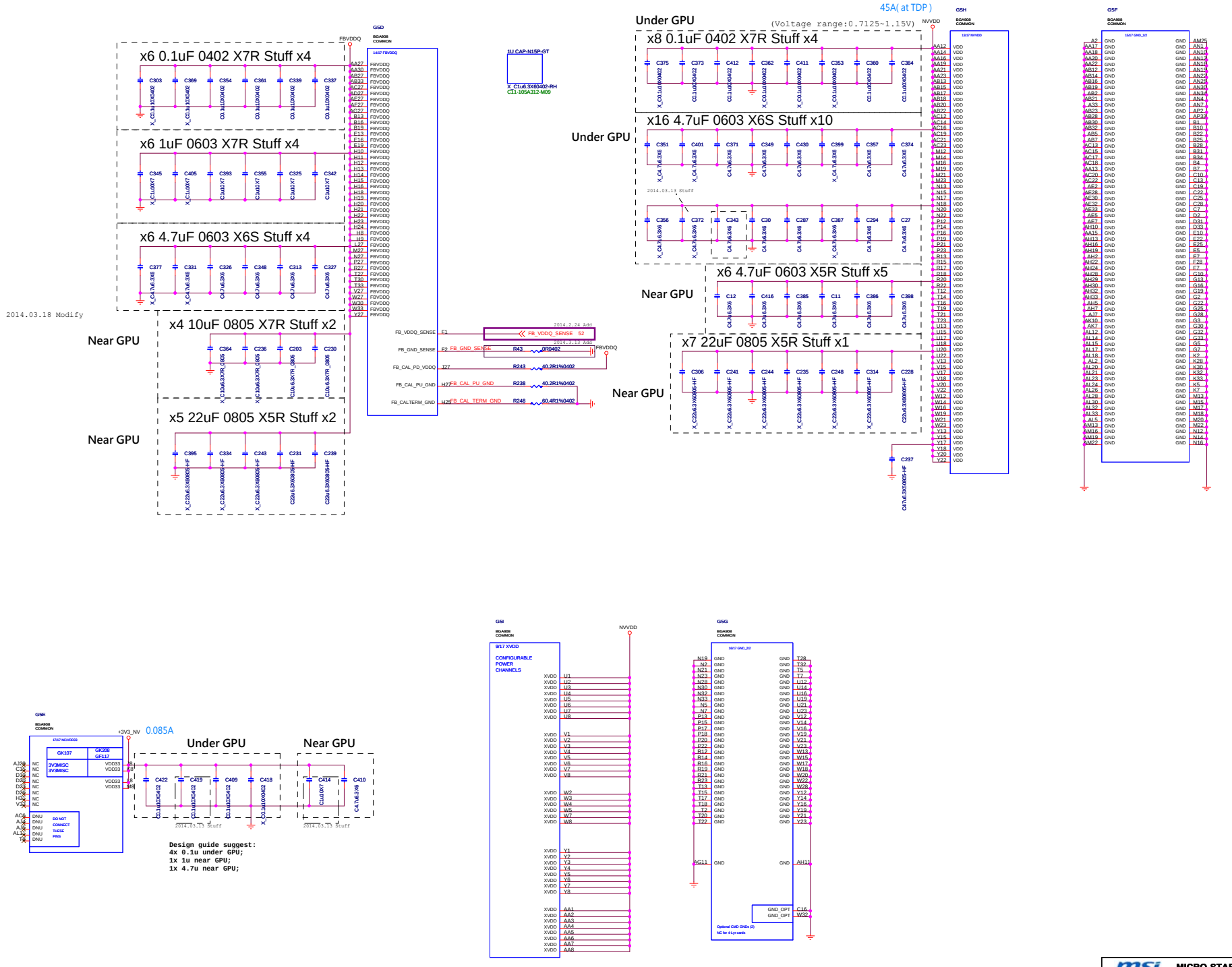

msi	MICRO-STAR INT'L CO.,LTD.		
Title	N15P-Q3 Power & GND		
Size	Document Number MS-16H3		Rev 0B
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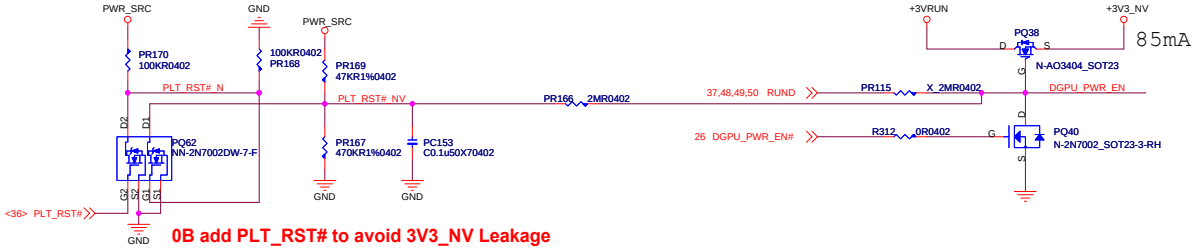
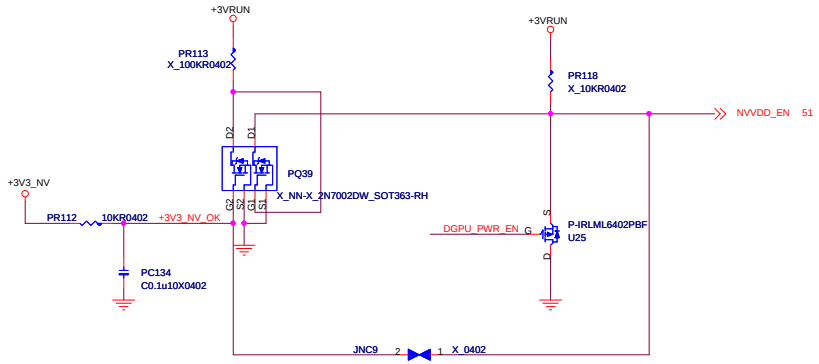
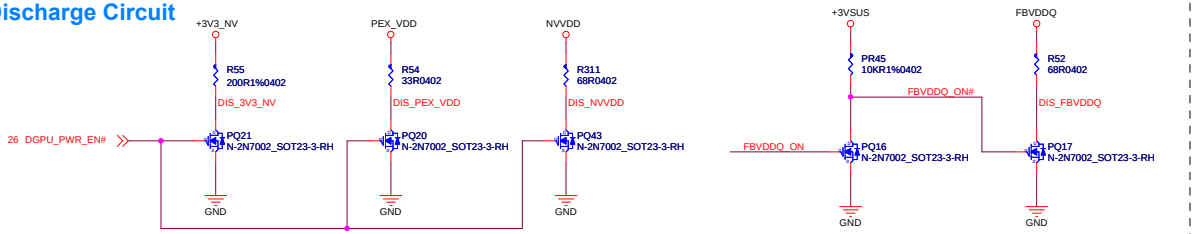
DGPU_Power Control

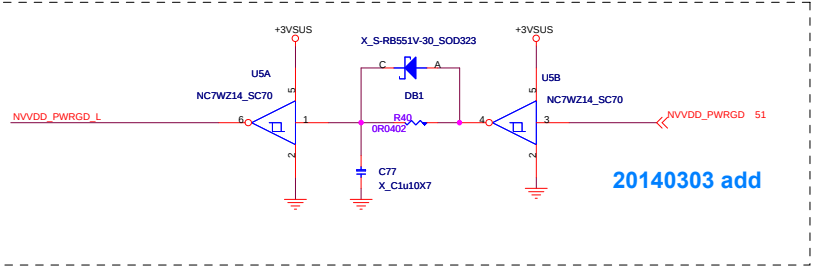


0B add PLT_RST# to avoid 3V3_NV Leakage

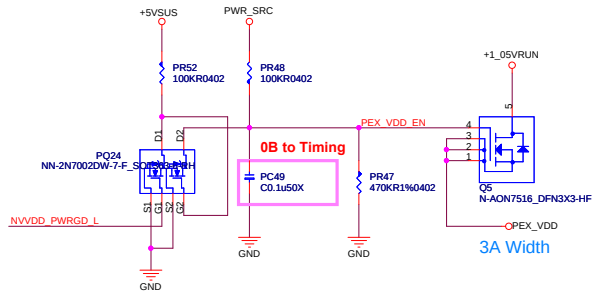


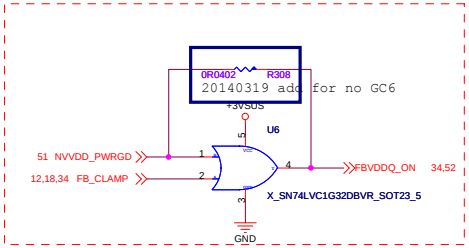
Discharge Circuit

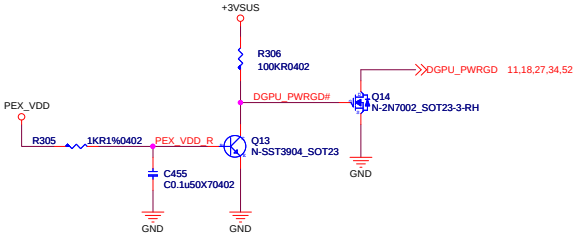




PEX_VDD

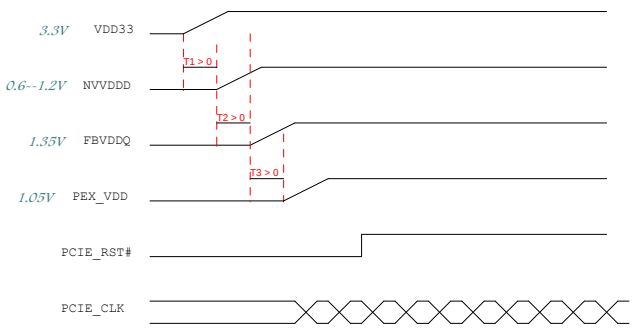






msi MICRO-STAR INT'L CO.,LTD.		
Title: N15P-Q3_Power Control		
Size	Document Number: MS-16H3	Rev: 0B
Date: Tuesday, May 20, 2014	Sheet 20 of 69	

GPU POWER ON SEQUENCE



NOTES: The ramp time for any rail must be more than 40 us.
The total time for all rails to ramp up should be within 6ms.
A power rail has to ramp up to 90% before the next rail in sequence can start ramping up.
No signal should be applied to the GPU before the power rails are fully ramped

NOTES: For optimus system, VDD33 usually drops down earlier than NVVDD and FBVDDQ.

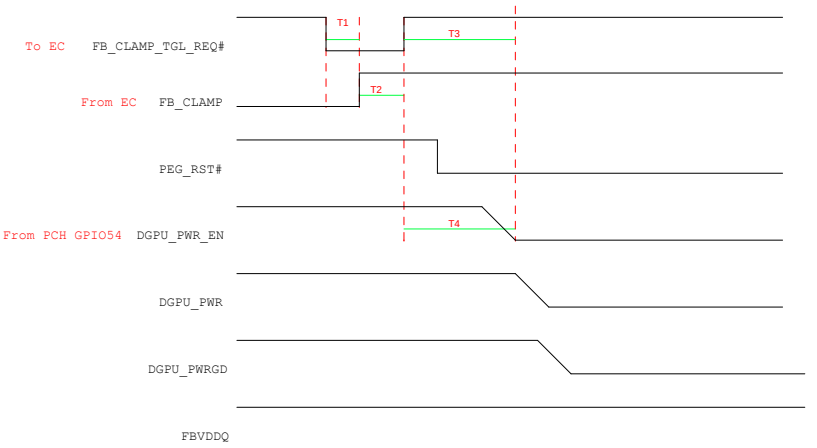
NOTES: All rails must be powered off within 10 ms from the first rail powering off.

GC6 TIMING

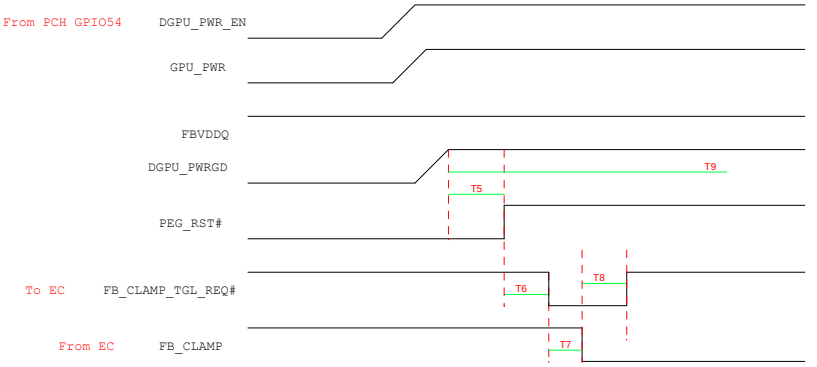
	Min	Max	Unit	Description
T1	0	10	mS	GPU asserts toggle request to GB_CLAMP assertion
T2	0	1	mS	Assertion of FB_CLAMP to de-assertion of toggle request
T3	0	10	mS	De-assertion of toggle request to GPU PWR_EN=0
T4	0.01	1	mS	PEX reset assertion to GPU PWR_EN de-assertion
T5	0.1	5	mS	GPU power stable to de-assertion of PEX reset
T6	3.3		mS	De-assertion of PEX reset to toggle request assertion
T7	0	1	mS	Assertion of toggle request to de-assertion of FB_CLAMP
T8	0	1	mS	De-assertion of FB_CLAMP to de-assertion of toggle request
T9	TBD	TBD	mS	GPU power enable to GPU ready for normal operatioon

Notes: *System designers should minimize T1,T3,T4,T5,T6,and T7 to increase the time spent in GC6.
This increased GC6 residency will improve both power savings and user experience.
**If10 ms expirs for T1, the GPU will de-assert FB_CLAMP_TGL_REQ# and abort the GC6 entry procedure.
FB_CLAMP should never assert outside an FB_CLAMP_TGL_REQ# handshake.

GC6 ENTRY SEQUENCE(NOT support)



GC6 EXIT SEQUENCE



MICRO-STAR INT'L CO.,LTD.

Title: N15P-Q3 Power Sequence

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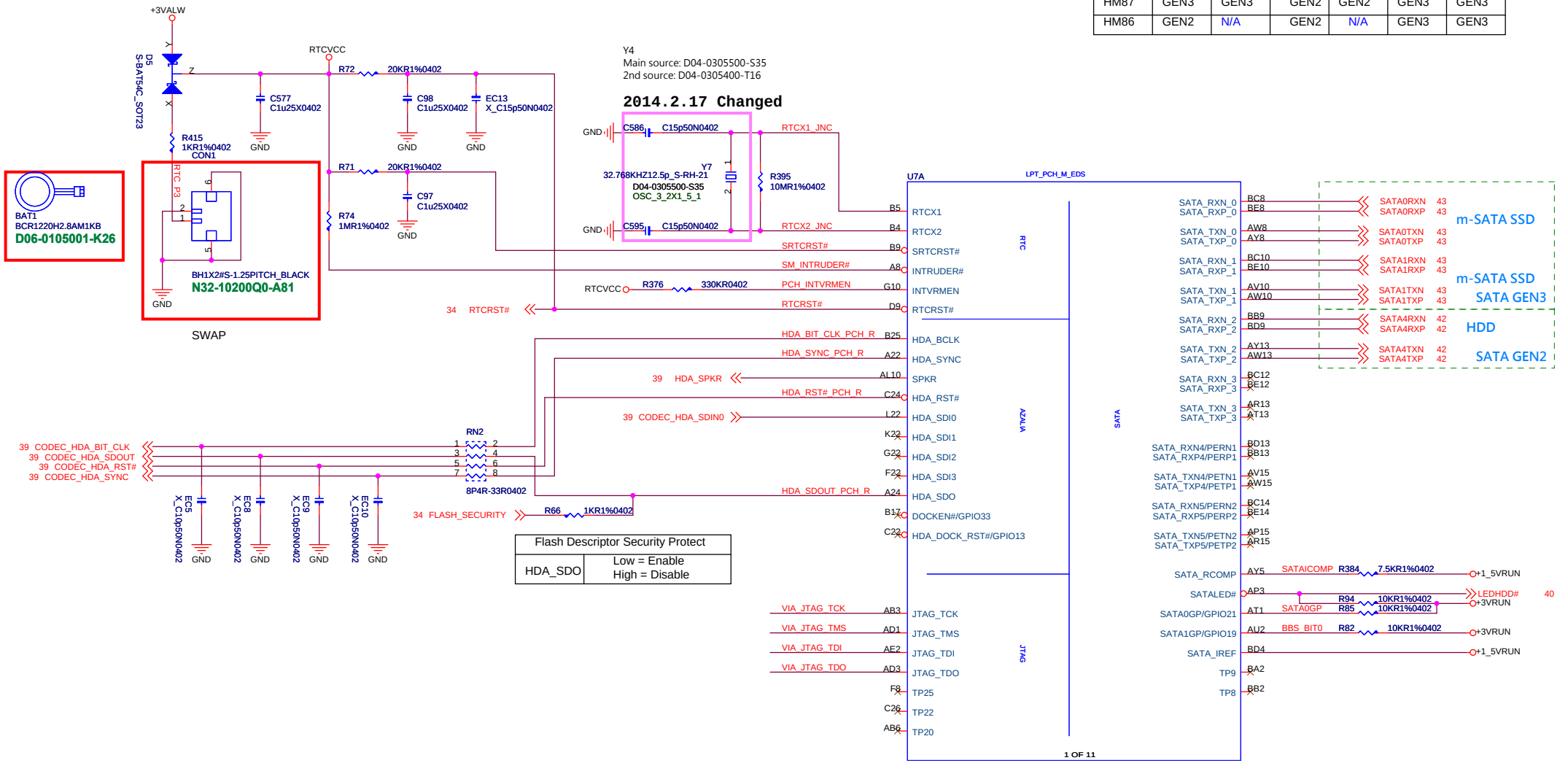
Lynx Point (HDA/JTAG/SATA)

SKU	High Speed SATA I/O Ports					
	SATA-0	SATA-1	SATA-2	SATA-3	SATA-4	SATA-5
HM87	GEN3	GEN3	GEN2	GEN2	GEN3	GEN3
HM86	GEN2	N/A	GEN2	N/A	GEN3	GEN3



Flash Descriptor Security Protect	
HDA_SDO	Low = Enable High = Disable

SPK	The Signal has a weak internal pull-down Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Panther Point will disable the TCO Timer system reboot feature)

MICRO-STAR INT'L CO.,LTD.

Title: PCH-1 (HDA/JTAG/SATA)

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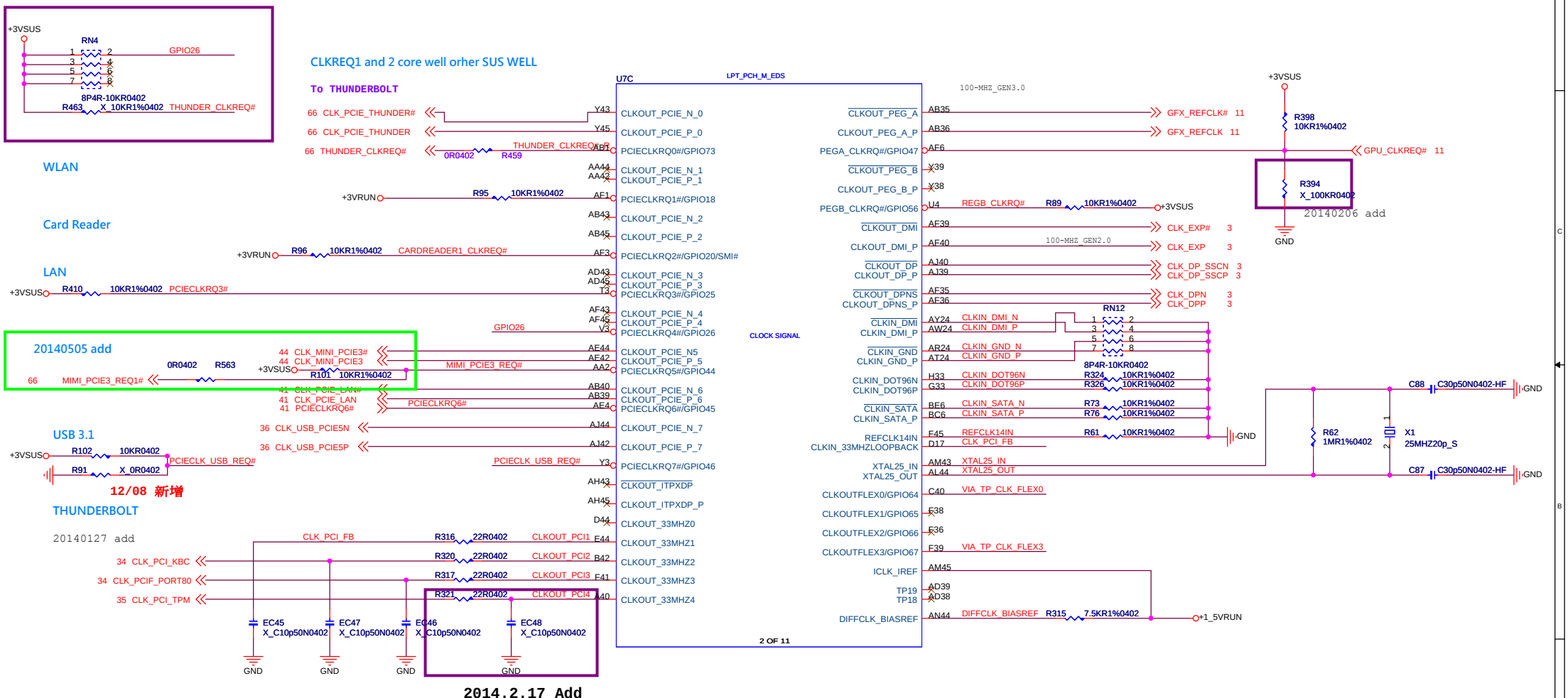
Lynx Point (Clock)

PCIe devices or addin cards that do NOT support CLKREQ# functionality should not route this signal to PCH.
Intel recommends terminating PCIECLKRQx# pin on PCH with 10 kΩ ±10% external pull-up resistor instead of No Connect.
Only PCIECLKRQ[2:1]# on PCH are core well powered. All other PCIECLKRQx# are suspend well powered.



2014.2.17 Add

The CLKREQ# function can be disabled via intel management engine FW .Please refer to INTEL ME FW Bring up guide for configuring/disabling CLKREQ#

MICRO-STAR INT'L CO.,LTD.		
Title: PCH-2 (CLK)		
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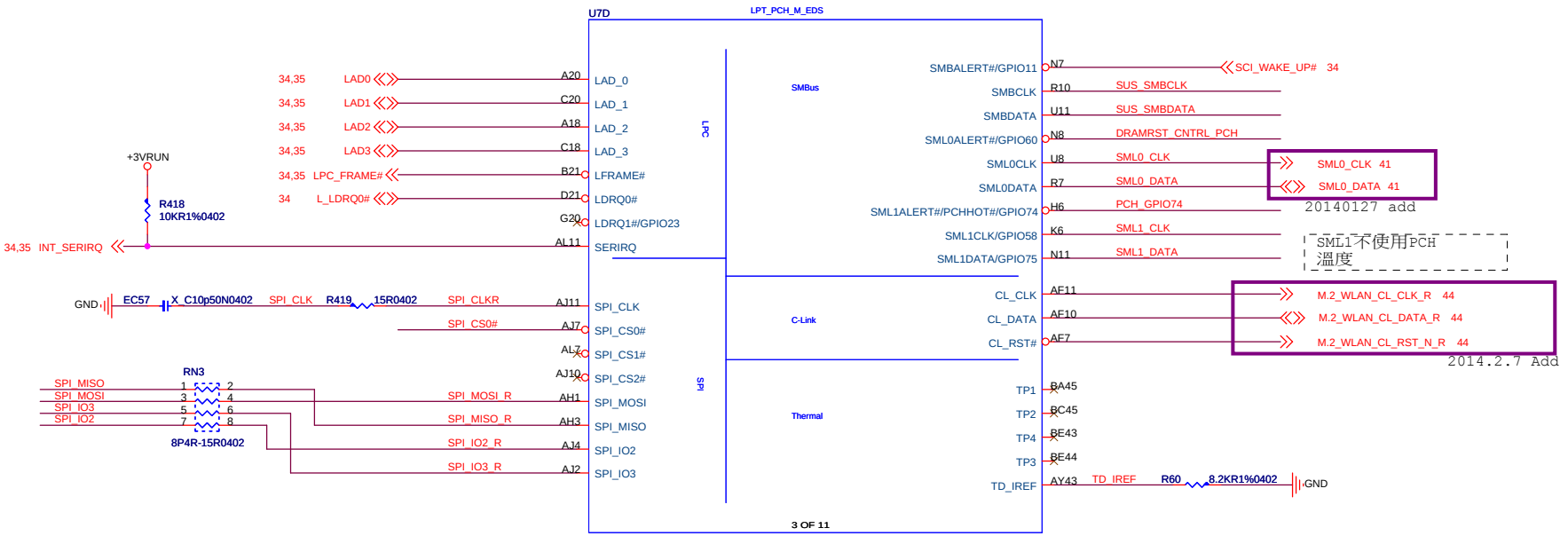
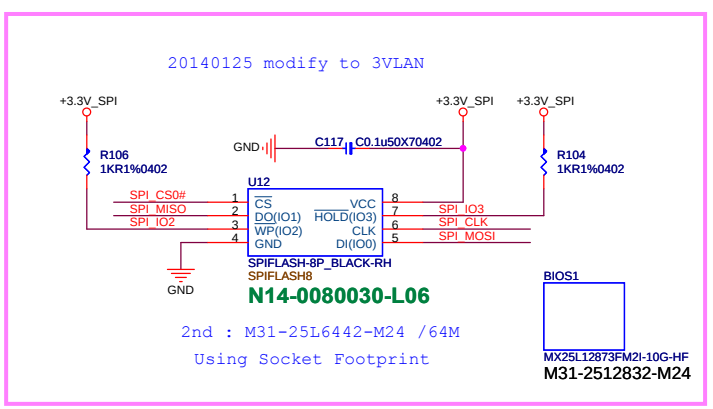
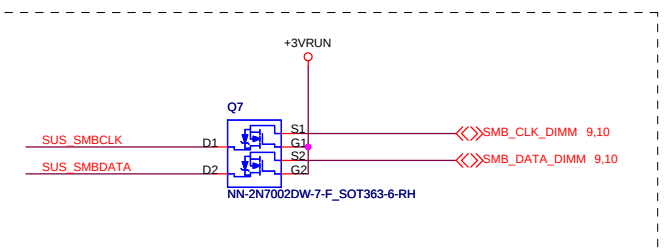
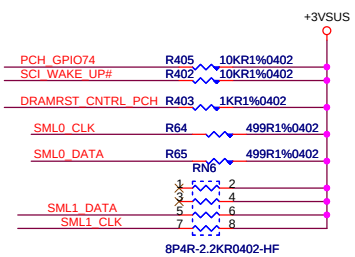
Lynx Point (LPC,SMBUS)

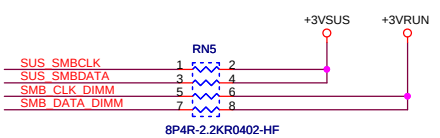


20140310 0A先上socket,N14-0080030-L06
顆粒,M31-25Q6402-E17
(0A Footprint共用SPIFLASH8 is Socket footprint)









MICRO-STAR INT'L CO.,LTD.

Title: PCH-3 (LPC,SMBUS)

Size | Document Number: MS-16H3 | Rev: 0B

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Lynx Point (DMI,FDI)

20140127 add

+3VSUS

SLP_LAN# R420 X_10KR0402
SUSPWRACK R406 10KR1%0402
AC_PRESENT R407 10KR1%0402
PM_RI# R401 10KR1%0402
PM_BATLOW# R404 8.2KR1%0402
PCIE_WAKE# R87 10KR1%0402

+3VRUN

PM_CLKRUN# R416 8.2KR1%0402
PM_SYSRST# R92 10KR1%0402

U7B — LPT_PCH_M_EDS

DMI_RXN0 AW22 DMI_RXN_0
DMI_RXN1 AR20 DMI_RXN_1
DMI_RXN2 AP17 DMI_RXN_2
DMI_RXN3 AV20 DMI_RXN_3
DMI_RXP0 AY22 DMI_RXP_0
DMI_RXP1 AP20 DMI_RXP_1
DMI_RXP2 AR17 DMI_RXP_2
DMI_RXP3 AW20 DMI_RXP_3
DMI_TXN0 BD21 DMI_TXN_0
DMI_TXN1 BE20 DMI_TXN_1
DMI_TXN2 BD17 DMI_TXN_2
DMI_TXN3 BE18 DMI_TXN_3
DMI_TXP0 BB21 DMI_TXP_0
DMI_TXP1 BC20 DMI_TXP_1
DMI_TXP2 BB17 DMI_TXP_2
DMI_TXP3 BC18 DMI_TXP_3
+1_5VRUN
BE16 DMI_IREF
R358 7.5KR1%0402 DMI_COMP_R AY17 DMI_RCOMP
AW17 TP12
AV17 TP7

DMI

FDI_RXN_0 AJ35
FDI_RXN_1 AL35
FDI_RXP_0 AJ36
FDI_RXP_1 AL36
TP16 AV43
TP5 AY45
TP15 AV45
TP10 AW44
FDI_CSYNC AL39 → FDI_CSYNC 3
FDI_INT AL40 → FDI_INT 3
FDI_IREF AT45
TP17 AU42
TP13 AU44
FDI_RCOMP AR44

FDI

2014.3.2 NON AMT
non-AMT R793 stuff
ANT
R793 unstuff

EC_PCH_PWROK
R412 X_0R0402
R411 10KR1%0402
GND

EC delay 99ms

20140306 modify

VIA_SUSACK# R6 SUSACK#
PM_SYSRST# AM1 SYS_RESET# ← 34 PM_SYSRST#
SYS_PWROK AD7 SYS_PWROK
F10 PWROK
45 PM_MPWROK AB7 APWROK
3 PM_DRAM_PWRGD H3 DRAMPWROK
34 RSMRST# J2 RSMRST#
34 SUSPWRACK J4 SUSWARN#/SUSPWRNACK/GPIO30
34 PM_PWRBTN# K1 PWRBTN#
34 AC_PRESENT E6 ACPRESENT/GPIO31
PM_BATLOW# K7 BATLOW#/GPIO72
PM_RI# N4 RI#
AB10 TP21
44 SLP_WLAN# D2 SLP_WLAN#/GPIO29

System Power Management

DSWVRMEN C8 DSWVRMEN R77 330KR0402 RTCVCC
DPWROK L13 RSMRST#
WAKE# K3 PCIE_WAKE# → PCIE_WAKE# 36,41,44,64
CLKRUN# AN7 PM_CLKRUN# R417 X_0R1%0402 EC_CLKRUN# 34
SUS_STAT#/GPIO61 U7
SUSCLK/GPIO62 Y6 SUSCLK R409 22R0402 EC_SUSCLK 34
SLP_S5#/GPIO63 Y7 VIA_PM_SLP_S5# 34,64 R408 X_22R0402 WLAN_SUSCLK 44
SLP_S4# C6 PM_SLP_S4# 34,49
SLP_S3# H1 PM_SLP_S3# 34,49,64
SLP_A# F3 SLP_M# 34,45
SLP_SUS# F1
PMSYNCH AY3 H_PM_SYNC 3
SLP_LAN# G5 SLP_LAN# 41,50

unstuff 0B
20140127 add
20140127 add

4 OF 11

APWROK not supporting Intel AMT , it can be connected to PWROK
GPIO31 : If not used,require pull up +3VSUS
DSWVRMEN - On Die DSW VR Enable HIGH : Enable internal 1.05V regulator LOW : Disable
DPWROK Without deep s4/s5 support tied together with RSMRST#

GPIO Setting : Ref 486708_LPT_EDS Section2.18

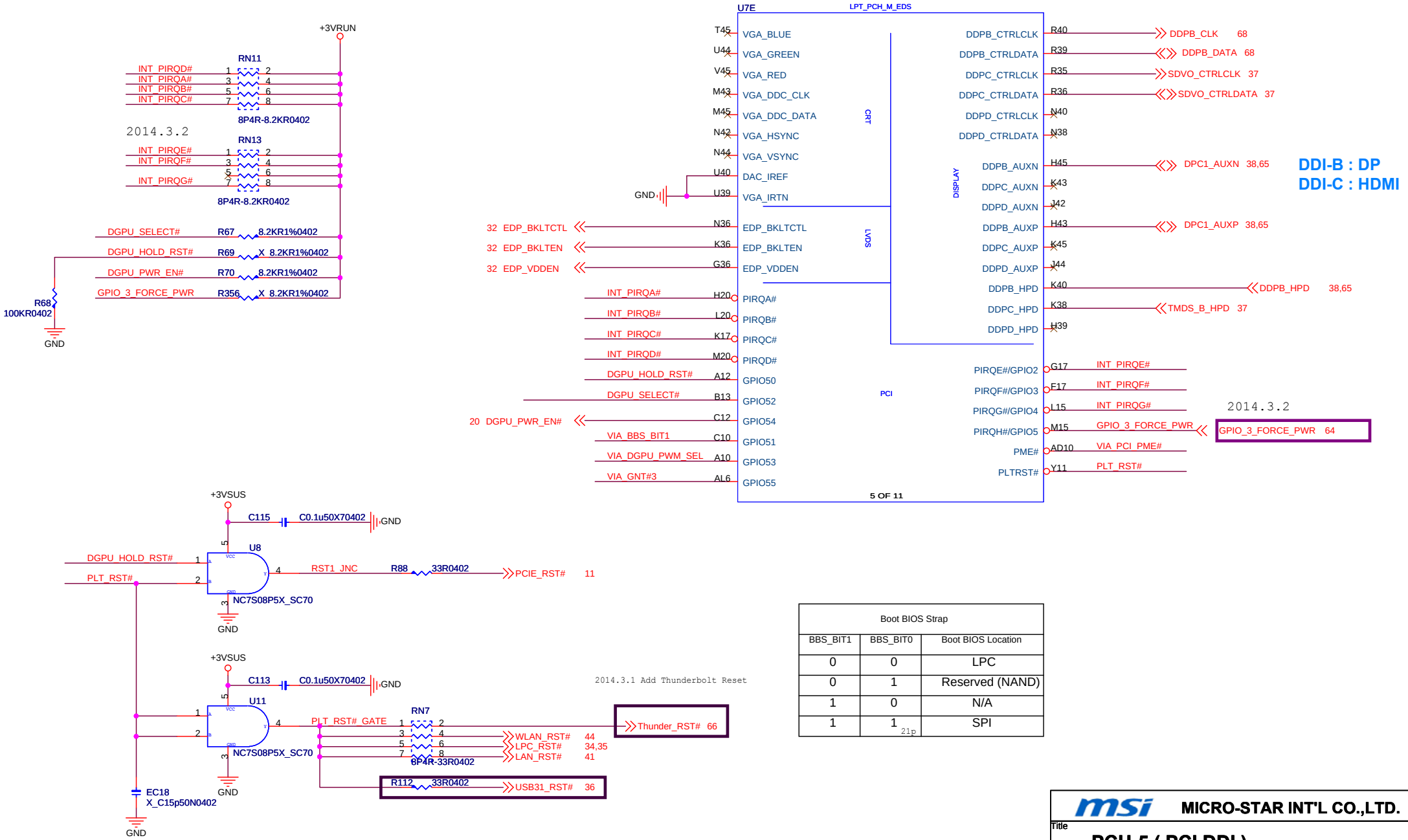
PLL ON DIE VR_ENABLE	
GPIO62	Internal pull high (Enable)
	Low: Disable

+3VSUS
C608 C0.1u50X70402 GND
53 CPU_PWROK
6,34 EC_PCH_PWROK
U32 NC7S08P5X_SC70
SYS_PWROK
EC55 X_C15p50N0402 GND
EC56 X_C15p50N0402 GND

MICRO-STAR INT'L CO.,LTD.

Title: PCH-4 (DMI,FDI)
Size: Document Number: MS-16H3 Rev: 0B
Date: Tuesday, May 20, 2014 Sheet 25 of 69

Lynx Point (PCI,DDI)



Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	N/A
1	1	SPI

21p

MICRO-STAR INT'L CO.,LTD.

Title: PCH-5 (PCI,DDI)

Size | Document Number: MS-16H3 | Rev: 0B

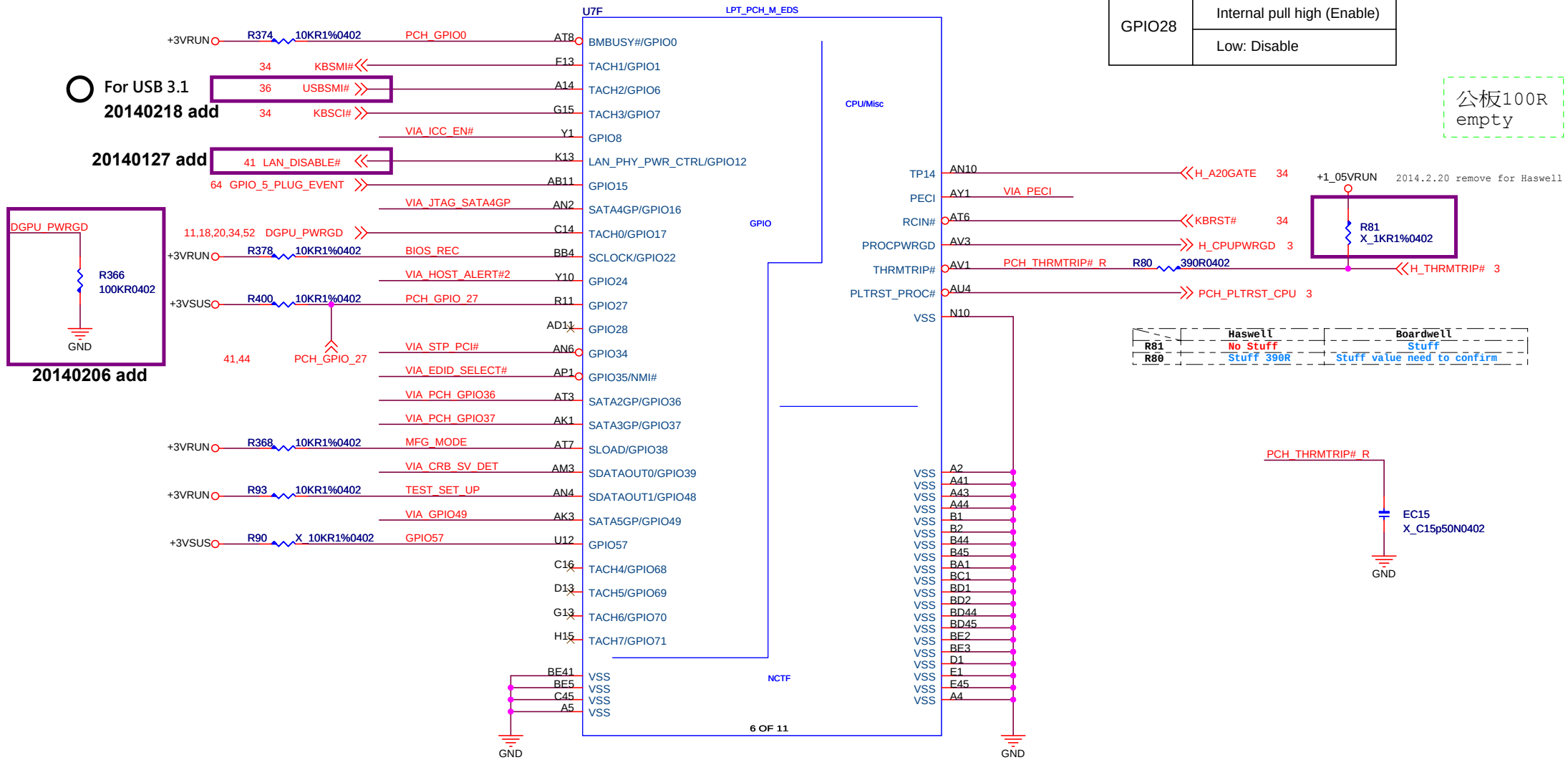
Date: Tuesday, May 20, 2014 | Sheet 26 of 69

Lynx Point (GPIO,MISC)

GPIO Setting : Ref 486708_LPT_EDS Section2.24

PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable)
	Low: Disable

公板100R empty

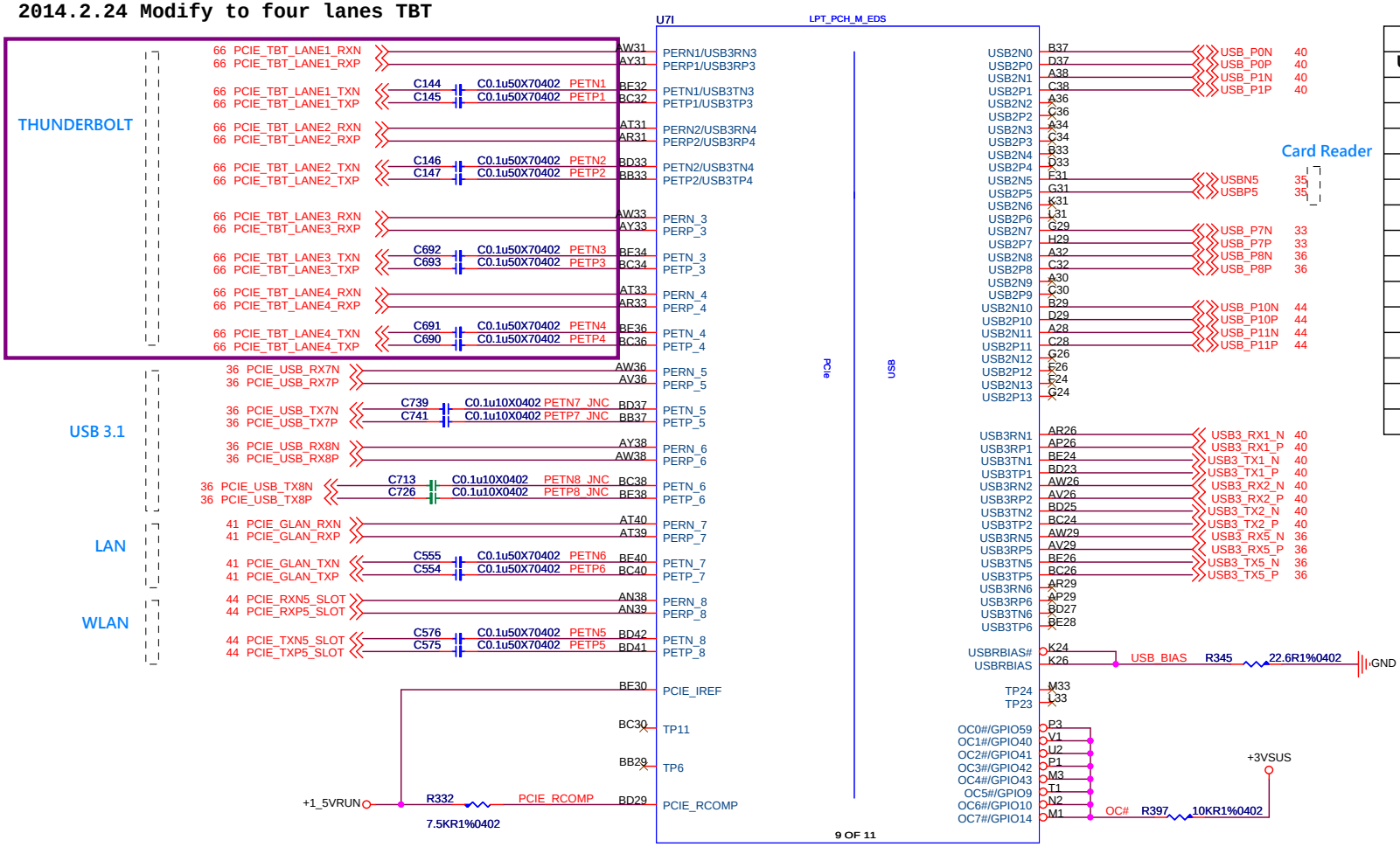


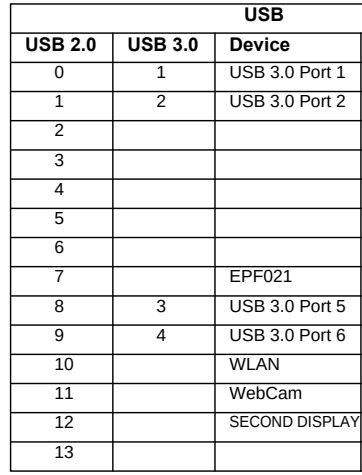
MSI	MICRO-STAR INT'L CO.,LTD.	
Title	PCH-6 (GPIO,MISC)	
Size	Document Number MS-16H3	Rev 0B
Date: Tuesday, May 20, 2014	Sheet 27 of 69	

Lynx Point (PCIE,USB)

Intel Lynx Point ECHI USB(2.0) debug transport 需接Port1 or Port9

2014.2.24 Modify to four lanes TBT





HM86 沒USB3.0 PORT 5,6

USB			
USB 2.0	USB 3.0	Device	Note
0	1	USB 3.0 Port 1	16H3A
1	2	USB 3.0 Port 2	16H3A
2			
3			NC
4			NC
5			NC
6			NC
7		EPF021	3 色KBC
8	3	USB 3.0 Port 5	16H31
9	4	USB 3.0 Port 6	no use
10		WLAN	
11		WebCam	
12		SECOND DISPLAY	
13			NC

MICRO-STAR INT'L CO.,LTD.

Title: PCH-7 (PCIE,USB)

Size | Document Number: MS-16H3 | Rev: 0B

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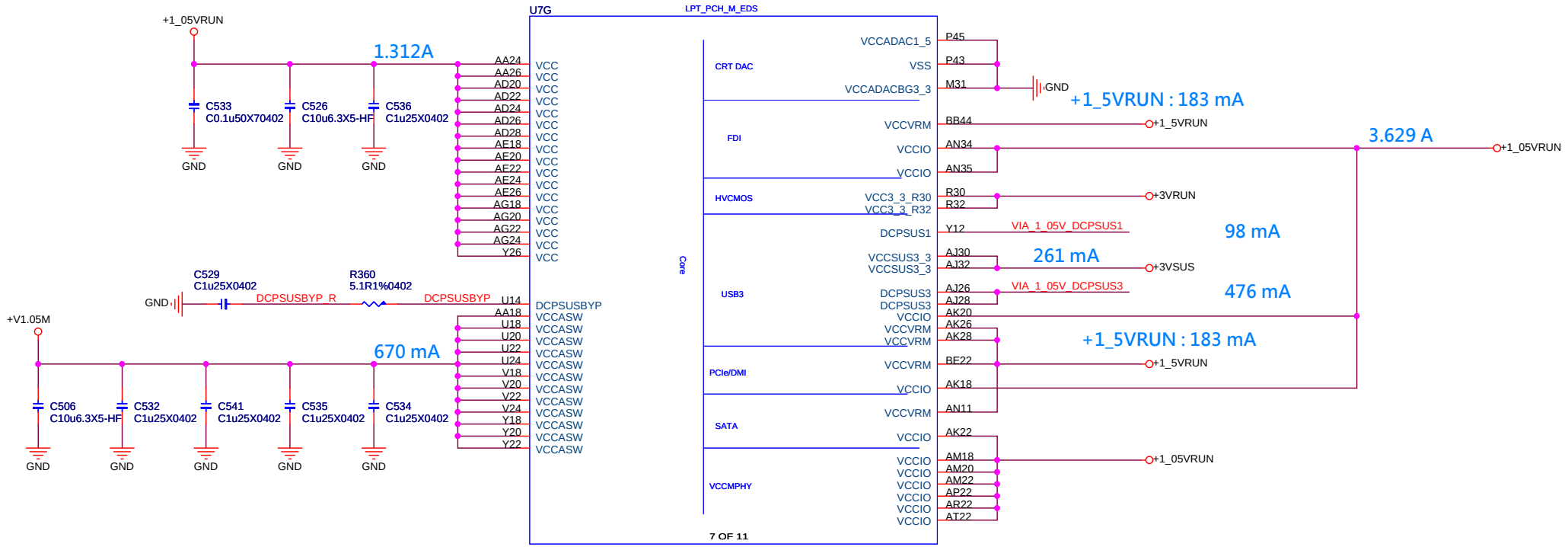
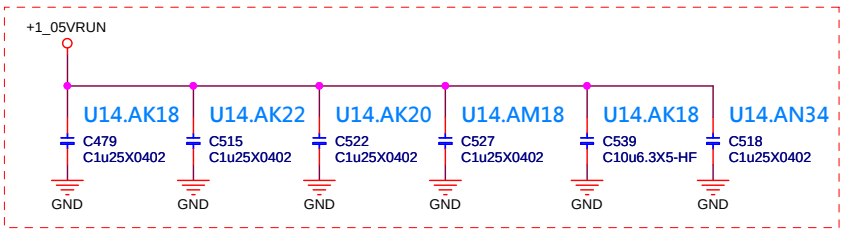
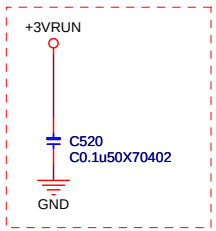
Lynx Point (Power)







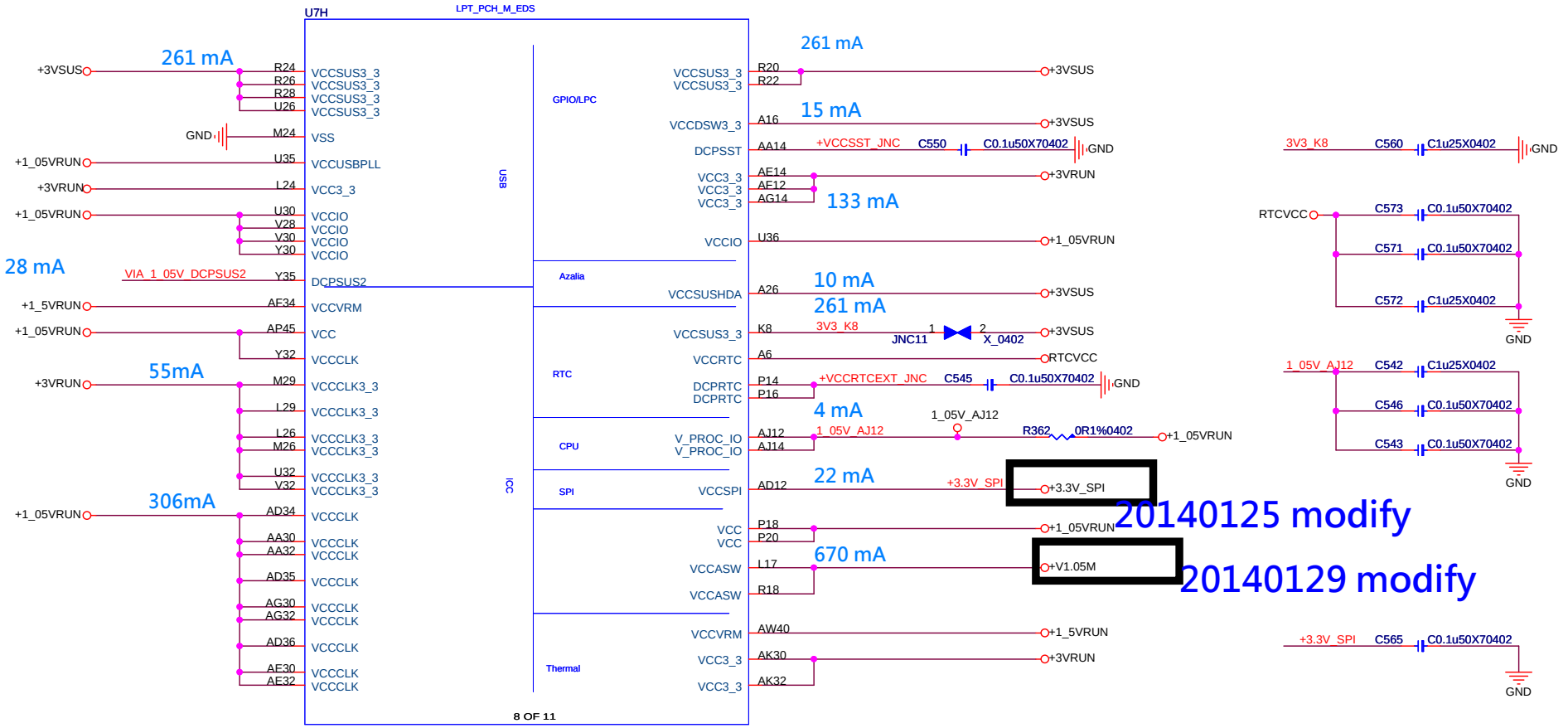
MICRO-STAR INT'L CO.,LTD.

Title: PCH-8 (Power)

Size | Document Number: MS-16H3 | Rev: 0B

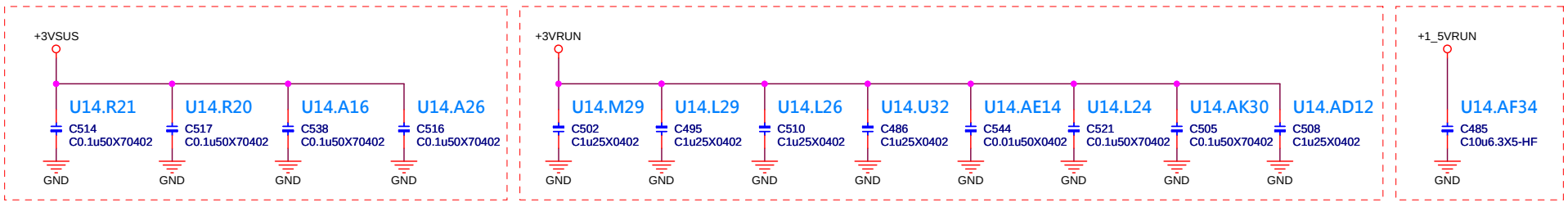
Date: Tuesday, May 20, 2014 | Sheet 29 of 69

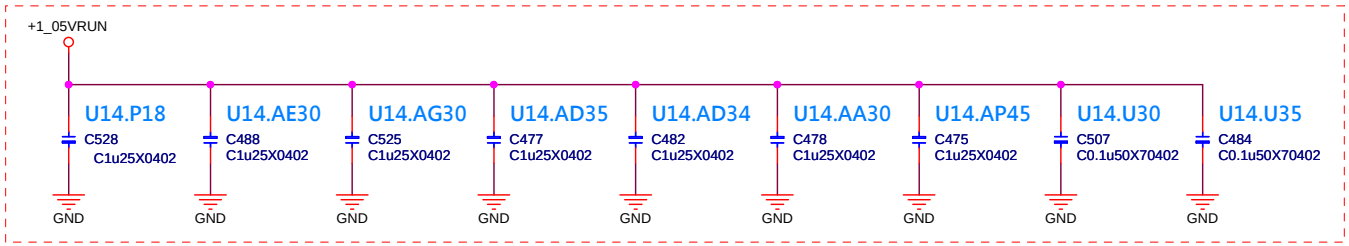
Lynx Point (Power)



20140125 modify

20140129 modify





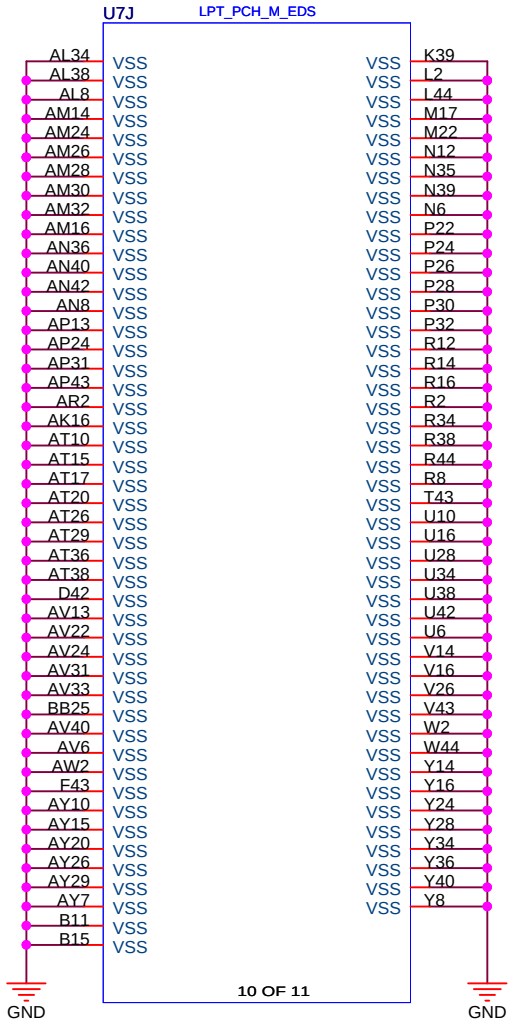
MICRO-STAR INT'L CO.,LTD.

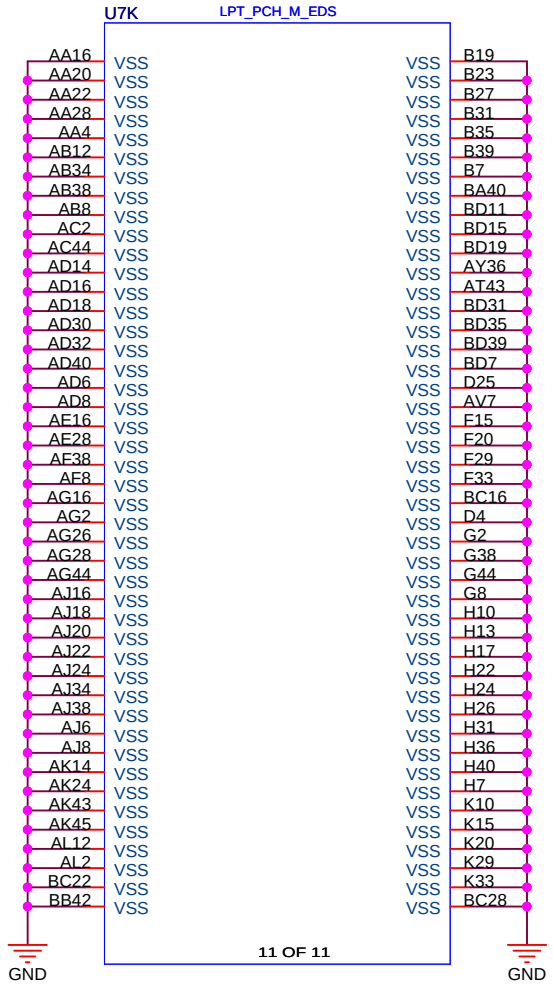
Title: PCH-8 (Power)

Size | Document Number: MS-16H3 | Rev: 0B

Date: Tuesday, May 20, 2014 | Sheet 30 of 69

Lynx Point (GND)





MICRO-STAR INT'L CO.,LTD.		
Title: PCH-8 (GND)		
Size	Document Number: MS-16H3	Rev: 0B
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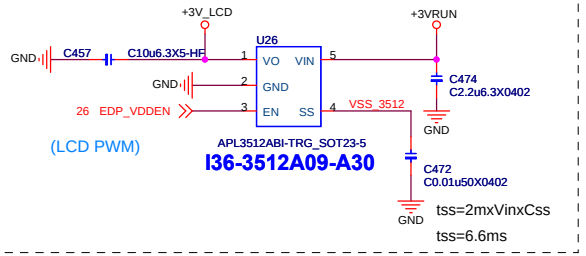
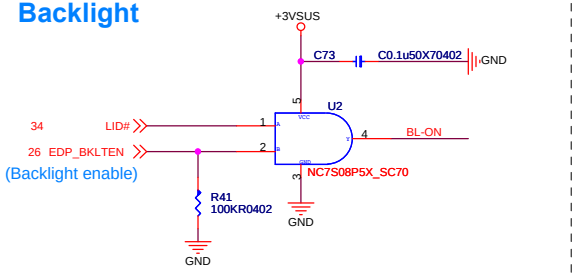
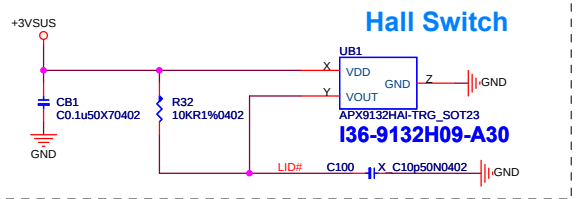
Pannel Device Logic Power



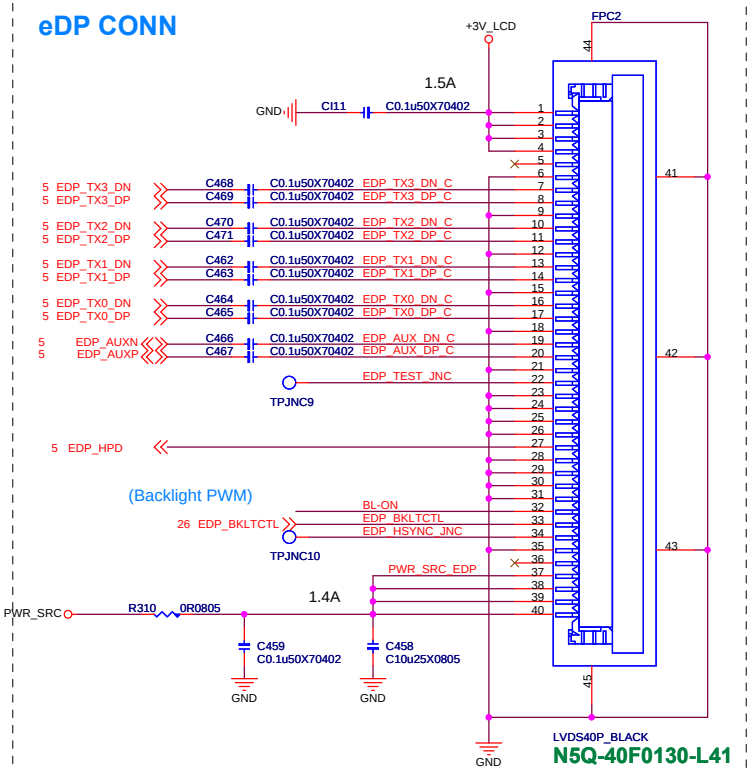
Backlight



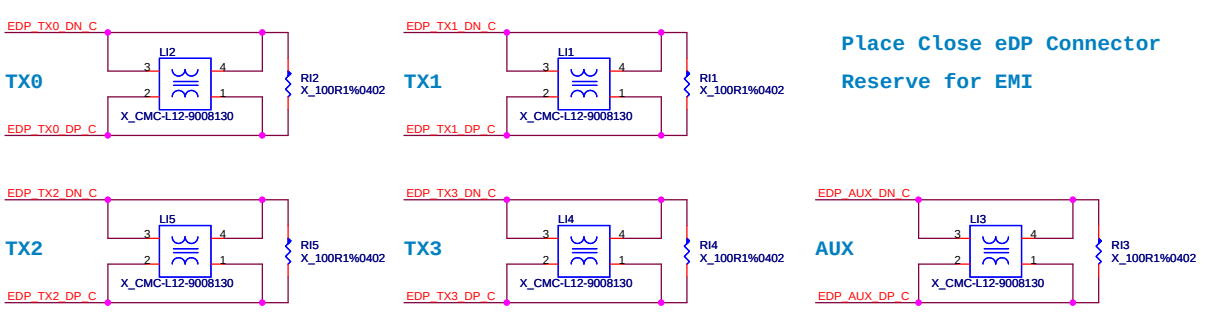
Hall Switch



eDP CONN



20140506 add for RF



Place Close eDP Connector

Reserve for EMI

LCD Module Pin Define

Pin No	Symbol	Description
1	WP	EEPROM Write Protect(Keep open)
2	H_GND	High Speed Ground(0V)
3	eDP_Rx_3N	Complement Signal Link Lane 3
4	eDP_Rx_3P	True Signal Link Lane 3
5	H_GND	High Speed Ground(0V)
6	eDP_Rx_2N	Complement Signal Link Lane 2
7	eDP_Rx_2P	True Signal Link Lane 2
8	H_GND	H_GND
9	eDP_Rx_1N	Complement Signal Link Lane 1
10	eDP_Rx_1P	True Signal Link Lane 1
11	H_GND	H_GND
12	eDP_Rx_0N	Complement Signal Link Lane 0
13	eDP_Rx_0P	True Signal Link Lane 0
14	H_GND	H_GND
15	eDP_AUX_CH_P	True Signal Aux Channel
16	eDP_AUX_CH_N	Complement Signal Aux Channel
17	H_GND	H_GND
18	LCD_VCC	LCD logic and driver power
19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	TEST	LCD Test Port
23	LCD_GND	LCD logic and driver ground(0V)
24	LCD_GND	LCD logic and driver ground(0V)
25	LCD_GND	LCD logic and driver ground(0V)
26	LCD_GND	LCD logic and driver ground(0V)
27	eDP_HPD	HPD signal pin
28	BL_GND	Backlight ground(0V)
29	BL_GND	Backlight ground(0V)
30	BL_GND	Backlight ground(0V)
31	BL_GND	Backlight ground(0V)
32	BL_ENABLE	Backlight enable
33	BL_PWM_DIM	System PWM signal input
34	SDA	I2C-bus Data
35	SCL	I2C-bus Clock
36	BL_PWR	Backlight power (5~21V)
37	BL_PWR	Backlight power (5~21V)
38	BL_PWR	Backlight power (5~21V)
39	BL_PWR	Backlight power (5~21V)
40	HSYNC	HSYNC output from Tcon

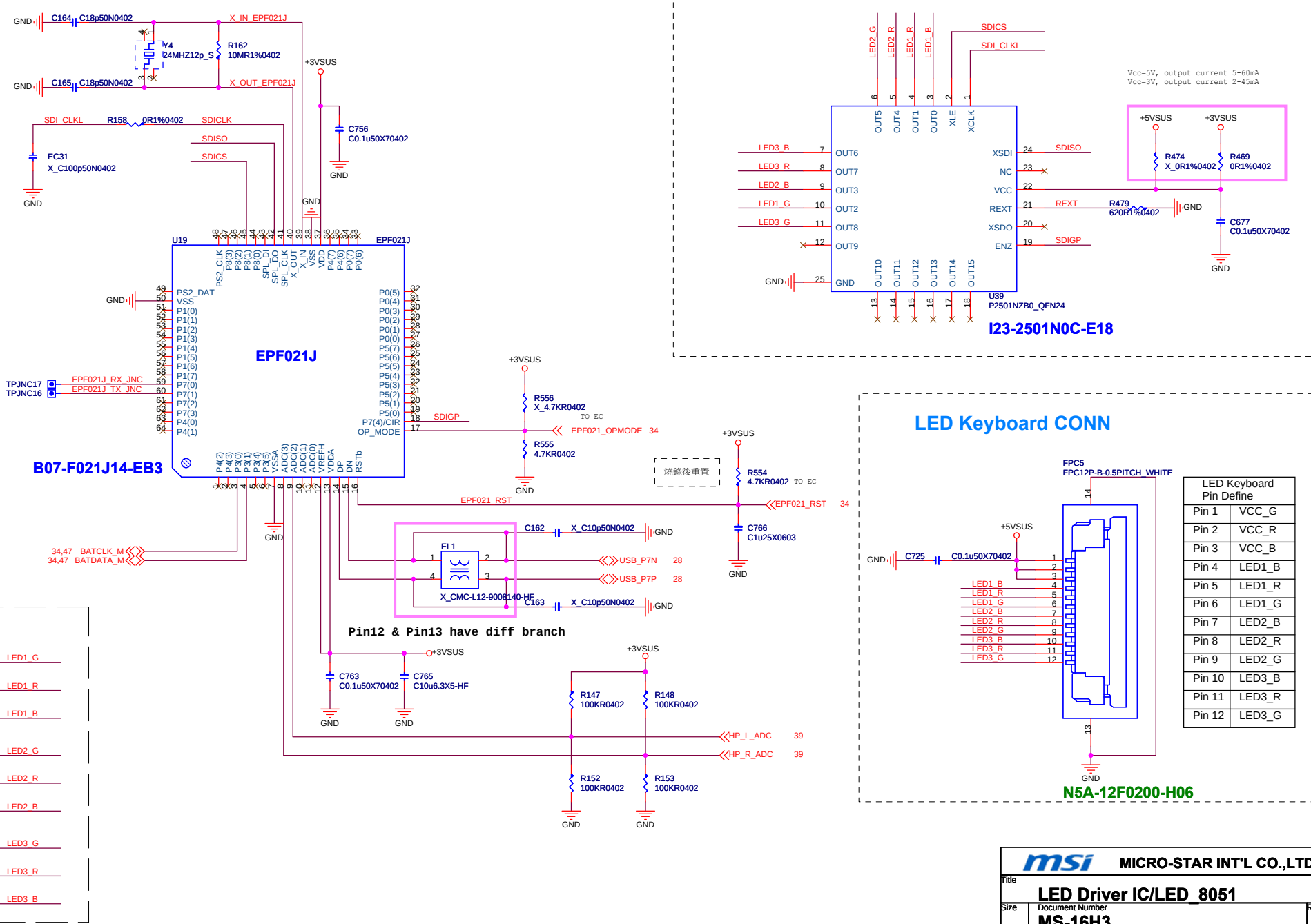
MICRO-STAR INT'L CO.,LTD.

Title: eDP switch & Conn/CAM/Lid

Size: Custom | Document Number: MS-16H3 | Rev: 0B

Date: Tuesday, May 20, 2014 | Sheet 32 of 69

LED 8051 Controller



LED Keyboard Pin Define	
Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G

MICRO-STAR INT'L CO.,LTD.

Title: LED Driver IC/LED_8051

Size | Document Number: MS-16H3 | Rev: 0B

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KBC(KB3930QFB1)

Hardware Reset

ED before RC

RC and R Close SW

SW-TACTB1-4PS5

N71-0100560-D02

SW Debug (LPC)

BH1X14#S-1PITCH

N32-1140130-H06

Keyboard conn

CON6 FPC26P-B-1PITCH_BLACK

N5A-26F0340-H06

2014.3.2 DELETE, then add it.

Pin 105-108 8mA-16mA Sink

2014.2.7 新增

Pin 92 16mA-20mA Sink

Pin 39,91 16mA-20mA Sink

2014.3.3 add

MB_ID

MB_ID=1=AMT

MB_ID=0=non-AMT

FLASH/ME DEBUG MODE STRAP

20140311 add

FOR APS TOOL

MP remove

ROM

M31-2551222-M24

ALLSYSPG

3/2 AMT

3/2 non-AMT

PU/PD

KBRST#, H_A20GATE

B02-0393024-E18

Title	KBC(KB3930QFB1)
Size	Document Number: MS-16H3
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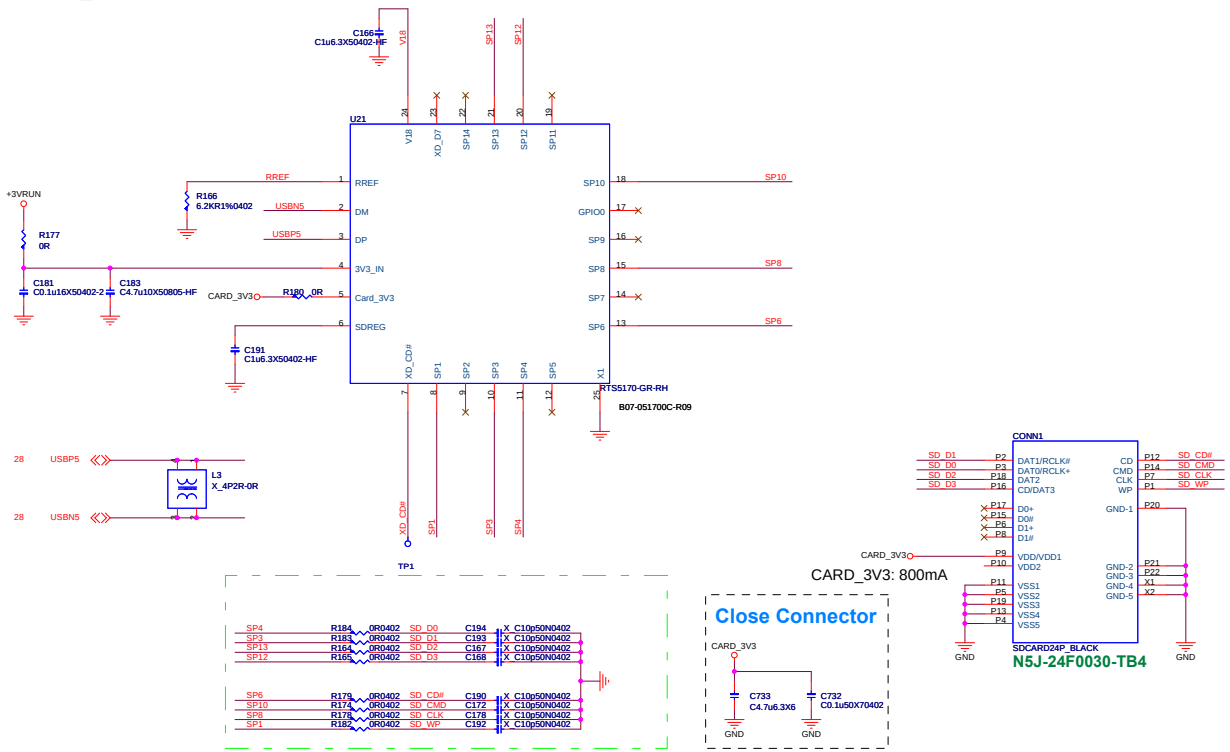
MICRO-STAR INT'L CO.,LTD.

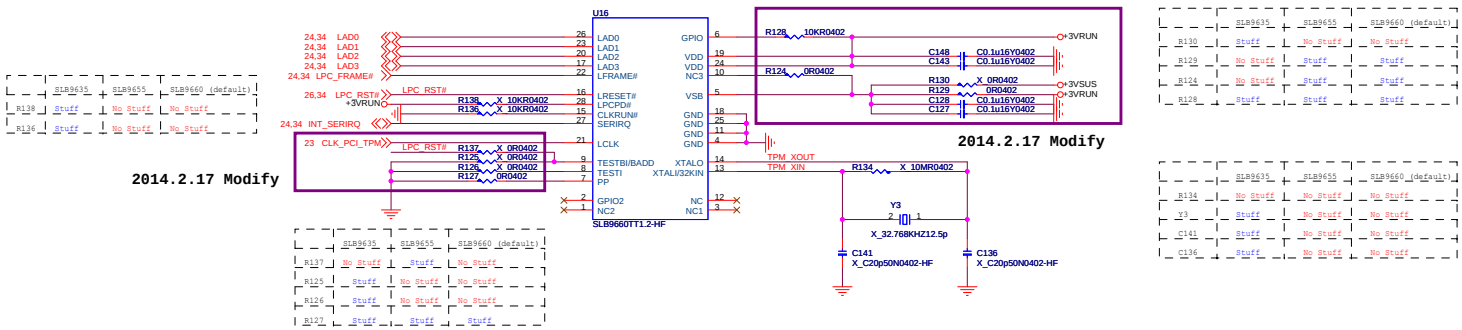
CARD READER_RTS5170



For EMI and Close to RTS5170

Pin#	Name	I/O Type	Description
1	RREF	I	Connect external resistor (6.2K ± 1%) to reference ground
2	DM	I/O	USB D- signal
3	DP	I/O	USB D+ signal
4	3V3_IN	I	3.3V power input
5	CARD_3V3	O	3.3V power for all cards
6	SDREG	O	Internal regulator for SD card. An external capacitor should be connected
7	XD_CD#	I	xD Card Detect (xD_CD#)
8	SP1	I/O	xD Ready Signal (xD_RDY), SD Write Protect (SD WP) and MS Clock (MS_CLK)
9	SP2	I/O	xD RE# and MS Card Detect (MS_INS#)
10	SP3	I/O	xD CE# and SD Data 1 (SD_DAT1)
11	SP4	I/O	xD_CLE, SD Data 0 (SD_DAT0) and MS Data 7 (MS_D7)
12	SP5	I/O	xD ALE, SD Data 7 (SD_DAT7) and MS Data 3 (MS_D3)
13	SP6	I/O	xD_WE# and SD Card Detect (SD_CD#)
14	SP7	I/O	xD Write Protect (xD_WP), SD_Data 6 (SD_DAT6) and MS Data 6 (MS_D6)
15	SP8	I/O	xD Data 0 (xD_D0), SD Clock (SD_CLK) and MS Data 2 (MS_D2)
16	SP9	I/O	xD Data 1 (xD_D1), SD Data 5 (SD_D5) and MS Data 0 (MS_D0)
17	GPIO0	I/O	General purpose input/output with interrupt ability
18	SP10	I/O	xD Data 2 (xD_D2) and SD command signal (SD_CMD)
19	SP11	I/O	xD Data 3 (xD_D3), SD Data 4 (SD_DAT4) and MS Data 4 (MS_D4)
20	SP12	I/O	xD Data 4 (xD_D4), SD Data 3 (SD_DAT3) and MS Data 1 (MS_D1)
21	SP13	I/O	xD Data 5 (xD_D5), SD Data 2 (SD_DAT2) and MS Data 5 (MS_D5)
22	SP14	I/O	xD Data 6 (xD_D6) and MS BS
23	XD_D7	I/O	xD Data 7 (xD_D7)
24	V18	O	Regulated supply voltage (1.8V ±10%) from internal 3.3V to 1.8V regulator; supplies internal digital circuits. An external capacitance should be connected

TPM



MICRO-STAR INT'L CO.,LTD.

Title: Card Reader & TPM

Size: | Document Number: MS-16H3 | Rev: 0B

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USB 3.0 / iCharger

USB3.0 CNT-1
USB3.0 Port-5
USB2.0 Port-8

SPI ROM For FW (stuff first)

M31-2551283-P81
需使用與EC ROM不同的料號上件

For 0A Consumption measure

PCIE to USB 3.1

B02-010422C-AD0

ASM1142

R830 default no stuff

Colay for 1142

Confirm BIOS USB SMI pin for legacy mode used

0.1uF*7

0.1uF*4

0.1uF*2

20140505add

I31-0111A29-U33

If Ipod charger none used, stuff it

I36-5478102-G07

20140312 add

I31-0111A29-U33

For 1142
Close Pin 13

USB 3.1 Port 1

i-Charger

I36-S25460C-T07

All C Close Connector

USB3.0 CNT-1
USB3.0 Port-6
USB2.0 Port-9

USB 3.0 / iCharger

N53-09M0241-AF2

EMI

SSTXSP_C	C202	X_C10p50N0402
SSTXSN_C	C199	X_C10p50N0402
USB_PN8_R	C198	X_C10p50N0402
USB_PP8_R	C197	X_C10p50N0402
USB31_RX2P_JNC	C196	X_C10p50N0402
USB31_RX2N_JNC	C195	X_C10p50N0402

MICRO-STAR INT'L CO.,LTD.

Title: USB 3.0 / iCharger
Size: Document Number: MS-16H3
Rev: 0B
Date: Tuesday, May 20, 2014
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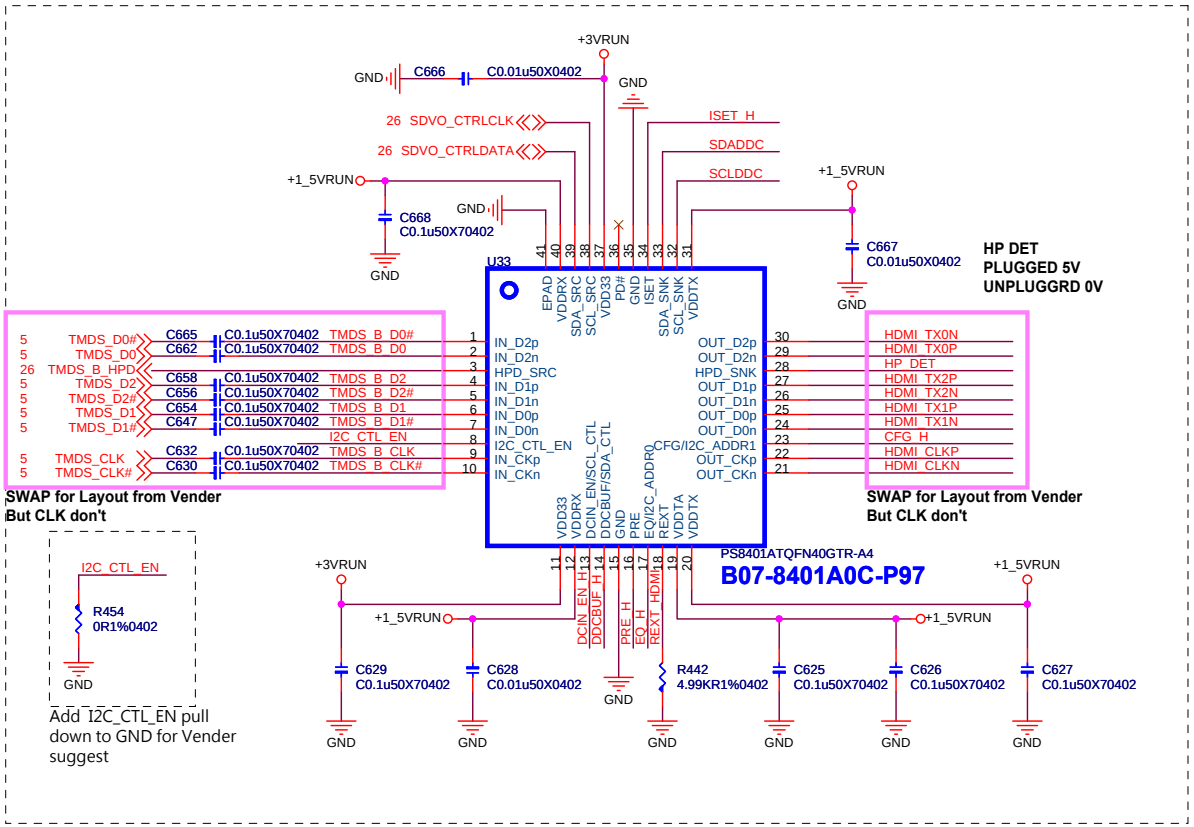
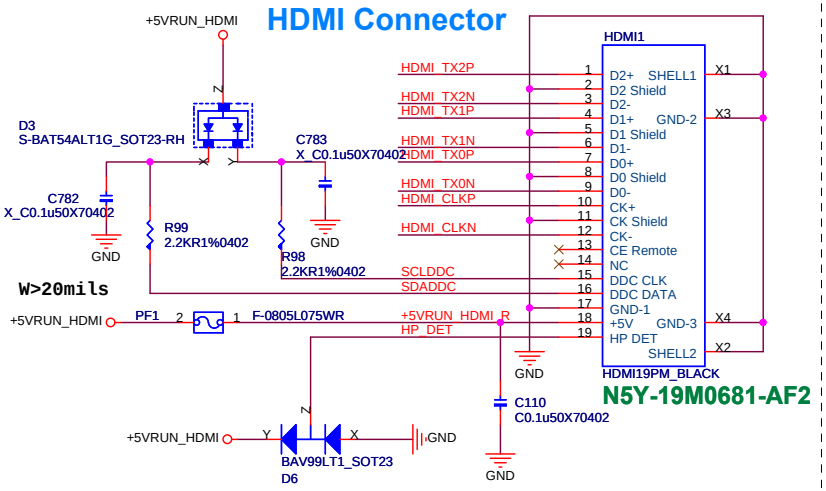
HDMI Repeater



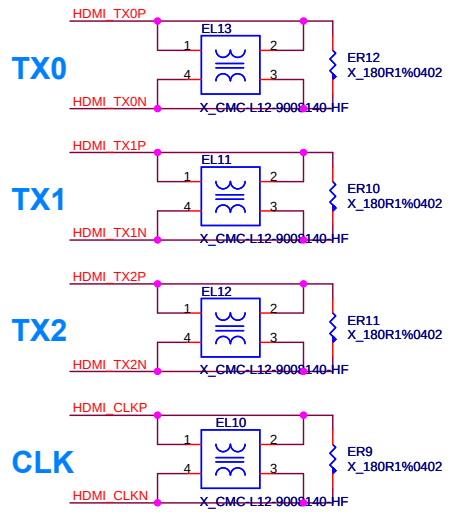
HDMI Connector

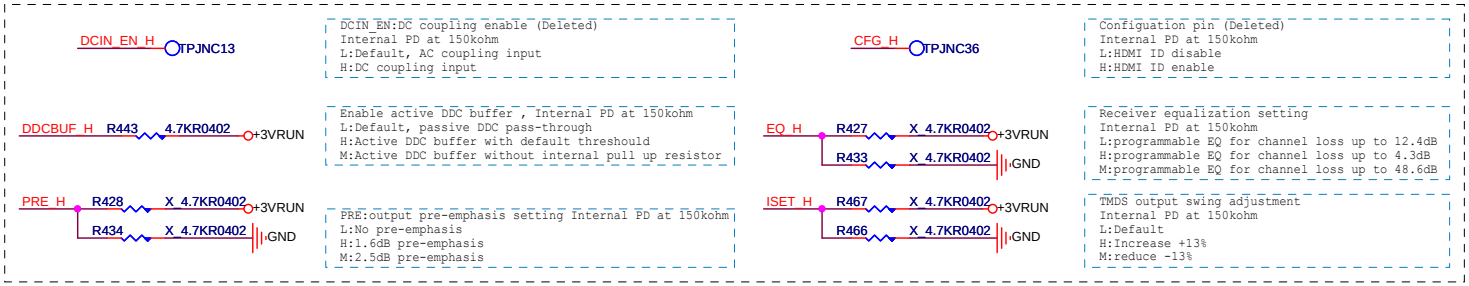


An HDMI Source shall have +5V Power signal over-current protection of no more than 0.5A.

HPD_SNK Internal PD 150kohm

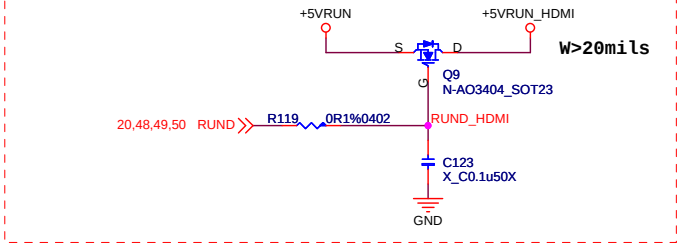
EMI Close Connector





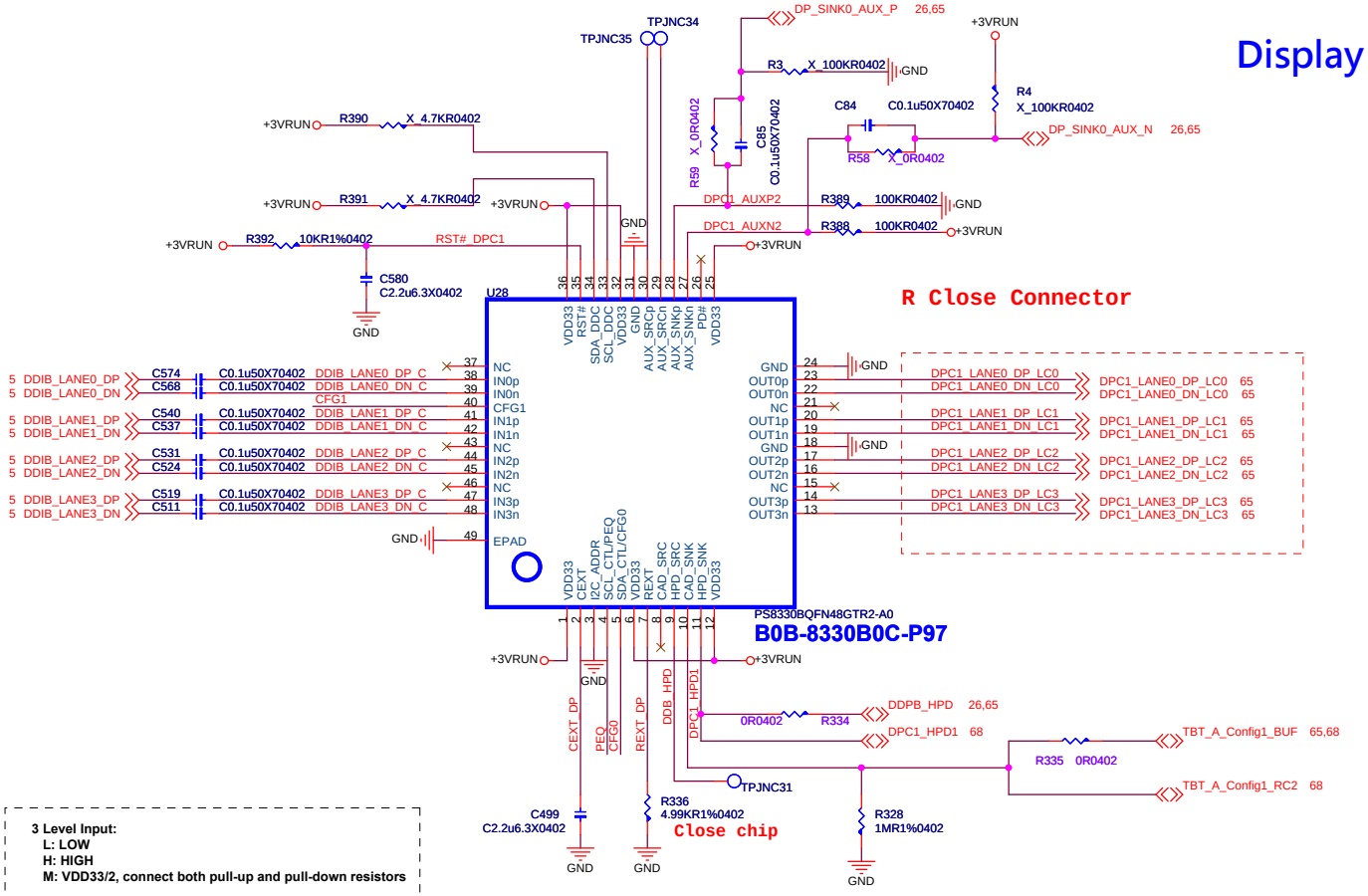
ADDR1 (CFG)	ADDR0 (EQ)	I2C control bus address (Internal pull down at ~150kΩ, 3.3V I/O)
0	0	0x4C / 4D (default)
0	1	0x5C / 5D
1	0	0xCC / CD
1	1	0xEC / ED

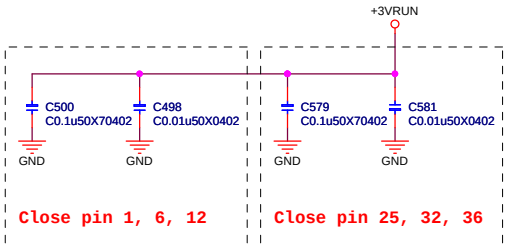
Avoid HDMI Leakage



MSI	MICRO-STAR INT'L CO.,LTD.
Title	HDMI Repeater
Size	Document Number: MS-16H3
Rev	0B
Date:	Tuesday, May 20, 2014
Sheet	37 of 69

Display Port

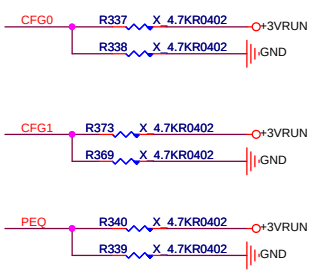




3 Level Input:
L: LOW
H: HIGH
M: VDD33/2, connect both pull-up and pull-down resistors

CAD_SNK Have internal Pull down 1Mohm.

HPD_SNK Have internal Pull down 150kohm.
No problem with Leakage from DP device
The DP_PWR and RETURN pins of the box-to-box connectors must support the maximum current rating of 500mA.

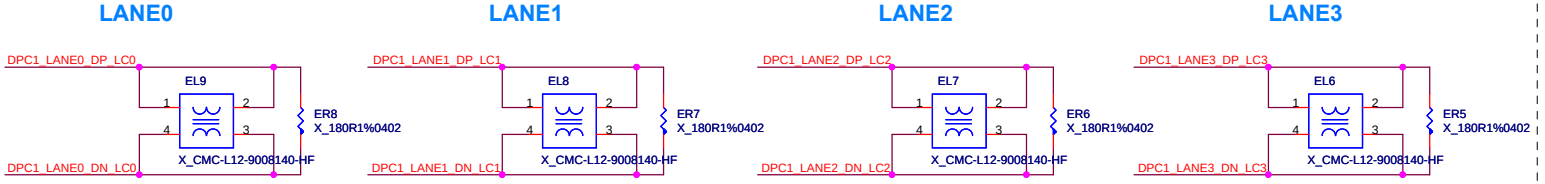


Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150k Ohm, 3.3V I/O.
L: default, automatic EQ enable & AUX interception enable
H: automatic EQ disable & AUX interception enable
M: automatic EQ disable & AUX interception disable, no pre-emphasis, 600mVpp swing

Configuration pin for auto test and input offset cancellation, 3.3V IO, internal pull up at ~150K Ohm
H: default, auto test disable & input offset cancellation enable
L: auto test enable & input offset cancellation enable
M: auto test disable & input offset cancellation disable

Programmable input equalization levels; Internal pull down at ~150k Ohm, 3.3V I/O.
L: default, LEQ, compensate channel loss up to 12dB @ HBR2
H: HEQ, compensate channel loss up to 15dB @ HBR2
M: LLEQ, compensate channel loss up to 5dB @ HBR2

EMI Close Connector



MICRO-STAR INT'L CO.,LTD.

Title: DP witch Repeater

Size: | Document Number: MS-16H3 | Rev: 0B

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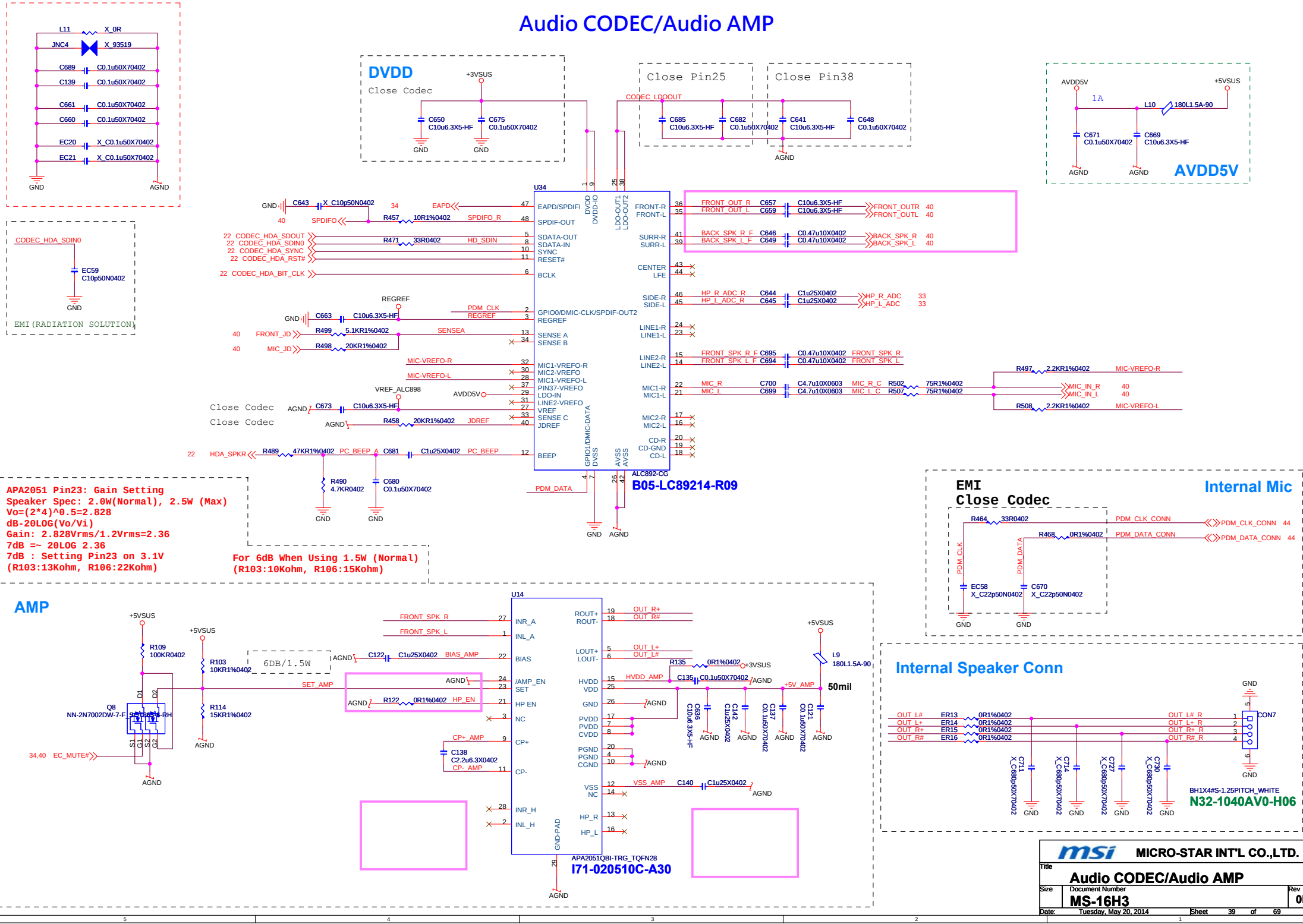
Audio CODEC/Audio AMP



MSI	MICRO-STAR INT'L CO.,LTD.		
Title	Audio CODEC/Audio AMP		
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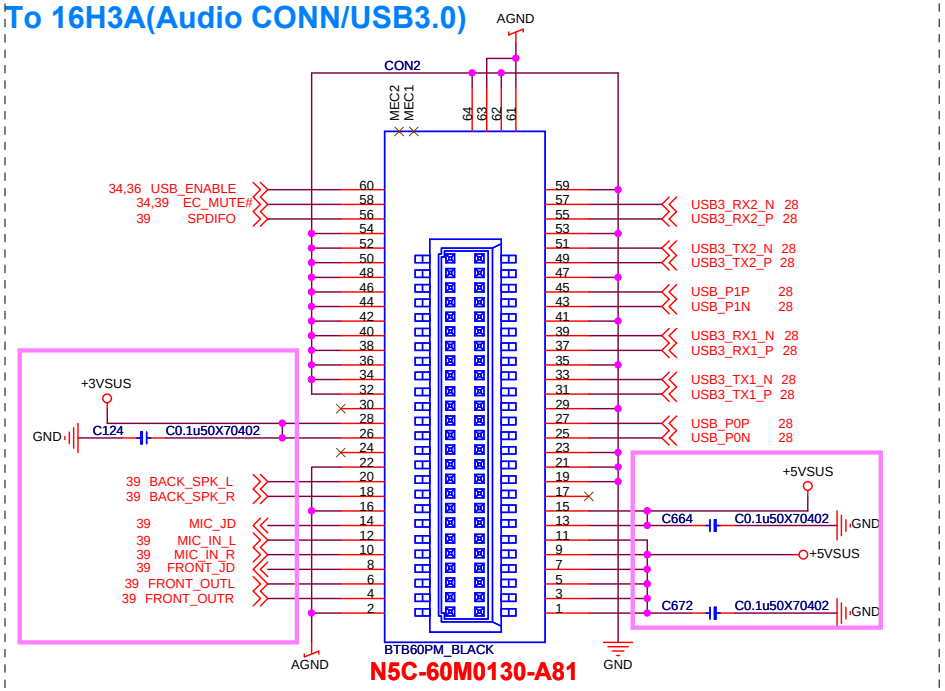
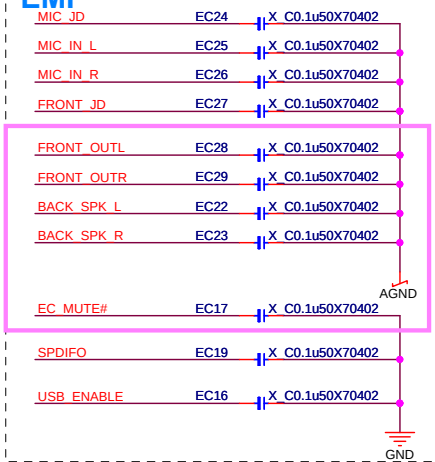
CPU FAN/BTB CONN

To 16H3A(Audio CONN/USB3.0)

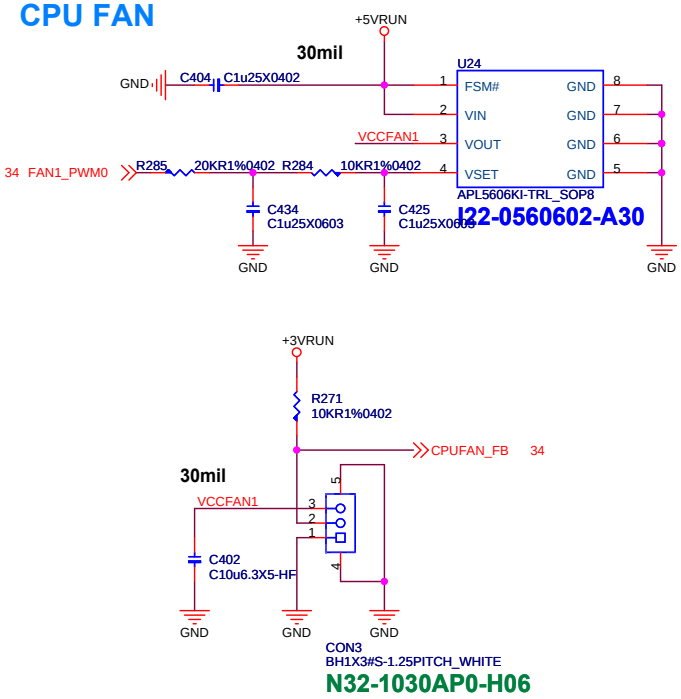


EMI

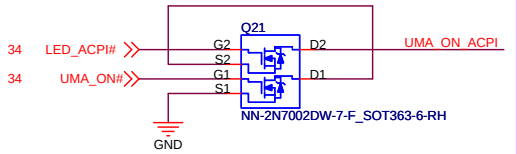


EMI

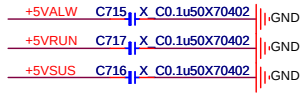
CPU FAN



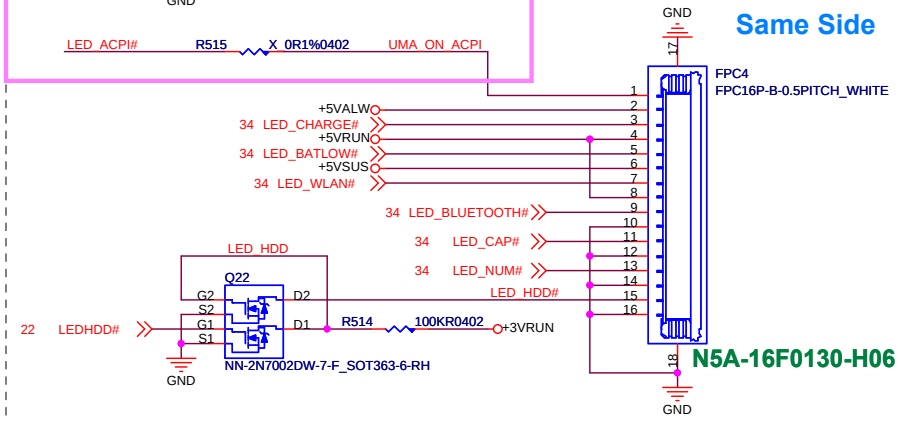
S3 Breath
S0 No active



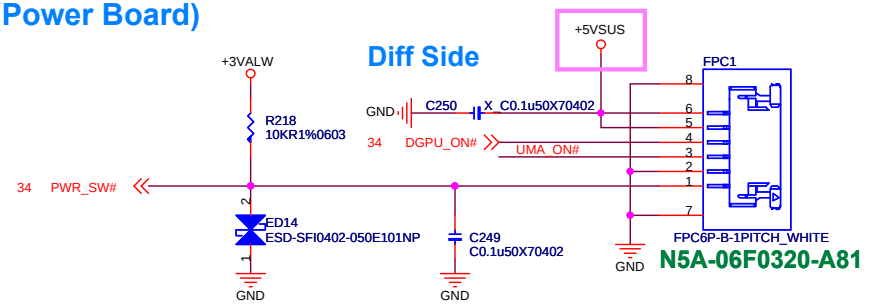
To 16H3B(LED Board)



Same Side



To 16H3C (Power Board)



MICRO-STAR INT'L CO.,LTD.		
Title: CPU FAN/BTB CONN		
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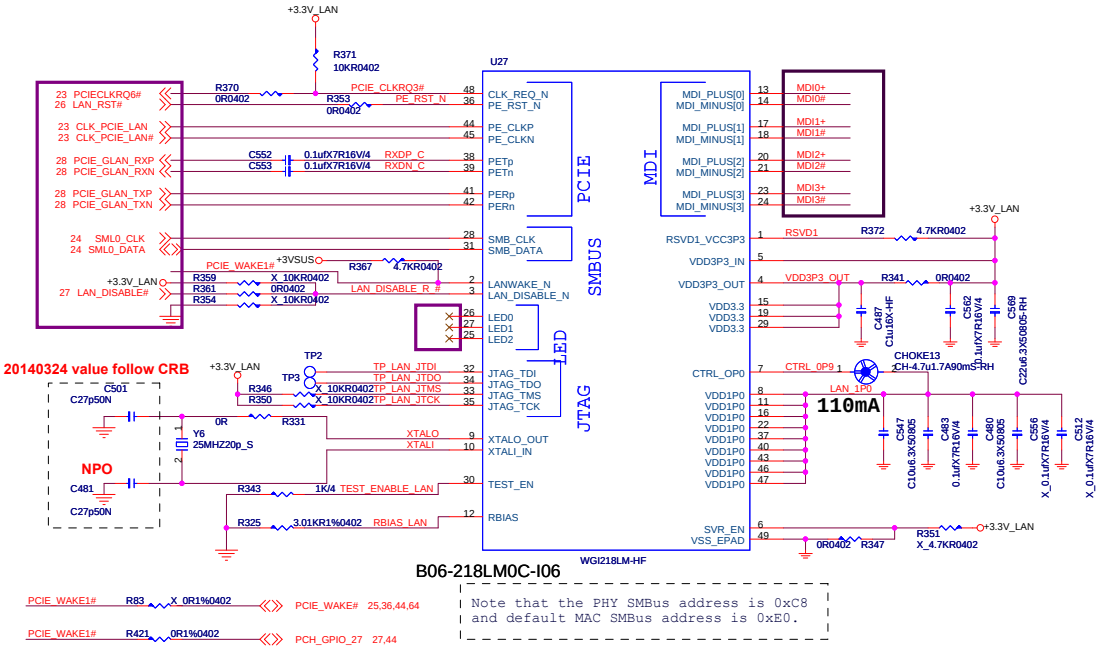
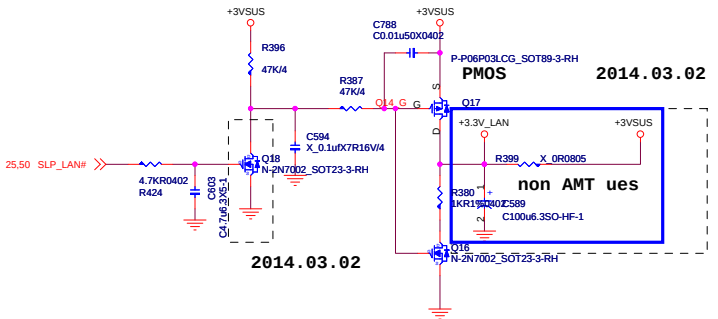
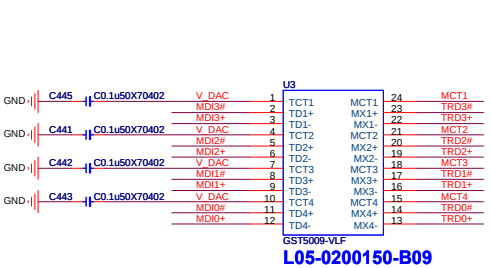
INTEL Clarkville LAN(I218LM)

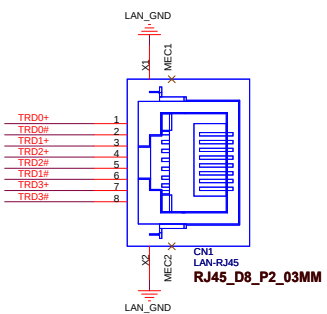


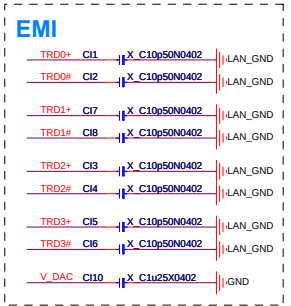
+3.3V_LAN
(132mA)

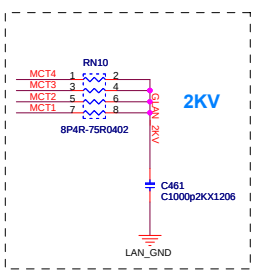


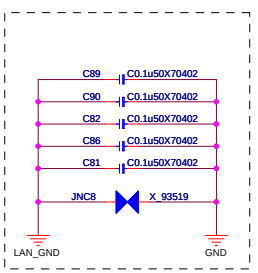
110mA











MSI	MICRO-STAR INT'L CO.,LTD.		
Title	INTEL Clarkville LAN (I218LM)		
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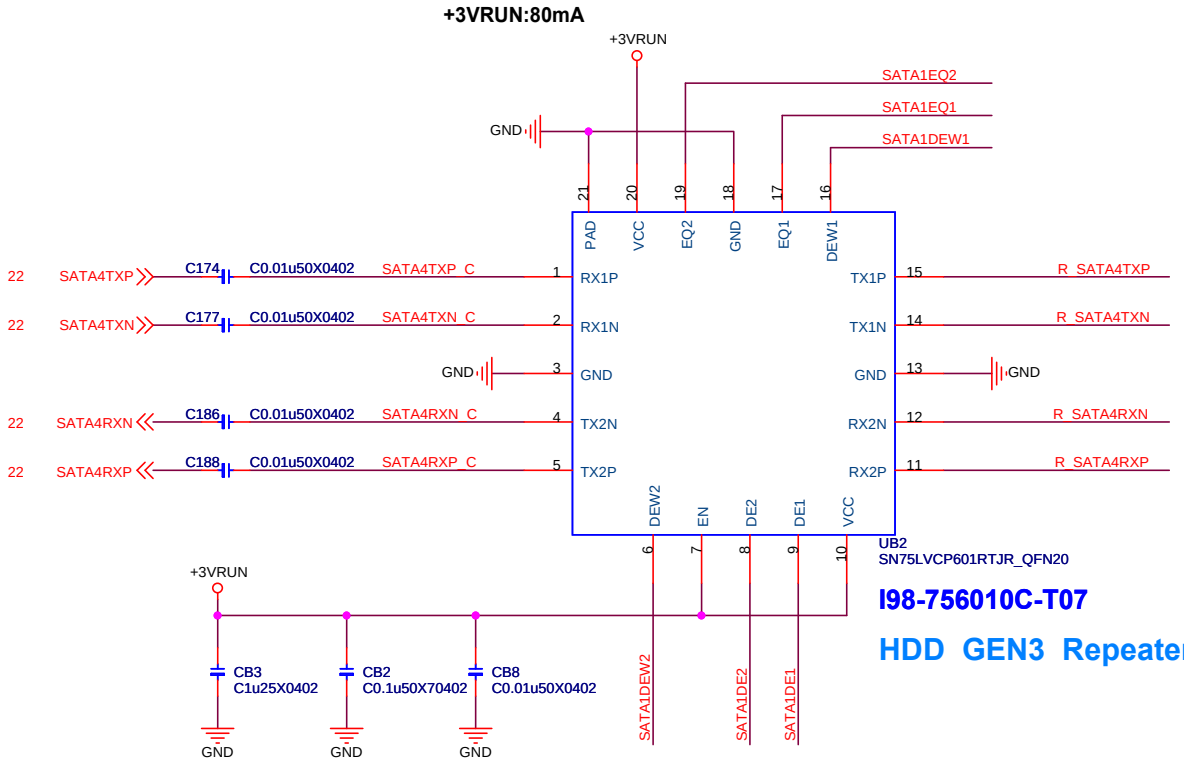
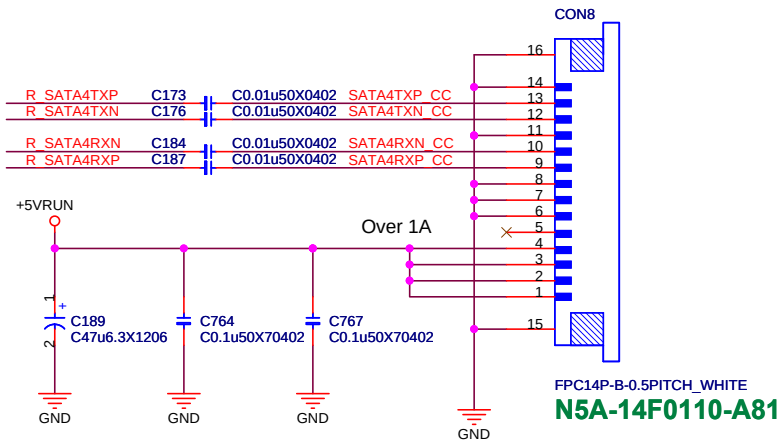
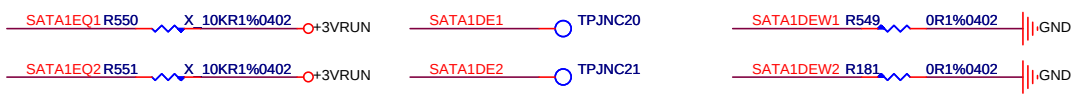
HDD (With Repeater)



BTB Connecter



TI SN75LVCP601RTJR HW Setting



DE1/DE2	CH1/CH2De-Emphasis dB (at 6Gbps)	EQ1/EQ2	CH1/CH2Equalization dB (at 6Gbps)
NC (***default***)	–4	NC (***default***)	0
0	0	0	7
1	–2	1	14

DEW1/DEW2	Device Function → DE Width for CH1/CH2
0	De-emphasis pulse duration, short (recommended setting when link operates at SATA 1.5/3/6 Gbps)
1 (***default***)	De-emphasis pulse duration, long (recommended setting when link operates at SATA 1.5/3 Gbps speed only)

MICRO-STAR INT'L CO.,LTD.

Title: **HDD With Repeater**

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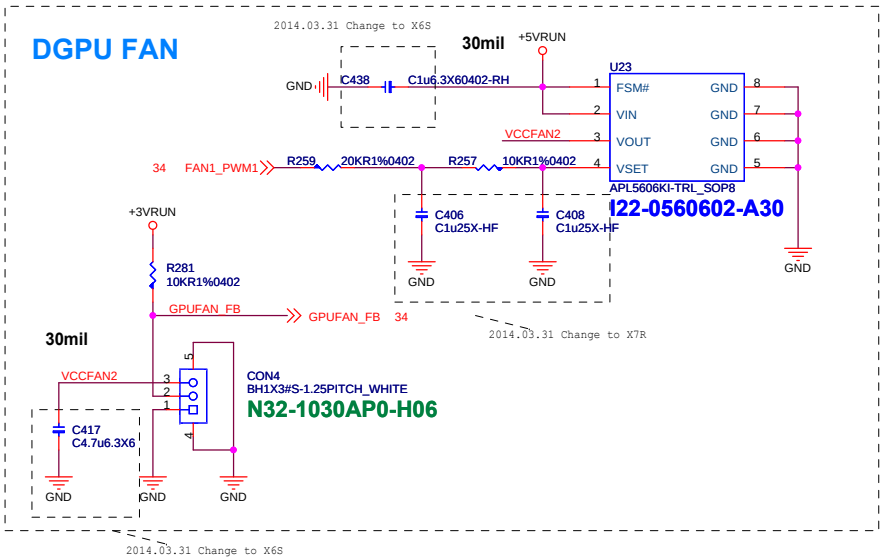
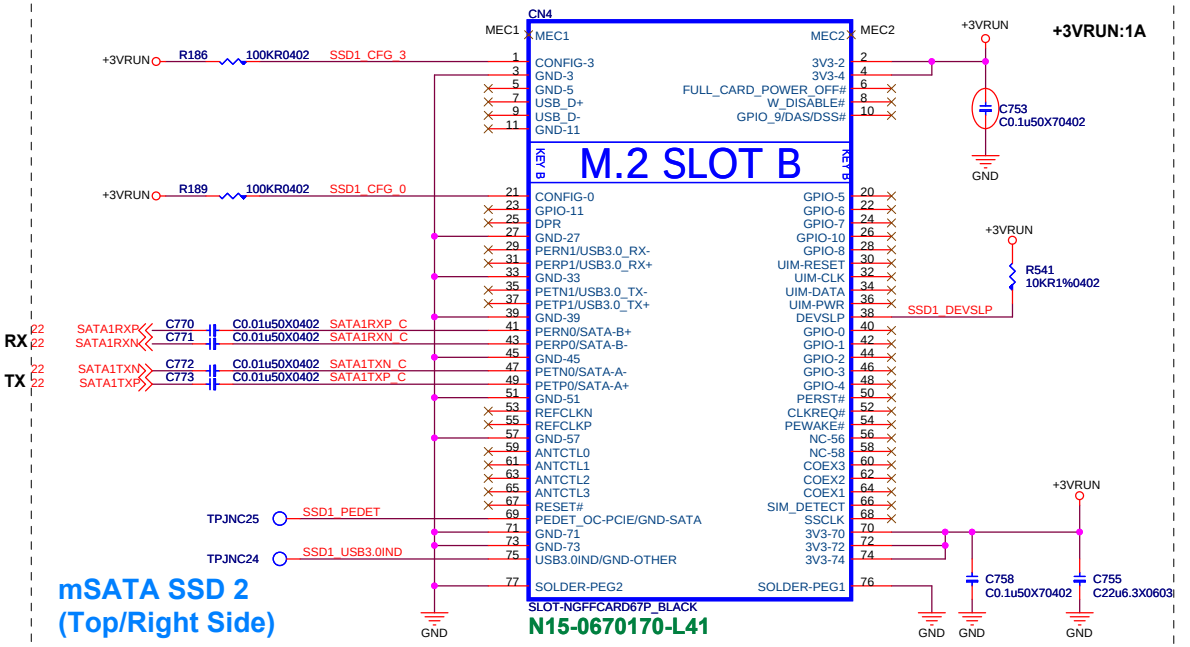
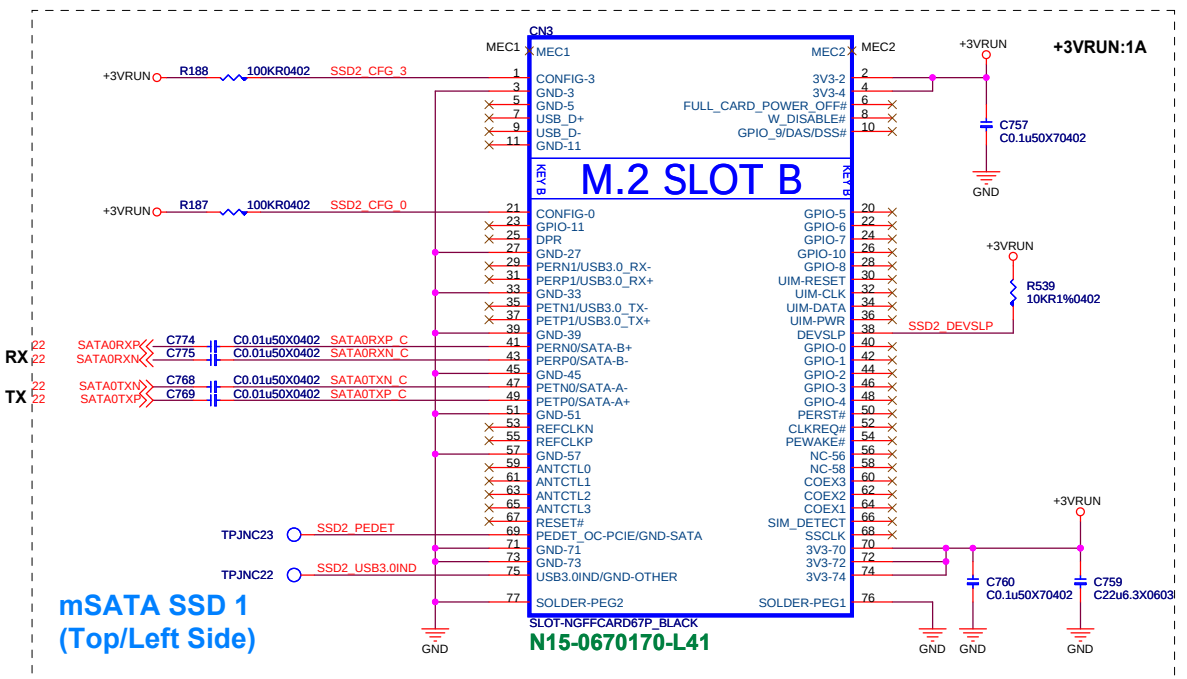
SSD/ DGPU FAN







40	NC	No Connect
41	SATA-B+/PERn0	Host receiver differential signal pair
42	NC	No Connect
43	SATA-B-/PERp0	Host receiver differential signal pair
44	NC	No Connect
45	GND	Ground
46	NC	No Connect
47	SATA-A-/PETn0	Host Transmitter differential signal pair
48	NC	No Connect
49	SATA-A+/PETp0	Host transmitter differential signal pair

MICRO-STAR INT'L CO.,LTD.

Title	SSD/ DGPU FAN	
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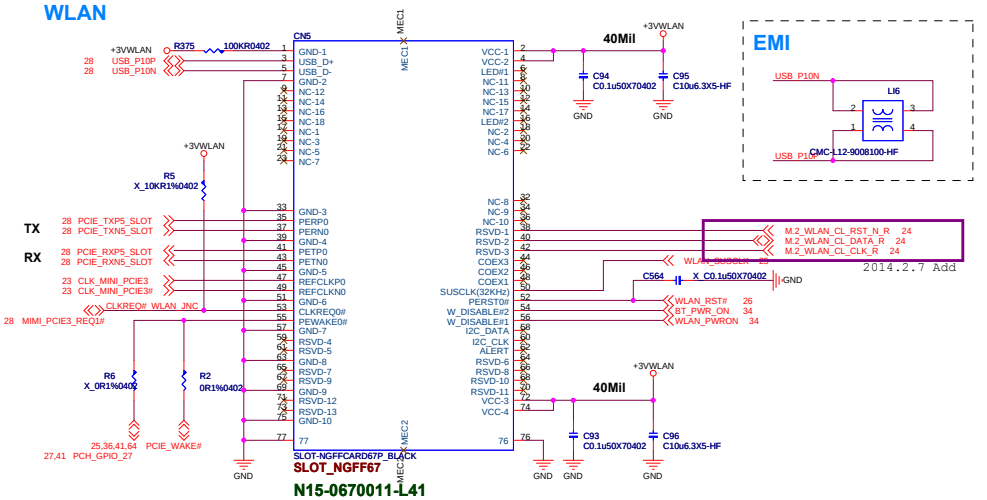
WLAN /Camera/ClickPad/FP

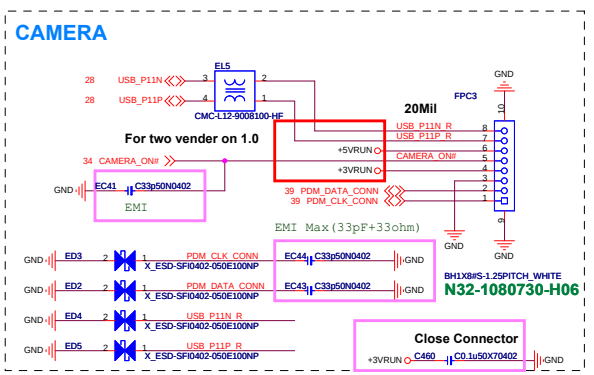
WLAN



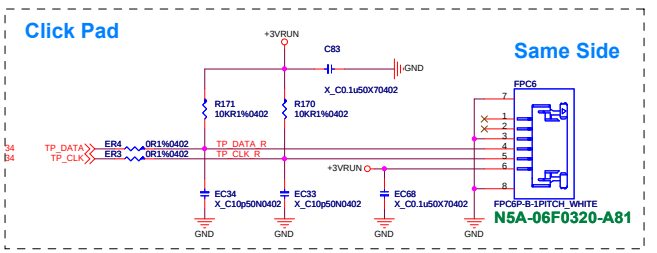
EMI

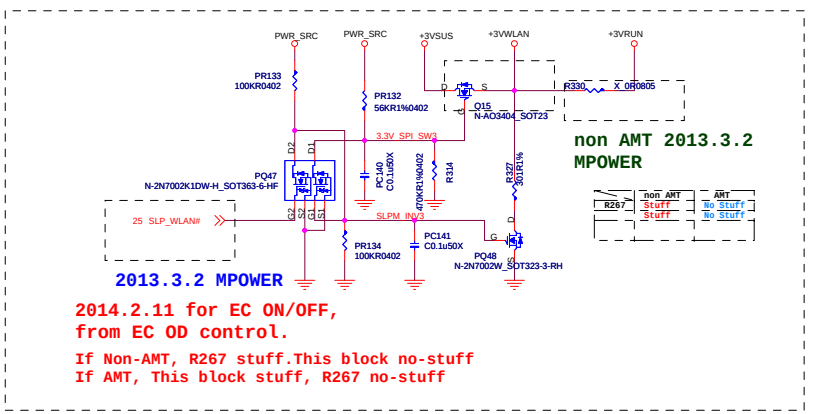
Pin 1	GND		
Pin 3	USB_D+	Pin 2	3.3V
Pin 5	USB_D-	Pin 4	3.3V
Pin 7	GND	Pin 6	LED1#
Pin 9	Module Key	Pin 8	Module Key
Pin 11	Module Key	Pin 10	Module Key
Pin 13	Module Key	Pin 12	Module Key
Pin 15	Module Key	Pin 14	Module Key
Pin 17	N/C	Pin 16	LED2#
Pin 19	N/C	Pin 18	GND
Pin 21	N/C	Pin 20	N/C
Pin 23	N/C	Pin 22	N/C
Pin 25	Module Key	Pin 24	Module Key
Pin 27	Module Key	Pin 26	Module Key
Pin 29	Module Key	Pin 28	Module Key
Pin 31	Module Key	Pin 30	Module Key
Pin 33	GND	Pin 32	N/C
Pin 35	PERP0	Pin 34	N/C
Pin 37	PERN0	Pin 36	N/C
Pin 39	GND	Pin 38	Clink Reset (I 3.3V)
Pin 41	PETP0	Pin 40	N/C
Pin 43	PETN0	Pin 42	N/C
Pin 45	GND	Pin 44	N/C
Pin 47	REFCLKP0	Pin 46	N/C
Pin 49	REFCLKN0	Pin 48	N/C
Pin 51	GND	Pin 50	N/C (SUSCLK (32kHz) for DSx)
Pin 53	CLKREQ0#	Pin 52	PERST0#
Pin 55	PEWAKE0#	Pin 54	BT_EN (W_DISABLE2#)
Pin 57	GND	Pin 56	WLAN_EN(W_DISABLE2#)
Pin 59	N/C	Pin 58	N/C
Pin 61	N/C	Pin 60	N/C
Pin 63	GND	Pin 62	N/C
Pin 65	N/C	Pin 64	Resever
Pin 67	N/C	Pin 66	N/C
Pin 69	GND	Pin 68	N/C
Pin 71	N/C	Pin 70	N/C
Pin 73	N/C	Pin 72	3.3V
Pin 75	GND	Pin 74	3.3V

CAMERA



Click Pad





MICRO-STAR INT'L CO.,LTD.

Title: WLAN /Camera/ClickPad/FP

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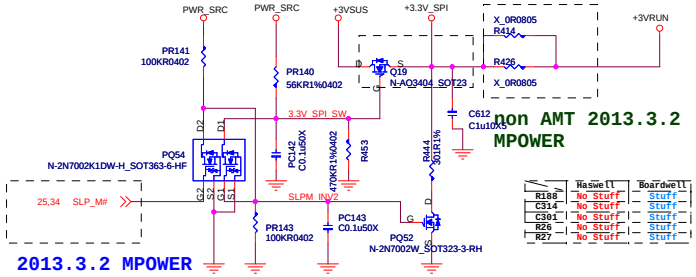
+3.3V_SPI

2A in 2013.3.2 MPOWER

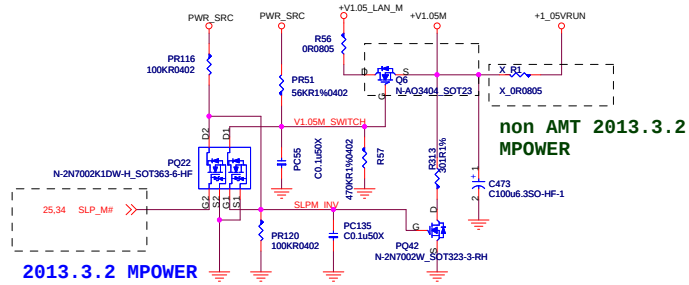


non AMT 2013.3.2 MPOWER

2013.3.2 MPOWER

+V1.05M

+V1.05M 2A in 2013.3.2 MPOWER



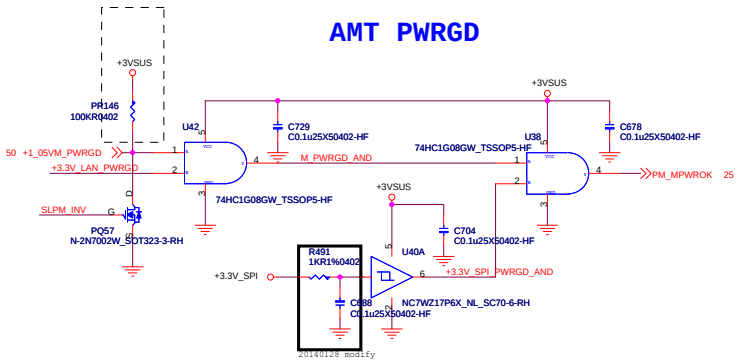
non AMT 2013.3.2 MPOWER

2013.3.2 MPOWER

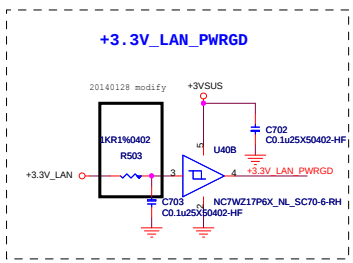
請靠近 PCH

AMT PWRGD

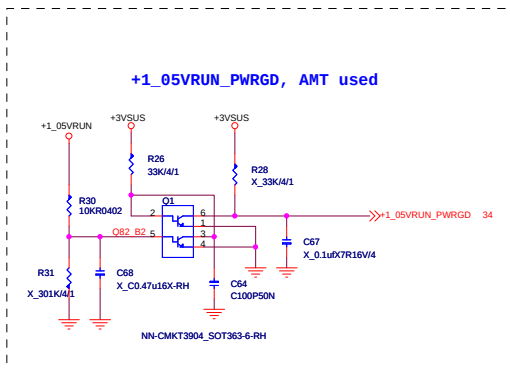
2013.3.2 for AMT



+3.3V_LAN_PWRGD



+1_05VRUN_PWRGD, AMT used



msi MICRO-STAR INT'L CO.,LTD.		
Title: M-POWER		
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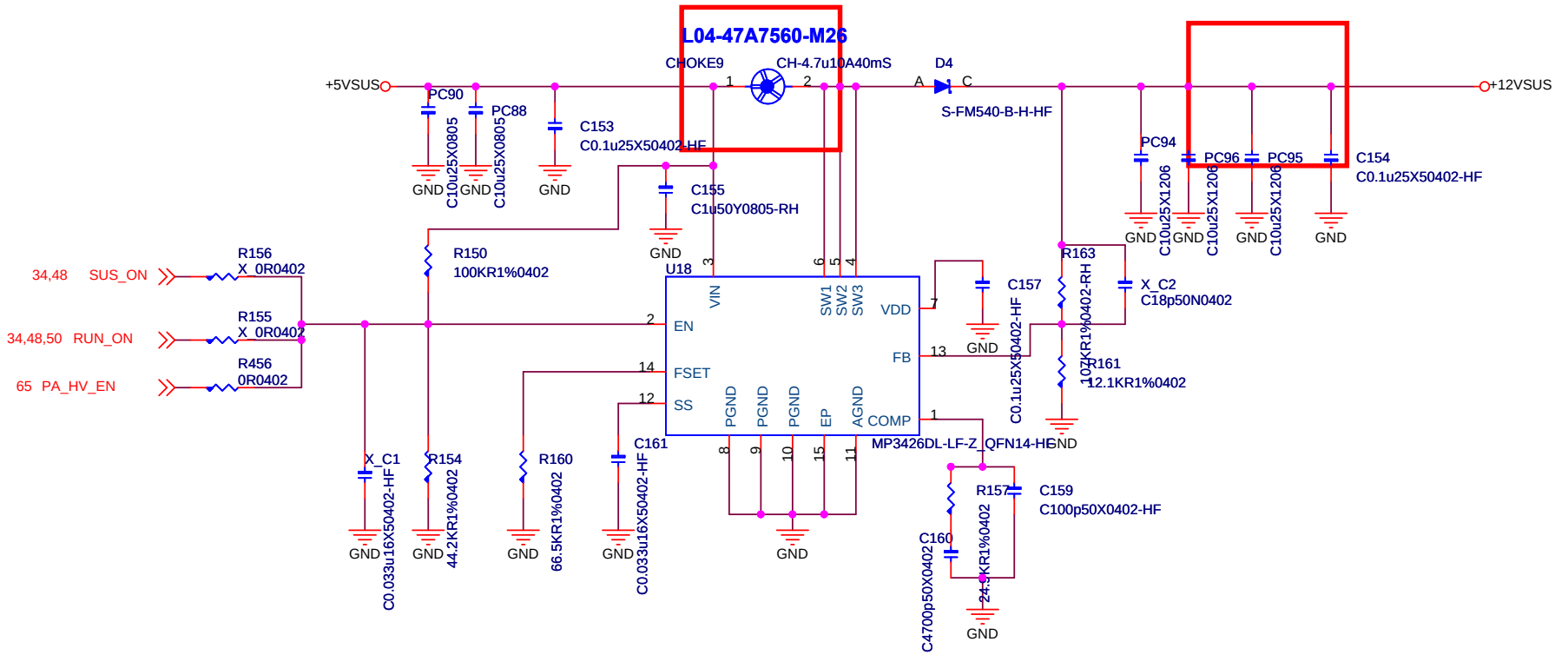
TBT Power 5V Boost 12V 1A



MICRO-STAR INT'L CO.,LTD.		
Title: Thunderbolt Power		
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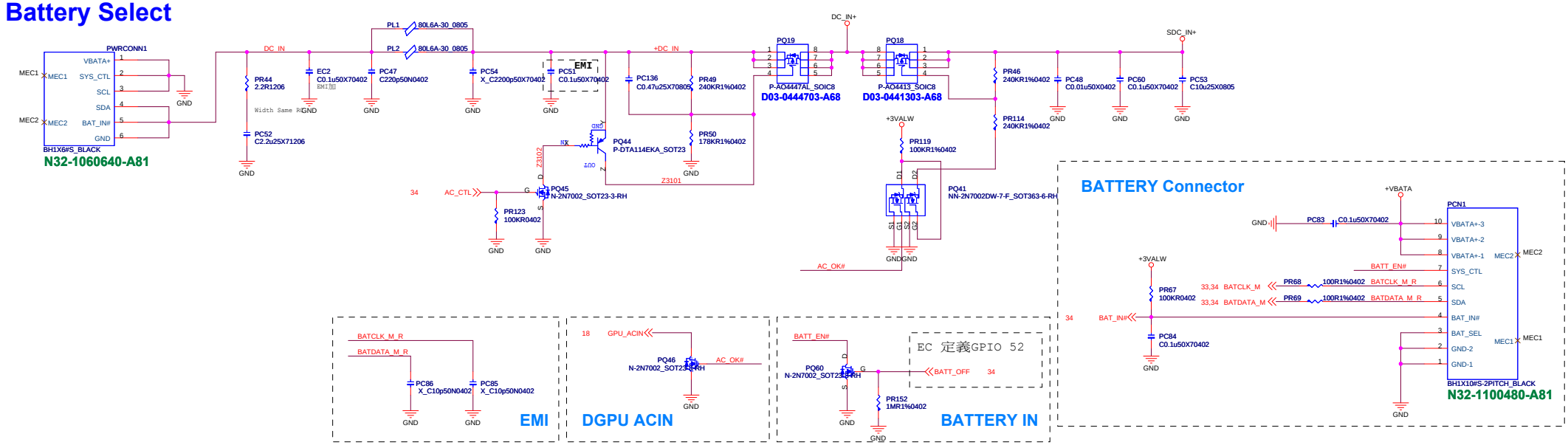
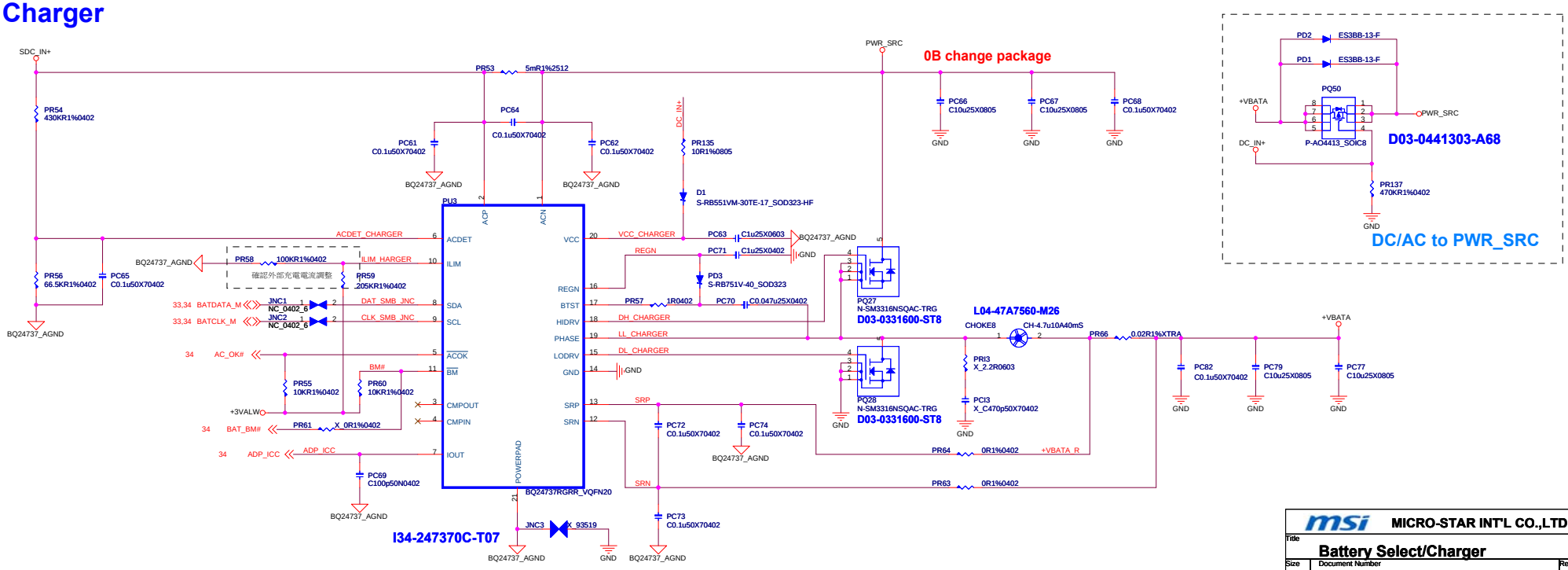
Battery Select/Charger

Battery Select



Battery Charger



MSI	MICRO-STAR INT'L CO.,LTD.
Title	Battery Select/Charger
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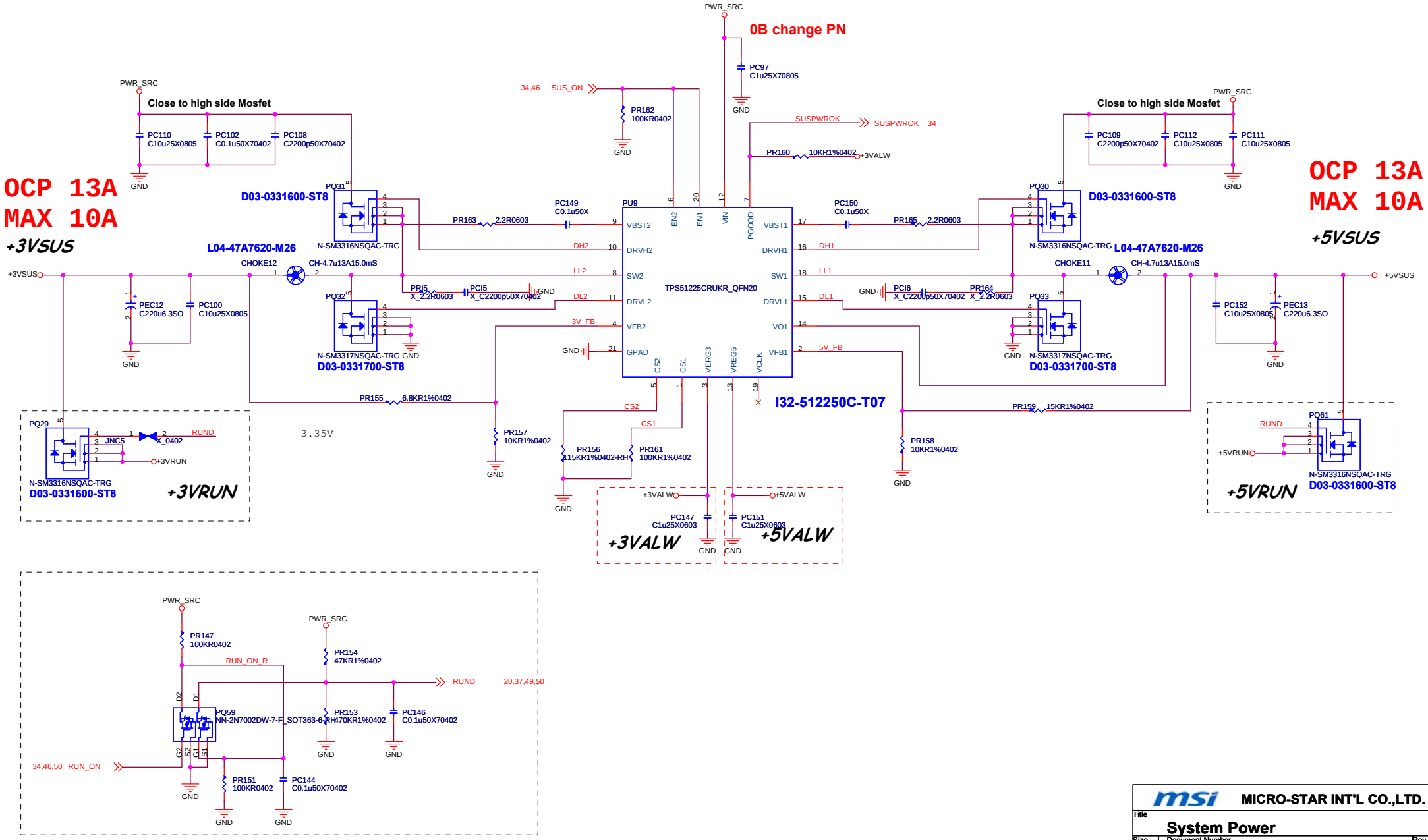
System Power



MICRO-STAR INT'L CO.,LTD.			
Title: System Power			
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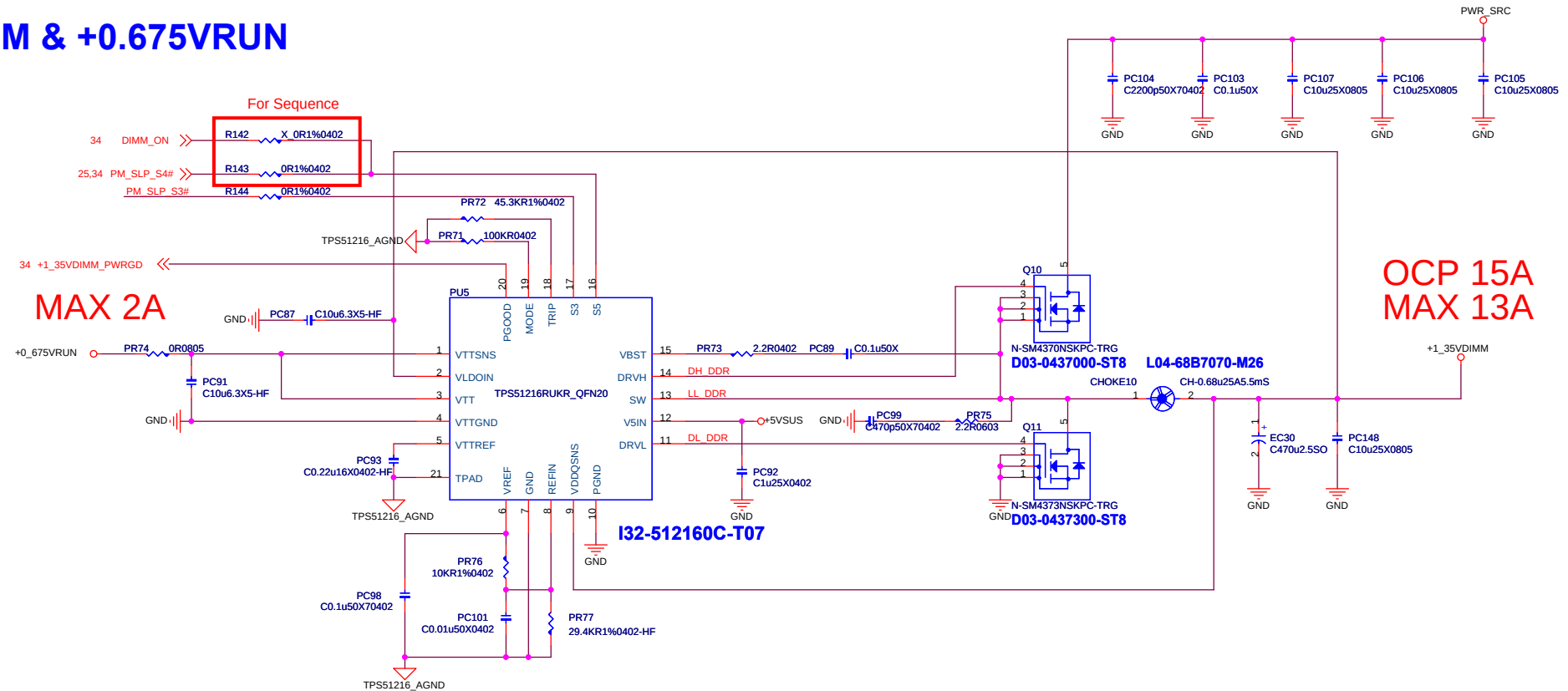
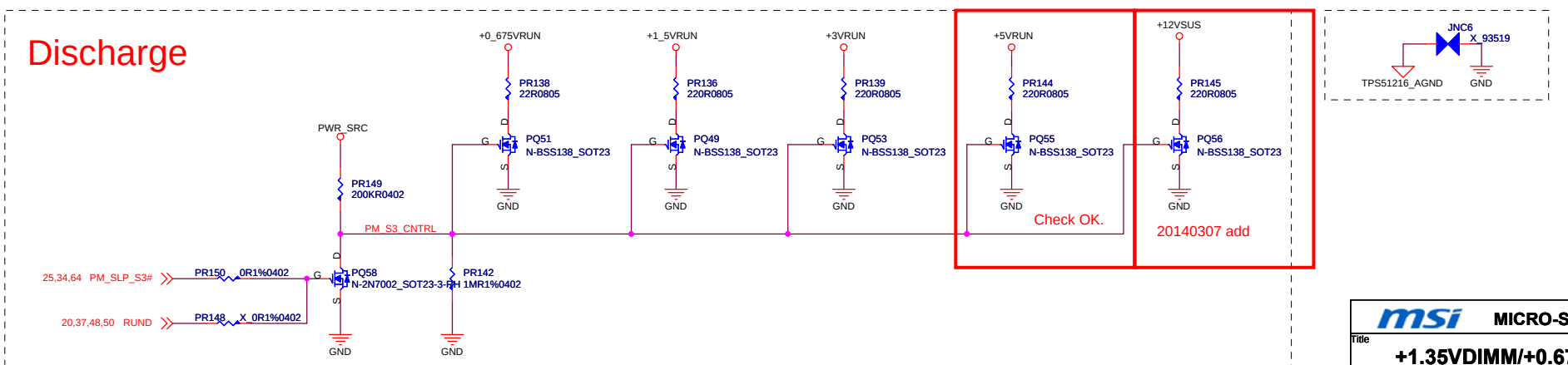
+1.35VDIMM/+0.675VRUN

+1.35VDIMM & +0.675VRUN





MICRO-STAR INT'L CO.,LTD.

Title	+1.35VDIMM/+0.675VRUN	
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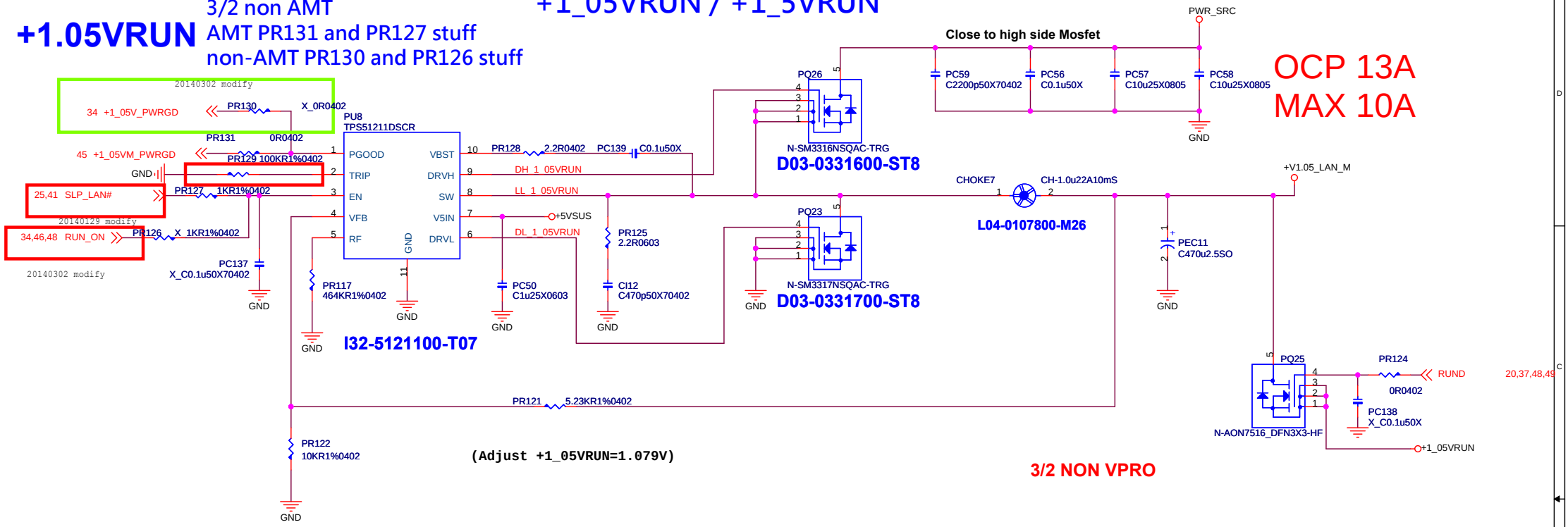
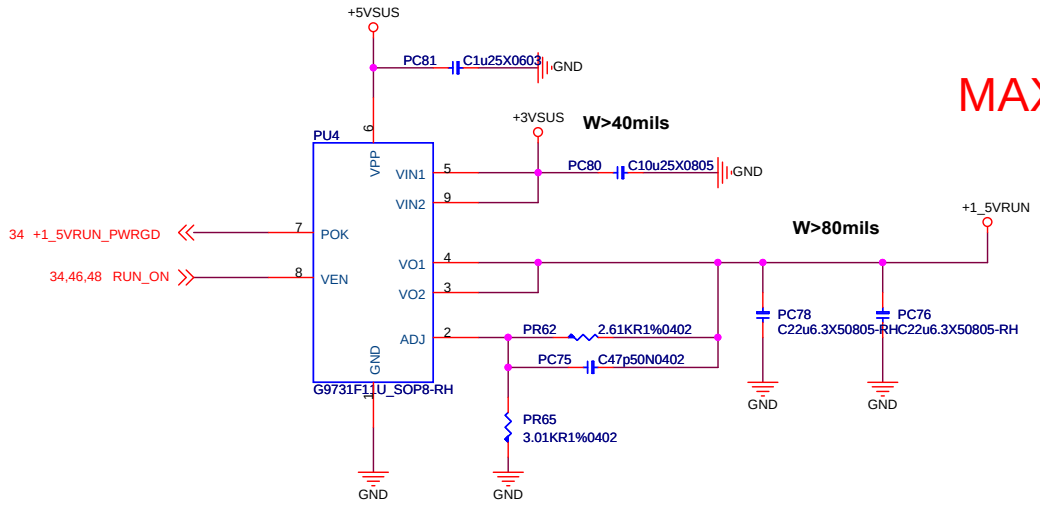
+1.05VRUN

3/2 non AMT
AMT PR131 and PR127 stuff
non-AMT PR130 and PR126 stuff

+1_05VRUN / +1_5VRUN



+1.5VRUN



MICRO-STAR INT'L CO.,LTD.		
Title: +1_05VRUN / +1_5VRUN		
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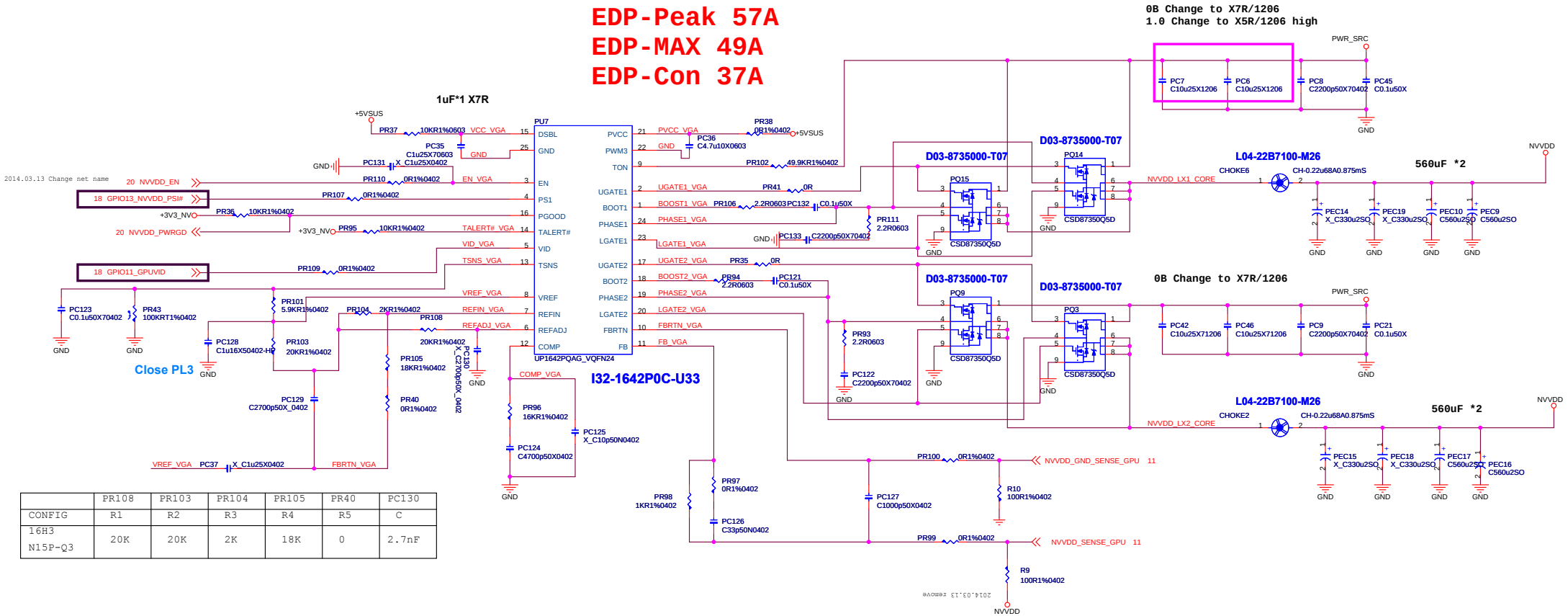
DGPU POWER NVVDD

DGPU POWER / UP1642PQAG

CONFIG B
VBoot:0.9V
Vmin:0.6V / Vmax:1.2V

EDP-Peak 57A
EDP-MAX 49A
EDP-Con 37A



	PR108	PR103	PR104	PR105	PR40	PC130
CONFIG	R1	R2	R3	R4	R5	C
16H3 N15P-Q3	20K	20K	2K	18K	0	2.7nF

msi	MICRO-STAR INT'L CO.,LTD.		
Title	DGPU POWER NVVDD		
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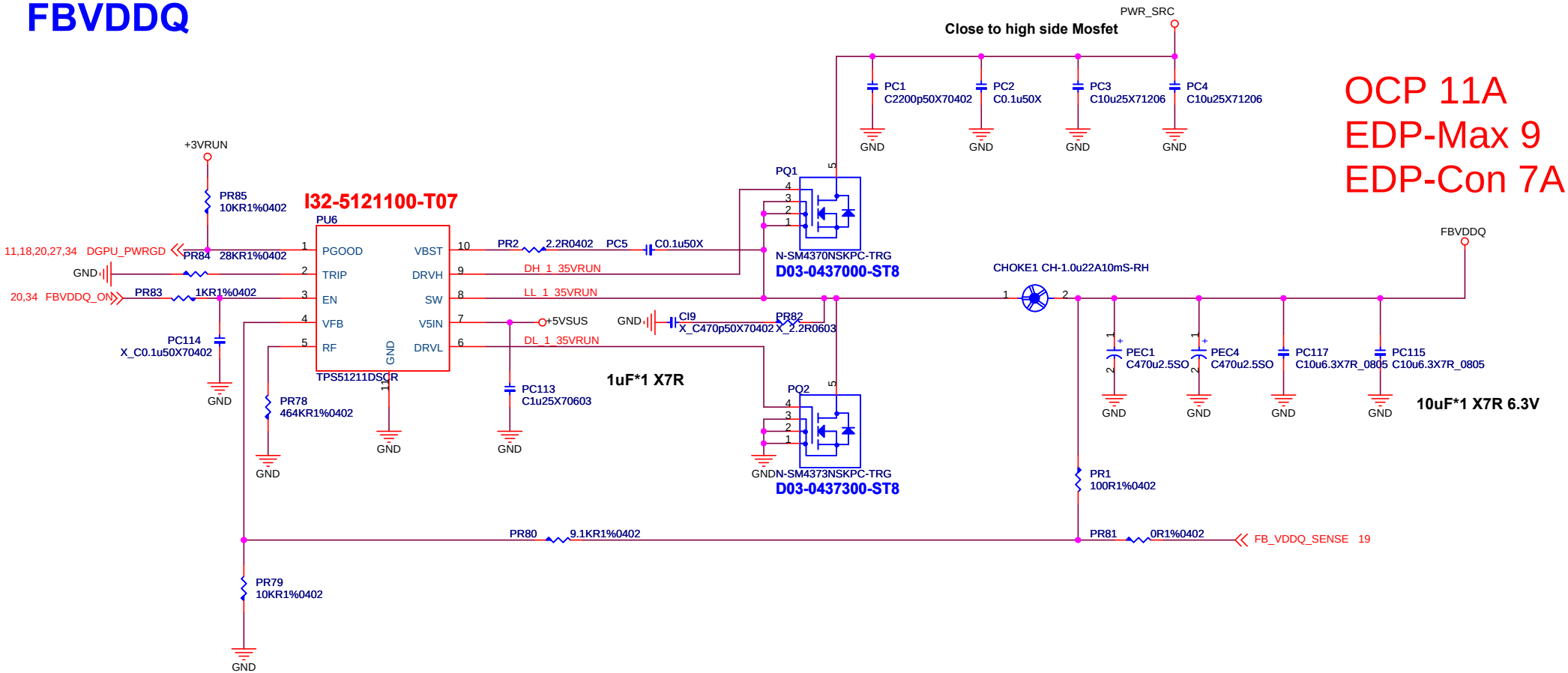
DGPU POWER FBVDDQ

FBVDDQ



MICRO-STAR INT'L CO.,LTD.		
Title: DGPU POWER FBVDDQ		
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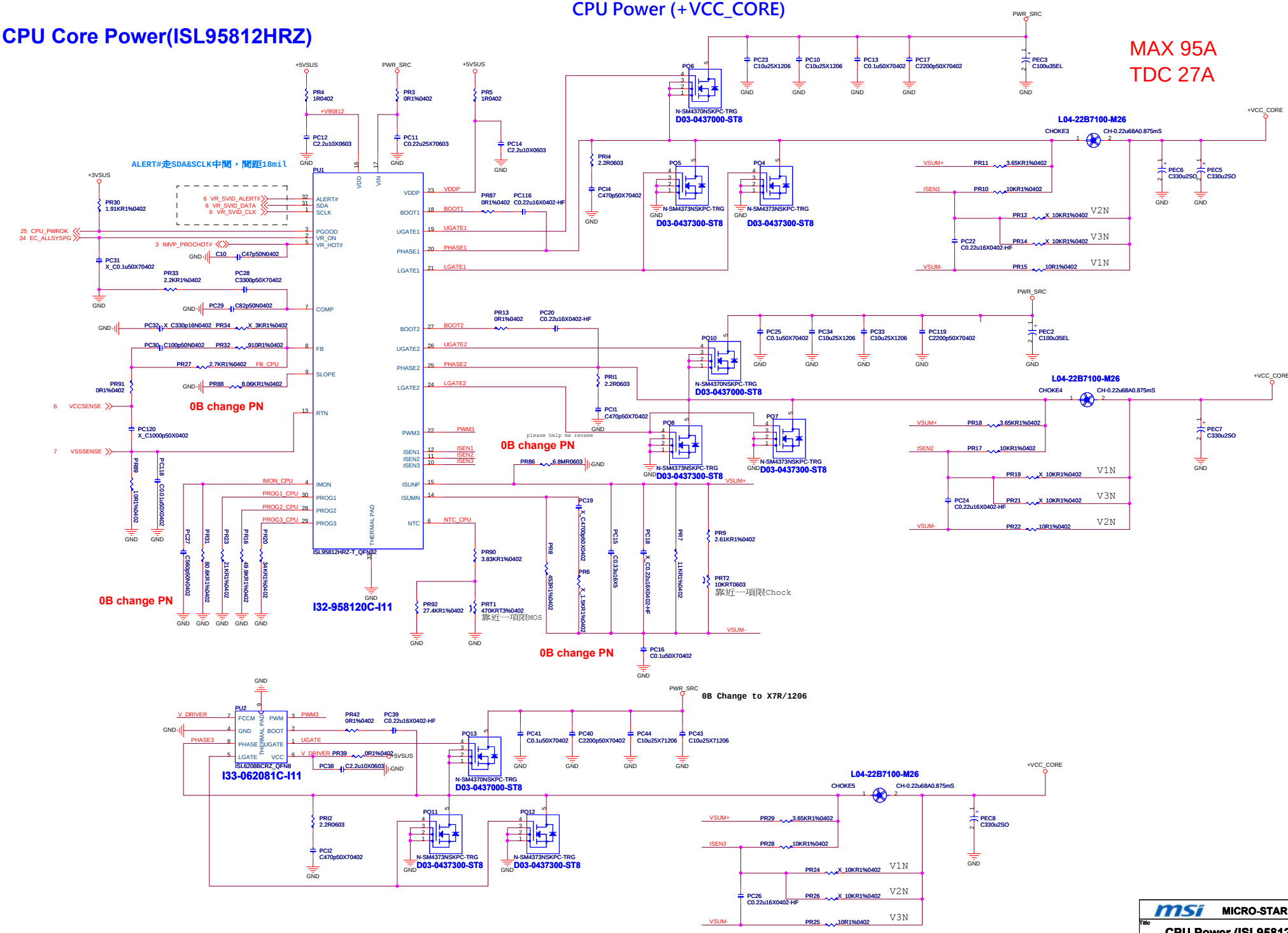
CPU Power (+VCC_CORE)

CPU Core Power(ISL95812HRZ)



EMI/ Impedence

Impedence Connector No PN

40 ohm

J29: L1_6.5mil_40_Ohm, GND2, X_H1X2M_BLACK	J21: L3_5mil_40_Ohm, GND2_GND4, X_H1X2M_BLACK	J14: L10_5mil_40_Ohm, GND9_GND11, X_H1X2M_BLACK

45 ohm

J31: L1_5.5mil_45_Ohm, GND2, X_H1X2M_BLACK	J28: L3_4mil_45_Ohm, GND2_GND4, X_H1X2M_BLACK	J4: L5_4mil_45_Ohm, GND4_GND6, X_H1X2M_BLACK	J20: L10_4mil_45_Ohm, GND9_GND11, X_H1X2M_BLACK	J9: L12_5.5mil_45_Ohm, GND11, X_H1X2M_BLACK

50 ohm

J30: L1_4mil_50_Ohm, GND2, X_H1X2M_BLACK	J27: L3_3mil_50_Ohm, GND2_GND4, X_H1X2M_BLACK	J12: L5_3mil_50_Ohm, GND4_GND6, X_H1X2M_BLACK	J13: L10_3mil_50_Ohm, GND9_GND11, X_H1X2M_BLACK	J1: L12_4mil_50_Ohm, GND11, X_H1X2M_BLACK

80 ohm

J35: L1_DIFF_4.5/4/4.5_80ohm+/-, X_H1X4_BLACK, GND2	J25: L3_DIFF_4.5/7/4.5_80ohm+/-, X_H1X4_BLACK, GND2_GND4	J10: L5_DIFF_4.5/7/4.5_80ohm+/-, X_H1X4_BLACK, GND4_GND6	J16: L10_DIFF_4.5/7/4.5_80ohm+/-, X_H1X4_BLACK, GND9_GND11	J2: L12_DIFF_4.5/4/4.5_80ohm+/-, X_H1X4_BLACK, GND11

85 ohm

J36: L1_DIFF_4.5/4.5/4.5_85ohm+/-, X_H1X4_BLACK, GND2	J26: L3_DIFF_4/6.5/4_85ohm+/-, X_H1X4_BLACK, GND2_GND4	J11: L5_DIFF_4/6.5/4_85ohm+/-, X_H1X4_BLACK, GND4_GND6	J18: L10_DIFF_4/6.5/4_85ohm+/-, X_H1X4_BLACK, GND9_GND11	J7: L12_DIFF_4.5/4.5/4.5_85ohm+/-, X_H1X4_BLACK, GND11

88 ohm

J34: L1_DIFF_4.5/6/4.5_88ohm+/-, X_H1X4_BLACK, GND2	J23: L3_DIFF_3.5/4.5/3.5_88ohm+/-, X_H1X4_BLACK, GND2_GND4	J17: L10_DIFF_3.5/4.5/3.5_88ohm+/-, X_H1X4_BLACK, GND9_GND11

90 ohm

J33: L1_DIFF_4/6/4_90ohm+/-, X_H1X4_BLACK, GND2	J24: L3_DIFF_3.5/5.5/3.5_90ohm+/-, X_H1X4_BLACK, GND2_GND4	J8: L5_DIFF_3.5/5.5/3.5_90ohm+/-, X_H1X4_BLACK, GND4_GND6	J15: L10_DIFF_3.5/5.5/3.5_90ohm+/-, X_H1X4_BLACK, GND9_GND11	J5: L12_DIFF_4/6/4_90ohm+/-, X_H1X4_BLACK, GND11

100 ohm

J32: L1_DIFF_3.5/7.5/3.5_100ohm+/-, X_H1X4_BLACK, GND2	J22: L3_DIFF_3/10/3_100ohm+/-, X_H1X4_BLACK, GND2_GND4	J6: L5_DIFF_3/10/3_100ohm+/-, X_H1X4_BLACK, GND4_GND6	J19: L10_DIFF_3/10/3_100ohm+/-, X_H1X4_BLACK, GND9_GND11	J3: L12_DIFF_3.5/7.5/3.5_100ohm+/-, X_H1X4_BLACK, GND11

EMI

+3VRUN: EC69 X_C0.1u50X70402 → GND

+1_35VDIMM: EC40 X_C0.1u50X70402, EC63 X_C0.1u50X70402, EC62 X_C0.1u50X70402 → GND

+3VSUS: EC66 C0.1u50X70402, EC54 X_C0.1u50X70402 → GND

+5VSUS: EC70 X_C0.1u50X70402, EC65 X_C0.1u50X70402, EC67 X_C0.1u50X70402, EC61 X_C0.1u50X70402, EC60 X_C0.1u50X70402 → GND

RFI

RFI

PWR_SRC — 0B stuff

EC35 C0.1u50X70402
EC38 C0.1u50X70402
EC51 C0.1u50X70402
EC42 C0.1u50X70402
EC50 C0.1u50X70402
EC7 X_C0.1u50X70402
EC12 X_C0.1u50X70402
EC6 C1000p50X0402
EC11 C0.1u50X70402
EC4 C0.1u50X70402
EC3 C0.1u50X70402
→ GND

+VBATA: EC52 C0.1u50X70402, EC64 C0.1u50X70402 → GND

RFI

NVVDD: EC36 X_C0.1u50X70402, EC37 X_C0.1u50X70402, EC39 X_C0.1u50X70402 → GND

+1_05VRUN: EC49 X_C0.1u50X70402 → GND

+0_675VRUN: EC53 X_C0.1u50X70402 → GND

PWR_SRC: C784 C0.1u10X0402, C785 C0.1u10X0402 → GNDGND

+VBATA: C787 C0.1u10X0402 → GND

+3VRUN: C786 C0.1u10X0402 → GND

0507 add for RF

J49, J48, J45: E21-5801010-RH → GND

J41, J43: E21-5801010-RH → GND

0507 add for RF clamp

J44, J42, J46: E21-5801010-RH → GND

msi	MICRO-STAR INT'L CO.,LTD.	
Title: EMI/ Impedence		
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CPU/GPU Holes

MCPU4 H_R200D150
MCPU2 H_R200D150
MCPU3 H_R200D150
MCPU1 H_R200D150
GND

MGPU2 H_R276D169_PB
MGPU4 H_R276D169_PB
MGPU1 H_R276D169_PB
MGPU3 H_R276D169_PB
GND

EMI

SPRING3
X_MECHCU,2.5*5.5*0.1mm

SPRING2
X_E2M-7213211-RH
GND
E2M-7213211-CA7

GND
E2M-2142011-CA7

SPRING1
X_E23-1029060-RH
GND
E23-1029060-CA7

SPRING4
X_E2M-7213211-RH
GND
E2M-7213211-CA7

RUBBER1
E2Y-6H20712-Y40
RUBBER

RUBBER2
E2Y-6H21312-Y40
RUBBER

RUBBER3
E2Y-6H21312-Y40
RUBBER

BRACKET1
307-6H20111-C22
CPU_BRACKET

BRACKET2
307-6H20111-C22
CPU_BRACKET

BRACKET3
307-6H20211-C22
GPU_BRACKET

MYLAR1
E2P-6H22111-Y42
MYLAR

MYLAR2
E2P-6H23111-Y42
MYLAR

MYLAR3
E2P-6H22711-Y42
MYLAR

PCB1
PF0-16H3110-H73
PF0-16H310B-H73

FM4 FM3 FM2 FM1
FM8 FM6 FM7 FM5

Hannstar: PF0-16H2110-H73
TRIPOD: PF0-16H2110-T53

M1
X_H_R197D118_PT_V3
H_R197D118_PT_V3
GND

M6
X_H_R197D118_PT_V3
H_R197D118_PT_V3
GND

UME1
HDMI Lable
X_HDMI ROYALTY
Y01-RHDMI03-000

UME2
BIOS Lable
X_BIOS_LABEL
G51-LA01678-A09

For MP

Fan Hole

MH4
H_R197D91
X_ME_ SCREW HOLE
GND

SSD Stand off

MH2
H_R220D146_PTB
E2B-16H2020
GND

MH1
H_R220D146_PTB
E2B-16H2020
GND

MH3
NPTH157
X_NPTH157

MICRO-STAR INT'L CO.,LTD.

Title: Screw/ME
Size:
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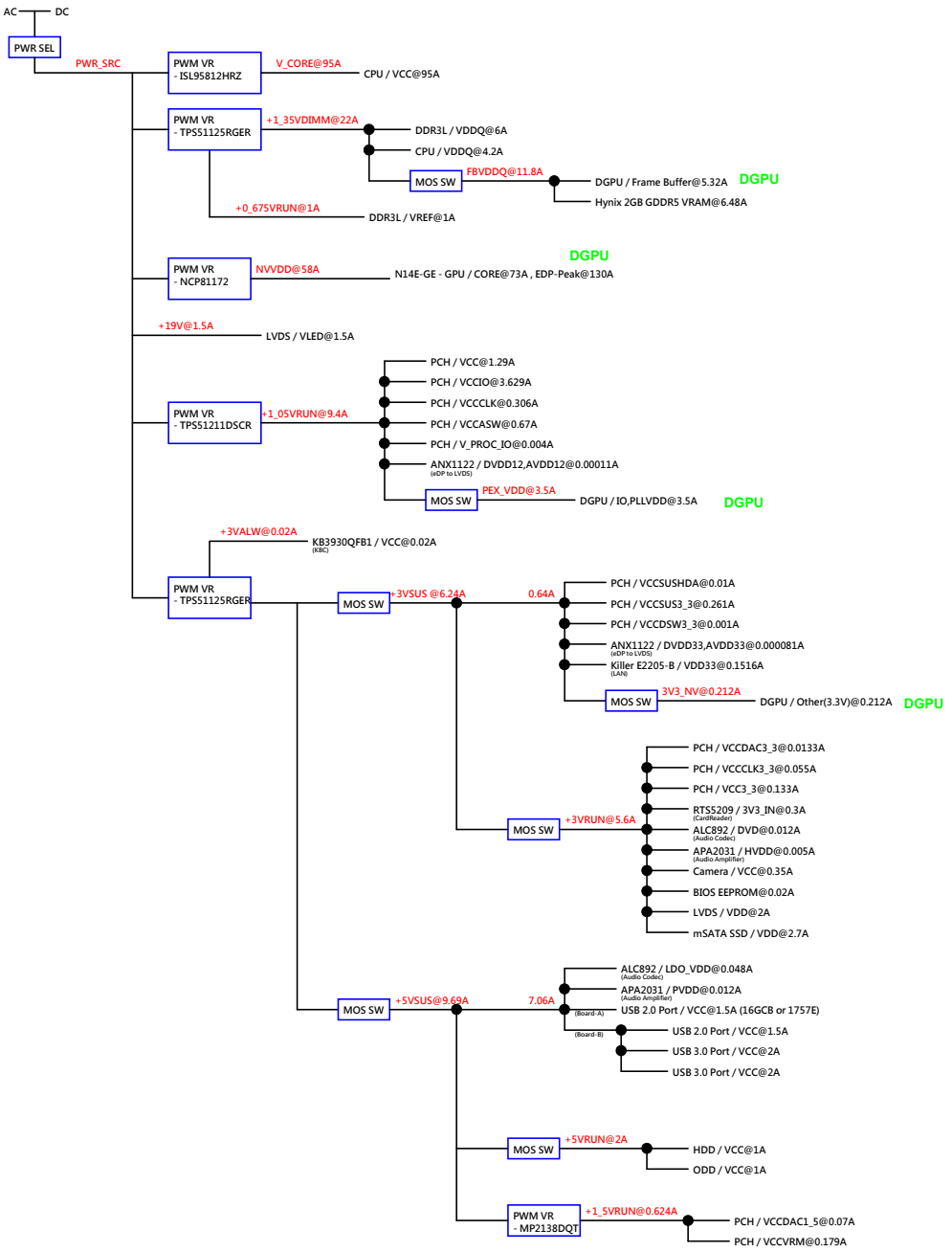
MS-16H2 Power Delivery Chart



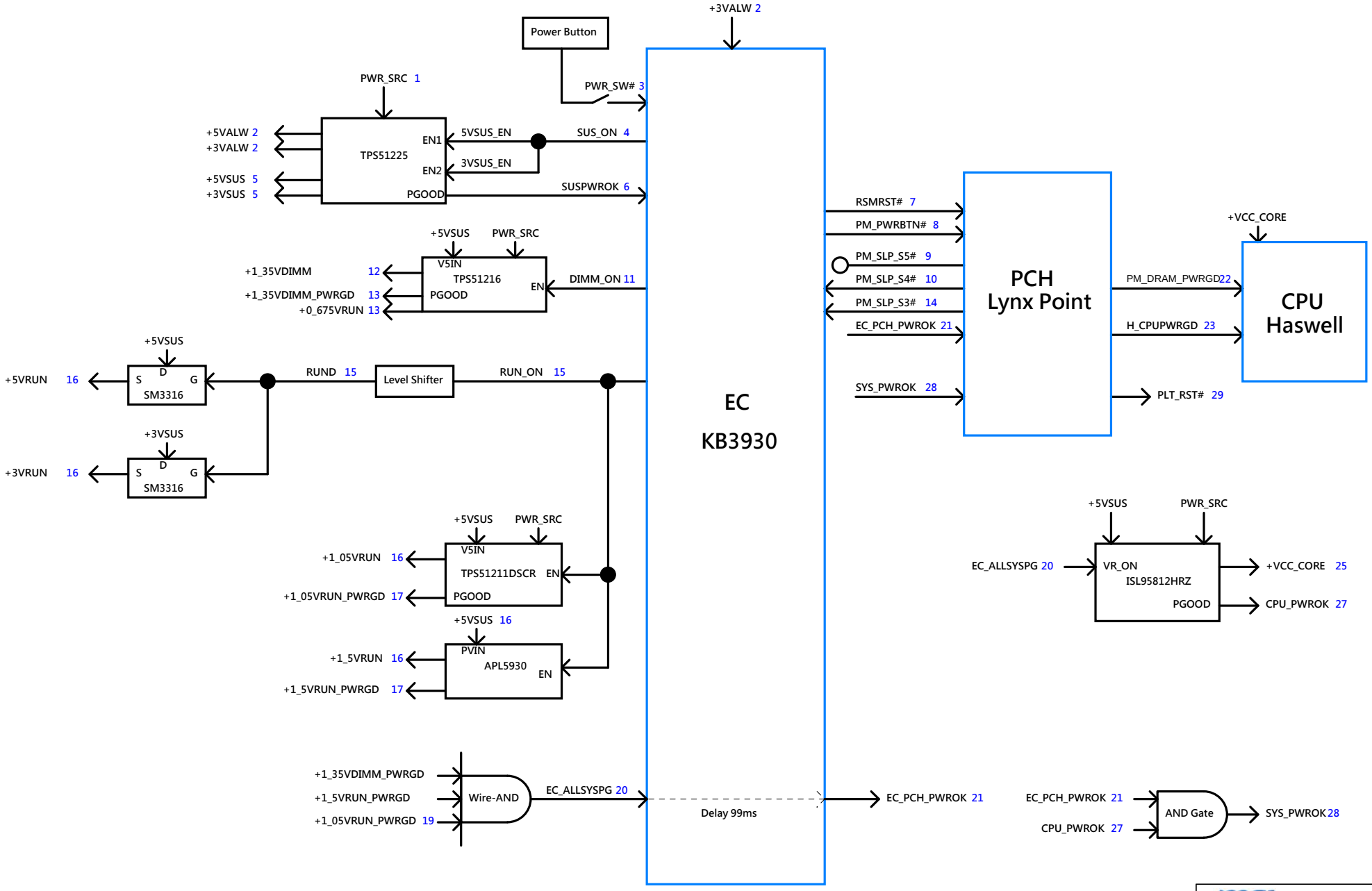
MICRO-STAR INT'L CO.,LTD.

Power Delivery Map

MS-16H3

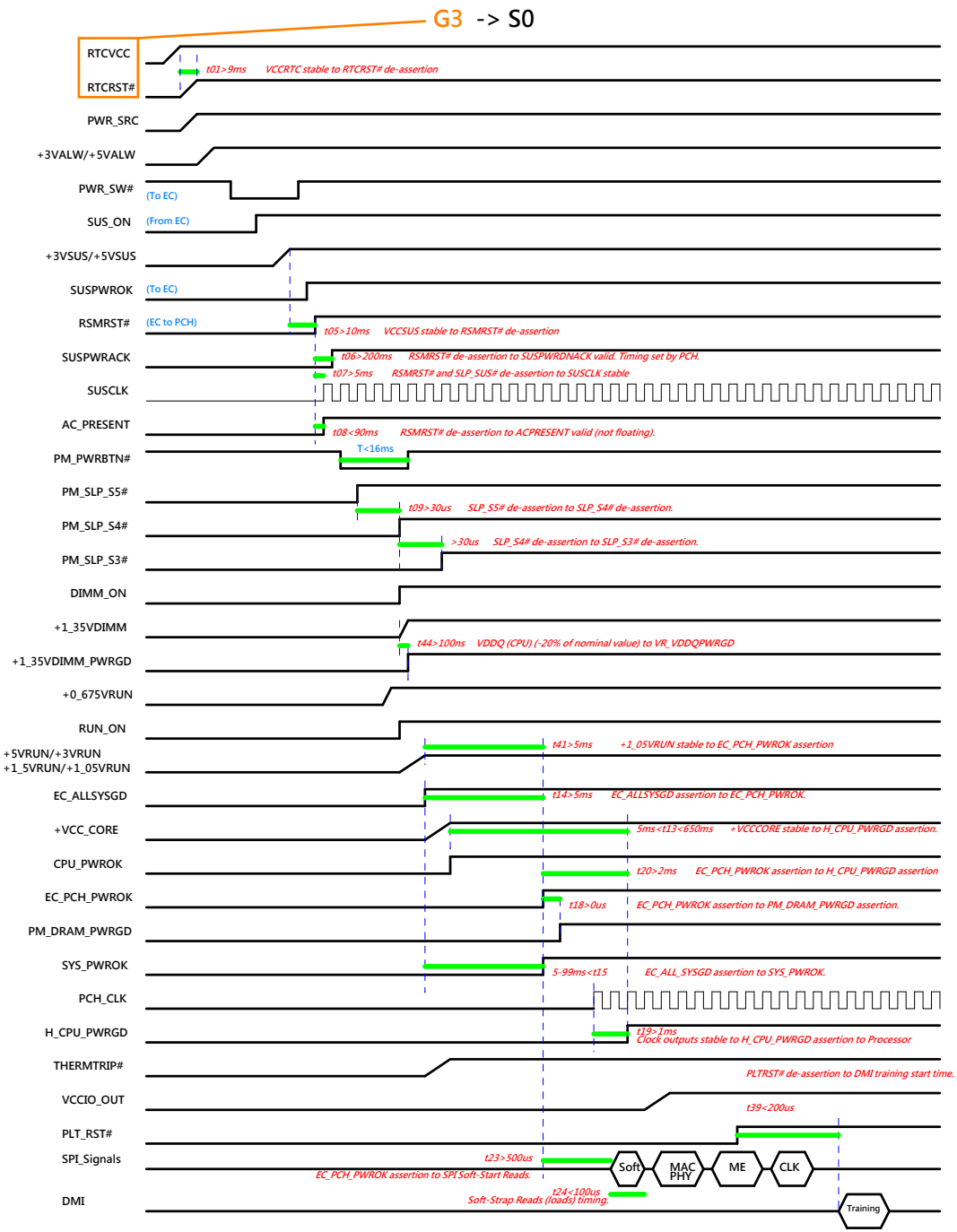
0B

MS-16H2 Power on Block Diagram

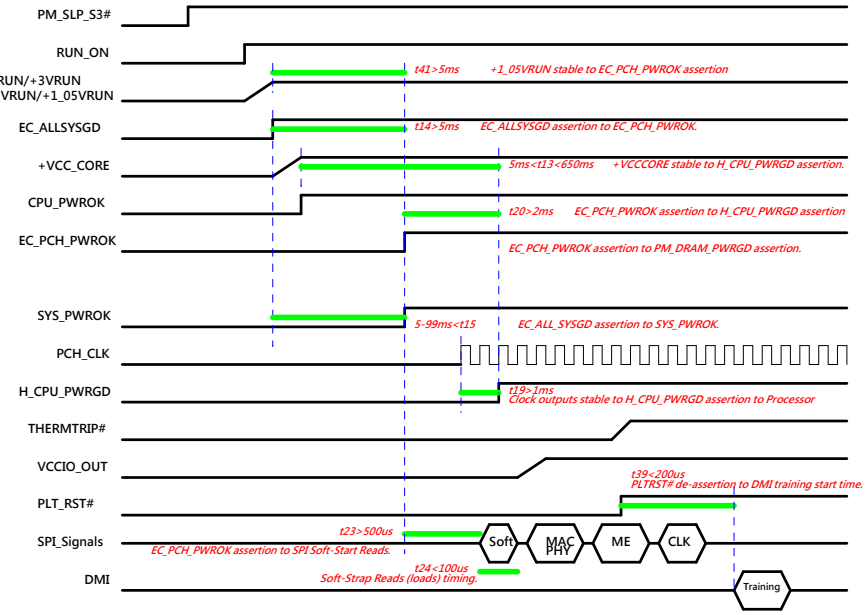


msi	MICRO-STAR INT'L CO.,LTD.	
Title	Power on Block Diagram	
Size	Document Number: MS-16H3	Rev: 0B
Date: Tuesday, May 20, 2014	Sheet 61 of 69	

Power on Sequence



S3-> S0



msi	MICRO-STAR INT'L CO.,LTD.	
Title	Power on Sequence	
Size	Document Number MS-16H3	Rev 0B
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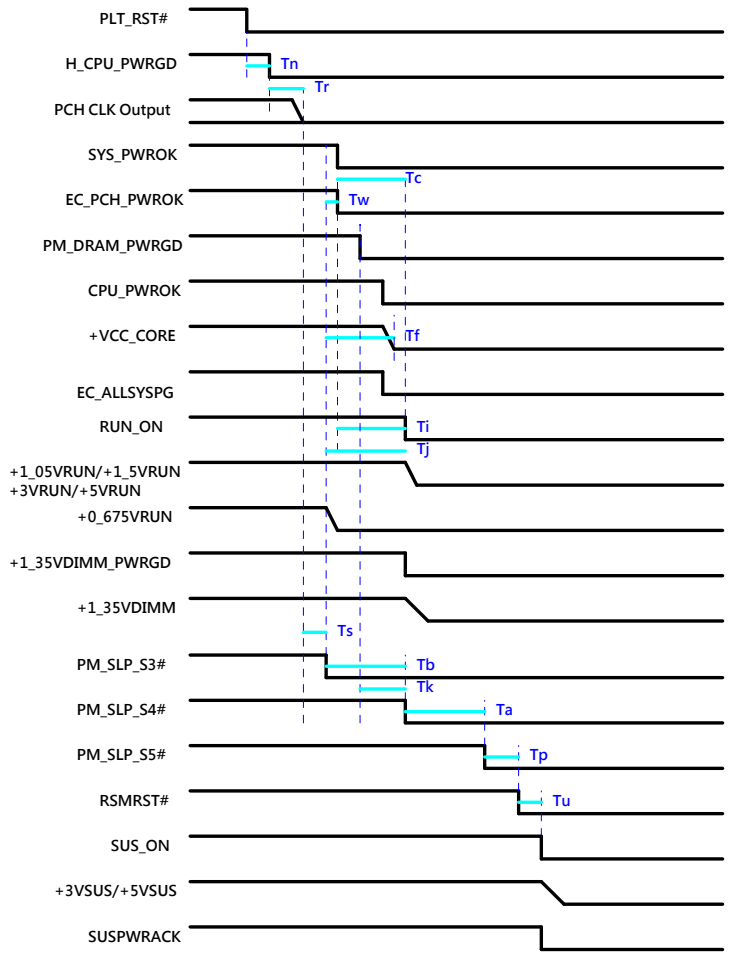
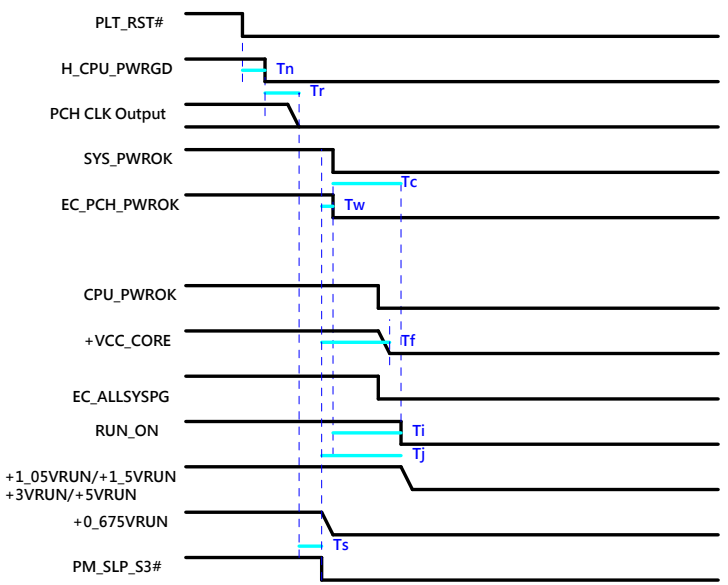
Power down Sequence

S0 -> G3



	MIN	MAX	Units	Description
Ta	30		us	SLP_S4# assertion to SLP_S5# assertion.
Tb	30		us	SLP_S3# assertion to SLP_S4# assertion.
Tc	40		ns	APWROK de-assertion to VCCASW/VCCSPI rails falling.
Tf		500	ms	SLP_S3# assertion to VCCIN(CPU) rail completely off.
Ti	40		ns	PWROK de-assertion to VCCCore (PCH) rail falling (-5% of nominal value).
Tj	5		us	SLP_S3# assertion to VCCCore (PCH) rails falling (-5% of nominal value).
Tk	-100		ns	DRAMPWROK de-assertion to SLP_S4# assertion
Tn	30		us	PLTRST# assertion to CPUPWRGOOD de-assertion.
Tp	500		us	Last SLP_Sx# or SLP_A# assertion to RSMRST# assertion
Tr	10		us	CPUPWRGOOD de-assertion to PCH clock outputs turning off.
Ts	1		us	PCH Clock outputs turning OFF to SLP_S3# assertion.
Tu	40		ns	RSMRST# assertion to VCCSUS rails falling (-5% of nominal value).
Tw	0		ms	SLP_S3# assertion to PWROK de-assertion.

S0 -> S3



MICRO-STAR INT'L CO.,LTD.

Title: Power down Sequence

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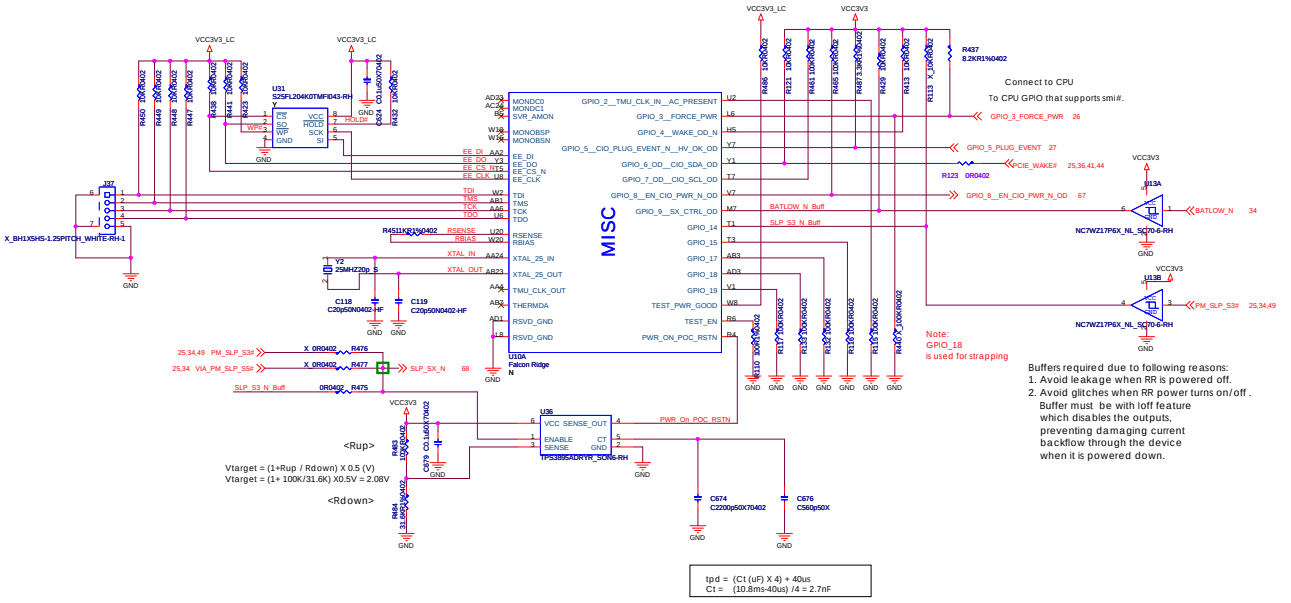
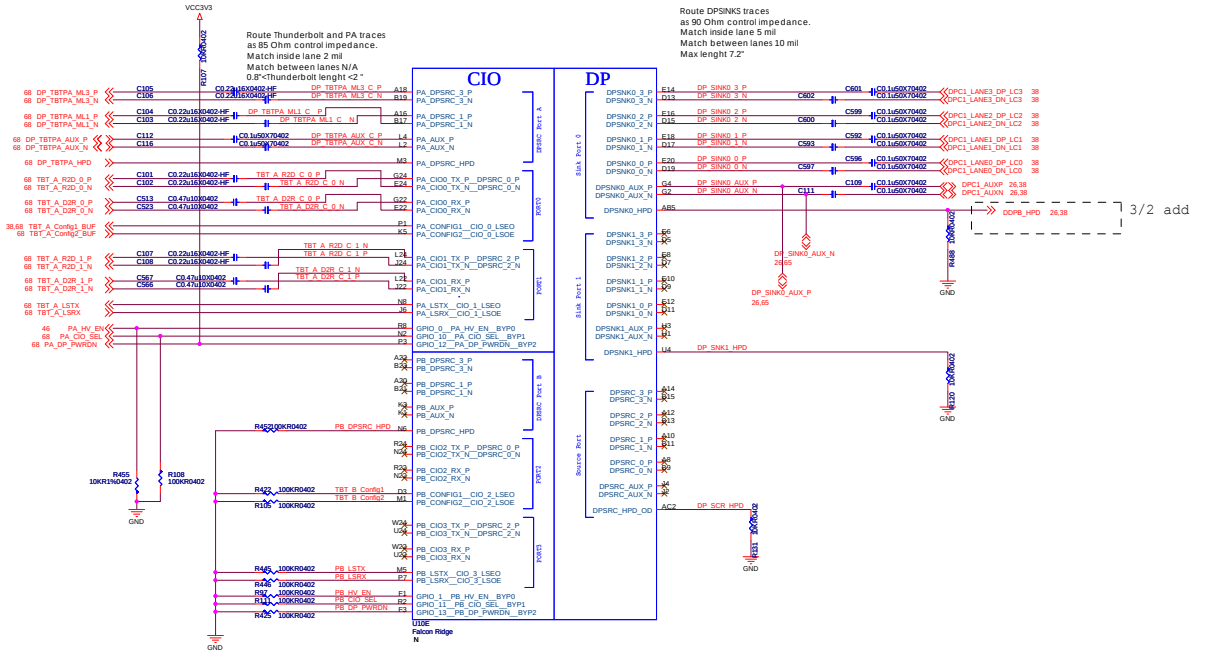
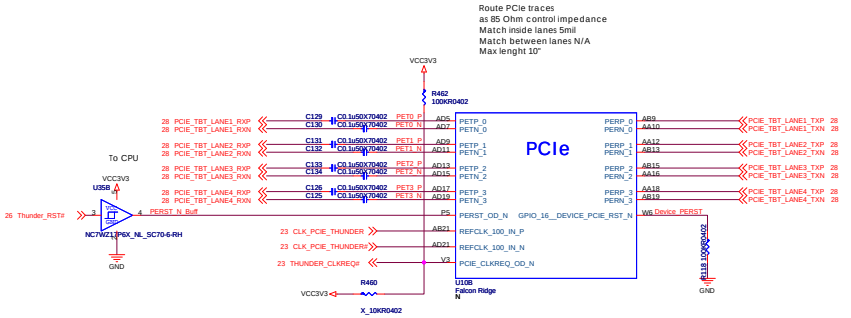


MICRO-STAR INT'L CO.,LTD.		
Title: INTEL Falcon Ridge 5320(2C)		
Size	Document Number: MS-16H3	Rev: 0B
Date: Tuesday, May 20, 2014	Sheet 64 of 69	



MSI	MICRO-STAR INT'L CO.,LTD.		
Title	INTEL Falcon Ridge 5320(2C)		
Size	Document Number	Rev	
	MS-16H3	0B	
Date:	Tuesday, May 20, 2014	Sheet 65 of 69	



Buffer required due to following reasons:

1. Avoid leakage when RR is powered off.
2. Avoid glitches when RR power turns on/off .
   Buffer must be with Ioff feature
   which disables the outputs,
   preventing damaging current
   backflow through the device
   when it is powered down.

MICRO-STAR INT'L CO.,LTD.			
Title: INTEL Falcon Ridge 5320(2C)			
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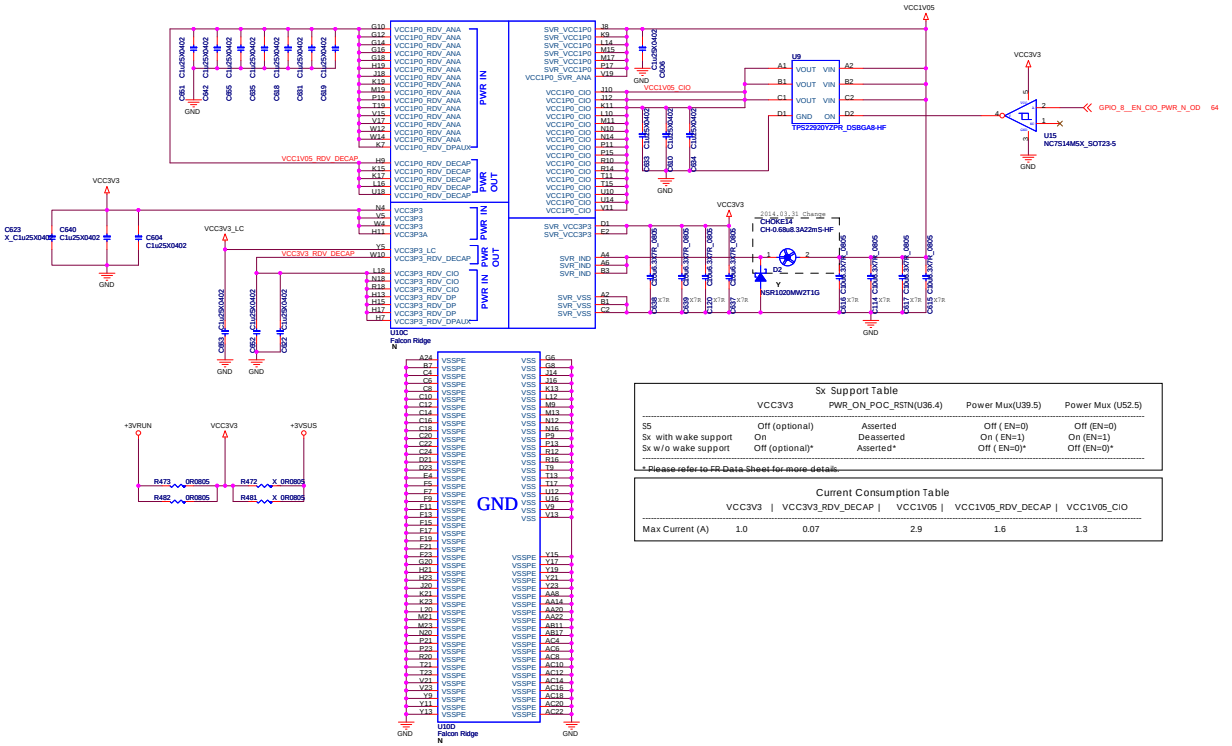

Sx Support Table

	VCC3V3	PWR_ON_POC_RSTN(U36.4)	Power Mux(U39.5)	Power Mux (U52.5)
S5	Off (optional)	Asserted	Off (EN=0)	Off (EN=0)
Sx with wake support	On	Deasserted	On (EN=1)	On (EN=1)
Sx w/o wake support	Off (optional)*	Asserted*	Off (EN=0)*	Off (EN=0)*

* Please refer to FR Data Sheet for more details.

Current Consumption Table

	VCC3V3	VCC3V3_RDV_DECAP	VCC1V05	VCC1V05_RDV_DECAP	VCC1V05_CIO
Max Current (A)	1.0	0.07	2.9	1.6	1.3

MICRO-STAR INT'L CO.,LTD.

Title: INTEL Falcon Ridge 5320(2C)

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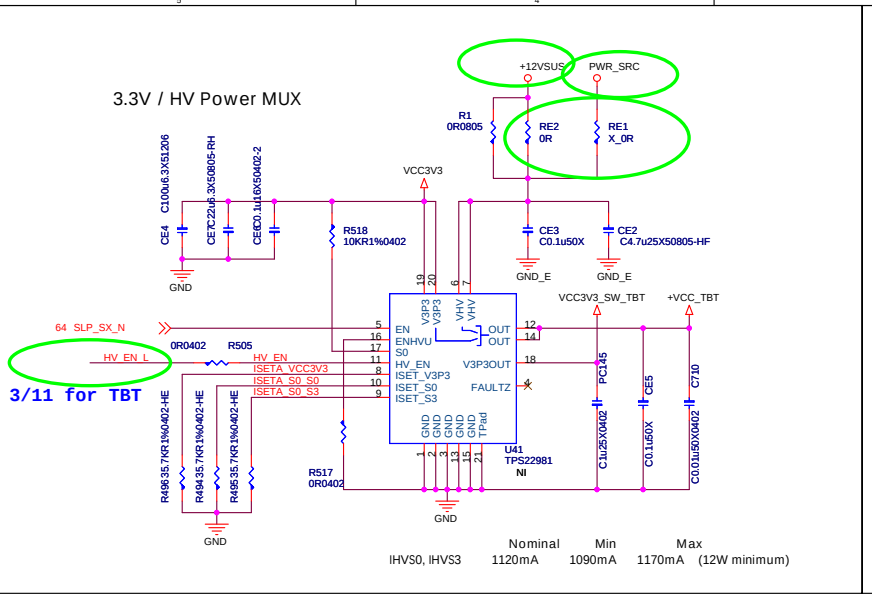
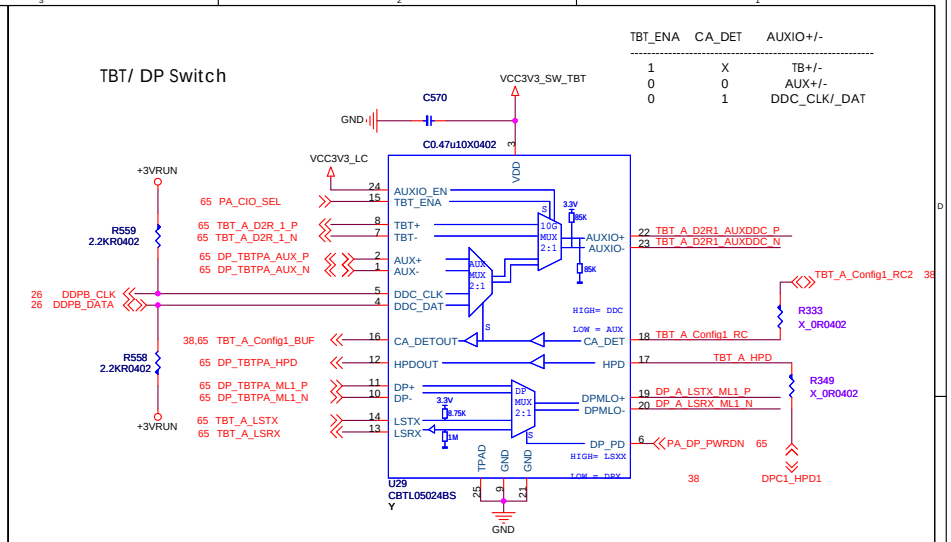
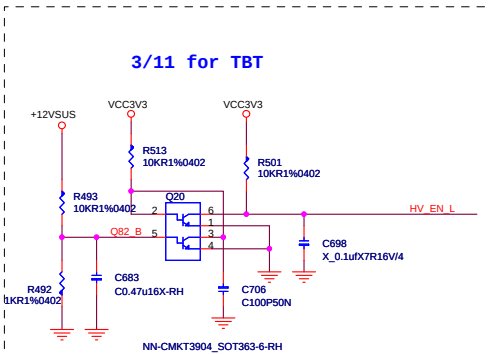
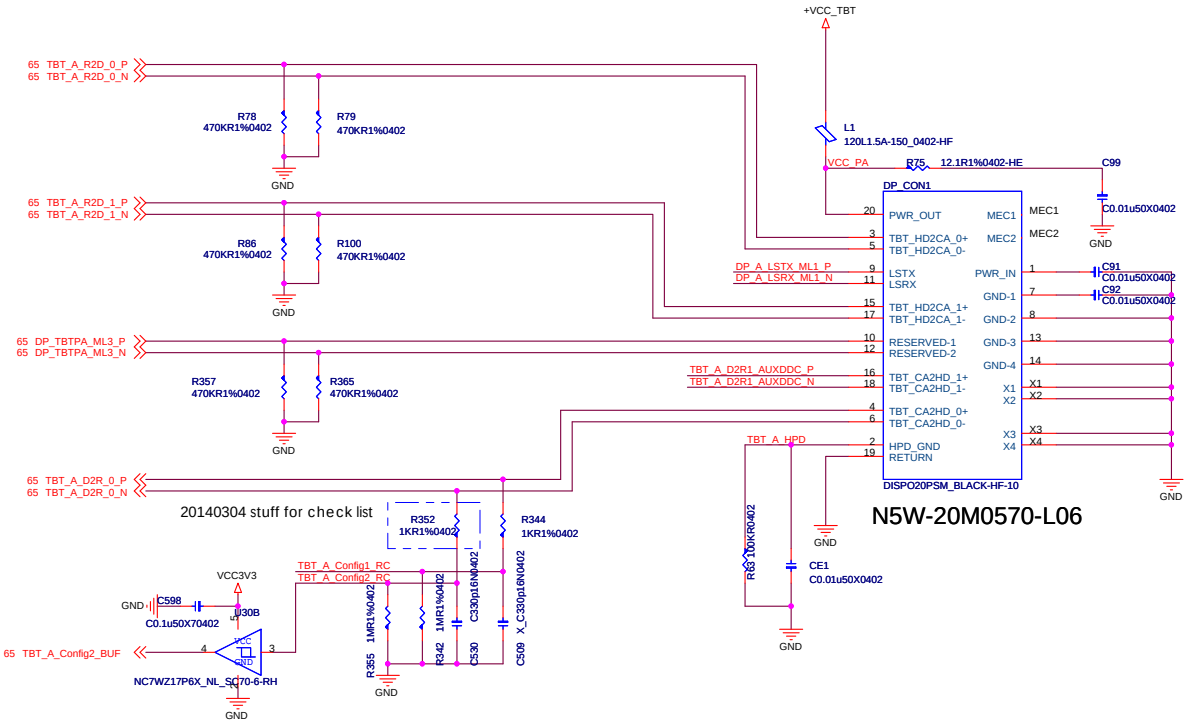






Power mux will be
on when VCC12V0 >=4.5V and
off when VCC12V0 <=3.4V
Vbe=770mV@Ic=10mA -->
4.5X2.05K/(10K+2.05K) = 0.766V

Note:
If generating the 12v from a supply
different than 3.3v - resistors values of
R52 and R53 should be different
Example: If VCC12V0 is boosted from 5V,
the R52 is 10K ohm and R53 is 1K ohm



History

0B: Hardware part

01. Remove All GAP for power parts.
02. Add 3V3_NV part for leakage
03. Change cardreader PN.
04. Change BTB PN
05. Change SPDIF/ Audio Jack PN
06. R116 unstuff, R117 stuff.
07. R346 unstuff
08. Remove SUBWOOFER
09. Add one more AMP for SPK

0B: Power part

01. PR33 2.2Kohm R11-0222T12-W08
02. PC29 82pF/50V C11-8201012-W08
03. PC30 100pF/16V C11-1011032-W08
04. PR34 unstuff
05. PC32 unstuff
06. PR27 2.7Kohm R11-0272T12-W08
07. PR90 8.06Kohm R11-8061T12-W08
08. PR32 910Rohm R11-0911T12-W08
09. PC27 560pF/16V C11-5611812-W08
10. PR31 80.6Kohm R11-8062T12-W08
11. PR23 21Kohm R11-0213T12-W08
12. PR88 6.8Mohm R11-0685T13-W08
13. PR8 453Rohm R11-4530T22-W08
14. PC19 unstuff
15. PR6 unstuff
16. PR140 100Kohm R11-0104T12-W08
17. PR145 93.1Kohm R11-9312T12-R01
18. PR143 15Kohm R11-0153T12-W08
19. PR124 95.3Kohm R11-9532T12-W08
20. PR86 28.7Kohm R11-2872T12-W08
21. PC69, PC70 change to 1206 package
22. PR88 6.8Mohm R11-0685T13-W08

MICRO-STAR INT'L CO.,LTD.		
Title: History		
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