MODEL NAME : *CKF50/CKA50*

PCB NO : *LA-E992P*

BOM P/N :

451A7631L51
451A7631L52
451A7631L01
451A7631L02

Dell/Compal Confidential

Schematic Document

KABYLAKE-H
N17E

Firestar/Armani

2017-07-25

Rev: 1.0 (A00)

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Issued Date	2011/08/25	Deciphered Date	2011/08/25

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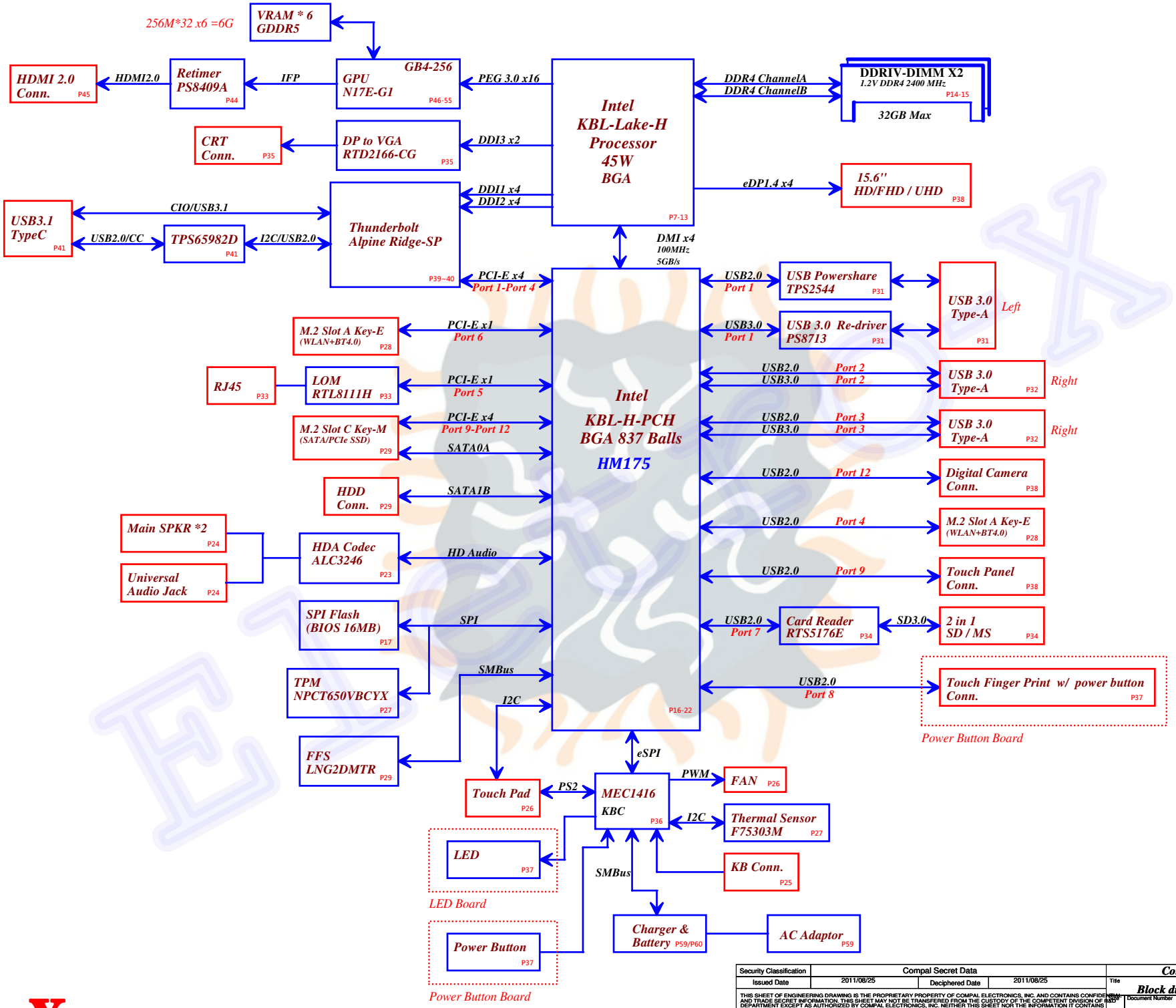
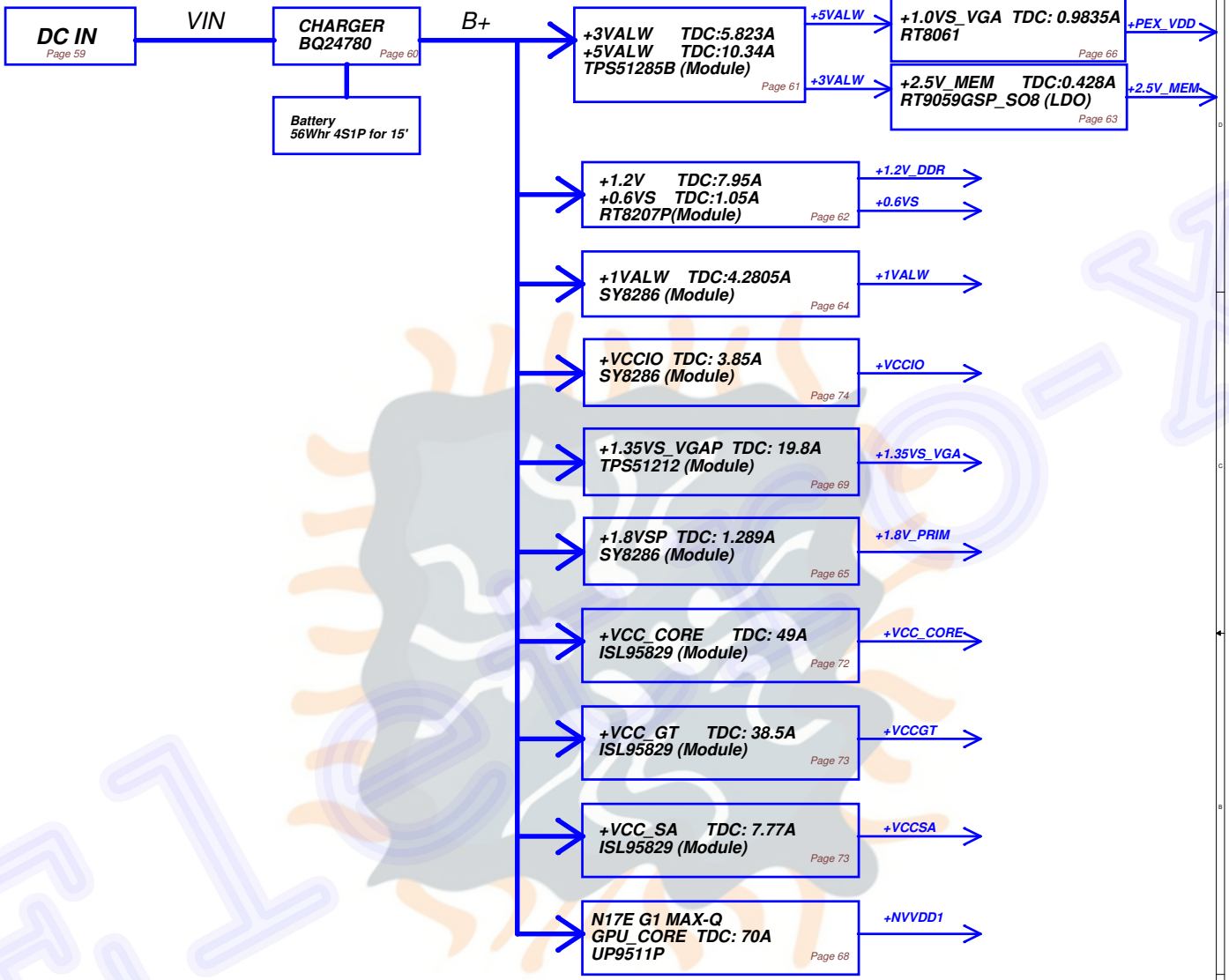
Title: *Cover Page*

Size: B | Document Number: *LA-E992P* | Rev: 1.0(A00)

Date: Tuesday, July 25, 2017 | Sheet 1 of 77



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date 2011/08/25	Title: Block diagram
			Document Number: LA-E992P
Date: Tuesday, July 25, 2017		Sheet 2	of 77



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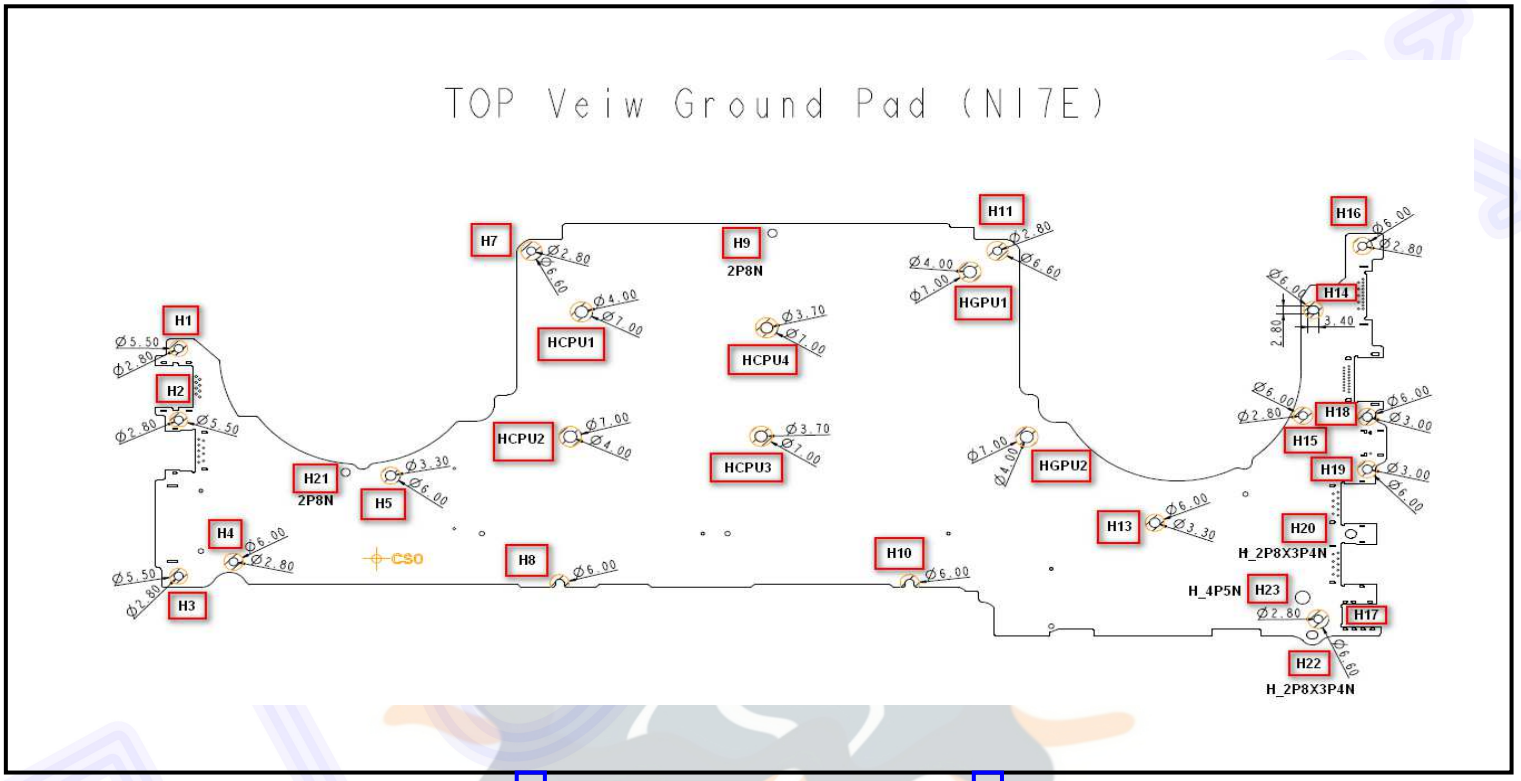
Issued Date	2011/08/25	Deciphered Date	2012/07/25
Title	Power Block Diagram		
Document Number	LA-E992P		Rev 0.3(002)
Date: Tuesday, July 25, 2017	Sheet 58 of 77		

Compal Confidential

Project Code :
File Name :

ME Hole Location
Base on ME 0505

M/B



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Issued Date	2011/08/25	Deciphered Date	2012/07/25

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Title: ***DB block diagram***

Size | Document Number: ***LA-E992P***

Date: Tuesday, July 25, 2017 | Sheet 3 of 77

Refer Page 36

PCI EXPRESS	DESTINATION	USB3	DESTINATION
Lane 1	Alpine Ridge - SP	7	None
Lane 2		8	None
Lane 3		9	None
Lane 4		10	None
Lane 5	LOM		
Lane 6	NGFF - WLAN + BT		
Lane 7	None		
Lane 8	None	SATA	DESTINATION
Lane 9	NGFF - SSD	0A	NGFF - SSD
Lane 10		1A	None
Lane 11			
Lane 12			
Lane 13	None	0B	None
Lane 14	None	1B	HDD
Lane 15	None	2	None
Lane 16	None	3	None

USB2	DESTINATION
1	USB JUSB3 (Left Side)
2	USB JUSB1 (Right Side)
3	USB JUSB2 (Right Side)
4	NGFF - WLAN + BT
5	None
6	None
7	CARD READER
8	Finger Print
9	Touch screen
10	None
11	None
12	CAMERA

USB3	DESTINATION
1	USB JUSB3 (Left Side)
2	USB JUSB1 (Right Side)
3	USB JUSB2 (Right Side)
4	None
5	None
6	None

DDI	DESTINATION
1	Alpine Ridge
2	Alpine Ridge
3	DP to VGA

Board ID	Resistor
X00	10K
X01	17.8K
X02	27K
X03	37.4K
A00	49.9K

Symbol Note :

: means Digital Ground

: means Analog Ground

CLK_PCIE	DESTINATION	CLK_REQ	DESTINATION
0	None	0	None
1	None	1	None
2	LOM	2	LOM
3	NGFF - WLAN + BT	3	NGFF - WLAN + BT
4	None	4	None
5	Alpine Ridge - SP	5	Alpine Ridge - SP
6	NGFF - SSD	6	NGFF - SSD
7	GPU	7	GPU
8	None	8	None
9	None	9	None
10	None	10	None
11	None	11	None
12	None	12	None
13	None	13	None
14	None	14	None
15	None	15	None

Table 1-3. PCH-H HSIO Detail (Lane 1-14)

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14
H110	USB 3.0/ OTG	USB 3.0	USB 3.0	USB 3.0	N/A	N/A	N/A	N/A	N/A	LAN Only	PCIe/ LAN	PCIe	PCIe	PCIe
H170	USB 3.0/ OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe	PCIe
HM170/ HM175	USB 3.0/ OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0/ PCIe	USB 3.0/ PCIe	PCIe	PCIe / LAN	PCIe/ LAN	PCIe	PCIe	PCIe
QM170/ QM175	USB 3.0/ OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0/ PCIe	USB 3.0/ PCIe	PCIe	PCIe / LAN	PCIe/ LAN	PCIe	PCIe	PCIe
Z170	USB 3.0/ OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0/ PCIe	USB 3.0/ PCIe	USB 3.0/ PCIe	USB 3.0/ PCIe/LAN	PCIe/ LAN	PCIe	PCIe	PCIe
B150	USB 3.0/ OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	N/A	N/A	N/A	LAN Only	PCIe/ LAN	PCIe	PCIe	PCIe
Q150	USB 3.0/ OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	N/A	LAN Only	PCIe/ LAN	PCIe	PCIe	PCIe
Q170	USB 3.0/ OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0/ PCIe	USB 3.0/ PCIe	USB 3.0/ PCIe	USB 3.0/ PCIe/LAN	PCIe / LAN	PCIe	PCIe	PCIe

Table 1-4. PCH-H HSIO Detail (Lane 15-26) (Sheet 1 of 2)

SKU	15[1]	16[1]	17	18	19[1]	20[1]	21	22	23	24	25	26
H110	PCIe/ LAN	PCIe	N/A	LAN Only	SATA0/ LAN	SATA1	SATA	SATA	N/A	N/A	N/A	N/A
H170	PCIe/LAN /SATA0	PCIe/ SATA1	PCIe	PCIe/ LAN	PCIe/LAN / SATA0	PCIe/ SATA1	PCIe/ SATA	PCIe/ SATA	SATA	SATA	PCIe	PCIe
HM170/ HM175	PCIe/LAN /SATA0	PCIe/LAN/ SATA1	PCIe	PCIe/ LAN	PCIe/LAN/ SATA0	PCIe/ SATA1	PCIe/ SATA	PCIe/ SATA	N/A	N/A	N/A	N/A
QM170/ QM175	PCIe/LAN /SATA0	PCIe/LAN/ SATA1	PCIe	PCIe/ LAN	PCIe/ LAN/ SATA0	PCIe/ SATA1	PCIe/ SATA	PCIe/ SATA	N/A	N/A	N/A	N/A
Z170	PCIe/LAN /SATA0	PCIe/ SATA1	PCIe	PCIe/ LAN	PCIe/LAN / SATA0	PCIe/ SATA1	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe	PCIe
B150	PCIe/LAN /SATA0	PCIe/ SATA1	PCIe	PCIe/ LAN	SATA0	SATA1	SATA	SATA	SATA	SATA	N/A	N/A
Q150	PCIe/LAN /SATA0	PCIe/ SATA1	PCIe	PCIe/ LAN	PCIe/LAN / SATA0	PCIe/ SATA1	SATA	SATA	SATA	SATA	N/A	N/A
Q170	PCIe/LAN /SATA0	PCIe/ SATA1	PCIe	PCIe/ LAN	PCIe/LAN / SATA0	PCIe/ SATA1	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe	PCIe

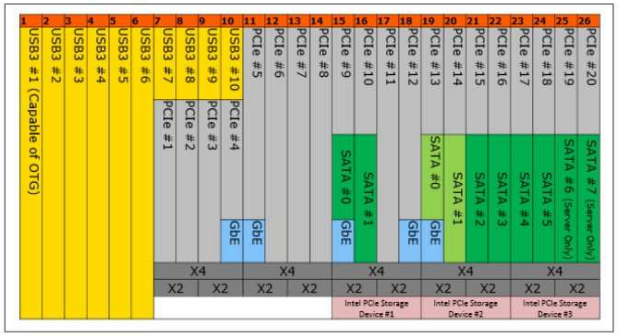
eSPI Virtual Wires (VW) (Sheet 1 of 2)

Virtual Wire	PCH Pin Direction	Reset Control	Pin Retained in PCH (For Use by Other Components)
SUS_STAT#	Output	ESPI_RESET#	No
SUS_PWRDN_ACK	Output	ESPI_RESET#	No
PLTRST#	Output	ESPI_RESET#	Yes
PME#	Input	ESPI_RESET#	No
WAKE#	Input	ESPI_RESET#	No
SMI#	Input	PLTRST#	N/A
SCI#	Input	PLTRST#	N/A
RCIN#	Input	PLTRST#	No
SLP_A#	Output	ESPI_RESET#	Yes

eSPI Virtual Wires (VW) (Sheet 2 of 2)

Virtual Wire	PCH Pin Direction	Reset Control	Pin Retained in PCH (For Use by Other Components)
SLP_S3#/SLP_S4#/ SLP_S5#/SLP_LAN#/ SLP_WLAN#	Output	DSW_PWROK	Yes

HSIO Multiplexing on PCH-H



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Title: Notes List

Size: Document Number: LA-E992P

Rev: 1.0

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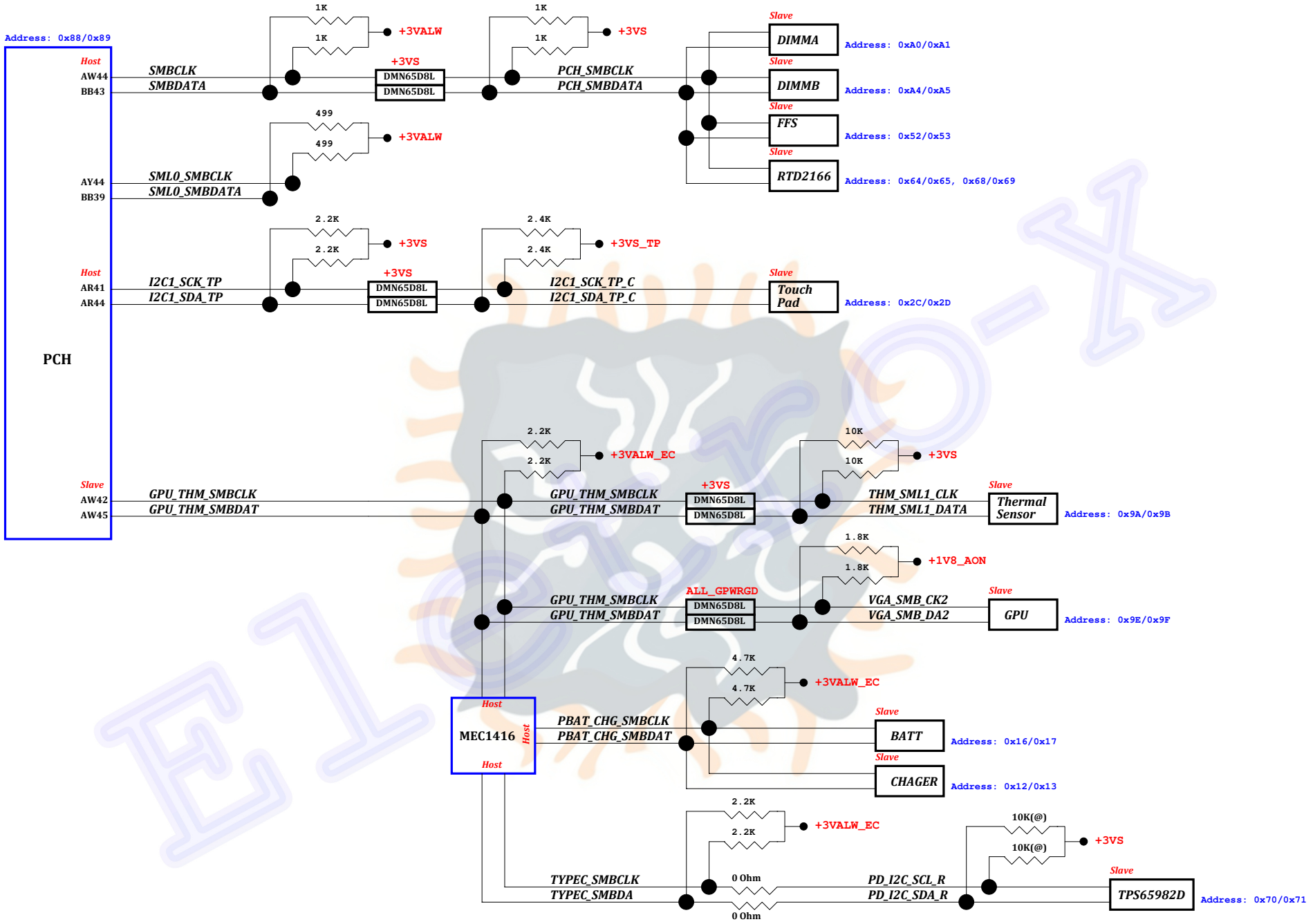


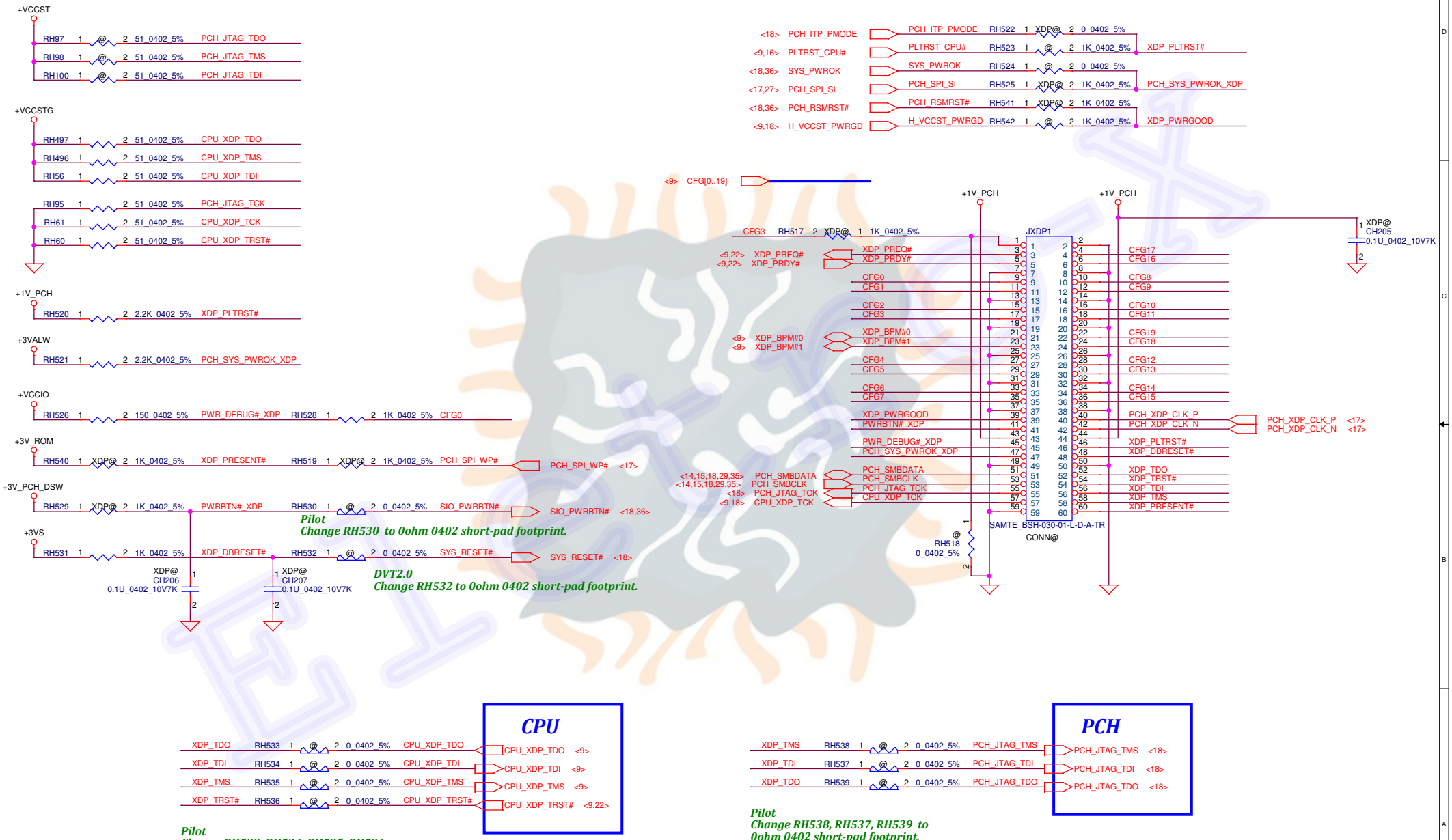
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: SMBus Block Diagram

Size: Custom | Document Number: LA-E992P | Rev: 0.7

Date: Tuesday, July 25, 2017 | Sheet 5 of 77



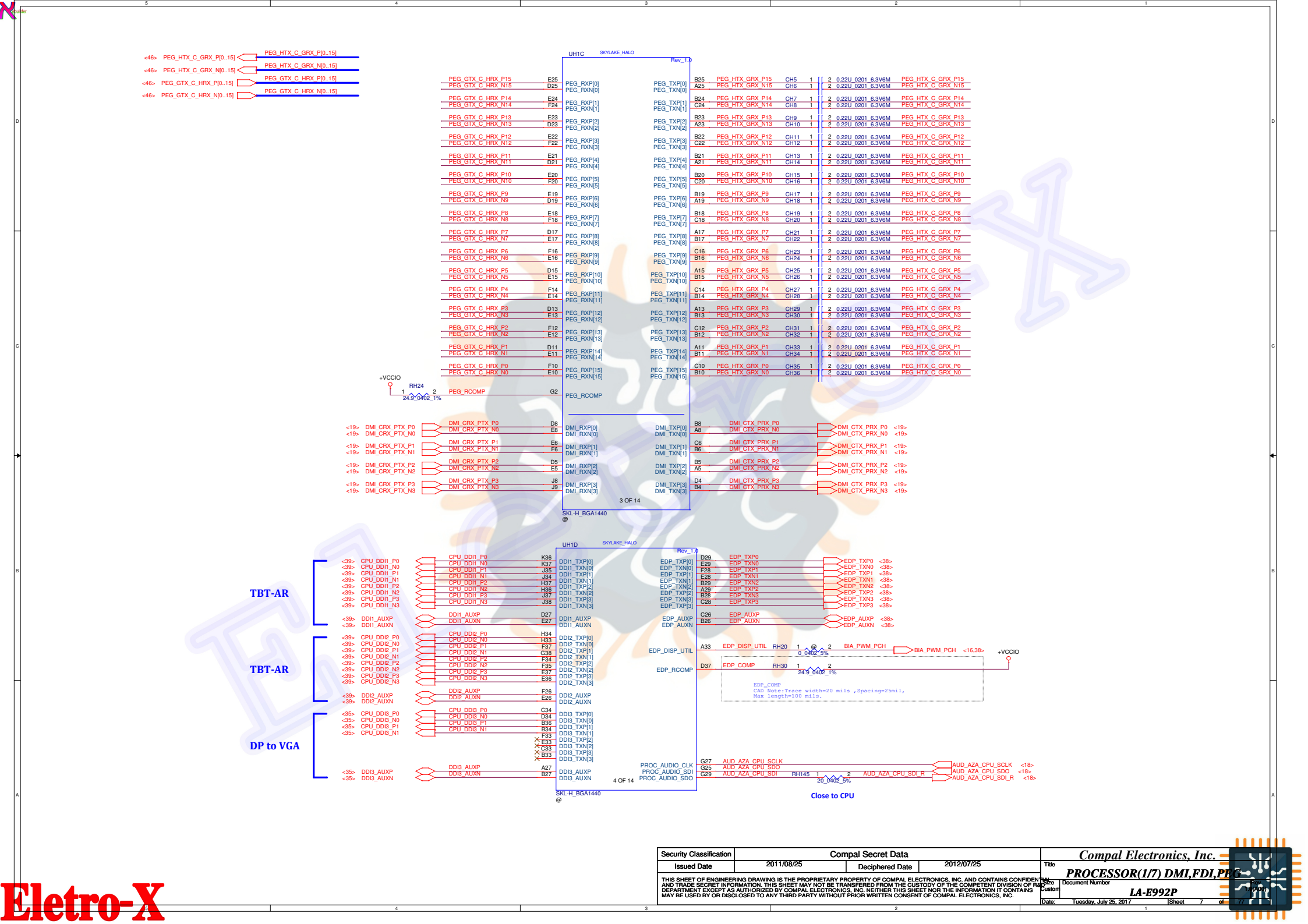
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: XDP CONN

Size | Document Number: LA-E992P | Rev: 1.0

Date: Tuesday, July 25, 2017 | Sheet 6 of 77



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.			
Title	PROCESSOR(1/7) DMI,FDI,PEG		
Size	Document Number	Rev	
Custom	LA-E992P	1.0	
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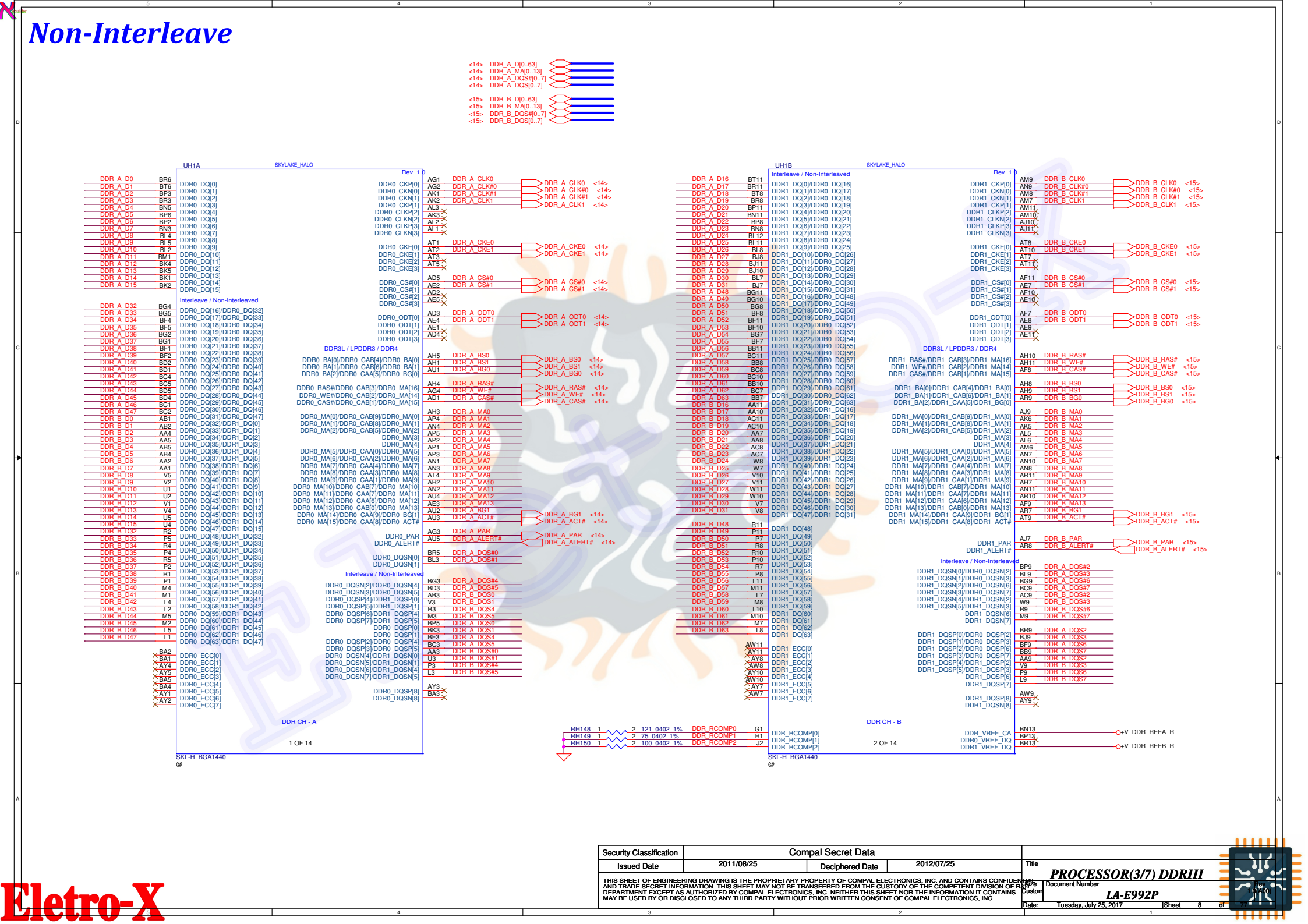
Non-Interleave



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Title: PROCESSOR(3/7) DDRIII

Size: Custom | Document Number: LA-E992P | Rev: 1.0

Date: Tuesday, July 25, 2017 | Sheet 8 of 77

CFG Straps for Processor

Stall reset sequence after CPU PLL lock until de-asserted	
CFG0	* 1 = (Default) Normal Operation; No stall. 0 = Stall.

CFG0 RH183 1 @ 2 1K_0402_5%

PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

CFG2 RH184 1 2 1K_0402_5%

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

CFG4 RH185 1 2 1K_0402_5%

PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

CFG5 RH186 1 @ 2 1K_0402_5%
CFG6 RH187 1 @ 2 1K_0402_5%

If change to x8, need cheange setting.

PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

CFG7 RH188 1 @ 2 1K_0402_5%

+VCCSTG
RH165 1 2 1K_0402_5% H_PROCHOT#

+VCCST
RH163 1 2 1K_0402_5% H_THERMTRIP#_R
RH156 1 @ 2 51_0402_5% XDP_PREQ#
RH164 1 2 1K_0402_5% H_VCCST_PWRGD
RH151 1 2 100_0402_5% VR_SVID_DATA
RH152 1 2 56.2_0402_1% VR_SVID_ALERT#
RH144 1 @ 2 49.9_0402_1% H_CATERR#

CFG[0..19] <6>

UH1E SKYLAKE_HALO Rev_1.0

<17> PCH_CPU_BCLK_P → PCH_CPU_BCLK_P B31 BCLKP
<17> PCH_CPU_BCLK_N → PCH_CPU_BCLK_N A32 BCLKN
<17> PCH_CPU_PCIBCLK_P → PCH_CPU_PCIBCLK_P D35 PCI_BCLKP
<17> PCH_CPU_PCIBCLK_N → PCH_CPU_PCIBCLK_N C36 PCI_BCLKN
<17> CPU_24MHZ_P → CPU_24MHZ_P E31 CLK24P
<17> CPU_24MHZ_N → CPU_24MHZ_N D31 CLK24N

<71> VR_SVID_ALERT# → VR_SVID_ALERT# RH153 1 2 220_0402_5% VR_SVID_ALERT#_R BH31 VIDALERT#
<71> VR_SVID_CLK → VR_SVID_CLK BH32 VIDSCK
<71> VR_SVID_DATA → VR_SVID_DATA BH29 VIDSOUT
<36,59,60,71> H_PROCHOT# → H_PROCHOT# RH158 1 2 499_0402_1% H_PROCHOT#_R BR30 PROCHOT#
DDR_VTT_PG_CTRL BT13 DDR_VTT_CNTL

<6,18> H_VCCST_PWRGD → H_VCCST_PWRGD RH154 1 2 60.4_0402_1% VCCST_PWRGD_CPU H13 VCCST_PWRGD
<18> H_CPUPWRGD → H_CPUPWRGD BT31 PROCPWRGD
<6,16> PLTRST_CPU# → PLTRST_CPU# BP35 RESET#
<16> H_PM_SYNC_R → H_PM_SYNC_R BM34 PM_SYNC
<16> H_PM_DOWN → H_PM_DOWN RH155 1 @ 2 20_0402_5% H_PM_DOWN_R BP31 PM_DOWN
<16,36> PECI_EC → PECI_EC RH190 1 @ 2 0_0402_5% PECI_EC_R BT34 PECI
<16> H_THERMTRIP#_R → H_THERMTRIP#_R J31 THERMTRIP#
<16> PROC_DETECT# → PROC_DETECT# RH89 1 @ 2 0_0402_5% BR33 SKTOCC#
BN1 PROC_SELECT#
H_CATERR# BM30 CATERR#

DVT2.0
Change RH190 to 0ohm 0402 short-pad footprint.

BPM#[0] BT27 XDP_BPM#1 <6>
BPM#[1] BM31
BPM#[2] BT30
BPM#[3]

PROC_TDO BL32 CPU_XDP_TDO <6>
PROC_TDI BP28 CPU_XDP_TDI <6>
PROC_TMS BP28 CPU_XDP_TMS <6>
PROC_TCK BR28 CPU_XDP_TCK <6,18>
PROC_TRST# BP30 CPU_XDP_TRST# <6,22>
PROC_PREQ# BL30 XDP_PREQ# <6,22>
PROC_PRDY# BP27 XDP_PRDY# <6,22>
CFG_RCOMP BT25 CFG_RCOMP

5 OF 14
SKL_H_BGA1440

RH59 49.9_0402_1%

+1.2V_DDR
CH197 0.1U_0402_10V7K
+3VS
RH93 220K_0402_5%
UC1 74AUP1G07SE-7_SOT353
DDR_VTT_PG_CTRL
<62> SM_PG_CTRL → SM_PG_CTRL

SA00007WE00

Reserve for ESD
H_VCCST_PWRGD CH210 @ESD@ 100P_0402_50V8J
H_PROCHOT#_R CH211 100P_0402_50V8J

UH1K SKYLAKE_HALO Rev_1.0

<22> PCH_TRIGGER → PCH_TRIGGER RH167 1 2 30_0402_5% PCH_TRIGGER_R H23 PROC_TRIGIN
<22> CPU_TRIGGER → CPU_TRIGGER RH192 1 2 30_0402_5% CPU_TRIGGER_R J23 PROC_TRIGOUT

11 OF 14
SKL_H_BGA1440

Security Classification	Compal Secret Data		
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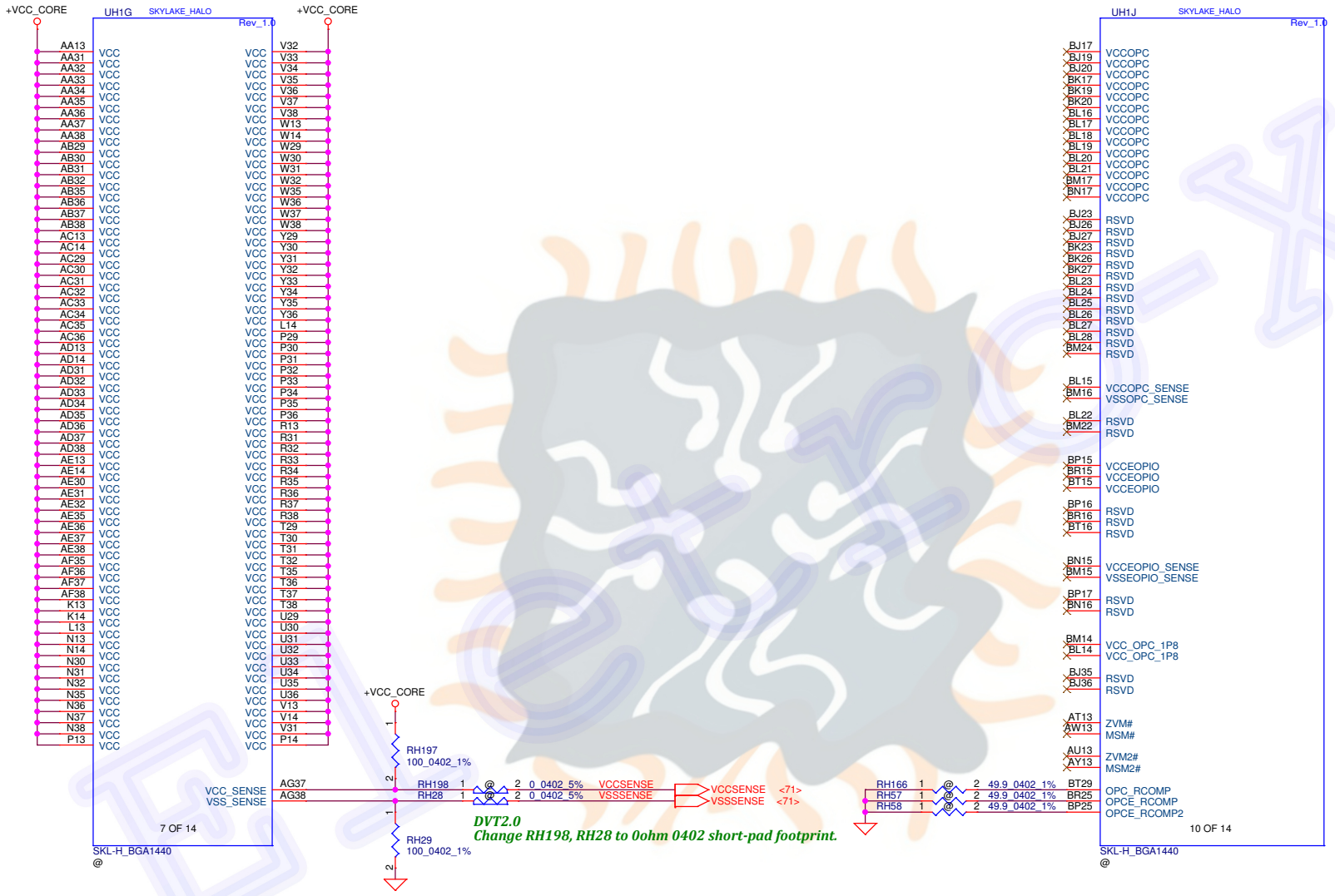
Compal Electronics, Inc.
Title: PROCESSOR(4/7) RSVD,CFG
Size: Custom
Document Number: LA-E992P
Rev: 1.0(A00)
Date: Tuesday, July 25, 2017 Sheet 9 of 77

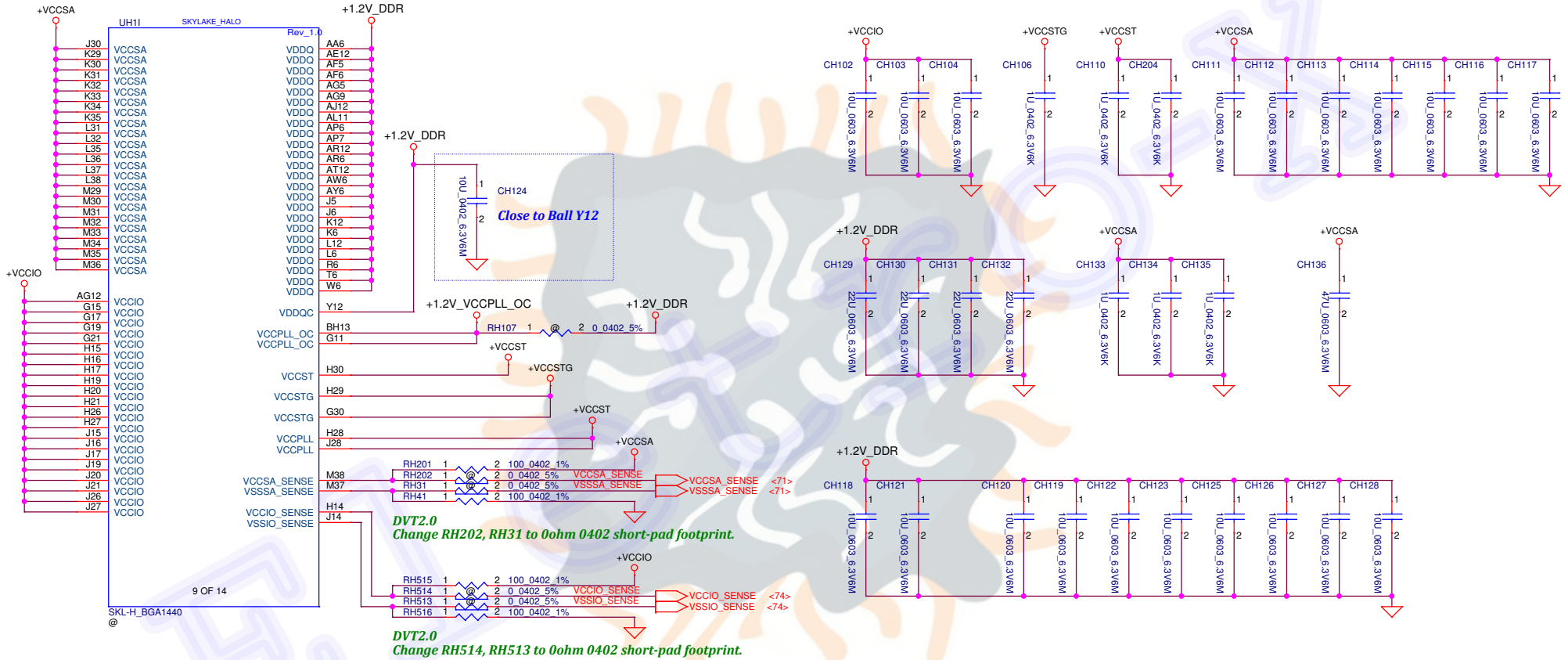


Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Title: PROCESSOR(5/7) PWR,BYPASS

Size: Custom | Document Number: LA-E992P | Rev: 1A0.0

Date: Tuesday, July 25, 2017 | Sheet 10 of 77



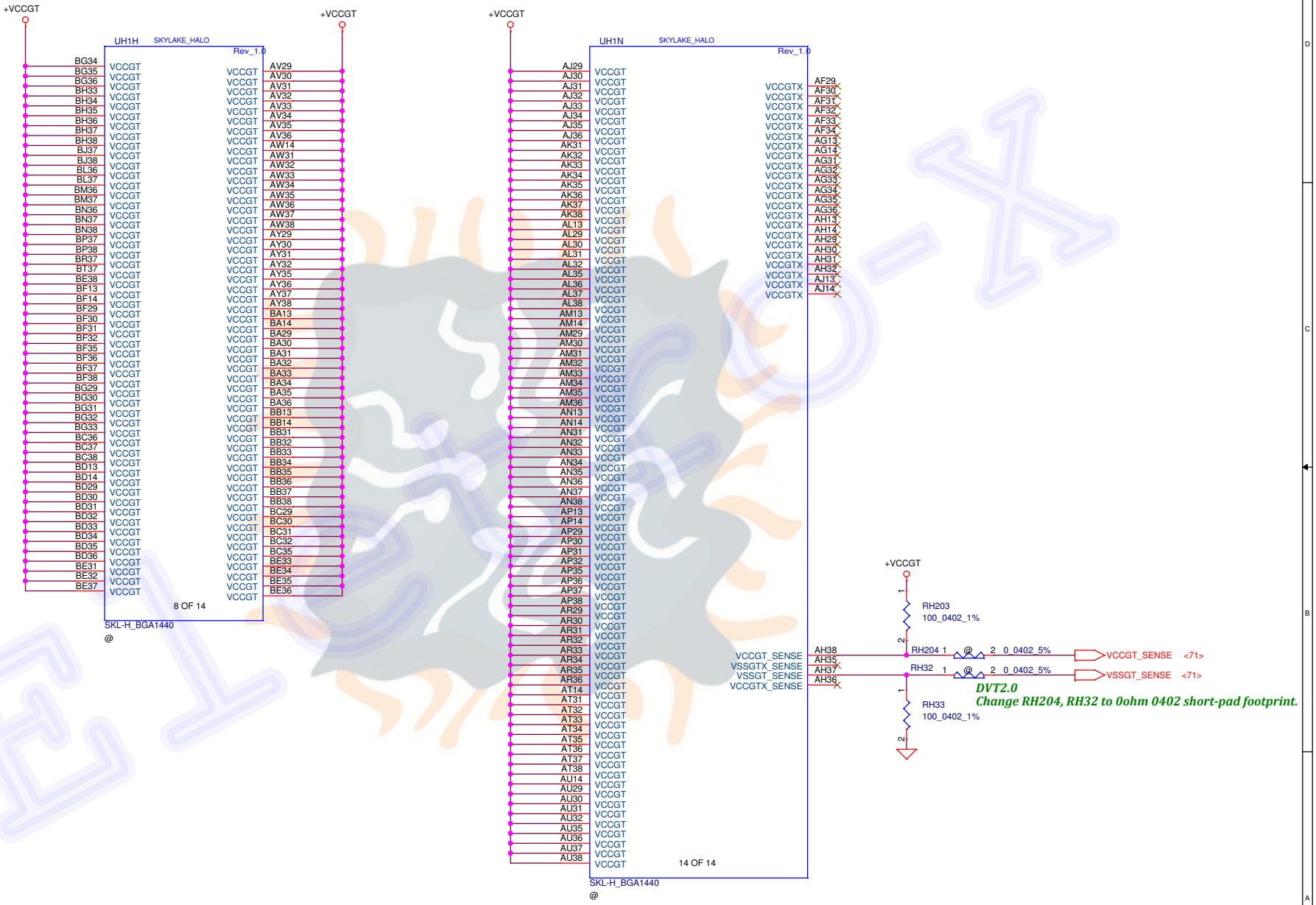
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: PROCESSOR(6/7) PWR

Size: Custom | Document Number: LA-E992P | Rev: 1.0

Date: Tuesday, July 25, 2017 | Sheet 11 of 77

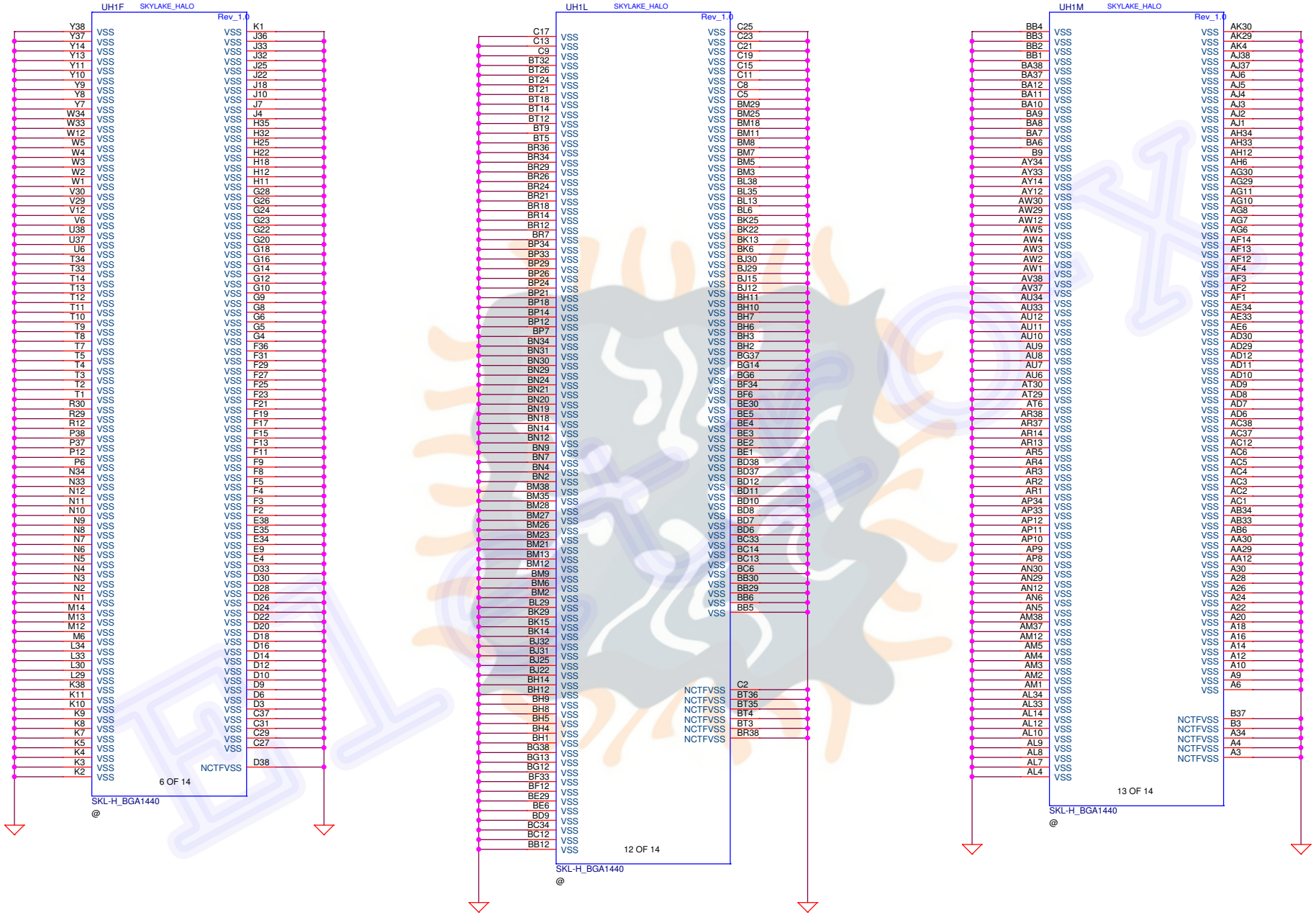


Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Title: PROCESSOR(2/7) PM,XDP,CL

Size: Custom | Document Number: LA-E992P | Rev: 1A0.0

Date: Tuesday, July 25, 2017 | Sheet 12 of 77

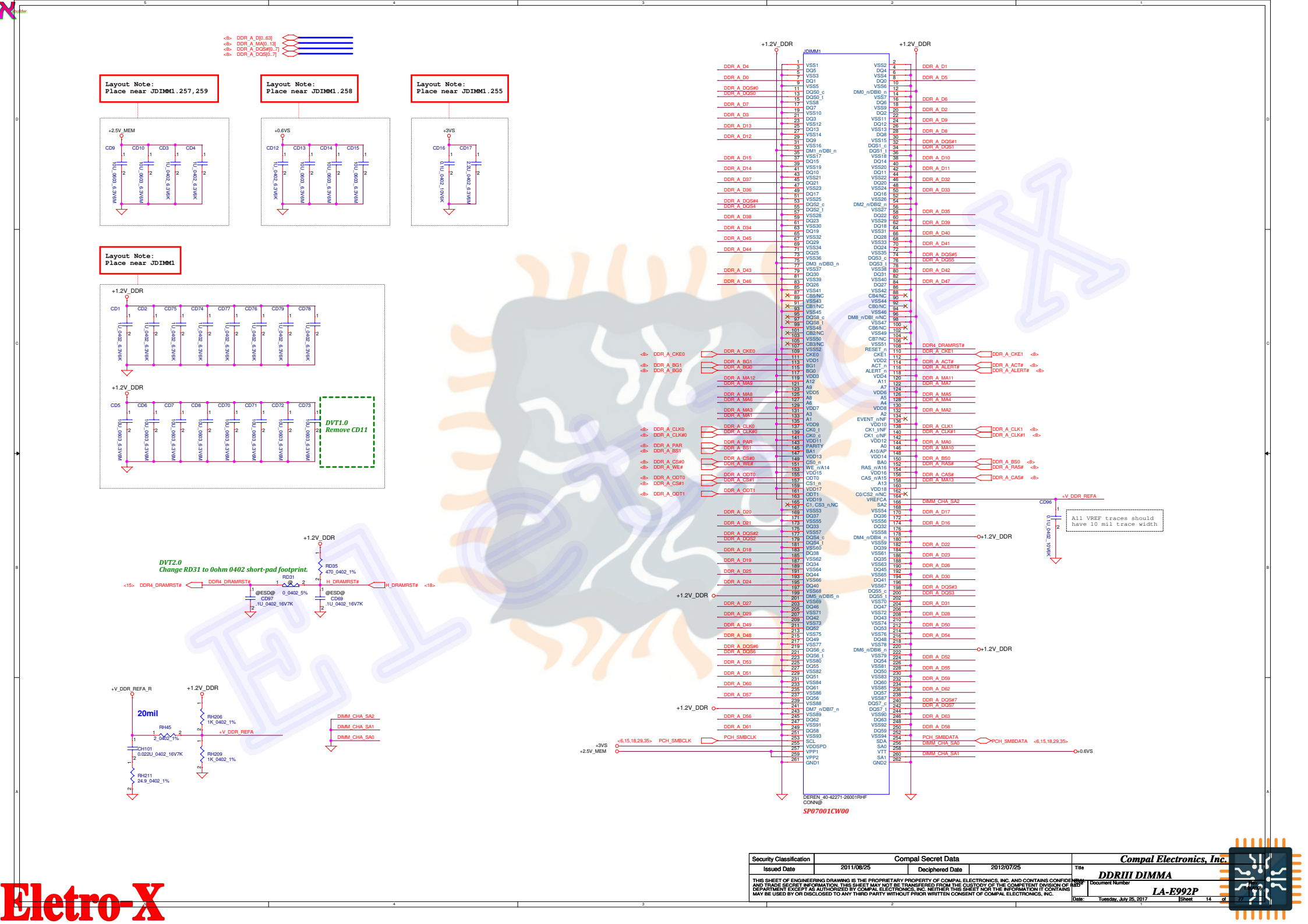


Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

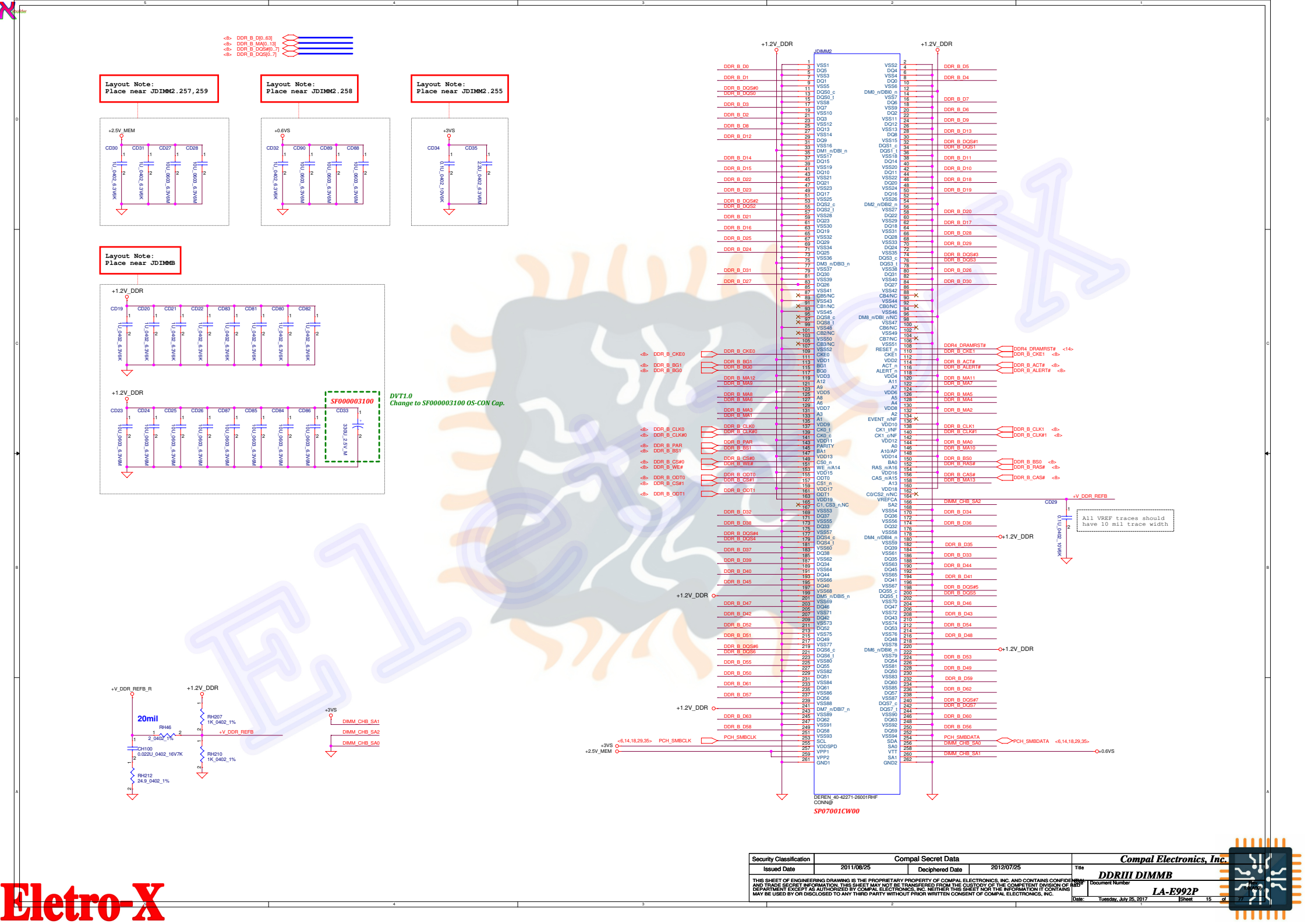
Title: PROCESSOR(7/7) VSS

Size: Custom | Document Number: LA-E992P | Rev: 1.0

Date: Tuesday, July 25, 2017 | Sheet 13 of 77



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date 2012/07/25	Title: DDRIII DIMMA
			Document Number: LA-E992P
			Date: Tuesday, July 25, 2017 Sheet 14 of 77



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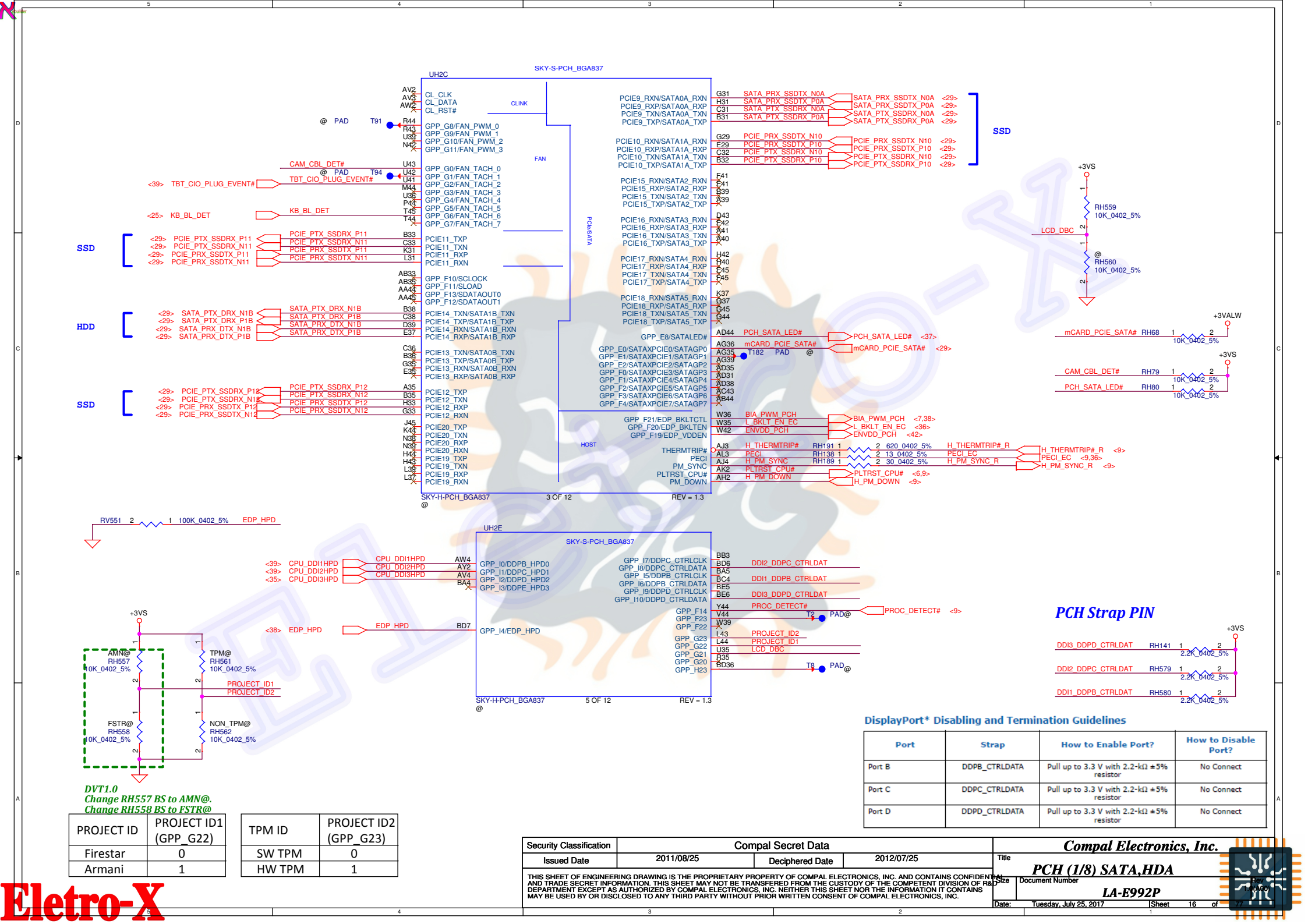

PCH Strap PIN

DisplayPort* Disabling and Termination Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
Port B	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port C	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port D	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect

DVT1.0
Change RH557 BS to AMN@.
Change RH558 BS to FSTR@

PROJECT ID	PROJECT ID1 (GPP_G22)
Firestar	0
Armani	1

TPM ID	PROJECT ID2 (GPP_G23)
SW TPM	0
HW TPM	1

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

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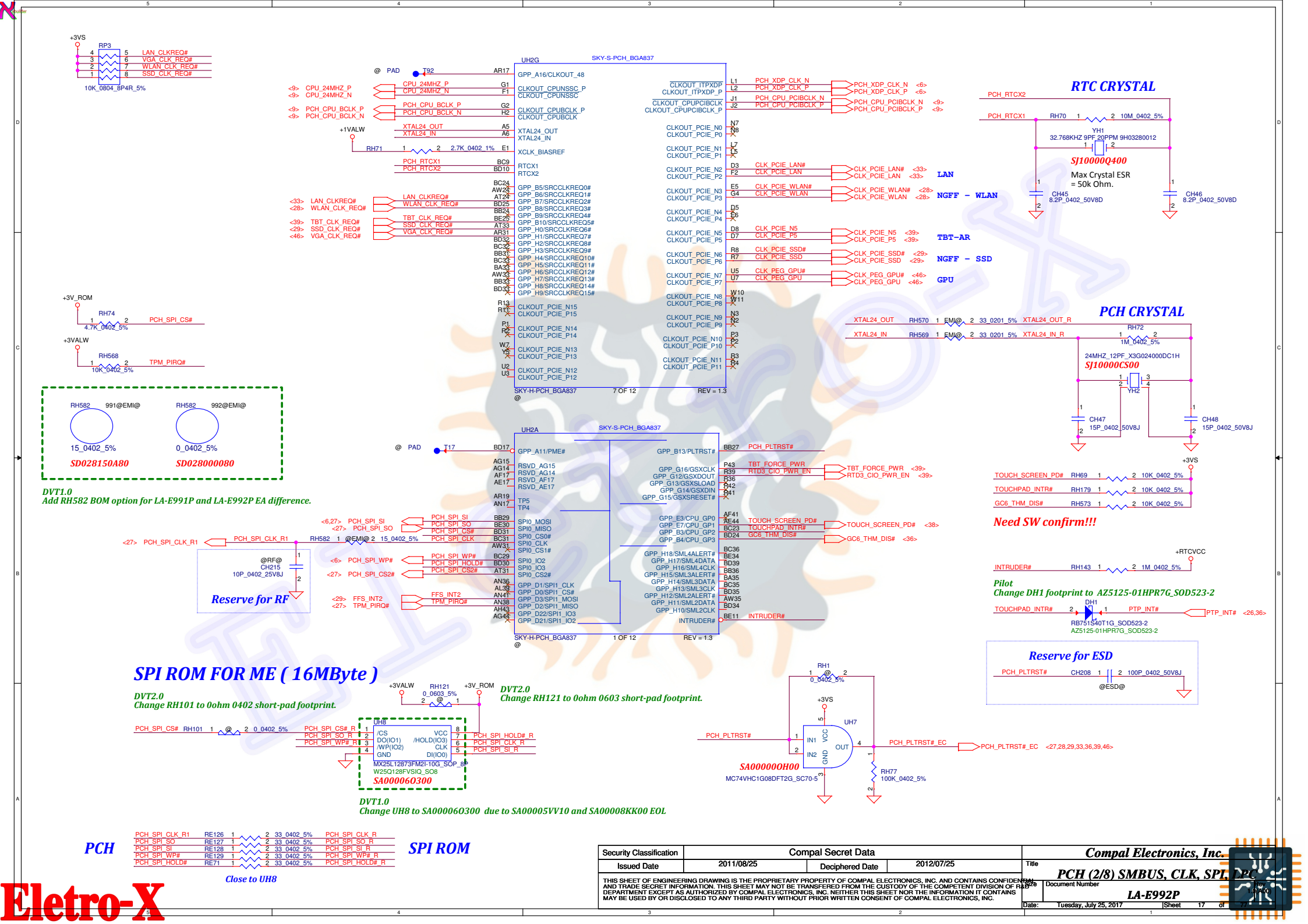
Title: PCH (1/8) SATA,HDA

Size | Document Number: LA-E992P | Rev: 1.0

Date: Tuesday, July 25, 2017 | Sheet 16 of 77



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Issued Date	2011/08/25	Deciphered Date	2012/07/25

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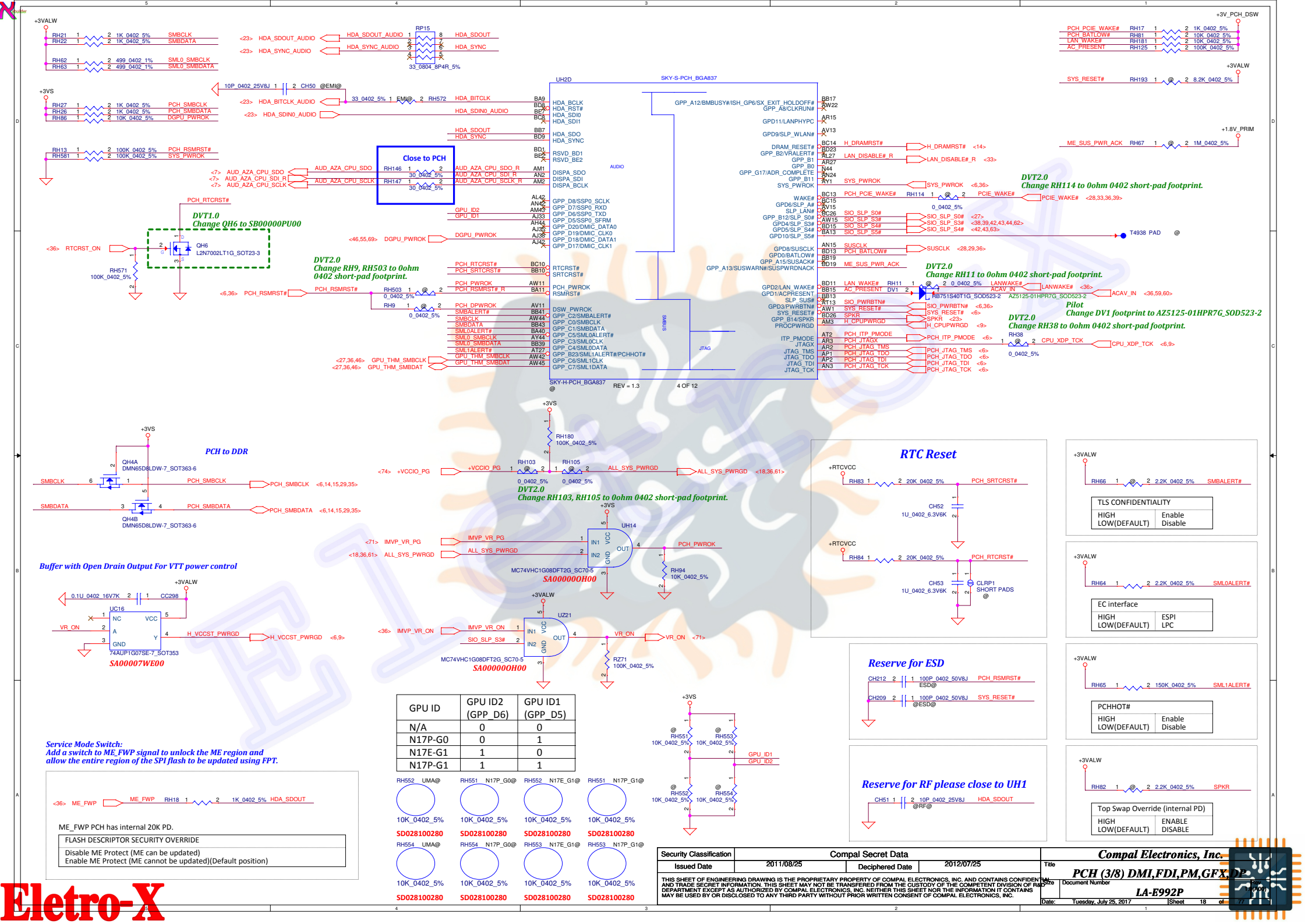
Compal Electronics, Inc.

Title: PCH (2/8) SMBUS, CLK, SPI, DPC

Size: B | Document Number: LA-E992P | Rev: 1.0A

Date: Tuesday, July 25, 2017 | Sheet 17 of 77


UH2D
SKY-S-PCH_BGA837
SKY-H-PCH_BGA837
REV = 1.3
4 OF 12
Close to PCH
DVT1.0
Change QH6 to SB00000PU00
DVT2.0
Change RH9, RH503 to 0ohm
0402 short-pad footprint.
DVT2.0
Change RH114 to 0ohm 0402 short-pad footprint.
DVT2.0
Change RH11 to 0ohm 0402 short-pad footprint.
DVT2.0
Change RH38 to 0ohm 0402 short-pad footprint.
Pilot
Change DV1 footprint to AZ5125-01HPR7G_SOD523-2
DVT2.0
Change RH103, RH105 to 0ohm 0402 short-pad footprint.
PCH to DDR
RTC Reset
Buffer with Open Drain Output For VTT power control
SA00000OH00
SA00007WE00
Reserve for ESD
Reserve for RF please close to UH1
Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and
allow the entire region of the SPI flash to be updated using FPT.
ME_FWP PCH has internal 20K PD.
FLASH DESCRIPTOR SECURITY OVERRIDE
Disable ME Protect (ME can be updated)
Enable ME Protect (ME cannot be updated)(Default position)
TLS CONFIDENTIALITY
HIGH Enable
LOW(DEFAULT) Disable
EC interface
HIGH ESPI
LOW(DEFAULT) LPC
PCHHOT#
HIGH Enable
LOW(DEFAULT) Disable
Top Swap Override (internal PD)
HIGH ENABLE
LOW(DEFAULT) DISABLE
GPU ID | GPU ID2 (GPP_D6) | GPU ID1 (GPP_D5)
N/A | 0 | 0
N17P-G0 | 0 | 1
N17E-G1 | 1 | 0
N17P-G1 | 1 | 1
SD028100280
Security Classification: Compal Secret Data
Issued Date: 2011/08/25
Deciphered Date: 2012/07/25
Compal Electronics, Inc.
PCH (3/8) DMI,FDI,PM,GFX,DP
LA-E992P
Tuesday, July 25, 2017
Sheet 18 of 77

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

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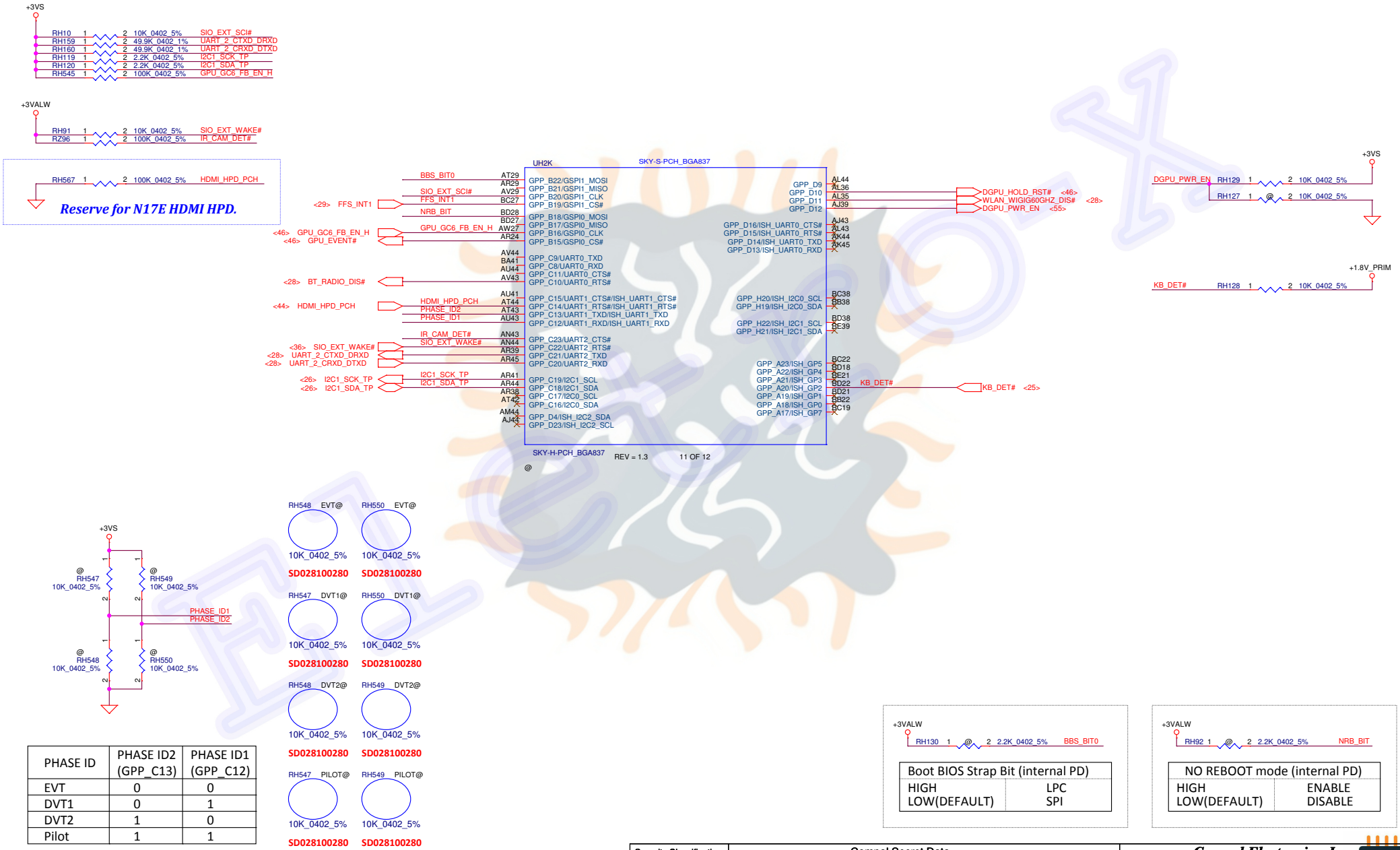
Compal Electronics, Inc.

Title: PCH (4/8) PCI, USB

Size: C | Document Number: LA-E992P | Rev: 1.0

Date: Tuesday, July 25, 2017 | Sheet 19 of 77



PHASE ID	PHASE ID2 (GPP_C13)	PHASE ID1 (GPP_C12)
EVT	0	0
DVT1	0	1
DVT2	1	0
Pilot	1	1

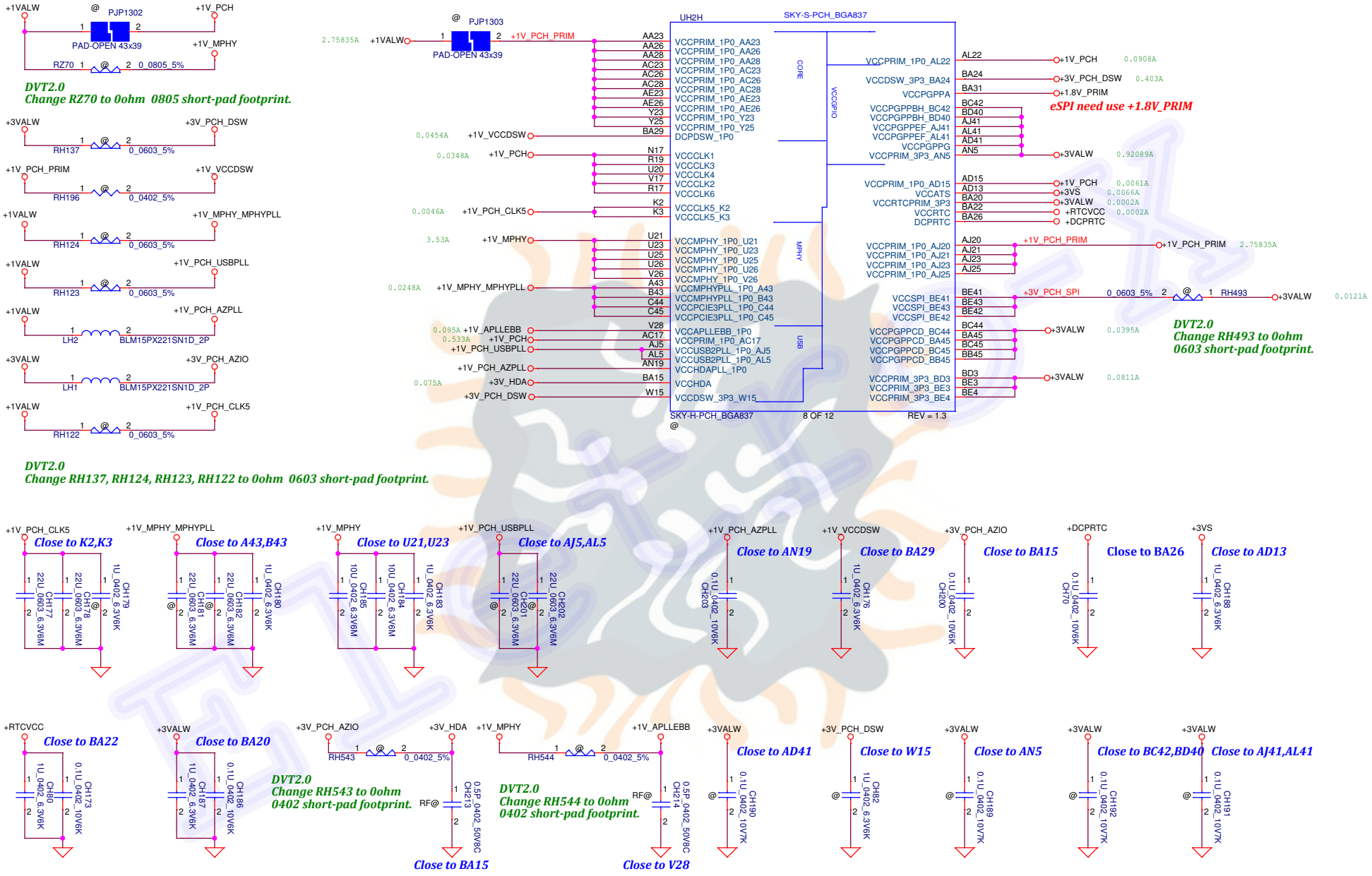
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: PCH (5/8) GPIO, CPU, MISC

Size: B | Document Number: LA-E992P | Rev: 1.0

Date: Tuesday, July 25, 2017 | Sheet 20 of 77



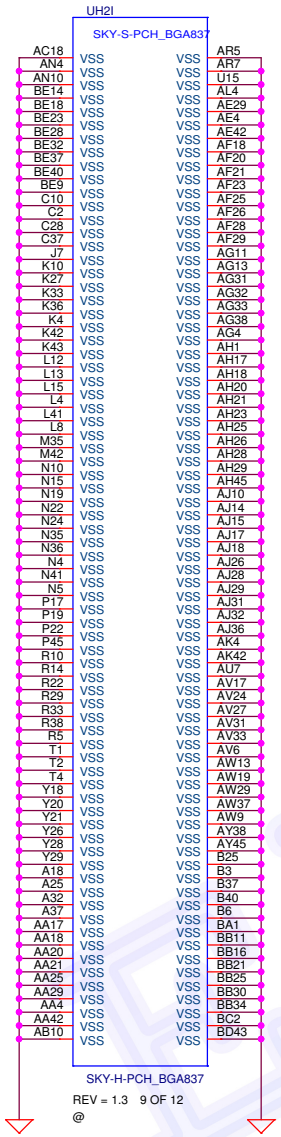
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

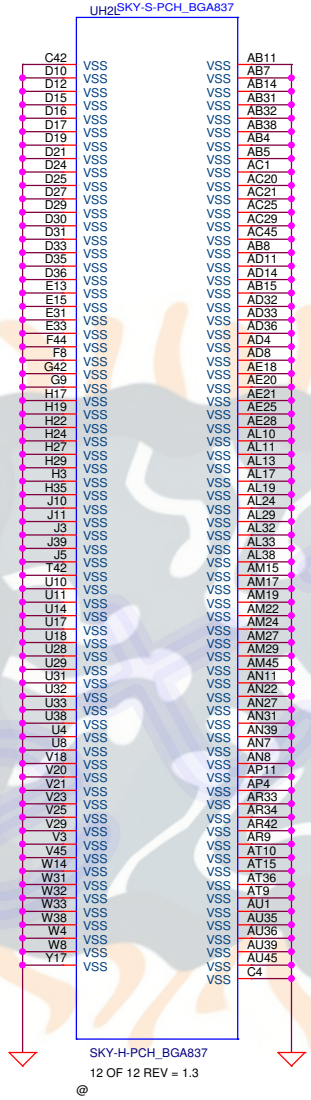
Compal Electronics, Inc.

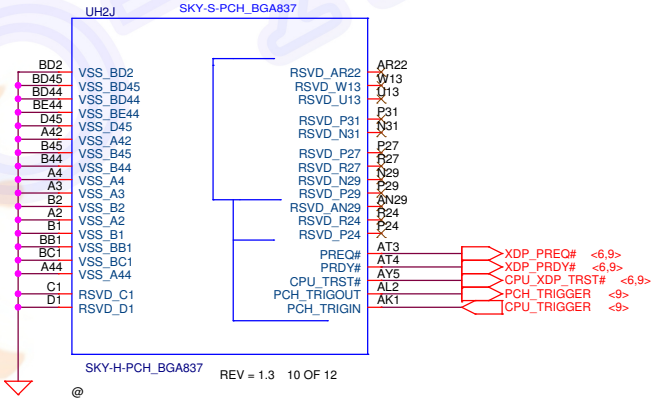
Title: PCH (6/8) PWR

Size | Document Number: LA-E992P | Rev: 1.0

Date: Tuesday, July 25, 2017 | Sheet 21 of 77







Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: PCH (8/8) VSS

Size: | Document Number: LA-E992P | Rev: 1.0

Date: Tuesday, July 25, 2017 | Sheet 22 of 77

Main Func = Audio

Pilot
Change RA1 to 0ohm 0402 short-pad footprint.

+1.8V_PRIM — QA1 N2306LT1G_SOT23-3 — RA58 @ 0_0603_5% — +3VS

DVT2.0
Reserve RA58

+1.8V_DVDD — RA1 @ 0_0402_5% — +1.8V_AVDD

CA3 0.1U_0402_10V6K — **Close pin36**

CA1 4.7U_0603_6.3V6K — CA2 0.1U_0402_10V6K — AUD_AGND

DVT2.0
Pop CA7, UA1, RA2, CA10, CA4,RA57

+1.8V_DVDD — RA57 @ 0_0603_5% — +1.8VS

UA1 G9090-180T11U_SOT23-5 (VIN, VOUT, GND, NC, EN) — **SA00004Z400**

RA2 10K_0402_5% — CA10 0.22U_0603_25V7K — CA4 1U_0402_6.3V6K — CA7 1U_0402_6.3V6K

Pilot
Change RA57 to 0ohm 0603 short-pad footprint.

+3VS — RA5 @ 0_0402_5% — +3V_DVDD

CA8 4.7U_0603_6.3V6K — CA9 0.1U_0402_10V6K — **Close pin9**

25mA

Pilot
Change RA5 to 0ohm 0402 short-pad footprint.

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

HDA1 — ALC3246-CG-GP — **SA00008GJ00**

<24> LINE1_VREFO_R
<24> LINE1_VREFO_L
<24> AUD_HP1_JACK_L
<24> AUD_HP1_JACK_R

CA15 1U_0603_10V6K — CPVEE — CBN — CBP
CA20 1U_0603_10V6K — +1.8V_DVDD
CA16 2.2U_0402_6.3V6M — CA19 4.7U_0603_6.3V6K — LDO1_CAP — +5V_AVDD — AUD_AGND
RA11 100K_0402_5%
MIC2_VREFO <24>

AUD_AGND — CA22 10U_0603_6.3V6M — LDO2_CAP
AUD_AGND — CA63 10U_0603_6.3V6M — +1.8V_AVDD
+5V_PVDD

<24> AUD_SPK_L+
<24> AUD_SPK_L-
<24> AUD_SPK_R-
<24> AUD_SPK_R+
+5V_PVDD

<36> EC_MUTE# — RA23 @ 100K_0402_5% — +3V_DVDD

LINE2_L — LINE2_R — LINE1_L — LINE1_R — 5/3D3VSTB — MIC-CAP — MIC2_R/SLEEVE — MIC2_L/RING2 — MONO-OUT — SPDIFO/FRONT_JD/JD3/GPIO3 — MIC2/LINE2_JD/JD2 — HP/LINE1_JD/JD1

LINE1_L <24> — LINE1_R <24> — SLEEVE <24> — RING2 <24>

CA23 10U_0402_6.3V6M — AUD_AGND

Layout Note:
Width>40mil, to improve Headpohone Crosstalk noise
Change it to sharp will be better.
Add 2 vias (>0.5A) when trace layer change.

RA19 @ 0_0402_5% — AUD_PC_BEEP

DVT2.0
Change RA19 to 0ohm 0402 short-pad footprint.

AUD_SENSE_A — RA22 200K_0402_5% — AUD_SENSE — AUD_SENSE <24>

Place close to Pin 13

moat

+3VALW — +RTCVCC

Pop RA18 to prevent "zizi" noise on G3 or DC S5/S4.

RA17 — RA18 — 0_0402_5%

AUD_SENSE_A — RA24 100K_0402_5% — +3V_DVDD
CA24 0.1U_0402_10V6K — AUD_AGND

DMIC_DATA_R — CA62 10P_0402_25V8J

+3V_DVDD — CA25 4.7U_0603_6.3V6K — CA26 0.1U_0402_10V6K

LDO3_CAP — CA27 4.7U_0603_6.3V6K — CA28 0.1U_0402_10V6K — +3V_DVDD

DVT 1.0
Change RA27 to 33 ohm.

<38> DMIC_DAT — RA27 33_0402_5% — DMIC_DATA_R — DMIC_CLK_R

<38> DMIC_CLK — LA1 EMI@ BLM15PX471SN1D_2P

@RF@ CA30 47P_0402_50V8J

Reserve for RF
Close pin3

DVT 2.0
EMI request change LA1 to 470 ohm bead to depress EMI rediation.

<18> HDA_SDOUT_AUDIO — HDA_SDOUT_AUDIO
<18> HDA_BITCLK_AUDIO — HDA_BITCLK_AUDIO
<18> HDA_SDIN0_AUDIO — RA32 33_0402_5% — HDA_CODEC_SDIN0
<18> HDA_SYNC_AUDIO — HDA_SYNC_AUDIO

@RF@ CA66 10P_0402_25V8J

Reserve for RF

<18> SPKR — D1 BAT54C-7-F_SOT23-3 — AUD_PC_BEEP_C — RA30 1K_0402_5% — CA29 0.1U_0402_10V6K — AUD_PC_BEEP
<36> BEEP — RA33 10K_0402_5%

+3VS To +1.8V_DVDD

Pilot
Change RA7, RA10 to 0ohm 0805 short-pad footprint.

+5VS — **1.5A** — +5V_PVDD — **5V_PVDD trace width > 40mil.**

RA7 — RA10 — 0_0805_5%

CA11 — CA12 — CA13 — CA14 — 10U_0603_6.3V6M-D — 0.1U_0402_10V6K

Close pin41 **Close pin46**

Pilot
Change RA8 to 0ohm 0603 short-pad footprint.

moat — RA8 0_0603_5% — +5V_AVDD

CA18 4.7U_0603_6.3V6K — CA17 0.1U_0402_10V6K — **Place close to Pin 26** — AUD_AGND

moat

Pilot
Change RA9, RA12, RA13, RA14, RA15 to 0ohm 0402 short-pad footprint.

RA9 — RA12 — RA13 — RA14 — RA15 — 0_0402_5% — AUD_AGND

Pilot
Change RA16 to 0ohm 0805 short-pad footprint.

RA16 @ 0_0805_5% — AUD_AGND

Security Classification	Compal Secret Data		
Issued Date	2015/07/15	Deciphered Date	2016/07/31

Compal Electronics, Inc.

Title: CODEC ALC3246

Size: — Document Number: LA-E992P — Rev: 1.0

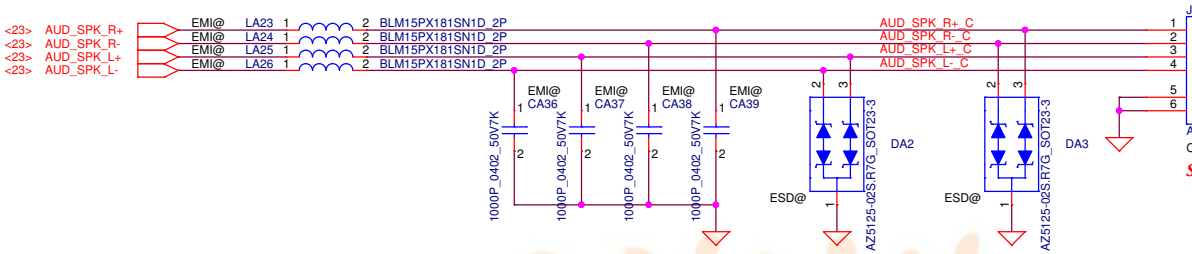
Date: Tuesday, July 25, 2017 — Sheet 23 of 77

Main Func = Audio

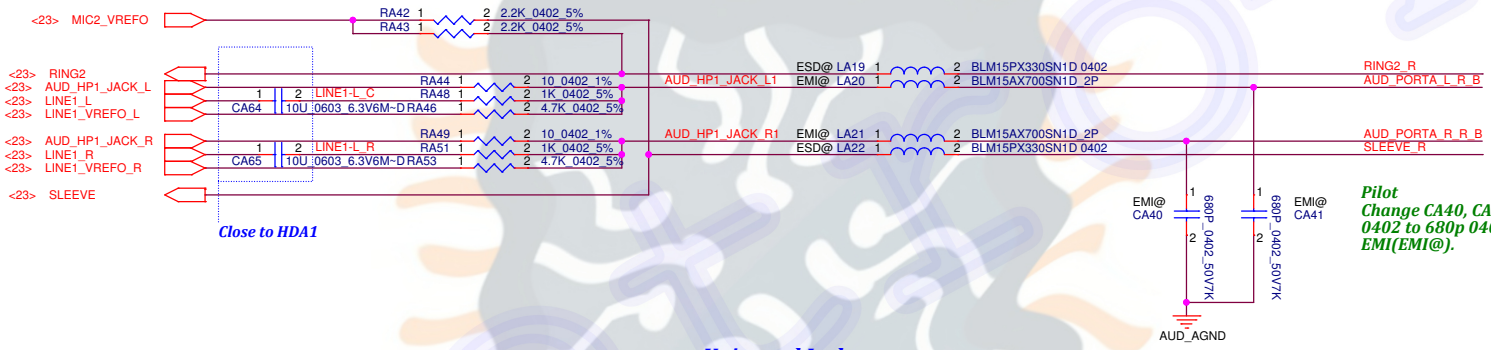
Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

Need to check Speaker pin define

Speaker



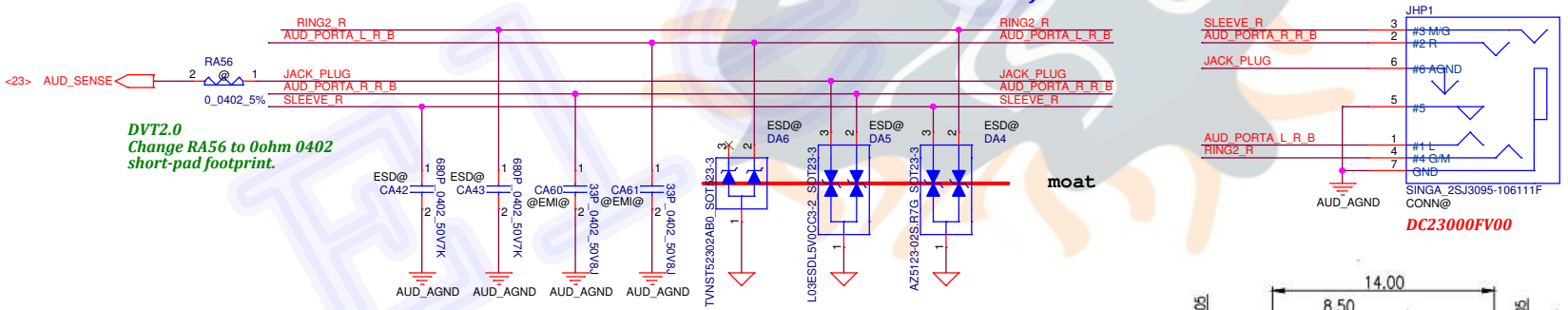
CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-



Close to HDA1

Pilot
Change CA40, CA41 from 100p 0402 to 680p 0402 and pop for EMI(EMI@).

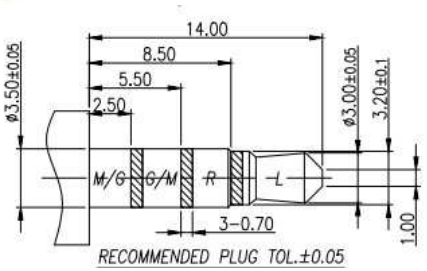
Universal Jack

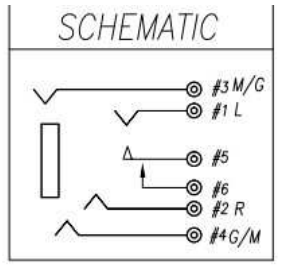


DVT2.0
Change RA56 to 0ohm 0402 short-pad footprint.

DC23000FV00

SINGA_2SJ3095-106111F





Pilot
Change connect CA42.2, CA43.2, CA60.2, CA61.2 from GND to AGND.
Change CA60, CA61 BS from EMI@ to @EMI@ reserve for EMI.

10 mils 10 mils

Security Classification	Compal Secret Data		
Issued Date	2015/07/15	Deciphered Date	2016/07/31

Compal Electronics, Inc.

Title: **SPKR/JACK**

Size: | Document Number: **LA-E992P** | Rev: 1.0

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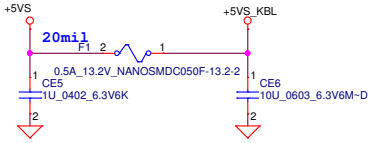
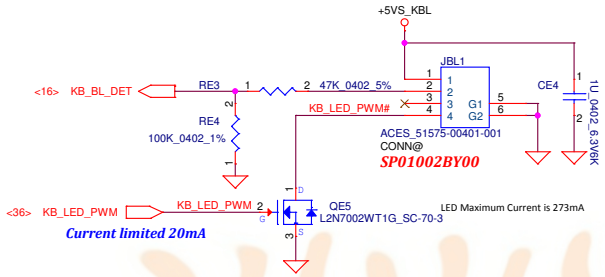
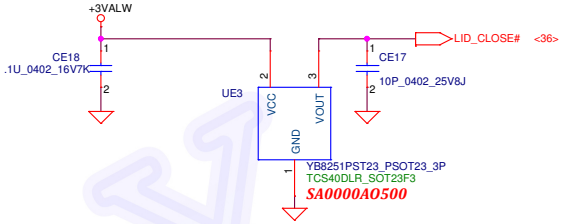
Fuse for Backlight



Connector for Keyboard Backlight

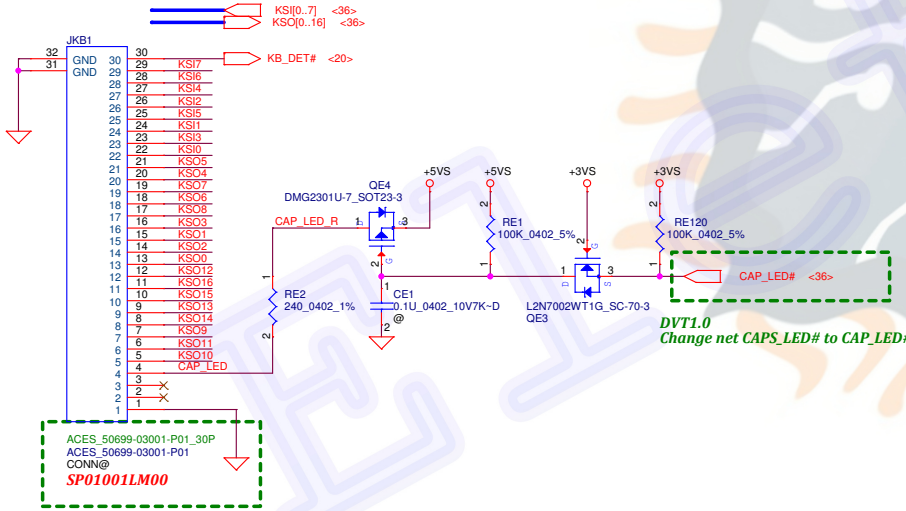


Lid Switch



Pilot
Change UE3 from SA00009CB00 TCS40DLR to SA0000AO500 YB8251PST23

Connector for Keyboard



DVT1.0
Change net CAPS_LED# to CAP_LED#

DVT1.0
Change to symbol ACES_50699-03001-P01

Connector for Touch Finger Print module. (Cancel)

DVT1.0
Remove Finger print connector and component.

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: KB/Lid/Finger Print

Size: B | Document Number: LA-E992P | Rev: 1.0

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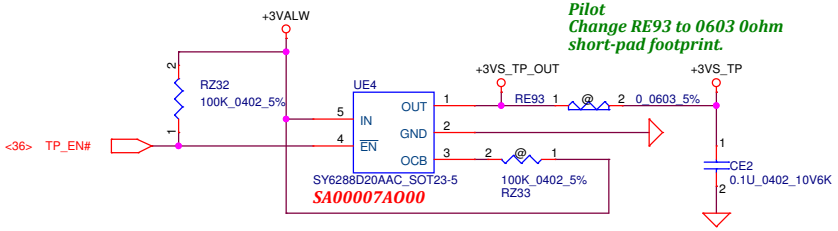
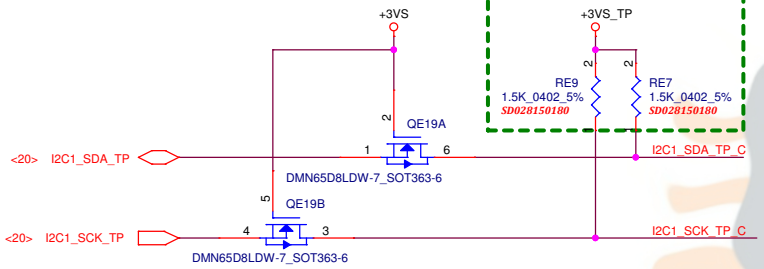
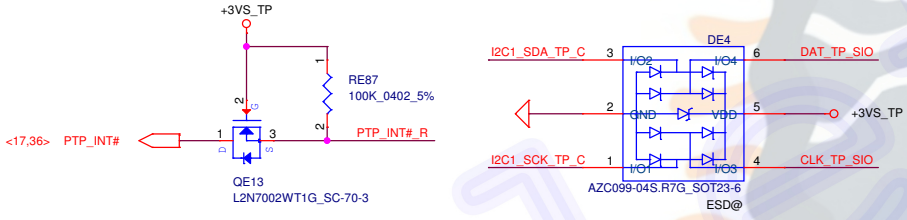
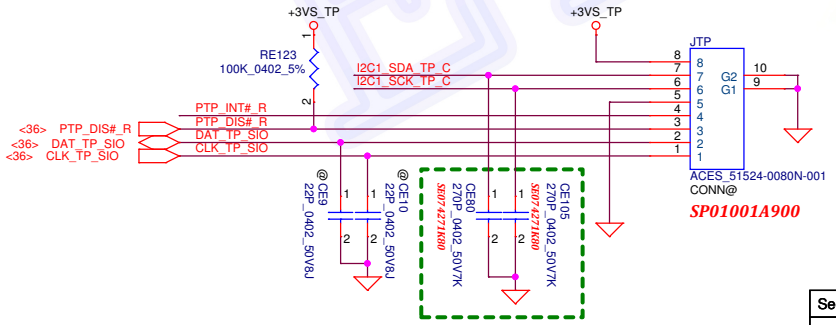
Touch pad

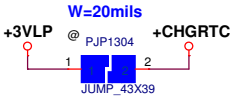


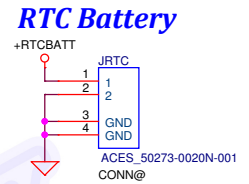


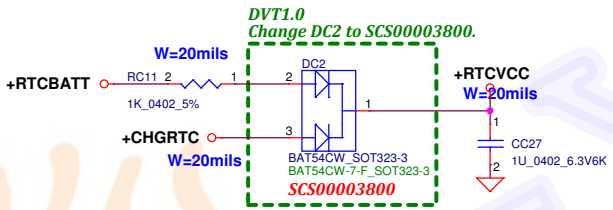




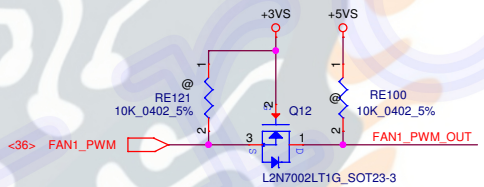
RTC Battery non- Charge Function

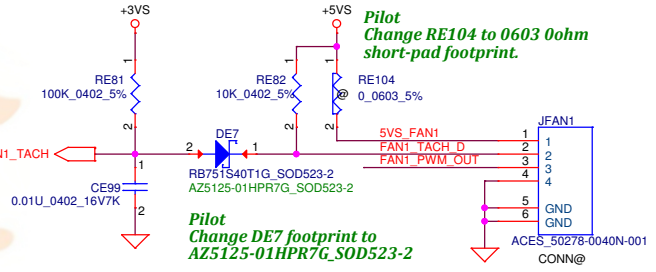


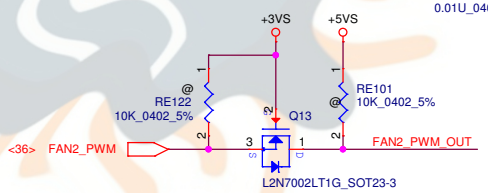


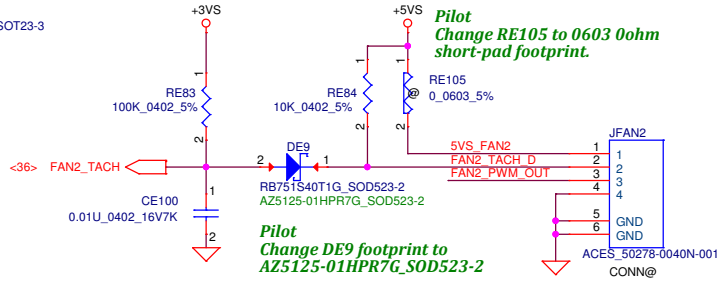


PWM FAN









Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: FAN/TP/KB/PWR SW

Size: Custom | Document Number: LA-E992P | Rev: 1.0

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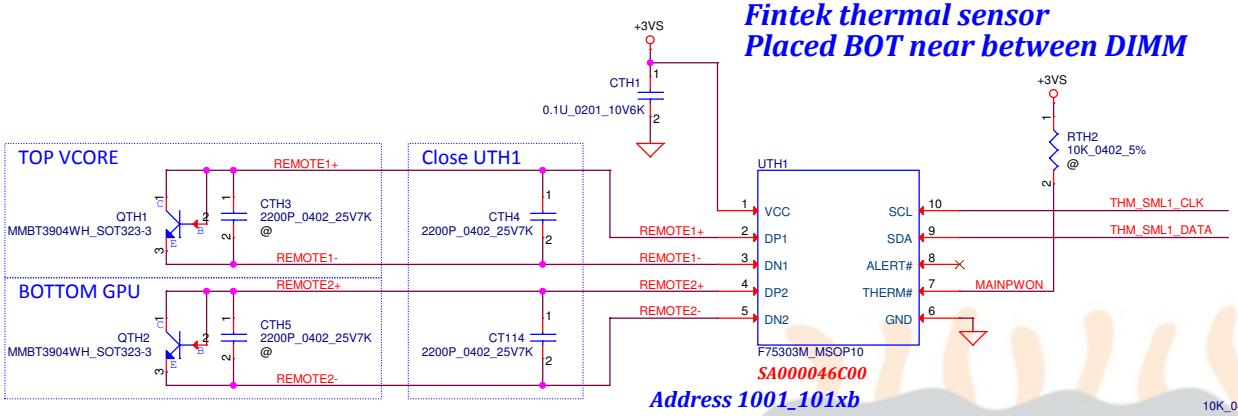
Thermal Sensor

Fintek thermal sensor
Placed BOT near between DIMM



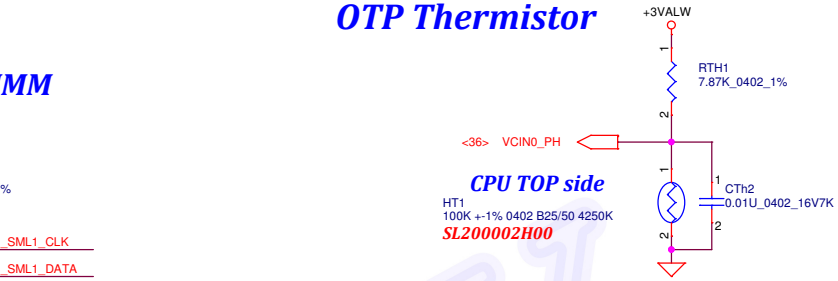
SA000046C00

Address 1001_101xb

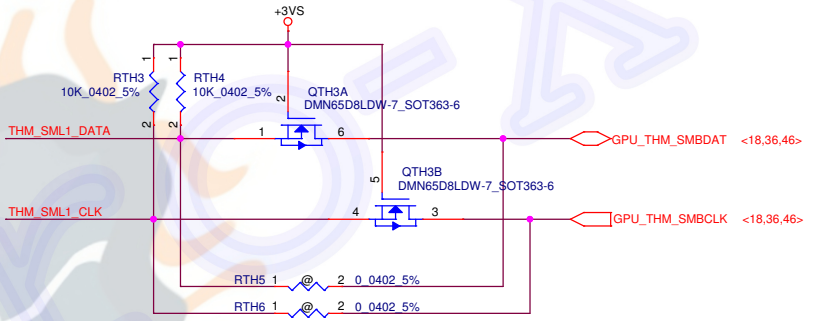
2nd source
SA000029210-->EMC1403-2-AIZL-TR

REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"

OTP Thermistor



Main SL200000U00 S THERM_100K +-1% TSM0B104F4251RZ 0402 Thinking
2nd SL200001J00 S THERM_100K +-1% ERTJ0ER104F 0402 Panasonic
3rd SL200000V00 S THERM_100K +-1% NCP15WF104F03RC 0402 MURATA



TPM

DVT1.0
Add RTPM5 BOM option for LA-E991P and LA-E992P EA difference.

RTPM5 991@TPM@
27_0402_5%
SD028270A80

RTPM5 992@TPM@
33_0402_5%
SD028330A80

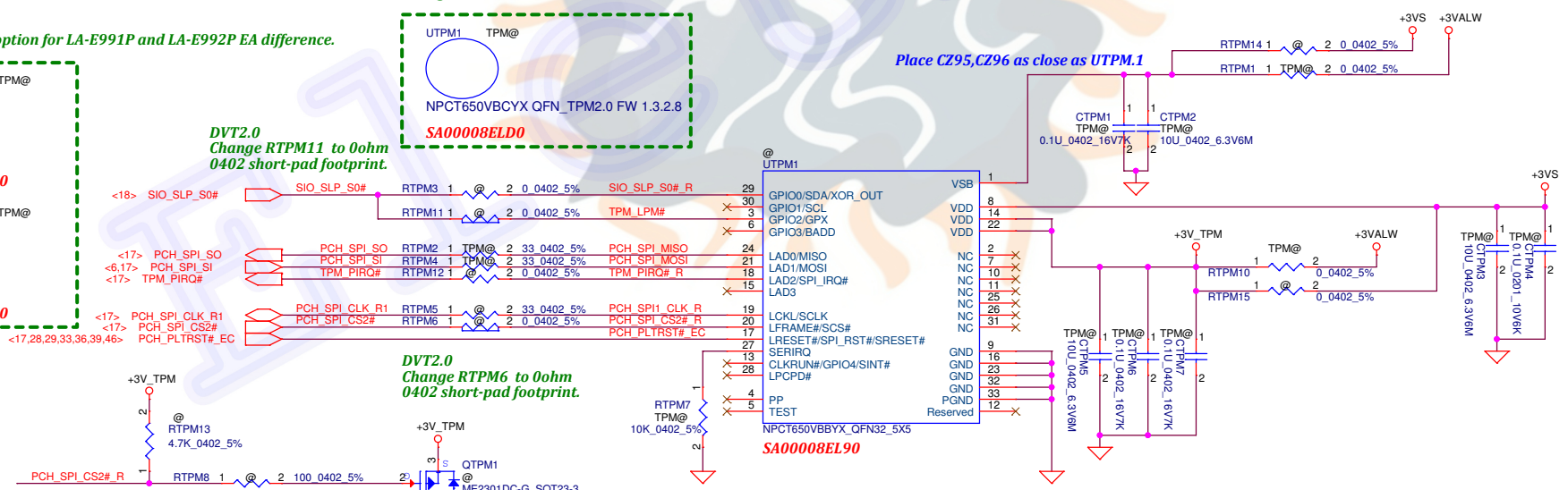
DVT1.0
Change TPM to NPCT650VBCYX with new FW version.

UTPM1 TPM@
NPCT650VBCYX QFN_TPM2.0 FW 1.3.2.8
SA00008ELD0

DVT2.0
Change RTPM11 to 0ohm
0402 short-pad footprint.

DVT2.0
Change RTPM6 to 0ohm
0402 short-pad footprint.

Place CZ95,CZ96 as close as UTPM.1

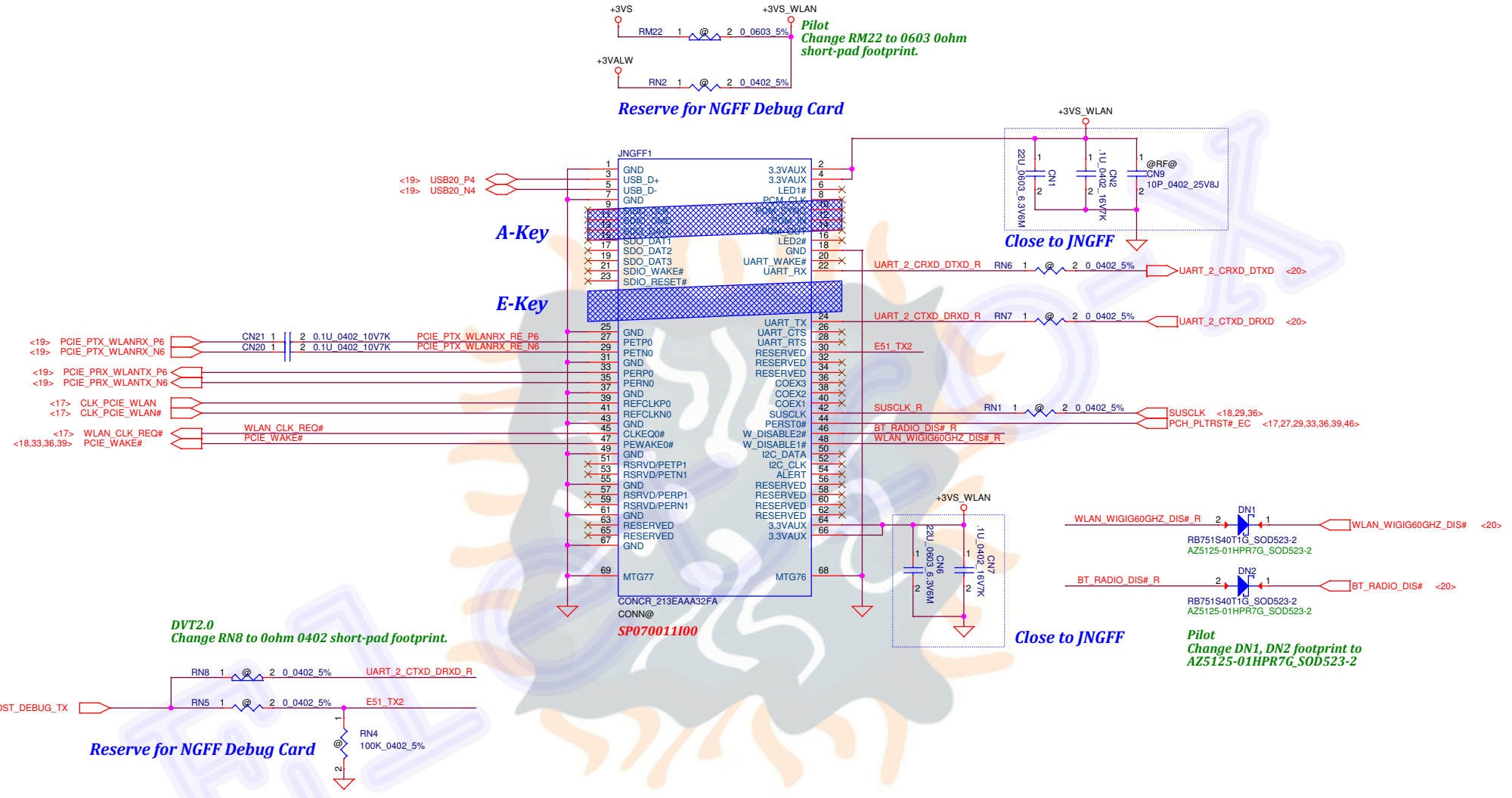


Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

Compal Electronics, Inc.

Title: Thermal Sensor
Size: Document Number: LA-E992P
Rev: 1.0
Date: Tuesday, July 25, 2017 Sheet 27 of 77

M.2 Key-E (WLAN + BT)



Key-E Debug Card Socket

	Standard NGFF pin define	Debug Card NGFF pin define
3.3VAUX	2, 4, 72, 74	2, 4, 56, 58
GND	1, 7, 18, 33, 39, 45, 51, 57, 63, 69, 75	1, 7, 10, 17, 23, 29, 35, 41, 47, 53, 59
NGFF_UART_TX	22	14
NGFF_UART_RX	32	16
EC_TX_P80DATA	38	22
EC_RX_P80CLK	40	24
PLT_RST#	52	36
NGFF_I2C_DATA	58	42
NGFF_I2C_CLK	60	44

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: NGFF-WLAN

Size: Custom | Document Number: LA-E992P | Rev: 1.0

Date: Tuesday, July 25, 2017 | Sheet 28 of 77

M.2 Key-M (SSD)

PCIe SSD

SATA SSD

Pilot
Change RZ36 to 0805
0ohm short-pad footprint.

+3VS — RZ36 1 @ 2 0_0805_5% — +3.3VDX_SSD

JNGFF2

PCIE_PRX_SSDTX_N12 / PCIE_PRX_SSDTX_P12
PCIE_PTX_SSDRX_N12 / PCIE_PTX_SSDRX_P12 — CD37, CD42 0.22U_0402_10V6K — PCIE_PTX_SSDRX_N12_C / PCIE_PTX_SSDRX_P12_C
PCIE_PRX_SSDTX_N11 / PCIE_PRX_SSDTX_P11
PCIE_PTX_SSDRX_N11 / PCIE_PTX_SSDRX_P11 — CD43, CD44 0.22U_0402_10V6K — PCIE_PTX_SSDRX_N11_C / PCIE_PTX_SSDRX_P11_C
PCIE_PRX_SSDTX_N10 / PCIE_PRX_SSDTX_P10
PCIE_PTX_SSDRX_N10 / PCIE_PTX_SSDRX_P10 — CD45, CD46 0.22U_0402_10V6K — PCIE_PTX_SSDRX_N10_C / PCIE_PTX_SSDRX_P10_C
SATA_PRX_SSDTX_P0A / SATA_PRX_SSDTX_N0A
SATA_PTX_SSDRX_N0A / SATA_PTX_SSDRX_P0A — CD53, CD51 0.22U_0402_10V6K — SATA_PTX_SSDRX_N0A_C / SATA_PTX_SSDRX_P0A_C
CLK_PCIE_SSD# / CLK_PCIE_SSD

GND, PERn3, PERp3, PETn3, PETp3, PERn2, PERp2, PETn2, PETp2, PERn1, PERp1, PETn1, PETp1, PERn0/SATA-B+, PERp0/SATA-B-, PETn0/SATA-A-, PETp0/SATA-A+, REFCLKN, REFCLKP

3P3VAUX, NC, DAS/DSS#, DEVSLP, PERST#, CLKREQ#, PEWake#, SUSCLK(32kHz), GND1, GND2

SSD_LED# — SSD_LED# <37>

DVT1.0
Un-pop RD7

RD7 2 @ 1 10K_0402_5% — +3.3VDX_SSD
RD59 1 @ 2 0_0402_5% — mSATA_DEVSLP <19>

DVT2.0
Change RD59 to 0ohm 0402 short-pad footprint.

PCH_PLTRST#_EC <17,27,28,33,36,39,46>
SSD_CLK_REQ# <17>
SSD_PCIE_WAKE# — RD8 1 2 10K_0402_5% — +3.3VDX_SSD

RD9 1 @ 2 0_0402_5% — SUSCLK <18,28,36>

<16> mCARD_PCIE_SATA# — RD58 1 @ 2 0_0402_5%

DVT2.0
Change RD58 to 0ohm
0402 short-pad footprint.

BELLW_SD-80159-4221
CONN@
SP07001D300

RF Reserved.

CD36 4.7U_0603_6.3V6K
CD38 0.1U_0402_10V6K
CD39 0.01U_0402_16V7K
CD40 47P_0402_50V8J
CD41 15P_0402_50V8J

Free Fall Sensor

U5603 FFS@ LNG2DM

VDD_IO, VDD, SDO/SA0, SDA/SDI/SDO, SCL/SPC, CS, RES, INT 1, INT 2, GND, GND, GND

CN19 FFS@ 0.1U_0402_16V7K
CN22 @ 10U_0603_6.3V6M

PCH_SMBDATA / PCH_SMBCLK <6,14,15,18,35>

RS40 100K_0402_5%
RS41 100K_0402_5%

FFS_INT1 / FFS_INT2 — FFS_INT1 <20> / FFS_INT2 <17>

LNG2DMTR_LGA12_2X2
SA000089W00

RS1 FFS@ 100K_0402_5%
RS39 FFS@ 100K_0402_5%

QC5A FFS@ DMN65D8LDW-7_SOT363-6
QC5B FFS@ DMN65D8LDW-7_SOT363-6

FFS_INT2_Q

HDD CONN

Pilot
Change RZ34 to 0805
0ohm short-pad footprint.

+5VS — RZ34 1 @ 2 0_0805_5% — +5VS_HDD

DVT2.0
Change JHDD1 to ACES_51625-01201-001

JHDD1

SATA_PTX_DRX_P1B / SATA_PTX_DRX_N1B — CS28, CS27 0.01U_0402_16V7K — SATA_PTX_DRX_P1B_RC / SATA_PTX_DRX_N1B_RC
SATA_PRX_DTX_N1B / SATA_PRX_DTX_P1B — CS25, CS26 0.01U_0402_16V7K — SATA_PRX_DTX_N1B_RC / SATA_PRX_DTX_P1B_RC

HDD_DEVSLP — RD62 1 @ 2 0_0402_5% — HDD_DEVSLP_R
FFS_INT2_Q
+5VS_HDD

GND, GND

CONN@
ACES_51625-01201-001
SP010028W00

Place near HDD CONN (JHDD1)

+5VS_HDD
CS12 1000P_0402_50V7K
CS13 0.1U_0402_10V6K
CS14 1U_0402_6.3V6K
CS15 10U_0603_6.3V6M

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: SSD/HDD

Size: Custom | Document Number: LA-E992P | Rev: 1.0

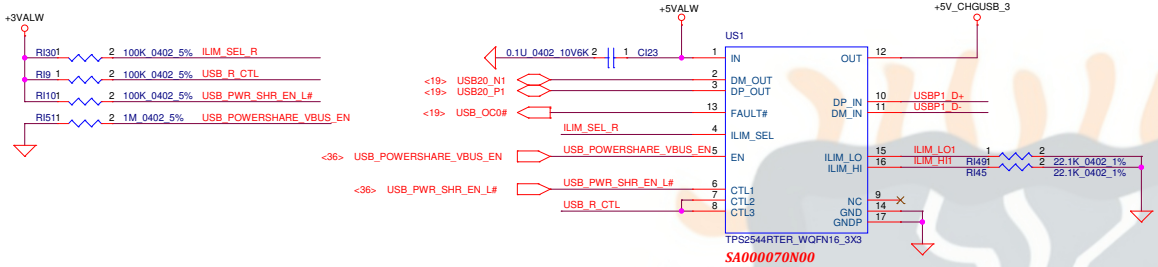
Date: Tuesday, July 25, 2017 | Sheet 29 of 77

USB Powershare

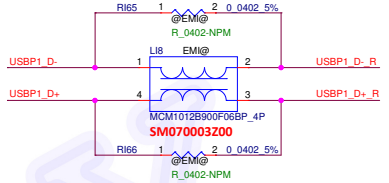
Device Control Pins				Flow Line Condition
CTL1	CTL2	CTL3	ILIM_SEL	
0	1	1	X	DCP AUTO
1	1	1	0	SDP
1	1	1	1	CDP

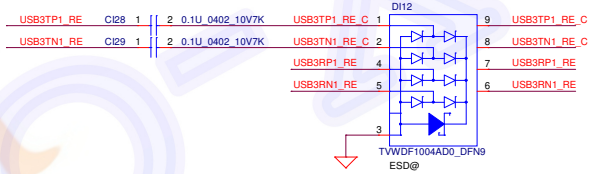
Suspend mode	CTL1 = 0 : Enable Power Share DCP mode in Suspend mode
	CTL1 = 1 : Disable Power Share in Suspend mode (For Support USB wake)
S0 mode	ILIM_SEL = 0 : SDP mode (0.9A by ILIM_LO setting)
	ILIM_SEL = 1 : CDP mode (STATUS# trigger by ILIM_HI =2.2A)

USB3.0 / USB2.0 Port1



Pilot
Change RI65, RI66 footprint to R_0402-NPM





Place close to JUSB3

USB3.0 Re-driver

Setting Status

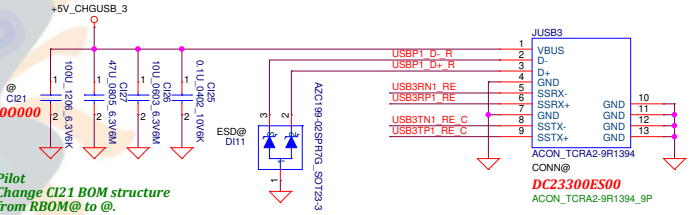
	B_EQ		A_EQ		B_DE		A_DE	
PI3EQX7502AI	NC	6.0dB	NC	6.0dB	NC	-3.5dB	NC	-3.5dB
	0	3.0dB	0	3.0dB	0	0.0dB	0	0.0dB
	1	9dB	1	9dB	1	-6.0dB	1	-6.0dB
PS8713	A EQ0 EQ1	A_EQ	B EQ0 EQ1	B_EQ	A DE0 DE1	A_DE	B DE0 DE1	B_DE
	0 0	9.5dB	0 0	9.5dB	0 0	-3.5dB	0 0	-3.5dB
	0 1	4.5dB	0 1	4.5dB	0 1	-2.7dB	0 1	-2.7dB
	1 0	13 dB	1 0	13 dB	1 0	0.0dB	1 0	0.0dB
	1 1	7.5dB	1 1	7.5dB	1 1	-5.0dB	1 1	-5.0dB

* red color is current setting

From PCH
PERICOM: RXA, PS8713: B_In
PERICOM: TXB, PS8713: A_Out

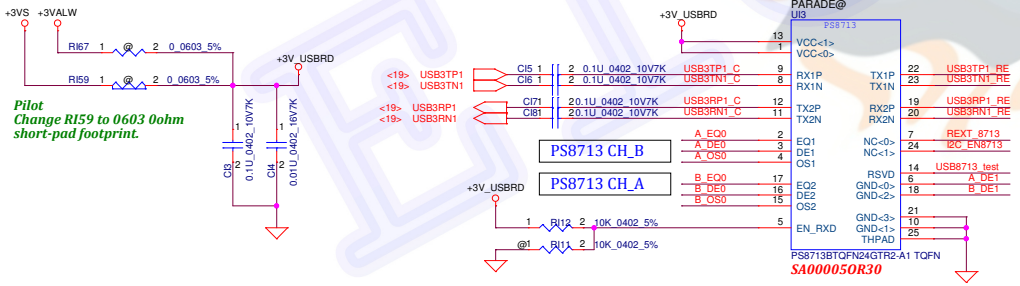
To USB3 CONN
PERICOM: TXA, PS8713:B_Out
PERICOM: RXB, PS8713:A_In

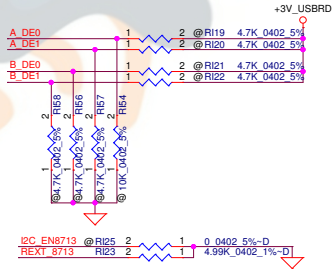
USB3.0 / USB2.0 Left Side

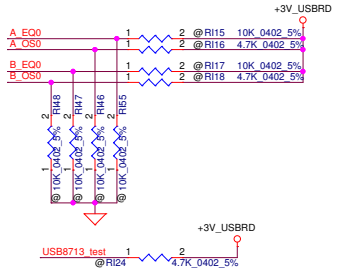


Pilot
Change CI21 BOM structure from RBOM@ to @.

Pilot
Change JUSB3 footprint from SINGA_2UB2309-000111F_9P-T to ACON_TCRA2-9R1394_9P







Pilot
Change RI59 to 0603 0ohm short-pad footprint.

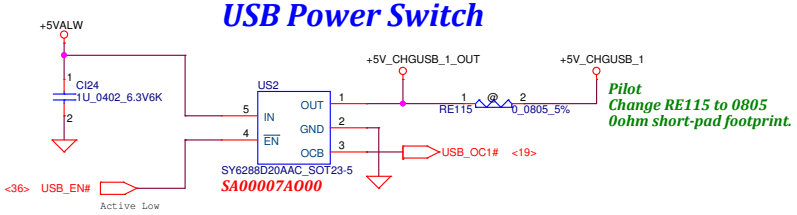
DVT2.0
Remove UI3 TI@ BOM option

UI3 PERICOM@
PI3EQX7502AIZDEX TQFN24 USB3.0 REDR
SA00006WV00

PS8713:
Pin8,9=B_In, P22,23=B_Out
Pin11,12=A_Out, Pin19,20=A_In
Pin 17=A_EQ0, Pin 15=A_EQ1
Pin 16=A_DE0, Pin 18=A_DE1
Pin 2=B_EQ0, Pin 4=B_EQ1
Pin 3=B_DE0, Pin 6=B_DE1

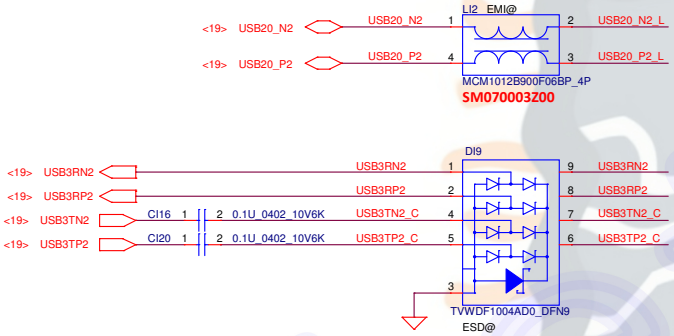
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date 2012/07/25	Title: USB Powershare
			Size: Document Number: LA-E992P
			Date: Tuesday, July 25, 2017 Sheet 31 of 77

USB Power Switch

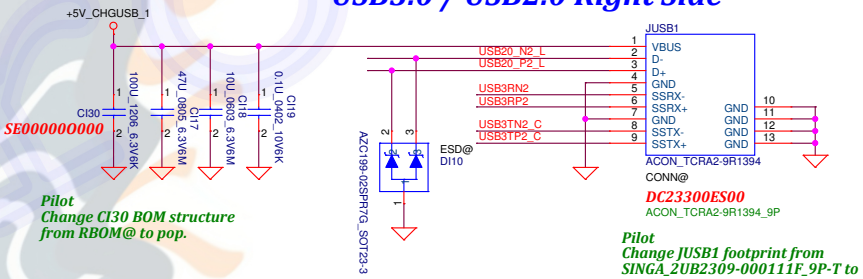


Pilot
Change RE115 to 0805
0ohm short-pad footprint.

+5VALW
+5V_CHGUSB_1
+5V_CHGUSB_1_OUT
Trace width : 100mil



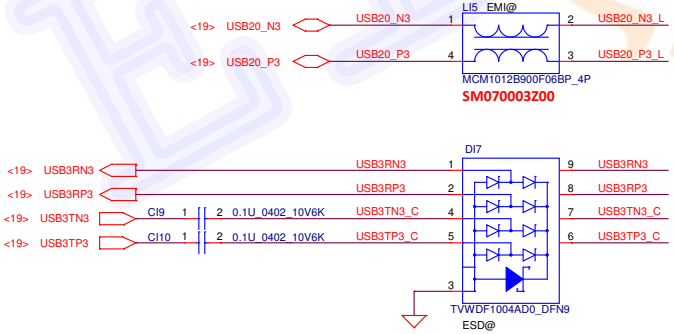
Place close to JUSB1



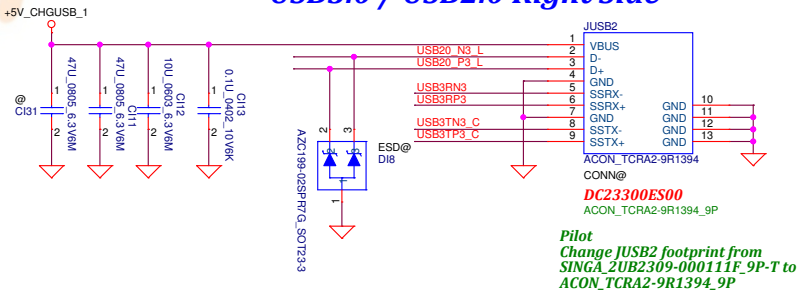
USB3.0 / USB2.0 Right Side

Pilot
Change CI30 BOM structure
from RBOM@ to pop.

Pilot
Change JUSB1 footprint from
SINGA_2UB2309-000111F_9P-T to
ACON_TCRA2-9R1394_9P



Place close to JUSB2



USB3.0 / USB2.0 Right Side

Pilot
Change JUSB2 footprint from
SINGA_2UB2309-000111F_9P-T to
ACON_TCRA2-9R1394_9P

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

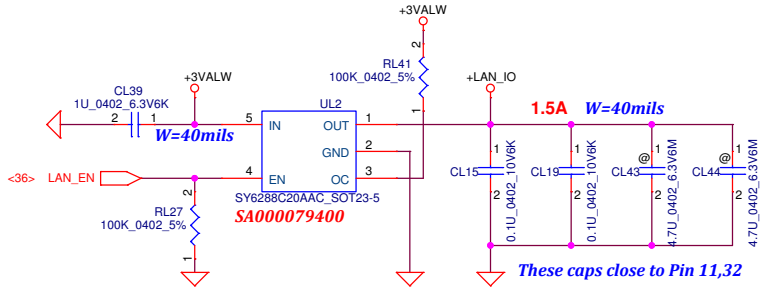
Title: **USB conn.**

Size: B | Document Number: **LA-E992P** | Rev: 1.0A00

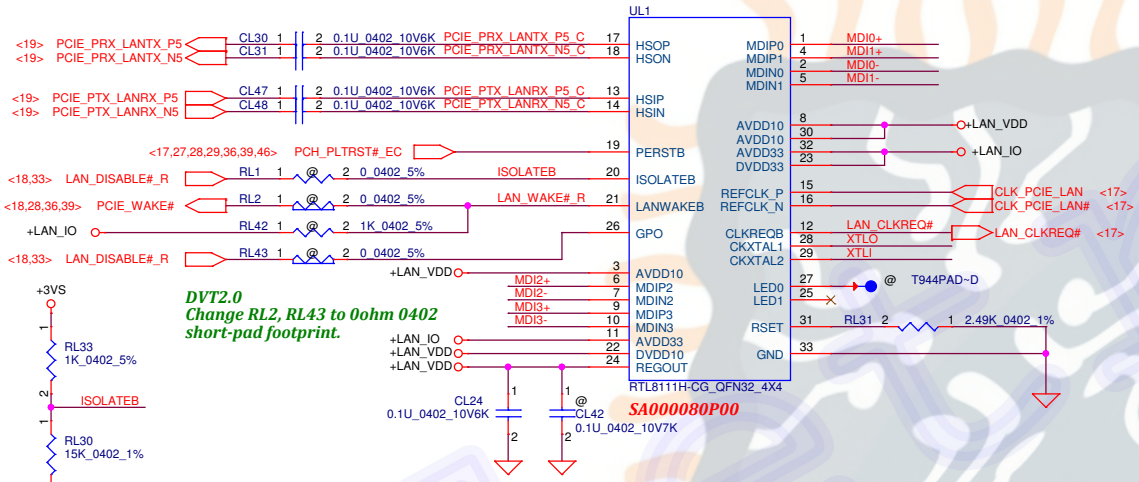
Date: Tuesday, July 25, 2017 | Sheet 32 of 77

LOM + RJ45

+LAN_IO rising time : >1ms and <100ms



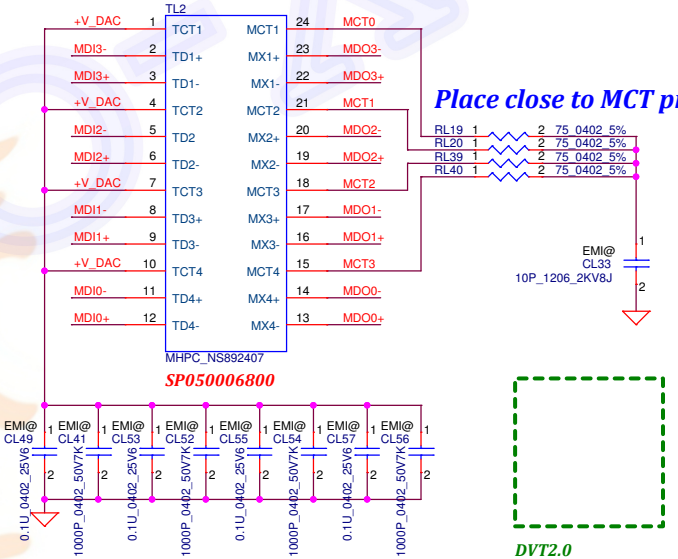
DVT2.0
Remove DL1, DL2



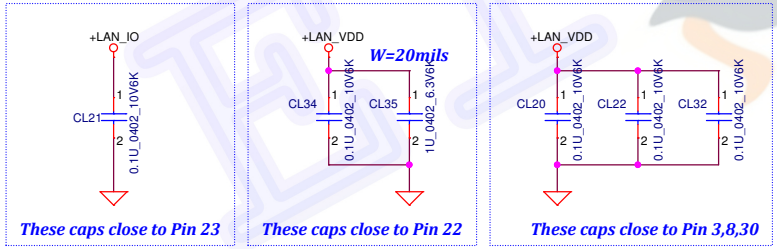
DVT2.0
Change RL2, RL43 to 0ohm 0402
short-pad footprint.

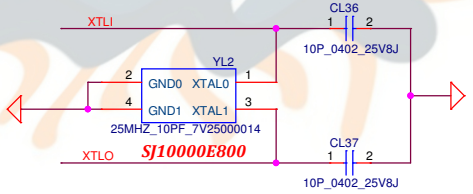
Main SP050006800 S X'FORM_ NS8924407 1G MHPC
2nd SP050006B10 S X'FORM_ GST5009-E LF LAN BOTHHAND
3rd SP050006F00 S X'FORM_ IH-160 LAN TAIMAG

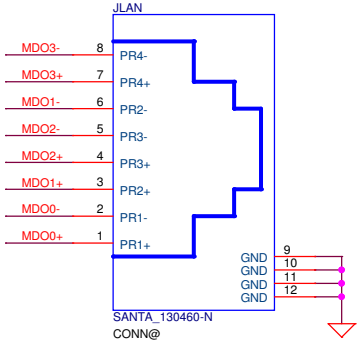
DVT2.0
Change SP050006800 as main source.



DVT2.0
Remove SP050009200
BOM option.







6.8. GPO Pin

Table 8. GPO Pin

Symbol	Type	Pin No	Description
GPO/LED1	I/O	26	General Purpose Input/Output Pin (1.8V/3.3V compatible input, 3.3V output only). The setting is changed from the register. Only one function (LED1 or GPIO) may be selected at one time (default: LED1). Power Saving Feature: Output pin. Link OK Feature: Output pin. PHY Disable Mode (active low): Input pin.

Note: The LED1 pin can be changed to a GPO pin. The setting is changed from the register. Only one function (LED1 or GPIO) may be selected at one time (Default: LED1).

Security Classification	Compal Secret Data		
Issued Date	2013/08/01	Deciphered Date	2014/07/31

Compal Electronics, Inc.

Title	LAN RTL8111GUS-CG
Size	Document Number: LA-E992P
Date:	Tuesday, July 25, 2017
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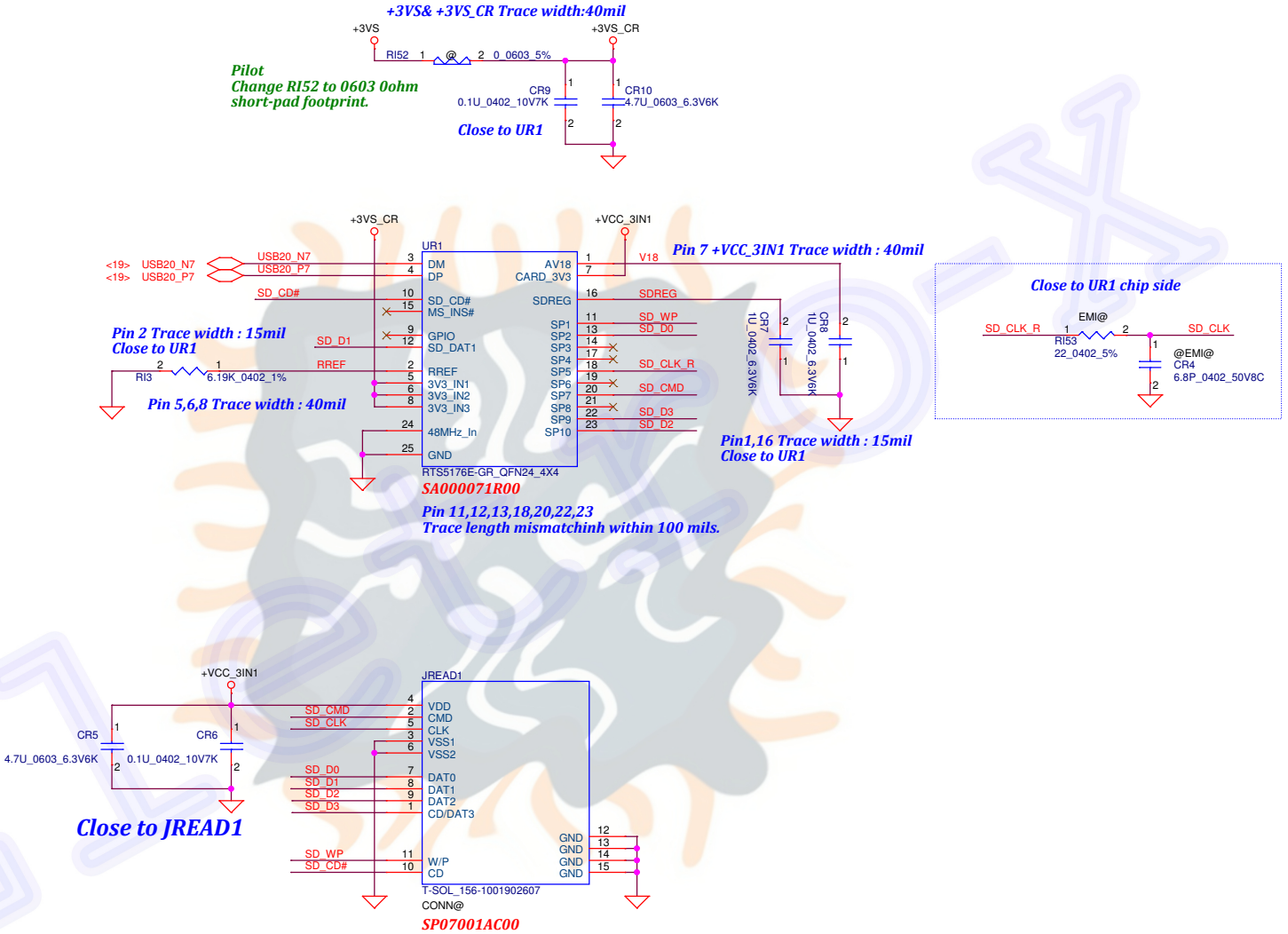
Card Reader



Security Classification	Compal Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/09/01

Compal Electronics, Inc.	
Title	Crad Reader RTS5176E
Size	Document Number: LA-E992P
Date: Tuesday, July 25, 2017	Sheet 34 of 77

Main Func = DP to VGA Converter

+3VS RVGA1 1 @ 2 0_0603_5% AVCC33
Pilot
Change RVGA1 to 0603
0ohm short-pad footprint.
CVGA1 10U_0603_6.3V6M VGA@

+3VS RVGA2 1 @ 2 0_0603_5% VDD_DAC_33
Pilot
Change RVGA2 to 0603
0ohm short-pad footprint.
CVGA2 10U_0603_6.3V6M VGA@

+CRT_5V_OUT FVGA1 1.1A_6V_SPR-P110 VGA@ DVGA1 LRB551V-30T1G_SOD323-2 VGA@ +5VS

Note:
CG3, CG4. CG6, CG8, CG15 need to place to Chip

+3VS
RVGA3 2 @ 1 DDI3_AUXN_C 100K_0402_5%
RVGA4 2 @ 1 DDI3_AUXP_C 100K_0402_5%

AVCC33
UVGA1
RTD2166
RTD2166-CG_QFN32_4X4
VGA@

1	AVC33			VDD_DAC_33	20
4	AVCC_12			VCK_12	25
14	VCC_33			PVCC_33	26
2	AUX_P				
3	AUX_N				
5	LANE0_P			HVSYNC_PWR	17
6	LANE0_N			VSYNC	18
7	LANE1_P			HSYNC	19
8	LANE1_N				
10	POL1/SPI_CEB			BLUE_P	21
9	POL2			GREEN_P	22
11	GPI1/SPI_CLK			RED_P	23
12	GPI2/SPI_SI				
13	GPI3/SPI_SO				
15	VGA_SCL			LDO_RSTB	27
16	VGA_SDA			EXT_CLK_IN	28
30	SMB_SCL			EXT1.2V_CTRL	31
29	SMB_SDA				
32	HPD			GND	24
				EPAD_GND	33

CVGA6 VGA@1 2 0.1U_0402_16V4Z +1.2V_VCCK
+3VS
<7> DDI3_AUXP DDI3_AUXP CVGA4 VGA@1 2 0.1U_0402_16V4Z DDI3_AUXP_C
<7> DDI3_AUXN DDI3_AUXN CVGA9 VGA@1 2 0.1U_0402_16V4Z DDI3_AUXN_C
<7> CPU_DDI3_P0 CPU_DDI3_P0 CVGA10 VGA@1 2 0.1U_0402_16V4Z DP_P0
<7> CPU_DDI3_N0 CPU_DDI3_N0 CVGA11 VGA@1 2 0.1U_0402_16V4Z DP_N0
<7> CPU_DDI3_P1 CPU_DDI3_P1 CVGA12 VGA@1 2 0.1U_0402_16V4Z DP_P1
<7> CPU_DDI3_N1 CPU_DDI3_N1 CVGA13 VGA@1 2 0.1U_0402_16V4Z DP_N1
AVCC33
RVGA5 VGA@2 1 4.7K_0402_5% POL1_SDA
RVGA6 VGA@2 1 4.7K_0402_5% POL1_SCL
+3VS RVGA16 2 @ 1 4.7K_0402_5%
CRT_DDCCLK_CON
CRT_DDCDATA_CON
<6,14,15,18,29> PCH_SMBCLK
<6,14,15,18,29> PCH_SMBDATA
<16> CPU_DDI3HPD CPU_DDI3HPD RVGA9 1 @ 2 0_0402_5% CRT_PCH_HPD

VDD_DAC_33
CVGA3 VGA@1 2 0.1U_0402_16V4Z
CVGA5 VGA@1 2 2.2U_0402_6.3V6M
+1.2V_VCCK CVGA7 VGA@1 2 0.1U_0402_16V4Z
+3VS CVGA8 VGA@1 2 0.1U_0402_16V4Z
DP_CRT_VSYNC_CON
DP_CRT_HSYNC_CON
+5VS
DP_CRT_B
DP_CRT_G
DP_CRT_R
4.7U_0603_6.3V6K CVGA14 VGA@
0.1U_0402_16V4Z CVGA15 VGA@

+CRT_5V_OUT
RVGA7 2.2K_0402_5% VGA@
RVGA8 2.2K_0402_5% VGA@
CRT_DDCDATA_CON
CRT_DDCCLK_CON

RVGA10 100K_0402_5%

DVT2.0
Change RVGA9 to 0ohm 0402
short-pad footprint.

CRT RGB
CRT H/VSYNC
CRT SMBUS

DVT 1.0
Change LVGA1, LVGA2, LVGA3 BS to VGA@EMI@.

DP_CRT_R LVGA11 VGA@EMI@ BLM15BB220SN1D CRT_R
DP_CRT_G LVGA21 VGA@EMI@ BLM15BB220SN1D CRT_G
DP_CRT_B LVGA31 VGA@EMI@ BLM15BB220SN1D CRT_B
RVGA11 RVGA12 RVGA13 75_0402_1%
CVGA16 CVGA17 CVGA18 CVGA19 CVGA20 CVGA21 2.2P_0402_50V8C

+CRT_5V_OUT JCRT1
CRT_R
CRT_DDCDATA_CON
CRT_G
CRT_HSYNC_CON
CRT_B
CRT_VSYNC_CON
CRT_DDCCLK_CON
CVGA22 0.01U_0402_16V7K
C-K_80454-5K1-152 CONN@
DC060004S10

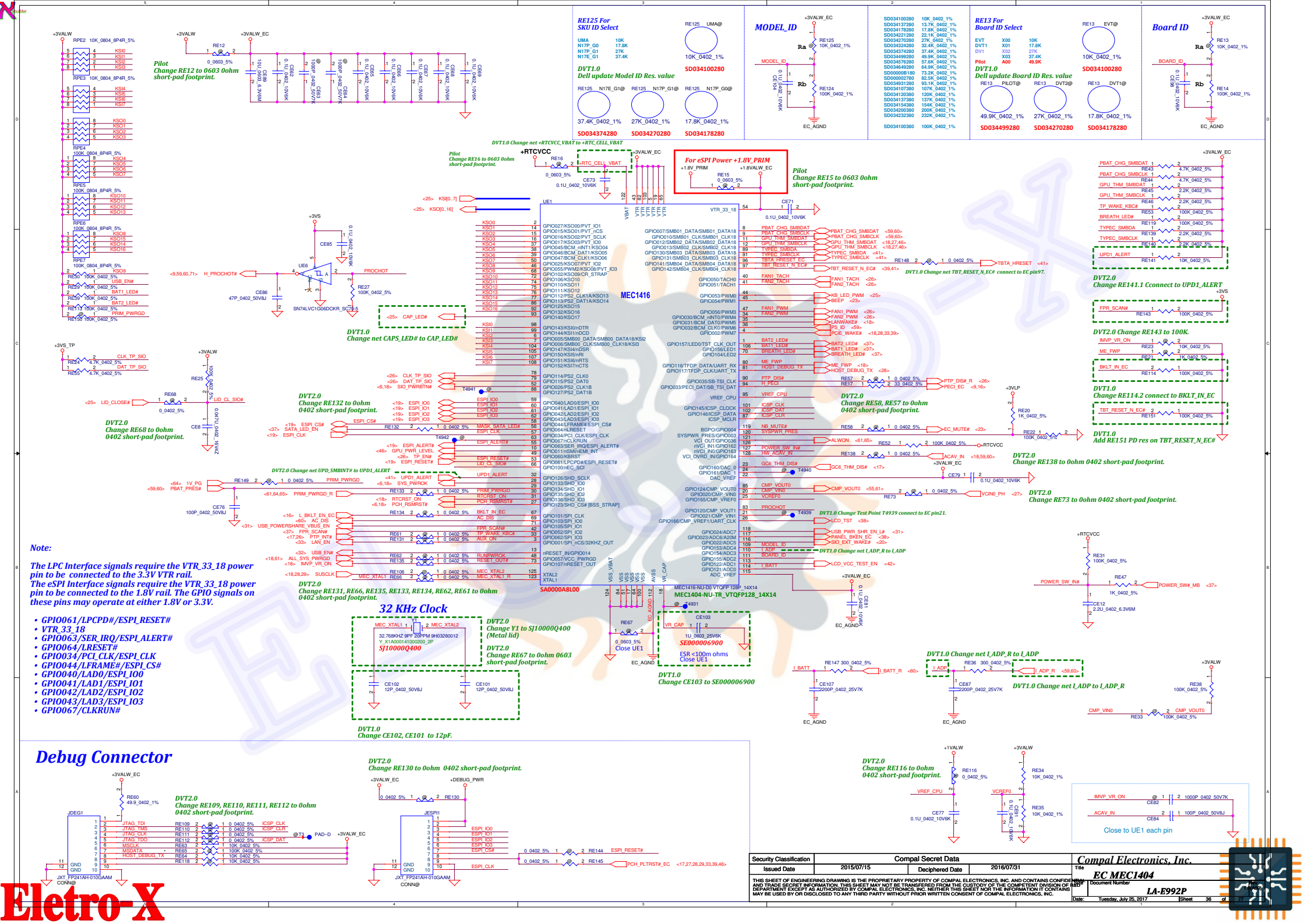
1. Red Video
2. Green Video
3. Blue Video
4. No Connect
5. Ground
6. Red Return
11. No Connect
7. Green Return
12. DDC Data
8. Blue Return
13. Horizontal Sync
9. DDC Power
14. Vertical Sync
10. Sync Return
15. DDC Clock

DP_CRT_HSYNC_CON 47_0402_5% RVGA14 CRT_HSYNC_CON
DP_CRT_VSYNC_CON 47_0402_5% RVGA15 CRT_VSYNC_CON
CVGA23 10P_0402_50V VGA@EMI@
CVGA24 10P_0402_50V VGA@EMI@

DVT 1.0
Change CVGA23, CVGA24 BS to VGA@EMI@.

Security Classification	Compal Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/09/01

Compal Electronics, Inc.
Title: DP to VGA Converter
Size: Custom
Document Number: LA-E992P
Rev: 1.0
Date: Tuesday, July 25, 2017
Sheet 35 of 77


RE125 For SKU ID Select
UMA N17P_G0 N17P_G1 N17E_G1
10K 17.8K 27K 37.4K
RE125 UMA@
10K_0402_1%
SD034100280
DVT1.0 Dell update Model ID Res. value
RE125_N17E_G1@ 37.4K_0402_1% SD034374280
RE125_N17P_G1@ 27K_0402_1% SD034270280
RE125_N17P_G0@ 17.8K_0402_1% SD034178280
MODEL_ID
RE125 10K_0402_1%
RE124 100K_0402_1%
SD034100280 10K_0402_1%
SD034137280 13.7K_0402_1%
SD034178280 17.8K_0402_1%
SD034221280 22.1K_0402_1%
SD034270280 27K_0402_1%
SD034324280 32.4K_0402_1%
SD034374280 37.4K_0402_1%
SD034498280 49.9K_0402_1%
SD034576280 57.6K_0402_1%
SD034649280 64.9K_0402_1%
SD000008180 73.2K_0402_1%
SD000002780 82.5K_0402_1%
SD034931280 93.1K_0402_1%
SD034107380 107K_0402_1%
SD034120380 120K_0402_1%
SD034137380 137K_0402_1%
SD034154380 154K_0402_1%
SD034200380 200K_0402_1%
SD034232380 232K_0402_1%
SD034100380 100K_0402_1%
RE13 For Board ID Select
EVT X00 10K
DVT1 X01 17.8K
DVT1 X02 27K
Pilot A00 49.9K
RE13 EVT@
10K_0402_1%
SD034100280
DVT1.0 Dell update Board ID Res. value
RE13 PILOT@ 49.9K_0402_1% SD034499280
RE13 DVT2@ 27K_0402_1% SD034270280
RE13 DVT1@ 17.8K_0402_1% SD034178280
Board ID
RE13 10K_0402_1%
RE14 100K_0402_1%
Pilot Change RE12 to 0603 0ohm short-pad footprint.
DVT1.0 Change net +RTCVCC_VBAT to +RTC_CELL_VBAT
Pilot Change RE16 to 0603 0ohm short-pad footprint.
For eSPI Power +1.8V_PRIM
Pilot Change RE15 to 0603 0ohm short-pad footprint.
MEC1416
MEC1416-NU-D0 VTQFP 128P_14X14
MEC1404-NU-TR_VTQFP128_14X14
SA0000A8L00
DVT1.0 Change net TBT_RESET_N_EC# connect to EC pin97.
DVT2.0 Change RE141.1 Cconnect to UPD1_ALERT
DVT2.0 Change RE143 to 100K.
DVT1.0 Change RE114.2 connect to BKLT_IN_EC
DVT1.0 Add RE151 PD res on TBT_RESET_N_EC#
DVT1.0 Change net CAPS_LED# to CAP_LED#
DVT2.0 Change net UPD_SMBINT# to UPD1_ALERT
DVT2.0 Change RE132 to 0ohm 0402 short-pad footprint.
DVT2.0 Change RE68 to 0ohm 0402 short-pad footprint.
DVT2.0 Change RE58, RE57 to 0ohm 0402 short-pad footprint.
DVT2.0 Change RE138 to 0ohm 0402 short-pad footprint.
DVT2.0 Change RE73 to 0ohm 0402 short-pad footprint.
DVT1.0 Change Test Point T4939 connect to EC pin21.
DVT2.0 Change RE131, RE66, RE135, RE133, RE134, RE62, RE61 to 0ohm 0402 short-pad footprint.
32 KHz Clock
DVT2.0 Change Y1 to SJ10000Q400 (Metal lid)
DVT2.0 Change RE67 to 0ohm 0603 short-pad footprint.
DVT1.0 Change CE103 to SE000006900
DVT1.0 Change net I_ADP_R to I_ADP
DVT1.0 Change CE102, CE101 to 12pF.
Note:
The LPC Interface signals require the VTR_33_18 power pin to be connected to the 3.3V VTR rail.
The eSPI Interface signals require the VTR_33_18 power pin to be connected to the 1.8V rail. The GPIO signals on these pins may operate at either 1.8V or 3.3V.
GPIO061/LPCPD#/ESPI_RESET#
VTR_33_18
GPIO063/SER_IRQ/ESPI_ALERT#
GPIO064/LRESET#
GPIO034/PCI_CLK/ESPI_CLK
GPIO044/LFRAME#/ESPI_CS#
GPIO040/LAD0/ESPI_IO0
GPIO041/LAD1/ESPI_IO1
GPIO042/LAD2/ESPI_IO2
GPIO043/LAD3/ESPI_IO3
GPIO067/CLKRUN#
Debug Connector
DVT2.0 Change RE109, RE110, RE111, RE112 to 0ohm 0402 short-pad footprint.
DVT2.0 Change RE130 to 0ohm 0402 short-pad footprint.
DVT2.0 Change RE116 to 0ohm 0402 short-pad footprint.
Close to UE1 each pin
Security Classification
Compal Secret Data
Issued Date 2015/07/15
Deciphered Date 2016/07/31
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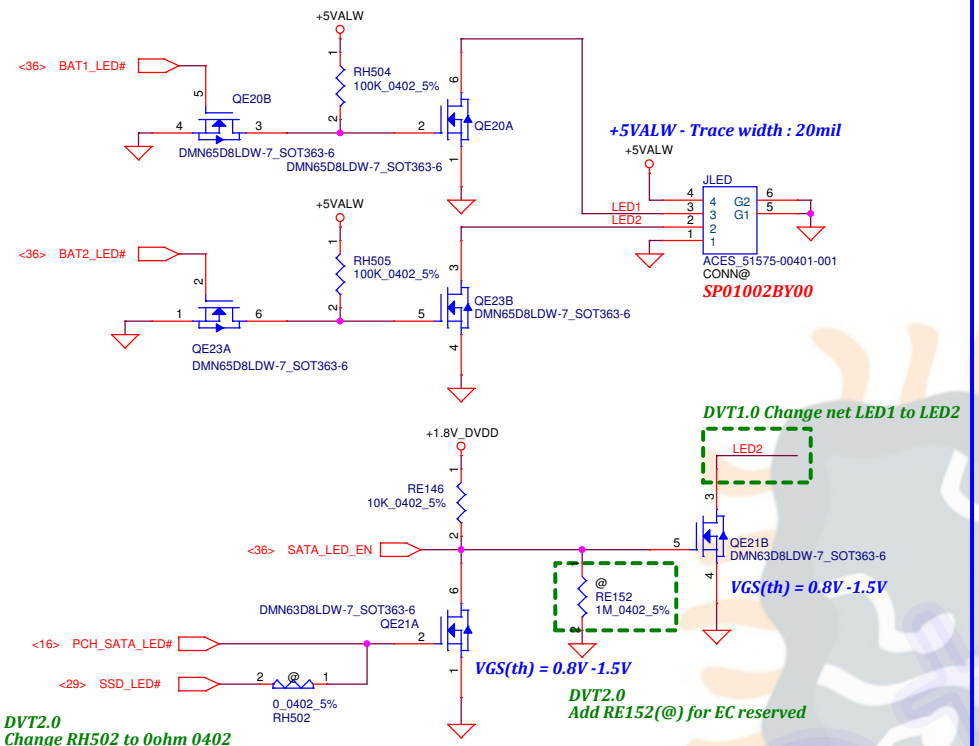
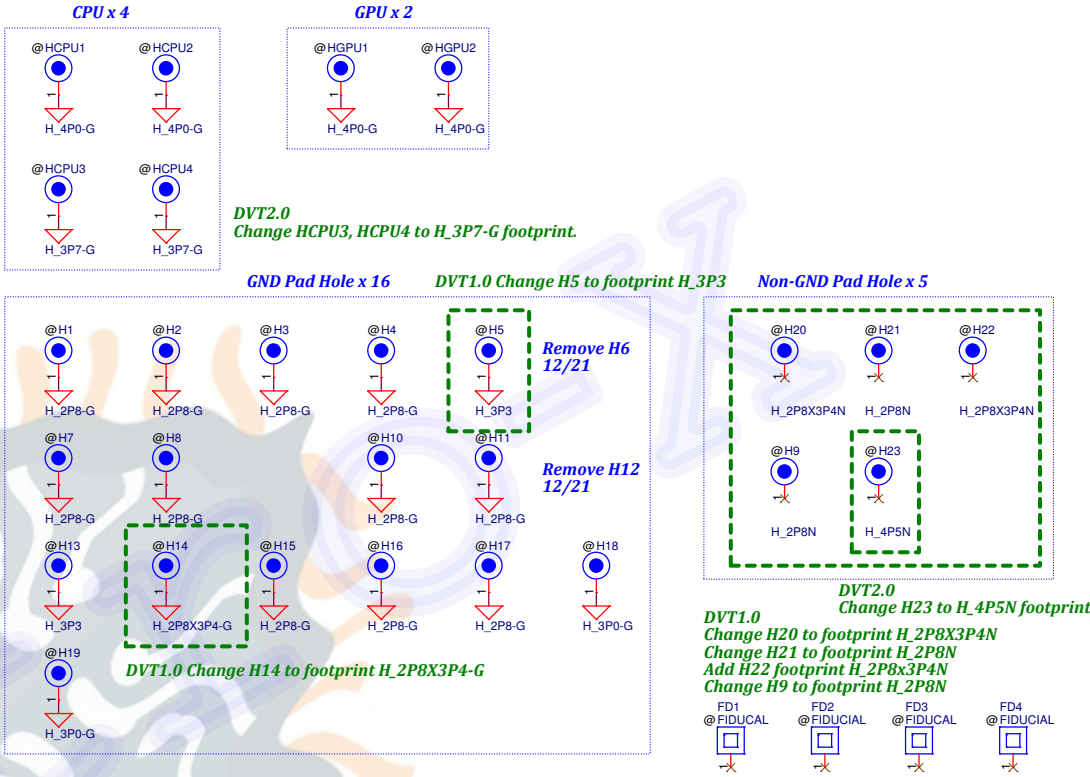
Compal Electronics, Inc.
Title EC MEC1404
Document Number LA-E992P
Date: Tuesday, July 25, 2017 Sheet 36
Eletro-X

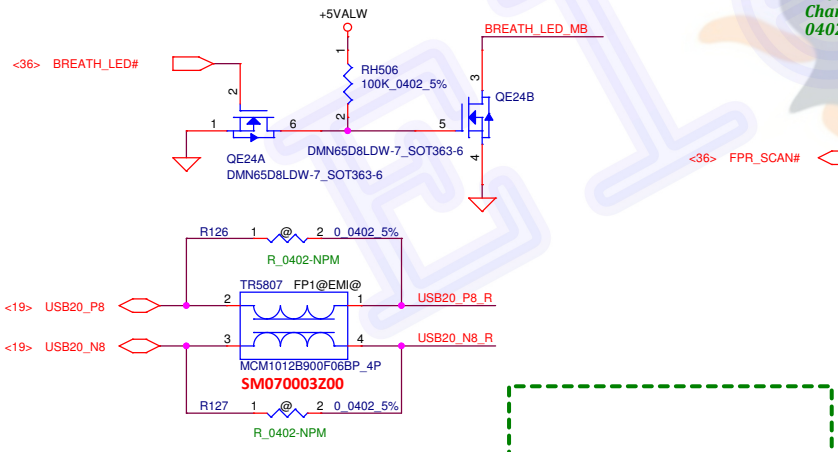
LED Board Connector



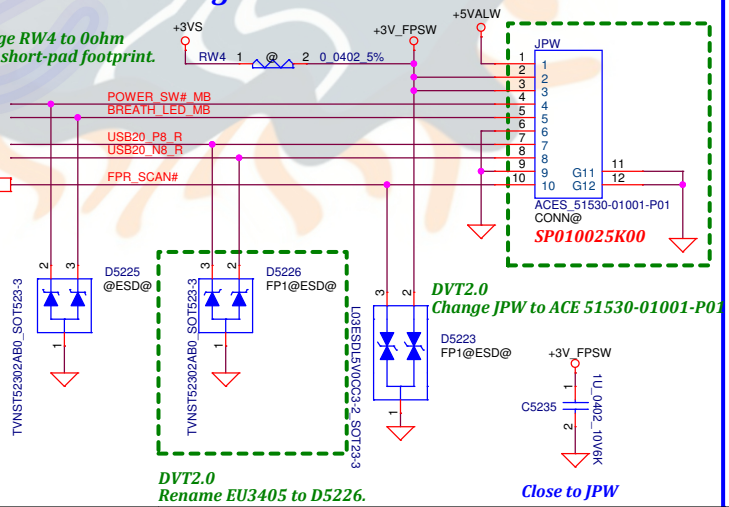
Screw Hole



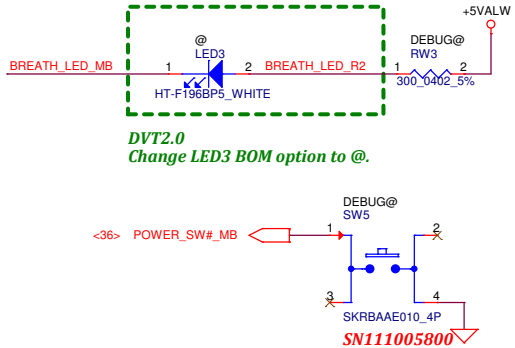
PWR BOARD Connector



Touch Finger Print module.



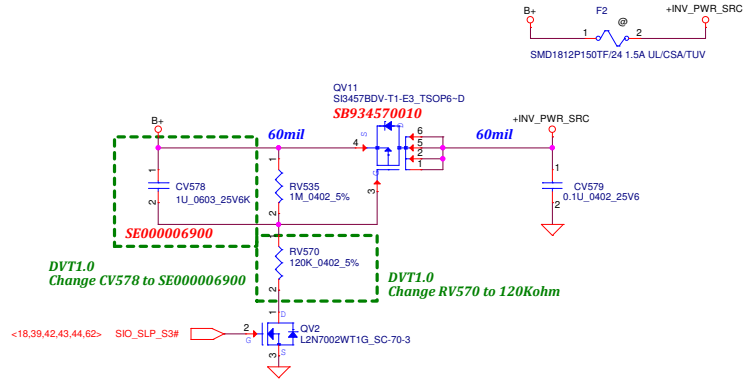
Power Button & LED (Reserve)



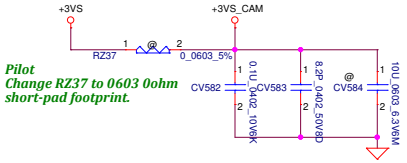
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

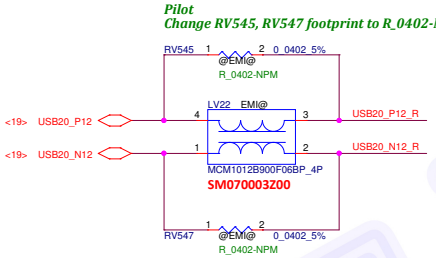
Compal Electronics, Inc.			
Title	TPM/BTB conn.		
Size	Document Number	LA-E992P	Rev 1A0.0
Date:	Tuesday, July 25, 2017	Sheet 37 of 77	

LCD backlight PWR CTRL



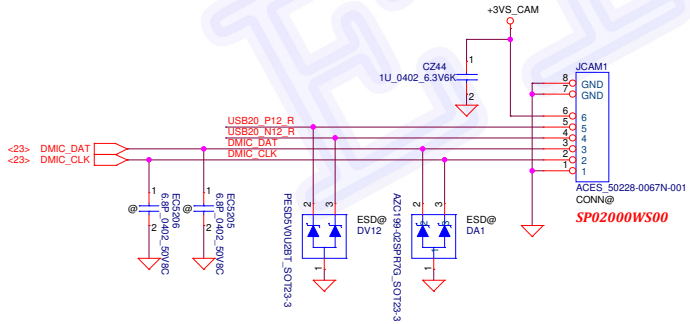
CCD +DMIC Circuit



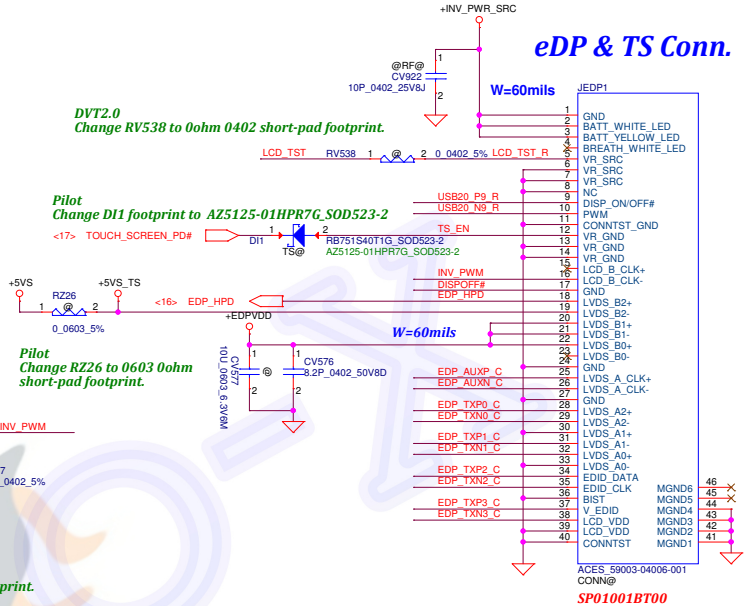


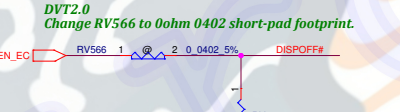
Need to check pin define

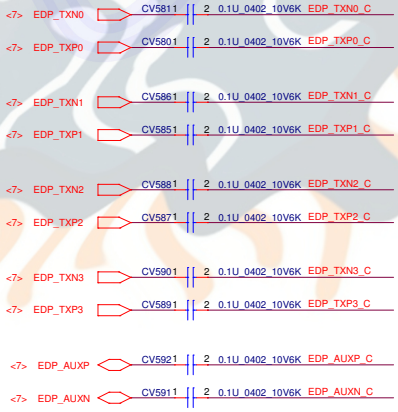
CCD +DMIC Connector

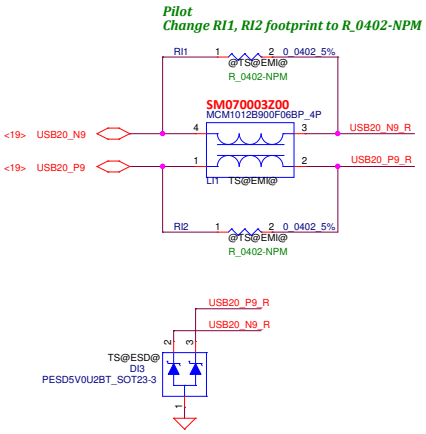


eDP & TS Conn.









Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.	
Title	eDP /TS conn.
Size	Document Number: LA-E992P
Date: Tuesday, July 25, 2017	Sheet 38 of 77

UT1 TBT@

S IC JHL6340 SLLSP C1 THUNDERBOLT A31!
SA00009YL3L

PCIE X4 Bus

PCIE CLK

CPU DDI1

CPU DDI2

Reserve for common DP design

DVT2.0
Change RT2 to 0 ohm
0201 short-pad footprint.

DVT1.0
Remove JTAG

DVT2.0
Change RT110 to 0 ohm 0201 short-pad footprint.

DVT1.0 Un-pop RT30

DVT1.0 Un-pop RT80

DVT2.0 Change RT13, RT16 to 0 ohm
0201 short-pad footprint.

DVT2.0 Change RT121 to 0 ohm
0201 short-pad footprint.

DVT1.0
Remove RT98, RT99, RT100

DVT1.0
Remove Off- page connector

SJ10000TZ00

SA00003EW10

Close to UT1

Closed to UT1

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2016/09/18

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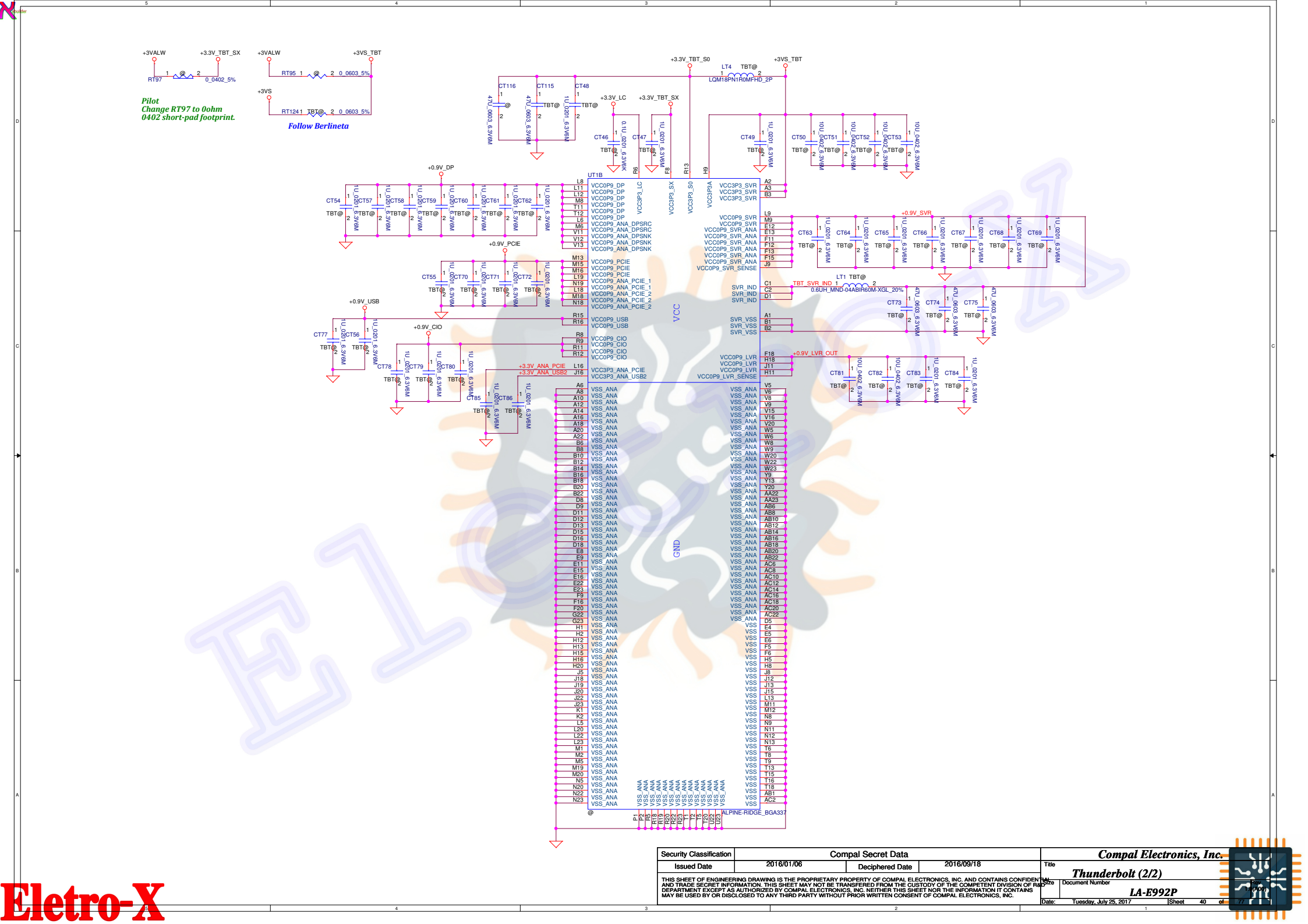
Compal Electronics, Inc.

Title: Thunderbolt (1/2)

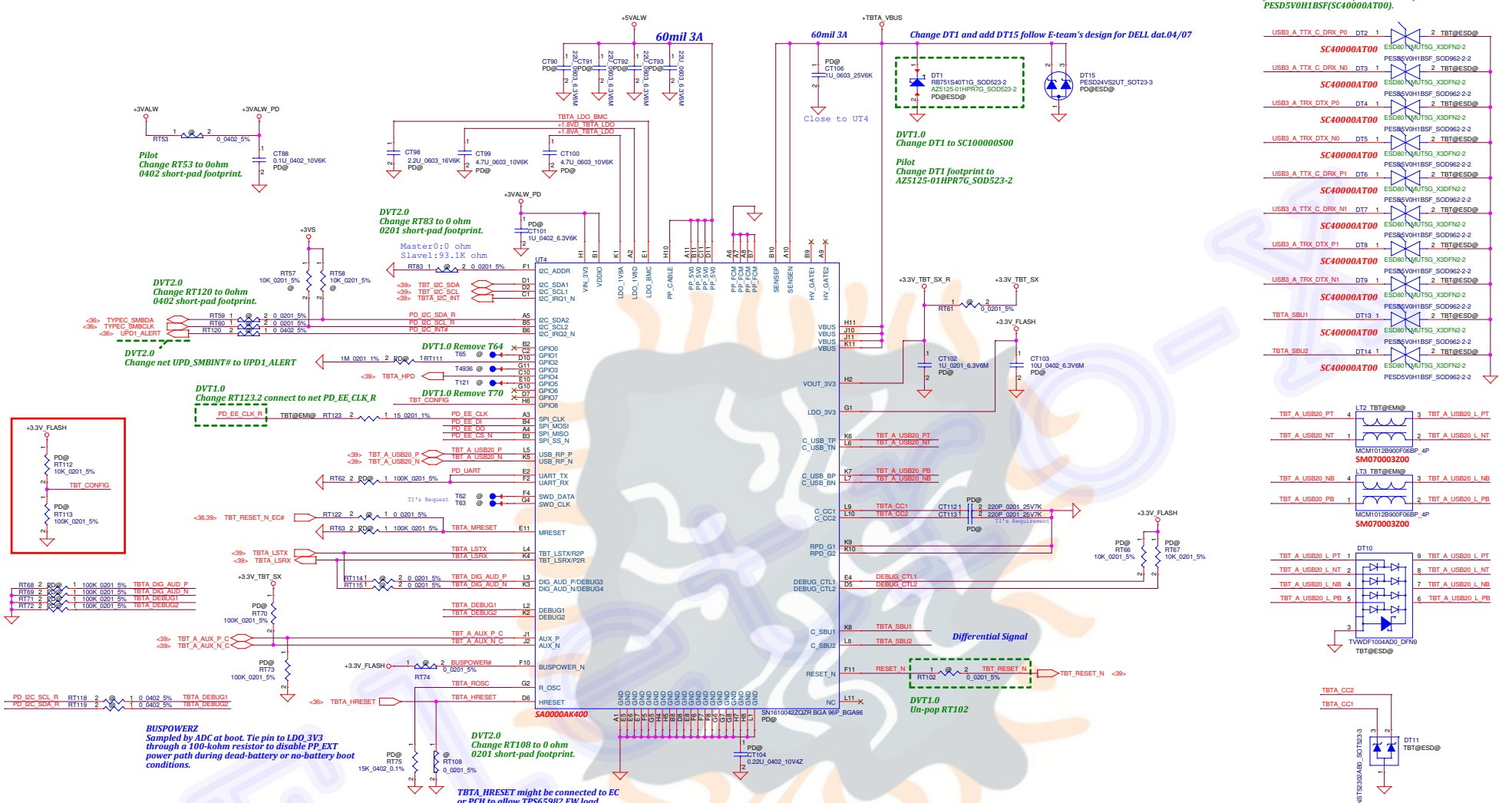
Size: C | Document Number: LA-E992P | Rev: 1.0

Date: Tuesday, July 25, 2017 | Sheet 39 of 77



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2016/09/18

Compal Electronics, Inc.			
Title	Thunderbolt (2/2)		
Size	Document Number	LA-E992P	Rev 1.0
Date: Tuesday, July 25, 2017	Sheet 40 of 77		



c. GPIO 8 (CONFIG) is a dedicated GPIO that must have a pull-up and pull-down resistor option included in the HW design.
When 82D has a SPI Flash Connected, the safest option is to use the "Infinite Retry" setting, which will prevent from loading an incorrect configuration. For this setting, GPIO 8 needs to be pulled to LDO_3V3, which effectively removes the divider (DIV = 1).

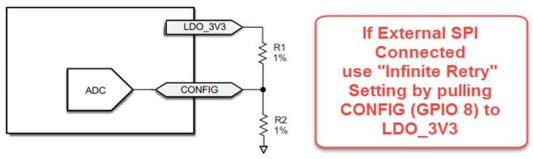


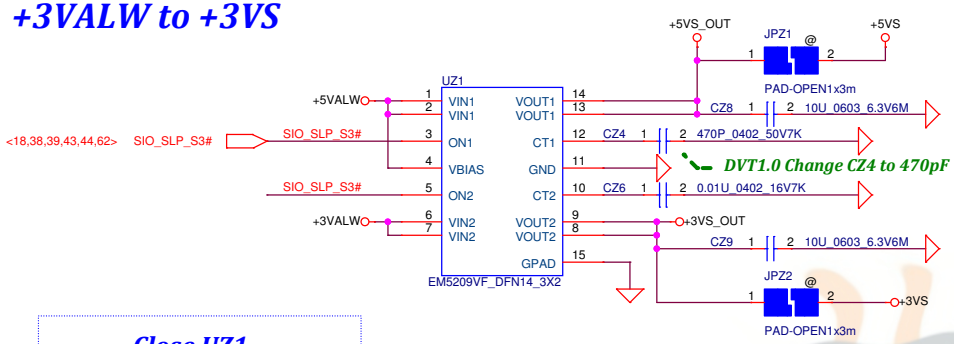
Figure 78. Factory Configuration Resistor Divider

Table 13. Factory Device Configuration Selection

DIV = R2/(R1+R2) (1)		Factory Device Configuration	Description
DIV_min	DIV_max		
0.70	1.00	7	Infinite boot retry from Flash to Host I/F cycles.

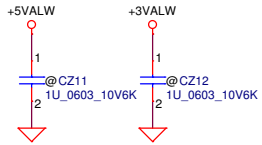
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/01/06	Deciphered Date 2016/09/18	Title PD+USB3.1 type C
			Document Number LA-E992P
			Date: Tuesday, July 25, 2017 Sheet 41 of 77

+5VALW to +5VS
+3VALW to +3VS

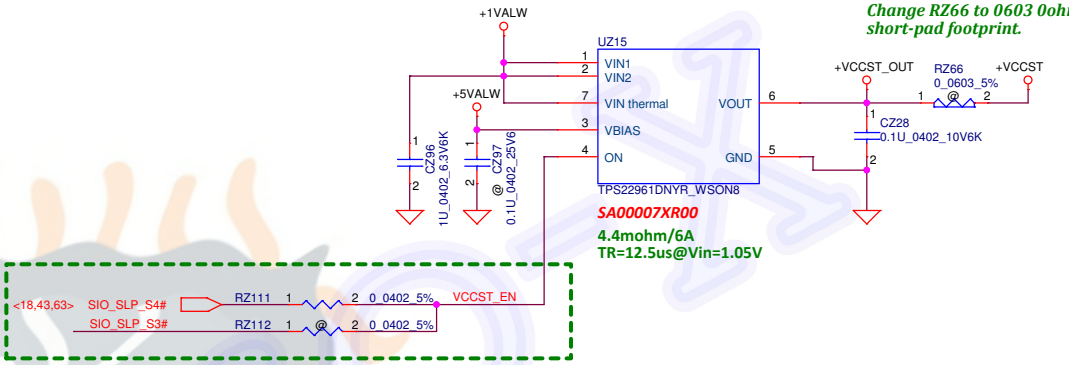


DVT1.0 Change CZ4 to 470pF

Close UZ1



+VCCST Load Switch

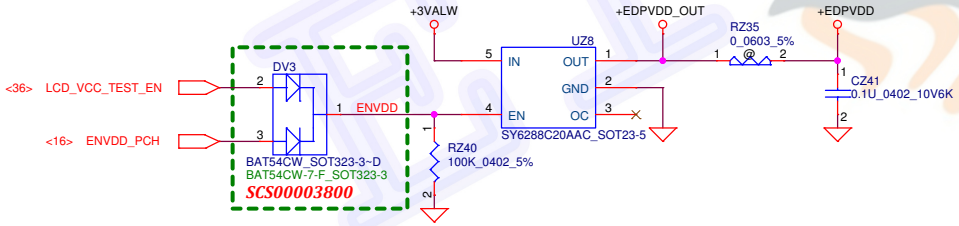


Pilot
Change RZ66 to 0603 0ohm short-pad footprint.

SA00007XR00
4.4mohm/6A
TR=12.5us@Vin=1.05V

DVT1.0
Add RZ111 connect to SIO_SLP_S4#
Add RZ112(@) connect to SIO_SLP_S3#
Add net VCCST_EN

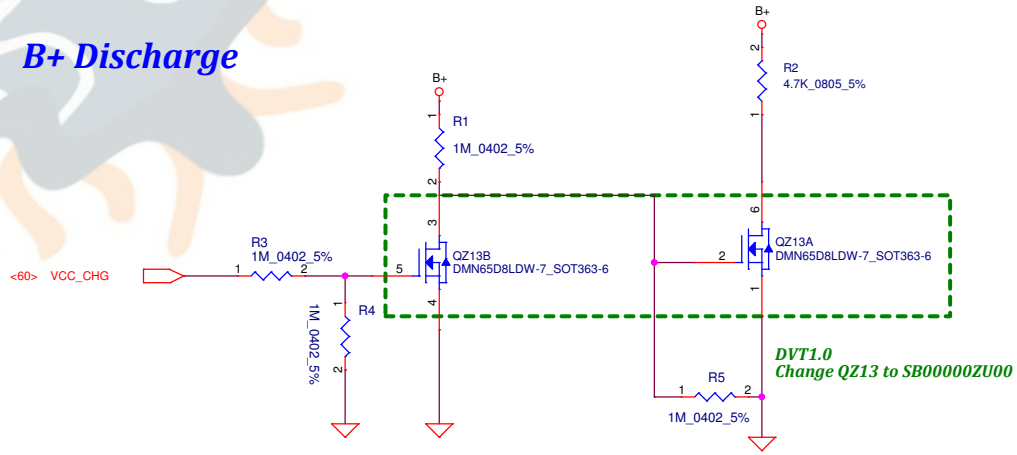
eDP Load Switch



Pilot
Change RZ35 to 0603 0ohm short-pad footprint.

DVT1.0
Change DV3 to SCS00003800.

B+ Discharge



DVT1.0
Change QZ13 to SB00000ZU00

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

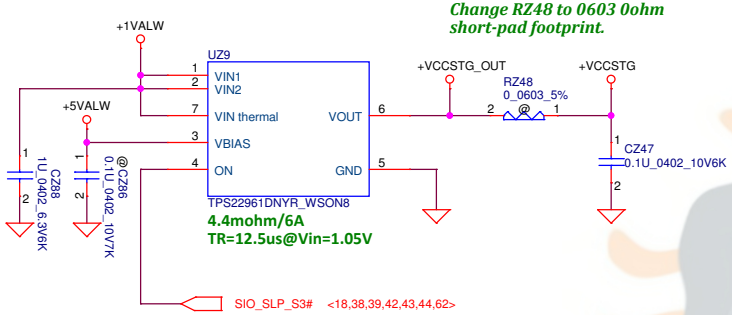
Compal Electronics, Inc.

Title: SYS DC/DC Interface

Size | Document Number: LA-E992P | Rev: 1.0A

Date: Tuesday, July 25, 2017 | Sheet 42 of 77

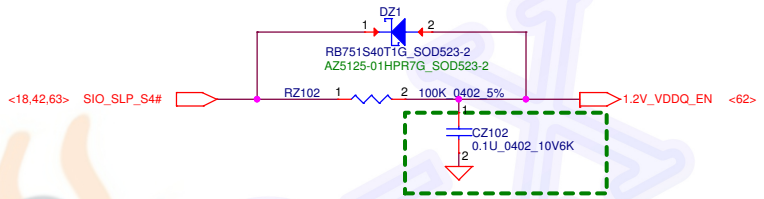
+VCCSTG Load Switch



Pilot
Change RZ48 to 0603 0ohm
short-pad footprint.

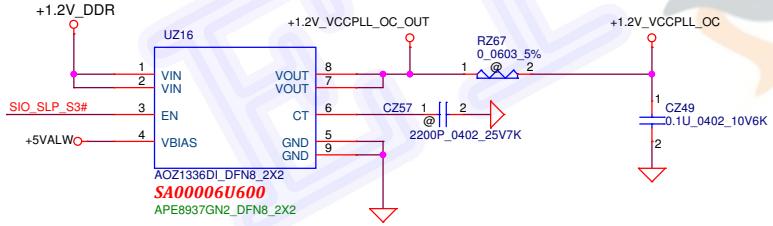
+1.2V_DDR Enable

Pilot
Change DZ1 footprint to AZ5125-01HPR7G_SOD523-2



DVT1.0 Change CZ102 to 0.1uF

+VCCPLL_OC Load Switch

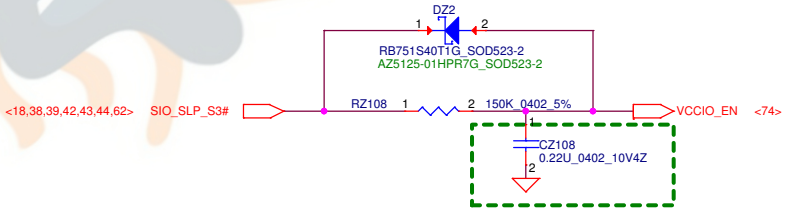


Pilot
Change RZ67 to 0603 0ohm
short-pad footprint.

Pilot
Change UZ16 form
APE8937GN2(SA000070L00) to
AOZ1336DI(SA00006U600), keep using
APE8937GN2_DFN8_2X2 footprint.

+VCCIO Enable

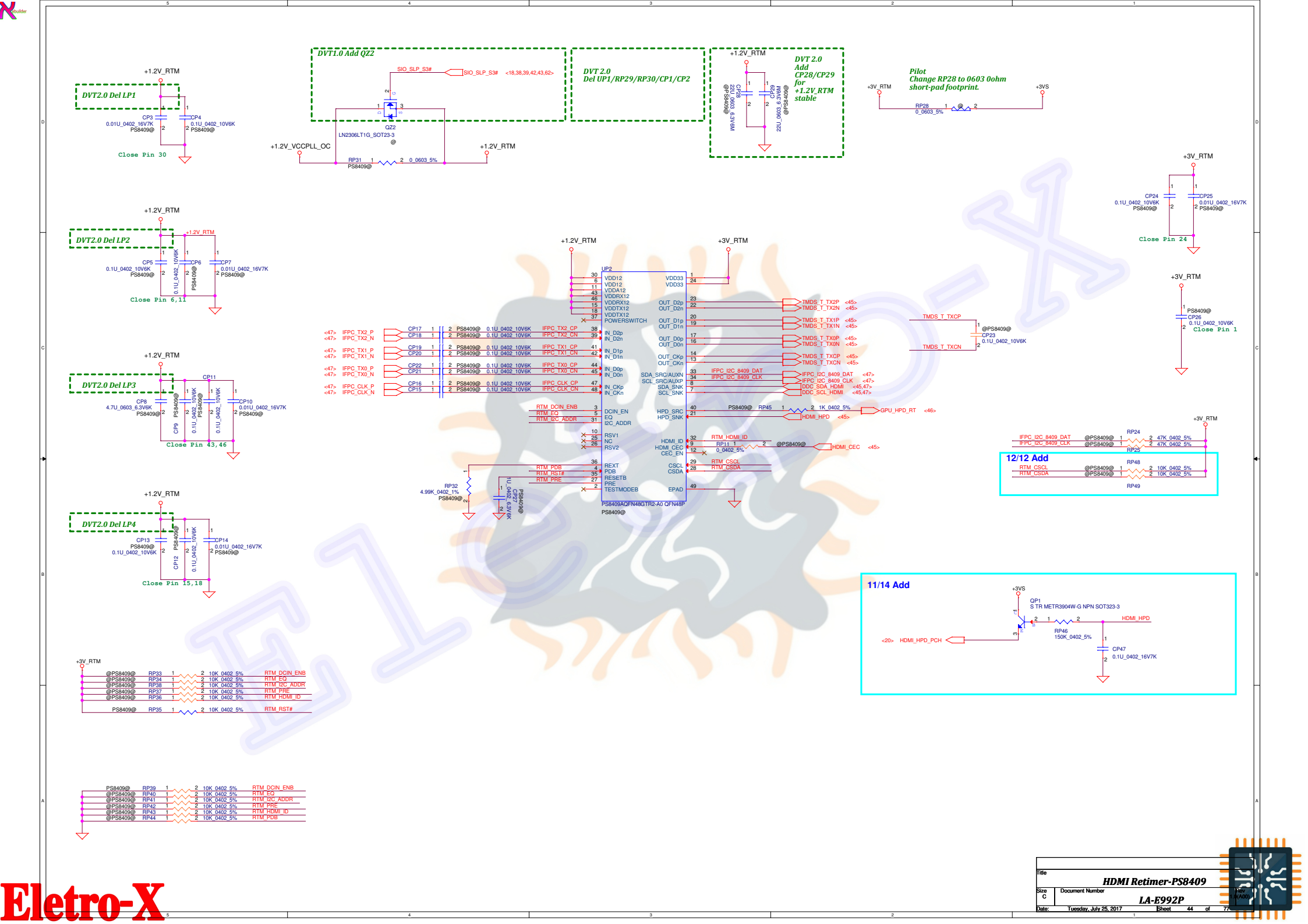
Pilot
Change DZ2 footprint to AZ5125-01HPR7G_SOD523-2



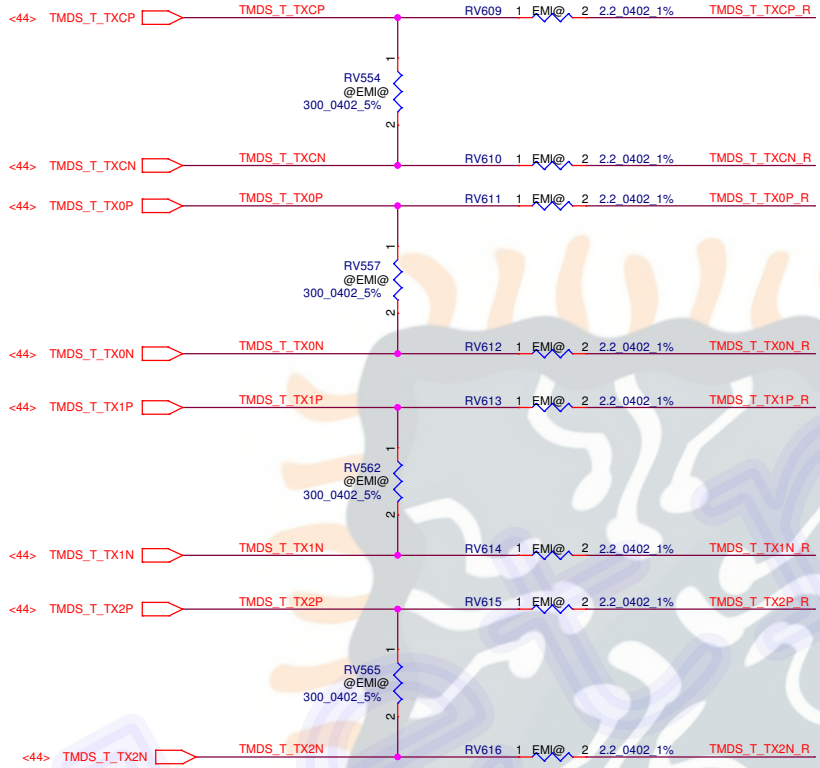
DVT1.0 Change CZ108 to 0.22uF

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

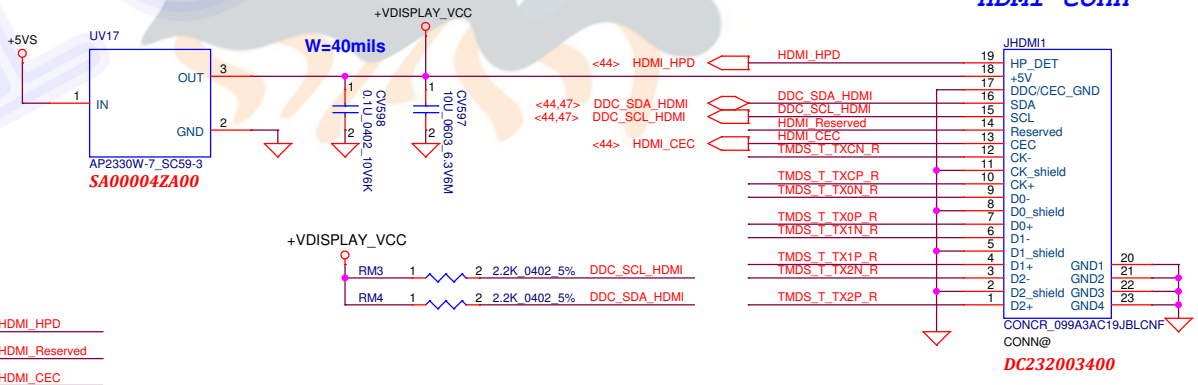
Compal Electronics, Inc.			
Title	DC/DC/S0iX/CS		
Size	Document Number	LA-E992P	Rev 1A0.0
Date: Tuesday, July 25, 2017	Sheet 43 of 77		


DVT2.0 Del LP1
DVT1.0 Add QZ2
DVT 2.0 Del UP1/RP29/RP30/CP1/CP2
DVT 2.0 Add CP28/CP29 for +1.2V_RTM stable
Pilot Change RP28 to 0603 0ohm short-pad footprint.
DVT2.0 Del LP2
DVT2.0 Del LP3
DVT2.0 Del LP4
Close Pin 30
Close Pin 6,11
Close Pin 43,46
Close Pin 15,18
Close Pin 24
Close Pin 1
PS8409AQFN48GTR2-A0 QFN48P
12/12 Add
11/14 Add
Eletro-X
HDMI Retimer-PS8409
LA-E992P

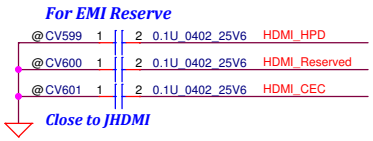
Place close to JHDMI1



HDMI conn



For EMI Reserve



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title	HDMI		
Size	Document Number	LA-E992P	Rev 1.0
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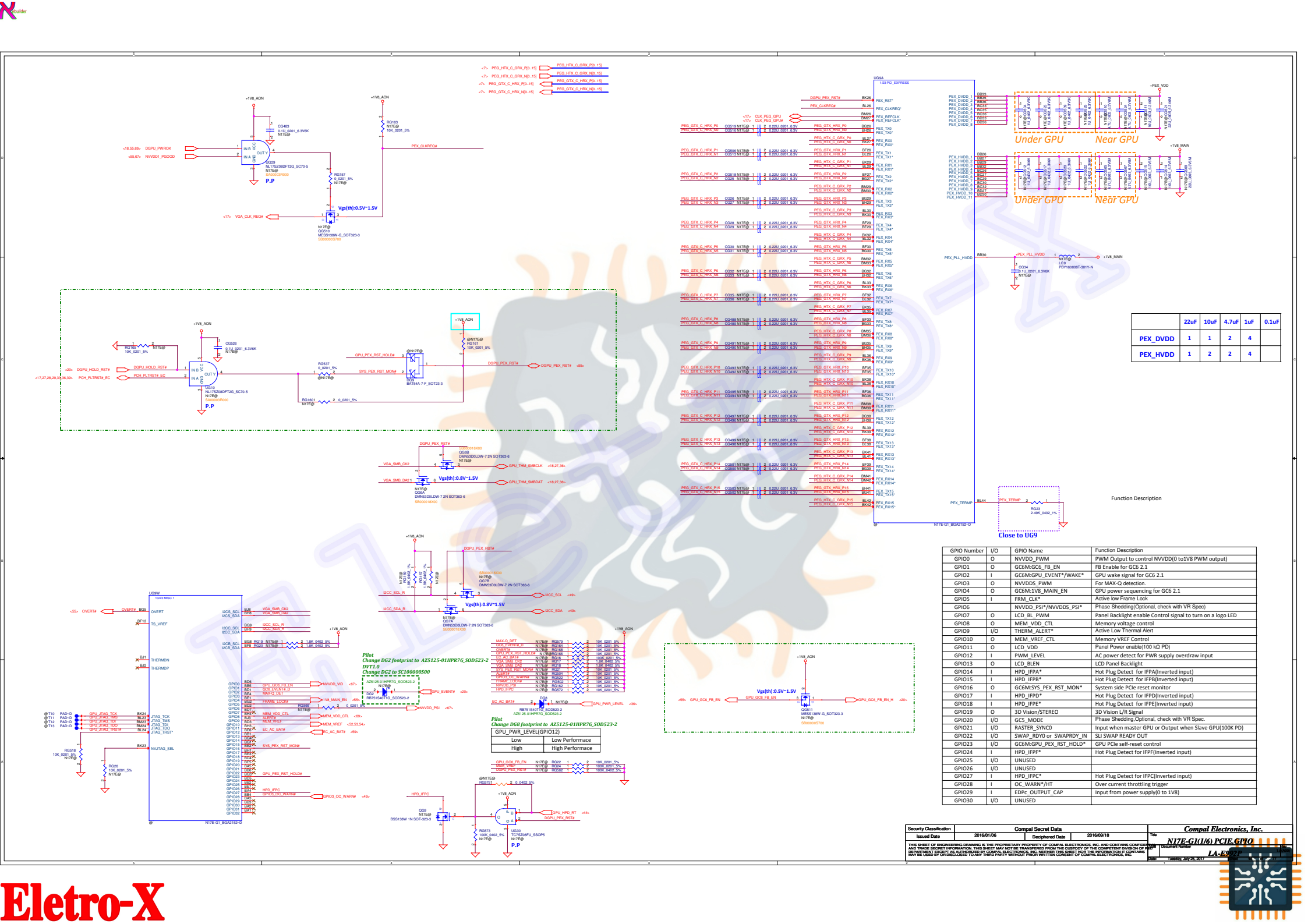

	22uF	10uF	4.7uF	1uF	0.1uF
PEX_DVDD	1	1	2	4	
PEX_HVDD	1	2	2	4	

GPIO Number	I/O	GPIO Name	Function Description
GPIO0	O	NVVDD_PWM	PWM Output to control NVVDD(0 to1V8 PWM output)
GPIO1	O	GC6M:GC6_FB_EN	FB Enable for GC6 2.1
GPIO2	I	GC6M:GPU_EVENT*/WAKE*	GPU wake signal for GC6 2.1
GPIO3	O	NVVDDS_PWM	For MAX-Q detection.
GPIO4	O	GC6M:1V8_MAIN_EN	GPU power sequencing for GC6 2.1
GPIO5	I	FRM_CLK*	Active low Frame Lock
GPIO6		NVVDD_PSI*/NVVDDS_PSI*	Phase Shedding(Optional, check with VR Spec)
GPIO7	O	LCD_BL_PWM	Panel Backlight enable Control signal to turn on a logo LED
GPIO8	O	MEM_VDD_CTL	Memory voltage control
GPIO9	I/O	THERM_ALERT*	Active Low Thermal Alert
GPIO10	O	MEM_VREF_CTL	Memory VREF Control
GPIO11	O	LCD_VDD	Panel Power enable(100 kΩ PD)
GPIO12	I	PWM_LEVEL	AC power detect for PWR supply overdraw input
GPIO13	O	LCD_BLEN	LCD Panel Backlight
GPIO14	I	HPD_IFPA*	Hot Plug Detect for IFPA(Inverted input)
GPIO15	I	HPD_IFPB*	Hot Plug Detect for IFPB(Inverted input)
GPIO16	O	GC6M:SYS_PEX_RST_MON*	System side PCIe reset monitor
GPIO17	I	HPD_IFPD*	Hot Plug Detect for IFPD(Inverted input)
GPIO18	I	HPD_IFPE*	Hot Plug Detect for IFPE(Inverted input)
GPIO19	O	3D Vision/STEREO	3D Vision L/R Signal
GPIO20	I/O	GC5_MODE	Phase Shedding,Optional, check with VR Spec.
GPIO21	I/O	RASTER_SYNC0	Input when master GPU or Output when Slave GPU(100K PD)
GPIO22	I/O	SWAP_RDY0 or SWAPRDY_IN	SLI SWAP READY OUT
GPIO23	I/O	GC6M:GPU_PEX_RST_HOLD*	GPU PCIe self-reset control
GPIO24	I	HPD_IFPF*	Hot Plug Detect for IFPF(Inverted input)
GPIO25	I/O	UNUSED	
GPIO26	I/O	UNUSED	
GPIO27	I	HPD_IFPC*	Hot Plug Detect for IFPC(Inverted input)
GPIO28	I	OC_WARN*/HT	Over current throttling trigger
GPIO29	I	EDPc_OUTPUT_CAP	Input from power supply(0 to 1V8)
GPIO30	I/O	UNUSED	

GPU_PWR_LEVEL(GPIO12)
Low — Low Performace
High — High Performace

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Title: N17E-G1(1/6) PCIE,GPIO

Size: LA-E992P | Document Number | Rev: 1.0

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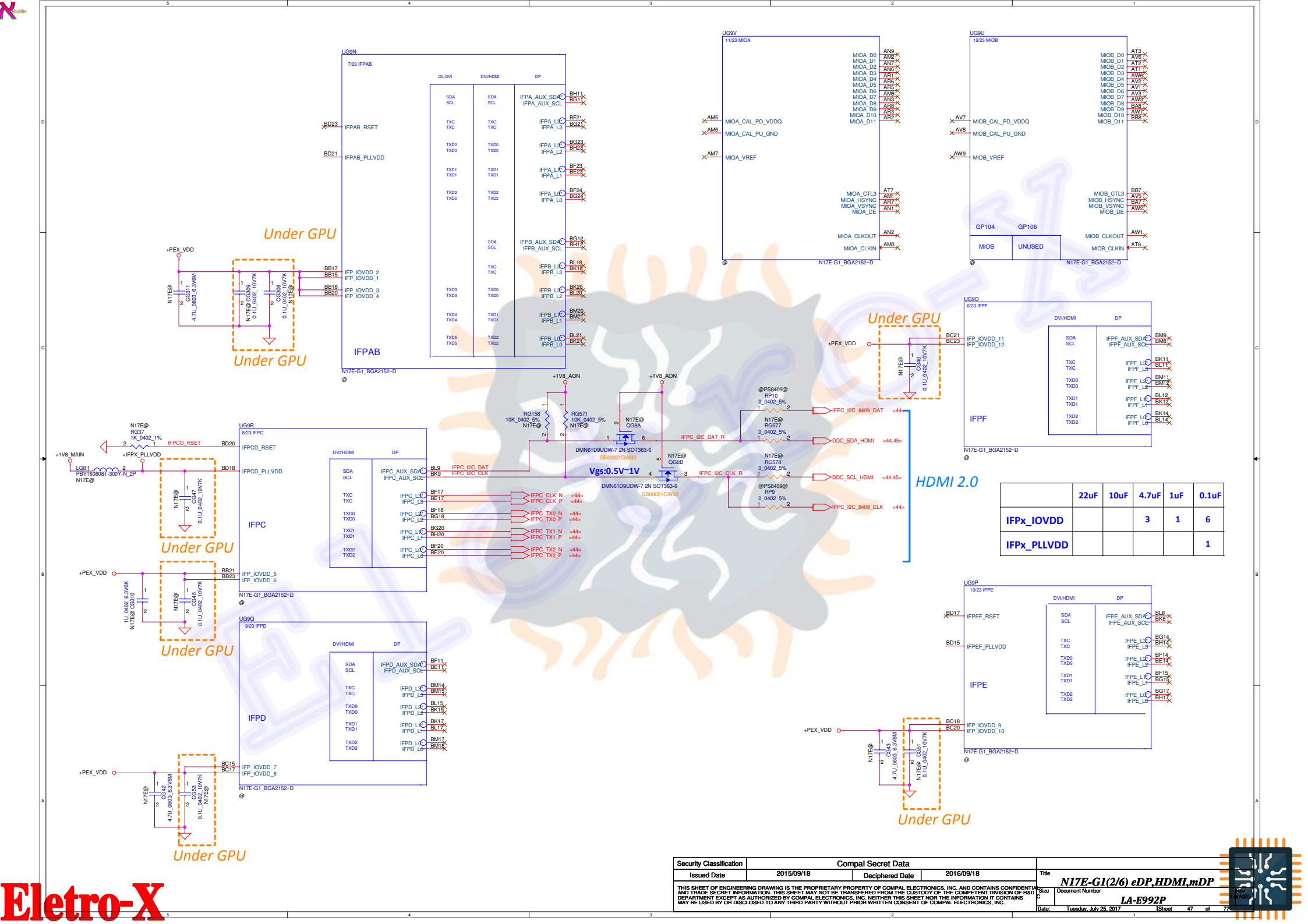

	22uF	10uF	4.7uF	1uF	0.1uF
IFPx_IOVDD			3	1	6
IFPx_PLLVDD					1

Security Classification	Compal Secret Data		
Issued Date	2015/09/18	Deciphered Date	2016/09/18

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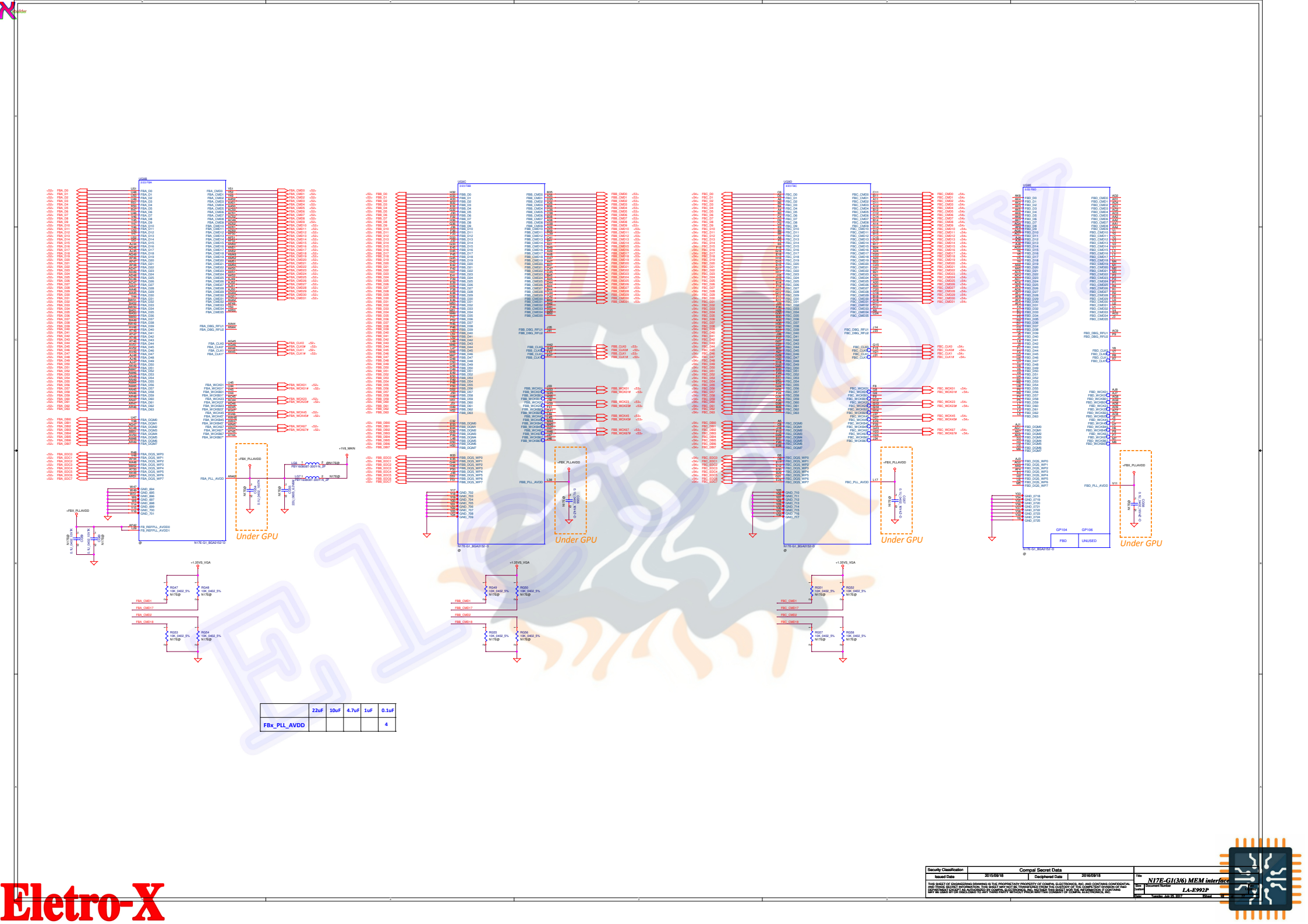
Title: N17E-G1(2/6) eDP,HDMI,mDP

Size: C | Document Number: LA-E992P | Rev: 1A(A00)

Date: Tuesday, July 25, 2017 | Sheet 47 of 77



	22uF	10uF	4.7uF	1uF	0.1uF
FBx_PLL_AVDD					4

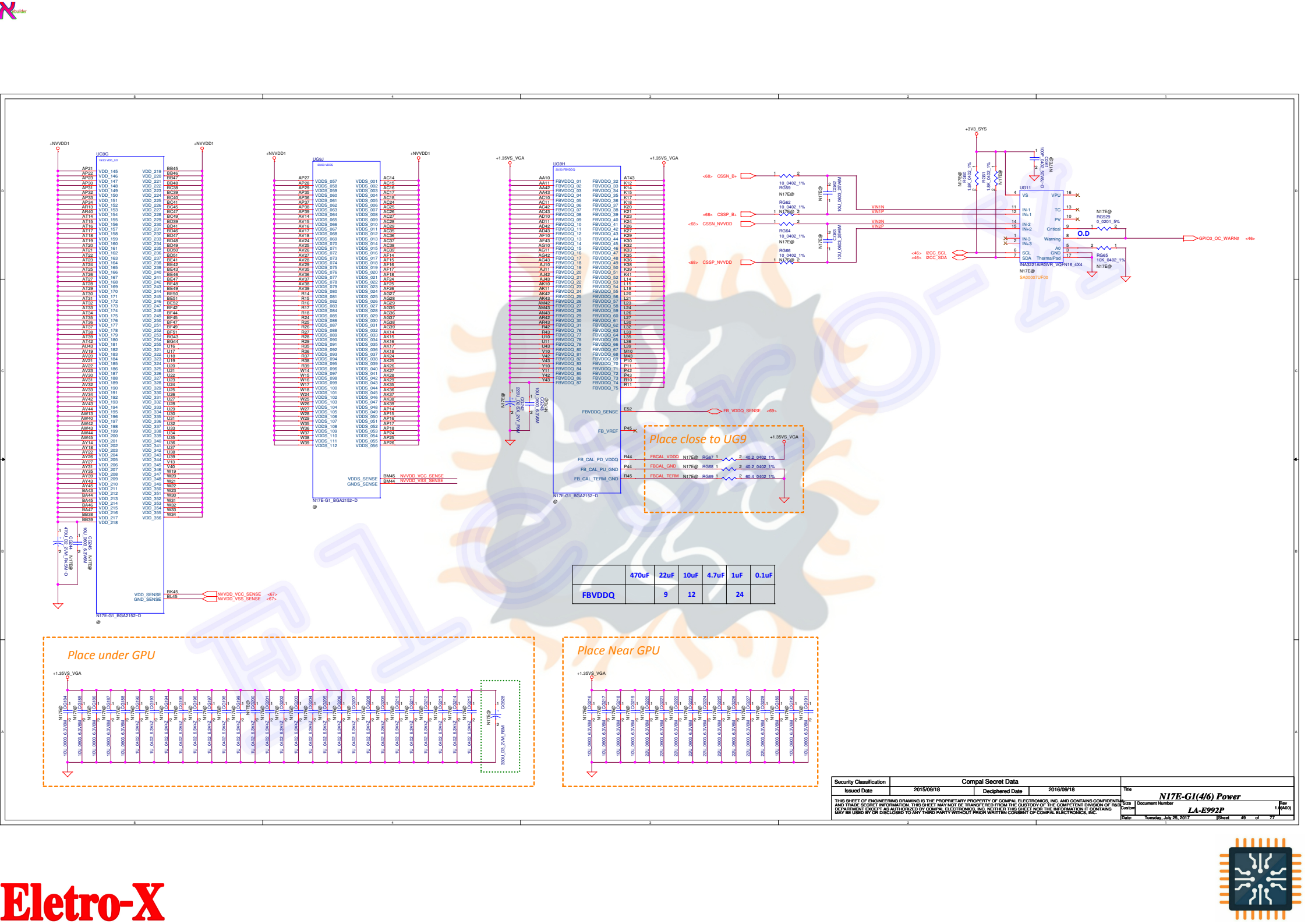
Security Classification	Compal Secret Data		
Issued Date	2015/09/18	Deciphered Date	2016/09/18

Title: N17E-G1(3/6) MEM interface

Size: Document Number: LA-E992P

Rev: 1.0

Date: Tuesday, July 26, 2016 Sheet 46 of 85

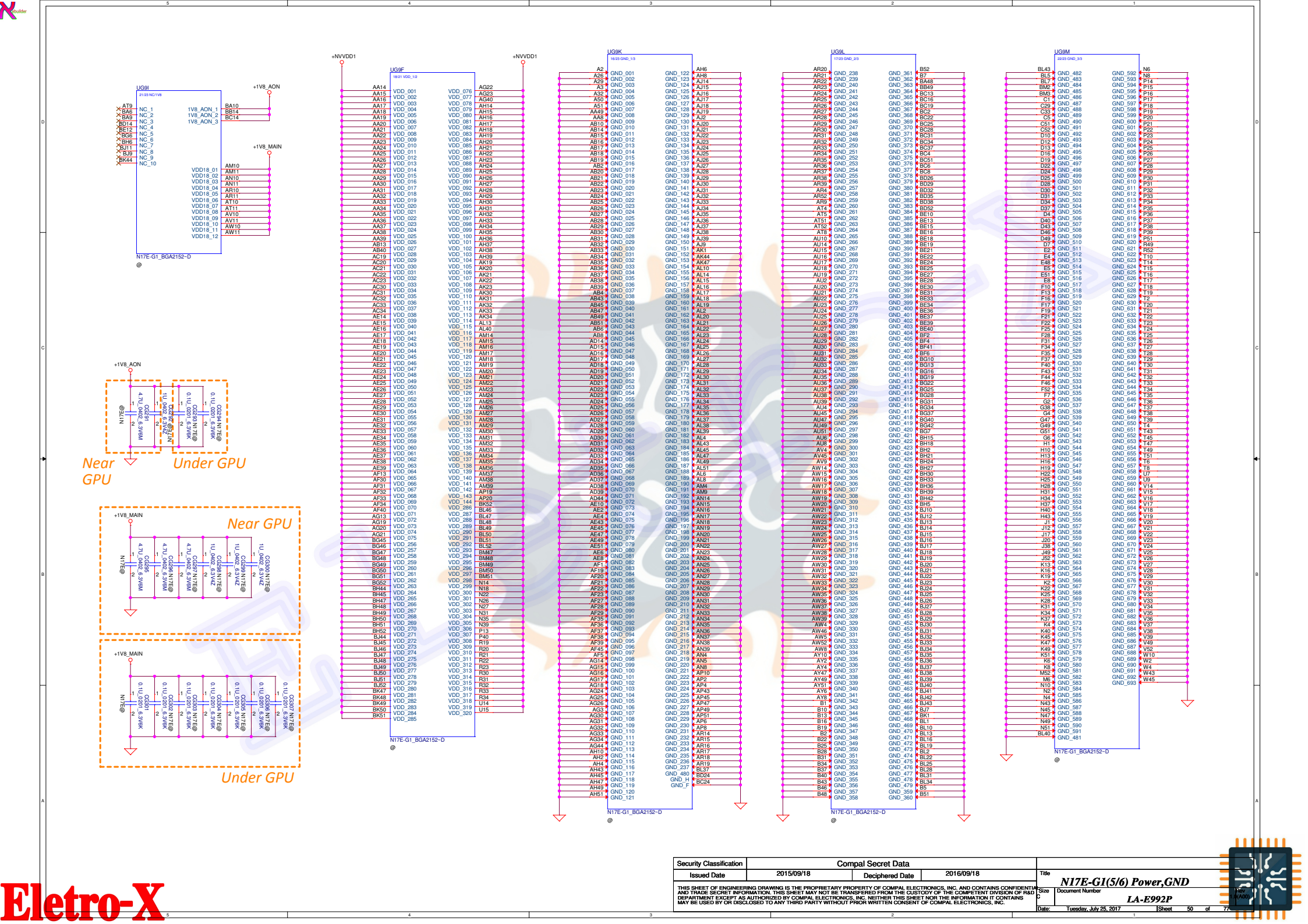


	470uF	22uF	10uF	4.7uF	1uF	0.1uF
FBVDDQ		9	12		24	

Security Classification	Compal Secret Data		
Issued Date	2015/09/18	Deciphered Date	2016/09/18

Title: N17E-G1(4/6) Power

Size: Custom	Document Number: LA-E992P		Rev: 1.0(A00)
Date: Tuesday, July 25, 2017	Sheet 49 of 77		



Security Classification	Compal Secret Data		
Issued Date	2015/09/18	Deciphered Date	2016/09/18

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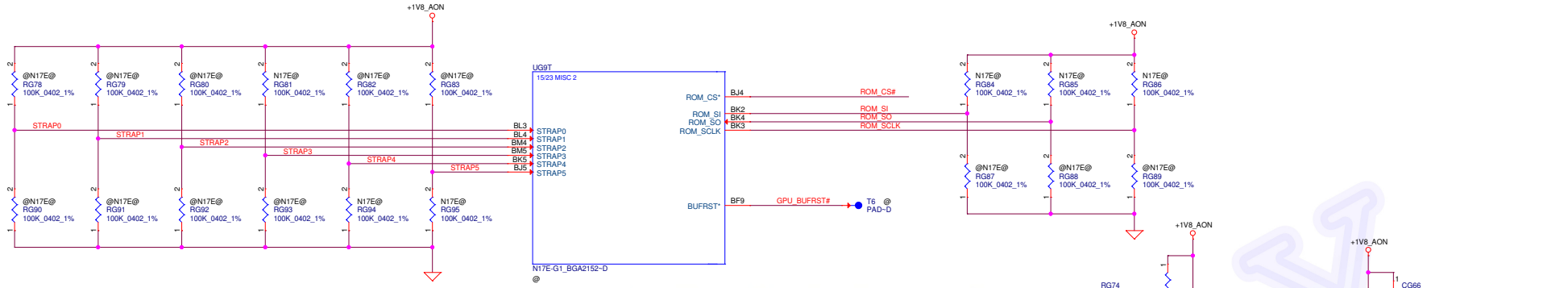
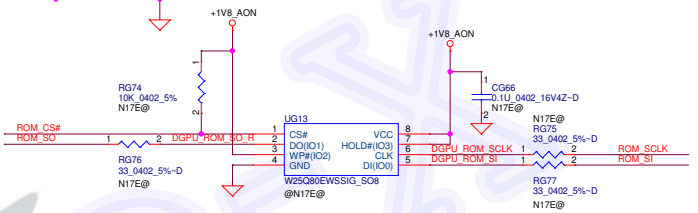
Title	N17E-G1(5/6) Power,GND		
Size C	Document Number LA-E992P		Rev 1A(00)
Date: Tuesday, July 25, 2017	Sheet 50 of 77		





10/25 Need check high(SOIC or WSON)

Table 5.4 Display Link to SORx_EXPOSED Mapping for Down Designs

Total Display Links (HDMI, DP or DVI)	Total Enabled for Audio (HDMI, DP or DVI)	Is IFPD used? (Only supports eDP.)	See This Row of Table 5.5
3	2	YES	12
2	2	NO	12
2	1	YES	8
1	1	NO	8

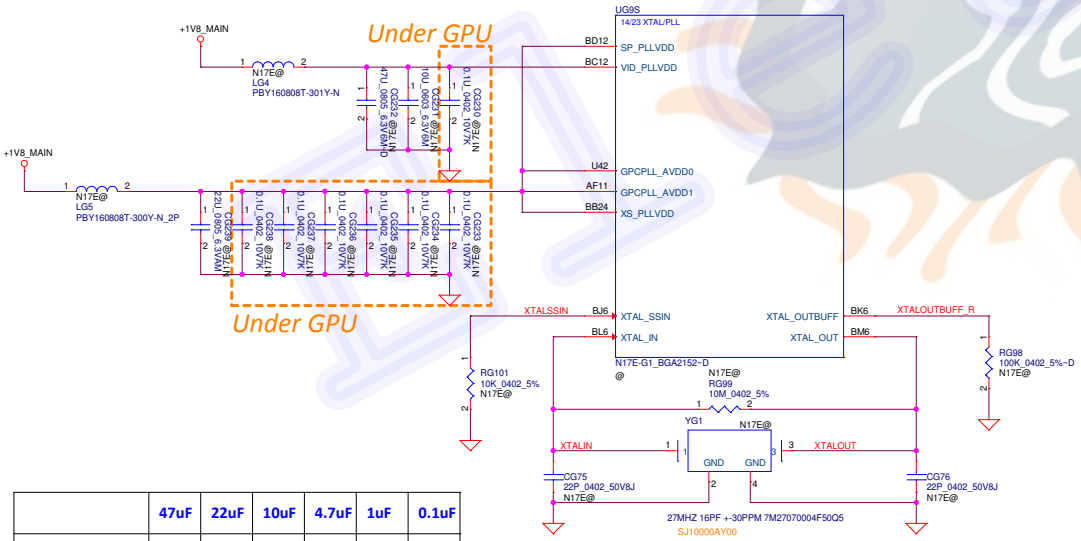
Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_ EXPOSED	SOR2_ EXPOSED	SOR1_ EXPOSED	SOR0_ EXPOSED
8	H	H	H	ENABLED	disabled	disabled	disabled

SMB_ALT_ADDR	
Low	Single GPU
High	Dual GPU

DEVID_SEL	
Low	Original Device ID
High	Re-brand Device ID

VGA_DEVICE	
Low	3D Device
High	VGA Device

PCIE_CFG	
Low	Normal signal swing
High	Reduce the signal amplitude



	47uF	22uF	10uF	4.7uF	1uF	0.1uF
VID_PLLVDD	1		1			1
SP_PLLVDD GPCPLL_AVDD		1				6

N17E-G1 VRAM	Strap0	Strap1	Strap2	Strap3	Strap4	Strap5	RAMCFG
SAMSUNG , K4G80325FB-HC25	L	L	L	H	L	L	0
MICRON , MT51J256M32HF-80:A	H	L	L	H	L	L	1
HYNIX , H5GQ8H24MJR-R4C	L	H	L	H	L	L	2

Table 2. N17E-G1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.55V[2]	Samsung	K4G80325FB-HC25	B-die	0x0	8 Gbps	N/A	Full	Production ready
		1.35V and 1.5V[2]	Micron	MT51J256M32HF-80:A	A-die	0x1	8 Gbps	N/A	Full	Production ready
		1.35V and 1.55V[2]	Hynix	H5GQ8H24MJR-R4C	M-die	0x2	8 Gbps	N/A	Full	Post production ready

Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Security Classification	Compal Secret Data		
Issued Date	2015/09/18	Deciphered Date	2016/09/18

Title	N17E-G1(6/6) strap pin,ROM		
Size C	Document Number	LA-E992P	Rev 1A00
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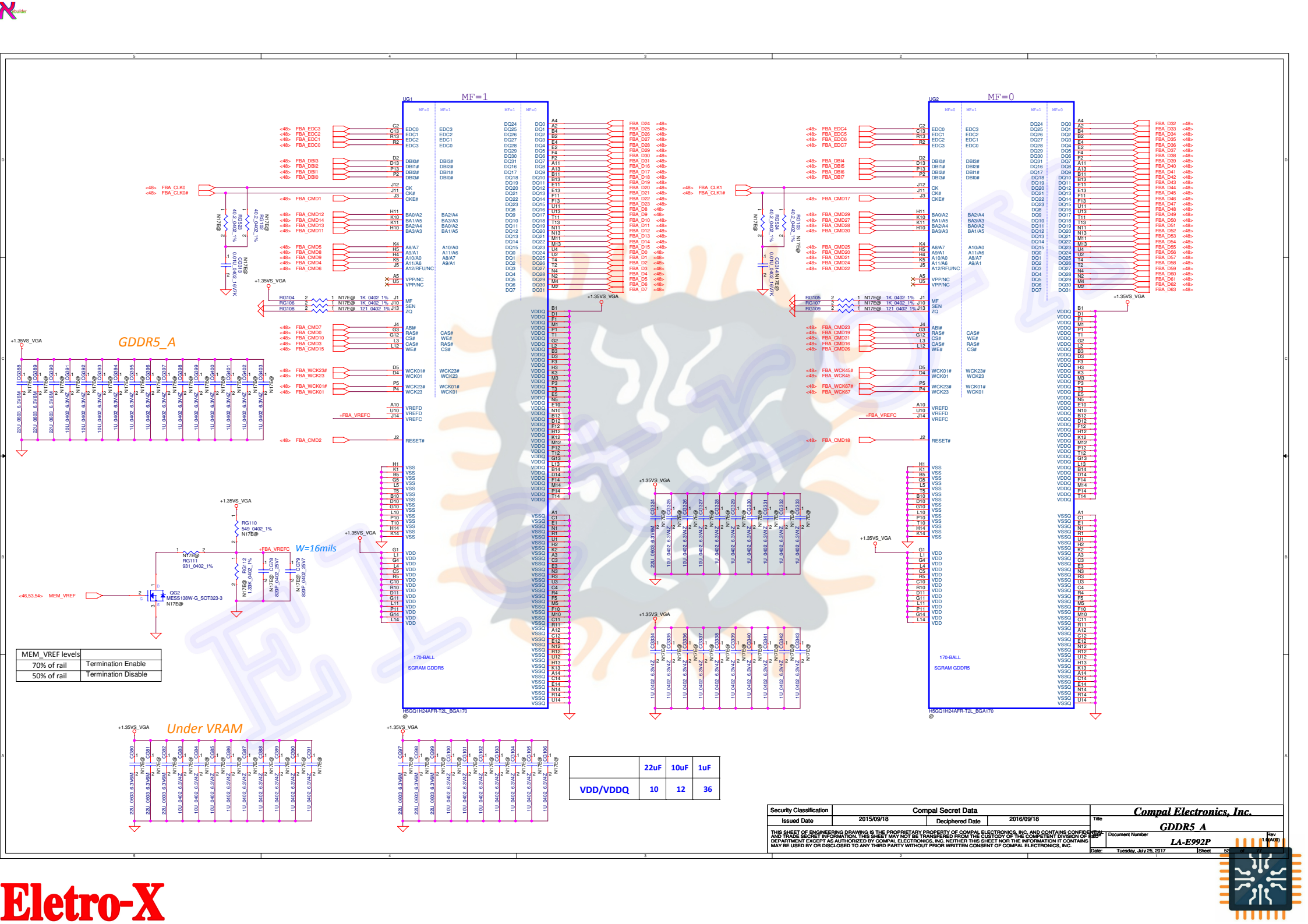
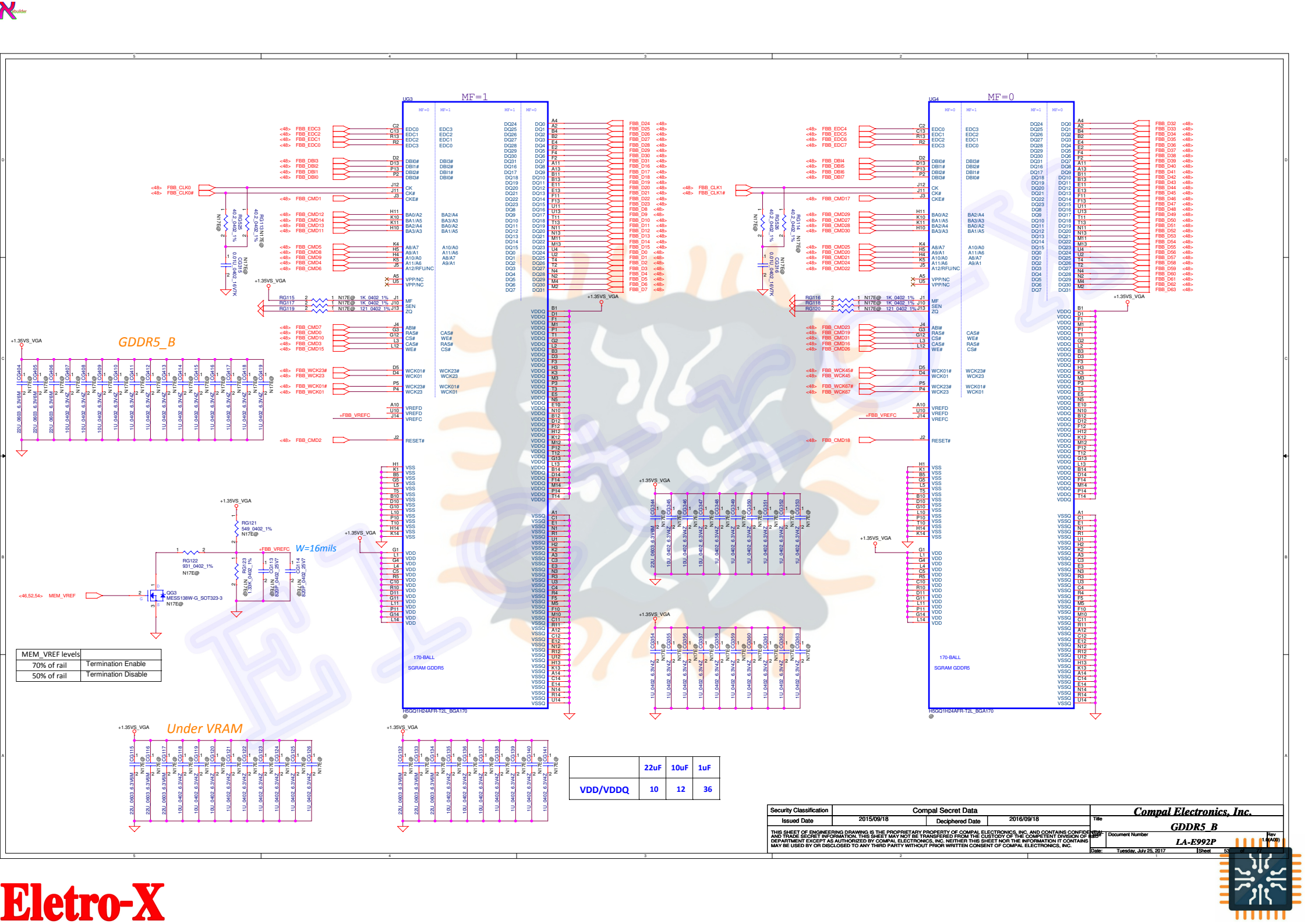
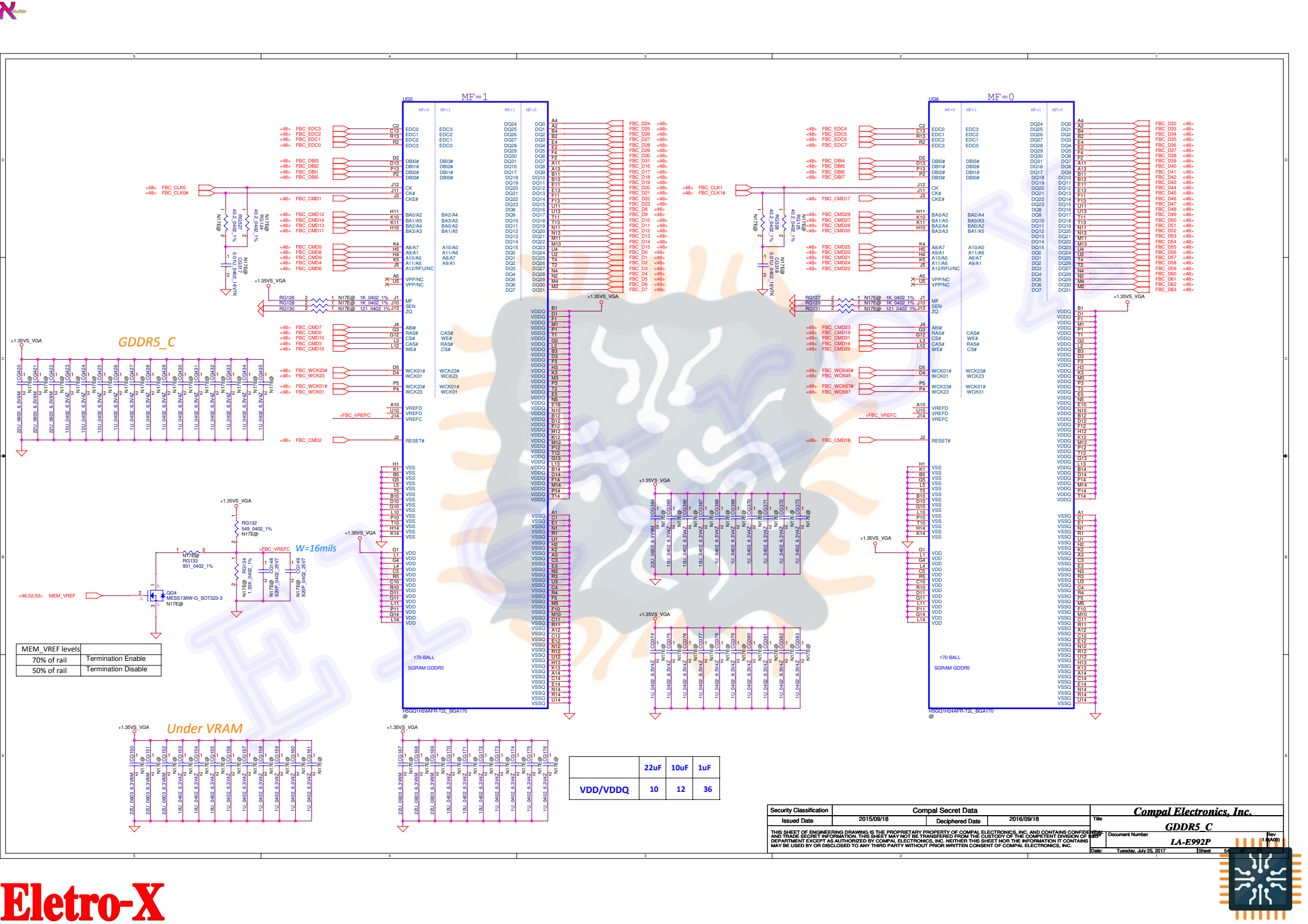

GDDR5_A
MF=1
MF=0
UG1
UG2
+1.35VS_VGA
+FBA_VREFC
MEM_VREF
W=16mils
Under VRAM
170-BALL
SGRAM GDDR5
H5GQ1H24AFR-T2L_BGA170
MEM_VREF levels
70% of rail
Termination Enable
50% of rail
VDD/VDDQ
22uF
10uF
1uF
10
12
36
Security Classification
Compal Secret Data
Issued Date
2015/09/18
Deciphered Date
2016/09/18
Compal Electronics, Inc.
GDDR5_A
LA-E992P
Rev 1.0(A00)
Tuesday, July 25, 2017
Eletro-X





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Title: GDDR5_C

Document Number: LA-E992P

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Eletro-X

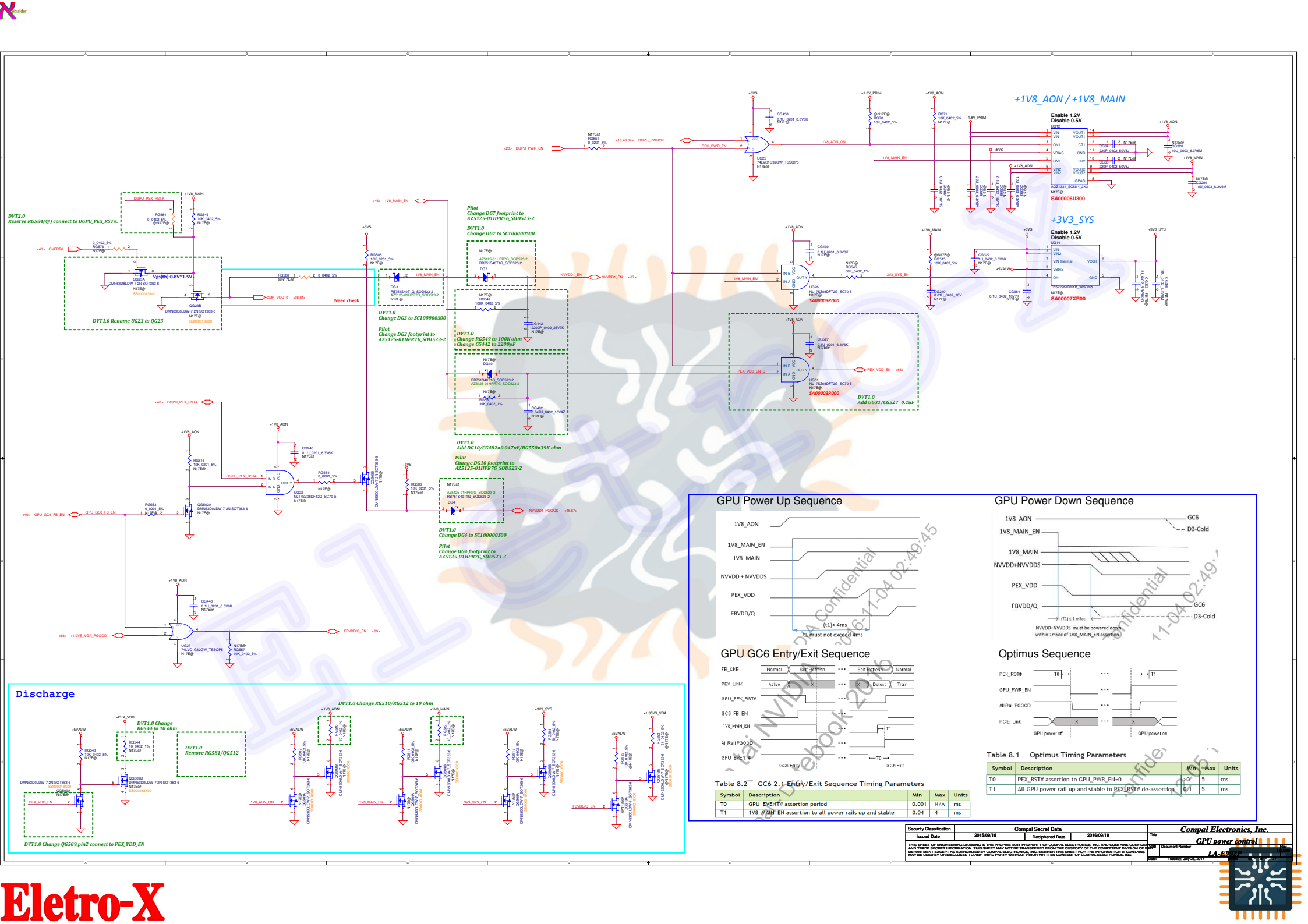

Table 8.2 GC6 2.1 Entry/Exit Sequence Timing Parameters

Symbol	Description	Min	Max	Units
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	1V8_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

Table 8.1 Optimus Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

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Issued Date	2015/09/18	Deciphered Date	2016/09/18

Compal Electronics, Inc.

Title: GPU power control

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MODEL NAME : *CKF50/CKA50*

PCB NO : *LA-E992P*

ZZZ PCB@

PCB CKA50 LA-E992P LS-E992P/E993P 02

DAZ21J00310

CPU

UH1 I7_QLM5@ — *R1* — KBL-H_QLM5 — *SA0000AD70L*

UH1 I5_QLM7@ — *R1* — KBL-H_QLM7 — *SA0000AD80L*

UH1 I7_MP@ — *R3* — KBL-H_SR32Q — *SA0000AD72L*

UH1 I5_MP@ — *R3* — KBL-H_SR32S — *SA0000AD82L*

PCH

UH2 QLF9@ — PCH_QLF9 — *SA0000ADB0L*

UH2 SR30W@ — PCH_SR30W — *SA0000ADB2L*

GPU

UG9 N17E_G1@ — N17E-G1-A1 — *SA00009PM1L*

Bom Structure

Samsung 6G X7673331L07 : S6G@

UG1 K4G80325FB-HC25 S6G@ *SA00009TA1L*	UG2 K4G80325FB-HC25 S6G@ *SA00009TA1L*	RG90 100K_0402_1% S6G@ *SD034100380*
UG3 K4G80325FB-HC25 S6G@ *SA00009TA1L*	UG4 K4G80325FB-HC25 S6G@ *SA00009TA1L*	RG91 100K_0402_1% S6G@ *SD034100380*
UG5 K4G80325FB-HC25 S6G@ *SA00009TA1L*	UG6 K4G80325FB-HC25 S6G@ *SA00009TA1L*	RG92 100K_0402_1% S6G@ *SD034100380*

Micron 6G X7673331L09 : M6G@

UG1 MT51J256M32HF-80:A M6G@ *SA00009TI1L*	UG2 MT51J256M32HF-80:A M6G@ *SA00009TI1L*	RG78 100K_0402_1% M6G@ *SD034100380*
UG3 MT51J256M32HF-80:A M6G@ *SA00009TI1L*	UG4 MT51J256M32HF-80:A M6G@ *SA00009TI1L*	RG91 100K_0402_1% M6G@ *SD034100380*
UG5 MT51J256M32HF-80:A M6G@ *SA00009TI1L*	UG6 MT51J256M32HF-80:A M6G@ *SA00009TI1L*	RG92 100K_0402_1% M6G@ *SD034100380*

Hynix 6G X7673331L08 : H6G@

UG1 H5GQ8H24MJR-R4C H6G@ *SA00009TM1L*	UG2 H5GQ8H24MJR-R4C H6G@ *SA00009TM1L*	RG90 100K_0402_1% H6G@ *SD034100380*
UG3 H5GQ8H24MJR-R4C H6G@ *SA00009TM1L*	UG4 H5GQ8H24MJR-R4C H6G@ *SA00009TM1L*	RG79 100K_0402_1% H6G@ *SD034100380*
UG5 H5GQ8H24MJR-R4C H6G@ *SA00009TM1L*	UG6 H5GQ8H24MJR-R4C H6G@ *SA00009TM1L*	RG92 100K_0402_1% H6G@ *SD034100380*

X43		431A7631L51 SMT MB AE992 CKF50 KBL I5 N17EG1 6G	431A7631L52 SMT MB AE992 CKF50 KBL I7 N17EG1 6G	431A7631L01 SMT MB AE992 CKA50 KBL I7 N17EG1 PTT 6G	431A7631L02 SMT MB AE992 CKA50 KBL I5 N17EG1 PTT 6G
PCB P/N	PCB@	V	V	V	V
Project ID	AMN@			V	V
	FSTR@	V	V		
CPU P/N	I5_MP@	V			V
	I7_MP@		V	V	
	I5_QLM7@				
	I7_QLM5@				
PCH P/N	SR30W@	V	V	V	V
	QLF9@				
GPU ID Model ID	UMA@				
	N17P_G0@				
	N17P_G1@				
	N17E_G1@	V	V	V	V
N17E GPU	N17E@	V	V	V	V
Phase ID Board ID	EVT@				
	DVT1@				
	DVT2@				
	PILOT@	V	V	V	V
TBT	TBT@	V	V	V	V
TPS65982D	PD@	V	V	V	V
PS8409	PS8409@	V	V	V	V
DP to VGA	VGA@			V	V
Free Fall sensor	FFS@			V	V
TPM	TPM@				
	NON_TPM@	V	V	V	V
E991/E992 TPM Option	991@TPM@				
	992@TPM@				
USB3.0 re-driver	PARADE@	V	V	V	V
	PERICOM@				
Touch Screen	TS@	V	V	V	V
XDP	XDP@	V	V	V	V
Debug LED&Button	DEBUG@				
USB Port 100u Cap	RBOM@				
Connector	CONN@				
Reserve	@N17E@				
	@PS8409@				

X4E		X4EA7631L51 SMT EMC FOR EE N17E AE992 CKF50	X4EA7631L01 SMT EMC FOR EE N17E AE992 CKA50
Touch FP with power buttoN	FP1@EMI@	V	V
	FP1@ESD@	V	V
Gernal EMI	EMI@	V	V
Gernal ESD	ESD@	V	V
TBT	TBT@EMI@	V	V
	TBT@ESD@	V	V
PD-TPS65982D	PD@ESD@	V	V
Touch Screen	TS@EMI@	V	V
	TS@ESD@	V	V
RF	RF@	V	V
VGA EMI	VGA@EMI@		V
991 PCH SPI CLK	991@EMI@		
992 PCH SPI CLK	992@EMI@	V	V
Reserve	@EMI@		
	@ESD@		
	@RF@		
	@TS@EMI@		

X76	X7673331L07 ALT. GROUP PARTS SAMSUNG 6G VRAM CKA50	X7673331L08 ALT. GROUP PARTS HYNIX 6G VRAM CKA50	X7673331L09 ALT. GROUP PARTS MICRON 6G VRAM CKA50
S6G@	√		
H6G@		√	
M6G@			√

Security Classification	Compal Secret Data		
Issued Date	2013/04/10	Deciphered Date	2014/05/01

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Title: *NOTE*

Size | Document Number: *LA-E992P* | Rev: 1.0(A00)

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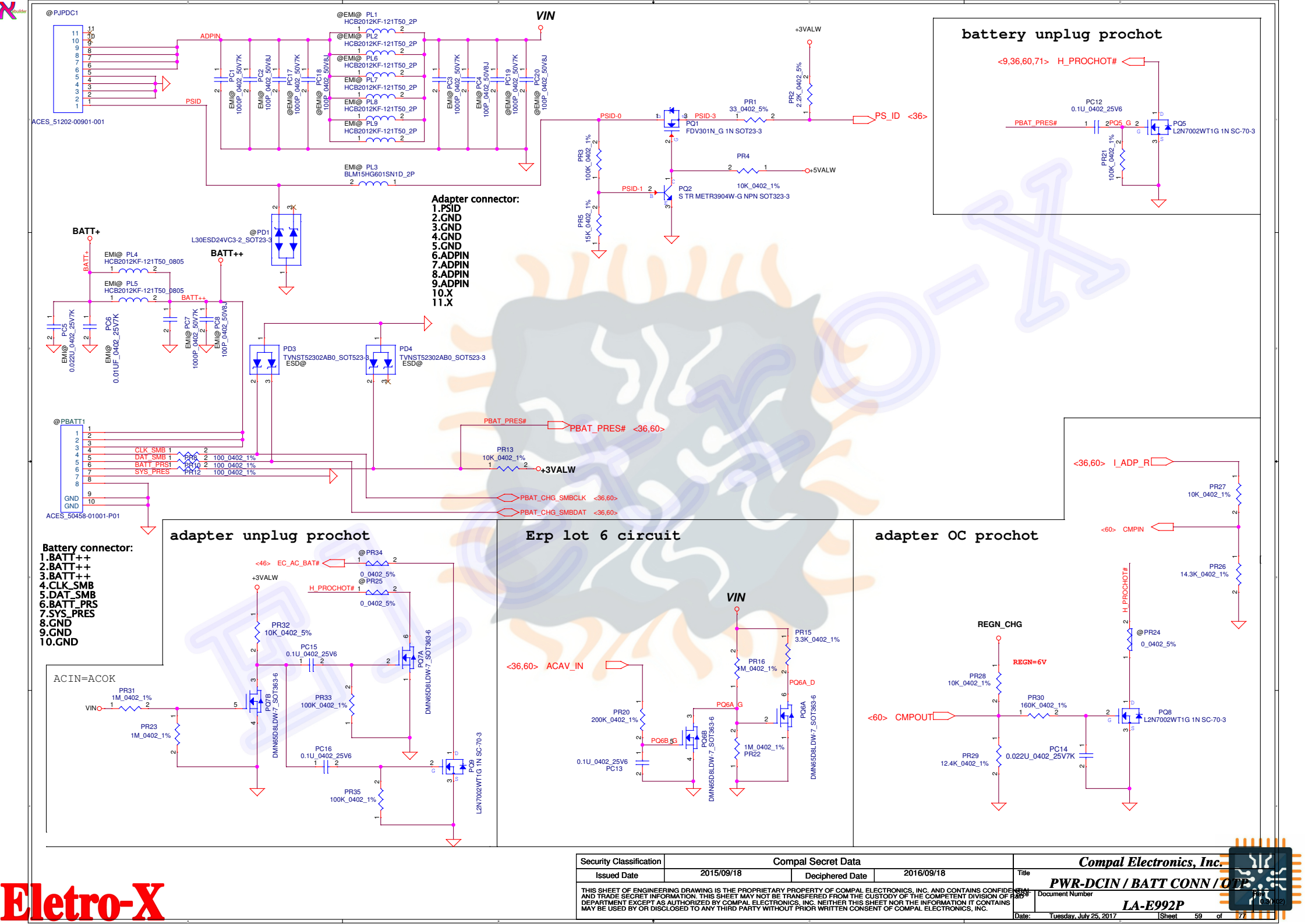

Security Classification	Compal Secret Data		
Issued Date	2015/09/18	Deciphered Date	2016/09/18

Compal Electronics, Inc.

Title: PWR-DCIN / BATT CONN / OTP

Size: A3 | Document Number: LA-E992P | Rev: 1.0

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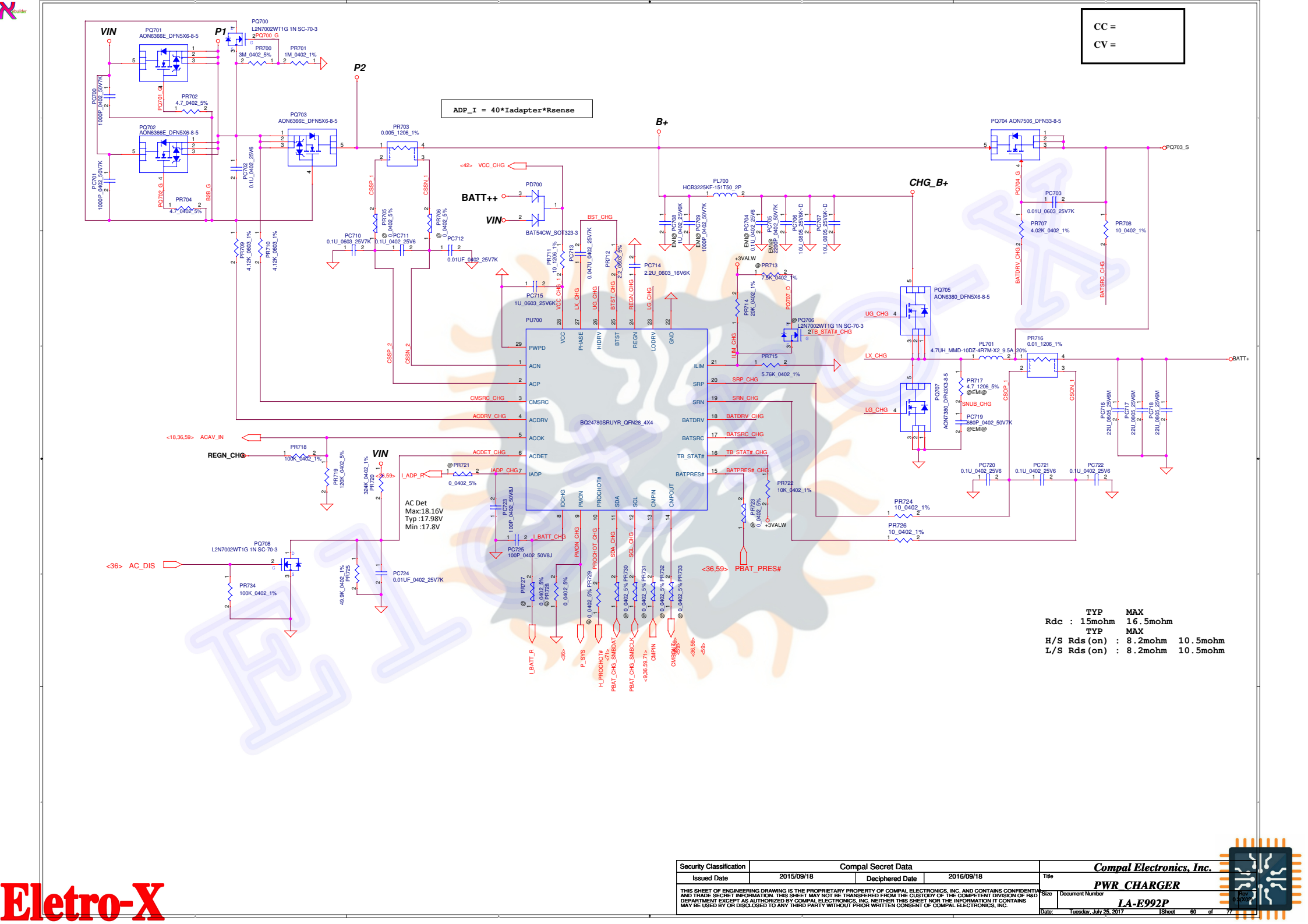
CC =
CV =
ADP_I = 40*Iadapter*Rsense
VIN
P1
P2
B+
CHG_B+
BATT++
VIN
BQ24780SRUYR_QFN28_4X4
AC Det
Max:18.16V
Typ :17.98V
Min :17.8V
TYP MAX
Rdc : 15mohm 16.5mohm
TYP MAX
H/S Rds(on) : 8.2mohm 10.5mohm
L/S Rds(on) : 8.2mohm 10.5mohm
Security Classification
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Issued Date
2015/09/18
Deciphered Date
2016/09/18
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Title
PWR_CHARGER
Size
Document Number
LA-E992P
Rev
0.3
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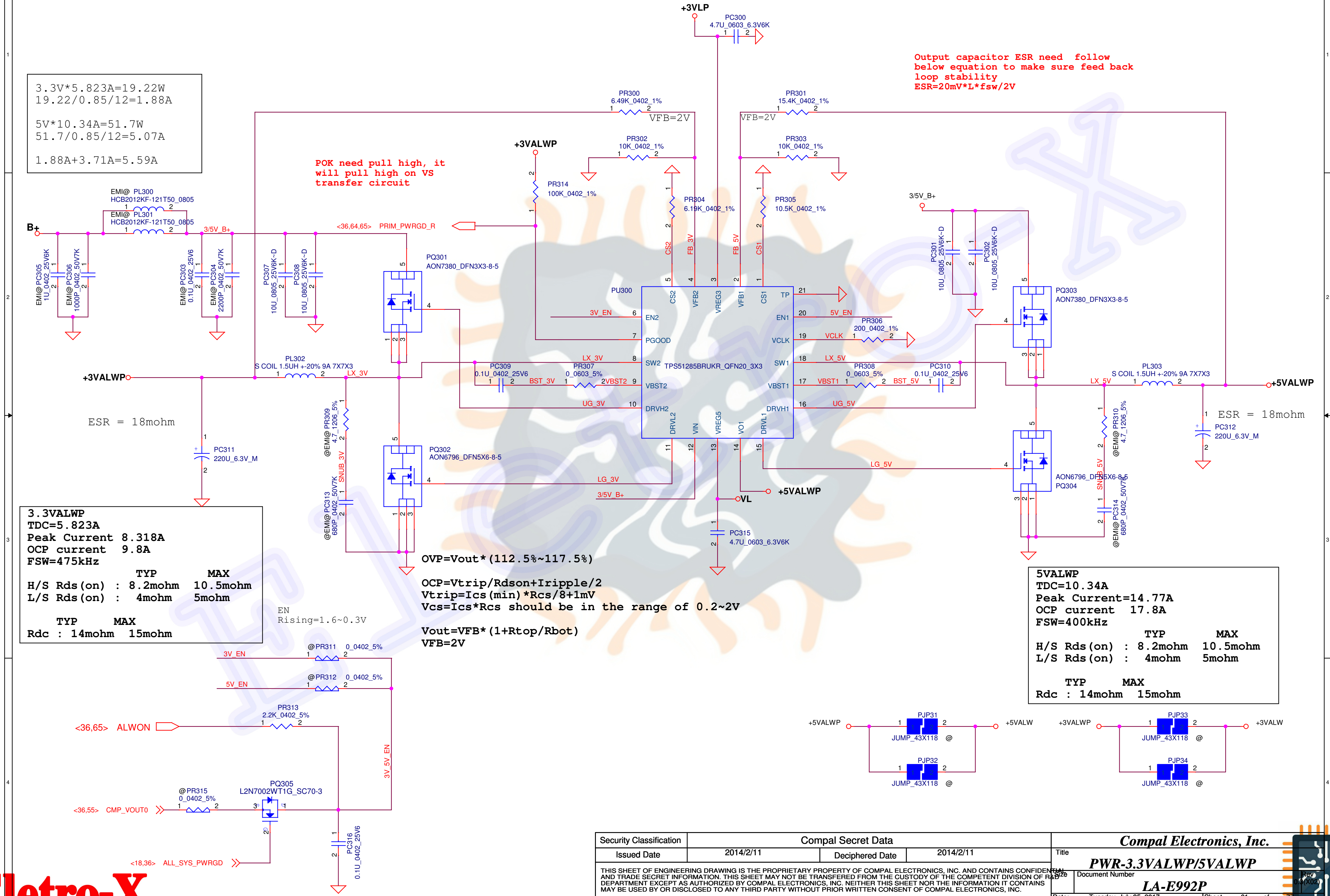


3.3V*5.823A=19.22W
19.22/0.85/12=1.88A

5V*10.34A=51.7W
51.7/0.85/12=5.07A

1.88A+3.71A=5.59A

3.3VALWP
TDC=5.823A
Peak Current 8.318A
OCP current 9.8A
FSW=475kHz

	TYP	MAX
H/S Rds(on) :	8.2mohm	10.5mohm
L/S Rds(on) :	4mohm	5mohm
Rdc :	14mohm	15mohm

OVP=Vout*(112.5%~117.5%)

OCP=Vtrip/Rdson+Iripple/2
Vtrip=Ics(min)*Rcs/8+1mV
Vcs=Ics*Rcs should be in the range of 0.2~2V

Vout=VFB*(1+Rtop/Rbot)
VFB=2V

5VALWP
TDC=10.34A
Peak Current=14.77A
OCP current 17.8A
FSW=400kHz

	TYP	MAX
H/S Rds(on) :	8.2mohm	10.5mohm
L/S Rds(on) :	4mohm	5mohm
Rdc :	14mohm	15mohm

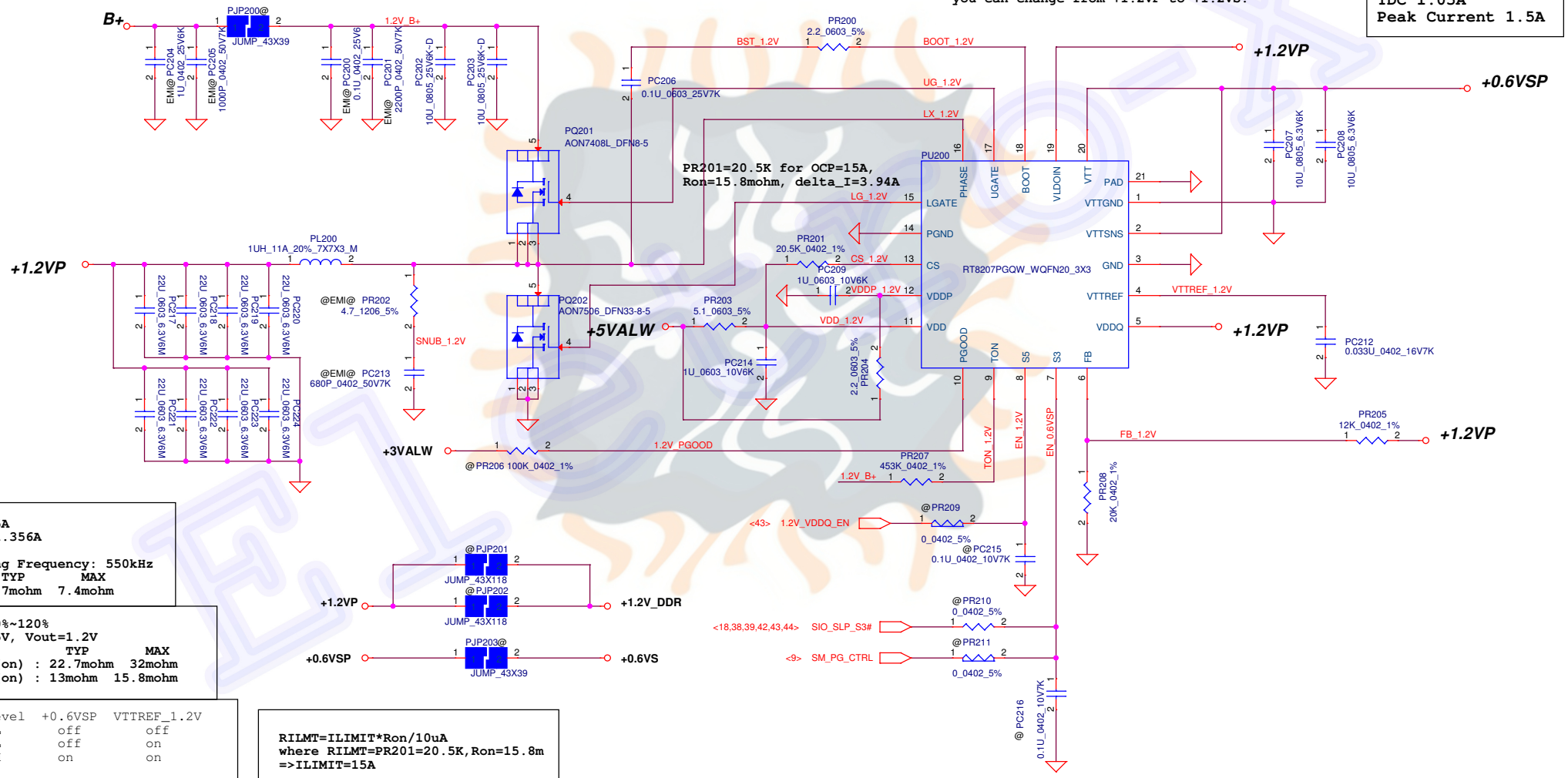
Security Classification	Compal Secret Data		
Issued Date	2014/2/11	Deciphered Date	2014/2/11

Compal Electronics, Inc.
Title: *PWR-3.3VALWP/5VALWP*
Document Number: *LA-E992P*
Date: Tuesday, July 25, 2017 Sheet 61 of 7?

Input Current: 0.935A
1.2V*7.95A/0.85/12V=0.935

Pin19 need pull separate from +1.2VP.
If you have +1.2V and +0.6V sequence question,
you can change from +1.2VP to +1.2VS.

0.6VSP
TDC 1.05A
Peak Current 1.5A



1.2VP
TDC=7.95A
Ipeak=11.356A
OCP=15A
Switching Frequency: 550kHz

	TYP	MAX
DCR :	6.7mohm	7.4mohm

OVP: 110%~120%
VFB=0.75V, Vout=1.2V

	TYP	MAX
H/S Rds(on) :	22.7mohm	32mohm
L/S Rds(on) :	13mohm	15.8mohm

Mode	Level	+0.6VSP	VTTREF_1.2V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

RILMT=ILIMIT*Ron/10uA
where RILMT=PR201=20.5K,Ron=15.8m
=>ILIMIT=15A

Security Classification	Compal Secret Data		
Issued Date	2015/09/18	Deciphered Date	2016/09/18

Compal Electronics, Inc.

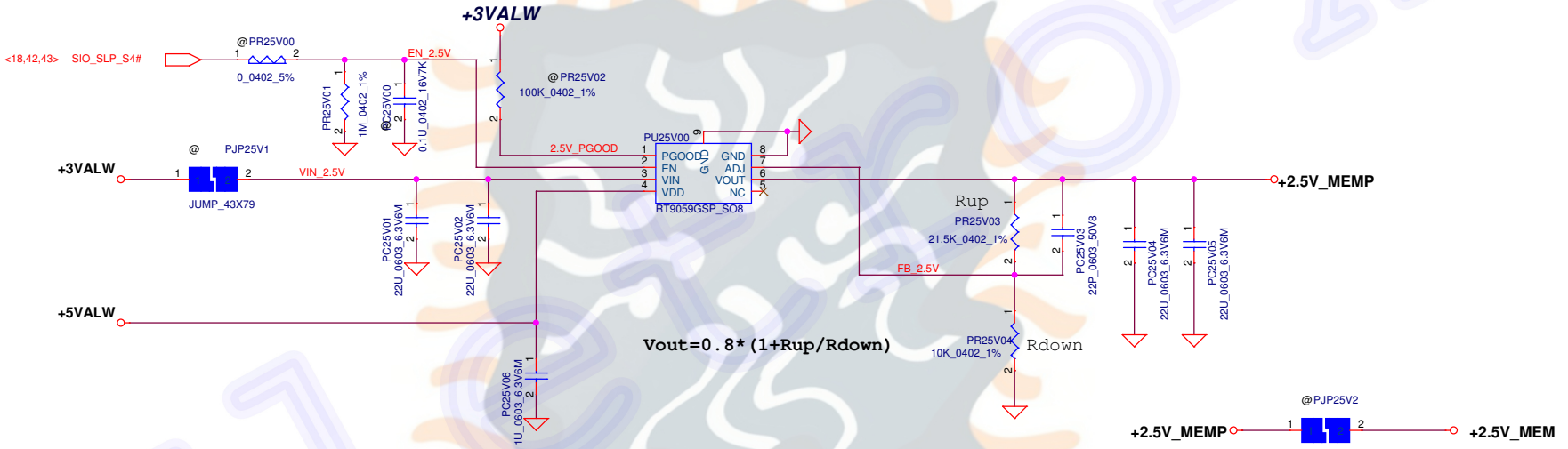
Title: PWR-1.2VP/0.6VSP

Size: | Document Number: LA-E992P | Rev: 1.0

Date: Tuesday, July 25, 2017 | Sheet 62 of 77

Input Current:0.42A

2.5*0.428=1.07W
1.07/0.85/3=0.42A



+2.5V_MEM
TDC 0.428A
Peak Current 0.612A
OCP Current 3.5A

Security Classification	Compal Secret Data		
Issued Date	2015/09/18	Deciphered Date	2016/09/18

Compal Electronics, Inc.

Title: PWR_+2.5V_MEM

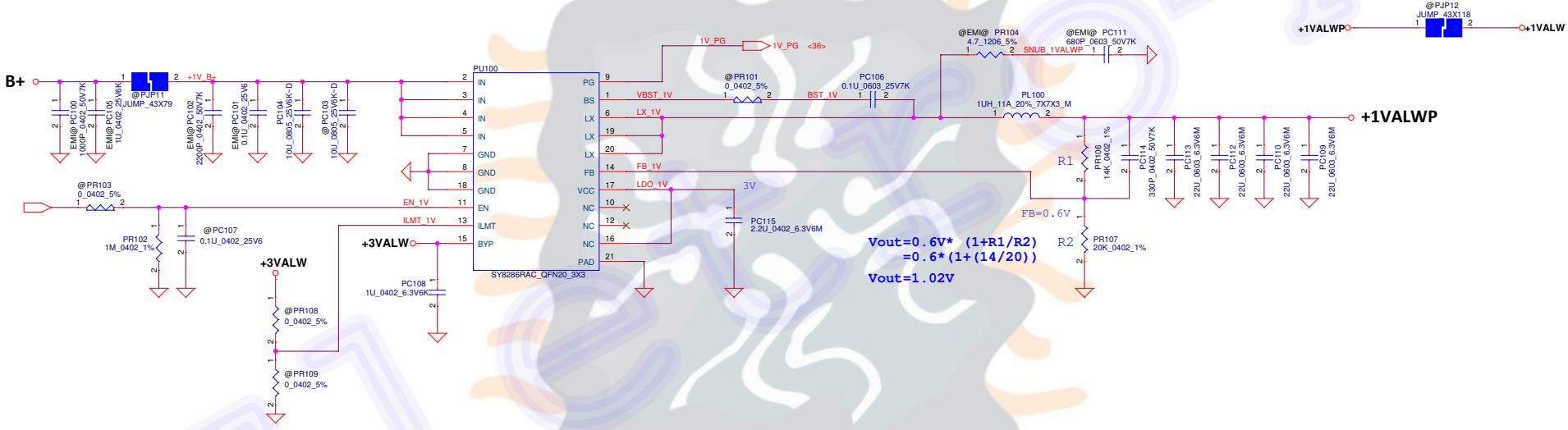
Size | Document Number: LA-E992P | Rev: 1.0(0.2)

Date: Tuesday, July 25, 2017 | Sheet 63 of 77

Input Current: 0.42A
1V*4.2805A/0.85/12V=0.42

+1VALW
TDC 4.2805A
Peak Current 6.115A
OCP current 9A
FSW=500KHz
TYP MAX
DCR: 6.7mohm 7.4mohm

IL=1.9A@19.5V
ripple=7.3mV@19.5V



The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high.

PWR.Plane.Regulator(35.25), Support component(35.26)

Security Classification	Compal Secret Data		
Issued Date	2015/09/18	Deciphered Date	2016/09/18

Compal Electronics, Inc.

Title: PWR-+1VALWP

Size: A3 | Document Number: LA-E991P | Rev: 0.3(X02)

Date: Tuesday, July 25, 2017 | Sheet 64 of 77

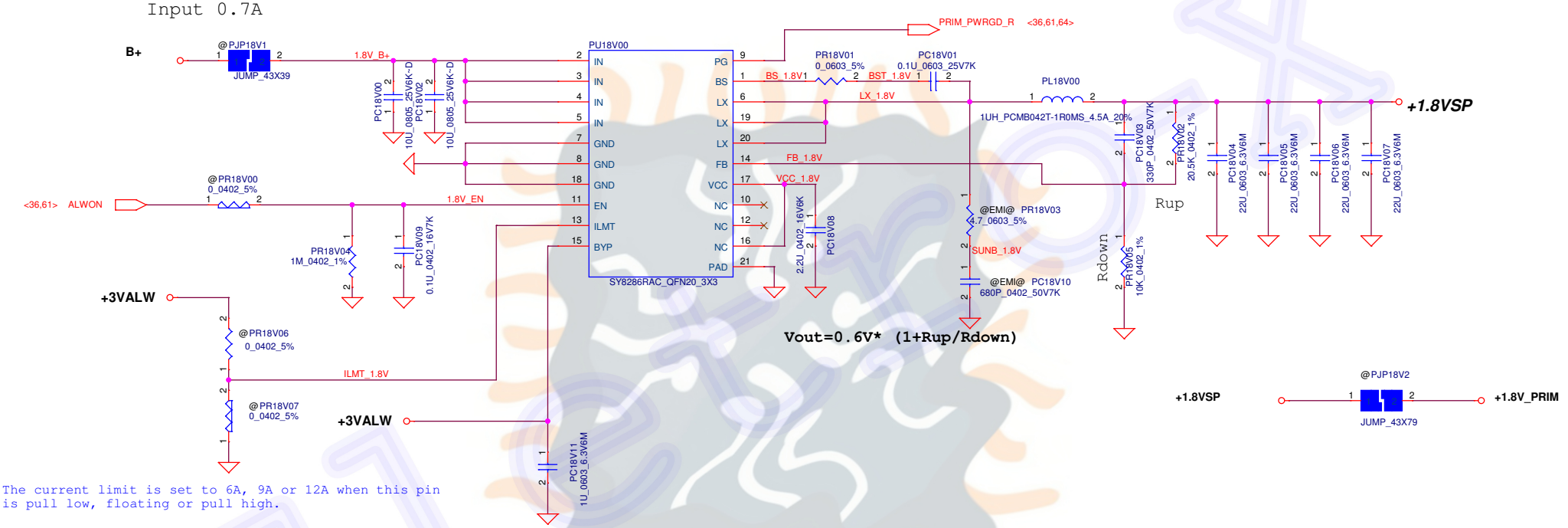
Input Current:0.227A

1.8*1.289/0.85/12V=0.227A

+1.8VSP
TDC 1.289A
Peak Current 1.842A
OCP current 6A
FSW=500KHz

	TYP	MAX
DCR:	24mohm	27mohm

Input 0.7A



The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high.

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: PWR_+1.8VSP

Size | Document Number: LA-E992P | Rev: 1.0(0X02)

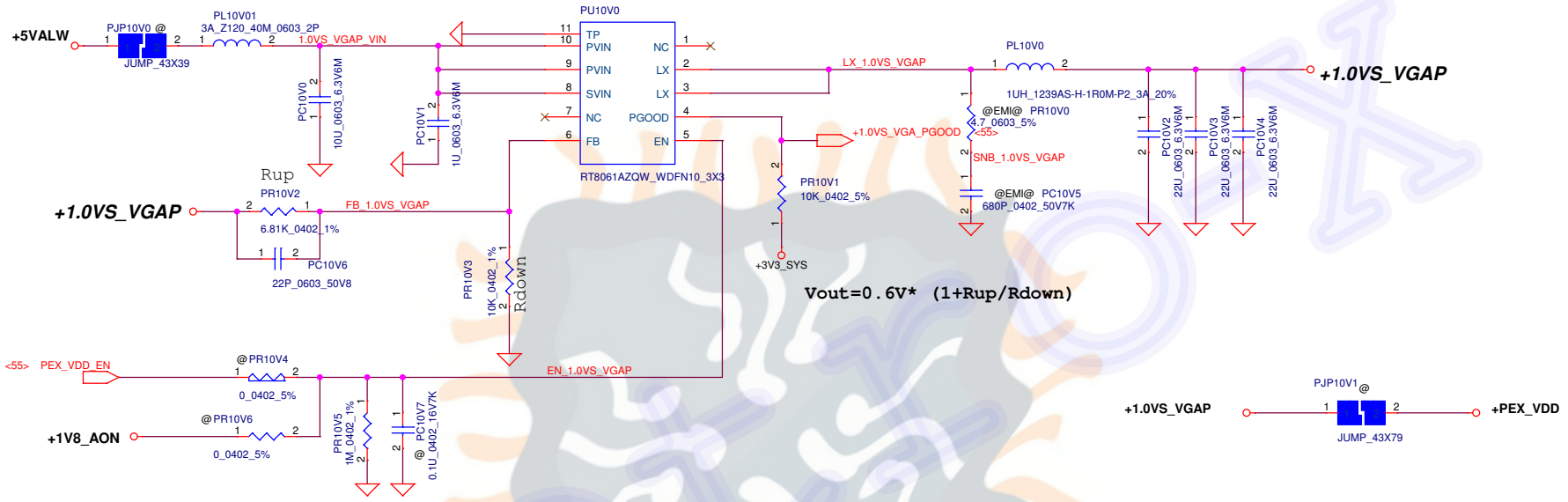
Date: Tuesday, July 25, 2017 | Sheet 65 of

Input Current:0.231A

1*0.9835/0.85/5=0.231A

+1.0VS_VGAP
TDC 0.9835A
Peak Current 1.405A
OCP current 4A
FSW=1MHz

	TYP	MAX
DCR	45mohm	59mohm



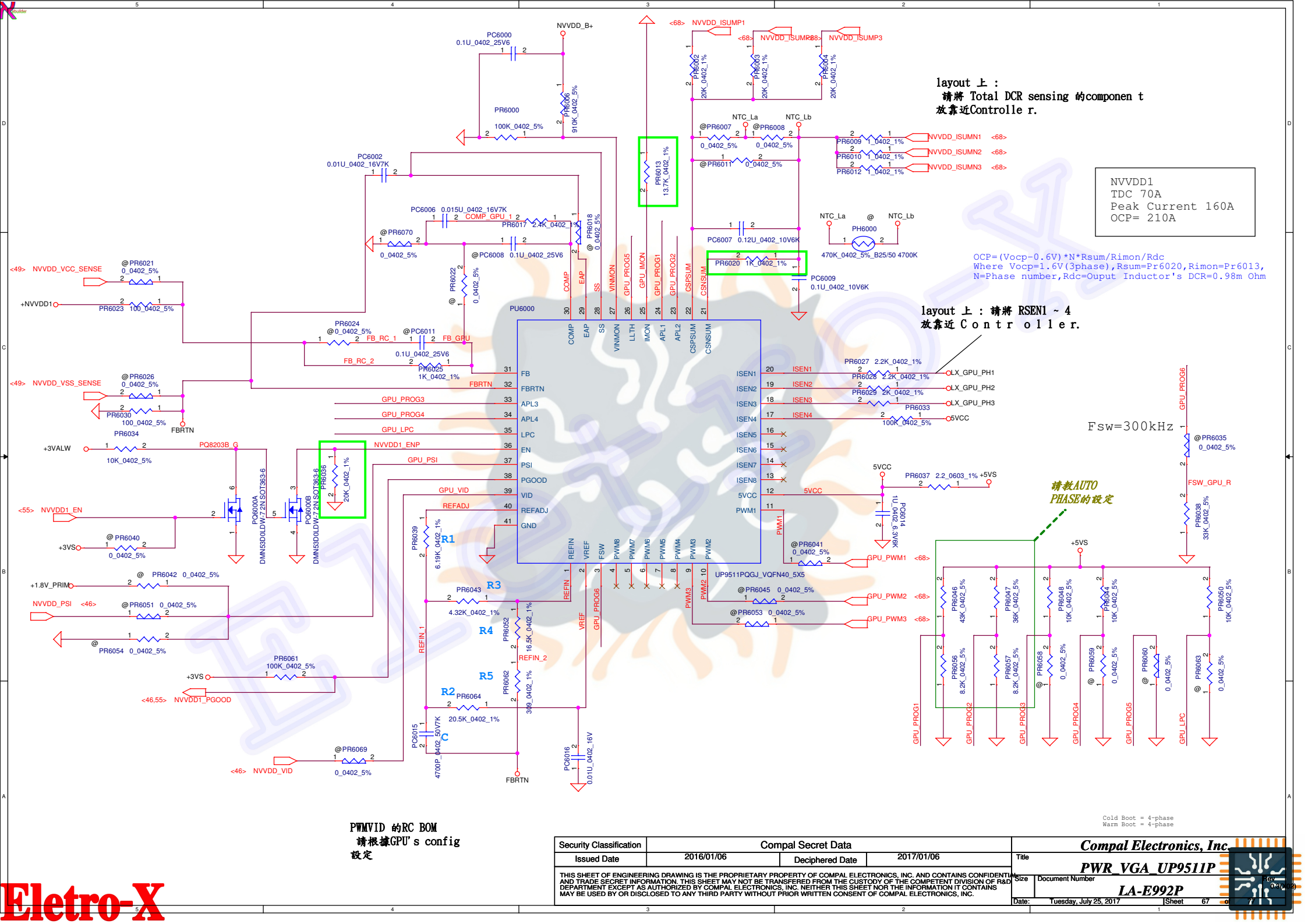
Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: PWR_+1.0VS_VGA

Size | Document Number: LA-E992P | Rev: 0.3(x2)

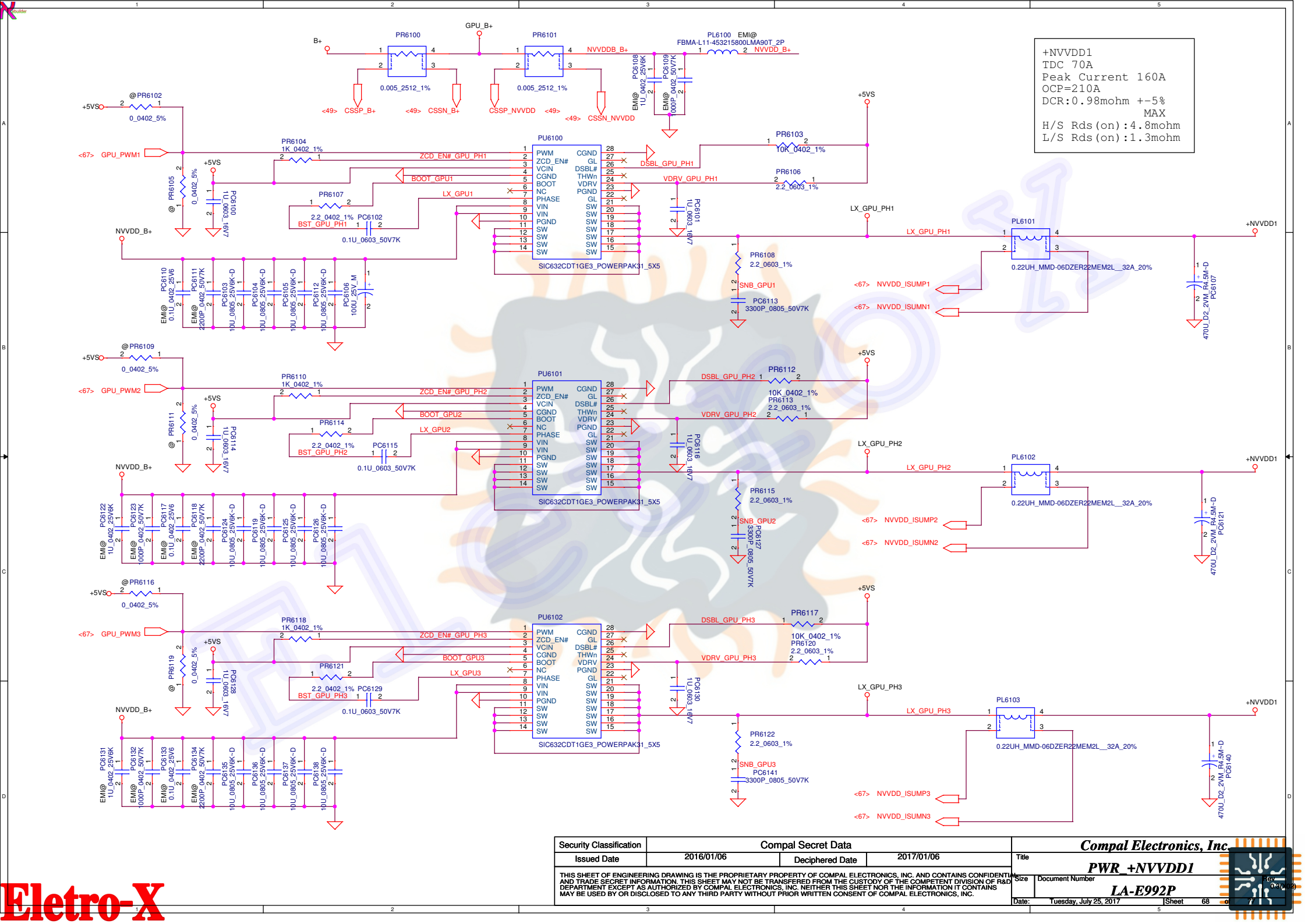
Date: Tuesday, July 25, 2017 | Sheet 66 of



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

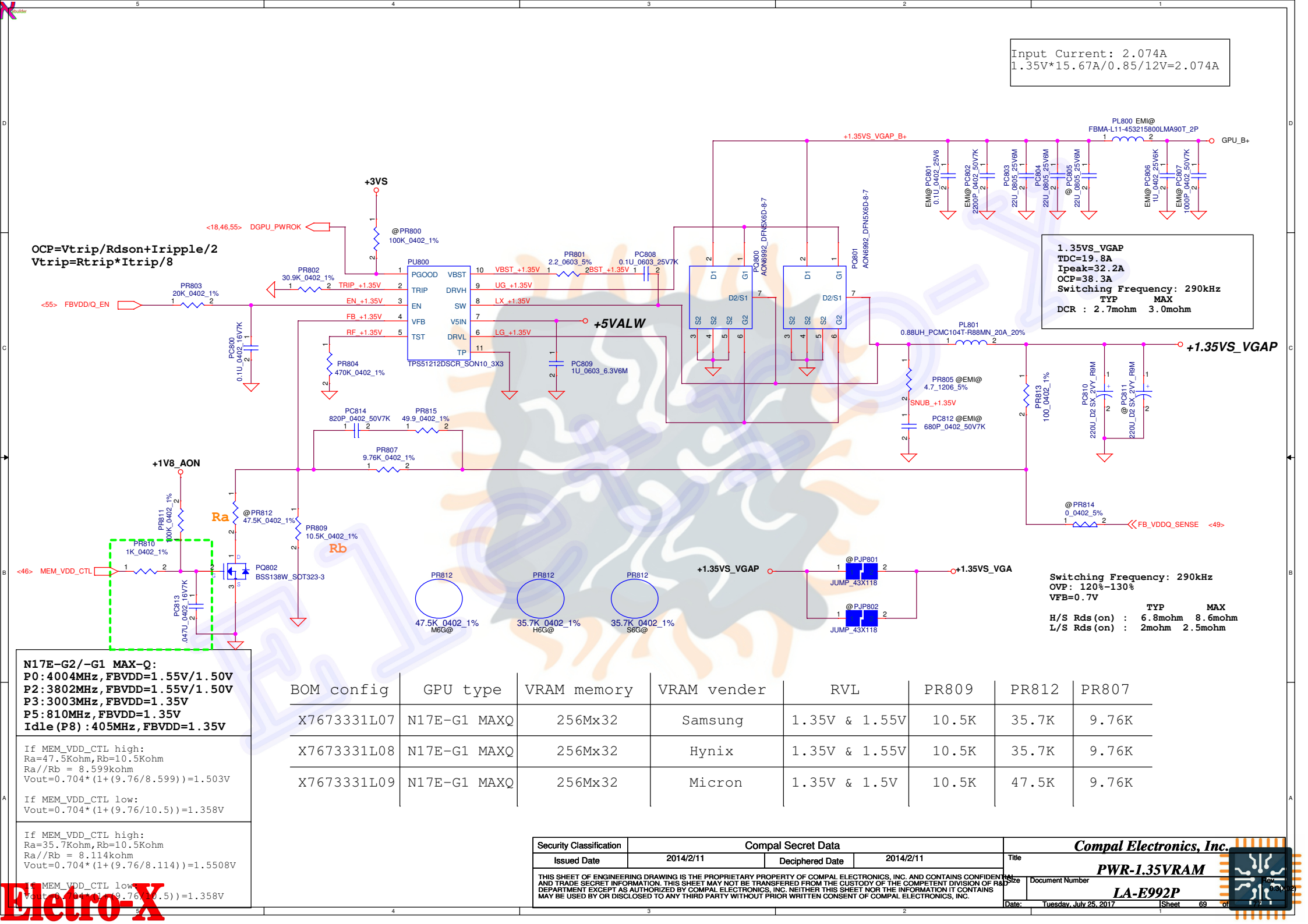
Title	PWR_VGA_UP9511P		
Size	Document Number	LA-E992P	Rev 0.1(Nv2)
Date: Tuesday, July 25, 2017	Sheet 67	of 77	



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title	PWR_+NVVDD1		
Size	Document Number	LA-E992P	Rev 0.1(0.2)
Date: Tuesday, July 25, 2017	Sheet 68	of 77	



BOM config	GPU type	VRAM memory	VRAM vender	RVL	PR809	PR812	PR807
X7673331L07	N17E-G1 MAXQ	256Mx32	Samsung	1.35V & 1.55V	10.5K	35.7K	9.76K
X7673331L08	N17E-G1 MAXQ	256Mx32	Hynix	1.35V & 1.55V	10.5K	35.7K	9.76K
X7673331L09	N17E-G1 MAXQ	256Mx32	Micron	1.35V & 1.5V	10.5K	47.5K	9.76K

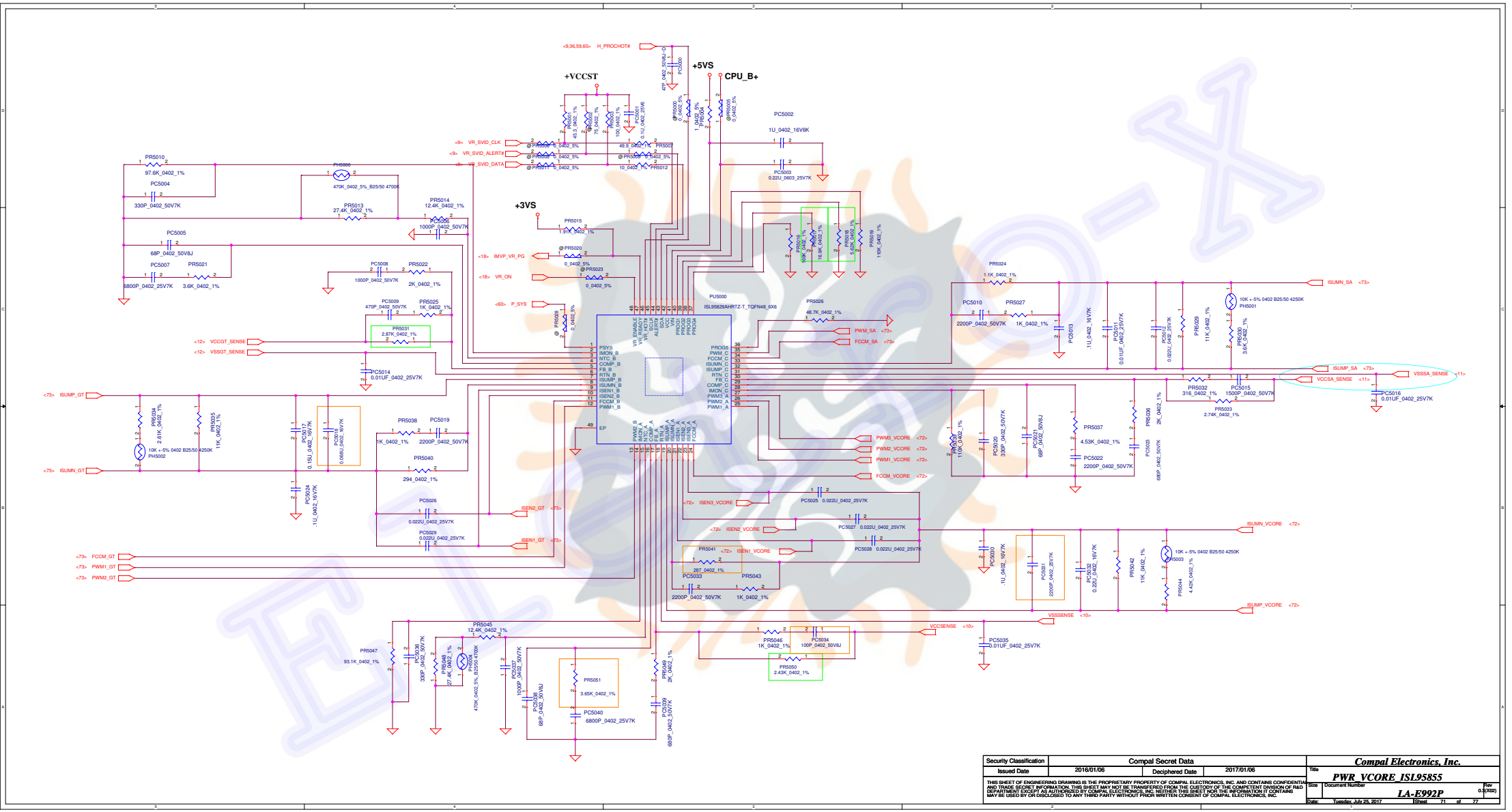
Security Classification	Compal Secret Data		
Issued Date	2014/2/11	Deciphered Date	2014/2/11

Compal Electronics, Inc.

Title: PWR-1.35VRAM

Size | Document Number: LA-E992P | Rev: 3.0(x2)

Date: Tuesday, July 25, 2017 | Sheet 69 of 77



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

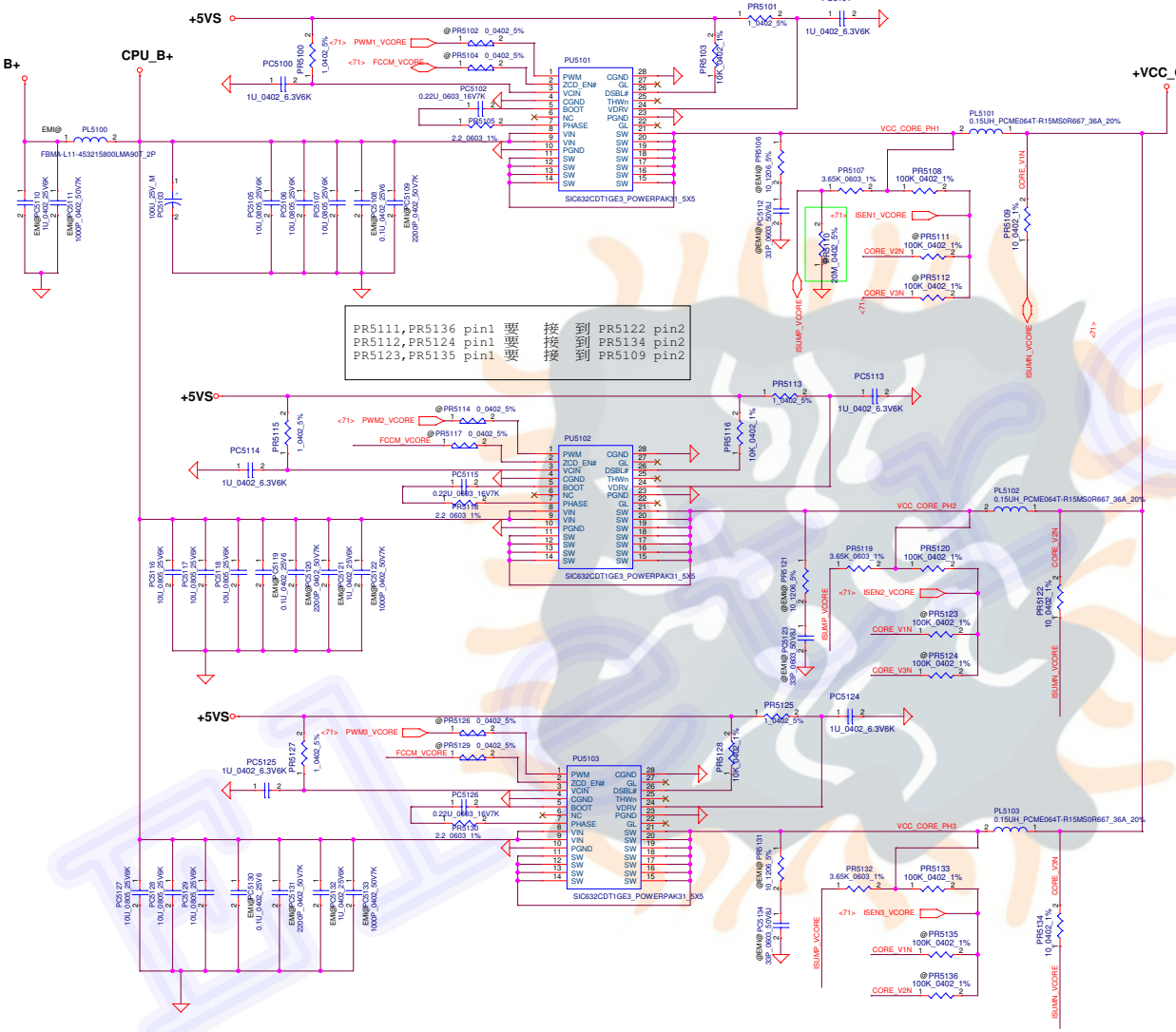
Compal Electronics, Inc.	
Title	PWR_VCORE_ISL95855
Size	Document Number: LA-E992P
Rev	0.3(X02)
Date: Tuesday, July 25, 2017	Sheet 71 of 77

Input Current: 7A
1.5V*47.6A/0.85/12V=7

+VCC_CORE
TDC PL2 :50A
Peak Current 70A
OCP Current 82A
DCR 0.66mohm +/-7%
Load Line 1.8mV/A

TDC PL2 refer to EDS REV1.5

PR5111,PR5136 pin1 要 接 到 PR5122 pin2
PR5112,PR5124 pin1 要 接 到 PR5134 pin2
PR5123,PR5135 pin1 要 接 到 PR5109 pin2



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			Size: Document Number: LA-E992P Rev: 0.1(X02)
			Date: Tuesday, July 25, 2017 Sheet 72 of 77

Input Current: 5.66A
1.5V*38.5A/0.85/12V=5.66

+VCC_GT
TDC PL2 :25A
Peak Current 55A
OCP Current 66A
DCR 0.66mohm +/-7%
Load Line 2.65mV/A

+5VS
CPU_B+
+VCCGT
PU5201
SIC632CDT1GE3_POWERPAK31_5X5
PR5211 pin1 要 接 到 PR5221 pin2
PR5222 pin1 要 接 到 PR5209 pin2

+VCC_SA
TDC PL2 :10A
Peak Current 11.1A
OCP Current 13.32A
DCR 6.2mohm +/-5%
Load Line 9.1mV/A

+5VS
PU5202
SIC632CDT1GE3_POWERPAK31_5X5

Input Current: 0.8A
1.05V*7.77A/0.85/12V=0.8

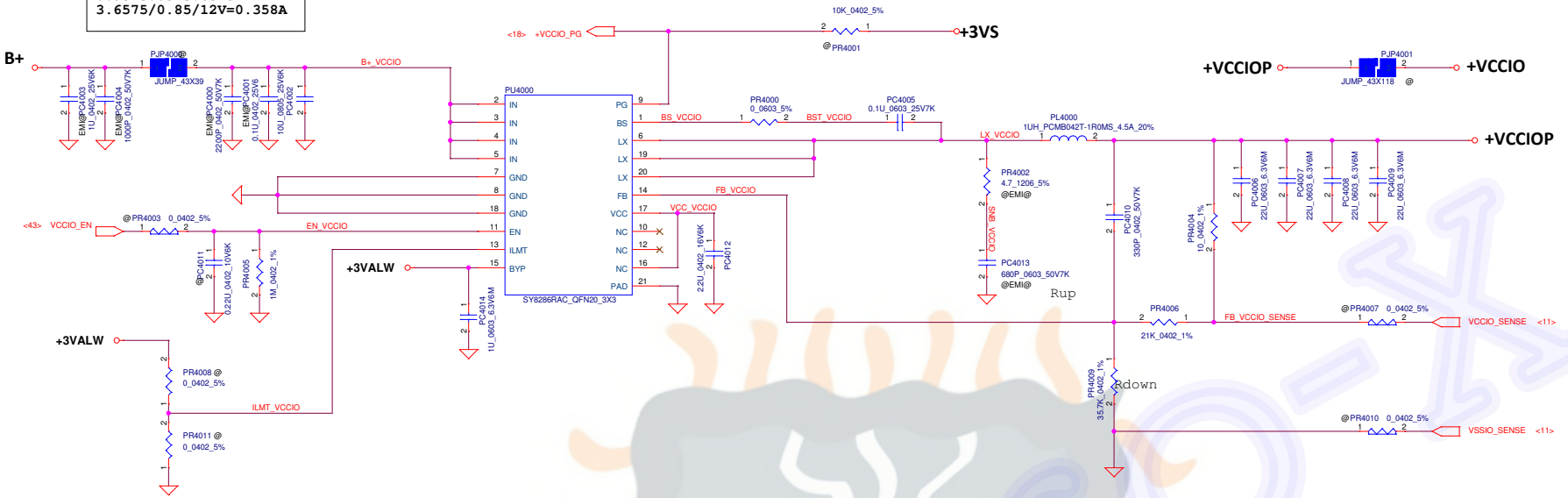
CPU_B+
+VCCSA
PU5203
SIC531CDT1GE3_POWERPAK22_4X3
+5VS

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.
Title: PWR_VCORE_+VCCGT,+VCCSA
Size: Document Number: LA-E992P
Rev: 1.0X02
Date: Tuesday, July 25, 2017 Sheet 73 of 77

Input Current:0.358A

0.95*3.85=3.6575W
3.6575/0.85/12V=0.358A

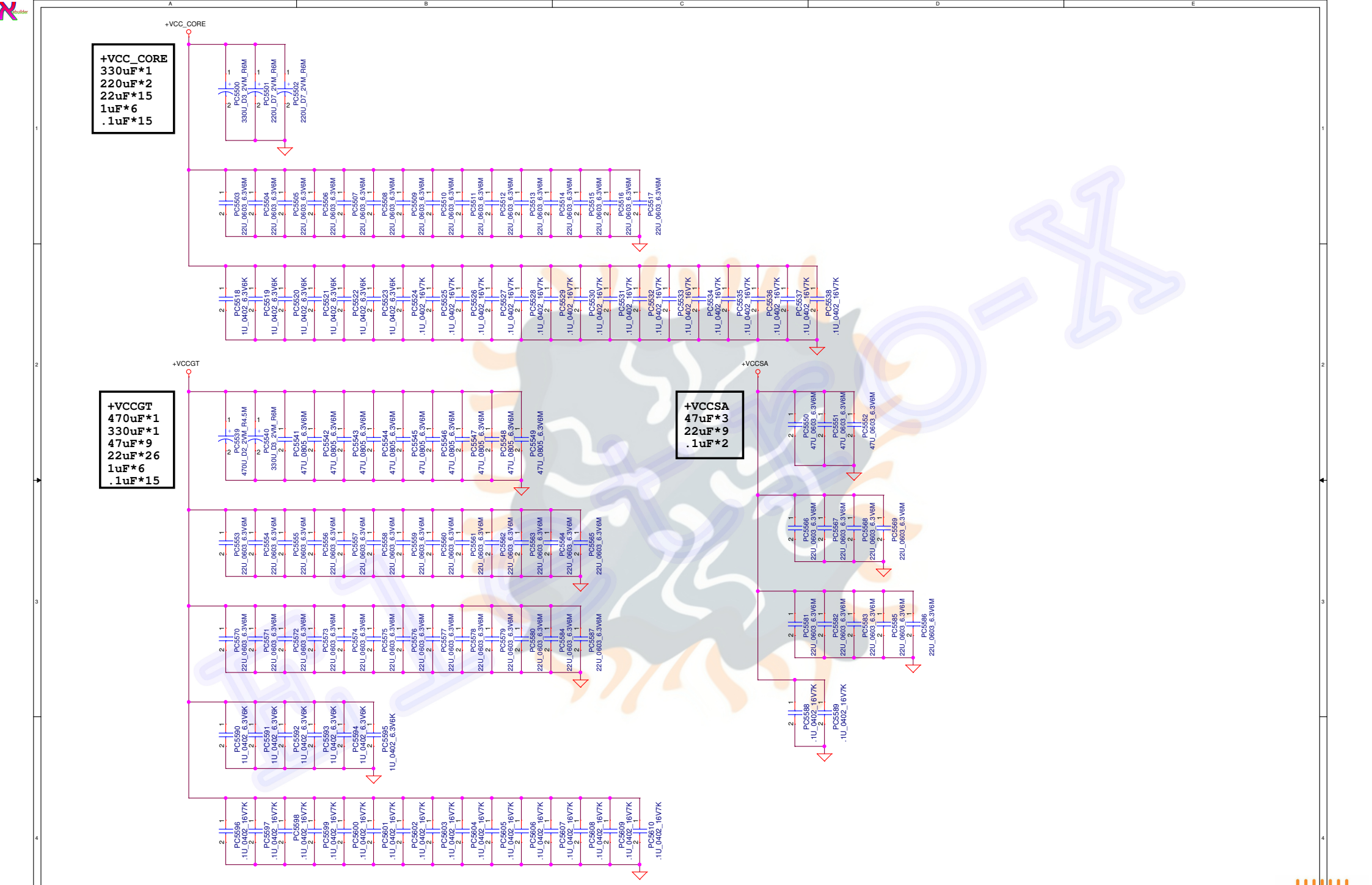


The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high.

+VCCIOP (0.95V)
TDC 3.85 A
Peak Current 5.5 A
OCP Current 9 A Fix by IC
FSW:500KHz

	TYP	MAX
DCR	24.0mohm	27.0mohm

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/01/06	Deciphered Date 2017/01/06	Title: PWR_+VCCIO
			Size: Document Number: LA-E992P Rev: 1.0
			Date: Tuesday, July 25, 2017 Sheet 74 of 77



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Issued Date	2016/01/06	Deciphered Date	2017/01/06

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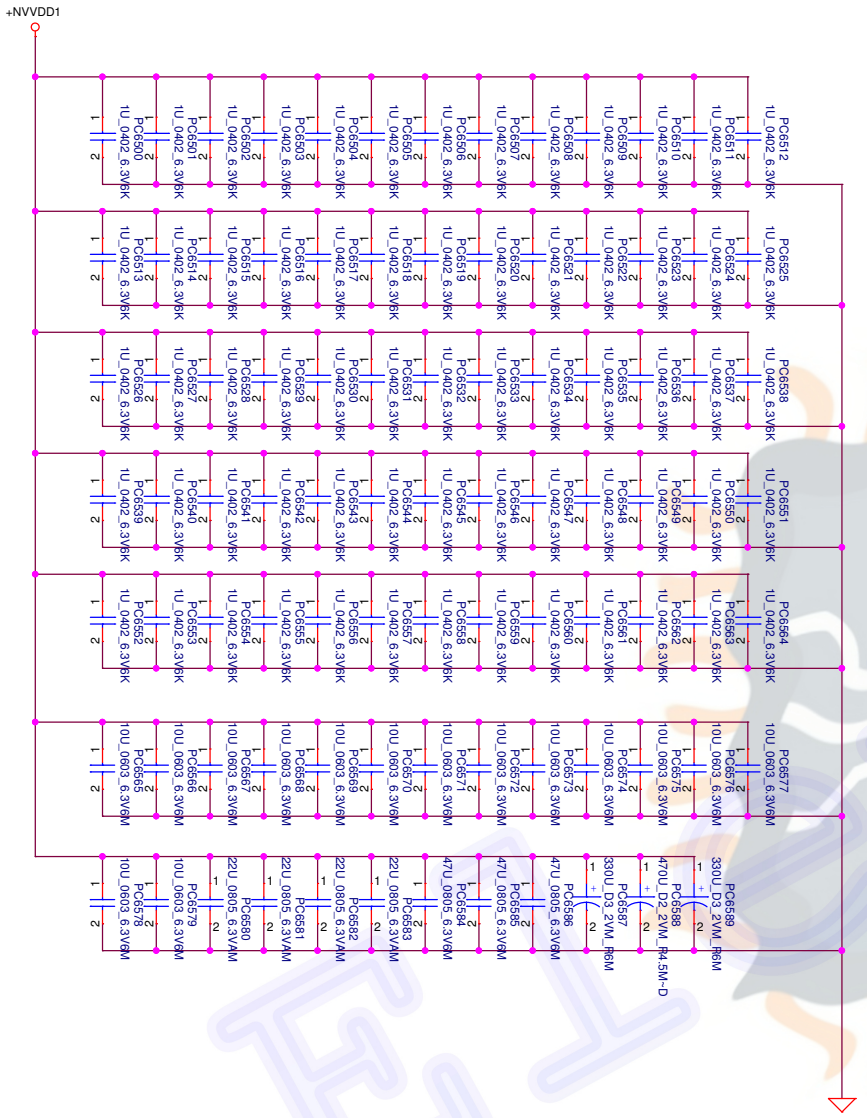
Compal Electronics, Inc.

Title: PWR_CPU DECOUPLING

Size: B | Document Number: LA-E992P | Rev: 1.0 (X04)

Date: Tuesday, July 25, 2017 | Sheet 75 of 77



+NVVDD
470uF X 1
330uF X 2
47uF_0805 X 3
22uF_0805 X 4
10uF_0603X 15
1uF_0402 X 65

Security Classification	Compal Secret Data		
Issued Date	2015/09/18	Deciphered Date	2016/09/18

Compal Electronics, Inc.

Title: **VGA DECOUPLING**

Size | Document Number: **LA-E992P**

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Version Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	60	CHARGER	2017/01/09	Compal_PWR	Modify ILMT.	1. Change PR714 from 20K(@) Ohm to 20K Ohm. 2. Change PR715 from 1.17K(@) Ohm to 5.76K Ohm	0.1
2	69	+1.35VRAM	2017/01/09	Compal_PWR	For BOM control	1. Add PR812 of 35.7k Ohm for S6G@ 2. Add PR812 of 35.7k Ohm for H6G@ 3. Add PR812 of 47.5k Ohm for M6G@	0.1
3	65	+1.8VGSP	2017/01/09	Compal_PWR	For EE request to add capacitor for avoiding noise	1. Change PC18V09 form 0.1u(@)F to 0.1uF.	0.1
4	61,64	+3/+5VALWP & +1VALWP	2017/02/13	Compal_PWR	Avoid to use Samsung Capcitor in common part, change to independent P/N.	1. Change PC103,PC104,PC301,PC302,PC307,PC308 from SE00000QK00 to SE00000QK0L	0.1
5	67	VGA_UP9511	2017/02/17	Compal_PWR	Avoid 5VCC leakage issue, so we amplify the divider resistance	1. Change PR6000 form 10K Ohm to 100K Ohm 2. Change PR6006 from 91K Ohm to 910K Ohm	0.1
6	59	DCIN / BATT CONN /OTP	2017/02/22	Compal_PWR	Follow EE's request,use the same part with EE.	1. Change PQ6 from SB00000DH00 to SB00000ZU00 2. Change PQ7 from SB00000I700 to SB00000ZU00	0.1
7	59,60	DCIN / BATT CONN /OTP & Charger	2017/03/02	Compal_PWR	Follow Dell &EC request,change I_ADP 's net name.	1. Change net name from I_ADP to I_ADP_R	0.1
8	60	Charger	2017/03/03	Compal_PWR	Before EC program,AC_DIS is floating. Avoid the siganal forcing PQ708 open quickly, add pull down resistor on AC_DIS siganal.	1. add PR734 100K Ohm on siganal AC_DIS	0.1
9	66	+1.0VS_VGA	2017/03/03	Compal_PWR	Follow EE's request,change enable siganl.	1. Change net name from NVVDD1_EN to PEX_VDD_EN.	0.1
10	60	Charger	2017/03/06	Compal_PWR	Follow sourcer request,change PD part.	1. Change PD700 from SCS00005400 to SCS00003800.	0.1
11	69	+1.35VRAM	2017/03/07	Compal_PWR	The VRAM voltage will switch between 1.5V and 1.35V, there will be a overshoot voltage.To solve this issue, we add 1K ohm and 47nF.	1. Change PR810 from 0 ohm to 1K ohm 2. add 47nF PC813 from PQ802 gate to source.	0.1
12	65	+1.8VGSP	2017/03/14	Compal_PWR	Follow EE's request,modify output voltage to solve 1.8VS drop test.	1. Change PR18V02 from 20K ohm to 20.5K ohm	0.1
13	61	+3/+5VALWP	2017/03/14	Compal_PWR	Follow EE's request,modify output voltage to solve TypeC VBUS drop test.	1. Change PR301 from 15K ohm to 15.4K ohm	0.1
14	69	+1.35VRAM	2017/03/14	Compal_PWR	The VRAM voltage will switch between 1.5V and 1.35V, there will be a overshoot voltage.To solve this issue, we add 49.9 ohm and 1.5nF.	1. add PC814 and PR815 parallel with PR807.	0.1
15	69	+1.35VRAM	2017/03/14	Compal_PWR	Avoid the mos PQ802 won't open,so we change the lower Vth 's Mos (Vth=1.5V)	1.Change PQ802 from SB00000ST00 to SB00000T000.	0.1
16	59	DCIN / BATT CONN /OTP	2017/03/16	Compal_PWR	Dell request us to change PD1 's position.	1.Change PD1's Pin2 from PSID-0 to PSID.	0.1
17	71	VCORE-ISL95829	2017/03/20	Compal_PWR	After CPU VRTT Test,we tune some resistor&capcitor.	1. Change PR5041 from 267 ohm to 287 ohm. 2. Change PC5031 from 4700 pF to 2200 pF. 3. Change PR5051 from 4.87K ohm to 3.65K ohm. 4. Change PC5034 from 470 pF to 100 pF. 5. Change PC5018 from 33 nF to 68 pF.	0.1
18	69	+1.35VRAM	2017/03/23	Compal_PWR	Because FBVDDQ transient noise issue,so we follow EE's request,remove 220uF*1 output cap.	1. Change PC811 220uF to 220uF(@)	0.1

Compal Electronics, Inc.

Title: NOTE

Size | Document Number: LA-E992P | Rev: 0.3

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Version Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	73	VCORE_+VCCGT_+VCCSA	2017/05/05	Compal_PWR	Because VCCSA's Choke DCR value would impact VRTT test result, so we choose SH000015M00 and SH000015P00 with same DCR value as main and 2nd source.	1. Change PL5203 from SH00000T500 to SH000015M00.	0.2
2	61	+3VALWP	2017/05/08	Compal_PWR	Modify +3VALWP OCP resistor.	1. Change PR304 from 8.87K ohm to 6.19K ohm.	0.2
3	69	+1.35VRAM	2017/05/08	Compal_PWR	Modify +1.35VRAM OCP resistor.	1. Change PR802 from 30.9K ohm to 42.2K ohm.	0.2
4	71	VCORE_ISL95829	2017/05/08	Compal_PWR	Modify VCCSA IMON resistor.	1. Change PR5024 from 1.27K ohm to 1.1K ohm.	0.2
5	59	DCIN	2017/05/08	Compal_PWR	Because DC-IN Cable is hard to plug and pull,we change dc-in beed from 2 pcs to 3 pcs.	1. Change PL1/PL2 from SM010008E10 to SM01000C000. 2. Add PL6=SM01000C000.	0.2
6	59	DCIN	2017/05/10	Compal_PWR	Adjust the battery unplug prochot delay time.	1. Change PC12 from 1uF to 0.1uF.	0.2
7	59	DCIN / BATT CONN / OTP	2017/05/11	Compal_PWR	Add another circuit to pull down the GPU power level.	1. Add PC16 0.1uF 2. Add PQ9=SB00000ST00. 3. Add PR34 0 ohm. 4. Add PR35 100Kohm.	0.2
8	59~74	All page	2017/06/22	Compal_PWR	For schematic cost down	1.Change PR721,PR706,PR723,PR730,PR733,PR6069,PR315,PR6051, PR6070,PR6035,PR5028,PR814,PR5011,PR6021,PR6018,PR101,PR103, PR5129,PR5213,PR705,PR732,PR5117,PR6026,PR5006,PR5102,PR731, PR5023,PR6060,PR727,PR6041,PR6045,PR5202,PR5215,PR4007,PR5020, PR5114,PR4003,PR5000,PR5005,PR5008,PR5224,PR5204,PR312,PR4010, PR5223,PR5009,PR5104,PR10V4,PR24,PR18V00,PR209,PR311,PR25,PR5126, PR211,PR25V00,PR18V07,PR6053,PR34 from 0 ohm to shortpad.	1.0
9	69	+1.35VRAM	2017/06/22	Compal_PWR	The VRAM voltage will switch between 1.5V and 1.35V, there will be a overshoot voltage.To solve this issue, we add 49.9 ohm and 820pF.	1. add PC814 and PR815 parallel with PR807.	1.0
10	69	+1.35VRAM	2017/07/11	Compal_PWR	Modify OCP resistor.	1.Change from 42.2Kohm to 30.9Kohm.	1.0
11	61	+5VALWP	2017/07/11	Compal_PWR	Modify OCP resistor.	1.Change from 16.5Kohm to 10.5Kohm.	1.0
12				Compal_PWR			
13				Compal_PWR			
14				Compal_PWR			
15				Compal_PWR			
16				Compal_PWR			
17				Compal_PWR			

Compal Electronics, Inc.

Title: NOTE

Size | Document Number: LA-E992P

Rev: 0.2

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