LCFC Confidential

Y540 M/B Schematics Document

Coffee Lake H-Processor with DDR4 + NV N18E-G1 GPU

2019-03-22

REV:2.0

Security Classification	LC Future Center Secret Data		
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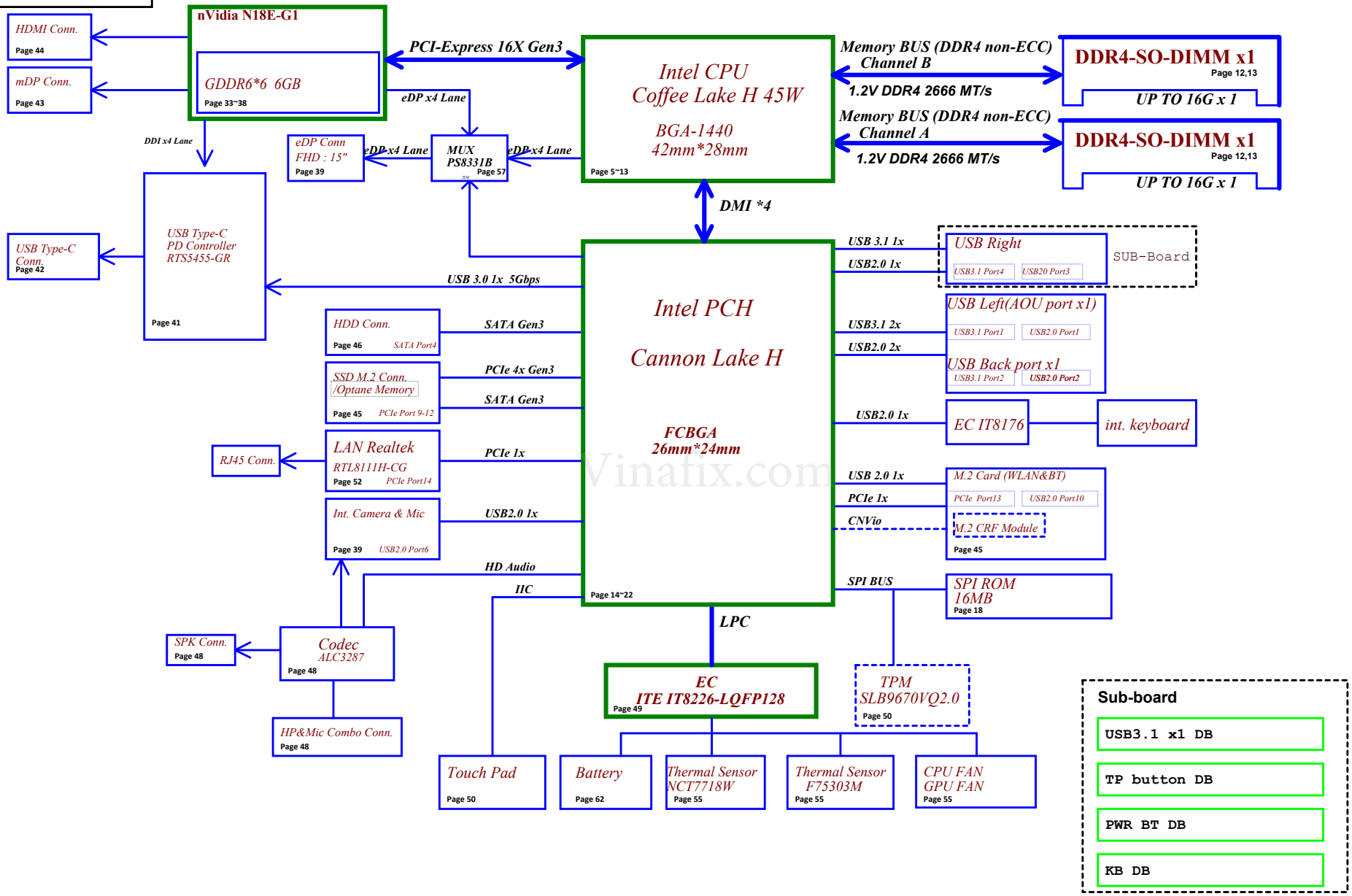
LCFC confidential

File Name:FY515
Board Number:NM-C221
PN:DAZ1DG00101



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Title: Block Diagram

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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW +5VALW	+3VALW_PCH	+1.2V	+5VS +3VS VCCIO VCCSA VCCSTG VCCCPUCORE VCCGFXCORE +1.8VS_AON +1.8VGS NVVDD +1.0VGS FBVDDQ
S0	O	O	O	O	O
S3	O	O	O	O	X
S3 Battery only	O	O	O	O	X
S5 S4/AC Only	O	O	O	X	X
S5 S4 Battery only	O	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE / SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOM Structure Control Table

BOM Structure	BTO Item
@	Not stuff
15@	15'' Stuff
17@	17'' stuff
7000P@	7000P stuff
7502M@	7502 stuff
8111GUL@	LAN Chip 8111GUL part
8111H@	LAN Chip 8111H part
AG@	Anti-ghost
AOAC@	AOAC support part
BL@	BL
CD@	Cost down part
CNVI@	CNVi support part
DCI@	DCI
Debug@	USB2.0 port 1for Debug
EMC@	EMC part
EMC_8111H@	LAN 8111H EMC Part
EMC_NS@	EMC not stuff
GC6@	GC6
GYSNC@	GSYNC support part
HDMI@	HDMI
i5@i7@i9@	CPU Part
ME@	ME part(connector, hole)
M6GX6@S6GX6@	VRAM part

BOM Structure	BTO Item
MIRROR@	MIRROR
N18EG0@N18EG1@	GPU part
NOMIRROR@	17'' stuff
NPI@	SPI VCC diode stuff
OPT@	For NV GPU part
OPTANE@	Optane memory support part
RT8816_NS@	RT8816 not stuff
TPM@	For support TPM sku part
UP1666_@	UP1666 stuff
UP1666_NS@	UP1666 not stuff
UP9632_@	UP9632 part stuff
USB@	USB2.0 port1 for USB Port
X76@	VRAM

USB2.0 Port table	
Port	Function
1	Back USB3.0
2	Left USB3.0
3	Right USB3.0
4	Type-C Port
5	NA
6	Camera
7:8	NA
9	AG
10:13	NA
14	BT

USB3.0 Port table	
Port	Function
1	Back USB3.0
2	Type-C Port
3	Left USB3.0
4	Right USB3.0
5	NA
6	NA

SATA Port table	
Port	Function
0A	M.2 SSD Gen3
0B	NA
1A	NA
1B	NA
2	NA
3	NA
4	HDD Gen3
5	NA

PCIE Port table	
Port	Function
1:8	NA
9	M.2 SSD/Optane
10	M.2 SSD/Optane
11	M.2 SSD/Optane
12	M.2 SSD/Optane
13	WLAN Gen1
14	LAN Gen1
15:24	NA

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Title	Notes List		
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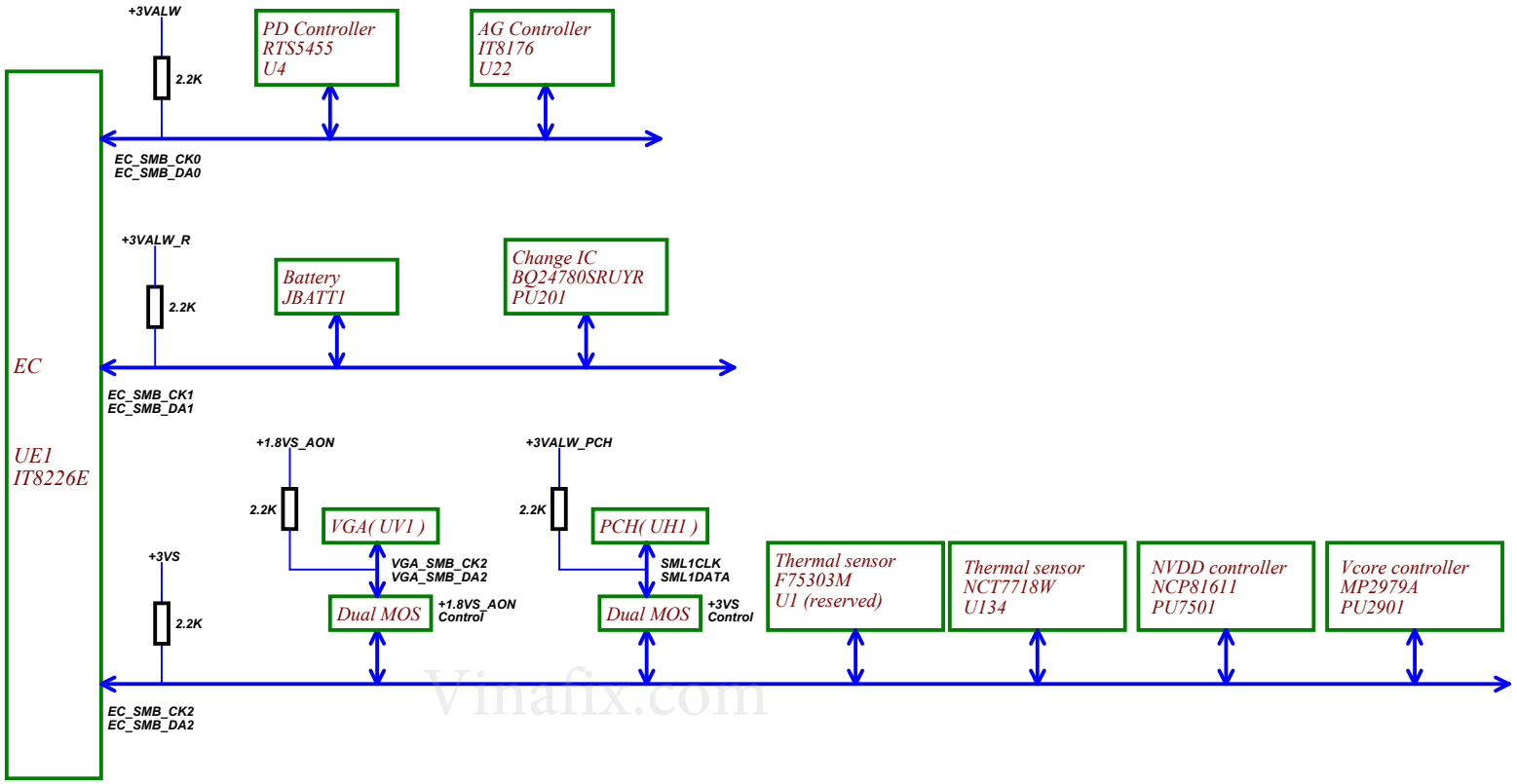

SMBUS Control Table

	SOURCE	VGA	BATT	IT8226E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module	Charger	RGB KB Backlight	USB-C PD	HiFi Audio	Anti-ghost
EC_SMB_CK0 EC_SMB_DA0	IT8226E +3VALW	X	X	X	X	X	X	X	X	X	X	V +5VS	X	V +3VALW_AG
EC_SMB_CK1 EC_SMB_DA1	IT8226E +3VALW_R	X	V +3VALW_R	V +3VALW_R	X	X	X	X	X	V +3VALW_R	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8226E +3VS	V +1.8VS_AON	X	V +3VS	X	X	V +3VS Reserve	V +3VALW_PCH	X	X	X	X	X	X
PCH_SMBCLK PCH_SMBDATA	PCH +3VALW_PCH	X	X	X	V +3VS	X	X	X	V +3VS	X	X	X	X	X
PCH_RGBKB_SCL PCH_RGBKB_SDA	X	X	X	X	X	X	X	X	X	X	V +LDO_3V3	X	X	X
EC_SMB_CK0 EC_SMB_DA0	IT8226E +3VALW	X	X	X	X	X	X	X	X	X	X	V +5VS	X	X

EC SM Bus1 address

Device	Address
Smart Battery	0X16
Charger	0001 0010 b

EC SM Bus2 address

Device	Address
Thermal Sensor F75303M	1001_100x b
VGA	0x9E (default)
PCH	Need to update
Thermal Sensor NCT7718W	1001100xb

PCH SM Bus address

Device	Address
DDR DIMMA	1010 000X b
DDR DIMMB	1010 010X b
TP Module	Need to update
Wlan	Reserved

PCH I2C 2 Bus address

Device	Address
RGB Backlight	Need to update

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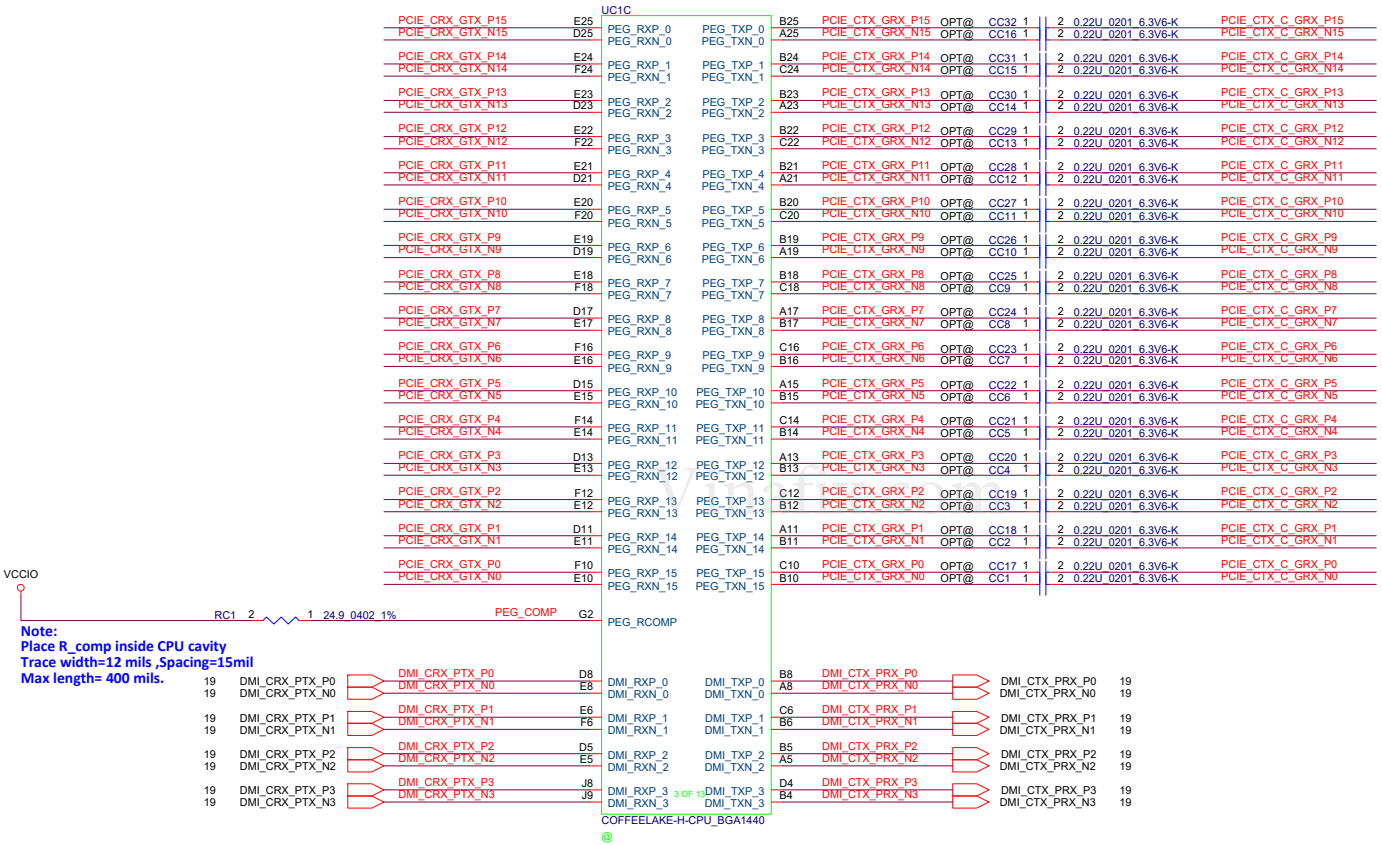
24 PCIE_CRX_GTX_N[0..15]

24 PCIE_CRX_GTX_P[0..15]

PCIE_CTX_C_GRX_N[0..15] 24

PCIE_CTX_C_GRX_P[0..15] 24



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Title: CPU (1/7) DMI,PEG

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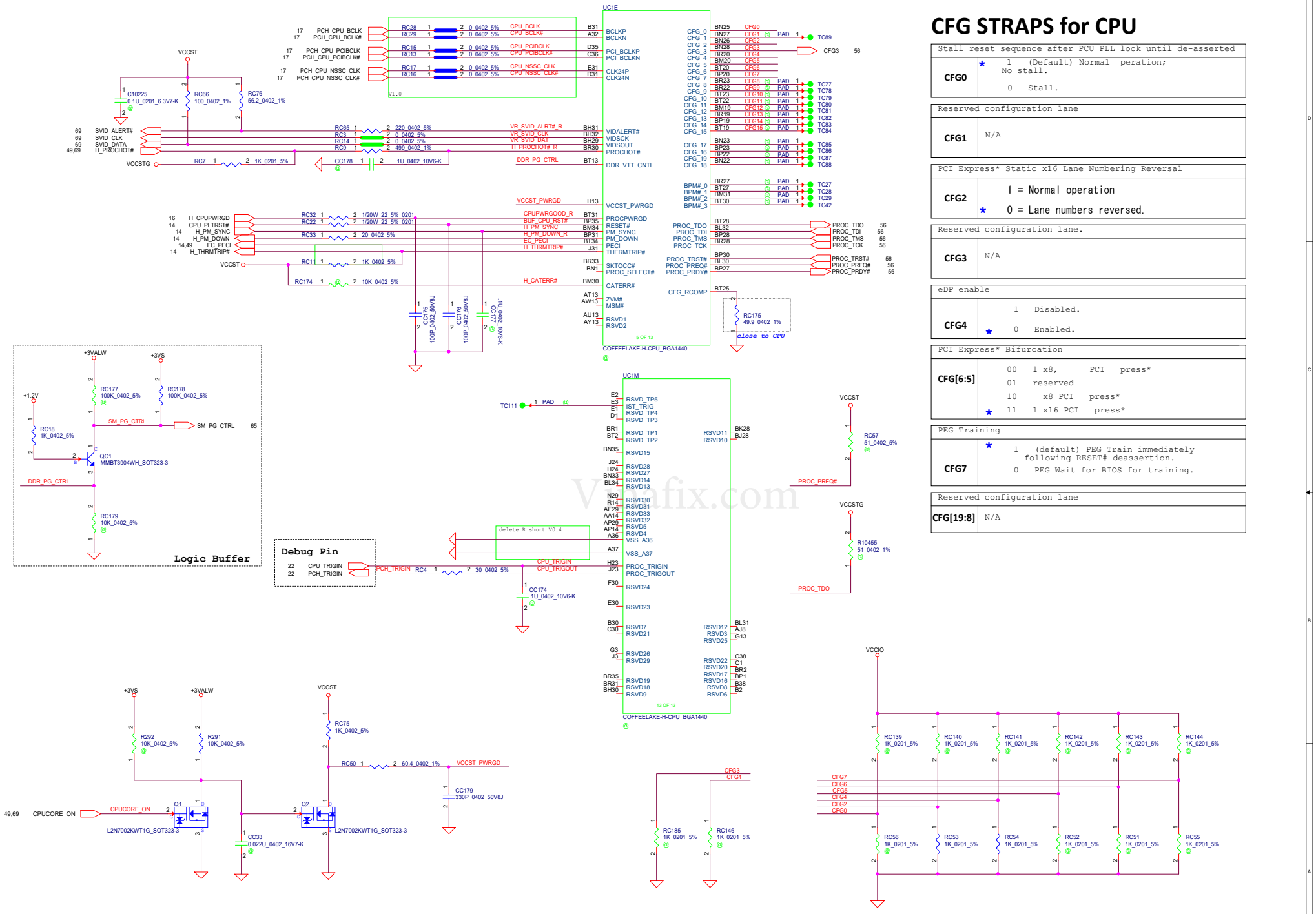

CFG STRAPS for CPU

Stall reset sequence after PCU PLL lock until de-asserted	
CFG0	* 1 (Default) Normal peration; No stall. 0 Stall.
Reserved configuration lane	
CFG1	N/A
PCI Express* Static x16 Lane Numbering Reversal	
CFG2	1 = Normal operation * 0 = Lane numbers reversed.
Reserved configuration lane.	
CFG3	N/A
eDP enable	
CFG4	1 Disabled. * 0 Enabled.
PCI Express* Bifurcation	
CFG[6:5]	00 1 x8, PCI press* 01 reserved 10 x8 PCI press* * 11 1 x16 PCI press*
PEG Training	
CFG7	* 1 (default) PEG Train immediately following RESET# deassertion. 0 PEG Wait for BIOS for training.
Reserved configuration lane	
CFG[19:8]	N/A

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Title	CPU (2/7) PM, XDP, CLK, CFG		
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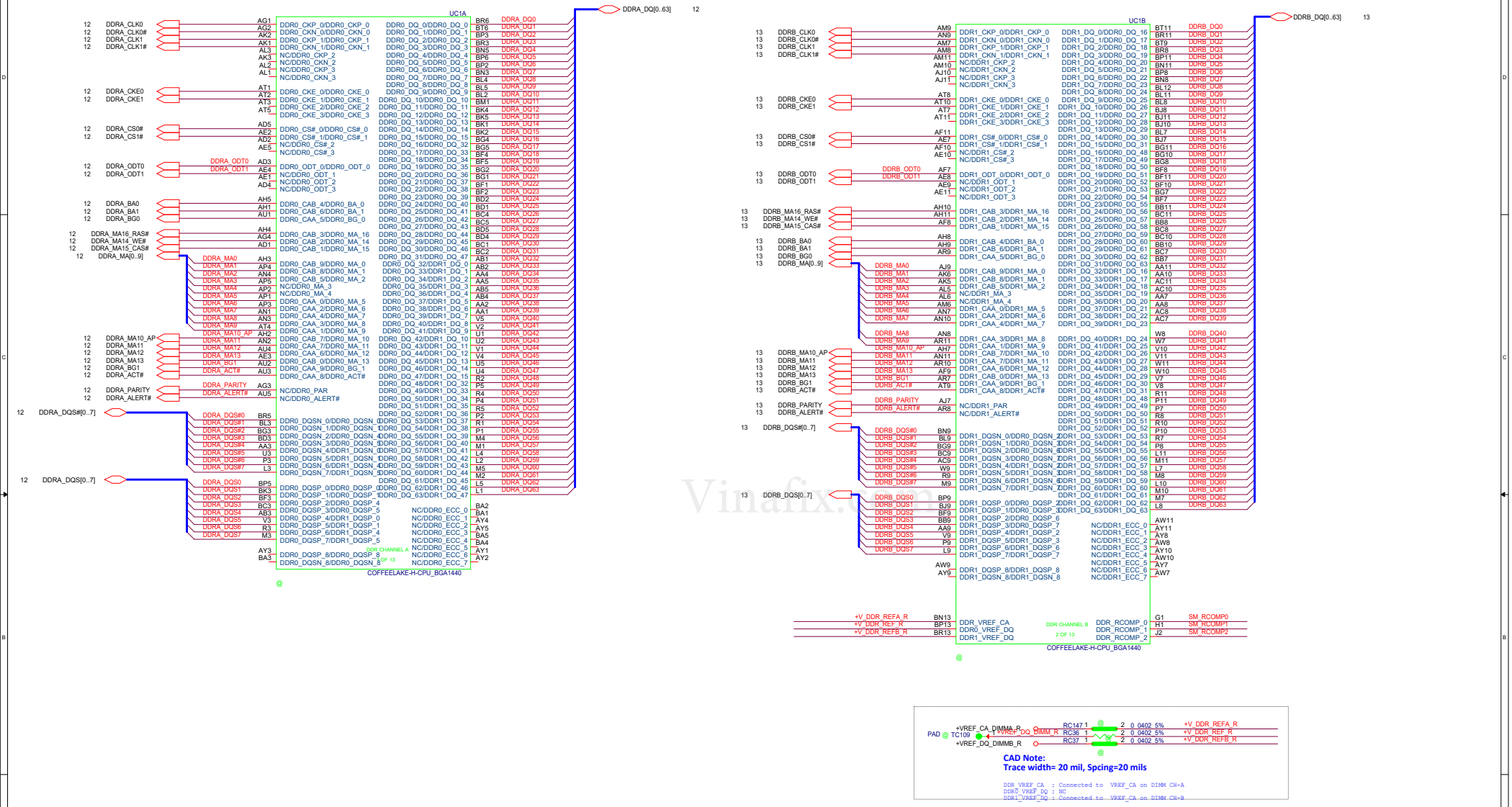

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Title: CPU (3/7) DDRVI

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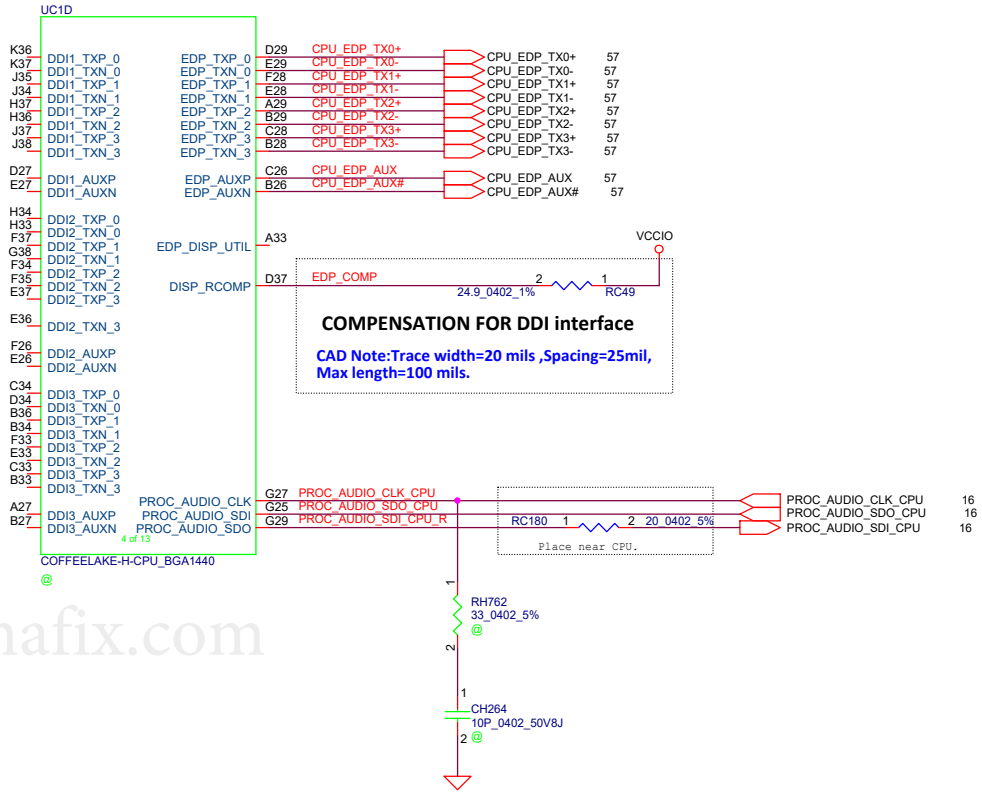

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **CPU (4/7) eDP, DDI**

Size	Document Number	Rev
A3	Y540	2.0

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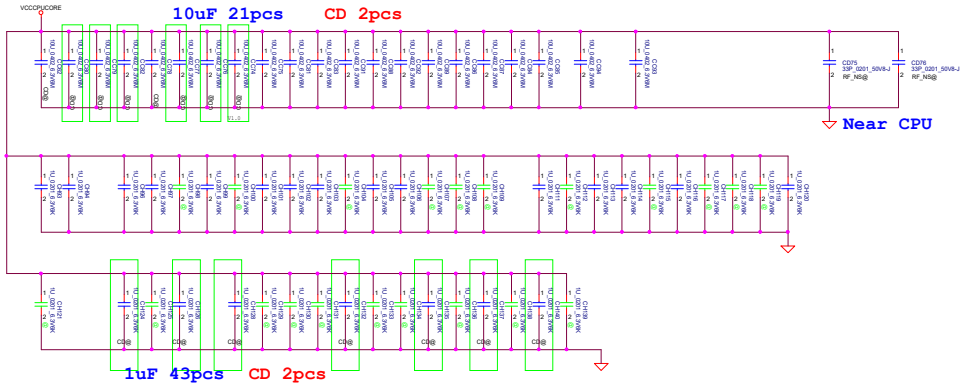

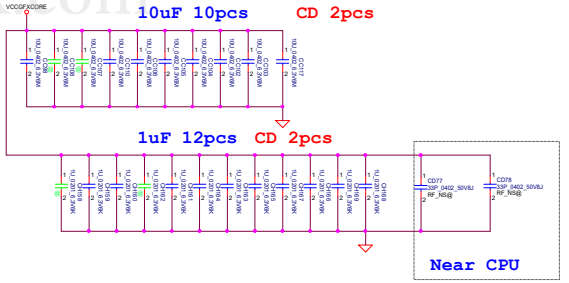

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Title: CPU (5/7) PWR, BYPASS

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D	Y540	2.0

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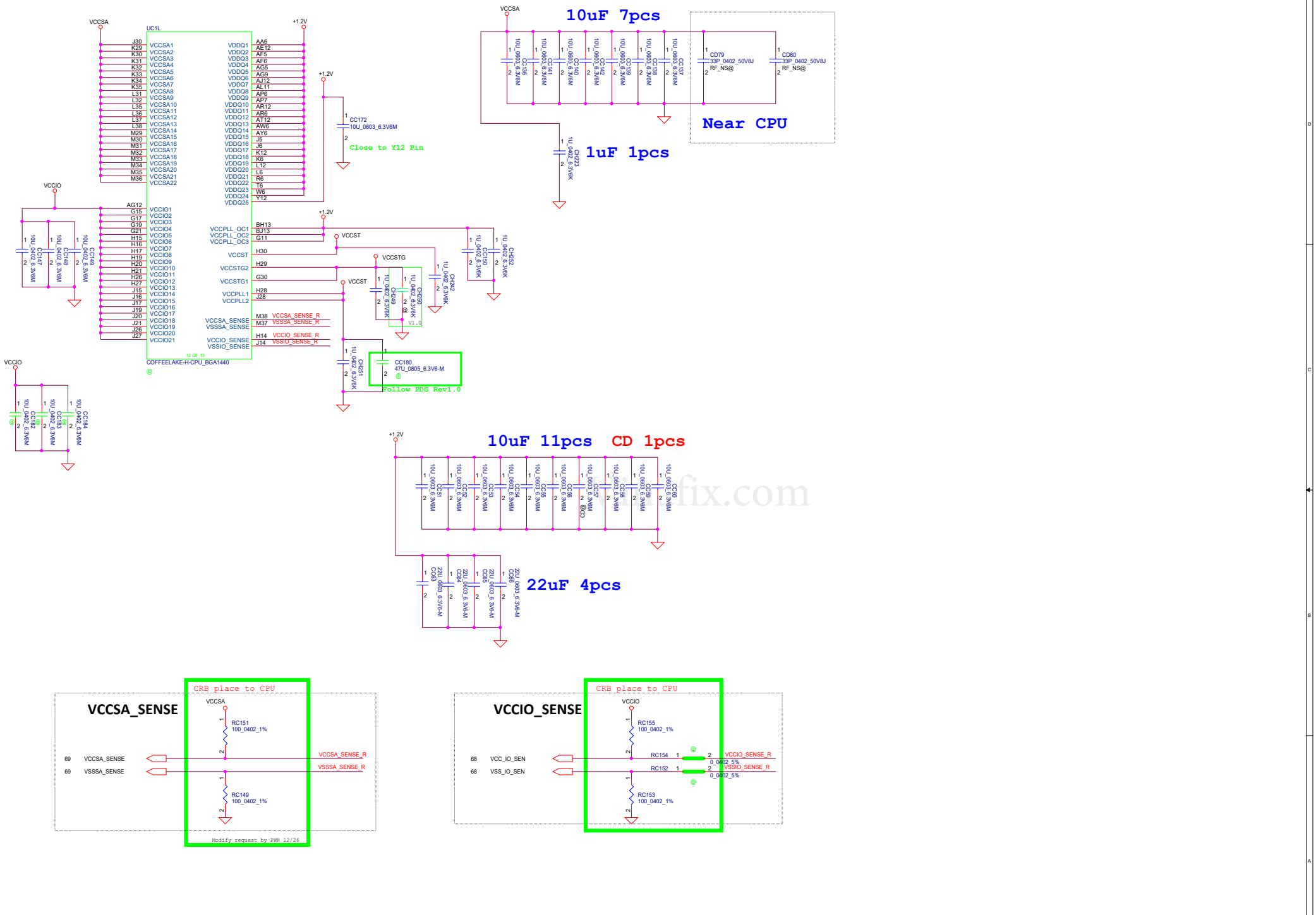

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Title: CPU (6/7) PWR, BYPASS

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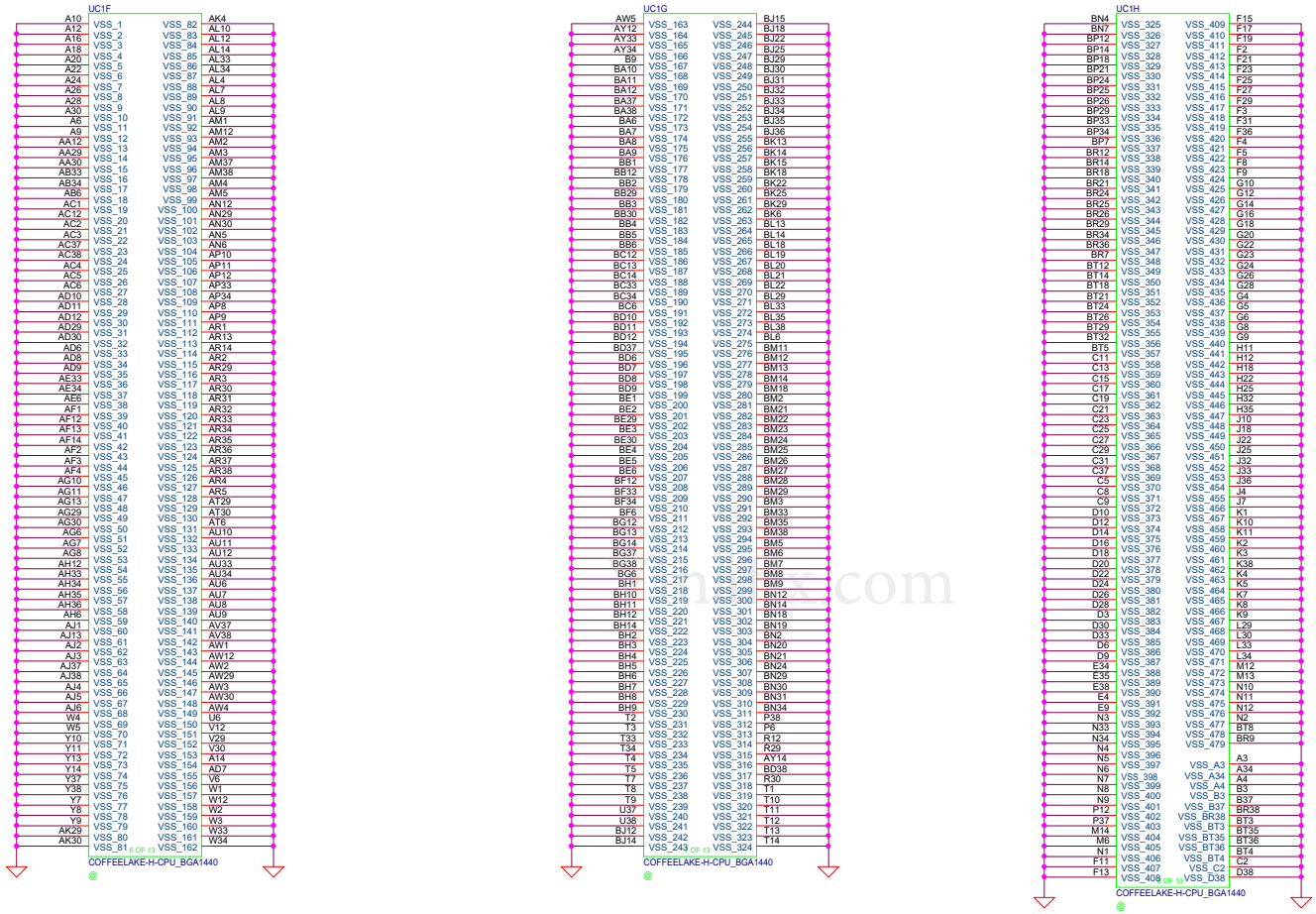

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Title: **CPU (6/7) PWR, VSS**

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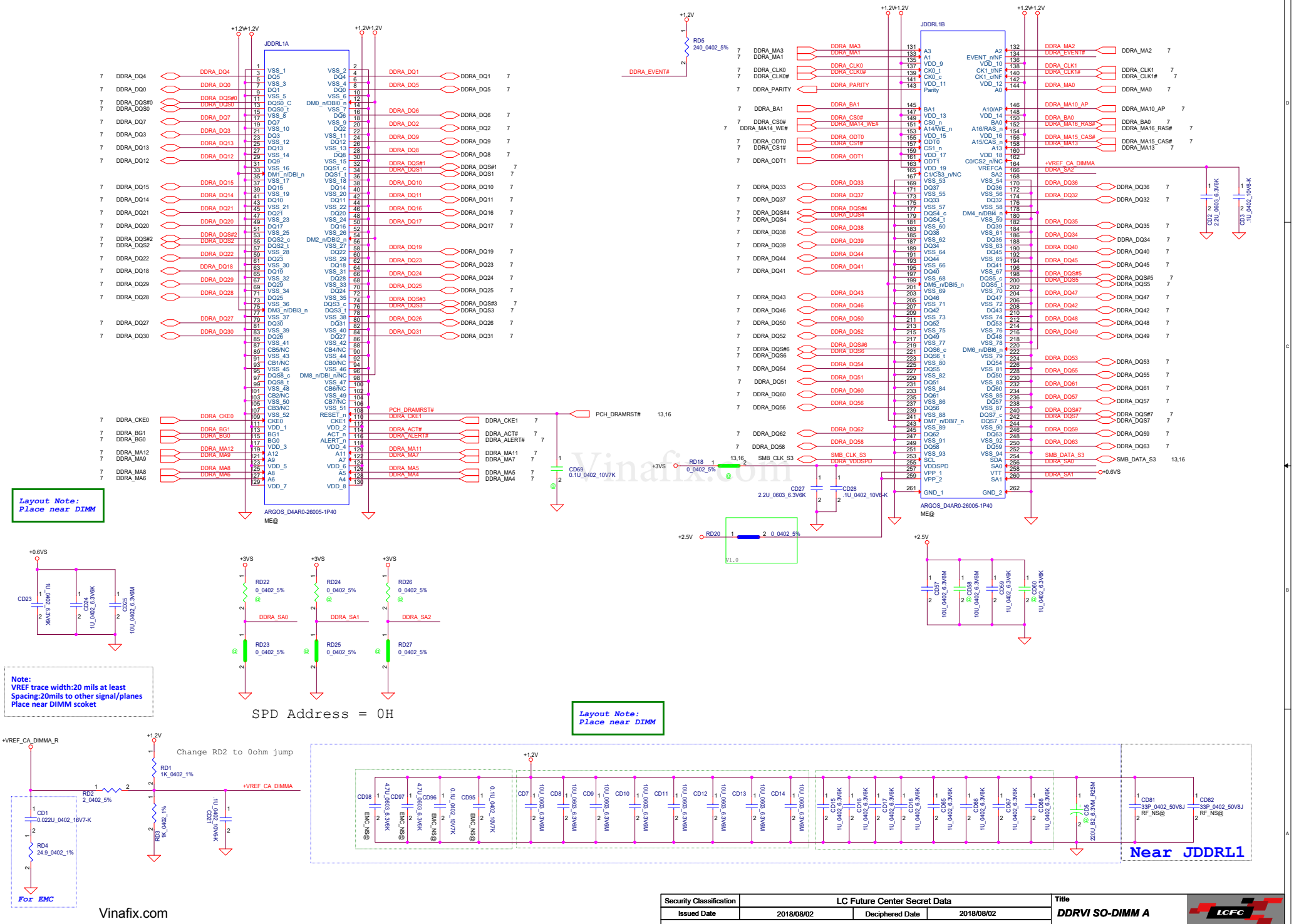
DDR4 SO-DIMM A



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Title: DDRVI SO-DIMM A

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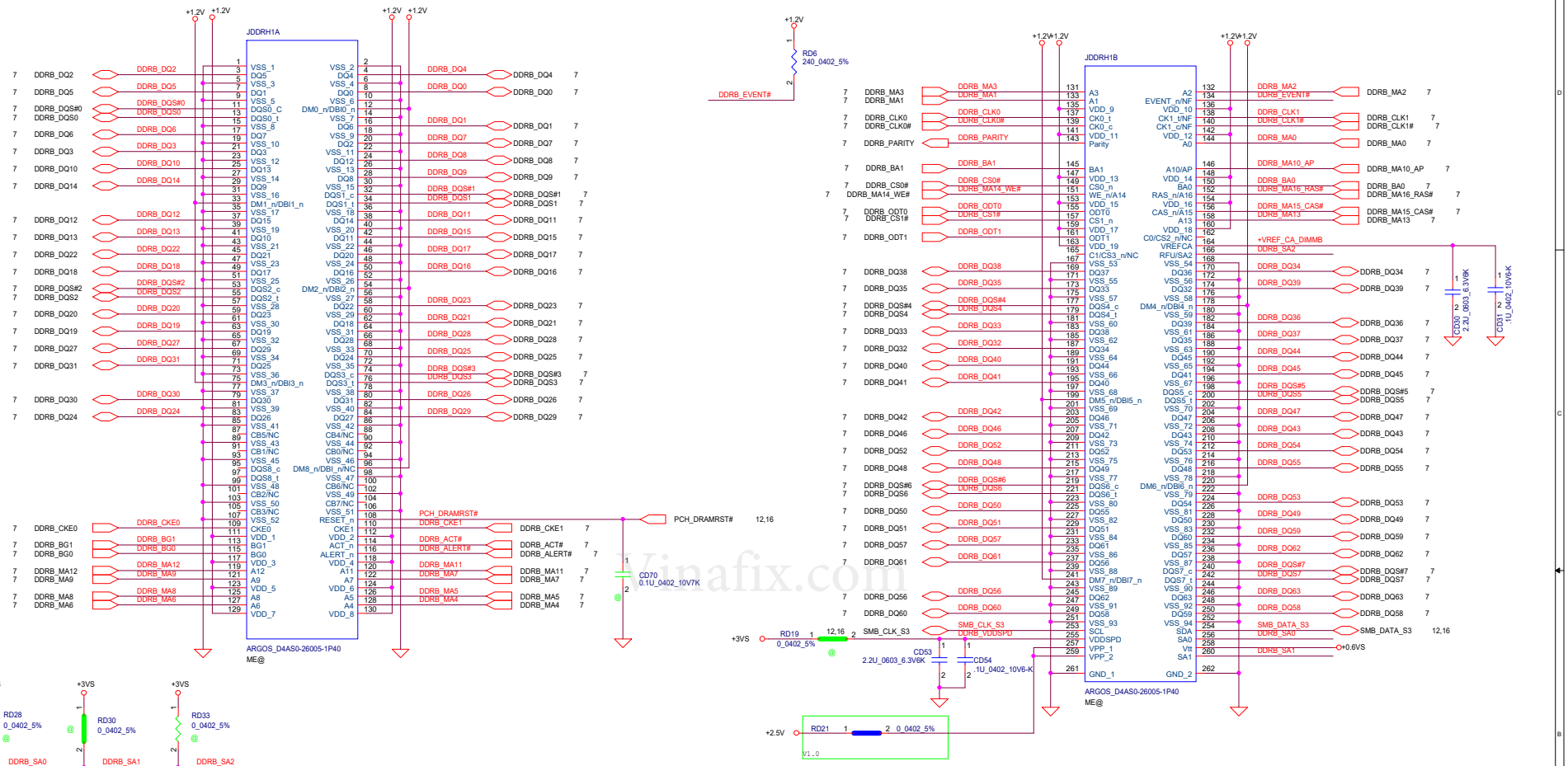
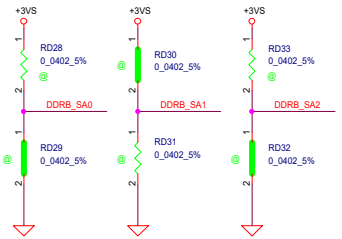
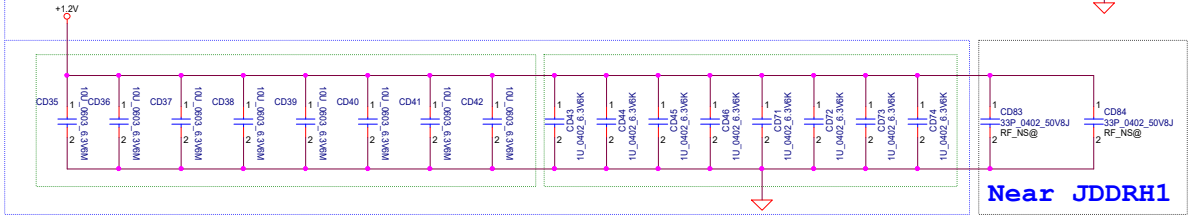
DDR4 SO-DIMM B



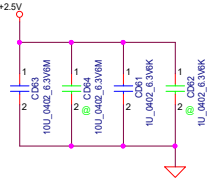


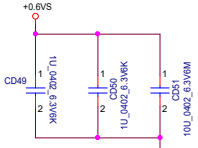
SPD Address = 2H

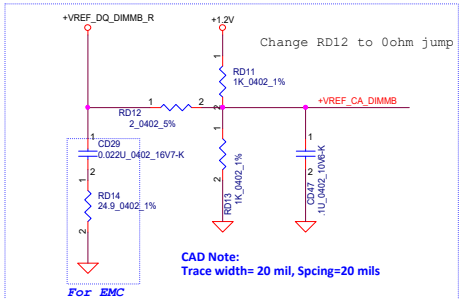
Layout Note:
Place near DIMM



Near JDDRH1







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Title	DDRVI SO-DIMM B		
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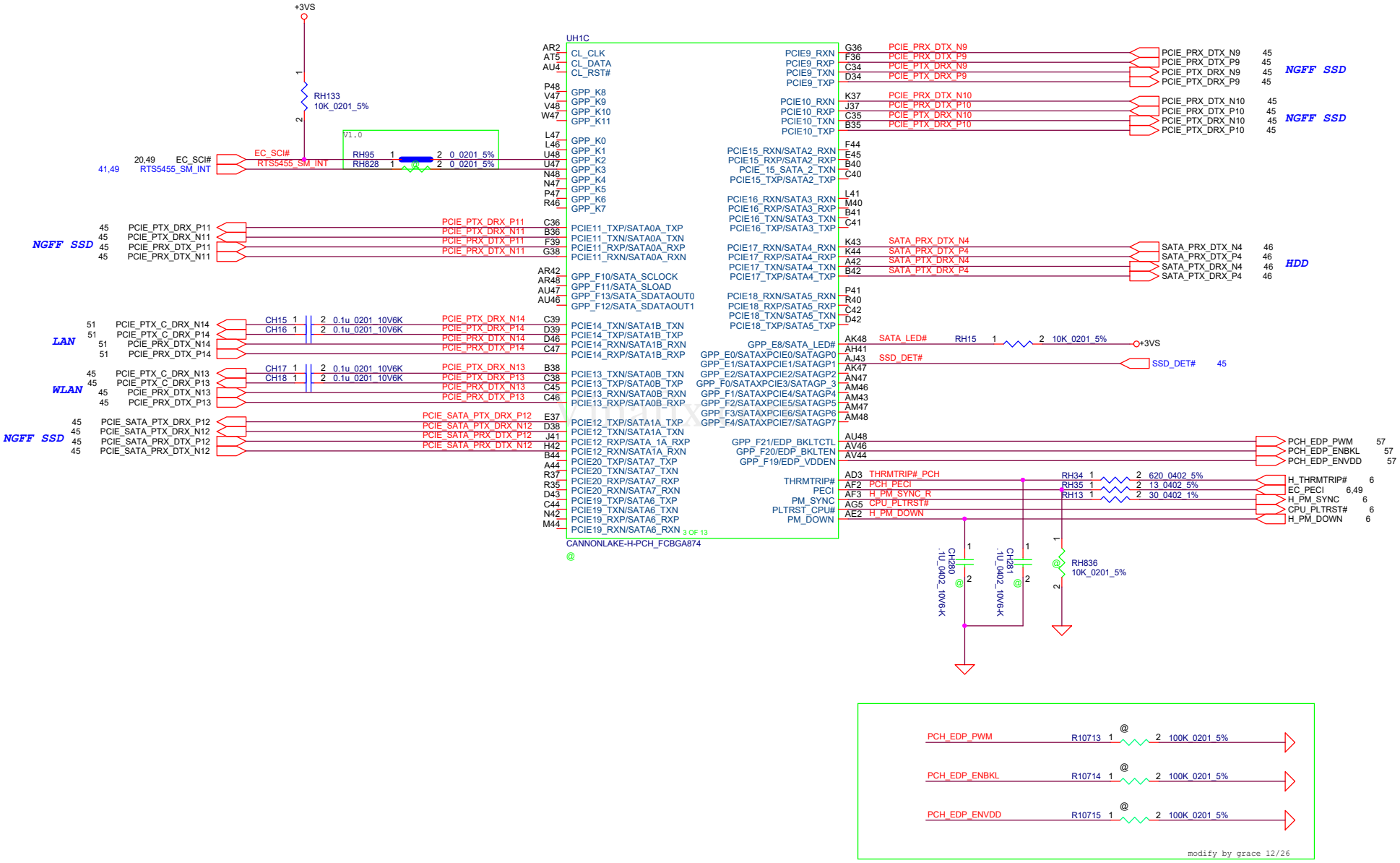

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Title: PCH (1/9) PCIe/SATA/GPPFG

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A3	Y540	2.0

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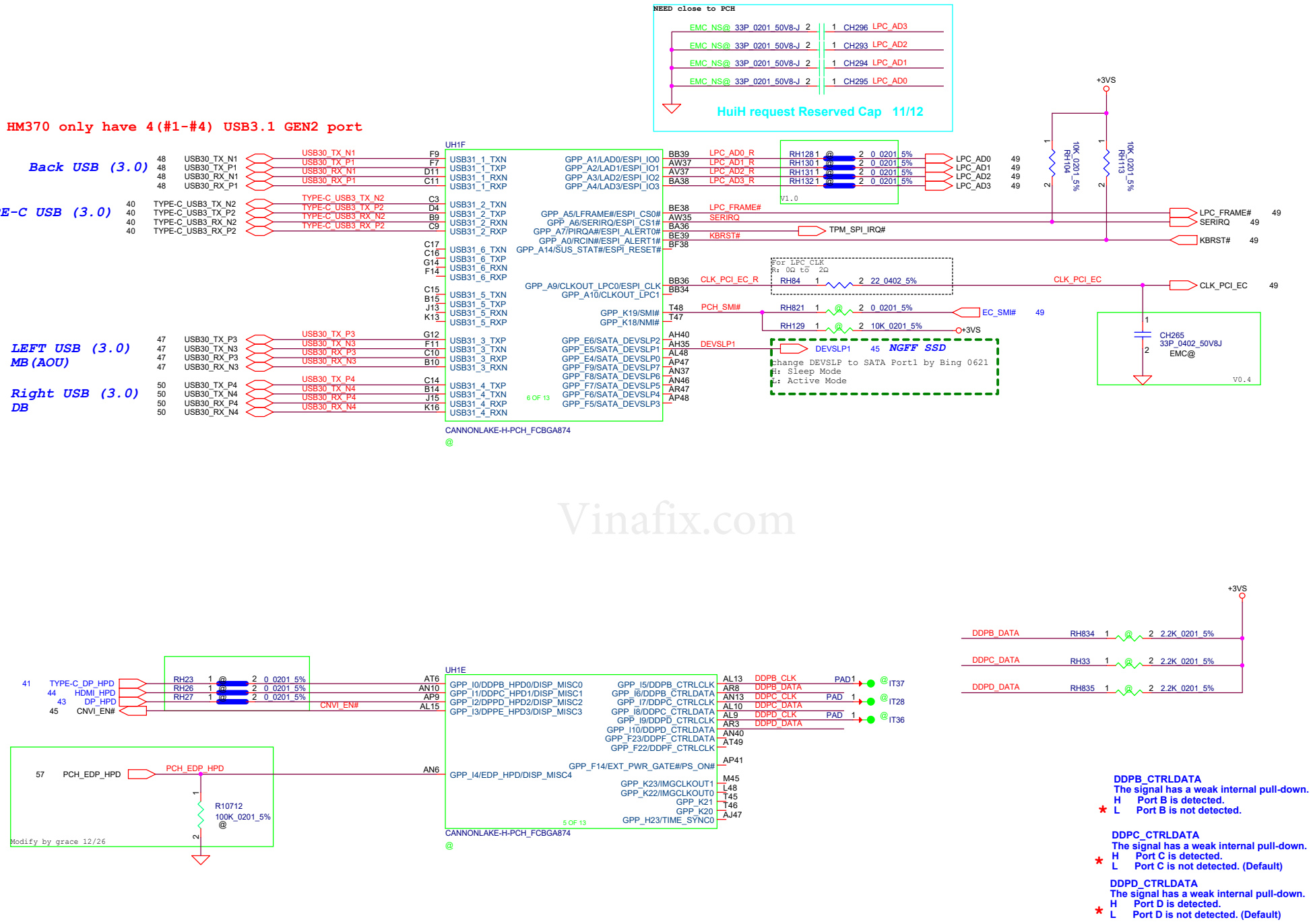

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DDPB_CTRLDATA
The signal has a weak internal pull-down.
H Port B is detected.
* L Port B is not detected.

DDPC_CTRLDATA
The signal has a weak internal pull-down.
H Port C is detected.
* L Port C is not detected. (Default)

DDPD_CTRLDATA
The signal has a weak internal pull-down.
H Port D is detected.
* L Port D is not detected. (Default)

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Title: **PCH (2/9) USB3/GPPAEFGHI**

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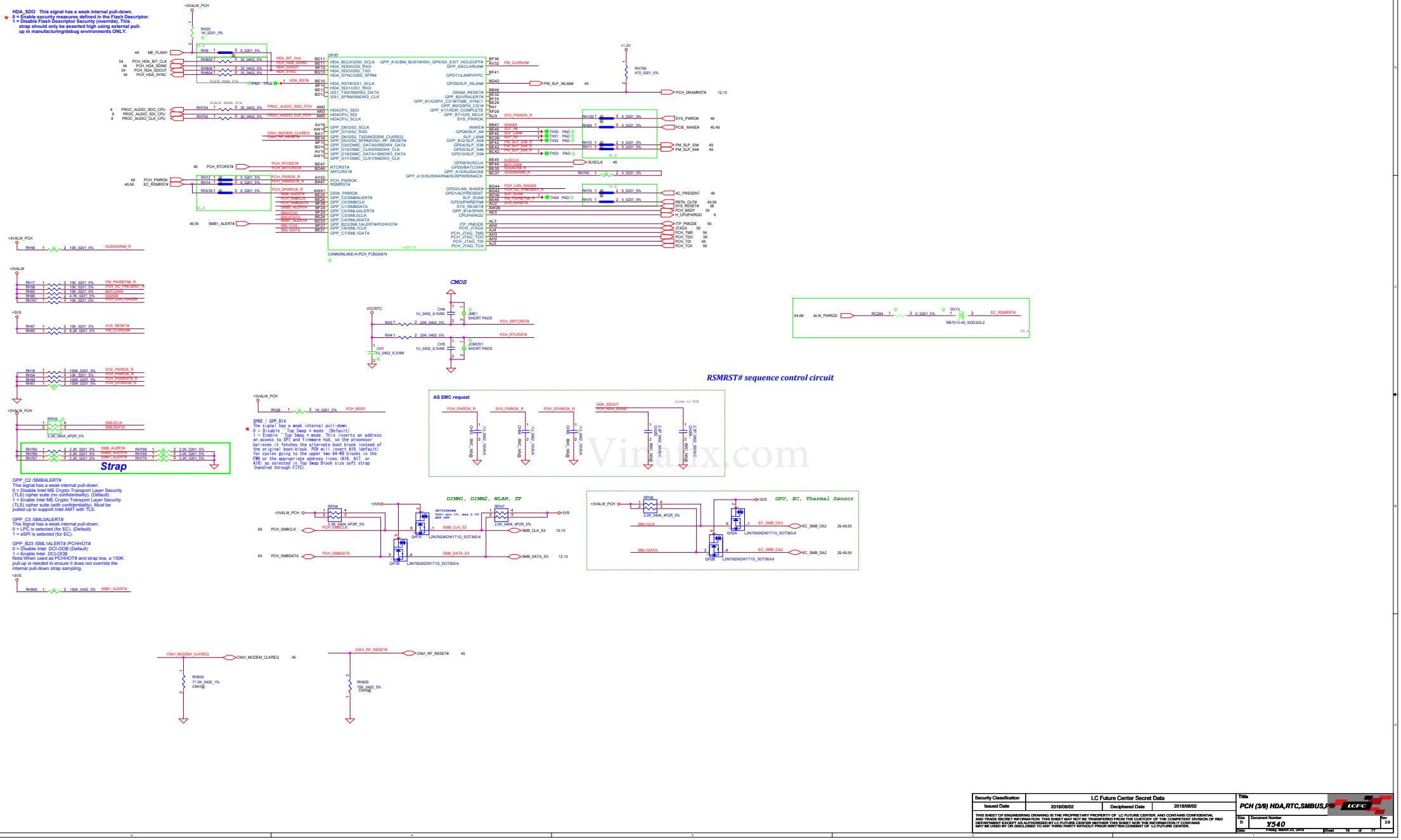

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Title: PCH (3/9) HDA,RTC,SMBUS,PM

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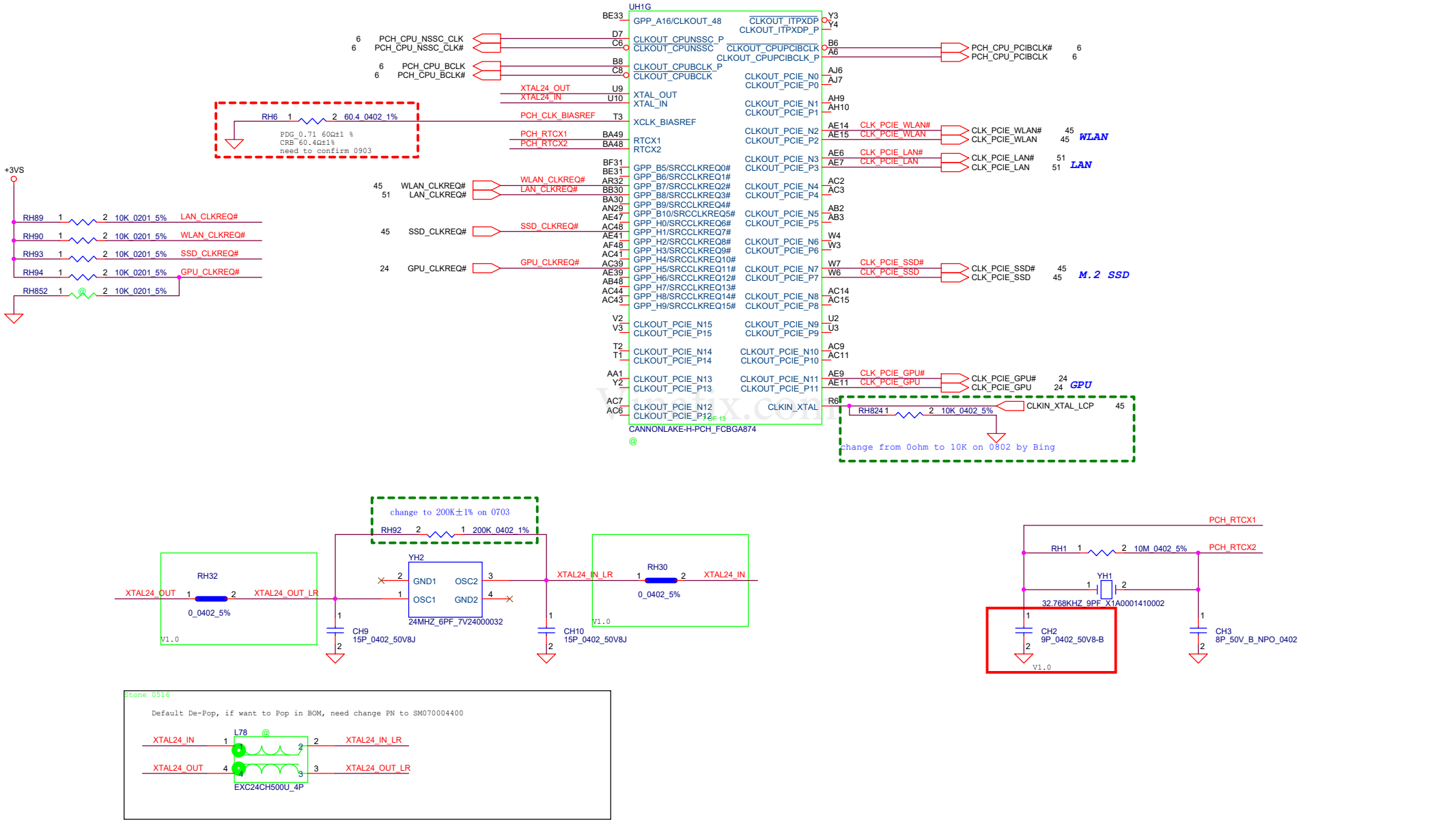

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Title: **PCH (3/9) CLOCK,GPPBH**

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A3	Y540	2.0

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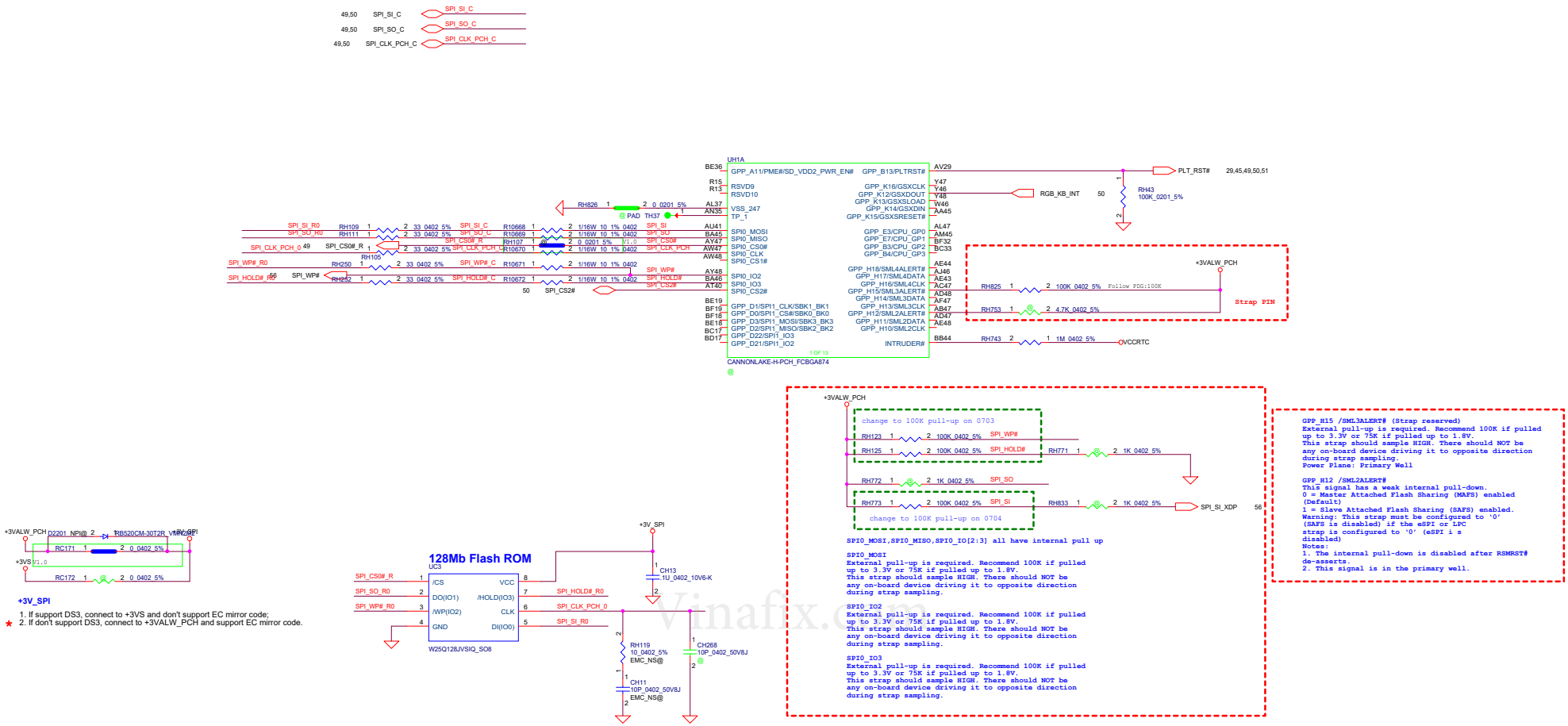

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Title: PCH (5/9) SPI,SMBUS,GPPBEGH

Size	Document Number	Rev
A2	Y540	2.0

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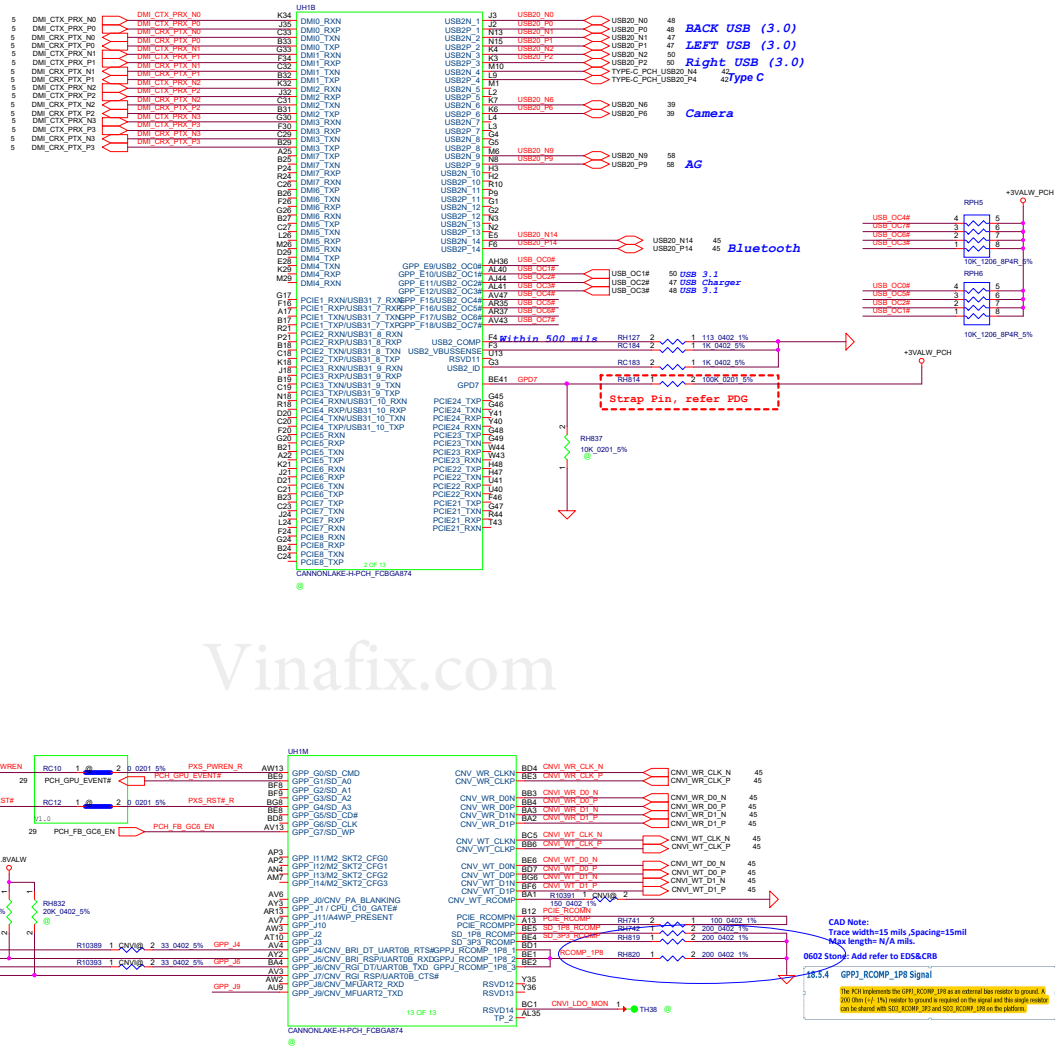

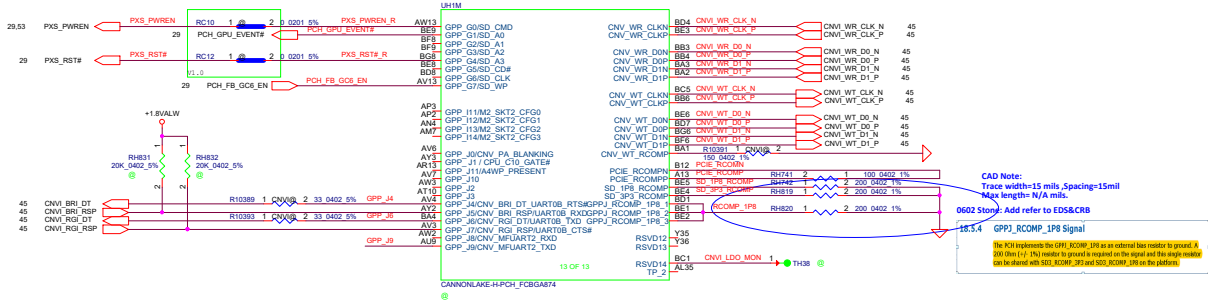

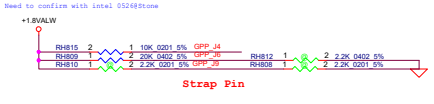

Primary Well Group J (1.8 V Only)

Signal	Usage	When Sampled	Comment
GPP_J4 / CNV_BRI_DT / UART0_RTS#	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_J6 / CNV_RGI_DT / UART0_TXD	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.
GPP_J9	1.8V VCCPSPI	Rising edge of RSMRST#	The signal has a weak internal pull-down 0 = VCCSPI is connected to 3.3V rail 1 = VCCSPI is connected to 1.8V rail ***Note:*** If VCCSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os

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Title	Blank		
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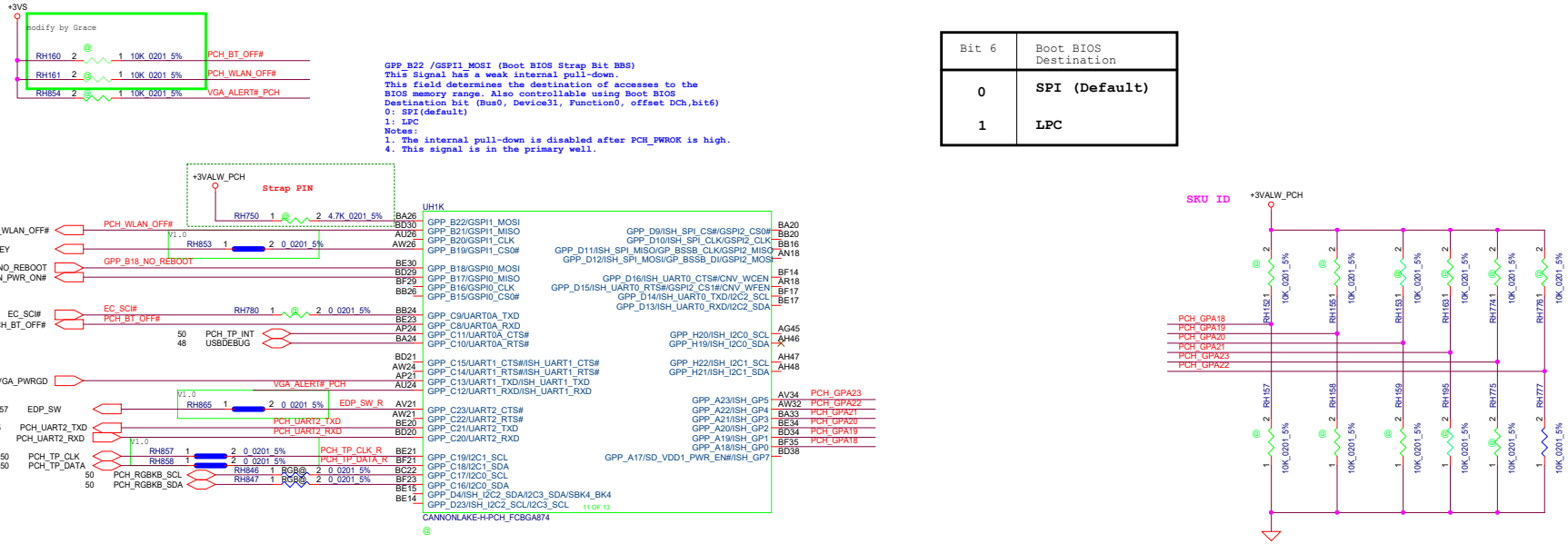
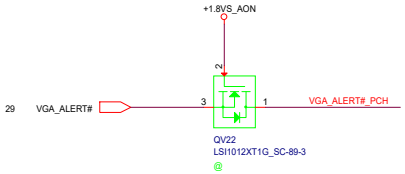
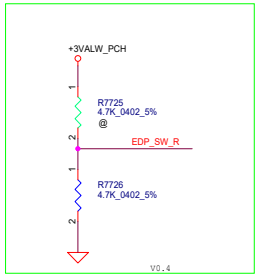


Bit 6	Boot BIOS Destination
0	SPI (Default)
1	LPC





Function	PCH_GPA18	PCH_GPA19	PCH_GPA20	PCH_GPA21	PCH_GPA22	PCH_GPA23
Y540-15-N17P	0	0	0	0	x	x
Y540-15-N18E G0	0	0	0	1	x	x
Y540-15-N18E G1	0	0	1	0	x	x
Y540-15-N18P	0	0	1	1	x	x
Y7000P-15-N17P	0	1	0	0	x	x
Y7000P-15-N18E G0	0	1	0	1	x	x
Y7000P-15-N18E G1	0	1	1	0	x	x
Y7000P-15-N18P	0	1	1	1	x	x
Y540-17-N17P	1	0	0	0	x	x
Y540-17-N18E G0	1	0	0	1	x	x
Y540-17-N18E G1	1	0	1	0	x	x
Y540-17-N18P	1	0	1	1	x	x

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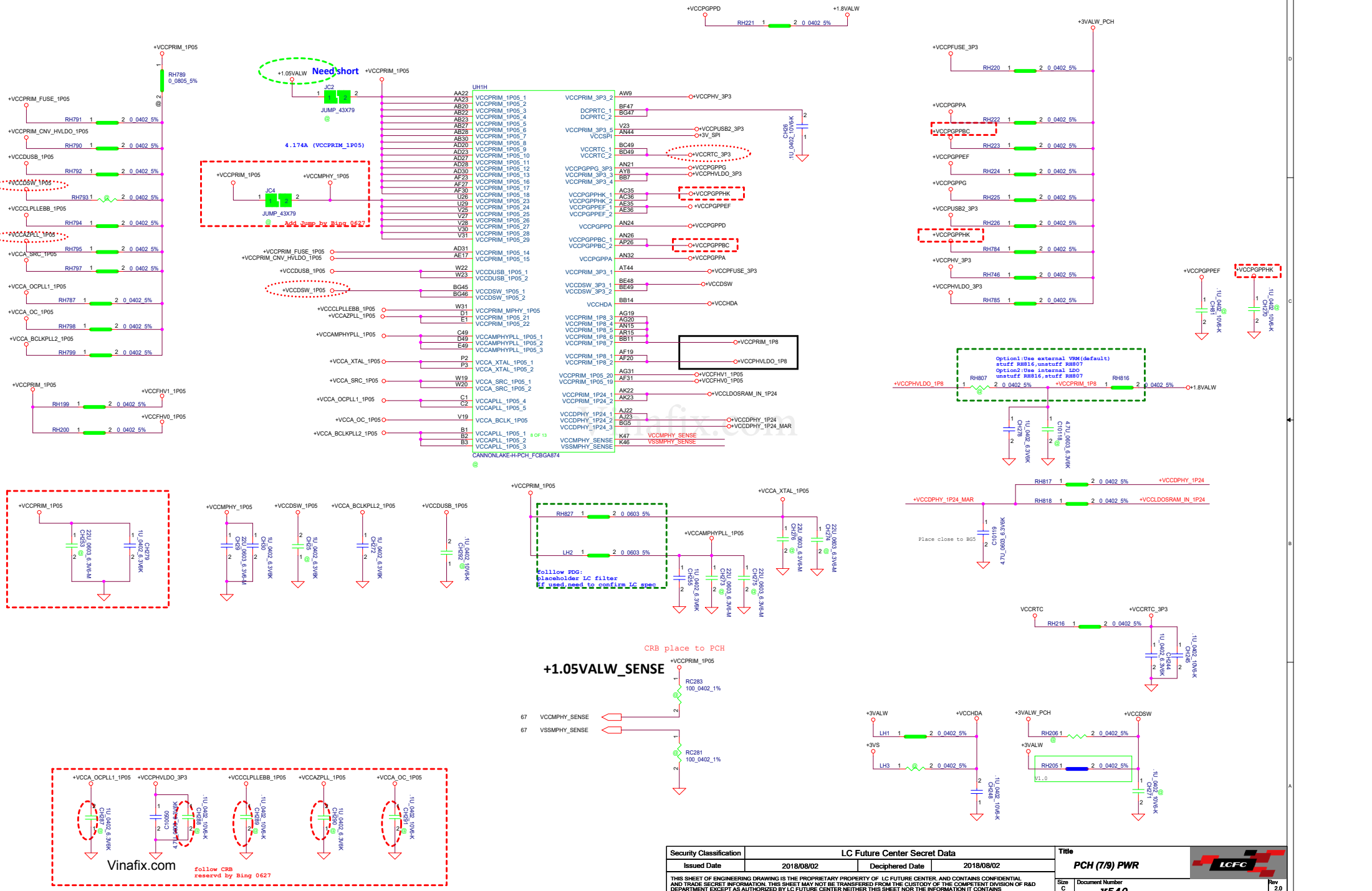
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: PCH (6/9) GPPPABCD, I2C

Size	Document Number	Rev
C	Y540	2.0

Date: Friday, March 22, 2019 Sheet 20 of 77


+VCCPGPPD
+1.8VALW
RH221
+3VALW_PCH
+VCCPRIM_1P05
+1.05VALW
Need short
JC2
JUMP_43X79
4.174A (VCCPRIM_1P05)
UH1H
+VCCPRIM_FUSE_1P05
+VCCPRIM_CNV_HVLDO_1P05
+VCCDUSB_1P05
+VCCDSW_1P05
+VCCCLPLLEBB_1P05
+VCCAZPLL_1P05
+VCCA_SRC_1P05
+VCCA_OCPLL1_1P05
+VCCA_OC_1P05
+VCCA_BCLKPLL2_1P05
+VCCFHV1_1P05
+VCCFHV0_1P05
+VCCPRIM_MPHY_1P05
+VCCAMPHYPLL_1P05
+VCCA_XTAL_1P05
+VCCA_BCLKPLL1_1P05
+VCCAPLL_1P05
+VCCPRIM_1P8
+VCCPHVLDO_1P8
+VCCPHY_1P24
+VCCPHY_1P24_MAR
+VCCLDOSRAM_IN_1P24
+VCCPHV_3P3
+VCCPUSB2_3P3
+3V_SPI
+VCCRTC_3P3
+VCCPGPPD
+VCCPGPPBC
+VCCPGPPA
+VCCPGPPEF
+VCCPGPPHK
+VCCPGPPG
+VCCPFUSE_3P3
+VCCDSW
+VCCHDA
+VCCPHVLDO_3P3
VCCMPHY_SENSE
VSSMPHY_SENSE
CANNONLAKE-H-PCH_FCBGA874
Option1:Use external VRM(default)
stuff RH816,unstuff RH807
Option2:Use internal LDO
unstuff RH816,stuff RH807
follow PDG:
placeholder LC filter
If used,need to confirm LC spec
CRB place to PCH
+1.05VALW_SENSE
RC283
RC281
100_0402_1%
follow CRB
reserved by Bing 0627
Vinafix.com
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2018/08/02
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2018/08/02
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Title
PCH (7/9) PWR
LCFC
Size
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Document Number
Y540
Rev
2.0
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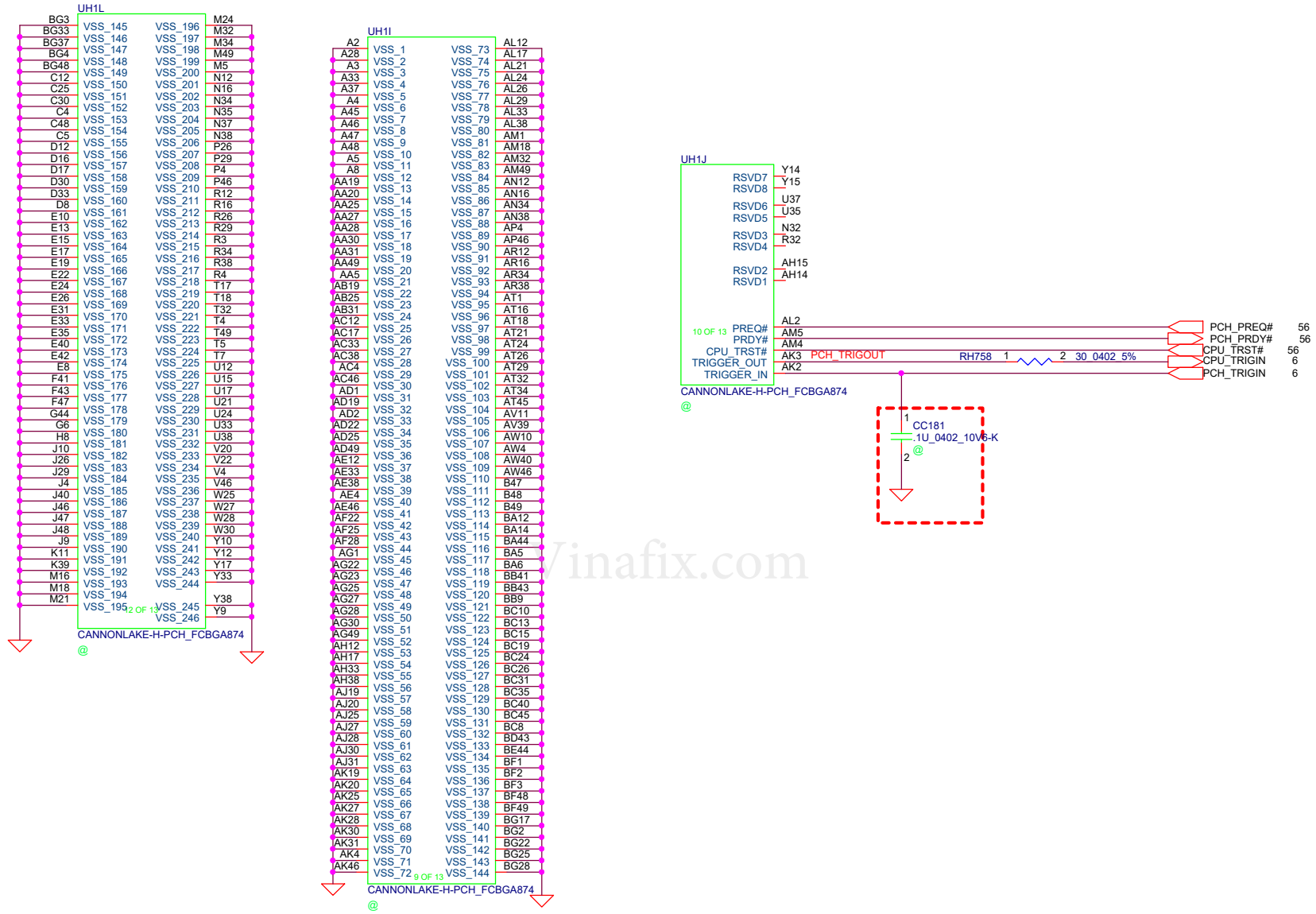

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: PCH (9/9) VSS

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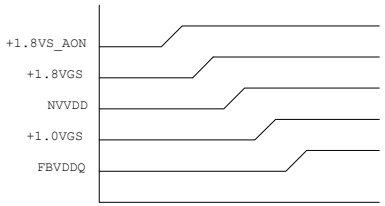
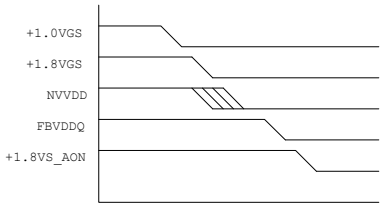
N18E-G1 GPIO

GPIO	I/O	GPIO Name	Function Description	Net name	I/O Termination
GPIO0	OUT	NVVDD_PWM_VID	PWM Output to control NVVDD	NVVDD_PWM_VID	
GPIO1	OUT	GC6:GC6_FB_EN	GC6 FRAME BUFFER ENABLE	FB_GC6_EN	(10K pull down)
GPIO2	IN	GC6:GPU_EVENT*	Wake the GPU from GC6 state	GPU_EVENT#_R	(10K pull High)
GPIO3	OUT	UNUSED	UNUSED	UNUSED	
GPIO4	OUT	GC6:1V8_MAIN_EN	GPU power sequencing for GC6 --- 1V8_MAIN_EN	1V8_MAIN_EN	(10K pull High)
GPIO5	IN	FRAME_LOCK*	Active low Frame Lock for NVSR panel	GPU_FRAME_LOCK#	
GPIO6	OUT	NVVDD_PSI*	Phase Shedding, NVVDD_PSI	NVVDD_PSI	(5.1K pull High)
GPIO7	OUT	LCD_BL_PWM	LCD Panel Backlight PWM	GPU_EDP_PWM	(100K pull down)
GPIO8	OUT	MEM_VDD_CTL	Memory voltage Control	FBVDDQ_SEL	(10K pull down)
GPIO9	I/O	THERM_ALERT*	Active Low Thermal Alert	VGA_ALERT#	(10K pull High)
GPIO10	OUT	MEM_VREF_CTL	Memory VREF Control	MEM_VREF	(10K pull down)
GPIO11	OUT	LCD_VCC	LCD Panel VOLTAGE	GPU_EDP_ENVDD	(10K pull down)
GPIO12	IN	PWR_LEVEL	AC power detect or power supply overdraw input	VGA_AC_DET_R	(10K pull High)
GPIO13	OUT	UNUSED	UNUSED	UNUSED	
GPIO14	IN	HPD_IFPA*	Hot Plug Detect for IFPA	IFPA_HPD	(10K pull High)
GPIO15	IN	HPD_IFPB*	Hot Plug Detect for IFPB	UNUSED	
GPIO16	OUT	UNUSED	UNUSED	UNUSED	
GPIO17	IN	HPD_IFPD*	Hot Plug Detect for IFPD	GPU_EDP_ENBKL	(100K pull down)
GPIO18	IN	HPD_IFPE*	Hot Plug Detect for IFPE	IFPE_HPD	(10K pull High)
GPIO19	OUT	Reserved	UNUSED	UNUSED	
GPIO20	OUT	GC6:NB_FGC6	Low Power States Fast CG6	NB_FGC6	(10K pull down)
GPIO21	OUT	LCD_BLEN	LCD Panel Backlight Enable	GPU_EDP_ENBKL	
GPIO22		UNUSED	UNUSED	UNUSED	
GPIO23		UNUSED	UNUSED	RASTER_SYNC1	(100K pull down)
GPIO24	IN	HPD_IFPF*/USBC_HPD* or DONGLE_DET*	Hot Plug Detect for IFPF or USBC	UNUSED	
GPIO25	OUT	FBVDD_PSI	Turns off phases of the Frame buffer power supply	FBVDDQ_PSI	(5.1K pull High)
GPIO26		FP_FUSE	Field-programming of select fuses	GPIO26_FP_FUSE	(10K pull down)
GPIO27	IN	HPD_IFPC*	Hot Plug Detect for IFPC	IFPC_HPD	(10K pull High)
GPIO28		ADC_MUX_SEL	OVRM MUX SEL	ADC_MUX_SEL_R	(10K pull High)
GPIO29	OUT	IDLE_IN_SW	IDLE_IN_SW	IDLE_IN_SW	(10K pull down)
GPIO30		UNUSED	UNUSED	UNUSED	

N18E-G1 Power Sequence



1. The ramp time for any rail must be more than 40us and is recommended to be less than 2ms.
2. Delay from 1V8_MAIN_EN to PEXVDD/NVVDD_PGOOD must NOT exceed 4ms.
3. It is recommended that the delay from 1V8_AON on to PEXVDD/NVVDD_PGOOD assertion not exceed 20ms.
4. Power up NVVDD must be 90% before PEXVDD can start ramp-up.
5. All 3.3V devices that connect to the GPU must be powered after 1V8_AON;GPU cannot have any 3.3V leakage paths before 1V8_AON is present.
6. Refer to the IFPD Memory SPEC for memory-related power sequencing.
7. FBVDD/Q, USB_VDDP and 1V8_AON don't need power cycle for GC6



1. PEXVDD must power down before NVVDD,
2. For GDDR6, VPP must be equal to or higher than FBVDD/Q at all times;use gate logic and discharge circuit as needed
3. All 3.3V devices that connect to the GPU must be ramp down before 1V8_AON; GPU can NOT have any 3.3V leakage path after 1V8_AON and 1.8V_MAIN power down.
4. Power down of PEXVDD must be less than 10% before NVVDD can start ramp-down..

H=High: Tied to 1.8V
M=Middle: Tied to 0.9V
L=Low: Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	N18E-G1 VRAM
L	L	L	0 (0x0000)	Samsung K4Z80325BC-HC14
L	L	H	1 (0x0001)	Micron MT61K256M32JE-14:A
L	H	L	2 (0x0002)	
L	H	H	3 (0x0003)	
H	L	L	4 (0x0004)	
H	L	H	5 (0x0005)	
H	H	L	6 (0x0006)	
H	H	H	7 (0x0007)	
L	L	M	8 (0x0008)	
L	M	L	9 (0x0009)	
L	M	H	10 (0x000A)	
L	H	M	11 (0x000B)	
M	L	L	12 (0x000C)	
M	L	H	13 (0x000D)	

FS_OVERT# FUNCTION

ROM_SO	ROM_SI	ROM_SCLK	FS_OVERT# FUNCTION
L	L	L	FS_OVERT# function ENABLE
L	L	H	FS_OVERT# function DISABLED Reserved; do not configure

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

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Title: *N18E VGA Notes List*

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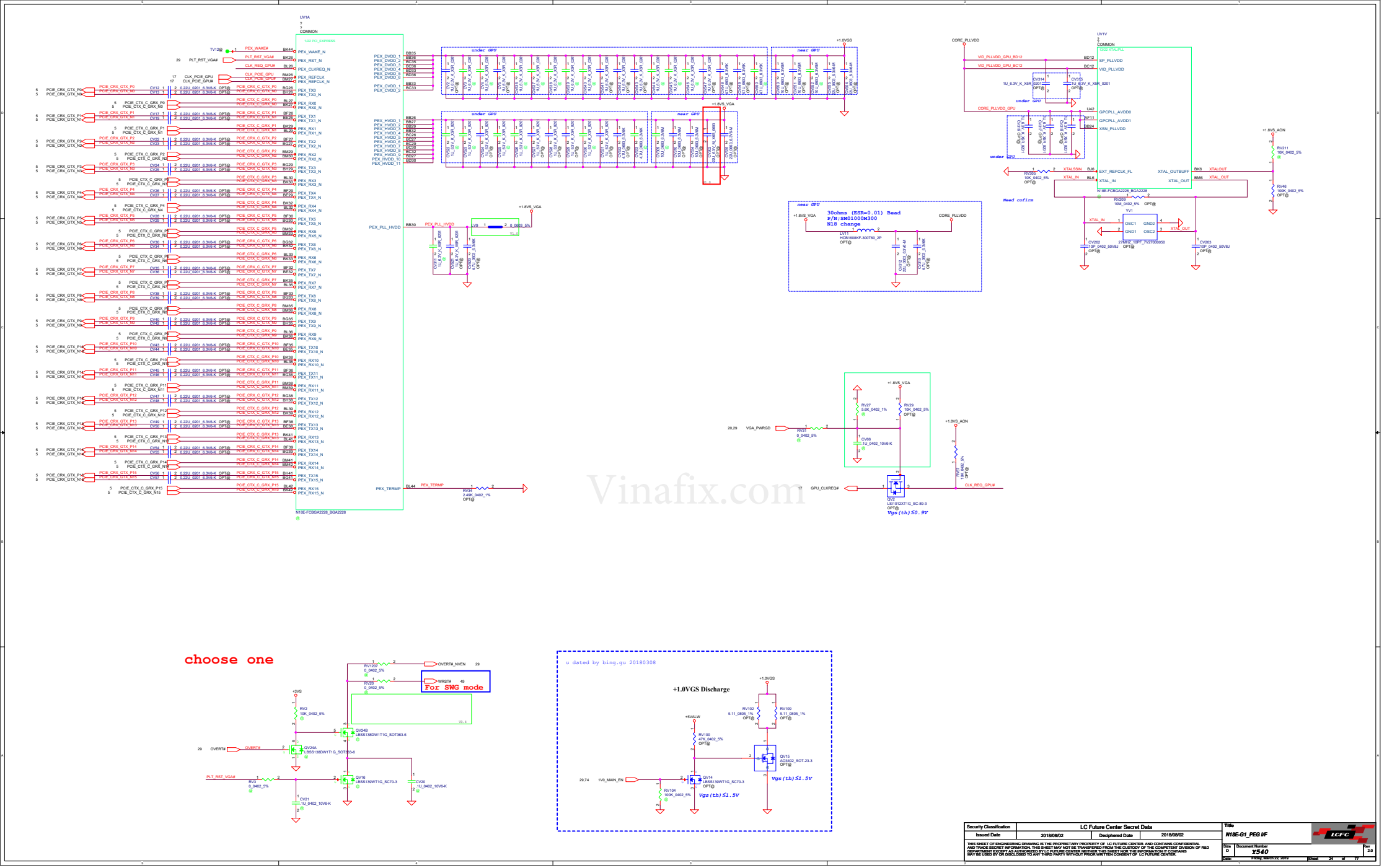

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Title	N18E-G1_PEG I/F		
Size D	Document Number Y540		Rev 2.0
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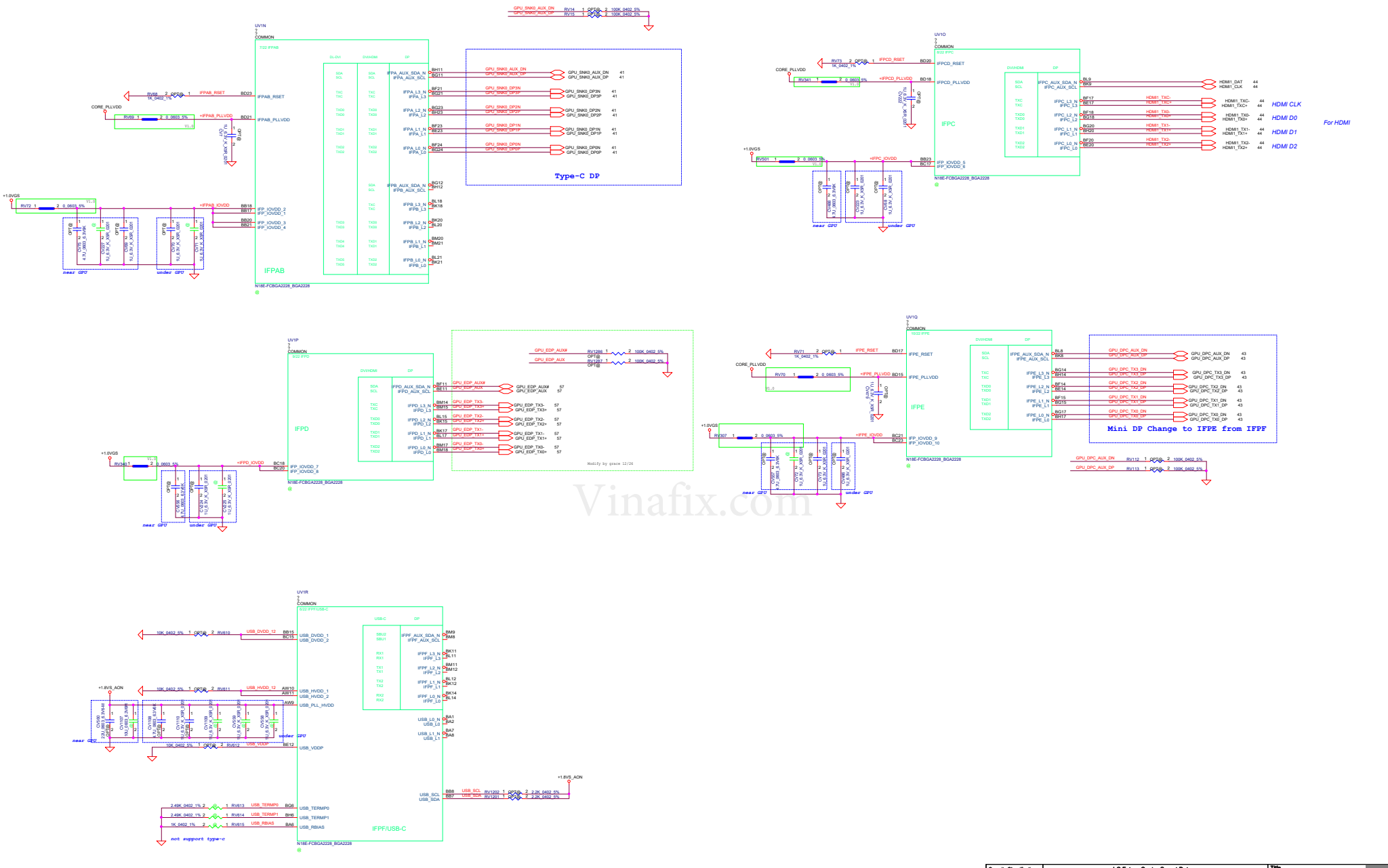

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Title: N18E-G1_DIGITAL OUT I/F

Size: D | Document Number: Y540 | Rev: 2.0

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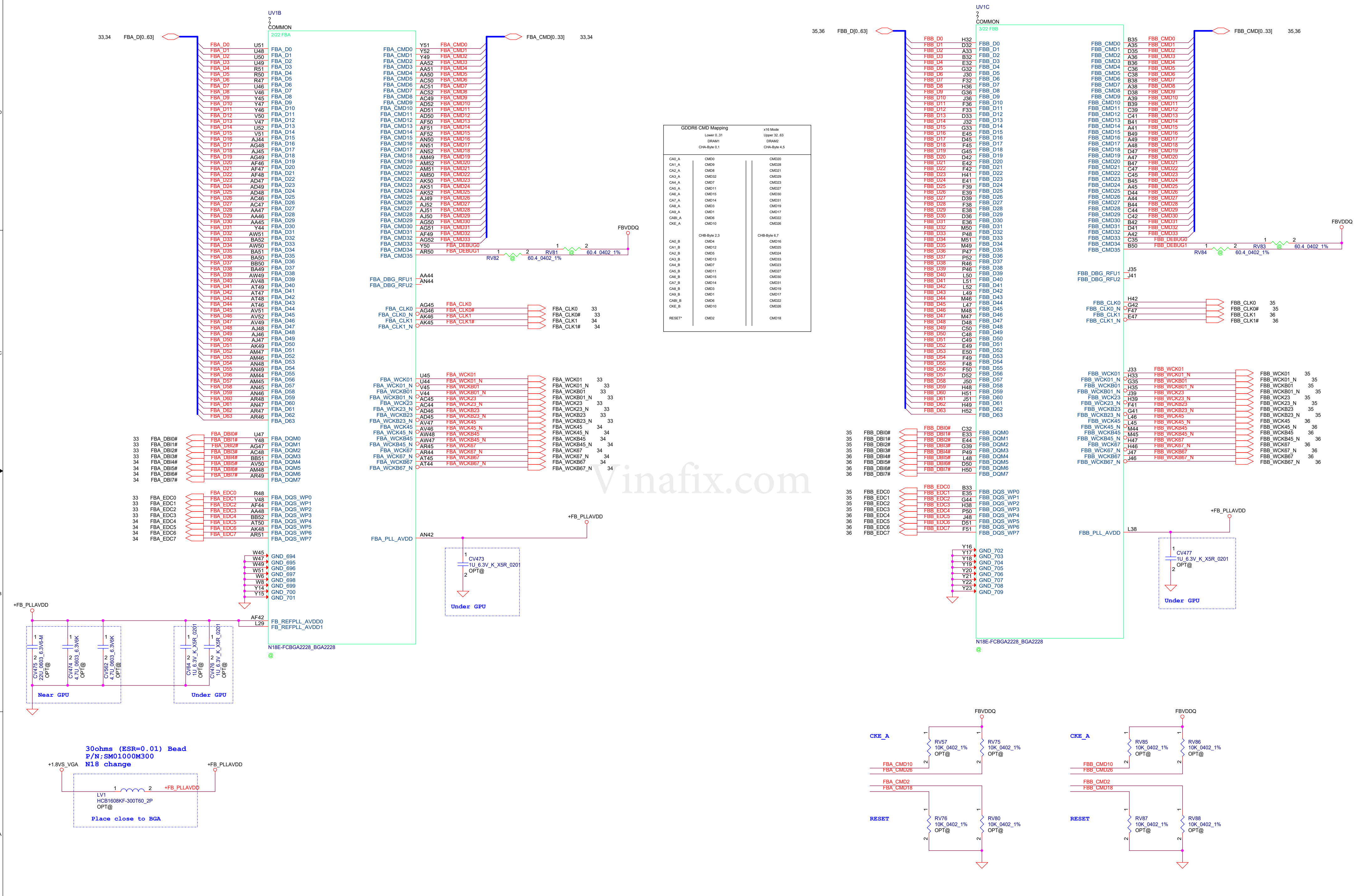

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Title: N18E-G1_VRAM A/B

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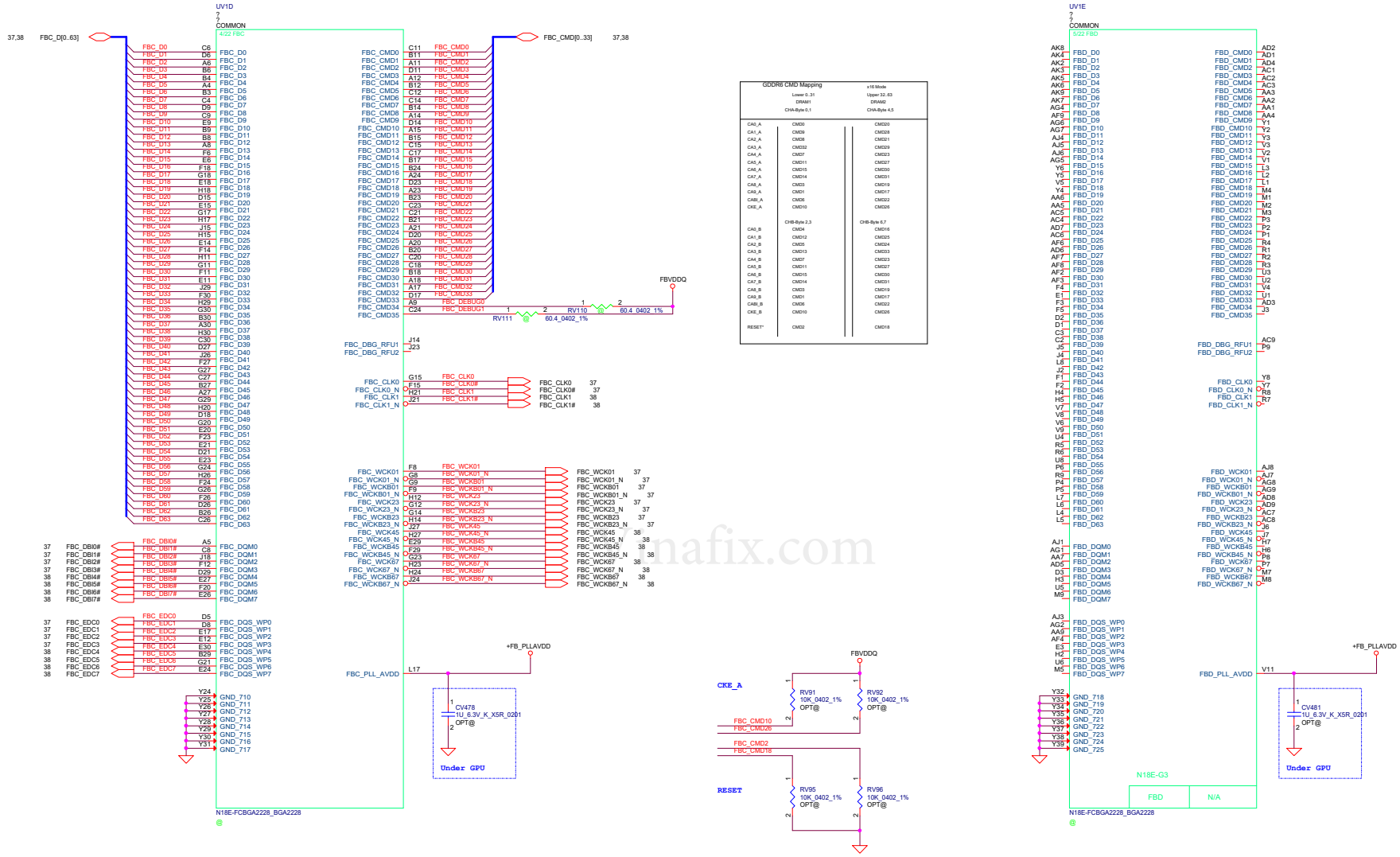
Size: A2 | Document Number: Y540 | Rev: 2.0

Date: Friday, March 22, 2019 | Sheet 26 of 77

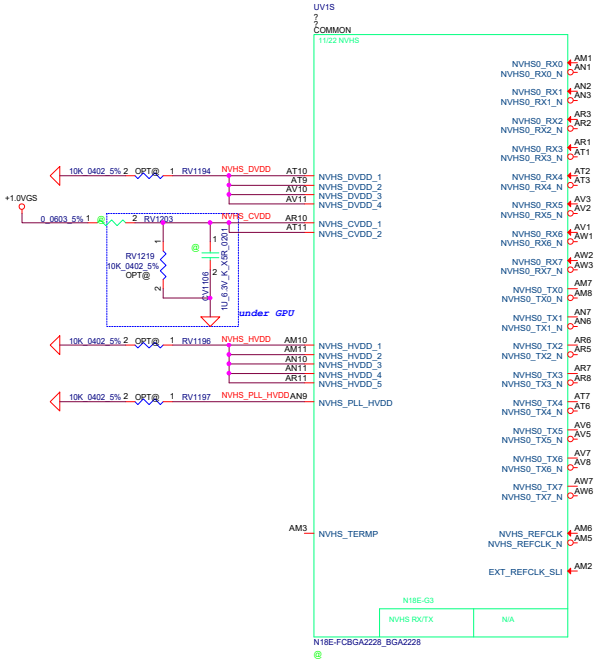


Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: N18E-G1_VRAM C/D

Size: A2 | Document Number: Y540 | Rev: 2.0

Date: Friday, March 22, 2019 | Sheet 27 of 77



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: N18E-G1_NVHS I/F

Size	Document Number	Rev
A2	Y540	2.0

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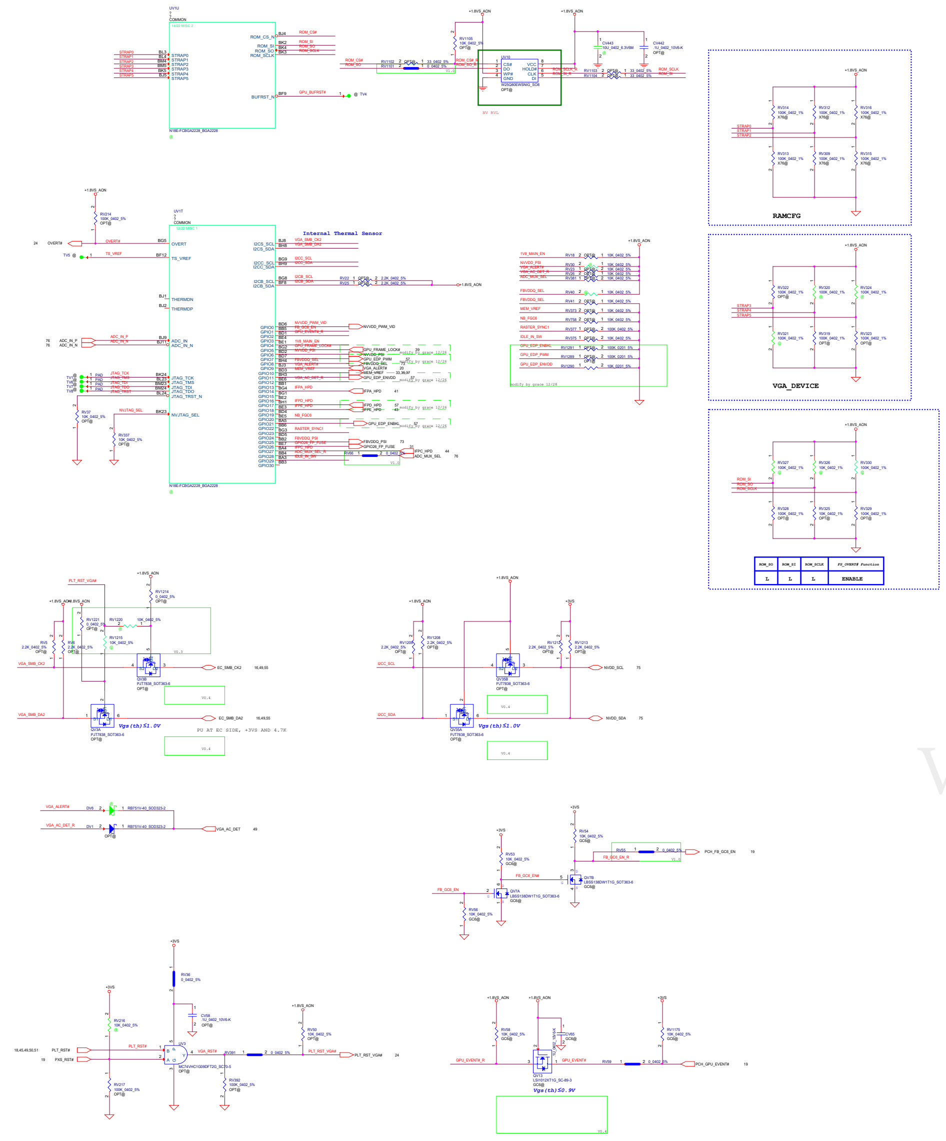
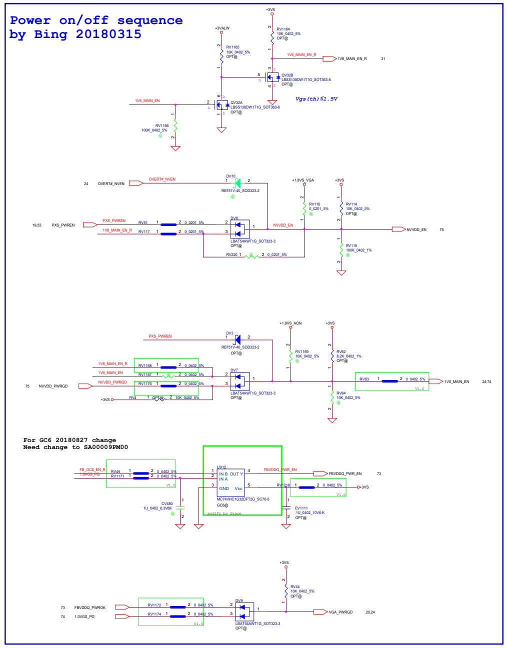
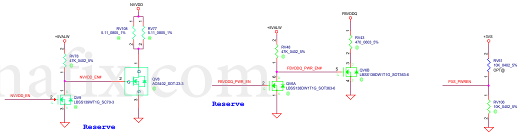


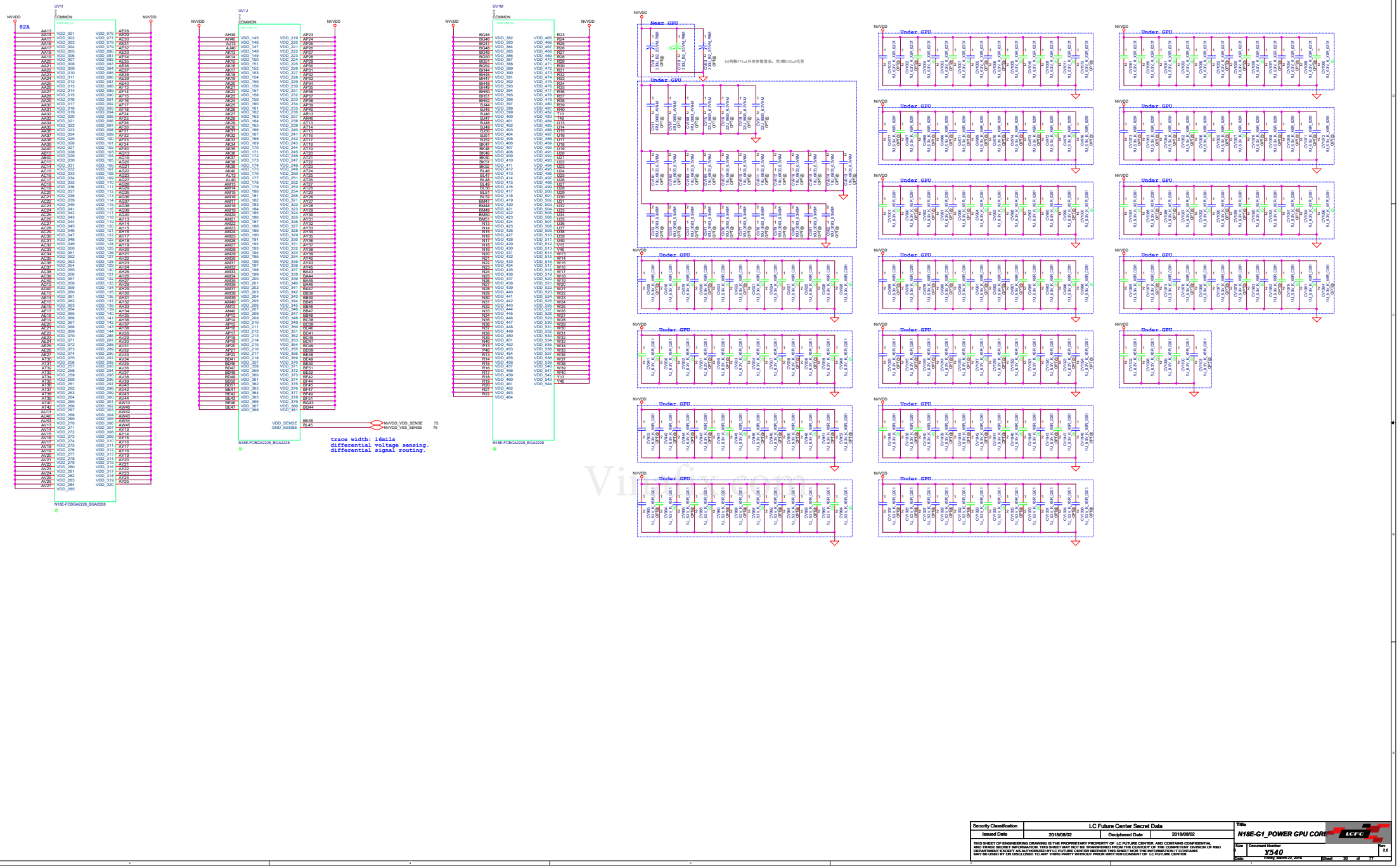




Y540 N18E	Strap5	Strap4	Strap3
DGPU only+Non G-sync panel	0	0	1
DGPU only+G-sync panel	1	0	1

Key Specifications:

	N18E-G3	N18E-G2	N18E-G1
Product Part Number	N18E-G3-A1	N18E-G2-A1	N18E-G1-KD-A1
NVIDIA Part Number[1] (used on labels of packaging materials)	TU104-750-A1	TU106-750-A1	TU106-725-KD-A1
Device ID	• Primary: 0x1E90 • Secondary: 0x1ED0	• Primary: 0x1F10 • Secondary: 0x1F50	• Primary: 0x1F11 • Secondary: 0x1F51
Memory interface	256-bit GDDR6	256-bit GDDR6	192-bit GDDR6
Package	GB4B-256	GB4B-256	GB4B-256



Security Classification	LC Future Center Secret Data		Title: N18E-G1_POWER GPU CORE
Issued Date	2018/08/02	Deciphered Date	2018/08/02	
Size: D	Document Number: ¥540		Rev: 2.0
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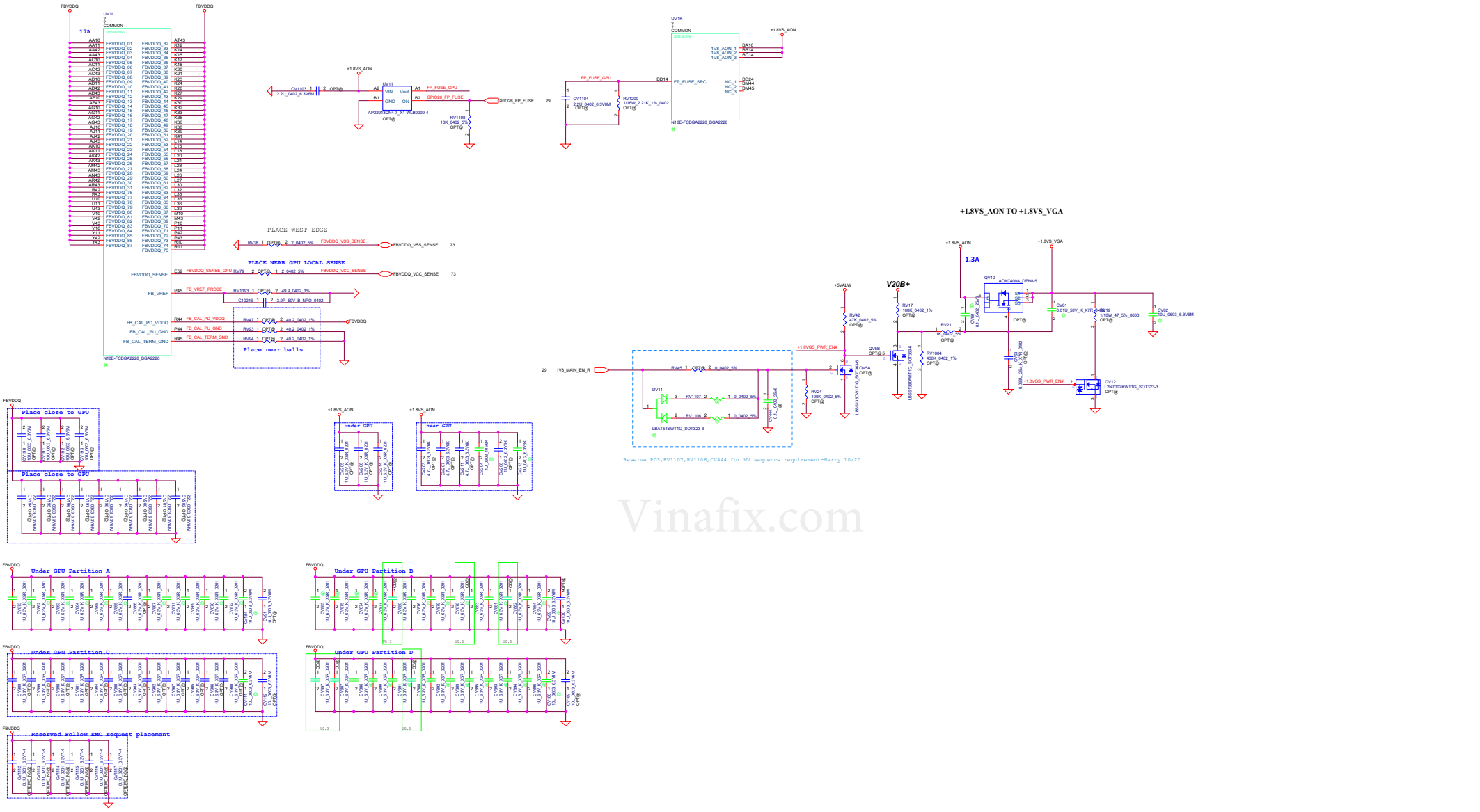

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Title	N18E-G1_POWER VDDQ		
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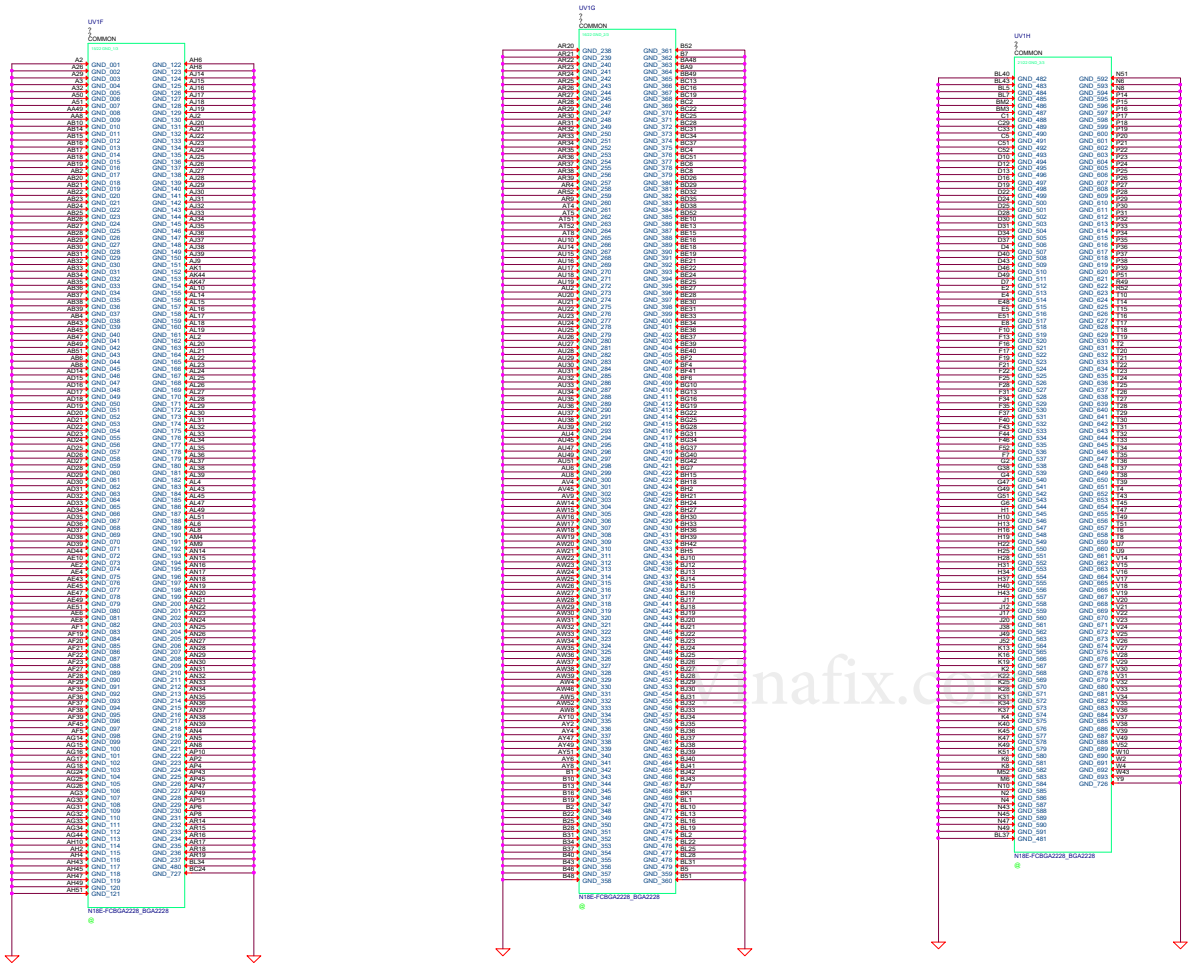

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Title	N18E-G1_GND		
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D	Y540		2.0
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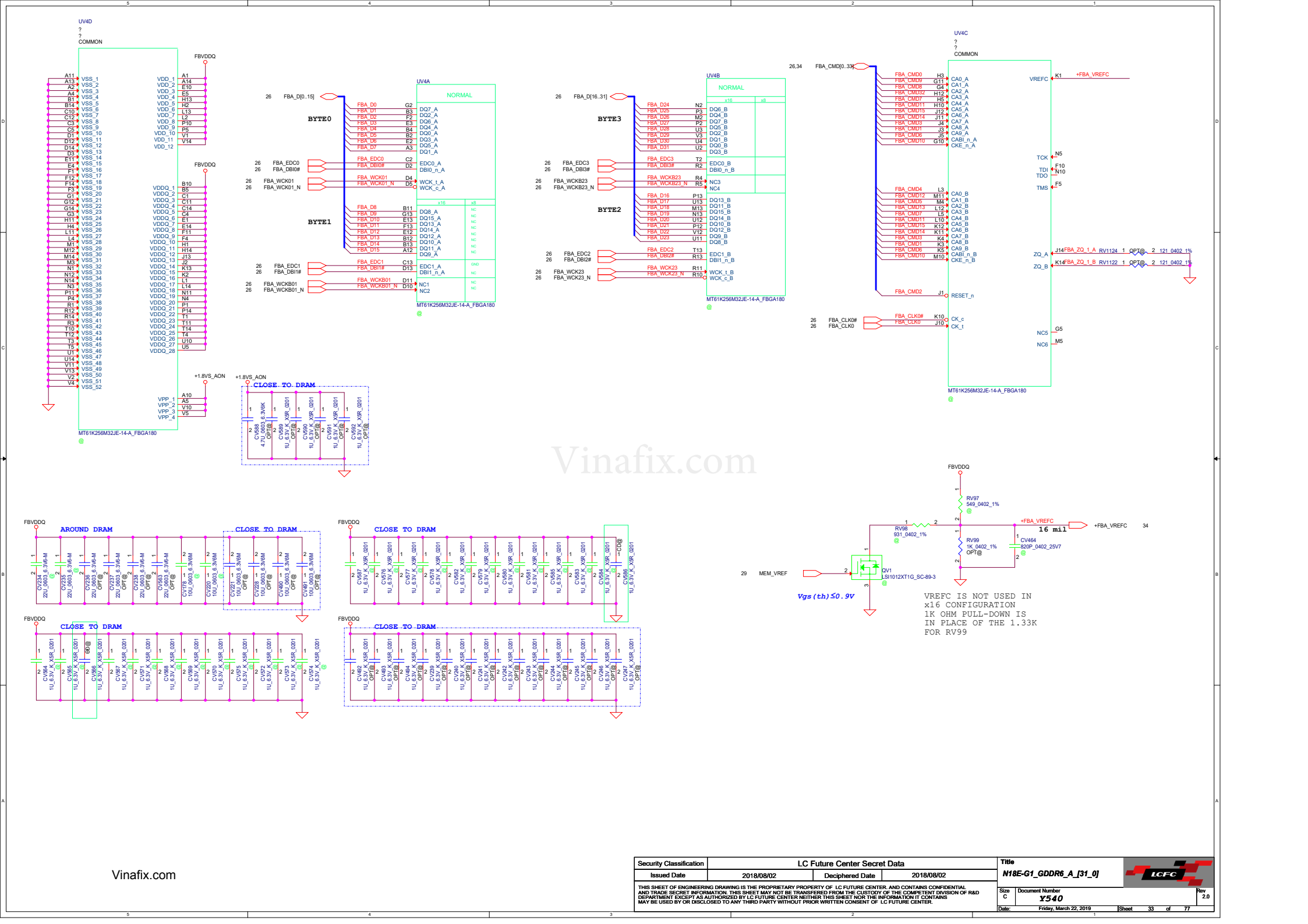

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Title: N18E-G1_GDDR6_A_[31_0]

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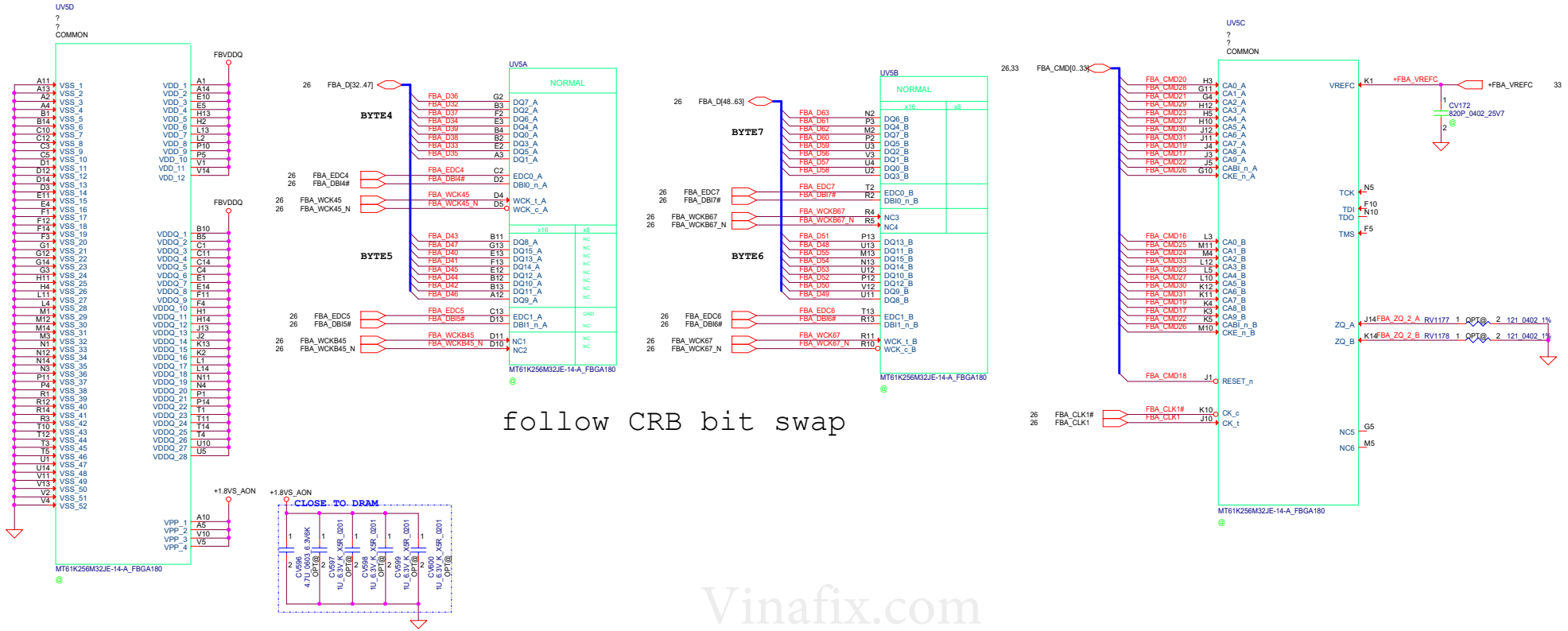
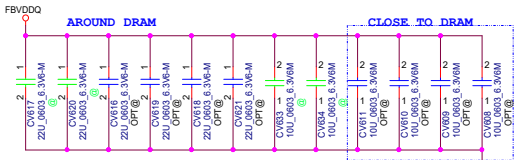
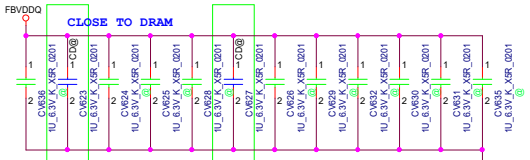
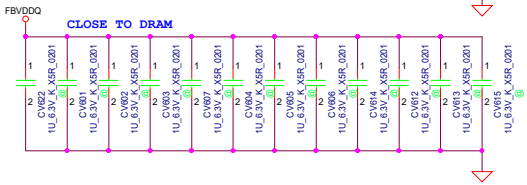
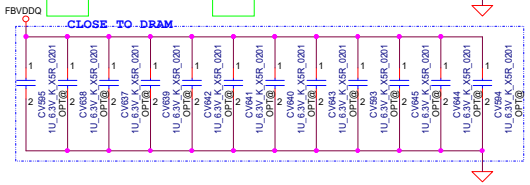




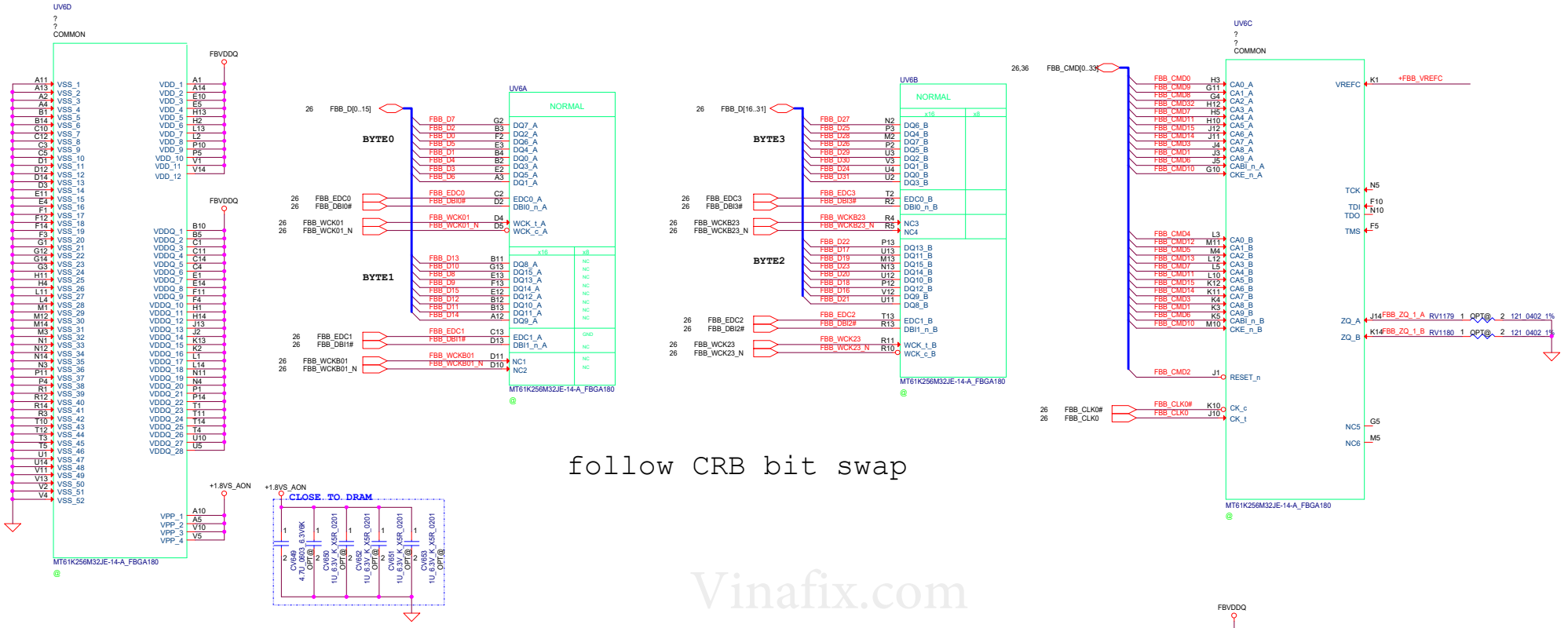


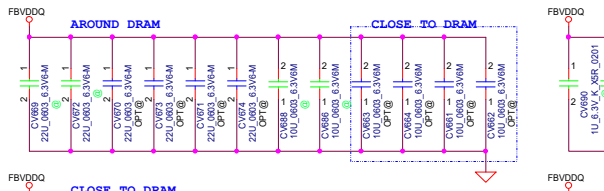


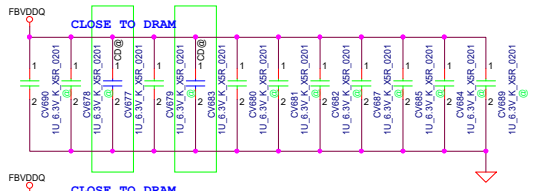


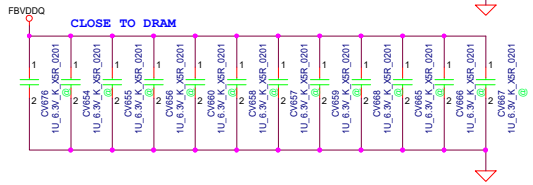
Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

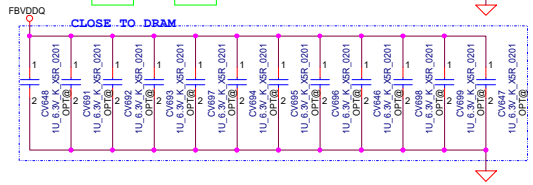
Title	N18E-G1_GDDR6_A_[63_32]		
Size C	Document Number Y540		Rev 2.0
Date: Friday, March 22, 2019	Sheet 34 of 77		

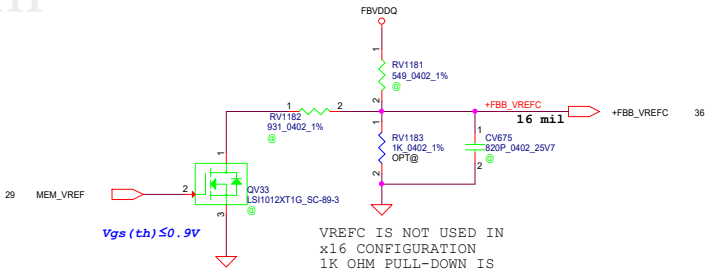






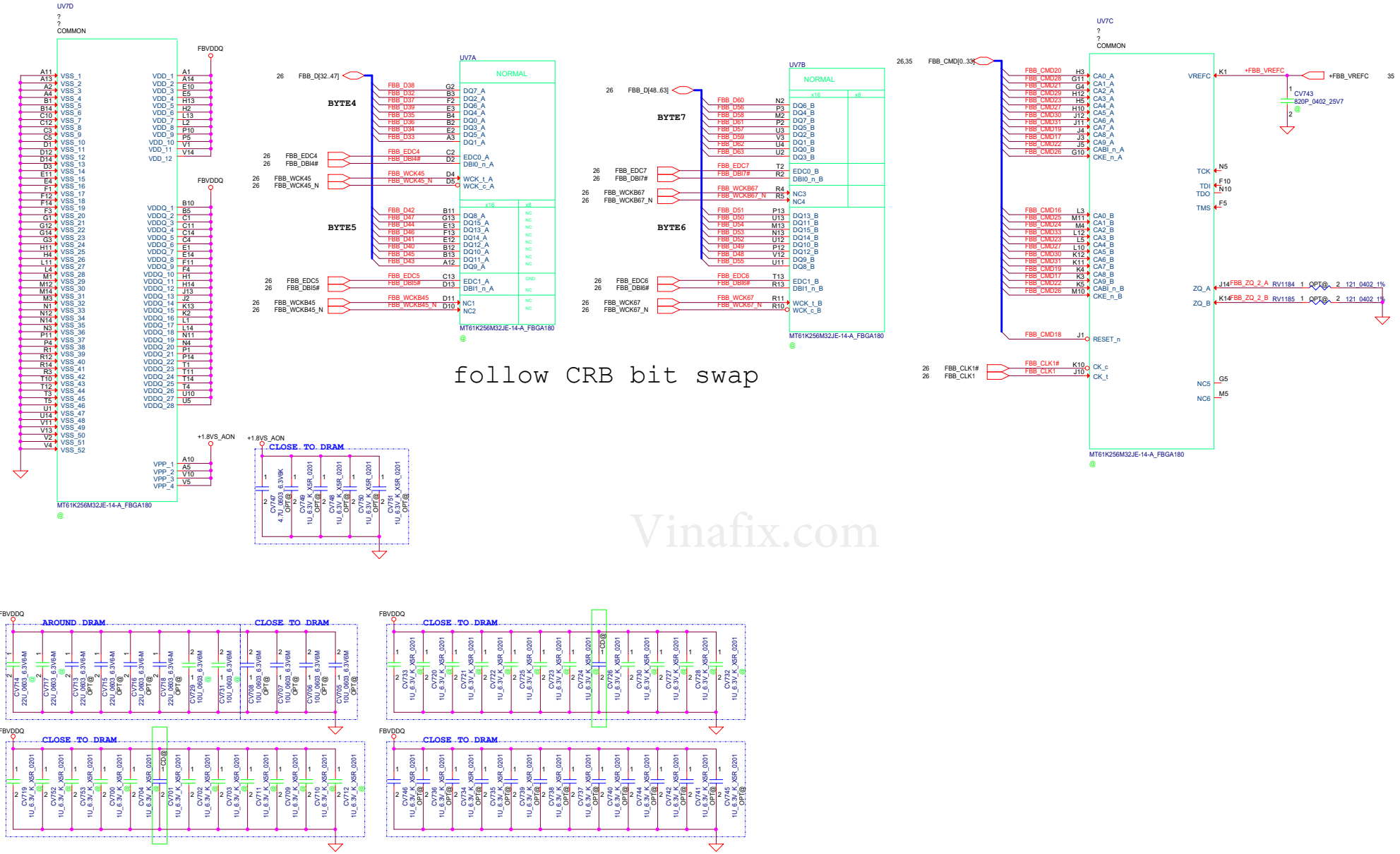






Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	N18E-G1_GDDR6_B_[31_0]		
Size C	Document Number Y540		Rev 2.0
Date: Friday, March 22, 2019	Sheet 35 of 77		



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Title: *N18E-G1_GDDR6_B_[63_32]*

Size	Document Number	Rev
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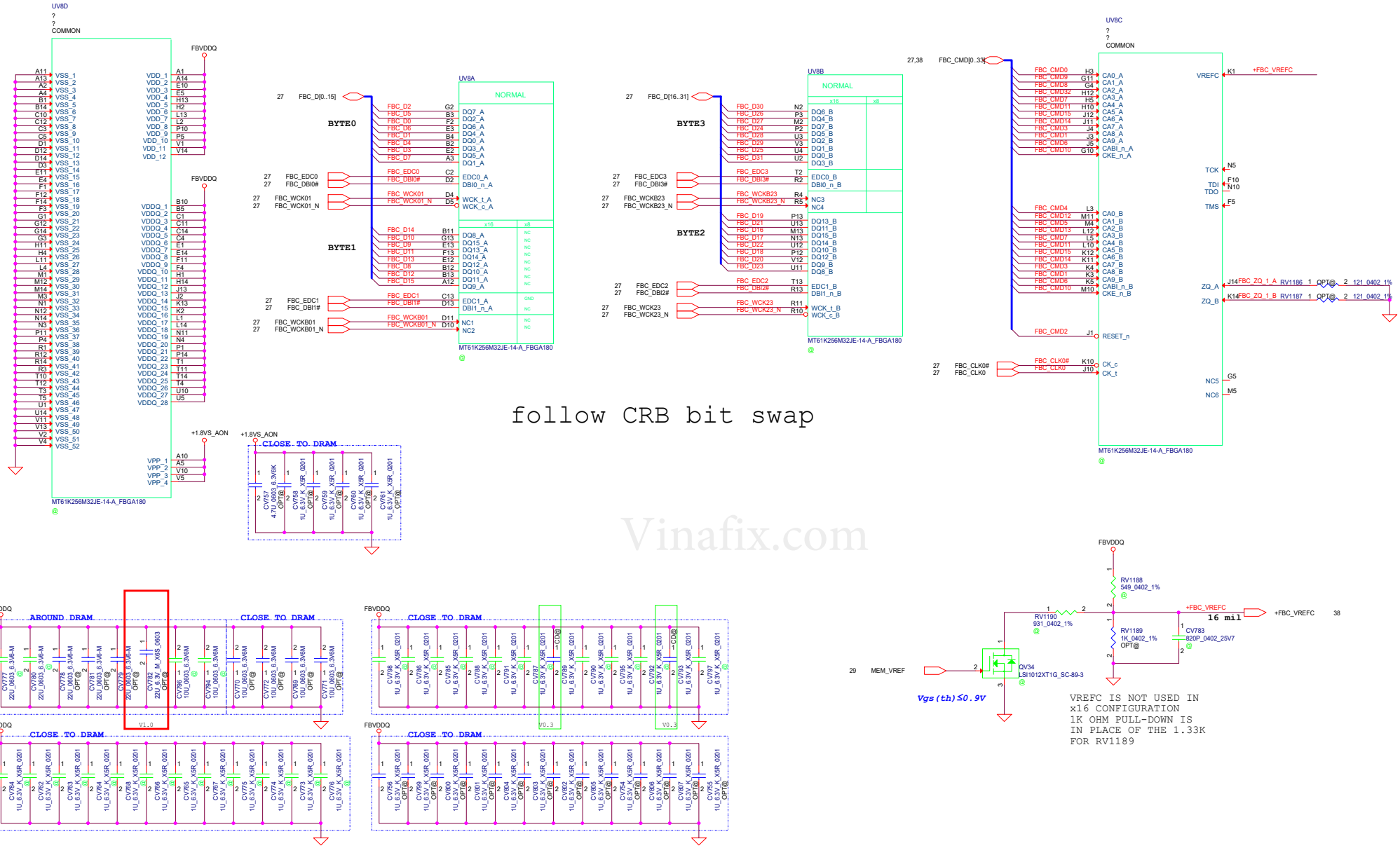

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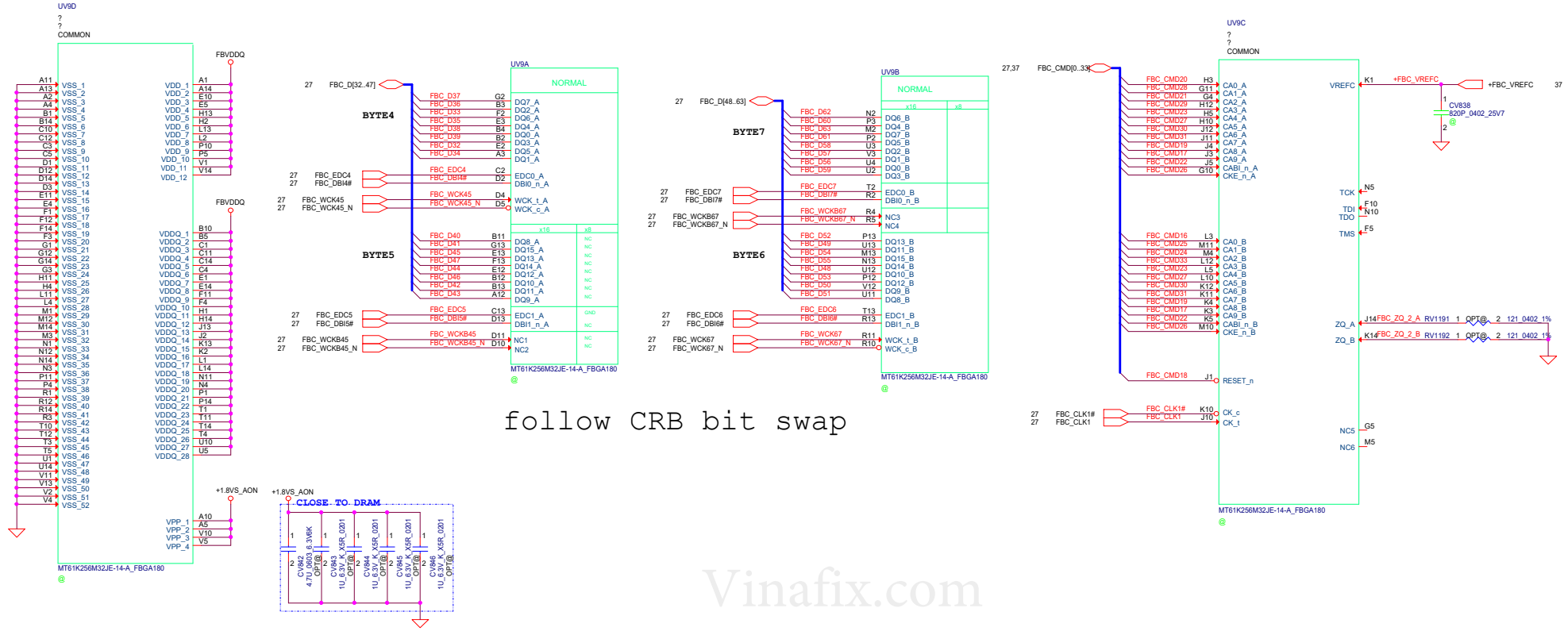
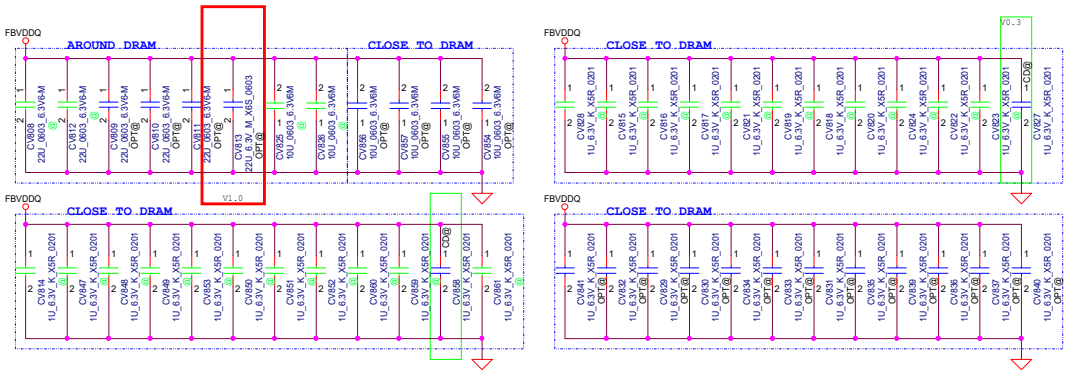
Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	N18E-G1_GDDR6_C_[31_0]		
Size C	Document Number Y540		Rev 2.0
Date: Friday, March 22, 2019	Sheet 37 of 77		





Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: *N18E-G1_GDDR6_C_[63_32]*

Size	Document Number	Rev
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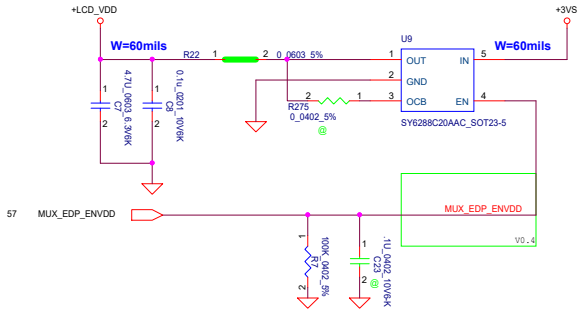
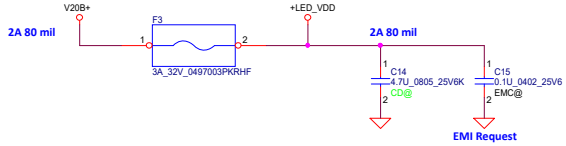
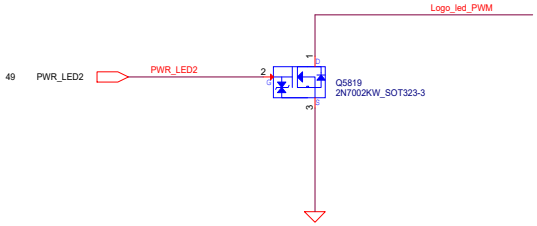
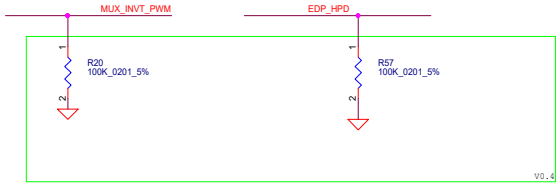
LCD POWER CIRCUIT









MKyoceraSP010020700
SiHIGHSTARSP010020800

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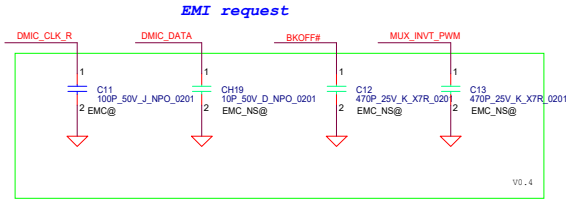

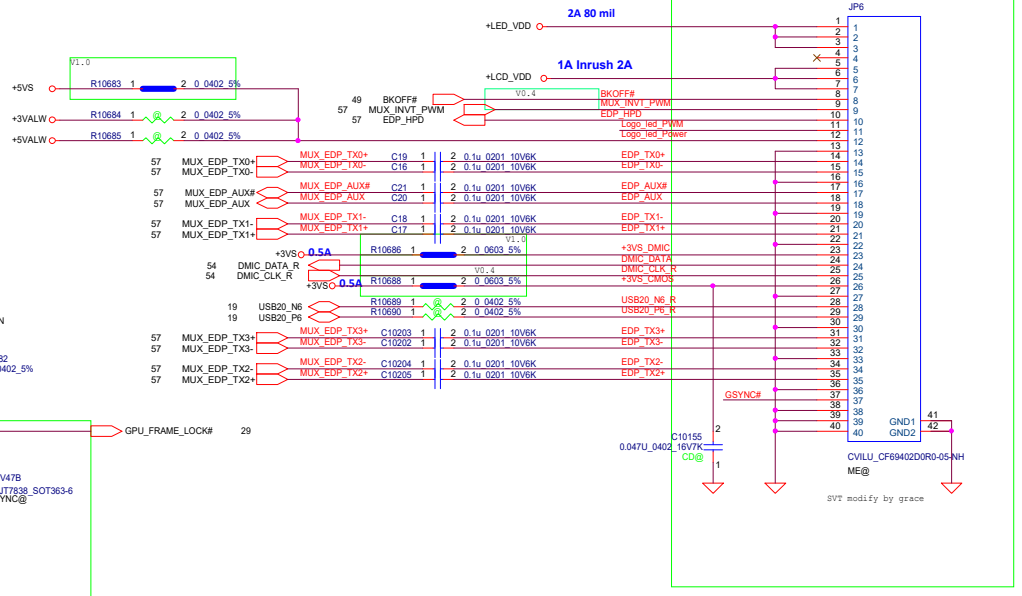

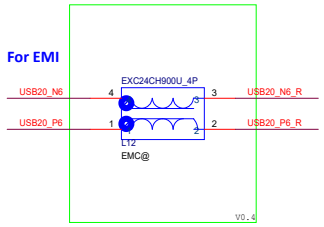

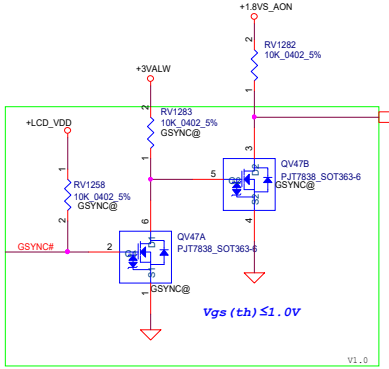

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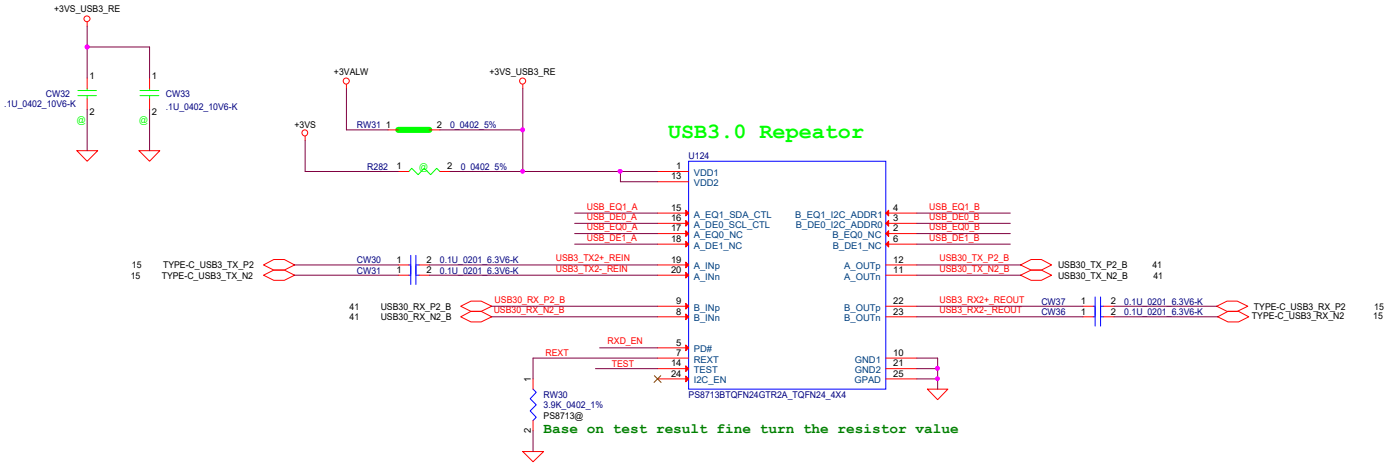
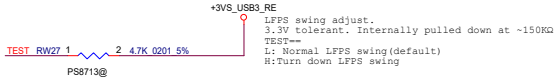
Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

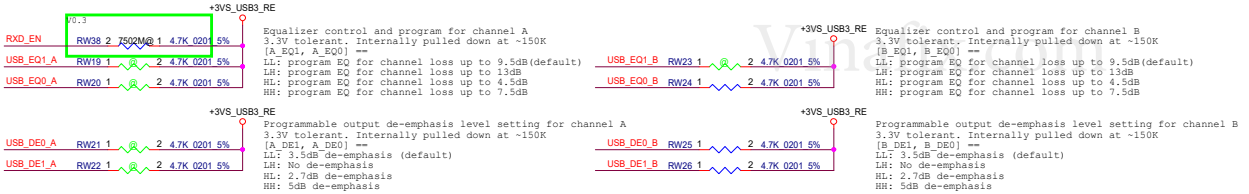
Title	eDP/ CMOS/Touch screen		
Size C	Document Number ¥540		Rev 2.0
Date: Friday, March 22, 2019	Sheet 39 of 77		

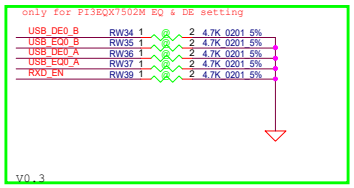




EQ & DE setting BOM structure
default setting, need fine tune

Location	PS8713BT	PI3EQX7502M
RW38	@ no need use	7502M@
RW34 RW35 RW36 RW37	@ internal pull down no need external resistance	@ default setting EQ_A/B: floating for EQ=6dB DE_A/B: floating for DE=-3.5dB need fine tune
RW30 RW27	PS8713@	@ floating without external connection
RW19 RW22 RW23 RW26	Used for EQ&DE setting base on fine tune result	@ NC pin no need use
RW20 RW21 RW24 RW25	Used for EQ&DE setting base on fine tune result	Used for EQ&DE setting base on fine tune result





Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	DDI Redriver PS8330		
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Slave Addr	Ra 1%	Rb 1%
addr0	NC	10K
addr1	54.9K	12.1K
addr2	27.4K	15.8K
addr3	18.2K	22.1K

500mA +5VALW R105 0_0603_5% VCONN_IN 500mA
Q8 LP2301ALT1G_SOT23-3 R2078 47K_0402_5%
TYPEC_GPIO9
Low HiZ

100mA +5V_IN_RTS5455 +5VALW R103 0_0603_5% 100mA +5V_IN_RTS5455
C4205 0.1U_0402_10V7K C10144 10U_0603_6.3V6M

VCONN_IN 500mA C10119 10U_0603_6.3V6M C101 1U_0402_10V6-K
+LDO_3V3 C4206 4.7U_0402_6.3V6M C10120 0.1U_0402_10V7K

+VBUS_P0 R4208 200K_0402_1% VMON R4209 10K_0402_1%

U4 RTS5455-GR_QFN46_6P5X4P5
VCONN_IN 10 5V_IN 25 LDO_3V3 26

PD Controller

Type-C Port side

Zdiff=90ohm No via
USB30_TX_N2_B 40 C4230 0.22U_0201_6.3V6-K USB3P2_TXN_C 41 SSTX_1P/2N
USB30_TX_P2_B 40 C4207 0.22U_0201_6.3V6-K USB3P2_TXP_C 42 SSTX_1N/2P
USB30_RX_N2_B 40 C10183 0.22U_0201_6.3V6-K USB3P2_RXN_C 39 SSRX_1P/2N
USB30_RX_P2_B 40 C10182 0.22U_0201_6.3V6-K USB3P2_RXP_C 40 SSRX_1N/2P

Zdiff=90ohm
GPU_SNK0_DP3P 25 C10125 0.1u_0201_10V6K TYPE-C_DP_RE_TXP3 38 DP3_1P/2P
GPU_SNK0_DP3N 25 C10127 0.1u_0201_10V6K TYPE-C_DP_RE_TXN3 37 DP3_1N/2P
GPU_SNK0_DP2P 25 C10128 0.1u_0201_10V6K TYPE-C_DP_RE_TXP2 46 DP2_1P/2P
GPU_SNK0_DP2N 25 C10126 0.1u_0201_10V6K TYPE-C_DP_RE_TXN2 45 DP2_1N/2P
GPU_SNK0_DP1P 25 C10121 0.1u_0201_10V6K TYPE-C_DP_RE_TXP1 44 DP1_1P/2P
GPU_SNK0_DP1N 25 C10124 0.1u_0201_10V6K TYPE-C_DP_RE_TXN1 43 DP1_1N/2P
GPU_SNK0_DP0P 25 C10122 0.1u_0201_10V6K TYPE-C_DP_RE_TXP0 36 DP0_1P/2P
GPU_SNK0_DP0N 25 C10123 0.1u_0201_10V6K TYPE-C_DP_RE_TXN0 35 DP0_1N/2P

+3VS 100K_0402_5% R39 Zdiff=100ohm
GPU_SNK0_AUX_DN 25 C10157 0.1U_0402_10V7K TYPE-C_DP_RE_AUXN 2 AUX_N/MGPIO5
GPU_SNK0_AUX_DP 25 C10156 0.1U_0402_10V7K TYPE-C_DP_RE_AUXP 1 AUX_P/MGPIO4
100K_0402_5% R38 TP4301 MGPIO3 6 H_DM/DCI_CLK/MGPIO3
5 H_DP/DCI_DATA/MGPIO2

+LDO_3V3 +5VALW R4210 0_0402_5% R4212 560K_0402_1% LOC_PWR_MON R4211 10K_0402_1% R4213 10K_0402_1%

42 VBUS_EN 27 I2C_EN/GPIO10
TYPEC_GPIO9 28 I2C_INT/GPIO9
42 TYPE_C_OCP# TYPE_C_OCP# R10271 0_0402_5% 29 I2C_SDA/GPIO8
TP4304 30 I2C_SCL/GPIO7
LOC_PWR_MON 23 LOC_PWR_MON
22 IMON
VMON 21 VMON

RTS5455

SM_INT/GPIO4 33 RTS5455_SM_INT RTS5455_SM_INT 14.49
SM_SDA/GPIO6 31 RTS5455_SM_SDA
SM_SCL/GPIO5 32 RTS5455_SM_CK
REXT 24
DB_CFG 20
HPD/GPIO3 34 TYPE-C_DP_RE_HPD
E_PAD 47

R4245 0_0402_5% R4244 6.2K_0402_1%

USBC_CC1_CONN C4212 220P_0402_50V7K USBC_CC2_CONN C4214 220P_0402_50V7K

SBU2/MGPIO7 4 USBC_DPAUX2_CONN USBC_DPAUX2_CONN 42
SBU1/MGPIO6 3 USBC_DPAUX1_CONN USBC_DPAUX1_CONN 42
C_DM/BB_DM 8 VBUS_DSCHG VBUS_DSCHG 42
C_DP/BB_DP 7 P4305
CC2 11 USBC_CC2_CONN USBC_CC2_CONN 42
CC1 9 USBC_CC1_CONN USBC_CC1_CONN 42

C_RX2_1N/2P 18 TYPEC_RXP2 TYPEC_RXP2 42
C_RX2_1P/2N 19 TYPEC_RXN2 TYPEC_RXN2 42
C_TX2_1N/2P 14 TYPEC_TXP2 C4220 0.1u_0201_10V6K TYPEC_C_TXP2 TYPEC_C_TXP2 42
C_TX2_1P/2N 15 TYPEC_TXN2 C4221 0.1u_0201_10V6K TYPEC_C_TXN2 TYPEC_C_TXN2 42
C_RX1_1N/2P 16 TYPEC_RXP1 TYPEC_RXP1 42
C_RX1_1P/2N 17 TYPEC_RXN1 TYPEC_RXN1 42
C_TX1_1N/2P 12 TYPEC_TXP1 C4215 0.1u_0201_10V6K TYPEC_C_TXP1 TYPEC_C_TXP1 42
C_TX1_1P/2N 13 TYPEC_TXN1 C4218 0.1u_0201_10V6K TYPEC_C_TXN1 TYPEC_C_TXN1 42

+LDO_3V3 RP2 4.7K_0404_4P2R_5%
RTS5455_SM_INT RTS5455_SM_SDA
R4350 4.7K_0402_5% RTS5455_SM_CK

+3VALW R2080 0_0402_5%
Change EC side SMbus power level HLZ SIV 0811
Address 0xAC
EC
49,58 EC_SMB_CK0 R139 0_0402_5% RTS5455_SM_CK
49,58 EC_SMB_DA0 R140 0_0402_5% RTS5455_SM_SDA
Q10A 2N7002KDWH_SOT363-6
Q10B 2N7002KDWH_SOT363-6
2N7002KDWH Vth= min 1V, max 2.5V ESD 2KV

HPD
+1.8VS_AON RRE67 10K_0402_5%
29 IFPA_HPD IFPA_HPD
to NV GPU
QRE8 MMBT3904WH_SOT323-3
RRE65 100K_0402_5% TYPE-C_DP_RE_HPD
RRE63 100K_0402_5%
15 TYPE-C_DP_HPD TYPE-C_DP_HPD RRE70 0_0402_5% TYPE-C_DP_RE_HPD
to PCH

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Title: USB TYPE-C Controller
Size: Custom | Document Number: Y540 | Rev: 2.0
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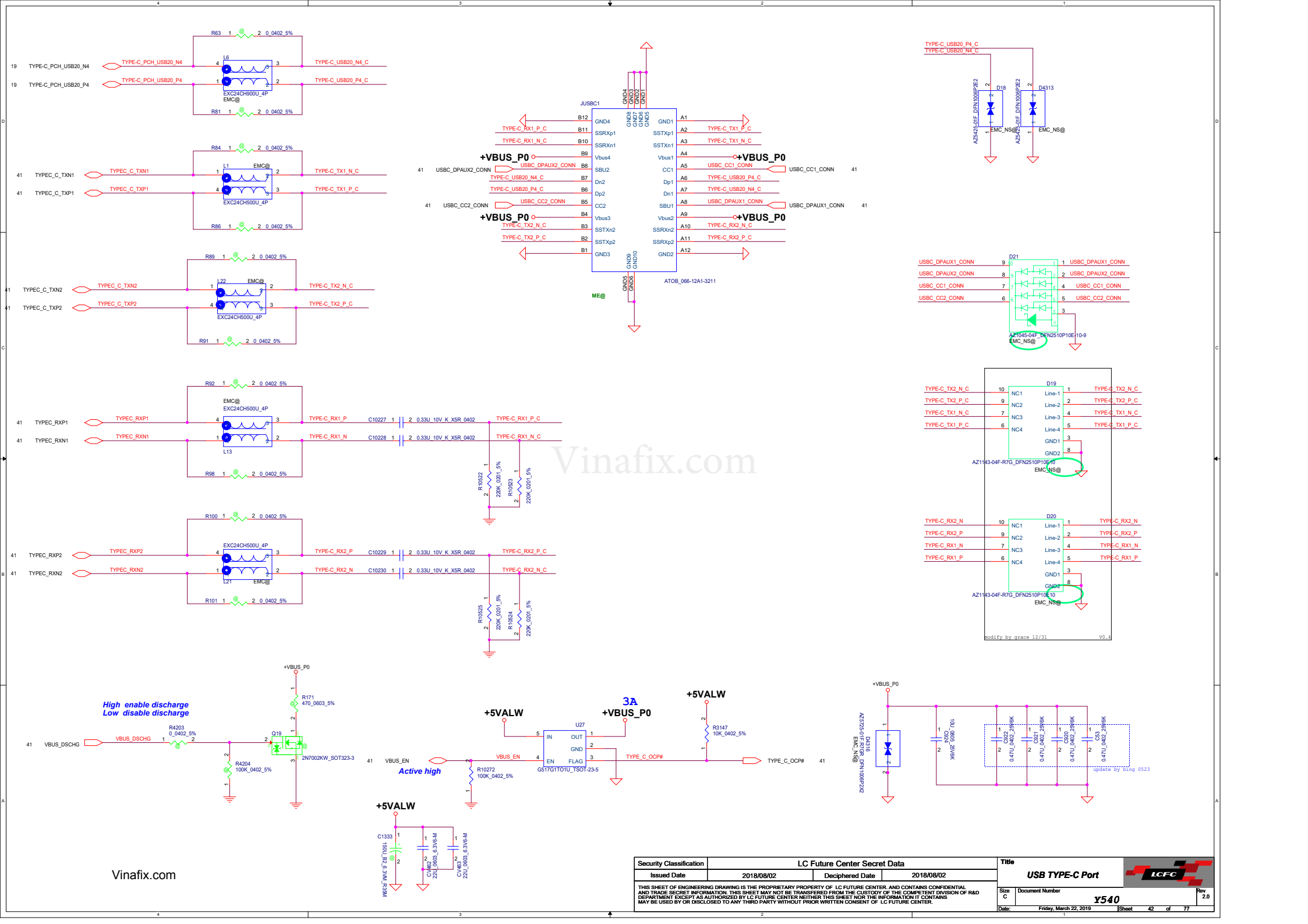

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Title: **USB TYPE-C Port**

Size	Document Number	Rev
C	Y540	2.0

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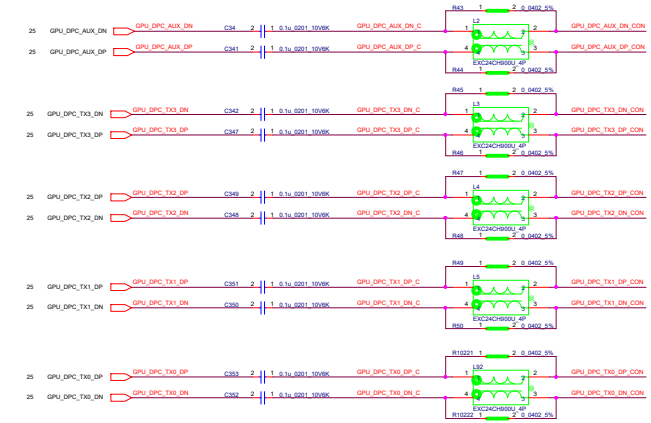
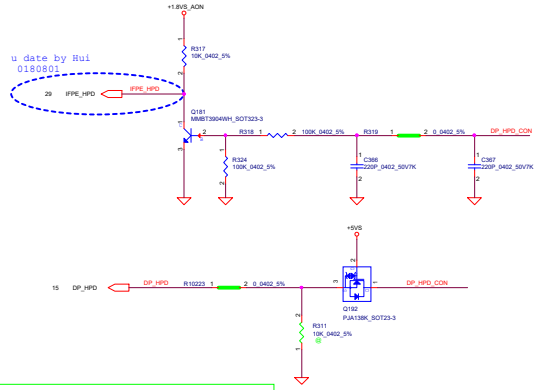
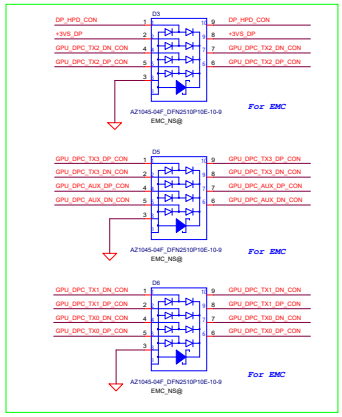
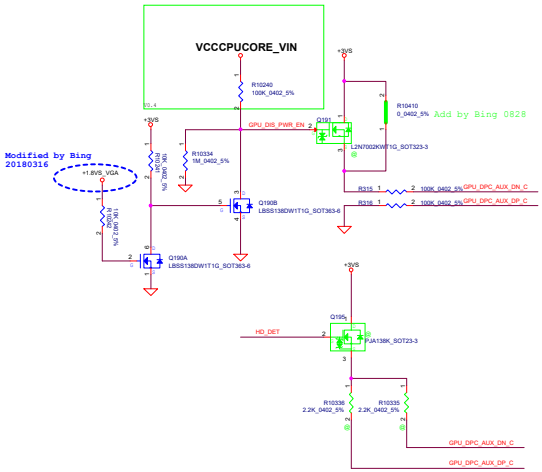
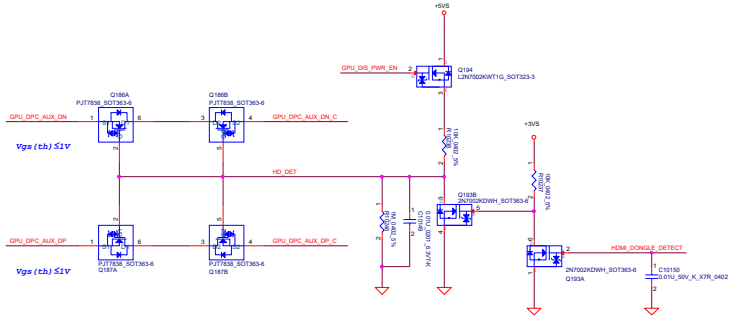
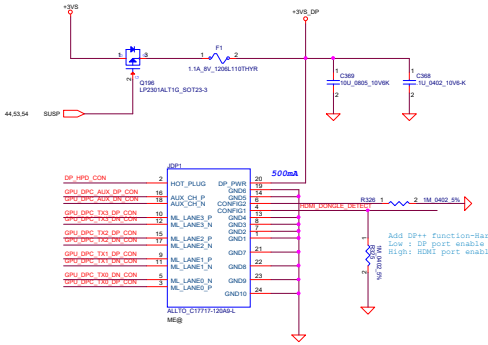






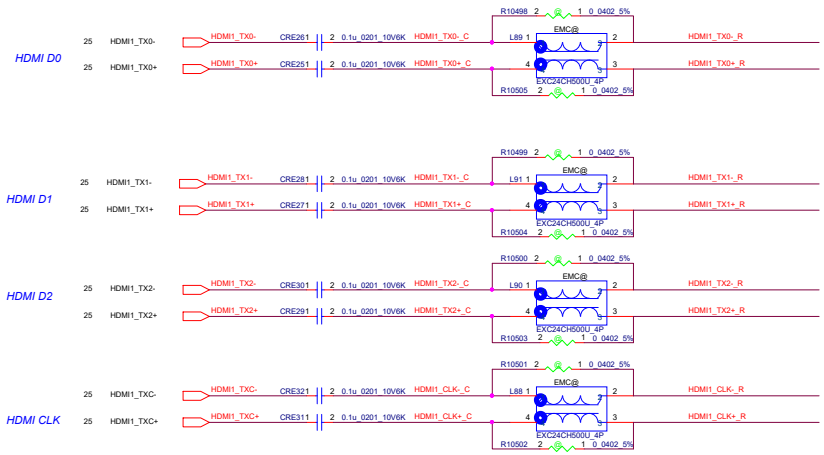


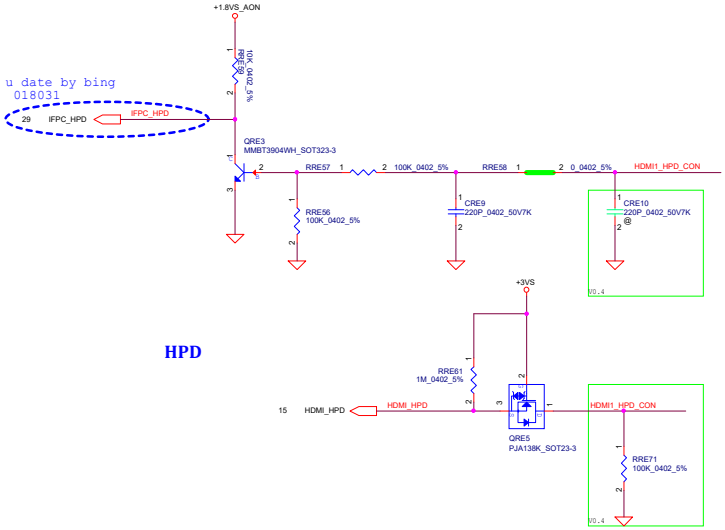


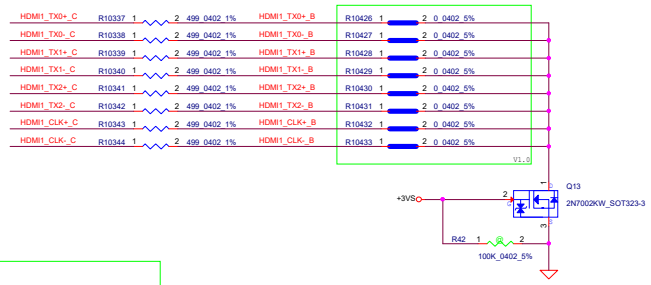


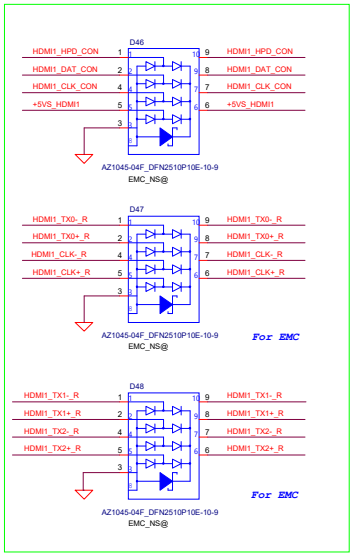
Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

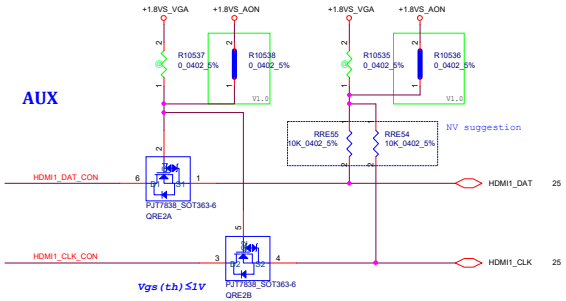
Title	DP		
Size D	Document Number Y540		Rev 2.0
Date: Friday, March 22, 2019		Sheet 43 of 77	

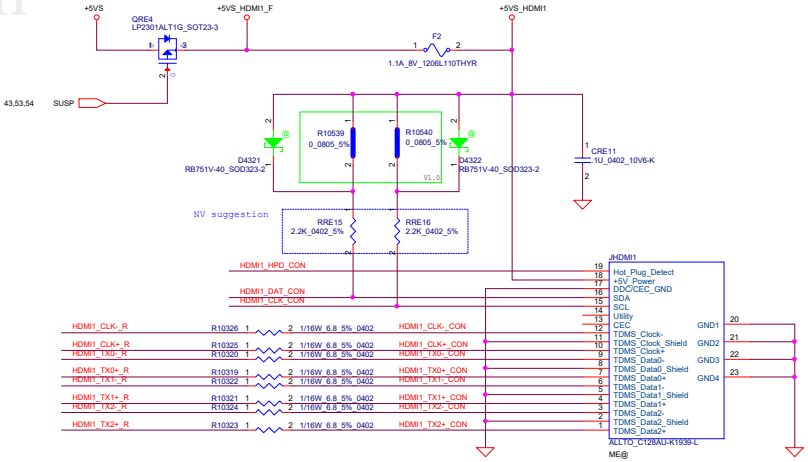












Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

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Title: HDMI_CONN

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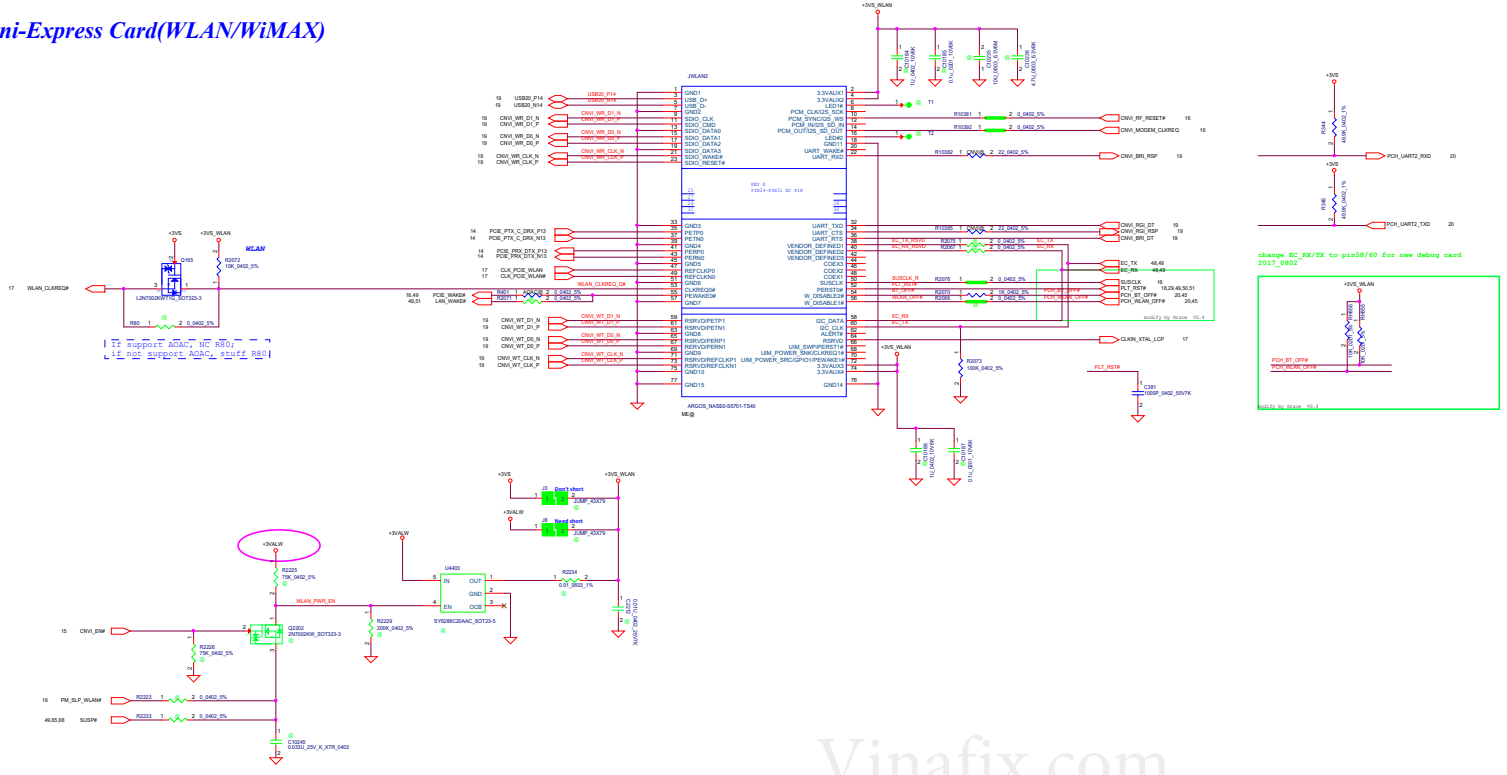
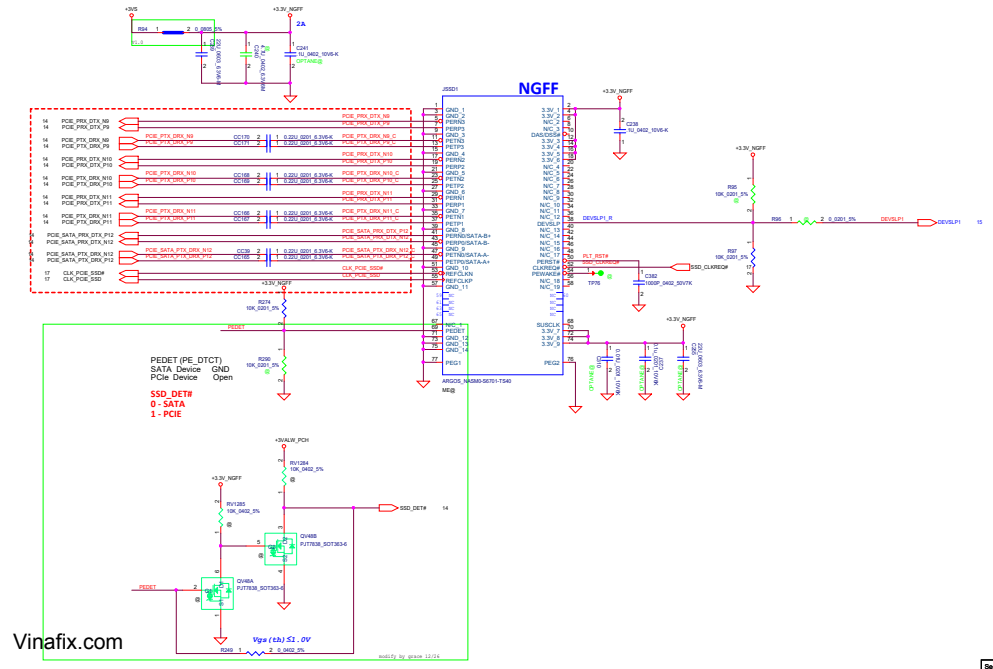
Mini-Express Card(WLAN/WiMAX)



M.2 SSD(SATA/PCIE)



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	NGFF WLAN		
Size	Document Number		Rev
Date	Y540		2.0
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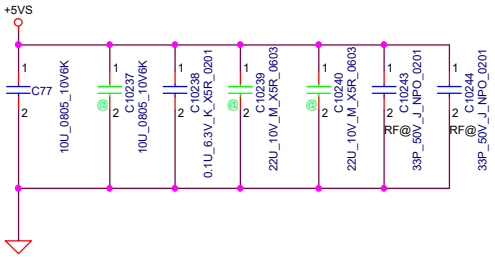
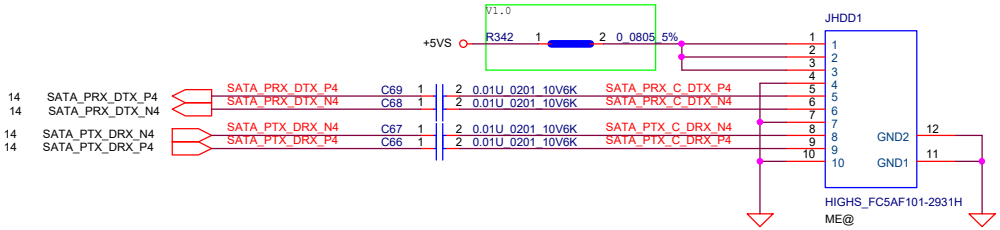
SATA HDD Conn.





Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **HDD/XBOX CONN**

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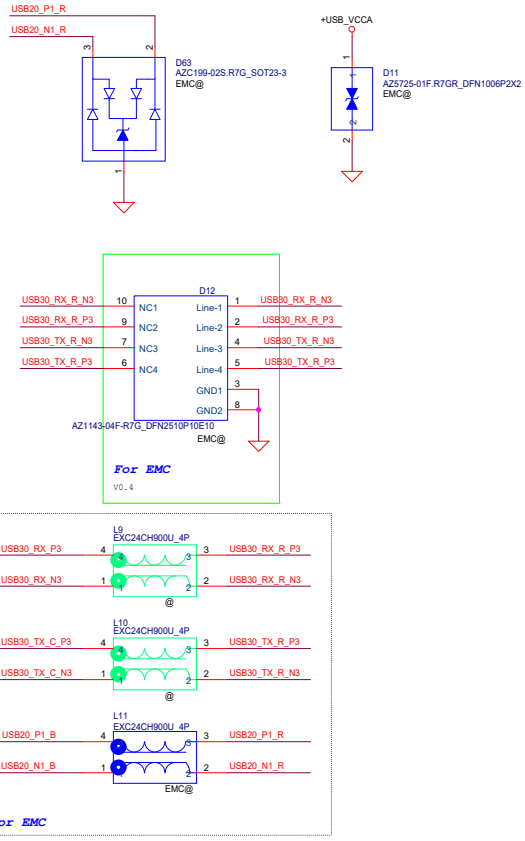
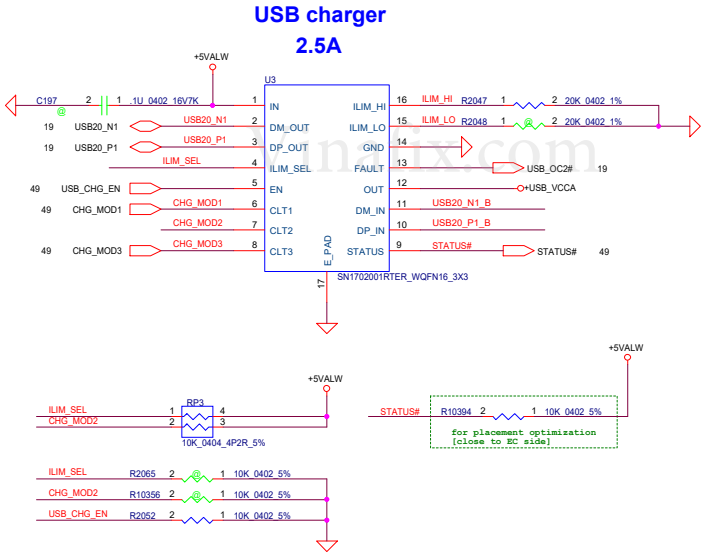
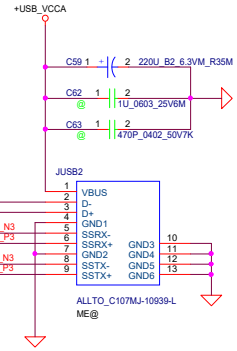






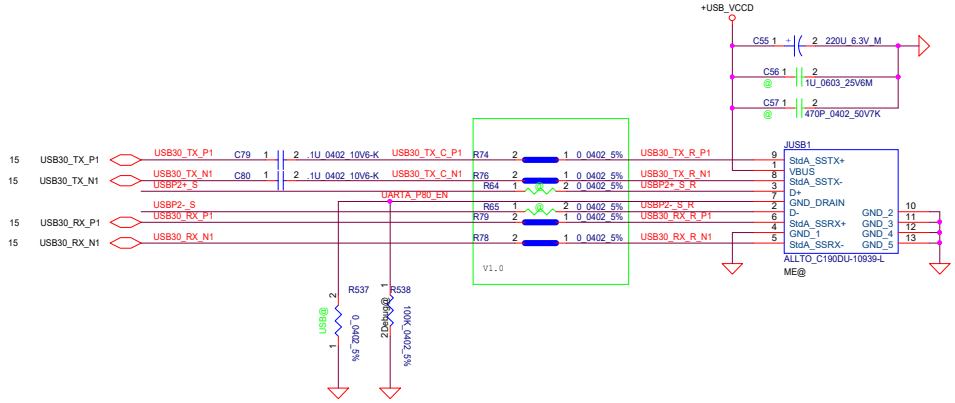
CLT1	CLT2	CLT3	ILIM_SEL	MOD	
0	0	0	X	DCH	OUT held low
1	1	1	1	CDP	Data Connected and Port Power Mgt. Function Active
1	1	1	0	SDP2	Data Connected
1	1	0	X	SDP1	Data Connected
0	1	0	X	SDP1	Data Connected
1	0	0	X	DCP_Short	Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	DCP_Divider	Device Forced to stay in DCP Divider 1 Charging Mode
0	1	1	X	DCP_Auto	Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	DCP_Auto	Data Disconnected and Power Wake Function Active

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **USB2.0/USB3.0 PORT (LEFT)**

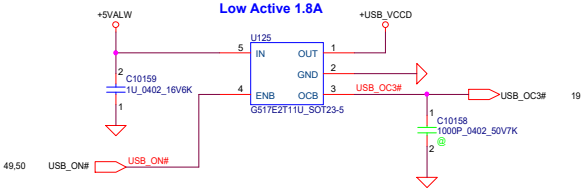
Size	Document Number	Rev
C	Y540	2.0

Date: Friday, March 22, 2019 | Sheet 47 of 77

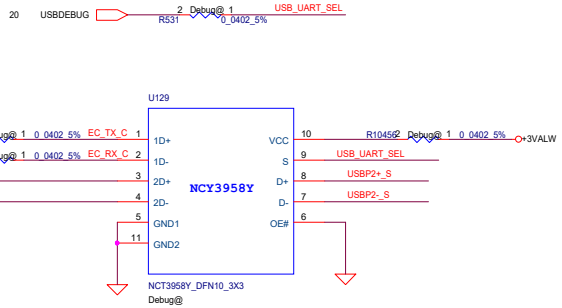


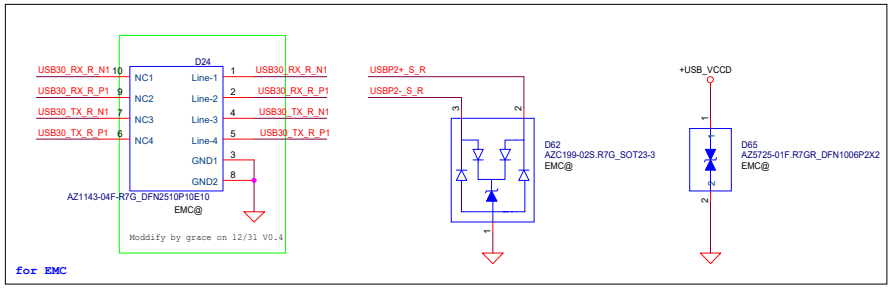
USB3.1 PORT x1

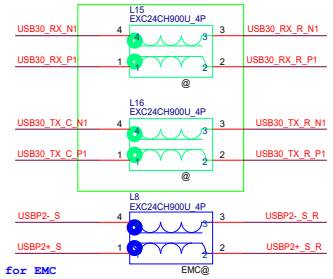
Low Active 1.8A



For USB Debug Function



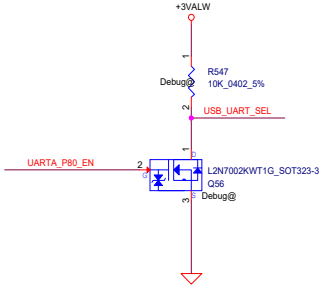




USBDEBUG	Kernel debug
Set input	Set input
Set output Low	ENABLE

UARTA_P80_EN	POST 80
Set input	DISABLE
Set output Low	ENABLE

OE#	S	FUNCTION
H	X	DISABLE
L	L	D(+/-) to 1D(+/-)
L	H	D(+/-) to 2D(+/-)

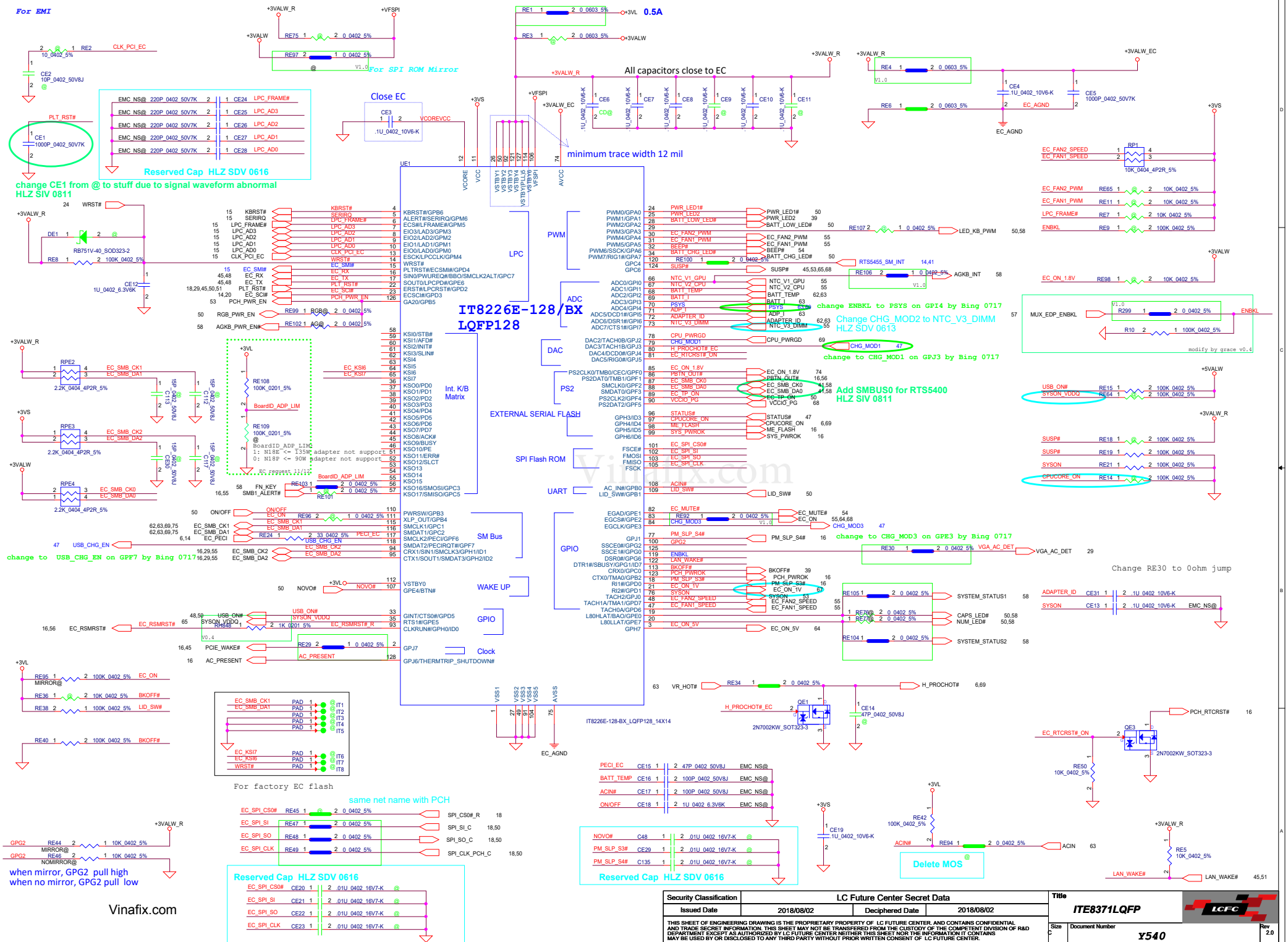


Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **USB2.0**

Size	Document Number	Rev
C	Y540	2.0

Date: Friday, March 22, 2019 Sheet 48 of 77



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

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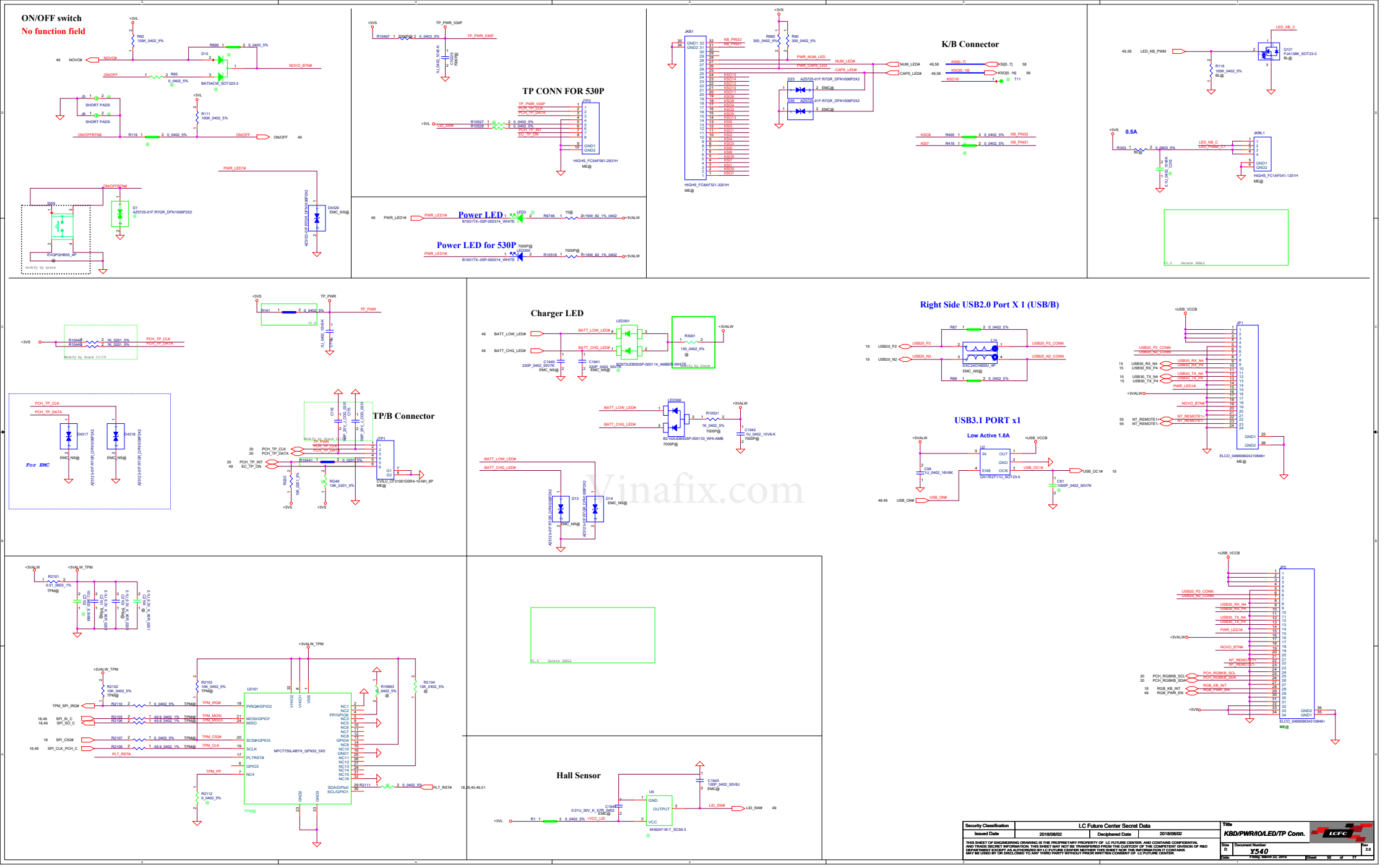
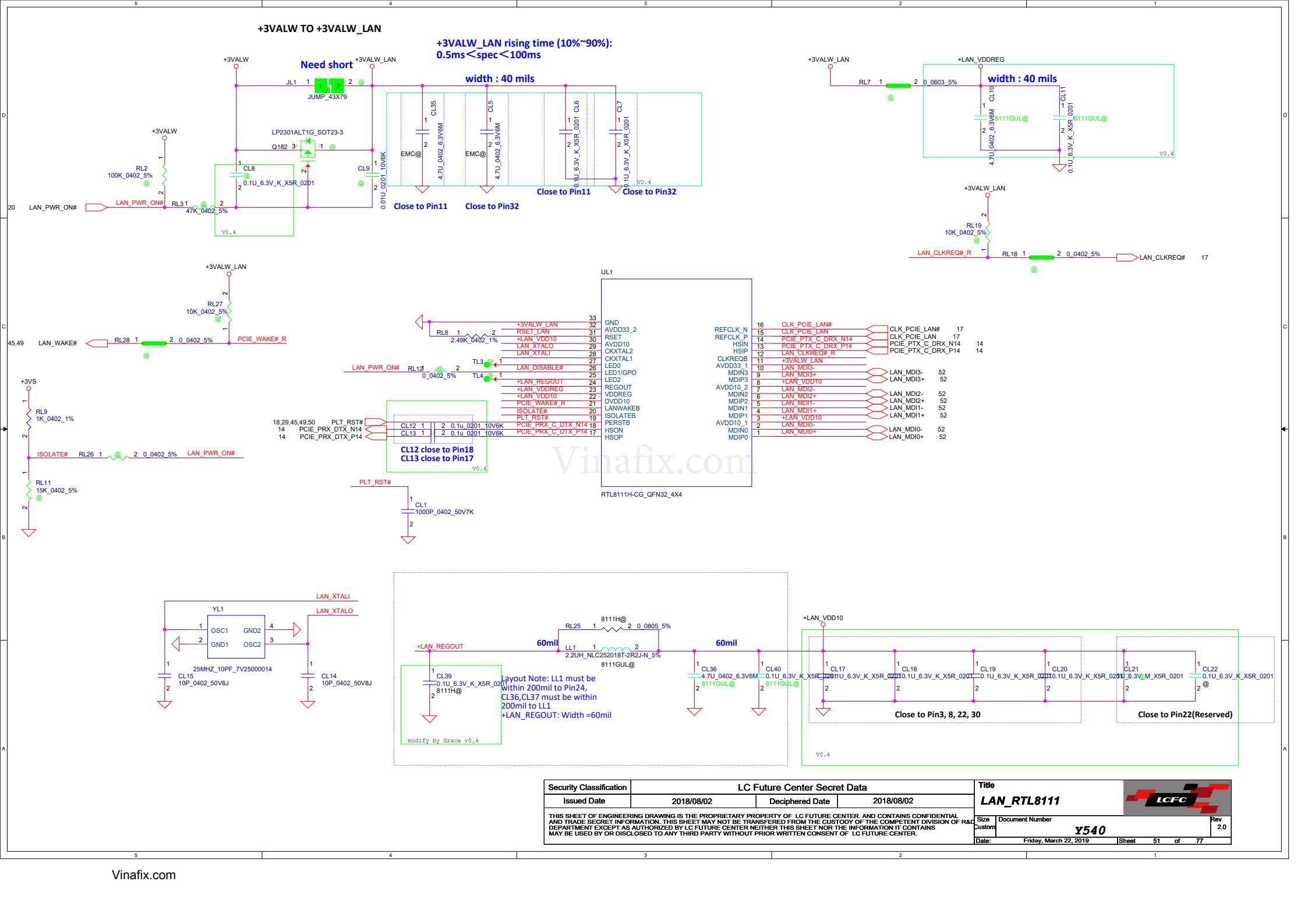
Title: ITE8371LQFP

Size	Document Number	Rev
C	Y540	2.0

Date: Friday, March 22, 2019 Sheet 49 of 77


ON/OFF switch
No function field
TP CONN FOR 530P
K/B Connector
Power LED
Power LED for 530P
Charger LED
TP/B Connector
Right Side USB2.0 Port X 1 (USB/B)
USB3.1 PORT x1
Low Active 1.8A
Hall Sensor
Vinafix.com



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	LAN_RTL8111		
Size	Custom	Document Number	Y540
Rev	2.0		
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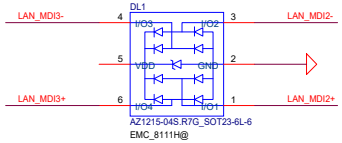
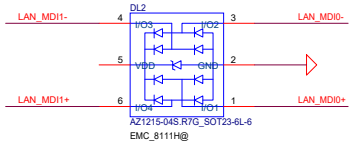
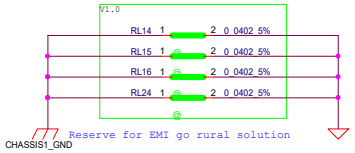
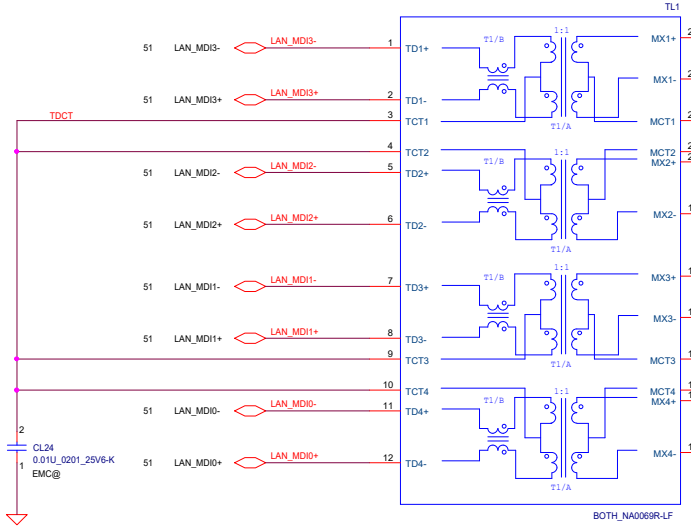
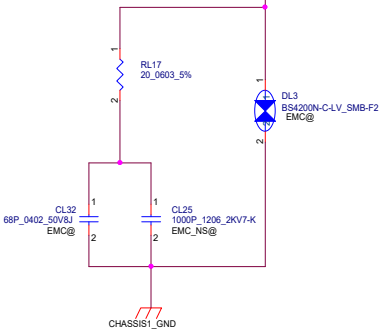
DL1/DL2
1'S PN:SC300005900
Place Close to TL1

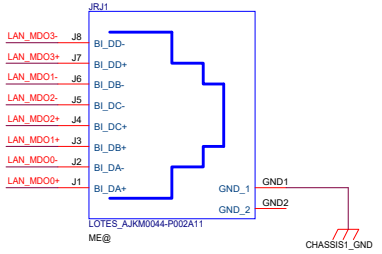






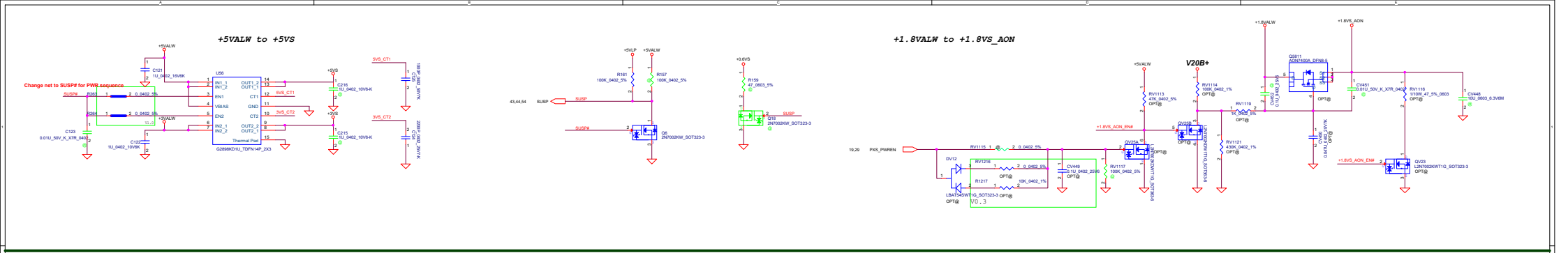


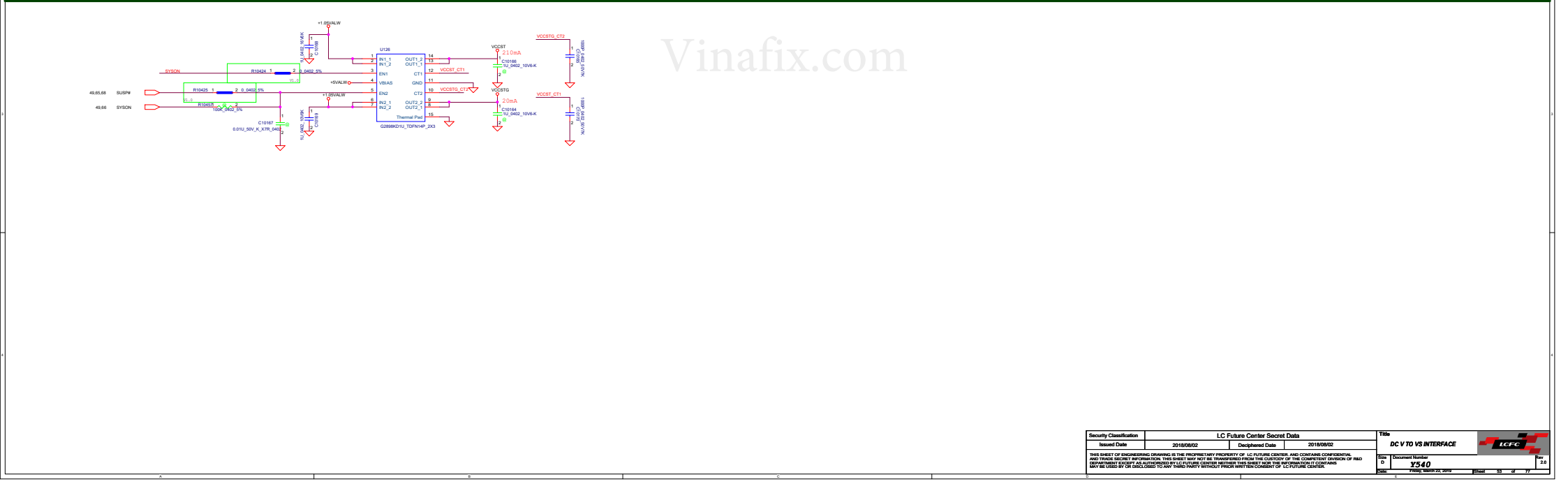




Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	LAN_Transformer		
Size	Document Number		Rev
C	Y540		2.0
Date:	Friday, March 22, 2019	Sheet	52 of 77





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Issued Date	2018/08/02	Deciphered Date	2018/08/02

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Title	DC V TO VS INTERFACE	
Size D	Document Number Y540	Rev 2.0
Date: Friday, March 22, 2019	Sheet 53 of 77	

Digital power for HDA link

Close to Pin18

Digital power for digital I/O circuit

Analog power for DACs, ADCs

Analog power for mixers, & IO ports

CA200,CA201,CA203 close to PIN40

Power supply for full-bridge left/Right channel

HP/MIC Jack

FOR ESD

Close to Connector

Place Close To Codec

For EMI

PC-BEEP

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

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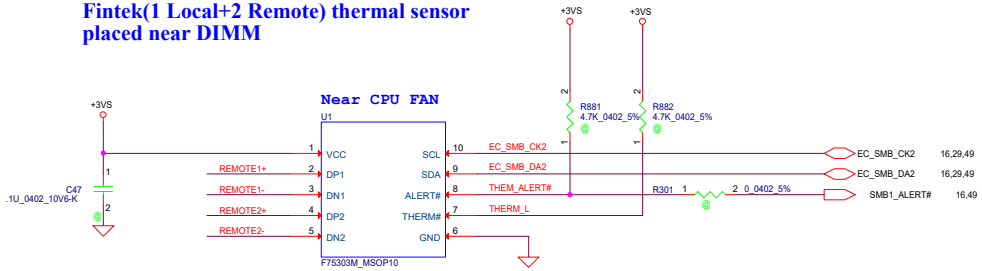
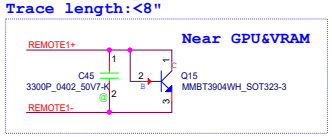
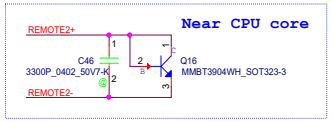
Title	Codec_CX20752
Size	D
Document Number	X540
Rev	2.0
Date	Friday, March 22, 2019
Sheet	54 of 77

Fintek(1 Local+2 Remote) thermal sensor placed near DIMM

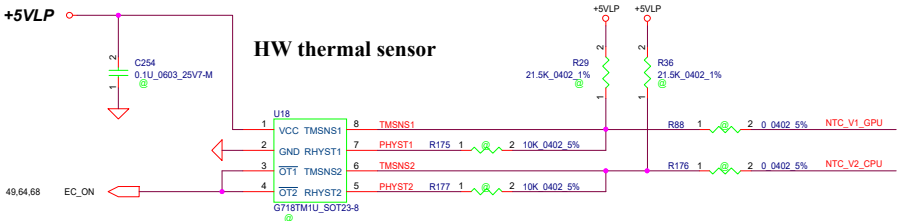


REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

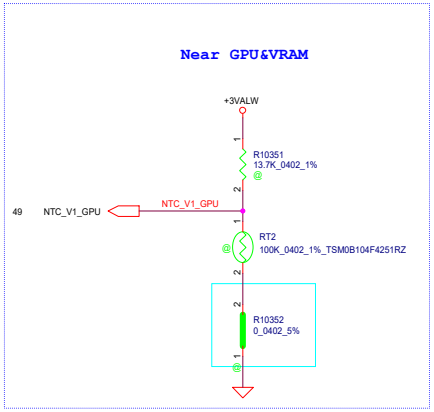


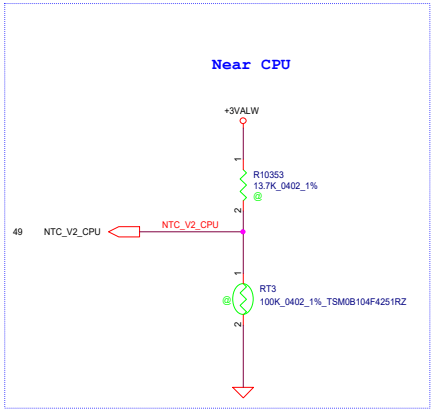


HW thermal sensor



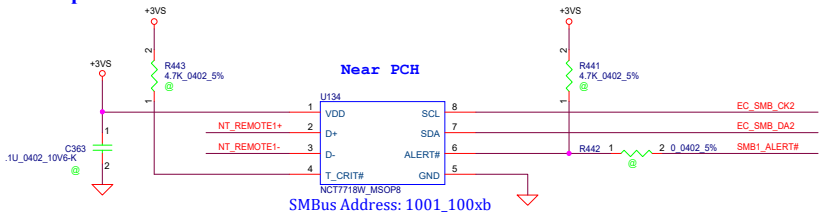
over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML)/(3*RTML-RSET)
56+/-30C



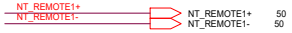


for layout optimized, change the EC_AGND to GND

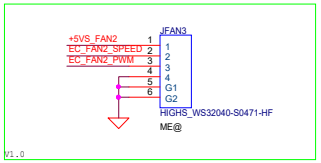
Nuvoton(1 Local+1 Remote) thermal sensor placed near TBD

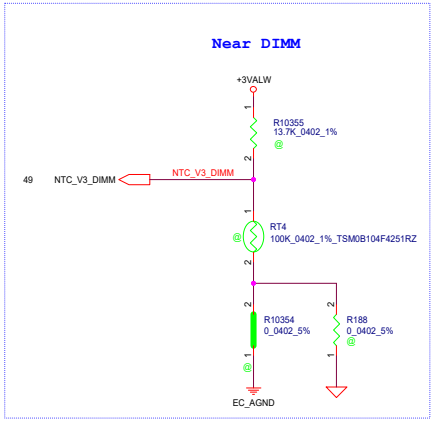


SMBus Address: 1001_100xb



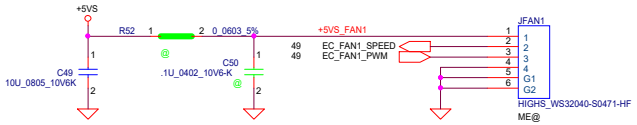
Thermal Diode Near GPU FAN(DB)
NT_REMOTE1+/-:
Trace width/space:10/10 mil
Trace length:<8"

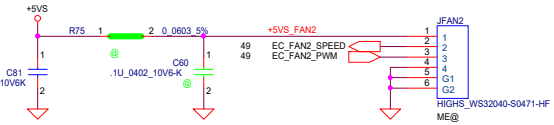




FAN Conn

Address 1001_101xb





Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	Thermal sensor/FAN CONN		
Size C	Document Number Y540		Rev 2.0
Date: Friday, March 22, 2019	Sheet 55 of 77		

TABLE : CPU ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R597	NO ASM	ASM	NO ASM
R9907	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9909	NO ASM	ASM	ASM
R9910	NO ASM	ASM	ASM
R9916	NO ASM	ASM	ASM
R99	NO ASM	ASM	ASM
R9912	NO ASM	ASM	ASM
R9934	NO ASM	ASM	ASM
R9930	NO ASM	ASM	ASM
R9931	NO ASM	ASM	ASM
R9932	NO ASM	ASM	ASM
R9933	NO ASM	ASM	ASM

LOGIC

TABLE : PCH ITP DEBUG REPORT

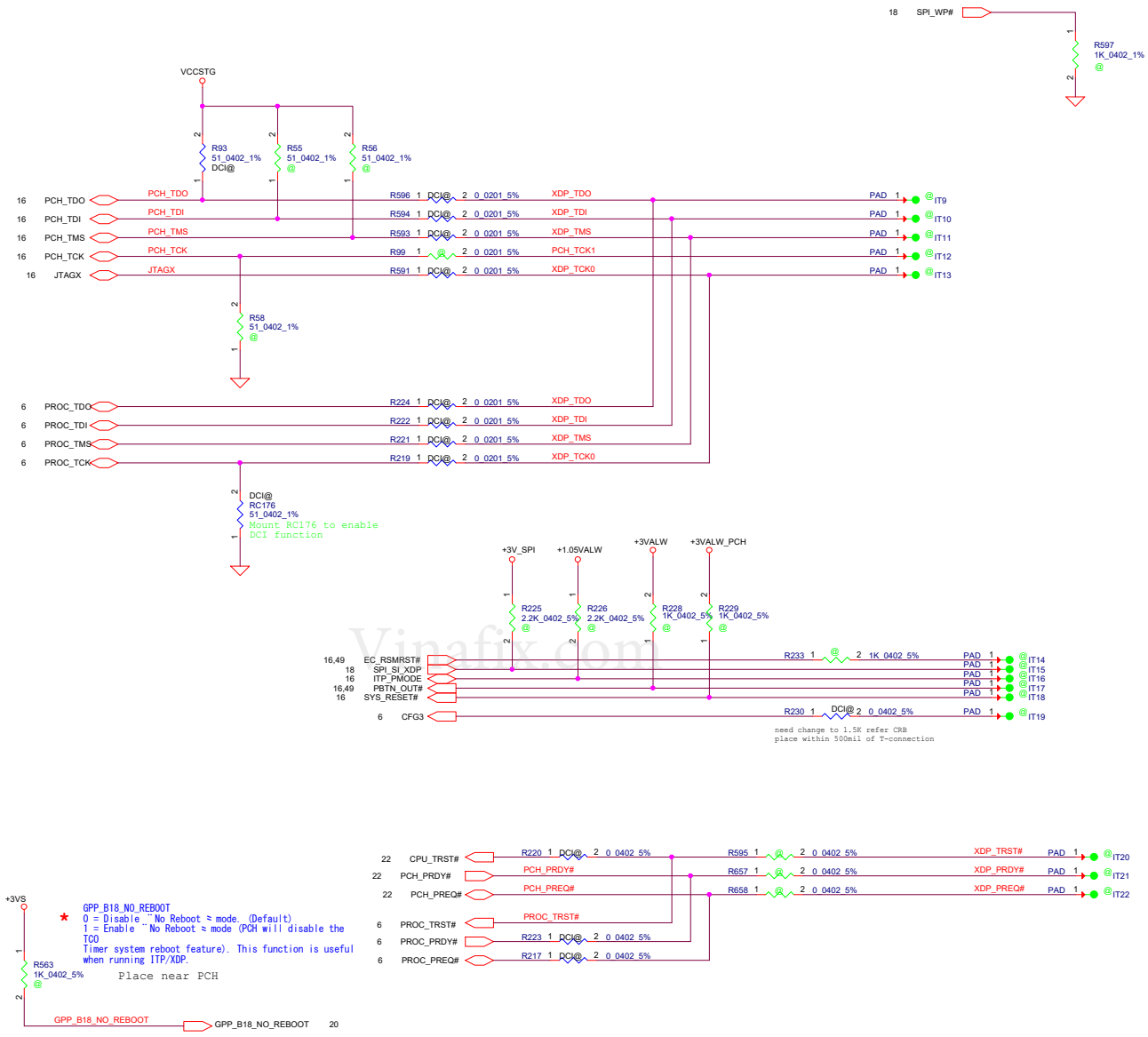
	No use	Individual Port	DCI 2.0 w/o connector
R93	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
R9917	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9908	NO ASM	ASM	NO ASM
R9911	NO ASM	ASM	NO ASM
R9913	NO ASM	ASM	NO ASM
R9915	NO ASM	ASM	NO ASM

LOGIC

TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)		R563
HIGH	Enable "No Reboot" Mode	ASM
LOW	Disable "No Reboot" Mode (Default)	NO ASM

LOGIC

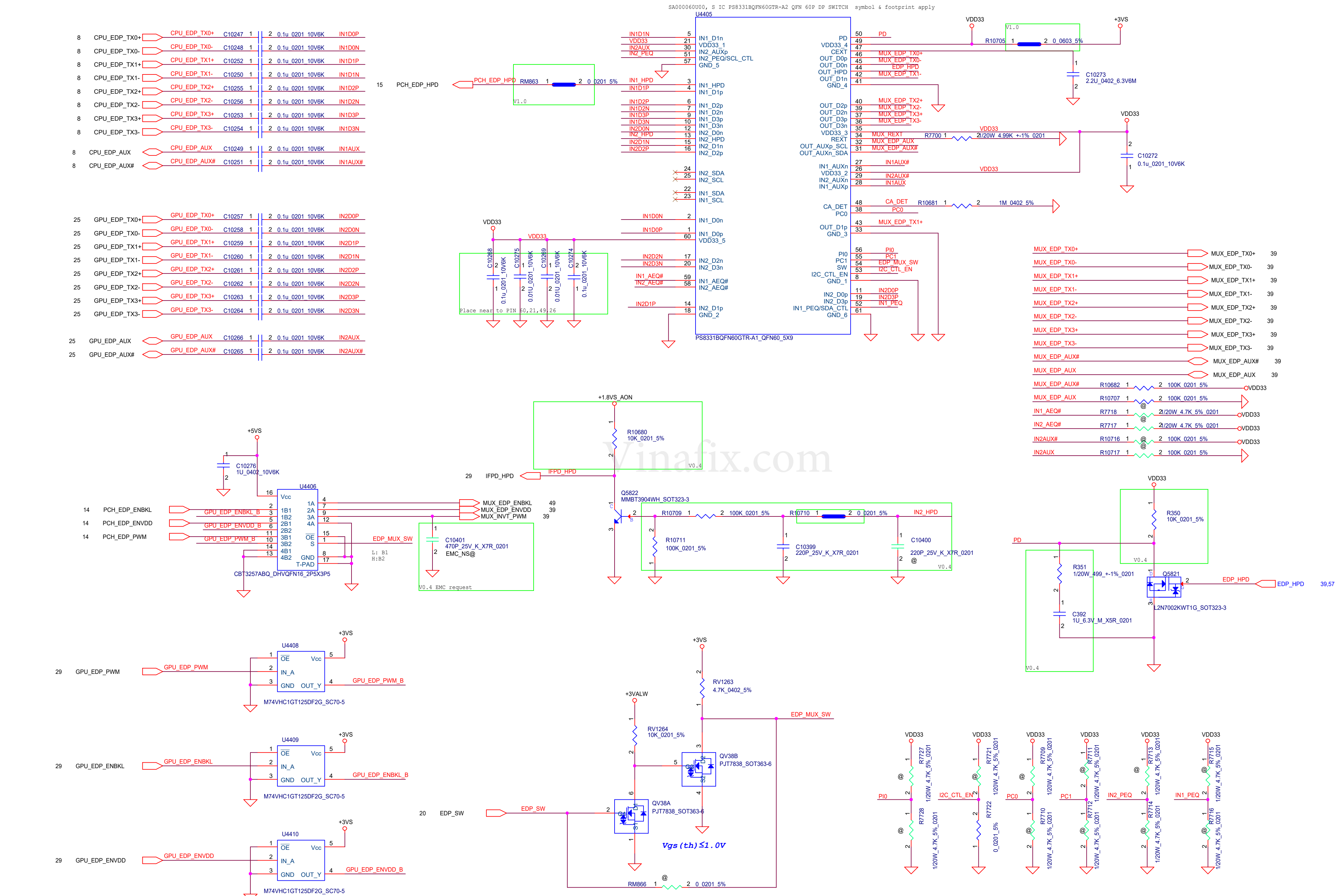


Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: XDP

Size: Custom | Document Number: Y540 | Rev: 2.0

Date: Friday, March 22, 2019 | Sheet 56 of 77



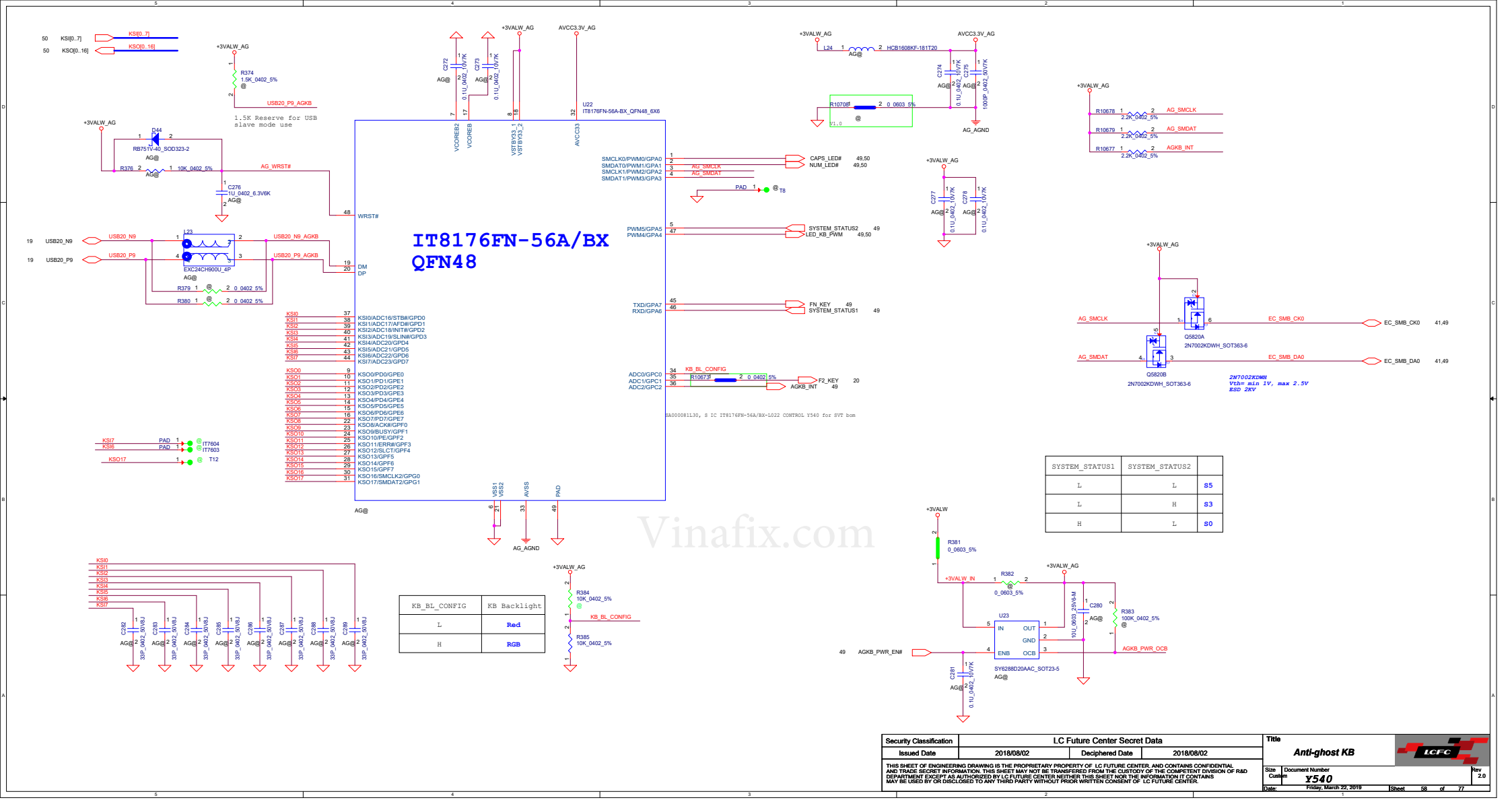
Vinafix.com

EDP_SW :Port switching configuration; Internal pull down at ~150KΩ, 3.3V I/O.
L: Input Port1 is selected (default)
H: Input Port2 is selected

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **EDP MUX**

Size: C | Document Number: Y540 | Rev: 2.0



SYSTEM_STATUS1	SYSTEM_STATUS2	
L	L	S5
L	H	S3
H	L	S0

KB_BL_CONFIG	KB Backlight
L	Red
H	RGB

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **Anti-ghost KB**

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HDMI Logo

ZZZ1 HDMI@

HDMI Logo
RO00000040J

PCB MB

ZZZ2

PCB FY515 NM-C221 NS-C225/C226/C227
DAZ1DG00101

GPU

UV1

S IC N18E-G1-KD-A1 BGA 2228 GPU, A.2
SA00009QU00
N18EG1@

UV1

S IC N18E-G0-A1 BGA 2228 GPU 12 !
SA00009V300
N18EG0@

CPU

UC1 i5@

S IC CL8068404121905 SRF6X U0 2.4G BGA 1440 12C
SA0000A0P10

UC1 i7@

S IC CL8068404100301 QQLT P0 2.4G BGA
SA0000A0N10

UC1 i9@

SA00009PG00

PCH

UH1

S IC FH82HM370 SR40B B0 BGA 874P PCH 12!
SA00009AG00

Samsung 6GB VRAM

ZZZ4 S6GX6@

SAMSUNG_6GB_VRAM
X7646K12001

Micron 6GB VRAM

ZZZ5 M6GX6@

MICRON_6GB_VRAM
X7646K12002

SW5 15@

SW EVQPQHB55
SN100006P00

D1 15@

AZ5725-01F
SC400008K00

U5 15@

AH9247-W-7
SA00007RN00

LED2 15@

B1931TX--05P-000314
SC50000DA00

LED301 15@

B2972UDBS05P-000114
SC50000FR00

LED301 17@

B2972UDBS05P-000114
SC50000FR00

SW5 7000P@

SW EVQPQHB55
SN100006P00

D1 7000P@

AZ5725-01F
SC400008K00

U5 7000P@

AH9247-W-7
SA00007RN00

R3001 15@

150_0402_5%
SD02815008J

R3001 17@

150_0402_5%
SD02815008J

modify by Grace

SKU ID

RH157 15@

S RES 1/20W 10K +-5% 0201
SD04310028J

RH158 15@

S RES 1/20W 10K +-5% 0201
SD04310028J

RH153 N18EG1@

10K_0201_5%
SD04310028J

RH195 N18EG1@

10K_0201_5%
SD04310028J

RH157 7000P@

S RES 1/20W 10K +-5% 0201
SD04310028J

RH155 7000P@

S RES 1/20W 10K +-5% 0201
SD04310028J

RH159 N18EG0@

10K_0201_5%
SD04310028J

RH163 N18EG0@

10K_0201_5%
SD04310028J

RH152 17@

S RES 1/20W 10K +-5% 0201
SD04310028J

RH158 17@

S RES 1/20W 10K +-5% 0201
SD04310028J

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	Virtual symbol		
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H1 HOLEA — PAD_CT8P0B6P0D2P3
H3 HOLEA — PAD_CT8P0D2P5
H5 HOLEA — PAD_CT8P0B6P0D2P3
NH6 HOLEA — PAD_C5P0D5P0N
H7 HOLEA — PAD_ST8P0CB6P0D2P3

H8 HOLEA — PAD_ST8P0D2P5
H9 HOLEA — PAD_ST8P0D2P5 — CHASSIS1_GND
H10 HOLEA — PAD_ST8P0CB8P0D2P5
NH11 HOLEA — PAD_O2P5X3P1D2P5X3P1N
H12 HOLEA — PAD_ST8P0D2P5
H13 HOLEA — PAD_ST8P0D2P5
H14 HOLEA — PAD_CB6P0D2P3

H15 HOLEA — PAD_CT5P5D3P2
H16 HOLEA — PAD_CT5P5D3P2
H17 HOLEA — PAD_CT5P5D3P0
H18 HOLEA — PAD_CT5P5D3P0
H19 HOLEA — PAD_CT5P5D3P2
H20 HOLEA — PAD_CT5P5D3P2
H21 HOLEA — PAD_CT5P5D3P2
H22 HOLEA — PAD_C8P0D4P5
NH23 HOLEA — PAD_C2P5D2P5N
NH24 HOLEA — PAD_O2P5X3P1D2P5X3P1N

H23 HOLEA — PAD_CT8P0D2P5
H24 HOLEA — PAD_CT8P0D2P5

add by Bing 04/08

SH9 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P
SH10 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P
SH11 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P
SH12 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P
SH13 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P
SH14 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P
SH15 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P
SH16 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P
SH17 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P

SO-DIMM Shielding

FD1 FD2 FD3 FD4 FD5 FD6

FD7

V1.0

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **Blank**

Size	Document Number	Rev
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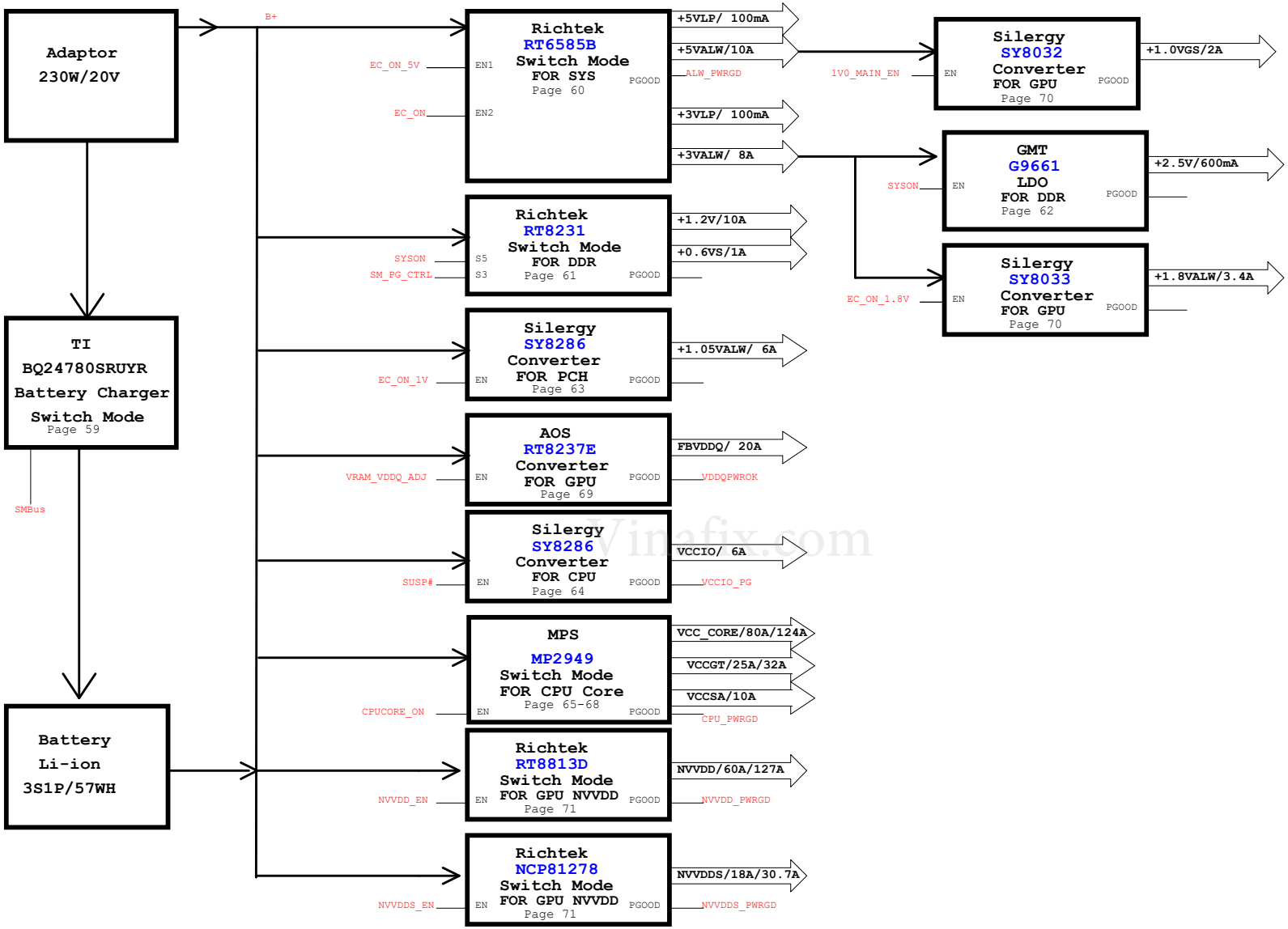

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **Power Diagram**

Size: Custom	Document Number: Y540	Rev: 2.0
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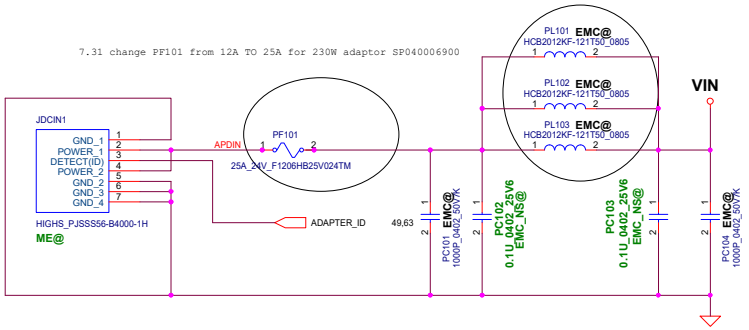

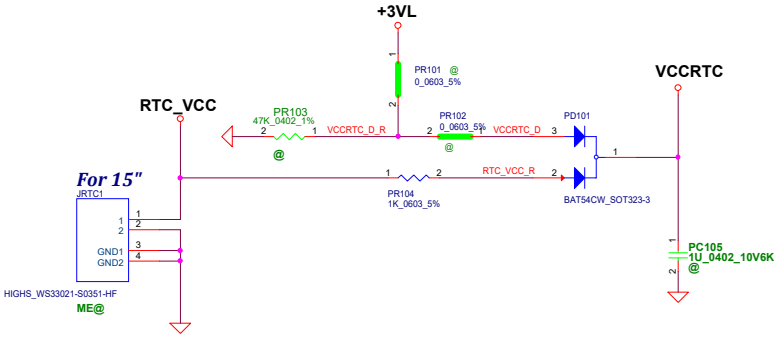

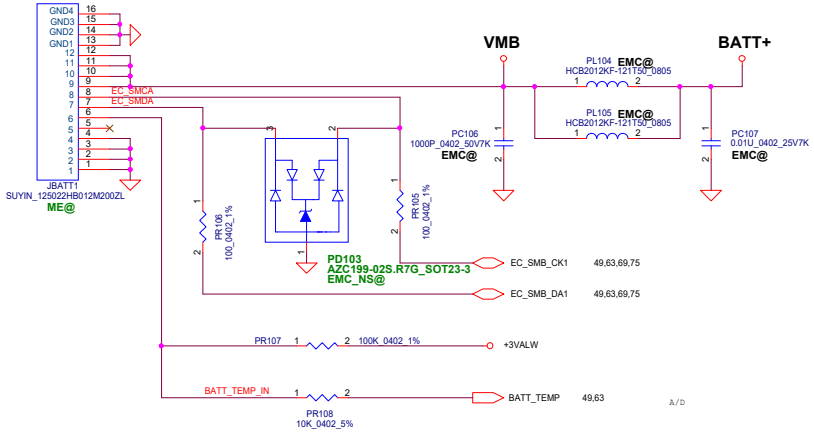

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	PWR-DCIN/BATT/RTC		
Size	Document Number	Y540	Rev 2.0
C			
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7.31 change PQ201 from AON6636 to PSMN2R0-30YLE for 230W adaptor

7.31 change PQ202 from AON6414 to AON6324 for 230W adaptor

7.31 change PR201 from 10mohm to 5mohm for 230W adaptor

8.1 add 10mohm resistor for power test

IchargeLIM=7A
IDischargeLIM=10A

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

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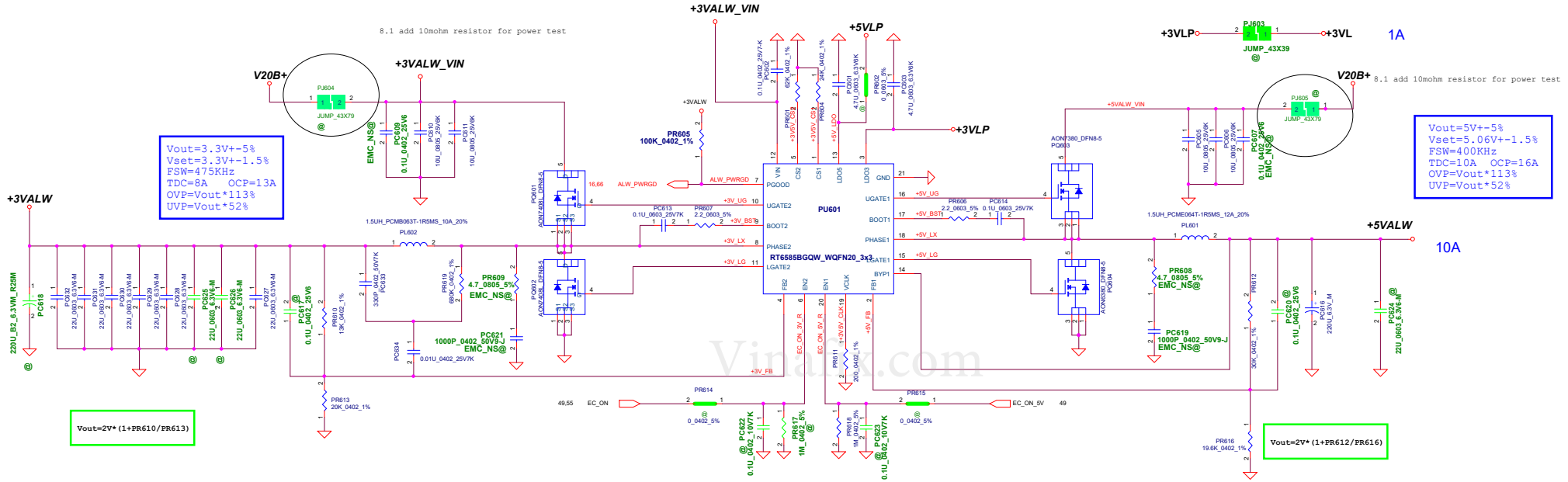
Title	PWR-charger		
Size	Custom	Document Number	Y540
Rev	2.0		
Date:	Friday, March 22, 2019	Sheet	63 of 77



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

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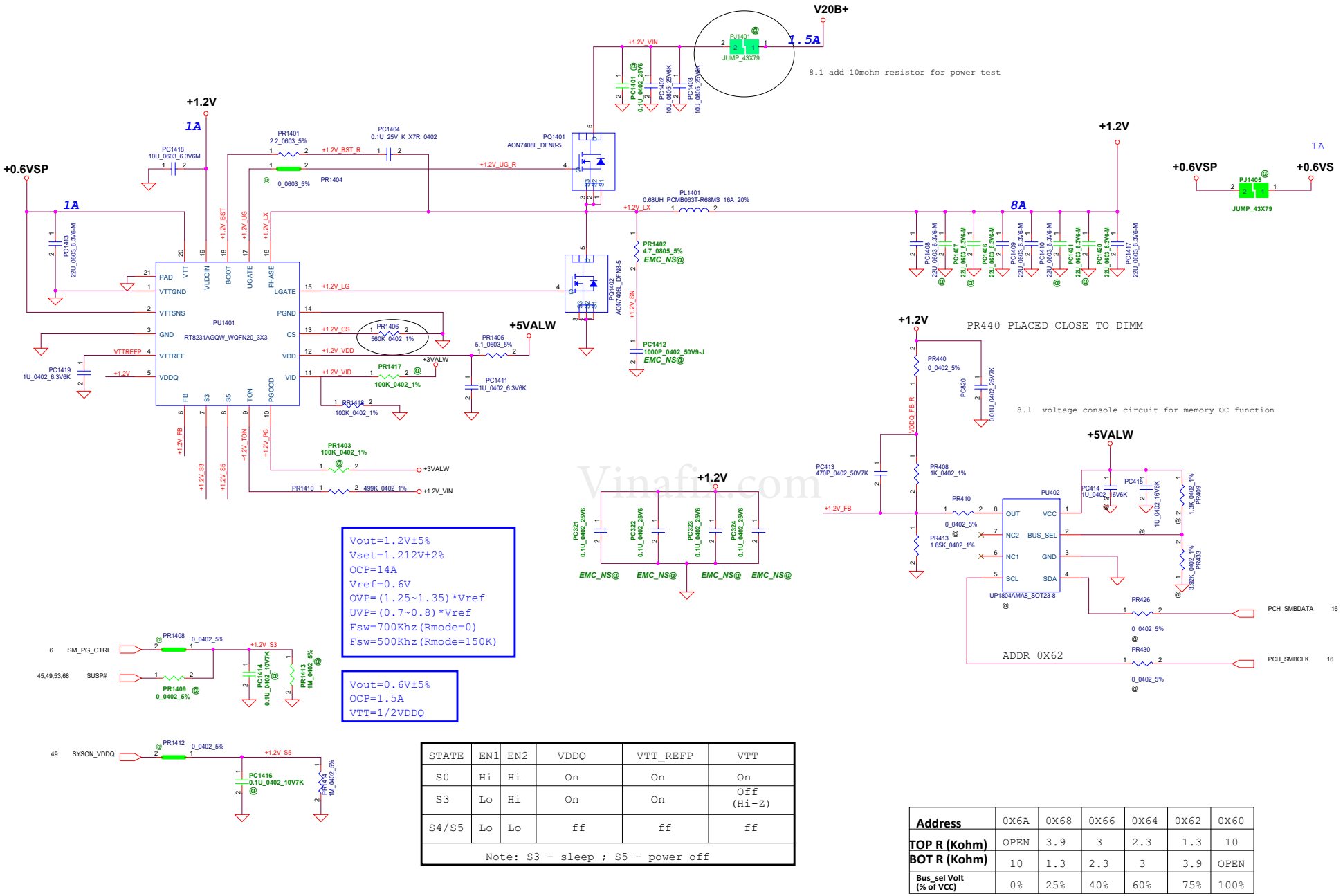
Title	PWR-3/5VALW		
Size: A3	Document Number: Y540		Rev: 2.0
Date: Friday, March 22, 2019	Sheet 64 of 77		



STATE	EN1	EN2	VDDQ	VTT_REFP	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	ff	ff	ff

Note: S3 - sleep ; S5 - power off

Address	0X6A	0X68	0X66	0X64	0X62	0X60
TOP R (Kohm)	OPEN	3.9	3	2.3	1.3	10
BOT R (Kohm)	10	1.3	2.3	3	3.9	OPEN
Bus_sel Volt (% of VCC)	0%	25%	40%	60%	75%	100%

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: PWR-VDDQ/VTT

Size: C | Document Number: Y540 | Rev: 2.0

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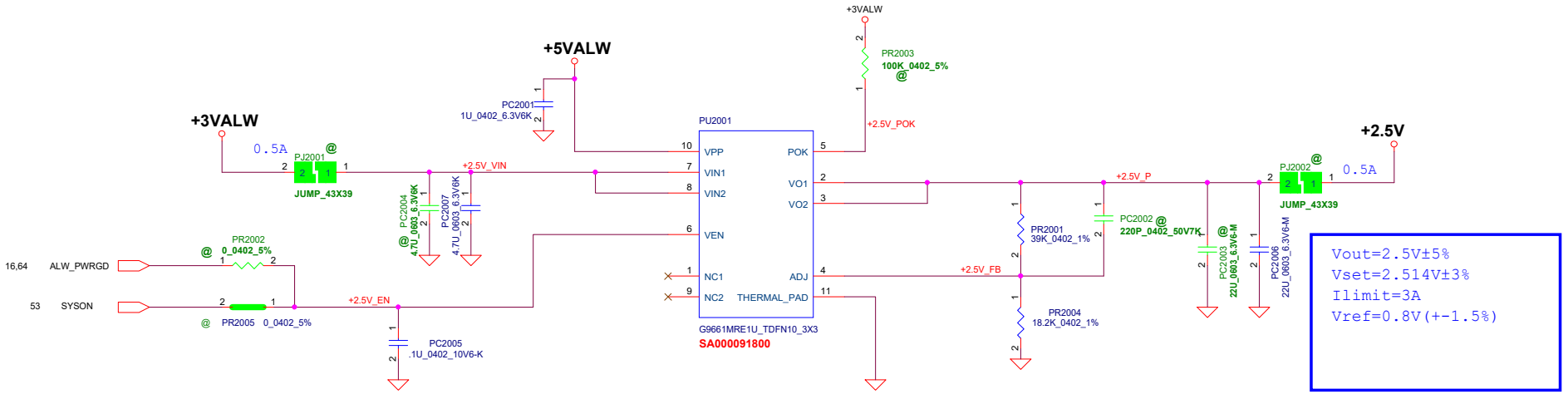

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **PWR-2.5V**

Size: Custom	Document Number: Y540	Rev: 2.0
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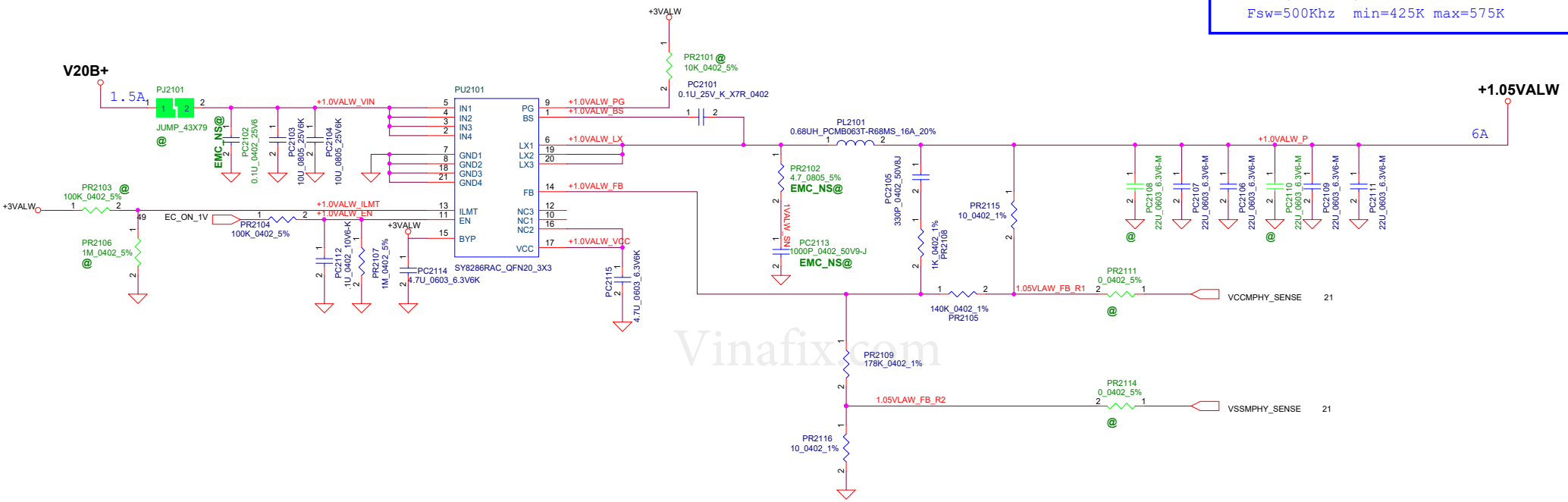

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	PWR-1.0VALW		
Size	Document Number	Y540	Rev
Custom			2.0
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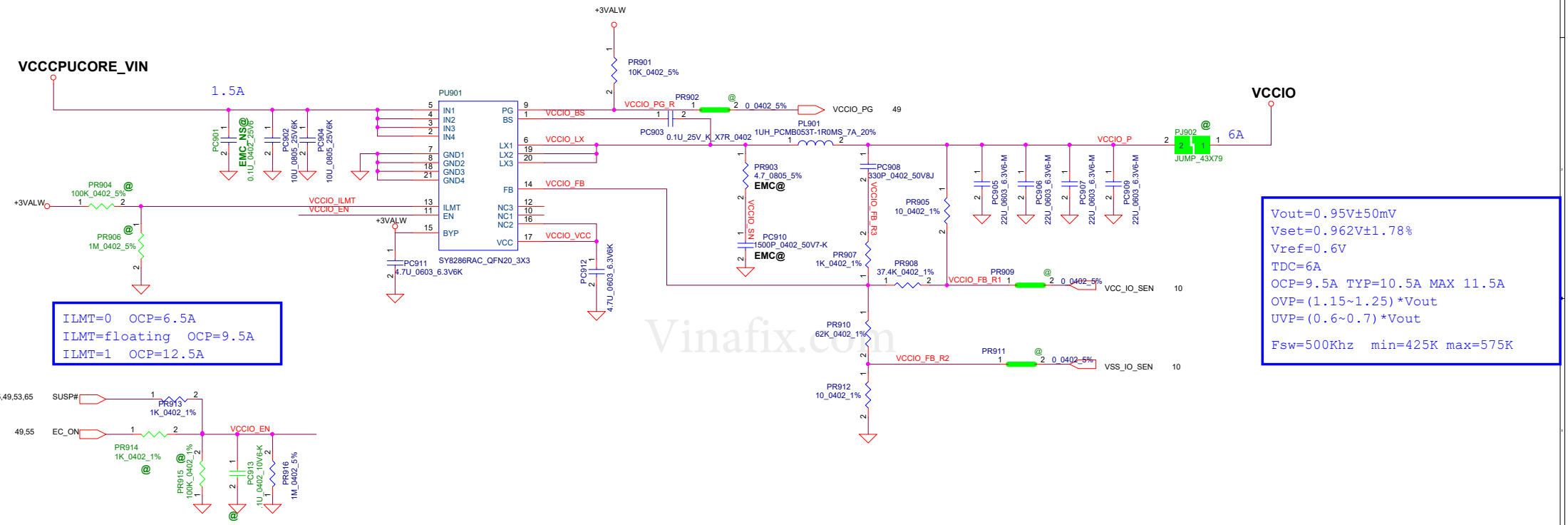
VCCIO 20VB+ change to Core VIN for layout



Vout=0.95V±50mV
Vset=0.962V±1.78%
Vref=0.6V
TDC=6A
OCP=9.5A TYP=10.5A MAX 11.5A
OVP=(1.15~1.25)*Vout
UVP=(0.6~0.7)*Vout

Fsw=500Khz min=425K max=575K

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: PWR-VCCIO

Size: Custom	Document Number: Y540		Rev: 2.0
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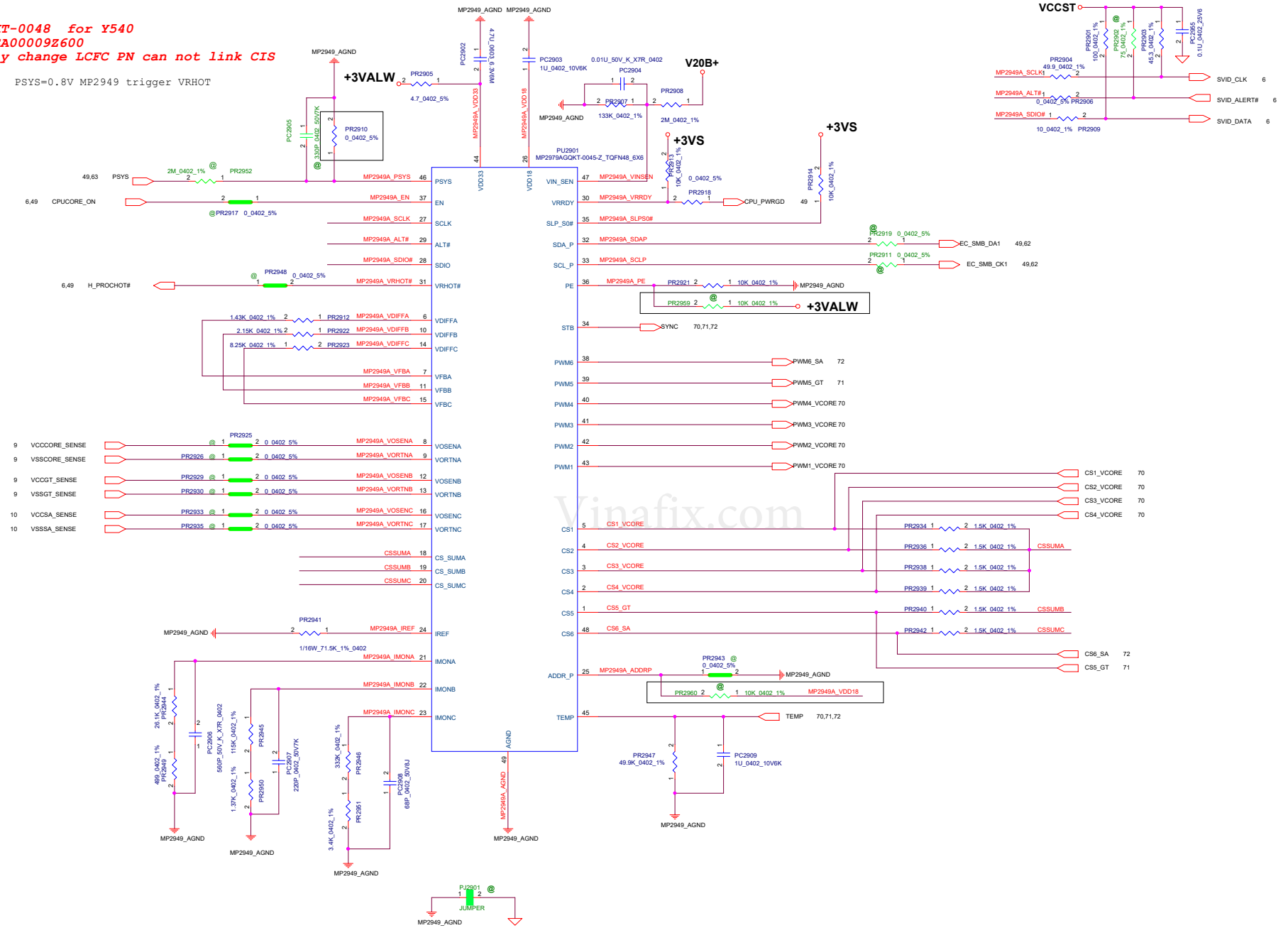
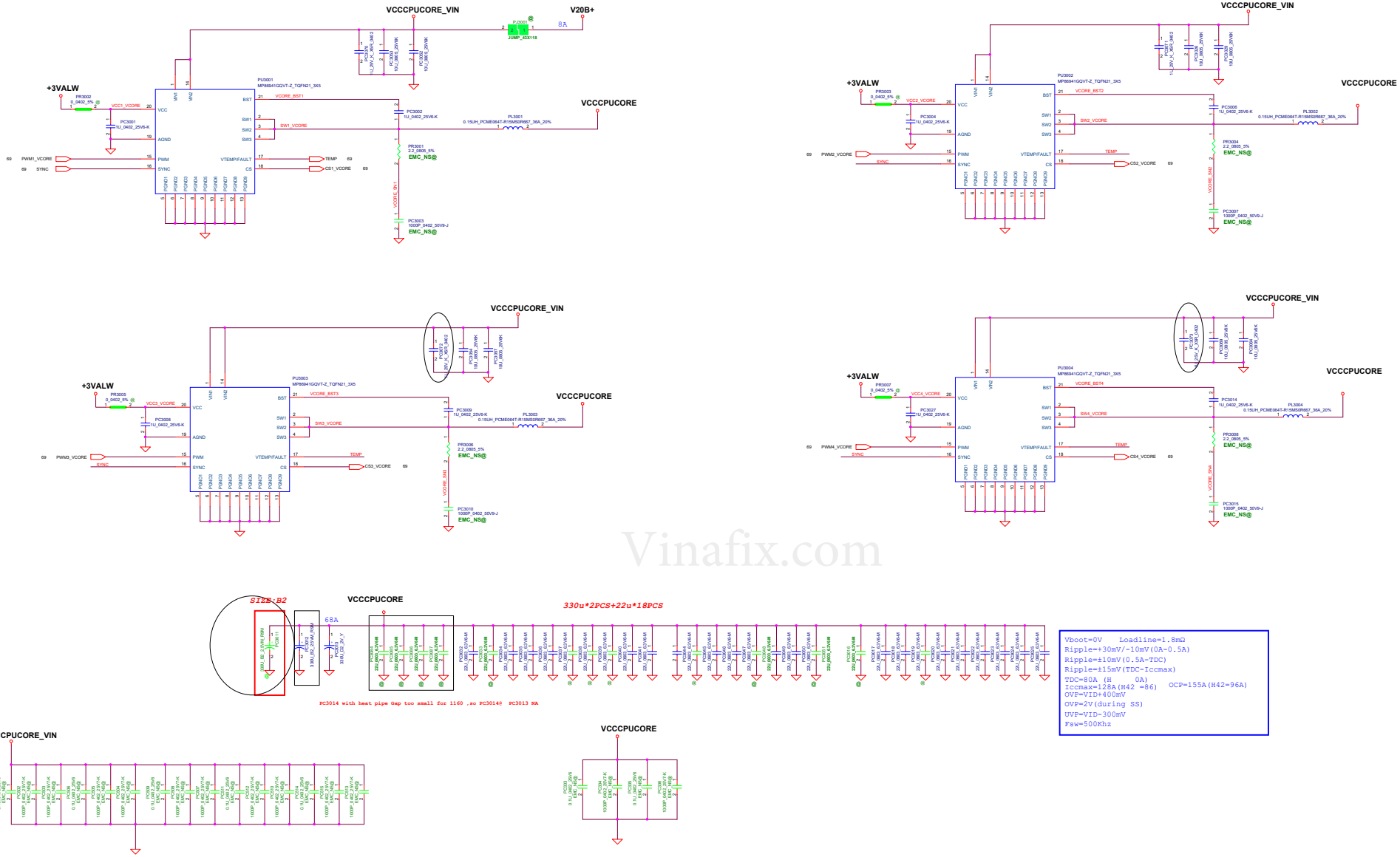
MP2979AGQKT-0048 for Y540
LCFC PN: SA00009Z600
PU2901 only change LCFC PN can not link CIS

PSYS=0.8V MP2949 trigger VRHOT



Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title	PWR-IMVP8_MP2949		
Size	Document Number	EY52U	Rev 2.0
Custom			
Date:	Friday, March 22, 2019	Sheet 69 of 75	



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

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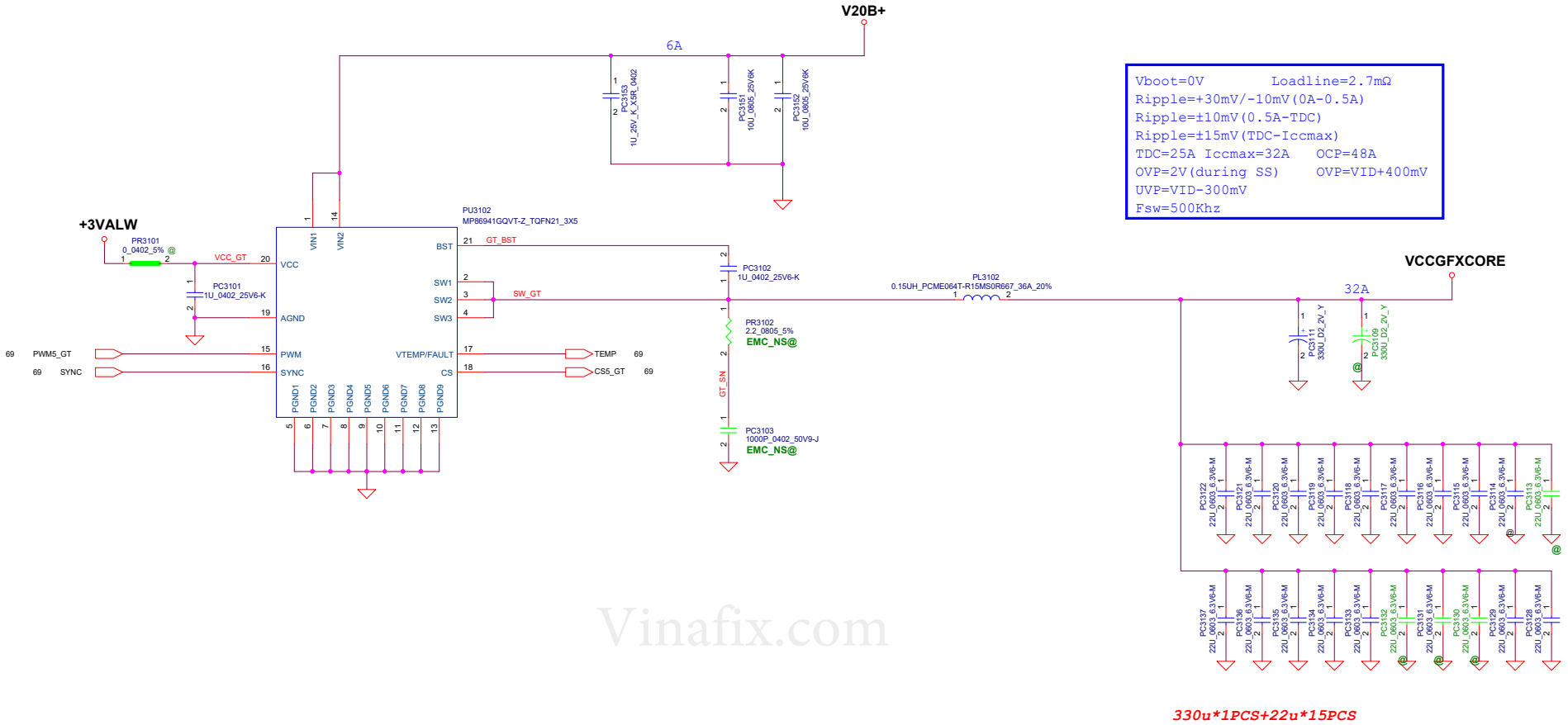
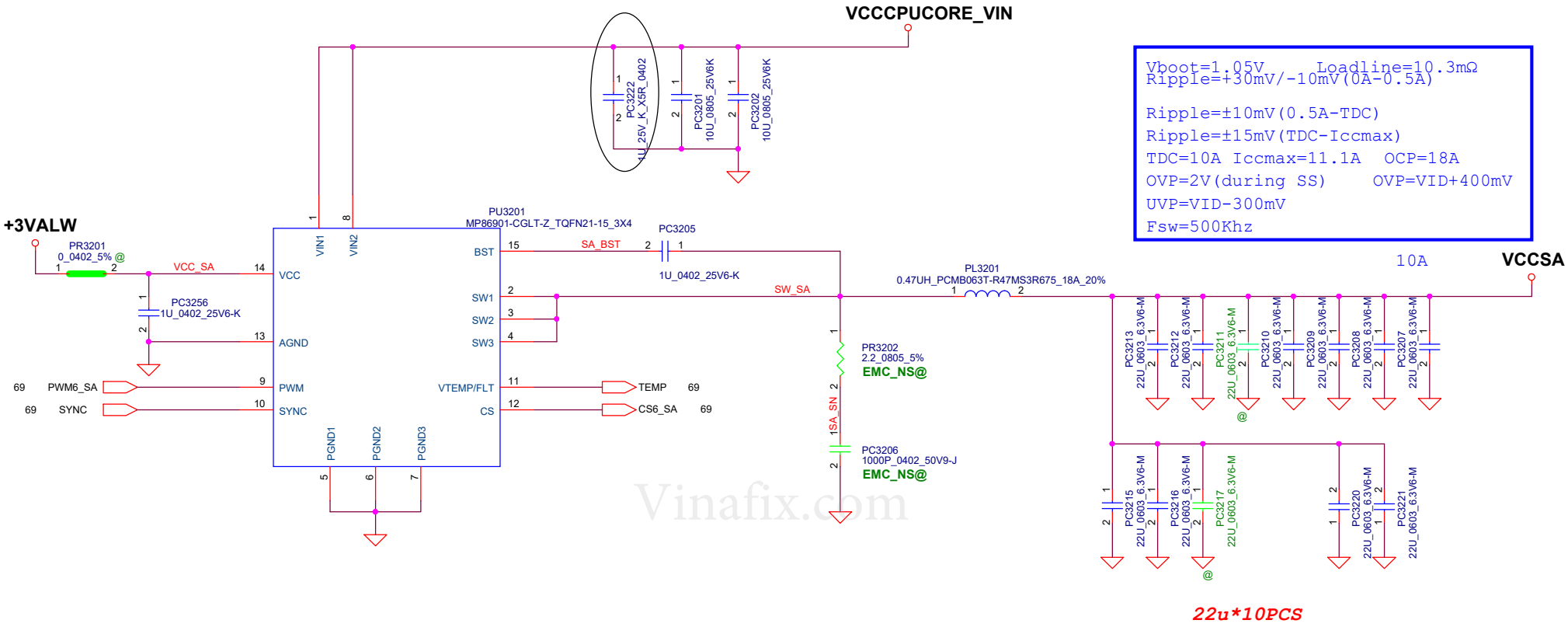
Title	PWR-VCCCPUCORE		
Size	Document Number	¥540	Rev 2.0
Custom			
Date: Friday, March 22, 2019	Sheet 78 of 77		



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **PWR-VCCGFXCORE**

Size: Custom	Document Number: Y540	Rev: 2.0
Date: Friday, March 22, 2019	Sheet 71 of 77	



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	PWR-VCCSA		
Size B	Document Number Y540		Rev 2.0
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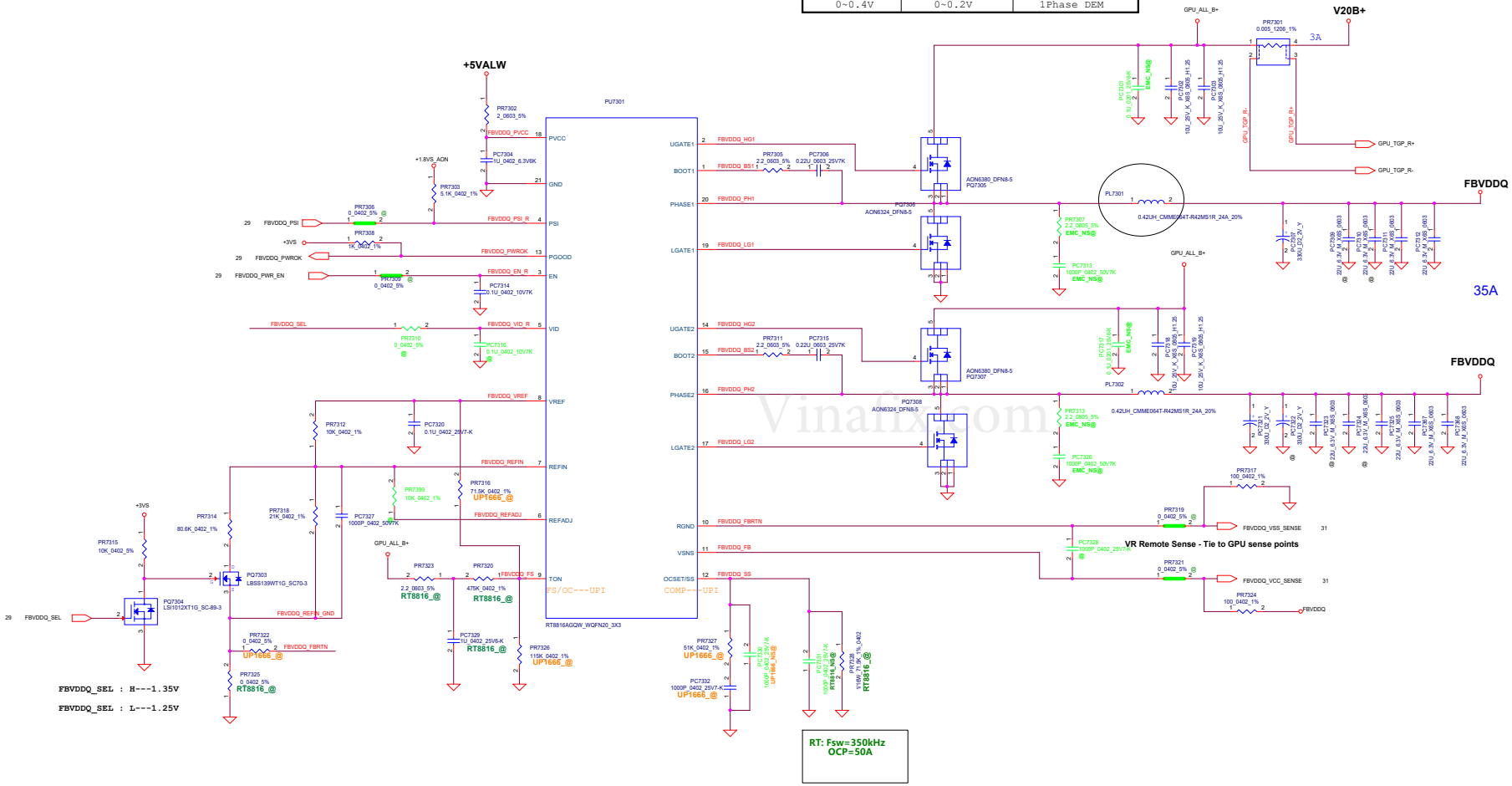
RT8816 PSI	UP1666 PSI	Phase Configuration
1.6V~5.5V	1.6~5.5V	2Phase CCM
1.08~1.35V	1~1.4V	2Phase DEM
0.7~0.88V	0.4V~0.8V	1Phase CCM
0~0.4V	0~0.2V	1Phase DEM



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	PWR-FBVDDQ		
Size: Custom	Document Number: Y540		Rev: 2.0
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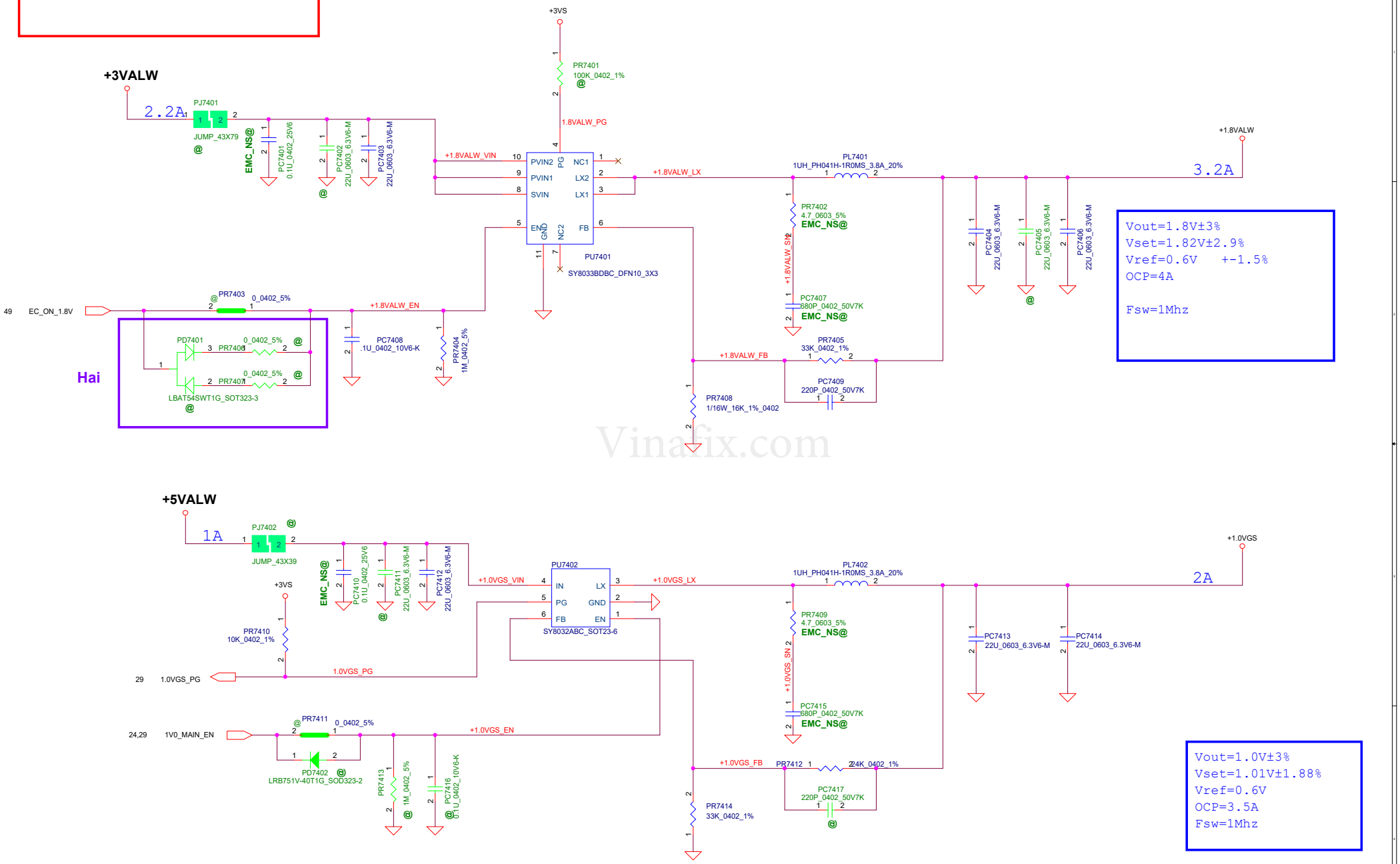
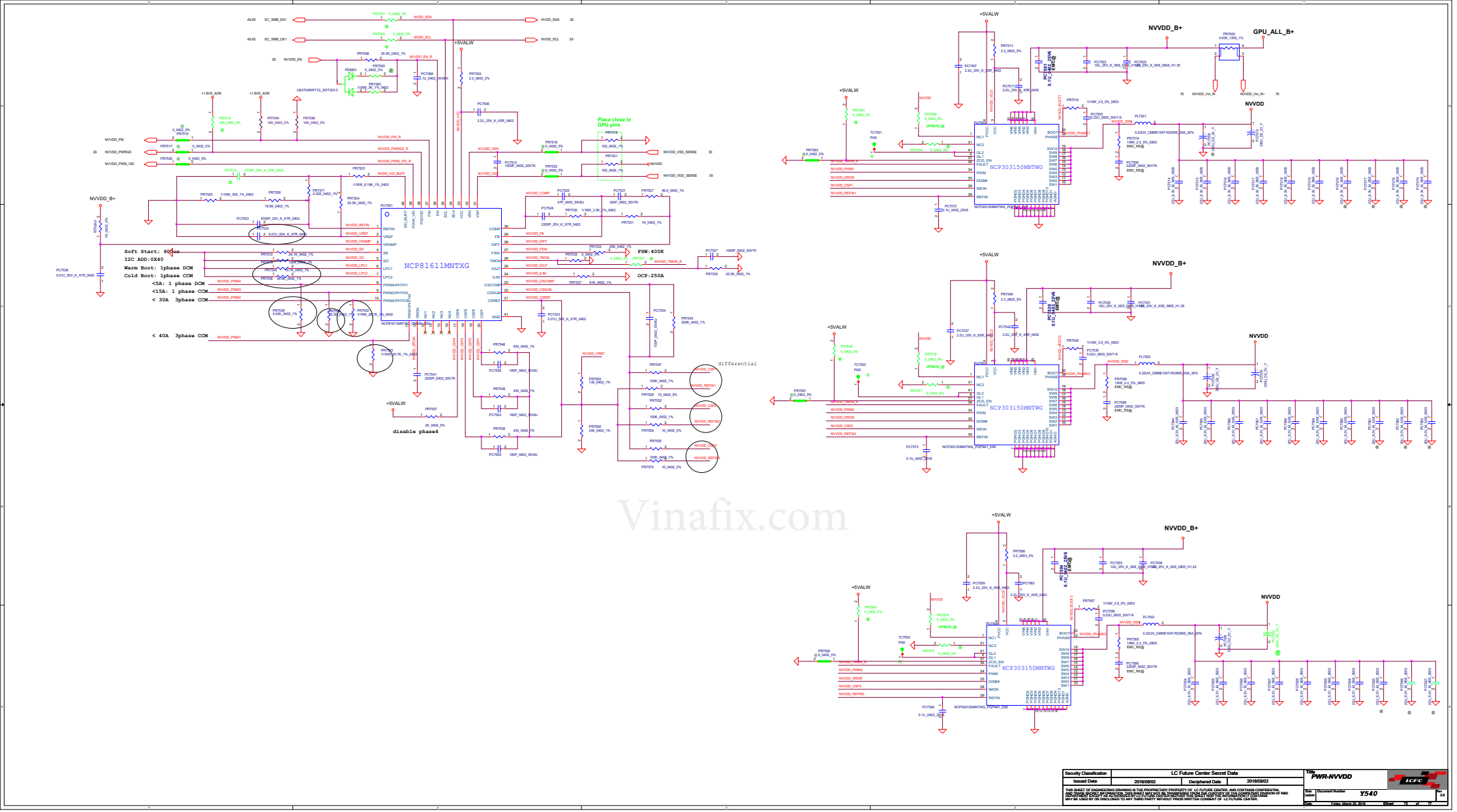
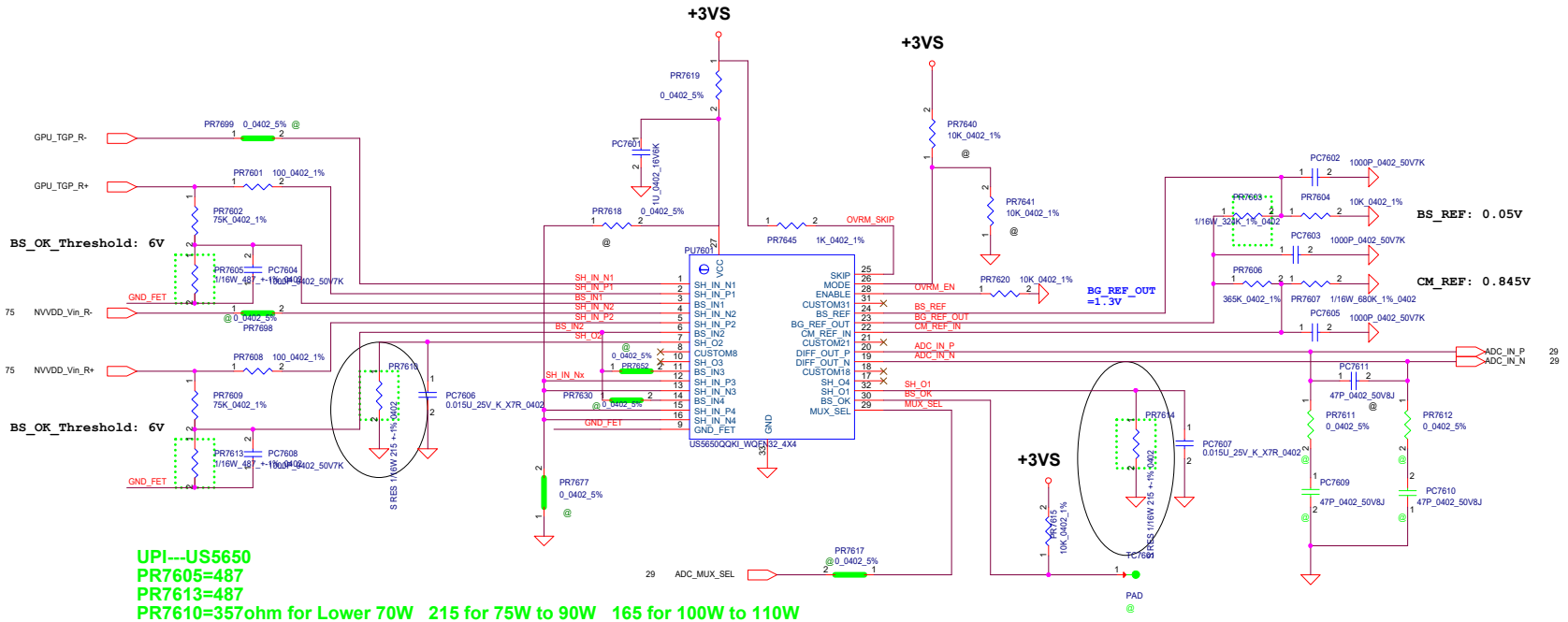
1.8V VIN change to 3.3V



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title			
PWR-1.8/1.0VGS			
Size: Custom	Document Number: Y540		Rev: 2.0
Date: Friday, March 22, 2019	Sheet 74 of 77		





UPI---US5650
PR7605=487
PR7613=487
PR7610=357ohm for Lower 70W 215 for 75W to 90W 165 for 100W to 110W
PR7614=357ohm for Lower 70W 215 for 75W to 90W 165 for 100W to 110W
PR7603=324K
PR7602=75K
PR7609=75K
PC7604=1nF
PC7608=1nF

ON---NCP45491
PR7605=649
PR7613=649
PR7610=475ohm for lower 70W 287 for 75W to 90W 221 for 100W to 110W
PR7614=475ohm for lower 70W 287 for 75W to 90W 221 for 100W to 110W
PR7603=243K
PR7602=75K
PR7609=75K
PC7604=1nF
PC7608=1nF

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	PWR-NVVDDS		
Size C	Document Number Y540		Rev 2.0
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Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: ***Virtual symbol***

Size	Document Number	Rev
C	***Y540***	2.0

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