14" Discrete Block Diagram

PCB Stackups

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : BOT

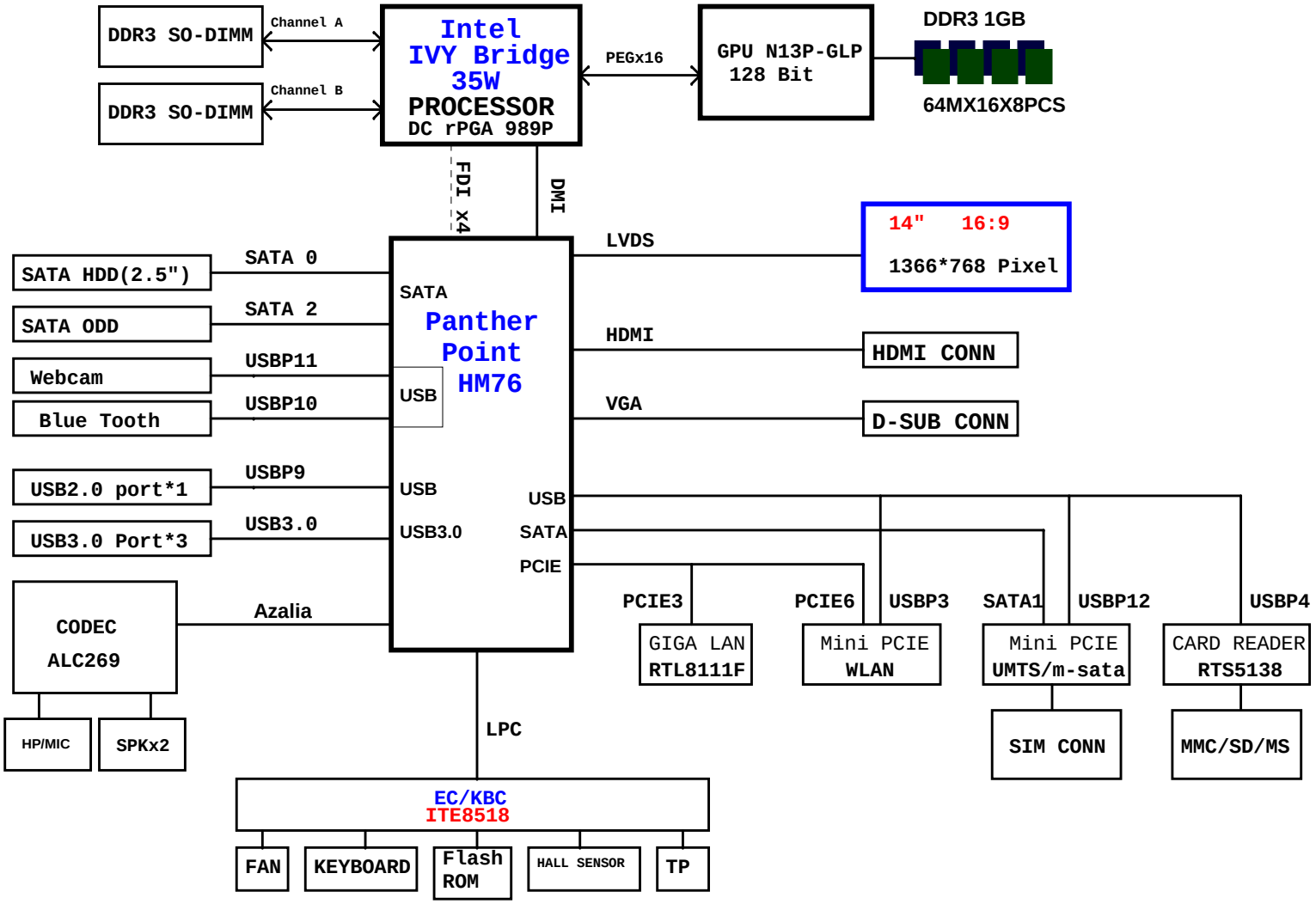

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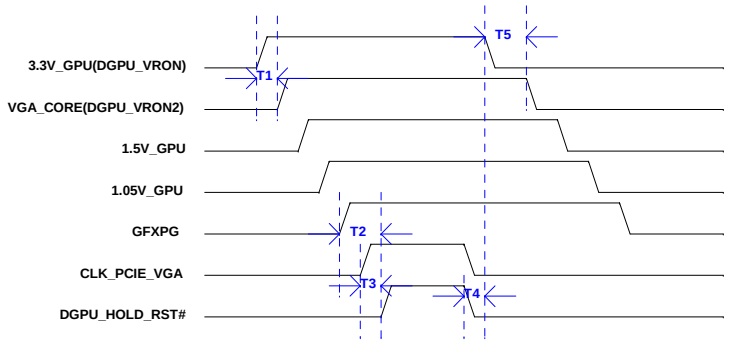
Table of Contents

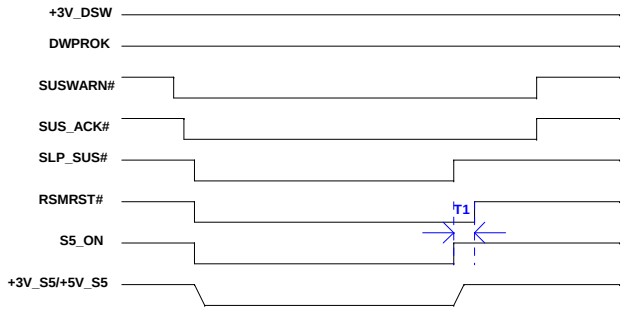
POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0~S5
3V_RTC	+3.0V~+3.3V		S0~G3
3V_S0	+3.3V	S0_ON1	S0
3V_S5	+3.3V	EC	S0~S5
3V_AUX	+3.3V	AC/DC Insert enable	AWLAYS
5V_S0	+5V	S0_ON1	S0
5V_S3	+5V	S3_ON	S0~S3
5V_S5	+5V	EC	S0~S5
5V_AUX	+5V	AC/DC Insert enable	AWLAYS
1.8V_S0	+1.8V	S0_ON2	S0
1.5V_S0	+1.5V	S0_ON2	S0
1.5V_S3	+1.5V	S3_ON	S0~S3
1.05V_S0	+1.05V	S0_ON2	S0
VCCSA	By VID	S0_ON2	S0
CPU_CORE	By VID	VR_ON	S0
VCC_AXG	By VID	VR_ON	S0
3V_LAN	+3.3V	LAN_ON	S0~S5(By WOL)
3V_GPU	+3.3V	DGPU_VRON	Optimus
1.5V_GPU	+1.5V	DGFX_VR_PWRGD	Optimus
1.05V_GPU	+1.05V	DGFX_VR_PWRGD	Optimus
VGA_CORE	By VID	DGPU_VRON1	Optimus

N13P-LP Power ON/OFF Sequence



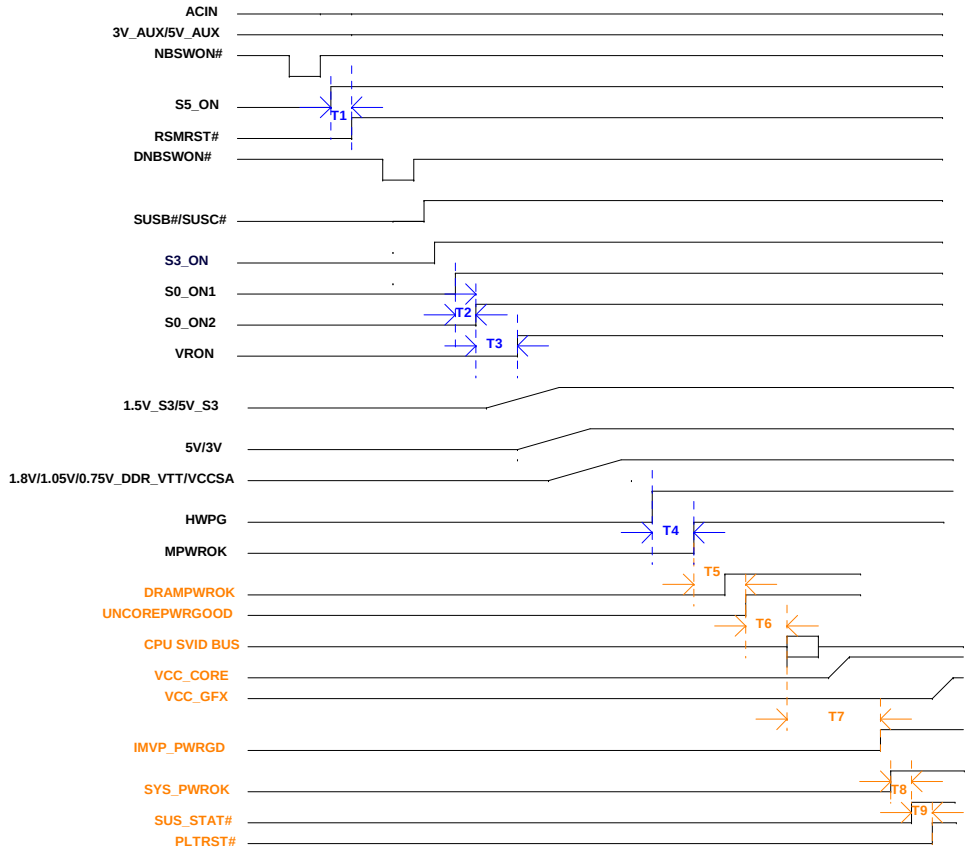
BIOS/ EC control:
T1:DGPU_VRON to DGPU_VRON2 = 500us
T2:GFXPG to DGPU_HOLD_RST# = 5ms
T3:CLK_PCIE_VGA to DGPU_HOLD_RST# >100us(Spec)
T4:DGPU_HOLD_RST# to DGPU_VRON = 5ms
Note: Clock must be shutdown before 3.3V_GPU
T5:DGPU_VRON to DGPU_VRON2 = 500us

Deep S4/S5 off-on Sequence



Deep S4/S5 Sequence
T1: S5_ON TO RSMRST# = 30ms (spec:mini 10ms)

System Power-ON Sequence

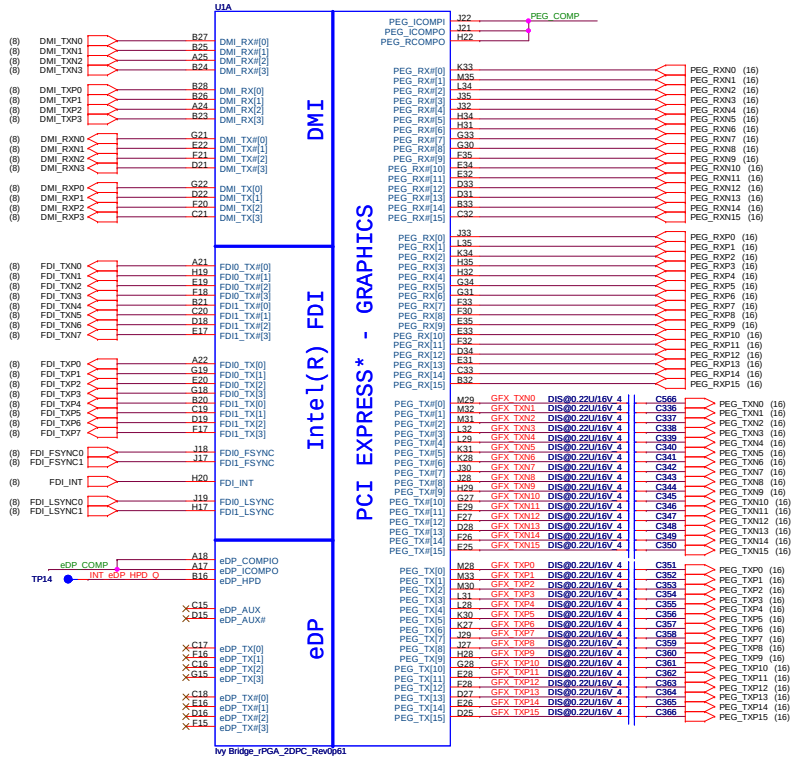


System Power Sequence

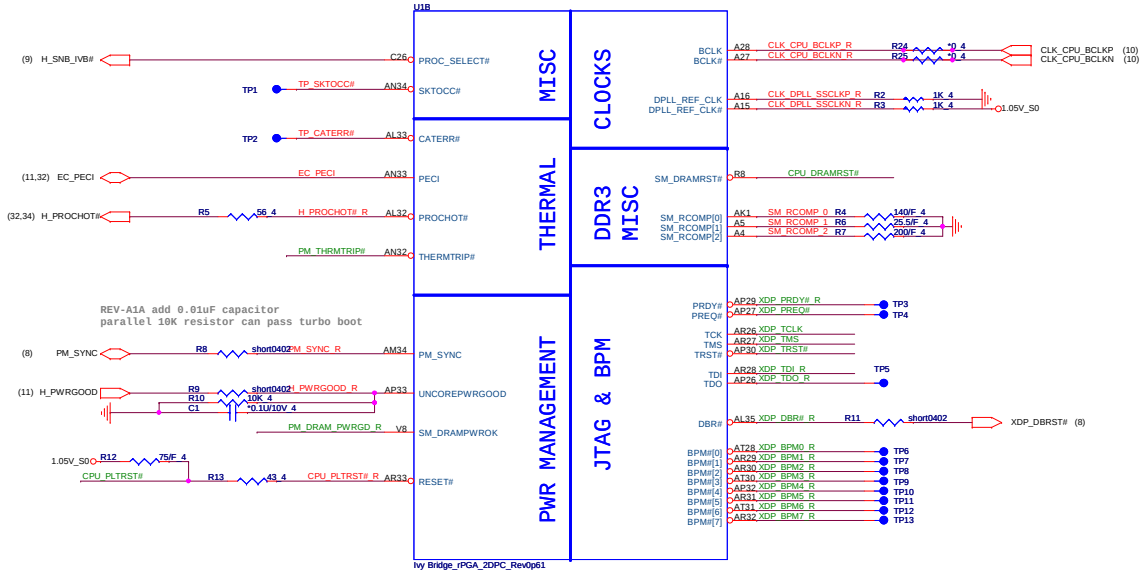
EC Control:
T1: S5_ON TO RSMRST# = 20ms (spec:mini 10ms)
T2: S0_ON1 TO S0_ON2 = 500us
T3: S0_ON2 TO VRON = 10ms
T4: HWPG TO MPWROK = 110ms (spec:mini 99ms)
Note:HWPG NEED TO BE HIGH at that time

System:
T5: MPWROK to UNCOREPWRGOOD =2ms(Min)
T6: UNCOREPWRGOOD to SVID Packet =500us(Max)
T7: SVID Packet to IMVP_PWRGD =5ms(Max)
T8: SYS_PWROK to SUS_STAT# =1ms(Min)
T9:SUS_STAT# to PLTRST# =60us(Min)

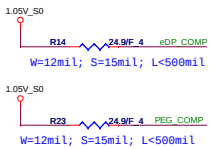
Ivy Bridge Processor (DMI,PEG,FDI)



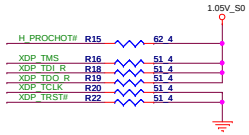
Ivy Bridge Processor (CLK,MISC,JTAG)



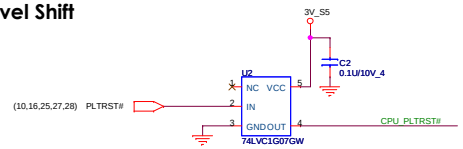
DP & PEG Compensation



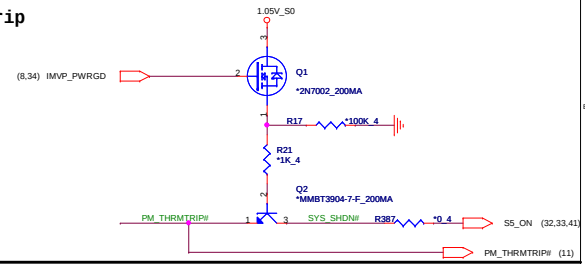
Processor pull-up



Level Shift



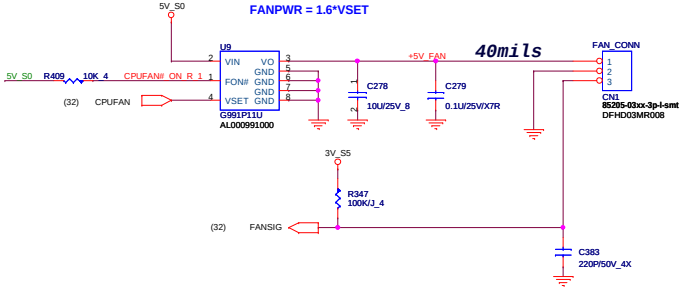
Thermal Trip



FAN Control-->For one FAN solution

VSET >= 1V, Enable

FANPWR = 1.6*VSET



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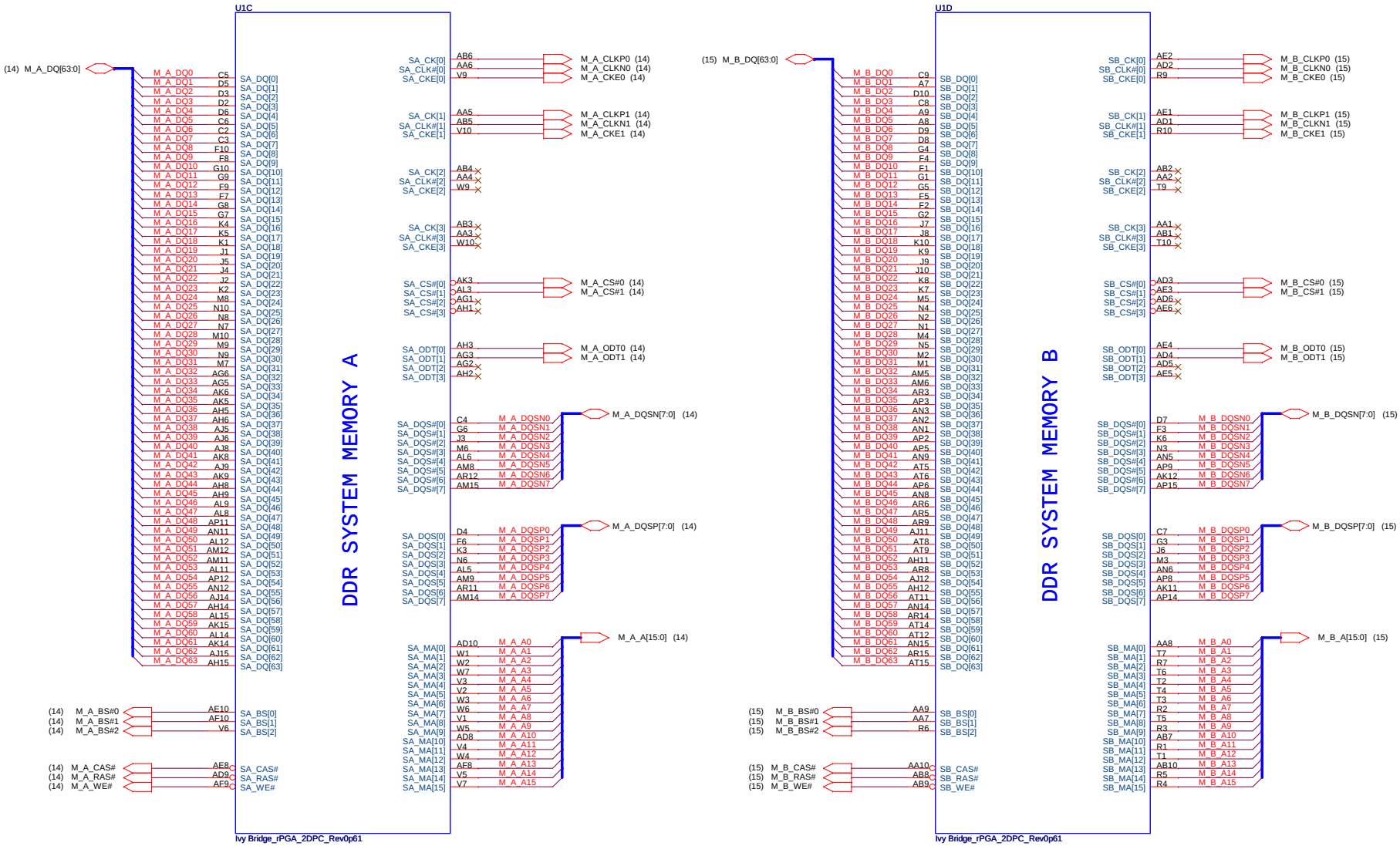
Ivy Bridge Processor (DDR3)

05



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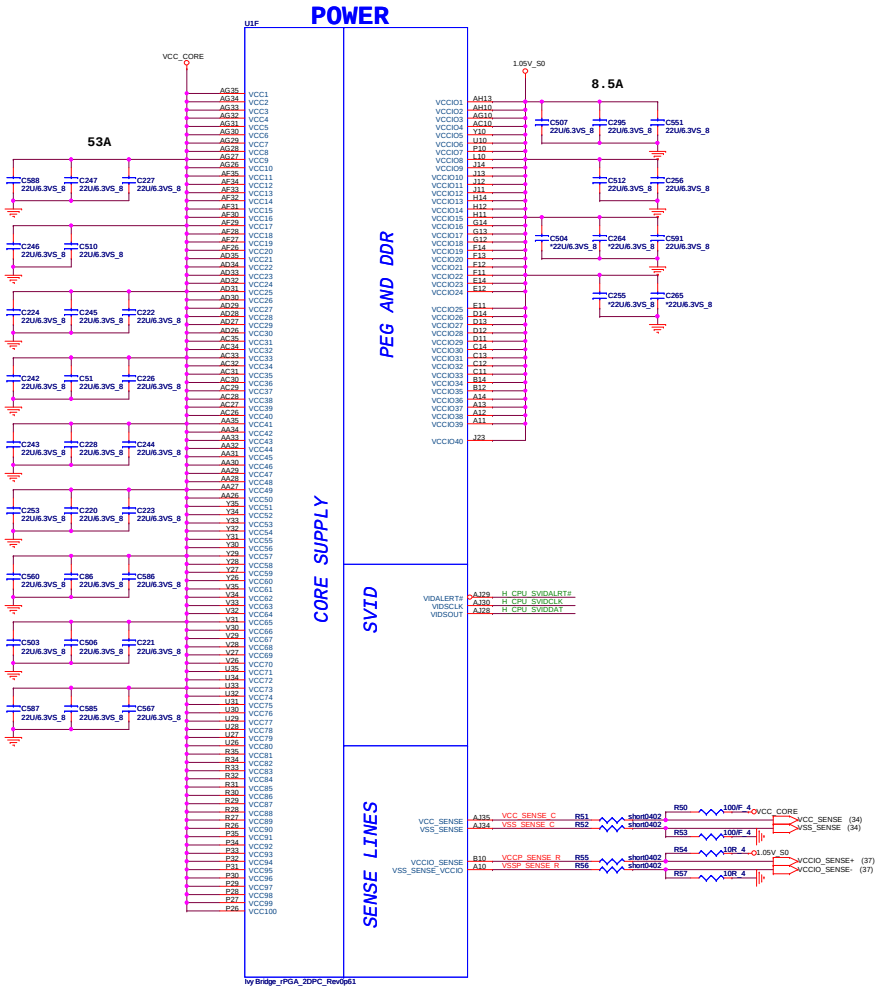
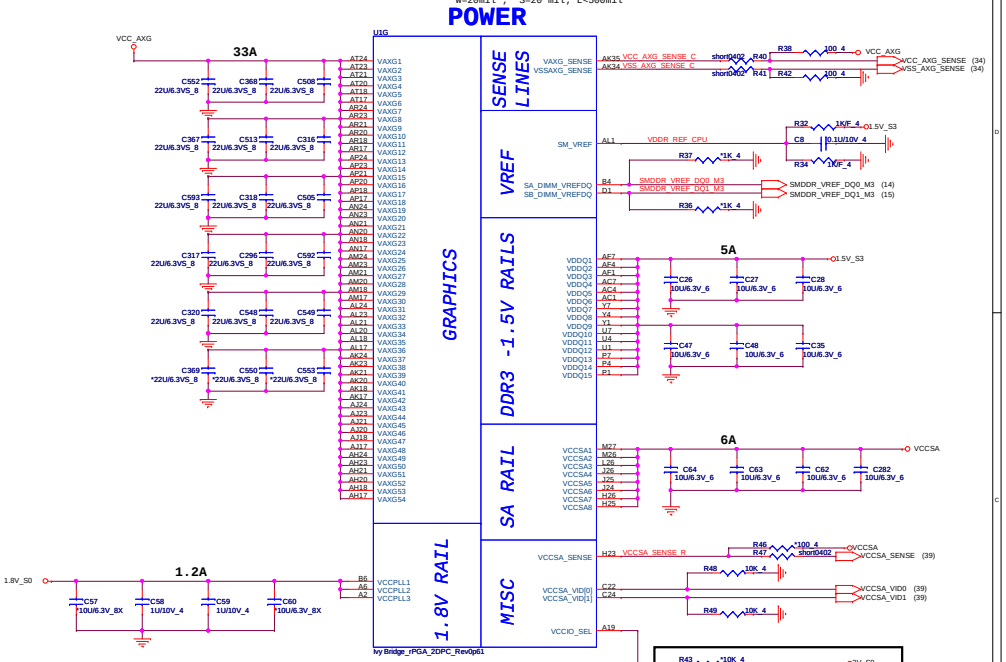
Ivy Bridge Processor (POWER)



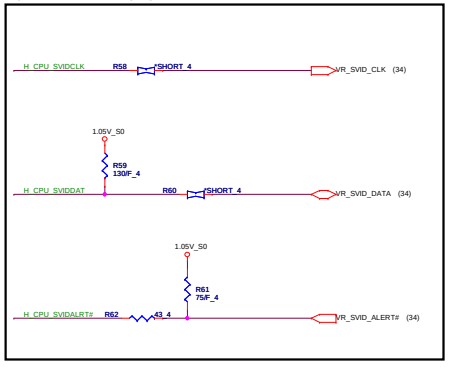
Ivy Bridge Processor (GRAPHIC POWER)

W=20mil ; S=20 mil; L<500mil

06



Layout note: need routing together and ALERT need between CLK and DATA



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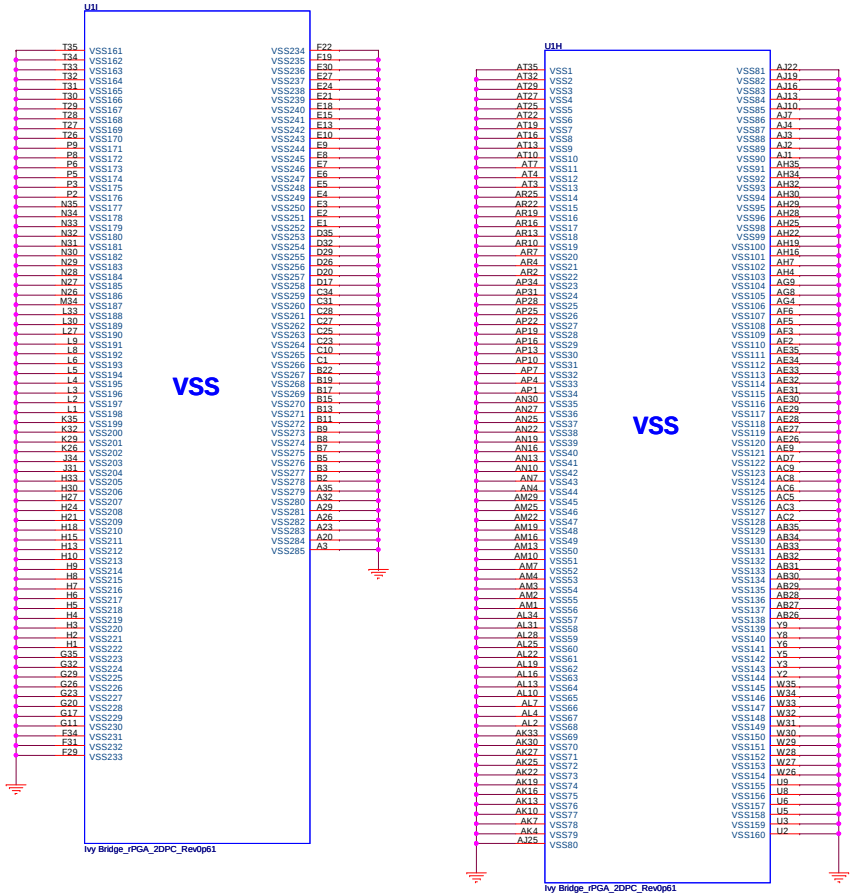
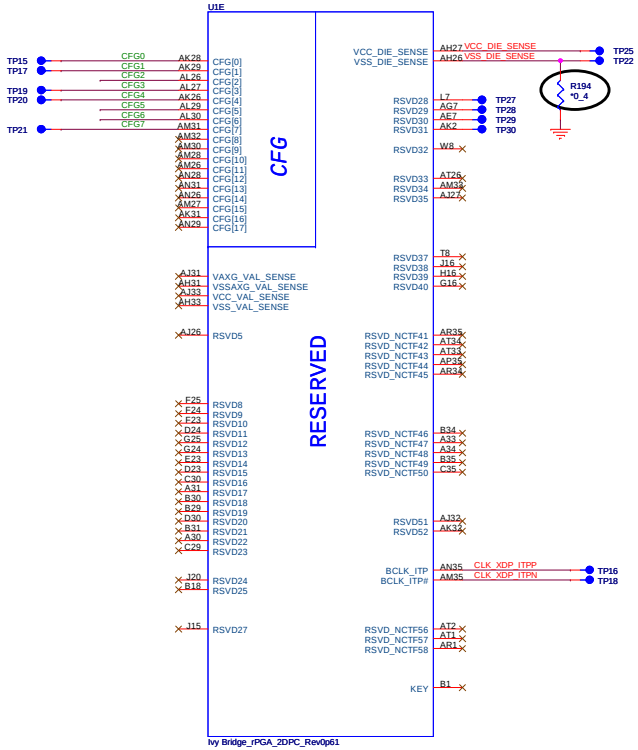
Ivy Bridge Processor (GND)

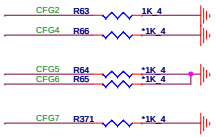


Ivy Bridge Processor (RESERVED, CFG)



Processor Strapping

CFG2	0	PCIe X16 LANE Reversed
	1	Normal Operation
CFG3	0	PCIe X4 LANE Reversed
	1	Normal Operation
CFG4	0	Enable; An ext DP device is connected to eDP
	1	Disable; No physical DP attached to eDP
CFG(5:6)	00	1 x 8 , 2 x 4 PCIe
	01	Reserve
	10	2 x 8 PCIe
	11	1 x 16 PCIe
CFG7	0	PEG Wait for BIOS for training
	1	PEG Train immediately following PLT_RST#



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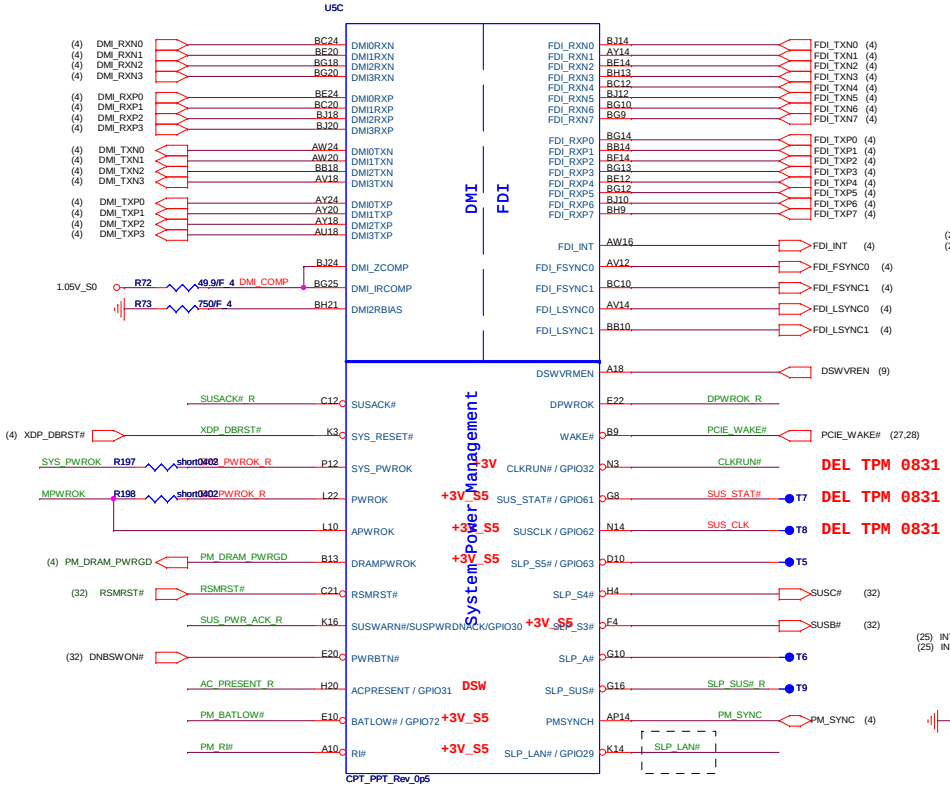
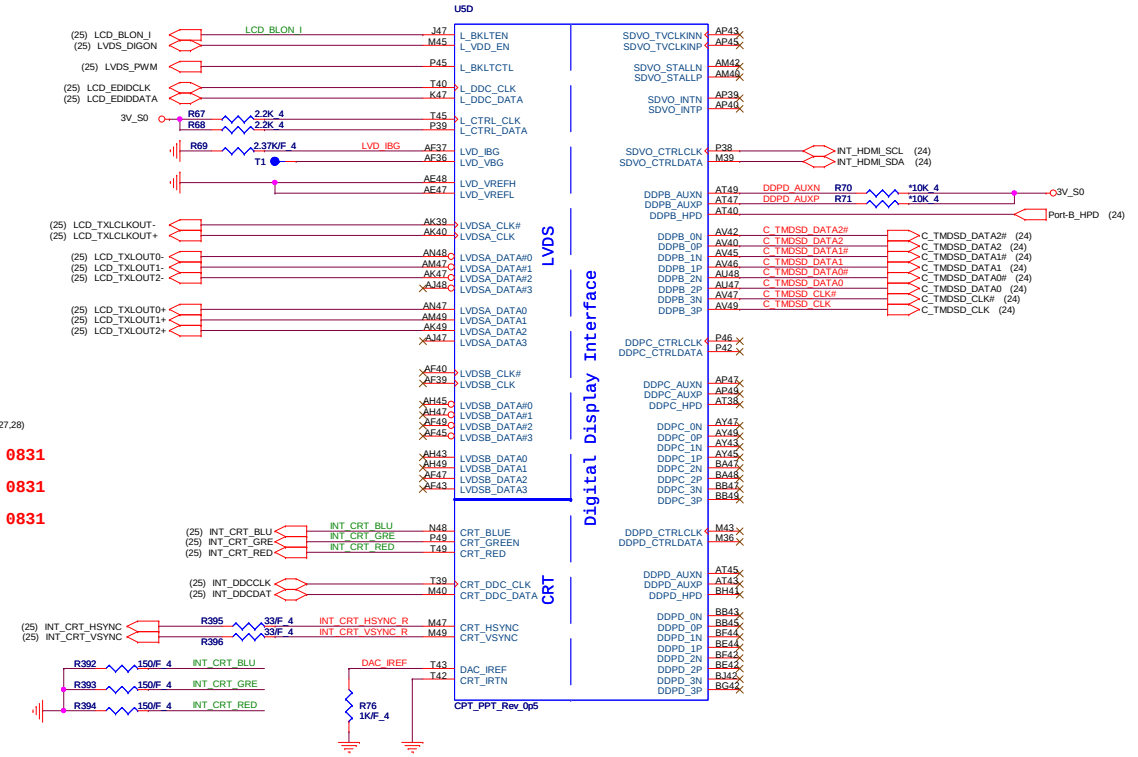
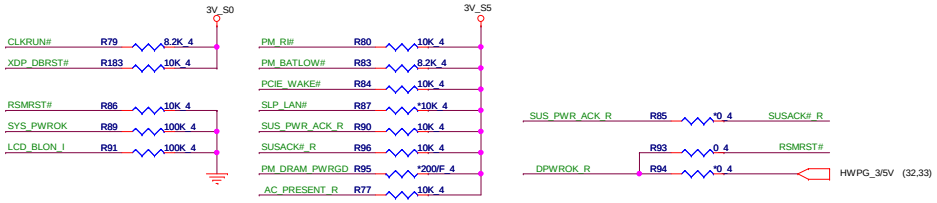
Panther Point (DMI,FDI,PM)



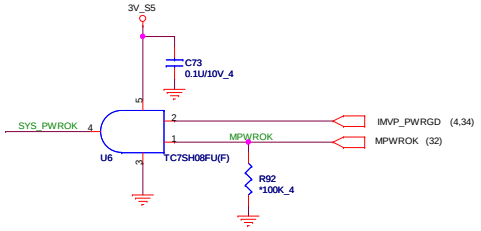
Panther Point (LVDS,DDI)



PCH Pull-high/low



System PWR_OK



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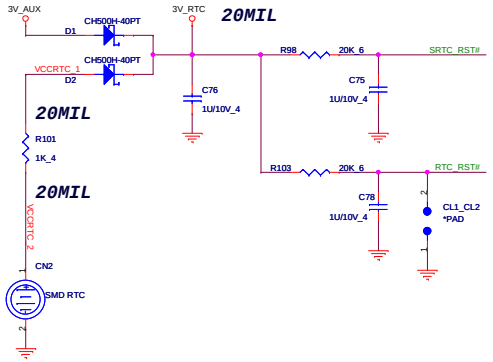
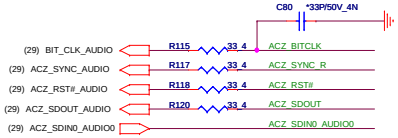
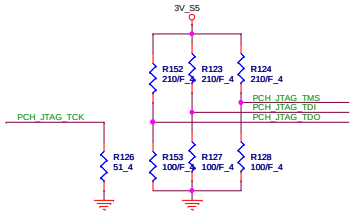
RTC Circuit



HDA Bus



PCH JTAG Debug

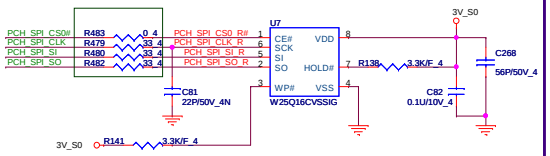


B-12

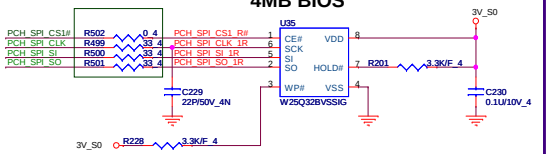
PCH Dual SPI

MX25L3205DM2I-12G: AKE39FP0Z00
W25X32VSSIG: AKE39ZP0N00

2MB ME



4MB BIOS

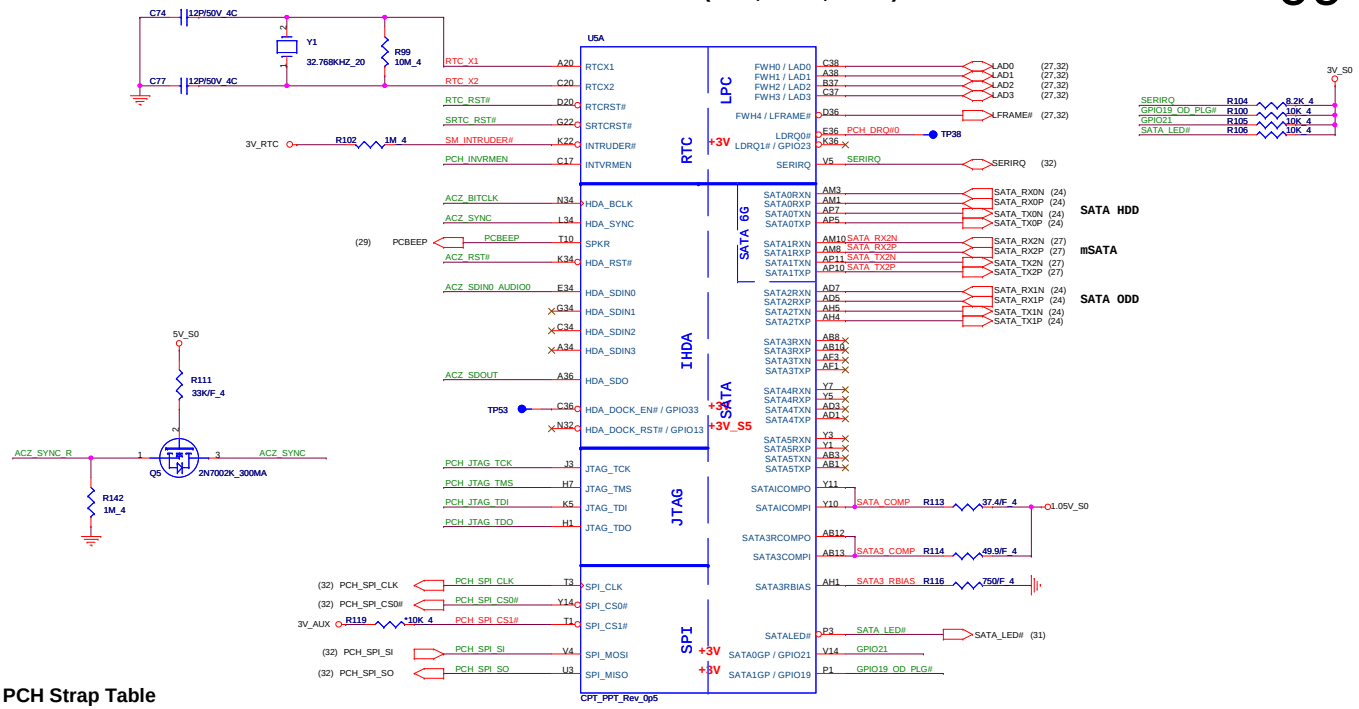


PCH2

1ST BG332768077
2ND BG332768453

Panther Point (HDA,JTAG,SATA)

09



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	3V_S0 R121 *1K_4 PCBEEP
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R122 *1K_4 PCI_GNT3# (10)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	3V_RTC R125 330K_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GPIO19 / Boot Location: 1 / 1 / SPI; 0 / 0 / LPC	R129 *1K_4 GNT1# (10) R130 *1K_4 GPIO19_OD_PLG#
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		
HDA_SDO	Flash Descriptor Security	RSMRST	1 = Override 0 = Default (weak PD 20K)	3V_S0 R131 *1K_4 ACZ_SDOUT ACZ_SDOUT (32)
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R132 2.2K_4 R133 1K_4 1.8V_S0 DF_TVS (11) H_SNB_IVB# (4)
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	3V_AUX R134 *10K_4 R135 *1K_4 PLL_ODVR_EN (11)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	3V_S5 R136 1K_4 ACZ_SYNC
GPIO15	TLS Confidentiality	RSMRST	0 = Default. TLS no Confidentiality 1 = TLS Confidentiality	3V_S5 R137 *1K_4 GPIO15 (11)
DSWVRMEN	Deep S4/S5 Well On -Die Voltage Regulator Enable	ALWAYS	0 = Disable 1 = Enable	DSWVREN (8) 3V_RTC R139 330K_4 R140 *330K_4
INIT3_3V#	**Reserved**	PWROK	1 = Default (weak pull-up 20K)	**Should not pull low. leave as No Connect**
GNT2#/ GPIO53	**ESI Strap (Server Only)**	PWROK	1 = Default. Should not be pulled low for desktop and mobile	**Should not pull low for desktop and mobile**
L_DDC_DATA	LVDS Detected	PWROK	0 = Default. Not Detected 1 = Detected	1= PU to 3V
SDVO_CTRLDATA	Port B Detected	PWROK	0 = Default. Not Detected 1 = Detected	1= PU to 3V
DDPC_CTRLDATA	Port C Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC
DDPD_CTRLDATA	Port D Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC
SATA3GP/ GPIO37	**Reserved**	PWROK	0 = Default	**Should not be pulled high when strap is sampled**
SATA2GP/ GPIO36	**Reserved**	PWROK	0 = Default	**Should not be pulled high when strap is sampled**

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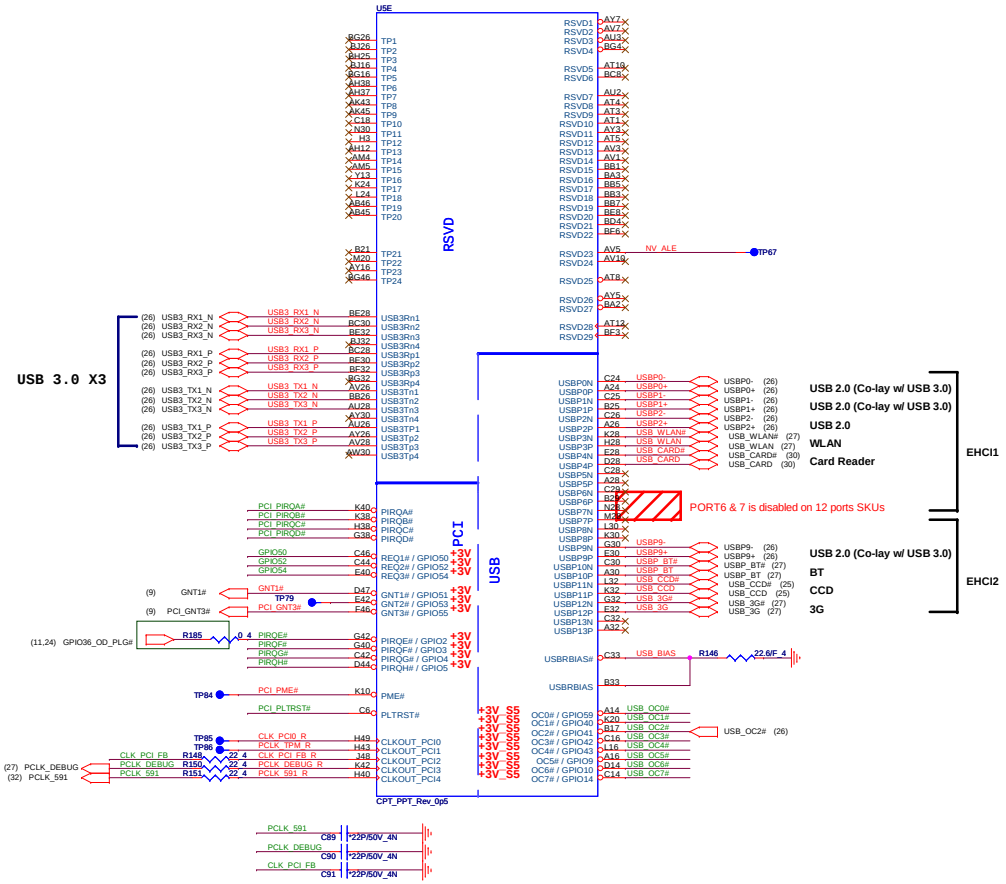
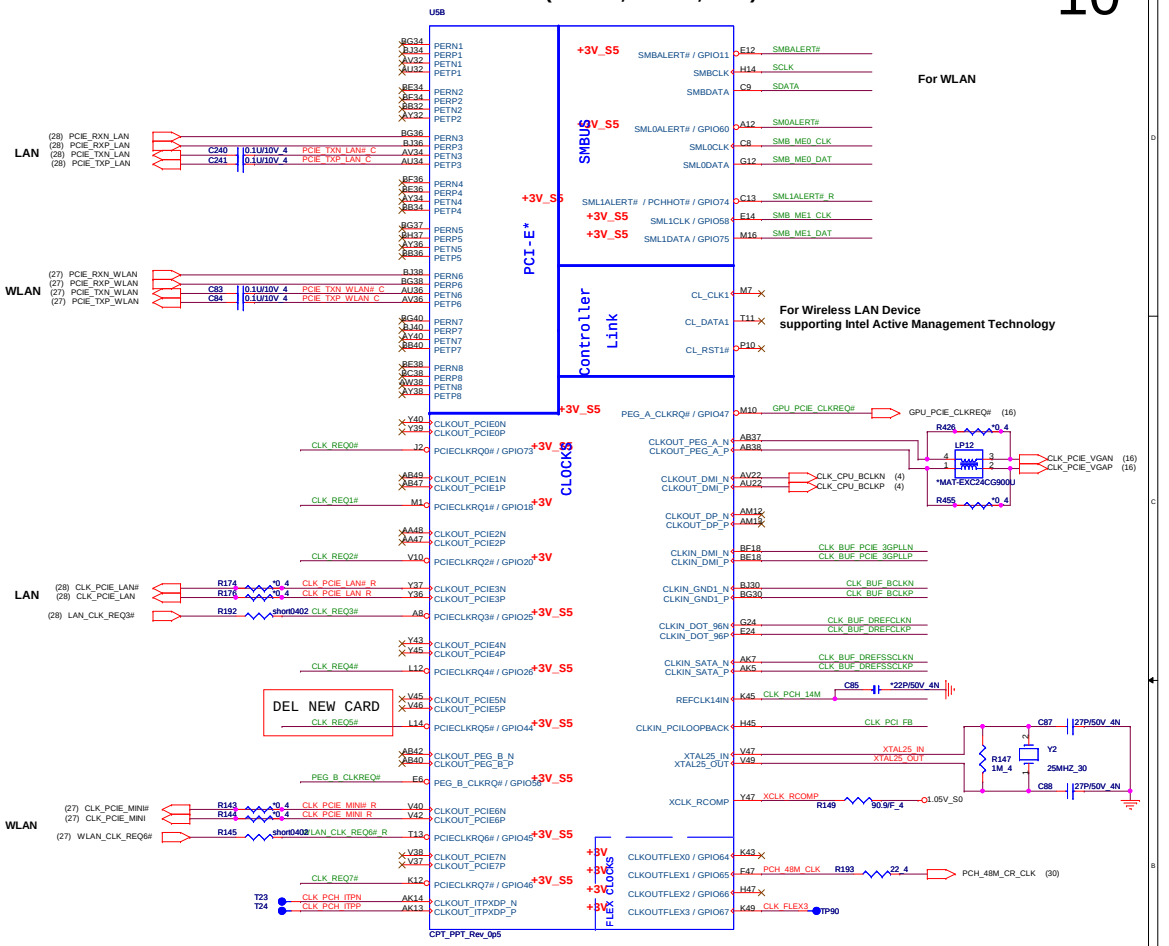
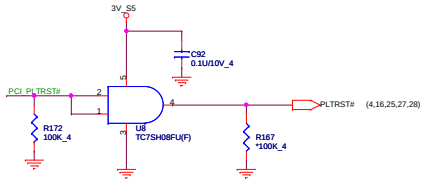
Panther Point-M (PCI,USB,NVRAM)



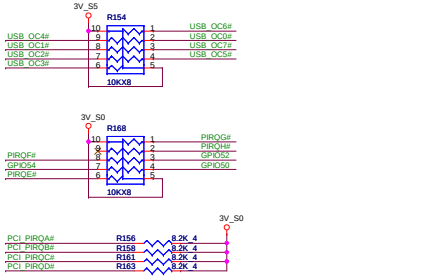
Panther Point-M (PCI-E,SMBUS,CLK)



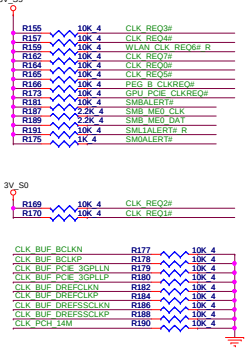
PLTRST#



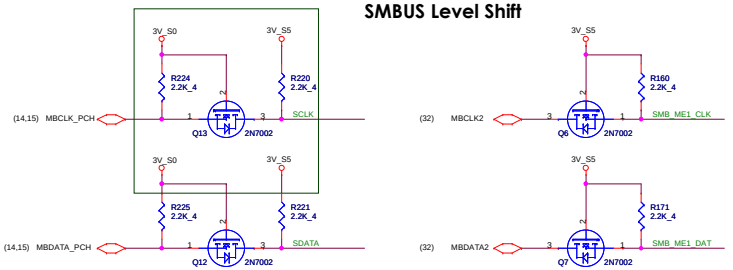
PCI/USBOC# PU



System PU



SMBUS Level Shift



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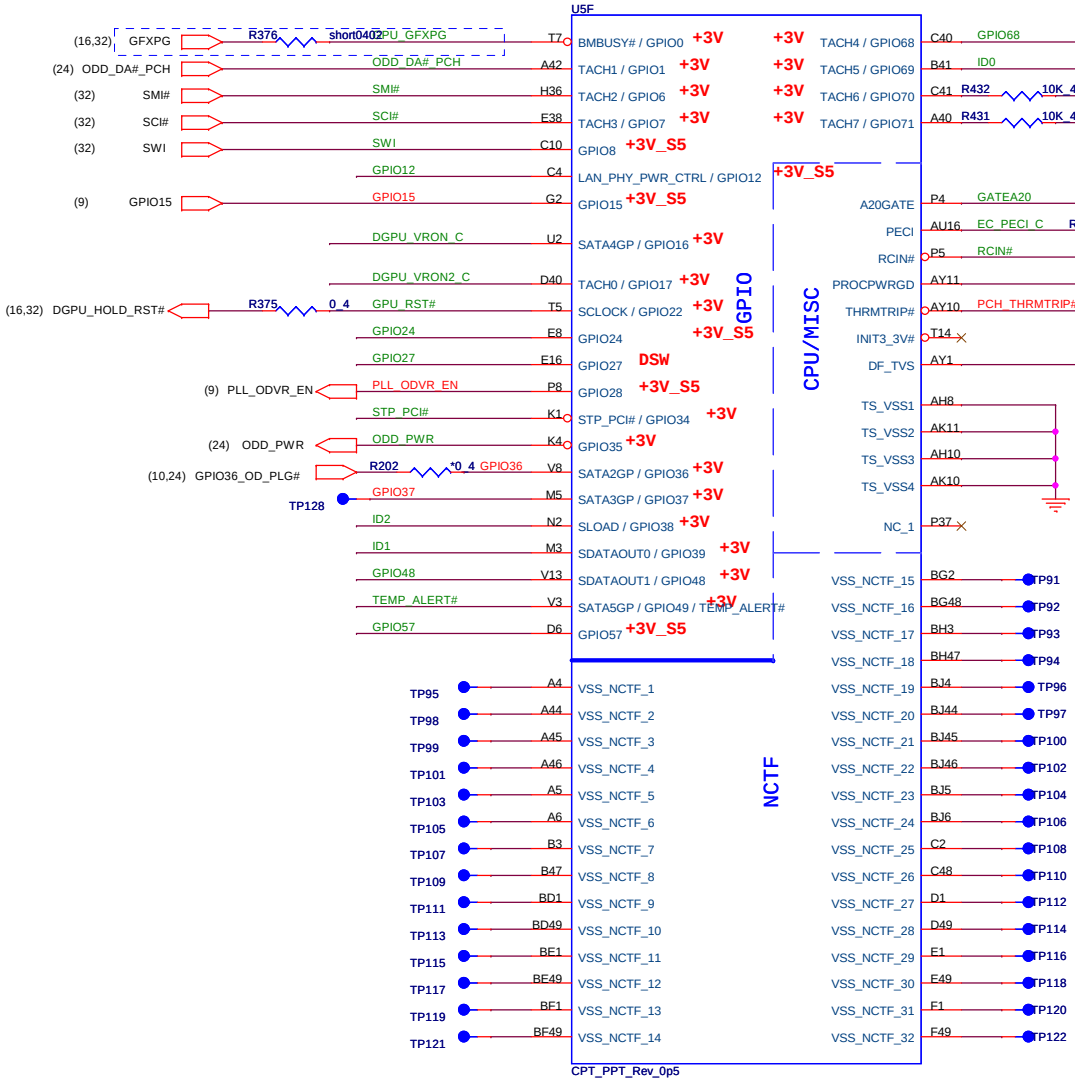
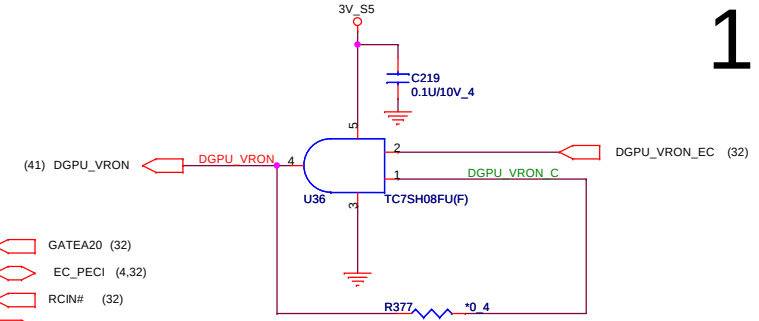
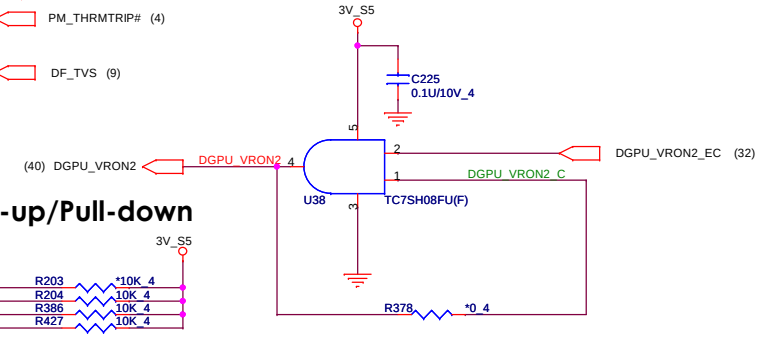
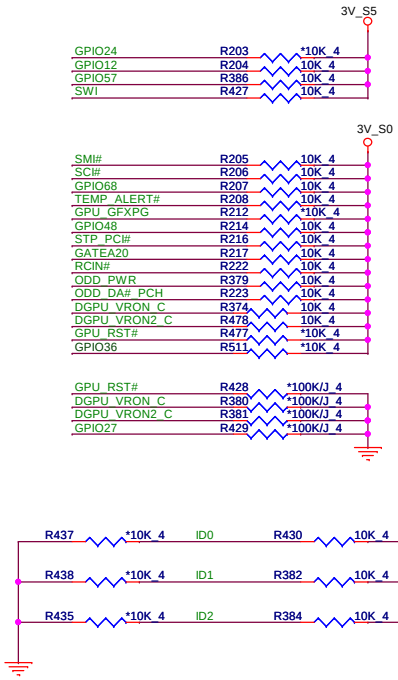
Panther Point (GPIO,VSS_NCTF,RSVD)

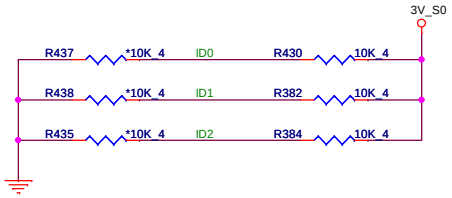






GPIO Pull-up/Pull-down





ID2	ID1	ID0	Model
0	0	0	TBD
0	0	1	TBD
0	1	0	FH6 UMA(Consumer)
0	1	1	FH6 UMA(Commercial)
1	0	0	FH6 N13P-LP
1	0	1	FH6 N13P-GLP
1	1	0	FJ8 UMA
1	1	1	FJ8 Discrete

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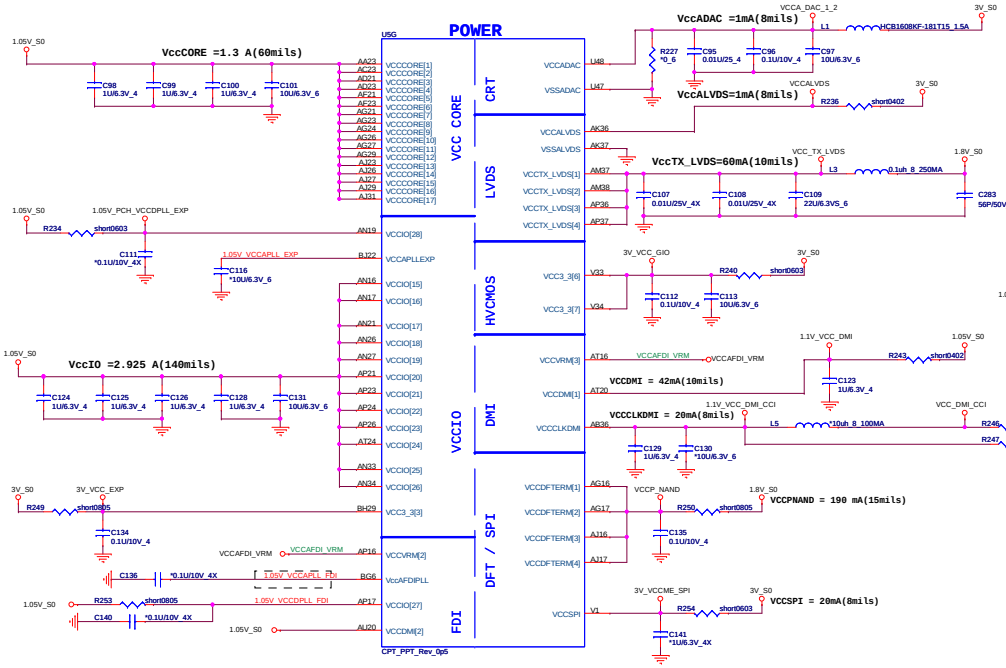
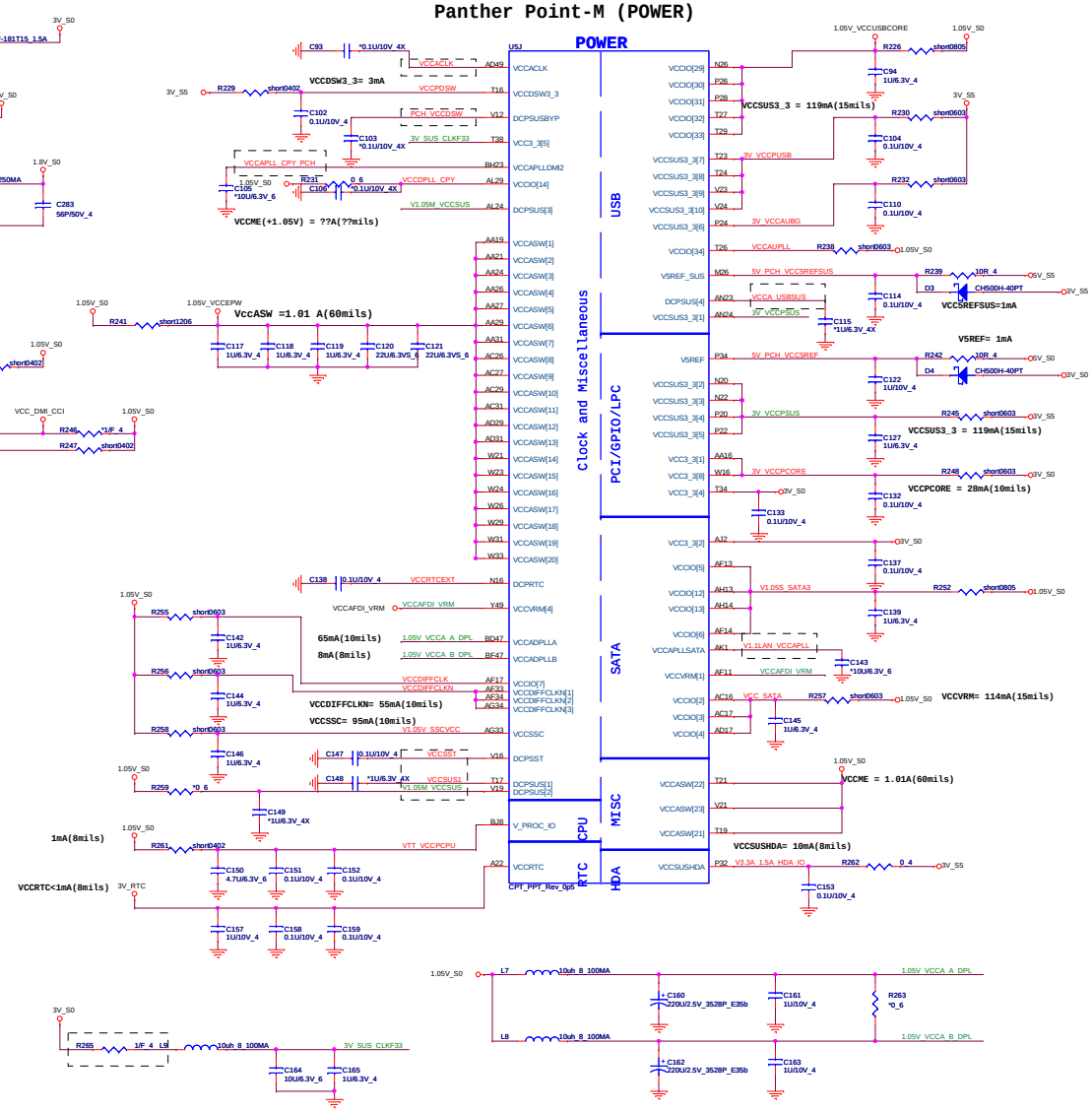
Panther Point (POWER)



Panther Point-M (POWER)



Quanta Computer Inc.
PROJECT : FJ8

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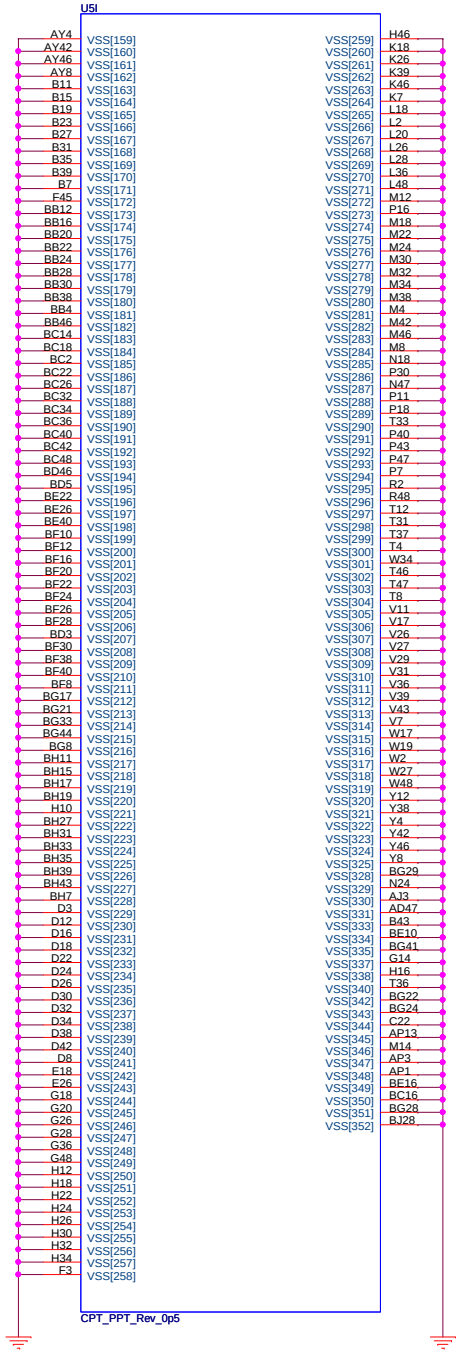
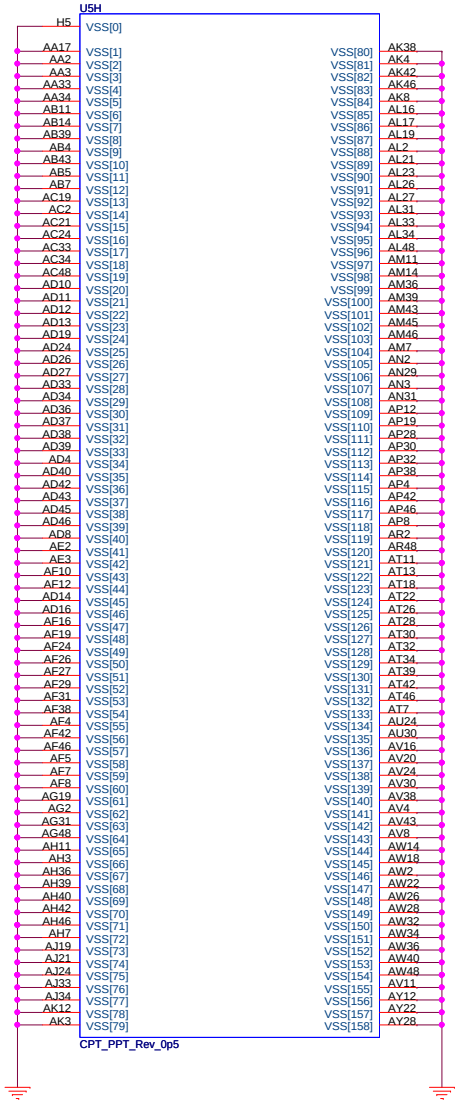
IBEX PEAK-M (GND)





Quanta Computer Inc.

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Size	Document Number	Rev
	Panther Point 6/6	2A
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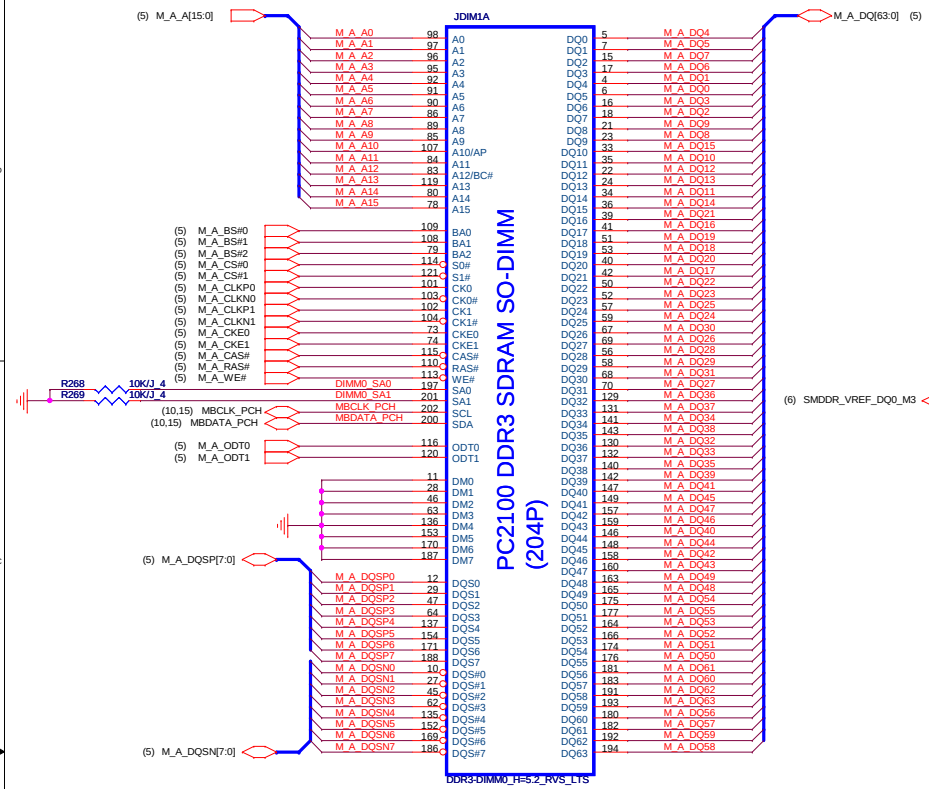
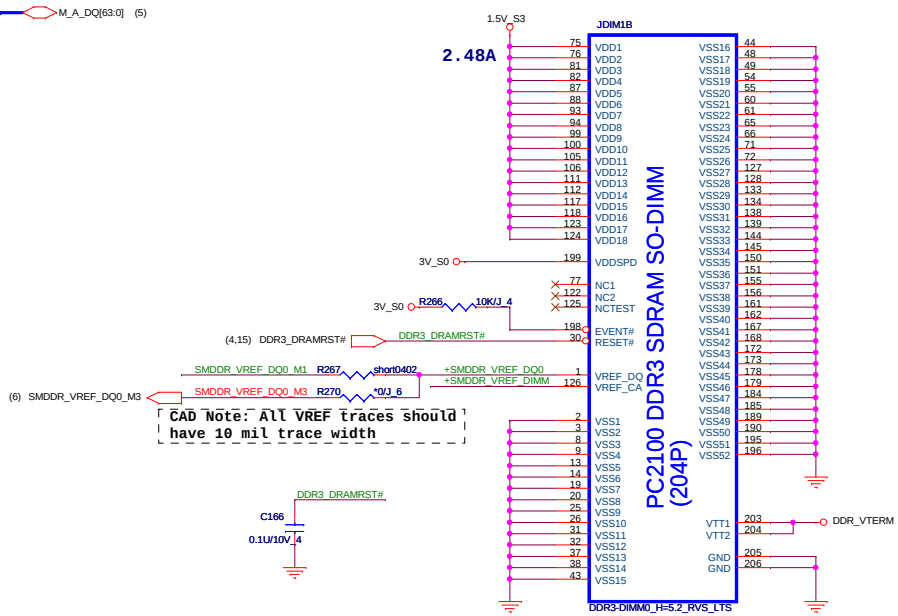
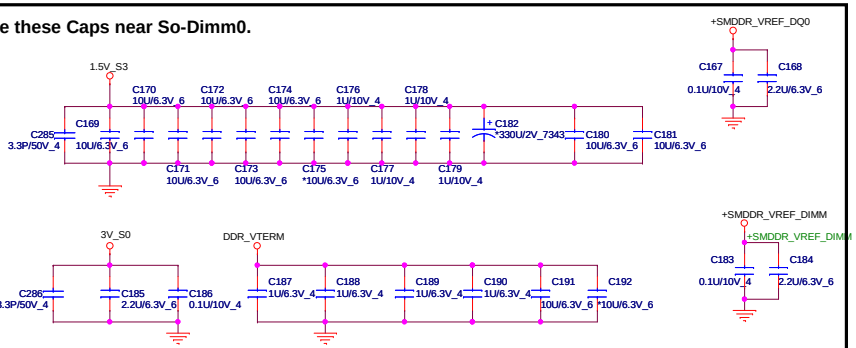
DDR3_RVS

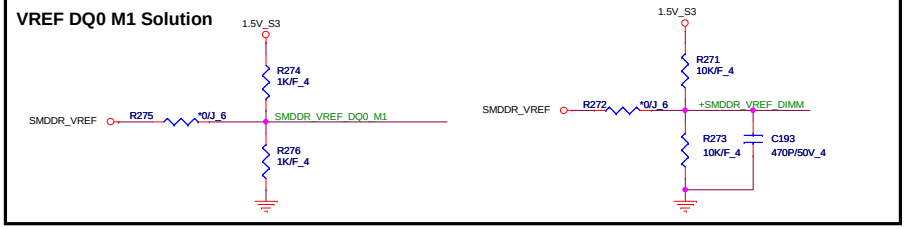




Place these Caps near So-Dimm0.



VREF DQ0 M1 Solution



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	DDRIII SO-DIMM-0	2A
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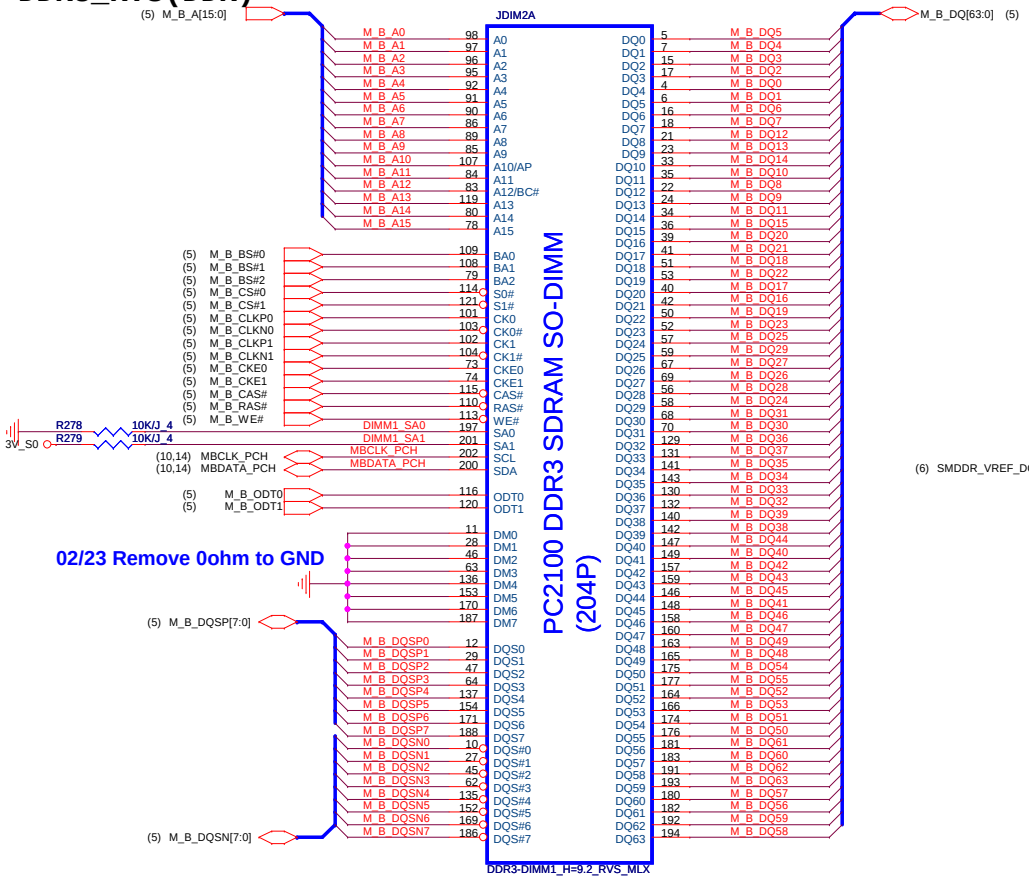
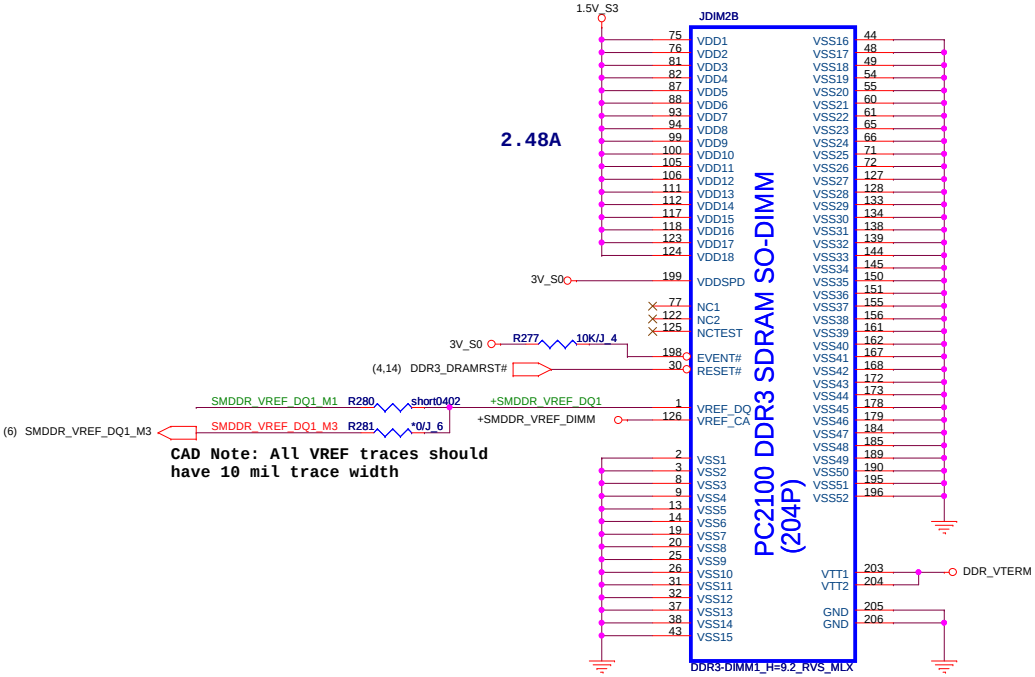
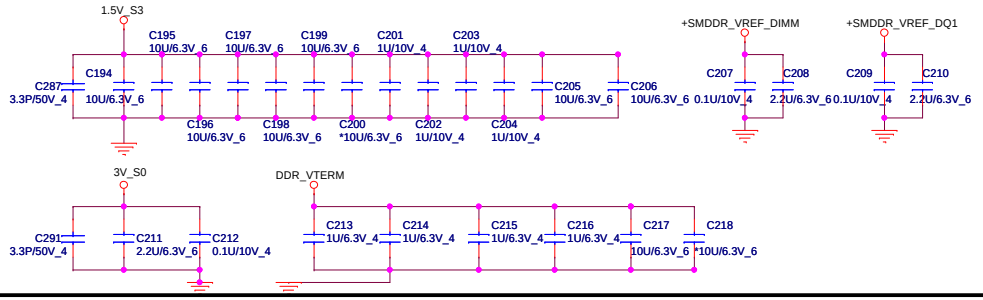
DDR3_RVS(DDR)

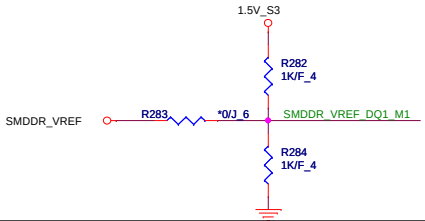




Place these Caps near So-Dimm1.



VREF DQ1 M1 Solution



Quanta Computer Inc.		
PROJECT : FJ8		
Size	Document Number: DDRIII SO-DIMM-1	Rev: 1A
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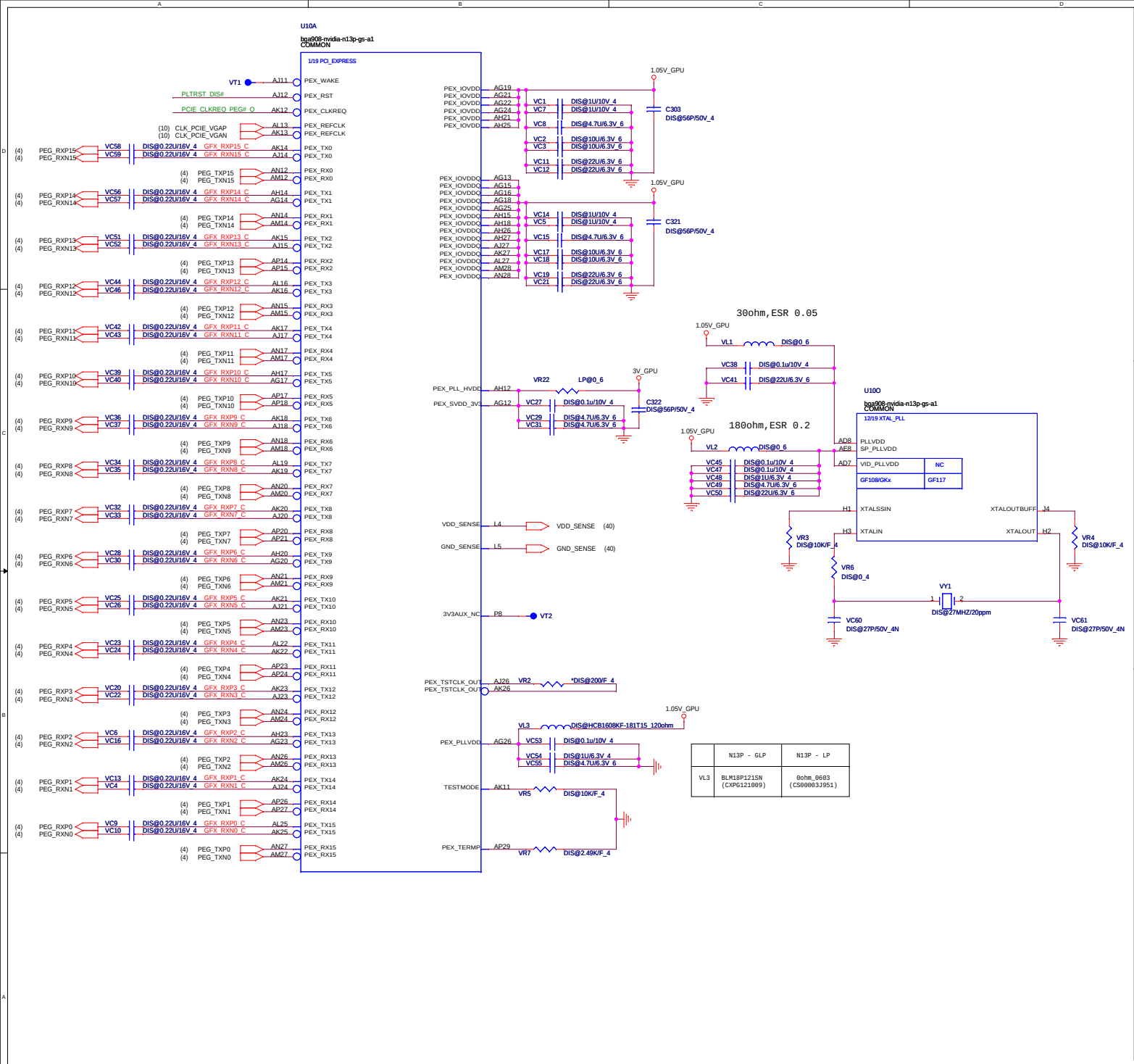
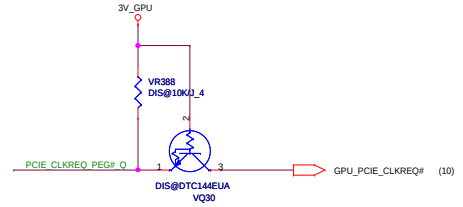
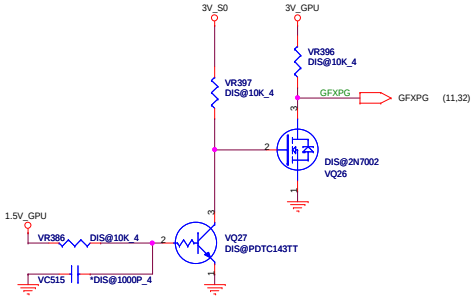


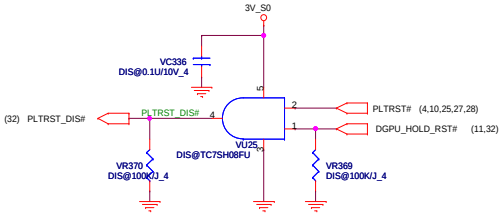
CLK REQ



GPU all PWROK



GPU RST#



1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : FJ8

Size	Document Number	Rev
	N13P PCIE	2A

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(22) FBA_DQ[0..63]
(22) FBA_DQM[0..7]
(22) FBA_WDQSP[0..7]
(22) FBA_RDQSN[0..7]
(22) FBA_CMD[0..31]

(23) FBB_DQ[0..63]
(23) FBB_DQM[0..7]
(23) FBB_WDQSP[0..7]
(23) FBB_RDQSN[0..7]
(23) FBB_CMD[0..31]

U10B
bga908-nvidia-n13p-gs-a1
COMMON
2/19 FBA

U10C
bga908-nvidia-n13p-gs-a1
COMMON
3/19 FBB

	N13P-GLP	N13P-LP
VR111	NA	10Kohm_0402 (CS31002FB26)

VR111 LP@10K/F_4
VC62 DIS@0.1u/10V_4
VC63 LP@0.1u/10V_4
VL4 DIS@bead_30ohm_6
VC64 DIS@0.1u/10V_4
VC65 DIS@22u/6.3V_6
VR18 *DIS@60.4/F_4
VR19 *DIS@60.4/F_4
VR20 *DIS@60.4/F_4
VR21 *DIS@60.4/F_4
1.5V_GPU
1.05V_GPU

VT3 VT4 VT5 VT6 VT7 VT8 VT9 VT10 VT11 VT12

FBA_CMD2 VR8 DIS@10K_4 FBA_ODT_L
FBA_CMD18 VR10 DIS@10K_4 FBA_ODT_H
FBA_CMD3 VR12 DIS@10K_4 FBA_CKE_L
FBA_CMD19 VR14 DIS@10K_4 FBA_CKE_H
FBA_CMD5 VR16 DIS@10K_4 FBA_RST#

FBB_CMD2 VR9 DIS@10K_4 FBB_ODT_L
FBB_CMD18 VR11 DIS@10K_4 FBB_ODT_H
FBB_CMD3 VR13 DIS@10K_4 FBB_CKE_L
FBB_CMD19 VR15 DIS@10K_4 FBB_CKE_H
FBB_CMD5 VR17 DIS@10K_4 FBB_RST#

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : FJ8

Size	Document Number	Rev
	N13P MEM I/F	2A

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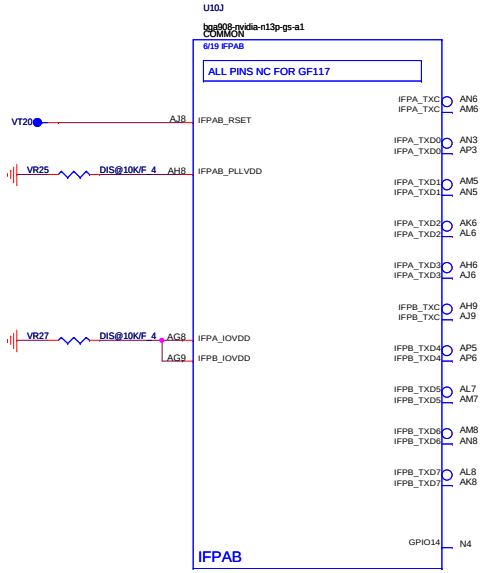
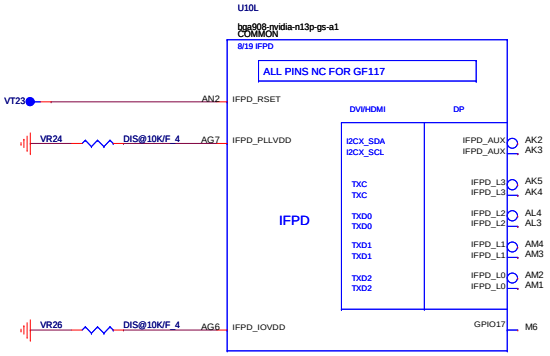
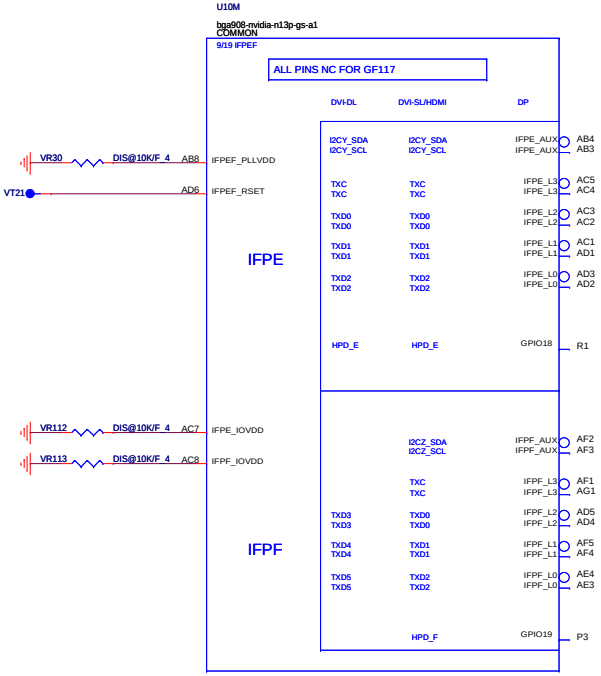
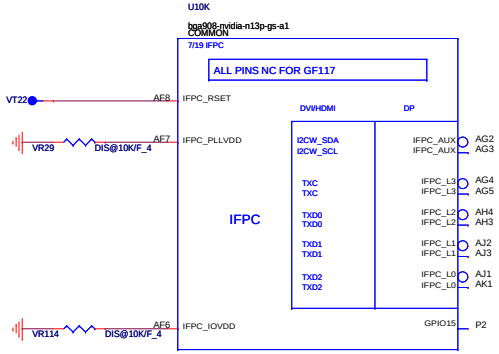
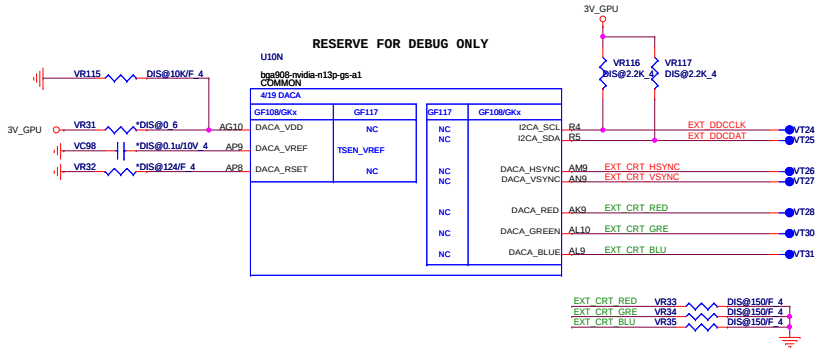








Discrete CRT for Debug



1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : FJ8

Size	Document Number	Rev
	N13P DISPLAY	2A
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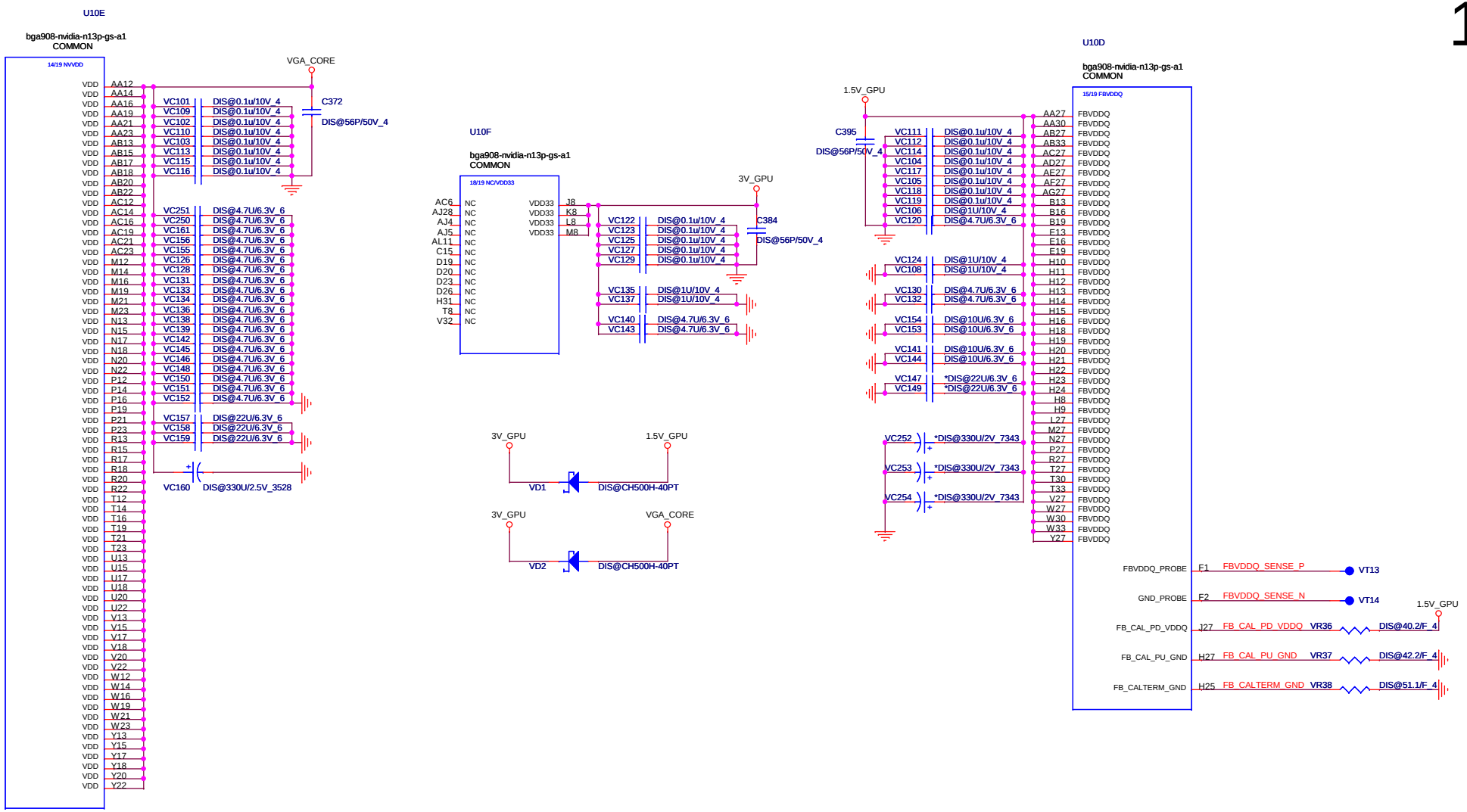

Quanta Computer Inc.		
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Size	Document Number: N13P POWER	Rev: 2A
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U10G

bga908-nvidia-n13p-gs-a1
COMMON

16/19 GND_1/2

A2	GND	GND	AM25
AA17	GND	GND	AN1
AA18	GND	GND	AN10
AA20	GND	GND	AN13
AA22	GND	GND	AN16
AB12	GND	GND	AN19
AB14	GND	GND	AN22
AB16	GND	GND	AN25
AB19	GND	GND	AN30
AB2	GND	GND	AN34
AB21	GND	GND	AN4
A33	GND	GND	AN7
AB23	GND	GND	AP2
AB28	GND	GND	AP33
AB30	GND	GND	B1
AB32	GND	GND	B10
AB5	GND	GND	B22
AB7	GND	GND	B25
AC13	GND	GND	B28
AC15	GND	GND	B31
AC17	GND	GND	B34
AC18	GND	GND	B4
AA13	GND	GND	B7
AC20	GND	GND	C10
AC22	GND	GND	C13
AE2	GND	GND	C19
AE28	GND	GND	C22
AE30	GND	GND	C25
AE32	GND	GND	C28
AE33	GND	GND	C7
AE5	GND	GND	D2
AE7	GND	GND	D31
AH10	GND	GND	D33
AA15	GND	GND	E10
AH13	GND	GND	E22
AH16	GND	GND	E25
AH19	GND	GND	E5
AH2	GND	GND	E7
AH22	GND	GND	F28
AH24	GND	GND	F7
AH28	GND	GND	G10
AH29	GND	GND	G13
AH30	GND	GND	G16
AH32	GND	GND	G19
AH33	GND	GND	G2
AH5	GND	GND	G22
AH7	GND	GND	G25
AJ7	GND	GND	G28
AK10	GND	GND	G3
AK7	GND	GND	G30
AL12	GND	GND	G32
AL14	GND	GND	G33
AL15	GND	GND	G5
AL17	GND	GND	G7
AL18	GND	GND	K2
AL2	GND	GND	K28
AL20	GND	GND	K30
AL21	GND	GND	K32
AL23	GND	GND	K33
AL24	GND	GND	K5
AL26	GND	GND	K7
AL28	GND	GND	M13
AL30	GND	GND	M15
AL32	GND	GND	M17
AL33	GND	GND	M18
AL5	GND	GND	M20
AM13	GND	GND	M22
AM16	GND	GND	N12
AM19	GND	GND	N14
AM22	GND	GND	N16

U10I

bga908-nvidia-n13p-gs-a1
COMMON

17/19 GND_2/2

N19	GND	GND	T28
N2	GND	GND	T32
N21	GND	GND	T5
N23	GND	GND	T7
N28	GND	GND	U12
N30	GND	GND	U14
N32	GND	GND	U16
N33	GND	GND	U19
N5	GND	GND	U21
N7	GND	GND	U23
P13	GND	GND	V12
P15	GND	GND	V14
P17	GND	GND	V16
P18	GND	GND	V19
P20	GND	GND	V21
P22	GND	GND	V23
R12	GND	GND	W13
R14	GND	GND	W15
R16	GND	GND	W17
R19	GND	GND	W18
R21	GND	GND	W20
R23	GND	GND	W22
T13	GND	GND	W28
T15	GND	GND	Y12
T17	GND	GND	Y14
T18	GND	GND	Y16
T2	GND	GND	Y19
T20	GND	GND	Y21
T22	GND	GND	Y23
AG11	GND	GND	AH11
	GND_OPT	GND_OPT	C16
	GND_OPT	GND_OPT	W32

Optional CMD GNDs (2)
NC for 4-Lyr cards

U10H

bga908-nvidia-n13p-gs-a1
COMMON

10/19 XVDD

CONFIGURABLE
POWER
CHANNELS

XVDD	U1	
XVDD	U2	
XVDD	U3	
XVDD	U4	
XVDD	U5	
XVDD	U6	
XVDD	U7	
XVDD	U8	
XVDD	V1	
XVDD	V2	
XVDD	V3	
XVDD	V4	
XVDD	V5	
XVDD	V6	
XVDD	V7	
XVDD	V8	
XVDD	W2	
XVDD	W3	
XVDD	W4	
XVDD	W5	
XVDD	W7	
XVDD	W8	
XVDD	Y1	
XVDD	Y2	
XVDD	Y3	
XVDD	Y4	
XVDD	Y5	
XVDD	Y6	
XVDD	Y7	
XVDD	Y8	
XVDD	AA1	
XVDD	AA2	
XVDD	AA3	
XVDD	AA4	
XVDD	AA5	
XVDD	AA6	
XVDD	AA7	
XVDD	AA8	

To be configured as needed on the PCB

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
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Size	Document Number	Rev
	N13P GND	2A

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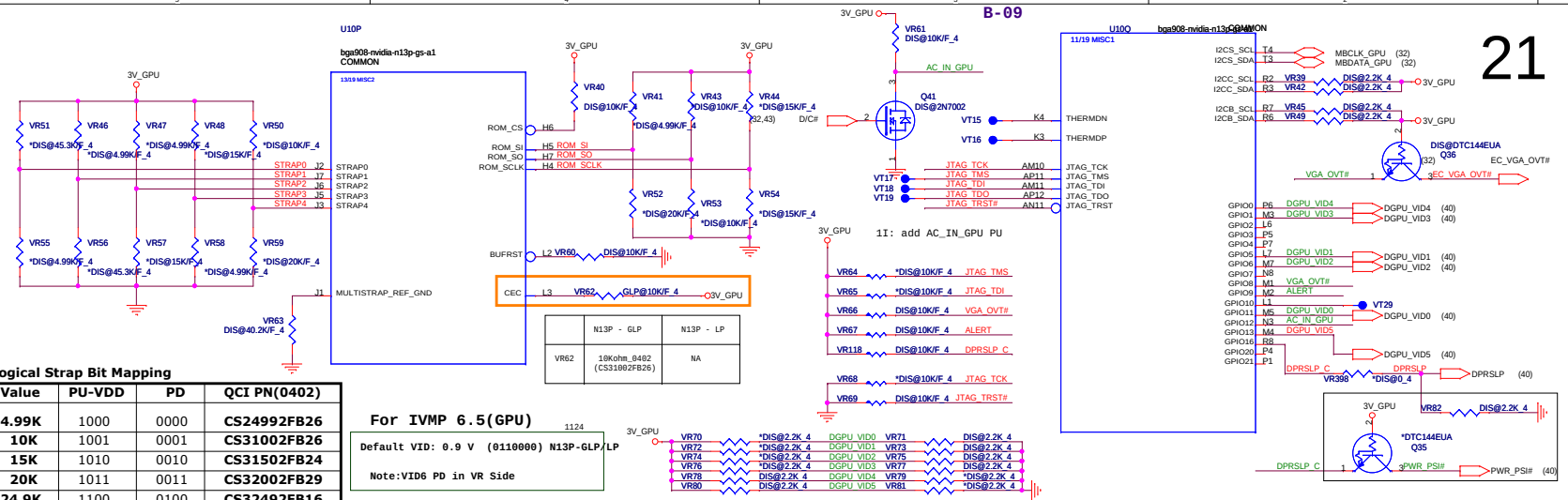

	N13P - GLP	N13P - LP
VR62	10Kohm_0402 (CS31002FB26)	NA

Logical Strap Bit Mapping

Value	PU-VDD	PD	QCI PN(0402)
4.99K	1000	0000	CS24992FB26
10K	1001	0001	CS31002FB26
15K	1010	0010	CS31502FB24
20K	1011	0011	CS32002FB29
24.9K	1100	0100	CS32492FB16
30.1K	1101	0101	CS33012FB18
34.8K	1110	0110	CS33482FB22
45.3K	1111	0111	CS34532FB18

For IVMP 6.5(GPU)

1124

Default VID: 0.9 V (0110000) N13P-GLP/LP

Note:VID6 PD in VR Side

VRAM(DDR3) Configuration Table

RAMCFG [3:0]	DESCRIPTION (Vendor P/N)	Vendor	QCI P/N	ROM_SI
0111	128*16-900MHz K4W2G1646C-HC11	Samsung	AKD5MGWT500	PD 45.3K
0110	128*16-900MHz H5TQ2G63BFR-11C	Hinyx	AKD5MGWTW00	PD 35K
0010	64*16-900MHz H5TQ1G63DFR-11C	Hinyx	AKD5LZWTW02	PD 15K
0011	64*16-900MHz K4W1G1646G-BC11	Samsung	AKD5EGGT500	PD 20K

		GLP 1GB HYN	GLP 1GB SAM	LP 2GB HYN	LP 2GB SAM	GLP 2GB HYN	GLP 2GB SAM
ROM_SCLK	VR44	NA	NA	CS31502FB24	CS31502FB24	NA	NA
	VR54	CS31502FB24	CS31502FB24	NA	NA	CS31502FB24	CS31502FB24
ROM_SI	VR41	NA	NA	NA	NA	NA	NA
	VR52	CS31502FB24	CS32002FB29	CS33482FB22	CS34532FB18	CS33482FB22	CS34532FB18
ROM_SO	VR43	NA	NA	NA	NA	NA	NA
	VR53	CS31002FB26	CS31002FB26	CS33012FB18	CS33012FB18	CS31002FB26	CS31002FB26
STRAP0	VR51	CS34532FB18	CS34532FB18	CS34532FB18	CS34532FB18	CS34532FB18	CS34532FB18
	VR55	NA	NA	NA	NA	NA	NA
STRAP1	VR46	NA	NA	NA	NA	NA	NA
	VR56	CS34532FB18	CS34532FB18	CS33482FB22	CS33482FB22	CS34532FB18	CS34532FB18
STRAP2	VR47	CS24992FB26	CS24992FB26	CS33482FB22	CS33482FB22	CS24992FB26	CS24992FB26
	VR57	NA	NA	NA	NA	NA	NA
STRAP3	VR48	NA	NA	NA	NA	NA	NA
	VR58	CS24992FB26	CS24992FB26	CS24992FB26	CS24992FB26	CS24992FB26	CS24992FB26
STRAP4	VR50	NA	NA	NA	NA	NA	NA
	VR59	NA	NA	CS34532FB18	CS34532FB18	NA	NA

N13P-LP	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	Value	Note
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG-GLP	PEX_PLL_EN_TERM	1000	LP:ES Samples 5K PU(0X0FDB)
			PCI_DEVIDE[5]-LP		0010	GLP:ES Samples 15K PD(0X0DFE)
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	0110	LP K4W2G1646C-HC11 45.3K PD
					0111	LP H5TQ2G63BFR-11C :35K PD
					0010	GLP H5TQ1G63DFR-11C :15K PD
					0011	GLP K4W1G1646G-BC11 :20K PD
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	1001	10K PU
	FB[1]-LP	FB[0]-LP	I2CS ADDR:0X9E		0001	10K PD
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111	EDID is used :45K PU
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110	LP:notebook default:35K PD
					0111	GLP: Reserve:45.3K PD
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	0011	ES Samples LP:20K PU(0X0FDB)
					1000	ES Samples GLP:45.3K PU(0X0DEF)
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000	Not in use :5K PD
STRAP4	RESERVED	Reserve PCIE_SPEED-LP	PCIE_MAX_SPEED	DP_PLL_VDD3V	0001	LP:10K PD GLP: NA

*LP QS Samples :5K PD(0X0FD3)

GLP:MP Samples:15K PD(0X0DE8)

*LP QS Samples : 20K PU(0X0FD3)

*GLP:MP Samples :5K PU(0X0DE8)

GPIO ASSIGNMENTS

GPIO	I/O	USAGE	
0	OUT	Y	NVVDD VID4
1	OUT	Y	NVVDD VID3
2	OUT	N	PANEL BACKLIGHT PWM
3	OUT	N	PANEL POWER ENABLE
4	OUT	N	PANEL BACKLIGHT ENABLE
5	OUT	Y	NVVDD VID1
6	OUT	Y	NVVDD VID2
7	OUT	N	3D STEREO
8	I/O	Y	GPU Overtemp
9	I/O	Y	GPU ALERT
10	OUT	N	FB Vref Control
11	OUT	Y	NVVDD VID0
12	IN	N	PWR_Level AC Detect
13	OUT	Y	NVVDD VID5
14	IN	N	HPD for IFP AB
15	IN	N	HPD for IFP C
16	OUT	N	MEM_VDD_CTL
17	OUT	N	HPD for IFP D
18	OUT	N	HPD for IFP E
19	OUT	N	HPD for IFP F
20	OUT	N	
21	OUT	N	

Quanta Computer Inc.

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Size | Document Number: N13P STRAP/GPIO | Rev 2A

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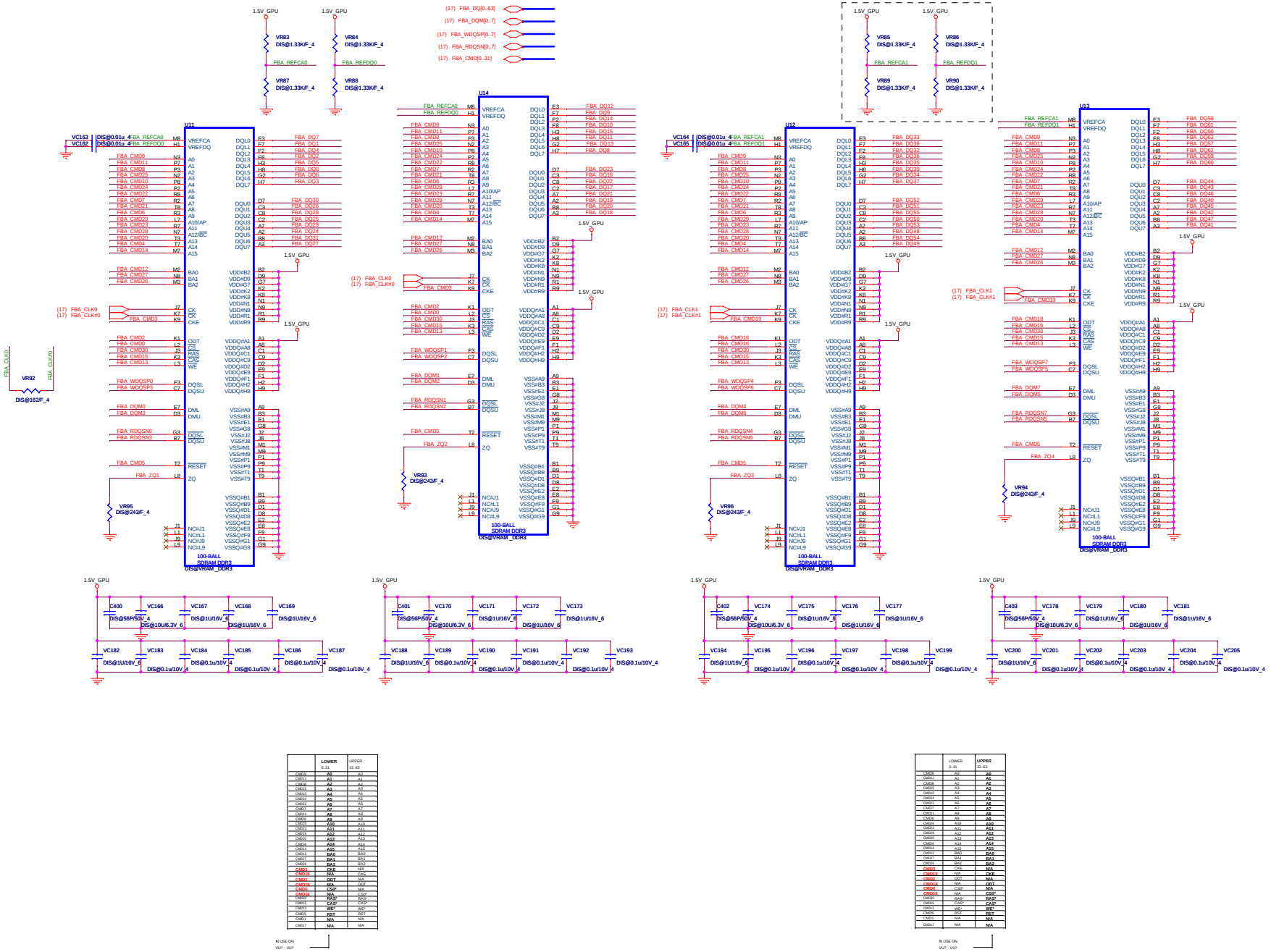
SAM : AKD5EGGT500
HYU : AKD5LZWTW02



	LOWER 0..31	UPPER 32..63
CMD0	A0	A0
CMD1	A1	A1
CMD2	A2	A2
CMD3	A3	A3
CMD4	A4	A4
CMD5	A5	A5
CMD6	A6	A6
CMD7	A7	A7
CMD8	A8	A8
CMD9	A9	A9
CMD10	A10	A10
CMD11	A11	A11
CMD12	A12	A12
CMD13	A13	A13
CMD14	A14	A14
CMD15	A15	A15
CMD16	BA0	BA0
CMD17	BA1	BA1
CMD18	BA2	BA2
CMD19	CKE	N/A
CMD20	N/A	CKE
CMD21	ODT	N/A
CMD22	N/A	ODT
CMD23	CS#	N/A
CMD24	N/A	CS#
CMD25	RAS#	RAS#
CMD26	CAS#	CAS#
CMD27	WE#	WE#
CMD28	RST	RST
CMD29	N/A	N/A
CMD30	N/A	N/A
CMD31	N/A	N/A

IN USE ON VU? - VU?

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

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N13P VRAM-A DDR3 | 2A
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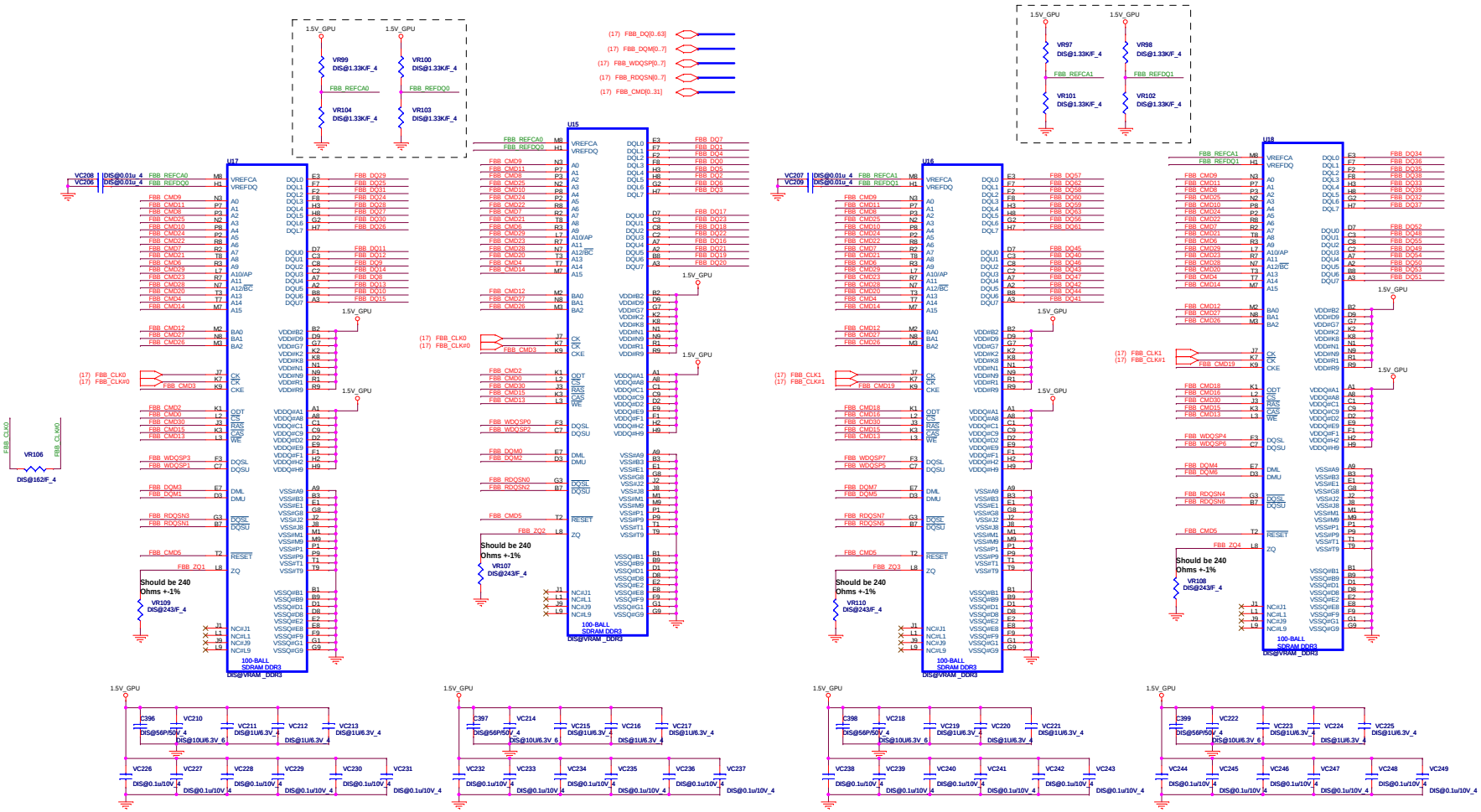
SAM : AKD5EGGT500
HYU : AKD5LZWTW02



	LOWER 0..31	UPPER 32..63
CMD0	A0	A0
CMD1	A1	A1
CMD2	A2	A2
CMD3	A3	A3
CMD4	A4	A4
CMD5	A5	A5
CMD6	A6	A6
CMD7	A7	A7
CMD8	A8	A8
CMD9	A9	A9
CMD10	A10	A10
CMD11	A11	A11
CMD12	A12	A12
CMD13	A13	A13
CMD14	A14	A14
CMD15	A15	A15
CMD16	BA0	BA0
CMD17	BA1	BA1
CMD18	BA2	BA2
CMD19	CKE	N/A
CMD20	N/A	CKE
CMD21	ODT	N/A
CMD22	N/A	ODT
CMD23	CS#	N/A
CMD24	N/A	CS#
CMD25	RAS#	N/A
CMD26	CAS#	RAS#
CMD27	WE#	CAS#
CMD28	RST	WE#
CMD29	N/A	RST
CMD30	N/A	N/A
CMD31	N/A	N/A

IN USE ON VU7 - VU7

	LOWER 0..31	UPPER 32..63
CMD0	A0	A0
CMD1	A1	A1
CMD2	A2	A2
CMD3	A3	A3
CMD4	A4	A4
CMD5	A5	A5
CMD6	A6	A6
CMD7	A7	A7
CMD8	A8	A8
CMD9	A9	A9
CMD10	A10	A10
CMD11	A11	A11
CMD12	A12	A12
CMD13	A13	A13
CMD14	A14	A14
CMD15	A15	A15
CMD16	BA0	BA0
CMD17	BA1	BA1
CMD18	BA2	BA2
CMD19	CKE	N/A
CMD20	N/A	CKE
CMD21	ODT	N/A
CMD22	N/A	ODT
CMD23	CS#	N/A
CMD24	N/A	CS#
CMD25	RAS#	N/A
CMD26	CAS#	RAS#
CMD27	WE#	CAS#
CMD28	RST	WE#
CMD29	N/A	RST
CMD30	N/A	N/A
CMD31	N/A	N/A

IN USE ON VU7 - VU7

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
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	N13P VRAM-B DDR3	2A

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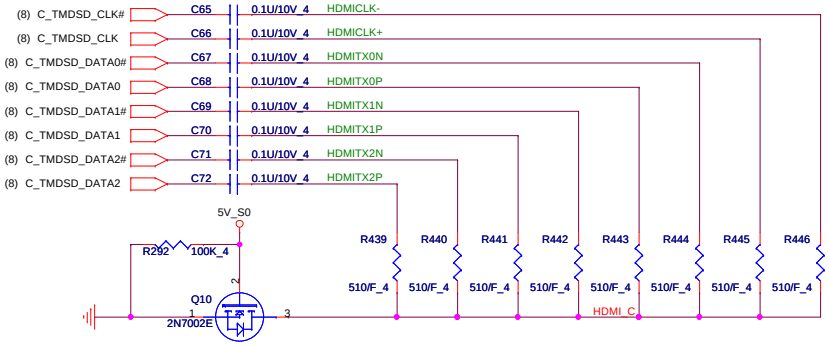
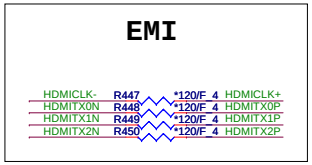
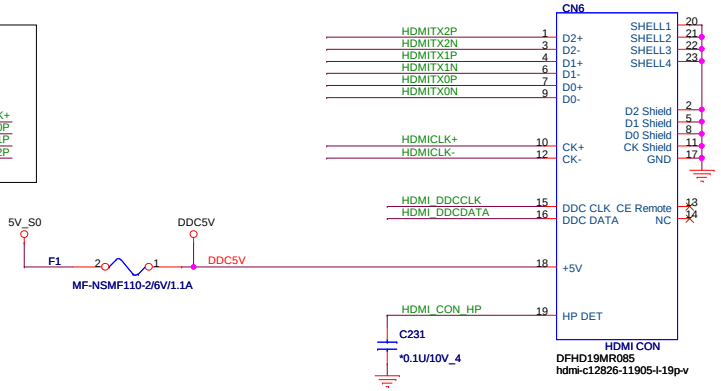


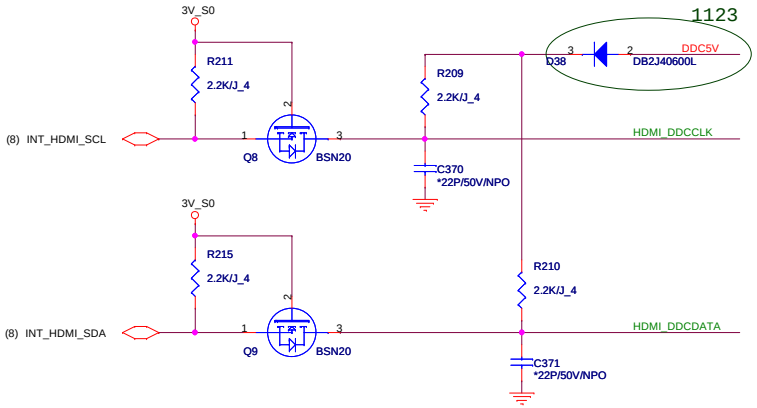
EMI



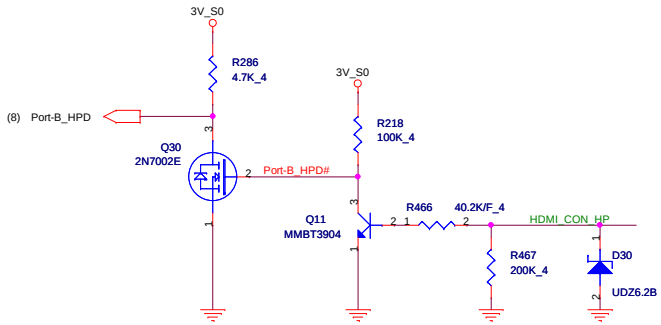
HDMI Conn



DDC Level Shift

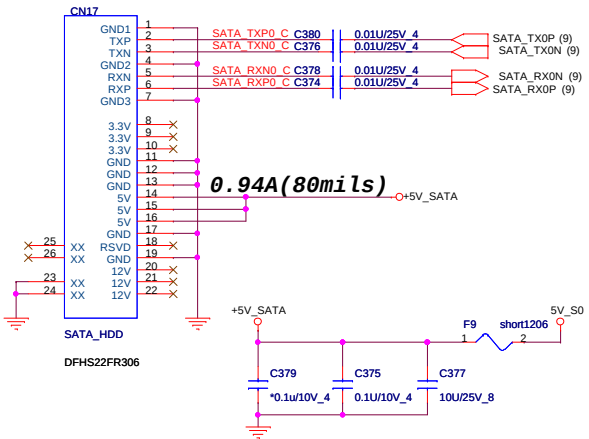


HPD

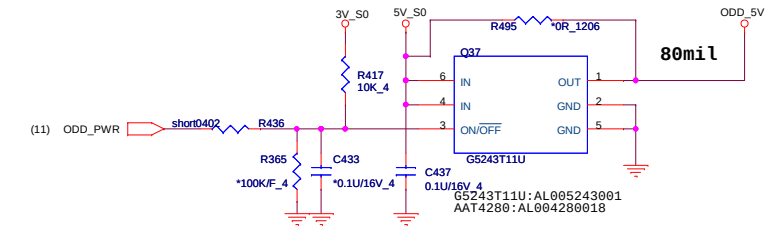


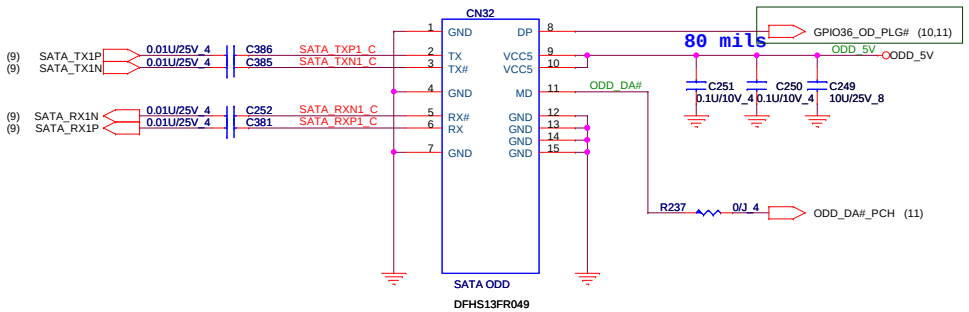
2.5" SATA HDD

DFHS22FR306
DFHS22FR282



SATA ODD





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	DMI/HDD/ODD	2A

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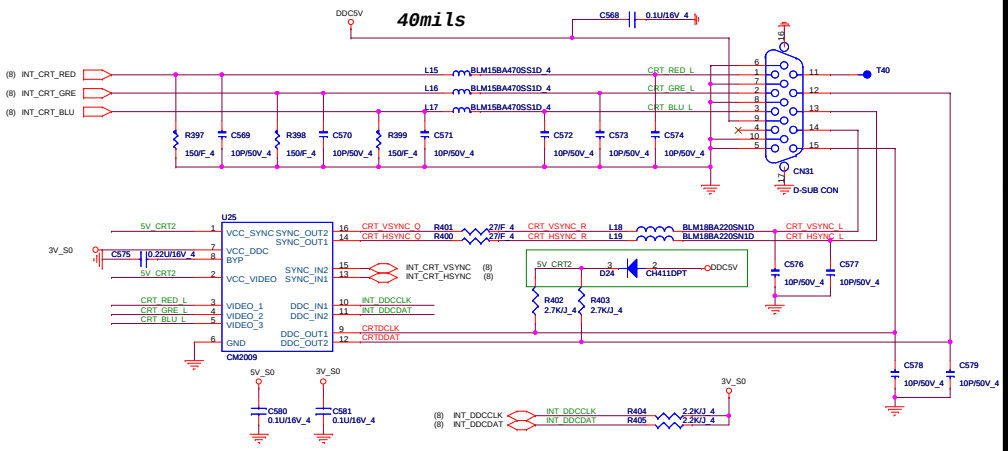
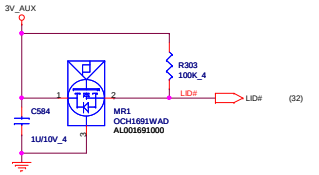
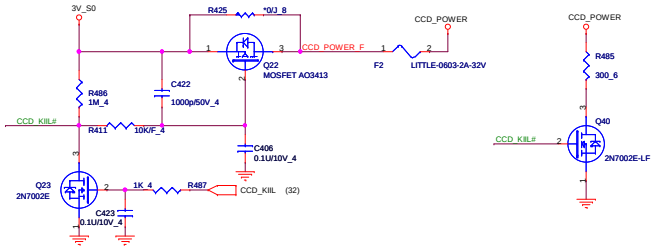
CRT CONN/DDC LEVEL SHIFT



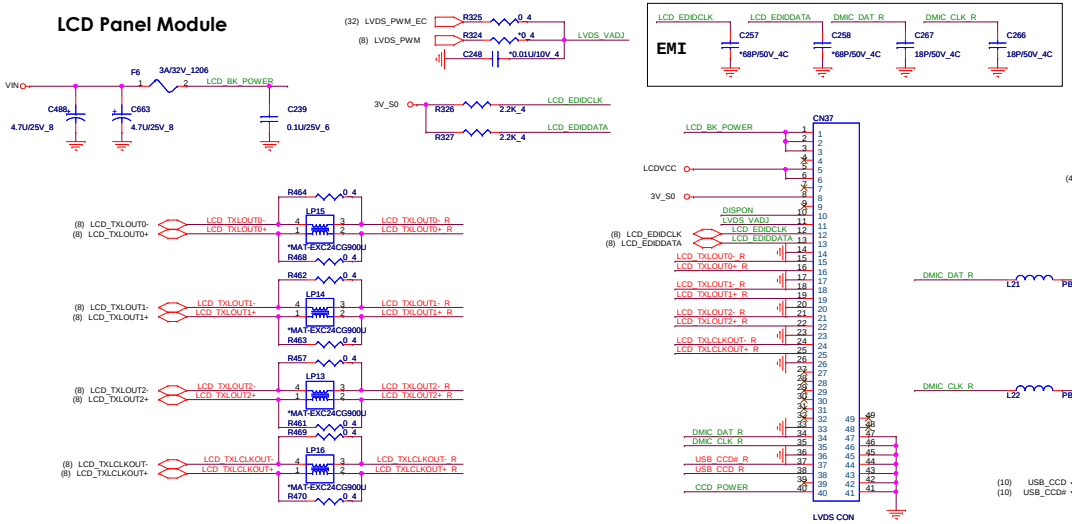
HALL SENSOR



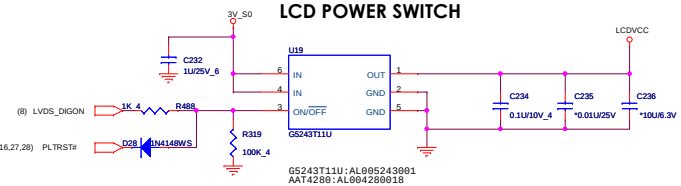
CCD KILL



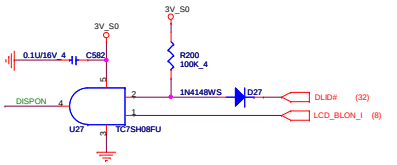
LCD Panel Module

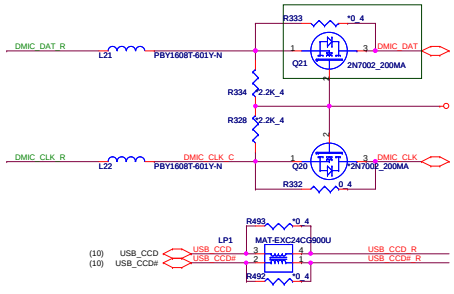


LCD POWER SWITCH



PANEL BACKLIGHT CONTROL





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	LVDS/CCD/CRT	2A

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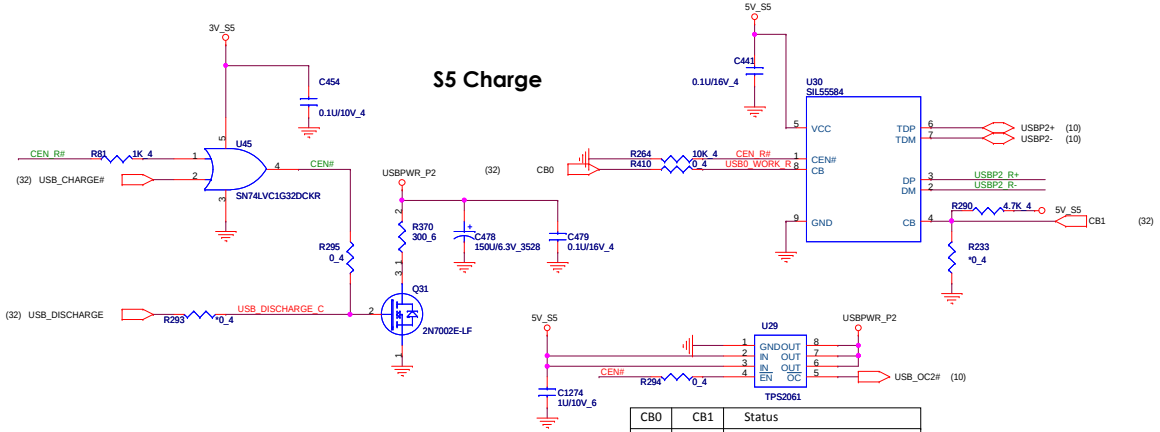
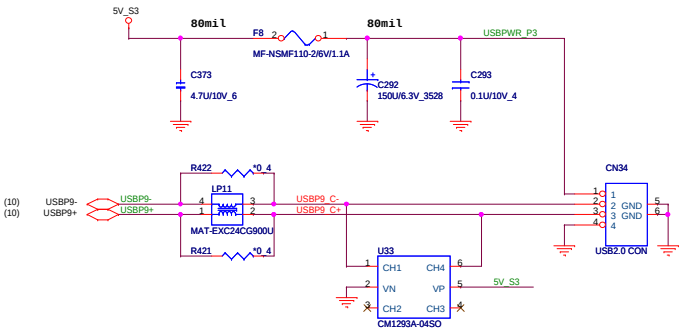
S5 Charge



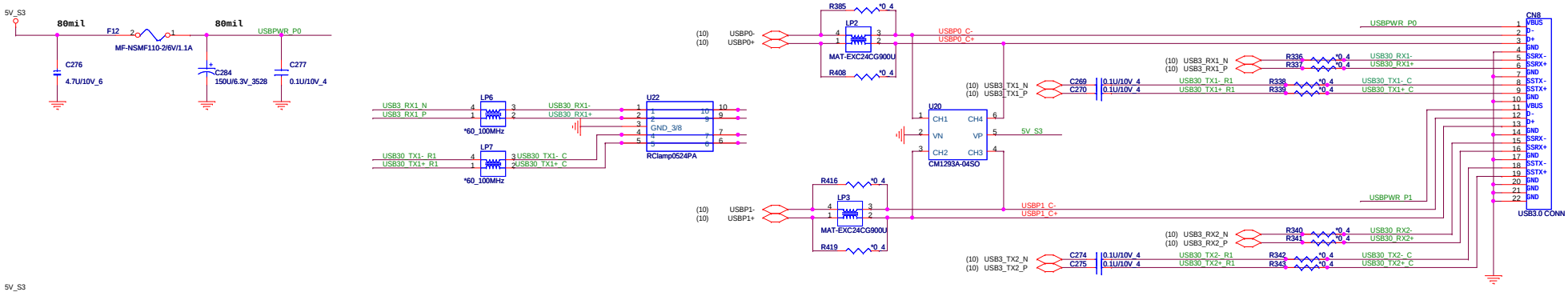
CB0	CB1	Status
0	0	Auto Dection Charge Mode
0	1	Force Dedicated Charger Mode
1	0	Pass Through Mode
1	1	Pass Through Mode with CDP

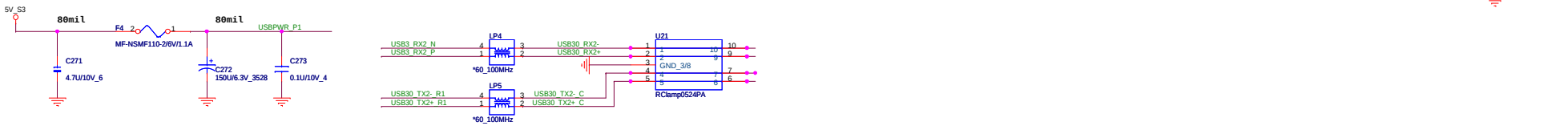
USB 2.0 CONN



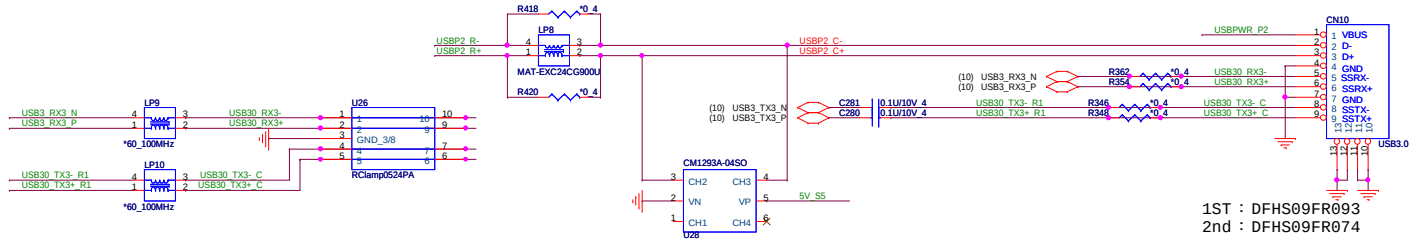
USB 3.0 CONN

SIT : DFHS18FR021
FOX : DFHS18FR019





USB 3.0 CONN (S5 Charge)



1ST : DFHS09FR093
2nd : DFHS09FR074

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	USB 3.0/USB 2.0	2A
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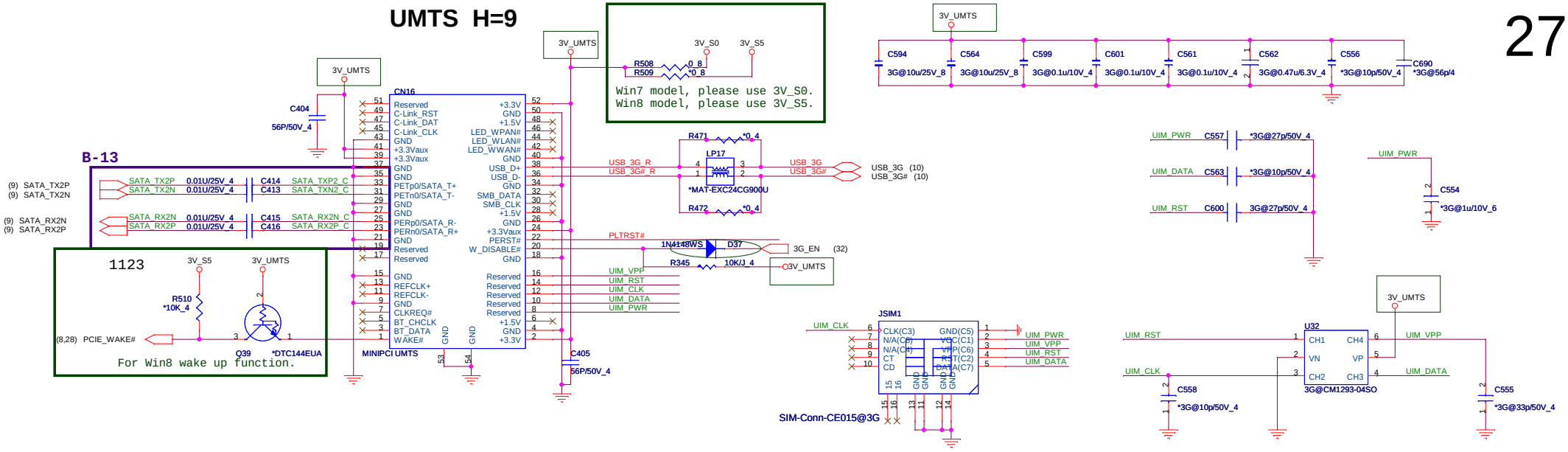
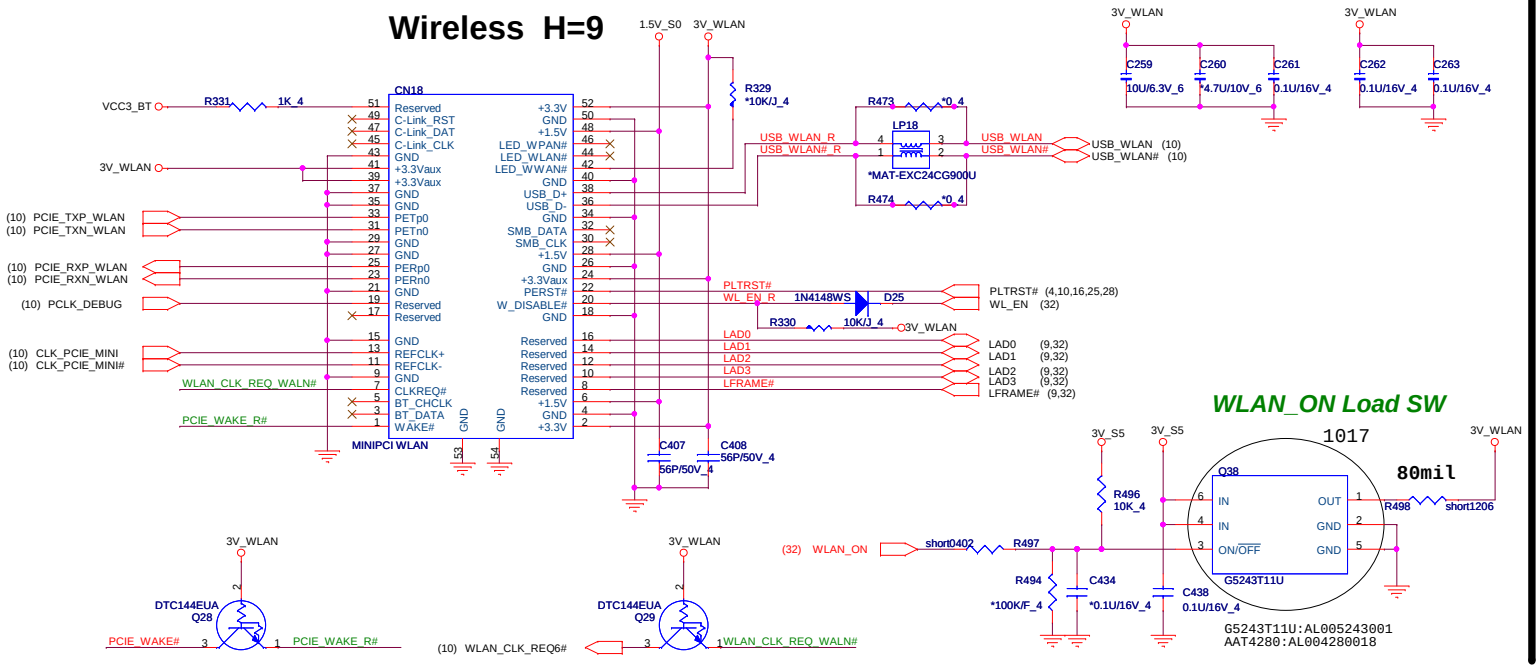
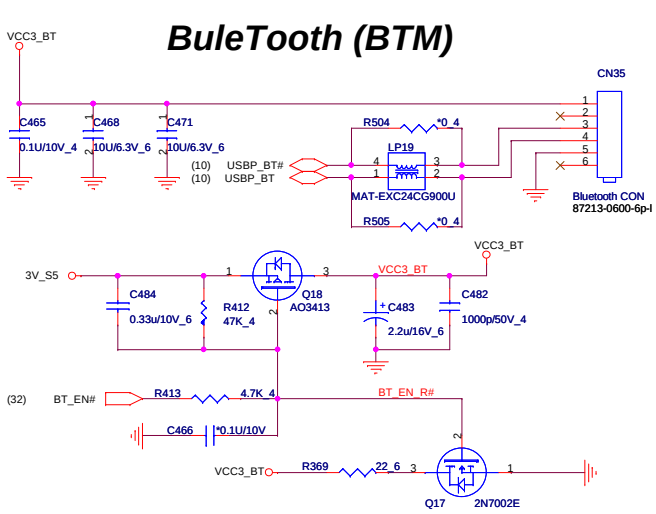
UMTS H=9



Wireless H=9



BuleTooth (BTM)



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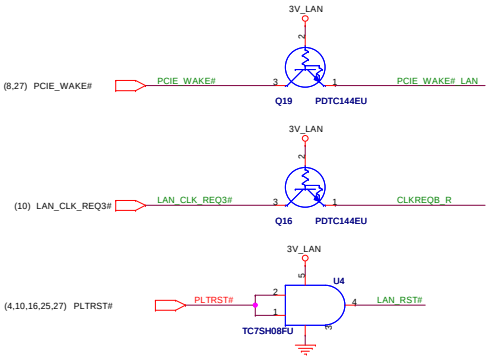

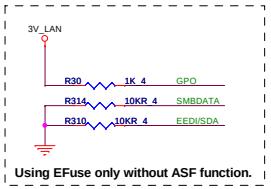

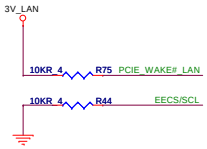

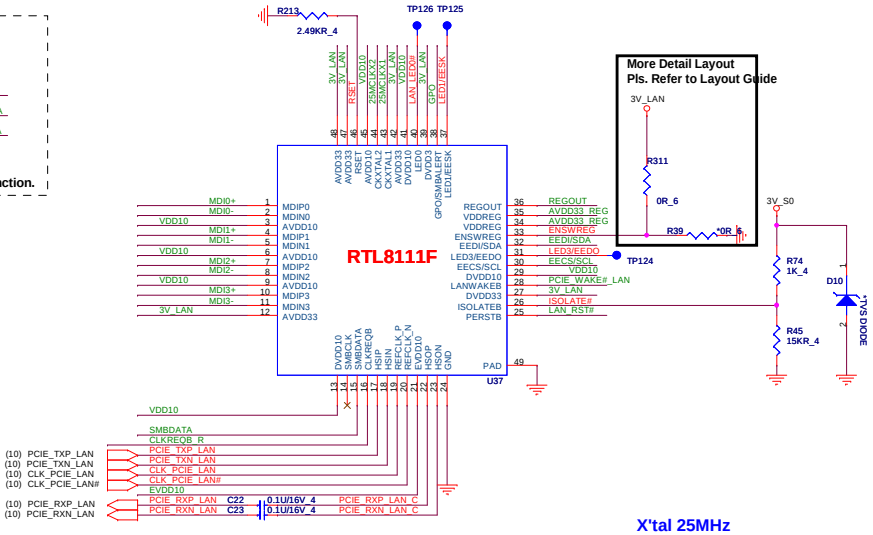

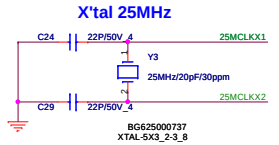

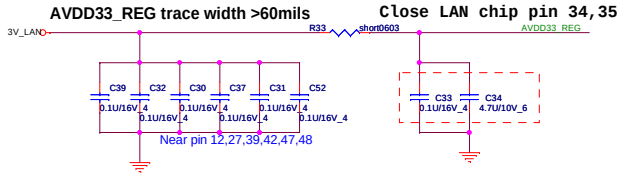

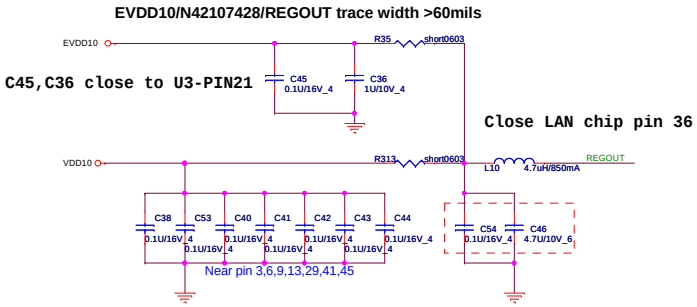

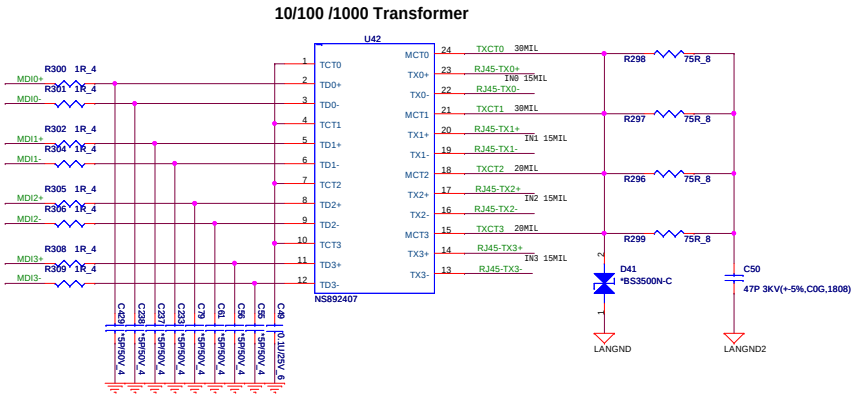

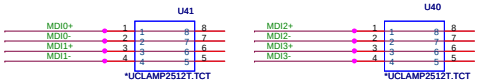

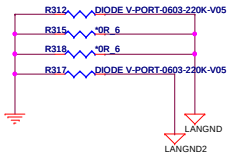

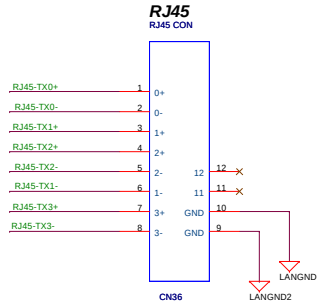

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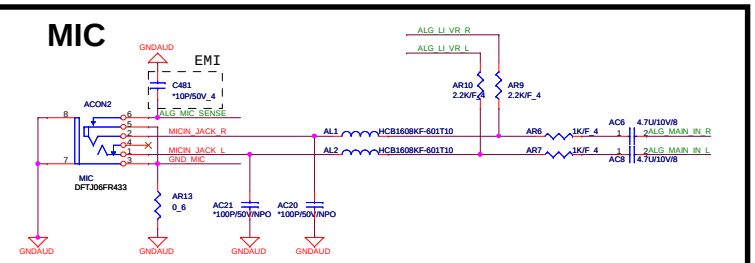
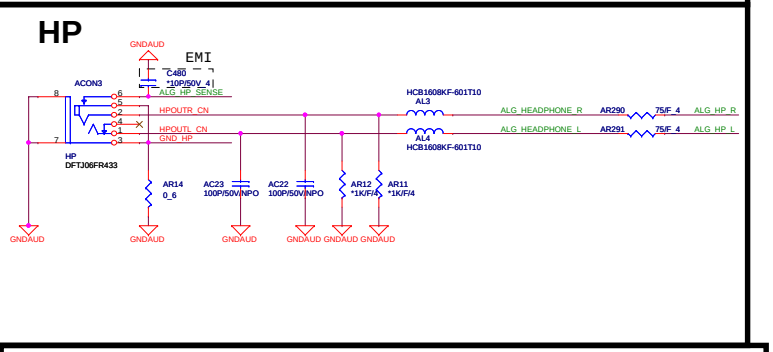
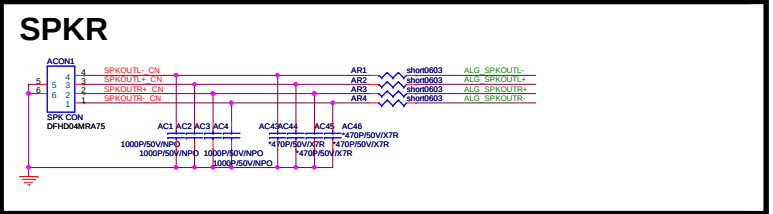
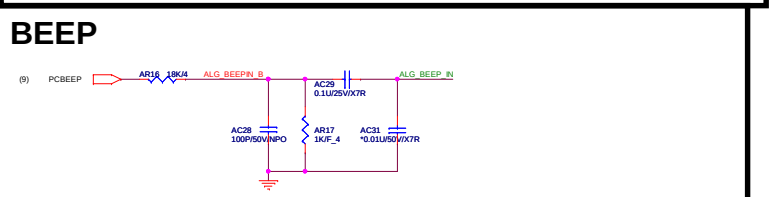
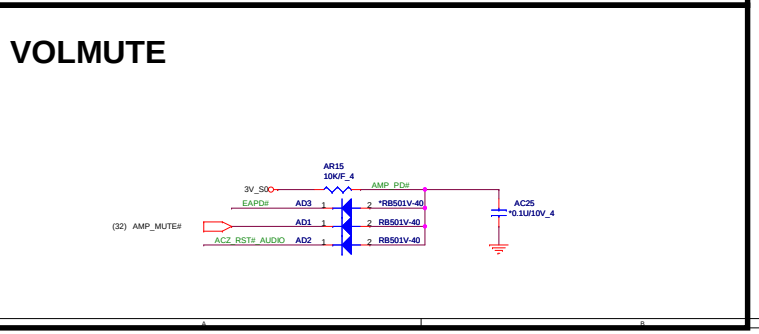
Codec ALC269-VC3

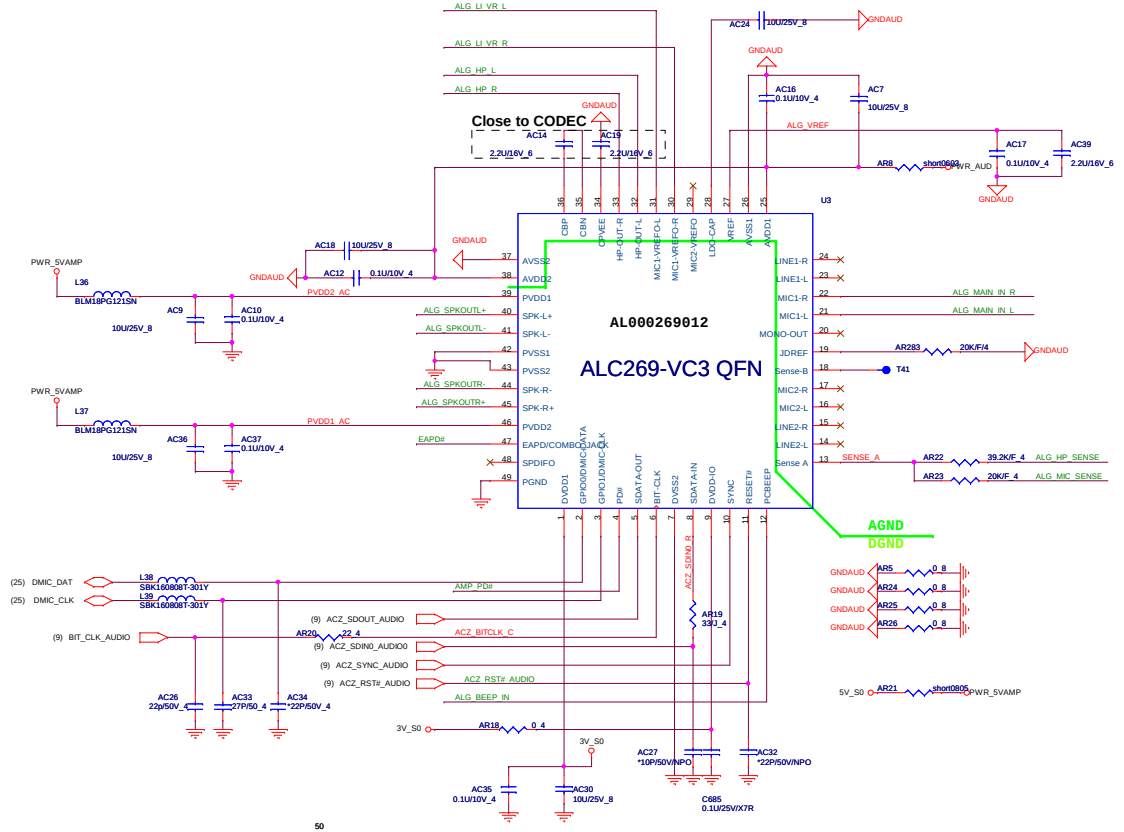


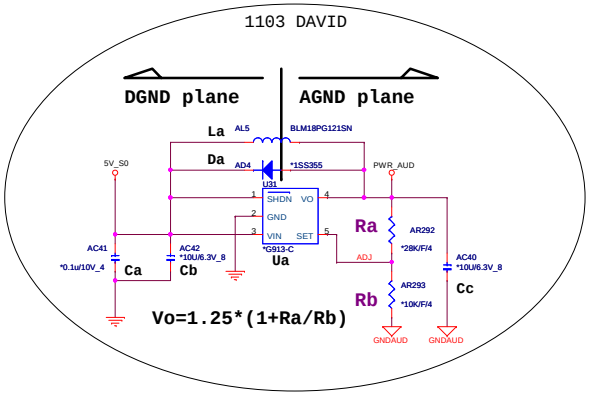


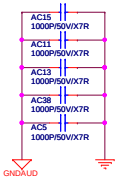












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	CODEC (ALC269Q-VC3)	2A

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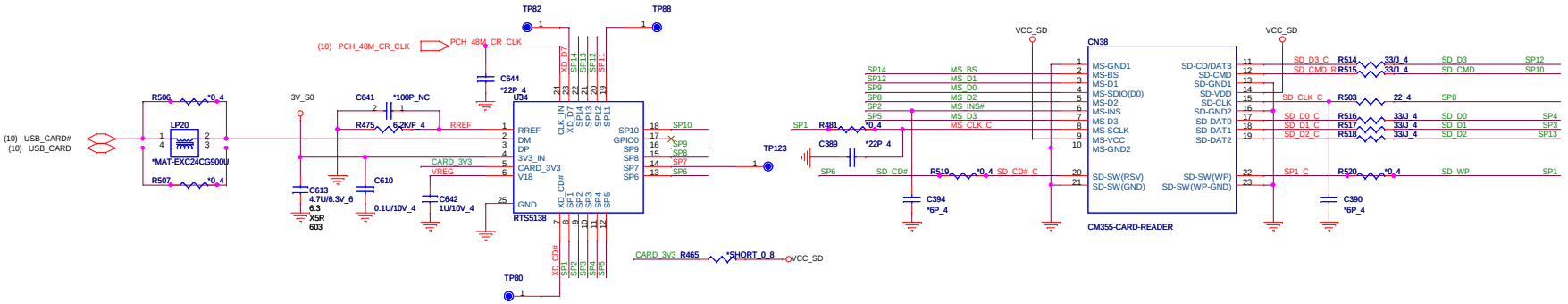
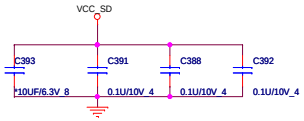
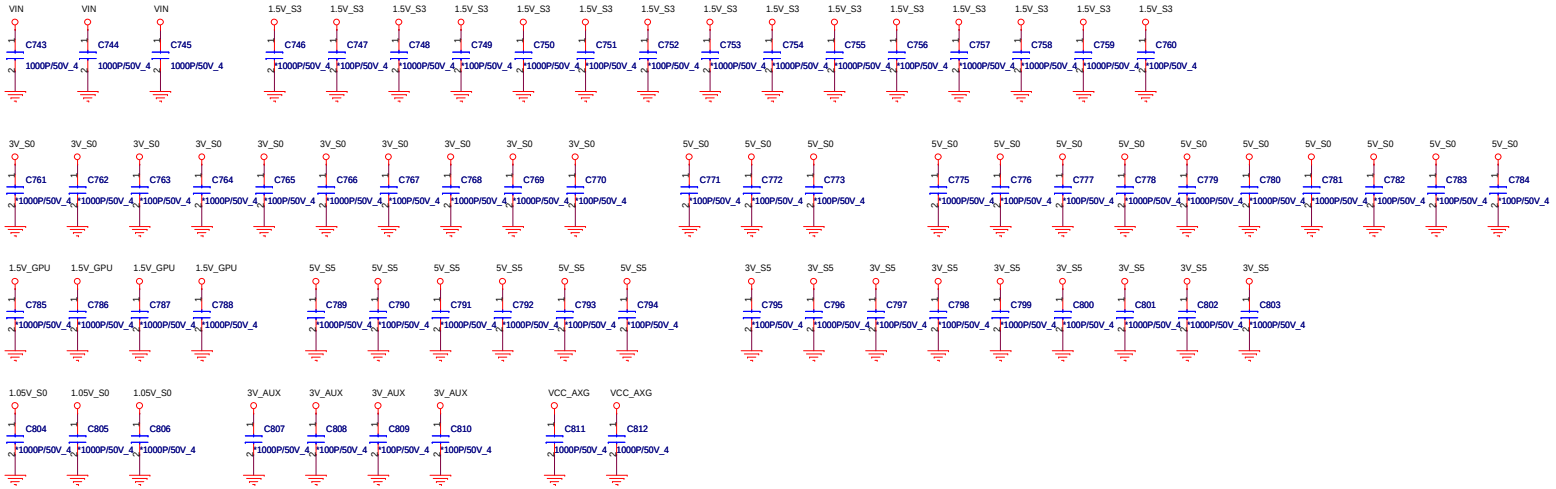




SP1	SD_WP	MS_CLK
SP2		MS_INS#
SP3	SD_D1	
SP4	SD_D0	
SP5		MS_D3
SP6	SD_CD#	
SP8	SD_CLK	MS_D2
SP9		MS_D0
SP10	SD_CMD	
SP12	SD_D3	MS_D1
SP13	SD_D2	
SP14		MS_BS



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	NEW CARD/CARD READER	2A
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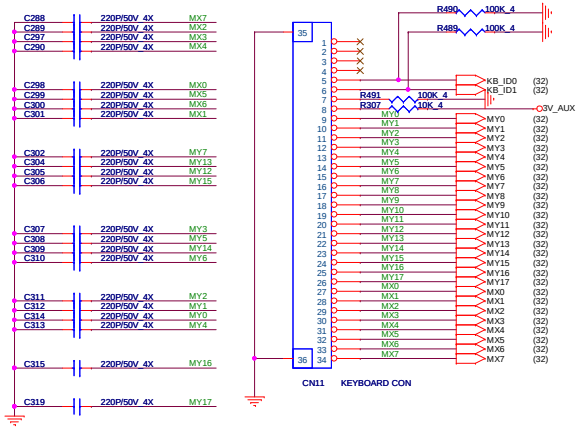
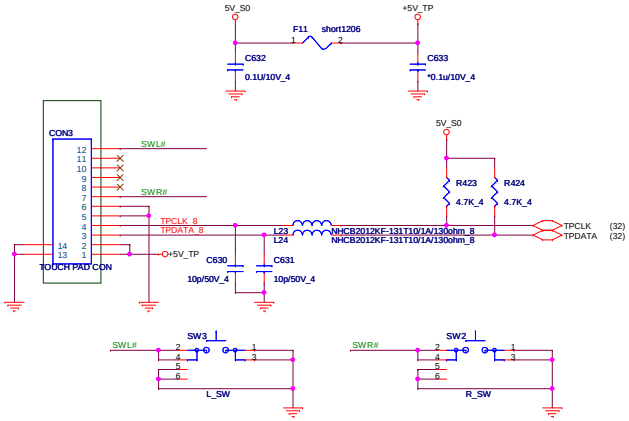
INT KeyBoard

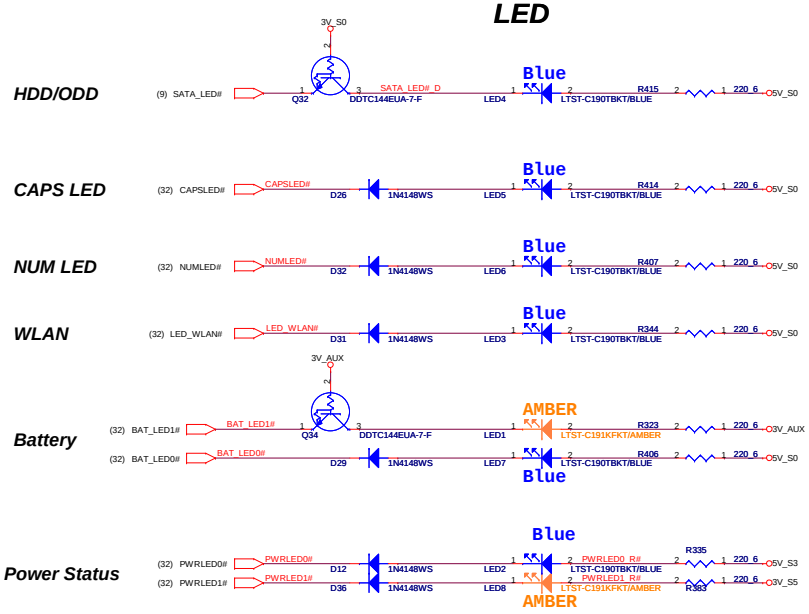


	R490 ID0	R489 ID1	R491 ID2	R307 KB_ID
UK	1	0	0	1
US	0	1	0	1
JP	1	1	0	1

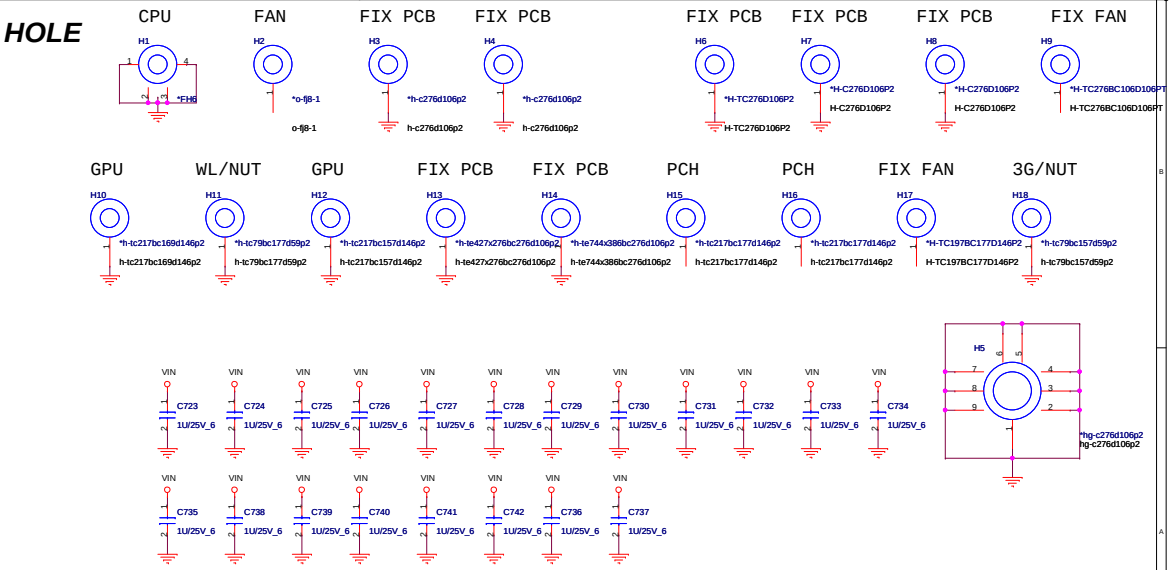
Touch Pad



LED



HOLE

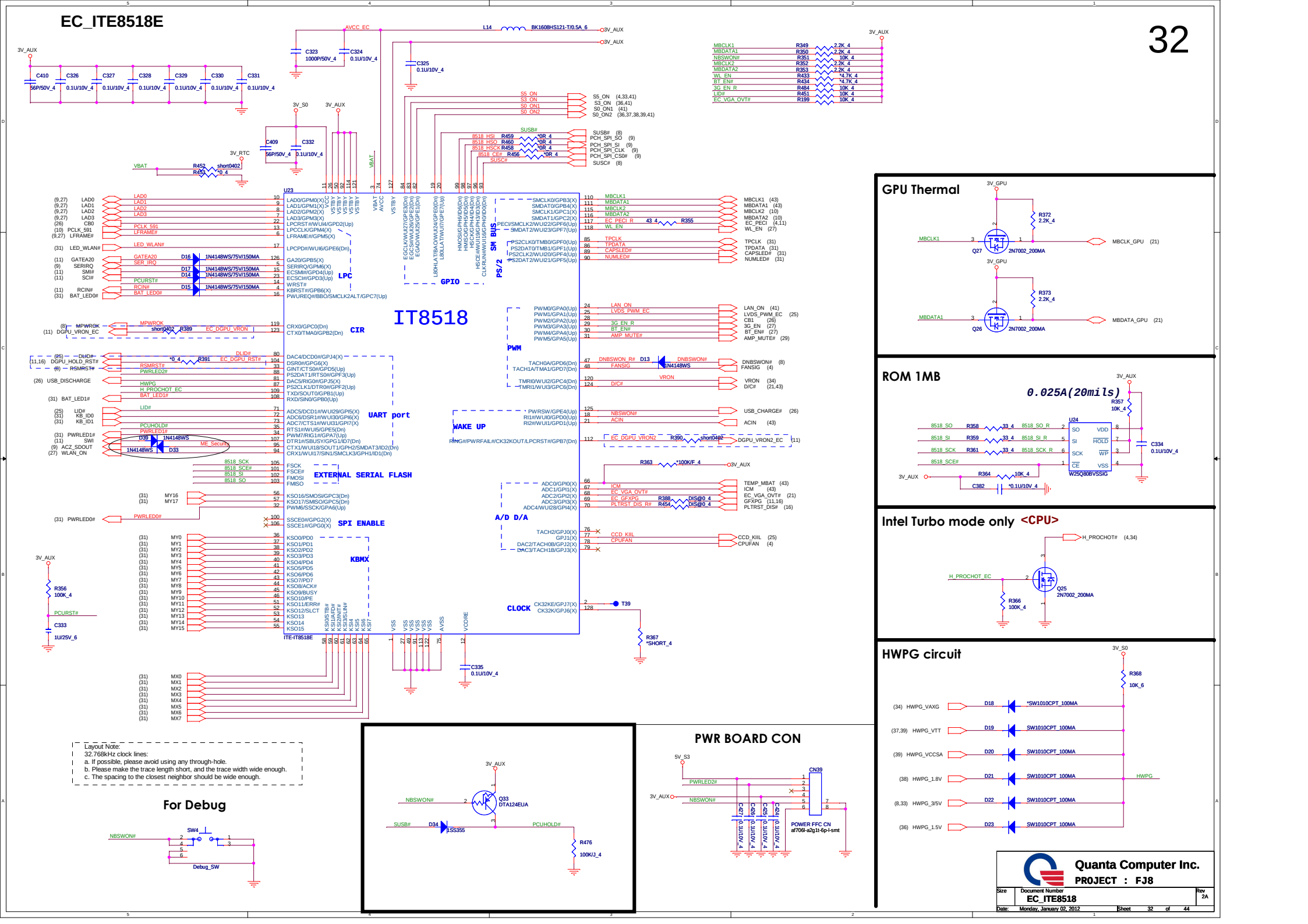


Quanta Computer Inc.
PROJECT : FJ8

Size	Document Number	Rev
	TPM/KB/TP/LED/HOLE	2A

Date: Monday, January 02, 2012 Sheet 31 of 44

EC_ITE8518E



GPU Thermal

ROM 1MB

Intel Turbo mode only <CPU>

HWPG circuit

Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.

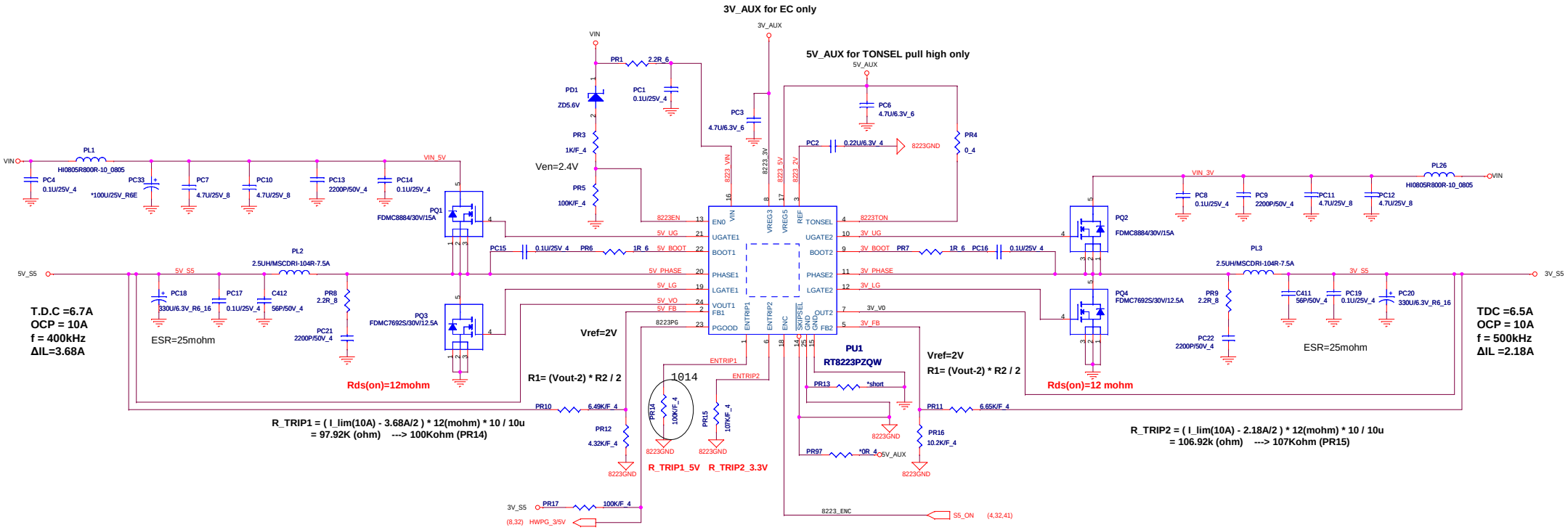
For Debug

PWR BOARD CON

Quanta Computer Inc.
PROJECT : FJ8

Size	Document Number	Rev
	EC_ITE8518	2A
Date: Monday, January 02, 2012	Sheet 32 of 44	

System 3V_S5 and 5V_S5 (RT8223PZQW)



Iripple=(Vin-Vout)*Vout/(Vin*L*f)

O.C.P setup information

Output	Mos Rds_on	I_OCP	OC_ΔIL(A)	Freq(KHz)	Inductor	R_TRIP
5V	17.5m_Max	10	3.68	400	2.5uH	100K
3.3V	17.5m_Max	10	2.18	500	2.5uH	107K

L/S Mosfet parameter

Mosfet	Package	ID (Ta=25C)	Rds_on_max
Si4134DY	SO-8	9.9A/14A	17.5m
AO4712	SO-8	10A/11.2A	18.0m
AO4710	SO-8	11A/12.7A	14.2m
AP4438GSM	SO-8	7A/11.7A	18.0m
DMG4812	SO-8	9.6A/10.7A	18.5m
AON7702	DFN3x3	11A/20A	14.0m
FDMC7692S	DFN3x3	12A/30A	12.0m

Power On sequencing

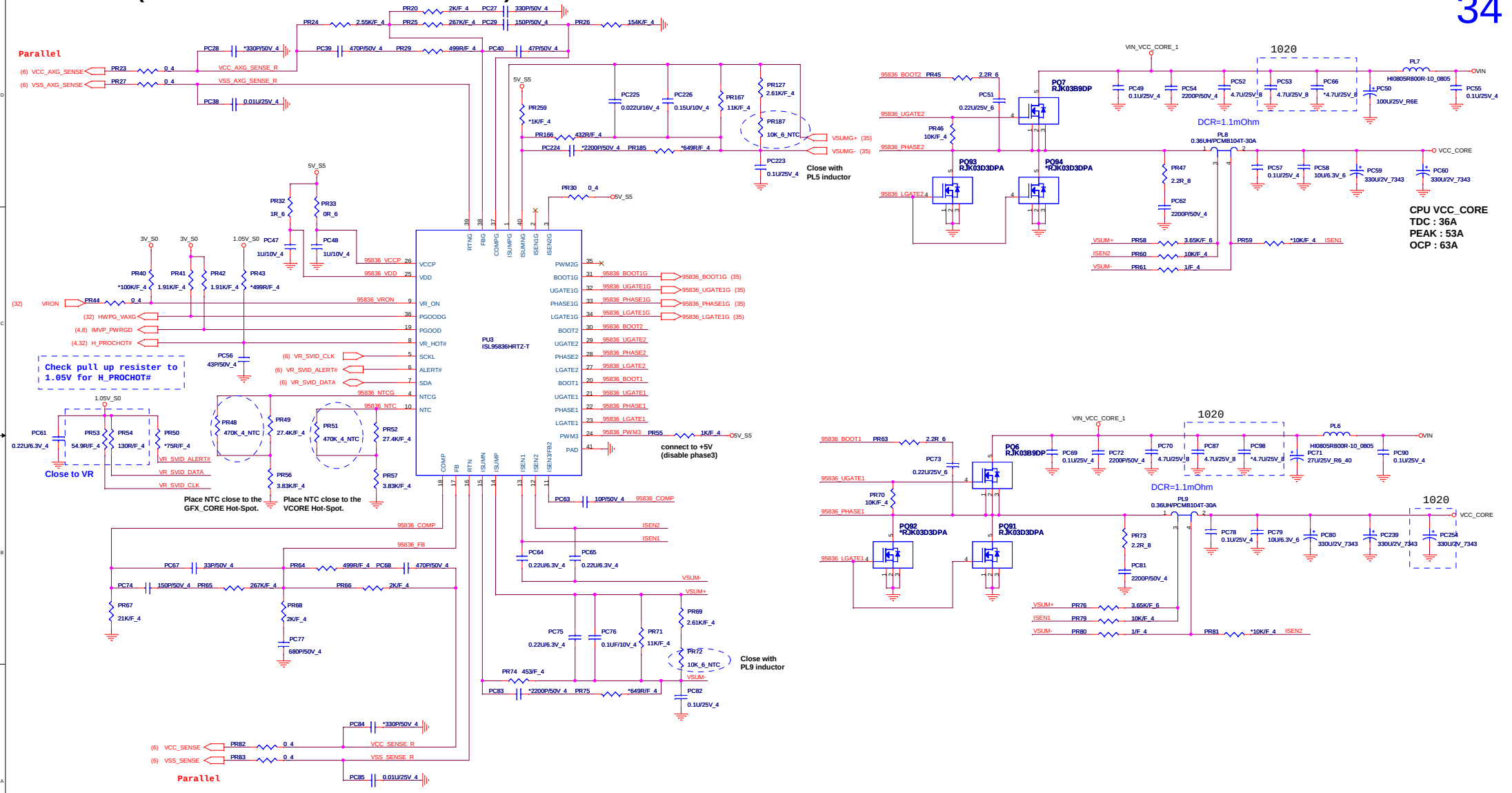
EN0	ENC	REF	VREG3	VREG5	SMPS1	SMPS2
LOW	LOW	OFF	OFF	OFF	OFF	OFF
> 2.4V	LOW	ON	ON	ON	OFF	OFF
> 2.4V	> 2.4V	ON	ON	ON	ON	ON

Quanta Computer Inc.
PROJECT : FJ8

Size	Document Number	Rev
	System 3V_S5 and 5V_S5 (RT8223PZQW)	2A

Date: Monday, January 02, 2012 Sheet 33 of 44

CPU VCORE (ISL95836HRTZ-T and ISL6208CRZ-T)



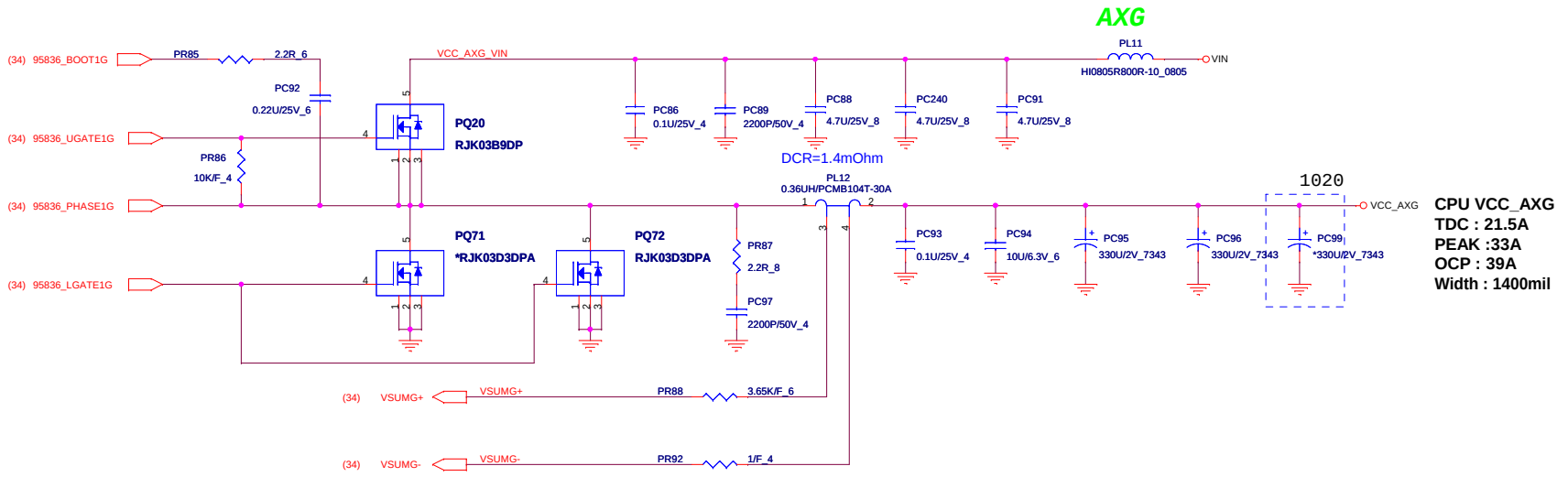
Inductor information

Value	Vendor	QCI P/N	Irms(A)	Isat(A)	Rdc (ohm)	Size	Vendor P/N
0.36uH 20%	CYN	CV+36V0MZ13	30	50	1.4m Max.	10x10x4	PCMB104T-R36MT
0.36uH 20%	Panasonic	CV+18V0MZ04	30	34	1.4m Max.	10x10x4	ETQP4LR36WFC

Quanta Computer Inc.
PROJECT : FJ8

Size	Document Number	Rev
	CPU_CORE (ISL95836HRTZ-T and ISL6208CRZ-T)	2A
Date: Monday, January 02, 2012	Sheet 34 of 44	

VCC_AXG (ISL95836HRTZ-T)



CPU VCC_AXG
TDC : 21.5A
PEAK :33A
OCP : 39A
Width : 1400mil

L/S Mosfet parameter

Mosfet	Package	ID (Ta=25C)	Rds_on_max	Schottky
RJK03D3DPA	P_PAK	20A/40A	4.7m	YES
AOL1718	P_PAK	20A/90A	4.3m	YES
RMW200N03FUB	P_PAK	20A/80A	4.6m	NO
FDMS0310S	P_PAK	14A/83A	5.2m	YES

Inductor information

Value	Vendor	QCI P/N	Irms(A)	Isat(A)	Rdc (ohm)	Size	Vendor P/N
0.36uH 20%	Panasonic	CV+36Q0MZ00	20	25	1.4m Max.	7X7X4	ETQP4LR36AFM

Quanta Computer Inc.
PROJECT : FJ8

Size	Document Number	Rev
	CPU_GFX (ISL95836HRTZ-T)	2A

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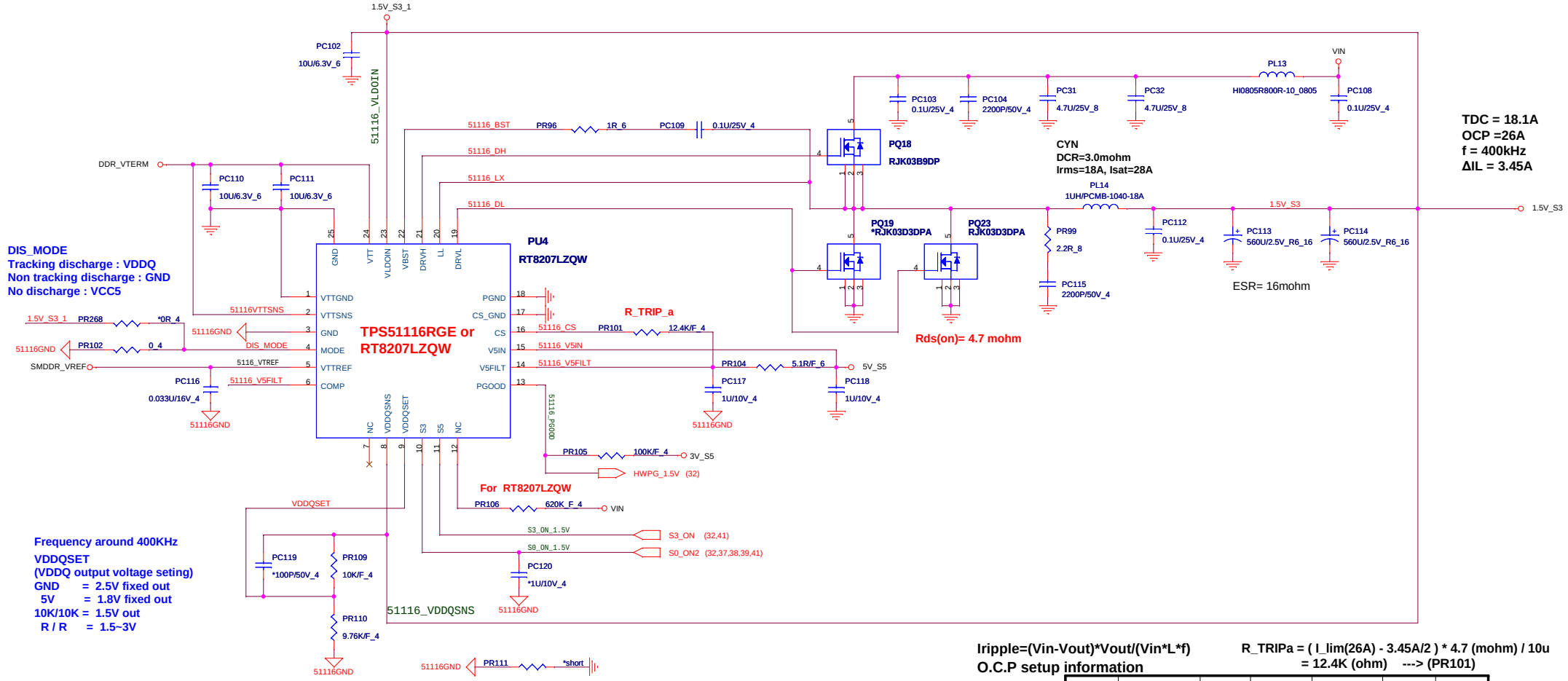
DDR3 1.5V_S3 (TPS51116RGE or RT8207LZQW)



Iripple=(Vin-Vout)*Vout/(Vin*L*f)

R_TRIPa = (I_lim(26A) - 3.45A/2) * 4.7 (mohm) / 10u
= 12.4K (ohm) ---> (PR101)

O.C.P setup information

Output	Mos Rds_on	I_OCP	OC_ΔIL(A)	Freq(KHz)	Inductor	R_TRIP
1.5V	4.7m_Max	26	3.45	400	1uH	12.4K

Inductor information

Value	Vendor	QCI P/N	Irms(A)	Isat(A)	Rdc (ohm)	Size
1uH 20%	CYN	CV-10I0MZ04	18	28	3.3m Max.	11X10X4
1uH 20%	MAG Layer	CV-10L0MZ28	21	30	3.1m Max.	11X10X4

L/S Mosfet parameter

Mosfet	Package	ID (Ta=25C)	Rds_on_max	Schottky
RJK03D3DPA	P_PAK	20A/40A	4.7m	YES
AOL1718	P_PAK	20A/90A	4.3m	YES
RMW200N03FUB	P_PAK	20A/80A	4.6m	NO
FDMS0310S	P_PAK	14A/83A	5.2m	YES

Quanta Computer Inc.
PROJECT : FJ8

Size	Document Number	Rev
	DDR3 1.5V_S3 (RT8207LZQW)	2A

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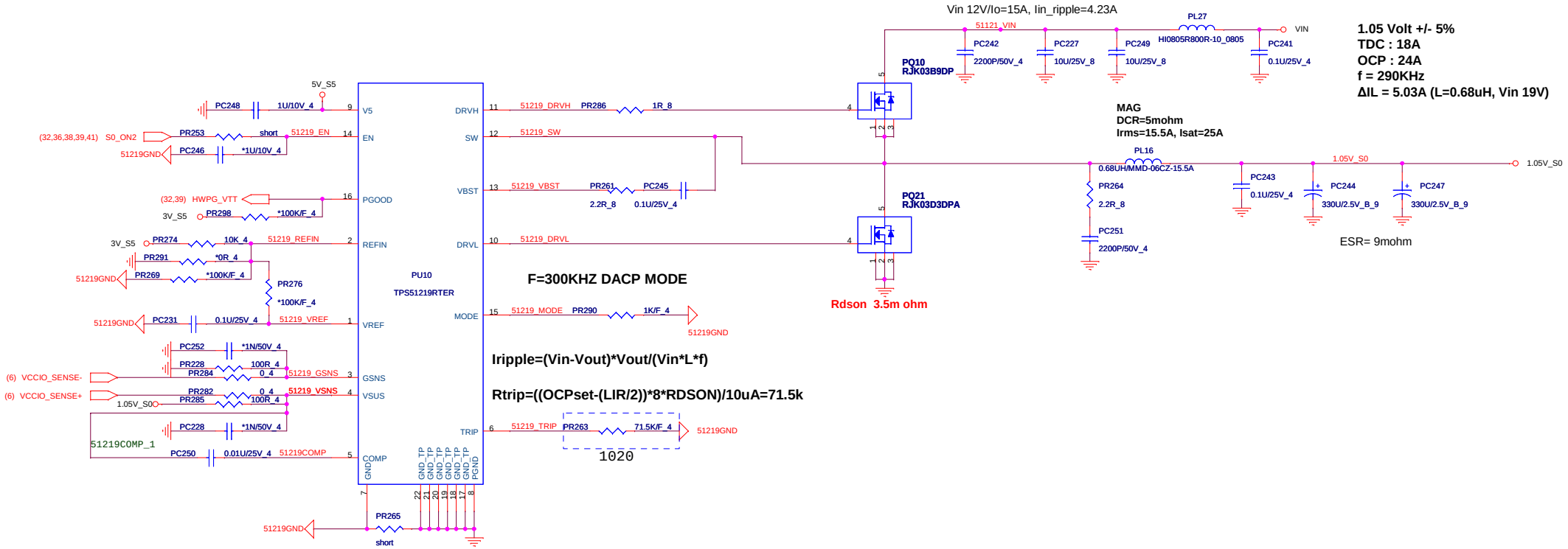
VCCIO and 1.05V_PCH (TPS51219RTER)



VCCIO_SENSE- connect to the GND sense point of the load
VCCIO_SENSE+ connect to the load voltage sense point.

Output Voltage Selection

RFIN=3.3V	output voltage=1.05V
RFIN=GND	output voltage=1.00V
Resister Divider	Adjutable from VREF

Inductor information

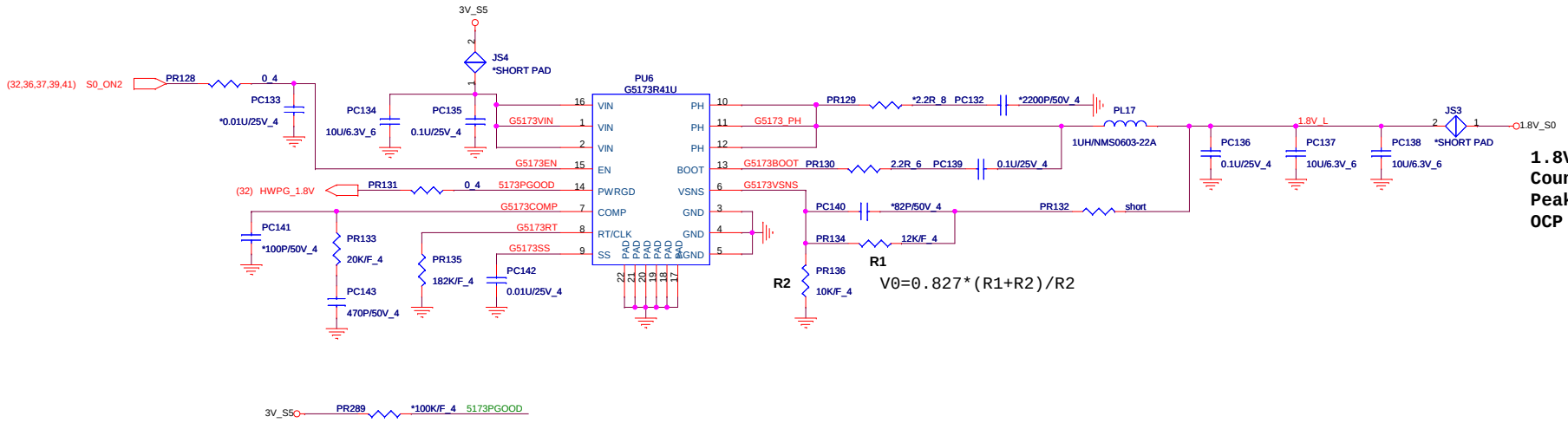
Value	Vendor	QCI P/N	Irms(A)	Isat(A)	Rdc (ohm)	Size
1uH 20%	CYN	CV-10I0MZ04	18	28	3.3m Max.	11X10X4
1uH 20%	MAG Layer	CV-10L0MZ28	21	30	3.1m Max.	11X10X4

O.C.P setup information

Output	Mos Rds_on	I_OCP	OC_ΔIL(A)	Freq(KHz)	Inductor	R_TRIP
1.05V	4.3m_Max	24	3.306	300	1uH	56.2K

Quanta Computer Inc.
PROJECT : FJ8
Size | Document Number: VCCIO and 1.05V_PCH (TPS51219RTER) | Rev 2A
Date: Monday, January 02, 2012 | Sheet 37 of 35

1.8V_S0(G5173R41U)



1.8V_S0 +/- 5%
Countinue current:1.4A
Peak current:3A
OCP minimum 4.5A

Quanta Computer Inc.		
PROJECT : FJ8		
Size	Document Number	Rev
	1.8V_S0(G5173R41U)	2A
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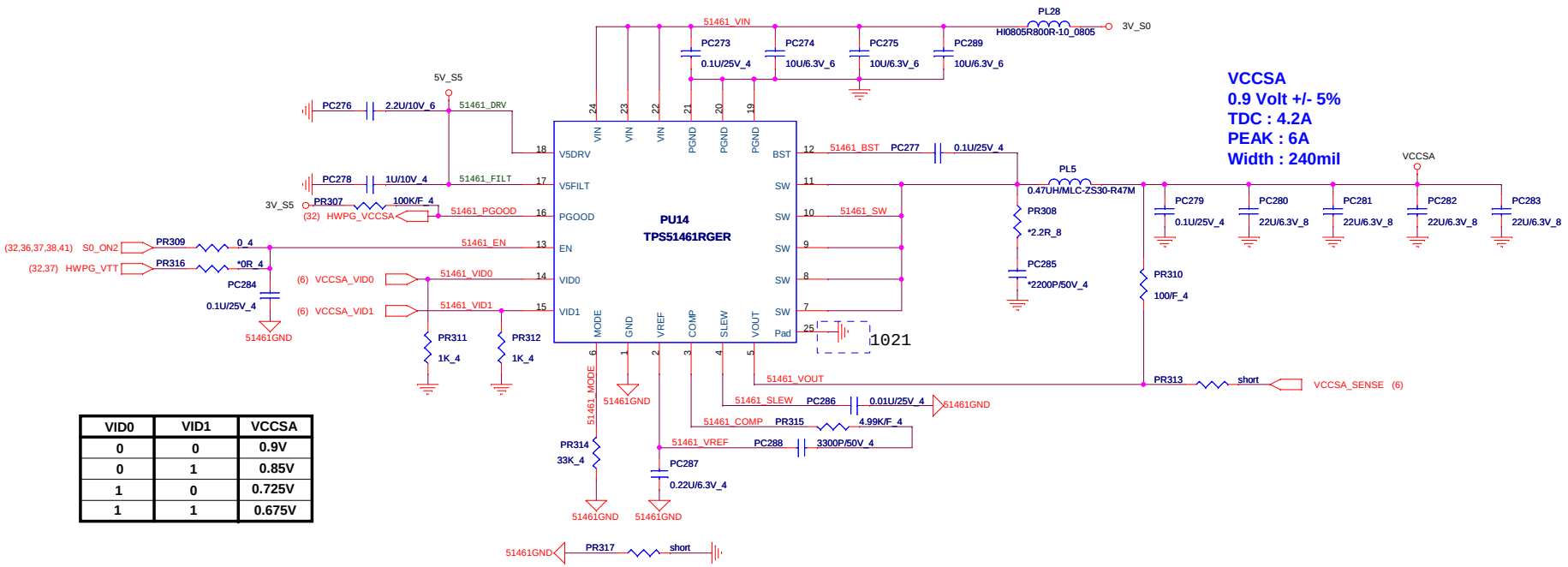
VCCSA (TPS51461RGER)



VID0	VID1	VCCSA
0	0	0.9V
0	1	0.85V
1	0	0.725V
1	1	0.675V

Quanta Computer Inc.

PROJECT : FJ8

Size	Document Number	Rev
	VCCSA (TPS51461RGER)	2A

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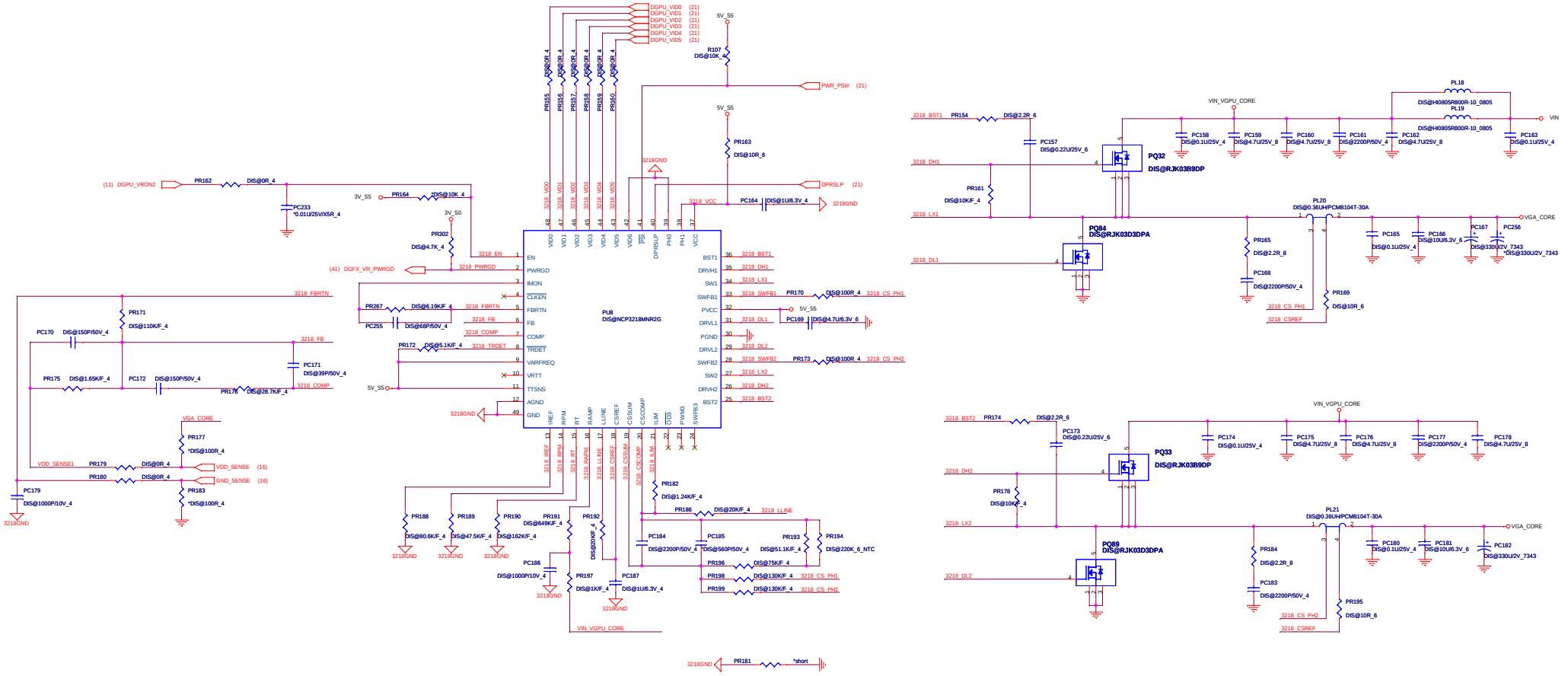
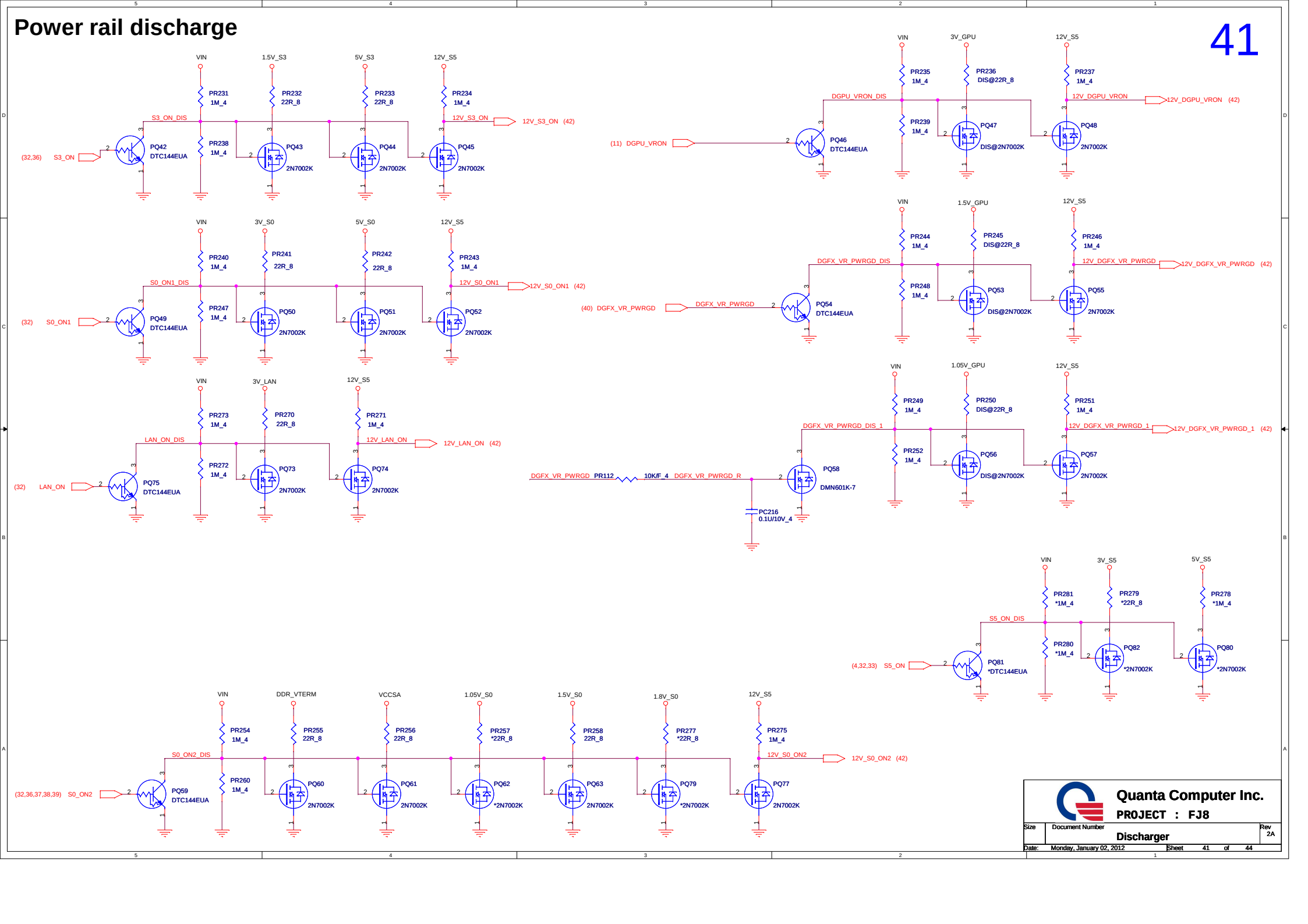


Quanta Computer Inc.			
PROJECT : FJ8			
Size	Document Number		Rev
	VGA_CORE (NCP3218MNR2G)		2A
Date: Monday, January 02, 2012		Sheet 40 of 44	

Power rail discharge



Quanta Computer Inc.		
PROJECT : FJ8		
Size	Document Number: Discharger	Rev 2A
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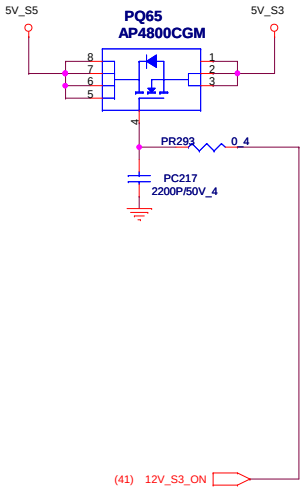
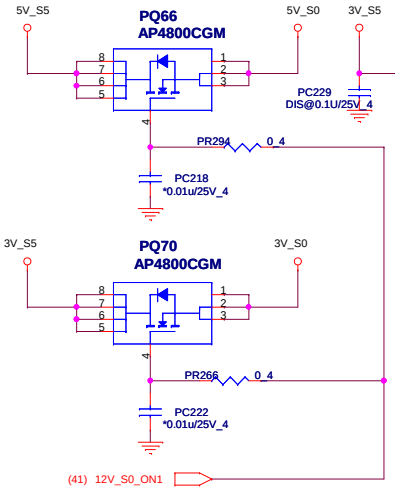
Load Switch

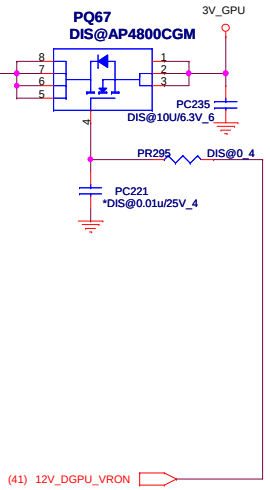
S3 ON Load SW



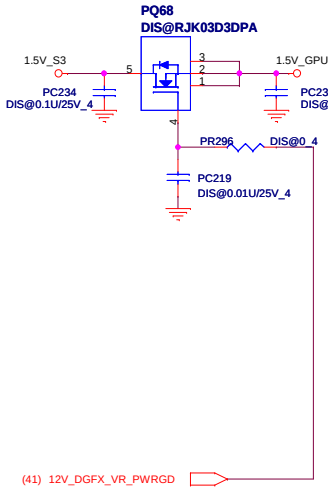
S0 ON1 Load SW



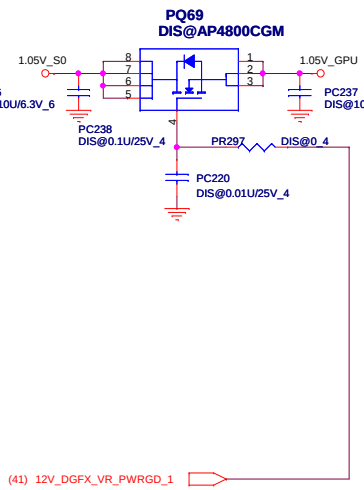
DGPU VRON Load SW



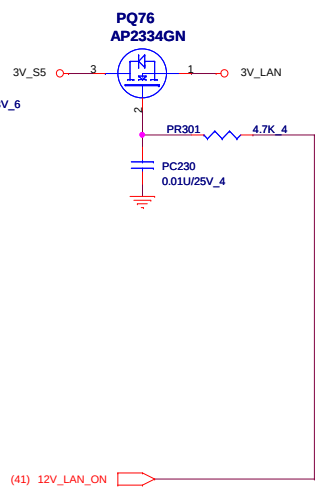
DGFX_VR_PWRGD Load SW



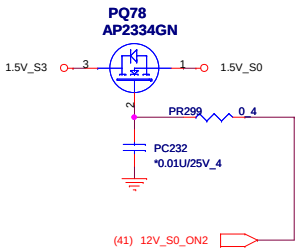
DGFX_VR_PWRGD_1 Load SW



LAN_ON Load SW



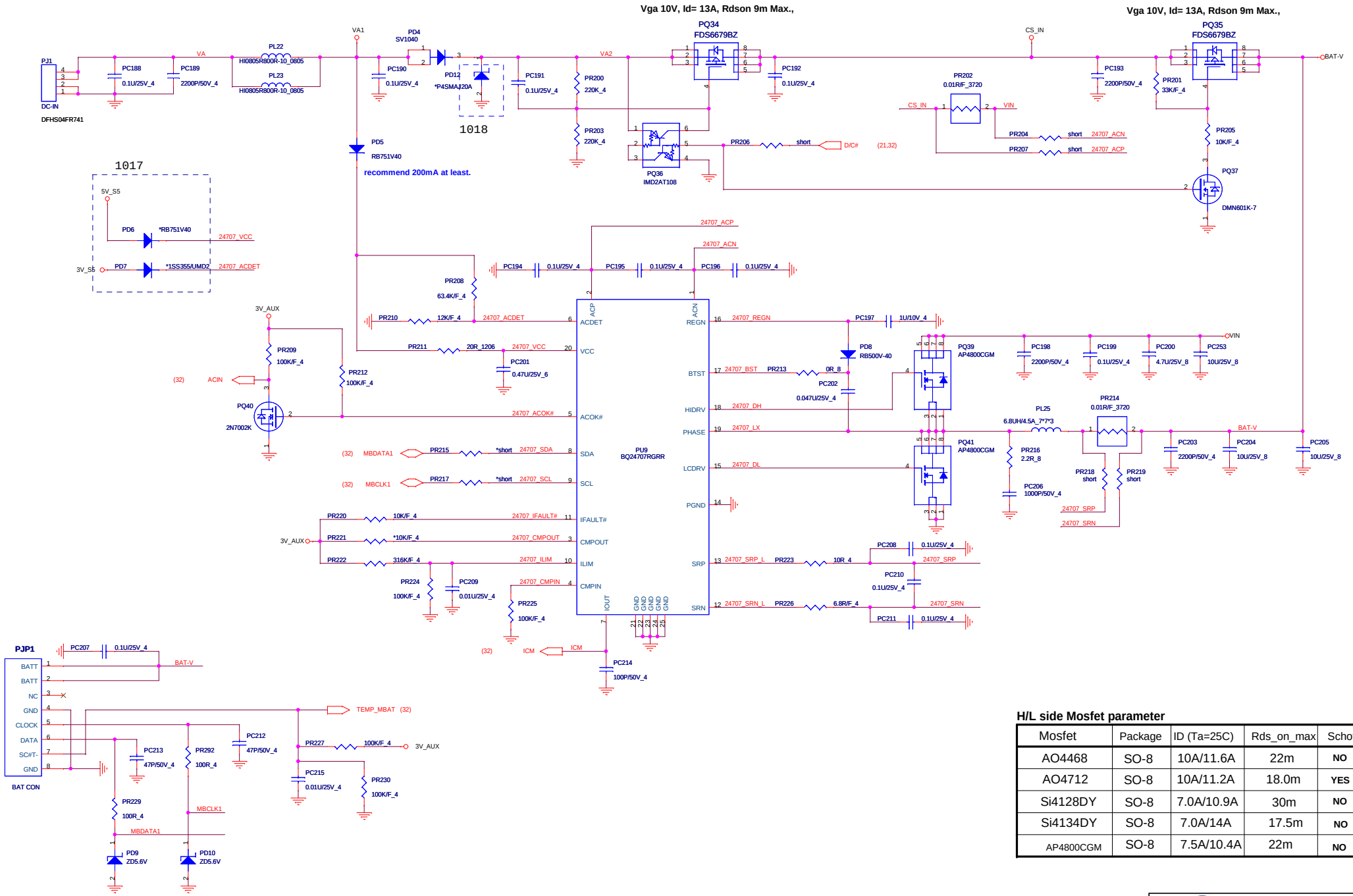
S0 ON2 Load SW



Mosfet parameter

Mosfet	Package	ID(Ta=25C)	Rds_on_max	Vgs_max
AO4468	SO-8	8.4A/10.4A	22m	+/- 20V
AP4800CGM	SO-8	7.5A/10.4A	22m	+/- 20V
Si4128DY	SO-8	7.0A/10.9A	30m	+/- 20V
Si4134DY	SO-8	7.0A/14A	17.5m	+/- 20V
ME3424D	TSOP-6	5.0A/6.7A	42m	+/- 20V
AP2334GN	SOT-23	4.5A/5.0A	42m	+/- 20V
AO3404	SOT-23	5.0A/5.8A	43m	+/- 20V

Adapter/Battery input & Charger



H/L side Mosfet parameter

Mosfet	Package	ID (Ta=25C)	Rds_on_max	Schottky
AO4468	SO-8	10A/11.6A	22m	NO
AO4712	SO-8	10A/11.2A	18.0m	YES
Si4128DY	SO-8	7.0A/10.9A	30m	NO
Si4134DY	SO-8	7.0A/14A	17.5m	NO
AP4800CGM	SO-8	7.5A/10.4A	22m	NO

Quanta Computer Inc.
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Size | Document Number | Rev
Charger (BQ24707RGRR) | 2A
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PCB REV:B

Page 27 : Change CN16,CN18 footprint for smt issue.
Page 27 : Del L20 Add LP19 for EMI issue.
Page 26 : Swap USBP0- & USBP0+ to solve USB can't detect.
Page 21: Add Q41 for correct AC_IN_GPU signal of GPU
Page 32: SWI Add D39 & pull high 10k(R427) to 3V_S5, VRON change to pin107 of EC
Page 27: Add mSATA function of block digarm
Page 17: Modify VL4,VC63,VC64,VC65 from LP@* to DIS@* for provide 1.05V_GPU PLL of VRAM
Page 21: Modify Q36 for discrete mode use and VR53 change to 10K/F_4 from 31K for discrete mode
Page 09,11 : Modify ODD SATA signal from SATA1 to SATA2 of PCH, exchange SATA1GP to SATA2GP
Page 09 : Add U35 4MB ROM for BIOS selection, modify U7 from 8MB ROM to 2MB for ME
Page 09,10,27 : Add SATA signal and repeater for mSATA function, delete 3G_PCIE signal of UMTS
Page 29 : Change Audio codec from Realtek ALC269Q-VC2 to ALC269Q-VC3-GR
Page 40 : Change PR162 from 154kohm to 0ohm for solve leakage current
Page 16 : To match the VY1 frequency stability of oscillation circuit , adjust VC60,VC61 to 27pF from 20pF
Page 16 : For PEX_PLL_HVDD is NC at N13P-GLP GF108, use 0ohm and un-stuff for N13P-GLP to avoid power inrush or leakage to chip internally.
Page 41 : Delete PR300/PD11 and PQ58 change to DMN601K-7 for fix +1.05V_GPU power on sequence.
Page 18 : For GPU debug use, stuff VR31/VR32/VC98 for B stage.
Page 11,32,40: Add U36 & U38 for control GPU power on sequence.
Page 26 : Modify USB S5 charge funtion control signal from EC.
Page 29 : Modify AR13 & AR14 of audio fuction.

PCB REV:D

Page 24 : Modify GPIO36_OD_PLG# and GPIO19 strap pin signal design for correct ODD function.
Page 24 : Add D38 for solve HDMI_DDC may enter abnormal when Plug&Play of HDMI.
Page 25 : Change connection around D24 for solve when "5V_CRT2" to GND short, D24 will break at first
Page 25 : Stuff Q21, R332 and un-stuff Q20, R328,R333, R334 for solve DMIC_DAT & CLK signal quality.
Page 27 : ADD R508,R509,R510,Q39,D37 For Win8 wake up function.
Page 09 : For use dual SPI ROM. Change dumping resistor from 0ohm to 33ohm.
Page 27 : Correct for wrong pin connection of mSATA RX pair.
Page 31 : Change con3 footprint.

PCB REV:E

Page 25 : Change cn37 footprint to lvds-fi-gr40sb-vf25-dt-40p-l.
Page 10 : Modify SMBUS LEVEL SHIFT circuit for solve leakage current.