MS-7363L2 *Version 0A*

CPU:

- Intel Conroe
- Intel Wolfdale

System Chipset:

- Intel Bearlake G33 - GMCH (North Bridge)
- Intel ICH9DH(South Bridge)

On Board Chipset:

- BIOS -- SPI 8Mb
- Realtek CODEC(ALC 662/888)
- IEEE-1394 VIA VT6308
- Super I/O --ITE ITE8718F
- LAN-INTEL 82562V & 82566DC
- Clock Generator - ICS9LPRS906

Main Memory:

- Dual Channel DDR II * 4

Expansion Slots:

- PCI Express X16 SLOT * 1
- PCI Express X1 SLOT * 2
- PCI 2.3 SLOT * 1

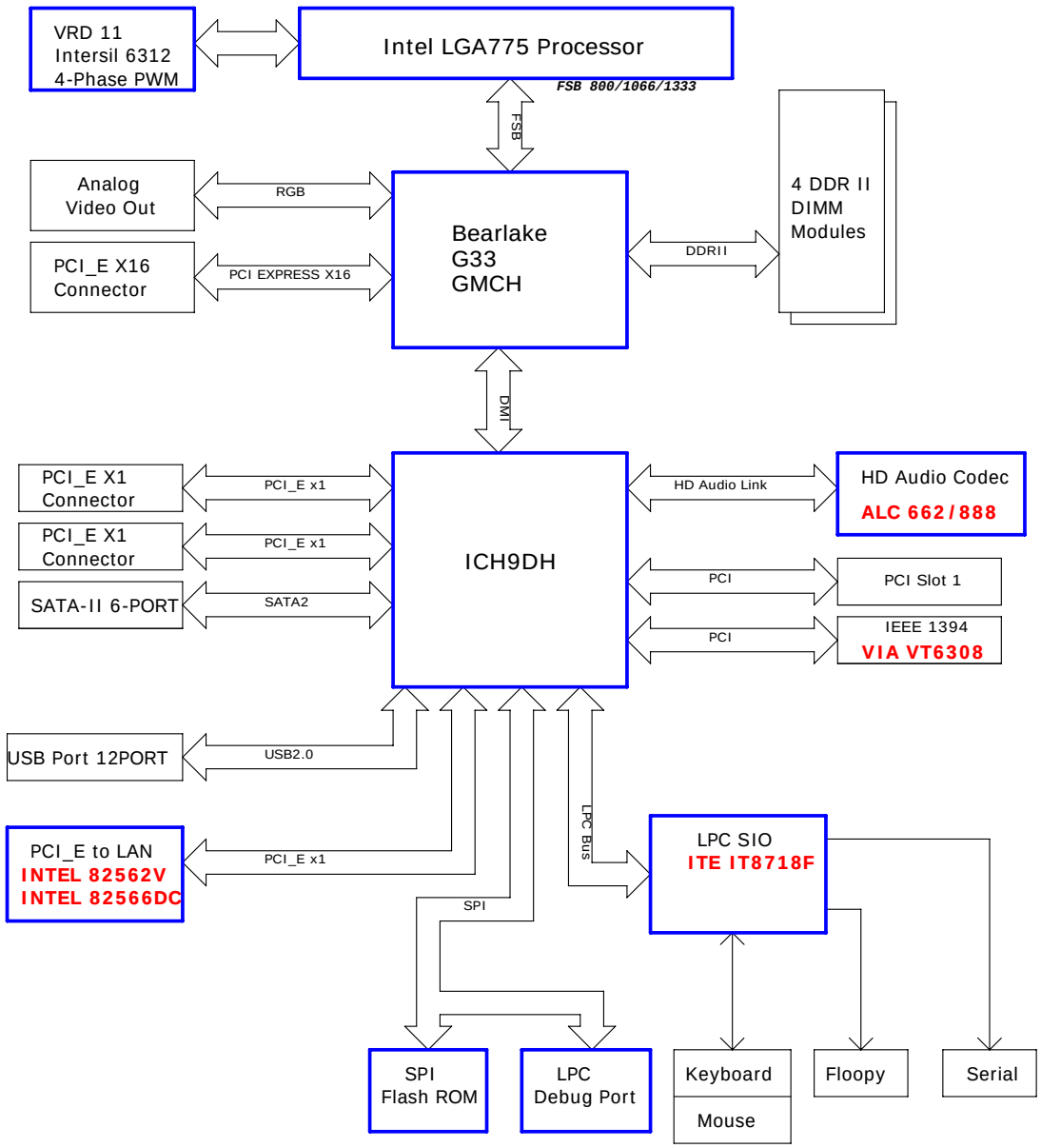
Intersil PWM:

- Intersil 6312 4 Phase

MSI Link to the Future MICRO-START INT'L CO.,LTD.

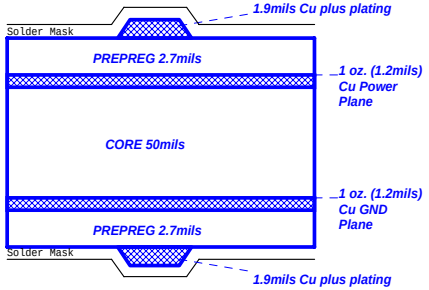
Title: COVER SHEET		
Size: Custom	Document Number: MS-7363L2	Rev: 0A
Date: Sunday, January 21, 2007	Sheet 1 of 36	

Block Diagram



Board Stack-up

(1080 Prepreg Considerations)



Single End 50ohm Top/Bottom : 4mils
USB2.0 - 90ohm : 15/7.5/4.5/7.5/15
SATA - 95ohm : 15/8/4/8/15
LAN - 100ohm : 15/10/4/10/15
PCIE - 95ohm : 15/8/4/8/15

MICRO-START INT'L CO.,LTD.

Title: BLOCK DIAGRAM		
Size: Custom	Document Number: MS-7363L2	Rev: 0A
Date: Sunday, January 21, 2007	Sheet 2 of 36	

ICH9

GPIO	Alt Func	Pin	I/O/NC	Power	PU	SMI	Tol	Default	Signal Name	
GPIO[0]	unmuxed	N7	I/O	Vcc3p3	Y	Y	3.3	GPI	straaped hi	
GPIO[1]	TACH1	AK21	I/O	Vcc3p3	Y	Y	3.3	GPI	strapped hi	
GPIO[2]	PIRQE#	K6	I/OD	V5REF	Y	Y	5	GPI	PIRQ#E	
GPIO[3]	PIRQF#	L7	I/OD	V5REF	Y	Y	5	GPI	PIRQ#F	
GPIO[4]	PIRQG#	F2	I/OD	V5REF	Y	Y	5	GPI	PIRQ#G	
GPIO[5]	PIRQH#	G2	I/OD	V5REF	Y	Y	5	GPI	PIRQ#H	
GPIO[6]	TACH2	AH22	I/O	Vcc3p3	Y	Y	3.3	GPI	strapped hi	
GPIO[7]	TACH3	AK23	I/O	Vcc3p3	Y	Y	3.3	GPI	strapped hi	
GPIO[8]	unmuxed	A20	I/O	VccSus3p3	Y	Y	3.3	GPI	strapped hi	
GPIO[9]	WOL_EN	A18	I/O	VccSus3p3	N	Y	3.3	GPI	Lenovo LEO GPIO	***
GPIO[10]	CLGPIO1	C17	I/O	VccSus3p3	Y	Y	3.3	GPI	B2_REFRESH#	
GPIO[11]	SMBALERT#	C16	I/O	VccSus3p3	N	Y	3.3	Native	SMB_ALERT#	
GPIO[12]	unmuxed	A8	I/O	VccSus3p3	N	Y	3.3	GPO	Lenovo CLR_CMOS	***
GPIO[13]	unmuxed	A19	I/O	VccSus3p3	Y	Y	3.3	GPI	SIO_PME#	***
GPIO[14]	GLGPIO2	A9	I/O	VccSus3p3	Y	Y	3.3	GPI	FP_CBL_DET#	
GPIO[15]	STO_PCI#	C15	I/O	VccSus3p3	N	Y	3.3	Native	Lenovo LEO GPIO	***
GPIO[16]	unmuxed	M2	I/O	Vcc3p3	N	N	3.3	GPO	Front Panel PLED GPIO	***
GPIO[17]	TACH0	AH21	I/O	Vcc3p3	Y	N	3.3	GPI	strapped hi	
GPIO[18]	unmuxed	K1	I/O	Vcc3p3	N	N	3.3	GPO	Front Panel PLED GPIO	***
GPIO[19]	SATA1GP	AE20	I/O	Vcc3p3	Y	N	3.3	GPI	strapped hi	
GPIO[20]	unmuxed	AF5	I/O	Vcc3p3	N	N	3.3	GPI	For Lenovo COM Port GPIO	***
GPIO[21]	SATA0GP	AK25	I/O	Vcc3p3	Y	N	3.3	GPI	strapped hi	
GPIO[22]	SCLOCK	AJ24	I/O	Vcc3p3	Y	N	3.3	GPI	strapped hi	
GPIO[23]	LDRQ1#	J3	I/O	Vcc3p3	N	N	3.3	Native	strapped hi	
GPIO[24]	MEM_LED	A14	I/O	VccSus3p3	N	N	3.3	GPO	Lenovo LEO CLOCK RUN	***
GPIO[25]	STP_CPU#	B18	I/O	VccSus3p3	N	N	3.3	GPO	Lenovo LEO GPIO	***
GPIO[26]	S4_STATE#	C11	I/O	VccSus3p3	N	N	3.3	GPO	For Lenovo SPI WP#1	***
GPIO[27]	QRT_STATE0	A11	I/O	VccSus3p3	N	N	3.3	GPO	For Lenovo SPI WP#2	***
GPIO[28]	QRT_STATE1	G18	I/O	VccSus3p3	Y	N	3.3	GPO	NC	
GPIO[29]	OC5#	N1	I/O	VccSus3p3	N	N	3.3	Native	OC#3	
GPIO[30]	OC6#	N5	I/O	VccSus3p3	Y	N	3.3	Native	OC#3	
GPIO[31]	OC7#	M1	I/O	VccSus3p3	Y	N	3.3	Native	OC#4	
GPIO[32]	unmuxed	K2	I/O	Vcc3p3	N	N	3.3	GPO	SPI_WP#(Normol)	***
GPIO[33]	unmuxed	AF6	I/O	Vcc3p3	N	N	3.3	GPO	strapped	
GPIO[34]	unmuxed	AH5	I/O	Vcc3p3	N	N	3.3	GPO	SPI HOLD GPIO	***
GPIO[35]	SATACLKREQ#	L1	I/O	Vcc3p3	N	N	3.3	GPO	NC	
GPIO[36]	SATA2GP	AE21	I/O	Vcc3p3	Y	N	3.3	GPI	strapped hi	
GPIO[37]	SATA3GP	AE22	I/O	Vcc3p3	Y	N	3.3	GPI	strapped hi	
GPIO[38]	SLOAD	AK24	I/O	Vcc3p3	Y	N	3.3	GPI	strapped hi	
GPIO[39]	SDATAOUT0	AH23	I/O	Vcc3p3	Y	N	3.3	GPI	strapped hi	
GPIO[40]	OC1#	N3	I/O	VccSuS3p3	Y	N	3.3	Native	OC#1	
GPIO[41]	OC2#	P7	I/O	VccSuS3p3	Y	N	3.3	Native	OC#1	
GPIO[42]	OC3#	R7	I/O	VccSuS3p3	Y	N	3.3	Native	OC#2	
GPIO[43]	OC4#	N2	I/O	VccSuS3p3	Y	N	3.3	Native	OC#2	
GPIO[44]	OC8#	P3	I/O	VccSuS3p3	Y	N	3.3	Native	OC#4	
GPIO[45]	OC9#	R6	I/O	VccSuS3p3	Y	N	3.3	Native	OC#4	
GPIO[46]	OC10#	T7	I/O	VccSuS3p3	Y	N	3.3	Native	strapped hi	
GPIO[47]	OC11#	P1	I/O	VccSuS3p3	Y	N	3.3	Native	strapped hi	
GPIO[48]	SDATAOUT1	AD20	I/O	Vcc3p3	Y	N	3.3	GPI	ICH_SGP48_PU	
GPIO[49]	unmuxed	AJ25	I/O	Vcc3p3	N	N	3.3	GPO	DMI_STRAP	
GPIO[50]	REQ1#	G13	I/O	V5REF	N	N	5	Native	PREQ#1	
GPIO[51]	GNT1#	A7	I/O	Vcc3p3	N	N	3.3	Native	TP7	
GPIO[52]	REQ2#	F13	I/O	V5REF	N	N	5	Native	PREQ#2	
GPIO[53]	GNT2#	C7	I/O	Vcc3p3	N	N	3.3	Native	PGNT#2	
GPIO[54]	REQ3#	G8	I/O	V5REF	N	N	5	Native	PREQ#3	
GPIO[55]	GNT3#	F7	I/O	Vcc3p3	N	N	3.3	Native	PGNT#3	
GPIO[56]	GLAN_DOCK#	F16	I/O	VccSuS3p3	Y	N	3.3	GPI	strapped hi	
GPIO[57]	CLGPIO5	C12	I/O	VccSuS3p3	Y	N	3.3	GPI	strapped hi	
GPIO[58]	SPI_CS#/ GLGPIO4	F23	I/O	VccSuS3p3	Y	N	3.3	GPI	SPI_CS1#	***
GPIO[59]	OC0#	P5	I/O	VccSuS3p3	Y	N	3.3	Native	OC#1	
GPIO[60]	LINKALERT#/ GLGPIO4	F18	I/O	VccSuS3p3	N	N	3.3	Native	LINK_ALERT#	

Following are the GPIOs that need to be terminated properly if not used:
GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3_3 if unused.
GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3_3 if unused.

FWH

Note: FWH GPs should only be used for static options, do not put dynamic nets on these

GPIO	Pin#	Power	Tol	Signal Name
FPGI[0]	6	Main	3.3	pull-up
FPGI[1]	5	Main	3.3	pull-up
FPGI[2]	4	Main	3.3	pull-up
FPGI[3]	3	Main	3.3	pull-up
FPGI[4]	30	Main	3.3	pull-down

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI SLOT 1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	PCI_CLK0
PCI 1394	PIRQ#C	PREQ#2 PGNT#2	AD18	CK_P_33M_1394

DDRII DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM_A1	A0H	MCLK_A0/MCLK_A#0 MCLK_A1/MCLK_A#1 MCLK_A2/MCLK_A#2
DIMM_A2	A2H	MCLK_A3/MCLK_A#3 MCLK_A4/MCLK_A#4 MCLK_A5/MCLK_A#5
DIMM_B1	A4H	MCLK_B0/MCLK_B#0 MCLK_B1/MCLK_B#1 MCLK_B2/MCLK_B#2
DIMM_B2	A6H	MCLK_B3/MCLK_B#3 MCLK_B4/MCLK_B#4 MCLK_B5/MCLK_B#5

JUMPER SETTING

CLR_CMOS	(1-2)NORMAL	(2-3)CLEAR

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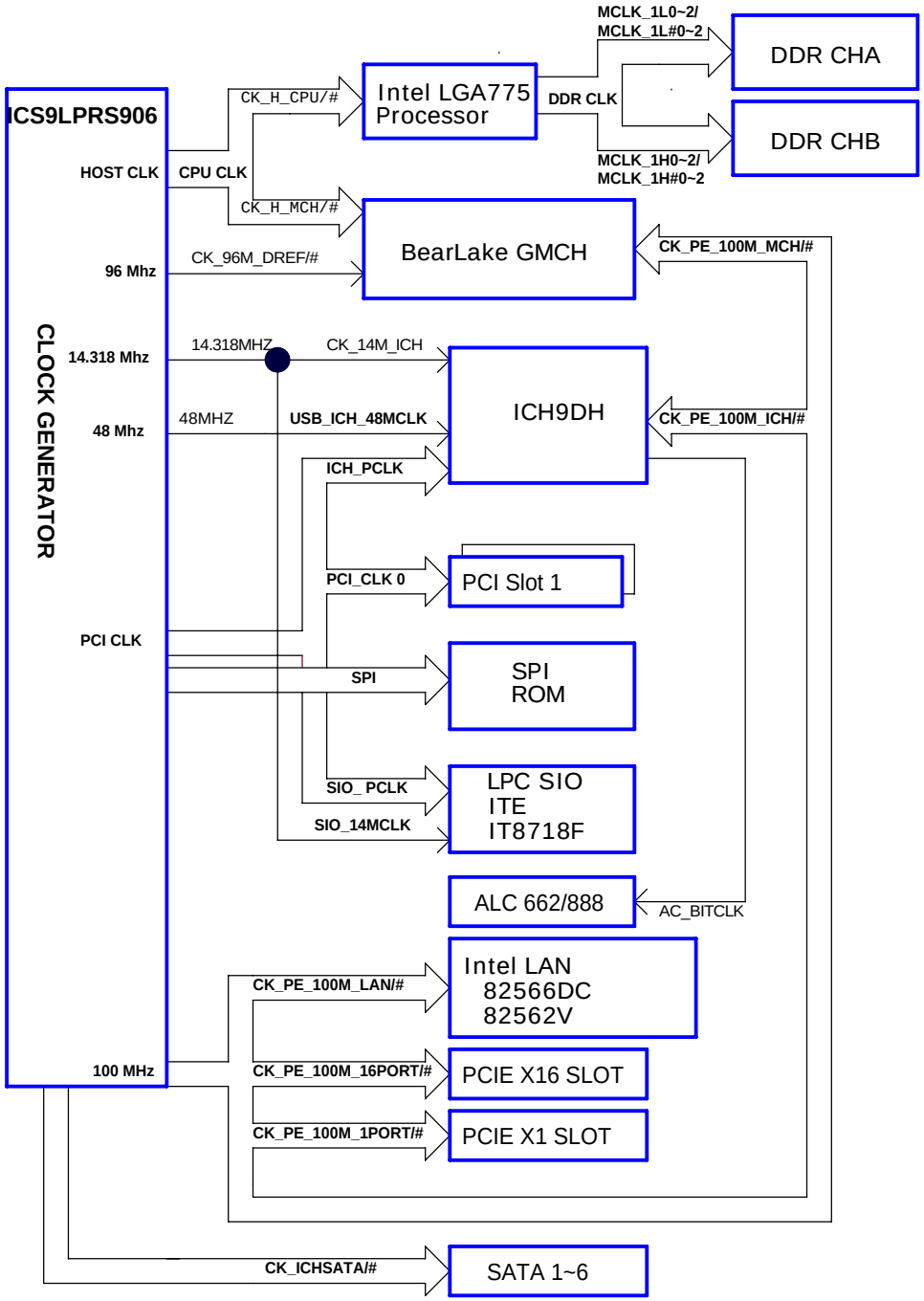
Title: GPIO MAP

Size: C | Document Number: MS-7363L2 | Rev: 0A

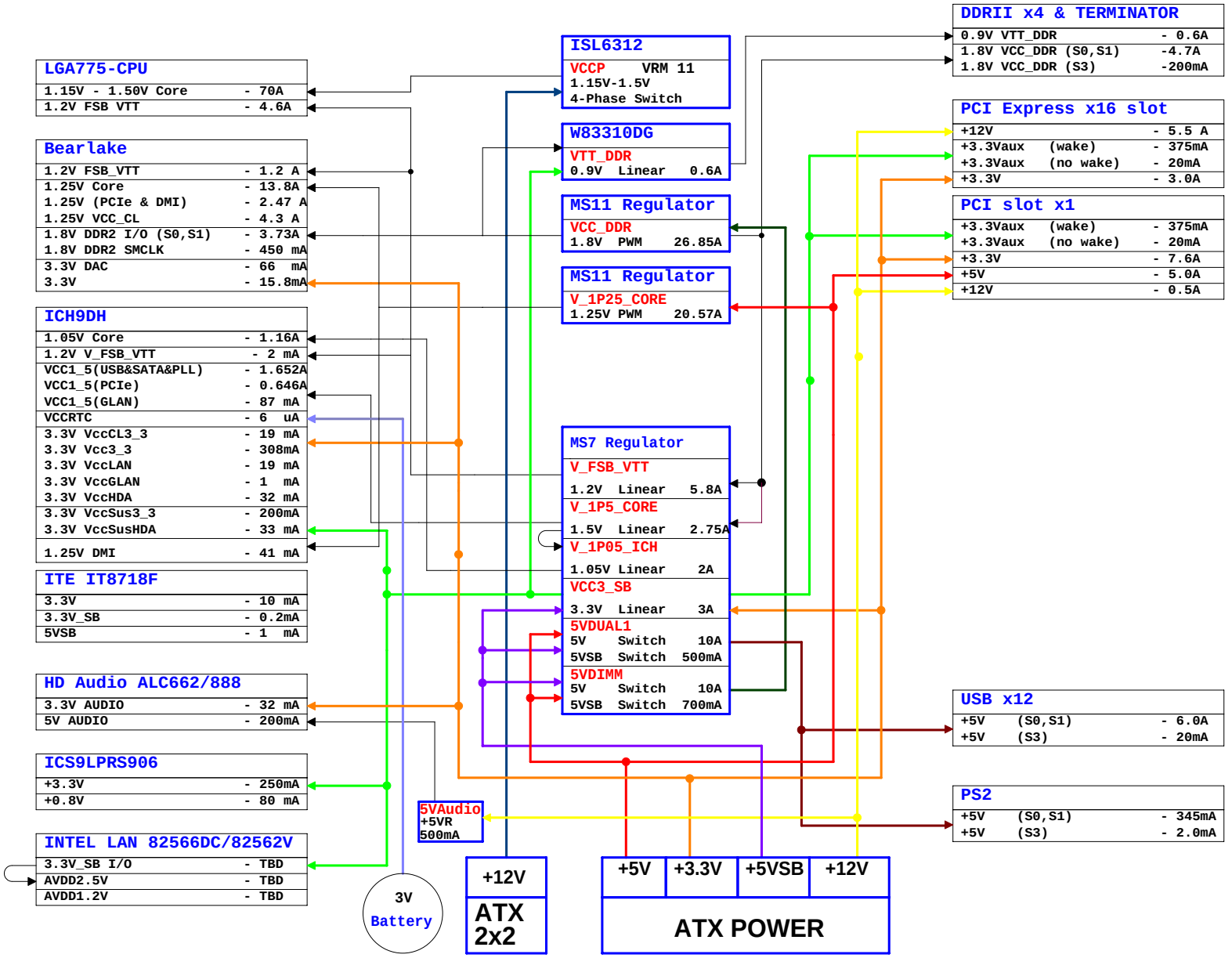
Date: Monday, January 29, 2007 | Sheet 3 of 36

INTEL LAKEPORT PLATFORM CLOCK GENERATOR MAP



MICRO-START INT'L CO.,LTD.

Title: Clock Map		
Size: Custom	Document Number: MS-7363L2	Rev: 0A
Date: Wednesday, January 17, 2007	Sheet 4 of 36	



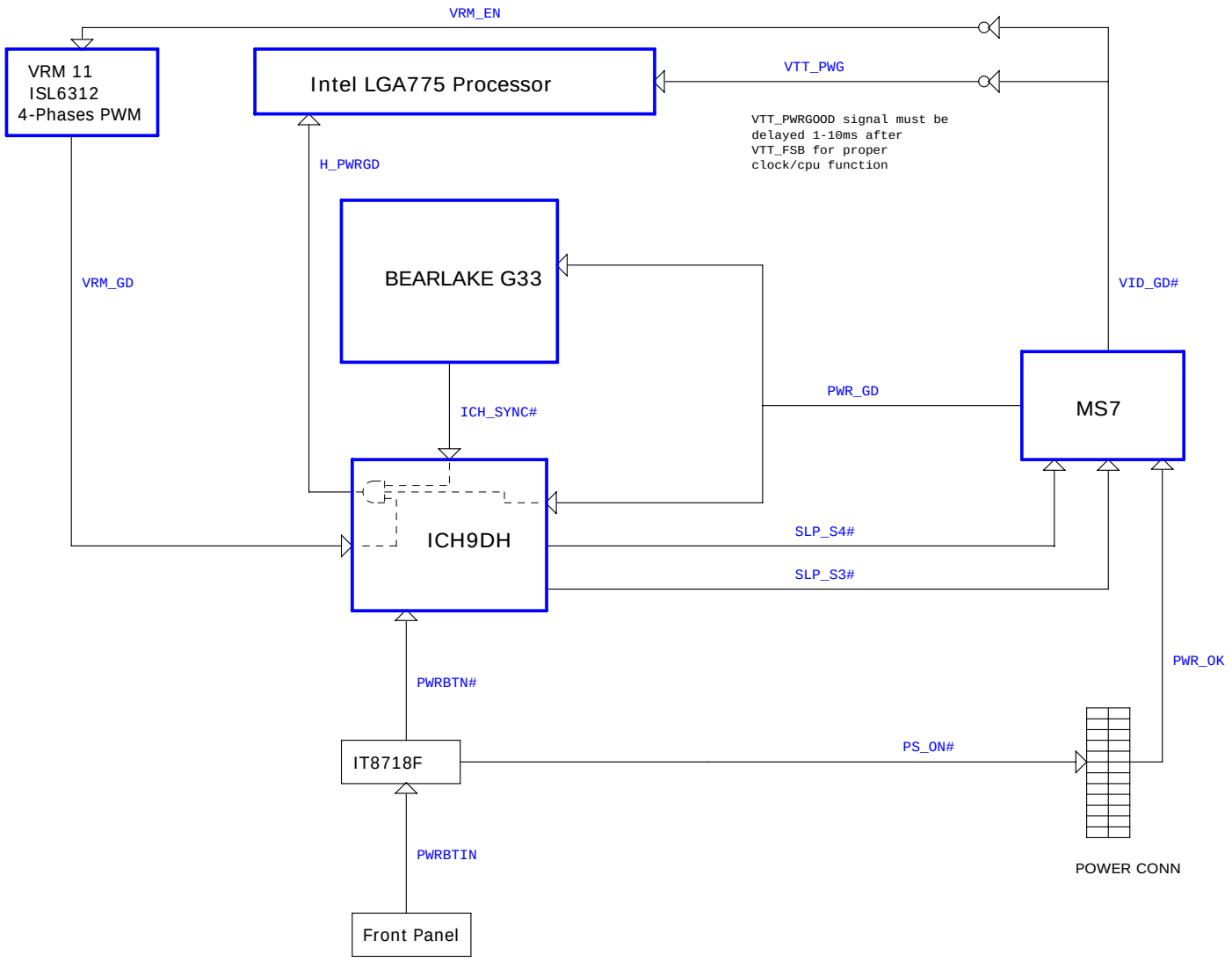
MICRO-START INT'L CO.,LTD.

Title: Power Delivery

Size: C | Document Number: MS-7363L2 | Rev: 0A

Date: Wednesday, January 17, 2007 | Sheet 5 of 36

Power OK MAP



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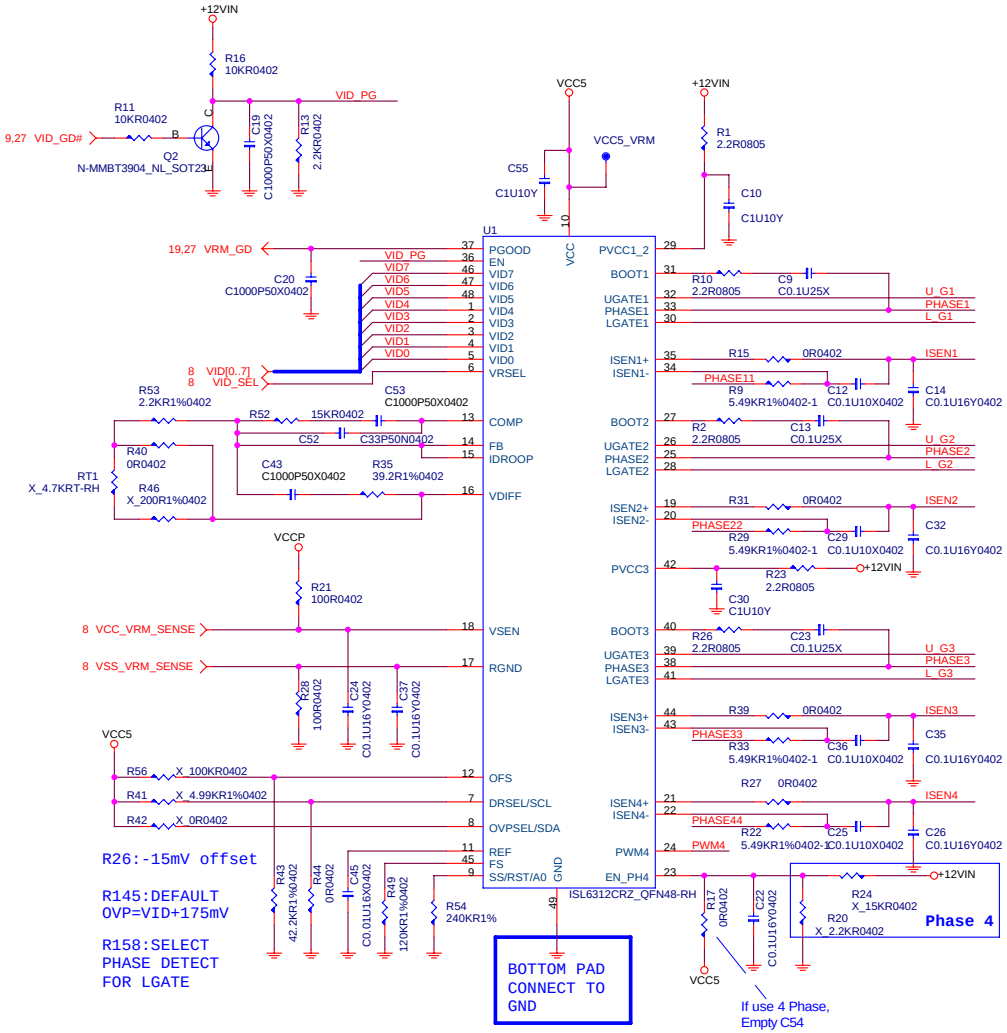
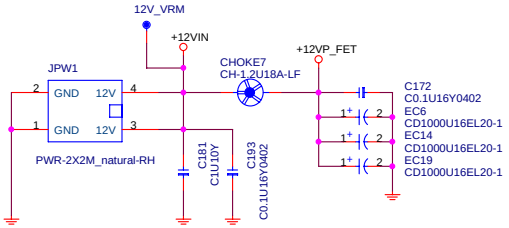
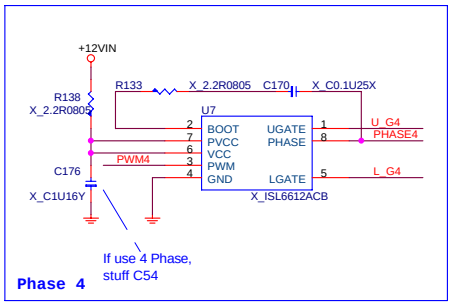
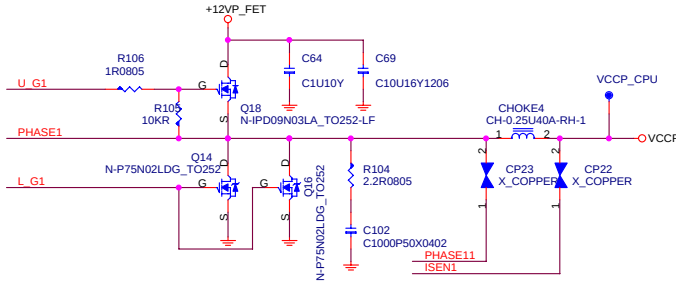
Title: Power OK MAP		
Size: Custom	Document Number: MS-7363L2	Rev: 0A
Date: Wednesday, January 17, 2007	Sheet 6 of 36	

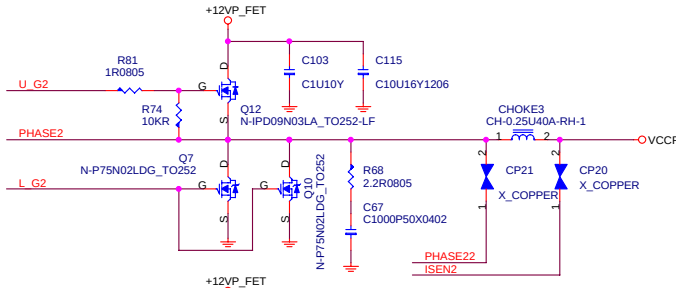
PWM Controllor ISL6312

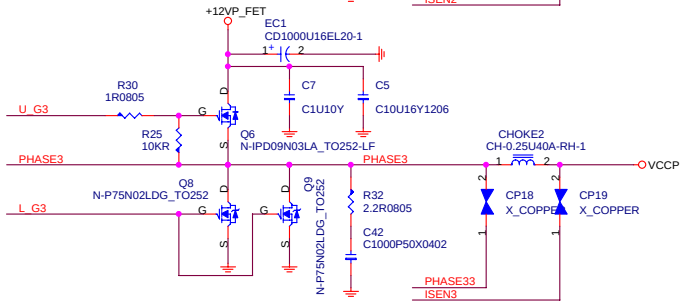


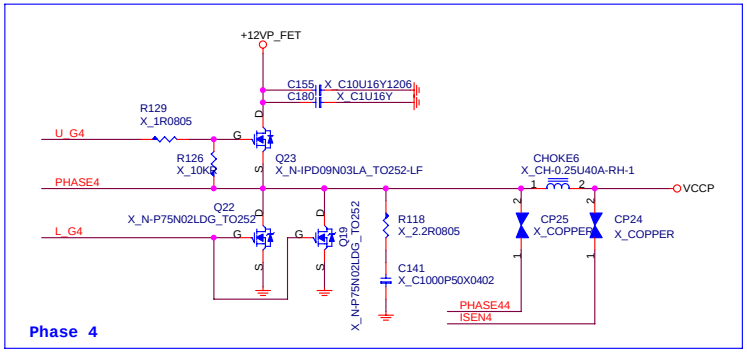




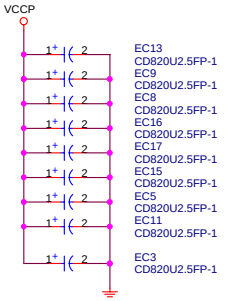






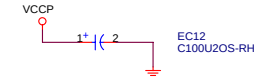


OS-CON Capactiors



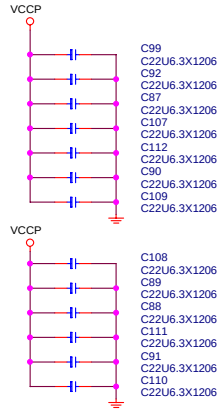
Phase 4

SP Capacitors



DECOUPLING CAPACITORS

Place these caps within socket cavity



MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: VRM11 Intersil 6312 4Phase		
Size: Custom	Document Number: MS-7363L2	Rev: 0A
Date: Tuesday, January 30, 2007	Sheet 7 of 36	

CPU SIGNAL BLOCK

BSEL			TABLE
2	1	0	FSB FREQUENCY
0	0	0	267 MHZ (1067)
0	1	0	200 MHZ (800)
0	0	1	133 MHZ (533)

Prescott / Cedar Mill
LL_ID[1:0] = 00
GTLREF_SEL = 0
VTT_SEL = 1

PLACE BPM TERMINATION NEAR CPU

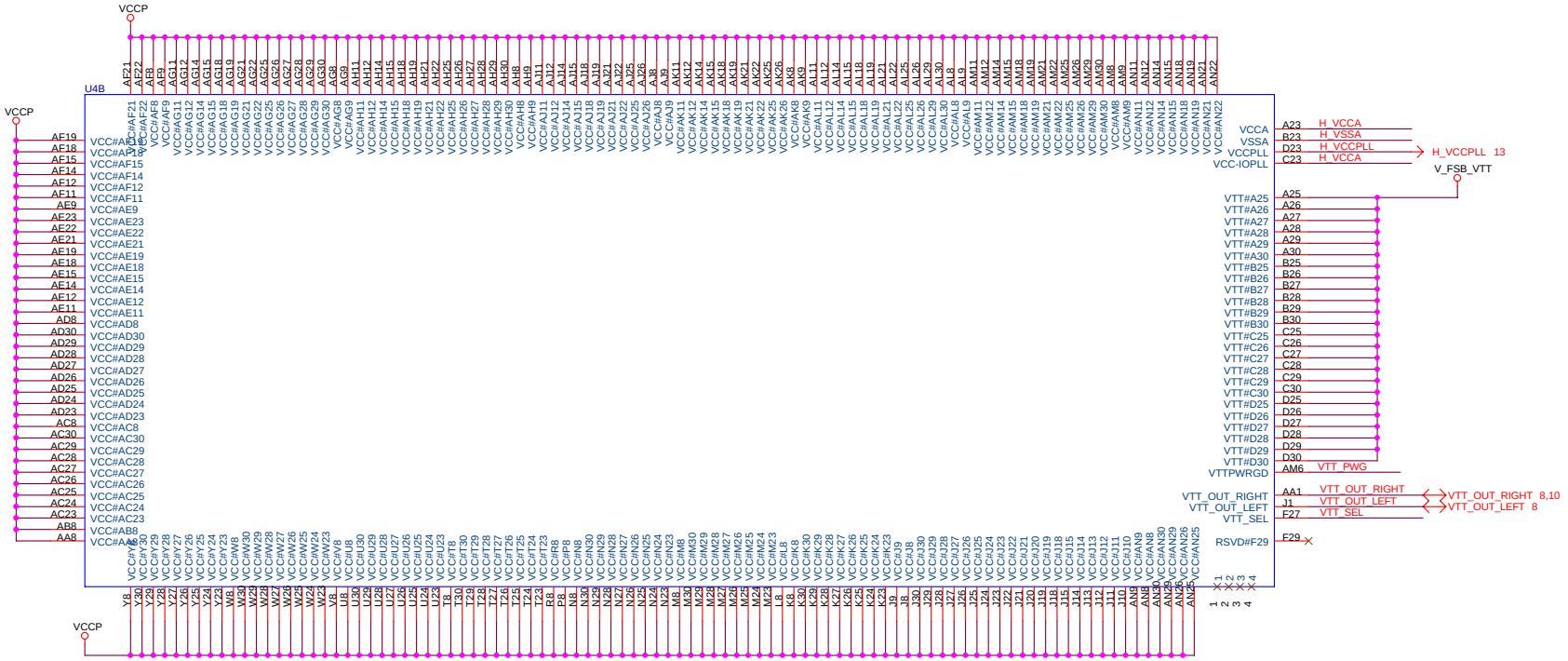
COMP4, COMP5, COMP6 and COMP7:No Pulled up is required for Conroe and later CPU.

Place close to R2087

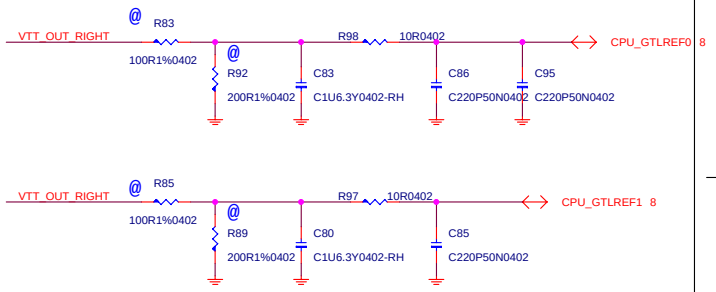
ZIF-SOCK775-15u-in

Title	Intel LGA775 - Signals
Size	Custom
Document Number	MS-7363L2
Rev	0A
Date:	Tuesday, January 30, 2007
Sheet	8 of 36

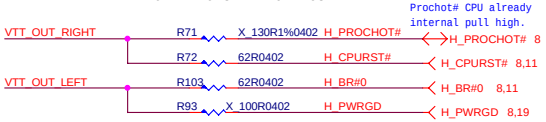
MICRO-START INT'L CO.,LTD.



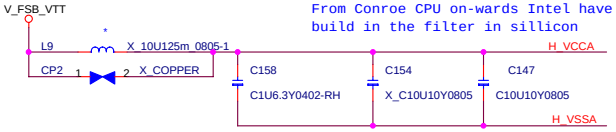
CAPS FOR FSB GENERIC

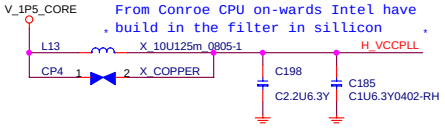


PLACE AT CPU END OF ROUTE

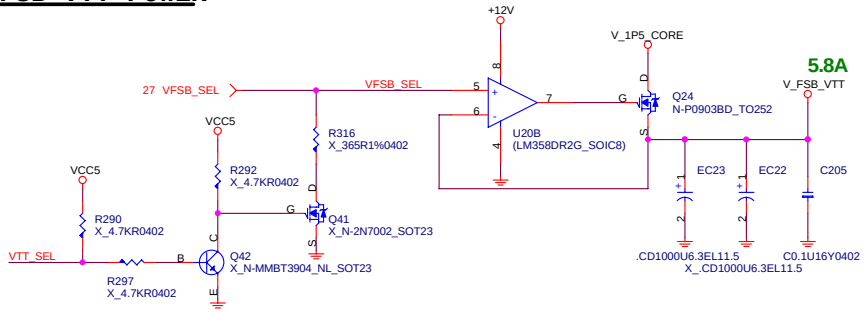


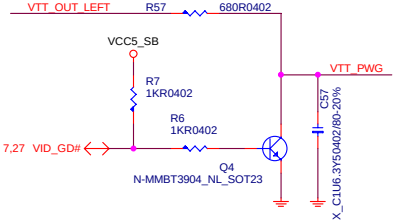
PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET
TRACE WIDTH TO CAPS MUST BE SMALLER THAN 12MILS





CPU FSB VTT POWER

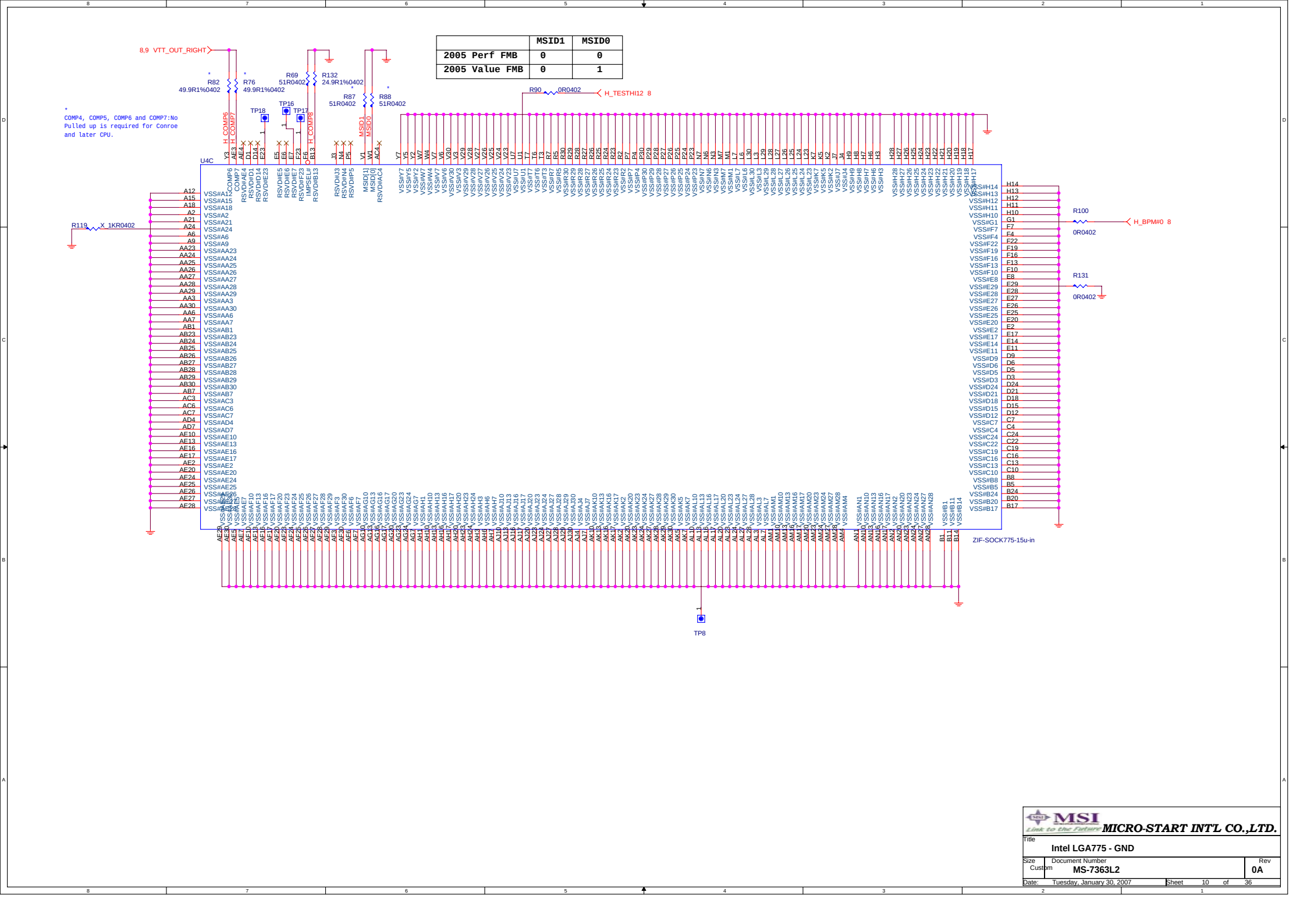




VTT_SEL = L	V_FSB_VTT=1.1V	For future KENTSFIELD processor. (FSB1333, Quad-Core)
VTT_SEL = H	V_FSB_VTT=1.2V	For normal processors.

MSI Link to the Future MICRO-START INT'L CO.,LTD.

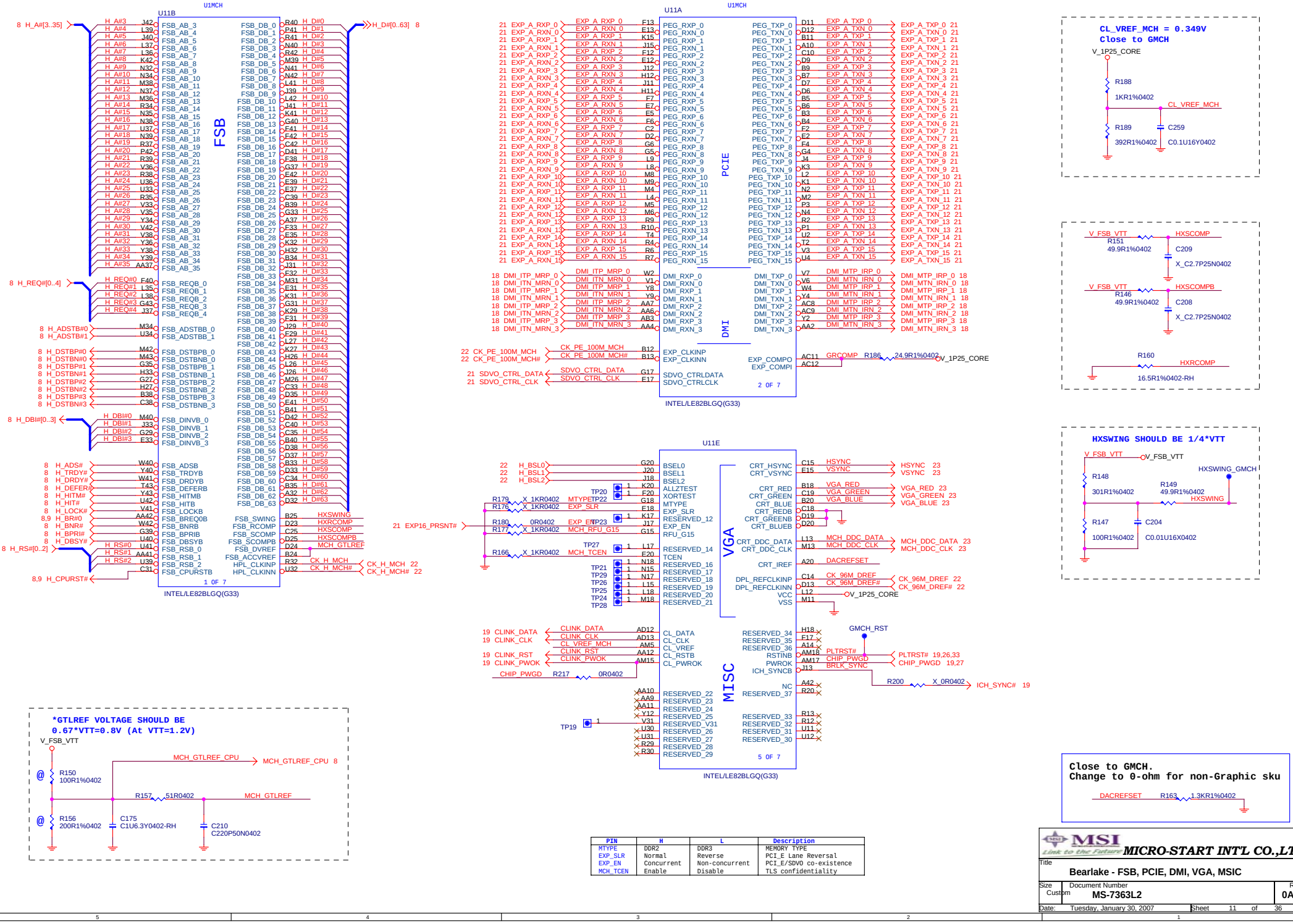
Title	Intel LGA775 - Power	
Size: Custom	Document Number: MS-7363L2	Rev: 0A
Date: Tuesday, January 30, 2007	Sheet 9 of 36	



	MSID1	MSID0
2005 Perf FMB	0	0
2005 Value FMB	0	1

MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: Intel LGA775 - GND		
Size: Custom	Document Number: MS-7363L2	Rev: 0A
Date: Tuesday, January 30, 2007	Sheet 10 of 36	


U1MCH
U11B
FSB
INTEL/LE82BLGQ(G33)
U11A
PCIE
DMI
U11E
VGA
MISC
*GTLREF VOLTAGE SHOULD BE
0.67*VTT=0.8V (At VTT=1.2V)
CL_VREF_MCH = 0.349V
Close to GMCH
HXSWING SHOULD BE 1/4*VTT
Close to GMCH.
Change to 0-ohm for non-Graphic sku
MICRO-START INT'L CO.,LTD.
Bearlake - FSB, PCIE, DMI, VGA, MSIC
MS-7363L2
Tuesday, January 30, 2007

U11C U1MCH

DDR_A

DDR3

NC

3 OF 7

INTEL/LE82BLGQ(G33)

U11D U1MCH

DDR_B

DDR_VREF

4 OF 7

INTEL/LE82BLGQ(G33)

Place close to GMCH

VCC_DDR

C237 C1U10Y

C130 C1U10Y

C219 C1U10Y

C122 C1U10Y

C200 C1U10Y

C162 C1U10Y

VTT_GMCH

VCC_DDR

R203 1KR1%0402

MCH_VREF_A AM6

R215 1KR1%0402

C285 C0.1U16Y0402

SRCOMP0 AL4

SRCOMP1 AL2

SRCOMP2 BB40

SRCOMP3 BA40

DDR_RCOMPVOL AM8

DDR_RCOMPVOH AM10

R214 1KR1%0402

DDR_RCOMPVOL

DDR_RCOMPVOL = 0.2 * VCC_DDR

R205 3.01KR1%0402

C284 C0.01U16X0402

VCC_DDR

R197 1KR1%0402

DDR_RCOMPVOH

DDR_RCOMPVOH = 0.2 * VCC_DDR

C272 C0.01U16X0402

VCC_DDR

@

R183 19.1R1%0402-RH SRCOMP0

R193 19.1R1%0402-RH SRCOMP1

R140 19.1R1%0402-RH SRCOMP2

R139 19.1R1%0402-RH SRCOMP3

C270 C0.1U16Y0402

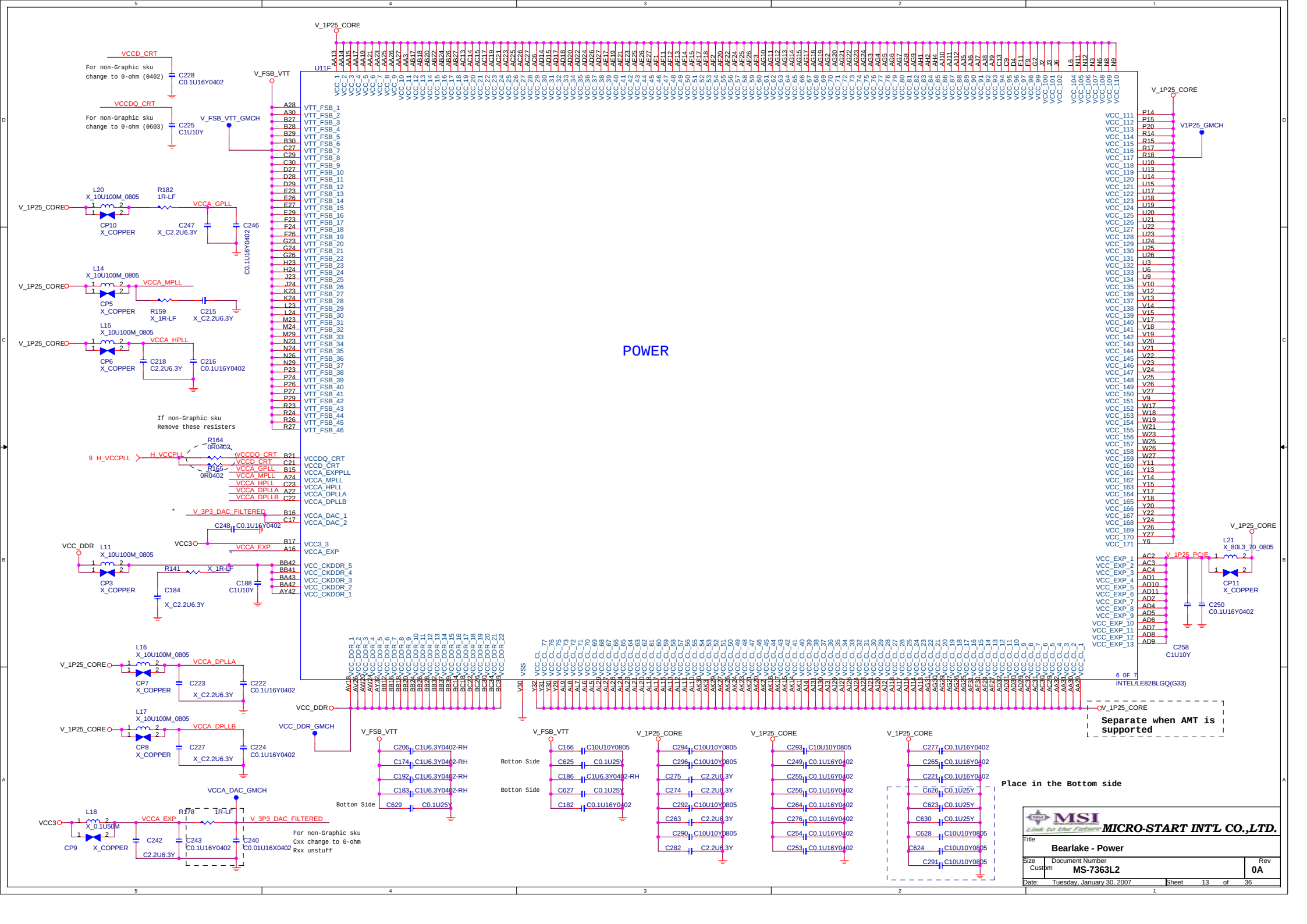
C289 C0.1U16Y0402

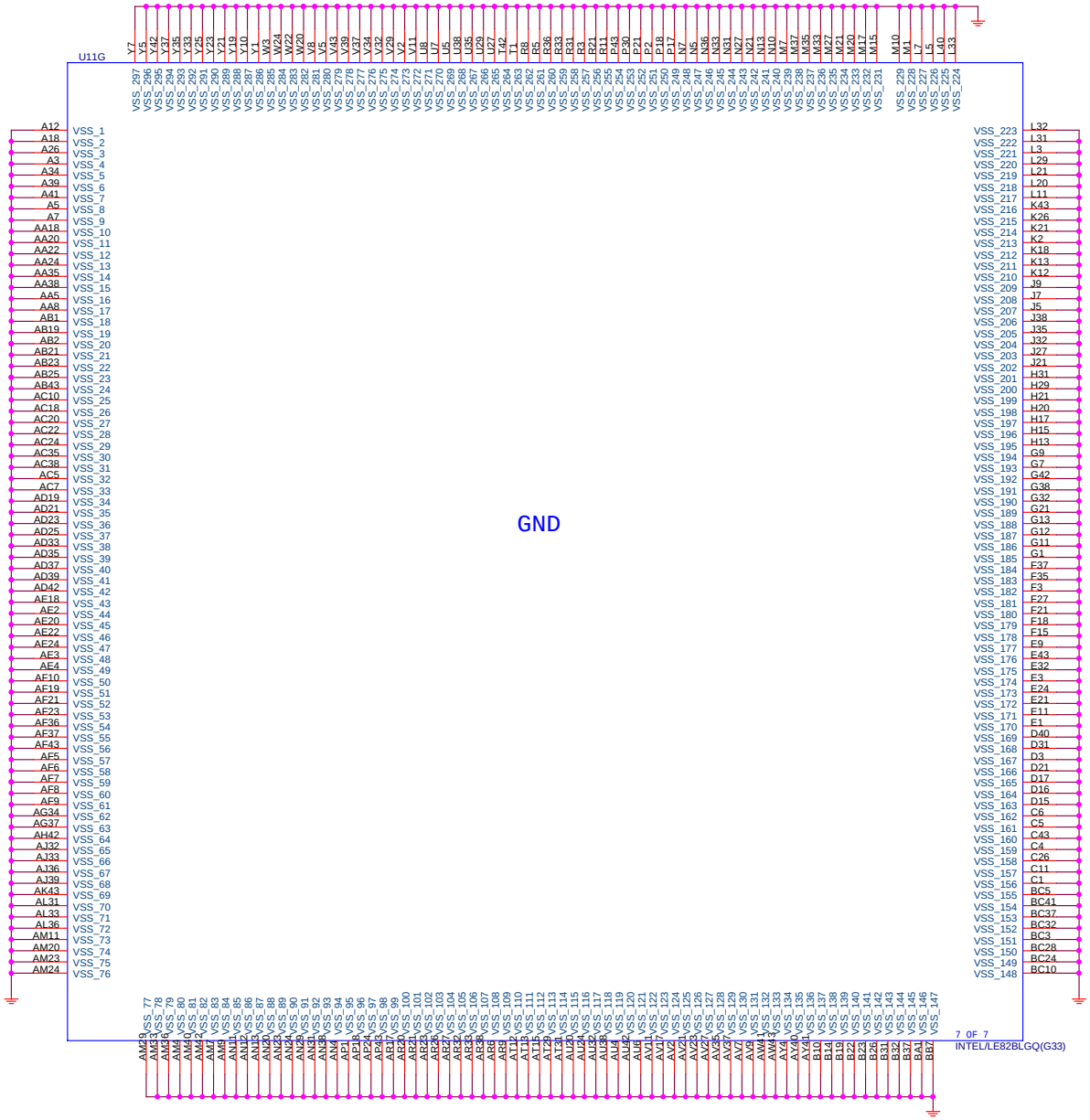
MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: Bearlake - Memory DDR2

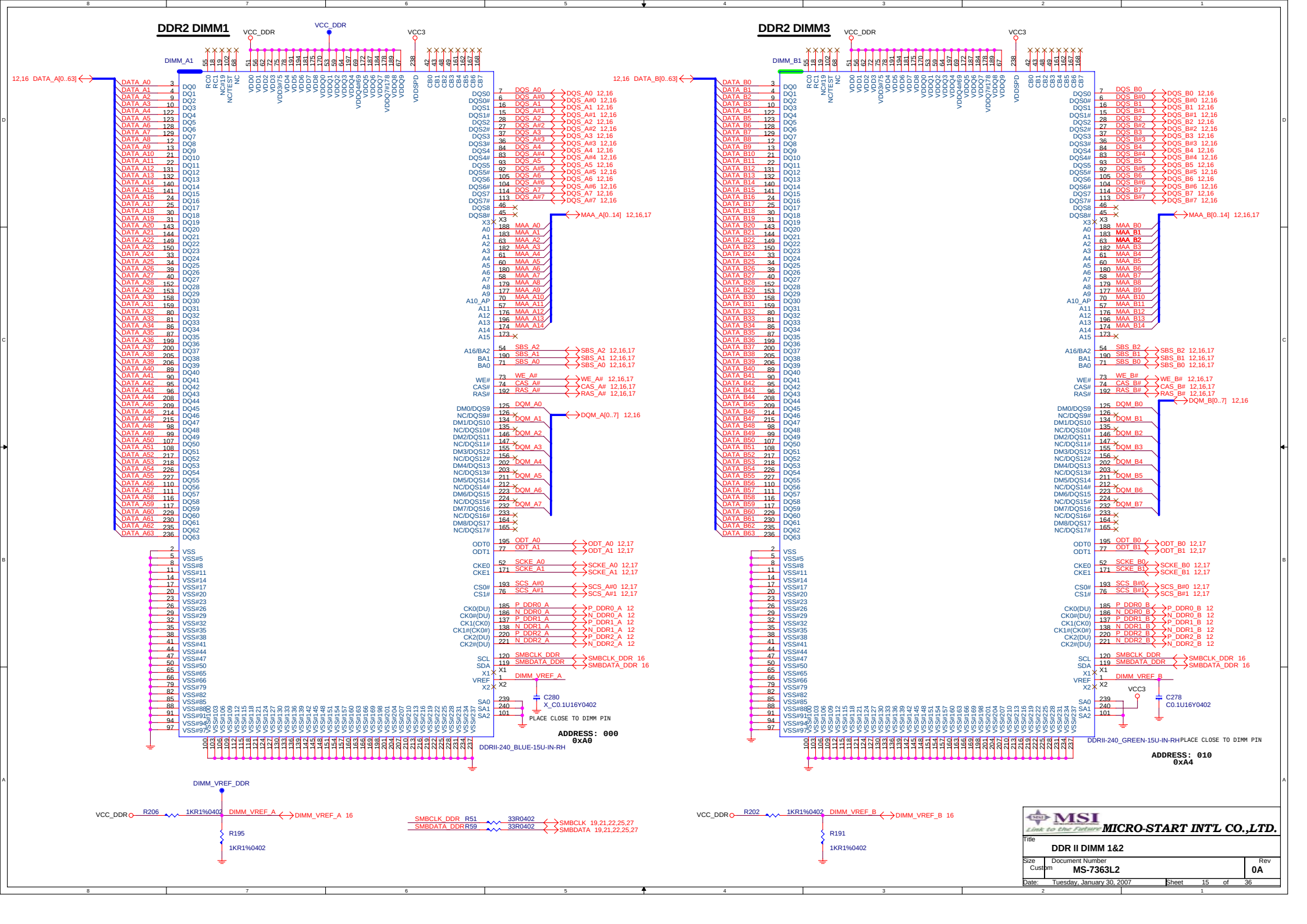
Size: Custom | Document Number: MS-7363L2 | Rev: 0A

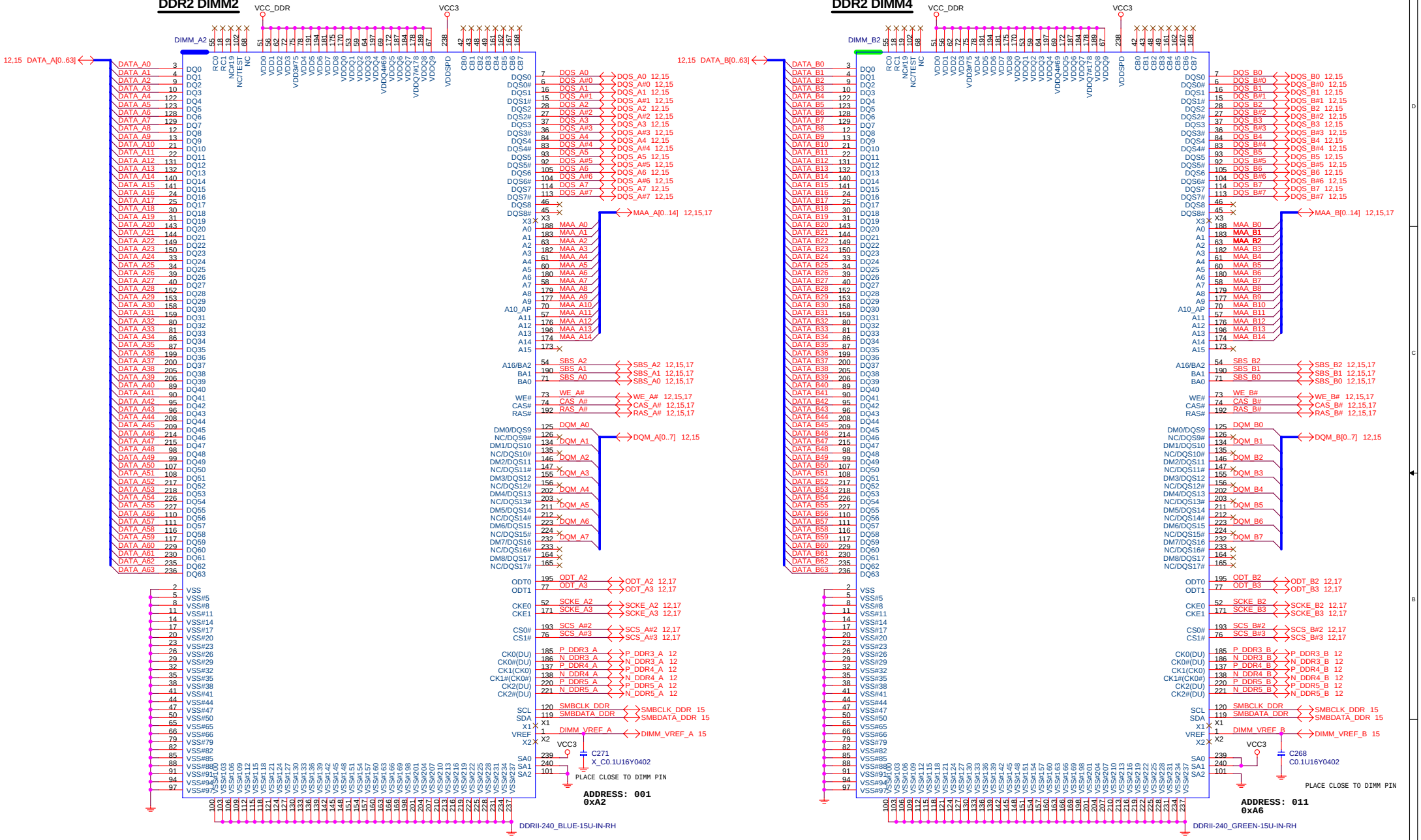
Date: Tuesday, January 30, 2007 | Sheet 12 of 36


POWER
U11F
V_1P25_CORE
V_FSB_VTT
V_FSB_VTT_GMCH
VCCD_CRT
VCCDQ_CRT
For non-Graphic sku
change to 0-ohm (0402)
change to 0-ohm (0603)
C228
C0.1U16Y0402
C225
C1U10Y
L20
X_10U100M_0805
R182
1R-LF
CP10
X_COPPER
C247
X_C2.2U6.3Y
C246
VCCA_GPLL
L14
CP5
R159
X_1R-LF
C215
VCCA_MPLL
L15
CP6
C218
C216
VCCA_HPLL
If non-Graphic sku
Remove these resisters
R164
0R0402
R165
H_VCCPLL
9 H_VCCPLL
V_3P3_DAC_FILTERED
C248
C0.1U16Y0402
VCC3
VCCA_EXP
L11
CP3
R141
X_1R-LF
C184
X_C2.2U6.3Y
C188
C1U10Y
VCC_DDR
L16
CP7
C223
C222
L17
CP8
C227
C224
VCCA_DPLLA
VCCA_DPLLB
VCCA_DAC_GMCH
L18
X_0.1U50M
CP9
C242
C243
C240
C0.01U16X0402
R178
For non-Graphic sku
Cxx change to 0-ohm
Rxx unstuff
VCC_DDR_GMCH
V_FSB_VTT
C206 C1U6.3Y0402-RH
C174 C1U6.3Y0402-RH
C192 C1U6.3Y0402-RH
C183 C1U6.3Y0402-RH
Botton Side
C629 C0.1U25Y
C166 C10U10Y0805
Botton Side
C625 C0.1U25Y
C186 C1U6.3Y0402-RH
C627 C0.1U25Y
C182 C1U10Y0402
V_1P25_CORE
C294 C10U10Y0805
C296 C10U10Y0805
C275 C2.2U6.3Y
C274 C2.2U6.3Y
C292 C10U10Y0805
C263 C2.2U6.3Y
C290 C10U10Y0805
C282 C2.2U6.3Y
C293 C10U10Y0805
C249 C0.1U16Y0402
C255 C0.1U16Y0402
C256 C0.1U16Y0402
C264 C0.1U16Y0402
C276 C0.1U16Y0402
C254 C0.1U16Y0402
C253 C0.1U16Y0402
C277 C0.1U16Y0402
C265 C0.1U16Y0402
C221 C0.1U16Y0402
C626 C0.1U25Y
C623 C0.1U25Y
C630 C0.1U25Y
C628 C10U10Y0805
C624 C10U10Y0805
C291 C10U10Y0805
Place in the Bottom side
V1P25_GMCH
V_1P25_PCIE
L21
X_80L3_70_0805
CP11
X_COPPER
C250
C0.1U16Y0402
C258
C1U10Y
6 OF 7
INTEL/LE82BLGQ(G33)
Separate when AMT is supported
MSI
MICRO-START INT'L CO.,LTD.
Title
Bearlake - Power
Size
Custom
Document Number
MS-7363L2
Rev
0A
Date: Tuesday, January 30, 2007
Sheet 13 of 36



MICRO-START INT'L CO.,LTD.	
Title	Bearlake - GND
Size: Custom	Document Number: MS-7363L2
Rev	0A
Date: Tuesday, January 30, 2007	Sheet 14 of 36


DDR2 DIMM1
DDR2 DIMM3
DIMM_A1
DIMM_B1
VCC_DDR
VCC3
12,16 DATA_A[0..63]
12,16 DATA_B[0..63]
MAA_A[0..14] 12,16,17
MAA_B[0..14] 12,16,17
DQM_A[0..7] 12,16
DQM_B[0..7] 12,16
DIMM_VREF_A
DIMM_VREF_B
C280
X_C0.1U16Y0402
C278
C0.1U16Y0402
PLACE CLOSE TO DIMM PIN
ADDRESS: 000
0xA0
ADDRESS: 010
0xA4
DDRII-240_BLUE-15U-IN-RH
DDRII-240_GREEN-15U-IN-RH
DIMM_VREF_DDR
R206
1KR1%0402
R195
R202
R191
SMBCLK_DDR R51
SMBDATA_DDR R59
33R0402
SMBCLK 19,21,22,25,27
SMBDATA 19,21,22,25,27
MICRO-START INT'L CO.,LTD.
Title
DDR II DIMM 1&2
Size
Custom
Document Number
MS-7363L2
Rev
0A
Date: Tuesday, January 30, 2007
Sheet 15 of 36

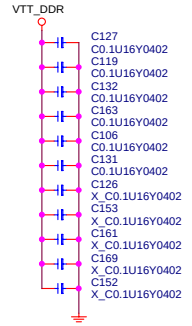


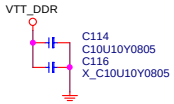
MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: DDR II DIMM 3 & 4		
Size: Custom	Document Number: MS-7363L2	Rev: 0A
Date: Tuesday, January 30, 2007	Sheet 16 of 36	

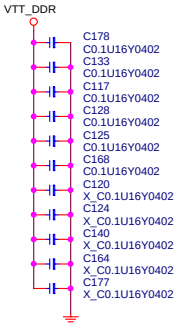
DDR II TERMINATION

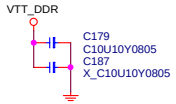
CHANNEL A VTT_DDR DECOULPING CAPS

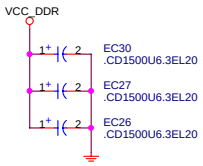


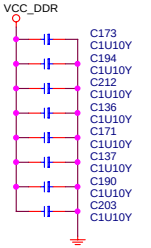


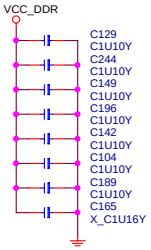
CHANNEL B VTT_DDR DECOULPING CAPS

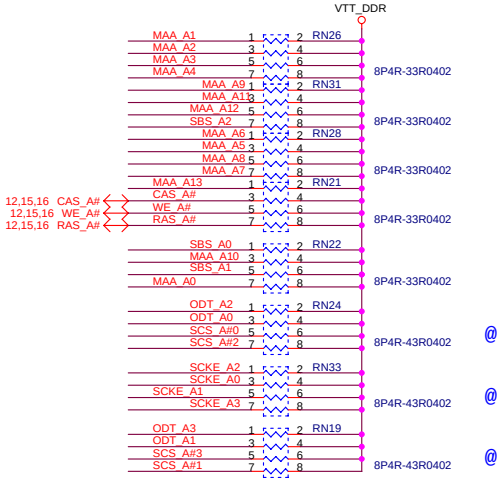


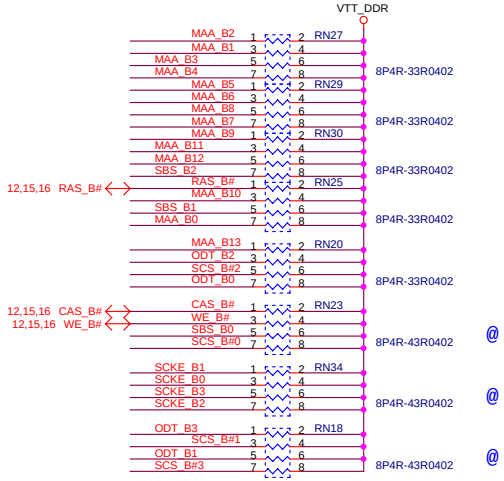


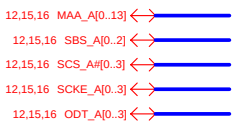


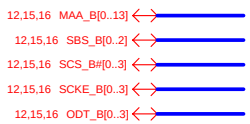






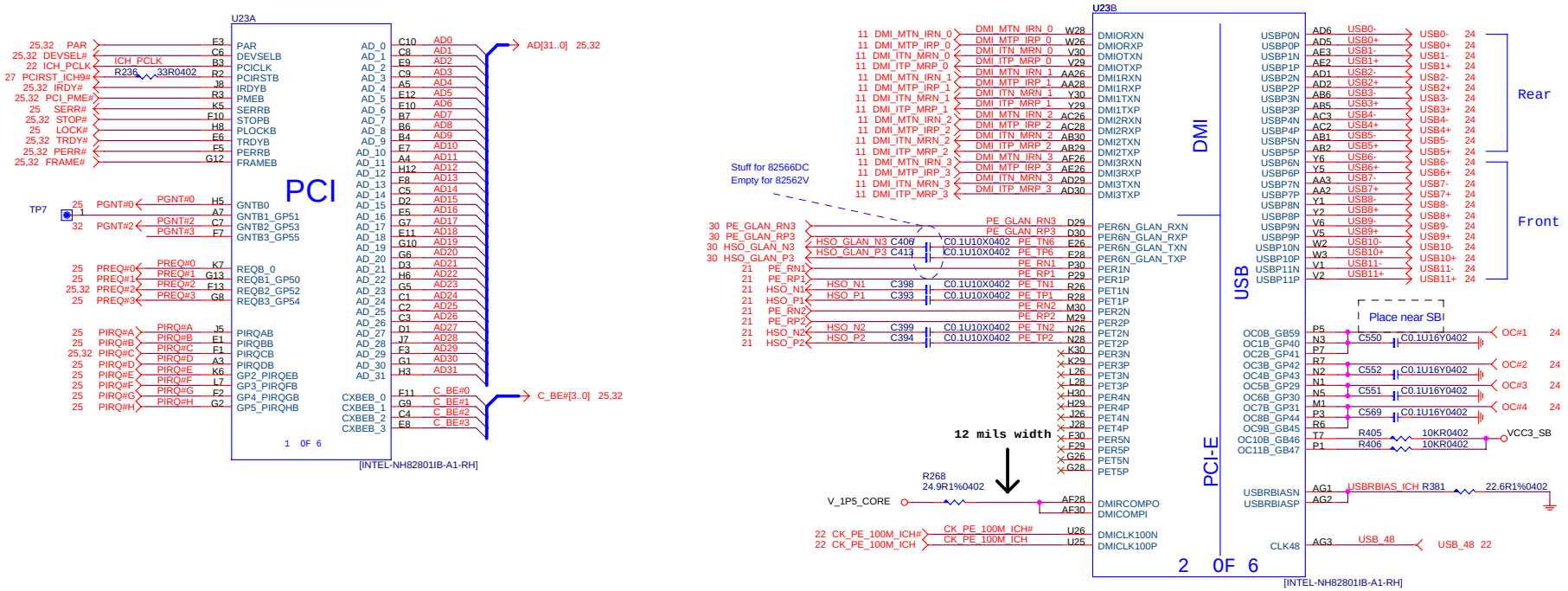


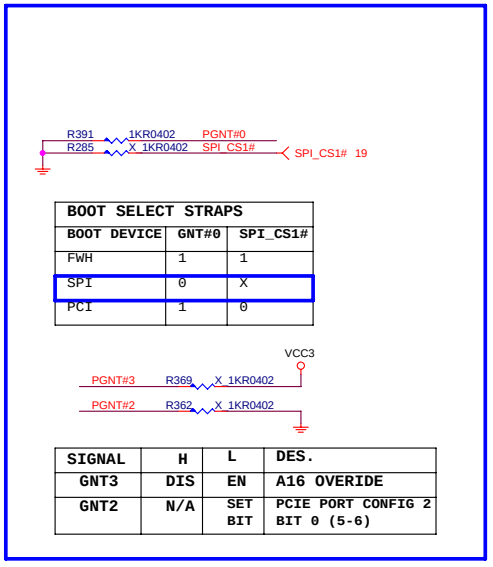


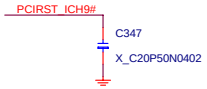


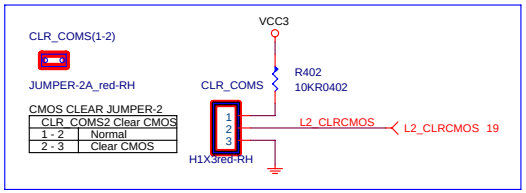
MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: DDR II Termination		
Size: Custom	Document Number: MS-7363L2	Rev: 0A
Date: Tuesday, January 30, 2007	Sheet 17 of 36	





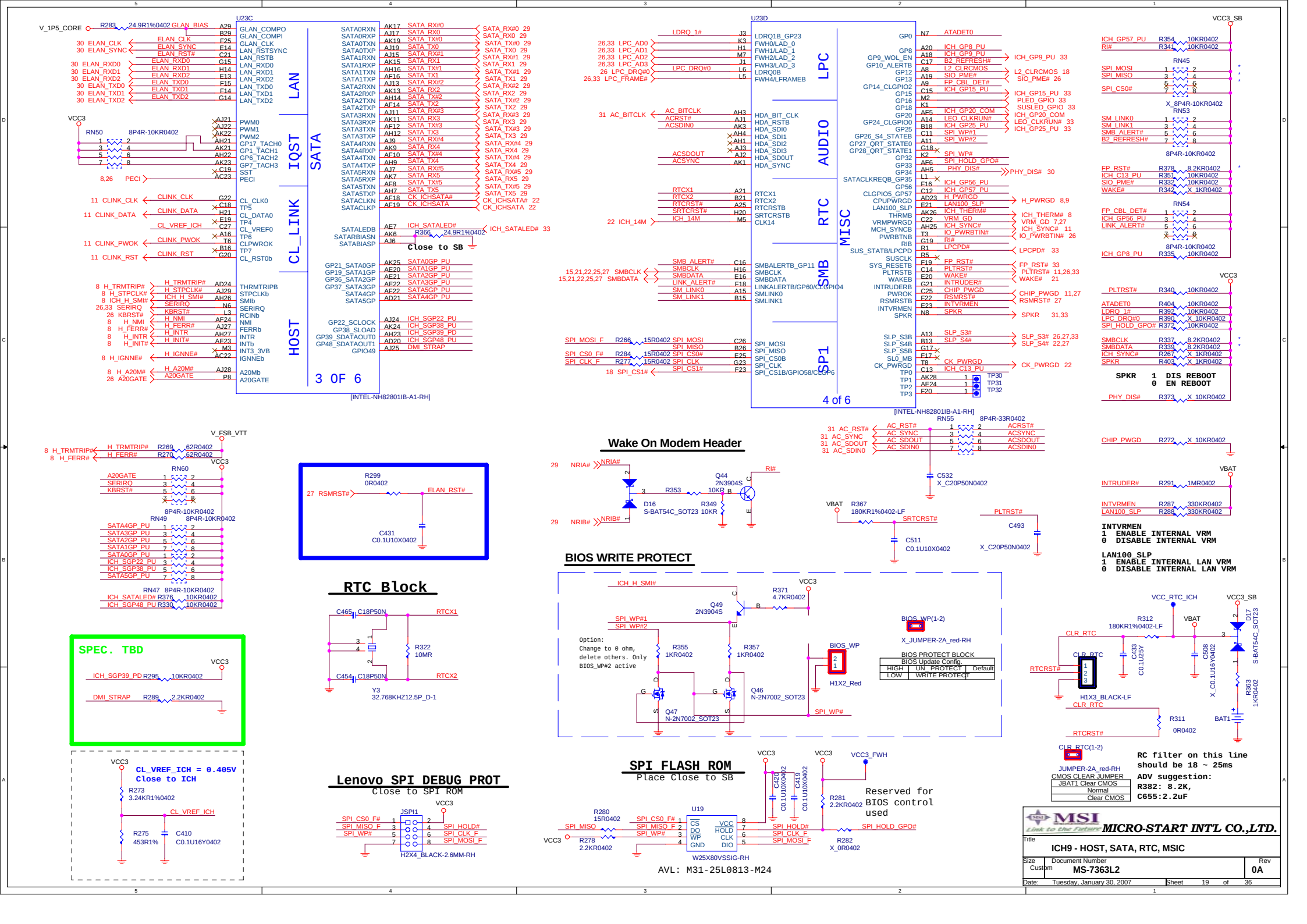




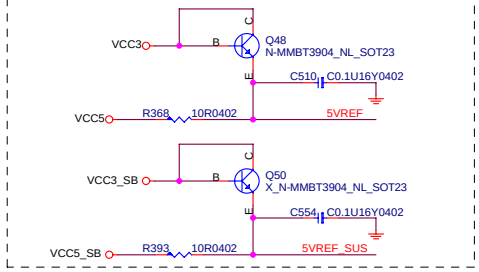
MSI MICRO-START INT'L CO.,LTD.

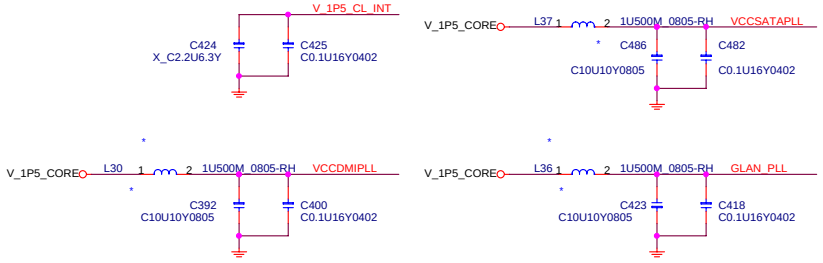
Link to the Future

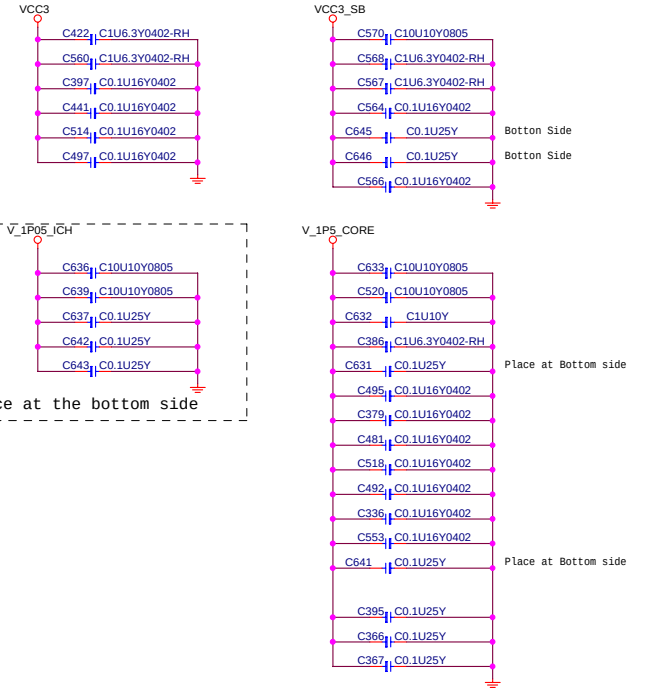
Title	ICH9 - PCI, USB, DMI, PCIEX1	
Size: Custom	Document Number: MS-7363L2	Rev: 0A
Date: Tuesday, January 30, 2007	Sheet 18 of 36	

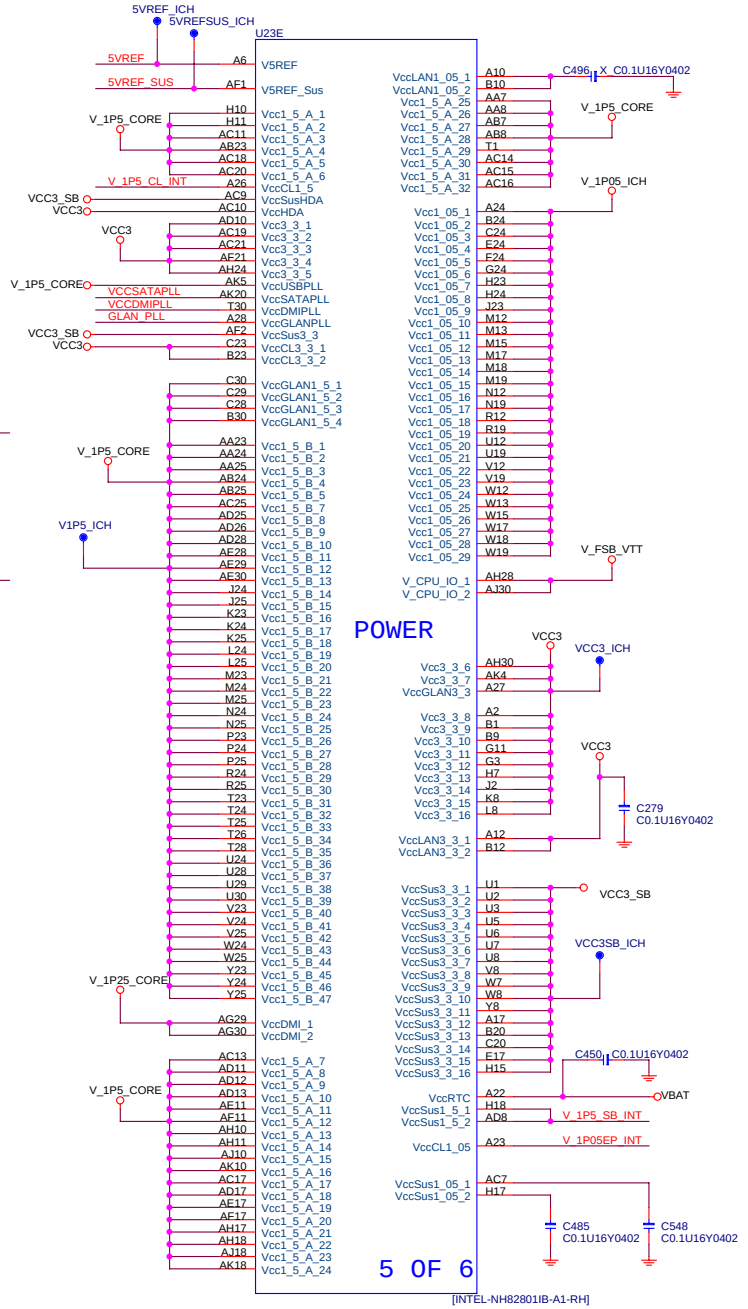

U23C
SATA
LAN
IQST
CL_LINK
HOST
3 OF 6
[INTEL-NH82801IB-A1-RH]
U23D
LPC
AUDIO
RTC
SMB
GPI
MISC
4 of 6
[INTEL-NH82801IB-A1-RH]
Close to SB
Wake On Modem Header
BIOS WRITE PROTECT
RTC Block
SPEC. TBD
CL_VREF_ICH = 0.405V
Close to ICH
Lenovo SPI DEBUG PROT
Close to SPI ROM
SPI FLASH ROM
Place Close to SB
Reserved for BIOS control used
W25X80VSSIG-RH
AVL: M31-25L0813-M24
SPKR 1 DIS REBOOT
0 EN REBOOT
INTVRMEN
1 ENABLE INTERNAL VRM
0 DISABLE INTERNAL VRM
LAN100_SLP
1 ENABLE INTERNAL LAN VRM
0 DISABLE INTERNAL LAN VRM
RC filter on this line should be 18 ~ 25ms
ADV suggestion:
R382: 8.2K,
C655:2.2uF
BIOS PROTECT BLOCK
BIOS Update Config.
HIGH UN_ PROTECT Default
LOW WRITE PROTECT
CMOS CLEAR JUMPER
JBAT1 Clear CMOS
Normal
Clear CMOS
MICRO-START INT'L CO.,LTD.
ICH9 - HOST, SATA, RTC, MSIC
MS-7363L2
0A
Tuesday, January 30, 2007
Sheet 19 of 36

5VREF & 5VREF_SUS Sequencing Circuit



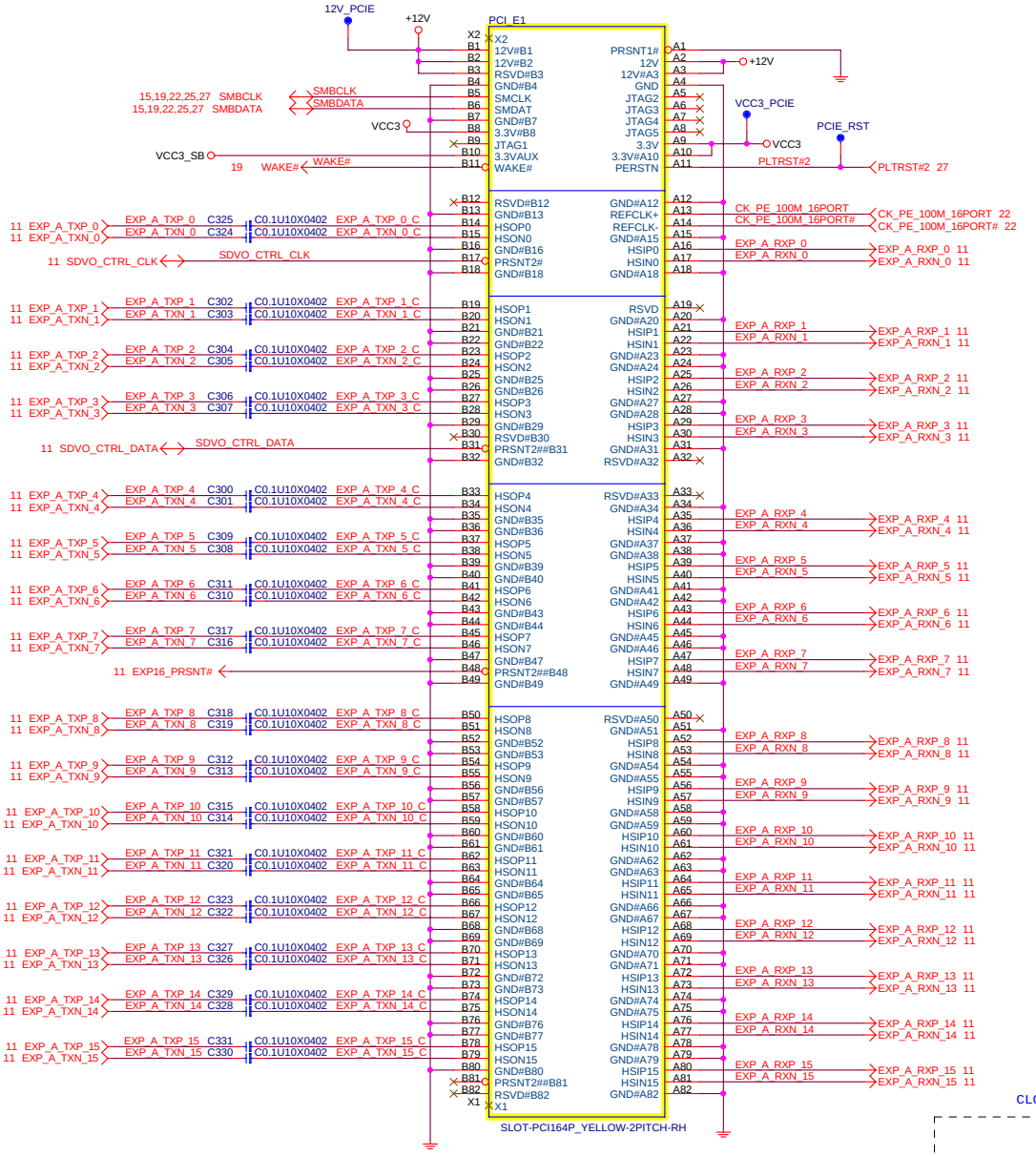


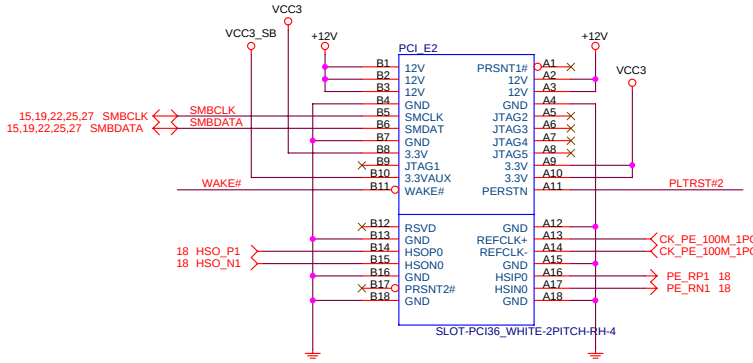


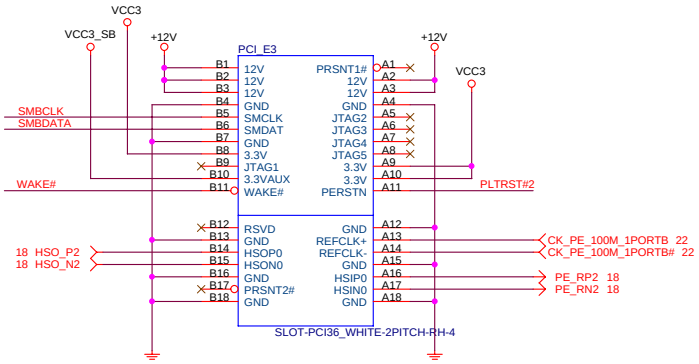


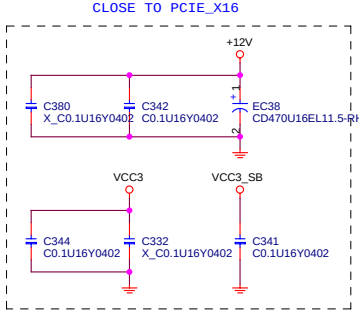
MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title	ICH9 - POWER, GND	
Size: Custom	Document Number: MS-7363L2	Rev: 0A
Date: Tuesday, January 30, 2007	Sheet 20 of 36	





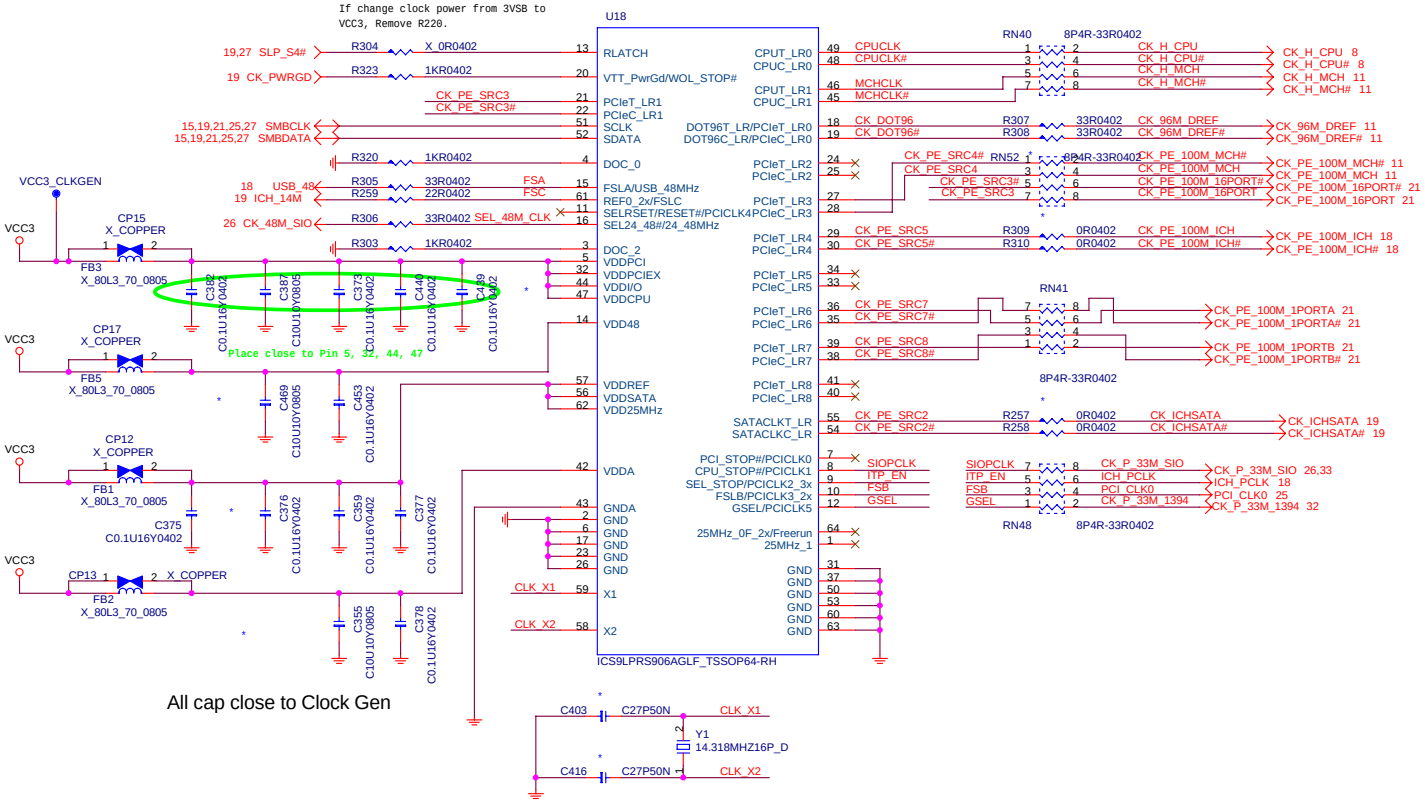




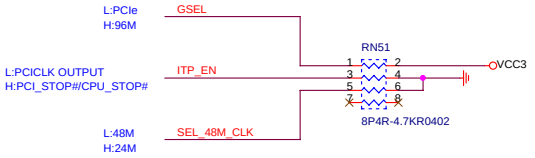
MICRO-START INT'L CO.,LTD.

Title	PCI Express Slot - X16, X1	
Size: Custom	Document Number: MS-7363L2	Rev: 0A
Date: Tuesday, January 30, 2007	Sheet 21 of 36	

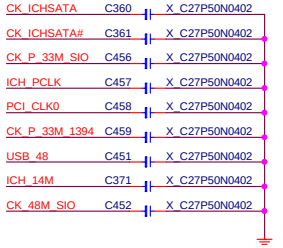
Clock Generator ICSLPRS906



CLOCK GEN STRAPING

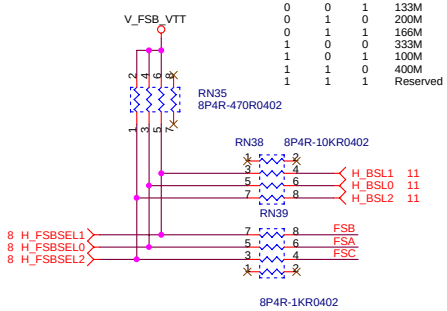


CLOCK GEN RISE/FALL TIME MODIFY



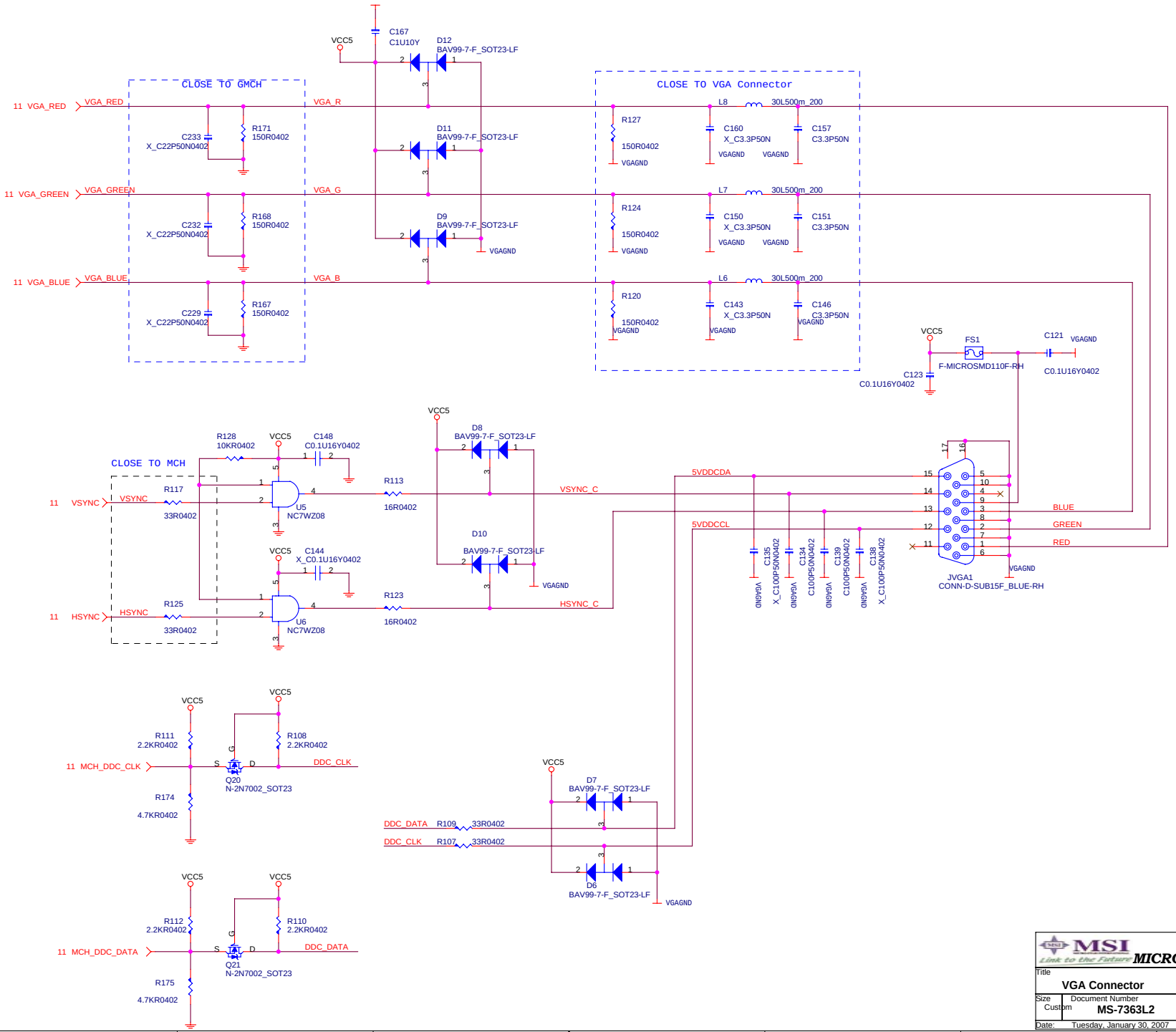
BSEL[0..2] Level Shift

FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M
1	1	1	Reserved



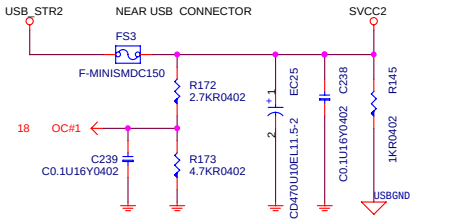
MSI MICRO-START INT'L CO.,LTD.

Title: Clock Generator ICS9LPRS906		
Size: Custom	Document Number: MS-7363L2	Rev: 0A
Date: Tuesday, January 30, 2007	Sheet 22 of 36	

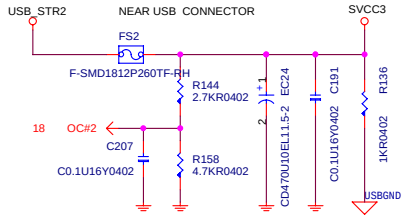


MSI MICRO-START INT'L CO.,LTD.		
Title: VGA Connector		
Size: Custom	Document Number: MS-7363L2	Rev: 0A
Date: Tuesday, January 30, 2007	Sheet 23 of 36	

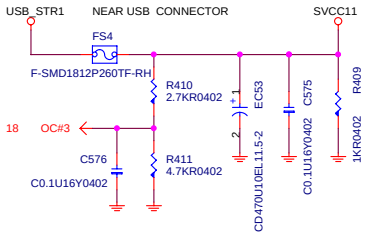
POWER CIRCUIT FOR USB PORT 0,1 — Rear



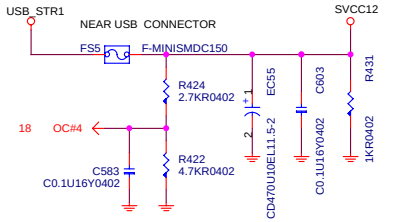
POWER CIRCUIT FOR USB PORT 2,3,4,5 — Rear



POWER CIRCUIT FOR USB PORT 6,7,8,9 — Front

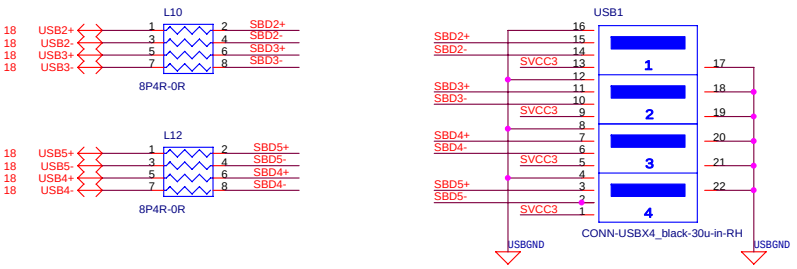


POWER CIRCUIT FOR USB PORT 10,11 — Front

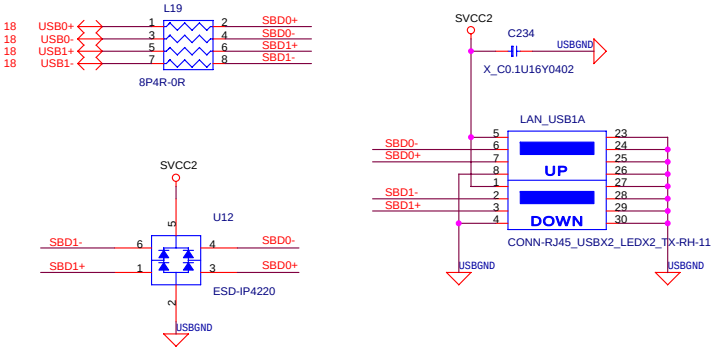


REAR PANEL USB CONNECTOR FOR USB PORT 2,3,4,5

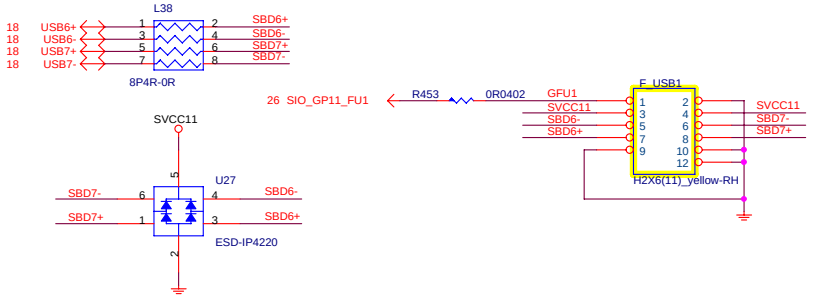
L12-181D017-CA8



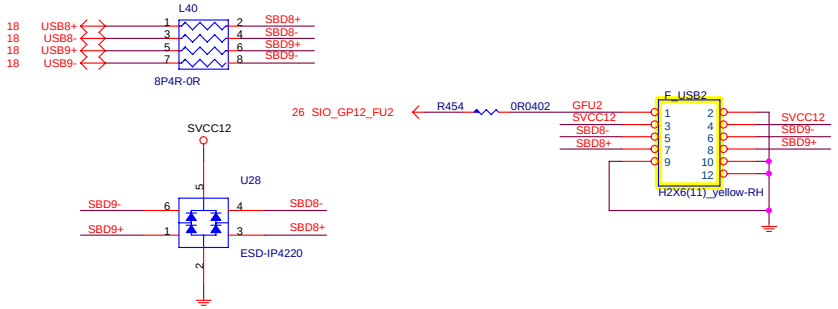
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



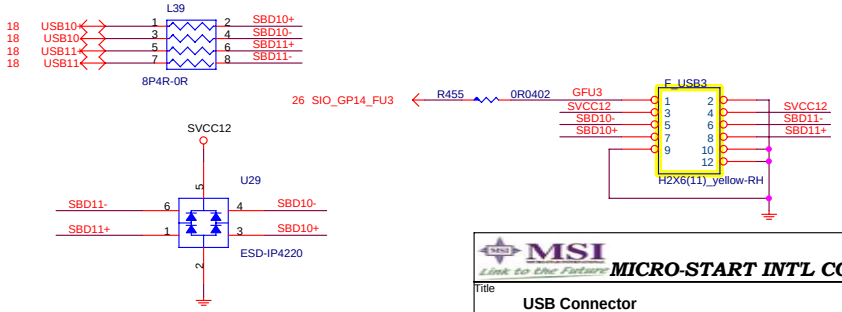
FRONT PANEL USB CONNECTOR FOR USB PORT 6,7



FRONT PANEL USB CONNECTOR FOR USB PORT 8,9



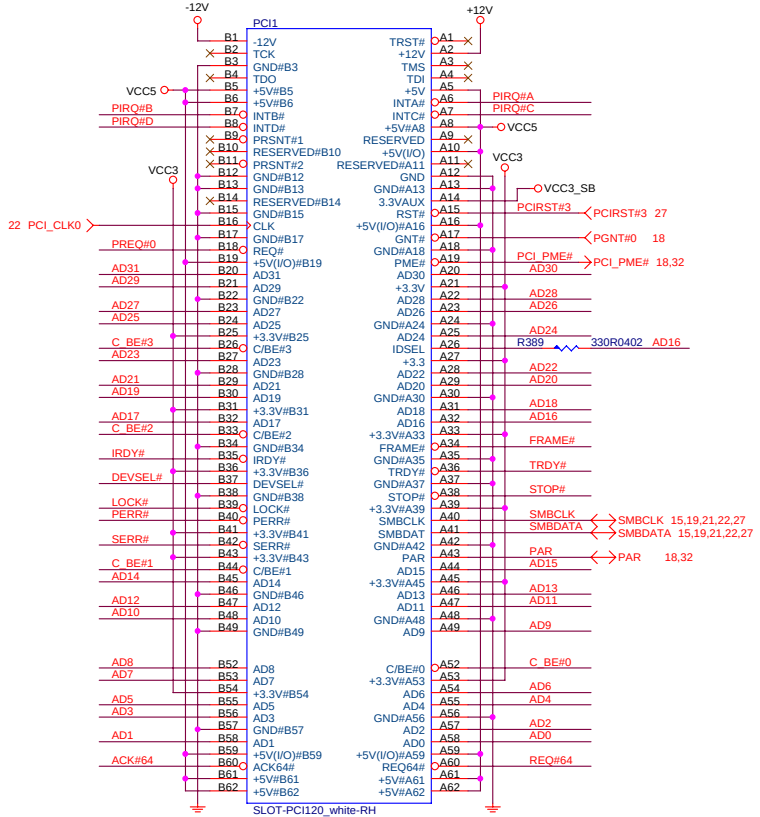
FRONT PANEL USB CONNECTOR FOR USB PORT 10,11



MICRO-START INT'L CO.,LTD.

Title: USB Connector		
Size: Custom	Document Number: MS-7363L2	Rev: 0A
Date: Tuesday, January 30, 2007	Sheet 24 of 36	

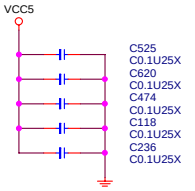
PCI SLOT 1 (PCI VER: 2.3 COMPLY)



18,32 AD[0..31] — AD[0..31]

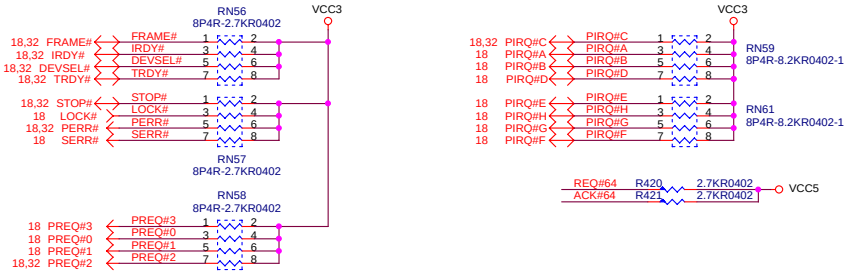
18,32 C_BE#[0..3] — C_BE#[0..3]

IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

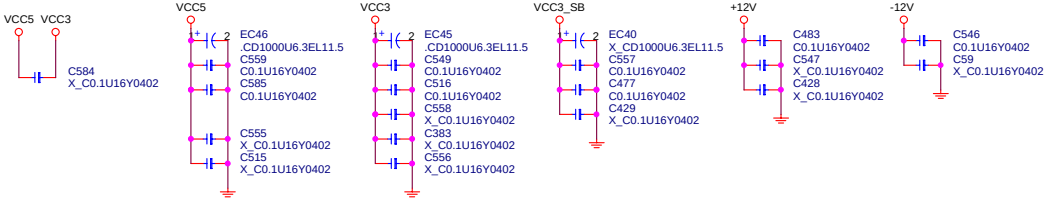


Place close to VGA side

PCI PULL-UP / DOWN RESISTORS

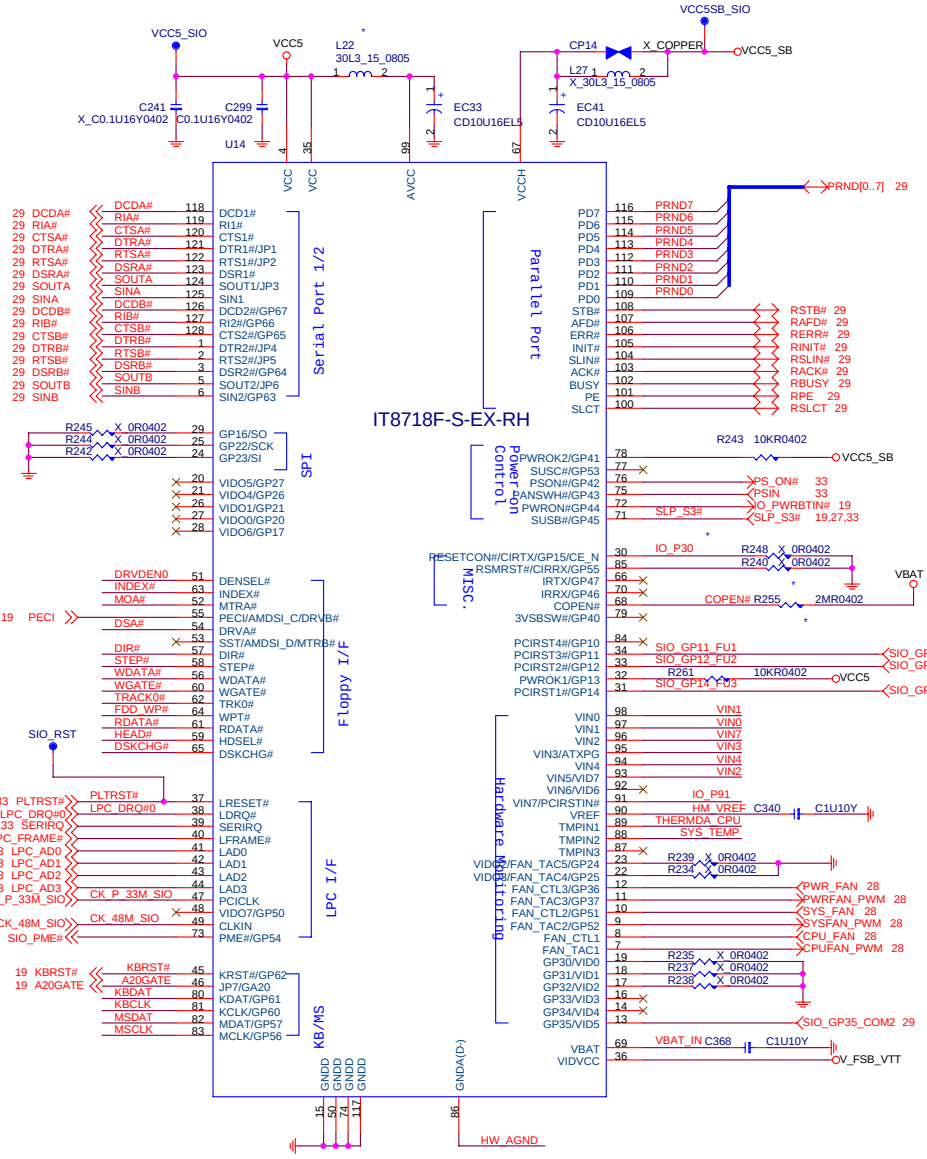


PCI SLOT DECOUPLING CAPACITORS

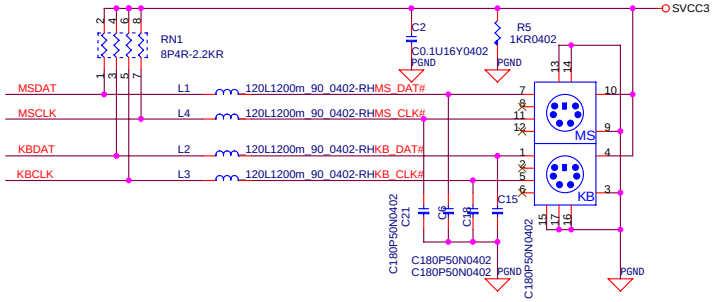


MSI Link to the Future **MICRO-START INT'L CO.,LTD.**

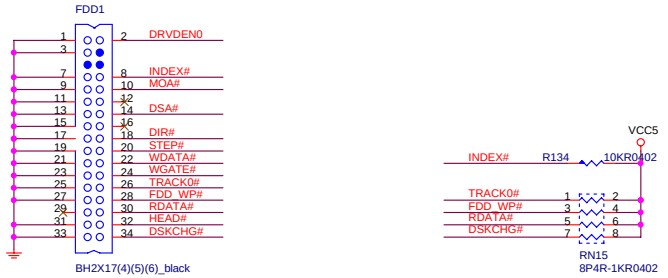
Title: PCI SLOT 1 & 2		
Size: Custom	Document Number: MS-7363L2	Rev: 0A
Date: Tuesday, January 30, 2007	Sheet 25 of 36	



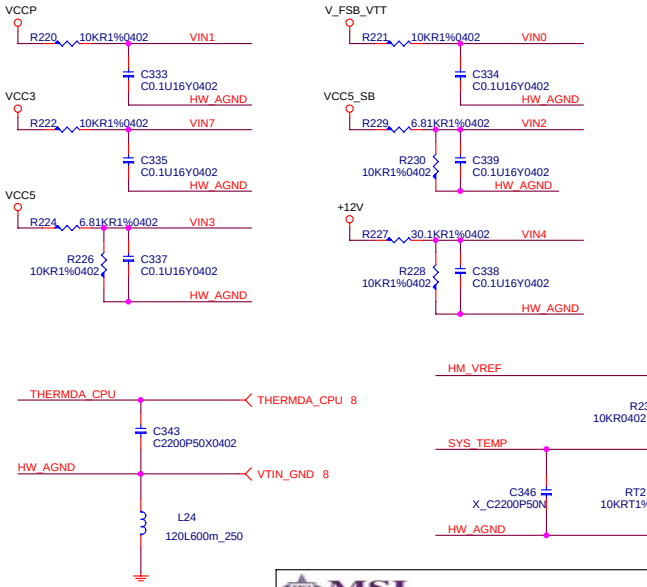
PS2 KEYBOARD & MOUSE CONNECTOR



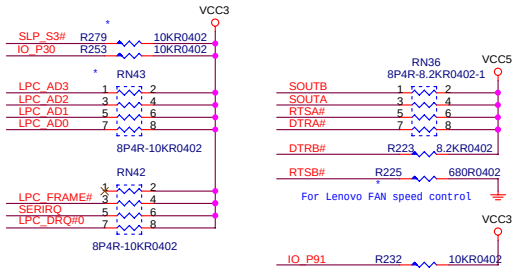
FLOPPY CONNECTOR



Thermal Resistor



SUPER I/O STRAPPING RESISTOR



Power On Strapping Options

Symbol	value	Description
Flashseg1_EN	1	Disabled.
	0	Flash I/F Address Segment 1 (FFFE_0000h~FFFF_FFFFh, 000F_0000h~000F_FFFFh) is enabled
VIDO_SEL	1	Disable VIDOUT pins(except VIDO6 & VIDO7)
	0	Enable VIDOUT pins
CHIP_SEL	--	Chip selection in configuration.
BUF_SEL	1	The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, PCIRST4# are open-drain.
	0	The output buffers are push-pull.
FAN_CTL_SEL	1	The default value of EC Index 15h / 16h / 17h is 00h
	0	The default value of EC Index 15h / 16h / 17h is 40h
VID_ISEL	1	The threshold voltage of VID is 2.0 / 0.8V
	0	The threshold voltage of VID is 0.8 / 0.4V

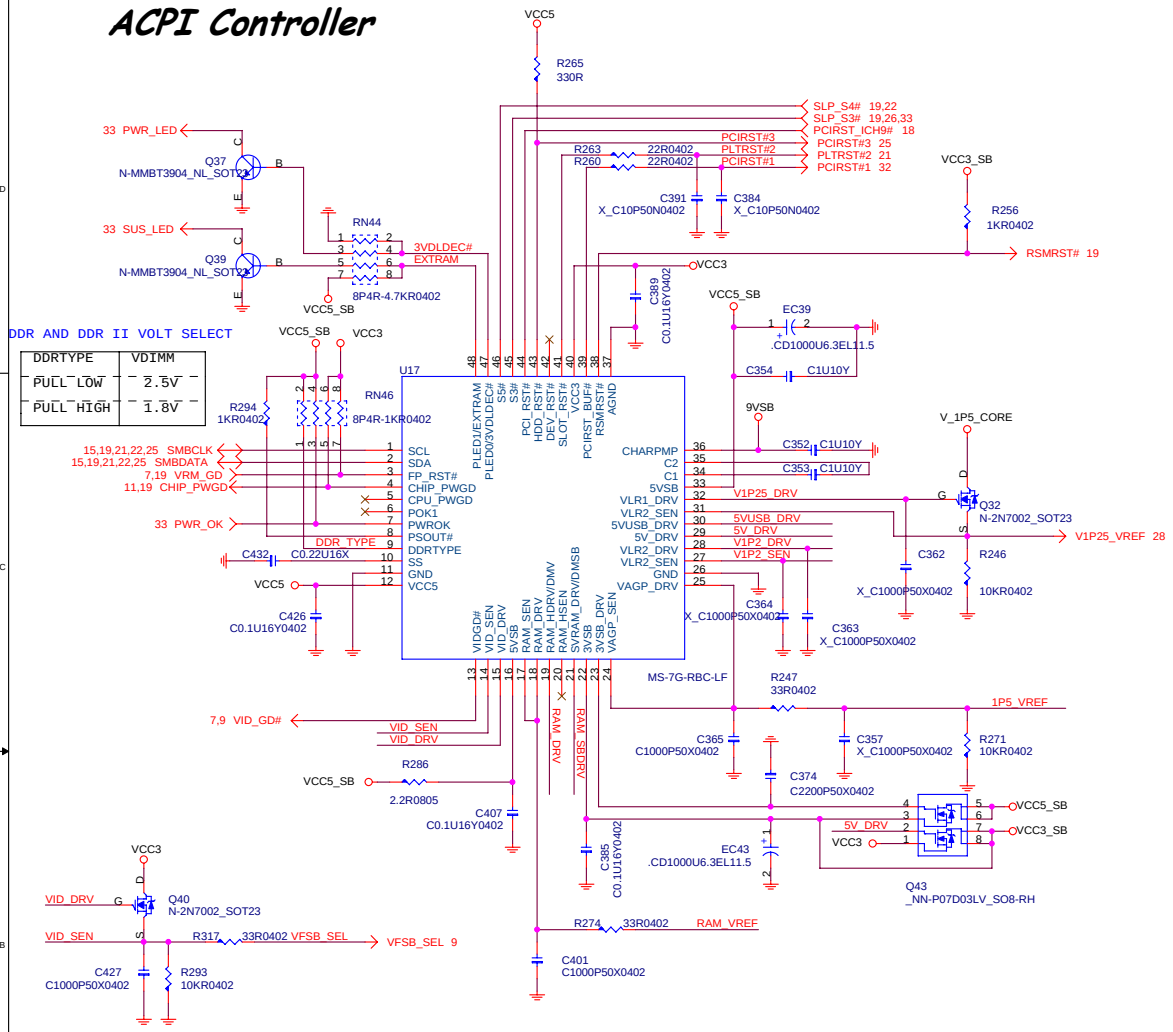
MICRO-START INT'L CO.,LTD.

Title: Super I/O ITE8718F

Size: Custom | Document Number: MS-7363L2 | Rev: 0A

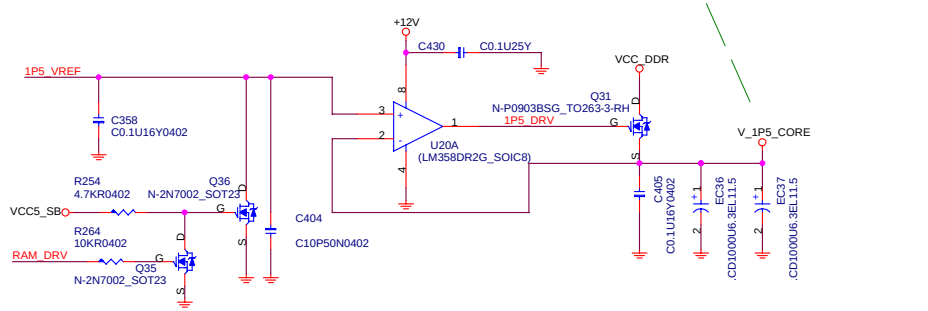
Date: Tuesday, January 30, 2007 | Sheet 26 of 36

ACPI Controller

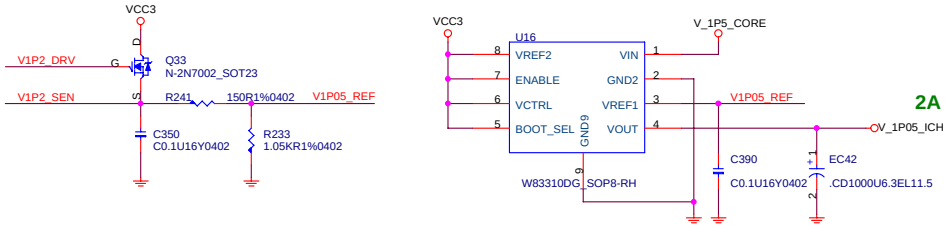


1.5V POWER

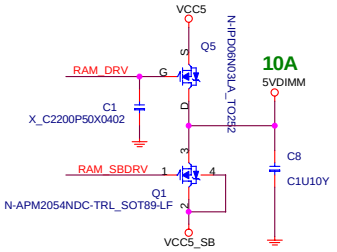
(1.0V-2A+V_FSB_VTT-5.8A+1.5V-2.75A)=10.55A



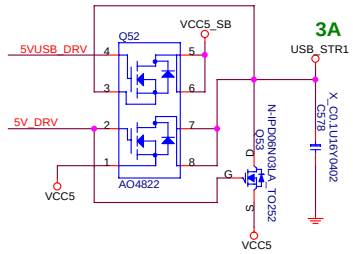
V_1P05_ICH Power



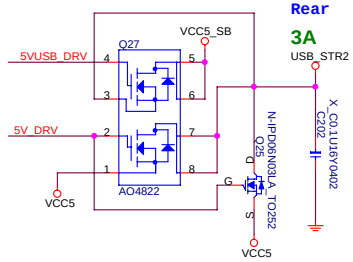
5V DIMM Power



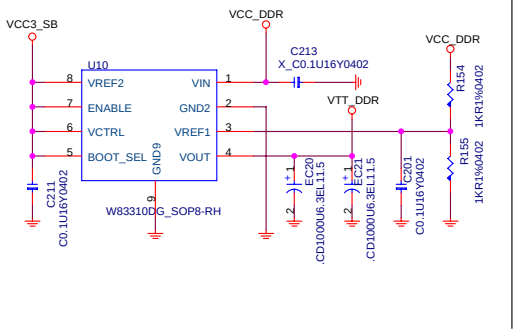
USB_STR1 Front



USB_STR2

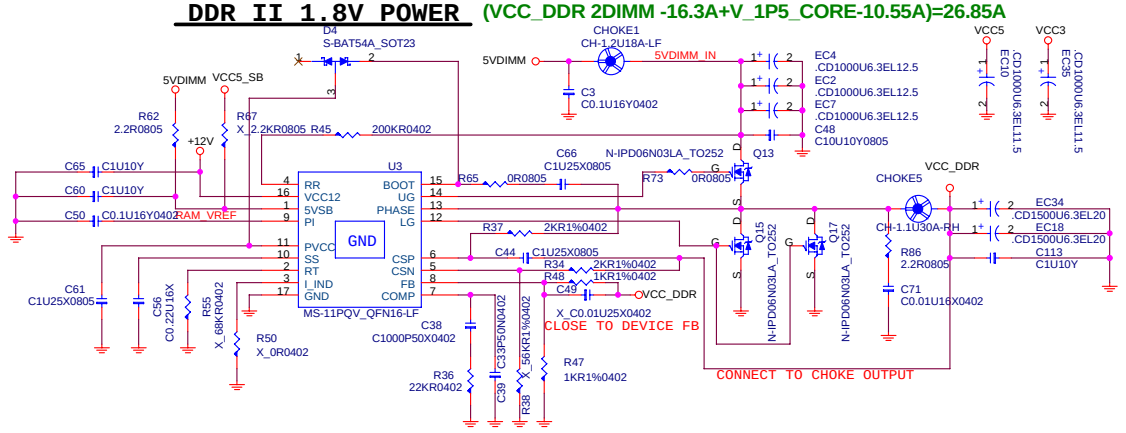


DDR II VTT POWER



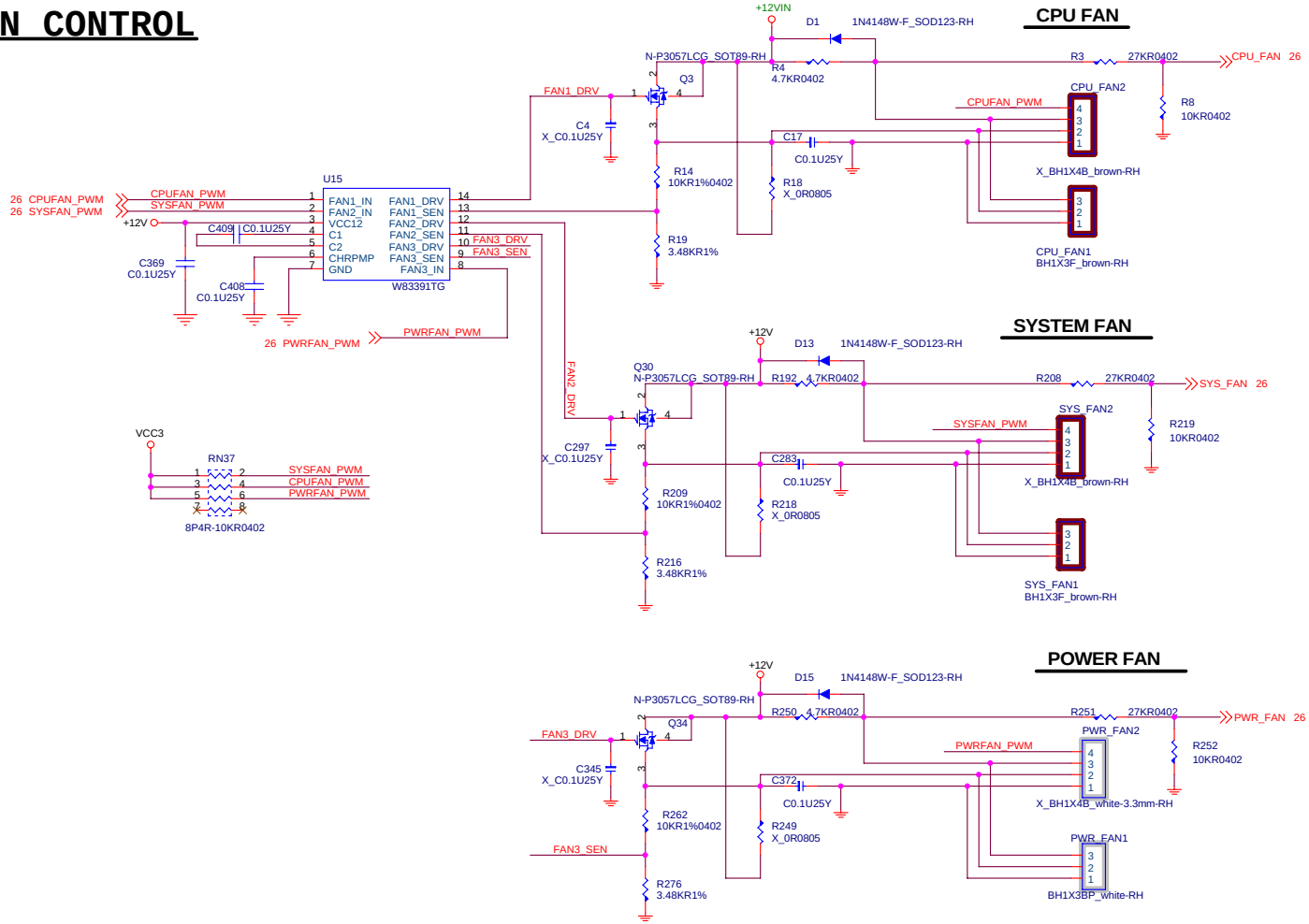
DDR II 1.8V POWER

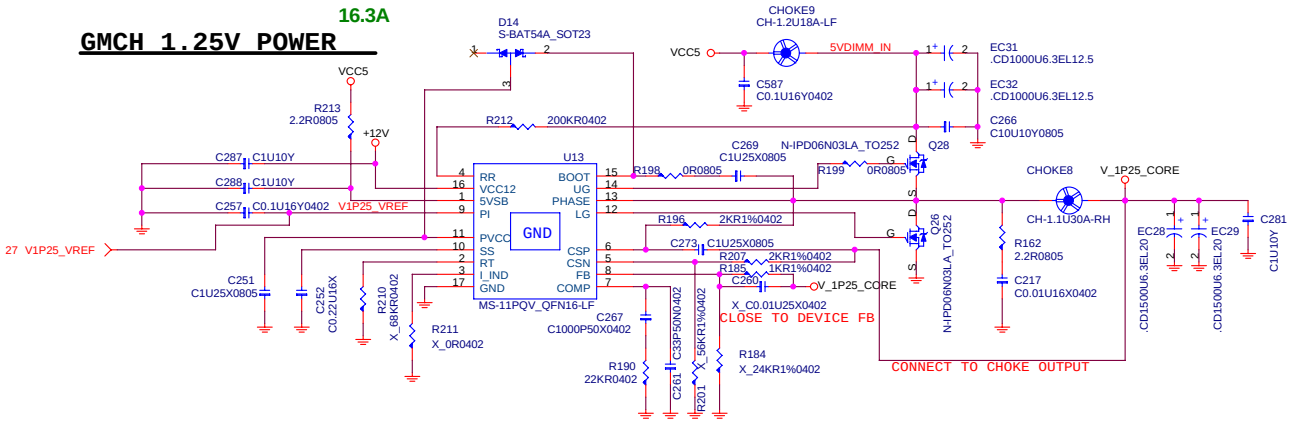
(VCC_DDR 2DIMM -16.3A+V_1P5_CORE-10.55A)=26.85A



MICRO-START INT'L CO.,LTD.	
Title	MS-7 ACPI Controller
Size: Custom	Document Number: MS-7363L2
Rev	0A
Date: Tuesday, January 30, 2007	Sheet 27 of 36

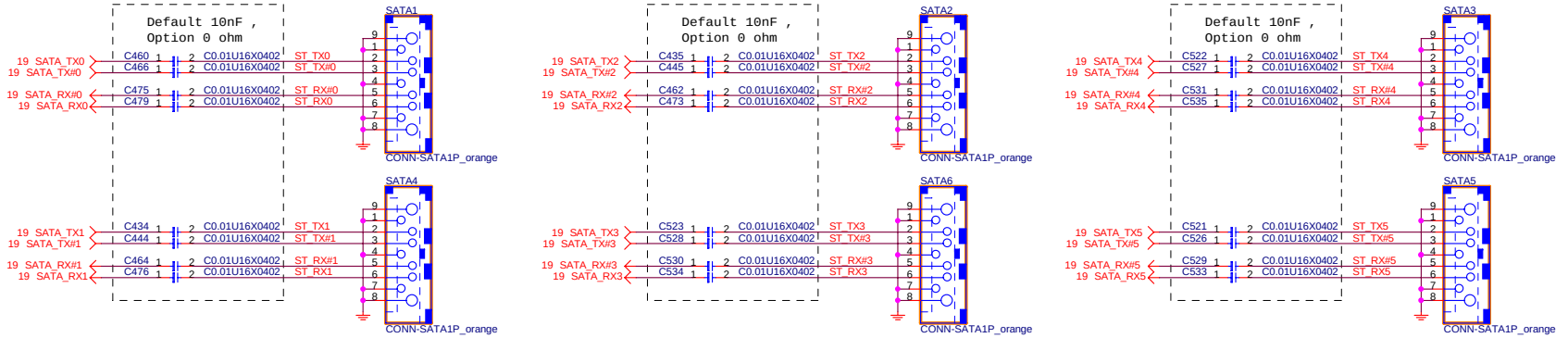
FAN CONTROL



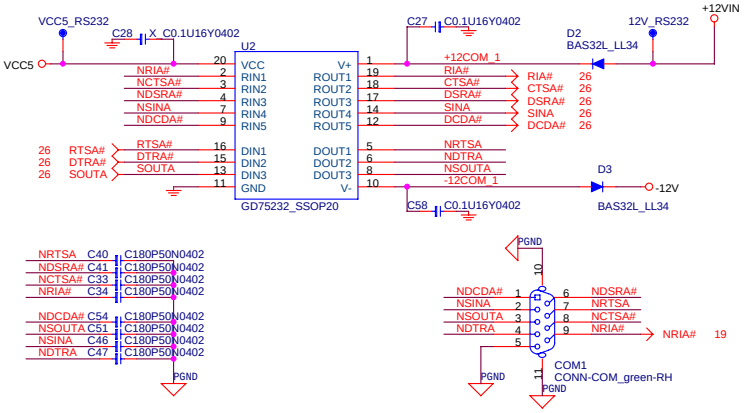


MSI Link to the Future MICRO-START INT'L CO.,LTD.		
Title: FWH & FAN & V_1P25_CORE		
Size: Custom	Document Number: MS-7363L2	Rev: 0A
Date: Tuesday, January 30, 2007	Sheet 28 of 36	

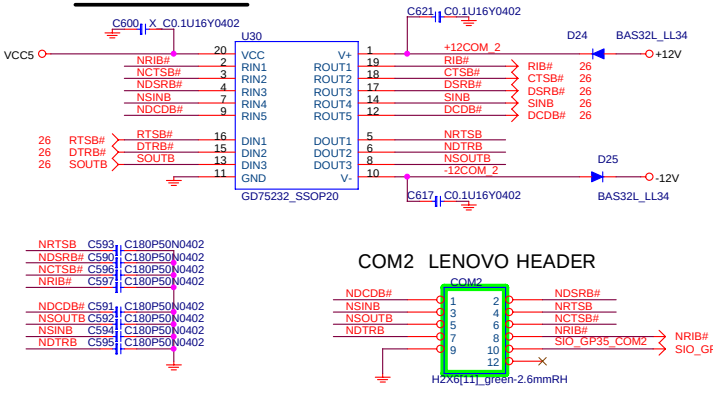
SERIAL ATA CONNECTOR BLOCK



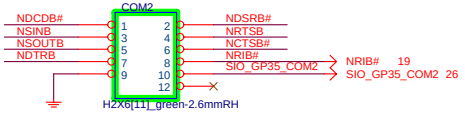
SERIAL PORT 1



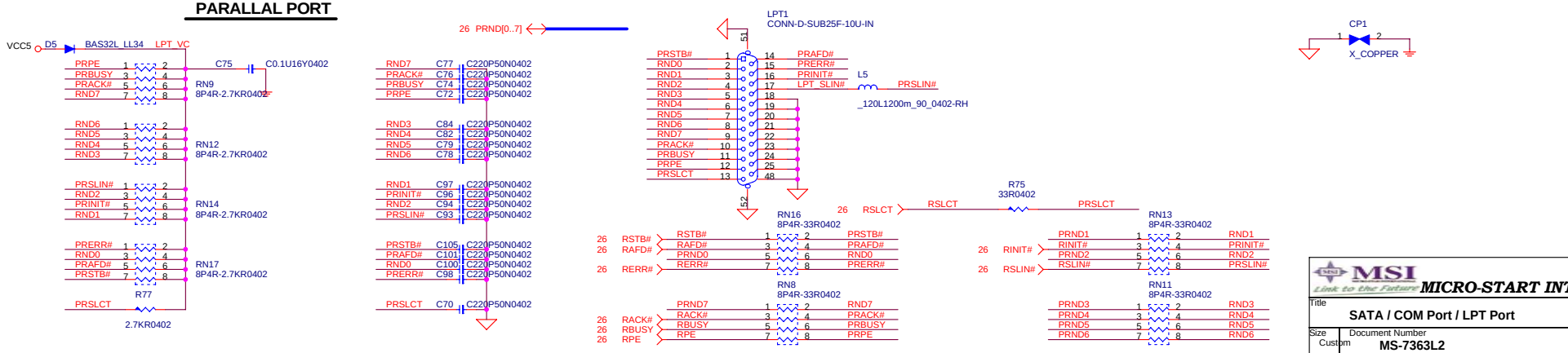
SERIAL PORT 2



COM2 LENOVO HEADER



PARALLAL PORT

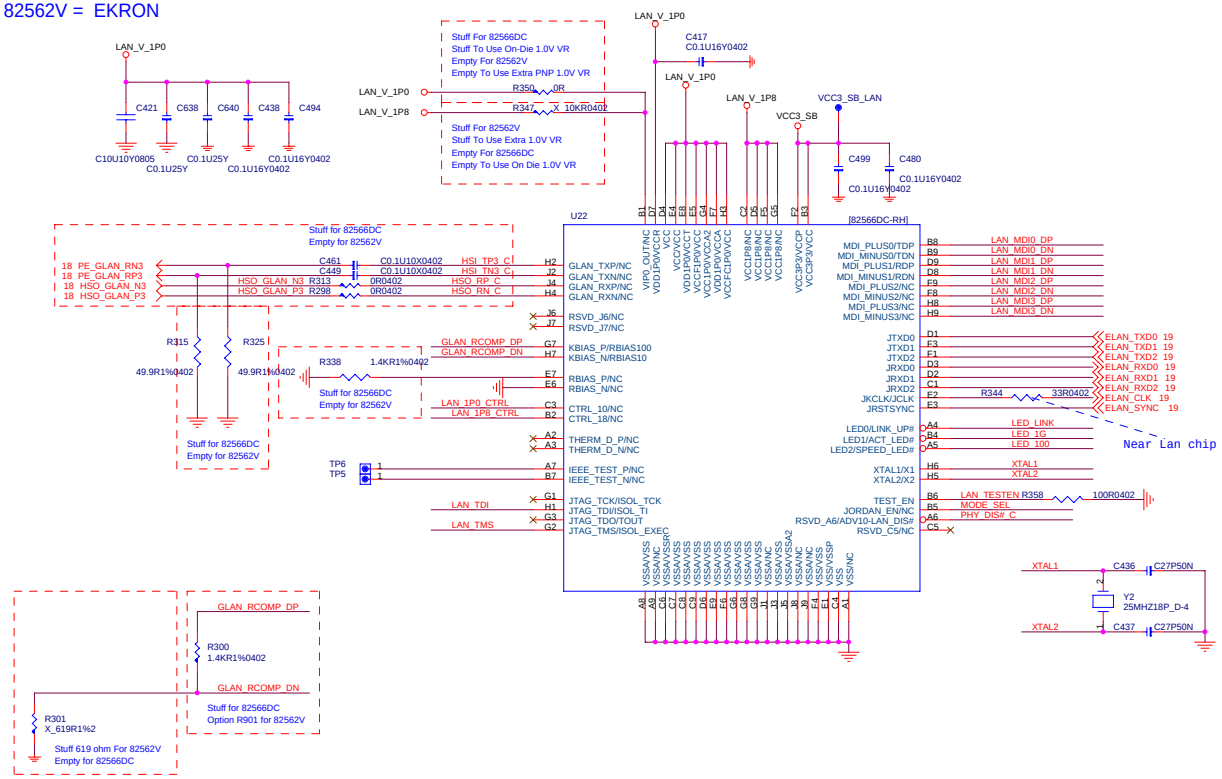


MSI MICRO-START INT'L CO.,LTD.

Title: SATA / COM Port / LPT Port		
Size: Custom	Document Number: MS-7363L2	Rev: 0A
Date: Tuesday, January 30, 2007	Sheet 29 of 36	

LAN - Intel LAN 82566DC/82562V

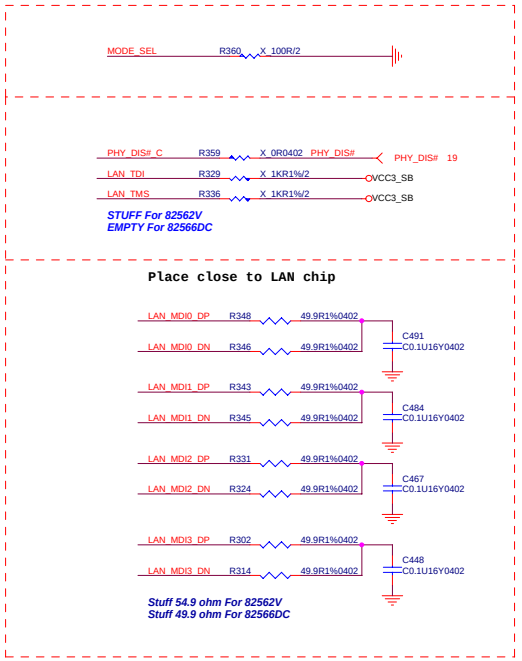
82566DC = NINEVEH
82562V = EKRON

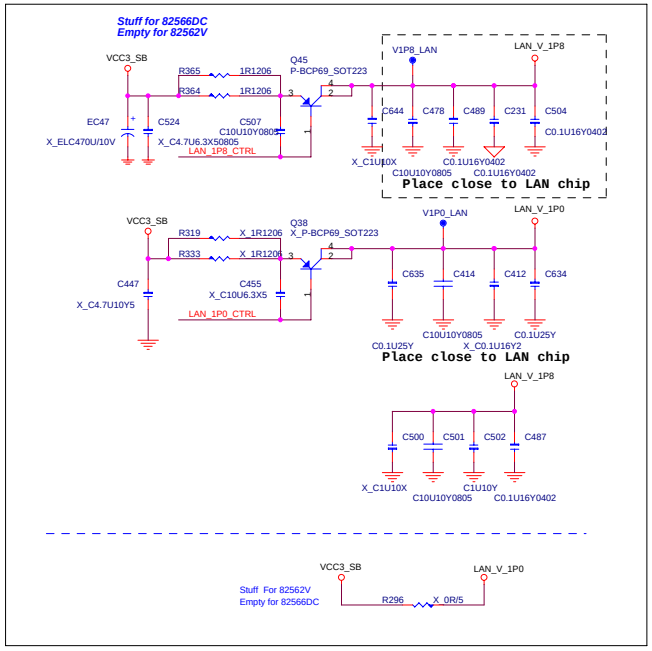


Intel 82556DC
For consumer desktop PC.Support Digital Home capabilities,WoL,PXE.
Intel 82562V
Basic 10/100 Ethernet connection.

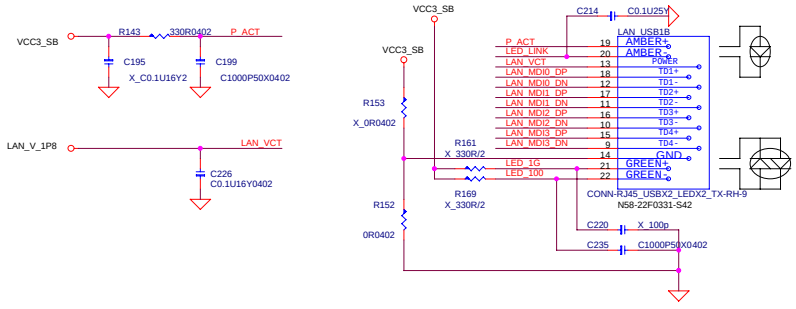
B06-8256615-I06
,CHIP LAN,INTEL/82566DC,,BGA-81pin,NINEVEH GIGA LAN CHIP(PHY),RoHS COMPLIANCE

B06-8256205-I06
,CHIP LAN,INTEL/82562V,,BGA-81pin,NINEVEH GIGA LAN CHIP(PHY),RoHS COMPLIANCE





LAN CONNECTOR



Speed LED Type
1000Mbps : Orange
100Mbps : Green
10Mbps : LED off
YELLOW : For Active/Link

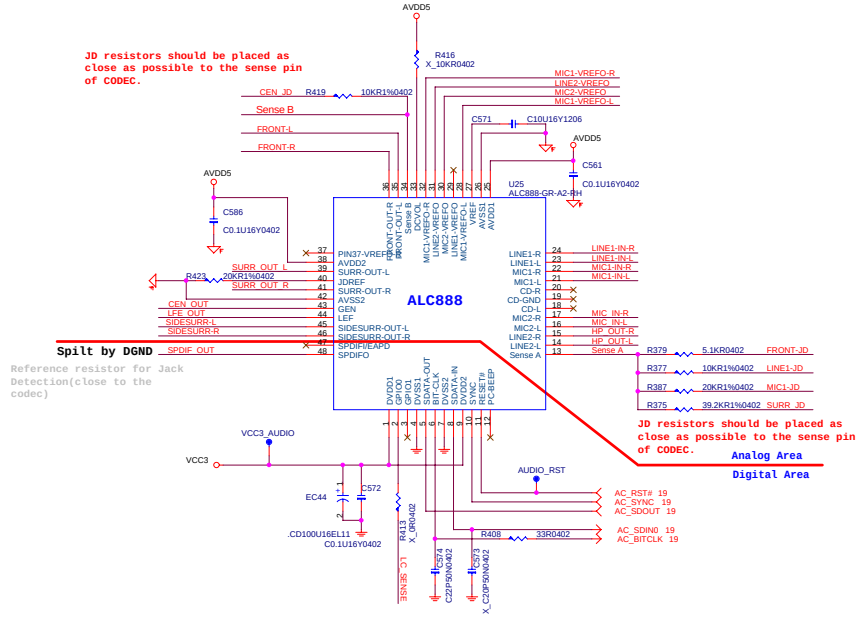
ACT_LED	Link_LED
S0: LOW	S0: LOW
S1/S3/S4/S5: HIGH	S5: HIGH
	S1/S3/S4: WOL EN-->LOW WOL DIS-->HIGH

Default

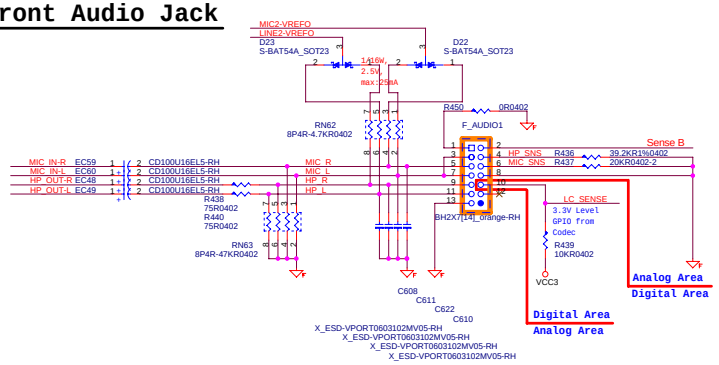
10/100-Lan	Giga-Lan
10/100 (BCM4401) :	GIGA(BCM5788) :
N58-22F0301-S42	N58-22F0331-S42
P25@157-P5P9	P25@153-P5Z9
Link Yellow Active Blinking 100 Green	Link Yellow Active Blinking 1000 Orange 100 Green
19 20 Yellow 21 22 Green	19 20 Yellow 21 Orange 22 Green

MICRO-START INT'L CO.,LTD.	
Title	Intel LAN 82562V&82566DC
Size	Document Number: MS-7363L2 — Rev: 0A
Date: Tuesday, January 30, 2007	Sheet 30 of 36

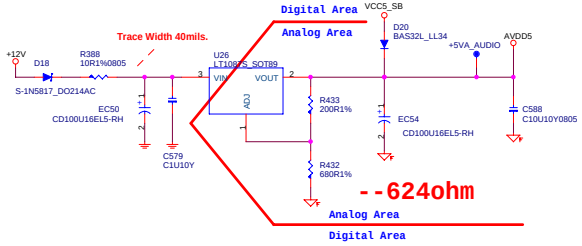
Audio Codec -ALC662/888



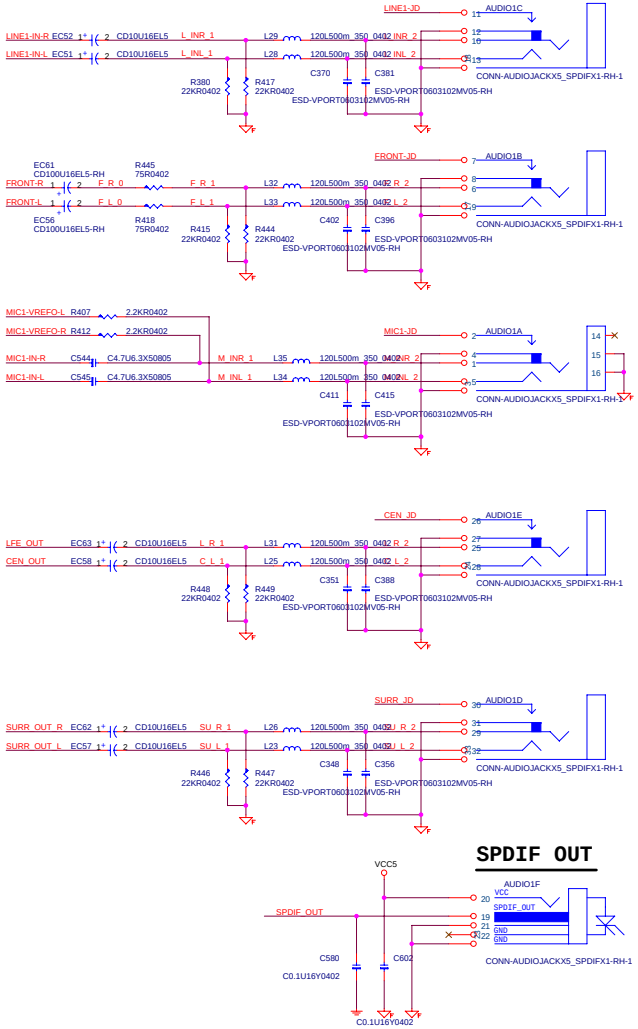
Front Audio Jack



Audio Power

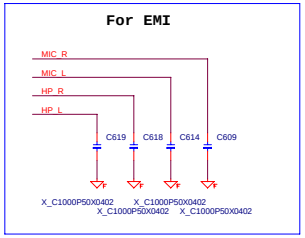


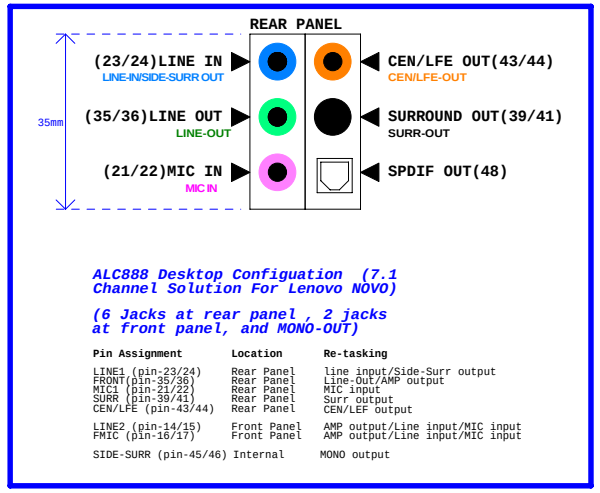
Rear HD Phone Jack_2*3



SPDIF OUT

EMI



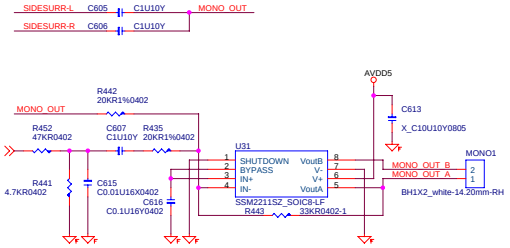


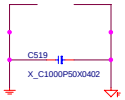
ALC888 Desktop Configuation (7.1 Channel Solution For Lenovo NOVO)

(6 Jacks at rear panel , 2 jacks at front panel, and MONO-OUT)

Pin Assignment	Location	Re-tasking
LINE1 (pin-23/24)	Rear Panel	line input/Side-Surr output
FRONT(pin-35/36)	Rear Panel	Line-Out/AMP output
MIC1 (pin-21/22)	Rear Panel	MIC input
SURR (pin-39/41)	Rear Panel	Surr output
CEN/LFE (pin-43/44)	Rear Panel	CEN/LEF output
LINE2 (pin-14/15)	Front Panel	AMP output/Line input/MIC input
FMIC (pin-16/17)	Front Panel	AMP output/Line input/MIC input
SIDE-SURR (pin-45/46)	Internal	MONO output

MONO Amplifier

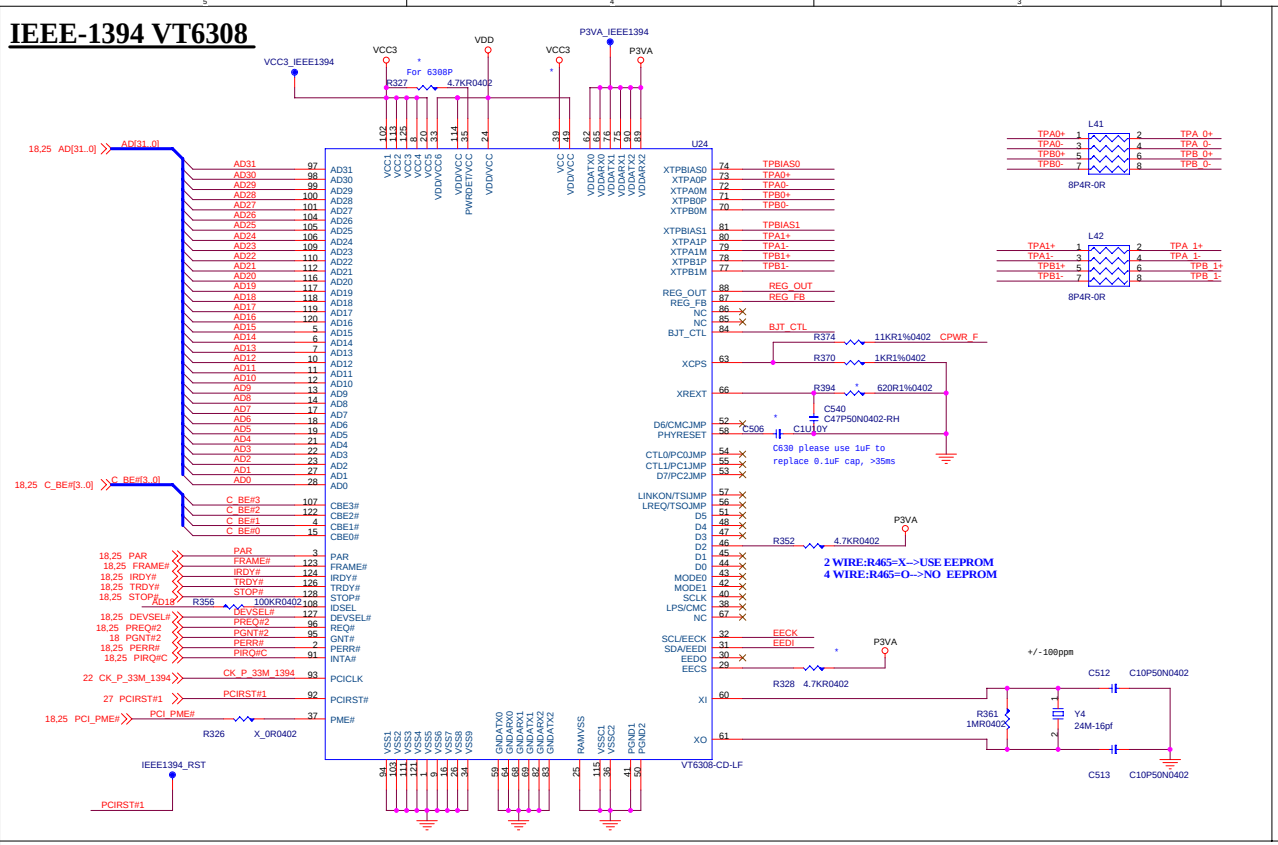


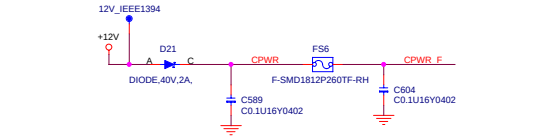


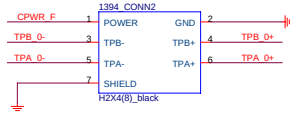
Tied at one point only under the codec or near the codec

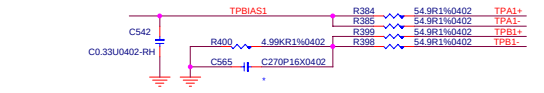
MSI Link to the Future	MICRO-START INT'L CO.,LTD.	
Title	HD Audio -ALC662/888	
Size: Custom	Document Number: MS-7363L2	Rev: 0A
Date: Tuesday, January 30, 2007	Sheet 31 of 36	

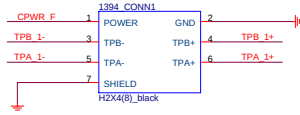
IEEE-1394 VT6308

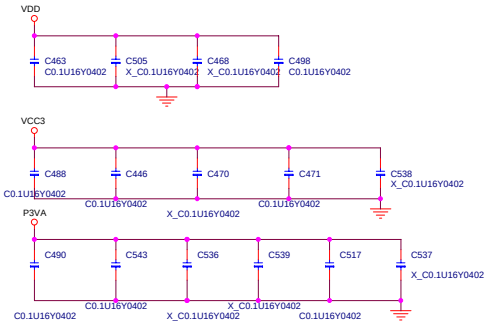


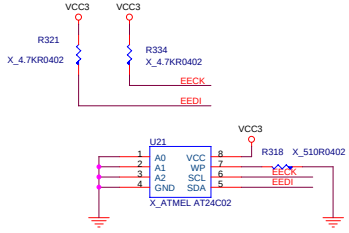


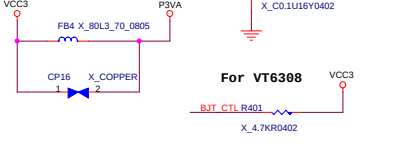


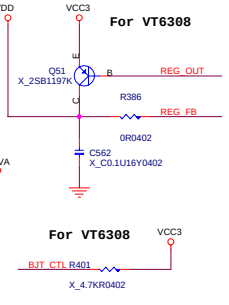






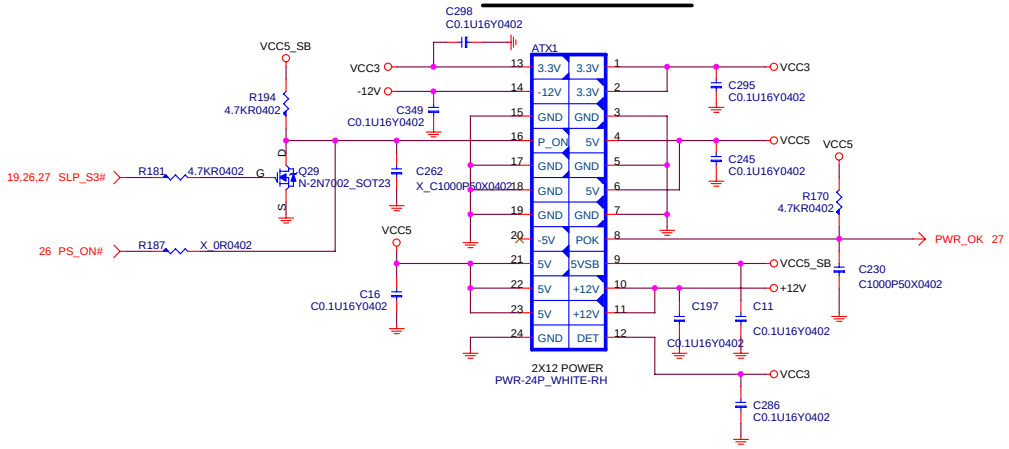




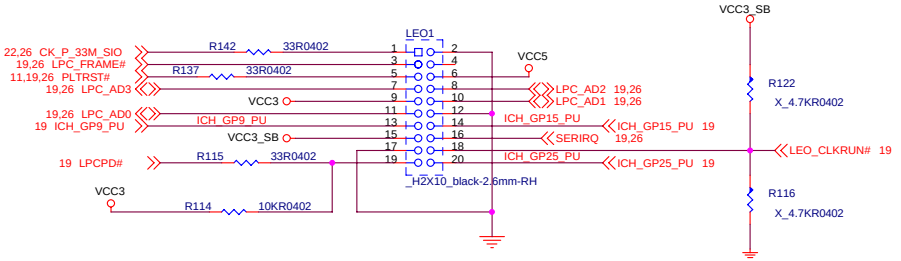


MSI Click to the Future	MICRO-START INT'L CO.,LTD.	
Title: IEEE-1394 VT6308		
Size: C	Document Number: MS-7363L2	Rev: 0A
Date: Tuesday, January 30, 2007	Sheet 32 of 36	

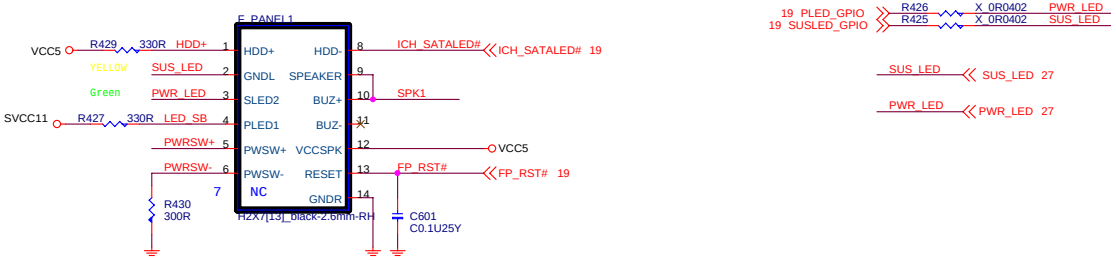
ATX CONNECTOR



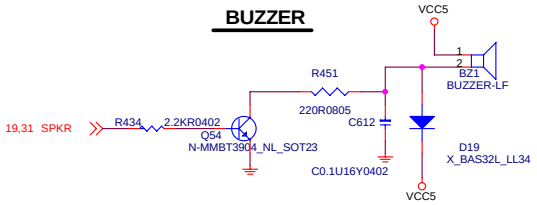
Lenovo LEO Chipset



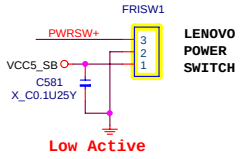
LENOVO Front Panel Connector

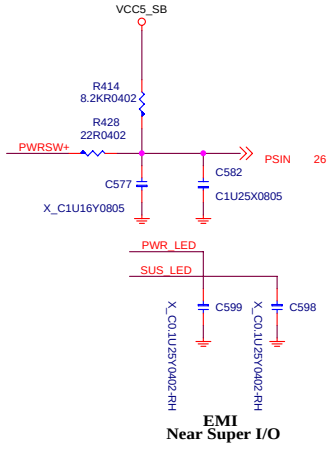


BUZZER



POWER BUTTON



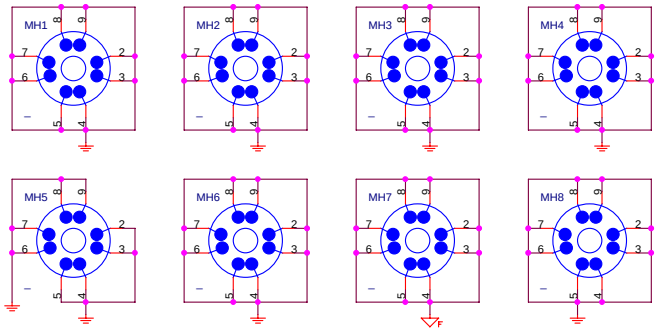


MSI MICRO-START INT'L CO.,LTD.

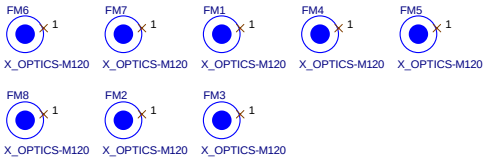
Title: ATX & FRONT PANEL

Size: Custom | Document Number: MS-7363L2 | Rev: 0A

Date: Tuesday, January 30, 2007 | Sheet 33 of 36



Optics Orientation Holes



MSI Link to the Future	MICRO-START INT'L CO.,LTD.		
Title: EMI CAP			
Size: Custom	Document Number: MS-7363L2		Rev: 0A
Date: Tuesday, January 30, 2007	Sheet 34 of 36		

Version 0A

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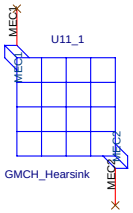
Title: History

Size: Custom | Document Number: MS-7363L2 | Rev: 0A

Date: Tuesday, January 23, 2007 | Sheet 35 of 36

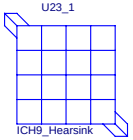
MANUAL PART

HEAT SINK



U11_1

GMCH_Hearsink



U23_1

ICH9_Hearsink

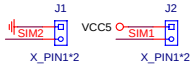
PCB1

P30-073630A-G37

P30-073630A-E48

BAT1_X1
BAT-2P-RH-1

Simulation



LAN

U900

LAN
10/100
82562V

[82562V-RH]

N900

10/100
LAN CONN

CONN-RJ45_USBX2_LEDX2_TX-RH-9

R900

54.9R1%0402

R901

649R1%2

LEGEND SPEC:

F_AUDIO1(1)

_JUMPER-1X2A_green-1

FRONT AUDIO MIC JUMP	
3 -5	MIC

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Title: Manual Part

Size: Custom | Document Number: MS-7363L2 | Rev: 0A

Date: Tuesday, January 30, 2007 | Sheet 36 of 36