MS-7362 Version : 0A

CPU :

Intel Conroe Family and Kentsfield Family Processor
Intel Pentium D Processor 900 and 800 Sequence
Intel Pentium 4 Processor 600 Sequence

System Chipset :

Intel G965 - GMCH (North Bridge)
Intel ICH8 (South Bridge)

On Board Chipset :

Clock Gen. -- ICS9LPRS514
Azalia Codec - ALC883 / ALC888
LAN -- RealTek RTL8111B / RTL8101E
VRM 11 - Intersil 6312 / 6322
ACPI Controller -- MS7 / MS11
IEEE 1394 -- VIA VT6308P
PATA -- Marvell 88SE6111
TPM 1.2 -- Infineon SLB9635TT1.2
Super I/O -- Winbond W83627DHG
SPI Flash 8Mb

Main Memory :

2 Channel DDR II * 4 (Max 8GB)

Expansion Slot :

PCI Express x16 Slot * 1
PCI Express x1 Slot * 1
PCI Slot * 2

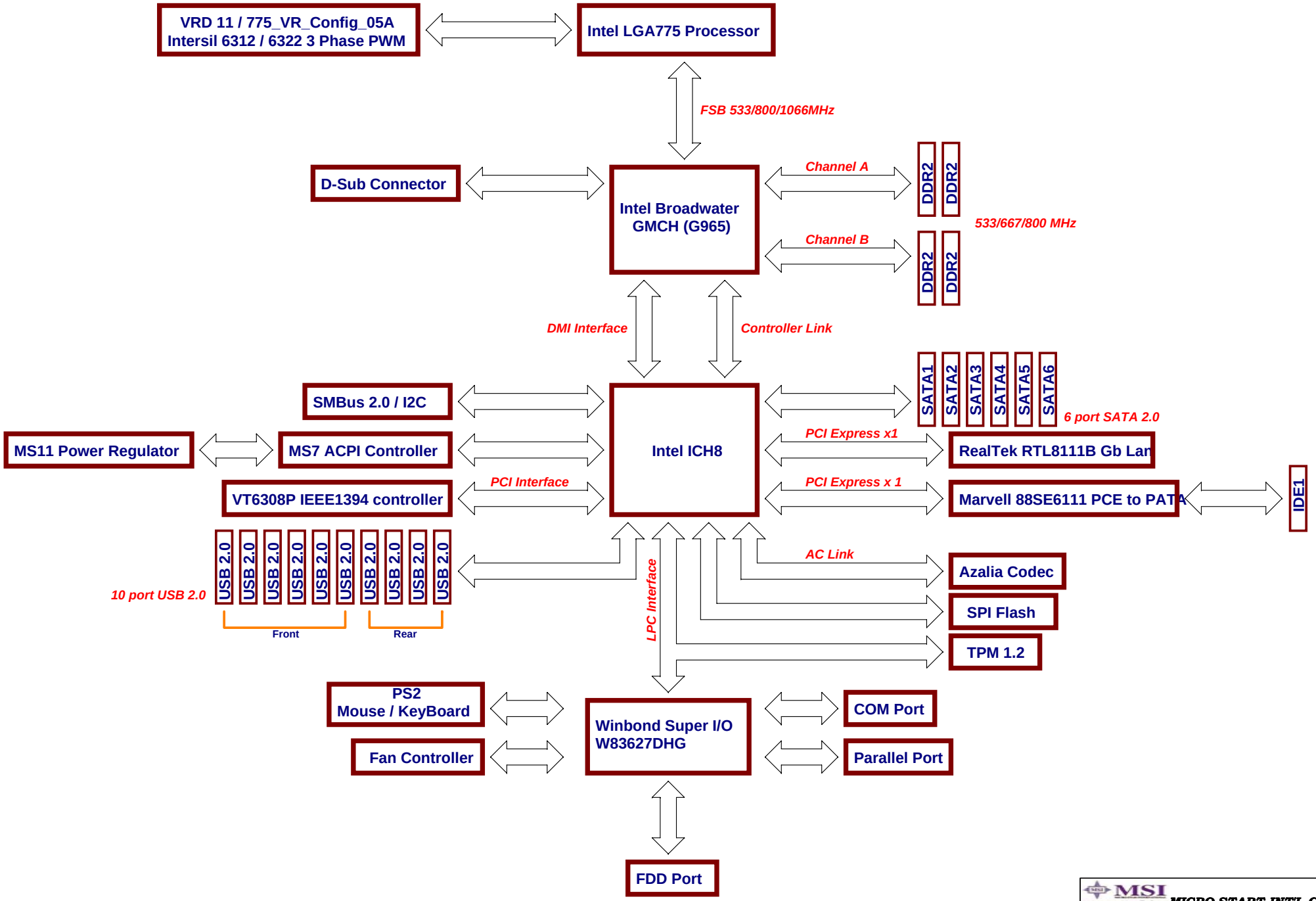
ERP No.	Config Item	PlatForm or Option	Option Select
7362-A10	Cfg-STD	G965 + ICH8 + RTL8111B + ALC888 + VT6308P + 88SE6111 + W83627 DHG	STD

MSI MICRO-START INT'L CO.,LTD.

Title: Cover Sheet

Size | Document Number: MS-7362 | Rev: 0A

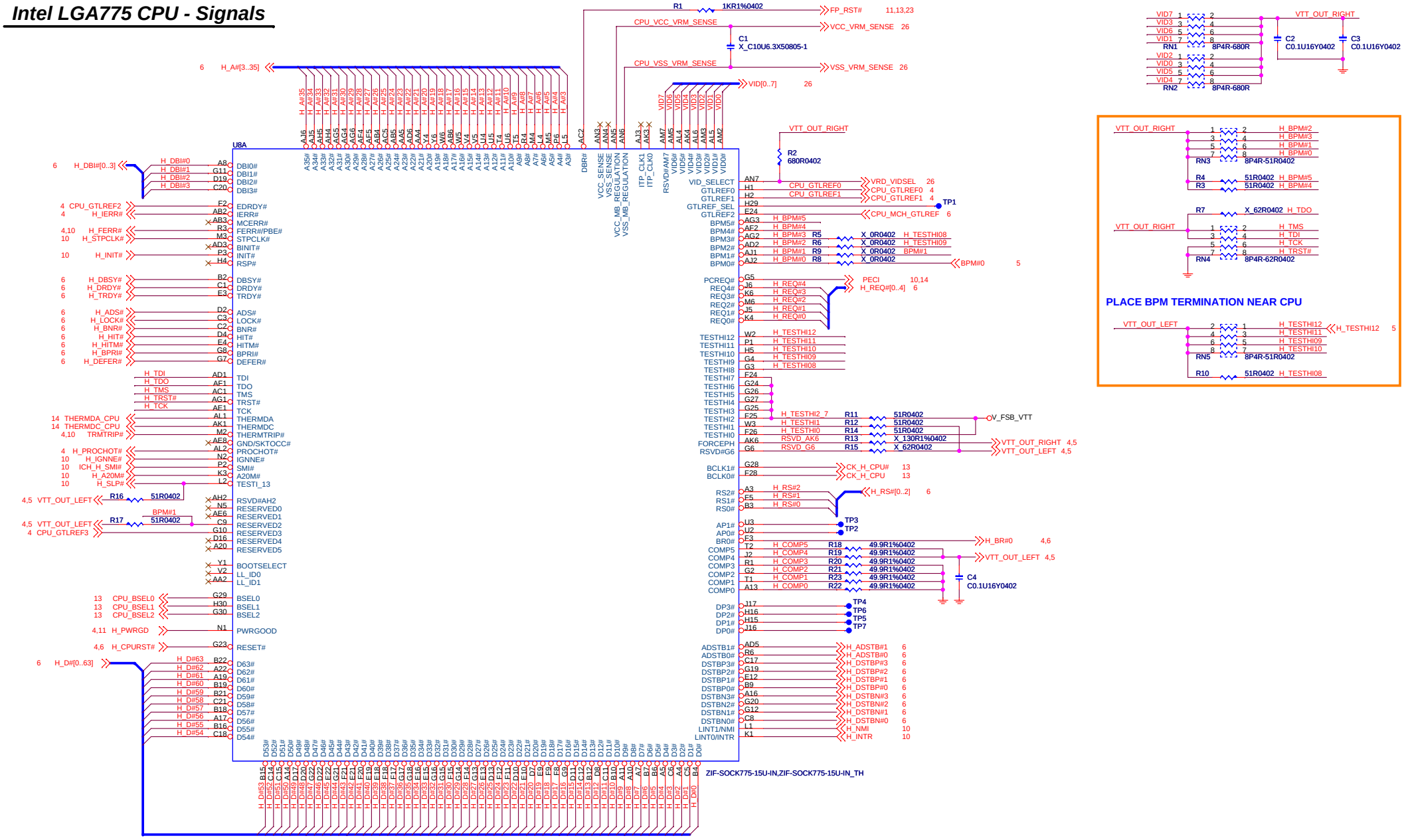
Date: Friday, January 19, 2007 Sheet 1 of 39



MSI Link to the Future MICRO-START INT'L CO.,LTD.

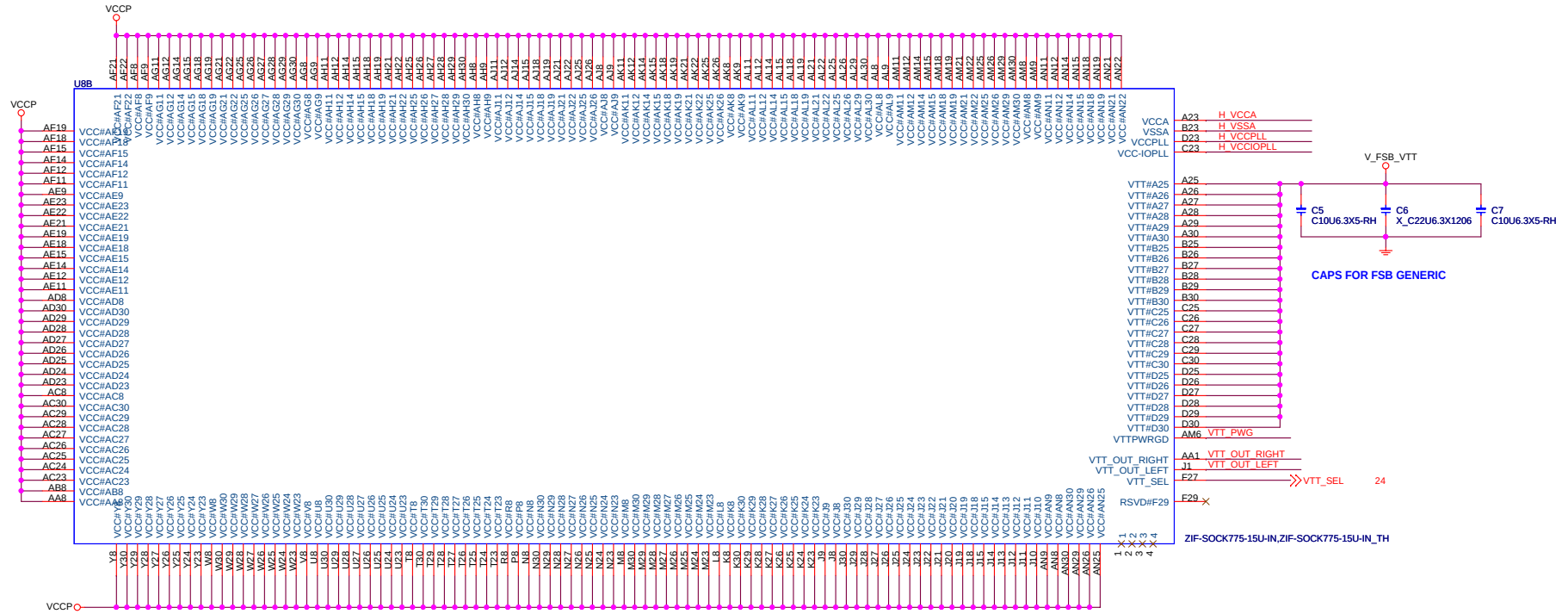
Title: System Block Diagram		
Size	Document Number: MS-7362	Rev: 0A
Date: Friday, January 19, 2007	Sheet 2 of 39	

Intel LGA775 CPU - Signals

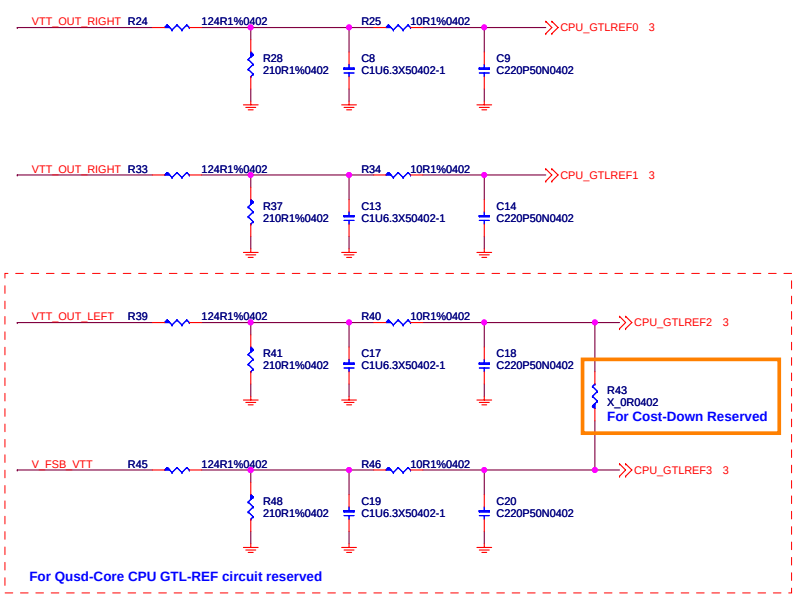


Title	Intel LGA775 CPU - Signals		
Size	Document Number		Rev
	MS-7362		0A
Date:	Friday, January 19, 2007	Sheet 3 of 39	

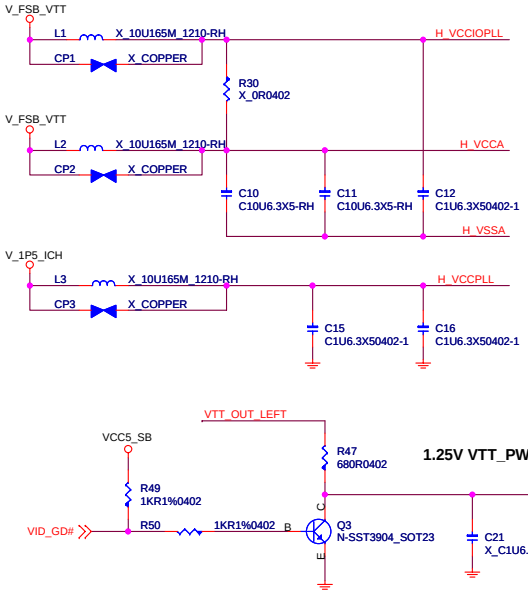
MSI MICRO-STAR INT'L CO.,LTD.



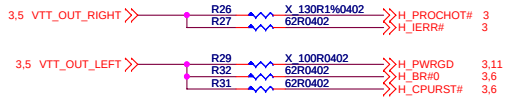
GTLREF Voltage Should Be 0.63 * VTT = 0.756V



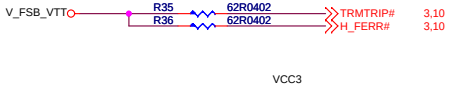
PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET
TRACE WIDTH TO CAPS MUST BE SMALLER THAN 12MILS

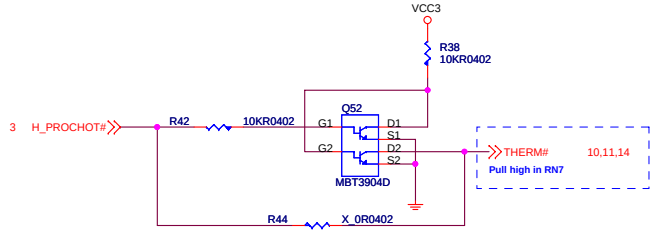


PLACE AT CPU END OF ROUTE



PLACE AT ICH END OF ROUTE



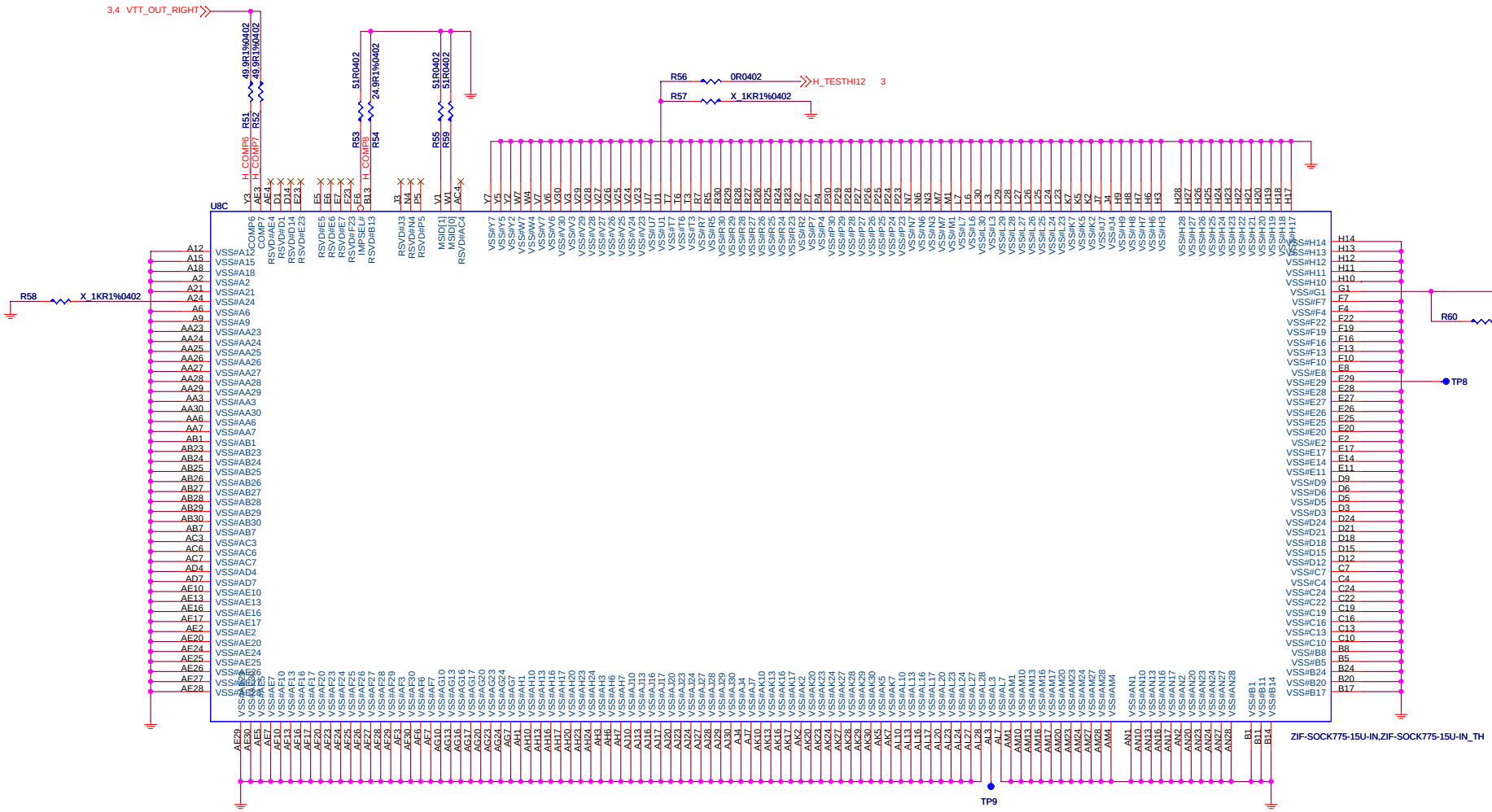


MICRO-START INT'L CO.,LTD.

Title: Intel LGA775 CPU - Power

Size	Document Number	Rev
	MS-7362	0A

Date: Friday, January 19, 2007 Sheet 4 of 39



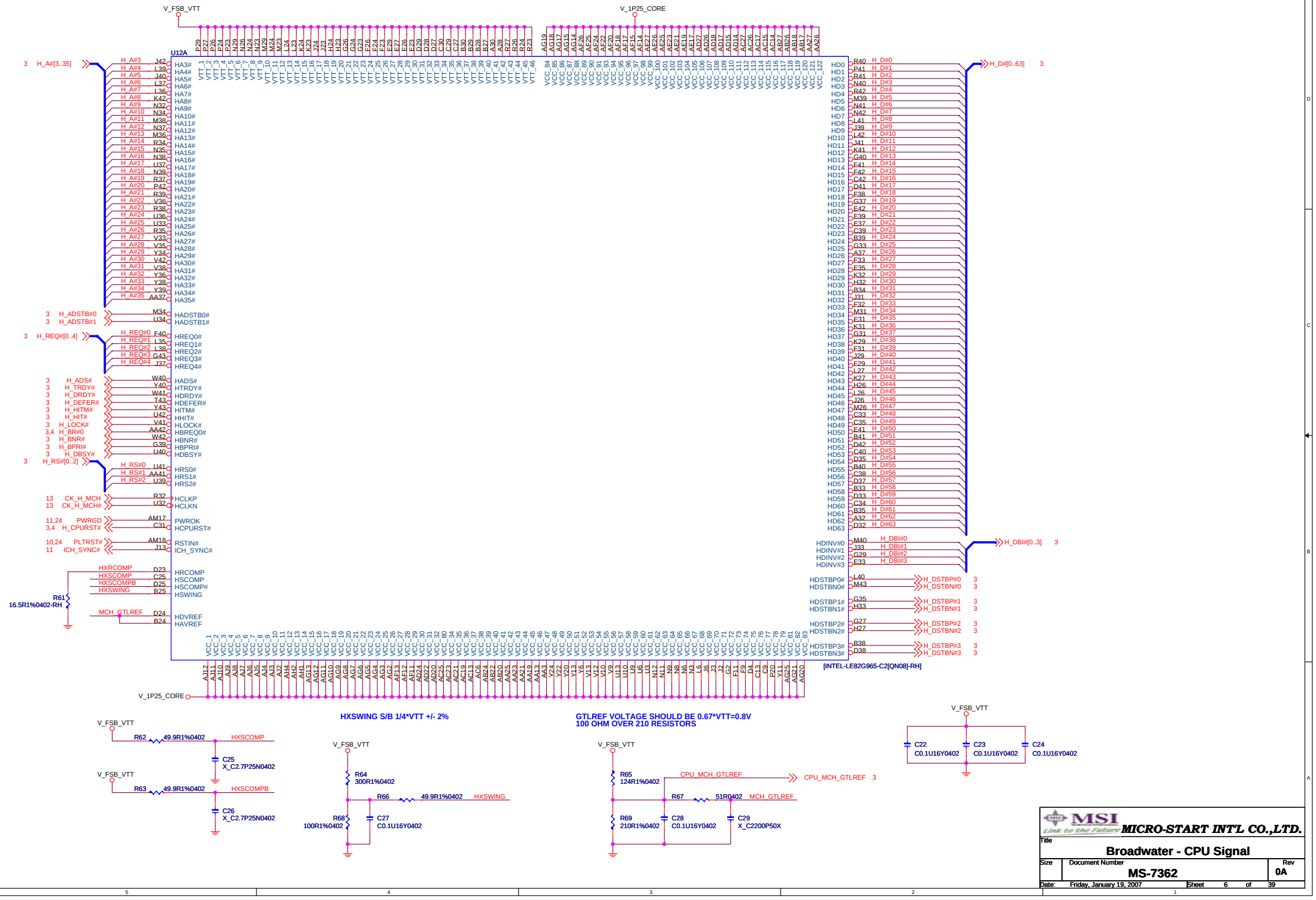
	MSID1	MSID0
2005 Perf FMB	0	0
2005 Value FMB	0	NC
2006 65W FMB	0	NC

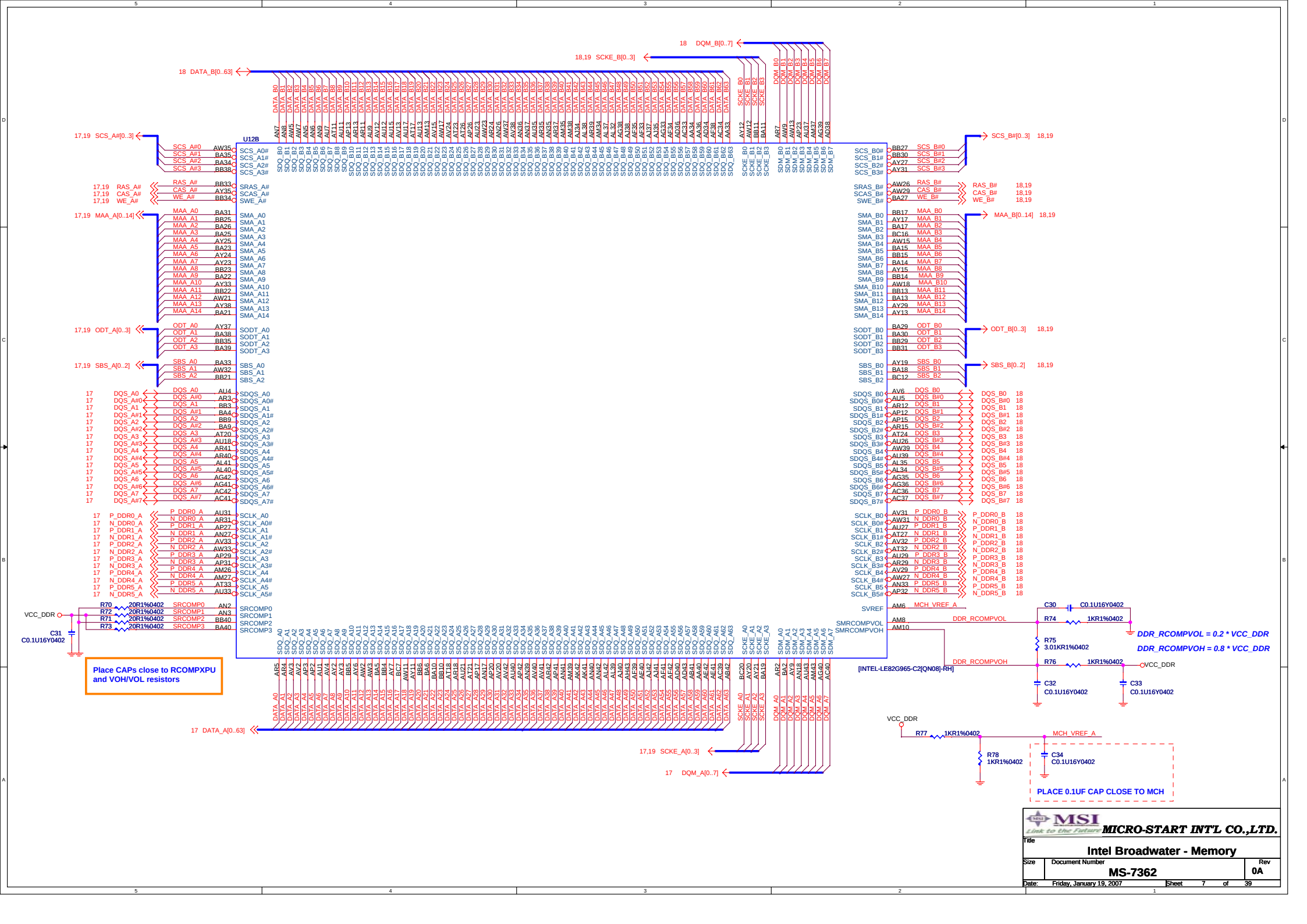
MICRO-START INT'L CO.,LTD.

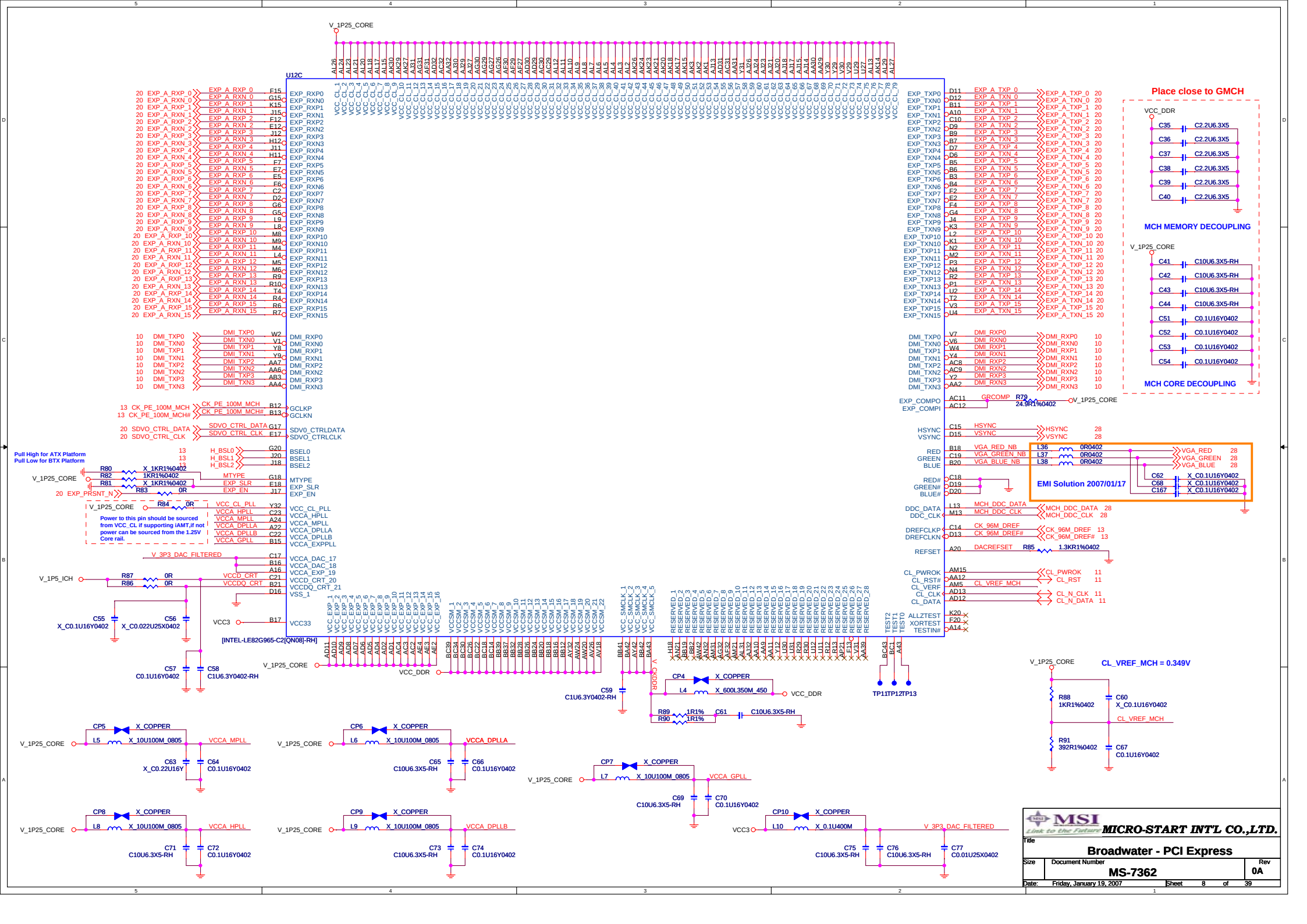
Title: Intel LGA775 CPU - GND

Size | Document Number: MS-7362 | Rev: 0A

Date: Friday, January 19, 2007 Sheet 5 of 39


V_FSB_VTT
V_1P25_CORE
U12A
[INTEL-LE82G965-C2[QN08]-RH]
HXSWING S/B 1/4*VTT +/- 2%
GTLREF VOLTAGE SHOULD BE 0.67*VTT=0.8V
100 OHM OVER 210 RESISTORS
R61 16.5R1%0402-RH
R62 49.9R1%0402 HXSCOMP
R63 49.9R1%0402 HXSCOMPB
C25 X_C2.7P25N0402
C26 X_C2.7P25N0402
R64 300R1%0402
R66 49.9R1%0402 HXSWING
R68 100R1%0402
C27 C0.1U16Y0402
R65 124R1%0402
CPU_MCH_GTLREF
R67 51R0402 MCH_GTLREF
R69 210R1%0402
C28 C0.1U16Y0402
C29 X_C2200P50X
C22 C0.1U16Y0402
C23 C0.1U16Y0402
C24 C0.1U16Y0402
MICRO-START INT'L CO.,LTD.
Broadwater - CPU Signal
MS-7362
0A
Friday, January 19, 2007
Sheet 6 of 39


U12B
18 DQM_B[0..7]
18,19 SCKE_B[0..3]
18 DATA_B[0..63]
17,19 SCS_A#[0..3]
17,19 RAS_A#
17,19 CAS_A#
17,19 WE_A#
17,19 MAA_A[0..14]
17,19 ODT_A[0..3]
17,19 SBS_A[0..2]
17 DQS_A0
17 DQS_A#0
17 DQS_A1
17 DQS_A#1
17 DQS_A2
17 DQS_A#2
17 DQS_A3
17 DQS_A#3
17 DQS_A4
17 DQS_A#4
17 DQS_A5
17 DQS_A#5
17 DQS_A6
17 DQS_A#6
17 DQS_A7
17 DQS_A#7
17 P_DDR0_A
17 N_DDR0_A
17 P_DDR1_A
17 N_DDR1_A
17 P_DDR2_A
17 N_DDR2_A
17 P_DDR3_A
17 N_DDR3_A
17 P_DDR4_A
17 N_DDR4_A
17 P_DDR5_A
17 N_DDR5_A
VCC_DDR
R70 20R1%0402 SRCOMP0
R72 20R1%0402 SRCOMP1
R71 20R1%0402 SRCOMP2
R73 20R1%0402 SRCOMP3
C31 C0.1U16Y0402
Place CAPs close to RCOMPXPU and VOH/VOL resistors
17 DATA_A[0..63]
17,19 SCKE_A[0..3]
17 DQM_A[0..7]
SCS_B#[0..3] 18,19
RAS_B# 18,19
CAS_B# 18,19
WE_B# 18,19
MAA_B[0..14] 18,19
ODT_B[0..3] 18,19
SBS_B[0..2] 18,19
DQS_B0 18
DQS_B#0 18
DQS_B1 18
DQS_B#1 18
DQS_B2 18
DQS_B#2 18
DQS_B3 18
DQS_B#3 18
DQS_B4 18
DQS_B#4 18
DQS_B5 18
DQS_B#5 18
DQS_B6 18
DQS_B#6 18
DQS_B7 18
DQS_B#7 18
P_DDR0_B 18
N_DDR0_B 18
P_DDR1_B 18
N_DDR1_B 18
P_DDR2_B 18
N_DDR2_B 18
P_DDR3_B 18
N_DDR3_B 18
P_DDR4_B 18
N_DDR4_B 18
P_DDR5_B 18
N_DDR5_B 18
SVREF
MCH_VREF_A
SMRCOMPVOL
SMRCOMPVOH
DDR_RCOMPVOL
DDR_RCOMPVOH
[INTEL-LE82G965-C2[QN08]-RH]
C30 C0.1U16Y0402
R74 1KR1%0402
DDR_RCOMPVOL = 0.2 * VCC_DDR
R75 3.01KR1%0402
DDR_RCOMPVOH = 0.8 * VCC_DDR
R76 1KR1%0402
VCC_DDR
C32 C0.1U16Y0402
C33 C0.1U16Y0402
R77 1KR1%0402
MCH_VREF_A
R78 1KR1%0402
C34 C0.1U16Y0402
PLACE 0.1UF CAP CLOSE TO MCH
MSI
MICRO-START INT'L CO.,LTD.
Title
Intel Broadwater - Memory
Size
Document Number
MS-7362
Rev
0A
Date: Friday, January 19, 2007
Sheet 7 of 39


U12C
[INTEL-LE82G965-C2[QN08]-RH]
V_1P25_CORE
VCC_DDR
V_3P3_DAC_FILTERED
V_1P5_ICH
V_1P25_CORE
Place close to GMCH
MCH MEMORY DECOUPLING
MCH CORE DECOUPLING
EMI Solution 2007/01/17
Pull High for ATX Platform
Pull Low for BTX Platform
Power to this pin should be sourced from VCC_CL if supporting iAMT,if not power can be sourced from the 1.25V Core rail.
CL_VREF_MCH = 0.349V
MICRO-START INT'L CO.,LTD.
Broadwater - PCI Express
MS-7362
0A
Friday, January 19, 2007
Sheet 8 of 39

MICRO-START INT'L CO.,LTD.

Title: Broadwater - GND

Size: | Document Number: MS-7362 | Rev: 0A

Date: Friday, January 19, 2007 | Sheet 9 of 39

ICH 8 PART 1/3

ICH8 H/W STRAPS

SIGNAL	H	L	DES.
SPKR	DIS	EN	REBOOT
GNT3	DIS	EN	A16 OVERIDE
INTVRMEN/LAN100_SLP	EN	DIS	INTERNAL_VRM VCCSUS1_05,1_5, VCCCL1_5 VCCLAN1_05,VCC, VCCCL1_05)
SATALED	NORM	REVERSE	PCIE 0-3 ORDER
HDA_SDOUT	DFX/PCIE	N/A	XOR MODE/PCIE PORT CONFIG BIT 1
HDA_SYNC	SET BIT	N/A	PCIE PORT CONFIG BIT 0 (1-4)
GNT2	N/A	SET BIT	PCIE PORT CONFIG 2 BIT 0 (5-6)

PGNT#2 R95 X_1KR1%0402

PGNT#3 R96 X_1KR1%0402 VCC3_SB

11 ACSDOUT R98 X_1KR1%0402 VCC3

11 ACSYNC R97 X_1KR1%0402

11,23 SPKR R99 X_1KR1%0402

VCC3_SB

R100 1KR1%0402 R101 1KR1%0402

PGNT#0 SPI_CS1#

R102 1KR1%0402 R103 1KR1%0402

BOOT SELECT STRAPS		
BOOT DEVICE	PGNT#0	SPI_CS1#
FWH	1	1
SPI	0	X
PCI	1	0

VCC3 RN6 8P4R-10KR0402

SERIRQ A20GATE KBRST# THERM# THERM# 4,11,14

SPI Debug Port

VCC3_SB VCC3_SB JSPI1

SPI_MISO SPI_MOSI_F

SPI_CS0_F# SPI_CLK_F

11 SPI_HOLD# From SB GPIO33

Reserved for BIOS control used

R107 X_0R0402 HOLD#

H2X5[1]_BLACK-RH

SPI FLASH

VCC3_SB R113 1KR1%0402 U25

SPI_CS0_F# SPI_MISO R114 15R0402

11 SPI_WP# From SB GPIO32

CE# VDD SO HOLD# WP# SCK VSS SI

MX25L8005M2C-15G-RH

HOLD# R115 1KR1%0402 SPI_CLK_F SPI_MOSI_F

VCC3_SB C85 C0.1U16Y0402 C86 C0.1U16Y0402

Please Close to SB

PCI INTERFACE

INTERRUPT SPI

CPU

PCI EXPRESS

DIRECT MEDIA

LAN

U24A

29,31 AD[31..0] AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31

29,31 C_BE#[3..0] C_BE#0 C_BE#1 C_BE#2 C_BE#3

29,31 DEVSEL# 29,31 FRAME# 29,31 IRDY# 29,31 TRDY# 29,31 STOP# 29,31 PAR 31 LOCK# 31 SERR# 29,31 PERR# 29,31 PME#

13 ICH_PCLK 24 PCIRST_ICH8# R104 10R1%0402

31 PREQ#0 31 PREQ#1 31 PREQ#2 29,31 PREQ#3

31 PGNT#0 31 PGNT#1 31 PGNT#2 29,31 PGNT#3

31 PIRQ#A 31 PIRQ#B 31 PIRQ#C 31 PIRQ#D 29,31 PIRQ#E 31 PIRQ#F 31 PIRQ#G 31 PIRQ#H

14,27 SERIRQ

SPI_MOSI_F R109 15R0402 SPI_MOSI

SPI_CS0_F# R110 15R0402 SPI_CS0#

SPI_CLK_F R112 15R0402 SPI_CLK

SPI_CS1#

VCC3_SB RN7 SPI_CS1# SPI_MISO SPI_MOSI SPI_CS0#

X_8P4R-10KR0402

Reserve

A20M# CPUSLP# FERR# IGNNE# INIT# INIT3_3V# INTR NMI SMI# STPCLK# RCIN# A20GATE THRMTRIP# PECI

H_A20M# H_SLP# H_FERR# H_IGNNE# H_INIT# TP10 H_INTR H_NMI ICH_H_SMI# H_STPCLK# KBRST# A20GATE TRMTRIP# PECI_SIO PECI

R92 X_0R0402 R93 0R0402

CPU SB For SIO 83627EHG Ver:H Add R622 ; Del R621

CPU SIO SB For SIO 83627DHG Add R621 ; Del R622

PLTRST# PLTRST_L R94 10R1%0402 PLTRST#

PERN_1 PERP_1 PETN_1 PETP_1 PE_RXN1 PE_RXP1 PE_TXN1_C C78 C0.1U16Y0402 PE_TXP1_C C79 C0.1U16Y0402 PE_TXN1 PE_TXP1

For PCIE x1 slot

PERN_2 PERP_2 PETN_2 PETP_2 PE_RXN2 PE_RXP2 PE_TXN2_C C80 C0.1U16Y0402 PE_TXP2_C C81 C0.1U16Y0402 PE_TXN2 PE_TXP2

For Marvell 88SE6111 PCIE to PATA

PERN_3 PERP_3 PETN_3 PETP_3

PERN_4 PERP_4 PETN_4 PETP_4

PERN_5 PERP_5 PETN_5 PETP_5

PERN_6/GLAN_RXN PERP_6/GLAN_RXP PETN_6/GLAN_TXN PETP_6/GLAN_TXP GLAN_RXN GLAN_RXP GLAN_TXN_C C82 C0.1U16Y0402 GLAN_TXP_C C83 C0.1U16Y0402 GLAN_RXN GLAN_RXP GLAN_TXN GLAN_TXP

For RealTek RTL8111B PCIE Gb Lan

DMI_0RXN DMI_0RXP DMI_0TXN DMI_0TXP DMI_RXN0 DMI_RXP0 DMI_TXN0 DMI_TXP0

DMI_1RXN DMI_1RXP DMI_1TXN DMI_1TXP DMI_RXN1 DMI_RXP1 DMI_TXN1 DMI_TXP1

DMI_2RXN DMI_2RXP DMI_2TXN DMI_2TXP DMI_RXN2 DMI_RXP2 DMI_TXN2 DMI_TXP2

DMI_3RXN DMI_3RXP DMI_3TXN DMI_3TXP DMI_RXN3 DMI_RXP3 DMI_TXN3 DMI_TXP3

DMI_CLKN DMI_CLKP R25 R24 CK_PE_100M_ICH# 13 CK_PE_100M_ICH 13

DMICOMPI AD27 DMI_BIAS R105 24.9R1%0402 V_1P5_ICH

DMI_IRCOMP AD28 <200mils

GLAN_CLK LAN_RSTSYNC LAN_RST# LAN_RXD0 LAN_RXD1 LAN_RXD2 LAN_TXD0 LAN_TXD1 LAN_TXD2

LAN_RST# X_10KR0402 R106 VCC3_SB

X_0R0402 R108 RSMRST# 11,24

R111 0R0402 C84 X_C0.1U16Y0402

LAN_RST# Options

Not Support Intel : Pull Low

Support Intel Lan and not Support WOL : Connect to RSMRST#

Support Intel Lan and WOL : Connect to PWROK#

VSS_001 VSS_002 VSS_003 VSS_004 VSS_005 VSS_006 VSS_007 VSS_008 VSS_009 VSS_010 VSS_011 VSS_012 VSS_013 VSS_014 VSS_015 VSS_016 VSS_017 VSS_018 VSS_019 VSS_020 VSS_021 VSS_022 VSS_023 VSS_024 VSS_025 VSS_026 VSS_027 VSS_028 VSS_029 VSS_030 VSS_031 VSS_032 VSS_033 VSS_034 VSS_035 VSS_036 VSS_037 VSS_038 VSS_039 VSS_040

A5 A24 A28 B2 B8 B11 B14 B17 B20 B24 C22 C27 C28 C3 D4 D6 D12 D16 D19 D22 D25 E9 E21 E24 E27 E28 F2 F7 F15 F22 F24 F25 F26 G1 G4 G6 G10 G13 G18

[INTEL-NH82801HH-B1[QM36]-RH]

MSI Link to the Future	MICRO-START INT'L CO.,LTD.		
Title	ICH8 - CPU/DMI/PCIE/LAN/SPI		
Size	Document Number MS-7362		Rev 0A
Date: Friday, January 19, 2007	Sheet 10 of 39		

ICH 8 PART 2/3

BATTERY

CMOS CLEAR	NORMAL	CLEAR
JBAT1	(1-2)	(2-3)

VCC3_SB, JBAT_JP1, JUMPER-1X2A_green-RH-1, VBAT, D1 S-BAT54C_SOT23, VBAT_DZ, R118 1KR1%0402, BAT1, BAT1 BAT-2P-RH-1, JBAT1, H1X3_black-LF, R116 20KR1%0402, RTC_RST#, R119 100R0402, C89 C1U6.3X50402-1, C90 C1U6.3X50402-1

Close to Pin AA2 of ICH6.

ICH8 PULL-UP RESISTORS

ALL COMPONENTS CLOSE TO ICH8

Trace length is less than 3inchs to ICH8.

GPIO_14, SMB_ALERT#, BATLOW#, GPIO_12, RN8 8P4R-10KR0402, LPC_PME#, RI#, GPIO_13, RN10 8P4R-10KR0402, GPIO_10, LINK_ALERT#, SM_LINK0, SM_LINK1, RN11 8P4R-10KR0402, SATA0GP, GPIO_39, GPIO_7, RN12 8P4R-10KR0402 — VCC3_SB / VCC3

SMBCLK_MAIN R124 X_4.7KR0402, SMBDATA_MAIN R123 X_4.7KR0402, GPIO_0 R126 1KR1%0402, CL_PWROK R125 X_4.7KR0402, LDRQ_1# R235 10KR0402, INTVRMEN R127 390KR0402, LAN100_SLP R129 390KR0402, INTRUDER# R128 1MR0402 — VCC3

PWRGD R131 X_10KR0402, CL_VREF1 R132 X_1KR1%0402 — VBAT

FP_RST# R133 8.2KR0402, WAKE# R135 1KR1%0402, CLEAR_PASSWORD R134 1KR1%0402, LPC_PD# R179 10KR0402 — VCC3_SB

VCC3 R136 10KR0402, 24,26 VRM_GD R137 0R0402 VRM_PWRGD, R139 100KR0402

SM_LINK0 R140 0R0402 SMBCLK_MAIN, SM_LINK1 R142 0R0402 SMBDATA_MAIN

WOL 10KR0402 R143 VCC3_SB, 100KR0402 R144

Unused SATAxGP pins must be terminated using 8.2k ohm to 10k ohm pull-up resistors to VCC3.(For device hot swap)

GPIO_6, SATA1GP, GPIO_22, GPIO_48, RN9 8P4R-10KR0402, SATA4GP R122 10KR0402, SATA5GP R121 10KR0402 — VCC3

SATA3GP, GPIO_38, SATA2GP, SATALED#, RN13 8P4R-10KR0402

Enable internal 2.5V VRM

RTCX1, RTCX2, R138 10MR, C93 C10P50N, Y1 32.768KHZ12.5P_D-RH, C94 C10P50N

CL_VREF_ICH = 0.405V

VCC3_SB, R159 3.24KR1%0402, CL_VREF_ICH, R161 453R1%, C98 C0.01U25X0402

Open Drain Ouput

ICH_FAN_PWM0 R163 X_10KR0402, ICH_FAN_PWM1 R162 X_10KR0402 — VCC5

AC_BITCLK, AC_RST#, AC_SDOUT, AC_SYNC, AC_SDIN0 — R152–R156 33R0402 — AC_BITCLK_ICH, ACRST#, ACSDOUT, ACSYNC, ACSDIN0

C95 X_C20P50N0402, C96 X_C10P50N0402

Please close to SB

U24B

LPC

LPC_AD0 F6 LAD0, LPC_AD1 F5 LAD1, LPC_AD2 G9 LAD2, LPC_AD3 E5 LAD3, LPC_DRQ#0 G8 LDRQ_0#, LDRQ_1# C3 LDRQ_1#/GPIO23, LPC_FRAME# B3 LFRAME#

AC-LINK

AC_BITCLK_ICH AE12 ACZ_BCLK, ACRST# AE13 ACZ_RST#, ACSDIN0 AE13 ACZ_SDIN_0, AC14 ACZ_SDIN_1, AH12 ACZ_SDIN_2, AD13 ACZ_SDIN_3, ACSDOUT AH11 ACZ_SDOUT, ACSYNC AH10 ACZ_SYNC

USB

USBP_0N G2, USBP_0P G3, USBP_1N H5, USBP_1P H4, USBP_2N H1, USBP_2P H2, USBP_3N J3, USBP_3P J2, USBP_4N K5, USBP_4P K4, USBP_5N K1, USBP_5P K2, USBP_6N L3, USBP_6P L2, USBP_7N M5, USBP_7P M4, USBP_8N M2, USBP_8P M1, USBP_9N N2, USBP_9P N3

OC#0 AE15 OC0#, OC#1 AG13 OC1#/GPIO40, OC#2 AG14 OC2#/GPIO41, AG15 OC3#/GPIO42, AH15 OC4#/GPIO43, AE15 OC5#/GPIO29, AG13 OC6#/GPIO30, AF14 OC7#/GPIO31, AD14 OC8#, AG16 OC9#

C0.1U16Y0402 C87, C0.1U16Y0402 C88, C0.1U16Y0402 C91, Please close to ICH8, R117 22.6R1% USB_BIAS, E1 USBRBIASN, E2 USBRBIASP

SM BUS

SMB_CLK_MAIN, SMB_DATA_MAIN — AD19 SMBCLK, AB18 SMBDATA, SMB_ALERT# AF21 SMBALERT#/GPIO11

SM_LINK0 AE19 SMLINK0, SM_LINK1 AG21 SMLINK1, LINK_ALERT# AH21 SMLALERT#

POWER MGNT

RSMRST# AD22, PWRBTN# A1, PWROK AE24, VRM_PWRGD AC16 VRMPWRGD_VGATE, H_PWRGD AE25 CPUPWRGD/GPIO49, CK_PWRGD F1, FP_RST# AF16 SYS_RESET#

SLP_S3# AD22, SLP_S4# AH23, SLP_S5# AC17, SLP_M# AG22, LAN100_SLP AG24, LPC_PD# G7 SUS_STAT#/LPCPD#, SUSCLK E4

MISC

INTRUDER# AF24, WAKE# AH18, RI# AG17, THRM# AH9, BATLOW# AE22, ICH_SYNC# AE10 MCH_SYNC#, SPKR AF6

R145 0R, R148 X_10KR0402

DPRSTP# AE25, DPSLP# AD24, DFXTESTB AD16

ICH_14M AG6 CLK14, USB_48 B1 CLK48

VCC5_SB, R158 4.7KR0402, RSMRST#, R160 10KR0402, C97 X_C1U6.3X50402-1

S-ATA

SATA_0RXN AC5 SATA_RX#0 22, SATA_0RXP AC4 SATA_RX0 22, SATA_0TXN AF4 SATA_TX#0 22, SATA_0TXP AE3 SATA_TX0 22

SATA_1RXN AF1 SATA_RX#1 22, SATA_1RXP AF2 SATA_RX1 22, SATA_1TXN AH2 SATA_TX#1 22, SATA_1TXP AH1 SATA_TX1 22

SATA_2RXN W5 SATA_RX#2 22, SATA_2RXP W4 SATA_RX2 22, SATA_2TXN AA3 SATA_TX#2 22, SATA_2TXP AA4 SATA_TX2 22

SATA_3RXN AB1 SATA_RX#3 22, SATA_3RXP AB2 SATA_RX3 22, SATA_3TXN AD2 SATA_TX#3 22, SATA_3TXP AD1 SATA_TX3 22

SATA_4RXN Y1 SATA_RX#4 22, SATA_4RXP Y2 SATA_RX4 22, SATA_4TXN U3 SATA_TX#4 22, SATA_4TXP U4 SATA_TX4 22

SATA_5RXN T1 SATA_RX#5 22, SATA_5RXP T2 SATA_RX5 22, SATA_5TXN V2 SATA_TX#5 22, SATA_5TXP V1 SATA_TX5 22

SATA_CLKN AG3 CK_ICHSATA# 13, SATA_CLKP AG4 CK_ICHSATA 13

SATARBIASN R2, SATABIASP R1, SATALED# AB10 SATALED# 23

R2 SATA_BIAS R120 24.9R1%0402

SATA0GP/GPIO21 AB11 SATA0GP, SATA1GP/GPIO19 AD8 SATA1GP, SATA2GP/GPIO36 AF8 SATA2GP, SATA3GP/GPIO37 AD9 SATA3GP, SATA4GP AD10 SATA4GP, SATA5GP AE9 SATA5GP

GPIO

BMBUSY#/PMSYNC#/GPIO0 AF9 GPIO_0, GPIO8 AE16 WOL — LPC_PME# 14, GLGP1O3/GPIO9 AG18 GPIO_10, GLGPIO1/GPIO10 AF20 GPIO_12, GP12 AC19 GPIO_13, GPIO13 AE18 GPIO_14, CLGPIO2/GPIO14 AH24

GPIO15 AE21, GPIO16 AE11, GPIO18 AC11, GPIO20 AG8, CLGPIO0/GPIO24 AG23 CLEAR_PASSWORD, GPIO25 AH17, S4_STATE#/GPIO26 AH25, QRT_STATE0/GPIO27 AD20, QRT_STATE1/GPIO28 AD15 — SPI_WP# 10, SPI_HOLD# 10, GPIO32 AH7, GPIO33 AG7 — R130 4.7KR0402 — VCC3, GPIO34 AG12, SATACLKREQ#/GPIO35 AD12, SCLOCK/GPIO22 AE7 GPIO_22, SLOAD/GPIO38 AH6 GPIO_39, SDATAOUT0/GPIO39 AC10 GPIO_38, SDATAOUT1/GPIO48 AF7 GPIO_48

RTC

VCCRTC AG26 — C0.1U16Y0402 C92 — VBAT, INTVRMEN AA22 INTVRMEN, RTCRST# AD21 RTC_RST#, RTCX1 AH26 RTCX1, RTCX2 AH27 RTCX2

AMT

GLAN_COMPO C24 < 200mils, GLAN_COMPI D24 R141 24.9R1%0402 V_1P5_ICH, CL_CLK0 F21 CL_N_CLK 8, CL_CLK1 AH20, CL_DATA0 G21 CL_N_DATA 8, CL_DATA1 AE18, CL_VREF0 B21 CL_VREF_ICH, CL_VREF1 AG20 CL_VREF1, CL_PWROK C2 — R147 0R0402 PWRGD, R146 0R0402 CL_PWROK 8, CL_RST# AG19 — CL_RST 8

AFSC

FAN_PWM0 AB6 ICH_FAN_PWM0 R149 X_0R0402 AFSC_CPUFAN_PWM 27, FAN_PWM1 AD6 ICH_FAN_PWM1 R150 X_0R0402 AFSC_SYSFAN_PWM 27, FAN_PWM2 AB8

TACH0/GPIO17 AC7 TACH0 R154 X_0R0402 AFSC_CPUFAN_IN 14,27, TACH1/GPIO1 AF5 TACH1 R157 X_0R0402 AFSC_SYSFAN_IN 14,27, TACH2/GPIO6 AE6 GPIO_6, TACH3/GPIO7 AC8 GPIO_7

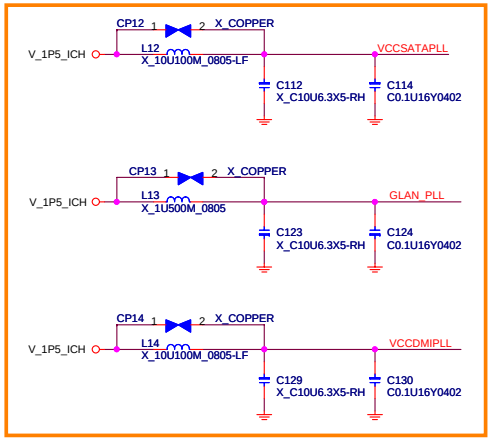
SSTCTL AD17 SSTCTL 14

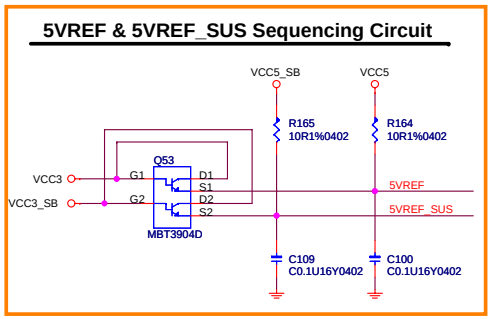
VSS_041 G24, VSS_042 G27, VSS_043 G28, VSS_044 H3, VSS_045 H6, VSS_046 H7, VSS_047 H22, VSS_048 H24, VSS_049 H25, VSS_050 H26, VSS_051 J1, VSS_052 J4, VSS_053 J5, VSS_054 J27, VSS_055 K3, VSS_056 K6, VSS_057 K7, VSS_058 K25, VSS_059 K26, VSS_060 L1, VSS_061 L4, VSS_062 L13, VSS_063 L15, VSS_064 L27, VSS_065 L28, VSS_066 M3, VSS_067 M12, VSS_068 M13, VSS_069 M14, VSS_070 M15, VSS_071 M16, VSS_072 M17, VSS_073 M22, VSS_074 M25, VSS_075 M26, VSS_076 N1, VSS_077 N4, VSS_078 N5, VSS_079 N11, VSS_080 N12, VSS_081 N13, VSS_082 N14, VSS_083 N15, VSS_084, VSS_085

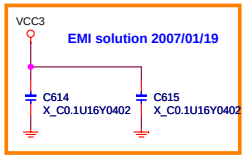
[INTEL-NH82801HH-B1[QM36]-RH]

Title	ICH8 - ACLink/USB/SATA/GPIO
Size	Document Number: MS-7362 — Rev: 0A
Date:	Friday, January 19, 2007 — Sheet 11 of 39

MSI Link to the Future — MICRO-START INT'L CO.,LTD.







ICH 8

PART 3/3

U24C [INTEL-NH82801HH-B1[QM36]-RH]

5VREF A15 V5REF
5VREF_SUS A2 V5REF_SUS
V_1P5_ICH G12 G15 VCC1_5_A
Y22 AB9 AB13 VCC1_5_A
VCC_CL_1_5 A21 VCC_CL_1_5
VCC3_SB AB14 VCCSUSHDA
VCC3 AC13 VCCHDA
C102 C0.1U16Y0402 C103 C10U6.3X5-RH
AB7 AD7 AE12 AE11 VCC3_3
V_1P5_ICH C1 VCCUSBPLL
VCCSATAPLL AH5 VCCSATAPLL
VCCDMIPLL P28 VCCDMIPLL
GLAN_PLL A25 VCCGLANPLL
VCC3_SB F3 VCCSUS3_3
VCC3 G20 F20 VCCCL3_3
C107 C0.1U16Y0402
B26 B25 A27 A26 VCCGLAN1_5
J22 J23 J24 K22 K23 K24 L22 L23 L24 M23 M24 N22 N23 N24 P23 P24 P25 P26 R22 R23 R26 R27 R28 T23 T24 U22 U23 U24 V23 V24 W22 W23 W24 Y23 Y24 Y25 Y26 AA26 AA27 AA28 VCC1_5_B
V_1P5_ICH C609 C0.1U16Y0402
C113 C0.1U16Y0402
C116 C0.1U16Y0402
C118 C0.01U25X0402
C120 X_C10U6.3X5-RH
C152 X_C10U6.3X5-RH
Close to ICH8
V_1P25_CORE
C610 C0.1U16Y0402
C128 X_C10U6.3X5-RH
Close to ICH8
AE27 AE28 VCCDMI
V_1P5_ICH T7 U5 U6 V3 V4 V5 W1 W2 W3 U7 V6 W6 Y6 AA5 AA6 AB3 AB4 AB5 AC1 AC2 AC3 VCC1_5_A
C131 C0.1U16Y0402
C132 C0.1U16Y0402
C133 C0.01U25X0402
C135 X_C10U6.3X5-RH
Close to ICH8
N16 N17 N18 N27 N28 P12 P13 P14 P15 P16 P17 P22 P27 R11 R12 R13 R14 R15 R16 R17 R18 T3 T4 T5 T6 T12 T13 T14 T15 T16 T22 T25 T26 U1 U2 U12 U13 U14 U15 U16 U17 U27 U28 V7 V13 V15 V22 VSS
V26 V25 W27 W26 Y3 Y4 Y5 AA1 AA2 AA23 AB22 AB24 AB25 AB26 AC6 AC9 AC15 AC18 AC21 AC22 AC28 AD3 AD4 AD5 AD11 AD26 AE1 AE2 AE5 AE8 AE14 AE17 AE20 AE23 AE3 AH1 AG1 AG2 AG5 AG11 AG25 AG27 AH3 AH4 AH13 AH16 AH19 AH22 G5 VSS
AH8 AE7 A4 F4 B22 VSS_ICHDET VSSKUMBG VSSAUBG VSSASATABG VSSA3GBG
VCCLAN1_05 F17 G17 C99 X_C0.1U16Y0402
VCC1_5_A D1 V_1P5_ICH
L6 L7 M6 M7 C108 C0.1U16Y0402 C101 C0.1U16Y0402
W7 Y7 AA7 A23 V_1P05_ICH
VCC1_05 B23 C23 D23 E23 F23 G22 G23 H22 L11 L12 L14 L16 L17 L18 M11 M18 P11 P18 T11 T18 U11 U18 V11 V12 V14 V16 V17 V18
C104 C2.2U6.3Y
C105 C2.2U6.3Y
C110 C0.1U16Y0402
C106 C0.1U16Y0402
Please close to ICH8
V_CPU_IO AD25 AE26 V_FSB_VTT
VCC3_3 AF28 P5 A22 VCC3
A6 B4 B15 B18 C8 C10 D14 E10 F11 G14 C111 C1U6.3Y0402-RH C115 C0.1U16Y0402 C117 C0.1U16Y0402 C119 C0.1U16Y0402 C121 C0.1U16Y0402
VCCLAN3_3 F19 G19 VCC3
C122 C0.1U16Y0402
VCCSUS3_3 N6 N7 P1 P2 P3 P6 P7 R3 R4 R5 R6 R7 AB16 AB21 AC20 AD18 AF19 VCC3_SB
C125 C0.1U16Y0402
C127 C0.022U25X0402
C126 C0.022U25X0402
C410 C0.1U16Y0402
C412 C0.1U16Y0402
C342 C10U6.3X5-RH
VCCSUS1_05 J6 AB17 VCCSUS_1_5-1 VCCSUS_1_5-2
C134 X_C0.01U25X0402
C136 X_C0.01U25X0402
VCCCL1_05 A20 V_1P05EP_INT
VCCSUS1_5 AB15 J7 V_1P5_SB_INT
C139 C4.7U6.3X5-1
C140 C1U6.3Y0402-RH
C137 C10U6.3X5-RH
C138 C0.1U16Y0402

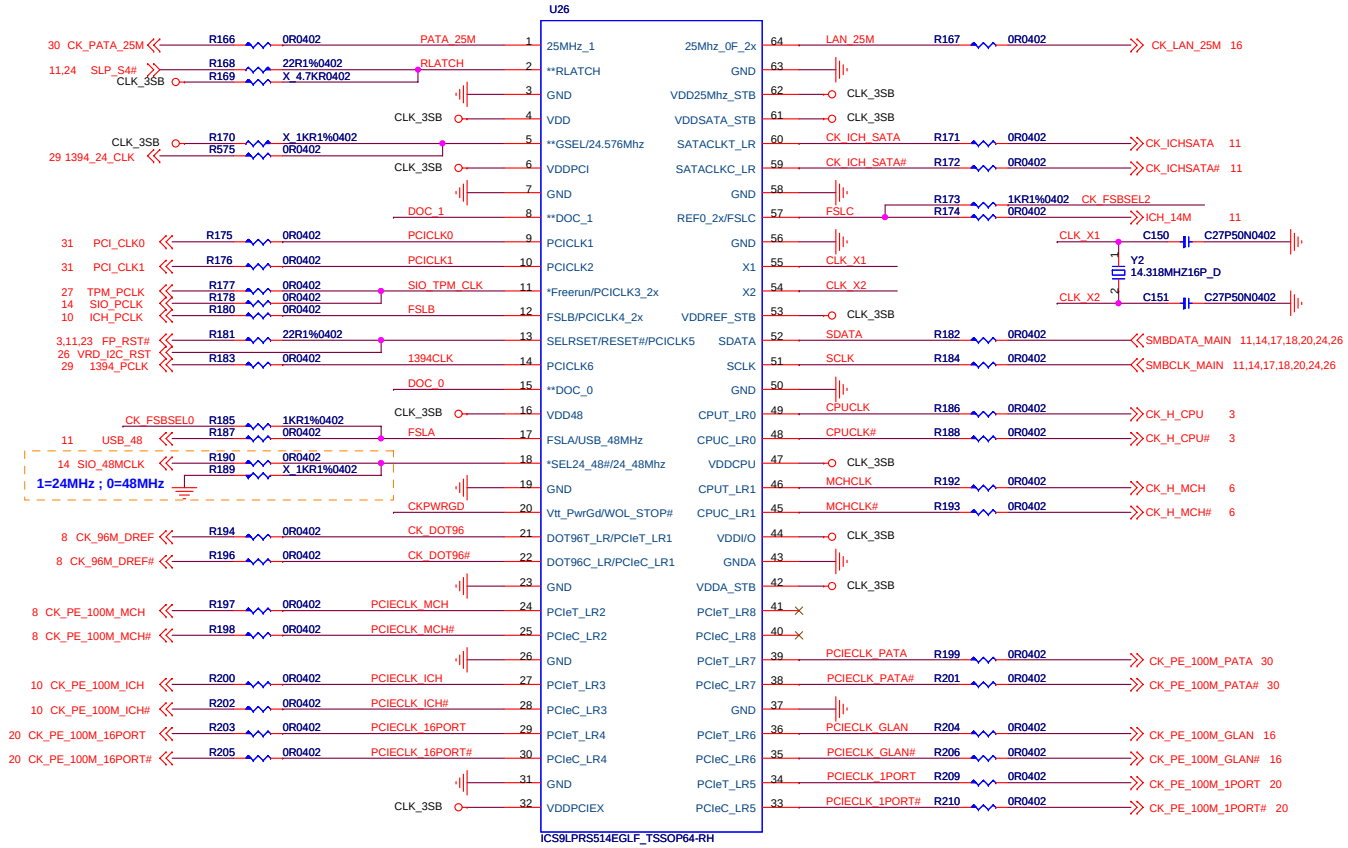
MSI MICRO-START INT'L CO.,LTD.

Title: Intel ICH8 - Power

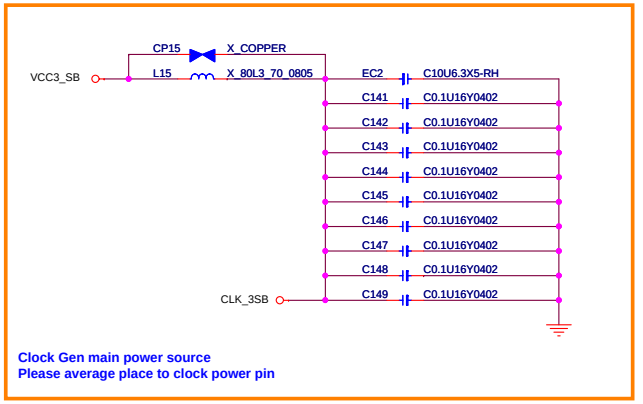
Size | Document Number: MS-7362 | Rev: 0A

Date: Friday, January 19, 2007 Sheet 12 of 39

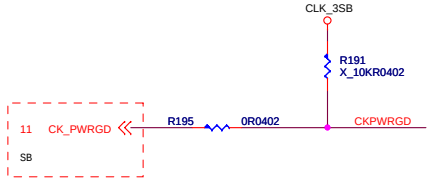
Clock Generator - ICS9LPRS514

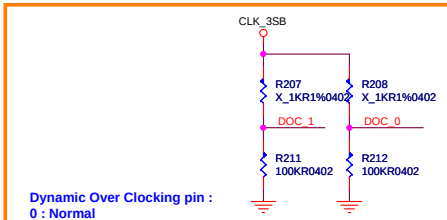


Trace length less than 0.5inchs

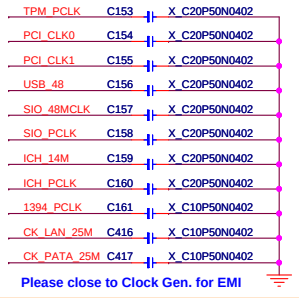


Clock Gen main power source
Please average place to clock power pin

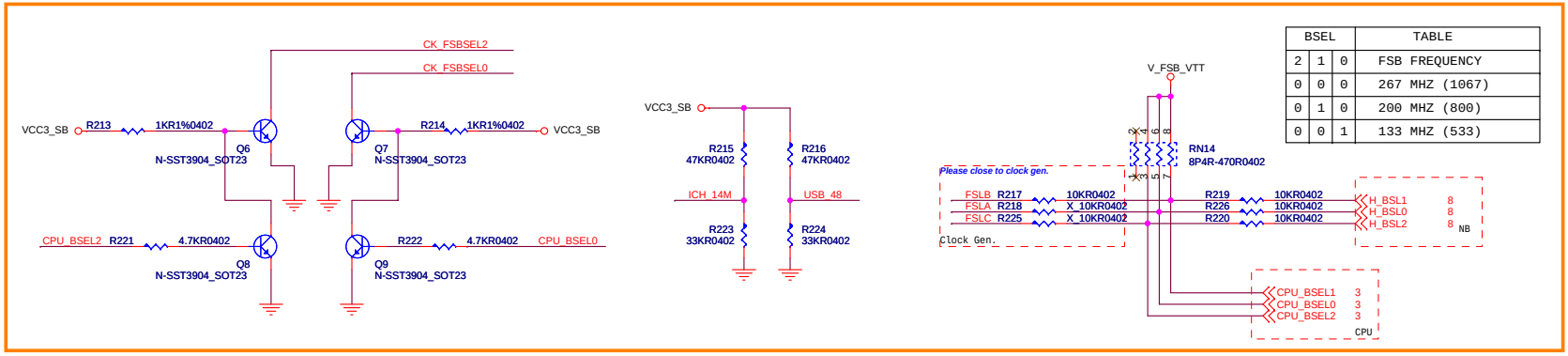




Dynamic Over Clocking pin :
0 : Normal
1 : Frequency will transition to a preprogrammed value in the I2c.



Please close to Clock Gen. for EMI



BSEL			TABLE
2	1	0	FSB FREQUENCY
0	0	0	267 MHZ (1067)
0	1	0	200 MHZ (800)
0	0	1	133 MHZ (533)

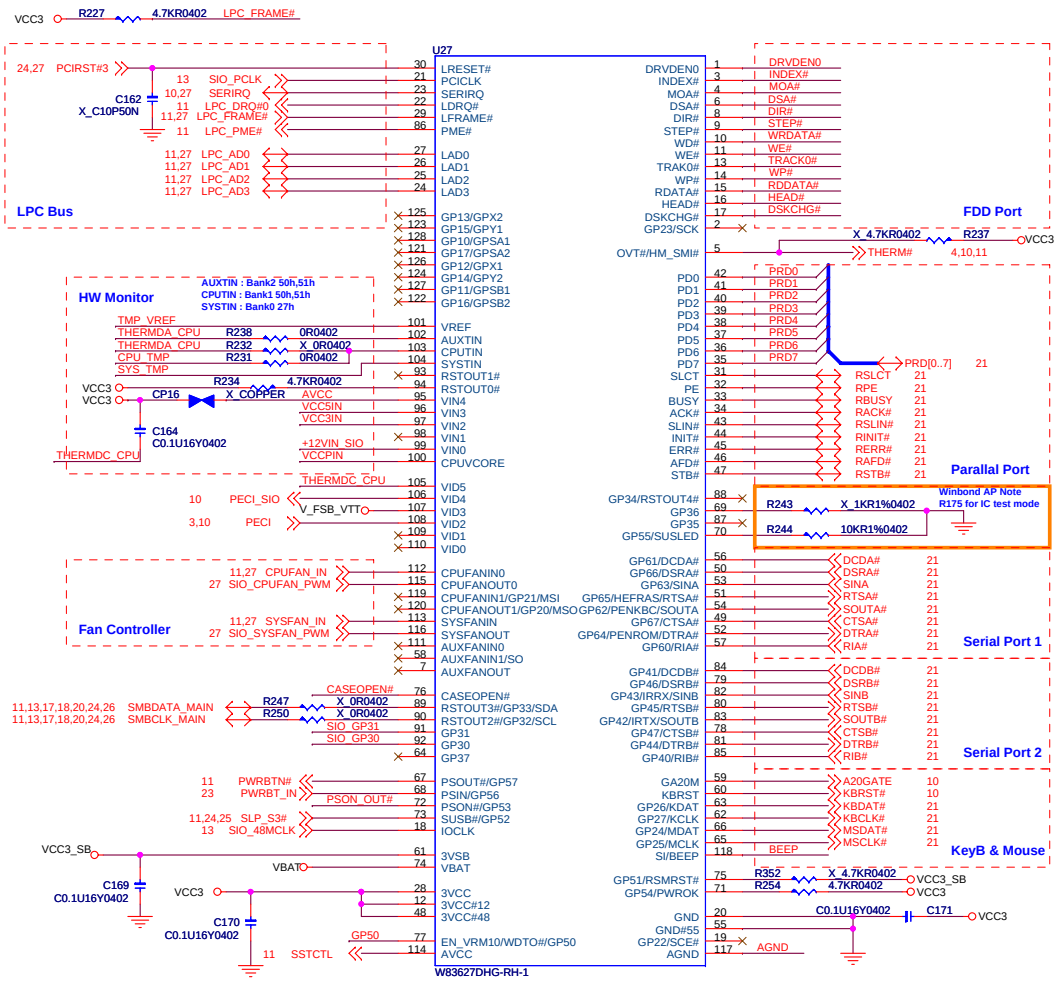
MSI MICRO-STAR INT'L CO.,LTD.

Title: Clock Gen. - ICS9LPRS512

Size | Document Number: MS-7362 | Rev: 0A

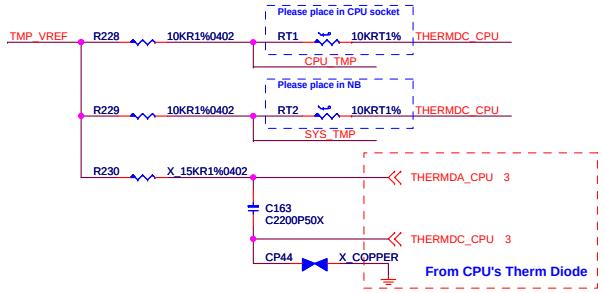
Date: Friday, January 19, 2007 | Sheet 13 of 39

Super I/O For Winbond W83627DHG

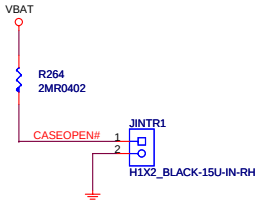


Thermal Resistor Block

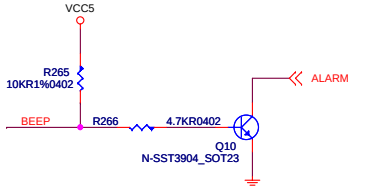
NOTE: LOCATE CLOSE STATUS PANEL



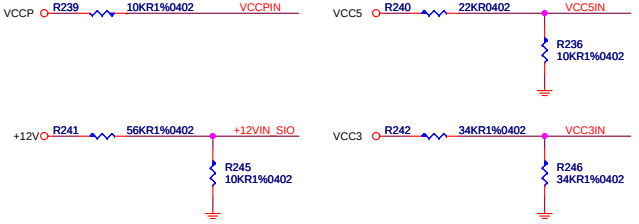
Chasiss Intrusion



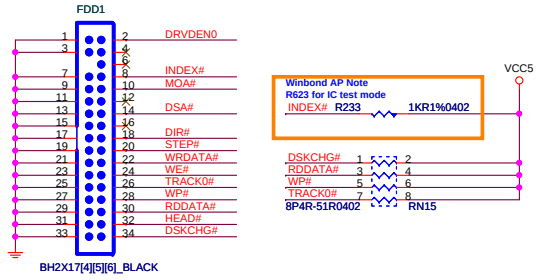
Beep

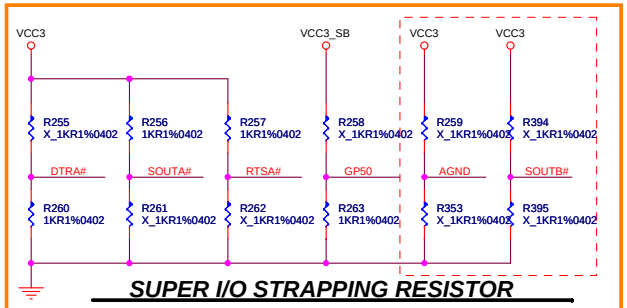


Voltage Monitor Block



Floppy Connector

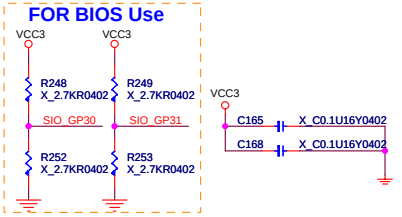




SUPER I/O STRAPPING RESISTOR

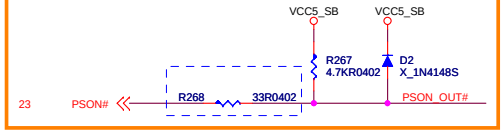
	0	1	
RTSA#	2E	4E	I/O Configuration Address
GP50	TTL Level	GTL Level	VID Level Sellection
SOUTA#	KBC Disable	KBC Enable	KBC Function Enable
DTRA#	Disable SPI	Enable SPI	Enable SPI
PLED	PWMOUT 50%	PWMOUT 100%	For W83627DHG pin 117 CPUFANOUT0 Only
SOUTB#	PWMOUT 50%	PWMOUT 100%	For W83627DHG pin 115 CPUFANOUT1 Only

FOR BIOS Use



AP note for Winbond Super I/O

R443 value might need to be tuned for EOS and compatibility



MICRO-START INT'L CO.,LTD.

Title: Super I/O - W83627DHG

Size | Document Number: MS-7362 | Rev: 0A

Date: Friday, January 19, 2007 | Sheet 14 of 39

Azalia Codec - ALC883 / ALC888

Add R264 to support ALC883
Del R264 to support ALC888

Closer to Codec

Close to Codec

Close to Codec

Trace Width 20mils.

Trace Width 30mils.

Please place in top-side and botton-side

ALC888-GR-A2-RH

AUDIO CODE REGULATORS

SPDIF OUT

Front Panel

D : Line in
E : Front line out
F : Mic in
A : Surround line out
B : Center / Lfe line out
C : Side surround line out

Desktop Configuation for pure ALC882/883:(7.1 Channel Solution)
Rear Panel:6 jacks have specific functionality
Front Panel:2 jacks are Universal Audio Jack

Pin Assignment	Location	Function
FRONT(pin-35/36)	Back Panel	Front line out w/ amplifier
SURR (pin-39/41)	Back Panel	Surround line out
CEN/LFE (pin-43/44)	Back Panel	Center/Lfe line out
SIDESURR (pin-45/46)	Back Panel	Side surround line out
LINE1 (pin-23/24)	Back Panel	Line in / Shared surround out
MIC1 (pin-21/22)	Back Panel	Mic in / Shared Center-Lfe out
LINE2 (pin-14/15)	Front Panel	Headphone out / line in / mic in
MIC2 (pin-16/17)	Front Panel	Mic in / Headphone out / line in

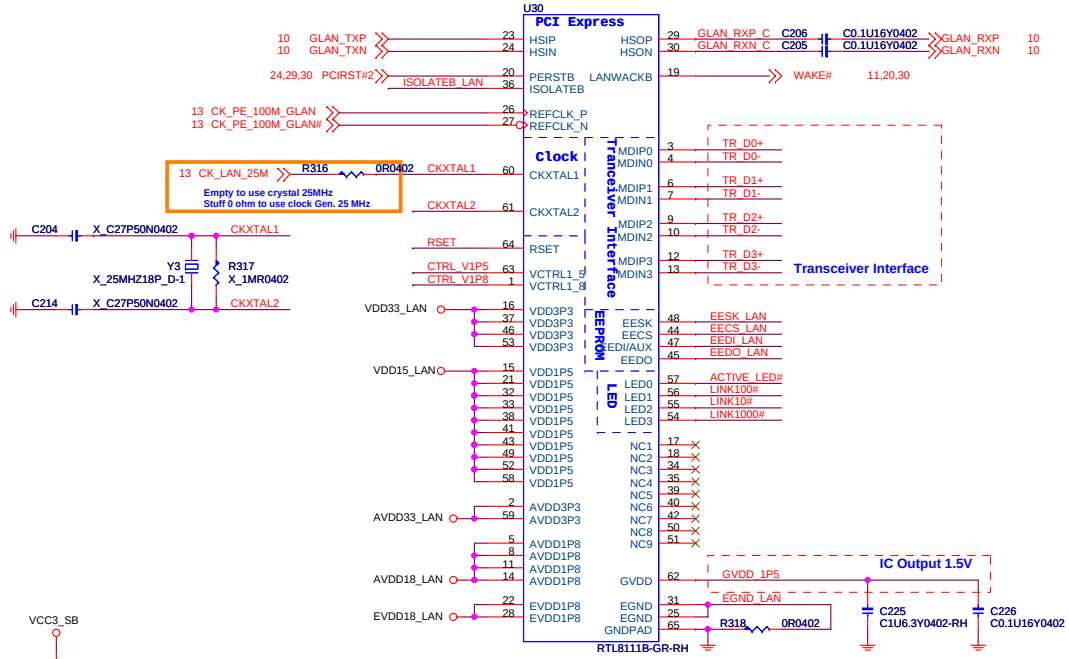
MICRO-START INT'L CO.,LTD.

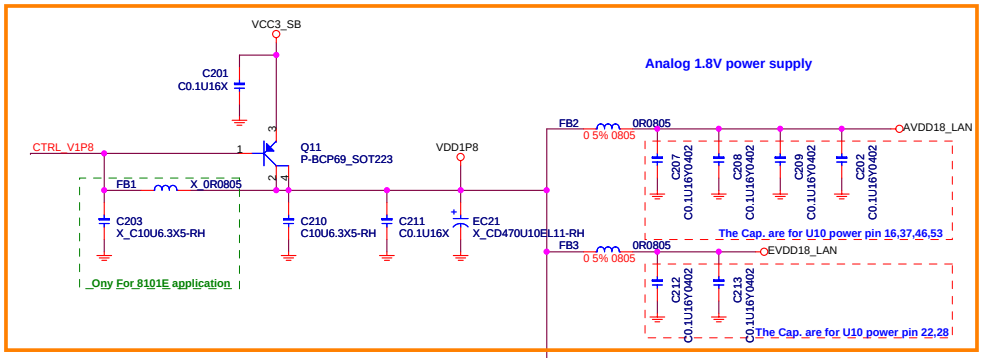
Title: Azalia Codec - ALC883 / 882

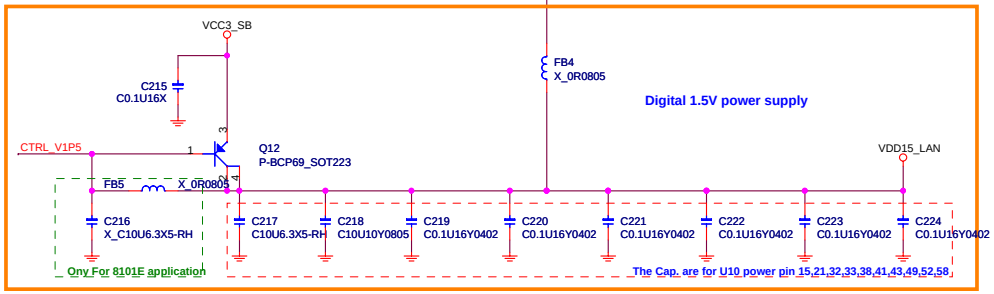
Size: | Document Number: MS-7362 | Rev: 0A

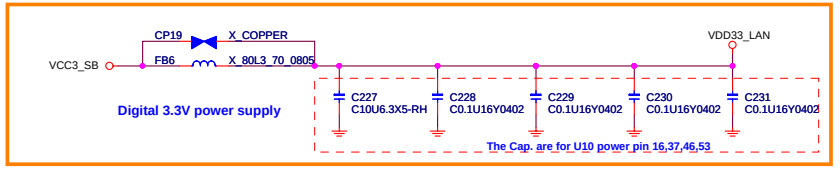
Date: Friday, January 19, 2007 | Sheet 15 of 39

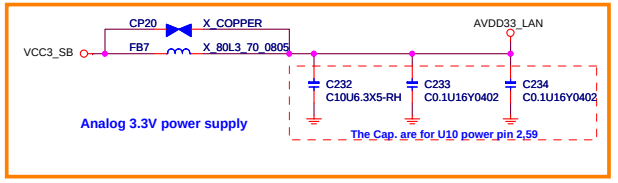
RealTek - RTL8111B-GR / RTL8101E-GR

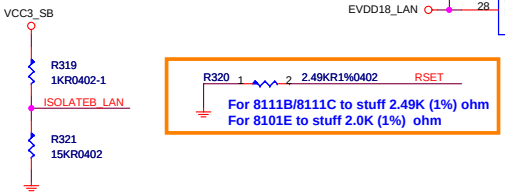


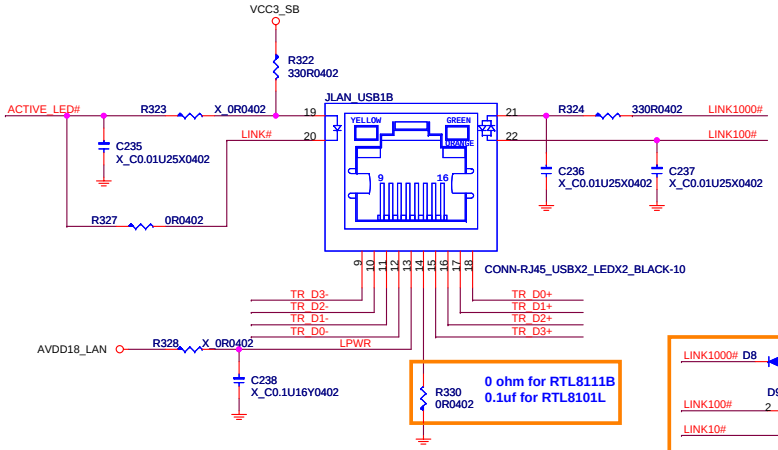


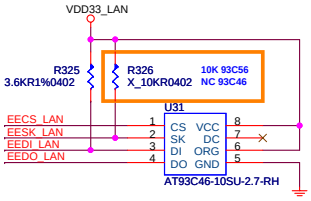


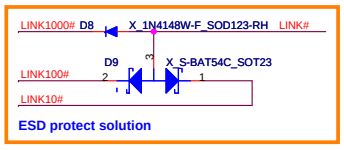


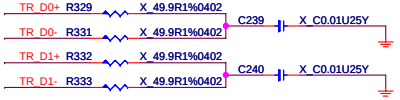












Power Domain Chart

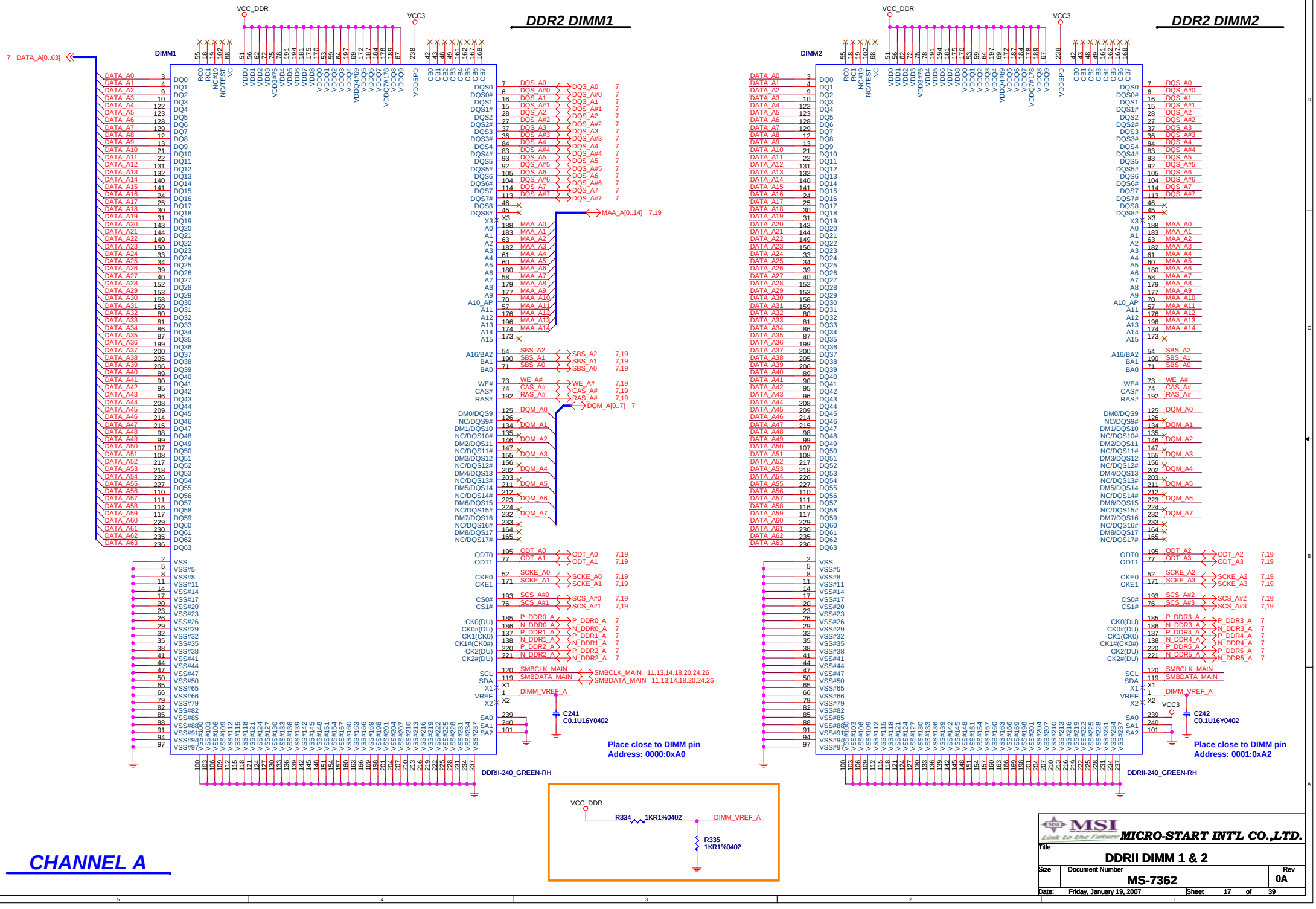
	RTL8111B	RTL8101E	RTL8111C
AVDD33	3.3V	3.3V	3.3V
AVDD18	1.8V	1.8V	1.2V
EVDD18	1.8V	1.8V	1.2V
DVDD15	1.5V	1.5V	1.2V
Q1	Need	N/A	N/A
Q2	Need	N/A	N/A

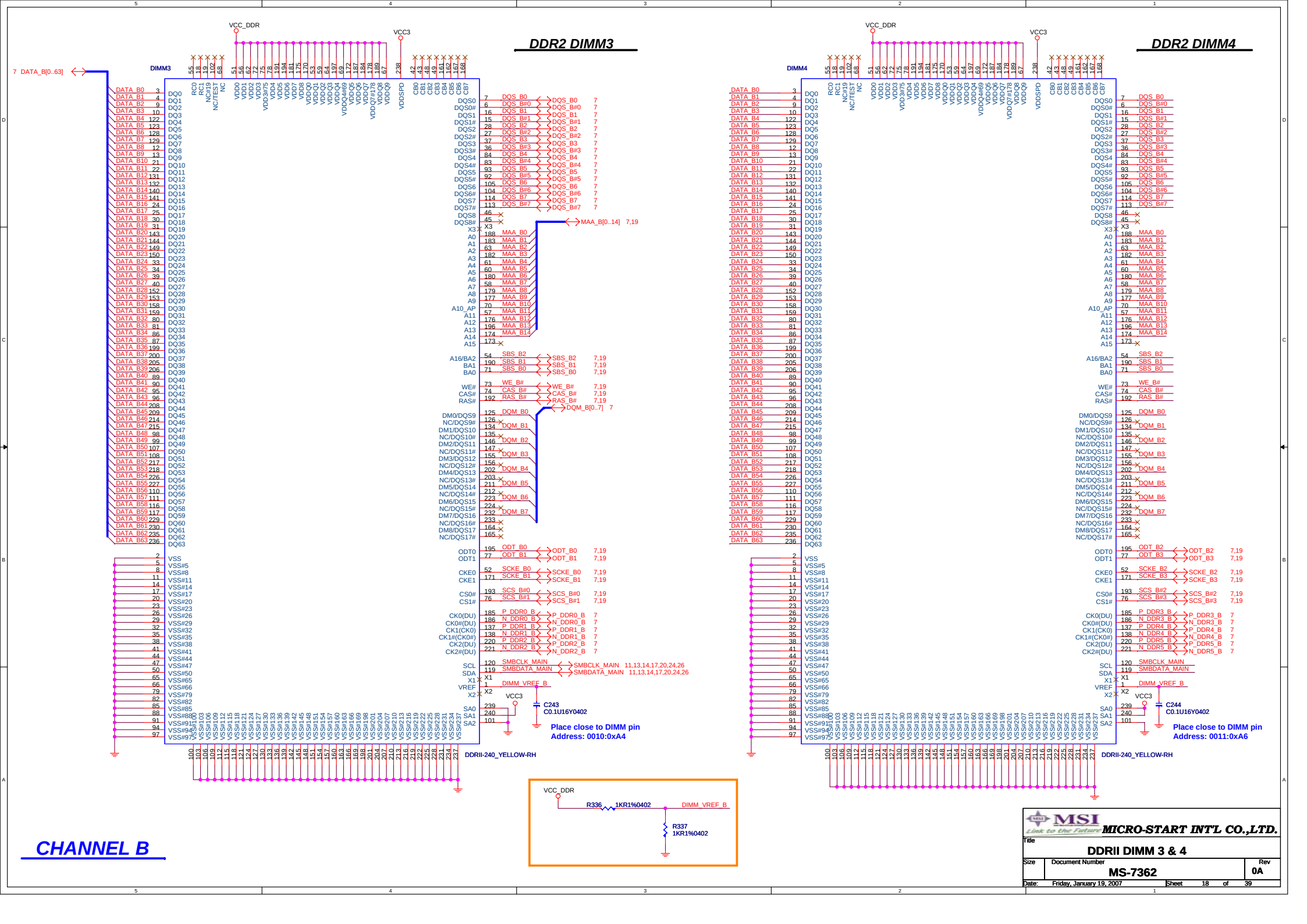
MICRO-START INTL CO.,LTD.

Title: Lan - RealTek 8111B/8101E

Size | Document Number: MS-7362 | Rev: 0A

Date: Friday, January 19, 2007 | Sheet 16 of 39

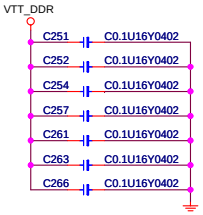

DDR2 DIMM1
DDR2 DIMM2
CHANNEL A
VCC_DDR
VCC3
DIMM1
DIMM2
7 DATA_A[0..63]
DDRII-240_GREEN-RH
Place close to DIMM pin
Address: 0000:0xA0
Place close to DIMM pin
Address: 0001:0xA2
C241
C0.1U16Y0402
C242
C0.1U16Y0402
R334 1KR1%0402
R335
1KR1%0402
DIMM_VREF_A
MAA_A[0..14] 7,19
DQM_A[0..7] 7
SMBCLK_MAIN 11,13,14,18,20,24,26
SMBDATA_MAIN 11,13,14,18,20,24,26
MICRO-START INT'L CO.,LTD.
Title
DDRII DIMM 1 & 2
Size
Document Number
MS-7362
Rev
0A
Date: Friday, January 19, 2007
Sheet 17 of 39



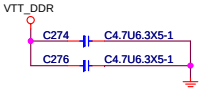
MICRO-START INTL CO.,LTD.

Title	DDRII DIMM 3 & 4	
Size	Document Number: MS-7362	Rev: 0A
Date: Friday, January 19, 2007	Sheet 18 of 39	

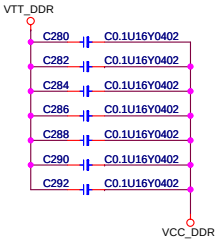
CHANNEL A V_SM_VTT
DECOULPING CAPS



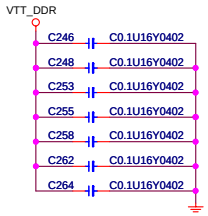
PLACED AT LEFT AND
RIGHT ENDS OF
VTT ISLAND



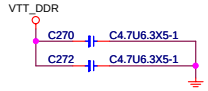
CHANNEL A ADDRESS/CONTROL
STITCHING CAPS



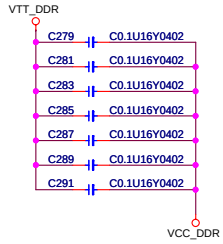
CHANNEL B V_SM_VTT
DECOULPING CAPS



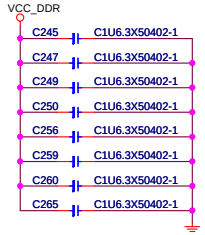
PLACED AT LEFT AND
RIGHT ENDS OF
VTT ISLAND



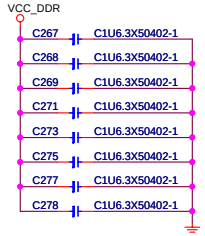
CHANNEL B ADDRESS/CONTROL
STITCHING CAPS



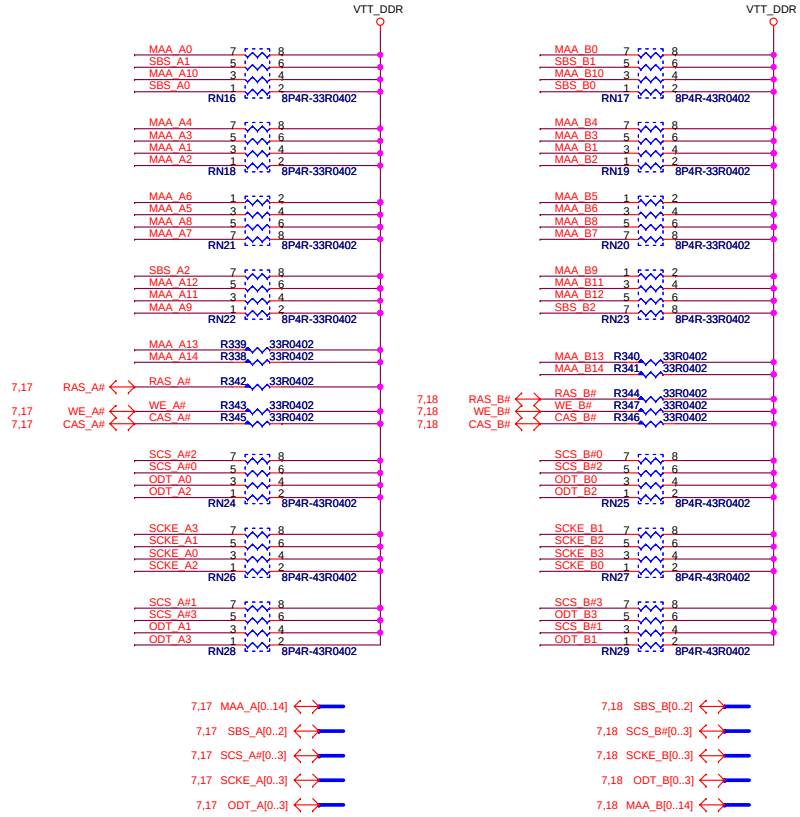
Close to DIMM slot
as possible



Close to DIMM slot
as possible



Close to DIMM slot
as possible



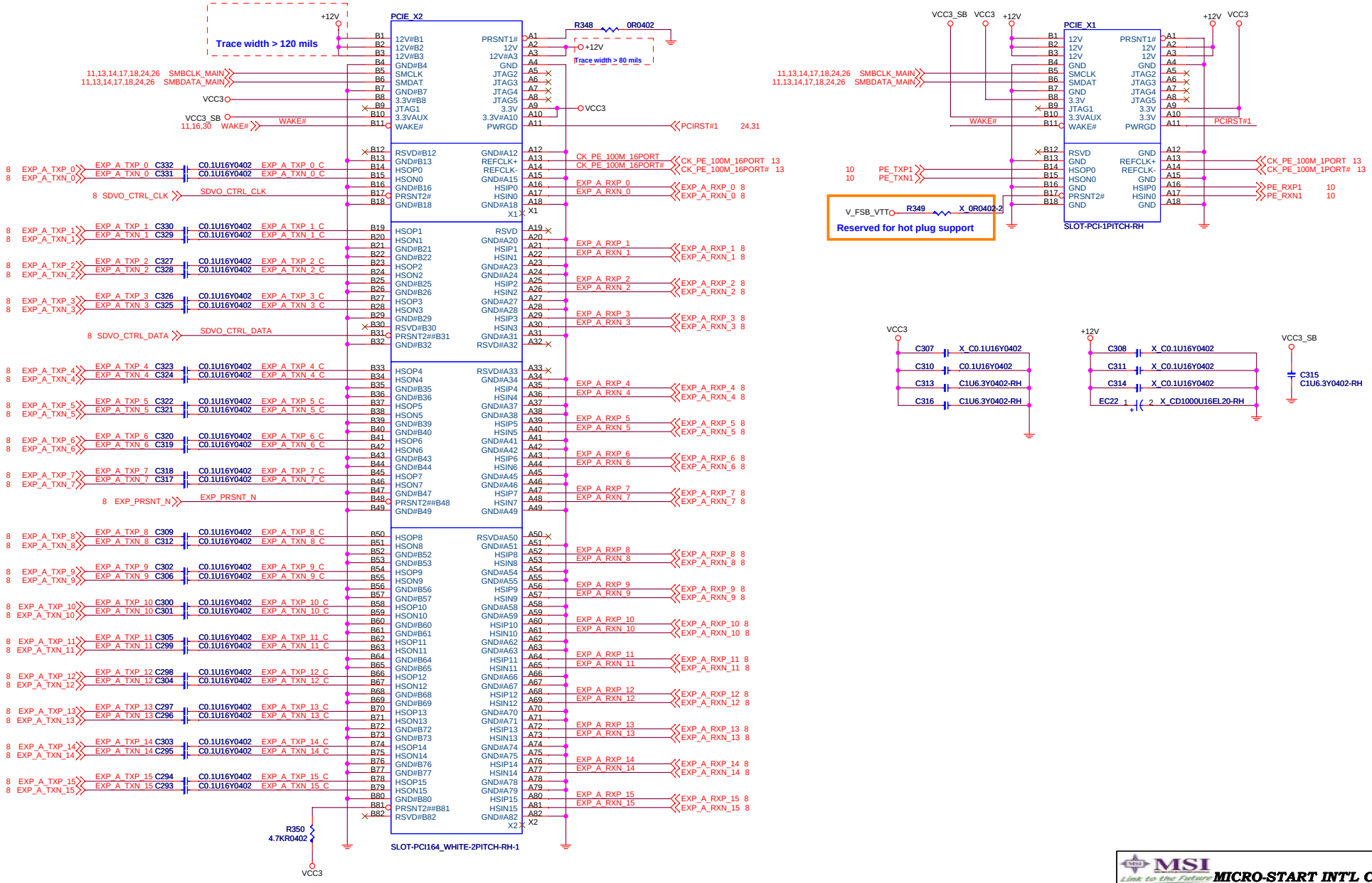
MICRO-START INT'L CO.,LTD.

Title: DDRII Termination

Size	Document Number	Rev
	MS-7362	0A

Date: Friday, January 19, 2007 Sheet 19 of 39

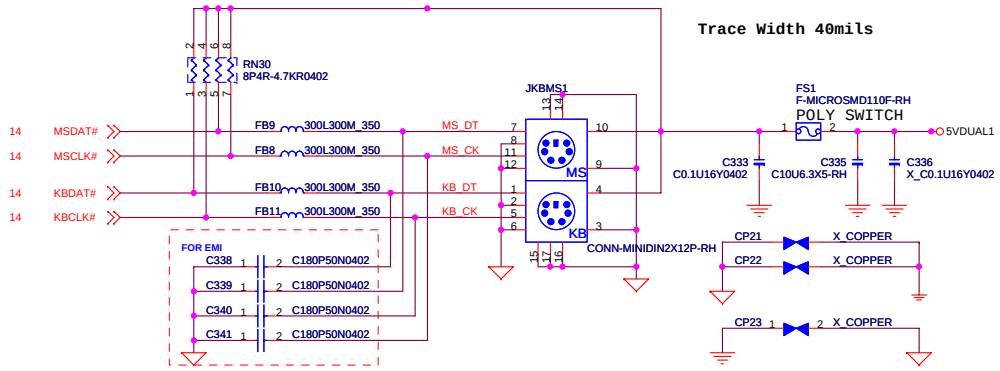
PCI Express x 16 & x 1 Slot



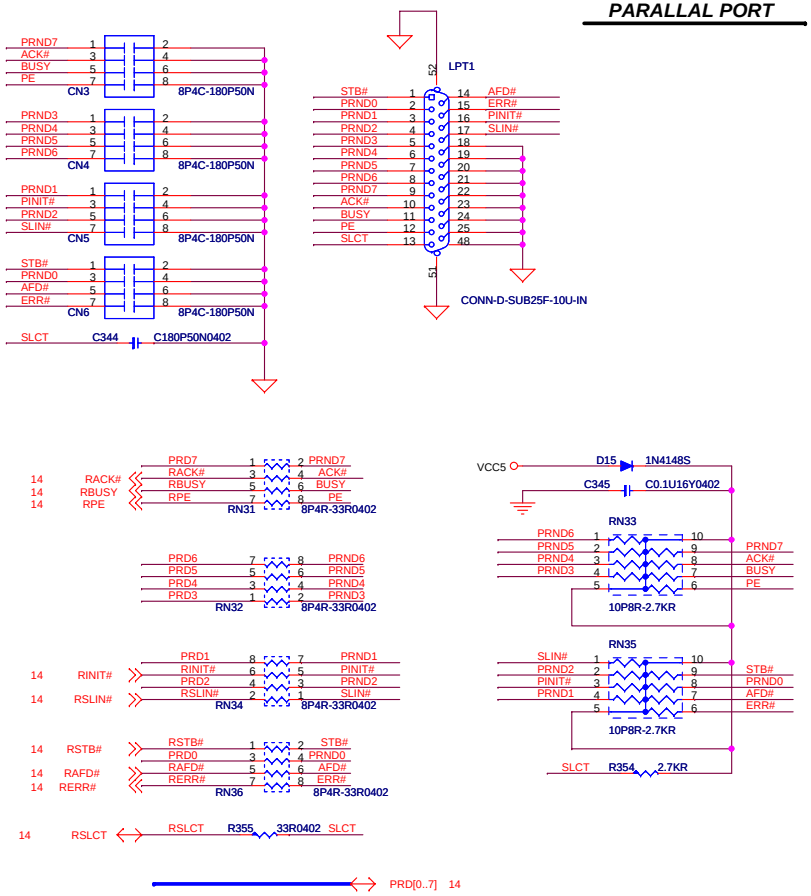
MICRO-START INT'L CO.,LTD.

Title	PCI Express x16 & x1	
Size	Document Number: MS-7362	Rev: 0A
Date: Friday, January 19, 2007	Sheet 20 of 39	

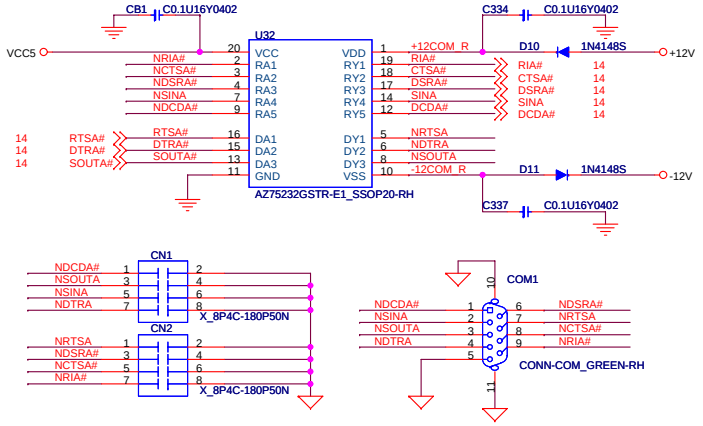
PS2 KEYBOARD & MOUSE CONNECTOR



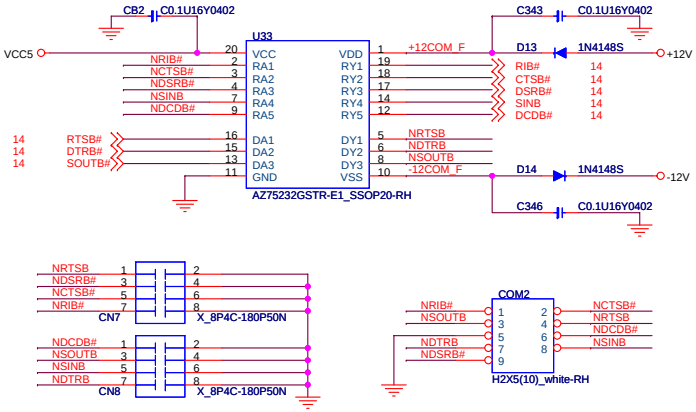
PARALLAL PORT

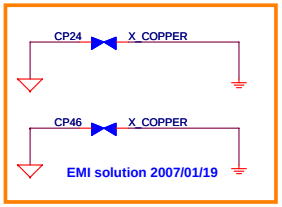


Serial Port 1



Serial Port 2

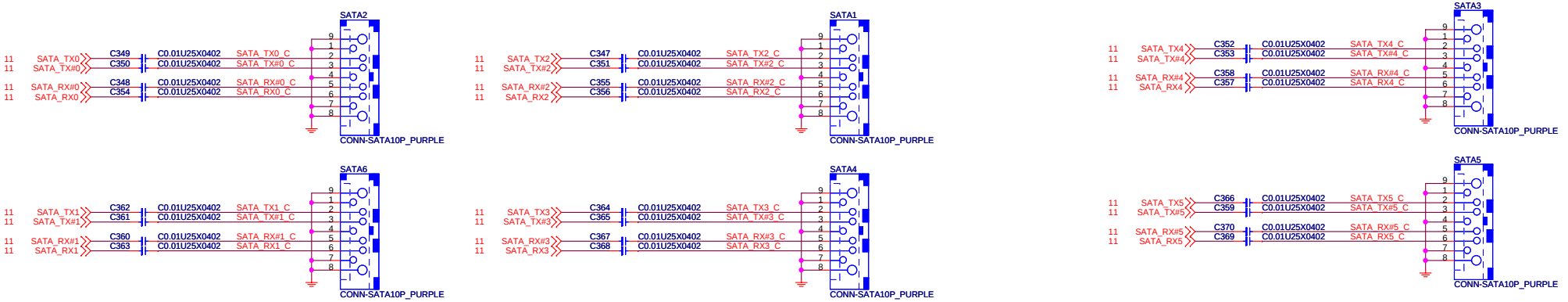




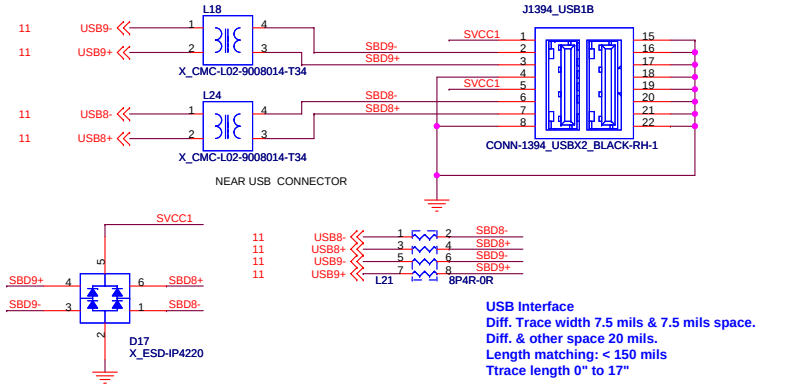
MSI MICRO-START INT'L CO.,LTD.

Title	LPT / COM / KB / MS	
Size	Document Number: MS-7362	Rev: 0A
Date: Friday, January 19, 2007	Sheet 21 of 39	

Serial ATA Connector and USB Connector

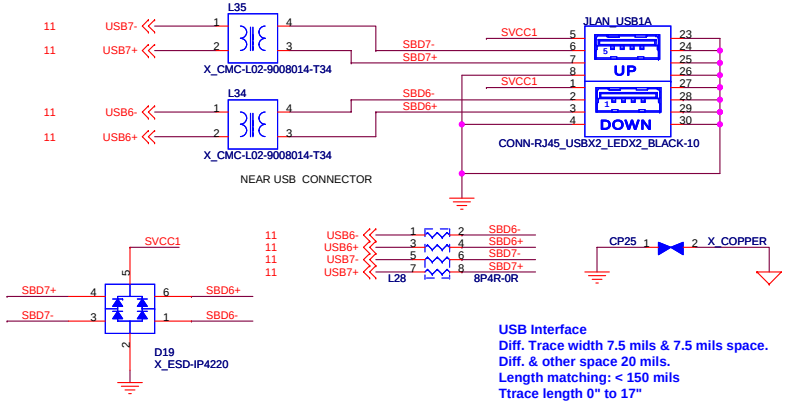


REAR PANEL USB CONNECTOR FOR USB PORT 8,9



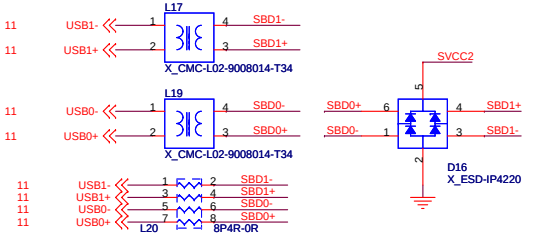
USB Interface
Diff. Trace width 7.5 mils & 7.5 mils space.
Diff. & other space 20 mils.
Length matching: < 150 mils
Ttrace length 0" to 17"

REAR PANEL USB CONNECTOR FOR USB PORT 6,7

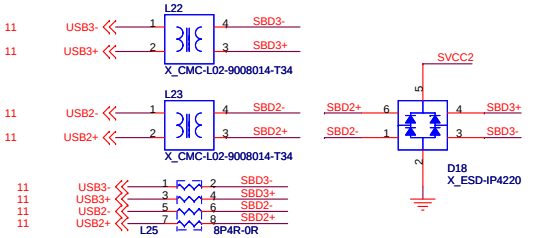


USB Interface
Diff. Trace width 7.5 mils & 7.5 mils space.
Diff. & other space 20 mils.
Length matching: < 150 mils
Ttrace length 0" to 17"

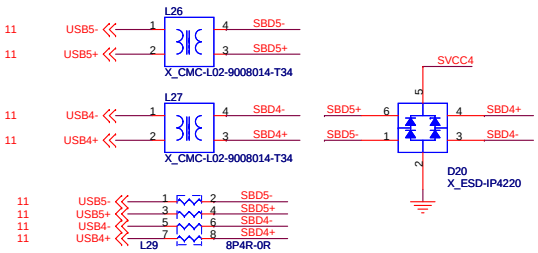
FRONT PANEL USB CONNECTOR FOR USB PORT 0,1



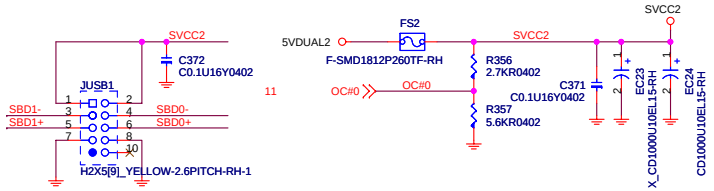
FRONT PANEL USB CONNECTOR FOR USB PORT 2,3



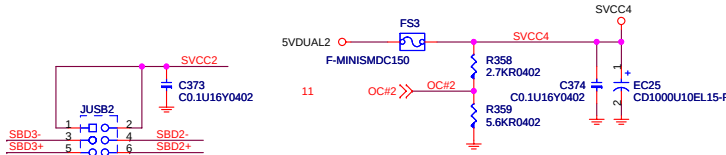
FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



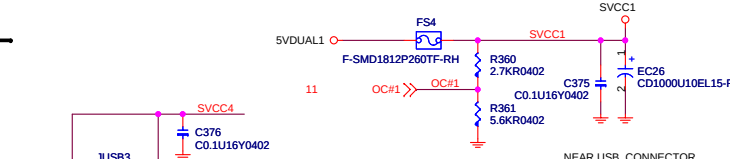
POWER CIRCUIT FOR USB PORT 0,1,2,3 (FRONT)



POWER CIRCUIT FOR USB PORT 4,5 (FRONT)



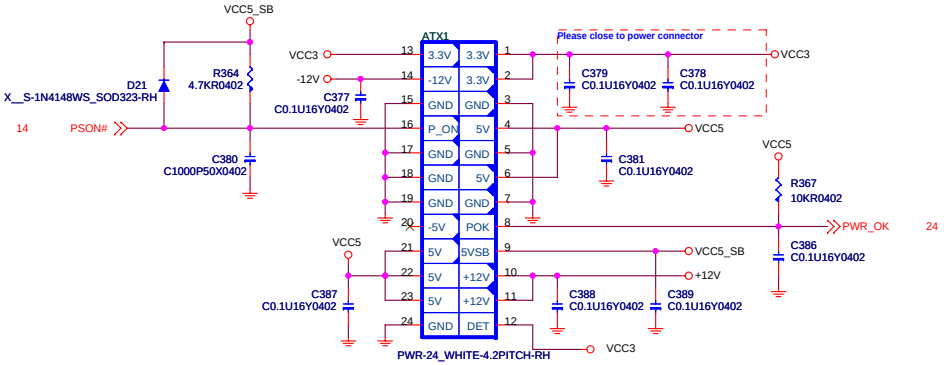
POWER CIRCUIT FOR USB PORT 6,7,8,9 (REAR)



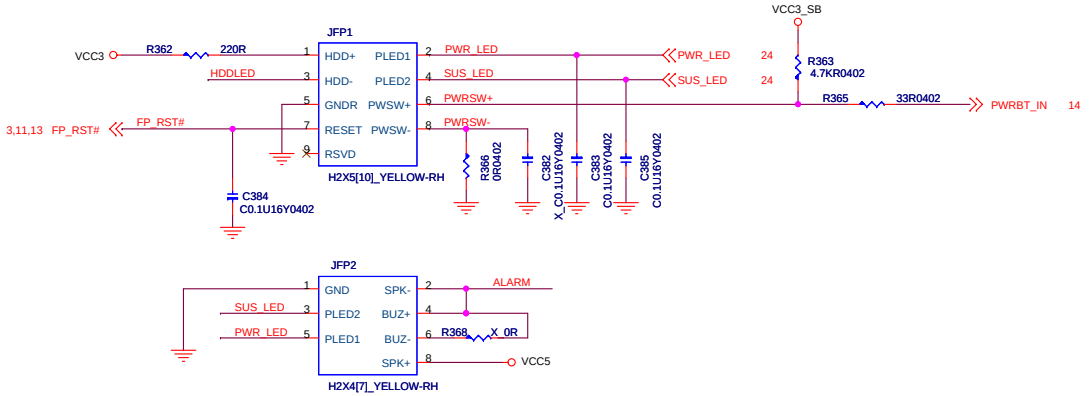
MSI MICRO-START INT'L CO.,LTD.

Title	USB / SATA Connectors	
Size	Document Number: MS-7362	Rev: 0A
Date: Friday, January 19, 2007	Sheet 22 of 39	

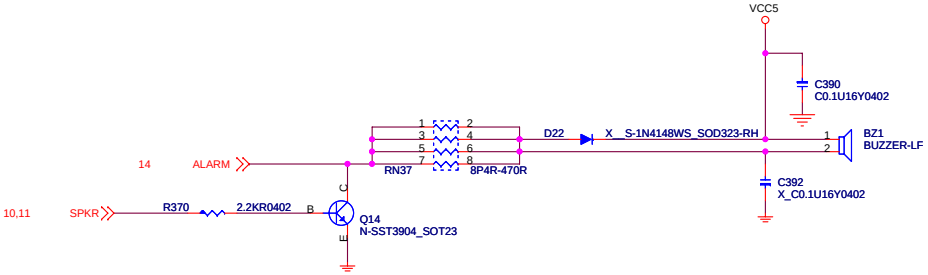
BTX Connector



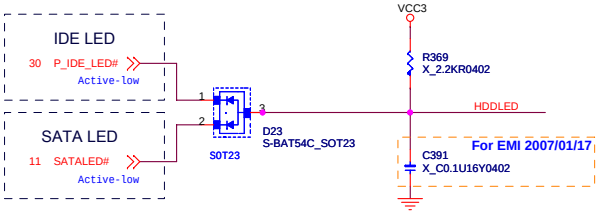
Intel Front Panel



BUZZER



HDD LED



MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title	BTX Connector & Front Panel	
Size	Document Number MS-7362	Rev 0A
Date: Friday, January 19, 2007	Sheet 23 of 39	

ACPI Controller

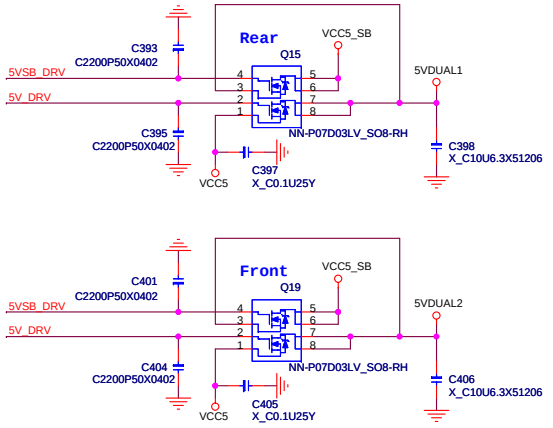
3VSB MODE SELECT

3VSB MODE	3VDLDEC#
SINGLE MOSFET	PULL HIGH
DUAL MOSFET	PULL LOW

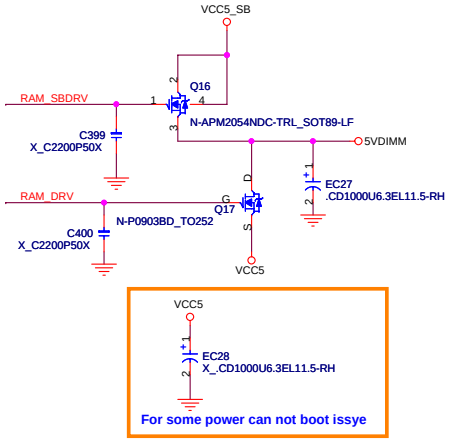
VDIMM LINEAR OR PWM SELECT

VDIMM MODE	EXTRAM
LINEAR REGULATOR	PULL LOW
PWM REGULATOR	PULL HIGH

5V DUAL Power (USB)



5VDIMM(DDRII Power)

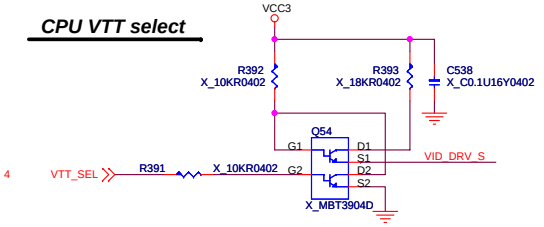


For some power can not boot issye

DDR AND DDR II VOLT SELECT

DDRTYPE (pin9)	DDR Voltage
Pull Low	2.5V
Pull High	1.8V

CPU VTT select



For CPU VTT 1.1V Power
VID Ref = 1.2V Remove this schematic

VTT_SEL = L	V_FSB_VTT=1.1V	For future KENTSFIELD processor. (FSB1333, Quad-Core)
VTT_SEL = H	V_FSB_VTT=1.2V	For normal processors.

V_FSB_VTT

CPU:5.3A + NB:1A

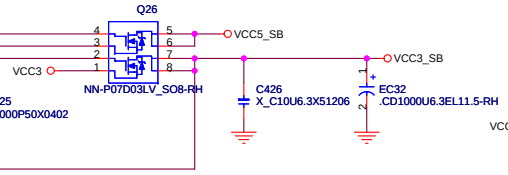
THIS PIN IS OPEN DRAIN OUTPUT

VID Ref = 1.1V
Remove R510,R514

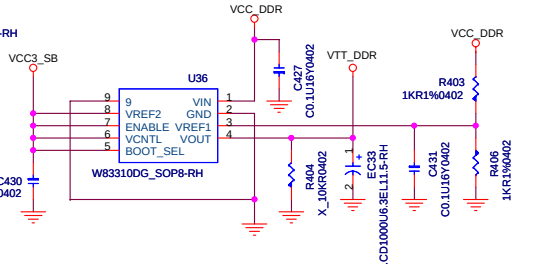
For V_FSB_VTT can't turn off at S3 state and S3 can't resume issue.
Form VCC_DDR change to V_1P25_CORE.

From Intel CRB rev:1.3 page 81
For cost down solution.

VCC3_SB Power



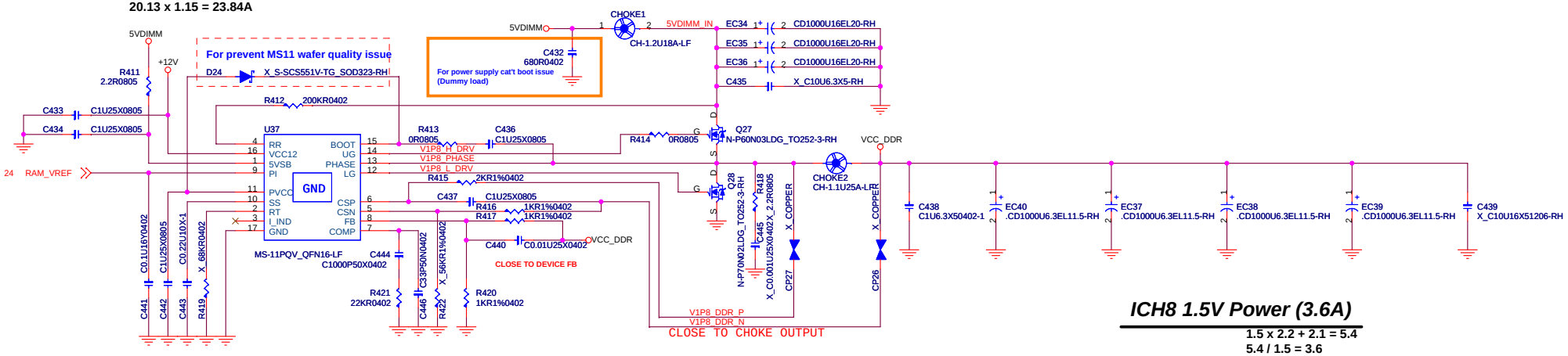
DDR VTT Power (1.2A)



Company	MICRO-START INT'L CO.,LTD.
Title	ACPI Controller - MS7
Size	Document Number: MS-7362
Rev	0A
Date:	Friday, January 19, 2007
Sheet	24 of 39

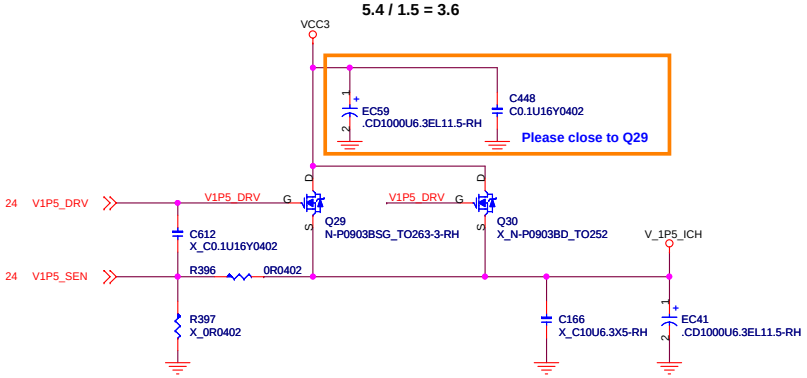
VCC_DDR 1.8V (25A)

16.92W + 6.714W + 1.08W + 7.2W + 3.3W + 2.1W = 37.314W
37.314 / 1.8 = 20.73A
20.13 x 1.15 = 23.84A



ICH8 1.5V Power (3.6A)

1.5 x 2.2 + 2.1 = 5.4
5.4 / 1.5 = 3.6

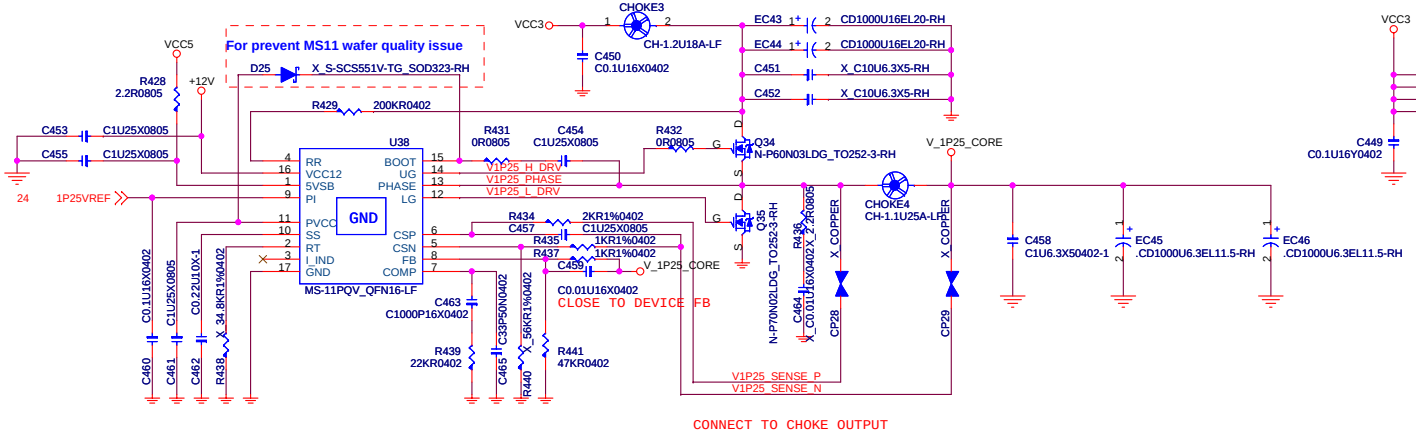


MS11 Switch Solution
High Side MOS
D03-60N032B-N03
,DIS MOSFET-N,NIKO/P60N03LDG,TO252,60A,25V,±20V,13.8mOhm(10V/22A),0.8V,1.2V,2.5V,600pF,,30nC,,RoHS COMPLIANCE

Low Side MOS
D03-70N023B-N03
,DIS MOSFET-N,NIKO/P70N02LDG,TO252,65A,25V,±20V,8.5mOhm(10V/25A),1V,1.6V,3V,1200pF,1800pF,25nC,50nC,RoHS COMPLIANCE

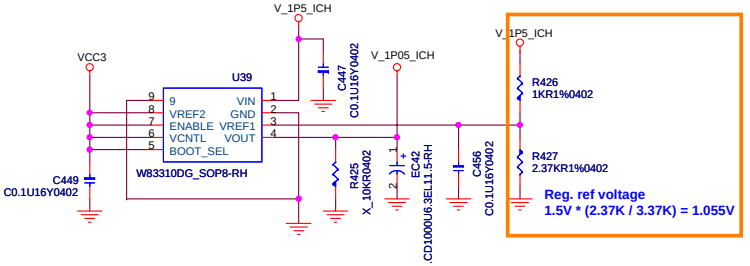
Liner Solution
D03-0903BDB-N03
,DIS MOSFET-N,NIKO/P0903BDG,TO252,50A,25V,+/-20V,9.5mohm(10V/25A),1V,,3V,1800pF,,50nC,,RoHS COMPLIANCE

GMCH/ICH8 1.25V Power (21.3A)



ICH8 1.05V Power (2A)

1.05 x 2 = 2.1



MICRO-START INT'L CO.,LTD.

Title: Power Regulator - MS11

Size | Document Number: MS-7362 | Rev: 0A

Date: Friday, January 19, 2007 | Sheet 25 of 39

ATX12V Power Connector

CP1,CP2,CP3,CP4,
CP5,CP6 PLACE ON
THE SOLDER SIDE,
CLOSE INDUCTOR

OUTPUT
INDUCTOR

VR Configuration	Starting Current	Ending Current	Dynamic Current Step	VTT Rise Time
775_VR_Config_04A	23A	78A	55A	800ns
775_VR_Config_04B	24A	119A	95A	800ns
775_VR_Config_05A	20A	85A	65A	50ns
775_VR_Config_05B	30A	125A	95A	50ns
775_VR_Config_06B	25A	65A	TBD	50ns

For EMI solution 2007/01/17
Q39 GND on +12VP_FET
Q43 GND on +12VP_FET
Q47 GND on +12VP_FET
Reverse at botton side

2006-04-12 Power team solution
R346 -> 4.7K ohm
R340 -> 30K ohm
R367 -> 47K ohm
C481 -> 1000p

2006-06-20 Power team solution
R346 -> 1.65 Kohm (Droop)
R340 -> 13 Kohm (Compensation)
R367 -> 49.9 Kohm (Offset)
R369 -> 1 Kohm (OVPSEL, VDAC+350mV)
R344 -> 89.9 ohm (ISEN1)
R351 -> 33 ohm (ISEN2)
R364 -> 0 ohm (ISEN3)

Reserve for ISL6322 I2C function!!!

BOTTOM PAD CONNECT
TO GND Through 8 VIAs

Ceramic Cap.
C11-1067017-T04
,CAP MLCC,10uF,6.3V,X5R,1206,20%,1.6mm,RoHS COMPLIANCE

OS-CON Cap.
Main source : C94-6810421-P01
,CAP EL,680uF,4V,DIP-8x9/3.5mm(NOT SLEEVE),20%,28mOhm,900mA,105C,2000hrs,RoHS COMPLIANCE
Second source : C94-6810411-O02
,CAP EL,680uF,4V,DIP-8x8/3.5mm,20%,28mOhm,750mA,105C,2000hrs,RoHS COMPLIANCE

High Side MOS
D03-0903BDB-N03
,DIS MOSFET-N,NIKO/P0903BDG,TO252,50A,25V,+/-20V,9.5mohm(10V/25A),1V,,3V,1800pF,,50nC,,RoHS COMPLIANCE
Low Side MOS
D03-70N023B-N03
,DIS MOSFET-N,NIKO/P70N02LDG,TO252,65A,25V,±20V,8.5mOhm(10V/25A),1V,1.6V,3V,1200pF,1800pF,25nC,50nC,RoHS COMPLIANCE

OS-CON
(EL-Cap)

SP-CON

X5R
Ceramic

Y5V
Ceramic

MSI MICRO-STAR INT'L CO.,LTD.

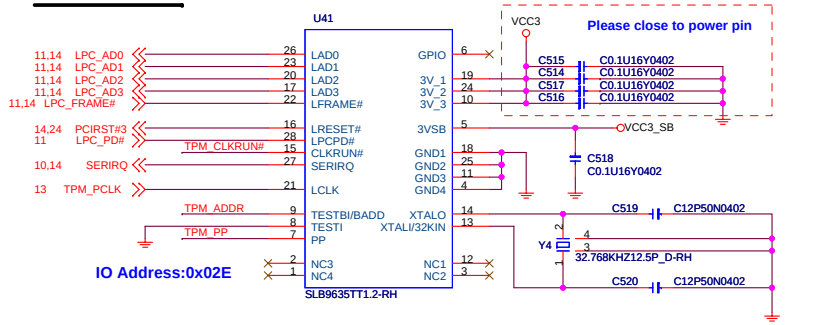
Title: VRM 11 - Intersil 6312/6322

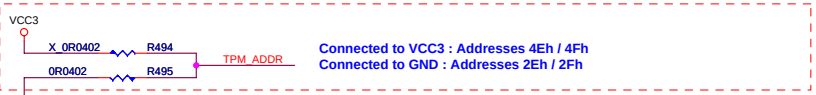
Size | Document Number: MS-7362 | Rev: 0A

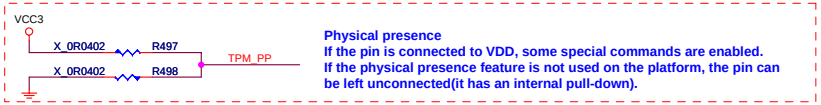
Date: Friday, January 19, 2007 | Sheet 26 of 39

TPM 1.2 / FAN Controller

TPM 1.2

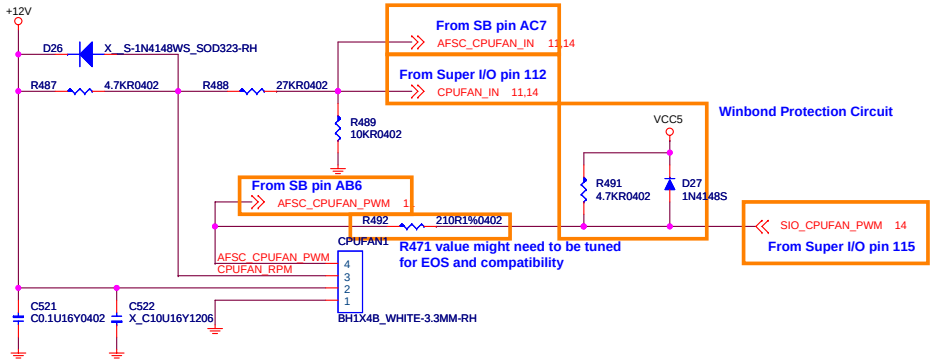






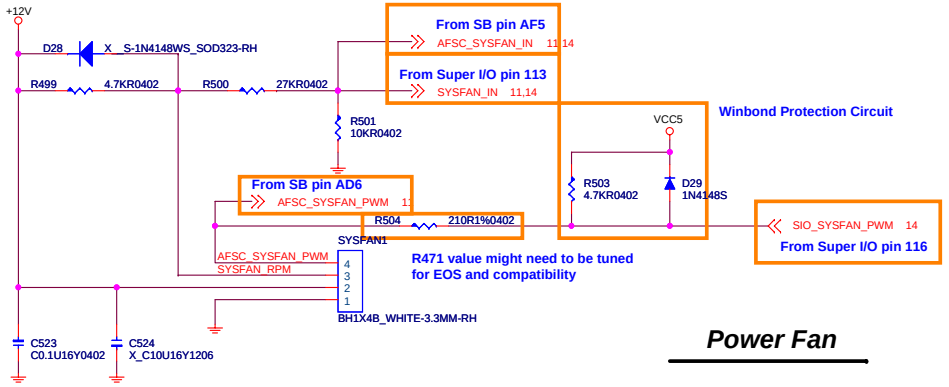
CPU Fan

PWM Mode

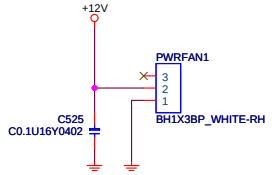


System Fan

PWM Mode



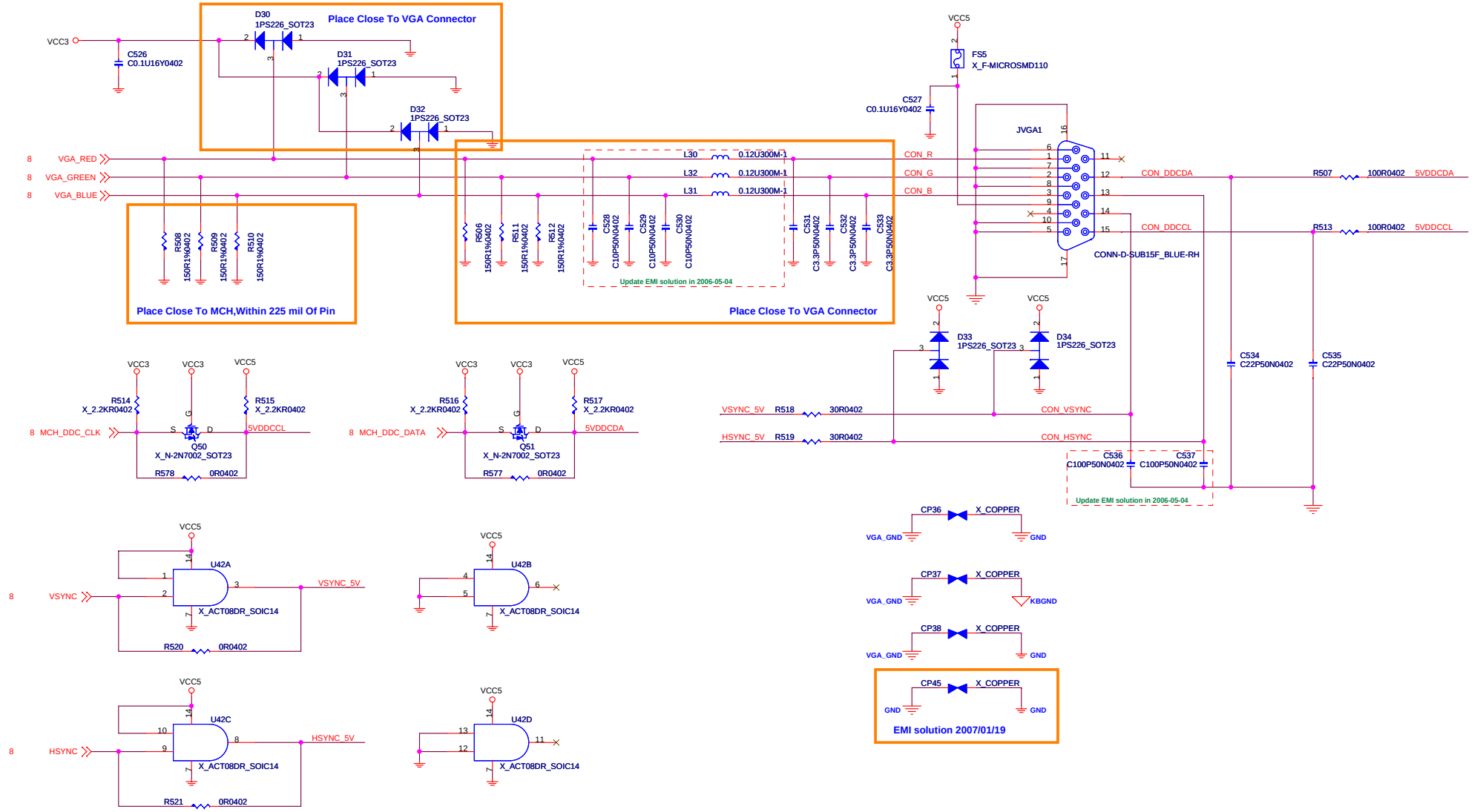
Power Fan



MICRO-START INT'L CO.,LTD.

Title	TPM 1.2 / FAN Controller	
Size	Document Number MS-7362	Rev 0A
Date: Friday, January 19, 2007	Sheet 27 of 39	

Video Connector

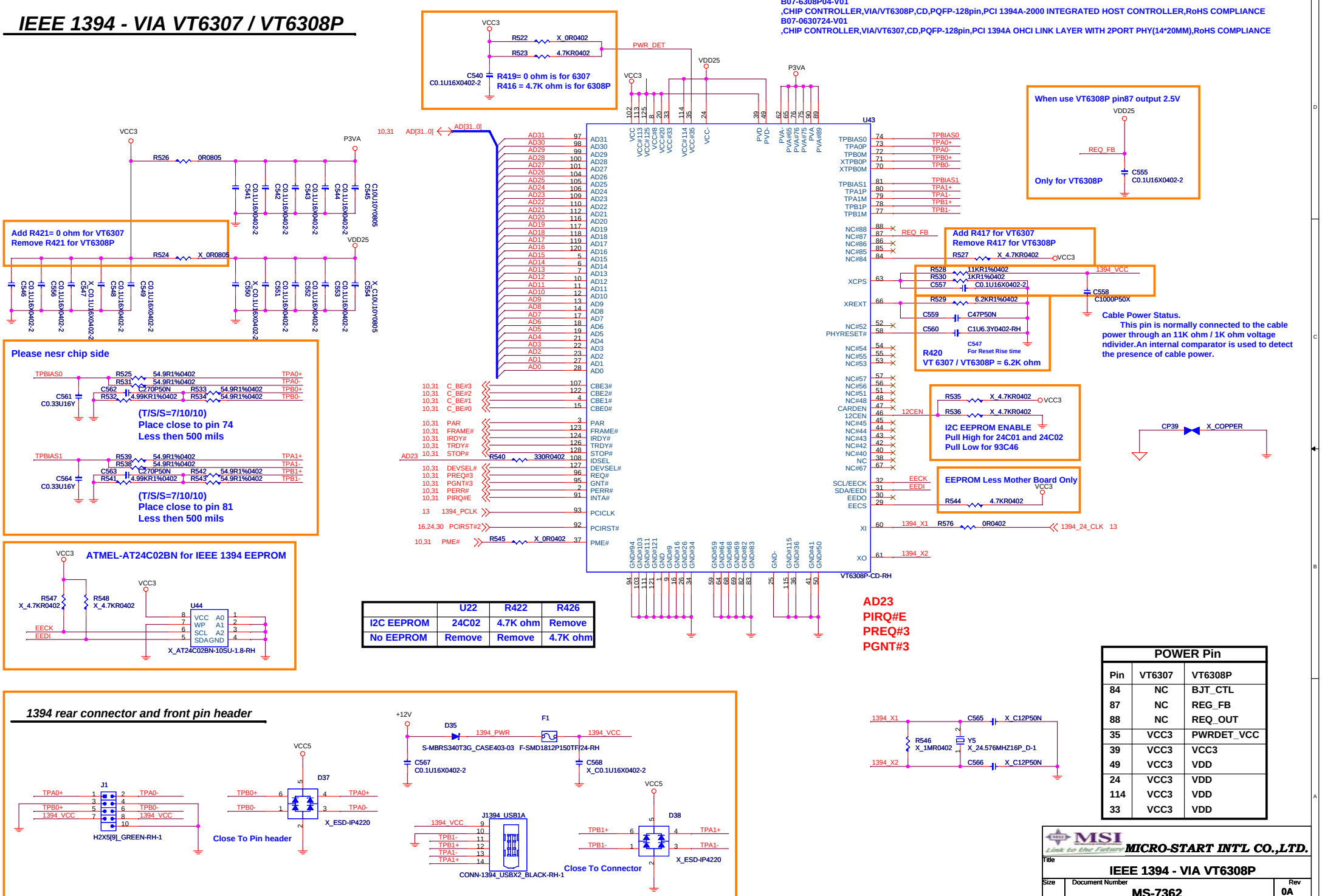


MICRO-START INT'L CO.,LTD.

Title	D-Sub Connector	
Size	Document Number MS-7362	Rev 0A
Date: Friday, January 19, 2007	Sheet 28 of 39	

IEEE 1394 - VIA VT6307 / VT6308P

B07-6308P04-V01
,CHIP CONTROLLER,VIA/VT6308P,CD,PQFP-128pin,PCI 1394A-2000 INTEGRATED HOST CONTROLLER,RoHS COMPLIANCE
B07-0630724-V01
,CHIP CONTROLLER,VIA/VT6307,CD,PQFP-128pin,PCI 1394A OHCI LINK LAYER WITH 2PORT PHY(14*20MM),RoHS COMPLIANCE



	U22	R422	R426
I2C EEPROM	24C02	4.7K ohm	Remove
No EEPROM	Remove	Remove	4.7K ohm

POWER Pin		
Pin	VT6307	VT6308P
84	NC	BJT_CTL
87	NC	REG_FB
88	NC	REQ_OUT
35	VCC3	PWRDET_VCC
39	VCC3	VCC3
49	VCC3	VDD
24	VCC3	VDD
114	VCC3	VDD
33	VCC3	VDD

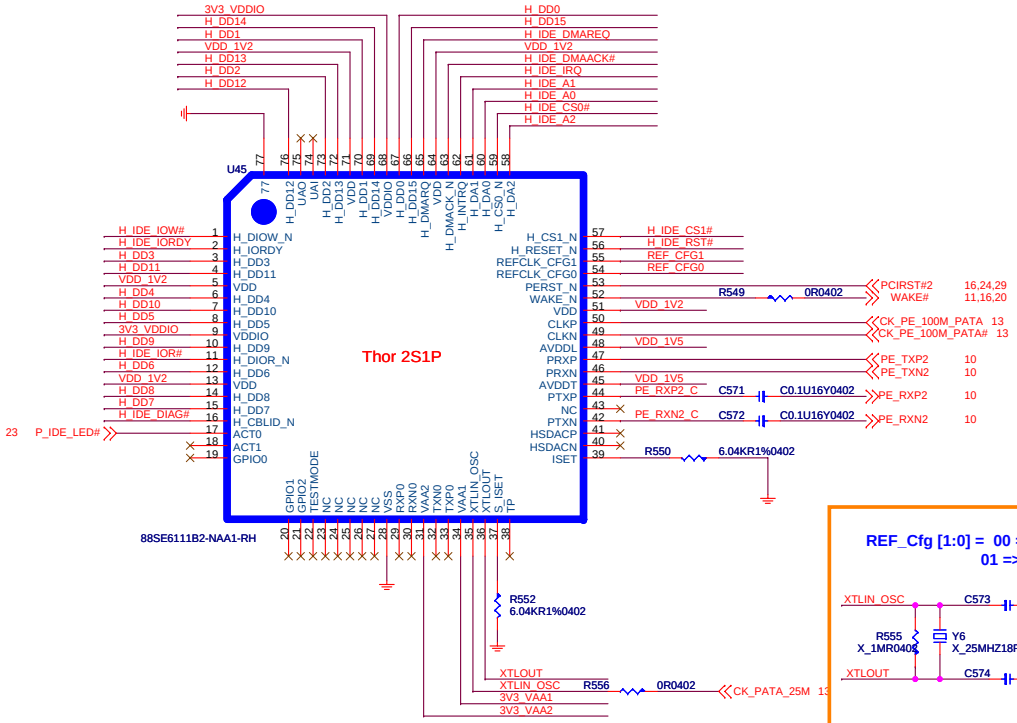
MICRO-START INT'L CO.,LTD.

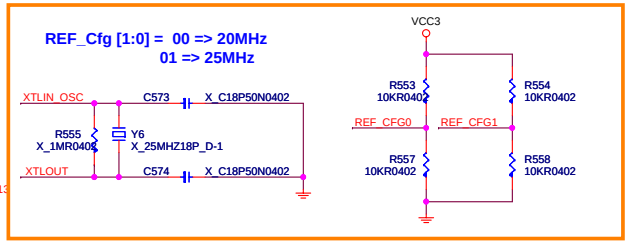
Title: IEEE 1394 - VIA VT6308P

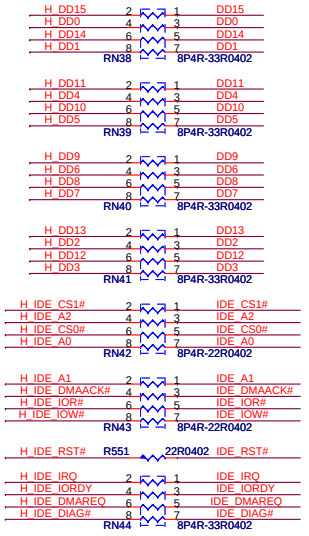
Size | Document Number: MS-7362 | Rev: 0A

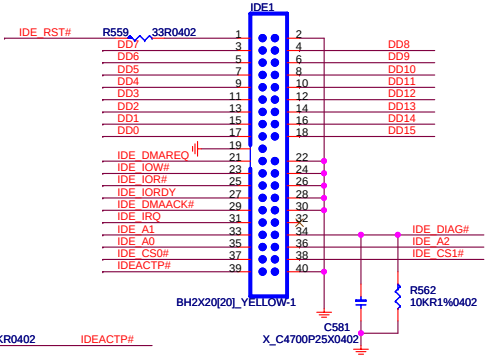
Date: Friday, January 19, 2007 | Sheet 29 of 39

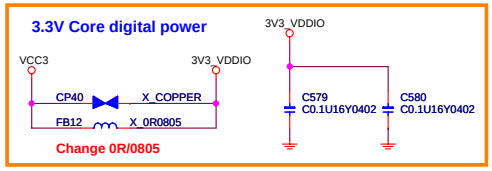
PCI Express To SATA / PATA Bridge



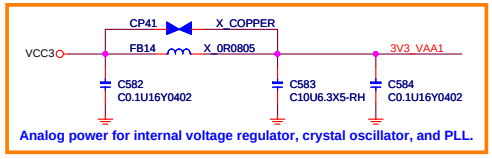


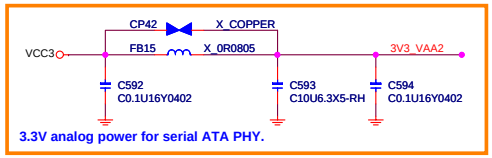


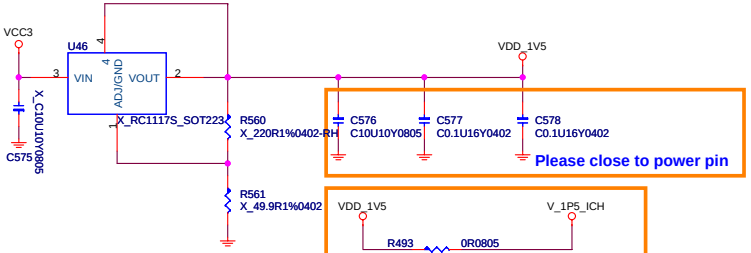


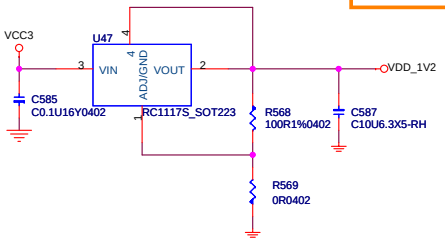


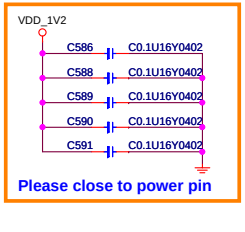
L02-8008074-J07 FOR BEAD

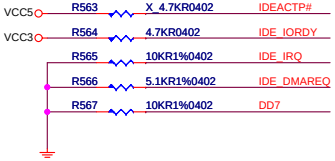










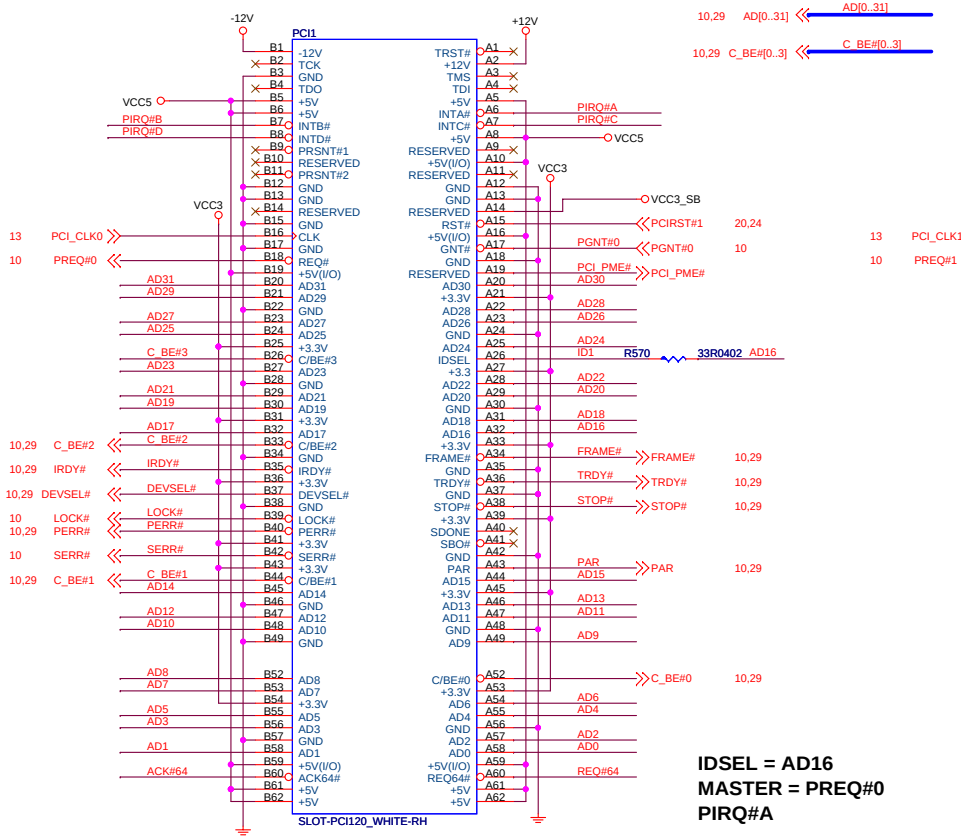


MSI MICRO-START INT'L CO.,LTD.

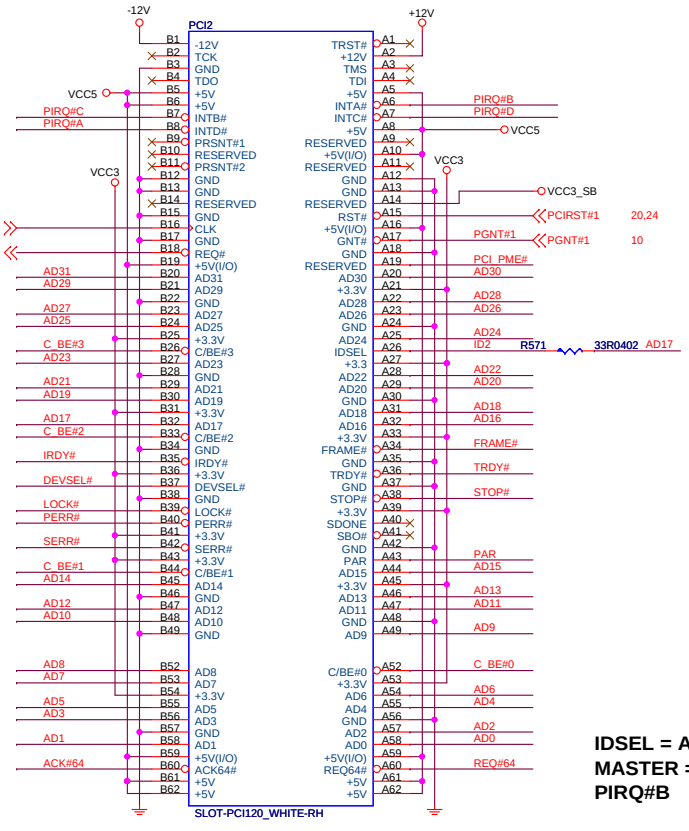
Title	Marvell - 88SE6111	
Size	Document Number MS-7362	Rev 0A
Date: Friday, January 19, 2007	Sheet 30 of 39	

PCI 2.2 Slot 1 & 2

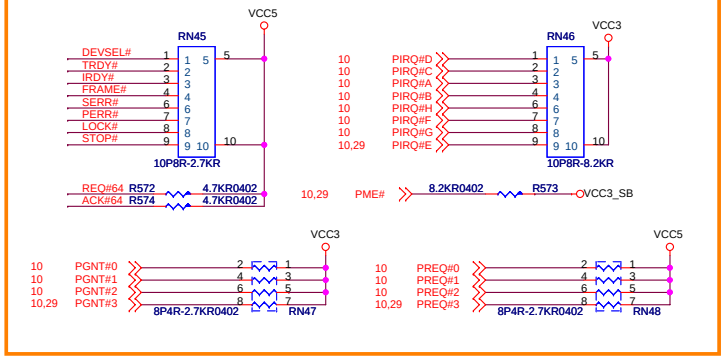
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



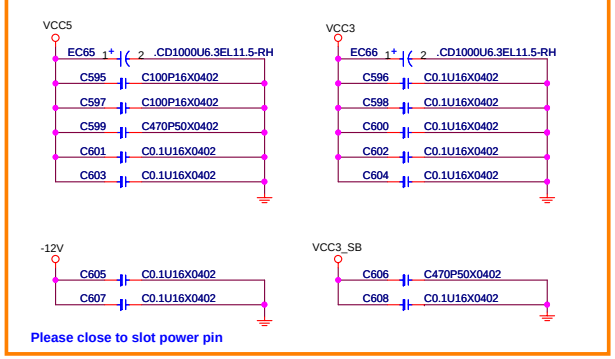
PCI SLOT 2 (PCI VER: 2.2 COMPLY)



PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS



Please close to slot power pin

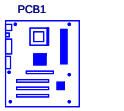
MICRO-START INT'L CO.,LTD.

Title	PCI 2.2 Slot 1 & 2	
Size	Document Number MS-7362	Rev 0A
Date: Friday, January 19, 2007	Sheet 31 of 39	

EMI Solution

MICRO-START INT'L CO.,LTD.		
Title: EMI Solution		
Size	Document Number: MS-7362	Rev: 0A
Date: Friday, January 19, 2007	Sheet 32 of 39	

Manual Part

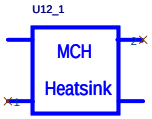


MS-7241-1.0,RED OSP

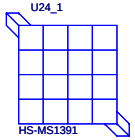
P80-0727810-D05
P80-0727810-Y34

BAT-BCR203ZP-RH

H1X2_BLACK-RH

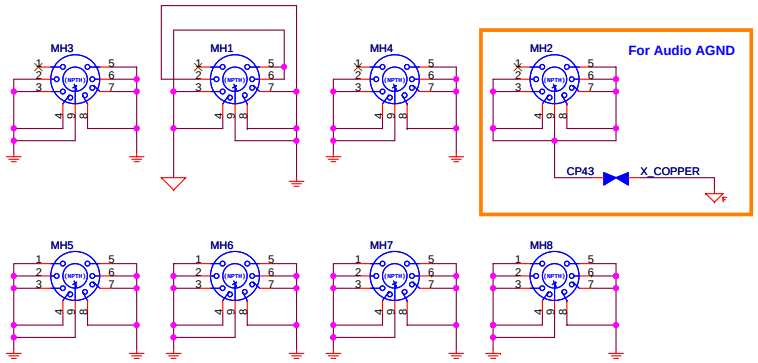


For Intel P965 push pin heat sink

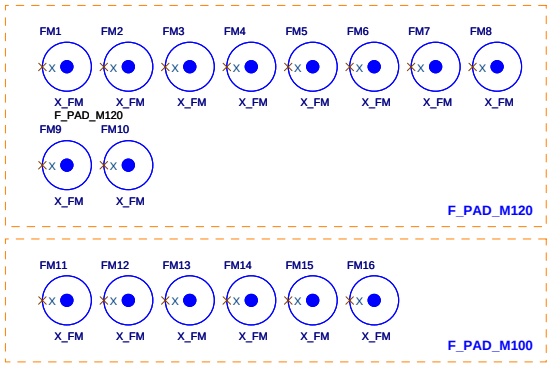


For Intel ICH8 push pin heat sink

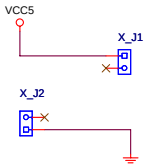
PCB Mounting Holes



Optics Orientation Holes



Simulation



MSI MICRO-START INT'L CO.,LTD.

Title: Manual Part		
Size	Document Number: MS-7362	Rev: 0A
Date: Friday, January 19, 2007	Sheet 33 of 39	

ICH8DH GPIO Pin Definition

GPIO Pin	Type	Default	Function	Power	Multi-Function	Pin-out
GPIO 0	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	Yes	AF9
GPIO 1	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	Yes	AF5
GPIO 2	I/O	GPI	PIRQ#E pull-up to VCC3 with 10K	VCC3		D5
GPIO 3	I/O	GPI	PIRQ#F pull-up to VCC3 with 10K	VCC3		F10
GPIO 4	I/O	GPI	PIRQ#G pull-up to VCC3 with 10K	VCC3		G11
GPIO 5	I/O	GPI	PIRQ#H pull-up to VCC3 with 10K	VCC3		F9
GPIO 6	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	Yes	AE6
GPIO 7	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	Yes	AC8
GPIO 8	I/O	GPI	SIO_PME# connect to SIO,pull_up VCC3_SB with 10k	VCC3_SB	No	AE16
GPIO 9	I/O	MGPIO3	Pull-up to VCC3_SB with 10K directly	VCC3_SB	Yes	AG18
GPIO 10	I/O	GPI	Pull-up to VCC3_SB with 10K directly	VCC3_SB	Yes	AF20
GPIO 11	I/O	SMBALERT#	SMB_ALERT# pull-up to VCC3_SB with 10K	VCC3_SB		AF21
GPIO 12	I/O	GPI	Clear password pull-up to VBT with 1M	VBT	No	AC19
GPIO 13	I/O	GPI	Pull-up to VCC3_SB with 10K directly	VCC3_SB	No	AF18
GPIO 14	I/O	GPI	Pull-up to VCC3_SB with 10K directly	VCC3_SB	Yes	AH24
GPIO 15	I/O	GPO	NC	VCC3_SB	No	AE21
GPIO 16	I/O	GPO	SIO HWM_INT,pull_up VCC3 with 10K(change to GPI)		No	AE11
GPIO 17	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AC7
GPIO 18	I/O	GPO	NC		No	AC11
GPIO 19	I/O	GPI	Pull-up to VCC3 with 10K	VCC3		AD8
GPIO 20	I/O	GPO	NC		No	AG8
GPIO 21	I/O	GPI	Pull-up to VCC3 with 10K	VCC3		AB11
GPIO 22	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	Yes	AE7
GPIO 23	I/O	LDRQ1#	LDRQ_1# pull_up VCC3 with 10K	VCC3	Yes	C3
GPIO 24	I/O	GPO	NC		Yes	AG23
GPIO 25	I/O	GPO	NC	3.3V_SB	No	AH17
GPIO 26	I/O	GPO	S4 STATE			AH25
GPIO 27	I/O	GPO	NC	3.3V_SB		AD20
GPIO 28	I/O	GPO	NC			AD15
GPIO 29	I/O	OC5#	OC#3 connect to USB connector	3.3V_SB		AE15
GPIO 30	I/O	OC6#	OC#4 connect to USB connector	3.3V_SB		AG13
GPIO 31	I/O	OC7#	OC#4 connect to USB connector	3.3V_SB		AF14
GPIO 32	I/O	GPO	SIO_SMI# connect to SIO,pull up VCC3 with 10k	VCC3	No	AH7
GPIO 33	I/O	GPO	NC		No	AG7
GPIO 34	I/O	GPO	NC		No	AG12
GPIO 35	I/O	GPO	NC			AD12
GPIO 36	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AF8
GPIO 37	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AD9
GPIO 38	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AH6
GPIO 39	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AC10
GPIO 40	I/O	OC1#	OC#1 connect to USB connector	VCC3		AH14
GPIO 41	I/O	OC2#	OC#2 connect to USB connector	VCC3		AG14
GPIO 42	I/O	OC3#	OC#2 connect to USB connector	VCC3		AG15
GPIO 43	I/O	OC4#	OC#3 connect to USB connector	VCC3		AH15
GPIO 44	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AF7
GPIO 45	I/O	CPUPWRGD	H_PWRGD connect to CPU	VTT_OUT		AF25
GPIO 46	I/O	REQ1#	REQ1 pull-up to VCC5 with 10K	VCC5	Yes	C16
GPIO 47	I/O	GNT1#	GNT1#		Yes	A15
GPIO 48	I/O	REQ2#	REQ2 pull-up to VCC5 with 10K	VCC5	Yes	B16
GPIO 49	I/O	GNT2#	GNT2#		Yes	D17
GPIO 50	I/O	REQ3#	REQ3 pull-up to VCC5 with 10K	VCC5	Yes	A9
GPIO 51	I/O	GNT3#	GNT3#		Yes	B9

PCI Configuration

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK	PCI Reset
VIA VT6308P	PIRQ#E	PREQ#3 PGNT#3	AD23	1394_PCLK	PCIRST#2
PCI slot 1	PIRQ#A	PREQ#0 PGNT#0	AD16	PCI_CLK0	PCIRST#1
PCI slot 2	PIRQ#B	PREQ#1 PGNT#1	AD17	PCI_CLK1	PCIRST#1

DDRII DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	0A0H	P_DDR0_A / N_DDR0_A P_DDR1_A / N_DDR1_A P_DDR2_A / N_DDR2_A
DIMM 2	0A2H	P_DDR3_A / N_DDR3_A P_DDR4_A / N_DDR4_A P_DDR5_A / N_DDR5_A
DIMM 3	0A4H	P_DDR0_B / N_DDR0_B P_DDR1_B / N_DDR1_B P_DDR2_B / N_DDR2_B
DIMM 4	0A6H	P_DDR3_B / N_DDR3_B P_DDR4_B / N_DDR4_B P_DDR5_B / N_DDR5_B

SMBus Distribution

SMBus	Power	Load
SMBDATA_MAIN SMBCLK_MAIN	VCC3_SB	ICH8 , Clock Gen , Super I/O , DDR II , PCI Express x16 , PCI Express x1 , MS7 , PWM

Jumper Setting

JBAT1	(1-2) Normal	(2-3) Clear

PCI Reset Device

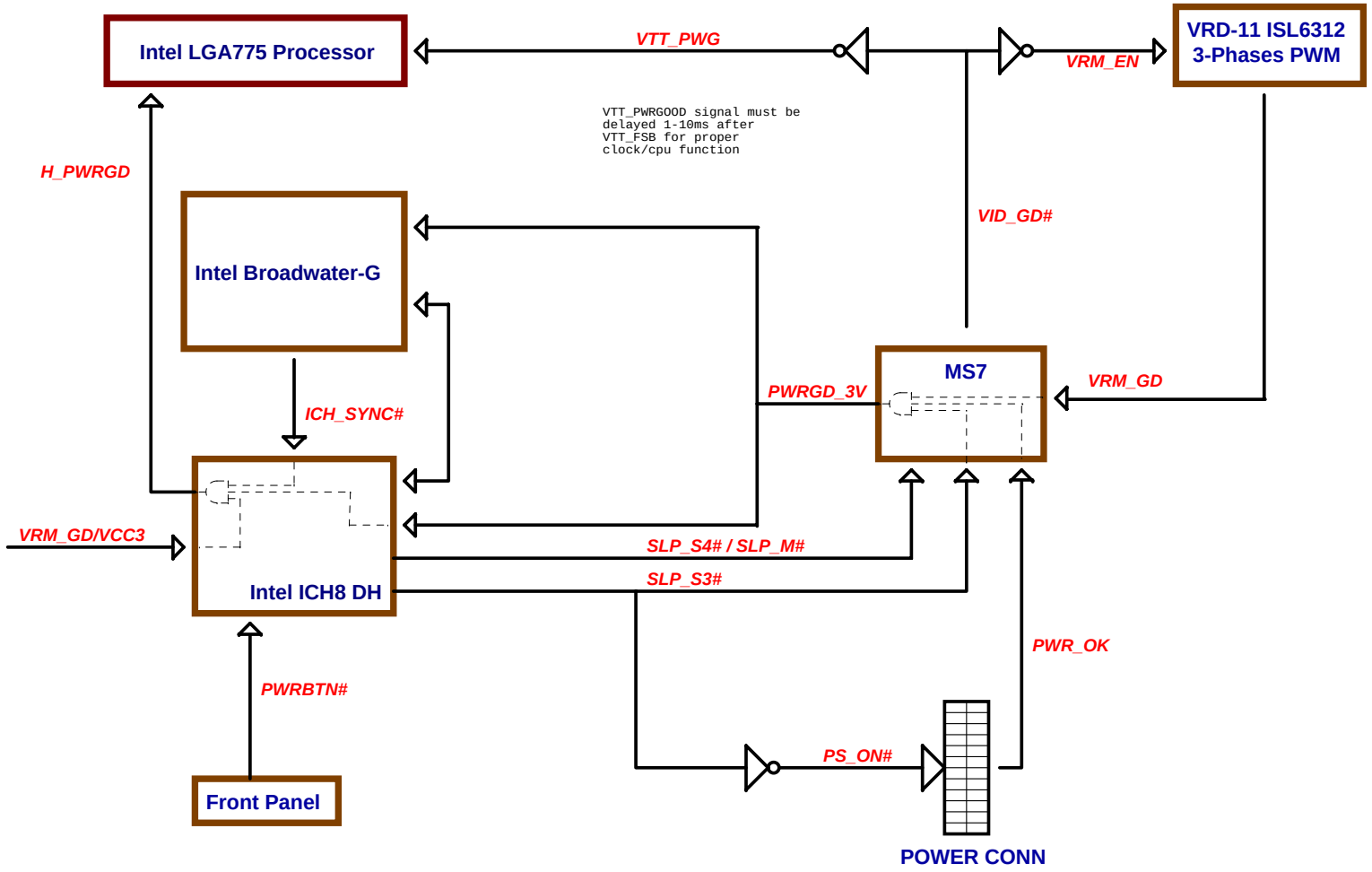
Signal	Device
PLTRST#	MS7 , NB
PCIRST_ICH8#	MS7
PCIRST#1	PCI1 , PCI2 , PCIE x16 , PCIE x1
PCIRST#2	VT6308P , 88SE6111
PCIRST#3	TPM , Super I/O

MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: GPIO & Jumper Setting

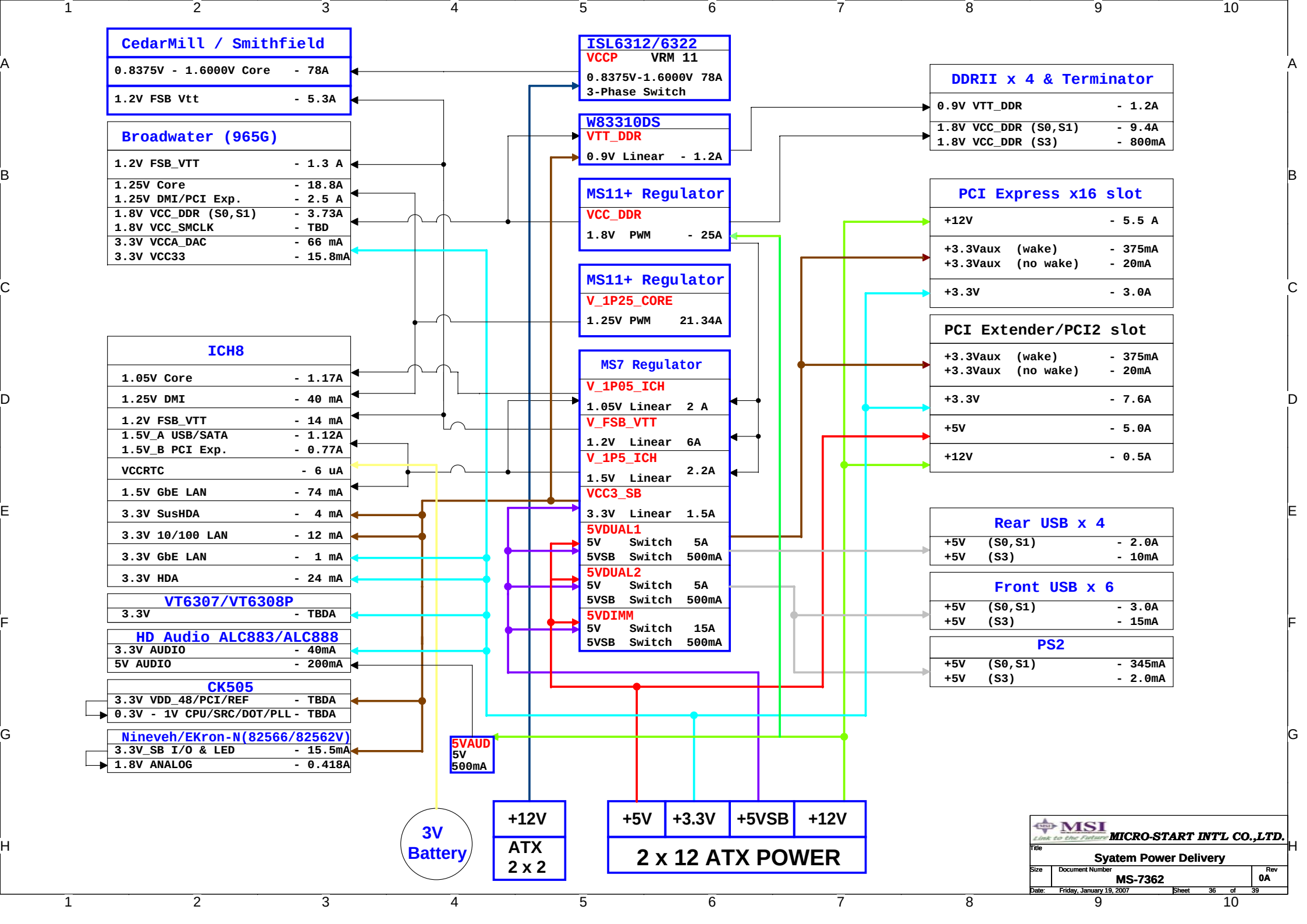
Size | Document Number: MS-7362 | Rev: 0A

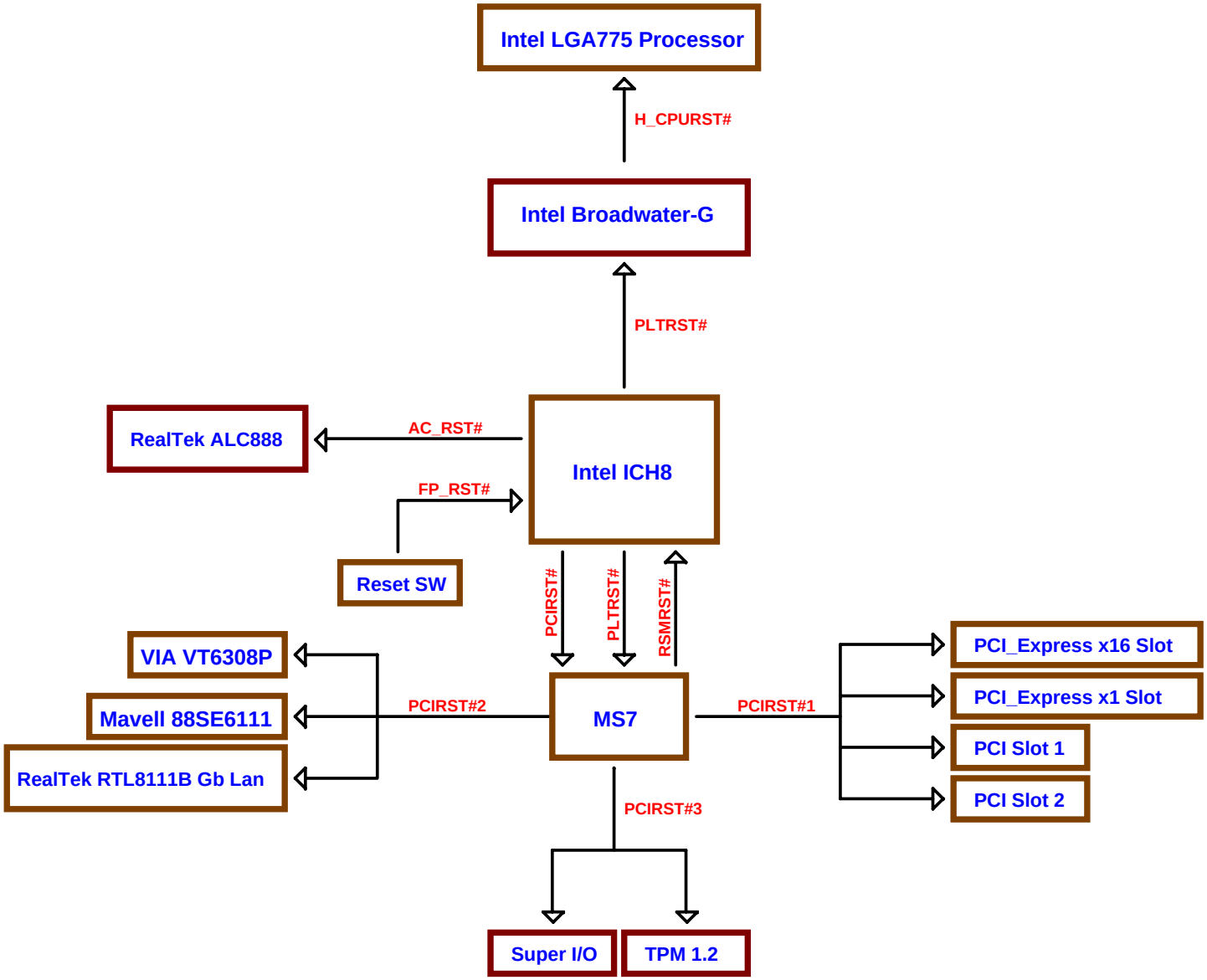
Date: Friday, January 19, 2007 | Sheet 34 of 39



MICRO-START INT'L CO.,LTD.

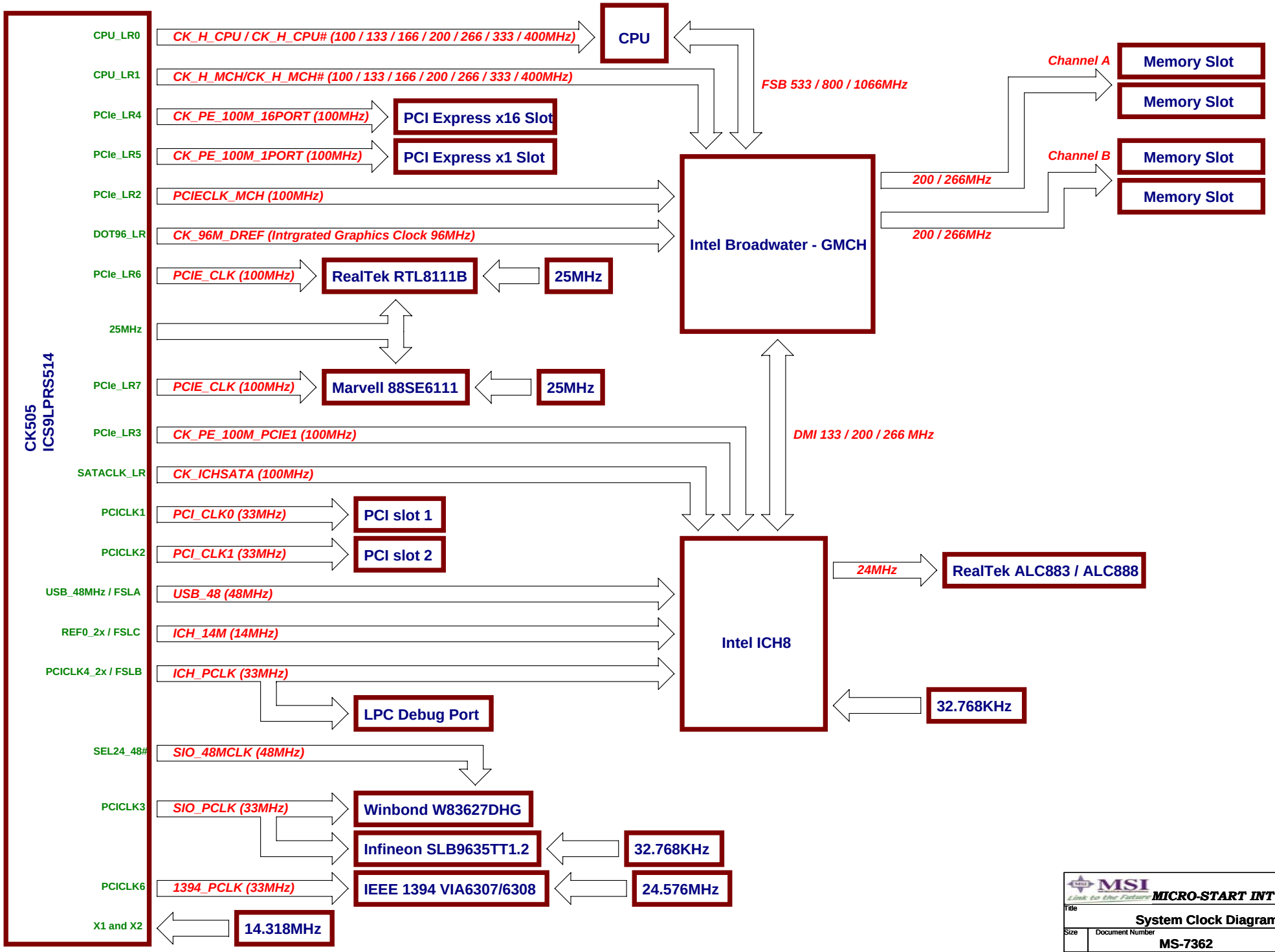
Title	Syatem Power OK Map	
Size	Document Number: MS-7362	Rev: 0A
Date: Friday, January 19, 2007	Sheet 35 of 39	


CedarMill / Smithfield
0.8375V - 1.6000V Core - 78A
1.2V FSB Vtt - 5.3A
Broadwater (965G)
1.2V FSB_VTT - 1.3 A
1.25V Core - 18.8A
1.25V DMI/PCI Exp. - 2.5 A
1.8V VCC_DDR (S0,S1) - 3.73A
1.8V VCC_SMCLK - TBD
3.3V VCCA_DAC - 66 mA
3.3V VCC33 - 15.8mA
ICH8
1.05V Core - 1.17A
1.25V DMI - 40 mA
1.2V FSB_VTT - 14 mA
1.5V_A USB/SATA - 1.12A
1.5V_B PCI Exp. - 0.77A
VCCRTC - 6 uA
1.5V GbE LAN - 74 mA
3.3V SusHDA - 4 mA
3.3V 10/100 LAN - 12 mA
3.3V GbE LAN - 1 mA
3.3V HDA - 24 mA
VT6307/VT6308P
3.3V - TBDA
HD Audio ALC883/ALC888
3.3V AUDIO - 40mA
5V AUDIO - 200mA
CK505
3.3V VDD_48/PCI/REF - TBDA
0.3V - 1V CPU/SRC/DOT/PLL - TBDA
Nineveh/EKron-N(82566/82562V)
3.3V_SB I/O & LED - 15.5mA
1.8V ANALOG - 0.418A
ISL6312/6322
VCCP VRM 11
0.8375V-1.6000V 78A
3-Phase Switch
W83310DS
VTT_DDR
0.9V Linear - 1.2A
MS11+ Regulator
VCC_DDR
1.8V PWM - 25A
MS11+ Regulator
V_1P25_CORE
1.25V PWM 21.34A
MS7 Regulator
V_1P05_ICH
1.05V Linear 2 A
V_FSB_VTT
1.2V Linear 6A
V_1P5_ICH
1.5V Linear 2.2A
VCC3_SB
3.3V Linear 1.5A
5VDUAL1
5V Switch 5A
5VSB Switch 500mA
5VDUAL2
5V Switch 5A
5VSB Switch 500mA
5VDIMM
5V Switch 15A
5VSB Switch 500mA
5VAUD
5V
500mA
DDRII x 4 & Terminator
0.9V VTT_DDR - 1.2A
1.8V VCC_DDR (S0,S1) - 9.4A
1.8V VCC_DDR (S3) - 800mA
PCI Express x16 slot
+12V - 5.5 A
+3.3Vaux (wake) - 375mA
+3.3Vaux (no wake) - 20mA
+3.3V - 3.0A
PCI Extender/PCI2 slot
+3.3Vaux (wake) - 375mA
+3.3Vaux (no wake) - 20mA
+3.3V - 7.6A
+5V - 5.0A
+12V - 0.5A
Rear USB x 4
+5V (S0,S1) - 2.0A
+5V (S3) - 10mA
Front USB x 6
+5V (S0,S1) - 3.0A
+5V (S3) - 15mA
PS2
+5V (S0,S1) - 345mA
+5V (S3) - 2.0mA
3V Battery
+12V
ATX 2 x 2
+5V
+3.3V
+5VSB
+12V
2 x 12 ATX POWER
MSI
MICRO-START INT'L CO.,LTD.
Title
Syatem Power Delivery
Size
Document Number
MS-7362
Rev
0A
Date: Friday, January 19, 2007
Sheet 36 of 39



MICRO-START INT'L CO.,LTD.

Title: System Reset Diagram		
Size	Document Number: MS-7362	Rev: 0A
Date: Friday, January 19, 2007	Sheet 37 of 39	



MICRO-START INT'L CO.,LTD.

Title: System Clock Diagram

Size | Document Number: MS-7362 | Rev: 0A

Date: Friday, January 19, 2007 | Sheet 38 of 39

2006-12-29

1. Create new schematic for 7362-0A

2007-01-02

1. New schematic net-in

2007-01-03

1. Placement and Layout

MSI Link to the Future **MICRO-START INT'L CO.,LTD.**

Title: **Project History**

Size | Document Number: **MS-7362** | Rev: **0A**

Date: Friday, January 19, 2007 Sheet 39 of 39