MS-7358 uATX Version: 1.0

CPU: Intel Pentium 4, Pentium D, Core2 Duo, Wolfdale, Kentsfield and Yorkfield processors in LGA775 Package.

System Chipset:

Intel Bearlake - Q35/G33 North Bridge
Intel ICH9 (DO/DH South Bridge)

On Board Device:

CLOCK Gen ICS 9LPRS906
LPC Super I/O -- Fintek F71882F
LPC TPM -- SLB9635

LAN -- INTEL NINEVEH/EKRON
HD Audio Codec -- ALC888
1394 Controller -- VT6308 (2-port)
PCIE to PATA Bridge -- Marvel 88SE6111

Main Memory:

Dual-channel DDR-II * 4

Expansion Slots:

PCI EXPRESS X16 SLOT *1
PCI EXPRESS X1 SLOT *1
PCI SLOT * 2

PWM: Intersil ISL6322 (4 Phases) w/ ISL6612 driver

Configration and BOM match up

Option	Function	Orcad Configure	BOM
STD	Bearlake-Q33/ICH9DO	cfg-7358-STD	

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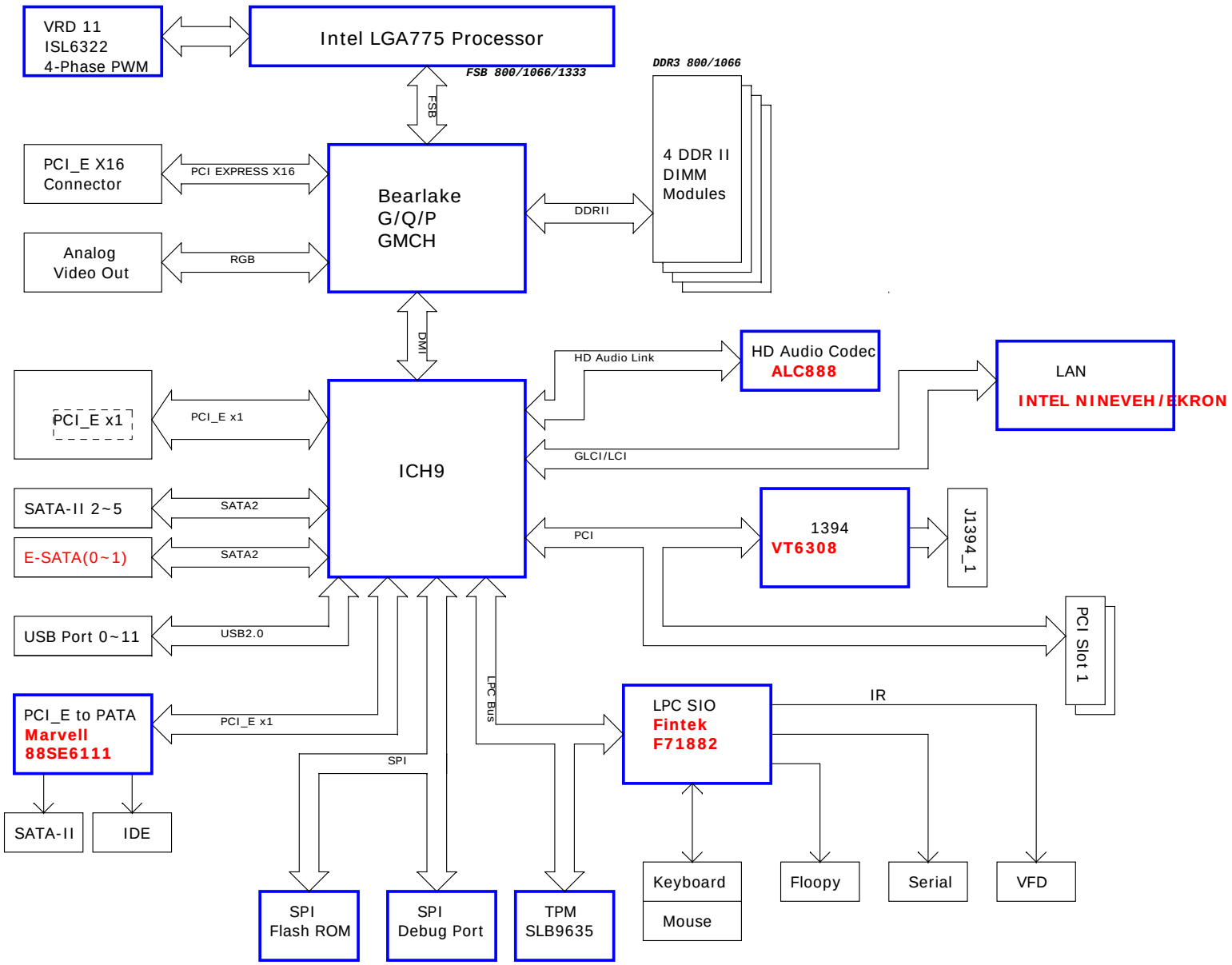
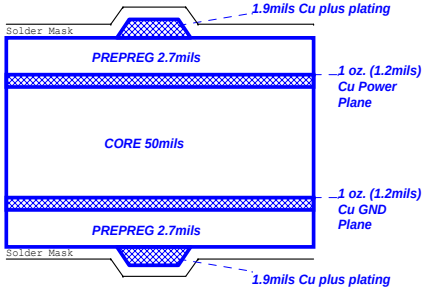
Block Diagram



Board Stack-up

(1080 Prepreg Considerations)



Single End 50ohm Top/Bottom : 4mils
USB2.0 - 90ohm : 15/4.5/7.5/4.5/15
SATA - 95ohm : 15/4/8/4/15
LAN - 100ohm : 15/4/8/4/15
PCIE - 95ohm : 15/4/8/4/15
IEEE1394 - 110ohm : 15/4/9/4/15
IDE : 15/4/8/4/15

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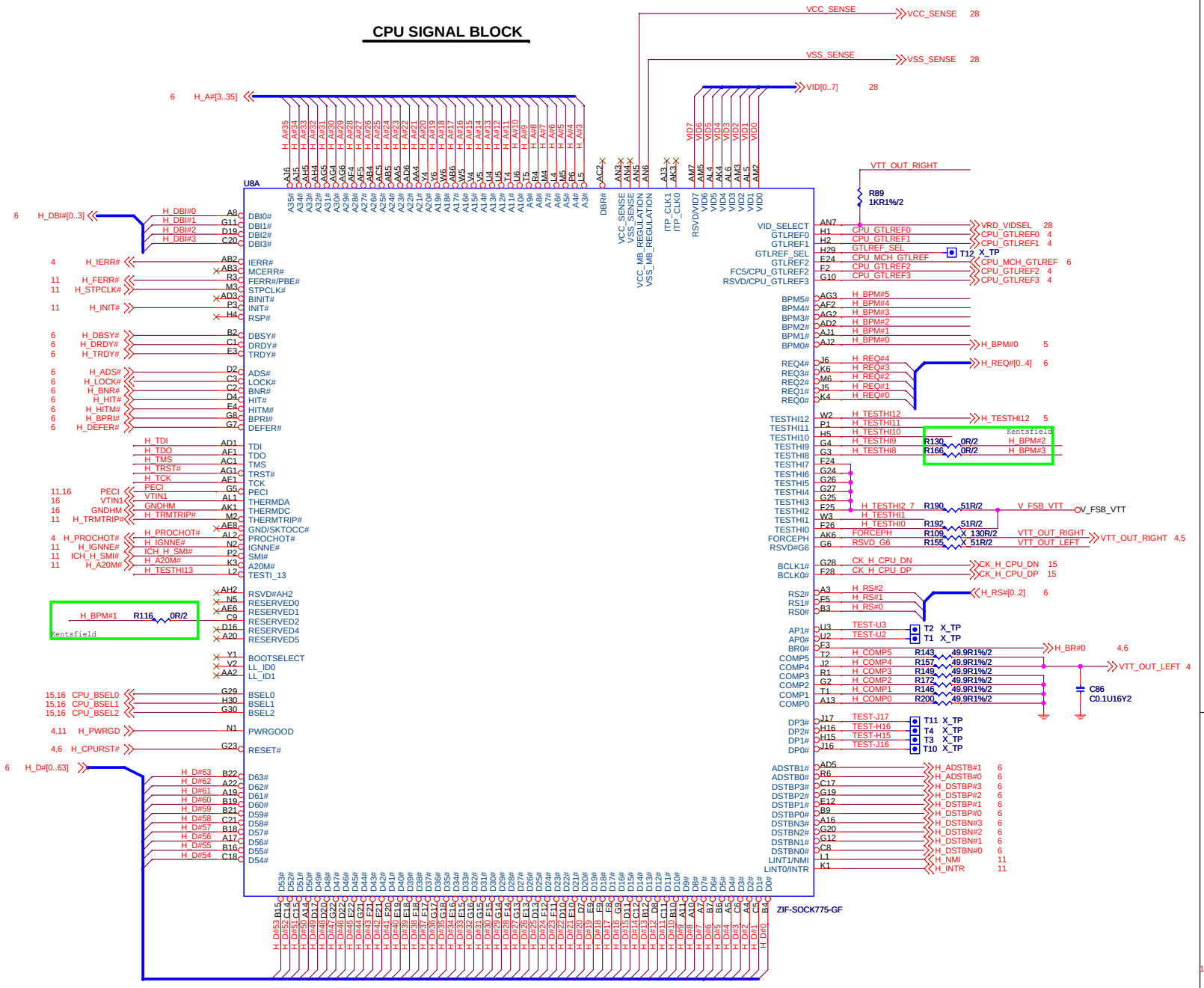
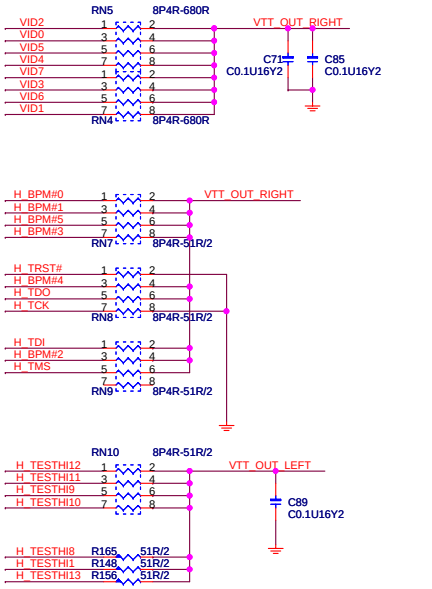
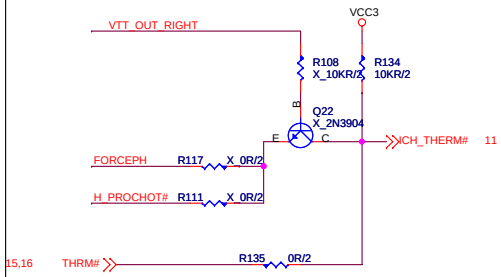
CPU SIGNAL BLOCK



PULL HIGHT PULL DOWN



Thermal TRIP



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Size: Custom	Document Description: LGA775 - Signal	Rev: 0A
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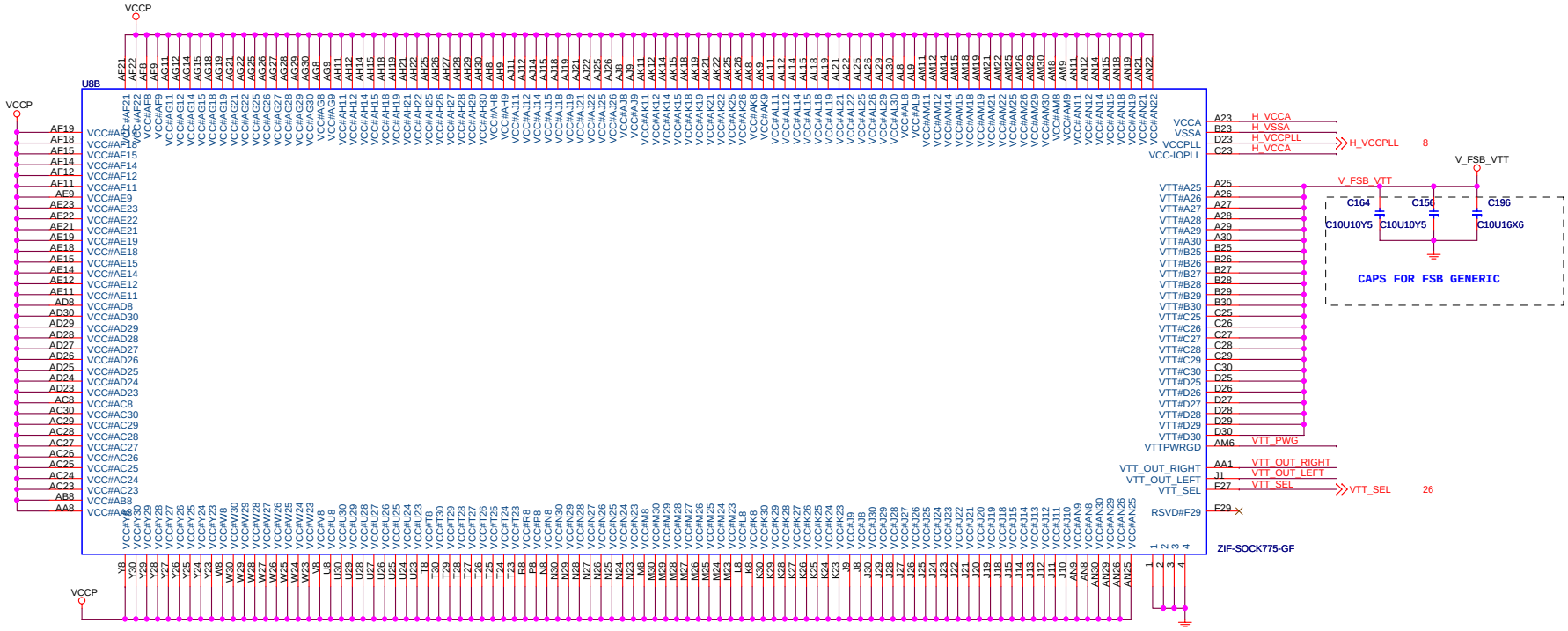
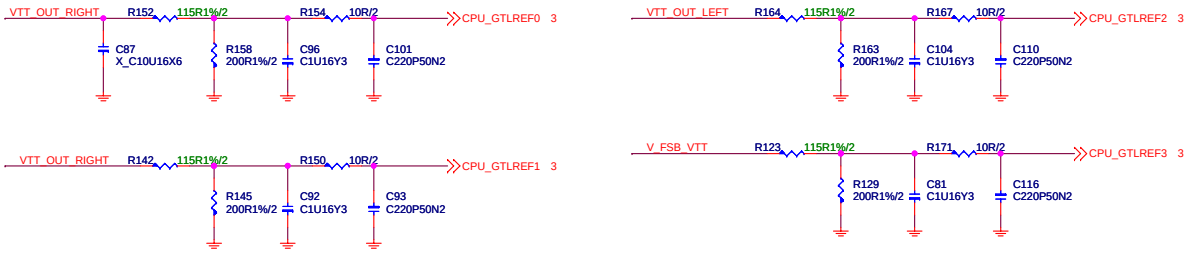
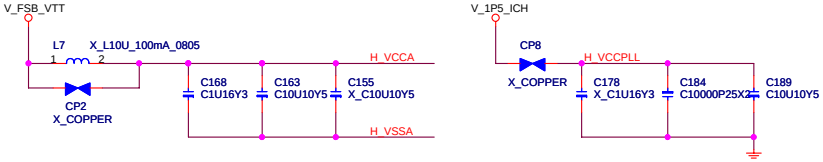


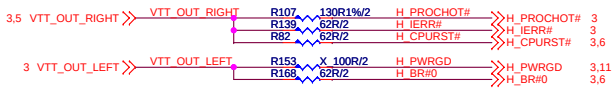
*GTLREF VOLTAGE SHOULD BE
0.67 * VTT = 0.8V (At VTT=1.2V)



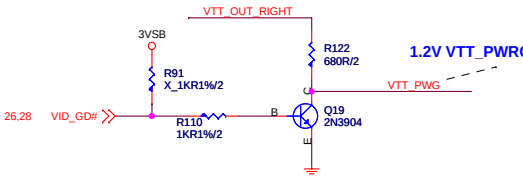
*PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET
*TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12MILS



PLACE AT CPU END OF ROUTE



VTT_PWRGOOD



VTT_PWG SPEC :
High > 0.9V
Low < 0.3V
Trise < 150ns

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Custom	LGA775 - Power	0A

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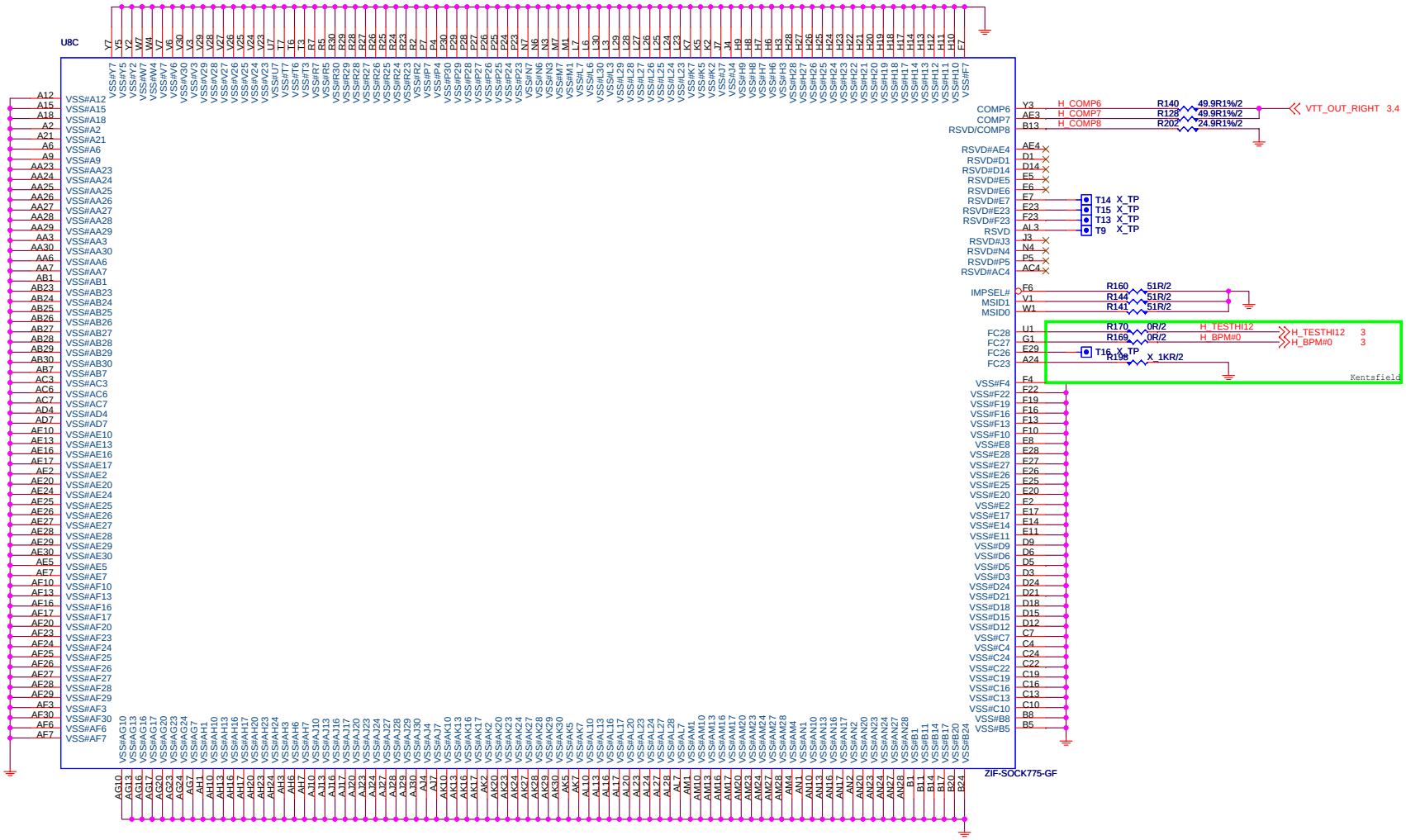

MICRO-STAR INT'L CO.,LTD	
MS-7358	
Size: Custom	Document Description: LGA775 - GND
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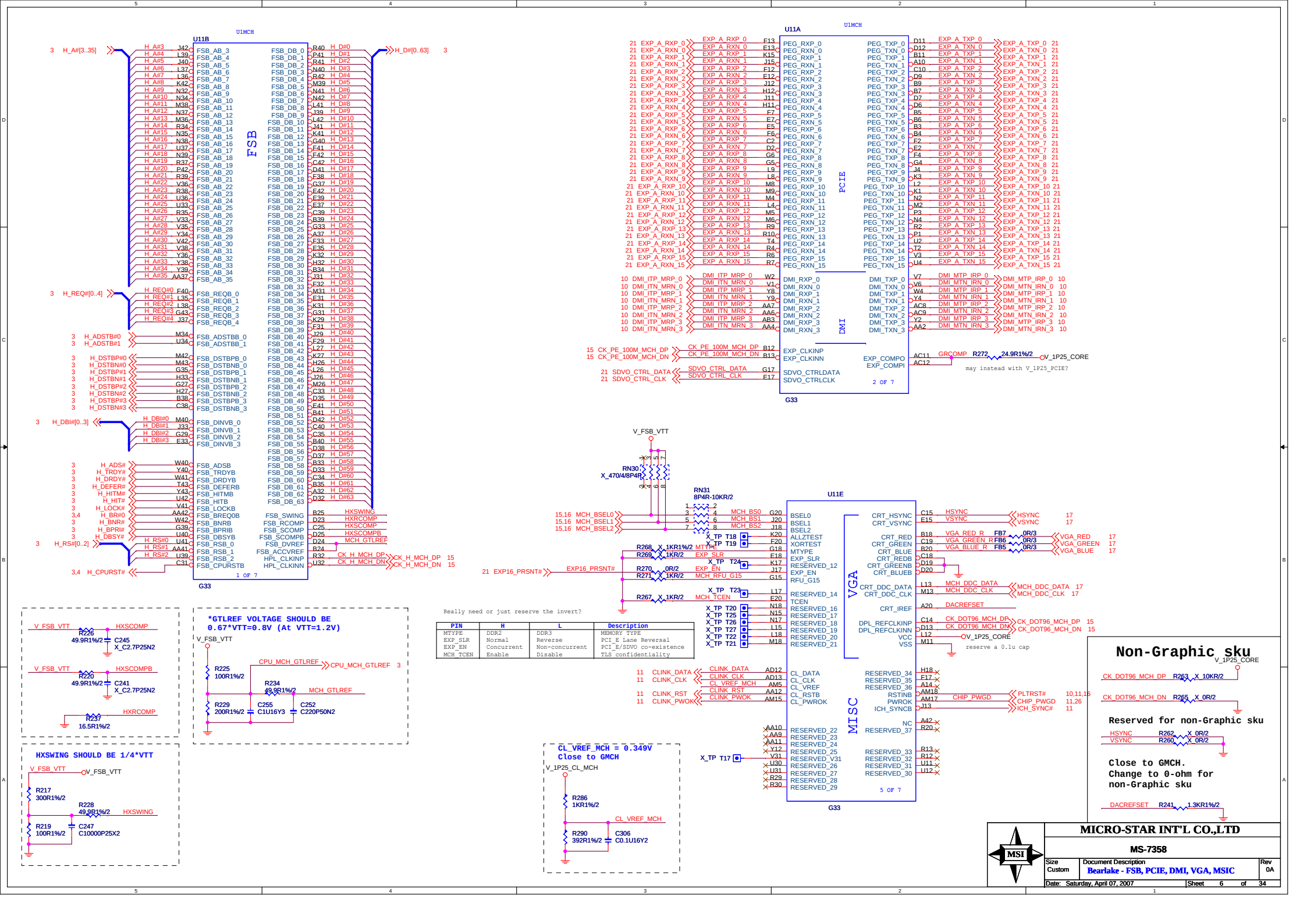
U1MCH
U11B
FSB
H_A#[3..35]
H_REQ#[0..4]
H_ADSTB#0
H_ADSTB#1
H_DSTBP#0
H_DSTBN#0
H_DSTBP#1
H_DSTBN#1
H_DSTBP#2
H_DSTBN#2
H_DSTBP#3
H_DSTBN#3
H_DBI#[0..3]
H_ADS#
H_TRDY#
H_DRDY#
H_DEFER#
H_HITM#
H_HIT#
H_LOCK#
H_BR#0
H_BNR#
H_BPRI#
H_DBSY#
H_RS#[0..2]
H_CPURST#
H_D#[0..63]
G33
1 OF 7
U11A
PCIE
DMI
EXP_COMPO
EXP_COMPI
GRCOMP
R272
24.9R1%/2
V_1P25_CORE
may instead with V_1P25_PCIE?
2 OF 7
G33
V_FSB_VTT
RN30
X_470/4/8P4R
RN31
8P4R-10KR/2
U11E
VGA
MISC
5 OF 7
G33
Really need or just reserve the invert?
PIN
H
L
Description
MTYPE
DDR2
DDR3
MEMORY TYPE
EXP_SLR
Normal
Reverse
PCI_E Lane Reversal
EXP_EN
Concurrent
Non-concurrent
PCI_E/SDVO co-existence
MCH_TCEN
Enable
Disable
TLS confidentiality
V_FSB_VTT
R226
49.9R1%/2
C245
X_C2.7P25N2
HXSCOMP
R229
49.9R1%/2
C241
X_C2.7P25N2
HXSCOMPB
R237
16.5R1%/2
HXRCOMP
*GTLREF VOLTAGE SHOULD BE
0.67*VTT=0.8V (At VTT=1.2V)
R225
100R1%/2
R234
49.9R1%/2
R229
200R1%/2
C255
C1U16Y3
C252
C220P50N2
CPU_MCH_GTLREF
MCH_GTLREF
HXSWING SHOULD BE 1/4*VTT
R217
300R1%/2
R228
49.9R1%/2
HXSWING
R219
100R1%/2
C247
C10000P25X2
CL_VREF_MCH = 0.349V
Close to GMCH
V_1P25_CL_MCH
R286
1KR1%/2
CL_VREF_MCH
R290
392R1%/2
C306
C0.1U16Y2
Non-Graphic sku
V_1P25_CORE
R263
X_10KR/2
R265
X_0R/2
Reserved for non-Graphic sku
R262
X_0R/2
R260
X_0R/2
Close to GMCH.
Change to 0-ohm for
non-Graphic sku
R241
1.3KR1%/2
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MS-7358
Size
Custom
Document Description
Bearlake - FSB, PCIE, DMI, VGA, MSIC
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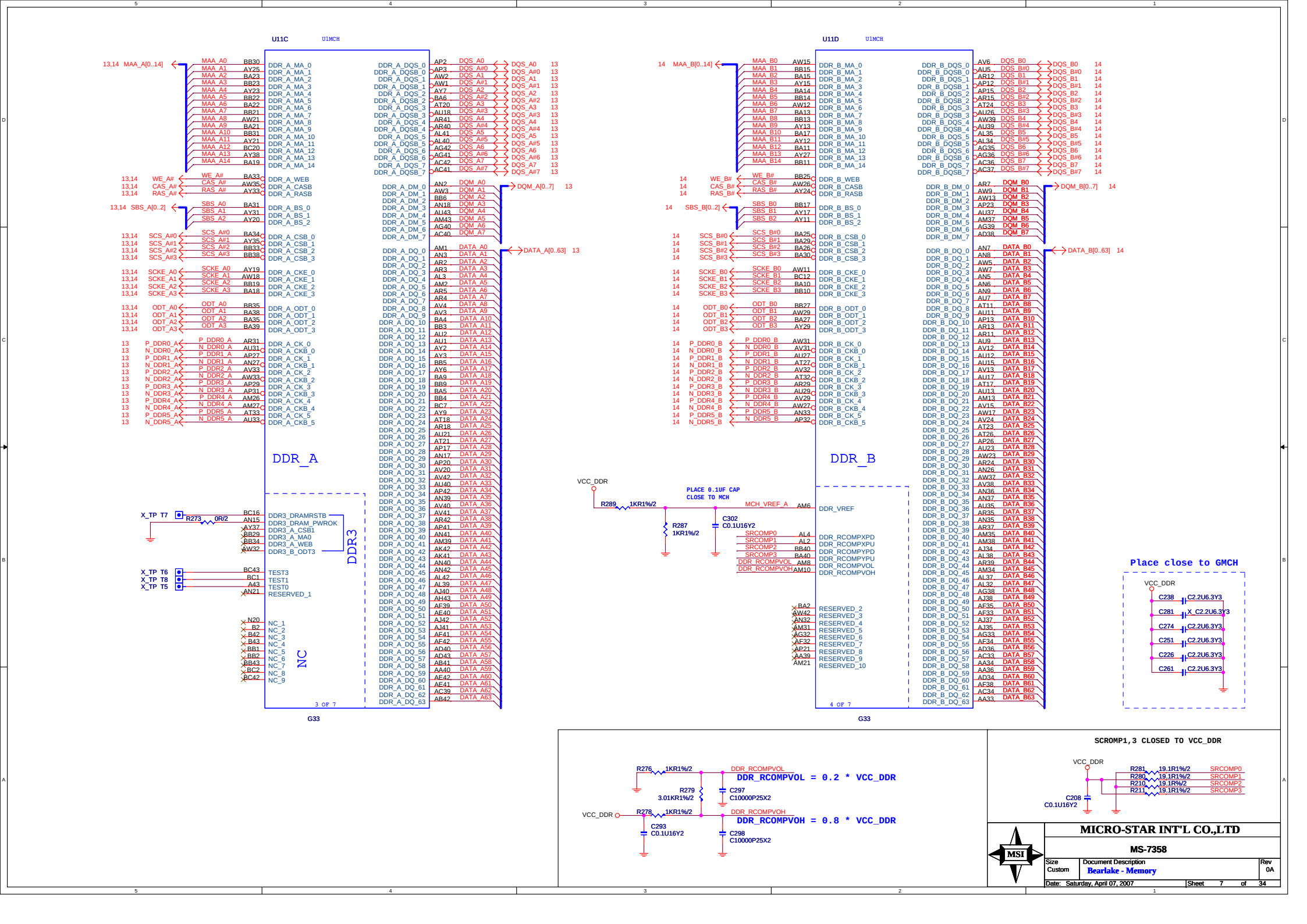
U11C
U1MCH
DDR_A
DDR3
NC
3 OF 7
G33
U11D
U1MCH
DDR_B
DDR_VREF
4 OF 7
G33
PLACE 0.1UF CAP
CLOSE TO MCH
VCC_DDR
R289 1KR1%/2
R287 1KR1%/2
C302 C0.1U16Y2
MCH_VREF_A
SRCOMP0
SRCOMP1
SRCOMP2
SRCOMP3
DDR_RCOMPVOL
DDR_RCOMPVOH
Place close to GMCH
C238 C2.2U6.3Y3
C281 X_C2.2U6.3Y3
C274 C2.2U6.3Y3
C251 C2.2U6.3Y3
C226 C2.2U6.3Y3
C261 C2.2U6.3Y3
SCROMP1,3 CLOSED TO VCC_DDR
R281 19.1R1%/2
R280 19.1R1%/2
R210 19.1R%/2
R211 19.1R1%/2
C208 C0.1U16Y2
R276 1KR1%/2
R279 3.01KR1%/2
C297 C10000P25X2
R278 1KR1%/2
C293 C0.1U16Y2
C298 C10000P25X2
DDR_RCOMPVOL = 0.2 * VCC_DDR
DDR_RCOMPVOH = 0.8 * VCC_DDR
MICRO-STAR INT'L CO.,LTD
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Size Custom
Document Description Bearlake - Memory
Rev 0A
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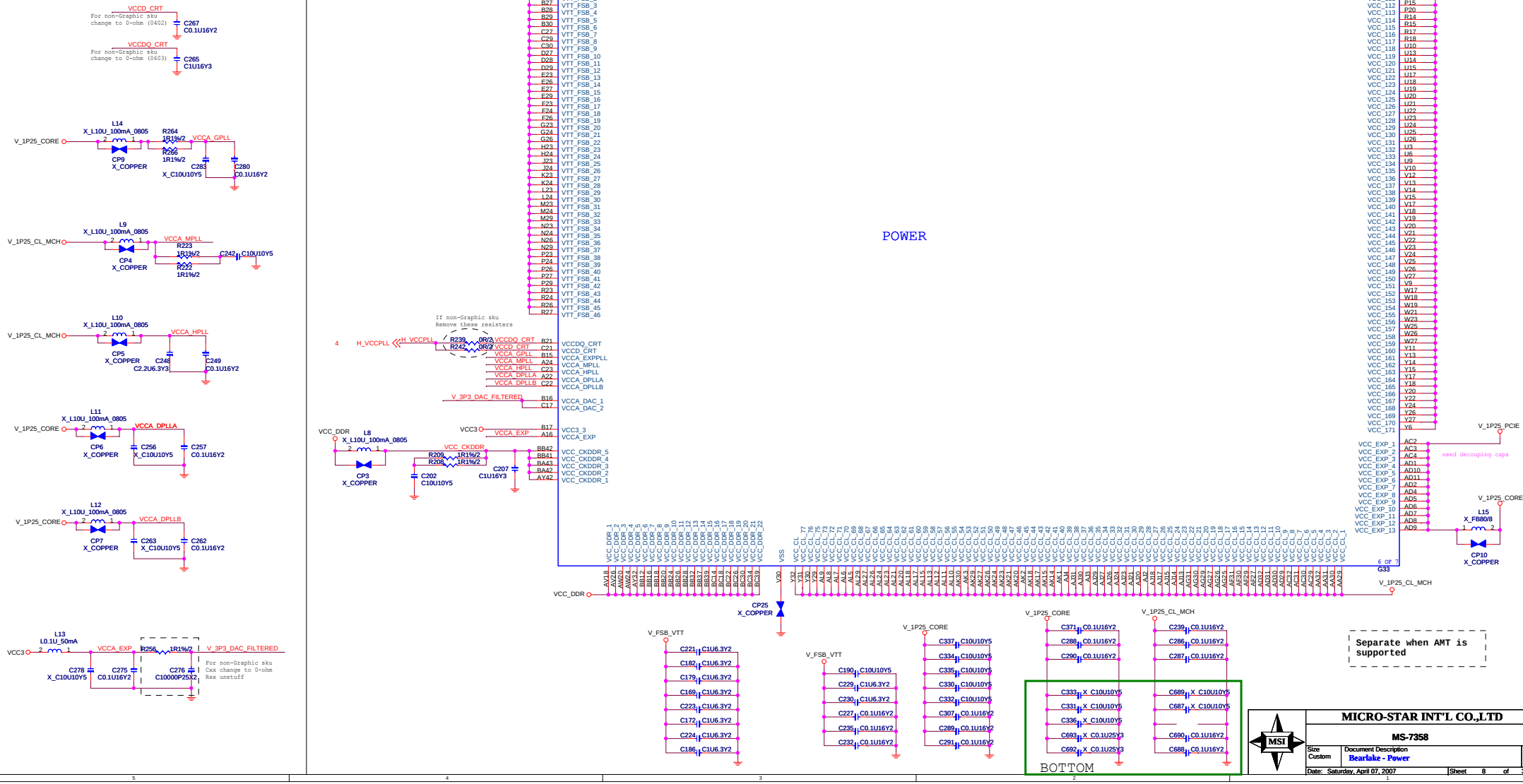
NB POWER



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Size: Custom	Document Description: Bearlake - Power
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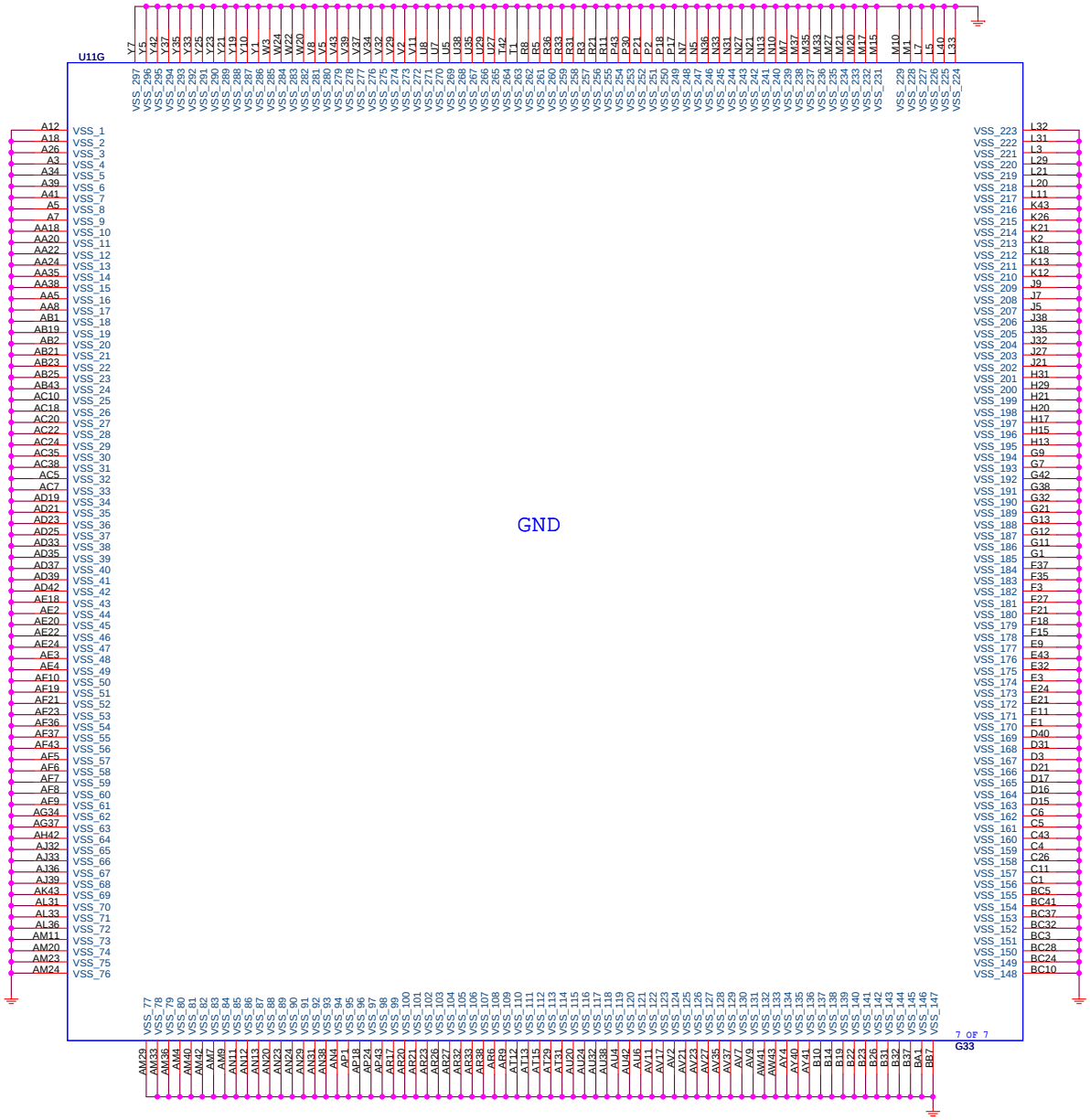

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Size: Custom	Document Description: Bearlake - GND	Rev: 0A
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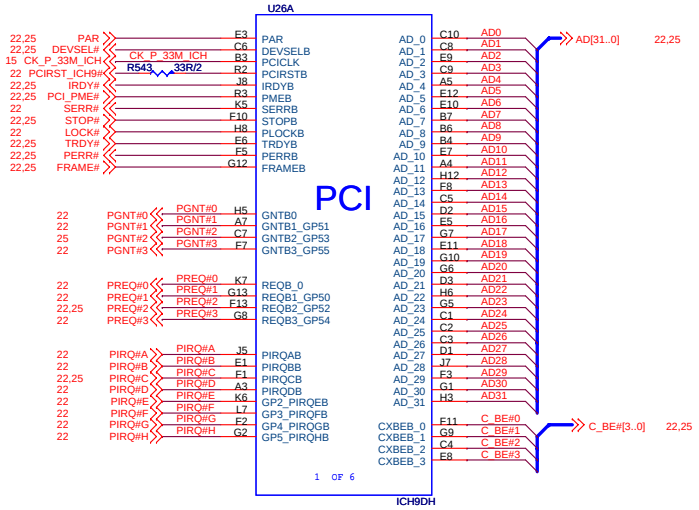
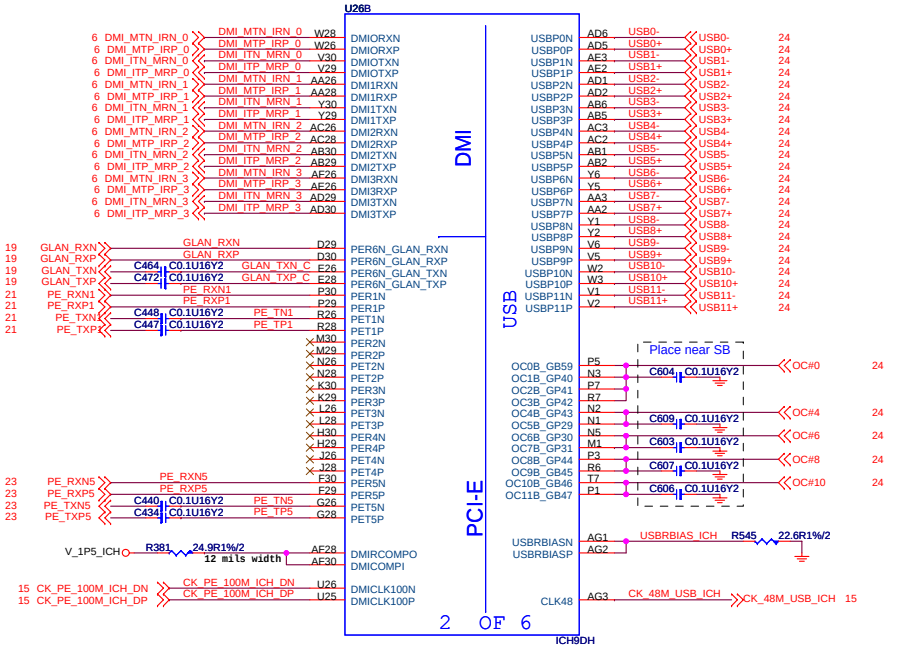
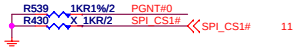


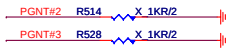


SB STRAPPING RESISTOR



BOOT SELECT STRAPS		
BOOT DEVICE	GNT#0	SPI_CS1#
FWH	1	1
SPI	0	1
PCI	1	0

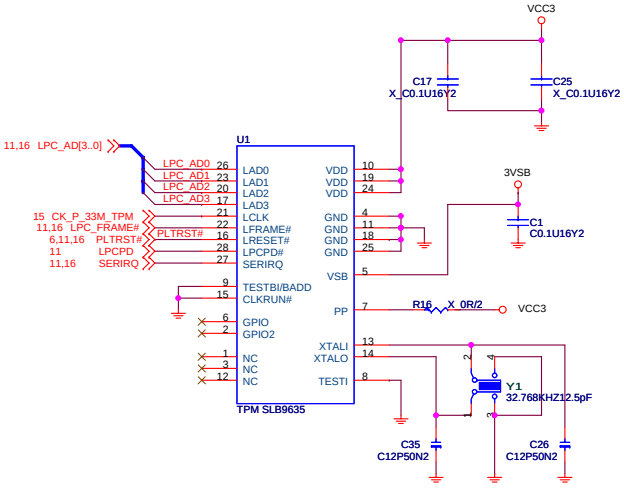
PGNT#[3:0]Internal Pull-up



SIGNAL	H	L	DES.
GNT3	DIS	EN	A16 OVERIDE
GNT2	N/A	SET BIT	PCIE PORT CONFIG 2 BIT 0 (5-6)

HDA_SDOUT/HDA_SYNC strap PCI_E port configuration bit[1:0].Internal weak pull down.
00:1X/1X/1X/1X 11:0X/0X/4X

TPM - Security Controller



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MS-7358		
Size: Custom	Document Description: ICH9 - PCI, DMI, USB, PCIE & Slots	Rev: 0A
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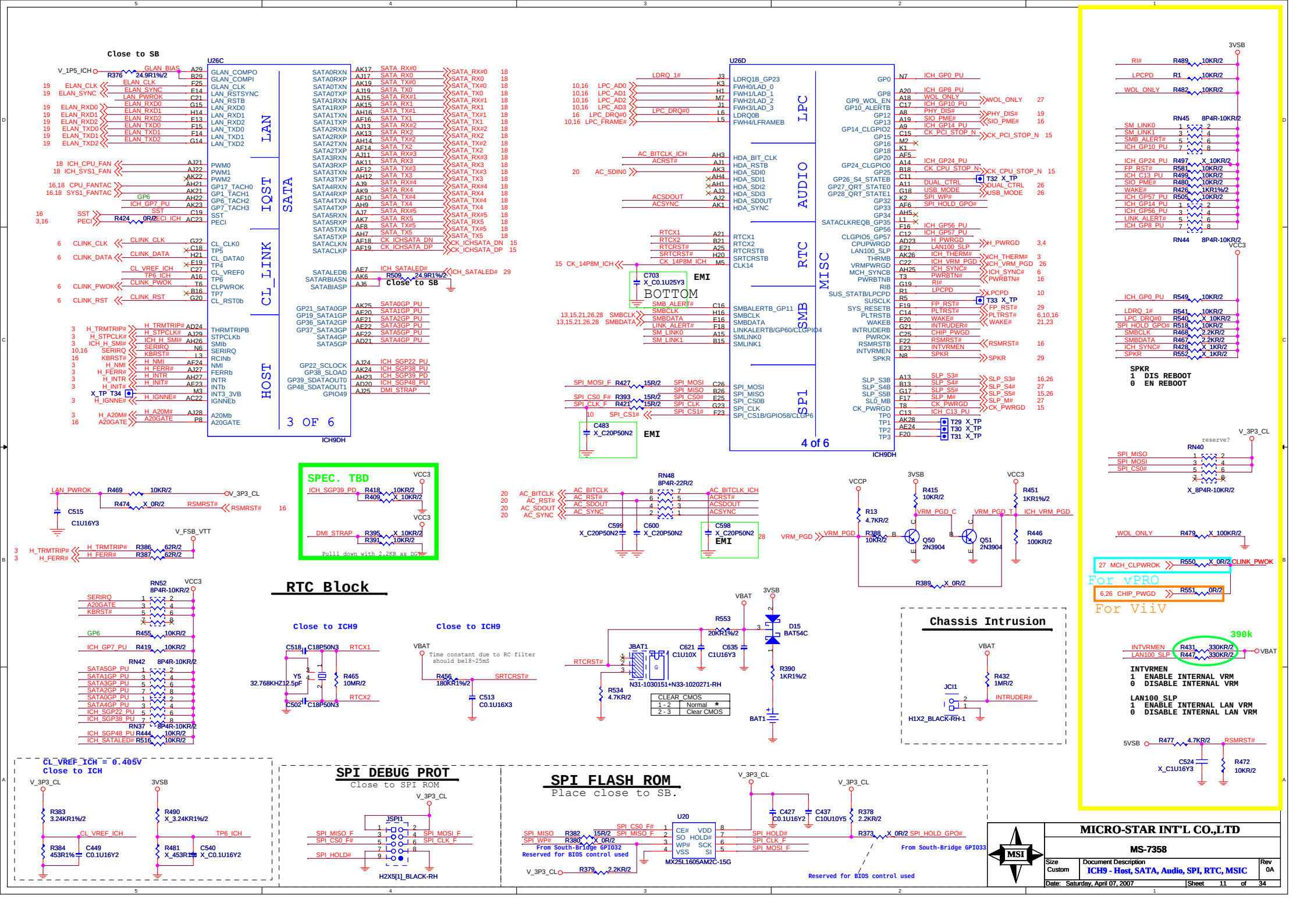
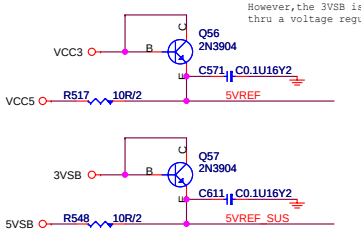
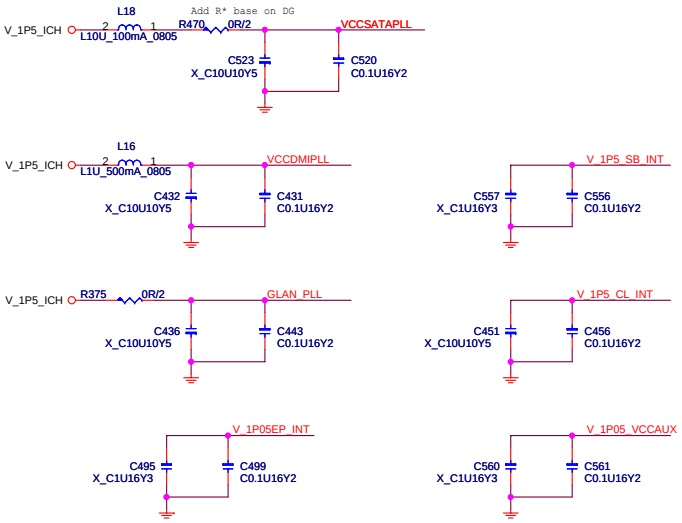

Close to SB
U26C
LAN
IQST
CL_LINK
SATA
HOST
3 OF 6
ICH9DH
U26D
LPC
AUDIO
RTC
MISC
SMB
SPI
4 of 6
ICH9DH
EMI
BOTTOM
SPEC. TBD
RTC Block
Close to ICH9
Close to ICH9
Chassis Intrusion
CL_VREF_ICH = 0.405V
Close to ICH
SPI DEBUG PROT
Close to SPI ROM
SPI FLASH ROM
Place close to SB.
MICRO-STAR INT'L CO.,LTD
MS-7358
ICH9 - Host, SATA, Audio, SPI, RTC, MSIC
SPKR
1 DIS REBOOT
0 EN REBOOT
INTVRMEN
1 ENABLE INTERNAL VRM
0 DISABLE INTERNAL VRM
LAN100_SLP
1 ENABLE INTERNAL LAN VRM
0 DISABLE INTERNAL LAN VRM
For vPRO
For ViiV
390k

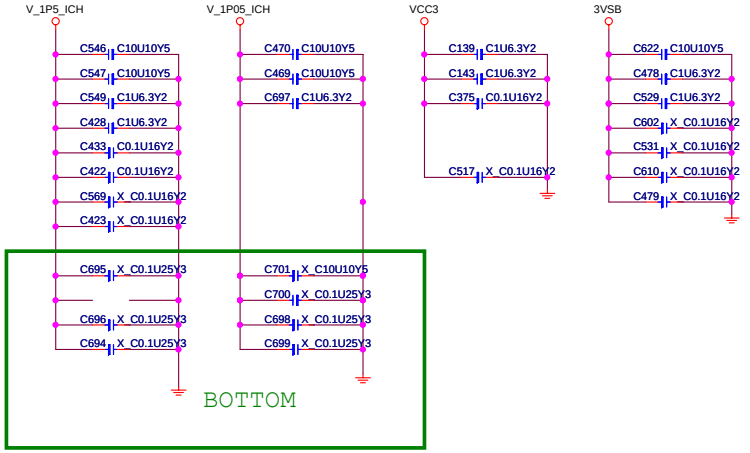
5VREF & 5VREF_SUS Sequencing Circuit

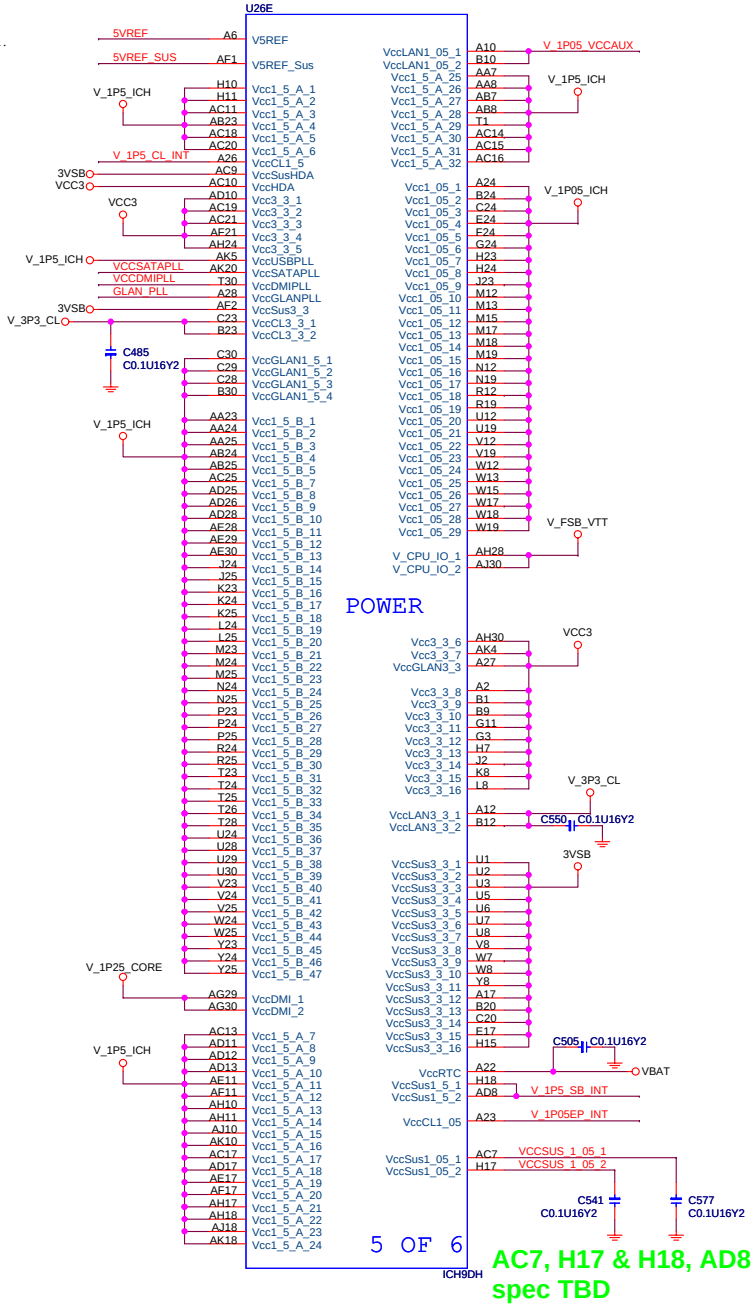
V5REF must be powered up beforeVCC3 or after VCC3 within 0.7V.
Also,V5REF must power down after VCC3 or before VCC3 within 0.7V.
This rule is also applies to V5REF_SUS and 3VSB.
However,the 3VSB is derived from the 5VSB on the power supply
thru a voltage regulator and therefore,they can satisfy the requirement.

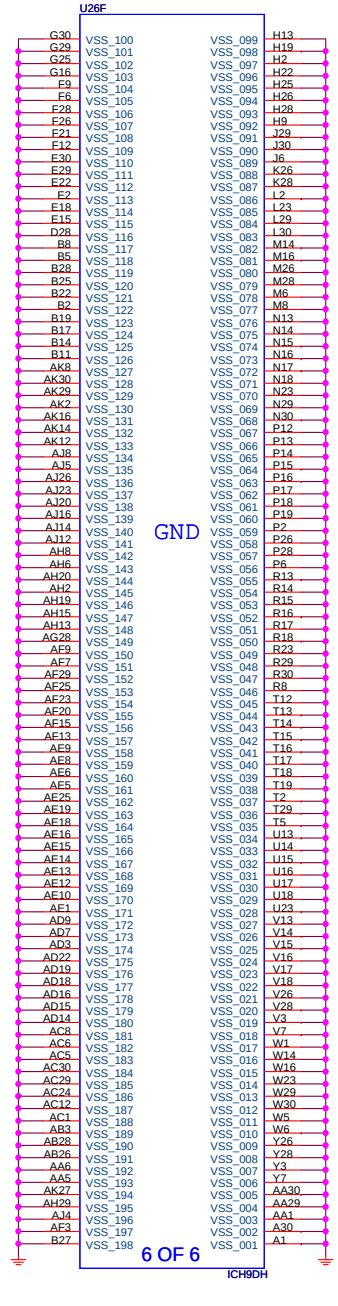


SB POWER









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Size: Custom	Document Description: ICH9 - Power, GND	Rev: 0A
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DDRII DIMM_A1

DDRII DIMM_A2

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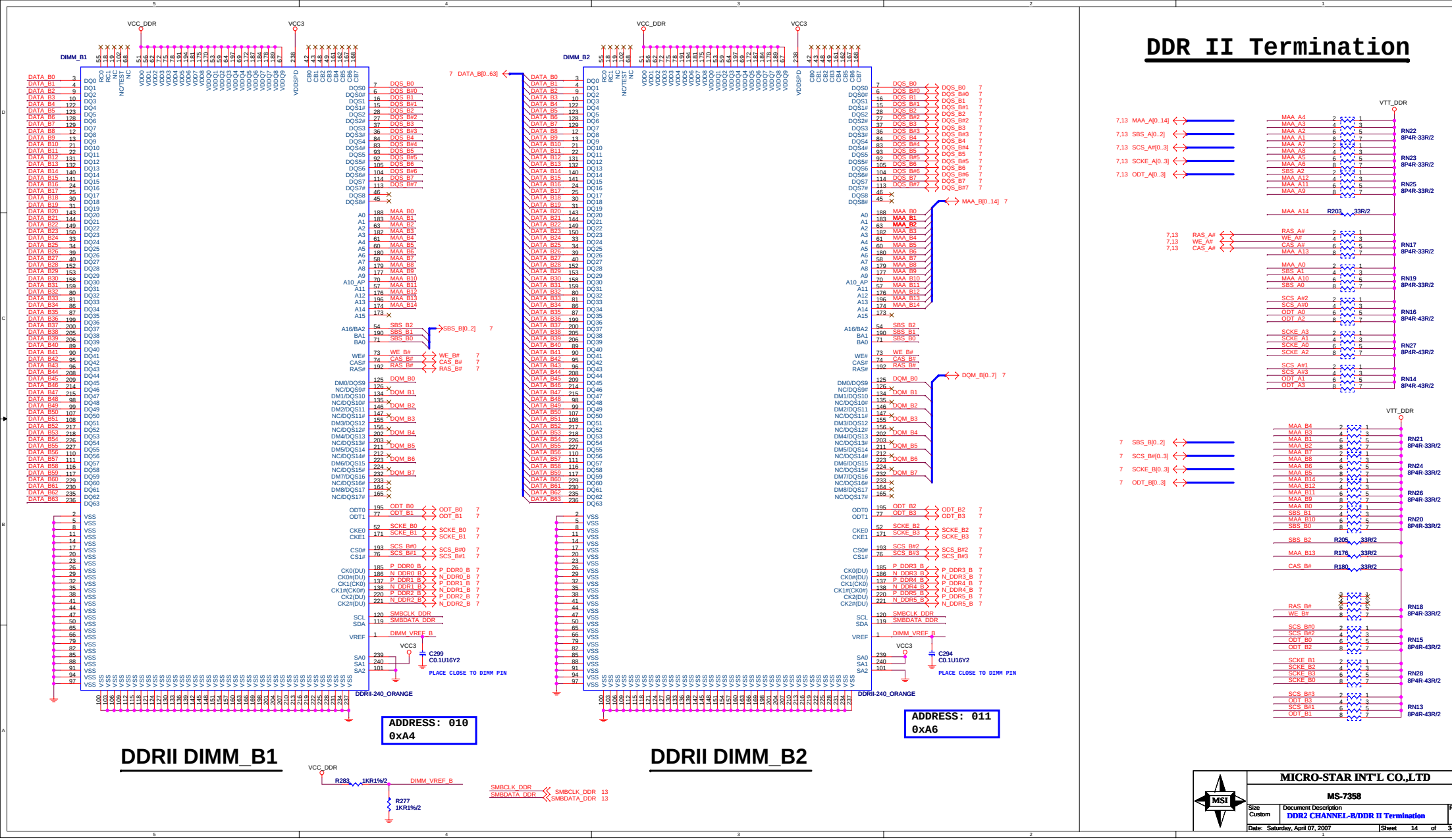
DDR II Termination



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Size: Custom	Document Description: DDR2 CHANNEL-B/DDR II Termination	Rev: 0A
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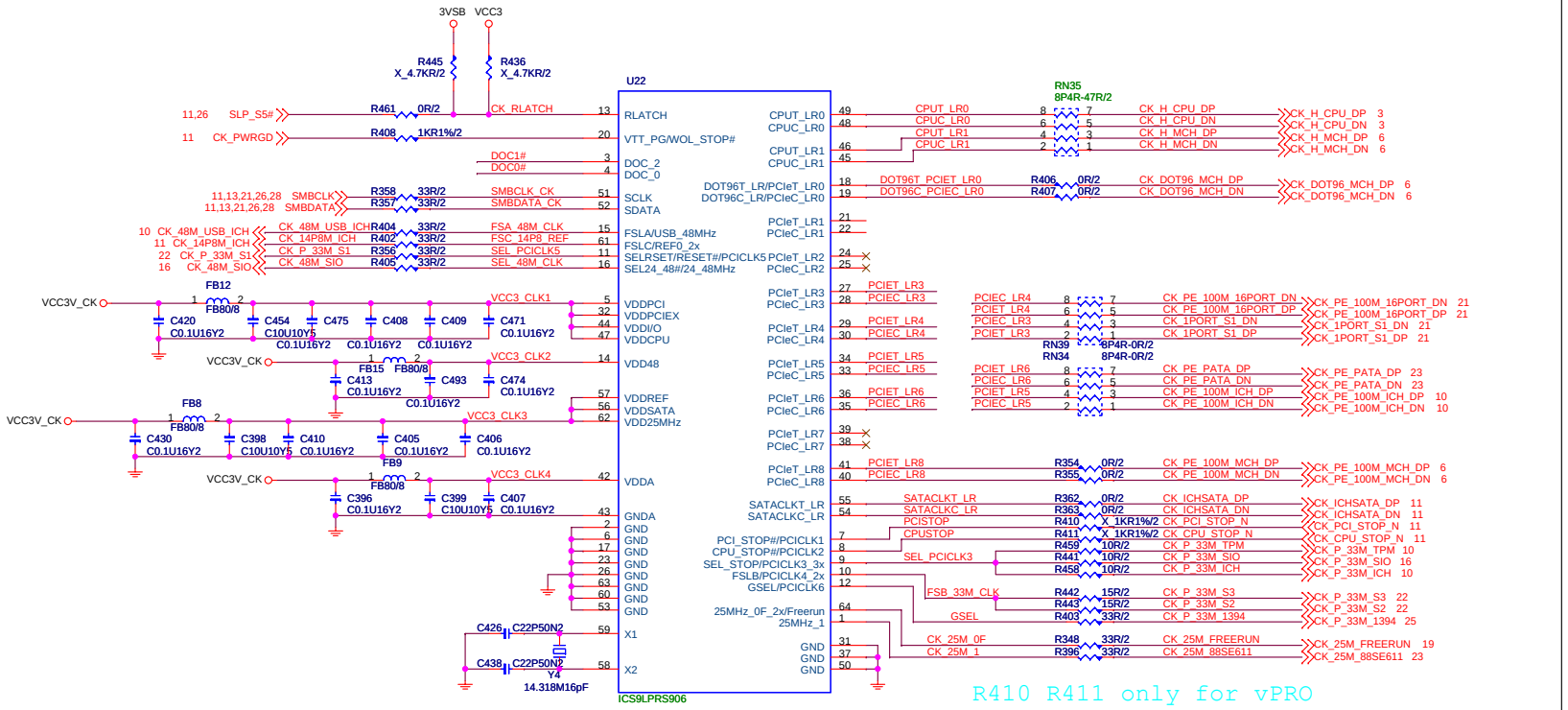
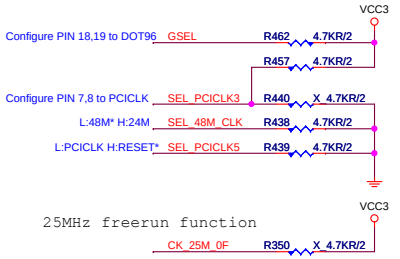
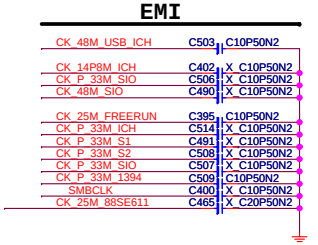


CLOCK GEN STRAPING

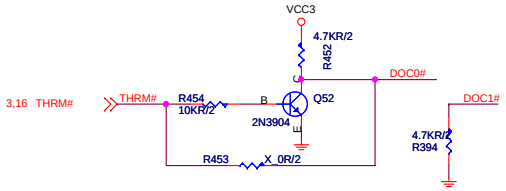


EMI

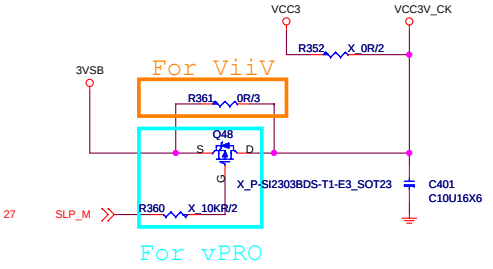


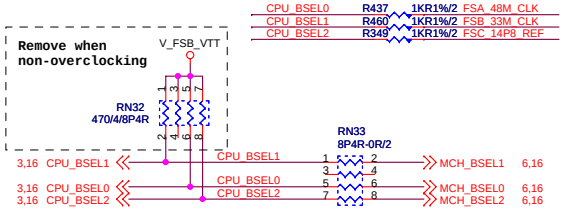
BSEL			TABLE
2	1	0	FSB FREQUENCY
0	0	0	266 MHz (1066)
0	0	1	133 MHZ (533)
0	1	0	200 MHZ (800)
1	0	0	333 MHz (1333)
1	1	0	400 MHZ (1600)

D.O.T



AMT POWER





MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: Clock Gen ICS9LPRS900
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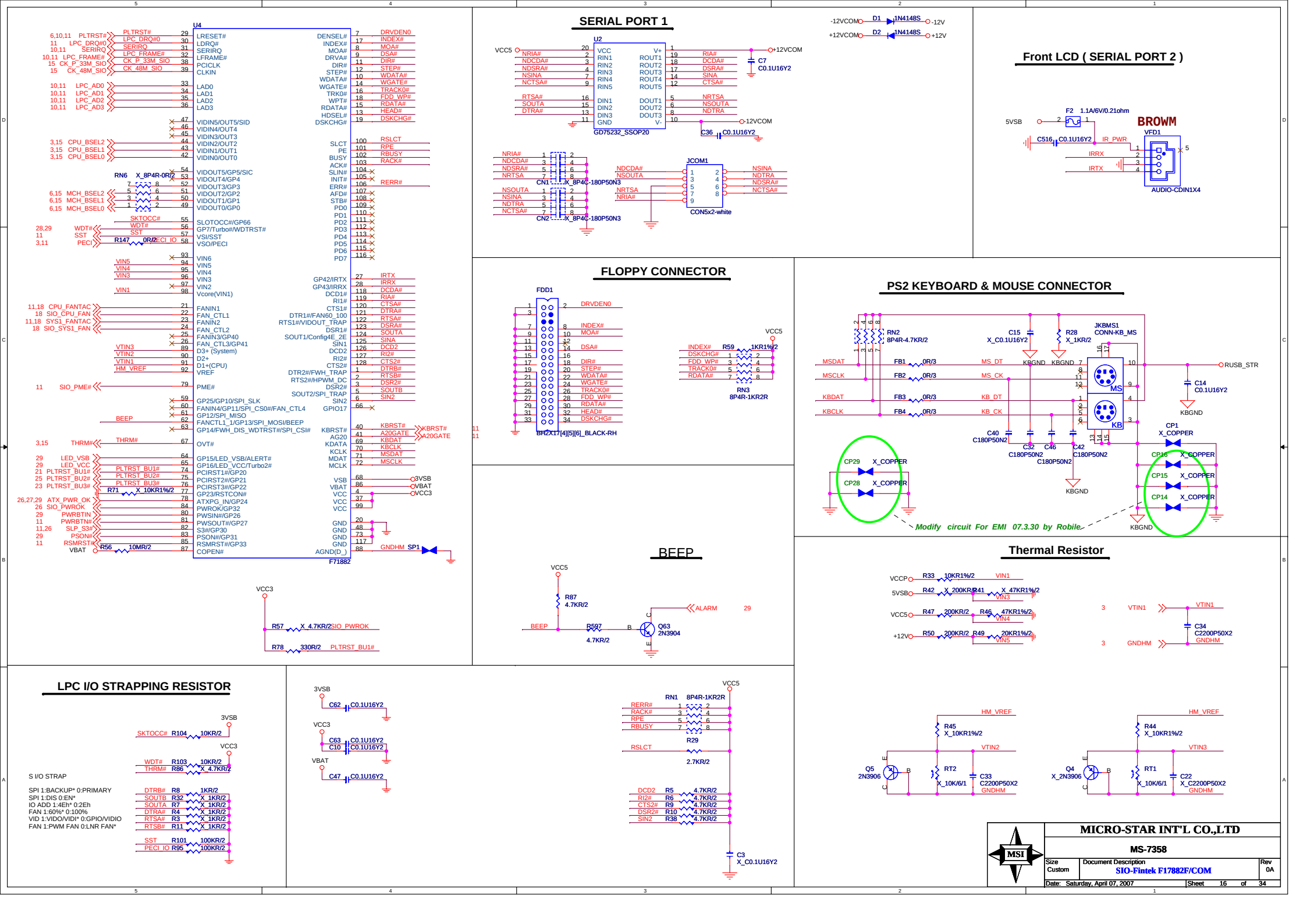
U4
F71882
SERIAL PORT 1
U2
GD75232_SSOP20
JCOM1
CON5x2-white
Front LCD (SERIAL PORT 2)
BROWM
AUDIO-CDIN1X4
FLOPPY CONNECTOR
FDD1
PS2 KEYBOARD & MOUSE CONNECTOR
Modify circuit For EMI 07.3.30 by Robile
BEEP
Thermal Resistor
LPC I/O STRAPPING RESISTOR
S I/O STRAP
SPI 1:BACKUP* 0:PRIMARY
SPI 1:DIS 0:EN*
IO ADD 1:4Eh* 0:2Eh
FAN 1:60%* 0:100%
VID 1:VIDO/VIDI* 0:GPIO/VIDIO
FAN 1:PWM FAN 0:LNR FAN*
MICRO-STAR INT'L CO.,LTD
MS-7358
SIO-Fintek F17882F/COM
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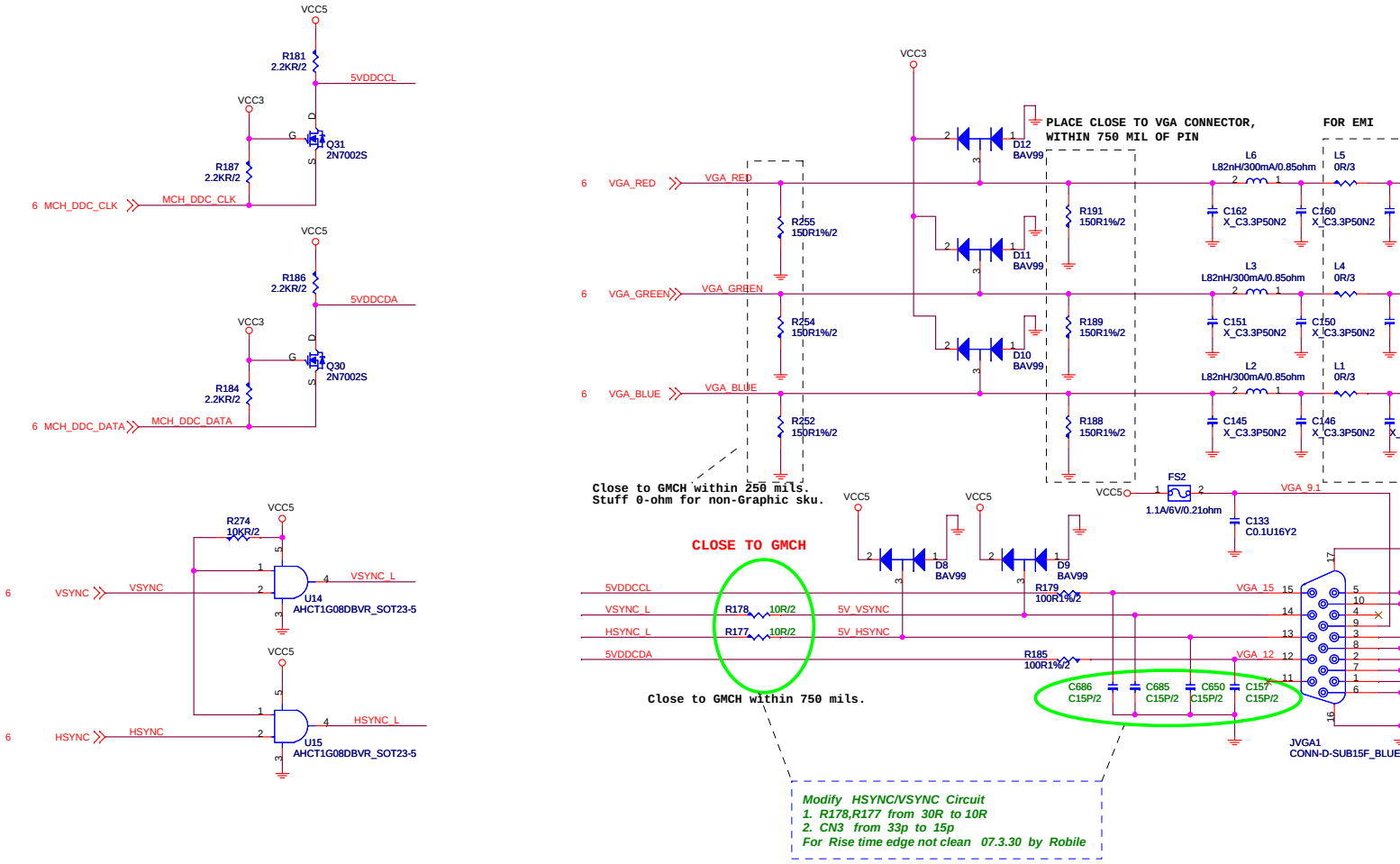
Video Connector



MICRO-STAR INT'L CO.,LTD		
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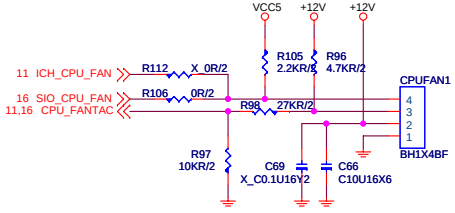
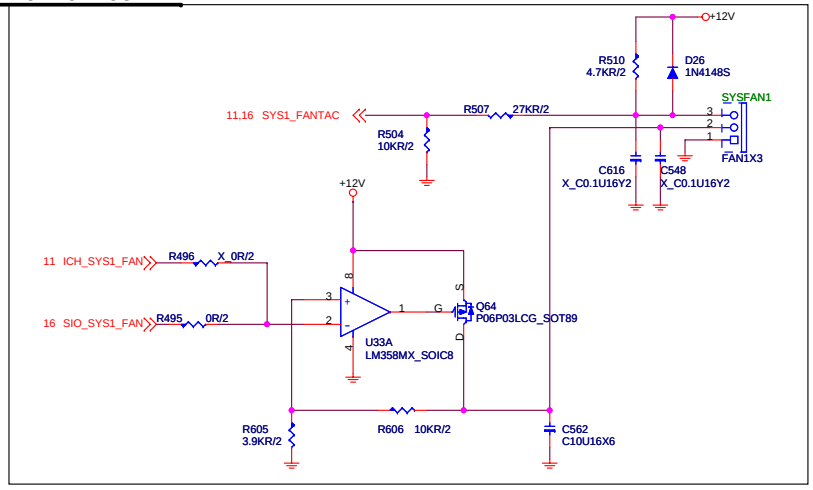
e-SATA trace length should be less than 10 inch.(Connector to Chip)

FAN-COUNTROL CIRCUIT





Modify System FAN circuit & Remove PWR_FAN for spec need 3pin DC Smart FAN 07.3.30 by Robile

MSI	MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: SATA & e-SATA Ports and Fan Control	Rev: 0A
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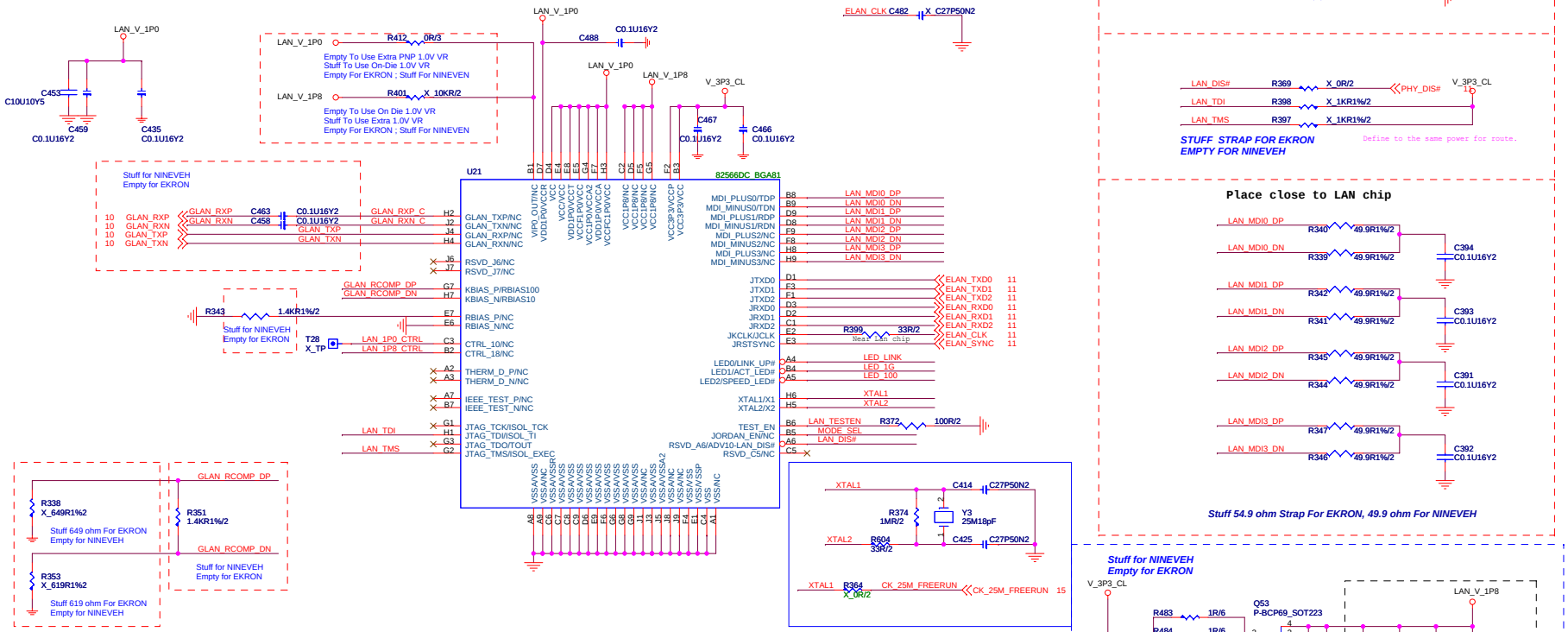
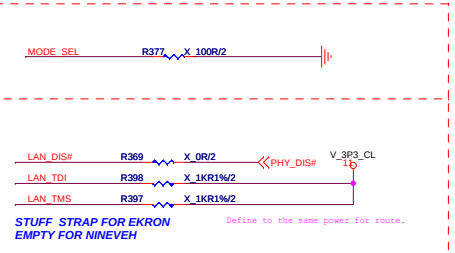
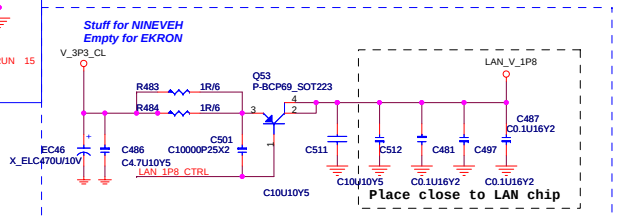
LAN - NINEVEH/EKRON







Intel 82556DM
For business desktop PCs.Support Intel AMT2 or ASF 2.0 alerting,Circuit Breaker,WoL,PXE,Multiport teaming,RSS,Intel Stable Image Platform Program drivers.
Intel 82556DC
For consumer desktop PC.Support Digital Home capabilities,WoL,PXE.
Intel 82562V
Basic 10/100 Ethernet connection.

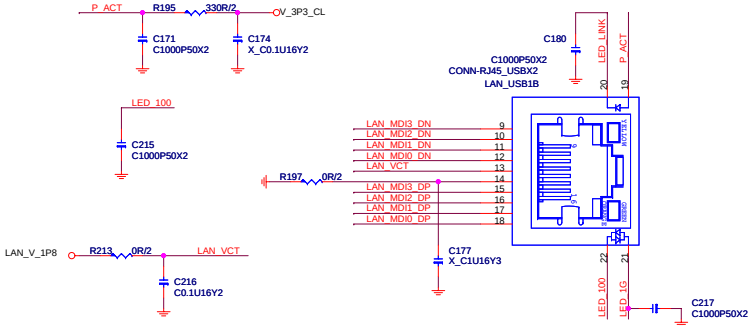
B06-8256605-IY6
FOR NECP CONSIGN,CHIP LAN,INTEL/82566DM,,BGA-81pin,NINEVEH GIGA LAN CHIP(PHY),RoHS COMPLIANCE

B06-8256615-I06
,CHIP LAN,INTEL/82566DC,,BGA-81pin,NINEVEH GIGA LAN CHIP(PHY),RoHS COMPLIANCE

B06-8256205-I06
,CHIP LAN,INTEL/82562V,,BGA-81pin,NINEVEH GIGA LAN CHIP(PHY),RoHS COMPLIANCE

Modify Lan CLK circuit only BOM changes 07.3.30 by Robile

LAN CONNECTOR

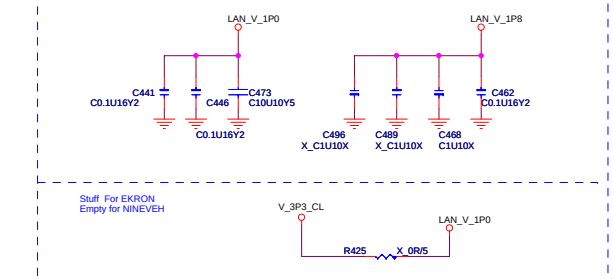


Speed LED Type
1000Mbps : Orange
100Mbps : Green
10Mbps : LED off

YELLOW : For Active/Link

ACT_LED	Link_LED
S0: LOW	S0: LOW
S1/S3/S4/S5: HIGH	S5: HIGH
	S1/S3/S4: WOL EN-->LOW WOL DIS-->HIGH

Giga-Lan	10/100-Lan
N58-22F0181-S42	N58-22F0061-S42 N58-22F0061-F02
Link Yellow Active Blinking 1000 Orange 100 Green 10 None	Link Yellow Active Blinking 100 Green 10 None
19 20 Yellow	19 20 Yellow
21 Orange 22 Green	21 22 Green



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	MS-7358	
Size: Custom	Document Description: LAN NINEVEH/EKRON	Rev: 0A
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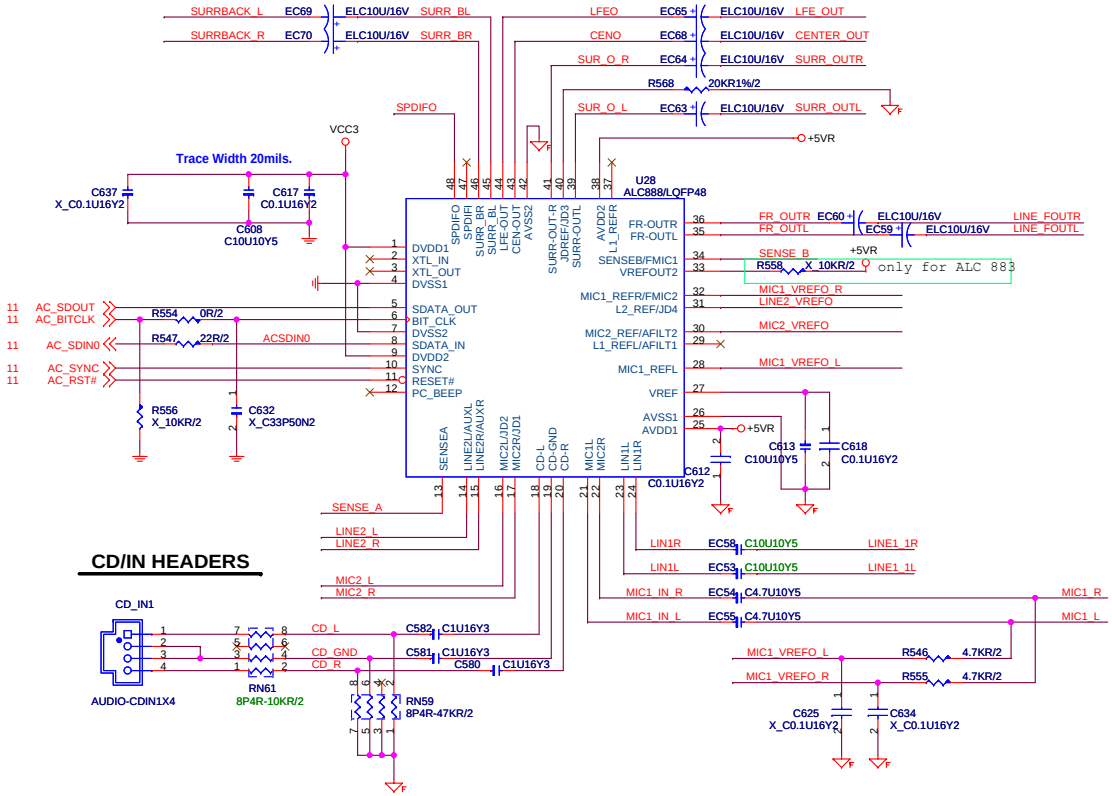
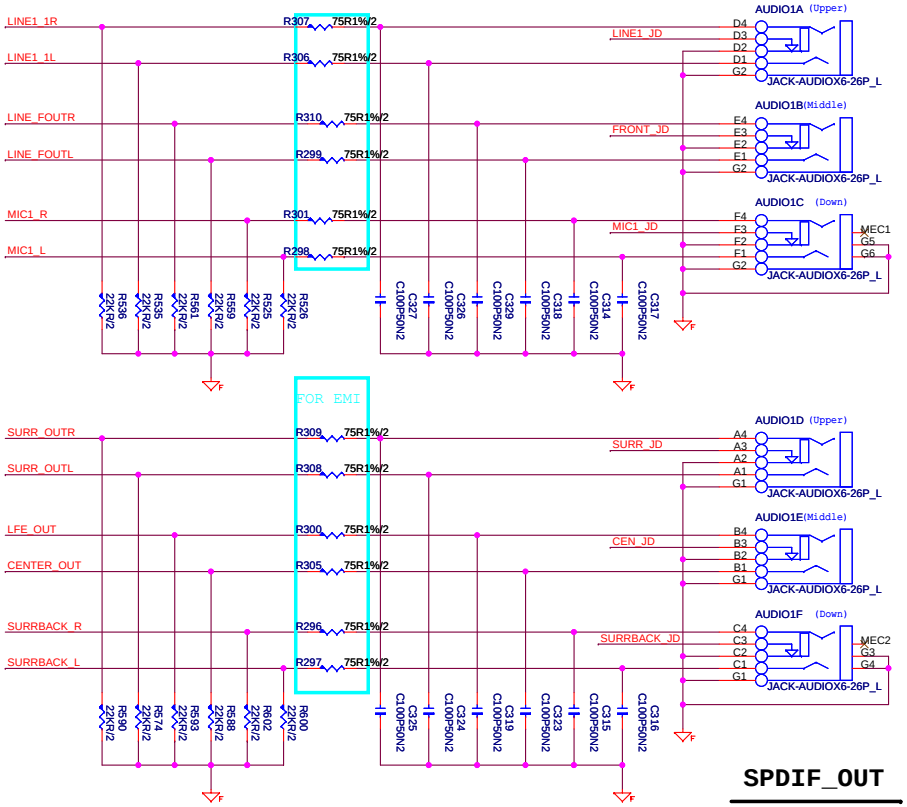
ALC883 CODEC



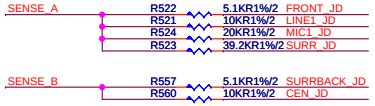
CD/IN HEADERS

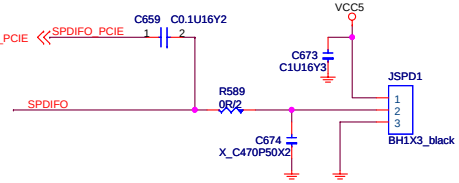
ALC883 JACK

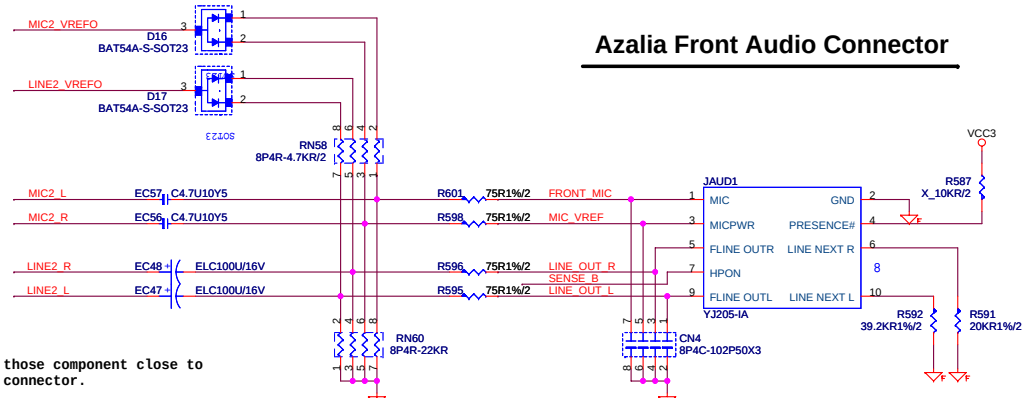


SPDIF_OUT

ALC883 JACK DETECT



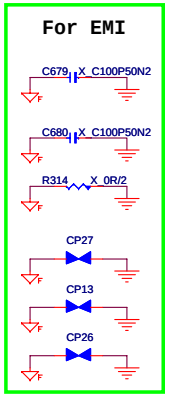




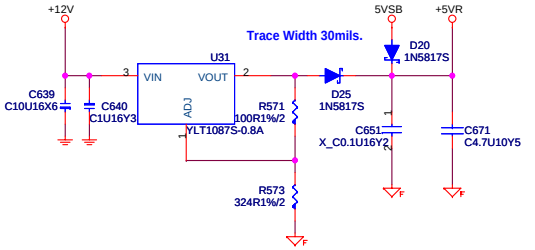
Azalia Front Audio Connector

Place those component close to audio connector.

For EMI



AUDIO CODE REGULATORS



MICRO-STAR INT'L CO.,LTD		
MS-7358		
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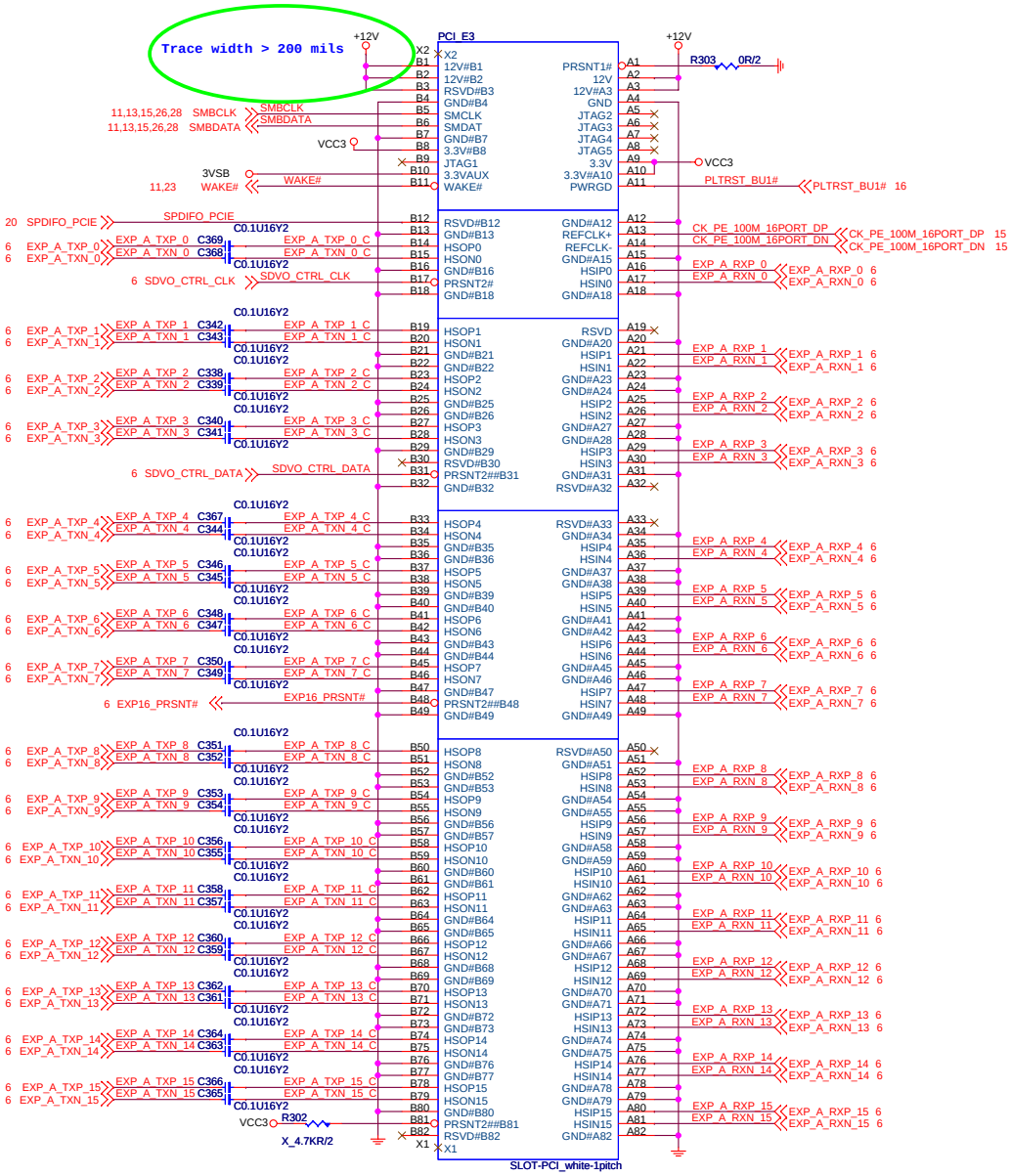
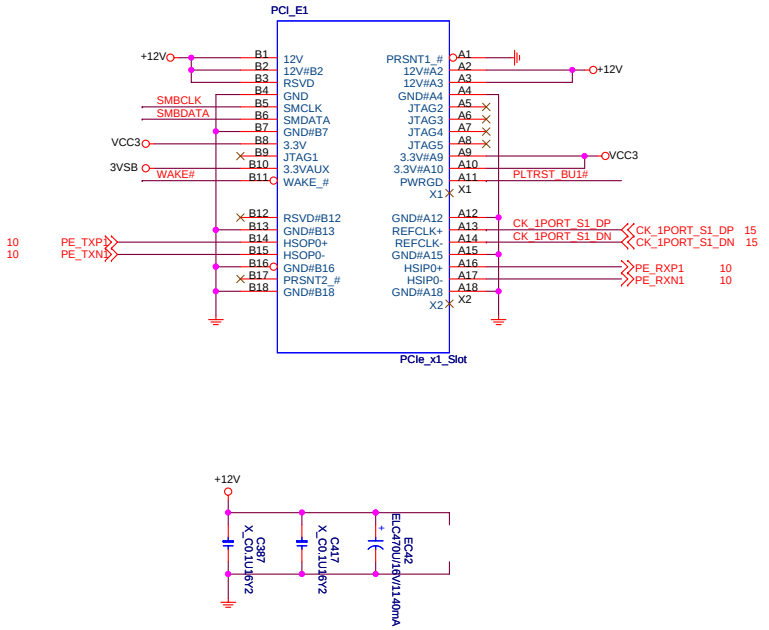
PCI_Express X16 Slot



PCI_Express X4 Slot
(Share with PCI_E x1 Slots)



MICRO-STAR INT'L CO.,LTD	
MS-7358	
Size: Custom	Document Description: PCIE x16, x4, x1 & Bus Switch
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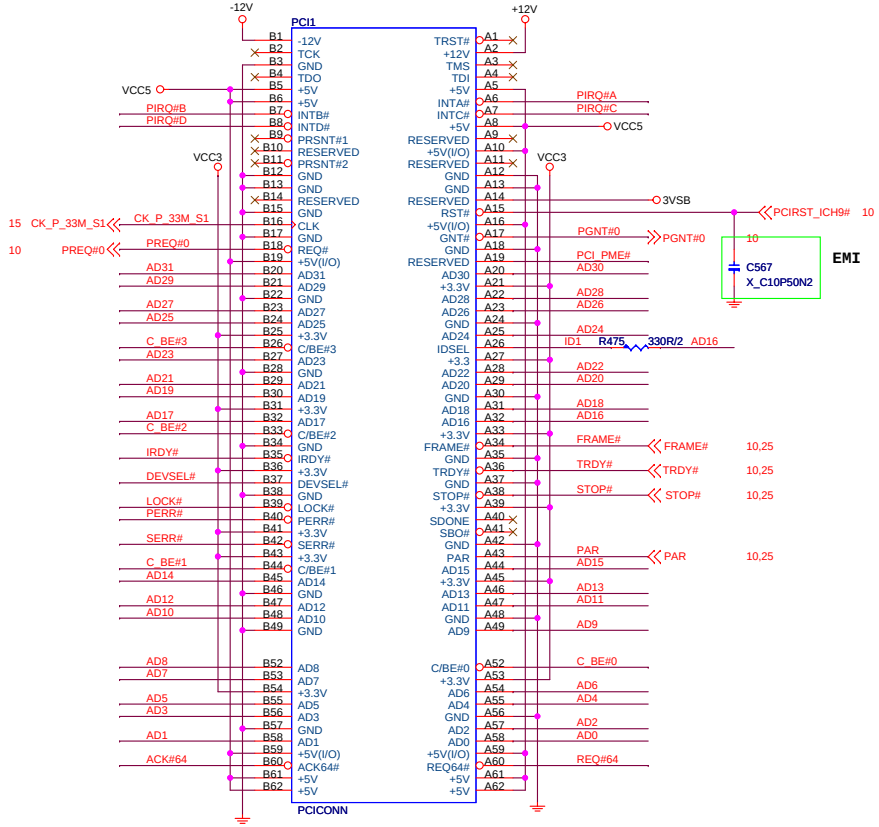
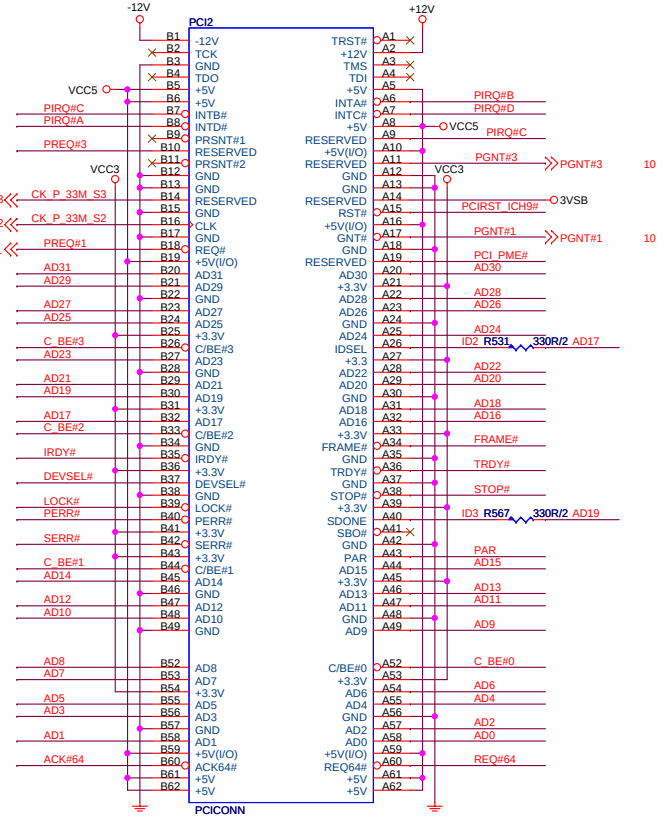
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

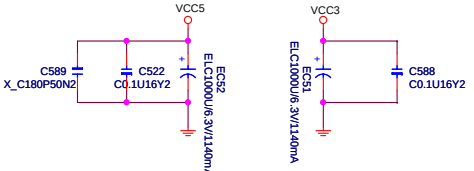
PCI SLOT 2 (PCI VER: 2.2 COMPLY)



IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

PCI PULL-UP / DOWN RESISTORS

PCI SLOT DECOUPLING CAPACITORS



MICRO-STAR INT'L CO.,LTD		
MS-7358		
Size: Custom	Document Description: PCI Slot 1 & 2	Rev: 0A
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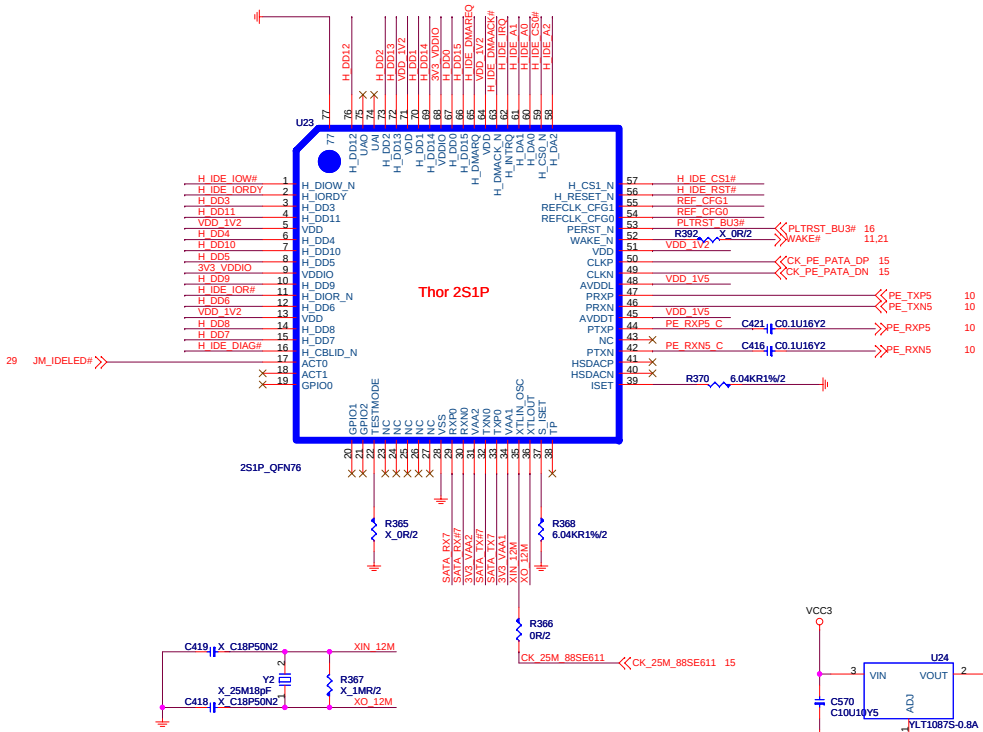
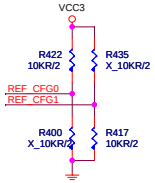
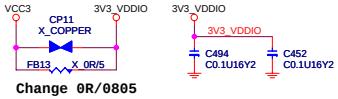
Hi-Speed PCIE to SATA/PATA Bridge



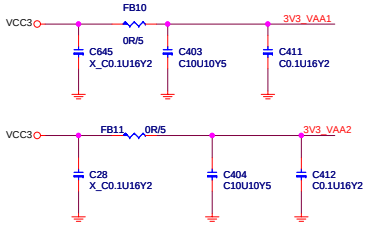
REF_CFG[1:0] =
00:20MHz
01:25MHz

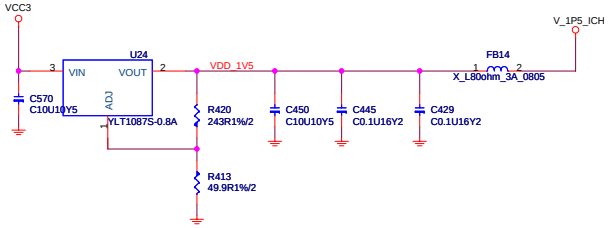


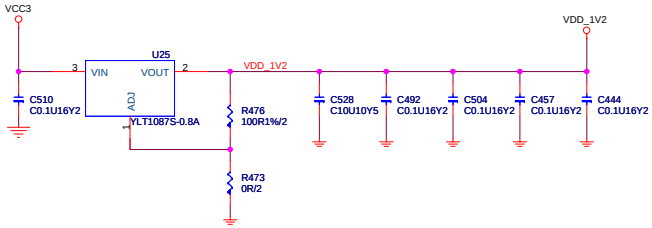


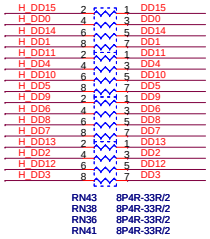
Change 0R/0805

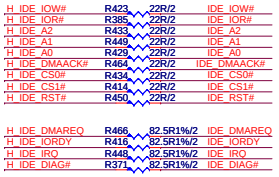
L02-8008074-J07 FOR BEAD

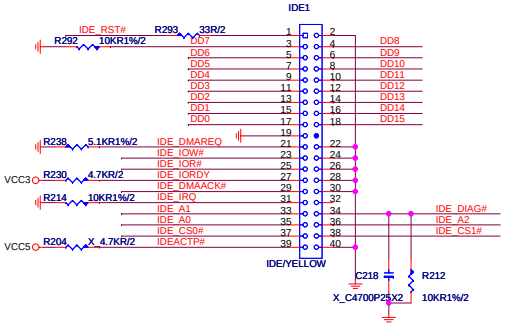


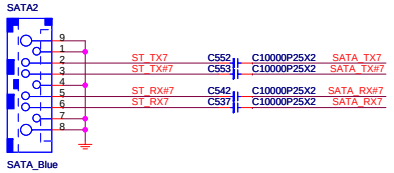












MICRO-STAR INT'L CO.,LTD		
MS-7358		
Size: Custom	Document Description: Marvell 88SE6111 PCIE to PATA/SATA	Rev: 0A
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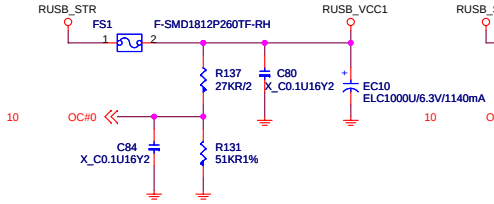
Rear USB Connector

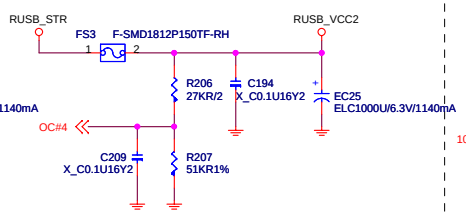
USB POWER FOR PORT 0,1

NEAR CONNECTOR



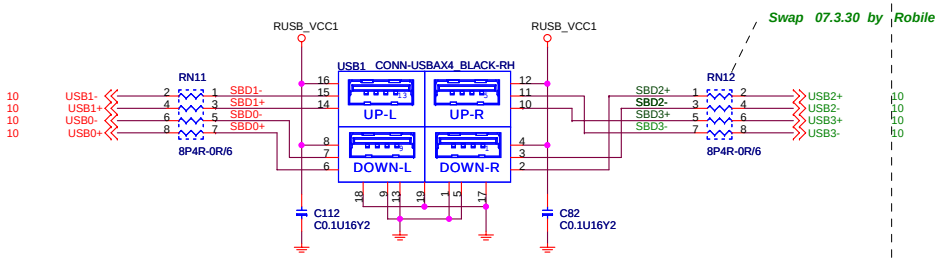
USB POWER FOR PORT 2,3,4,5

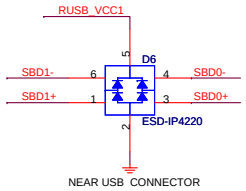
NEAR CONNECTOR

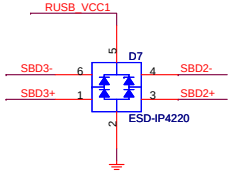


REAR USB PORT 0~3 (2x2)

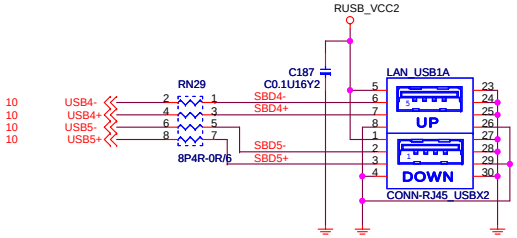
Swap 07.3.30 by Robile

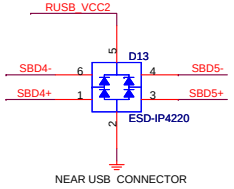






REAR USB PORT 4,5 (With LAN)

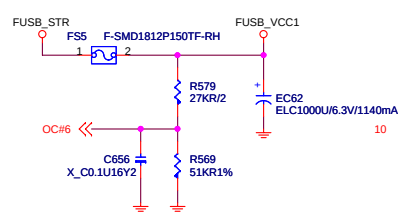




Front USB Connector

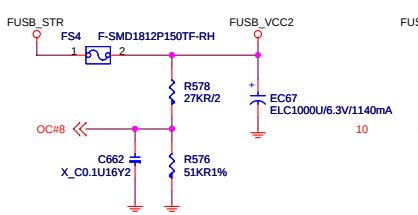
USB POWER FOR PORT 6,7

NEAR CONNECTOR



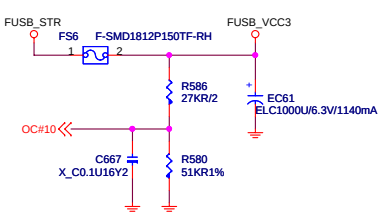
USB POWER FOR PORT 6,7

NEAR CONNECTOR

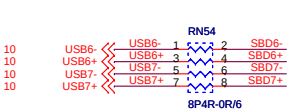


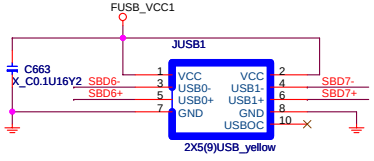
USB POWER FOR PORT 6,7

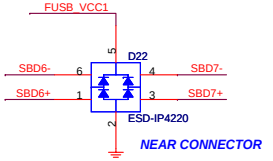
NEAR CONNECTOR



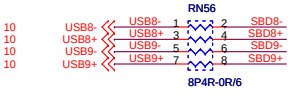
FRONT USB PORT 6,7

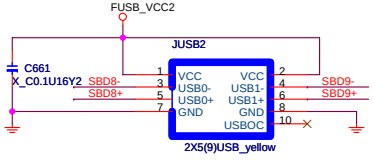


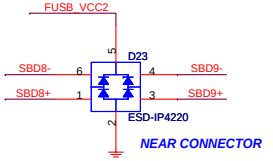




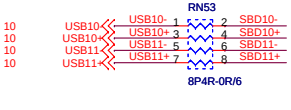
FRONT USB PORT 8,9

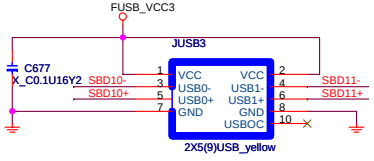


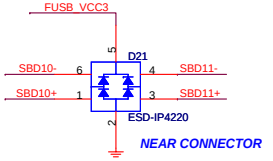




FRONT USB PORT 10,11







MICRO-STAR INT'L CO.,LTD

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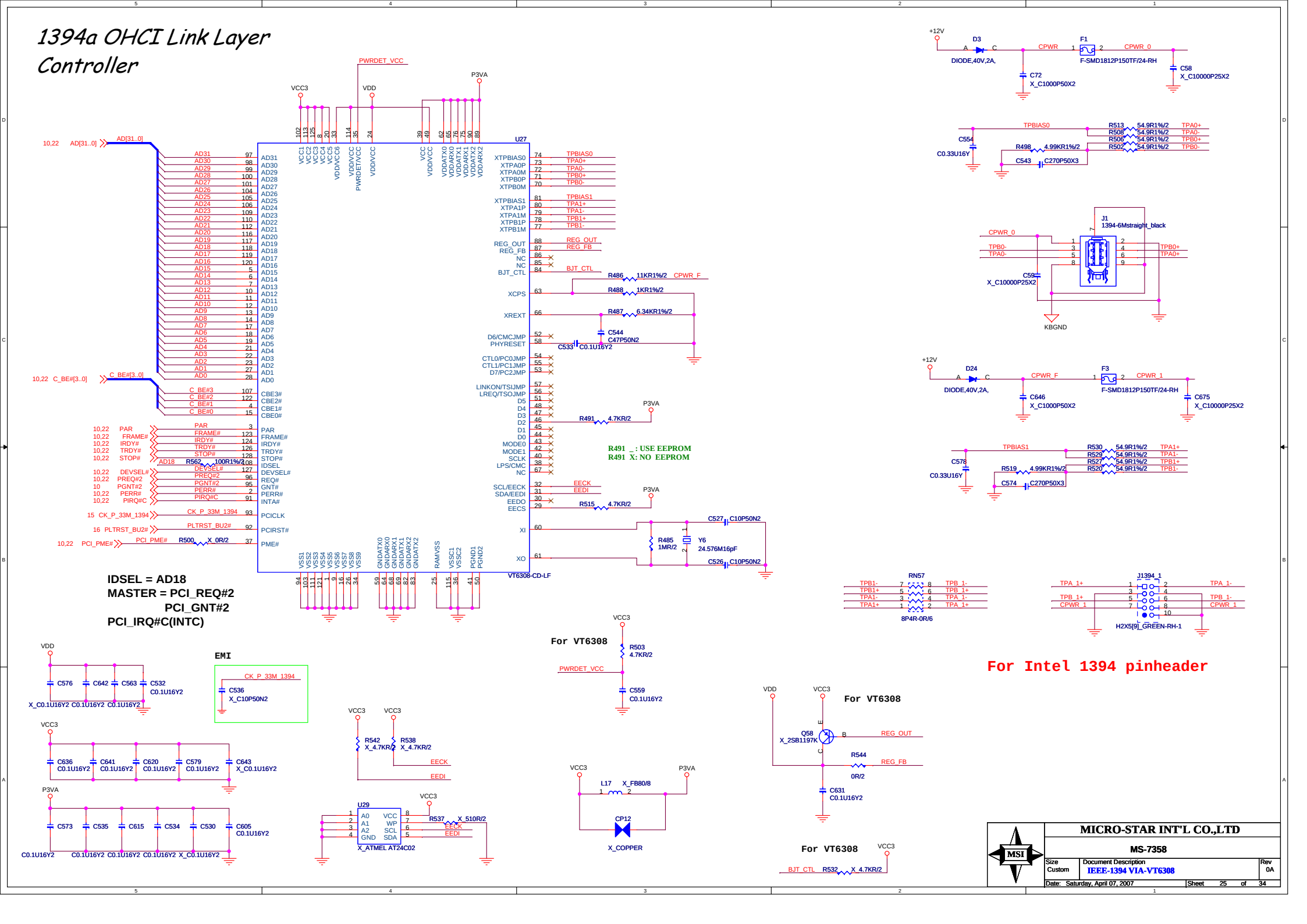
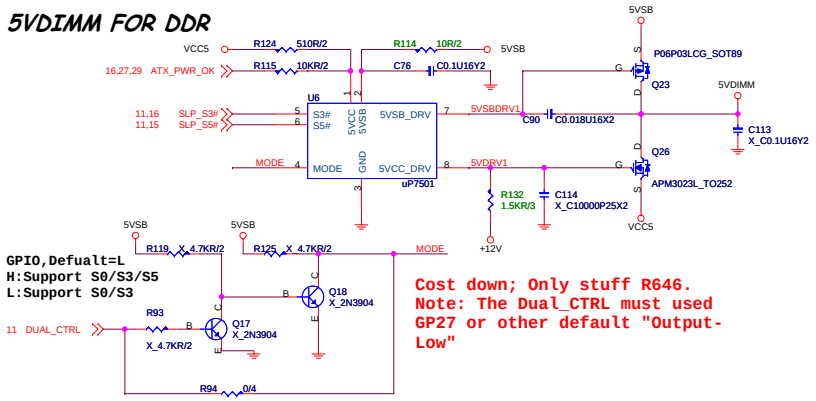
1394a OHCI Link Layer Controller



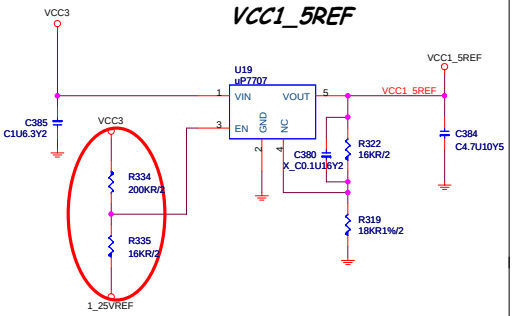
5VDIMM FOR DDR



GPIO,Defualt=L
H:Support S0/S3/S5
L:Support S0/S3

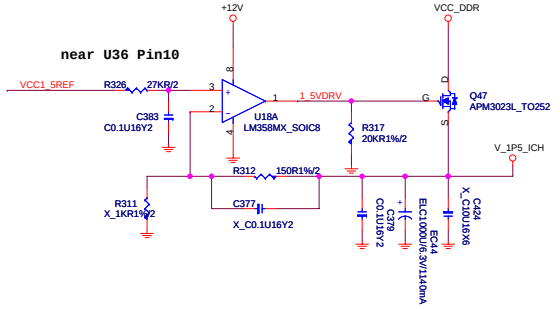
Cost down; Only stuff R646.
Note: The Dual_CTRL must used GP27 or other default "Output-Low"

VCC1_5REF



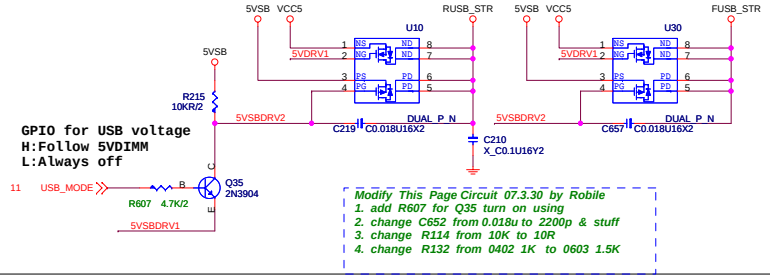
Let 1.25V and 1.5V at the same tine power up or power down

SB 1.5V 2.75A



5VSB FOR Rear USB

5VSB FOR Front USB



GPIO for USB voltage
H:Follow 5VDIMM
L:Always off

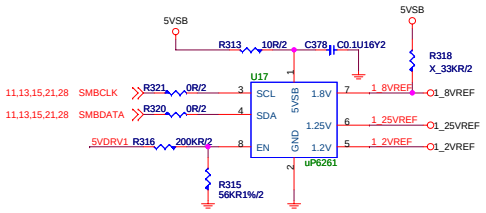
Modify This Page Circuit 07.3.30 by Robile
1. add R607 for Q35 turn on using
2. change C652 from 0.018u to 2200p & stuff
3. change R114 from 10K to 10R
4. change R132 from 0402 1K to 0603 1.5K

*Reference sinking/sourcing 100uA
*Reference ramp-up 5mS
*5VSB > 4.2V POR
*Pin8 > 1.dV Enable
*Pin8 < 0.4V Disable

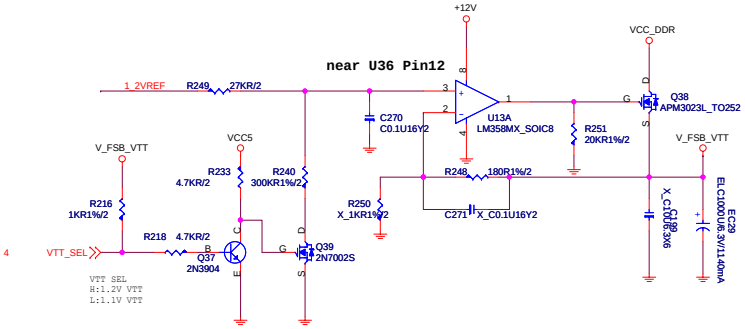
Stuff R361 to prevent the source current not enough issue (5.1-1.8)/33K=100uA

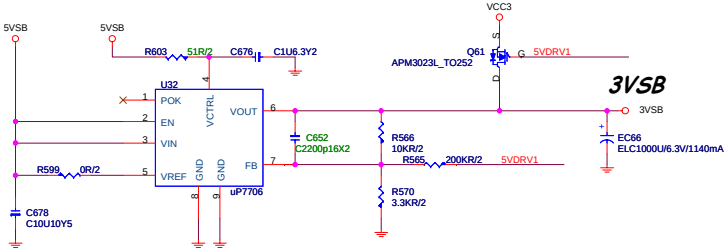
reference Voltage

DDR REF
NB 1.25V REF
V_FSB_VTT REF

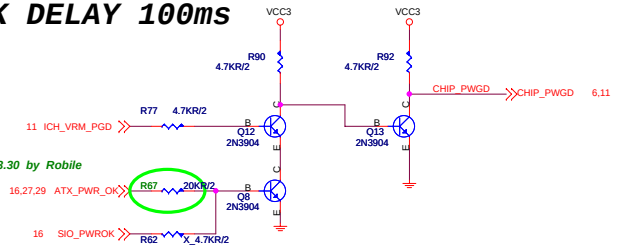


1.2V 5.8A



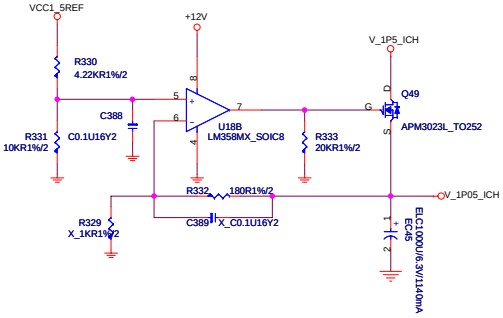


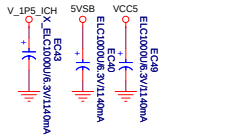
PWROK DELAY 100ms

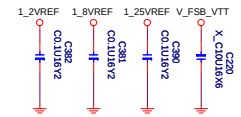


Modify R67 from 4.7K to 20K 07.3.30 by Robile

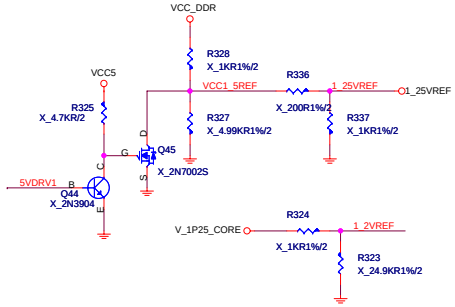
SB 1.05V 2A



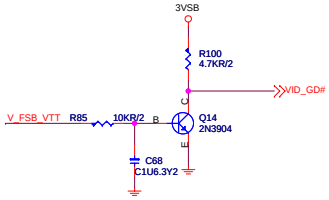




*Reserve for remove uP6261 and uP7707
*1_8REF use uP6103's internal 0.8VREF



VID before PWROK >3ms



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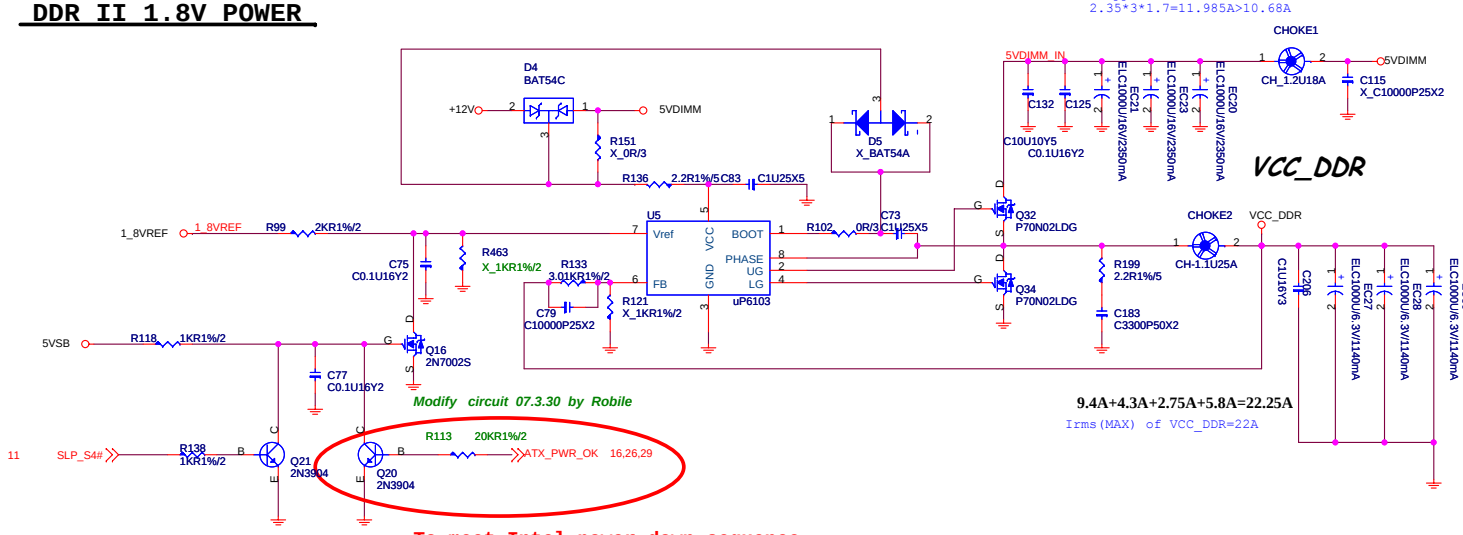
DDR II 1.8V POWER

Iripple=22.25*0.6*0.8/1=10.68A
2.35*3*1.7=11.985A>10.68A

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



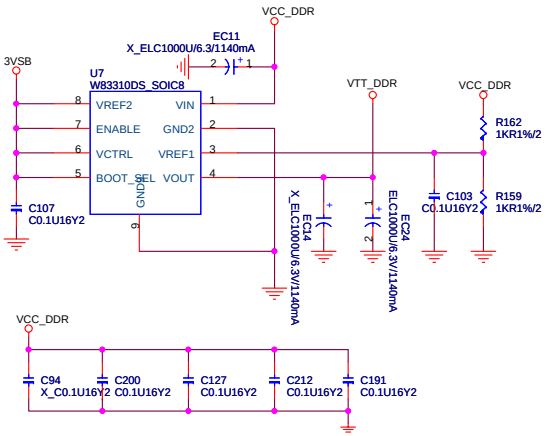
Modify circuit 07.3.30 by Robile

To meet Intel power down sequence.

9.4A+4.3A+2.75A+5.8A=22.25A

Irms(MAX) of VCC_DDR=22A

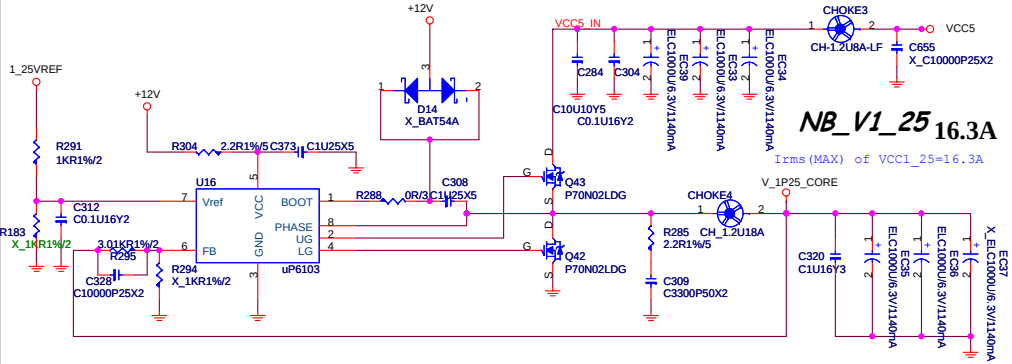
DDR VTT Power



de- VCC_DDR high frequency noise.

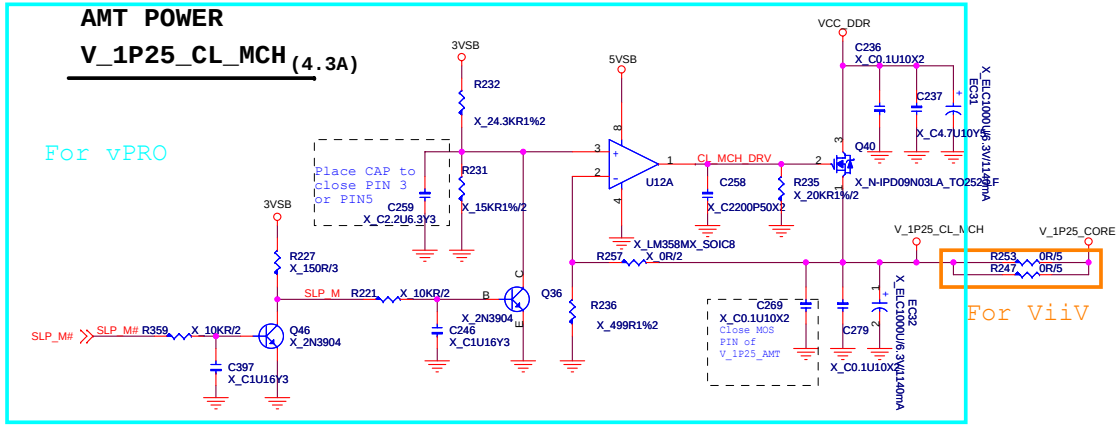
NB 1.25V POWER

Iripple=16.3*0.49*0.878/1=7A
1.14*3*1.7=5.814A>5.59A

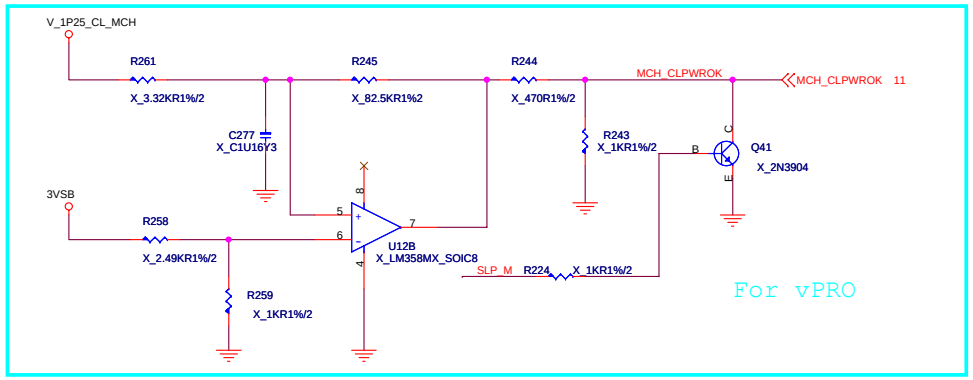


AMT POWER

V_1P25_CL_MCH (4.3A)

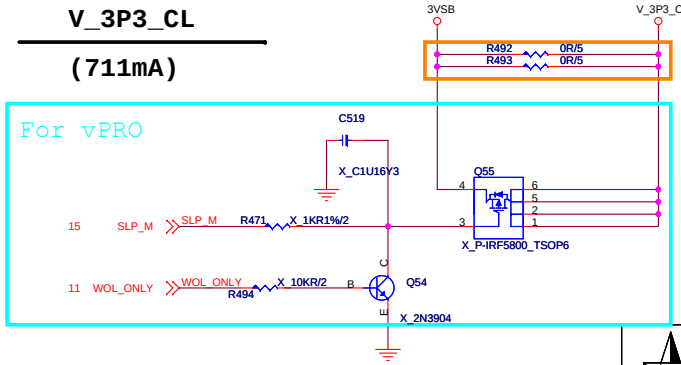


CLINK PWROK GENERATION



V_3P3_CL

(711mA)



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Voltage Regular Module

N-P0903BDG_TO252	mosfet/n-channel,P0903BDG,SMT/TO252,Rds(on)=9.5mΩ(10V/25A),Vgs(on) =1~3V,Id=50A,Ciss=1800pf,Qg=50nC,Vds=25V,Vgs=±20V,RoHS compliance
P75N02LDG/TO252	mosfet/n-channel,P75N02LDG,SMT/TO252,Rds(on)=7mΩ(@10V,30A),Vgs(on)=1~3V,Id=75A,Ciss=5000pf,Qg=140nC,Vds=25V,Vgs=±20V,RoHS compliance
C100U2SP	ESR<13mΩ,Ripple cur:2.7A,Lc<12uA,105c
CD560U40S-2	CAP,OS-CON,560U/4V,Dip-2/8*9/3.5mm,ESR<7mohm, Ripplecur.=6100mA ,Lc. <500uA,SPEC series,RoHS compliance
1800UF/6.3V	ESR<12mΩ, Ripplecur<2350mA,105C, longlife change from 2000hrs to 3000hrs ,KZJ series
0.25uH/40A	,IND CHOKE,0.25uH,20%,DIP/8.5mm,40A,0.6mOhm,,,PEW,FERRITE,SQUARE,RoHS COMPLIANCE
CH-1.1U25A-LF	IND CHOKE,1.1uH,20%,DIP/9mm,25A,1.4mOhm,5.5T,0.9mmx3,PEW,IRON,,LEAD FREE
CD1000U16EL20-2	CAP,EL,1000u,16V,Dip-8x20/3.5mm,20%,12mOhm,2350mA,105C,3000hrs,RoHS COMPLIANCE

0.8375~1.6V / 125A

CP25,CP26,CP27,CP28 PLACE ON THE SOLDER SIDE, CLOSE TO INDUCTOR

Place close to inductor

Only reserve for 3 phase operate

BOTTOM PAD CONNECT TO GND

FOR WATCH DOG

680uF EL Capacitors

PANASONIC Cap.

MLCC Inside Socket

Sansung Cap.

SP Capacitors

EL Capacitors

OSTOR Cap.

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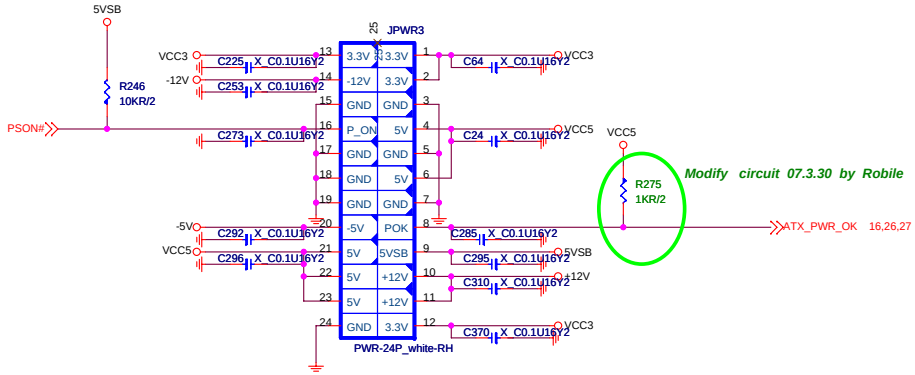
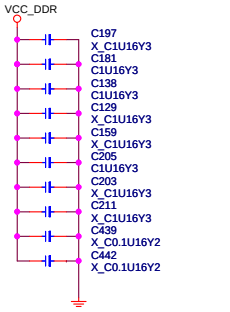
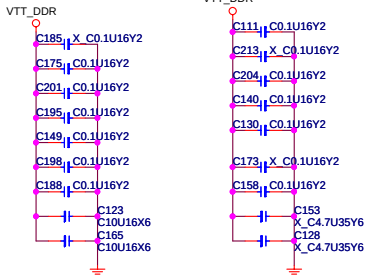
ATX POWER CONNECTOR



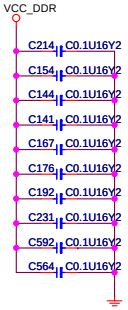
CHANNEL A V_SM_VTT DECOULPING CAPS

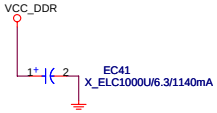


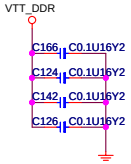
CHANNEL B V_SM_VTT DECOULPING CAPS



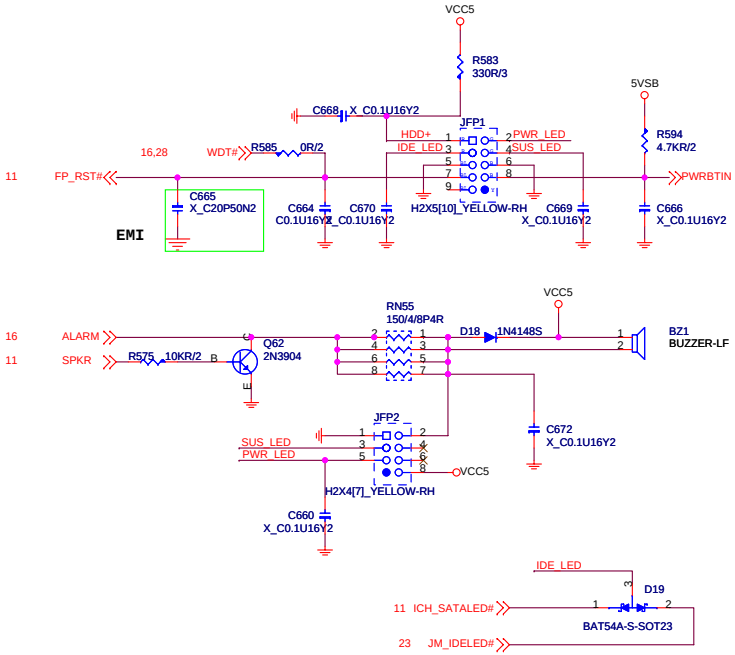
FOR EMI



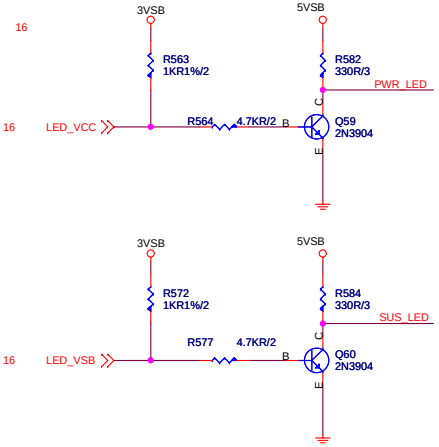




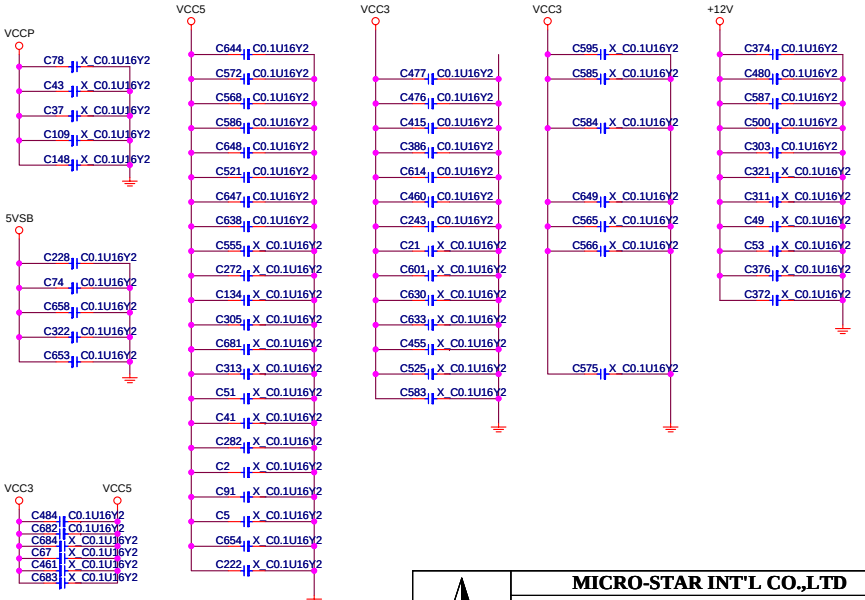
FRONT PANNEL



LED (for Fintek 71882)



Cap. for EMI & Power



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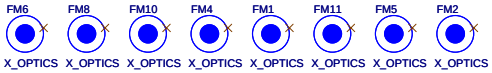
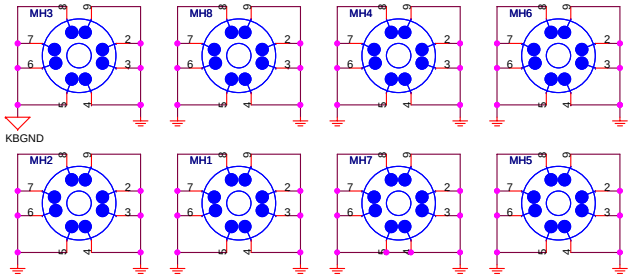
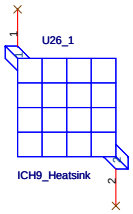
Optical Fiducial Marks-120

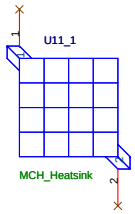
Optical Fiducial Marks-100



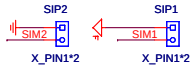
Mounting Holes







Simulation



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