MS-7357 uATX Version: 1.0

CPU: Intel, Socket 775 (Intel Core 2 Duo Processors, Intel Pentium D Processors, Intel Pentium 4 Processors, Intel Celeron D Processors)--65-130 watts Intel Core 2 Duo, Pentium D, Celeron D

System Chipset:

Intel Bearlake - Q (North Bridge)
Intel ICH9 (South Bridge)

On Board Device:

CLOCK Gen -- ICS9LPRS906
LPC Super I/O -- Fintek F71882FG
IEEE1394 -- VIA VT6308
Storage controler -- Marvell 88SE6111
LAN -- Marvell 88E8071/8056/8039
HD Audio Codec -- ALC888

Main Memory:

Dual-channel DDR-II * 4

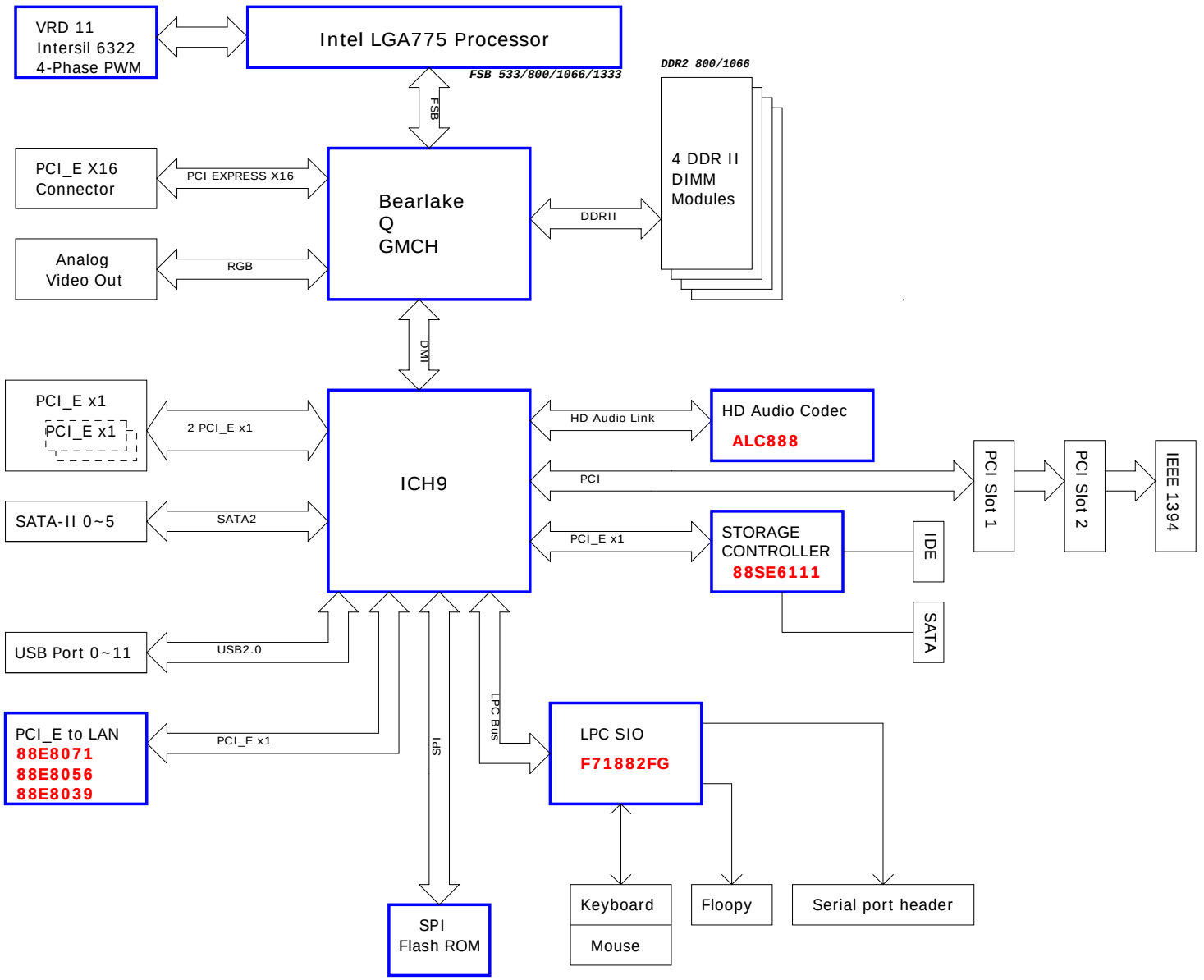
Expansion Slots:

PCI EXPRESS X16 SLOT *1
PCI EXPRESS X1 SLOT * 1
PCI SLOT * 2

PWM: VRD11 Intersil 6322 4Phase

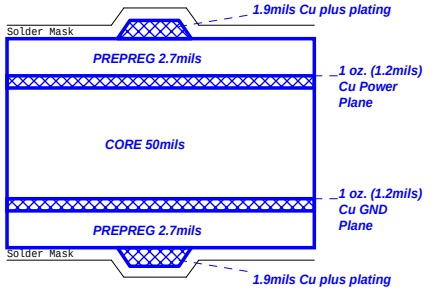
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7357	
Size: Custom	Document Description: COVER SHEET	Rev: 1.0
Date: Monday, March 26, 2007	Sheet 1 of 35	

Block Diagram



Board Stack-up

(1080 Prepreg Considerations)



Single End 50ohm Top/Bottom : 4mils
USB2.0 - 90ohm : 15/7.5/4.5/7.5/15
SATA - 95ohm : 15/8/4/8/15
LAN - 100ohm : 15/10/4/10/15
PCIE - 95ohm : 15/8/4/8/15

MICRO-STAR INT'L CO.,LTD		
MS-7357		
Size: Custom	Document Description: BLOCK DIAGRAM	Rev: 1.0
Date: Monday, March 26, 2007	Sheet 2 of 35	

CPU SIGNAL BLOCK

U7A

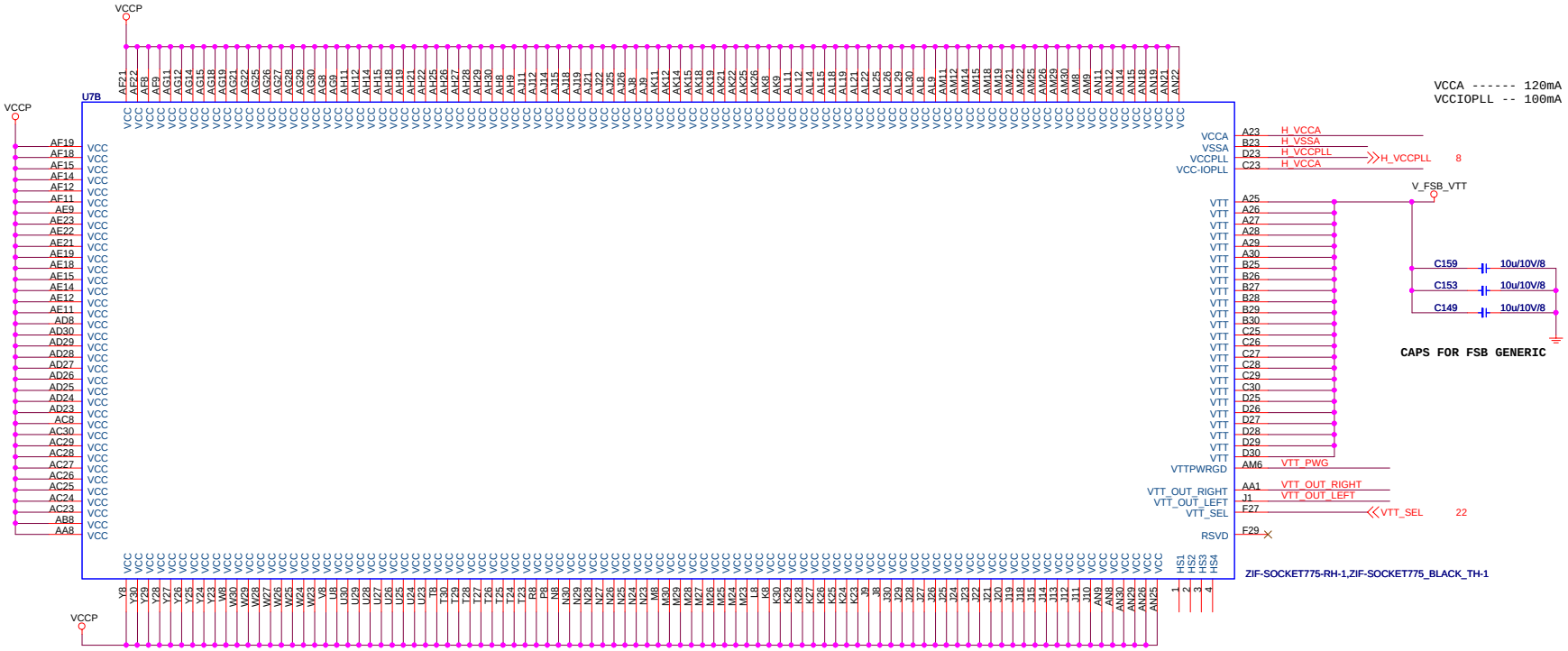
ZIF-SOCKET775-RH-1,ZIF-SOCKET775_BLACK_TH-1

Prescott / Cedar Mill
LL_ID[1:0] = 00
GTLREF_SEL = 0
VTT_SEL = 1

BSEL			TABLE
2	1	0	FSB FREQUENCY
0	0	0	267 MHZ (1067)
0	1	0	200 MHZ (800)
0	0	1	133 MHZ (533)

PLACE BPM TERMINATION NEAR CPU

MICRO-STAR INT'L CO.,LTD	
MS-7357	
Size: Custom	Document Description: Intel LGA775 - Signals
Rev: 1.0	
Date: Monday, March 26, 2007	Sheet 3 of 35

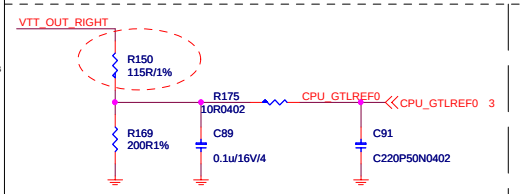


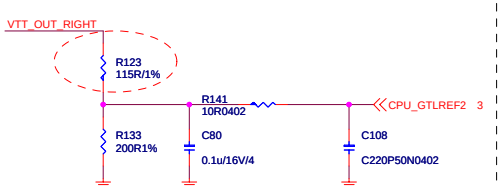
Follow Intel suggestion document to set CPU_GTLREF[3:0] to 63.5%.

* Use 57.6 Ohm 1% resistor over 100 Ohm 1% resistor.

* Divider could also be 115 Ohm 1% resistor over 200 Ohm 1% resistor.

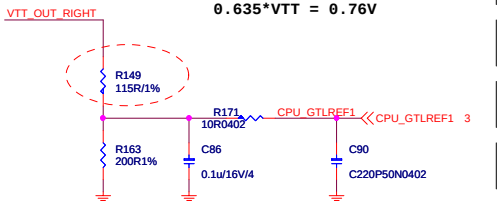
2007/4/3 R(123,125,149,150) change to 115 ohm 1%.

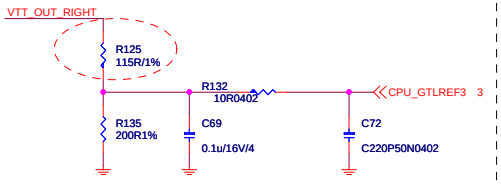




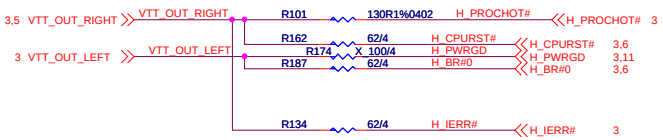
GTLREF VOLTAGE SHOULD BE 0.635*VTT = 0.76V

Reserved for Kentsfield (Q-core)



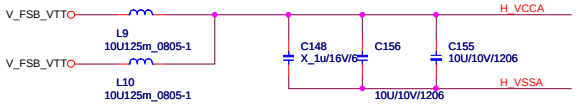


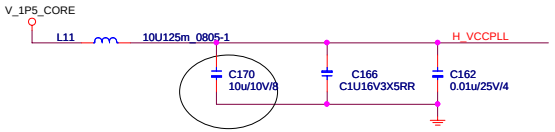
PLACE AT CPU END OF ROUTE



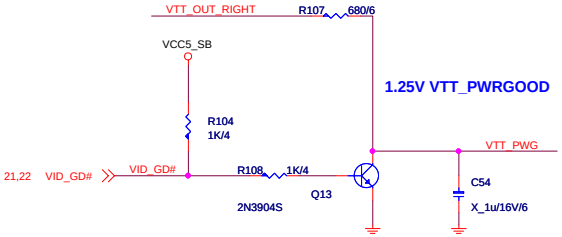
PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET

TRACE WIDTH TO CAPS MUST BE SMALLER THAN 12MILS

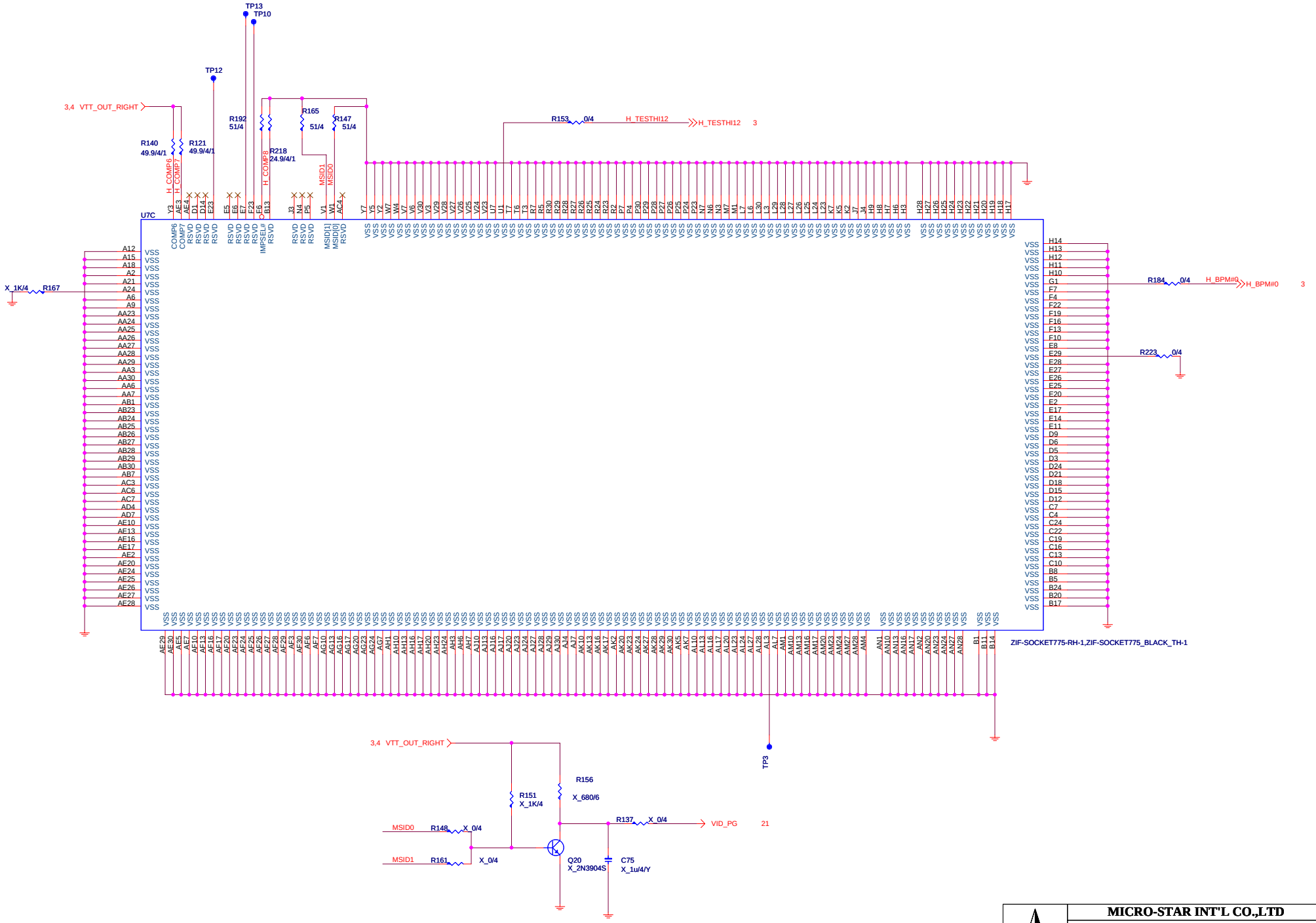




VTT_PWG SPEC :
High > 0.9V
Low < 0.3V
Trise < 150ns



MICRO-STAR INT'L CO.,LTD		
MS-7357		
Size: Custom	Document Description: Intel LGA775 CPU - Power	Rev: 1.0
Date: Tuesday, May 08, 2007	Sheet 4 of 35	



MICRO-STAR INT'L CO.,LTD		
MS-7357		
Size: Custom	Document Description: Intel LGA775 CPU - GND	Rev: 1.0
Date: Wednesday, March 28, 2007	Sheet 5 of 35	

U1MCH

U12B

FSB

INTEL-LE82G33-A2[SLA9Q]-RH

1 OF 7

U12A

U1MCH

PCIE

DMI

INTEL-LE82G33-A2[SLA9Q]-RH

2 OF 7

V_1P25_CORE

C662 X_0.1u/16V/4
C663 X_0.1u/16V/4
C664 X_0.1u/16V/4
C665 X_0.1u/16V/4
C666 X_0.1u/16V/4
C667 X_0.1u/16V/4
C668 X_0.1u/16V/4
C669 X_0.1u/16V/4
C670 X_0.1u/16V/4

Reserved for non-Graphic sku

HSYNC R264 0/4
VSYNC R262 0/4
CK_96M_DREF# R271 0/4
CK_96M_DREF R270 10K/4 V_1P25_CORE

Close to GMCH.
Change to 0-ohm for non-Graphic sku
Change to 1.3K-ohm 1% for Graphic sku

DACREFSET R252 0/4

U12E

VGA

MISC

INTEL-LE82G33-A2[SLA9Q]-RH

5 OF 7

R276 X_1K/4 MTYPE
R279 X_1K/4 EXP_SLR
R296 0/4 EXP_EN
R278 X_1K/4 MCH_RFU_G15
R273 X_1K/4 MCH_TCEN

PIN	H	L	Description
MTYPE	DDR2	DDR3	MEMORY TYPE
EXP_SLR	Normal	Reverse	PCI_E Lane Reversal
EXP_EN	Concurrent	Non-concurrent	PCI_E/SDVO co-existence
MCH_TCEN	Enable	Disable	TLS confidentiality

R293 0/4

V_FSB_VTT
R242 49.9R1%/2 C220 X_C2.7P25N2
R243 49.9R1%/2 C221 X_C2.7P25N2
R246 16.5R1%/2

***GTLREF VOLTAGE SHOULD BE 0.67*VTT=0.8V (At VTT=1.2V)**

R239 100R1%
R245 51/4/1%
R238 200R1%
C217 1u/16V/6
C227 C220P50N2
CPU_MCH_GTLREF

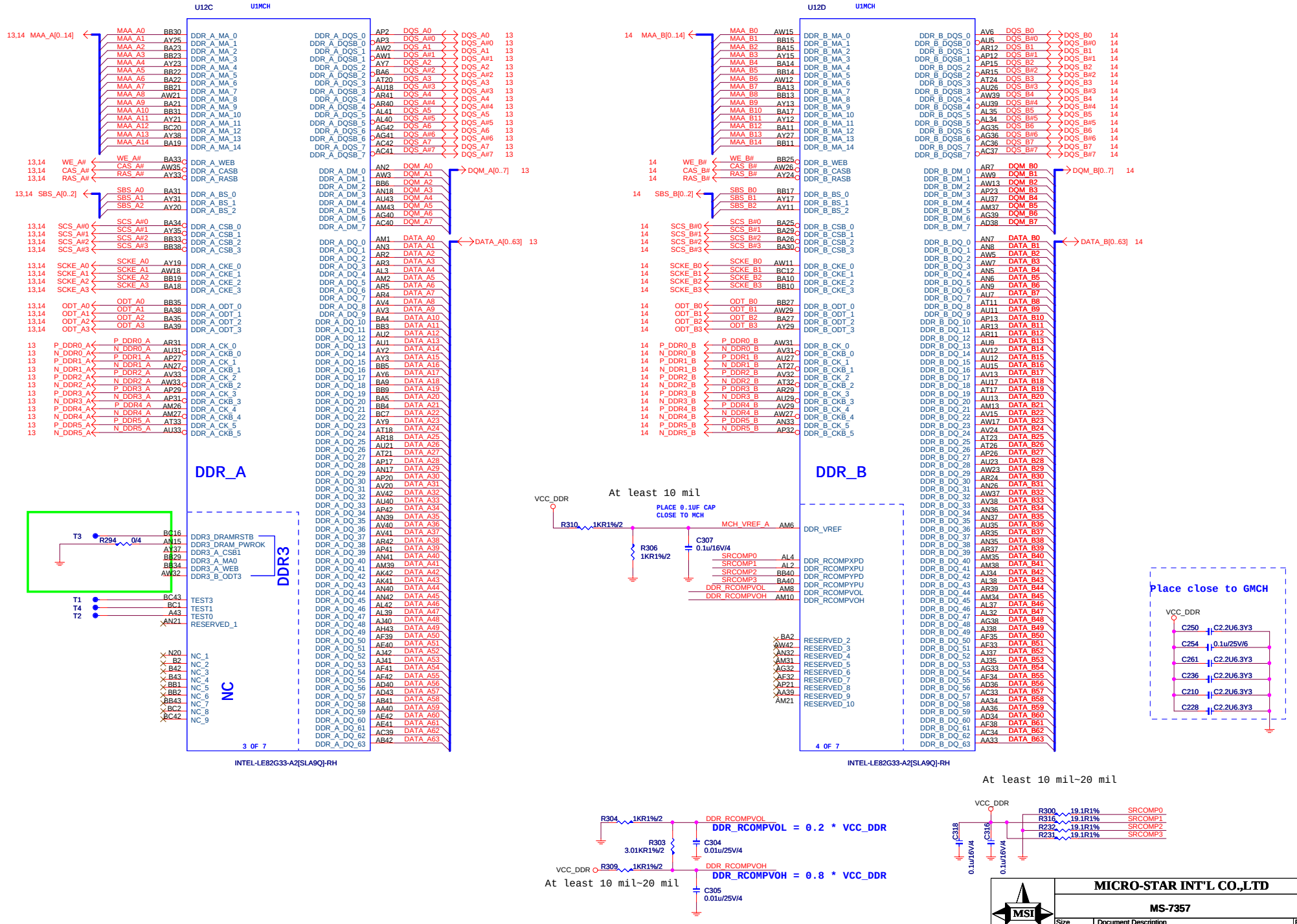
HXSWING SHOULD BE 1/4*VTT

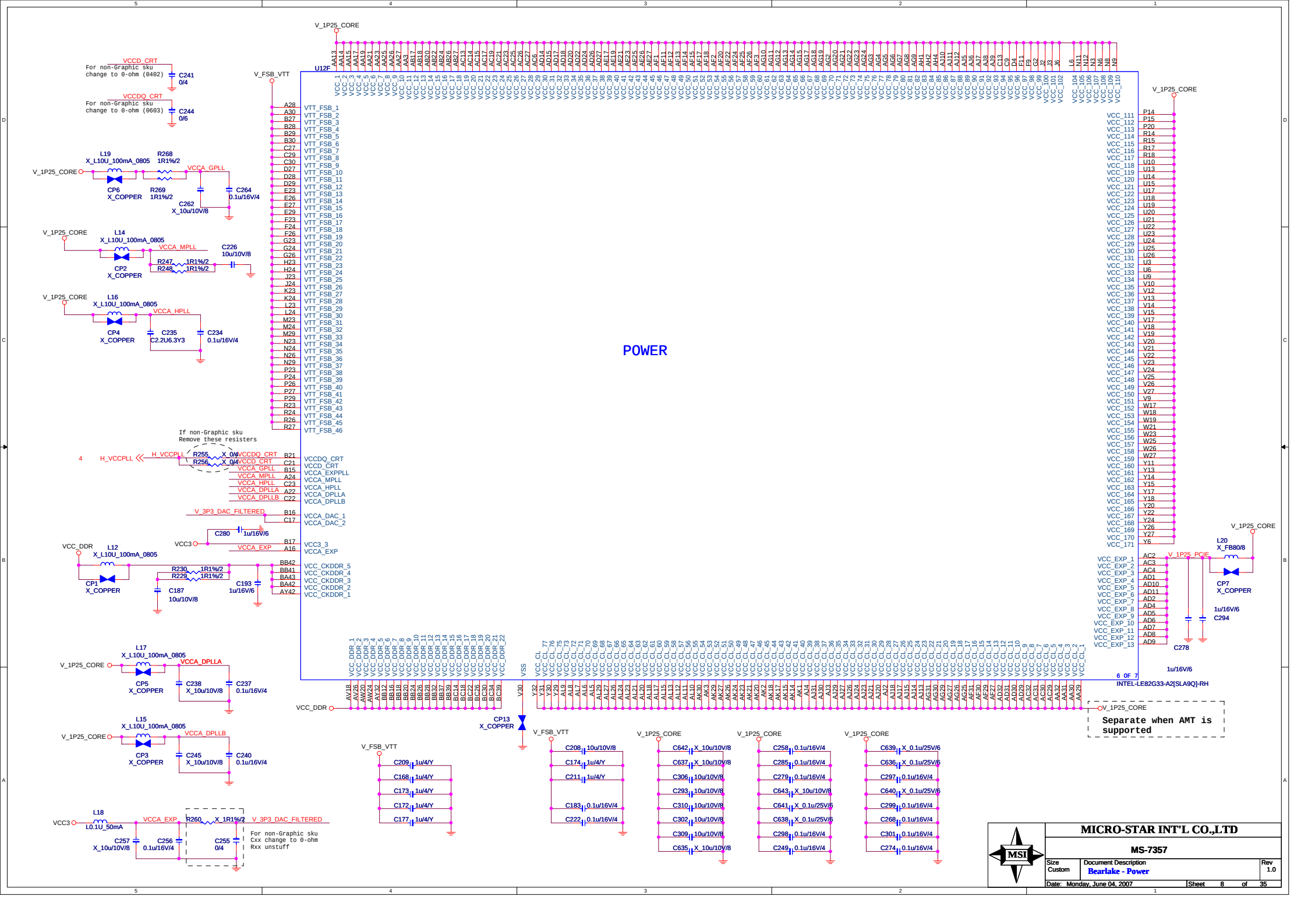
R240 301R1%0402
R244 49.9R1%/2
R241 100R1%/2
C219 0.01u/25V/4

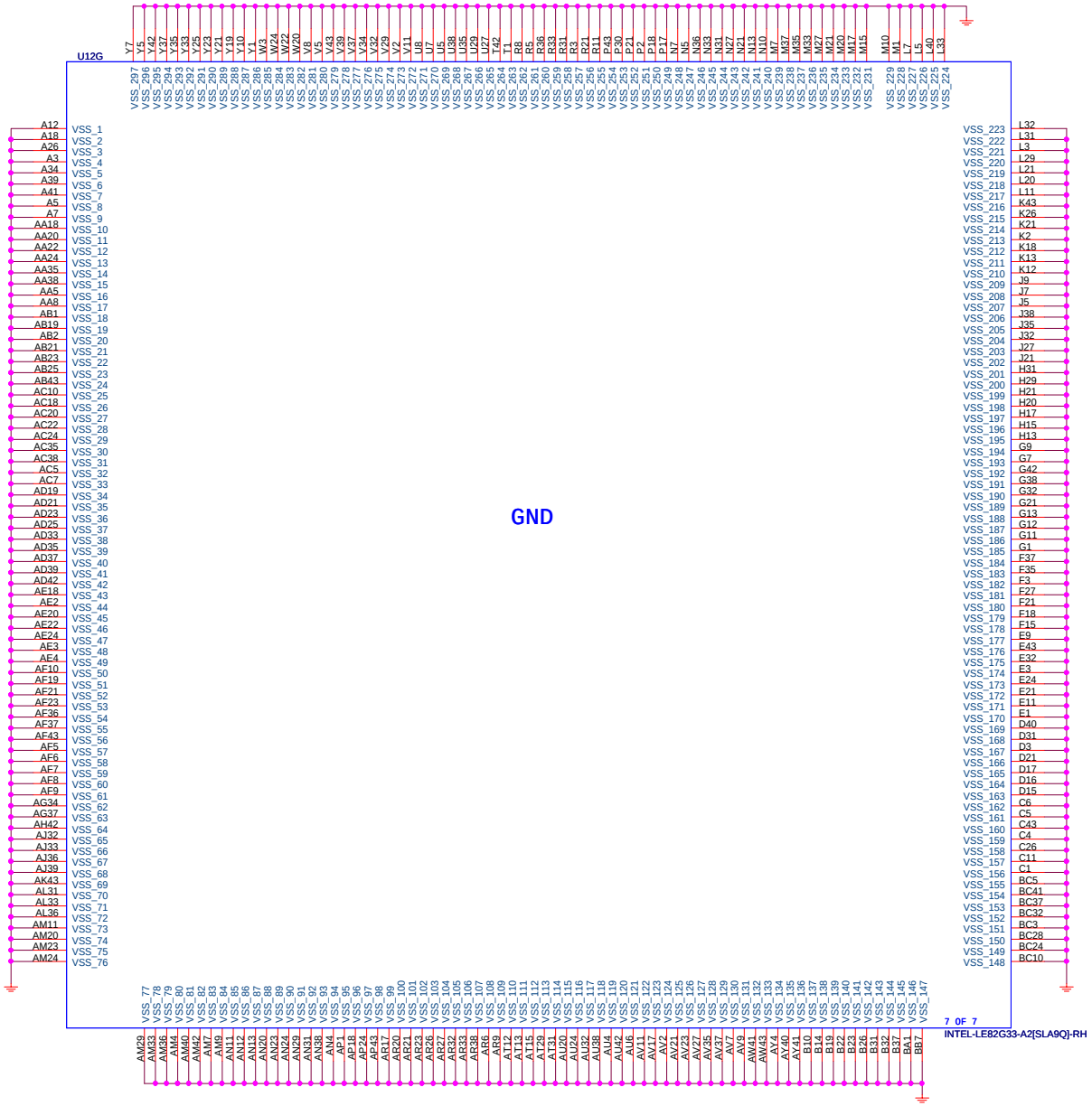
CL_VREF_MCH = 0.349V
Close to GMCH

R297 1KR1%/2
R298 392R1%/2
C295 0.1u/16V/4

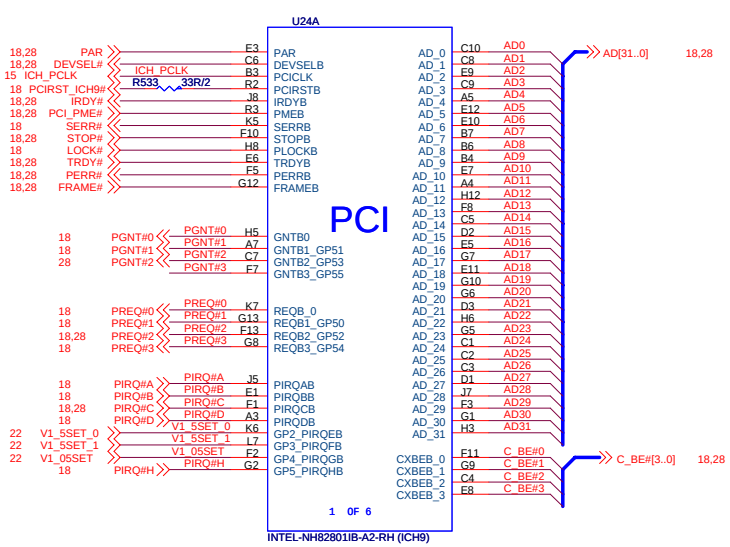
MICRO-STAR INT'L CO.,LTD	
MS-7357	
Size: Custom	Document Description: Bearlake - FSB, PCIE, DMI, VGA, MSIC
Rev: 1.0	
Date: Tuesday, May 29, 2007	Sheet 6 of 35

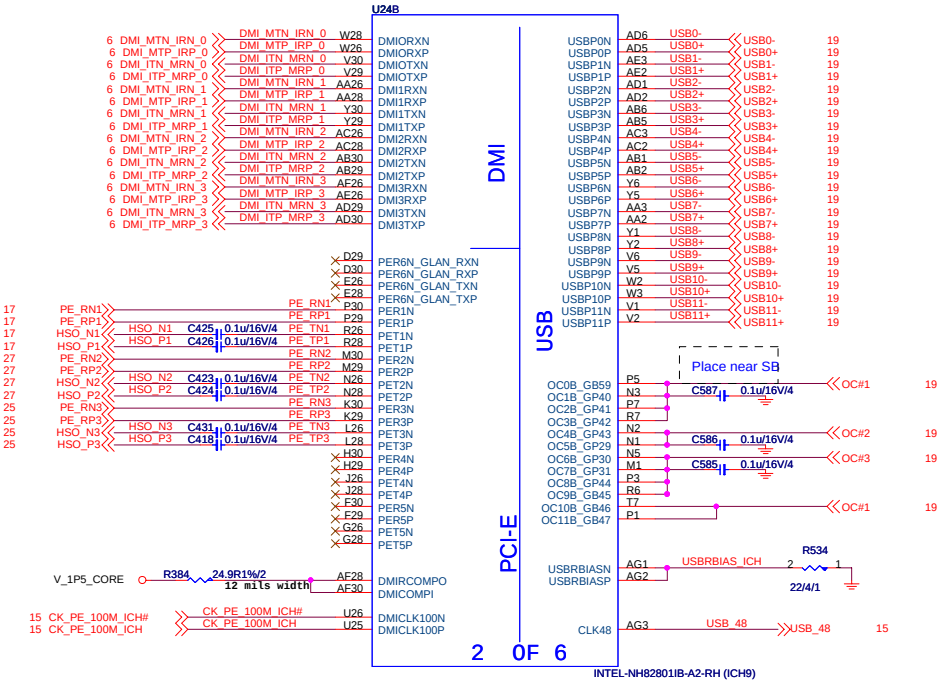

U12C
U1MCH
DDR_A
DDR3
NC
3 OF 7
INTEL-LE82G33-A2[SLA9Q]-RH
U12D
U1MCH
DDR_B
4 OF 7
INTEL-LE82G33-A2[SLA9Q]-RH
At least 10 mil
PLACE 0.1UF CAP
CLOSE TO MCH
VCC_DDR
R310 1KR1%/2
R306 1KR1%/2
C307 0.1u/16V/4
MCH_VREF_A
SRCOMP0
SRCOMP1
SRCOMP2
SRCOMP3
DDR_RCOMPVOL
DDR_RCOMPVOH
Place close to GMCH
C250 C2.2U6.3Y3
C254 0.1u/25V/6
C261 C2.2U6.3Y3
C236 C2.2U6.3Y3
C210 C2.2U6.3Y3
C228 C2.2U6.3Y3
At least 10 mil~20 mil
R304 1KR1%/2
R303 3.01KR1%/2
R309 1KR1%/2
C304 0.01u/25V/4
C305 0.01u/25V/4
DDR_RCOMPVOL = 0.2 * VCC_DDR
DDR_RCOMPVOH = 0.8 * VCC_DDR
At least 10 mil~20 mil
R300 19.1R1%
R316 19.1R1%
R232 19.1R1%
R231 19.1R1%
C318 0.1u/16V/4
C316 0.1u/16V/4
MICRO-STAR INT'L CO.,LTD
MS-7357
Size Custom
Document Description
Bearlake - Memory
Rev 1.0
Date: Tuesday, May 15, 2007
Sheet 7 of 35

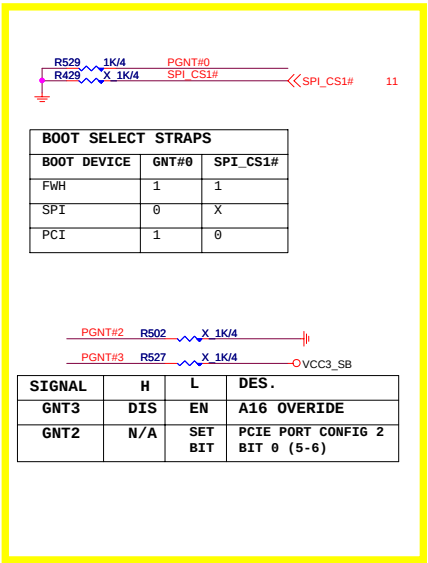

POWER
U12F
INTEL-LE82G33-A2[SLA9Q]-RH
6 OF 7
V_1P25_CORE
V_FSB_VTT
V_3P3_DAC_FILTERED
VCC_DDR
VCC3
V_1P25_PCIE
VCCD_CRT
For non-Graphic sku
change to 0-ohm (0402)
C241
0/4
VCCDQ_CRT
For non-Graphic sku
change to 0-ohm (0603)
C244
0/6
L19
X_L10U_100mA_0805
R268
1R1%/2
VCCA_GPLL
CP6
X_COPPER
R269
1R1%/2
C264
0.1u/16V/4
C262
X_10u/10V/8
L14
X_L10U_100mA_0805
VCCA_MPLL
C226
10u/10V/8
CP2
X_COPPER
R247
R248
1R1%/2
L16
X_L10U_100mA_0805
VCCA_HPLL
CP4
X_COPPER
C235
C2.2U6.3Y3
C234
0.1u/16V/4
If non-Graphic sku
Remove these resisters
H_VCCPLL
R255
R256
X_0/4
L12
X_L10U_100mA_0805
R230
R229
1R1%/2
CP1
X_COPPER
C187
10u/10V/8
C193
1u/16V/6
C280
1u/16V/6
VCCA_EXP
L17
X_L10U_100mA_0805
VCCA_DPLLA
CP5
X_COPPER
C238
X_10u/10V/8
C237
0.1u/16V/4
L15
X_L10U_100mA_0805
VCCA_DPLLB
CP3
X_COPPER
C245
X_10u/10V/8
C240
0.1u/16V/4
L18
L0.1U_50mA
R260
X_1R1%/2
C257
X_10u/10V/8
C256
0.1u/16V/4
C255
0/4
For non-Graphic sku
Cxx change to 0-ohm
Rxx unstuff
CP13
X_COPPER
C209
1u/4/Y
C168
1u/4/Y
C173
1u/4/Y
C172
1u/4/Y
C177
1u/4/Y
C208
10u/10V/8
C174
1u/4/Y
C211
1u/4/Y
C183
0.1u/16V/4
C222
0.1u/16V/4
C642
X_10u/10V/8
C637
X_10u/10V/8
C306
10u/10V/8
C293
10u/10V/8
C310
10u/10V/8
C302
10u/10V/8
C309
10u/10V/8
C635
X_10u/10V/8
C258
0.1u/16V/4
C285
0.1u/16V/4
C279
0.1u/16V/4
C643
X_10u/10V/8
C641
X_0.1u/25V/6
C638
X_0.1u/25V/6
C298
0.1u/16V/4
C249
0.1u/16V/4
C639
X_0.1u/25V/6
C636
X_0.1u/25V/6
C297
0.1u/16V/4
C640
X_0.1u/25V/6
C299
0.1u/16V/4
C268
0.1u/16V/4
C301
0.1u/16V/4
C274
0.1u/16V/4
L20
X_FB80/8
CP7
X_COPPER
C294
1u/16V/6
C278
1u/16V/6
Separate when AMT is supported
MICRO-STAR INT'L CO.,LTD
MS-7357
Size
Custom
Document Description
Bearlake - Power
Rev
1.0
Date: Monday, June 04, 2007
Sheet 8 of 35



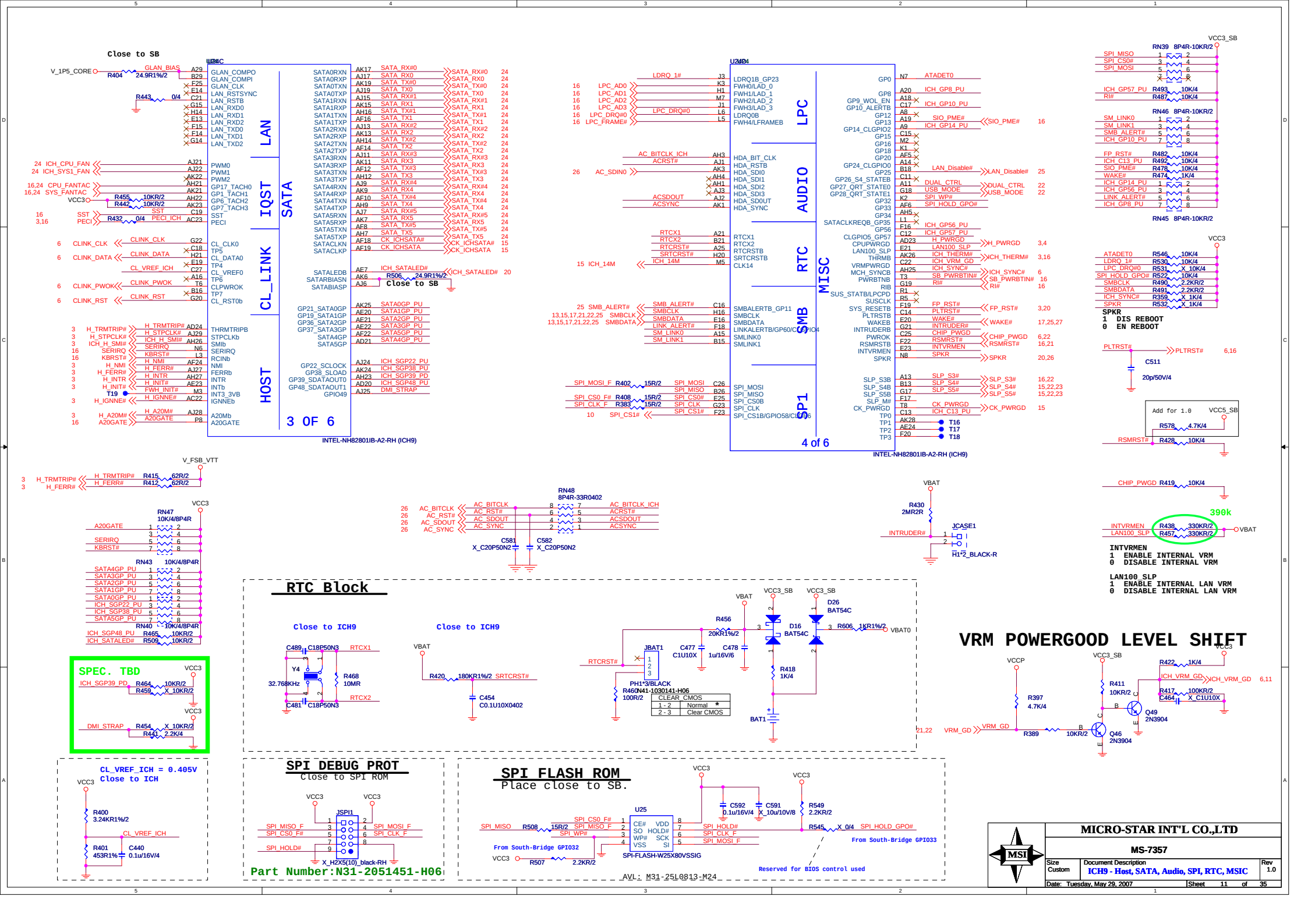
MICRO-STAR INT'L CO.,LTD	
MS-7357	
Size: Custom	Document Description: Bearlake - GND
Rev: 1.0	
Date: Tuesday, May 15, 2007	Sheet 9 of 35

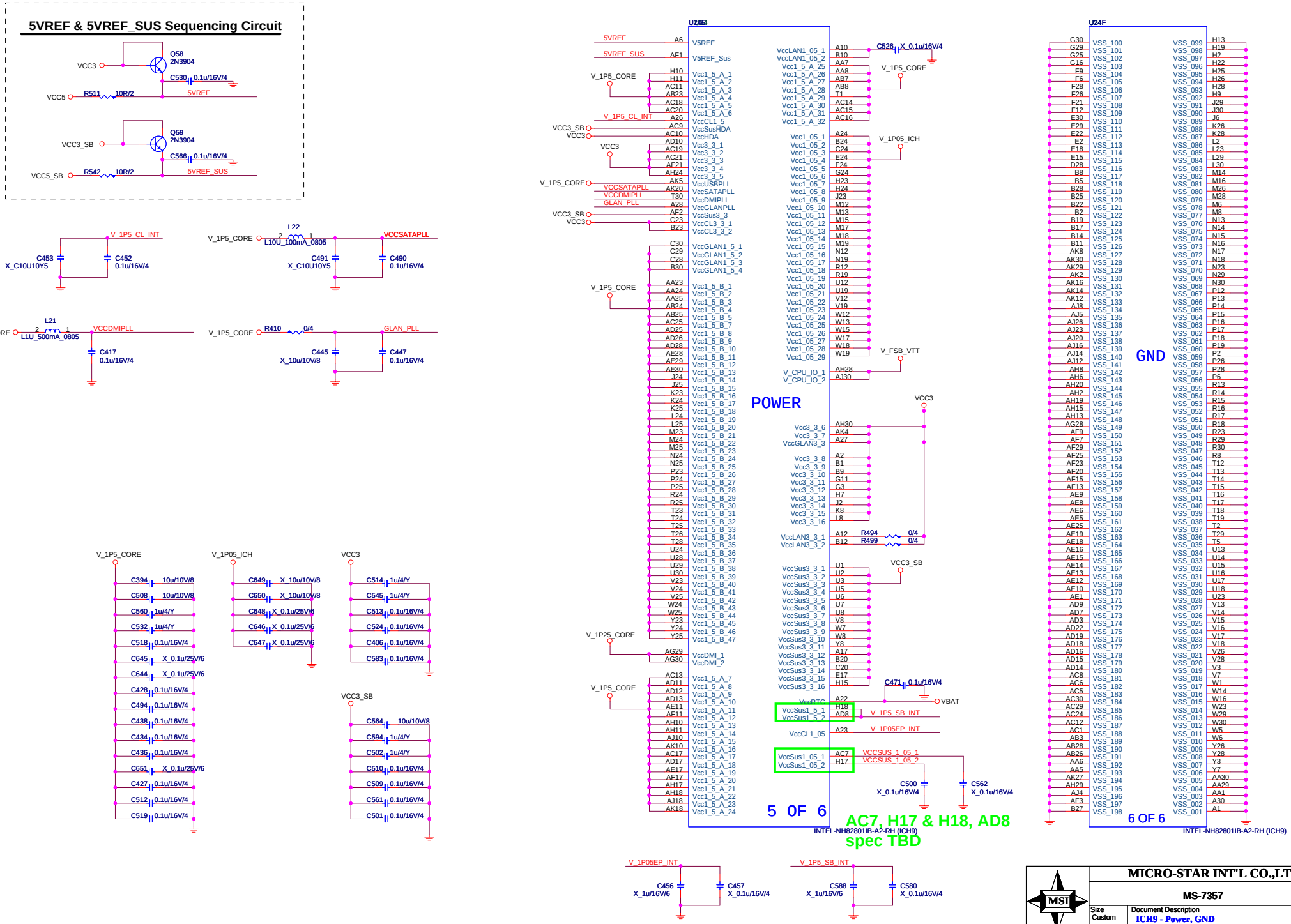


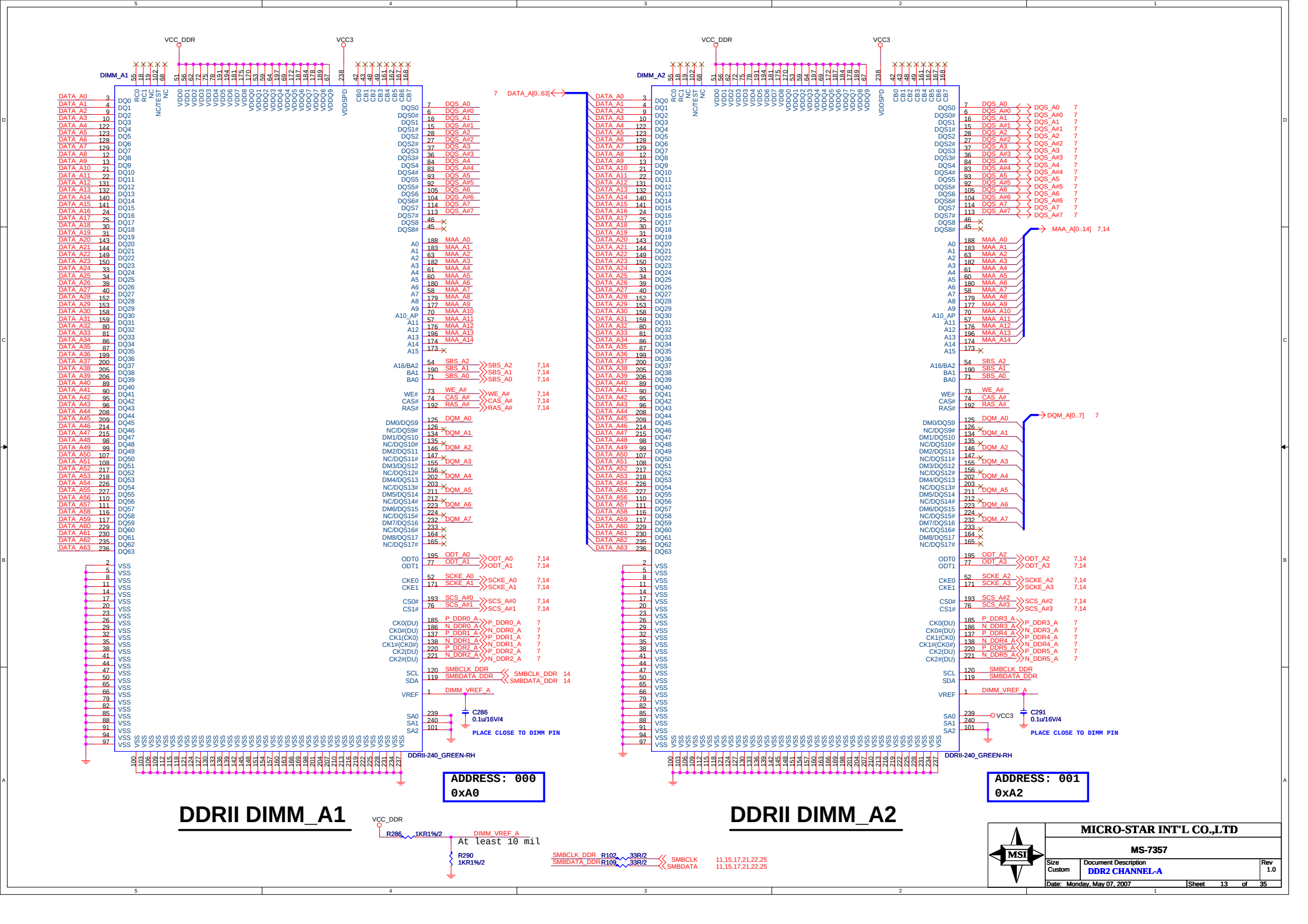




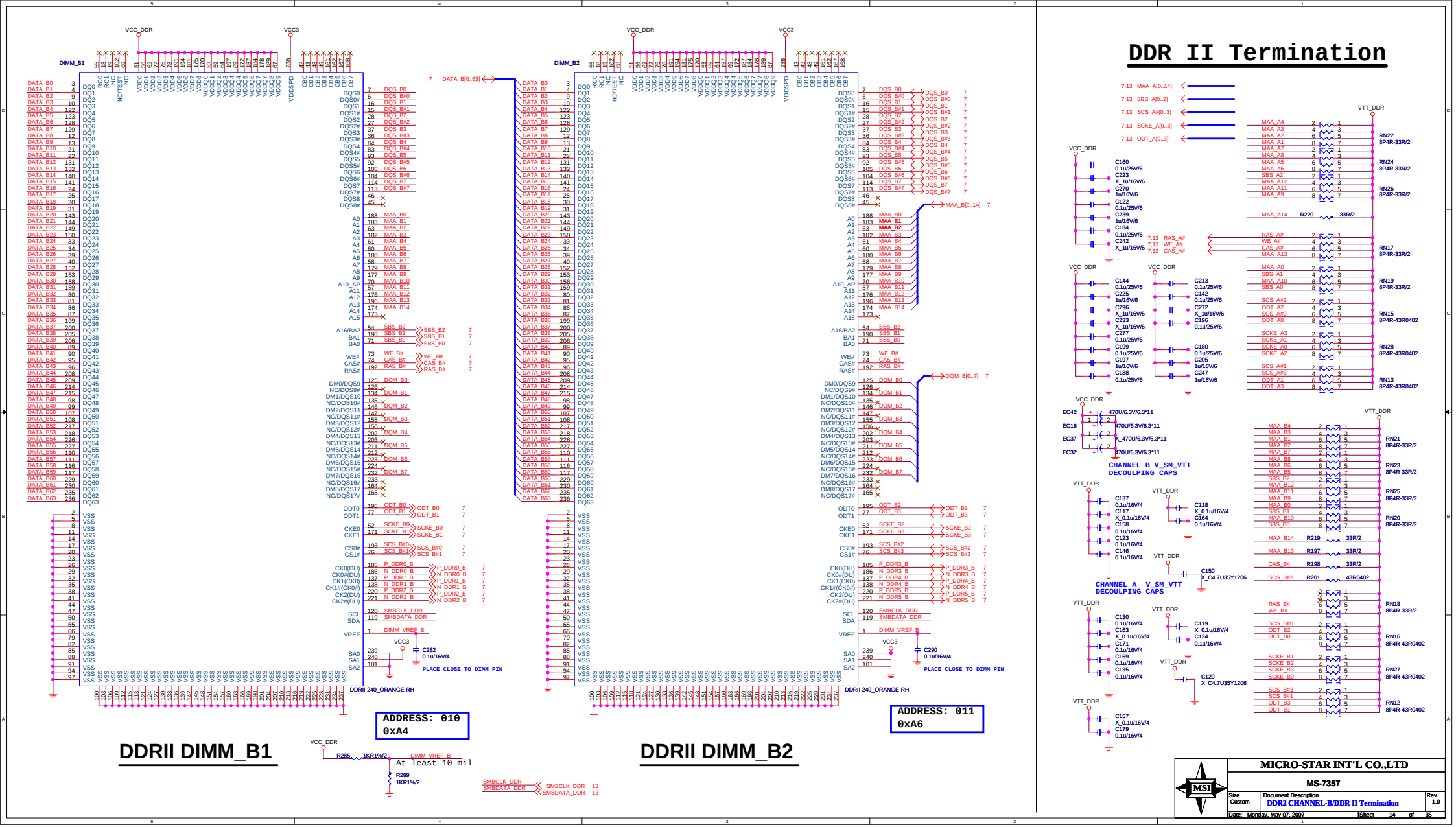
MICRO-STAR INT'L CO.,LTD			
MS-7357			
Size: Custom	Document Description: ICH9 - PCI, DMI, USB, PCIE & Slots		Rev: 1.0
Date: Tuesday, May 29, 2007		Sheet 10 of 35	


Close to SB
U28C
V_1P5_CORE
GLAN_BIAS
R404 24.9R1%/2
R443 0/4
GLAN_COMPO
GLAN_COMPI
GLAN_CLK
LAN_RSTSYNC
LAN_RSTB
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
LAN
IQST
CL_LINK
HOST
SATA
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA3RXN
SATA3RXP
SATA3TXN
SATA3TXP
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATACLKN
SATACLKP
SATA_RX#0
SATA_RX0
SATA_TX#0
SATA_TX0
SATA_RX#1
SATA_RX1
SATA_TX#1
SATA_TX1
SATA_RX#2
SATA_RX2
SATA_TX#2
SATA_TX2
SATA_RX#3
SATA_RX3
SATA_TX#3
SATA_TX3
SATA_RX#4
SATA_RX4
SATA_TX#4
SATA_TX4
SATA_RX#5
SATA_RX5
SATA_TX#5
SATA_TX5
CK_ICHSATA#
CK_ICHSATA
SATALEDB
SATARBIASN
SATABIASP
ICH_SATALED#
R506 24.9R1%/2
Close to SB
GP21_SATA0GP
GP19_SATA1GP
GP36_SATA2GP
GP37_SATA3GP
SATA4GP
SATA5GP
SATA0GP_PU
SATA1GP_PU
SATA2GP_PU
SATA3GP_PU
SATA4GP_PU
SATA5GP_PU
GP22_SCLOCK
GP38_SLOAD
GP39_SDATAOUT0
GP48_SDATAOUT1
GPIO49
ICH_SGP22_PU
ICH_SGP38_PU
ICH_SGP39_PD
ICH_SGP48_PU
DMI_STRAP
3 OF 6
INTEL-NH82801IB-A2-RH (ICH9)
U28D
LDRQ_1#
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_DRQ#0
LPC_FRAME#
LDRQ1B_GP23
FWH0/LAD_0
FWH1/LAD_1
FWH2/LAD_2
FWH3/LAD_3
LDRQ0B
FWH4/LFRAMEB
LPC
AC_BITCLK_ICH
ACRST#
AC_SDIN0
ACSDOUT
ACSYNC
HDA_BIT_CLK
HDA_RSTB
HDA_SDI0
HDA_SDI1
HDA_SDI2
HDA_SDI3
HDA_SD0UT
HDA_SYNC
AUDIO
RTCX1
RTCX2
RTCRST#
SRTCRST#
ICH_14M
RTCRSTB
SRTCRSTB
CLK14
RTC
SMB_ALERT#
SMBCLK
SMBDATA
LINK_ALERT#
SM_LINK0
SM_LINK1
SMBALERTB_GP11
LINKALERTB/GP60/CLKRUN#
SMLINK0
SMLINK1
SMB
SPI_MOSI_F
SPI_CS0_F#
SPI_CLK_F
SPI_CS1#
SPI_MOSI
SPI_MISO
SPI_CS0#
SPI_CLK
SPI_CS1/GPIO58/CLKRUN#
SPI
GP0
GP8
GP9_WOL_EN
GP10_ALERTB
GP12
GP13
GP14_CLGPIO2
GP15
GP16
GP18
GP20
GP24_CLGPIO0
GP25
GP26_S4_STATEB
GP27_QRT_STATE0
GP28_QRT_STATE1
GP32
GP33
GP34
SATACLKREQB_GP35
GP56
CLGPIO5_GP57
CPUPWRGD
LAN100_SLP
THRMB
VRMPWRGD
MCH_SYNCB
PWRBTNB
RIB
SUS_STATB/LPCPD
SUSCLK
SYS_RESETB
PLTRSTB
WAKEB
INTRUDERB
PWROK
RSMRSTB
INTVRMEN
SPKR
SLP_S3B
SLP_S4B
SLP_S5B
SLP_M#
CK_PWRGD
TP0
TP1
TP2
TP3
ATADET0
ICH_GP8_PU
ICH_GP10_PU
SIO_PME#
LAN_Disable#
DUAL_CTRL
USB_MODE
SPI_WP#
SPI_HOLD_GPO#
ICH_GP56_PU
ICH_GP57_PU
H_PWRGD
LAN100_SLP
ICH_THERM#
ICH_VRM_GD
ICH_SYNC#
SB_PWRBTIN#
RI#
PLTRST#
FP_RST#
WAKE#
INTRUDER#
CHIP_PWGD
RSMRST#
INTVRMEN
SPKR
SLP_S3#
SLP_S4#
SLP_S5#
CK_PWRGD
ICH_C13_PU
T16
T17
T18
4 of 6
MISC
INTEL-NH82801IB-A2-RH (ICH9)
VCC3_SB
RN39 8P4R-10KR/2
SPI_MISO
SPI_CS0#
SPI_MOSI
ICH_GP57_PU R493 10K/4
RI# R487 10K/4
RN46 8P4R-10KR/2
SM_LINK0
SM_LINK1
SMB_ALERT#
ICH_GP10_PU
FP_RST# R482 10K/4
ICH_C13_PU R492 10K/4
SIO_PME# R478 10K/4
WAKE# R474 1K/4
ICH_GP14_PU
ICH_GP56_PU
LINK_ALERT# R475 10K/4
ICH_GP8_PU
RN45 8P4R-10KR/2
VCC3
ATADET0 R546 10K/4
LDRQ_1# R530 10K/4
LPC_DRQ#0 R531 X_10K/4
SPI_HOLD_GPO# R522 10K/4
SMBCLK R496 2.2KR/2
SMBDATA R491 2.2KR/2
ICH_SYNC# R359 X_1K/4
SPKR R532 X_1K/4
SPKR
1 DIS REBOOT
0 EN REBOOT
PLTRST#
PLTRST# 6,16
C511
20p/50V/4
Add for 1.0
VCC5_SB
R578 4.7K/4
RSMRST# R428 10K/4
V_FSB_VTT
H_TRMTRIP# R415 62R/2
H_FERR# R412 62R/2
VCC3
RN47 10K/4/8P4R
A20GATE
SERIRQ
KBRST#
RN43 10K/4/8P4R
SATA4GP_PU
SATA3GP_PU
SATA2GP_PU
SATA1GP_PU
SATA0GP_PU
ICH_SGP22_PU
ICH_SGP38_PU
SATA5GP_PU
RN40 10K/4/8P4R
ICH_SGP48_PU R465 10K/2
ICH_SATALED# R509 10K/2
SPEC. TBD
ICH_SGP39_PD R464 10K/2
R459 X_10K/2
DMI_STRAP R454 X_10K/2
R441 2.2K/4
RN48 8P4R-33R0402
AC_BITCLK
AC_RST#
AC_SDOUT
AC_SYNC
AC_BITCLK_ICH
ACRST#
ACSDOUT
ACSYNC
C581 X_C20P50N2
C582 X_C20P50N2
VBAT
R430 2MR2R
INTRUDER#
JCASE1
H1*2_BLACK-R
CHIP_PWGD R419 10K/4
390k
INTVRMEN R438 330KR/2
LAN100_SLP R457 330KR/2
INTVRMEN
1 ENABLE INTERNAL VRM
0 DISABLE INTERNAL VRM
LAN100_SLP
1 ENABLE INTERNAL LAN VRM
0 DISABLE INTERNAL LAN VRM
RTC Block
Close to ICH9
Close to ICH9
C489 C18P50N3
Y4
32.768KHz
C481 C18P50N3
RTCX1
RTCX2
R468 10MR
VBAT
R420 180KR1%/2
SRTCRST#
C454 C0.1U10X0402
R456 20KR1%/2
D16 BAT54C
D26 BAT54C
R606 1KR1%/2
VBAT0
JBAT1
RTCRST#
C477 C1U10X
C478 1u/16V/6
R418 1K/4
PH1*3/BLACK
R460N41-1030141-H06
100R/2
CLEAR_CMOS
1 - 2 Normal
2 - 3 Clear CMOS
BAT1
VRM POWERGOOD LEVEL SHIFT
VCCP
R397 4.7K/4
R389 10KR/2
VRM_GD
21,22
VRM_GD
VCC3_SB
R411 10KR/2
R422 1K/4
ICH_VRM_GD
ICH_VRM_GD 6,11
R417 100KR/2
C464 X_C1U10X
Q49 2N3904
Q46 2N3904
CL_VREF_ICH = 0.405V
Close to ICH
R400 3.24KR1%/2
CL_VREF_ICH
R401 453R1%
C440 0.1u/16V/4
SPI DEBUG PROT
Close to SPI ROM
JSPI1
SPI_MISO_F
SPI_CS0_F#
SPI_HOLD#
SPI_MOSI_F
SPI_CLK_F
X_H2X5(10)_black-RH
Part Number:N31-2051451-H06
SPI FLASH ROM
Place close to SB.
U25
SPI-FLASH-W25X80VSSIG
SPI_MISO
R508 15R/2
SPI_CS0_F#
SPI_MISO_F
SPI_WP#
SPI_HOLD#
SPI_CLK_F
SPI_MOSI_F
From South-Bridge GPIO32
R507 2.2KR/2
C592 0.1u/16V/4
C591 X_10u/10V/8
R549 2.2KR/2
R545 X_0/4
SPI_HOLD_GPO#
From South-Bridge GPIO33
Reserved for BIOS control used
AVL: M31-25L0813-M24
MICRO-STAR INT'L CO.,LTD
MS-7357
Size Custom
Document Description
ICH9 - Host, SATA, Audio, SPI, RTC, MSIC
Rev 1.0
Date: Tuesday, May 29, 2007
Sheet 11 of 35

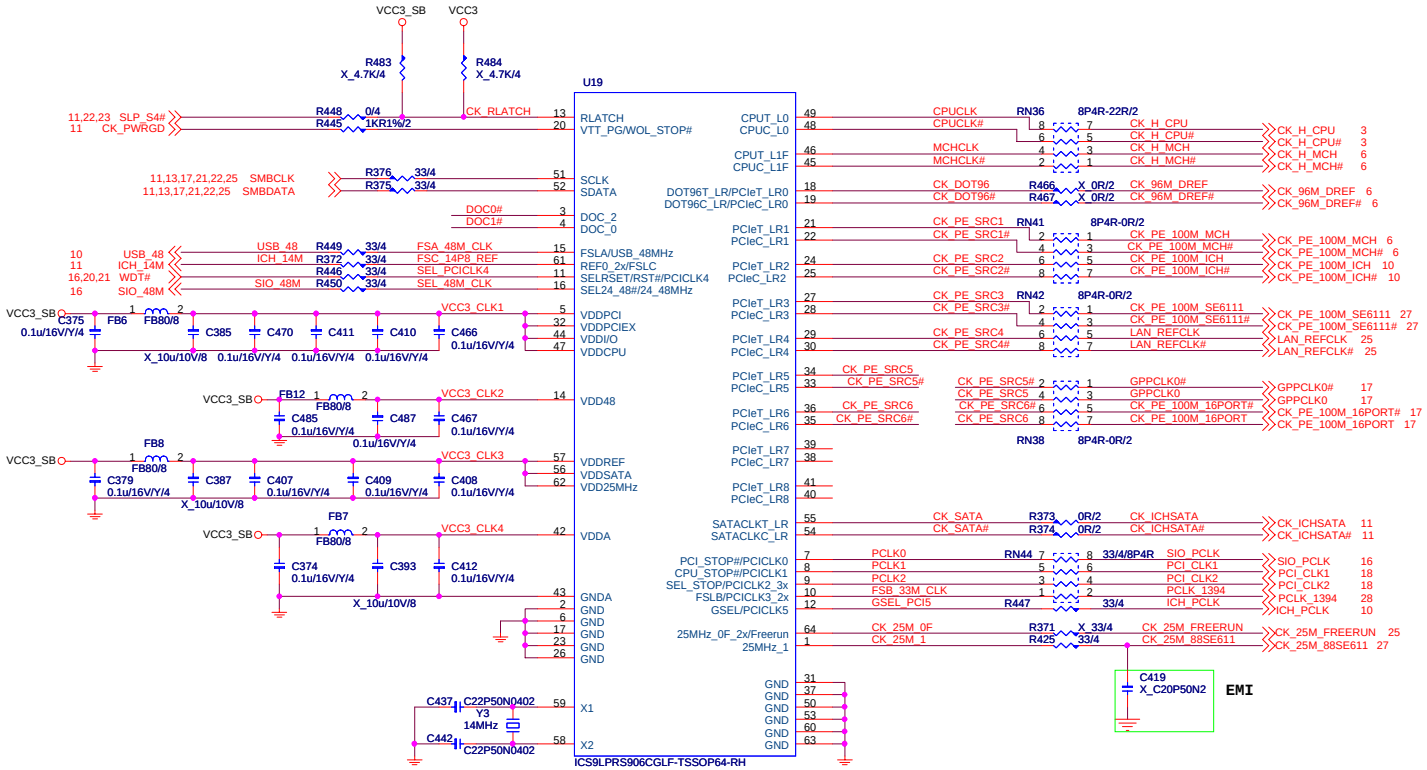

5VREF & 5VREF_SUS Sequencing Circuit
VCC3
Q58
2N3904
C530 0.1u/16V/4
VCC5
R511 10R/2
5VREF
VCC3_SB
Q59
2N3904
C566 0.1u/16V/4
VCC5_SB
R542 10R/2
5VREF_SUS
V_1P5_CL_INT
C453 X_C10U10Y5
C452 0.1u/16V/4
V_1P5_CORE
L22
L10U_100mA_0805
VCCSATAPLL
C491 X_C10U10Y5
C490 0.1u/16V/4
L21
L1U_500mA_0805
VCCDMIPLL
C417 0.1u/16V/4
R410 0/4
GLAN_PLL
C445 X_10u/10V/8
C447 0.1u/16V/4
V_1P05_ICH
C394 10u/10V/8
C508 10u/10V/8
C560 1u/4/Y
C532 1u/4/Y
C518 0.1u/16V/4
C645 X_0.1u/25V/6
C644 X_0.1u/25V/6
C428 0.1u/16V/4
C494 0.1u/16V/4
C438 0.1u/16V/4
C434 0.1u/16V/4
C436 0.1u/16V/4
C651 X_0.1u/25V/6
C427 0.1u/16V/4
C512 0.1u/16V/4
C519 0.1u/16V/4
C649 X_10u/10V/8
C650 X_10u/10V/8
C648 X_0.1u/25V/6
C646 X_0.1u/25V/6
C647 X_0.1u/25V/6
C514 1u/4/Y
C545 1u/4/Y
C513 0.1u/16V/4
C524 0.1u/16V/4
C406 0.1u/16V/4
C583 0.1u/16V/4
C564 10u/10V/8
C594 1u/4/Y
C502 1u/4/Y
C510 0.1u/16V/4
C509 0.1u/16V/4
C561 0.1u/16V/4
C501 0.1u/16V/4
U24E
5VREF
5VREF_SUS
V_1P5_CORE
V_1P5_CL_INT
VCC3_SB
VCC3
VCCSATAPLL
VCCDMIPLL
GLAN_PLL
POWER
5 OF 6
C526 X_0.1u/16V/4
V_1P05_ICH
V_FSB_VTT
VCC3
R494 0/4
R499 0/4
VCC3_SB
C471 0.1u/16V/4
VBAT
V_1P5_SB_INT
V_1P05EP_INT
VCCSUS_1_05_1
VCCSUS_1_05_2
C500 X_0.1u/16V/4
C562 X_0.1u/16V/4
V_1P25_CORE
AC7, H17 & H18, AD8
spec TBD
INTEL-NH82801IB-A2-RH (ICH9)
U24F
GND
6 OF 6
INTEL-NH82801IB-A2-RH (ICH9)
V_1P05EP_INT
C456 X_1u/16V/6
C457 X_0.1u/16V/4
V_1P5_SB_INT
C588 X_1u/16V/6
C580 X_0.1u/16V/4
MICRO-STAR INT'L CO.,LTD
MS-7357
Size Custom
Document Description
ICH9 - Power, GND
Rev 1.0
Date: Friday, March 30, 2007
Sheet 12 of 35


DIMM_A1
DDRII-240_GREEN-RH
ADDRESS: 000
0xA0
DDRII DIMM_A1
DIMM_A2
DDRII-240_GREEN-RH
ADDRESS: 001
0xA2
DDRII DIMM_A2
VCC_DDR
VCC3
C286
0.1u/16V/4
PLACE CLOSE TO DIMM PIN
C291
0.1u/16V/4
PLACE CLOSE TO DIMM PIN
R286 1KR1%/2
R290
1KR1%/2
At least 10 mil
R102 33R/2
R109 33R/2
MICRO-STAR INT'L CO.,LTD
MS-7357
Size
Custom
Document Description
DDR2 CHANNEL-A
Rev
1.0
Date: Monday, May 07, 2007
Sheet 13 of 35

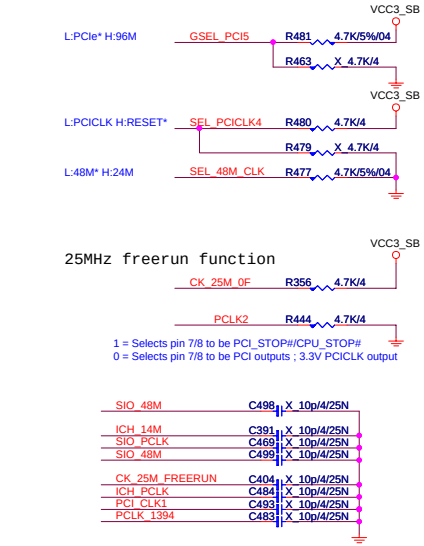
DDR II Termination

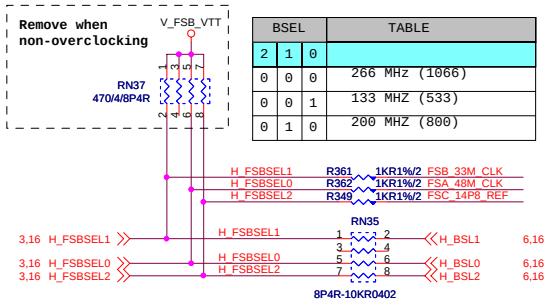


MICRO-STAR INT'L CO.,LTD	
MS-7357	
Size: Custom	Document Description: DDR2 CHANNEL-B/DDR II Termination
Rev: 1.0	
Date: Monday, May 07, 2007	Sheet 14 of 35

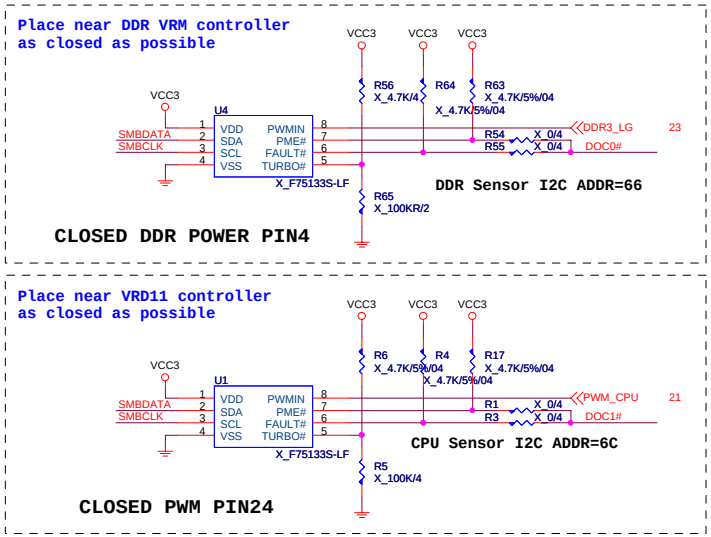


CLOCK GEN STRAPING

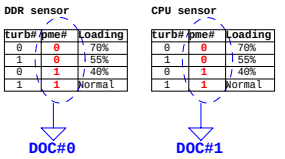




BSEL			TABLE
2	1	0	
0	0	0	266 MHz (1066)
0	0	1	133 MHZ (533)
0	1	0	200 MHZ (800)

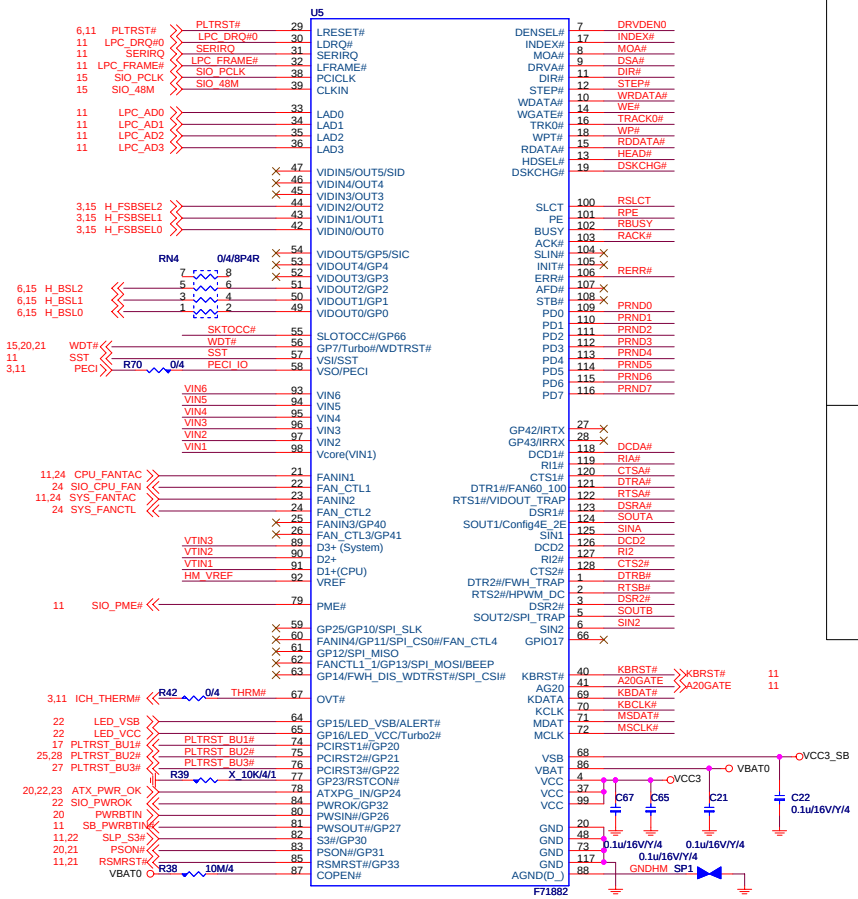


EASY DOT FUNCTION

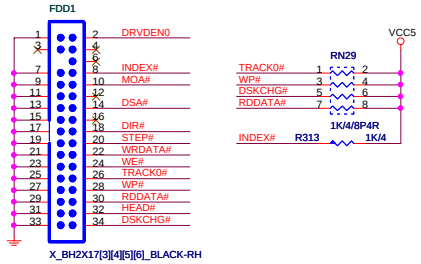


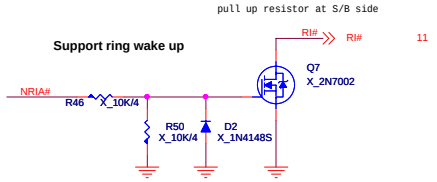
DOC#0	DOC#1	Over-clk
0	0	15%
1	0	10%
0	1	5%
1	1	Normal

MICRO-STAR INT'L CO.,LTD		
MS-7357		
Size: Custom	Document Description: ICS 9LPRS906 CLK Gen.	Rev: 1.0
Date: Tuesday, May 29, 2007	Sheet 15 of 35	

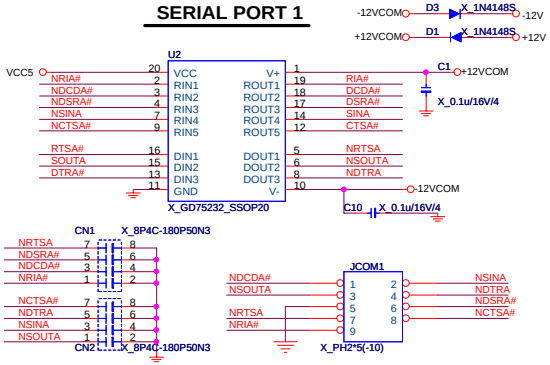


FLOPPY CONNECTOR

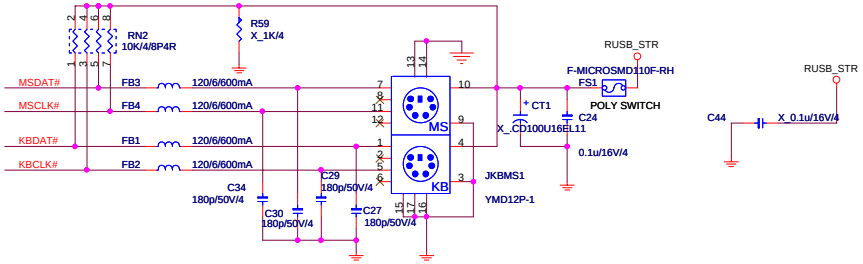




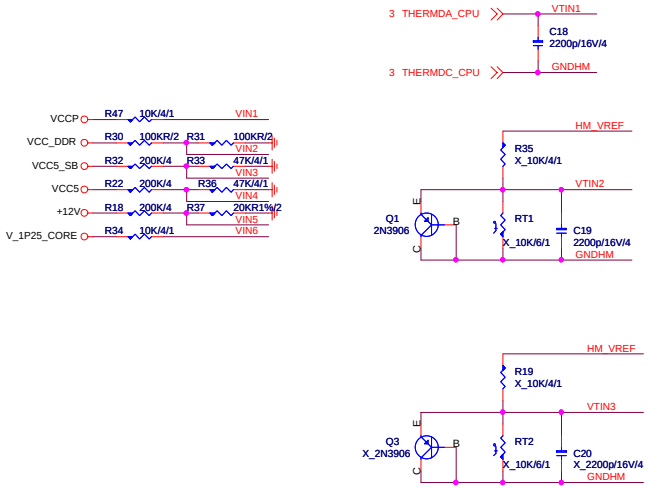
SERIAL PORT 1



PS2 KEYBOARD & MOUSE CONNECTOR



Thermal Resistor



LPC I/O STRAPPING RESISTOR

DTRB#(FWH_TRAP)
HI : SPI as a backup BIOS (Default)
LO : SPI as a primary BIOS

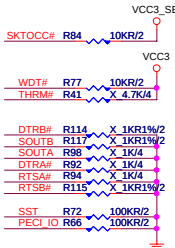
RTSB#(HPWM_DC)
HI : FAN control with PWM mode (Default)
LO : FAN control with Linear mode

SOUTB(SPI_TRAP)
HI : SPI function disable (Default)
LO : SPI function enable

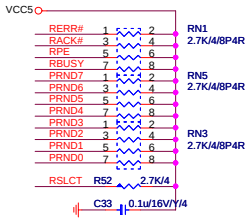
RTSA#(VIDOUT)
HI : 6 pins VIDIN and 6 pins VIDOUT (Default)
LO : VIDIN/VIDOUT on 6 pins, Original
VIDOUT pins will be GPIO pins

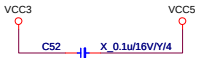
SOUTA(Config4E_2E)
HI : Configuration Register I/O port is 4E/4F (Default)
LO : Configuration Register I/O port is 2E/2F

DTRA#(FAN60_100)
HI : Power on FAN speed default duty is 60% (PWM) (Default)
LO : Power on FAN speed default duty is 100% (PWM)



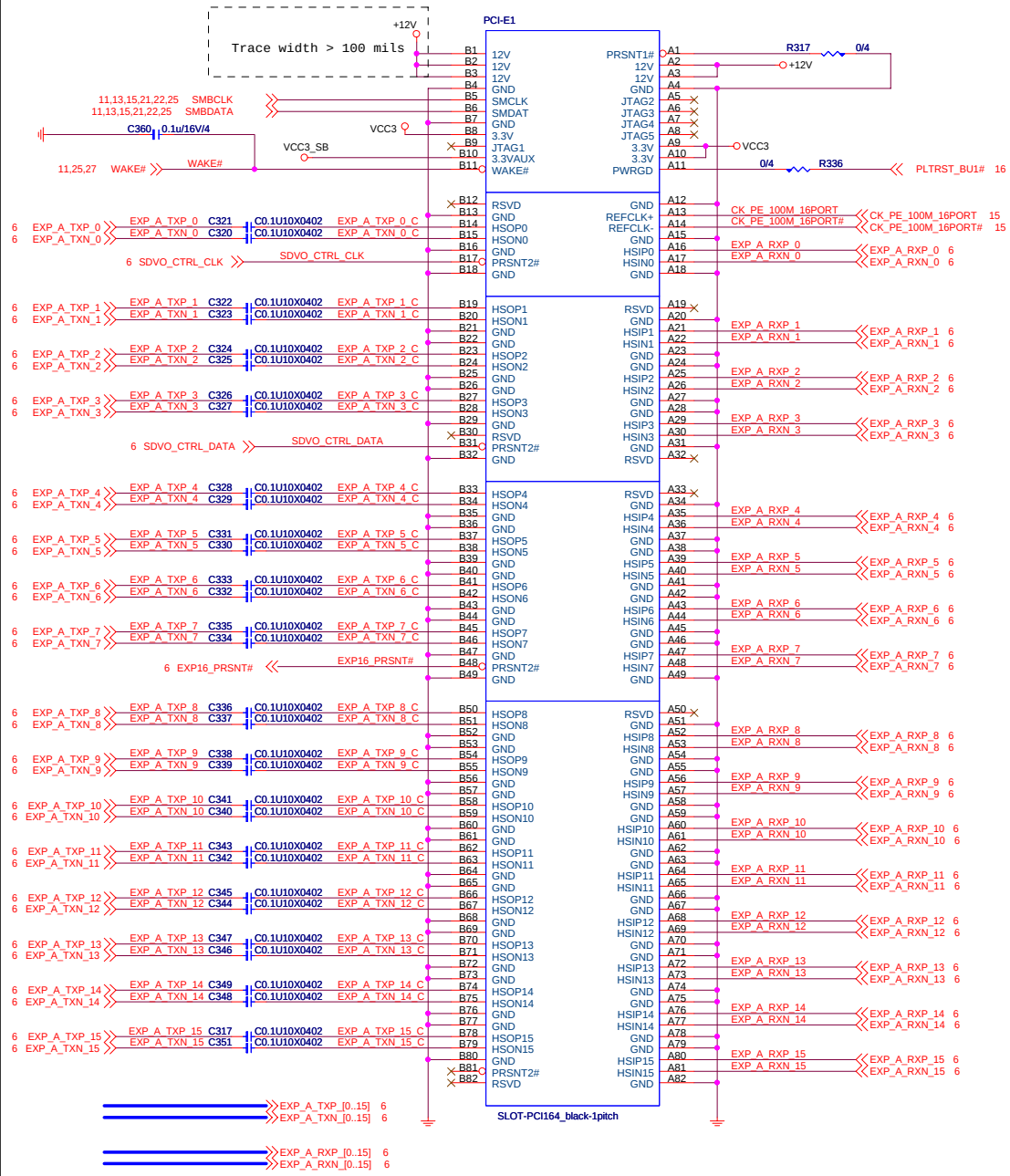
PARALLAL PORT

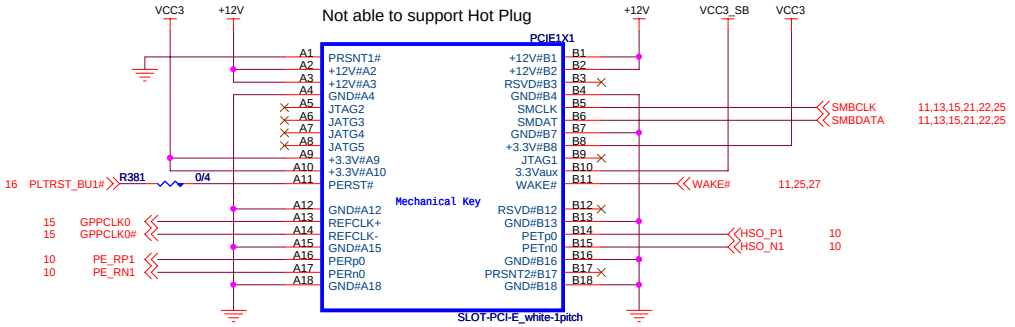


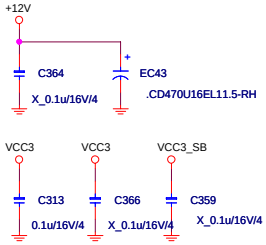


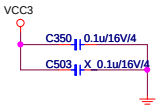
MICRO-STAR INT'L CO.,LTD	
MS-7357	
Size: Custom	Document Description: F71882FG, COM1, LPT, PS2
Rev: 1.0	
Date: Tuesday, May 29, 2007	Sheet 16 of 35

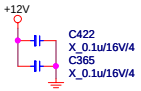
PCI EXPRESS 16-PORT

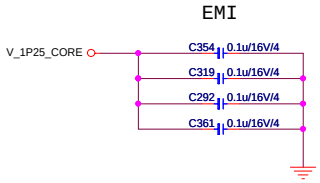






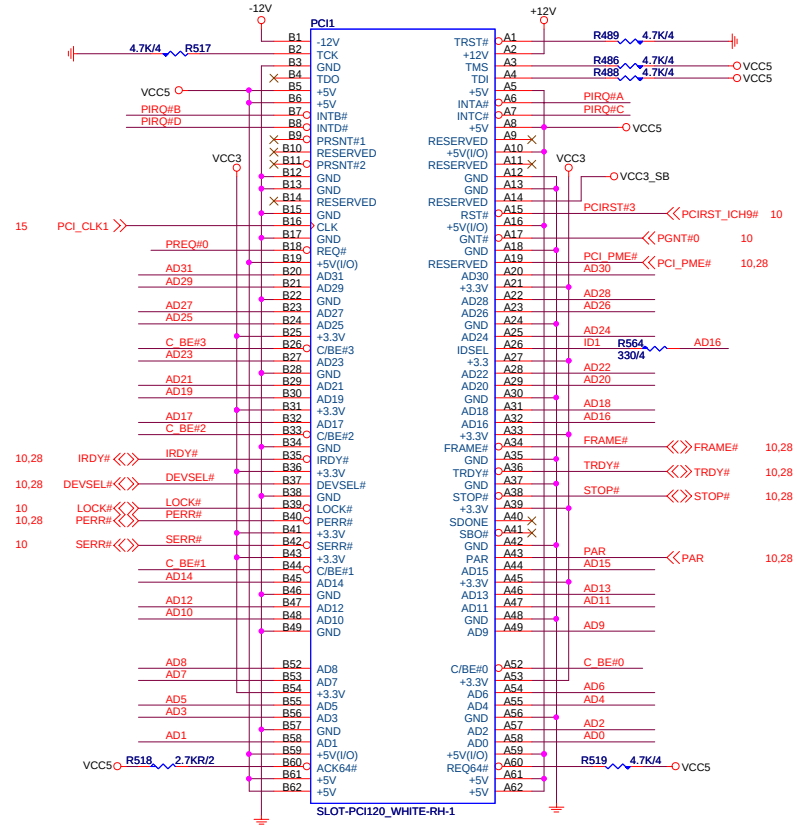






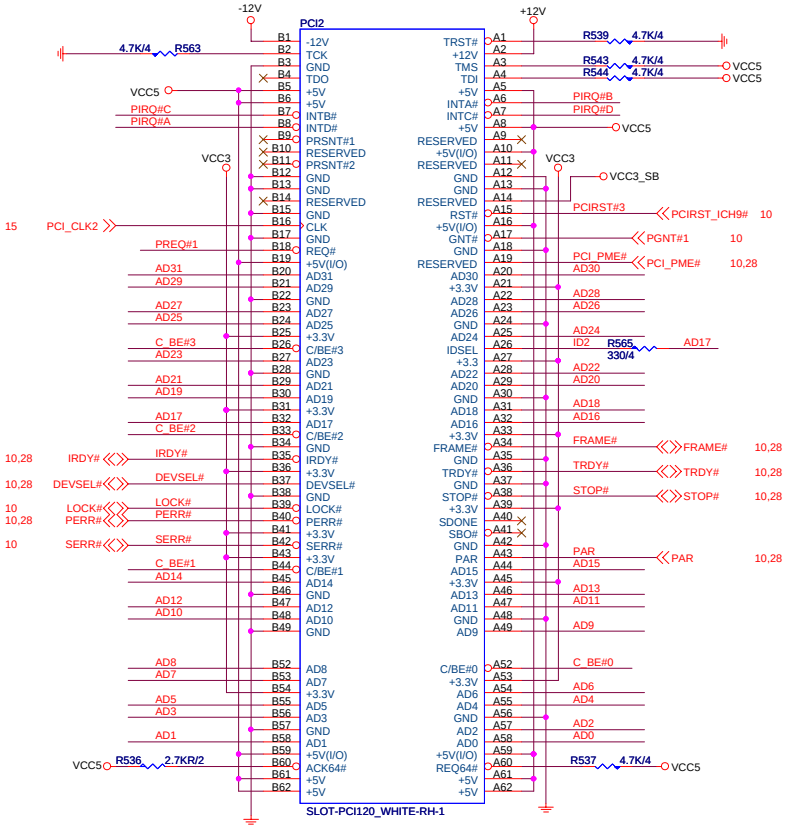
MICRO-STAR INT'L CO.,LTD		
MS-7357		
Size: Custom	Document Description: PCI-Express x16 & x1	Rev: 1.0
Date: Monday, March 26, 2007	Sheet 17 of 35	

PCI SLOT 1 (PCI VER: 2.2 COMPLY)



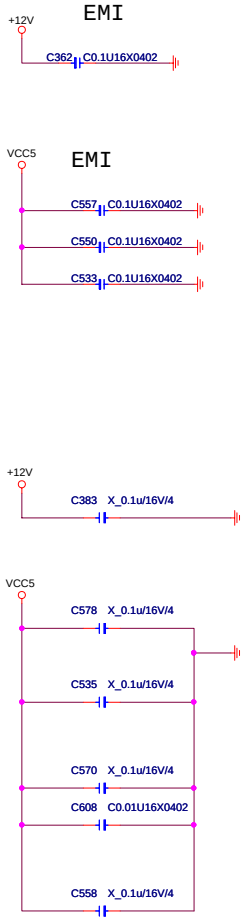
IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

PCI SLOT 2 (PCI VER: 2.2 COMPLY)

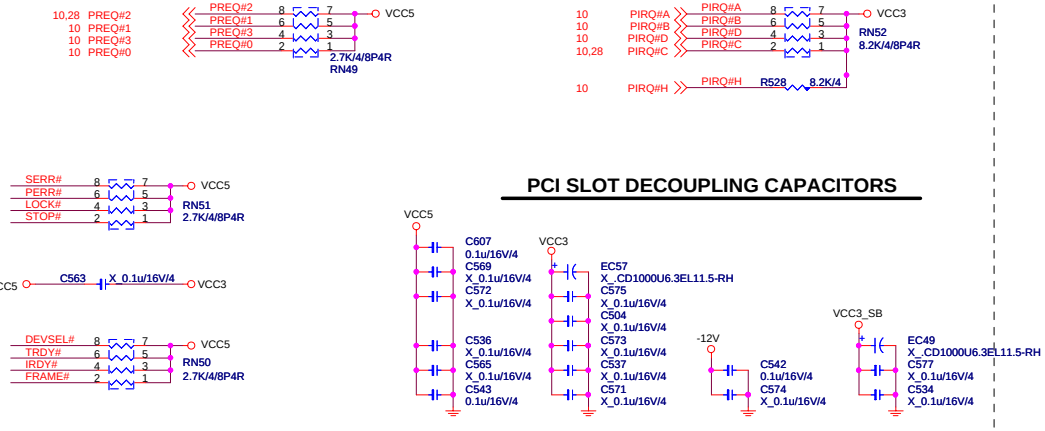


IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

EMI



PCI PULL-UP / DOWN RESISTORS

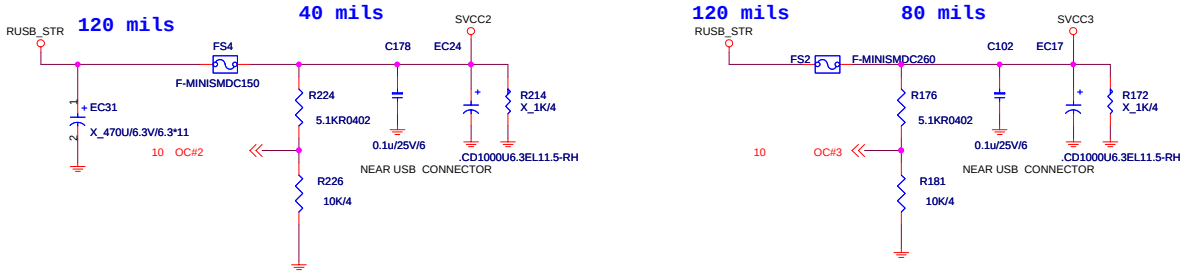


PCI SLOT DECOUPLING CAPACITORS

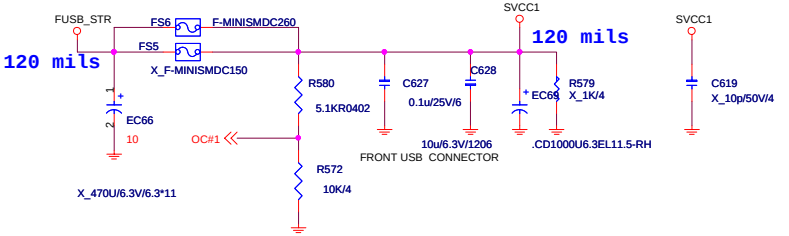
EMI

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7357	
Size: Custom	Document Description: PCI Slot	Rev: 1.0
Date: Tuesday, May 29, 2007	Sheet 18 of 35	

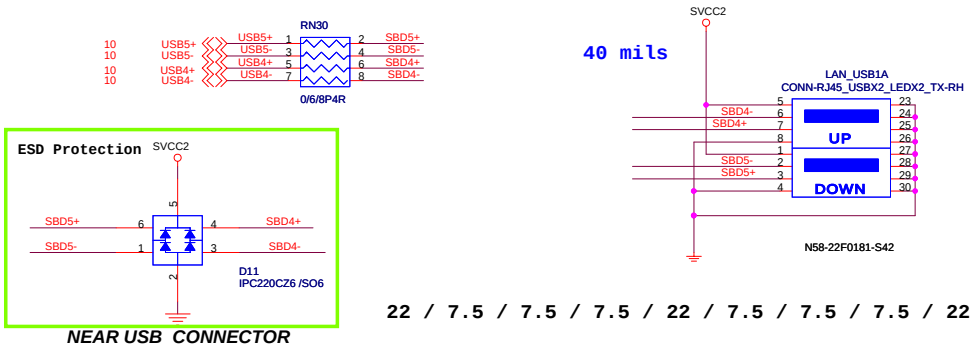
POWER CIRCUIT FOR USB PORT 4~7



POWER CIRCUIT FOR USB PORT 0~3



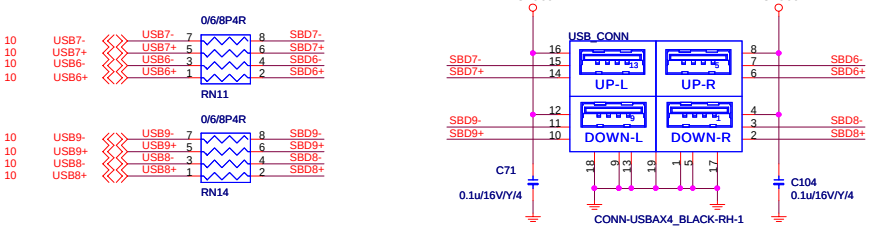
REAR PANEL USB CONNECTOR FOR USB PORT 4,5



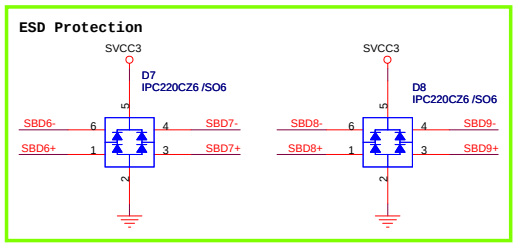
NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

REAR PANEL USB CONNECTOR FOR USB PORT 6,7,8,9

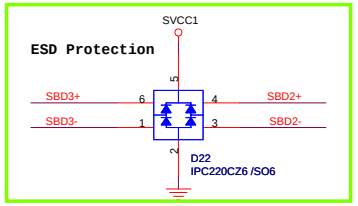


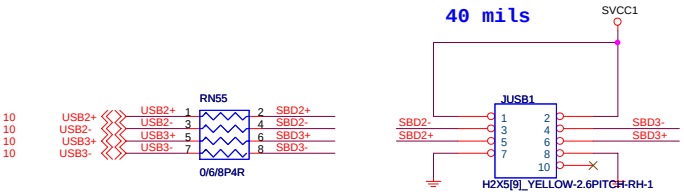
22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22



FRONT PANEL USB CONNECTOR FOR USB PORT 2,3

Reserved, can be taken off riser card within bead

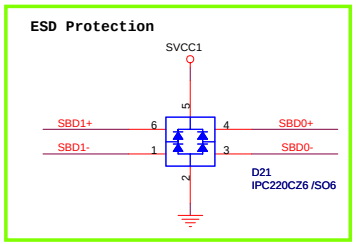


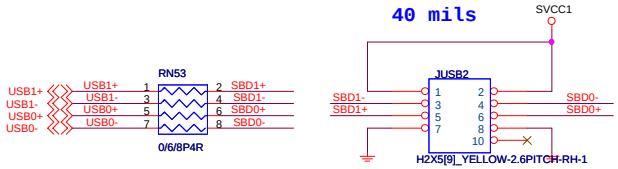


NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

FRONT PANEL USB CONNECTOR FOR USB PORT 0,1

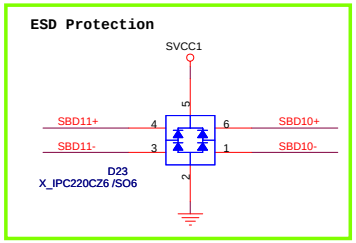


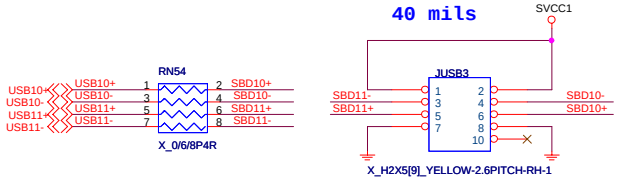


NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

FRONT PANEL USB CONNECTOR FOR USB PORT 0,1



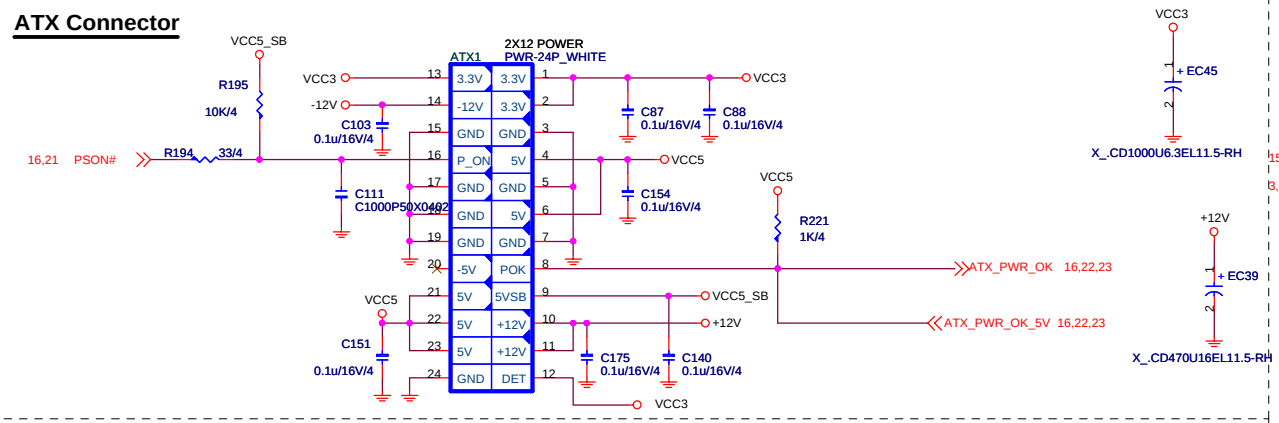


NEAR USB CONNECTOR

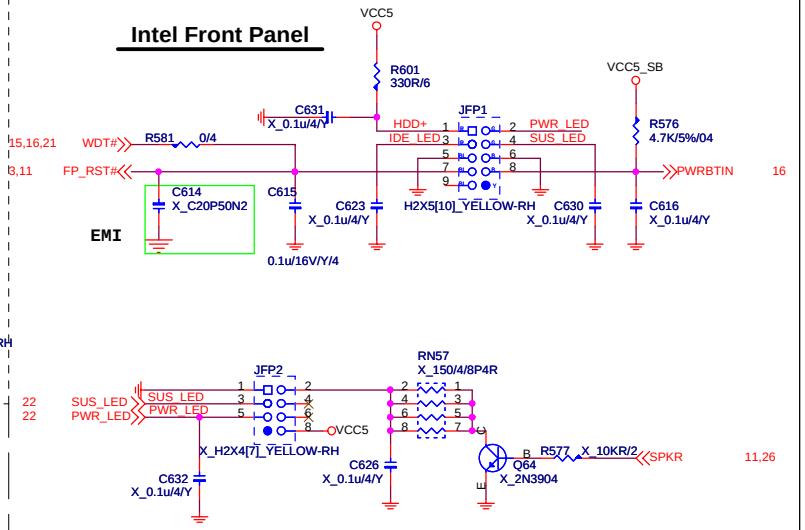
22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

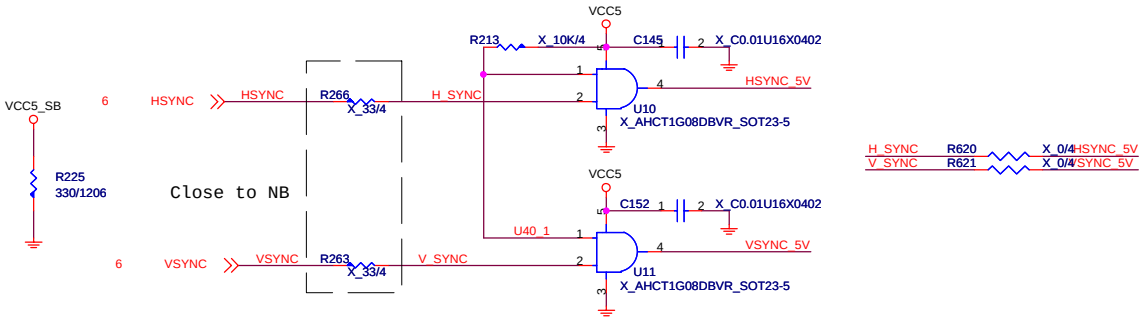
MICRO-STAR INT'L CO.,LTD		
MS-7357		
Size: Custom	Document Description: USB CONNECTORS	Rev: 1.0
Date: Tuesday, May 29, 2007	Sheet 19 of 35	

ATX Connector

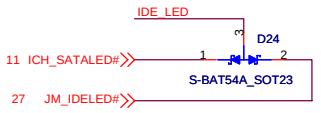


Intel Front Panel

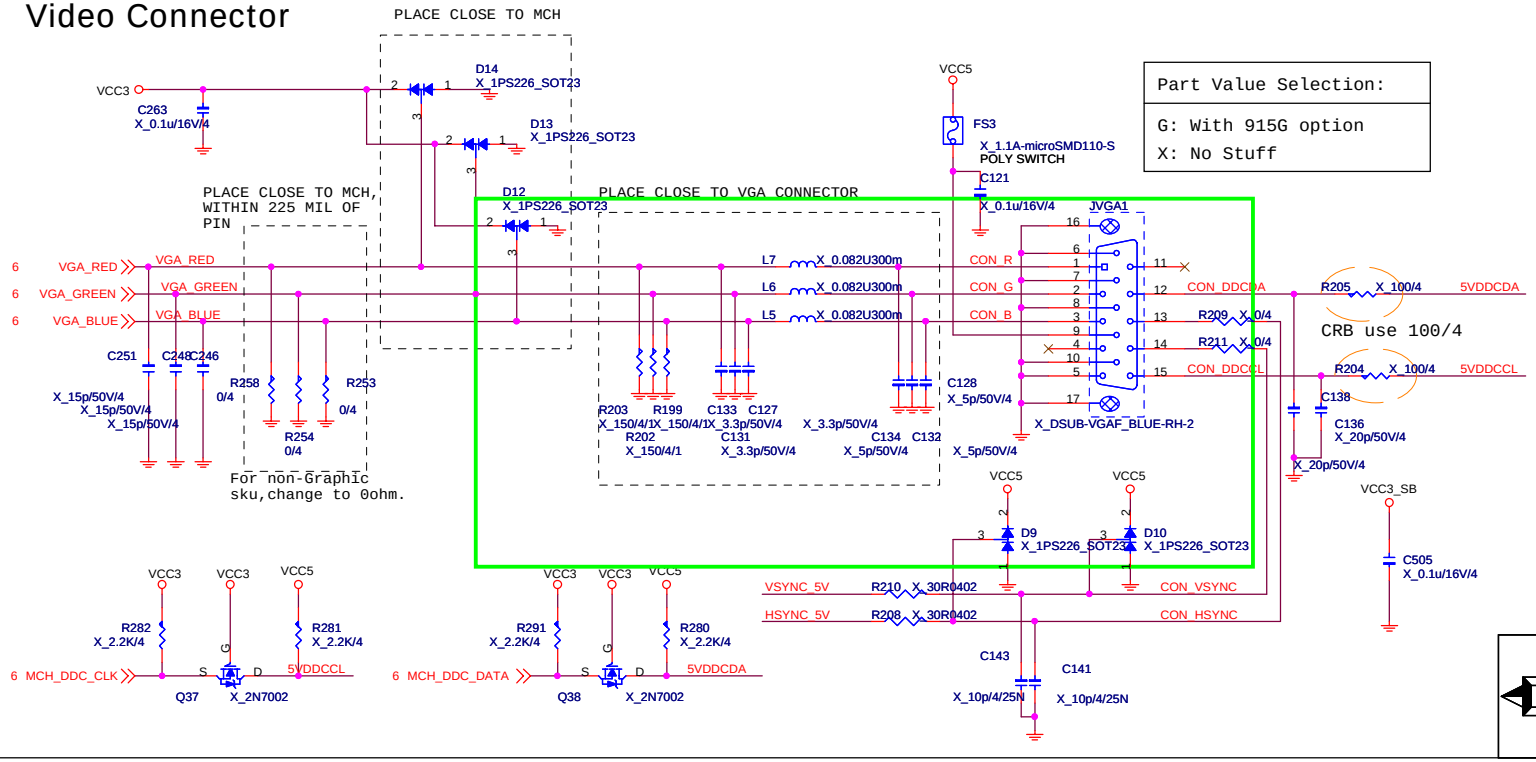




IDE LED



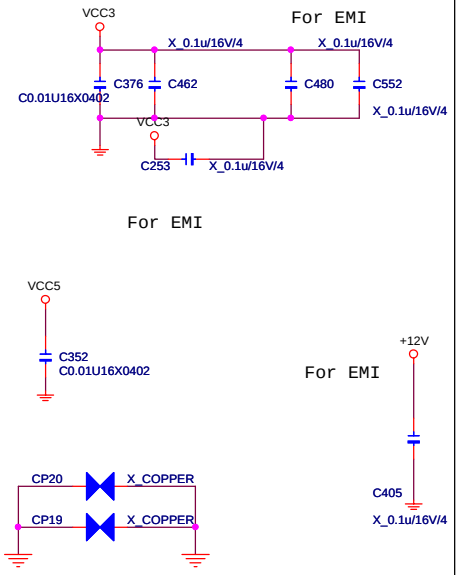
Video Connector



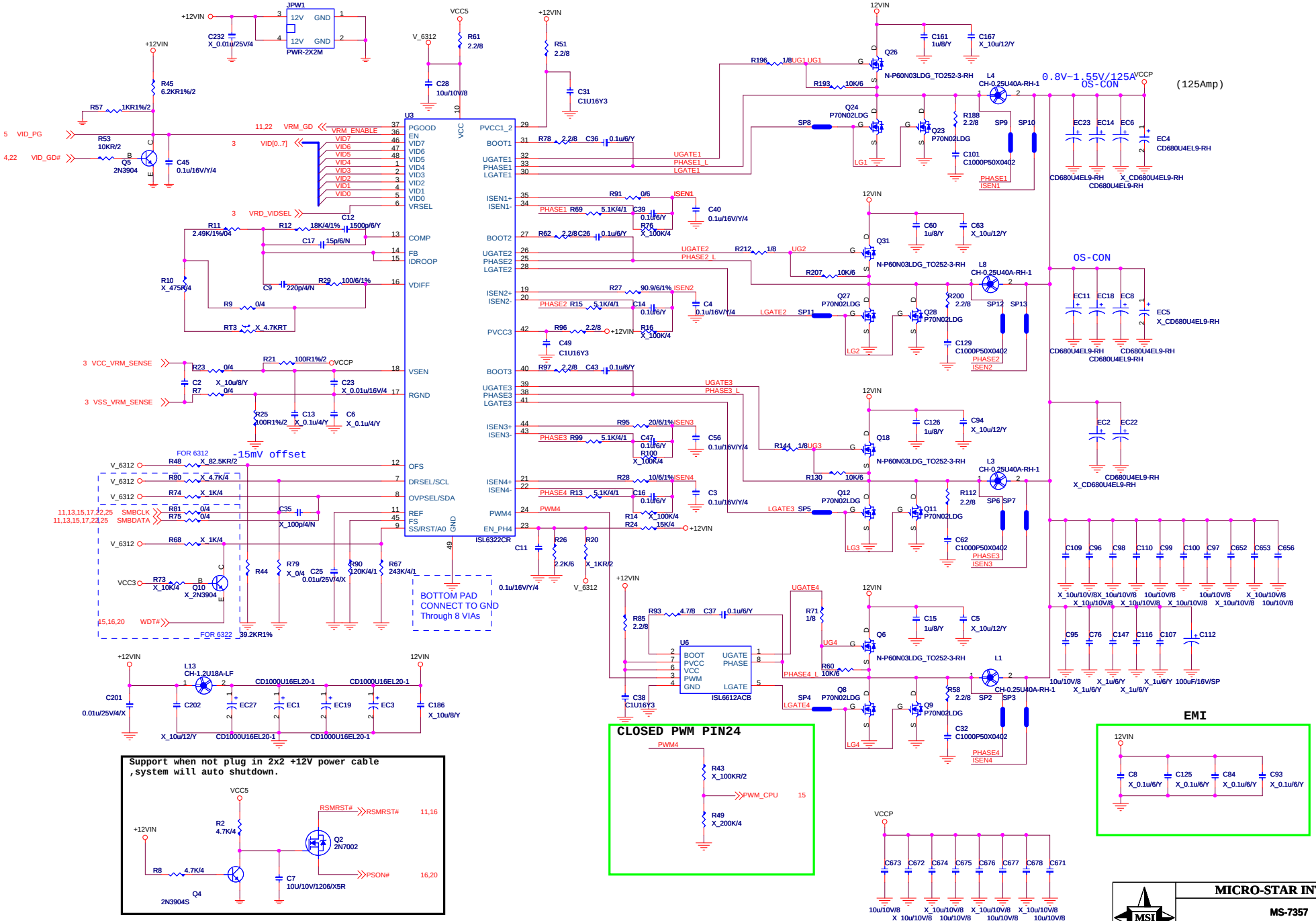
Part Value Selection:

G: With 915G option

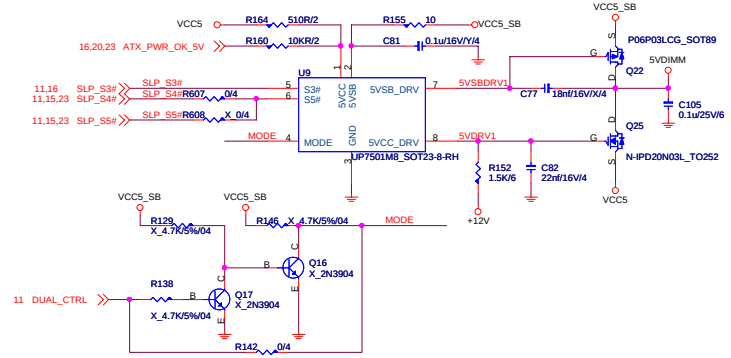
X: No Stuff



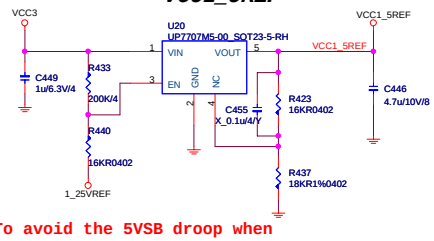
MICRO-STAR INT'L CO.,LTD		
MS-7357		
Size: Custom	Document Description: ATX ,Front Panel & VGA Conn	Rev: 1.0
Date: Monday, June 04, 2007	Sheet 20 of 35	


JPW1
PWR-2X2M
U3
ISL6322CR
U6
ISL6612ACB
0.8V~1.55V/125A
(125Amp)
OS-CON
-15mV offset
FOR 6312
FOR 6322
39.2KR1%
BOTTOM PAD
CONNECT TO GND
Through 8 VIAs
CLOSED PWM PIN24
EMI
Support when not plug in 2x2 +12V power cable
,system will auto shutdown.
MICRO-STAR INT'L CO.,LTD
MS-7357
VRD11 Intersil 6322 4Phase
Wednesday, May 30, 2007

5VDIMM FOR DDR

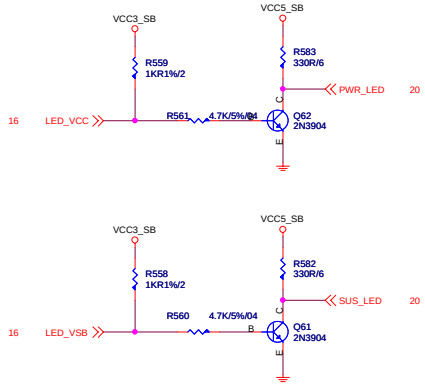


VCC1_5REF

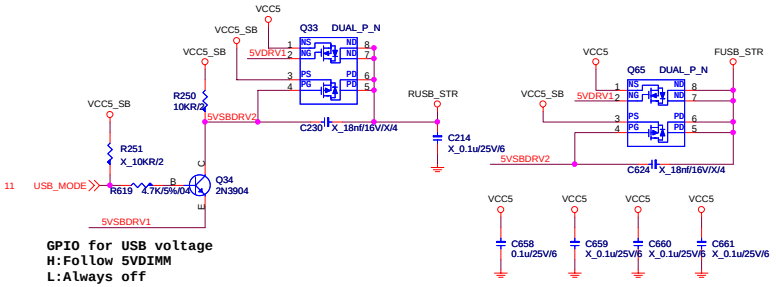


To avoid the 5VSB droop when V1_5 power up

LED (for Fintek 71882)



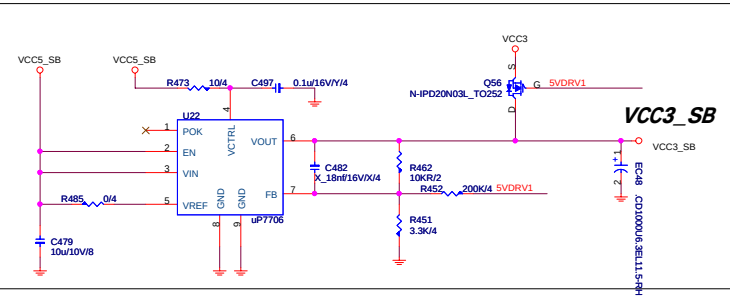
5VSB FOR Rear USB



GPIO for USB voltage
H:Follow 5VDIMM
L:Always off

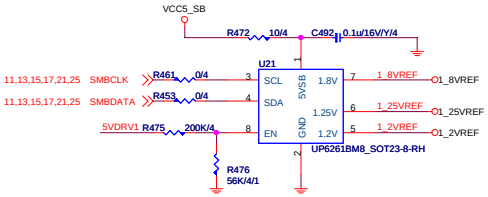
5VSB FOR Front USB

VCC3_SB

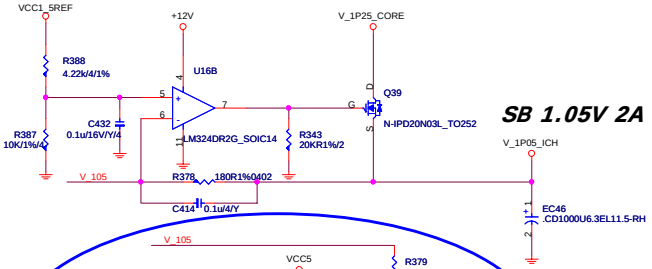


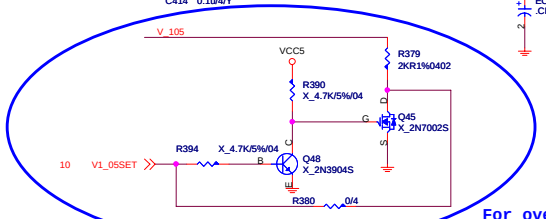
reference Voltage

DDR REF
NB 1.25V REF
V_FSB_VTT REF

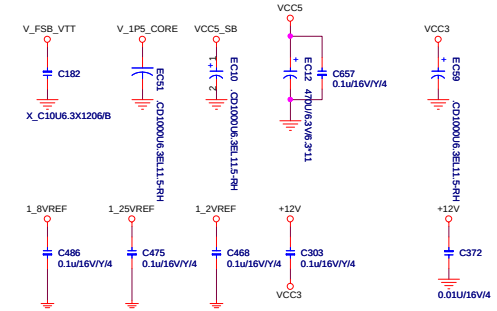


SB 1.05V 2A

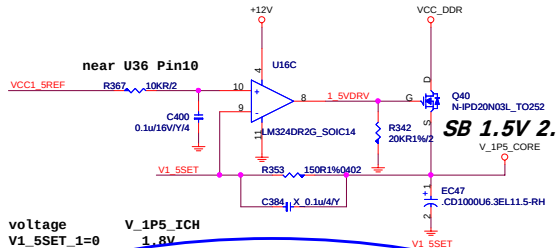




For over voltage

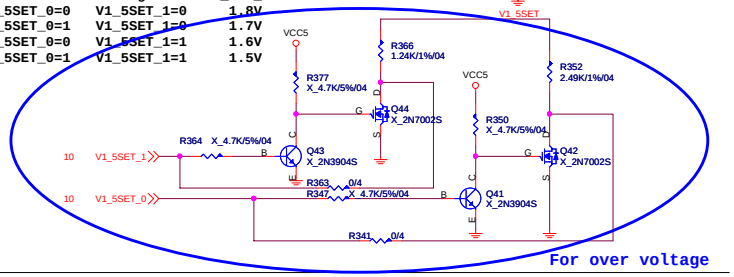


SB 1.5V 2.75A



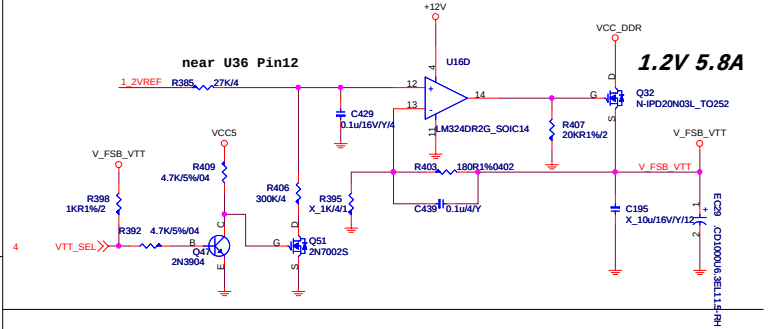
GPIO for over voltage V_1P5_ICH

V1_5SET_0=0	V1_5SET_1=0	1.8V
V1_5SET_0=1	V1_5SET_1=0	1.7V
V1_5SET_0=0	V1_5SET_1=1	1.6V
V1_5SET_0=1	V1_5SET_1=1	1.5V



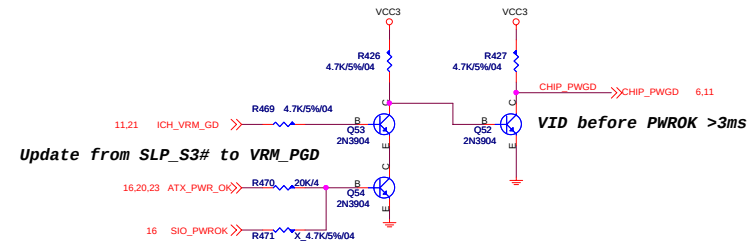
For over voltage

1.2V 5.8A

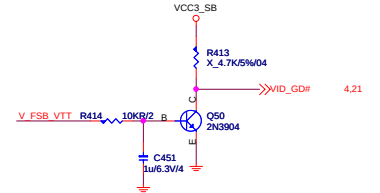


VID before PWROK >3ms

Update from SLP_S3# to VRM_PGD



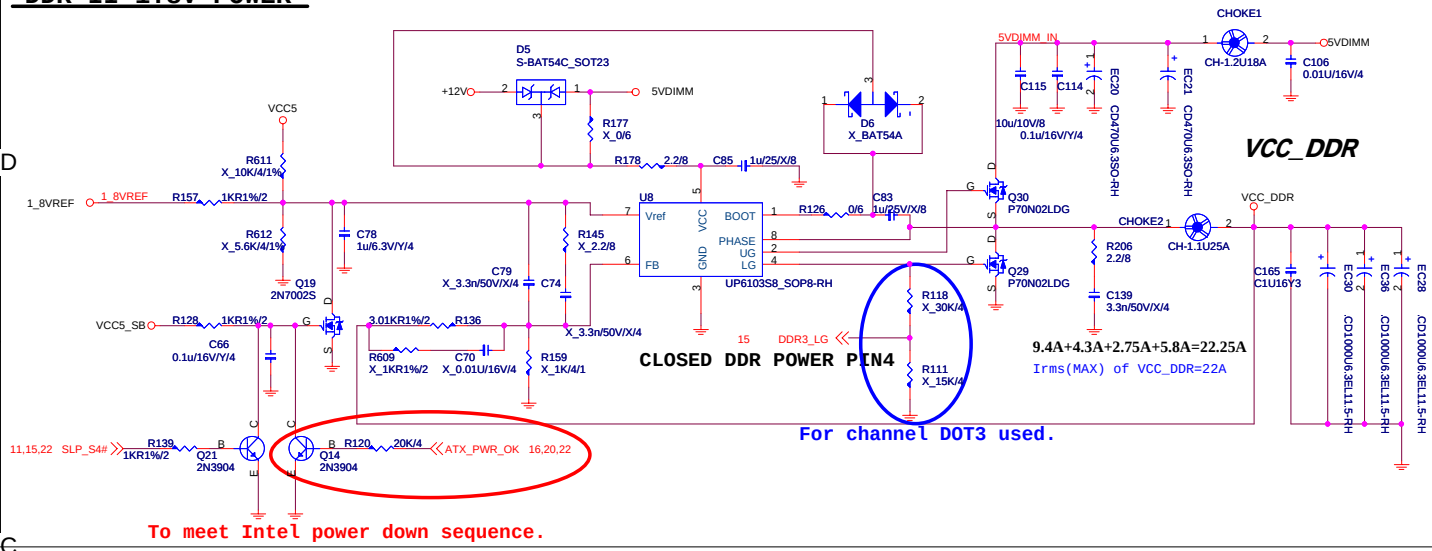
PWROK DELAY



MICRO-STAR INT'L CO.,LTD			
MS-7357			
Size: Custom	Document Description: ACPI Controller UPI		Rev: 1.0
Date: Wednesday, May 16, 2007	Sheet 22 of 35		

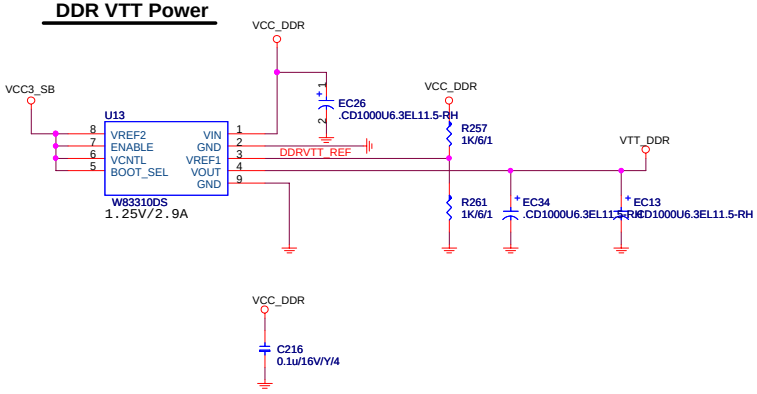
DDR II 1.8V POWER

Iripple=21*0.6*0.8/1=10.08A
2.22*3*1.7=11.322A>10.08A



DDR VTT Power

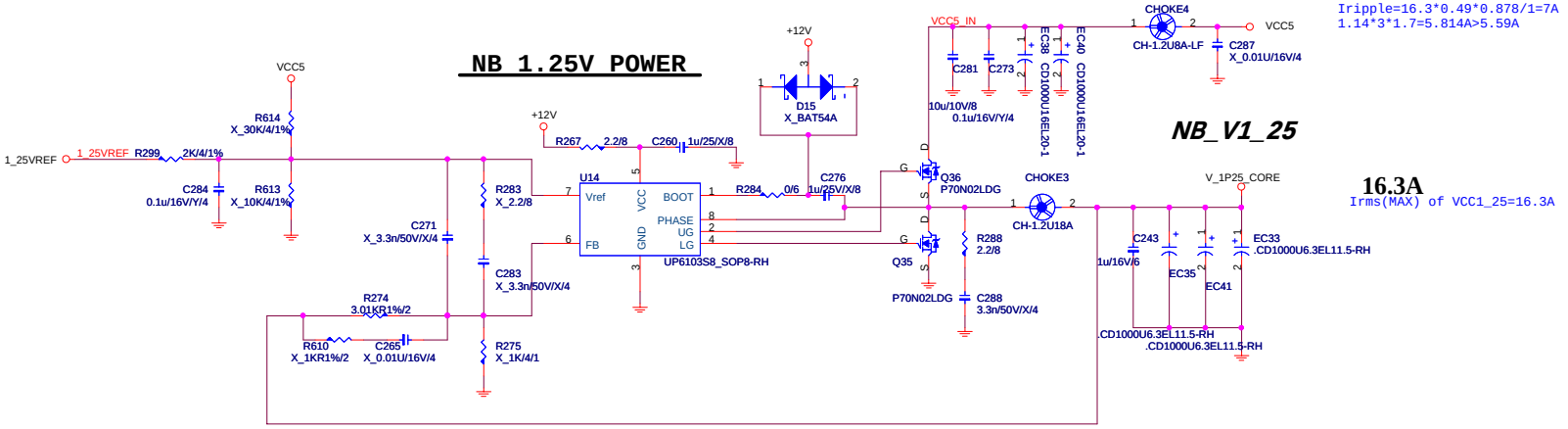
To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



de- VCC_DDR high frequency noise.

NB 1.25V POWER

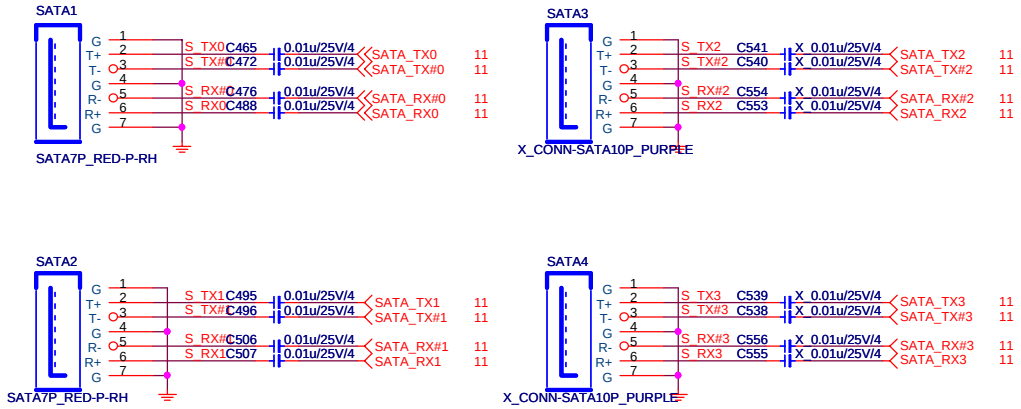
Iripple=16.3*0.49*0.878/1=7A
1.14*3*1.7=5.814A>5.59A

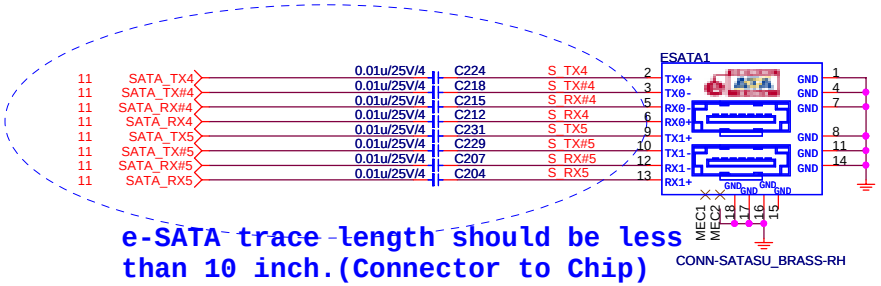


CHANNEL B V_SM_VTT
DECOULPING CAPS

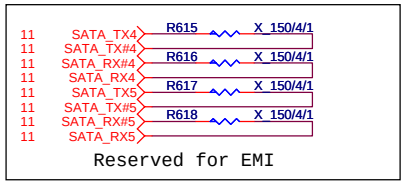
MICRO-STAR INT'L CO.,LTD		
MS-7357		
Size: Custom	Document Description: NB Core Power & DDR Power	Rev: 1.0
Date: Friday, March 30, 2007	Sheet 23 of 35	

SERIAL ATA CONNECTOR BLOCK

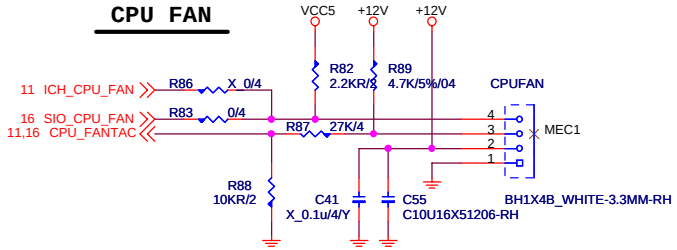




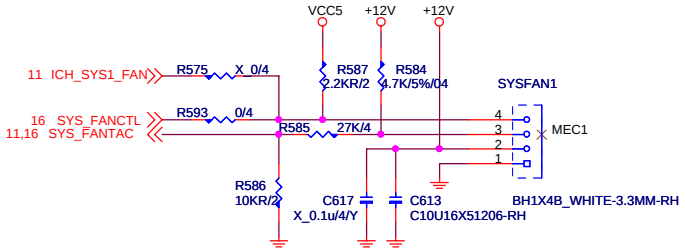
e-SATA trace length should be less than 10 inch.(Connector to Chip)

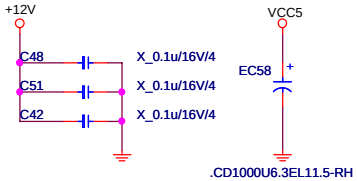


CPU FAN



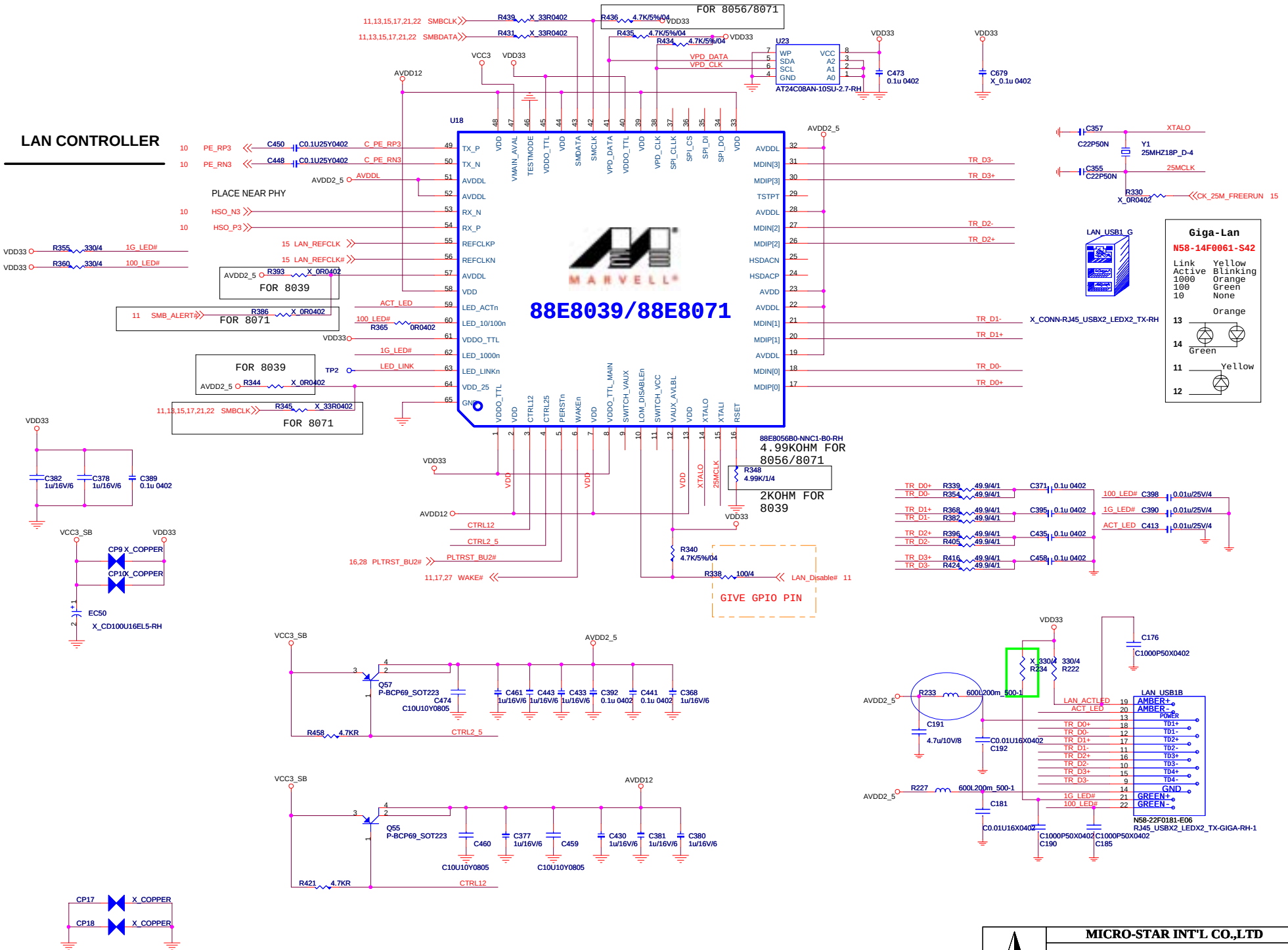
SYS FAN



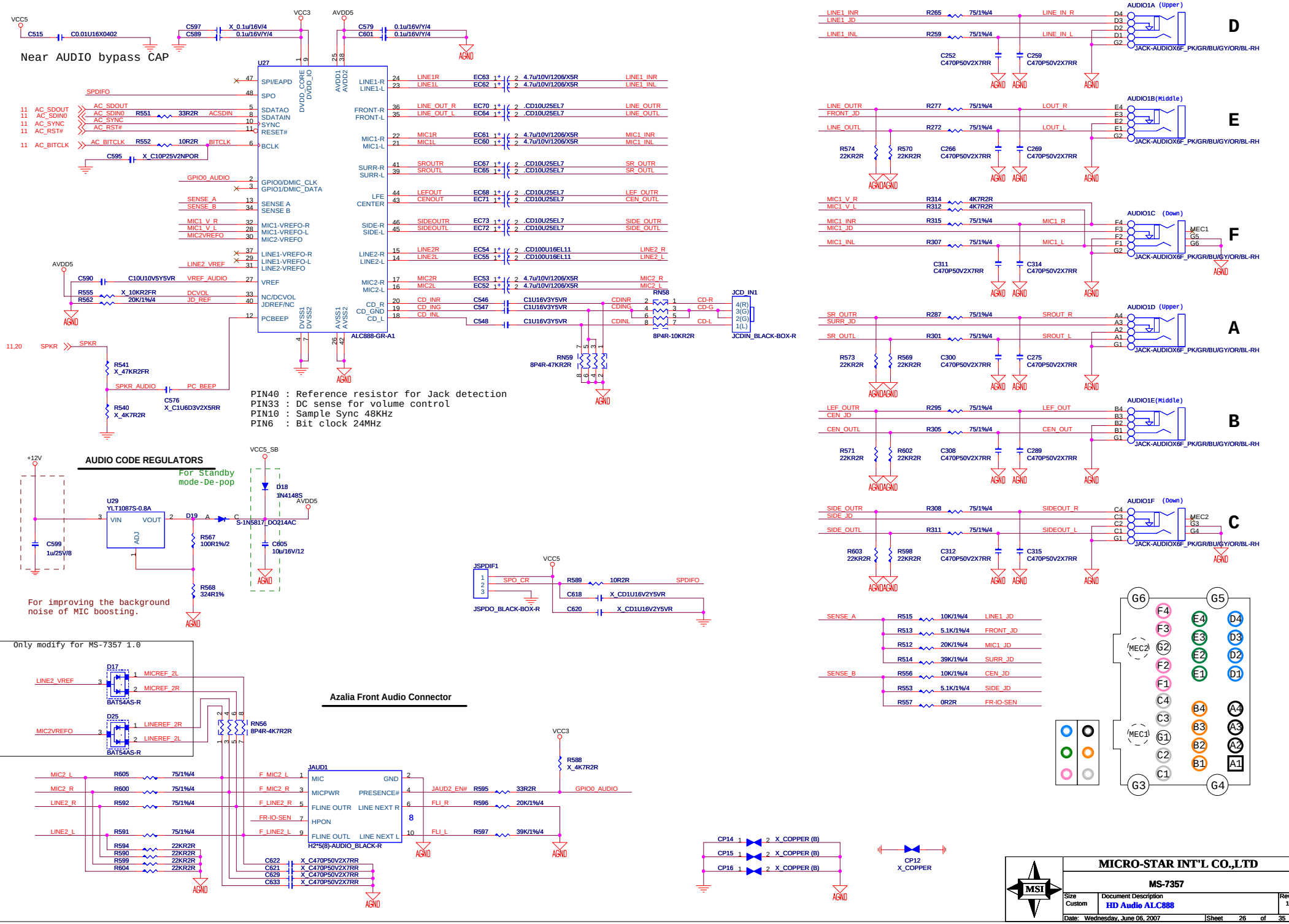


MICRO-STAR INT'L CO.,LTD		
MS-7357		
Size: Custom	Document Description: FAN & SATA	Rev: 1.0
Date: Tuesday, May 29, 2007	Sheet 24 of 35	

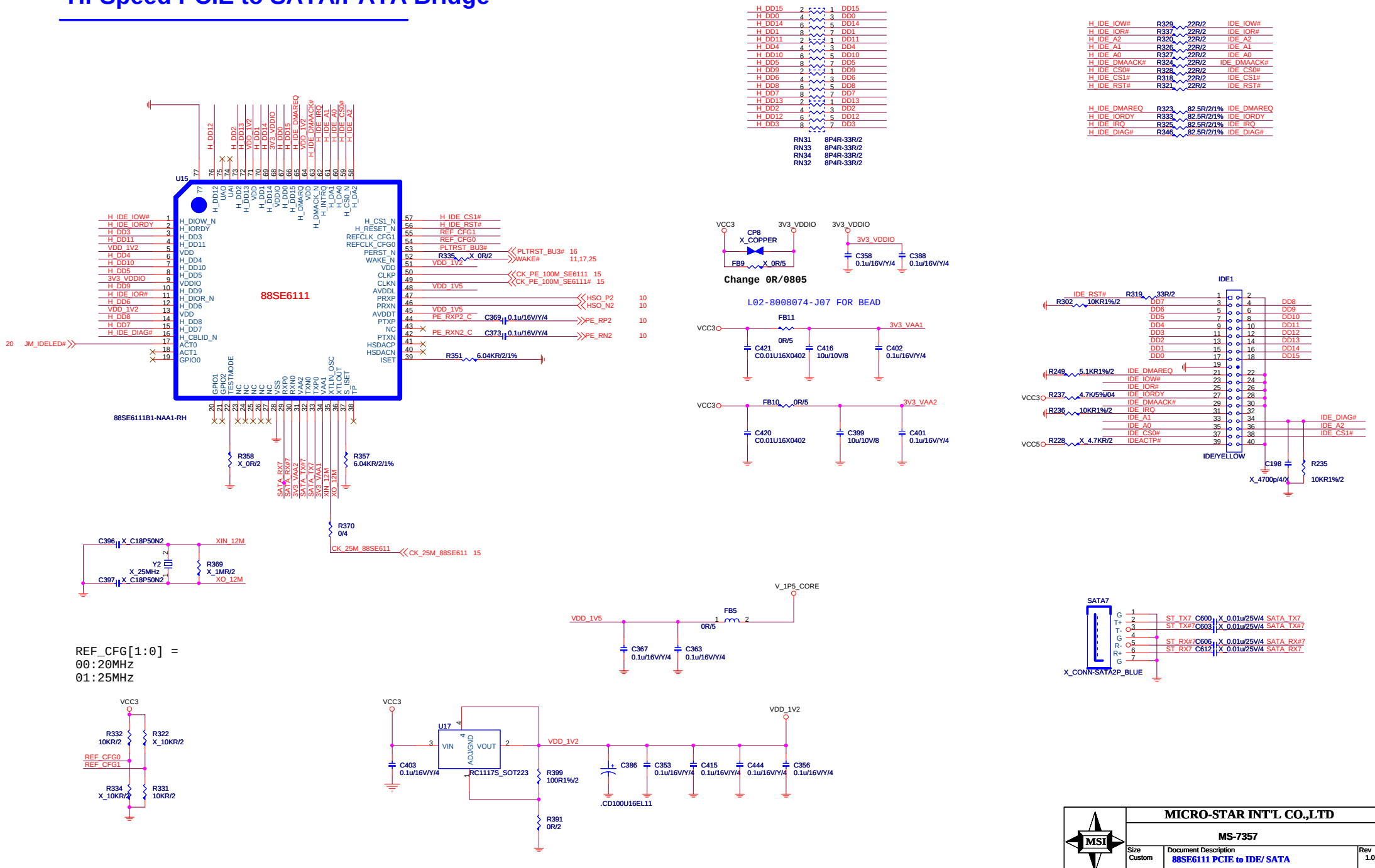
LAN CONTROLLER



MICRO-STAR INT'L CO.,LTD			
MS-7357			
Size: Custom	Document Description: MARVELL 88E8039 / 56 / 71		Rev: 1.0
Date: Tuesday, May 29, 2007	Sheet 25 of 35		

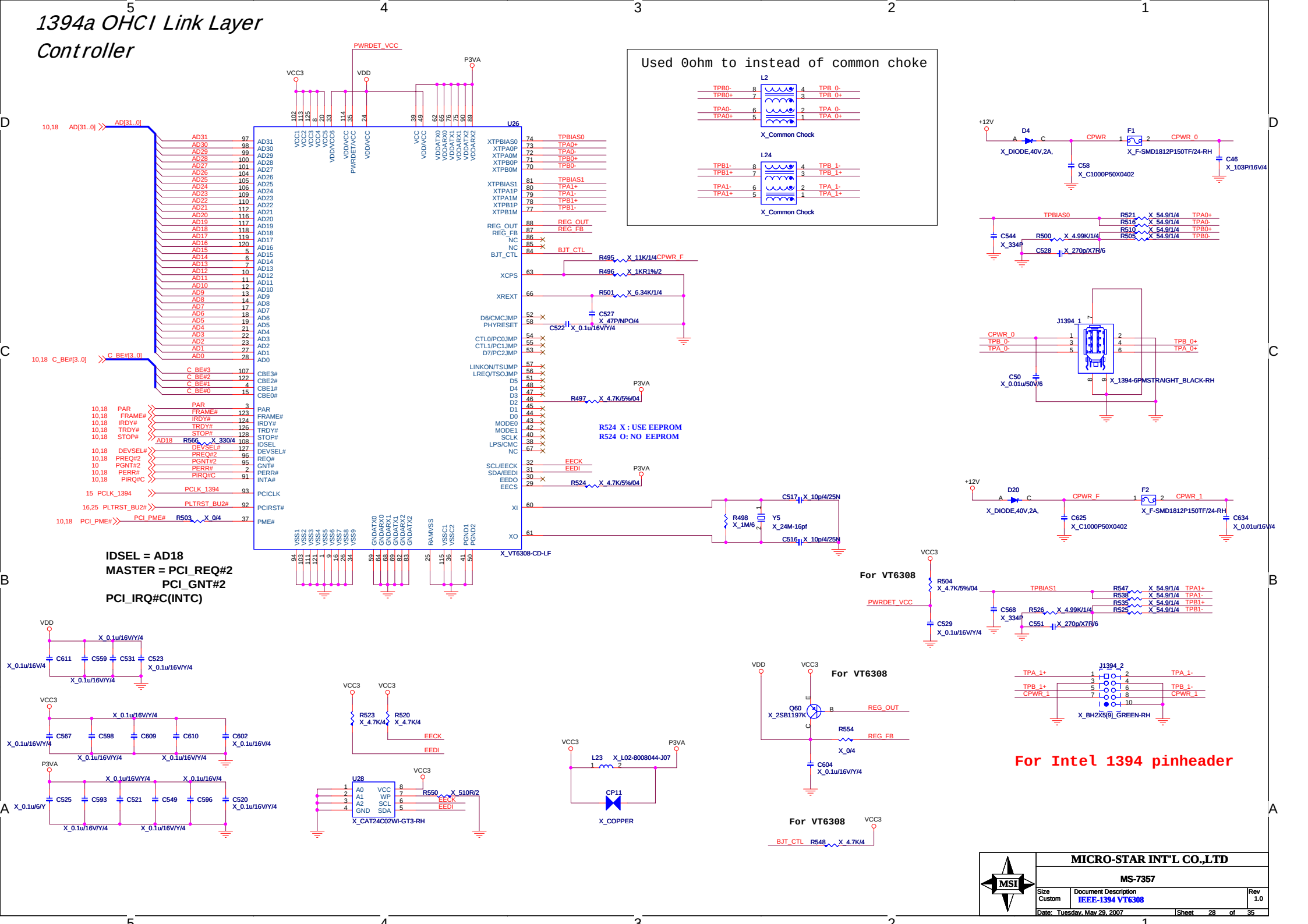

Near AUDIO bypass CAP
U27
ALC888-GR-A1
PIN40 : Reference resistor for Jack detection
PIN33 : DC sense for volume control
PIN10 : Sample Sync 48KHz
PIN6 : Bit clock 24MHz
AUDIO CODE REGULATORS
For Standby mode-De-pop
For improving the background noise of MIC boosting.
Only modify for MS-7357 1.0
Azalia Front Audio Connector
JAUD1
AUDIO1A (Upper)
AUDIO1B(Middle)
AUDIO1C (Down)
AUDIO1D (Upper)
AUDIO1E(Middle)
AUDIO1F (Down)
JACK-AUDIOX6F_PK/GR/BU/GY/OR/BL-RH
JCD_IN1
JCDIN_BLACK-BOX-R
JSPDIF1
JSPDO_BLACK-BOX-R
MICRO-STAR INT'L CO.,LTD
MS-7357
HD Audio ALC888
Date: Wednesday, June 06, 2007
Sheet 26 of 35

Hi-Speed PCIE to SATA/PATA Bridge

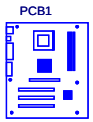


MICRO-STAR INT'L CO.,LTD	
MS-7357	
Size: Custom	Document Description: 88SE6111 PCIE to IDE/ SATA
Rev: 1.0	
Date: Tuesday, May 29, 2007	Sheet 27 of 35

1394a OHCI Link Layer Controller



MANUAL PART

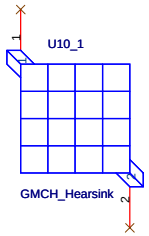


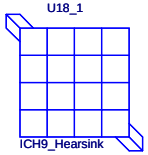
P80-0735710-E48,競華

P80-0735710-G37,精成

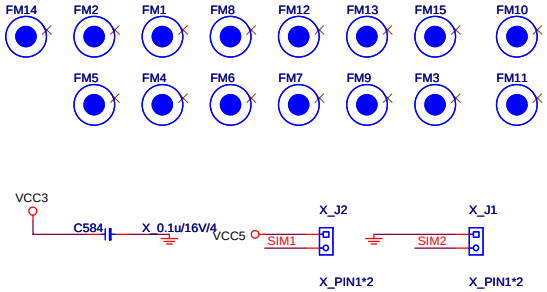
P80-0735710-D05,昆穎

P80-0735710-Y34,元茂

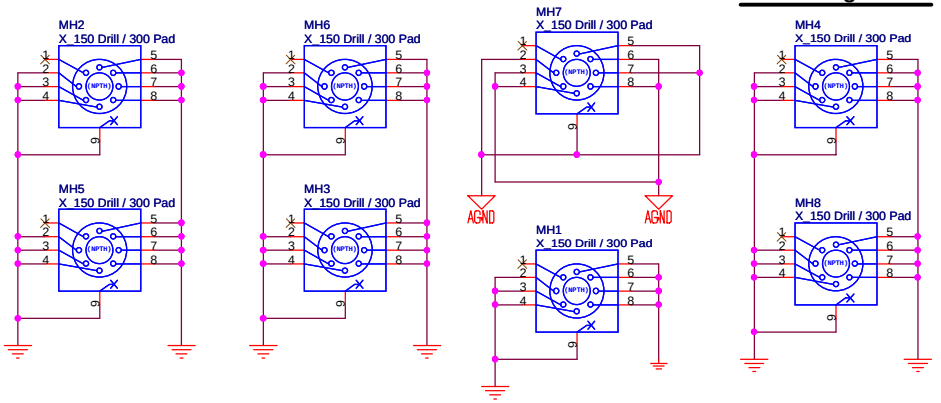




Optical Fiducial Marks



Mounting Holes



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7357	
Size: Custom	Document Description: MANUAL PARTS	Rev: 1.0
Date: Tuesday, March 27, 2007	Sheet 29 of 35	

ICH9

GPIO	Alt Func	Pin	I/O/NC	Power	PU	Tol	Default	Signal Name or condition
GPIO[0]	ATADET0	N7	I/O	Vcc3	Y	3.3	INPUT	ATADET0
GPIO[1]	PULL HIGH	AK21	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 10K
GPIO[2]	PIRQ#E	K6	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 8.2K
GPIO[3]	PIRQ#F	L7	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 8.2K
GPIO[4]	PIRQ#G	F2	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 8.2K
GPIO[5]	PIRQ#H	G2	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 8.2K
GPIO[6]	PULL HIGH	AH22	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 10K
GPIO[7]	PULL HIGH	AK23	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 10K
GPIO[8]	ICH_GP8_PU	A20	I/O	Vcc3SB	Y	3.3	INPUT	PULL HIGH 10K
GPIO[9]	NC	A18	NC	Vcc3	N	3.3	WOL_EN	NC
GPIO[10]	ICH_GP10_PU	C17	I/O	Vcc3SB	Y	3.3	INPUT	PULL HIGH 10K
GPIO[11]	SMB_ALERT#	C16	I/O	Vcc3SB	Y	3.3	SMB_ALERT#	PULL HIGH 10K
GPIO[12]	NC	A8	NC	Vcc3SB	N	3.3	OUTPUT	NC
GPIO[13]	SIO_PME#	A19	I/O	Vcc3SB	Y	3.3	INPUT	SIO_PME#
GPIO[14]	ICH_GP14_PU	A9	I/O	Vcc3SB	Y	3.3	INPUT	PULL HIGH 10K
GPIO[15]	NC	C15	NC	Vcc3SB	Y	3.3	STP_PCI#	NC
GPIO[16]	NC	M2	NC	Vcc3	Y	3.3	OUTPUT	NC
GPIO[17]	PULL HIGH	AH21	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 10K
GPIO[18]	NC	K1	NC	Vcc3	N	3.3	OUTPUT	NC
GPIO[19]	SATA1GP_PU	AE20	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 10K
GPIO[20]	NC	AF5	NC	Vcc3	N	3.3	OUTPUT	NC
GPIO[21]	SATA0GP_PU	AK25	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 10K
GPIO[22]	ICH_SGP22_PU	AJ24	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 10K
GPIO[23]	LDRQ_1#	J3	I/O	Vcc3	Y	3.3	LDRQ_1#	PULL HIGH 10K
GPIO[24]	NC	A14	NC	Vcc3SB	N	3.3	OUTPUT	NC
GPIO[25]	NC	B18	NC	Vcc3SB	N	3.3	STP_CPU#	NC
GPIO[26]	NC	C11	NC	Vcc3SB	N	3.3	S4_STATE#	NC
GPIO[27]	NC	A11	NC	Vcc3SB	N	3.3	QRT_STATE0	NC
GPIO[28]	NC	G18	NC	Vcc3SB	N	3.3	QRT_STATE1	NC
GPIO[29]	OC#2	N1	I/O	Vcc3SB	Y	3.3	OC#2	OC#2
GPIO[30]	OC#3	N5	I/O	Vcc3SB	Y	3.3	OC#3	OC#3
GPIO[31]	OC#3	M1	I/O	Vcc3SB	Y	3.3	OC#3	OC#3
GPIO[32]	SPI_WP#	K2	I/O	Vcc3	N	3.3	OUTPUT	SPI_WP#
GPIO[33]	SPI_HOLD_GPO#	AF6	I/O	Vcc3	N	3.3	OUTPUT	SPI_HOLD_GPO#
GPIO[34]	LAN_Disable#	AH5	I/O	Vcc3	N	3.3	OUTPUT	LAN_Disable#
GPIO[35]	NC	L1	NC	Vcc3	N	3.3	OUTPUT	NC
GPIO[36]	SATA2GP_PU	AE21	I/O	Vcc3	Y	3.3	INPUT	SATA2GP_PU
GPIO[37]	SATA3GP_PU	AE22	I/O	Vcc3	Y	3.3	INPUT	SATA3GP_PU
GPIO[38]	ICH_SGP38_PU	AK24	I/O	Vcc3	Y	3.3	INPUT	ICH_SGP38_PU
GPIO[39]	ICH_SGP39_PD	AH23	I/O	Vcc3	Y	3.3	SDATAOUT0	ICH_SGP39_PD
GPIO[40]	OC#1	N3	I/O	Vcc3SB	Y	3.3	OC#1	OC#1
GPIO[41]	OC#1	P7	I/O	Vcc3SB	Y	3.3	OC#1	OC#1
GPIO[42]	OC#1	R7	I/O	Vcc3SB	Y	3.3	OC#1	OC#1
GPIO[43]	OC#2	N2	I/O	Vcc3SB	Y	3.3	OC#2	OC#2
GPIO[44]	OC#3	P3	I/O	Vcc3SB	Y	3.3	OC#3	OC#3
GPIO[45]	OC#3	R6	I/O	Vcc3SB	Y	3.3	OC#3	OC#3
GPIO[46]	PULL HIGH	T7	I/O	Vcc3SB	Y	3.3	OC#	PULL HIGH 10K
GPIO[47]	PULL HIGH	P1	I/O	Vcc3SB	Y	3.3	OC#	PULL HIGH 10K
GPIO[48]	ICH_SGP48_PD	AD20	I/O	Vcc3	Y	3.3	SDATAOUT1	PULL HIGH 10K
GPIO[49]	DMI_STRAP	AJ25	I/O	Vcc3	N	3.3	OUTPUT	PULL LOW 2.2K
GPIO[50]	PREQ#1	G13	I/O	Vcc5	Y	5.5	PREQ#1	PULL HIGH 2.7K
GPIO[51]	NC	A7	I/O	Vcc3	N	3.3	PGNT#1	NC
GPIO[52]	PREQ#2	F13	I/O	Vcc5	Y	5.5	PREQ#2	PULL HIGH 2.7K
GPIO[53]	PGNT#2	C7	I/O	Vcc3	N	3.3	PGNT#2	STRAP PIN
GPIO[54]	PREQ#3	G8	I/O	Vcc5	Y	5.5	PREQ#3	PULL HIGH 2.7K
GPIO[55]	PGNT#3	F7	I/O	Vcc3	N	3.3	PGNT#3	STRAP PIN
GPIO[56]	ICH_GP56_PU	F16	I/O	Vcc3SB	Y	3.3	GPIO_SEL	PULL HIGH 10K
GPIO[57]	ICH_GP57_PU	C12	I/O	Vcc3SB	Y	3.3	INPUT	PULL HIGH 10K
GPIO[58]	SPI_CS1#	F23	I/O	Vcc3SB	Y	3.3	SPI_CS1#	SPI_CS1#
GPIO[59]	OC#1	P5	I/O	Vcc3SB	Y	3.3	OC#1	OC#1
GPIO[60]	LINK_ALERT#	F18	I/O	Vcc3SB	Y	3.3	LINK_ALERT#	LINK_ALERT#

PCI Config.

DEVICE	Interrupt Request Pin	REQ# /GNT#	IDSEL	CLOCK
PCI1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	PCI_CLK1
PCI2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD17	PCI_CLK2
IEEE-1394	PIRQ#C	PREQ#2 PGNT#2	AD18	PCI_CLK3

DDRII DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	A0H	MCLK_A0/MCLK_A#0 MCLK_A1/MCLK_A#1 MCLK_A2/MCLK_A#2
DIMM 2	A2H	MCLK_A1/MCLK_A#3 MCLK_A2/MCLK_A#4 MCLK_A2/MCLK_A#5
DIMM 3	A4H	MCLK_B0/MCLK_B#0 MCLK_B2/MCLK_B#1 MCLK_B1/MCLK_B#2
DIMM 4	A6H	MCLK_B0/MCLK_B#3 MCLK_B1/MCLK_B#4 MCLK_B2/MCLK_B#5

JUMPER SETTING

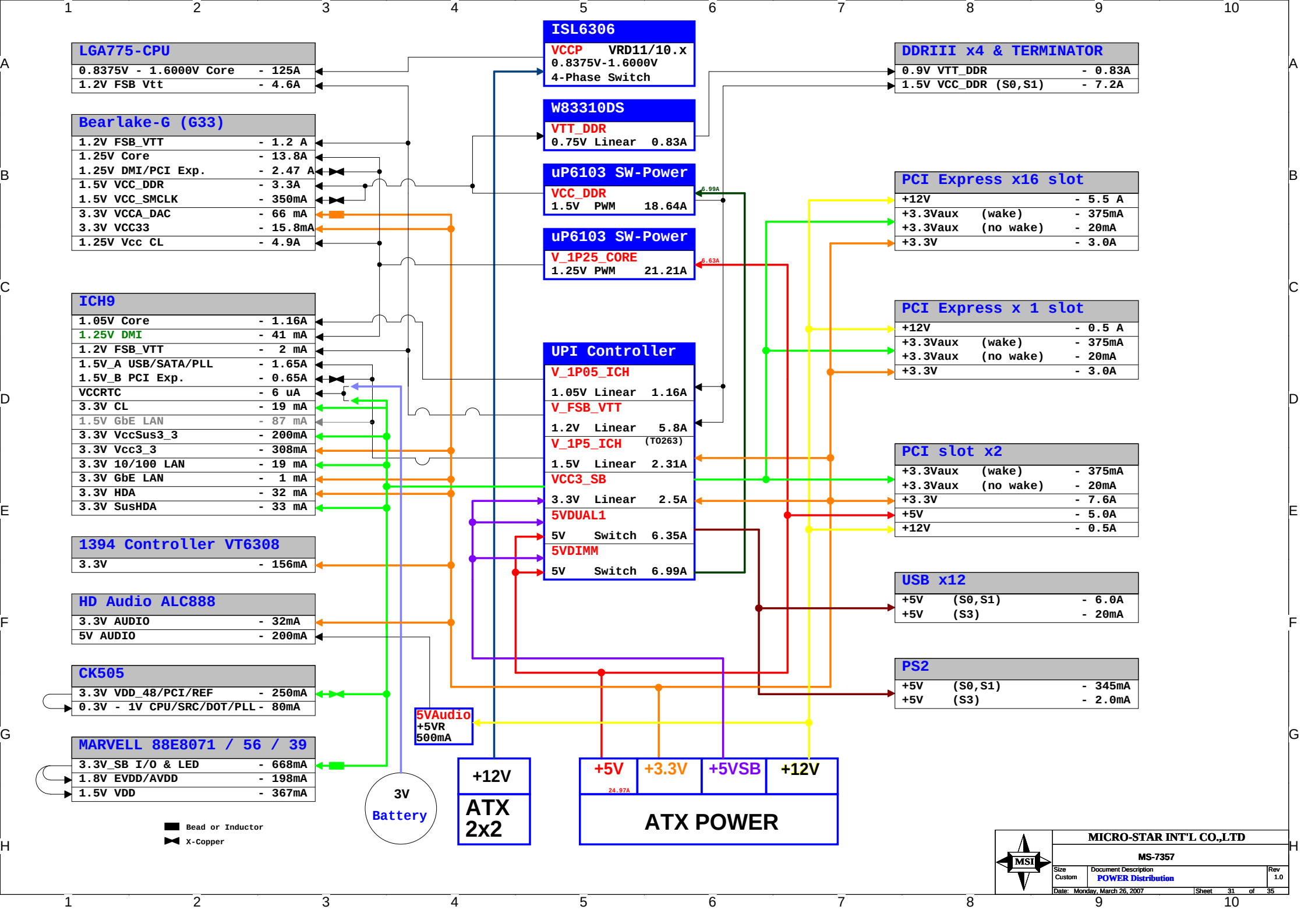
JBAT1	(1-2)NORMAL	(2-3)CLEAR

MICRO-STAR INT'L CO.,LTD

MS-7357

Size: Custom | Document Description: GPIO & Jumper setting | Rev: 1.0

Date: Monday, March 26, 2007 | Sheet 30 of 35


LGA775-CPU
0.8375V - 1.6000V Core - 125A
1.2V FSB Vtt - 4.6A
Bearlake-G (G33)
1.2V FSB_VTT - 1.2 A
1.25V Core - 13.8A
1.25V DMI/PCI Exp. - 2.47 A
1.5V VCC_DDR - 3.3A
1.5V VCC_SMCLK - 350mA
3.3V VCCA_DAC - 66 mA
3.3V VCC33 - 15.8mA
1.25V Vcc CL - 4.9A
ICH9
1.05V Core - 1.16A
1.25V DMI - 41 mA
1.2V FSB_VTT - 2 mA
1.5V_A USB/SATA/PLL - 1.65A
1.5V_B PCI Exp. - 0.65A
VCCRTC - 6 uA
3.3V CL - 19 mA
1.5V GbE LAN - 87 mA
3.3V VccSus3_3 - 200mA
3.3V Vcc3_3 - 308mA
3.3V 10/100 LAN - 19 mA
3.3V GbE LAN - 1 mA
3.3V HDA - 32 mA
3.3V SusHDA - 33 mA
1394 Controller VT6308
3.3V - 156mA
HD Audio ALC888
3.3V AUDIO - 32mA
5V AUDIO - 200mA
CK505
3.3V VDD_48/PCI/REF - 250mA
0.3V - 1V CPU/SRC/DOT/PLL - 80mA
MARVELL 88E8071 / 56 / 39
3.3V_SB I/O & LED - 668mA
1.8V EVDD/AVDD - 198mA
1.5V VDD - 367mA
Bead or Inductor
X-Copper
ISL6306
VCCP VRD11/10.x
0.8375V-1.6000V
4-Phase Switch
W83310DS
VTT_DDR
0.75V Linear 0.83A
uP6103 SW-Power
VCC_DDR
1.5V PWM 18.64A
6.99A
uP6103 SW-Power
V_1P25_CORE
1.25V PWM 21.21A
6.63A
UPI Controller
V_1P05_ICH
1.05V Linear 1.16A
V_FSB_VTT
1.2V Linear 5.8A
V_1P5_ICH (TO263)
1.5V Linear 2.31A
VCC3_SB
3.3V Linear 2.5A
5VDUAL1
5V Switch 6.35A
5VDIMM
5V Switch 6.99A
5VAudio
+5VR
500mA
3V
Battery
+12V
ATX
2x2
+5V
24.97A
+3.3V
+5VSB
+12V
ATX POWER
DDRIII x4 & TERMINATOR
0.9V VTT_DDR - 0.83A
1.5V VCC_DDR (S0,S1) - 7.2A
PCI Express x16 slot
+12V - 5.5 A
+3.3Vaux (wake) - 375mA
+3.3Vaux (no wake) - 20mA
+3.3V - 3.0A
PCI Express x 1 slot
+12V - 0.5 A
+3.3Vaux (wake) - 375mA
+3.3Vaux (no wake) - 20mA
+3.3V - 3.0A
PCI slot x2
+3.3Vaux (wake) - 375mA
+3.3Vaux (no wake) - 20mA
+3.3V - 7.6A
+5V - 5.0A
+12V - 0.5A
USB x12
+5V (S0,S1) - 6.0A
+5V (S3) - 20mA
PS2
+5V (S0,S1) - 345mA
+5V (S3) - 2.0mA
MICRO-STAR INT'L CO.,LTD
MS-7357
Size Custom
Document Description
POWER Distribution
Rev 1.0
Date: Monday, March 26, 2007
Sheet 31 of 35

PWROK MAP

12V

5V

3.3V

1.5VREF

NB 1.25V Core

VDDR

SB 1.5V

V_FSB_VTT

VID_GD

VTT_PWGD

VRM_EN

CPU VCore

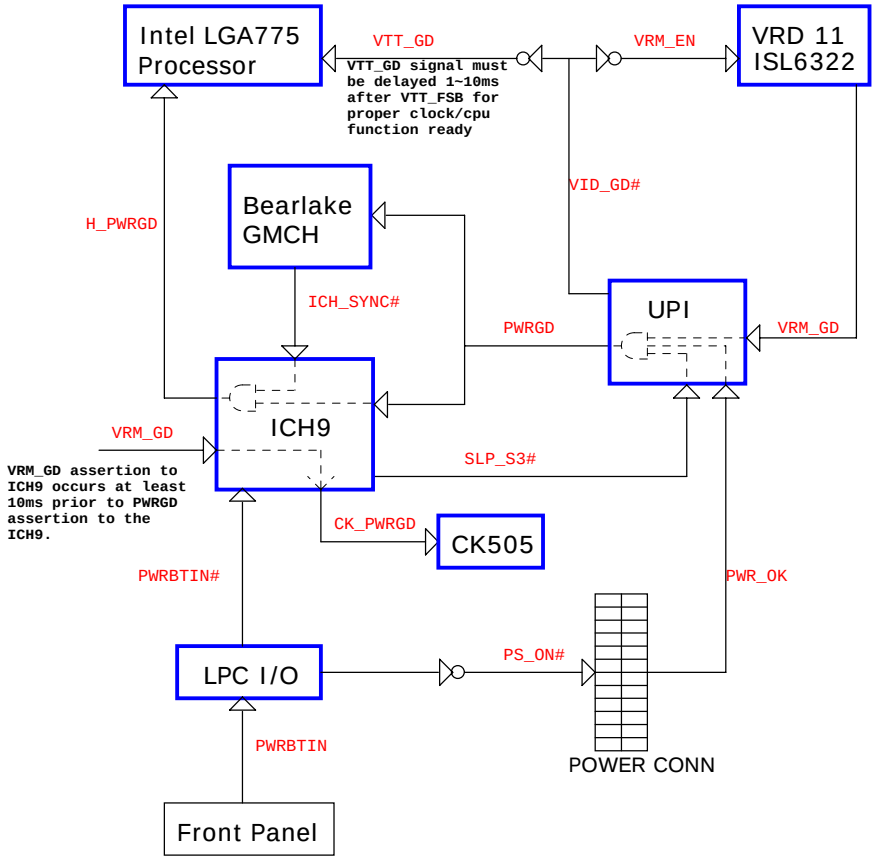
VRMGD to SB

CK_PGD

CHIP_GD

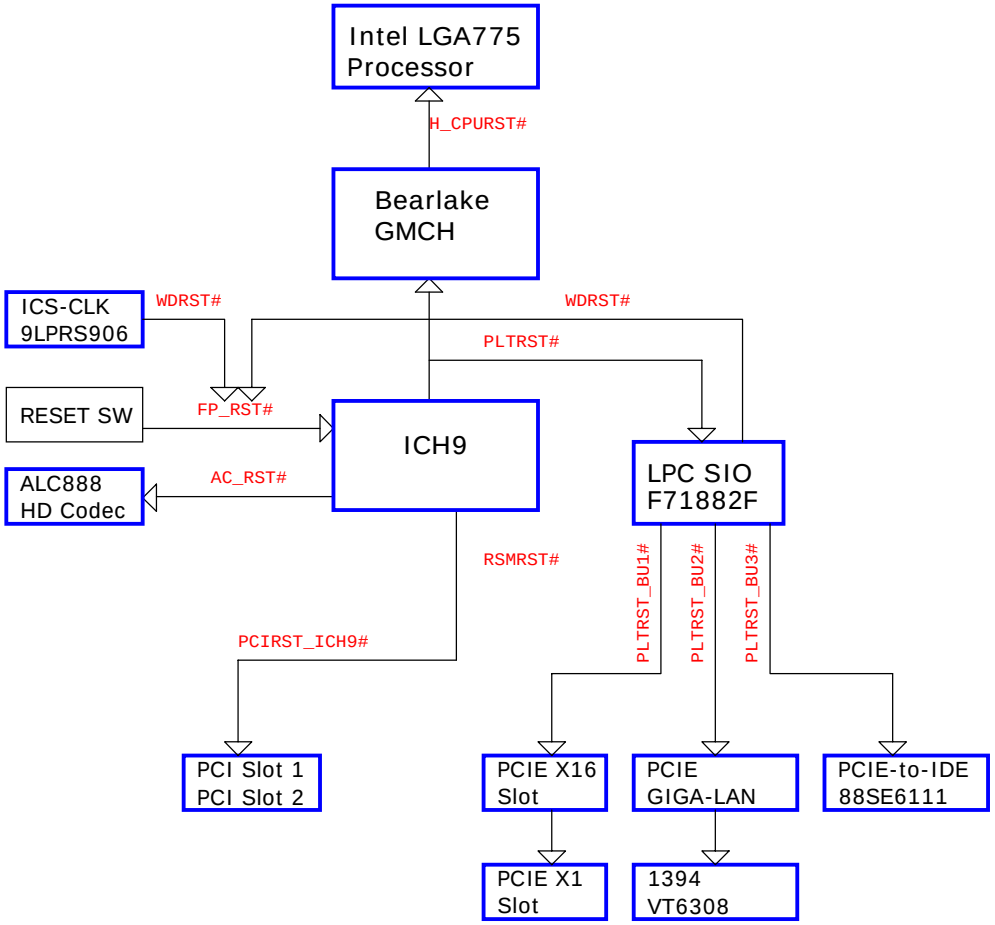
PL_RST

PCI_RST



MICRO-STAR INT'L CO.,LTD		
MS-7357		
Size: Custom	Document Description: PWROK MAP	Rev: 1.0
Date: Monday, March 26, 2007	Sheet 32 of 35	

RESET MAP



MICRO-STAR INT'L CO.,LTD		
MS-7357		
Size: Custom	Document Description: RESET MAP	Rev: 1.0
Date: Monday, March 26, 2007	Sheet 33 of 35	

0A change to 1.0

2007/03/19

1. Page15 : CLOCK GEN NEW P/N UPDATE TO ver: C (I11-RS90622-I02).
2. Page16 : COM port connector change to N51-09M0091-A10 , channel suggestion part.
3. Page16 : Remove beep circuit with F71882.
4. Page11 : Add a pull-hi to VCC5_ SB resistor(4.7K) for RSMRST# (R578).
5. Page22 : Reserve option resistor for UP7501 pin6, to select control by SLP_S4# or SLP_S5# (R607,R608).
6. Modify power solution.(Page21,22,23)
   1). Uninstall parts (R44 , RT3 , R10).
   2). R9 change to 0ohm.
   3). R48 install 82.5K resistor.
   4). C17 change to 33pf.
   5). R11 change to 2.49K ohm.
   6). R12 change to 15K ohm.
   7). C400,C432 change to 0.1uF.
   8). R343 install a 20K ohm resistor.
   9). R388 change to 4.22K ohm.
   10). R387 change to 1K ohm.
   11). Remove C230 , C624 , C70 , C265.
   12). R164 change to 510 ohm.
   13). R160 change to 10K ohm.
   14). R299 change to 2K ohm.
   15). C78 change to 1uF.
7. Page15 : Uninstall F75133 circuit.

2007/03/28

1. Page26 : D17 pin3 connect to LINE2_VREF & D25 pin3 connect to MIC2VREF0.

2007/03/30

1. Page23 : EC20,EC21,EC40,EC38 change footprint to 560UF_4V_R71D55.
2. Page20 : Add 2 resistors for H_SYNC & V_SYNC.
3. Page10-12 : SB change to ICH9.
4. Page24 : Uninstall SATA3 & SATA4.
5. Page10 : R534 change to 22 ohm 0402 1%.
6. Page6 : Follow Intel suggestion document to set CPU_GTLREF[3:0] to 63.5%.

2007/05/07

1. Modify part number to meet channel's suggestion.
   1). JVGA1 change to N51-15F0391-F02 .
   2). DIMM_A1 & DIMM_A2 change to N13-2400301-L06.
   3). DIMM_A1 & DIMM_A2 change to N13-2400351-L06.
   4). LAN_USB1 change to N58-22F0181-E06.
2. Page16 : FDD1 change to N32-2174011-H06.
3. Page16 : FS1 change to D08-0100200-P16.
4. Page21 : Uuinstall R48 and install R44 with 39.2K 1%.
5. Modify power team solution.
   1). R12 change to 18K.
   2). Install 100ohm resistor on R29.
   3). Install 220pF cap on C9.
   4). C17 change to 15pf.
   5). R27 change to 90.9ohm.
   6). R95 change to 20ohm.
   7). R28 change to 10ohm.
   8). Uninstall EC(2,5,6) & C(109,676).

2007/05/15

1. Page27 : SATA5 location name change to SATA7.
2. Page6-9 : Northbridge change new P/N to B01-LE82G25-I06.
3. Page16 : FS1 change to D08-0100210-P16 (RoHS).

2007/05/29 Create a new BOM for OEM customer Dixon.

1. Page16 : Remove JCOM1 & FDD1.
2. Page24 : SATA1 & SATA2 change color to RED (N5N-07M0311-H06).
3. Page27 : Remove SATA7.
4. Page11 : Remove JSPD1.
5. Page28 : Remove IEEE1394.
6. Page19 : Remove JUSB3.
7. Page6 & 20 : Remove onboard VGA function.