MS-7302 VER:0A

CPU:

AMD M2 Athlon 64/Athlon 64 FX AM2R2

System Chipset:

AMD/ATI RS780 colay RS740

AMD/ATI SB700

On Board Chipset:

FINTEK Super I/O -- F71882
LAN -- RTL8111C(B)/RTL8101E
HD Codec -- ALC888
BIOS -- SPI ROM 8M
1394 -- JMB381

Main Memory:

DDR II X 2 (Max 4GB)

Expansion Slots:

PCI-E X 1 *1
PCI-E X 16 *1

PCI 2.2 Slot X 2

Clock Generator:

Controller--ICS9LPRS477

PWM:

INTSIL6566 3 Phase+75125

Title	Cover Sheet
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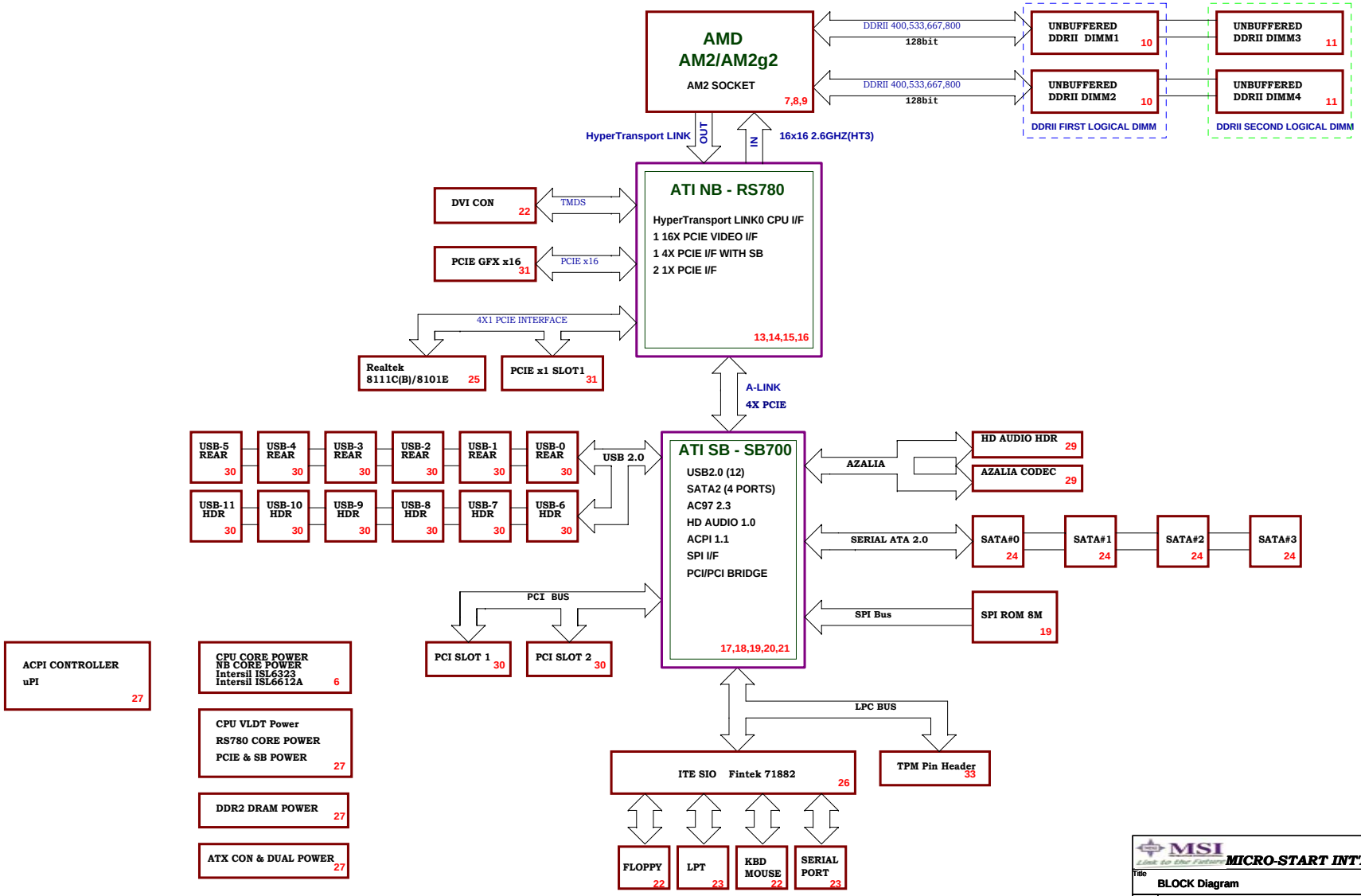
Project RS-780 BLOCK DIAGRAM



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Title: BLOCK Diagram		
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SB700 GPIO Config

GPIO Name	Type	Function Description	Pin	Page
PCICLK5/GPIO41	3.3V	PCI_CLK5	T3	17
REQ3#/GPIO70		PREQ#3	AE6	17
REQ4#/GPIO71		PREQ#4	AB6	17
GNT3#/GPIO72		Unused	AC6	17
GNT4#/GPIO73		Unused	AE5	17
INTE#/GPIO33		PCI_INTA#	AD3	17
INTF#/GPIO33		PCI_INTB#	AC4	17
INTG#/GPIO33		PCI_INTC#	AE2	17
INTH#/GPIO33		PCI_INTD#	AE3	17
LDRQ1#/GNT5#/GPIO68		Unused	AB8	17
BMREQ#/REQ5#/GPIO65		PREQ#5	AD7	17
RI#/EXTEVNT0#		RI#	E2	18
SLP_S2/GPM9#		Unused	H7	18
GA20IN/GEVENT0#		A20GATE	Y15	18
KBRST#/GEVENT1#		KBRST#	W15	18
LPC_PME#/GEVENT3#		LPC_PME#	K4	18
LPC_SMI#/EXTEVNT1#		LPC_SMI#	K24	18
S3_STATE/GEVENT5#		Unused	F1	18
SYS_RESET#/GPM7#		FP_RST#	J2	18
WAKE#/GEVENT8#		WAKE#	H6	18
BLINK/GPM6#		Unused	F2	18
SMBALERT#/THRMTRIP#/GEVENT2#		SMBALERT#	J6	18
SATA_ISO#/GPIO10		SB_GPIO10(Strapping)	AE18	18
CLK_REQ3#/SATA_IS1#/GPIO6		SB_GPIO6(Strapping)	AD18	18
SMARTVOLT/SATA_IS2#/GPIO4		SB_GPIO4(Strapping)	AA19	18
CLK_REQ0#/SATA_IS3#/GPIO0		SB_GPIO0(Strapping)	W17	18
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39		SB_GPIO39(Strapping)	V17	18
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40		SB_GPIO40(Strapping)	W20	18
SPKR/GPIO2		SPKR	W21	18
SCL0/GPOC0#		SCLK	AA18	18
SDA0/GPOC1#		SDATA	W18	18
SCL1/GPOC2#		SCLK1	K1	18
SDA1/GPOC3#		SDATA1	K2	18
DDC1_SCL/GPIO9		Unused	AA20	18
DDC1_SDA/GPIO8		SPI_WP#	Y18	18
LLB#/GPIO66		LC_SENSE	C1	18
SHUTDOWN#/GPIO5		SB_GPIO5(Strapping)	Y19	18
DDR3_RST#/GEVENT7#		Unused	G5	18
USB_OC6#/IR_TX1/GEVENT6#		OC4#	B9	18
USB_OC5#/IR_TX0/GPM5#		OC4#	B8	18
USB_OC4#/IR_RX0/GPM4#		OC3#	A8	18
USB_OC3#/IR_RX1/GPM3#		OC3#	A9	18
USB_OC2#/GPM2#		OC2#	E5	18
USB_OC1#/GPM1#		OC2#	F8	18
USB_OC0#/GPM0#		OC1#	E4	18
AZ_SDIN0/GPIO42		SDATA_IN_R	J7	18
AZ_SDIN1/GPIO43		Unused	J8	18
AZ_SDIN2/GPIO44		Unused	L8	18
AZ_SDIN3/GPIO46		Unused	M3	18

GPIO Name	Type	Function Description	Pin	Page
AZ_DOCK_RST#/GPM8#		Unused	L5	18
PS2_DAT/EC_GPIO0		Unused	H19	18
PS2_CLK/EC_GPIO1		Unused	H20	18
SPI_CS2#/EC_GPIO2		Unused	H21	18
IDE_RST#/F_RST#/EC_GPO3		Unused	F25	18
PS2KB_DAT/EC_GPIO4		Unused	D22	18
PS2KB_CLK/EC_GPIO5		Unused	E24	18
PS2M_DAT/EC_GPIO6		Unused	E25	18
PS2M_CLK/EC_GPIO7		Unused	D23	18
USBCLK/14M_25M_48M_OSC		USB_48M_CLK	C8	18
KSO_16/EC_GPIO8		Unused	A18	18
KSO_17/EC_GPIO9		Unused	B18	18
EC_PWM0/EC_GPIO10		Unused	F21	18
SCL2/EC_GPIO11		Unused	D21	18
SDA2/EC_GPIO12		Unused	F19	18
SCL3_LV/EC_GPIO13		Unused	E20	18
SDA3_LV/EC_GPIO14		Unused	E21	18
EC_PWM1/EC_GPIO15		Unused	E19	18
EC_PWM2/EC_GPIO16		SB_GP16(Strapping)	D19	18
EC_PWM3/EC_GPIO17		Unused	E18	18
KSI_0/EC_GPIO18		Unused	G20	18
KSI_1/EC_GPIO19		Unused	G21	18
KSI_2/EC_GPIO20		Unused	D25	18
KSI_3/EC_GPIO21		Unused	D24	18
KSI_4/EC_GPIO22		Unused	C25	18
KSI_5/EC_GPIO23		Unused	C24	18
KSI_6/EC_GPIO24		Unused	B25	18
KSI_7/EC_GPIO25		Unused	C23	18
KSO_0/EC_GPIO26		Unused	B24	18
KSO_1/EC_GPIO27		Unused	B23	18
KSO_2/EC_GPIO28		Unused	A23	18
KSO_3/EC_GPIO29		Unused	C22	18
KSO_4/EC_GPIO30		Unused	A22	18
KSO_5/EC_GPIO31		Unused	B22	18
KSO_6/EC_GPIO32		Unused	B21	18
KSO_7/EC_GPIO33		Unused	A21	18
KSO_8/EC_GPIO34		Unused	D20	18
KSO_9/EC_GPIO35		Unused	C20	18
KSO_10/EC_GPIO36		Unused	A20	18
KSO_11/EC_GPIO37		Unused	B20	18
KSO_12/EC_GPIO38		Unused	B19	18
KSO_13/EC_GPIO39		Unused	A19	18
KSO_14/EC_GPIO40		Unused	D18	18
KSO_15/EC_GPIO41		Unused	C18	18
SATA_ACT#/GPIO67		SATA_LED#	W11	19
IDE_D0/GPIO15		Unused	AD24	19
IDE_D1/GPIO16		Unused	AD23	19
IDE_D2/GPIO17		Unused	AE22	19
IDE_D3/GPIO18		Unused	AC22	19

GPIO Name	Type	Function Description	Pin	Page
IDE_D4/GPIO19		Unused	AD21	19
IDE_D5/GPIO20		Unused	AE20	19
IDE_D6/GPIO21		Unused	AB20	19
IDE_D7/GPIO22		Unused	AD19	19
IDE_D8/GPIO23		Unused	AE19	19
IDE_D9/GPIO24		Unused	AC20	19
IDE_D10/GPIO25		Unused	AD20	19
IDE_D11/GPIO26		Unused	AE21	19
IDE_D12/GPIO27		Unused	AB22	19
IDE_D13/GPIO28		Unused	AD22	19
IDE_D14/GPIO29		Unused	AE23	19
IDE_D15/GPIO30		Unused	AC23	19
SPI_DI/GPIO12		SPI_DATAIN	G6	19
SPI_DO/GPIO11		SPI_DATAOUT	D2	19
SPI_CLK/GPIO47		SPI_CLK	D1	19
SPI_HOLD#/GPIO31		SPI_HOLD_L	F4	19
SPI_CS#/GPIO32		SPI_CS#	F3	19
LAN_RST#GPIO13		CPU_PRESENT#	U15	19
ROM_RST#/GPIO14		Unused	J1	19
FANOUT0/GPIO3		Unused	M8	19
FANOUT1/GPIO48		COM_GPIO	M5	19
FANOUT2/GPIO49		Unused	M7	19
FANIN0/GPIO50		Unused	P5	19
FANIN1/GPIO51		Unused	P8	19
FANIN2/GPIO52		Unused	E8	19
TEMPIN0/GPIO61		Unused	B6	19
TEMPIN1/GPIO62		Unused	A6	19
TEMPIN2/GPIO63		Unused	A5	19
TEMPIN3/TALERT#/GPIO64		TALERT#	B5	19
VIN0/GPIO53		BIOS_WP#1	A4	19
VIN1/GPIO54		BIOS_WP#2	B4	19
VIN2/GPIO55		CLR_CMOS	C4	19
VIN3/GPIO56		LAN_DISABLE	D4	19
VIN4/GPIO57		Unused	D5	19
VIN5/GPIO58		Unused	D6	19
VIN6/GPIO59		Unused	A7	19
VIN7/GPIO60		Unused	B7	19

Super I/O GPIO Config

GPIO Name	Type	Function Description	Pin	Page
VID0/GP27		LEO_GPIO2	20	26
VID0/GP26		LEO_GPIO1	21	26
VID0/GP21/VGP0		LEO_GPIO0	26	26
PME#/GP54		LPC_PME#	73	26
KRST#/GP62		KBRST#	45	26
GA20/JP7		A20GATE	46	26
KDAT/GP61		KBDATA	80	26
KCLK/GP60		KBCLK	81	26
MDAT/GP57		MSDATA	82	26
MCLK/GP56		MSCLK	83	26
SUSC#/GP53		LPC_SMI#	77	26
PSON#/GP42		PS_ON#	76	26
PANSWH#/GP43		PSIN	75	26
PWRON#/GP44		SB_PWRON#	72	26
PCIRST3#/GP11		ASSID_GPIO0	34	26
PCIRST2#/GP12		ASSID_GPIO1	33	26
FAN_CTL3/GP36		PWRFAN_PWM	12	26
FAN_TAC3/GP37		PWRFAN_TAC	11	26
FAN_CTL2/GP51		SYSFAN_PWM	10	26
FAN_TAC2/GP52		SYSFAN_TAC	9	26
FAN_CTL1		CPUFAN_PWM	8	26
FAN_TAC1		CPUFAN_TAC	7	26
VID2/GP32		COM_GPIO2	17	26
VID3/GP33		FUSB_G1	16	26
VID4/GP34		FUSB_G2	14	26
VID5/GP35		FUSB_G3	13	26

PCI Config.

DEVICE	MCP1 INT Pin	REQ# / GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INTA# PCI_INTB# PCI_INTC# PCI_INTD#	PREQ#0 PGNT#0	AD16	PCICLK0
PCI Slot 2	PCI_INTB# PCI_INTC# PCI_INTD# PCI_INTA#	PREQ#1 PGNT#1	AD17	PCICLK1

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Title: GPIO Configuration

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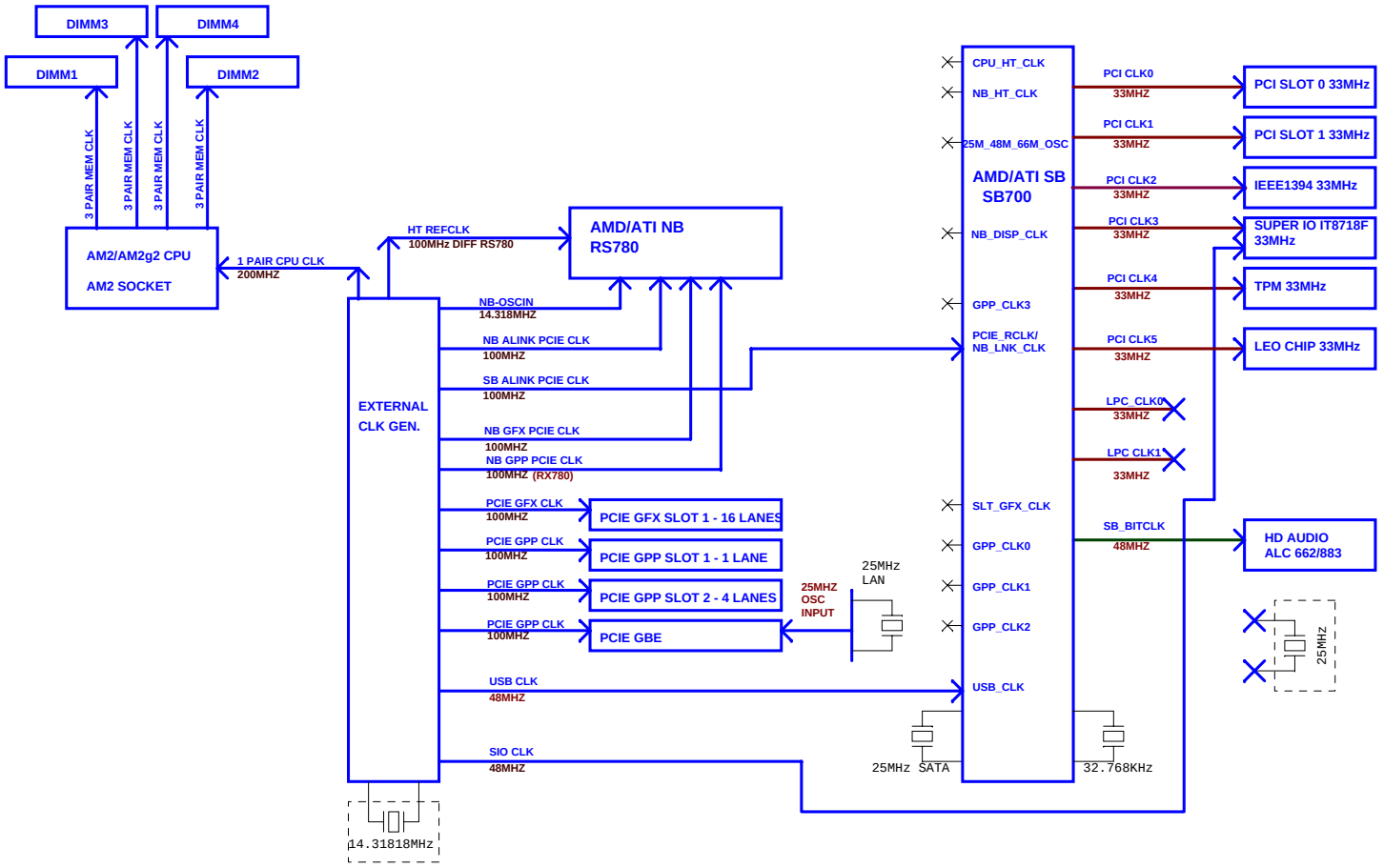

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Title: Clock Distribution		
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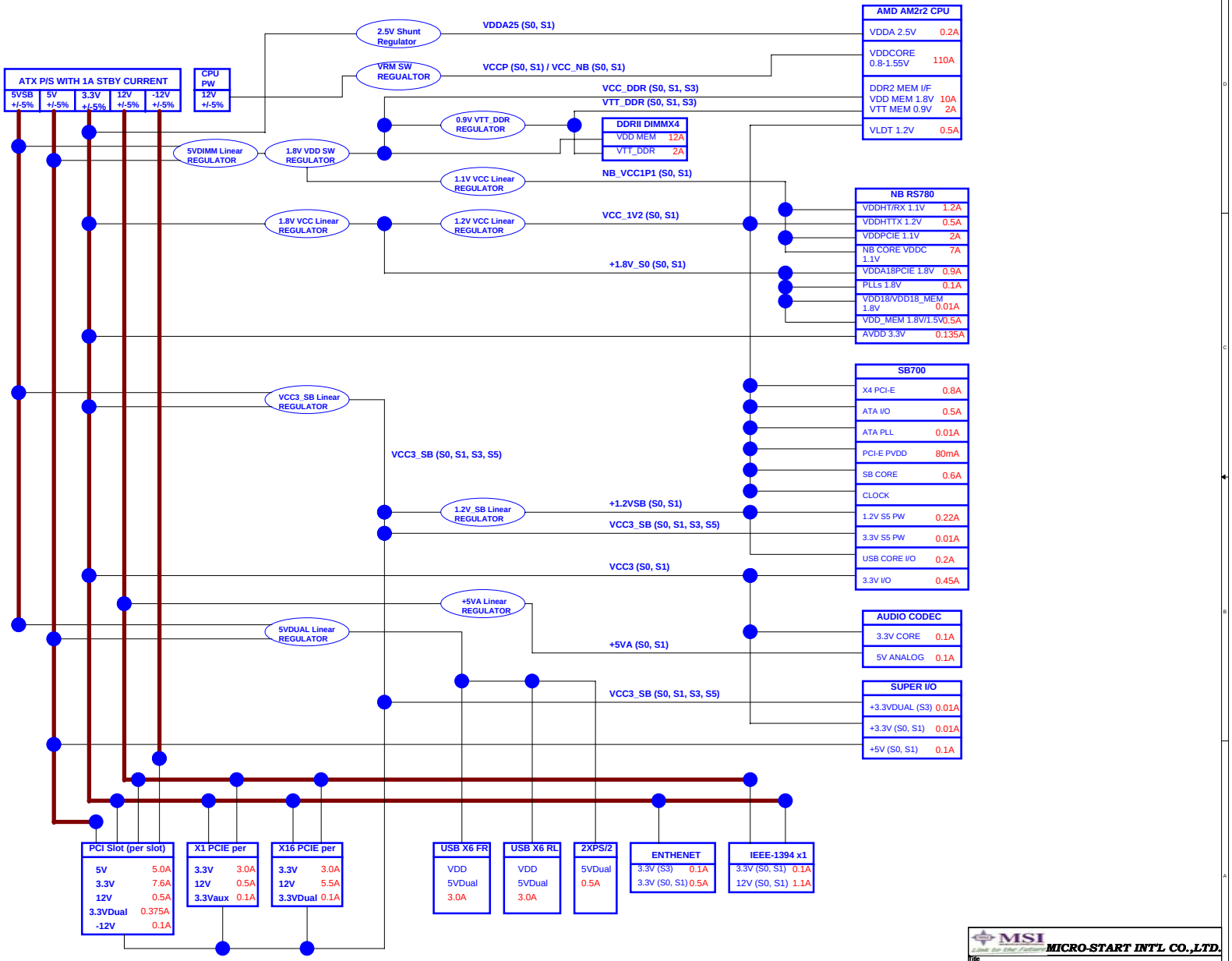
Power Deliver Chart



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Title: Power Deliver Chart

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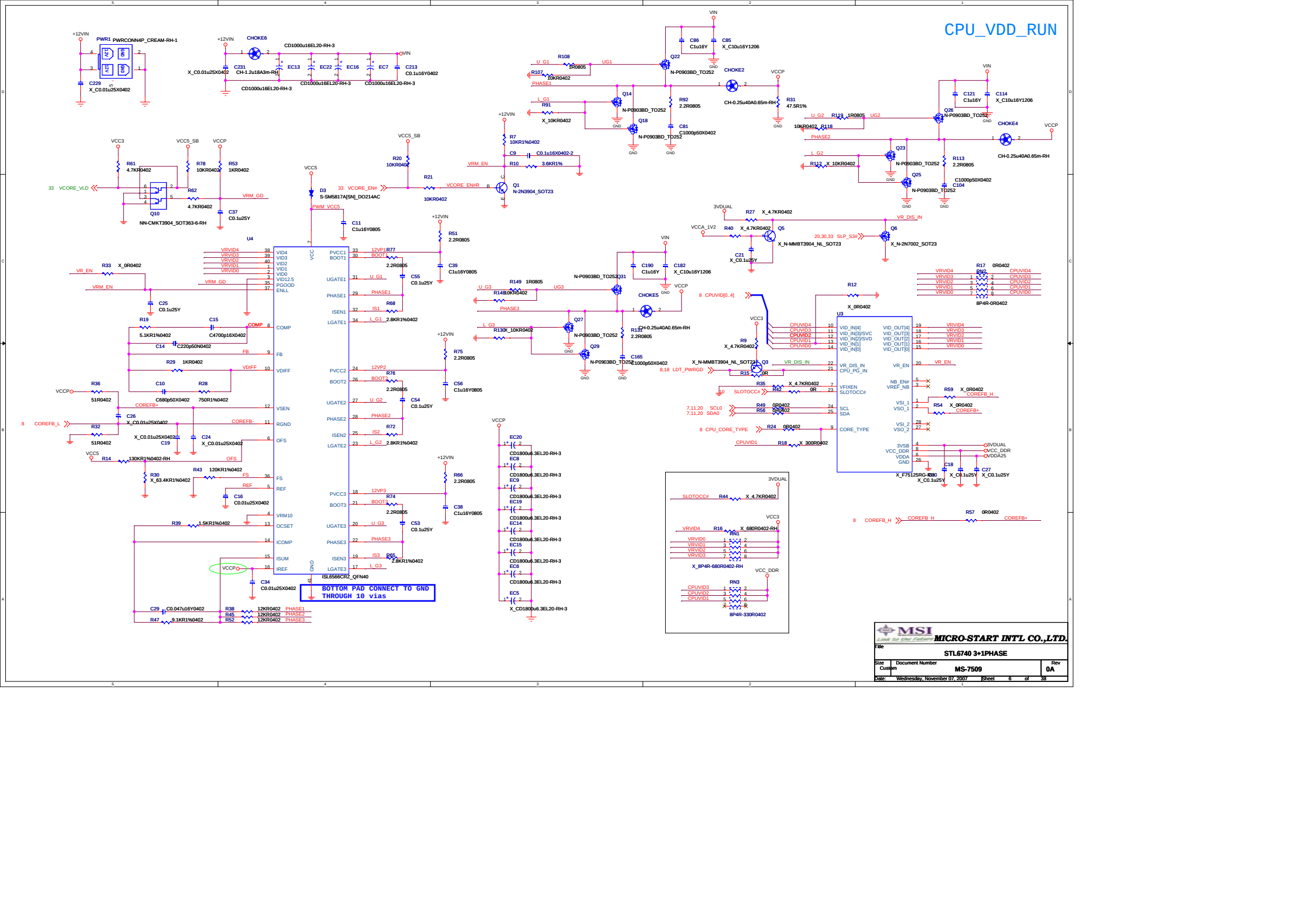
CPU_VDD_RUN
BOTTOM PAD CONNECT TO GND THROUGH 10 vias
MICRO-START INTL CO.,LTD.
STL6740 3+1PHASE
MS-7509
0A
Wednesday, November 07, 2007
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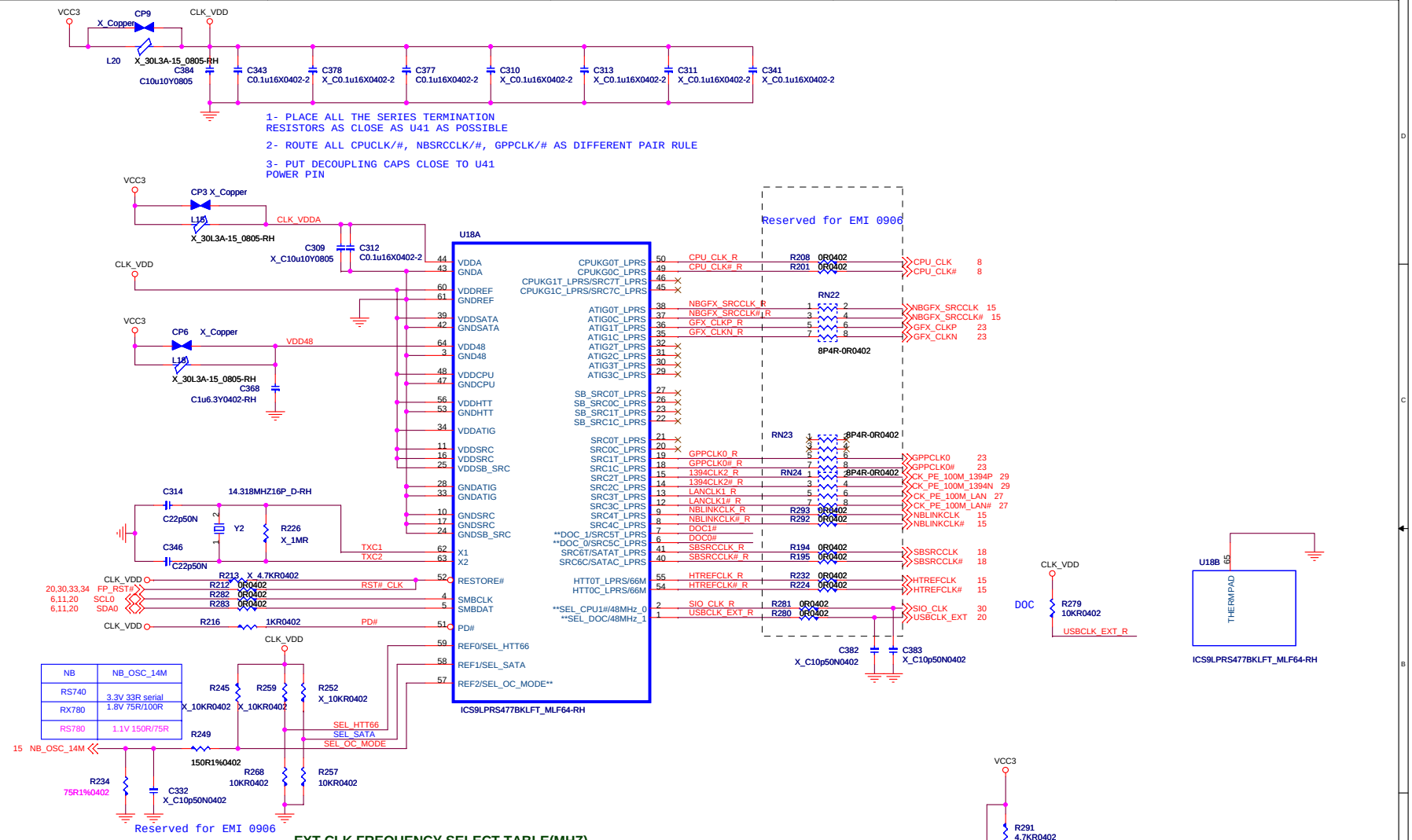

EXT CLK FREQUENCY SELECT TABLE(MHZ)

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal HAMMER operation

Micro Star Restricted Secret

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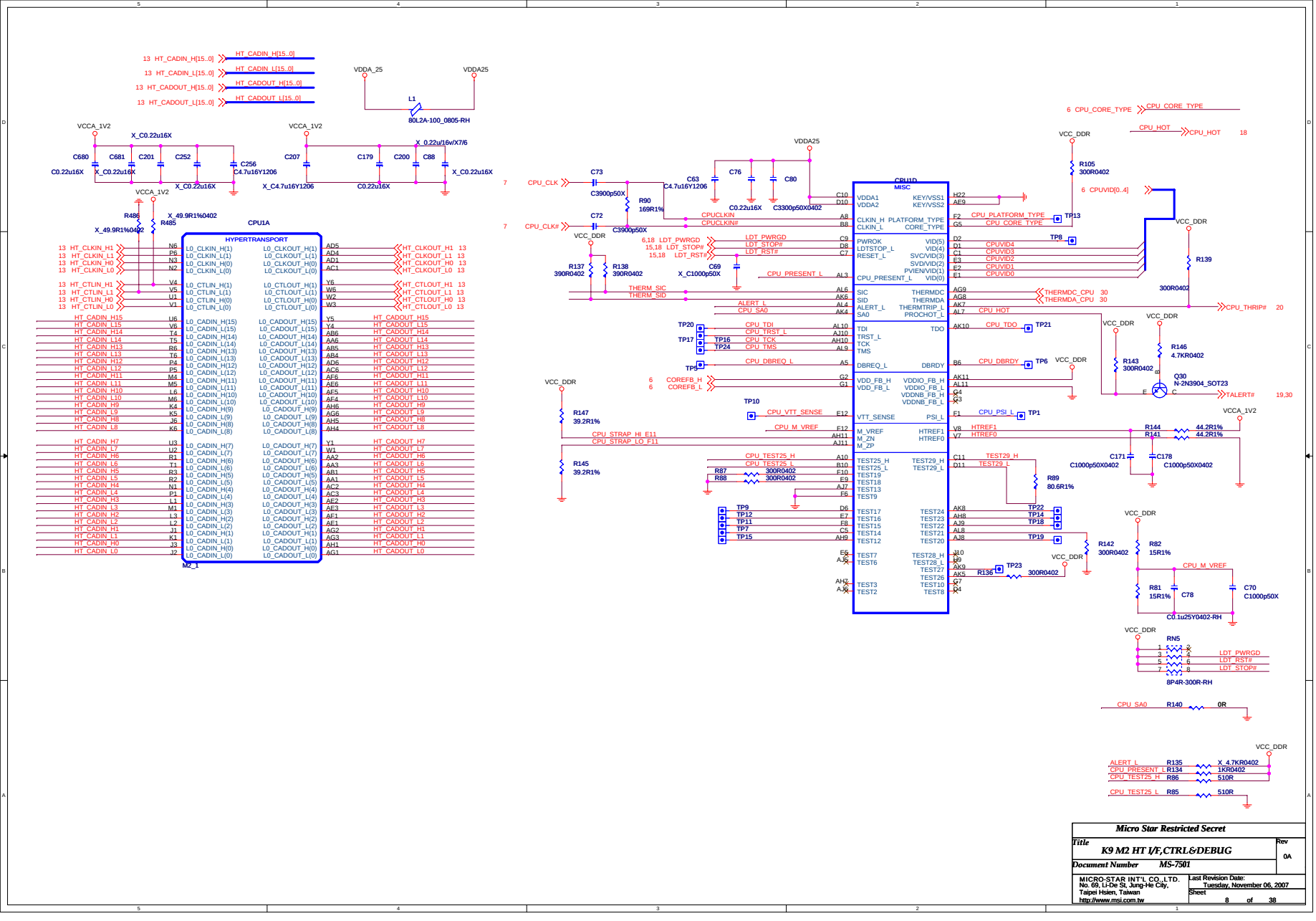

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Title	*K9 M2 HT I/F,CTRL&DEBUG*	Rev 0A
Document Number	*MS-7501*	
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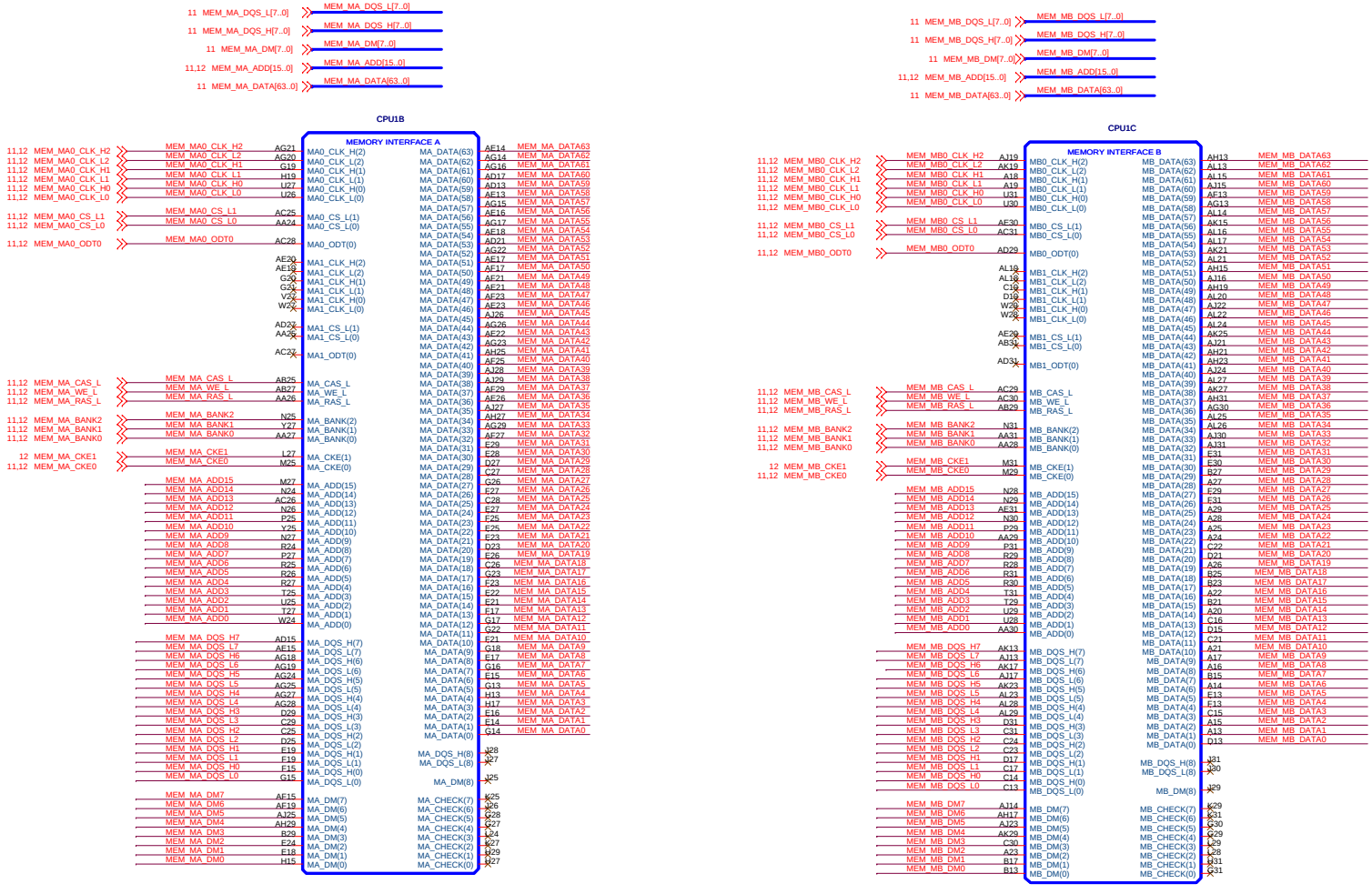
11 MEM_MA_DQS_L[7..0]
MEM_MA_DQS_L[7..0]
11 MEM_MA_DQS_H[7..0]
MEM_MA_DQS_H[7..0]
11 MEM_MA_DM[7..0]
MEM_MA_DM[7..0]
11,12 MEM_MA_ADD[15..0]
MEM_MA_ADD[15..0]
11 MEM_MA_DATA[63..0]
MEM_MA_DATA[63..0]
CPU1B
MEMORY INTERFACE A
11,12 MEM_MA0_CLK_H2
11,12 MEM_MA0_CLK_L2
11,12 MEM_MA0_CLK_H1
11,12 MEM_MA0_CLK_L1
11,12 MEM_MA0_CLK_H0
11,12 MEM_MA0_CLK_L0
MEM_MA0_CLK_H2
MEM_MA0_CLK_L2
MEM_MA0_CLK_H1
MEM_MA0_CLK_L1
MEM_MA0_CLK_H0
MEM_MA0_CLK_L0
AG21
AG20
G19
H19
U27
U26
MA0_CLK_H(2)
MA0_CLK_L(2)
MA0_CLK_H(1)
MA0_CLK_L(1)
MA0_CLK_H(0)
MA0_CLK_L(0)
11,12 MEM_MA0_CS_L1
11,12 MEM_MA0_CS_L0
MEM_MA0_CS_L1
MEM_MA0_CS_L0
AC25
AA24
MA0_CS_L(1)
MA0_CS_L(0)
11,12 MEM_MA0_ODT0
MEM_MA0_ODT0
AC28
MA0_ODT(0)
AE20
AE19
G20
G21
V21
W22
MA1_CLK_H(2)
MA1_CLK_L(2)
MA1_CLK_H(1)
MA1_CLK_L(1)
MA1_CLK_H(0)
MA1_CLK_L(0)
AD22
AA22
MA1_CS_L(1)
MA1_CS_L(0)
AC27
MA1_ODT(0)
11,12 MEM_MA_CAS_L
11,12 MEM_MA_WE_L
11,12 MEM_MA_RAS_L
MEM_MA_CAS_L
MEM_MA_WE_L
MEM_MA_RAS_L
AB25
AB27
AA26
MA_CAS_L
MA_WE_L
MA_RAS_L
11,12 MEM_MA_BANK2
11,12 MEM_MA_BANK1
11,12 MEM_MA_BANK0
MEM_MA_BANK2
MEM_MA_BANK1
MEM_MA_BANK0
N25
Y27
AA27
MA_BANK(2)
MA_BANK(1)
MA_BANK(0)
12 MEM_MA_CKE1
11,12 MEM_MA_CKE0
MEM_MA_CKE1
MEM_MA_CKE0
L27
M25
MA_CKE(1)
MA_CKE(0)
MEM_MA_ADD15
MEM_MA_ADD14
MEM_MA_ADD13
MEM_MA_ADD12
MEM_MA_ADD11
MEM_MA_ADD10
MEM_MA_ADD9
MEM_MA_ADD8
MEM_MA_ADD7
MEM_MA_ADD6
MEM_MA_ADD5
MEM_MA_ADD4
MEM_MA_ADD3
MEM_MA_ADD2
MEM_MA_ADD1
MEM_MA_ADD0
M27
N24
AC26
N26
P25
Y25
N27
R24
P27
R25
R26
R27
T25
U25
T27
W24
MA_ADD(15)
MA_ADD(14)
MA_ADD(13)
MA_ADD(12)
MA_ADD(11)
MA_ADD(10)
MA_ADD(9)
MA_ADD(8)
MA_ADD(7)
MA_ADD(6)
MA_ADD(5)
MA_ADD(4)
MA_ADD(3)
MA_ADD(2)
MA_ADD(1)
MA_ADD(0)
MEM_MA_DQS_H7
MEM_MA_DQS_L7
MEM_MA_DQS_H6
MEM_MA_DQS_L6
MEM_MA_DQS_H5
MEM_MA_DQS_L5
MEM_MA_DQS_H4
MEM_MA_DQS_L4
MEM_MA_DQS_H3
MEM_MA_DQS_L3
MEM_MA_DQS_H2
MEM_MA_DQS_L2
MEM_MA_DQS_H1
MEM_MA_DQS_L1
MEM_MA_DQS_H0
MEM_MA_DQS_L0
AD15
AE15
AG18
AG19
AG24
AG25
AG27
AG28
D29
C29
C25
D25
E19
F19
F15
G15
MA_DQS_H(7)
MA_DQS_L(7)
MA_DQS_H(6)
MA_DQS_L(6)
MA_DQS_H(5)
MA_DQS_L(5)
MA_DQS_H(4)
MA_DQS_L(4)
MA_DQS_H(3)
MA_DQS_L(3)
MA_DQS_H(2)
MA_DQS_L(2)
MA_DQS_H(1)
MA_DQS_L(1)
MA_DQS_H(0)
MA_DQS_L(0)
MEM_MA_DM7
MEM_MA_DM6
MEM_MA_DM5
MEM_MA_DM4
MEM_MA_DM3
MEM_MA_DM2
MEM_MA_DM1
MEM_MA_DM0
AF15
AF19
AJ25
AH29
B29
E24
E18
H15
MA_DM(7)
MA_DM(6)
MA_DM(5)
MA_DM(4)
MA_DM(3)
MA_DM(2)
MA_DM(1)
MA_DM(0)
AE14
AG14
AG16
AD17
AD13
AE13
AG15
AE16
AG17
AE18
AD21
AG22
AE17
AE17
AF21
AE23
AF23
AJ26
AG26
AE22
AG23
AH25
AF25
AJ28
AJ29
AE29
AE26
AJ27
AG29
AF27
E29
E28
D27
C27
G26
E27
C28
E27
F25
E25
E23
D23
E26
C26
G23
F23
E22
E21
E17
G17
G22
E21
G18
E17
G16
E15
G13
H13
H17
E16
E14
G14
MA_DATA(63)
MA_DATA(62)
MA_DATA(61)
MA_DATA(60)
MA_DATA(59)
MA_DATA(58)
MA_DATA(57)
MA_DATA(56)
MA_DATA(55)
MA_DATA(54)
MA_DATA(53)
MA_DATA(52)
MA_DATA(51)
MA_DATA(50)
MA_DATA(49)
MA_DATA(48)
MA_DATA(47)
MA_DATA(46)
MA_DATA(45)
MA_DATA(44)
MA_DATA(43)
MA_DATA(42)
MA_DATA(41)
MA_DATA(40)
MA_DATA(39)
MA_DATA(38)
MA_DATA(37)
MA_DATA(36)
MA_DATA(35)
MA_DATA(34)
MA_DATA(33)
MA_DATA(32)
MA_DATA(31)
MA_DATA(30)
MA_DATA(29)
MA_DATA(28)
MA_DATA(27)
MA_DATA(26)
MA_DATA(25)
MA_DATA(24)
MA_DATA(23)
MA_DATA(22)
MA_DATA(21)
MA_DATA(20)
MA_DATA(19)
MA_DATA(18)
MA_DATA(17)
MA_DATA(16)
MA_DATA(15)
MA_DATA(14)
MA_DATA(13)
MA_DATA(12)
MA_DATA(11)
MA_DATA(10)
MA_DATA(9)
MA_DATA(8)
MA_DATA(7)
MA_DATA(6)
MA_DATA(5)
MA_DATA(4)
MA_DATA(3)
MA_DATA(2)
MA_DATA(1)
MA_DATA(0)
MEM_MA_DATA63
MEM_MA_DATA62
MEM_MA_DATA61
MEM_MA_DATA60
MEM_MA_DATA59
MEM_MA_DATA58
MEM_MA_DATA57
MEM_MA_DATA56
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MEM_MA_DATA40
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MEM_MA_DATA29
MEM_MA_DATA28
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MEM_MA_DATA26
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MEM_MA_DATA23
MEM_MA_DATA22
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MEM_MA_DATA13
MEM_MA_DATA12
MEM_MA_DATA11
MEM_MA_DATA10
MEM_MA_DATA9
MEM_MA_DATA8
MEM_MA_DATA7
MEM_MA_DATA6
MEM_MA_DATA5
MEM_MA_DATA4
MEM_MA_DATA3
MEM_MA_DATA2
MEM_MA_DATA1
MEM_MA_DATA0
MA_DQS_H(8)
MA_DQS_L(8)
MA_DM(8)
MA_CHECK(7)
MA_CHECK(6)
MA_CHECK(5)
MA_CHECK(4)
MA_CHECK(3)
MA_CHECK(2)
MA_CHECK(1)
MA_CHECK(0)
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MEM_MB_DQS_L[7..0]
11 MEM_MB_DQS_H[7..0]
MEM_MB_DQS_H[7..0]
11 MEM_MB_DM[7..0]
MEM_MB_DM[7..0]
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MEM_MB_ADD[15..0]
11 MEM_MB_DATA[63..0]
MEM_MB_DATA[63..0]
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11,12 MEM_MB0_CLK_L2
11,12 MEM_MB0_CLK_H1
11,12 MEM_MB0_CLK_L1
11,12 MEM_MB0_CLK_H0
11,12 MEM_MB0_CLK_L0
MEM_MB0_CLK_H2
MEM_MB0_CLK_L2
MEM_MB0_CLK_H1
MEM_MB0_CLK_L1
MEM_MB0_CLK_H0
MEM_MB0_CLK_L0
AJ19
AK19
A18
A19
U31
U30
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MB0_CLK_L(2)
MB0_CLK_H(1)
MB0_CLK_L(1)
MB0_CLK_H(0)
MB0_CLK_L(0)
11,12 MEM_MB0_CS_L1
11,12 MEM_MB0_CS_L0
MEM_MB0_CS_L1
MEM_MB0_CS_L0
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AC31
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MB0_CS_L(0)
11,12 MEM_MB0_ODT0
MEM_MB0_ODT0
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MB0_ODT(0)
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AL18
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MB1_CLK_H(2)
MB1_CLK_L(2)
MB1_CLK_H(1)
MB1_CLK_L(1)
MB1_CLK_H(0)
MB1_CLK_L(0)
AE29
AB31
MB1_CS_L(1)
MB1_CS_L(0)
AD31
MB1_ODT(0)
11,12 MEM_MB_CAS_L
11,12 MEM_MB_WE_L
11,12 MEM_MB_RAS_L
MEM_MB_CAS_L
MEM_MB_WE_L
MEM_MB_RAS_L
AC29
AC30
AB29
MB_CAS_L
MB_WE_L
MB_RAS_L
11,12 MEM_MB_BANK2
11,12 MEM_MB_BANK1
11,12 MEM_MB_BANK0
MEM_MB_BANK2
MEM_MB_BANK1
MEM_MB_BANK0
N31
AA31
AA28
MB_BANK(2)
MB_BANK(1)
MB_BANK(0)
12 MEM_MB_CKE1
11,12 MEM_MB_CKE0
MEM_MB_CKE1
MEM_MB_CKE0
M31
M29
MB_CKE(1)
MB_CKE(0)
MEM_MB_ADD15
MEM_MB_ADD14
MEM_MB_ADD13
MEM_MB_ADD12
MEM_MB_ADD11
MEM_MB_ADD10
MEM_MB_ADD9
MEM_MB_ADD8
MEM_MB_ADD7
MEM_MB_ADD6
MEM_MB_ADD5
MEM_MB_ADD4
MEM_MB_ADD3
MEM_MB_ADD2
MEM_MB_ADD1
MEM_MB_ADD0
N28
N29
AE31
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R29
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R31
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T31
T29
U29
U28
AA30
MB_ADD(15)
MB_ADD(14)
MB_ADD(13)
MB_ADD(12)
MB_ADD(11)
MB_ADD(10)
MB_ADD(9)
MB_ADD(8)
MB_ADD(7)
MB_ADD(6)
MB_ADD(5)
MB_ADD(4)
MB_ADD(3)
MB_ADD(2)
MB_ADD(1)
MB_ADD(0)
MEM_MB_DQS_H7
MEM_MB_DQS_L7
MEM_MB_DQS_H6
MEM_MB_DQS_L6
MEM_MB_DQS_H5
MEM_MB_DQS_L5
MEM_MB_DQS_H4
MEM_MB_DQS_L4
MEM_MB_DQS_H3
MEM_MB_DQS_L3
MEM_MB_DQS_H2
MEM_MB_DQS_L2
MEM_MB_DQS_H1
MEM_MB_DQS_L1
MEM_MB_DQS_H0
MEM_MB_DQS_L0
AK13
AJ13
AK17
A17
AK23
AL23
AL28
AL29
D31
C31
C24
C23
D17
C17
C14
C13
MB_DQS_H(7)
MB_DQS_L(7)
MB_DQS_H(6)
MB_DQS_L(6)
MB_DQS_H(5)
MB_DQS_L(5)
MB_DQS_H(4)
MB_DQS_L(4)
MB_DQS_H(3)
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MB_DQS_H(2)
MB_DQS_L(2)
MB_DQS_H(1)
MB_DQS_L(1)
MB_DQS_H(0)
MB_DQS_L(0)
MEM_MB_DM7
MEM_MB_DM6
MEM_MB_DM5
MEM_MB_DM4
MEM_MB_DM3
MEM_MB_DM2
MEM_MB_DM1
MEM_MB_DM0
AJ14
AH17
AJ23
AK29
C30
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MB_DM(7)
MB_DM(6)
MB_DM(5)
MB_DM(4)
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AH13
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AL15
AJ15
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AL16
AL17
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AH15
AJ16
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MB_DQS_H(8)
MB_DQS_L(8)
MB_DM(8)
MB_CHECK(7)
MB_CHECK(6)
MB_CHECK(5)
MB_CHECK(4)
MB_CHECK(3)
MB_CHECK(2)
MB_CHECK(1)
MB_CHECK(0)
MEM_MB_DATA63
MEM_MB_DATA62
MEM_MB_DATA61
MEM_MB_DATA60
MEM_MB_DATA59
MEM_MB_DATA58
MEM_MB_DATA57
MEM_MB_DATA56
MEM_MB_DATA55
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MEM_MB_DATA53
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MEM_MB_DATA49
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MEM_MB_DATA13
MEM_MB_DATA12
MEM_MB_DATA11
MEM_MB_DATA10
MEM_MB_DATA9
MEM_MB_DATA8
MEM_MB_DATA7
MEM_MB_DATA6
MEM_MB_DATA5
MEM_MB_DATA4
MEM_MB_DATA3
MEM_MB_DATA2
MEM_MB_DATA1
MEM_MB_DATA0
Micro Star Restricted Secret
Title
K9 M2 DDR MEMORY I/F
Rev
0A
Document Number
MS-7501
MICRO-STAR INT'L CO.,LTD.
No. 69, Li-De St, Jung-He City,
Taipei Hsien, Taiwan
http://www.msi.com.tw
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Tuesday, November 06, 2007
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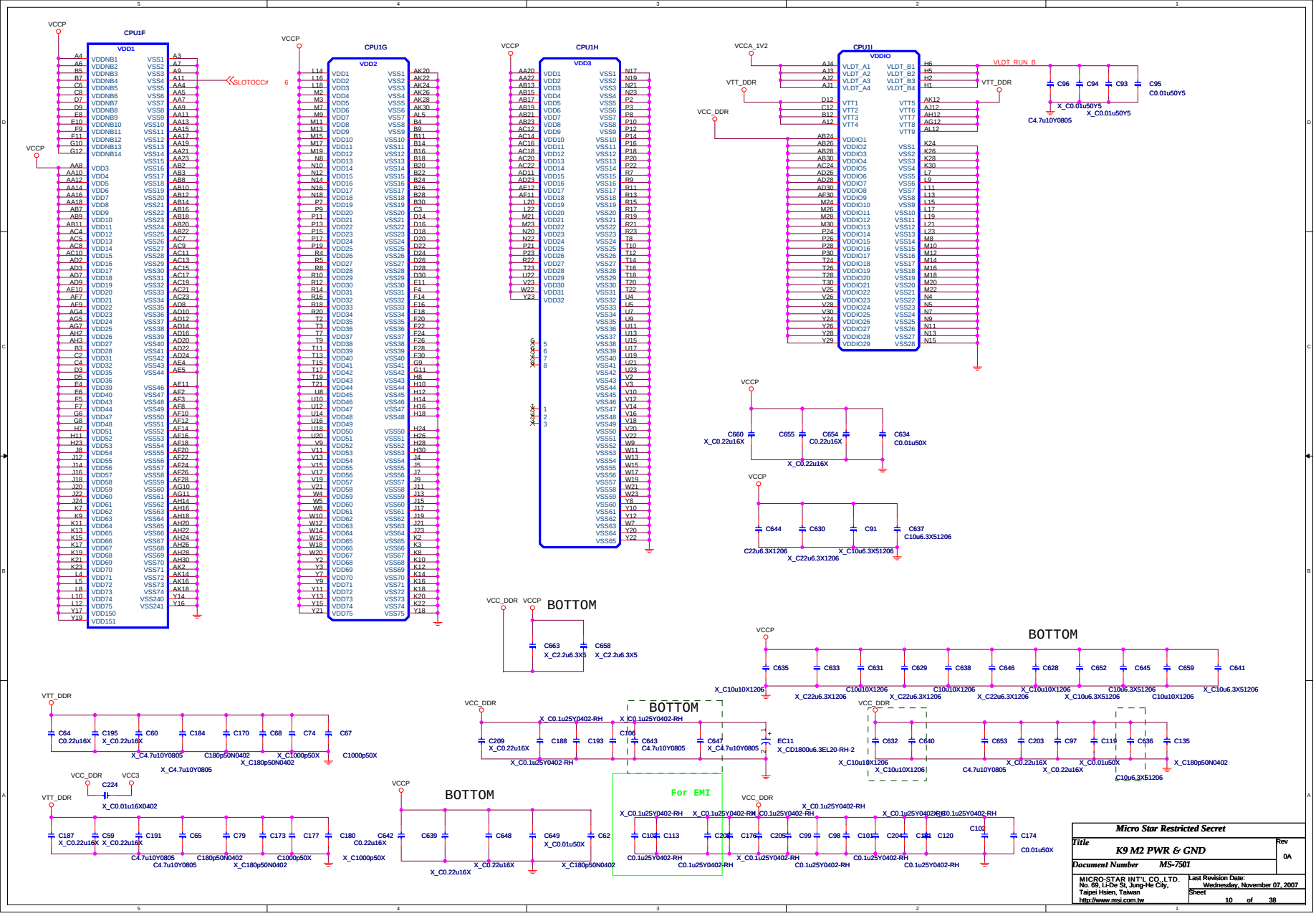
CPU1F
VDD1
CPU1G
VDD2
CPU1H
VDD3
CPU1I
VDDIO
VCCP
VTT_DDR
VCC_DDR
VCCA_1V2
VCC3
SLOTOCC#
VLDT_RUN_B
BOTTOM
For EMI
Micro Star Restricted Secret
Title
K9 M2 PWR & GND
Rev
0A
Document Number
MS-7501
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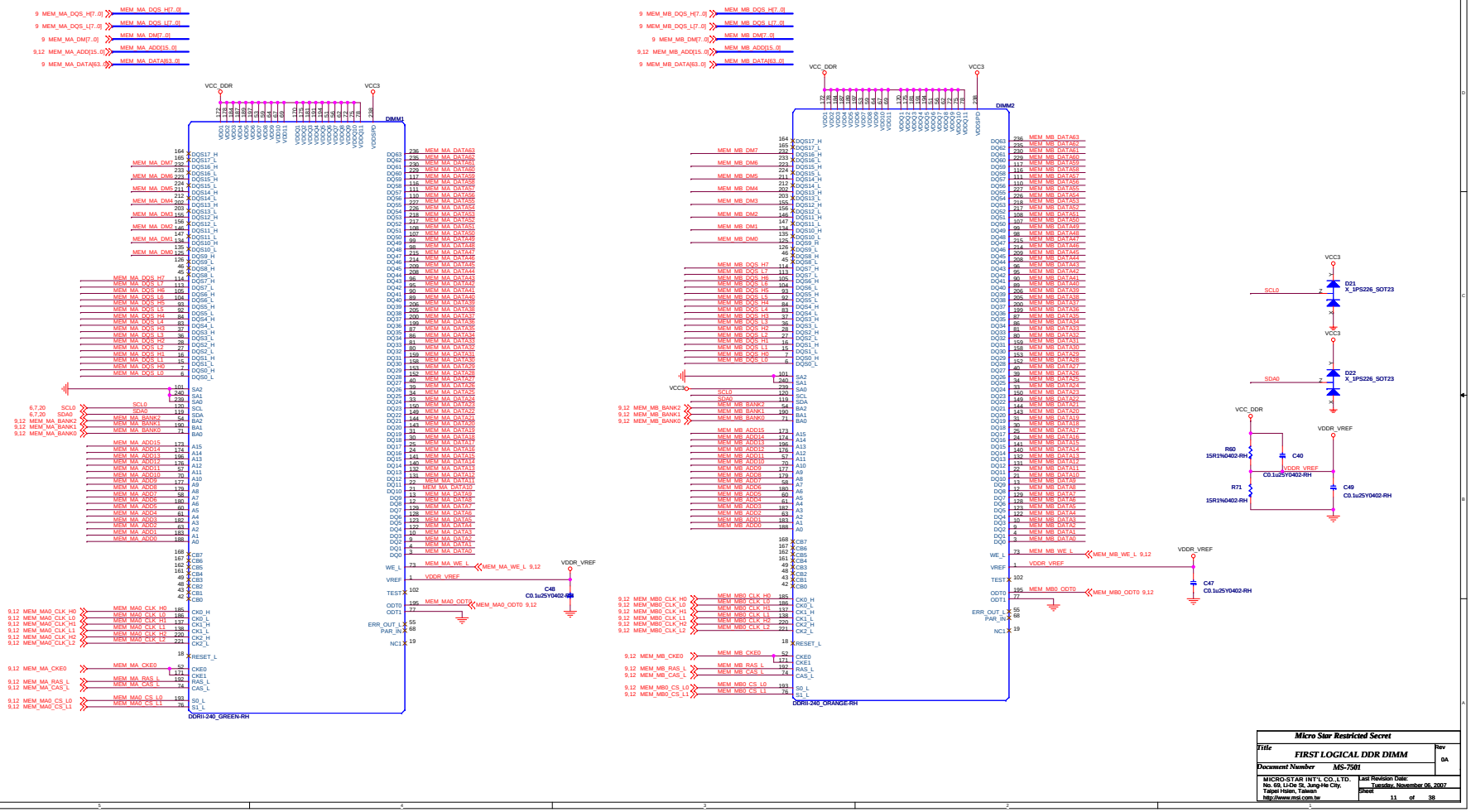

Micro Star Restricted Secret	
Title: **FIRST LOGICAL DDR DIMM**	Rev: 0A
Document Number: **MS-7501**	
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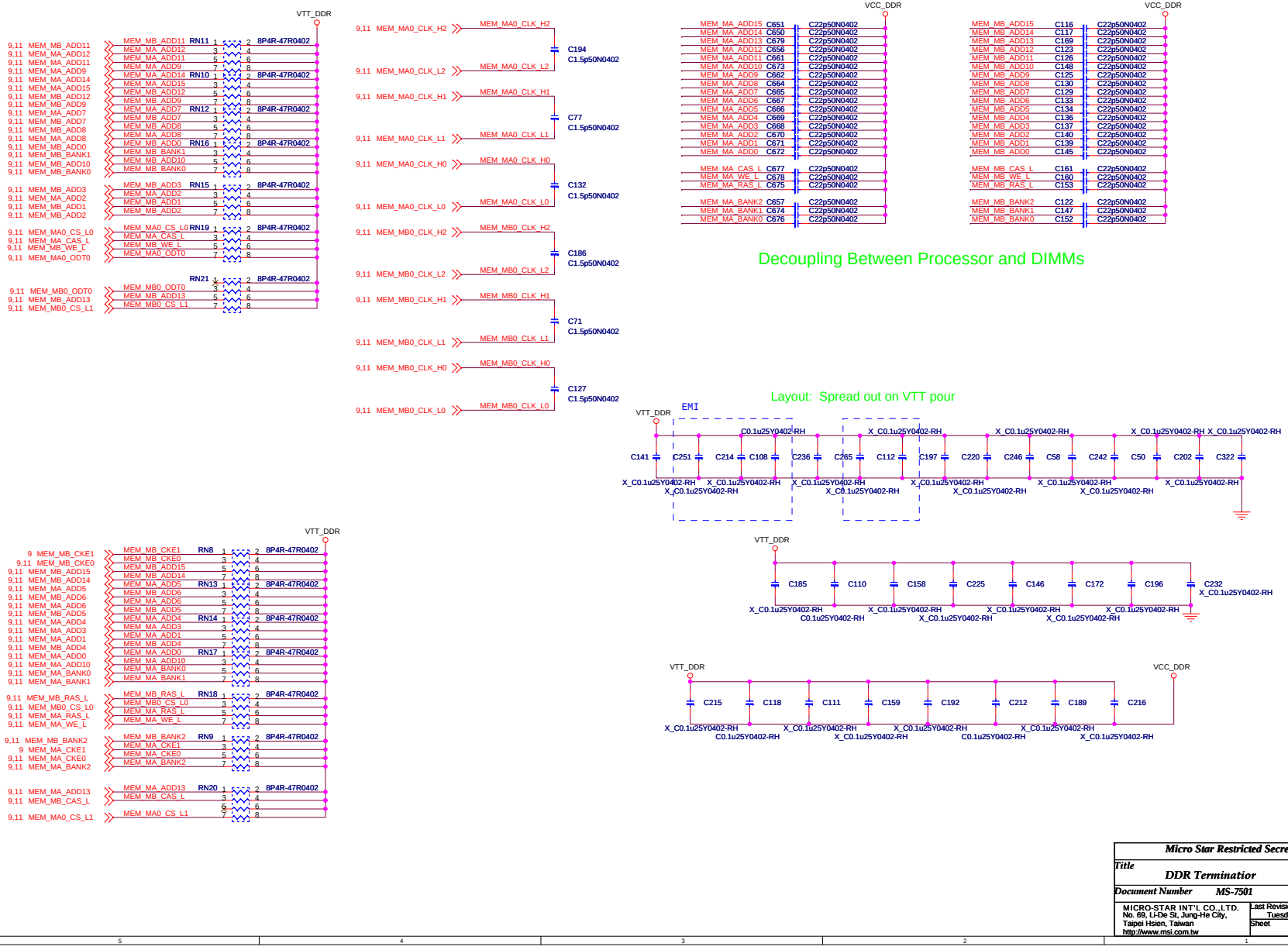

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Document Number	*MS-7501*	
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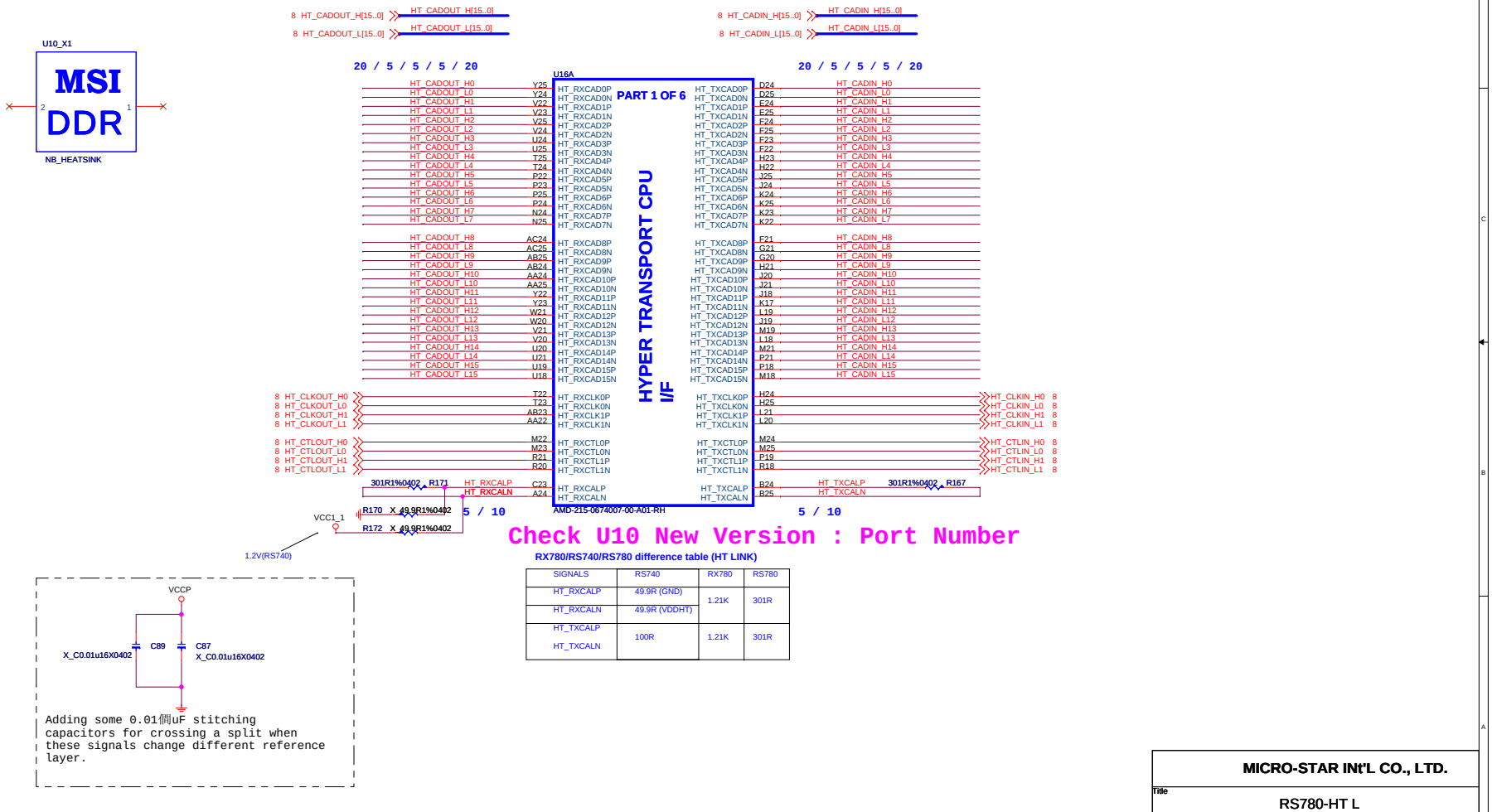

Check U10 New Version : Port Number

RX780/RS740/RS780 difference table (HT LINK)

SIGNALS	RS740	RX780	RS780
HT_RXCALP	49.9R (GND)	1.21K	301R
HT_RXCALN	49.9R (VDDHT)		
HT_TXCALP HT_TXCALN	100R	1.21K	301R

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Title: RS780-HT L		
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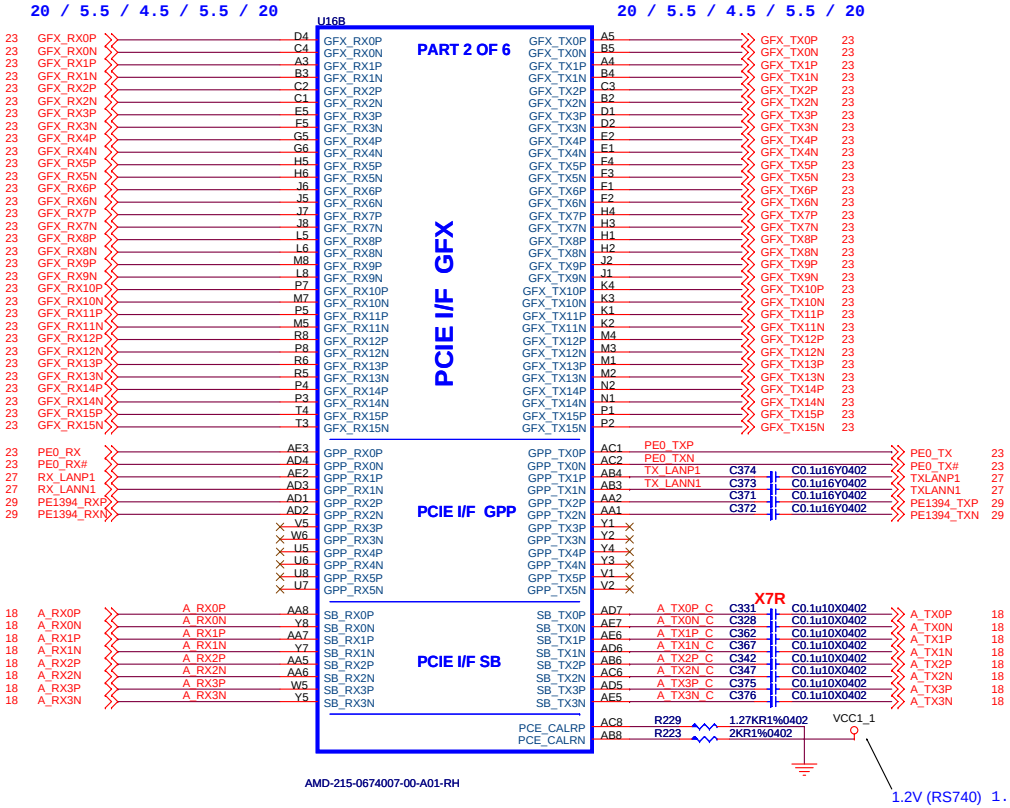

RX780/RS740/RS780 GPP difference table

	RS740	RX780/RS780
PCE_CALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

RX780/RS740/RS780 GPP Routing table

	RS740	RX780/RS780
GPP X4 CONNECTOR	GPP[2:0]	GPP[3:0]
GPP X1 CONNECTOR		GPP4
GIGABIT ETHERNET	GPP3	GPP5

RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

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Title	RS780-PCIE I/F	
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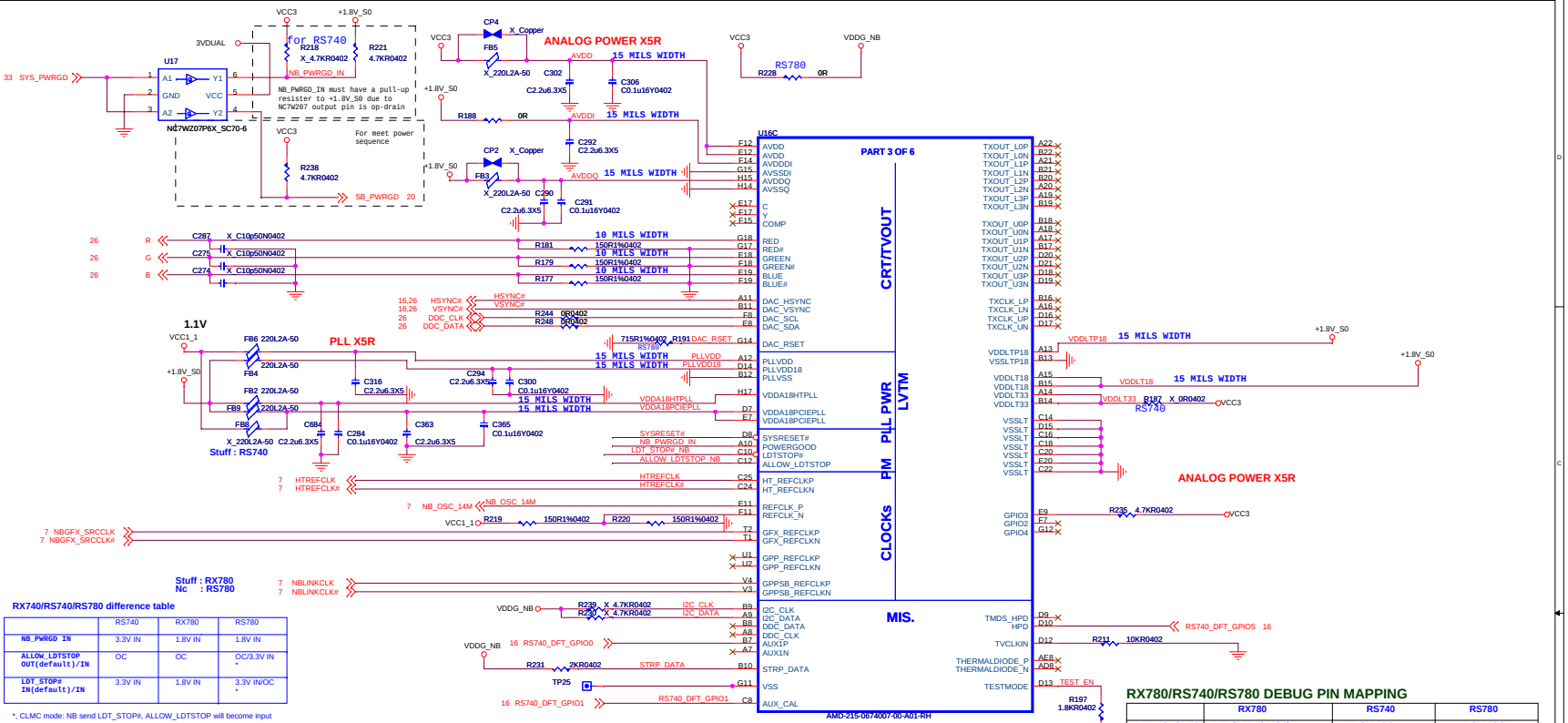


RX740/RS740/RS780 difference table

	RS740	RX780	RS780
NB_PWRGD_IN	3.3V IN	1.8V IN	1.8V IN
ALLOW_LDTSTOP OUT(default)/IN	OC	OC	OC/3.3V IN *
LDT_STOP# IN(default)/IN	3.3V IN	1.8V IN	3.3V IN/OC *

*, CLMC mode: NB send LDT_STOP#, ALLOW_LDTSTOP will become input

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* RS780 can be used as clock buffer to output two PCIE refereceence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.

RS740/RS780/RS780: STRAP_DEBUG_BUS_GPIO_ENABLE

Enables the Test Debug Bus using GPIO and/or memory IO
1 : Disable (RS740); Enable (RX780/RS780)
0 : Enable (RS740); Disable(RX780/RS780)

RX780: pin DFT_GPIO5
RS780: pin VSYNC

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.
111: register defined (register default to Config E) default
110: 4-0-0-0-0 Config A
101: 4-4-0-0-0 Config B
100: 4-2-2-0-0 Config C
011: 4-2-1-1-0 Config D
010: 4-1-1-1-1 Config E
others: register defined (default to Config E)

RS740/RS780/RS780: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RX780: pin DFT_GPIO1
RS780: pin SUS_STAT#

RS740/RX780/RS780: SIDE-PORT MEMORY ENABLE

Enables Side port memory
1. Disable (RS740/RS780)
0 : Enable (RS740/RS780)
RS780: pin HSYNC
RX780: Not Appicable

RX780/RS740/RS780 DEBUG PIN MAPPING

	RX780	RS740	RS780
DEBUG_OUT0	RED(DFT_GPIO0)	LVDS_DIGON	LVDS_DIGON
DEBUG_OUT1	GREEN(DFT_GPIO1)	LVDS_ENA_BL	LVDS_ENA_BL
DEBUG_OUT2	Y(DFT_GPIO2)	LVDS_BLON	LVDS_BLON
DEBUG_OUT3	BLUE(DFT_GPIO3)	TMDS_HPD	TMDS_HPD
DEBUG_OUT4	TXOUT_L2N(DBG_GPIO0)	X	AUX1N
DEBUG_OUT5	TXCLK_LP(DBG_GPIO1)	X	AUX1P
DEBUG_OUT6	TXOUT_L3N(DBG_GPIO2)	X	HPD
DEBUG_OUT7	TXCLK_LN(DBG_GPIO3)	X	AUX_CAL

RX740/RS740/RS780 JTAG PIN MAPPING

	RX780	RS740/RS780
TRST	TEST_EN	TEST_EN
TMS(TP220)	PCIE_RST3(TP222)	DDC_DATA(TP223)
TDI	I2C_DATA	I2C_DATA
TCK	I2C_CLK	I2C_CLK
TDO(TP218)	PWM_GPIO6(TP219)	TMDS_HPD(TP221)

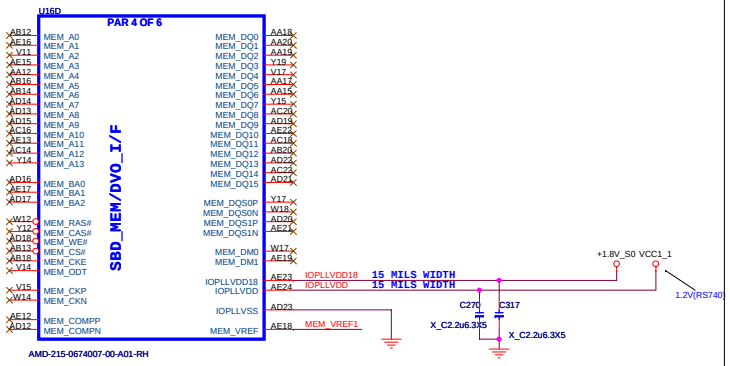
JTAG interface	RS780 Ball Name	Ball #
TEST_EN	TESTMODE	D13
TCK	I2C_CLK	B9
TDI	I2C_DATA	A9
TDO	TMDS_HPD	D9
TMS	DDC_DATA0/AUX0N	B8

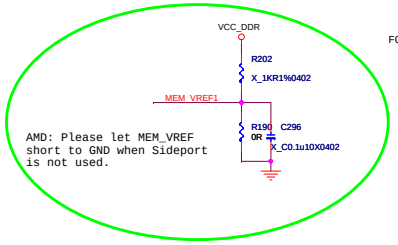
MICRO-STAR INt'L CO., LTD.

Title: RS780-SYSTEM I/F

Size: | Document Number: MS-7501 | Rev: 0A

Date: Wednesday, November 07, 2007 | Sheet 15 of 38





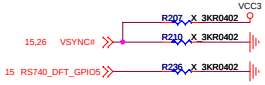
FOR RS780,R148,R162,C203 and C202 will be populated.

Note: If the Side-port memory interface is **not** used, make sure that:

- The memory interface IO power (VDD_MEM) is connected to 1.5 V for DDR3 or 1.8 V for DDR2.
- The memory interface IO transform power (VDD18_MEM) is connected to 1.8 V.
- The voltage divider for memory interface reference voltage MEM_VREF is connected to 1.5 V for DDR3 or 1.8 V for DDR2.
- The memory interface PLL power IOPLLVDD18 is connected to 1.8 V and IOPLLVDD is connected to 1.2 V for the RS740 and to 1.1 V for the RS780.
- The memory interface enable strap DFT_GPIO0 is **not** connected to the GND.

RS740/RX780/RS780 STRAPS

Note: for RS780, change R232 to 150R as AUX_CAL, place close to pin C8



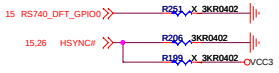
RS740/RX780/RS780: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RS740: pin DFT_GPIO1

RS780: pin SUS_STAT#
```

RS740/RX780/RS780: STRAP_DEBUG_BUS_GPIO_ENABLE

```
Enables the Test Debug Bus using GPIO and/or memory IO
1 : Disable (RS740/RS780); Enable (RX780)
0 : Enable  (RS740/RS780); Disable(RX780)
RS740: pin DFT_GPIO5

RS780: pin VSYNC
```

RS740/RX780/RS780: SIDE-PORT MEMORY ENABLE




```
Enables Side port memory
1.  Disable (RS740/RS780)
0 : Enable (RS740/RS780)
RS740:  pin DFT_GPIO0
RS780:  pin HSYNC
```

RX780/RS780: STRAP_DEBUG_BUS_PCIE_ENABLE

```
Enables Test debug bus
using PCIE bus
1.  Disable (can be enabled
      thru nbcfg register)
0 : Enable

RS780: configurable thru register
          setting only
RS740: Not supported
```

MICRO-STAR INt'L CO., LTD.		
Title: RS780-SPMEM/STRAPS		
Size	Document Number: MS-7501	Rev: 0A
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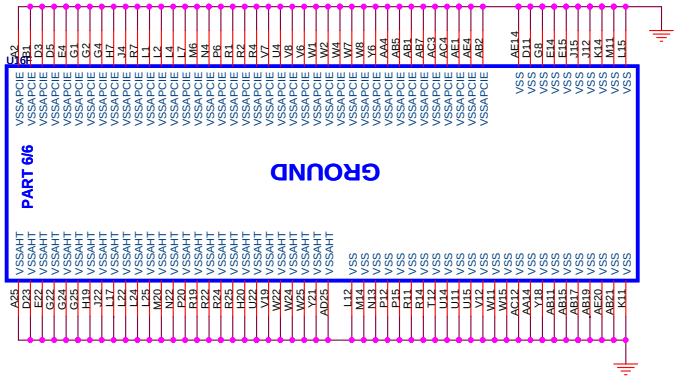
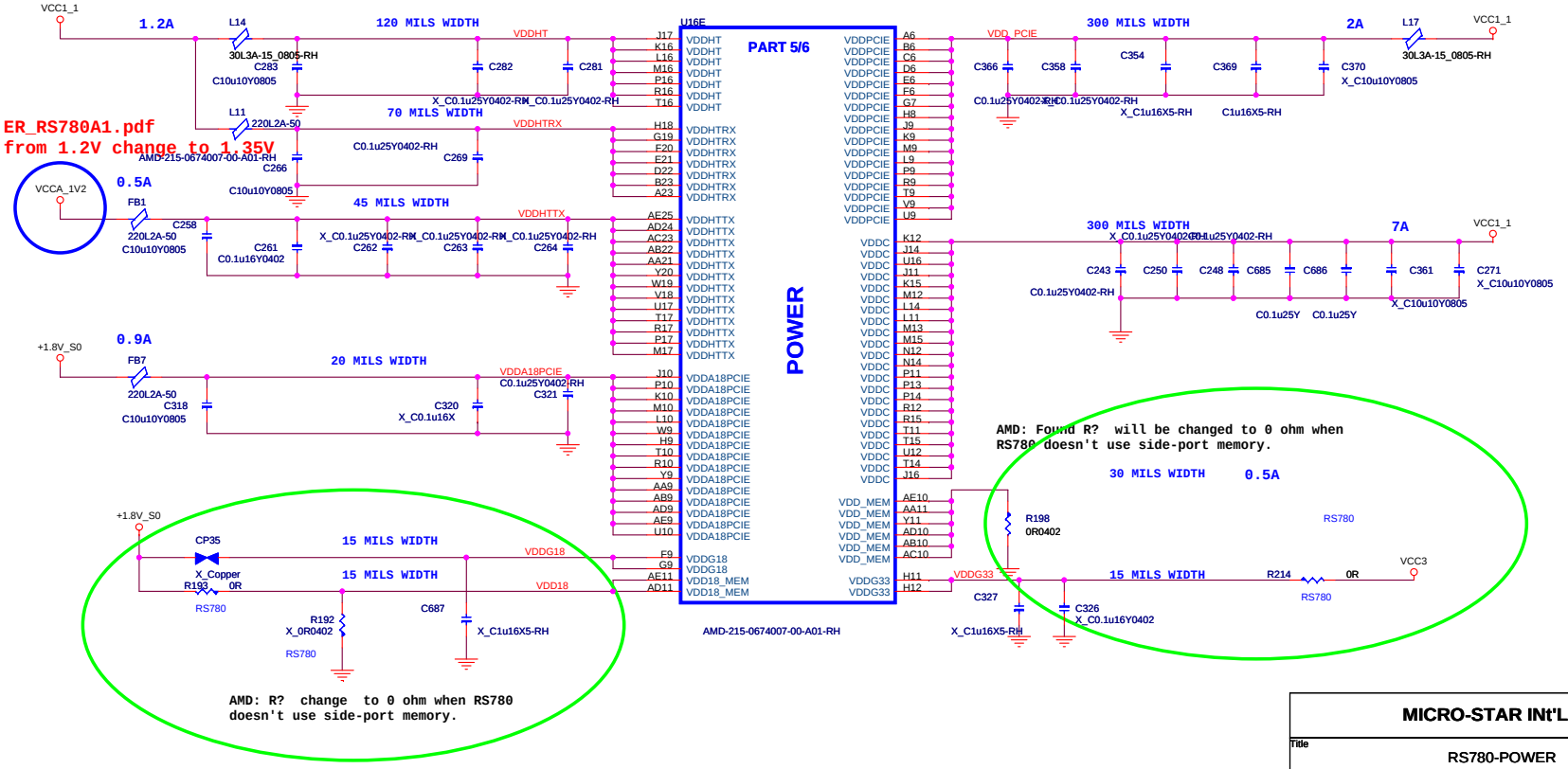


RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVDD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVDD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVDD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V/1.5V	NC	+1.8V/1.5V	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLT18	+1.8V	NC	+1.8V
IOPLLVDD18	+1.8V	NC	+1.8V	VDDLT33	+3.3V	NC	NC



MICRO-STAR INt'L CO., LTD.	
Title	RS780-POWER
Size / Document Number	MS-7501
Rev	0A
Date: Tuesday, November 06, 2007	Sheet 17 of 38

SIO PCICLK has beaneged
PCICLK5 to PCICLK4 for AMD
recommand

For EMI

10 pf For SA

Adding some 0.1個uF stitching capacitors for crossing a split when these signals change different reference layer.

SB HEAT-SINK

MSI DDR

SB700 Part 1 of 5

PLACE PCIE CAPS CLOSE TO U13

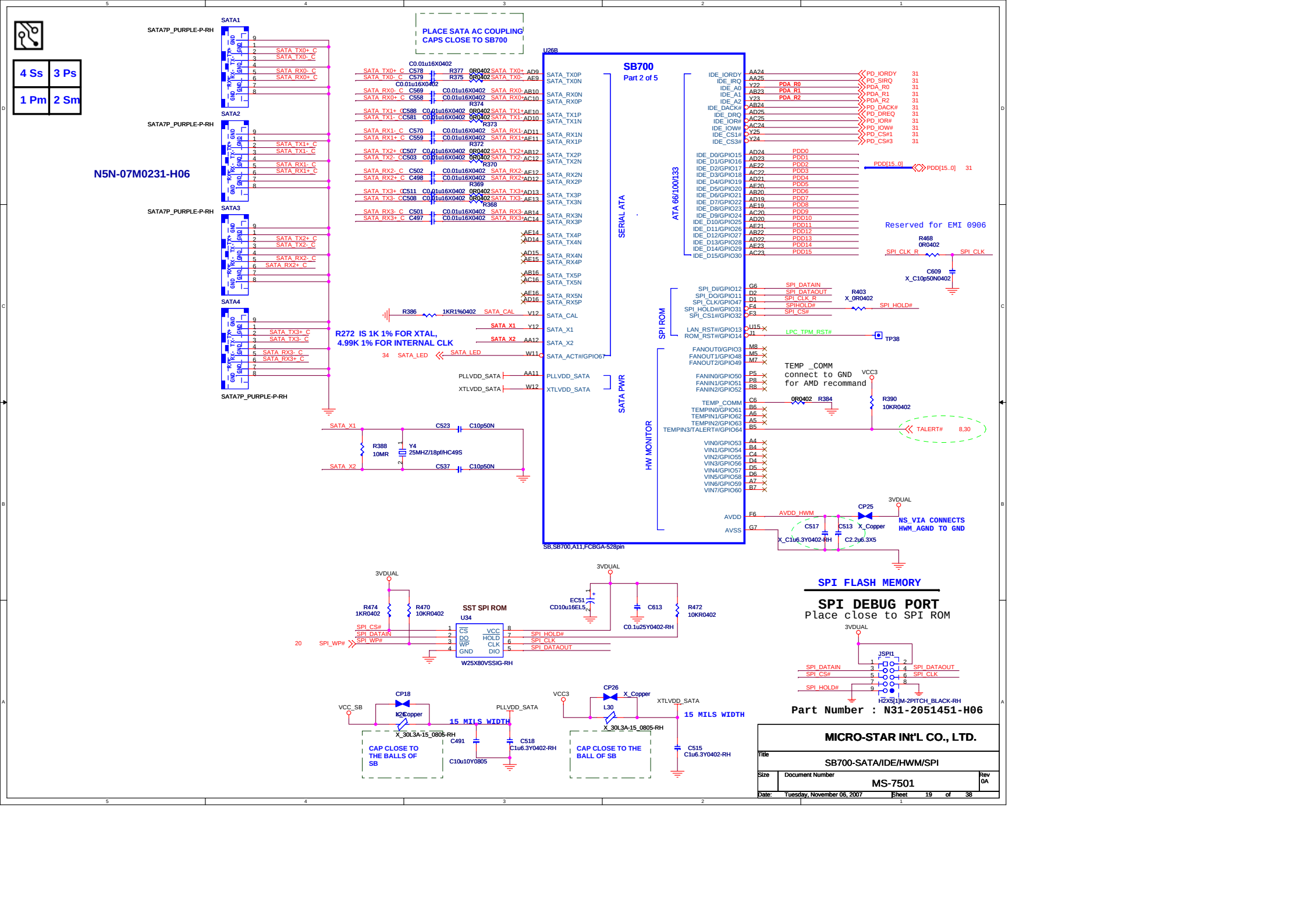
PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR 32K_X1 AND 32K_X2

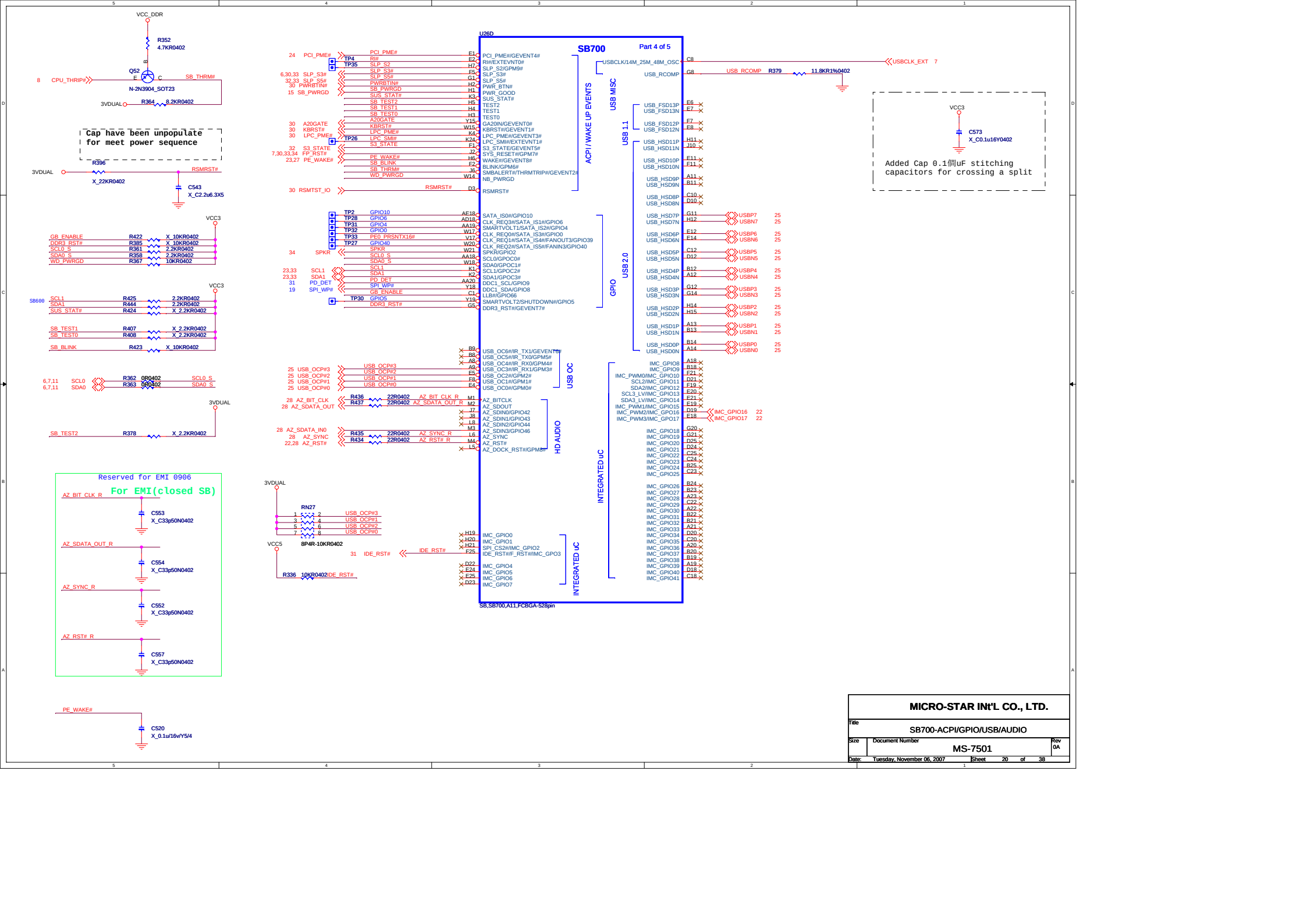
Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.

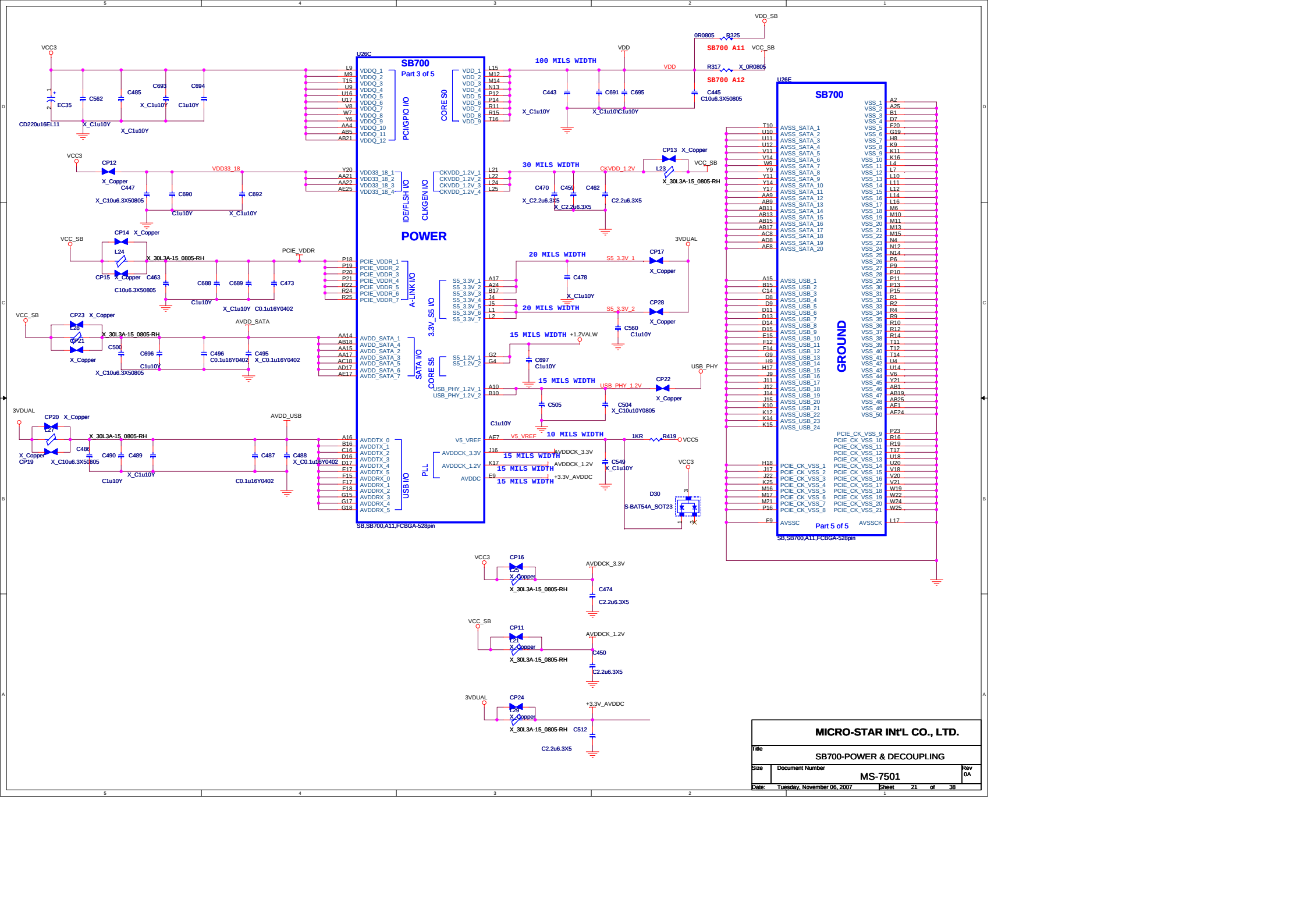
Check U13 New Version : Port Number

Title	SB700-PCIE/PCI/CPU/LPC
Size	Document Number: MS-7501
Rev	0A
Date:	Tuesday, November 06, 2007
Sheet	18 of 38

MICRO-STAR INT'L CO., LTD.

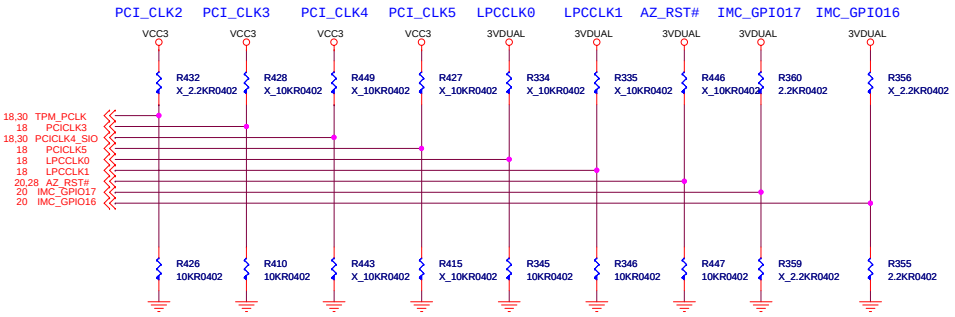

4 Ss
3 Ps
1 Pm
2 Sm
N5N-07M0231-H06
SATA1
SATA2
SATA3
SATA4
SATA7P_PURPLE-P-RH
PLACE SATA AC COUPLING CAPS CLOSE TO SB700
SB700
Part 2 of 5
U26B
SERIAL ATA
ATA 66/100/133
SPI ROM
HW MONITOR
SATA PWR
R272 IS 1K 1% FOR XTAL, 4.99K 1% FOR INTERNAL CLK
Reserved for EMI 0906
TEMP _COMM connect to GND for AMD recommand
SB,SB700,A11,FCBGA-528pin
SPI FLASH MEMORY
SPI DEBUG PORT
Place close to SPI ROM
SST SPI ROM
W25X80VSSIG-RH
CAP CLOSE TO THE BALLS OF SB
15 MILS WIDTH
Part Number : N31-2051451-H06
MICRO-STAR INt'L CO., LTD.
SB700-SATA/IDE/HWM/SPI
MS-7501
Tuesday, November 06, 2007
Sheet 19 of 38


SB700
Part 4 of 5
U26D
SB,SB700,A11,FCBGA-528pin
ACPI / WAKE UP EVENTS
USB MISC
USB 1.1
USB 2.0
GPIO
USB OC
HD AUDIO
INTEGRATED uC
Cap have been unpopulate for meet power sequence
Added Cap 0.1倆uF stitching capacitors for crossing a split
Reserved for EMI 0906
For EMI(closed SB)
MICRO-STAR INt'L CO., LTD.
Title
SB700-ACPI/GPIO/USB/AUDIO
Size
Document Number
MS-7501
Rev
0A
Date: Tuesday, November 06, 2007
Sheet 20 of 38


SB700
Part 3 of 5
POWER
GROUND
Part 5 of 5
SB,SB700,A11,FCBGA-528pin
100 MILS WIDTH
30 MILS WIDTH
20 MILS WIDTH
15 MILS WIDTH
10 MILS WIDTH
SB700 A11
SB700 A12
VDD_SB
VCC_SB
VCC3
3VDUAL
VDD
CKVDD_1.2V
AVDDCK_3.3V
AVDDCK_1.2V
+3.3V_AVDDC
+1.2VALW
USB_PHY_1.2V
PCIE_VDDR
AVDD_SATA
AVDD_USB
V5_VREF
VCC5
CORE S0
PCI/GPIO I/O
IDE/FLSH I/O
CLKGEN I/O
A-LINK I/O
3.3V_S5 I/O
CORE S5
SATA I/O
PLL
USB I/O
MICRO-STAR INT'L CO., LTD.
SB700-POWER & DECOUPLING
MS-7501
Tuesday, November 06, 2007
Sheet 21 of 38

REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	AZ_RST#	IMC_GPIO17 IMC_GPIO16
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	IMC ENABLED	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT L, H = LPC ROM L, L = FWH ROM
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	IMC DISABLED DEFAULT	

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[30:23]

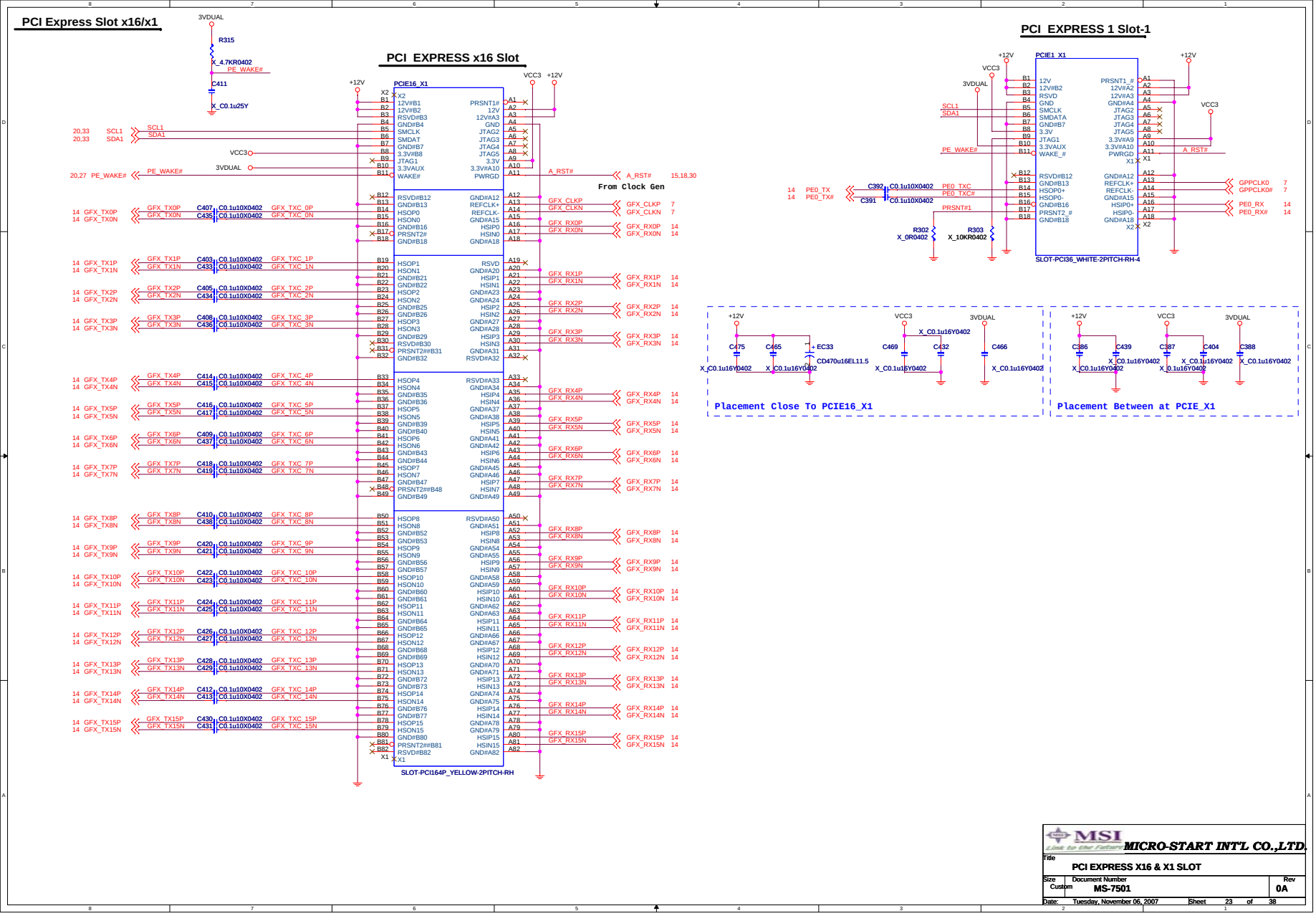
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

MICRO-STAR INt'L CO., LTD.

Title: SB700-STRAPS

Size | Document Number: MS-7501 | Rev: 0A

Date: Tuesday, November 06, 2007 | Sheet 22 of 38


PCI Express Slot x16/x1
PCI EXPRESS x16 Slot
PCI EXPRESS 1 Slot-1
PCIE16_X1
SLOT-PCI164P_YELLOW-2PITCH-RH
PCIE1_X1
SLOT-PCI36_WHITE-2PITCH-RH-4
From Clock Gen
Placement Close To PCIE16_X1
Placement Between at PCIE_X1
MSI
MICRO-START INT'L CO.,LTD.
PCI EXPRESS X16 & X1 SLOT
MS-7501
0A
Tuesday, November 06, 2007
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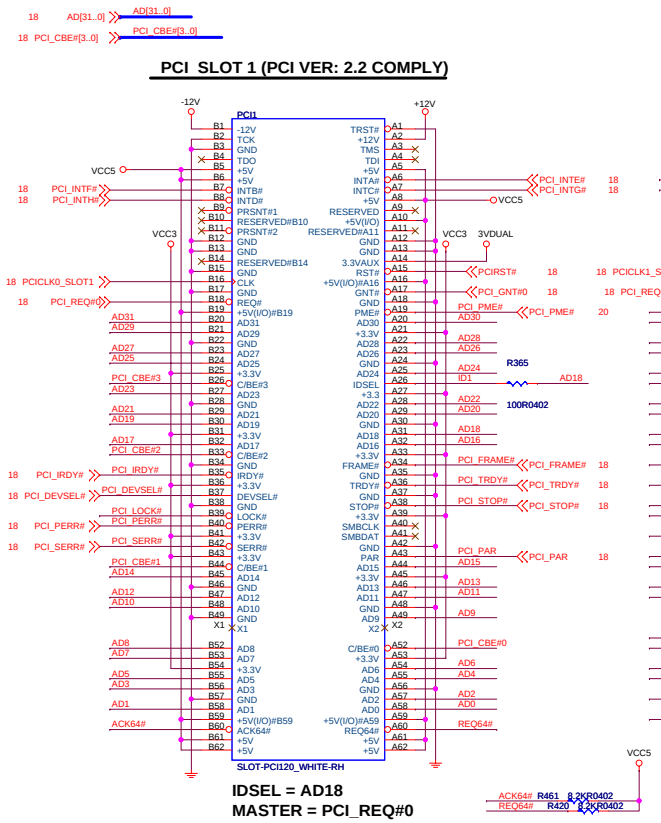
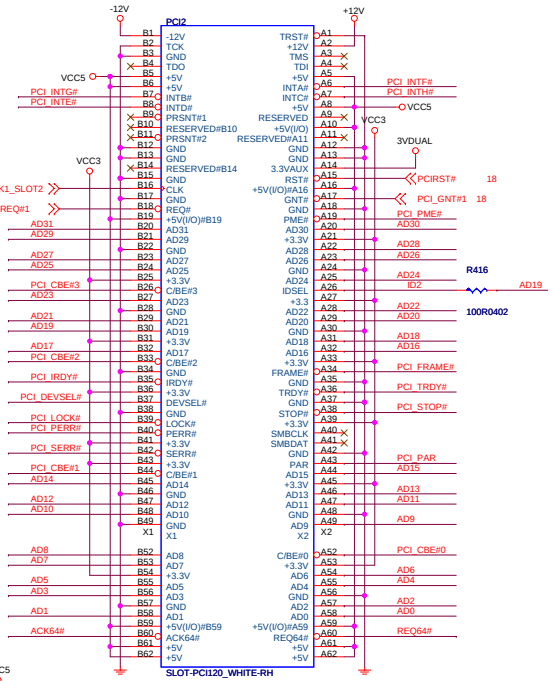
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



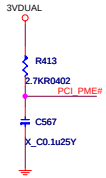
IDSEL = AD18
MASTER = PCI_REQ#0
PCI_GNT#0

ACK64# R461 8.2KR0402
REQ64# R420 8.2KR0402

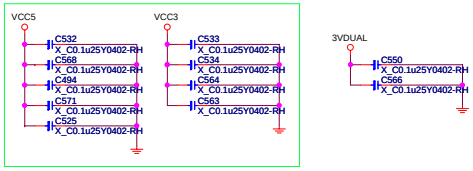
PCI SLOT 2 (PCI VER: 2.2 COMPLY)



IDSEL = AD19
MASTER = PCI_REQ#1
PCI_GNT#1

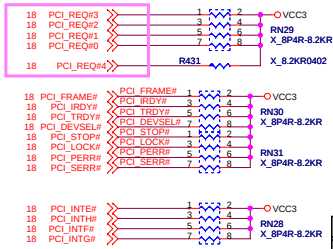


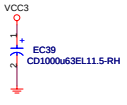
PCI SLOT DECOUPLING CAPACITORS



For EMI

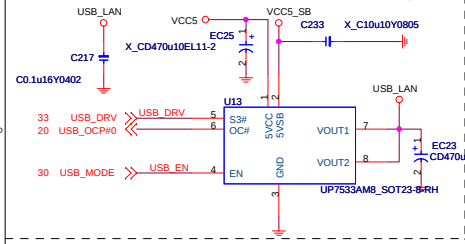
PCI PULL-UP / DOWN RESISTORS



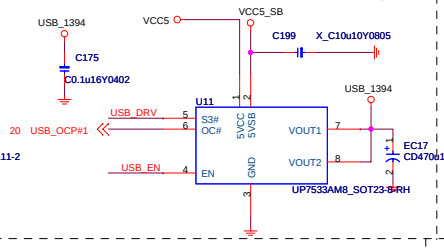


Micro Star Restricted Secret	
Title PCI Slot 1 2	Rev 0A
Document Number MS-7501	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, November 06, 2007 Sheet 24 of 38

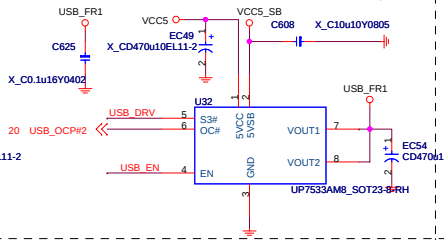
POWER CIRCUIT FOR USB PORT 4,5



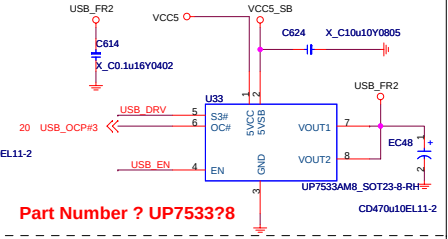
POWER CIRCUIT FOR USB PORT 2,3



POWER CIRCUIT FOR USB PORT 0,1



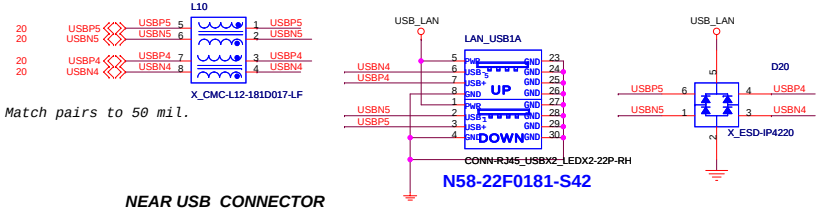
POWER CIRCUIT FOR USB PORT 6,7



Part Number ? UP7533?8

REAR PANEL USB CONNECTOR FOR USB PORT 4,5

Trace lengths must be less 12 inches



Match pairs to 50 mil.

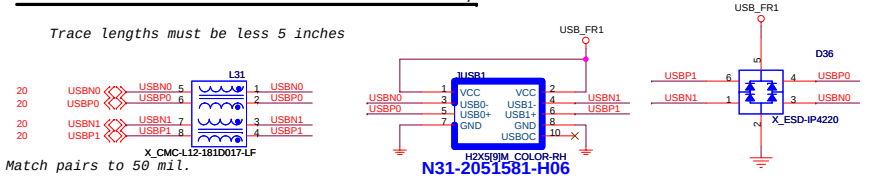
N58-22F0181-S42

NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

FRONT PANEL USB CONNECTOR FOR USB PORT 0,1

Trace lengths must be less 5 inches



Match pairs to 50 mil.

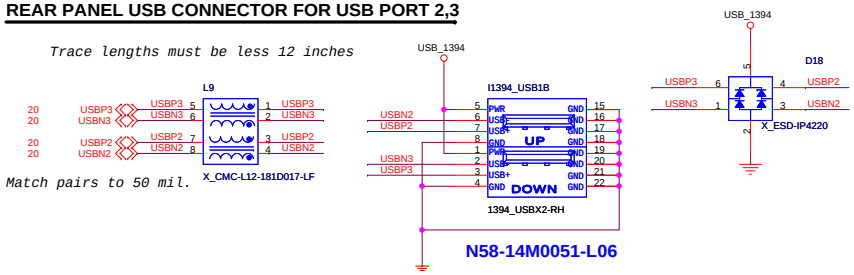
N31-2051581-H06

NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

REAR PANEL USB CONNECTOR FOR USB PORT 2,3

Trace lengths must be less 12 inches



Match pairs to 50 mil.

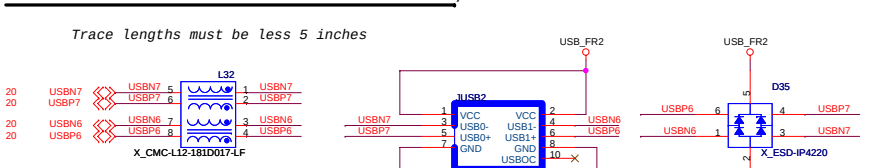
N58-14M0051-L06

NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

Trace lengths must be less 5 inches



Match pairs to 50 mil.

N31-2051581-H06

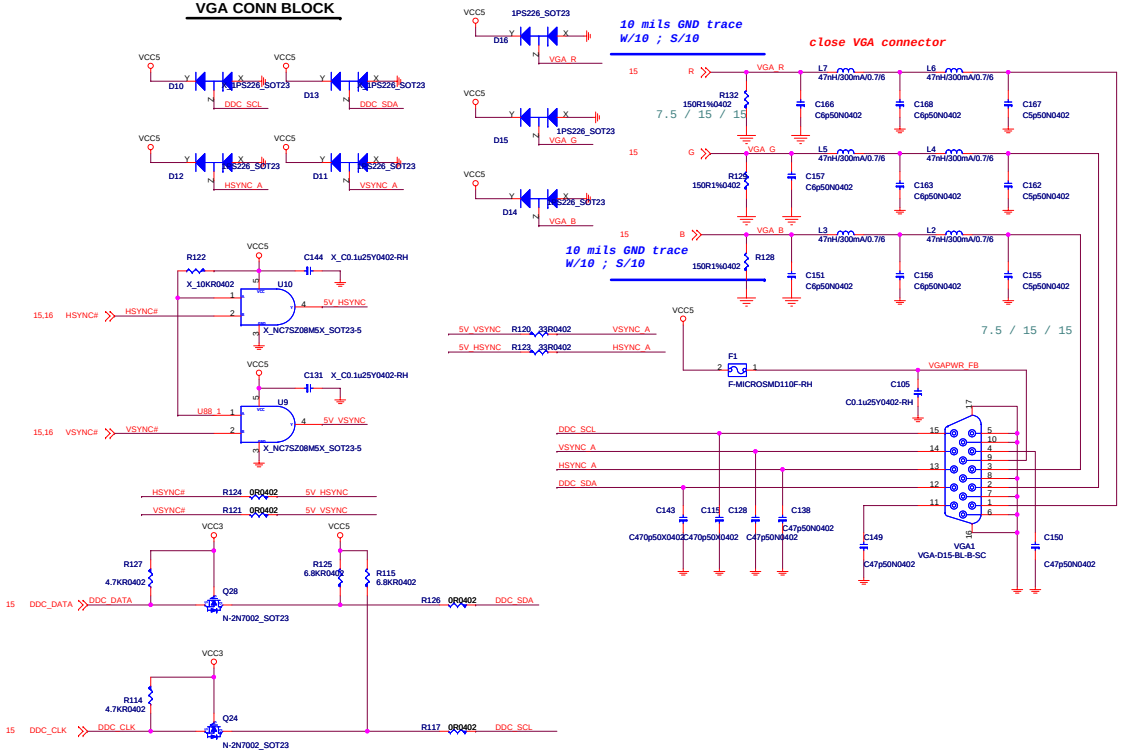
NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

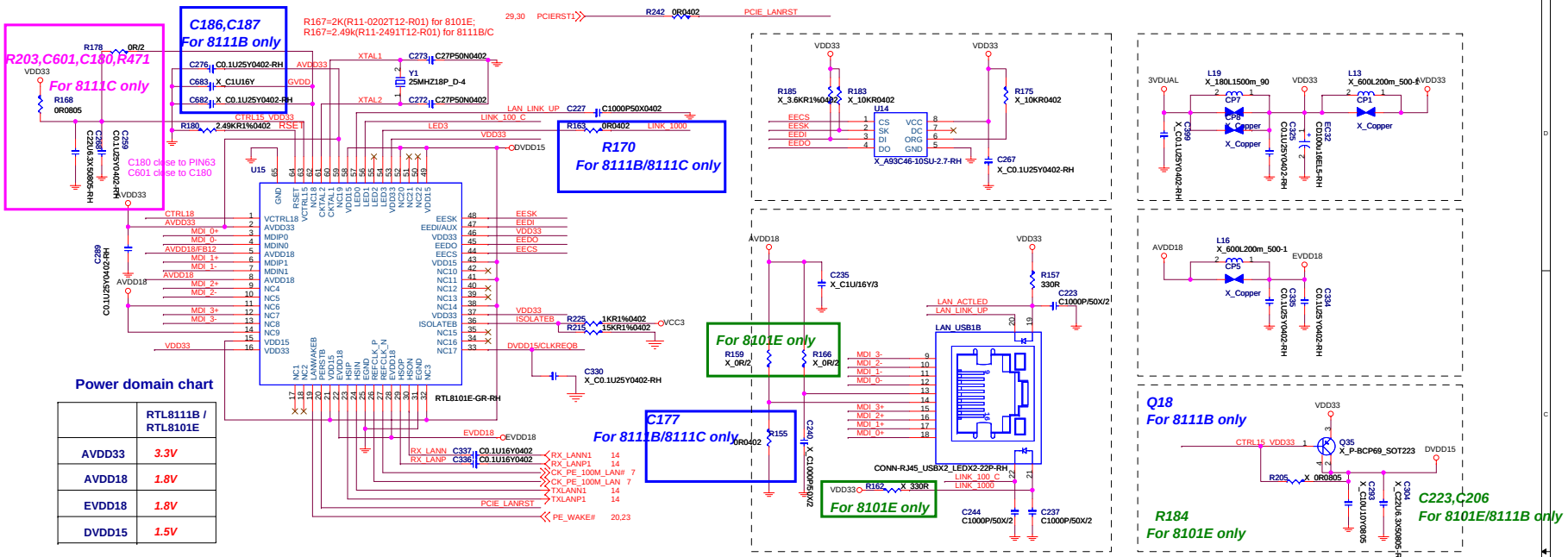
MICRO-STAR INt'L CO., LTD.

Title	USB Conn.	
Size	Document Number MS-7501	Rev 0A
Date: Tuesday, November 06, 2007	Sheet 25 of 38	

VGA CONN BLOCK



MICRO-STAR INt'L CO., LTD.		
Title: VGA CONN / TVOUT		
Size	Document Number: MS-7501	Rev: 0A
Date: Tuesday, November 06, 2007	Sheet 26 of 38	



	Q18	Q20	R169	R184	R167	R170	R160	R205	R164	R188	R186	R177	R175	R470	R472	L22	R471	C601	C186	C187
RTL8101E	N/A	N/A	Need	Need	2K	N/A	Need	Need	Need	Need	Need	Need	Need	Need	N/A	N/A	N/A	N/A	N/A	N/A
RTL8111B	Need	Need	N/A	N/A	2.49K	Need	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Need	N/A	N/A	N/A	N/A	Need	Need
RTL8111B	Need	Need	N/A	N/A	2.49K	Need	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Need	Need	Need	Need	N/A	N/A

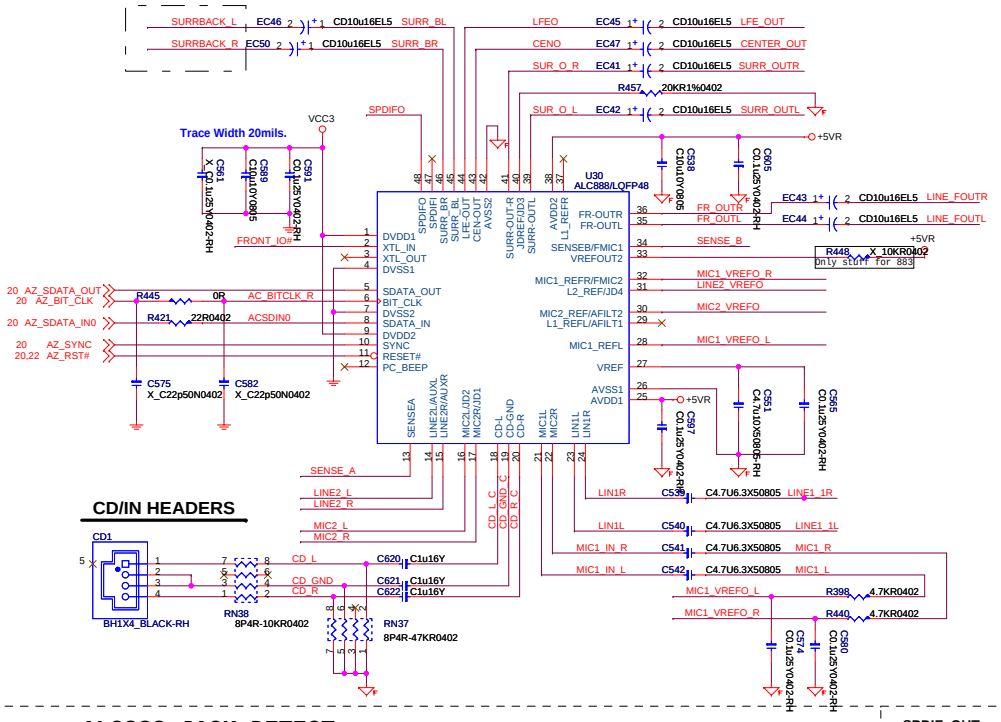
	8101E	8111B	8111C
VDD33	16,37,46,53	16,37,46,53	VDD33 16,37,46,53
AVDD33	2	2,59	AVDD33 2,59
AVDD18	5,8	5,8,11,14	AVDD12 8,11,14,58
EVDD18	22,28	22,28	EVDD12 22,28
VDD15	15,21,43,49,58	15,21,32,33,38,41,43,49,52,58	DVDD12 21,32,38,43,49,52
GND	65	65	GND 65
AGND	25,31	25,31	AGND 25,31

Giga-Lan	10/100-Lan
N58-22F0181-S42	N58-22F0201-S42
Link Active 1000 100 10 / Blinking Orange Green None	Link Active 100 10 / Blinking Green None
19 Yellow 20	19 Yellow 20
21 Orange 22 Green	21 Green 22

Micro Star Restricted Secret		
Title	RTL8101E/8111B/8111C	Rev 3.0
Document Number	MS-7379	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, November 06, 2007	Sheet 27 of 38

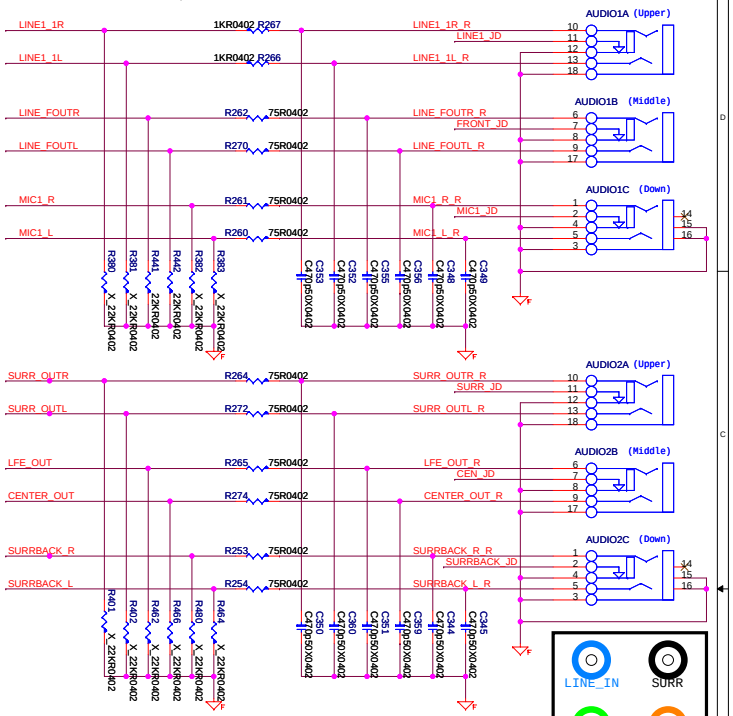
ALC888 CODEC

883 :B09-LC88304-R09
888: B09-LC88804-R09
861D:B09-LC86124-R09



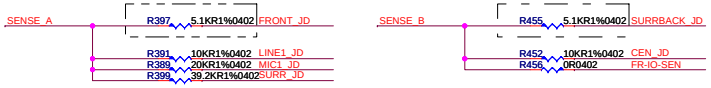
CD/IN HEADERS

ALC888 JACK

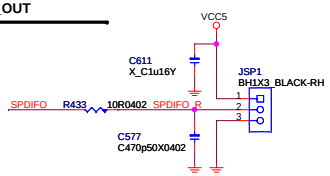


PN:N54-26F0151-S42

ALC883 JACK DETECT

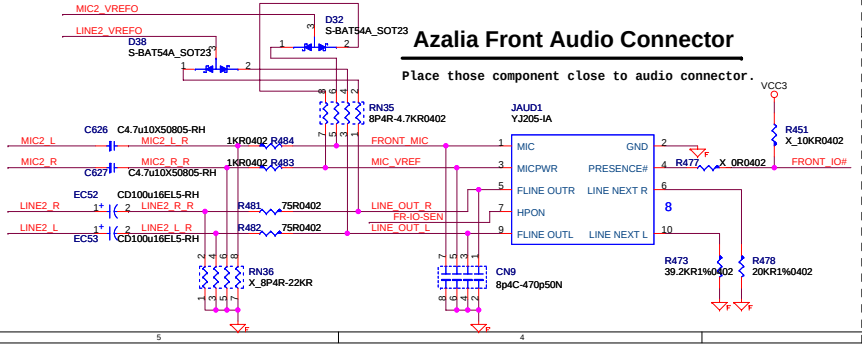


SPDIF_OUT

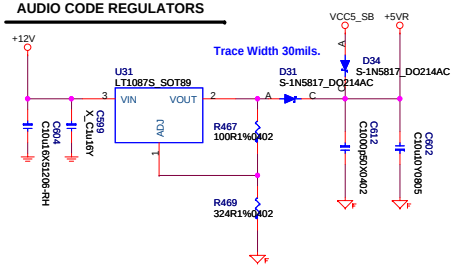


Azalia Front Audio Connector

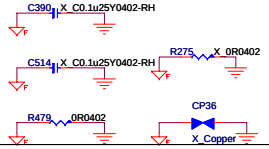
Place those component close to audio connector.



AUDIO CODE REGULATORS

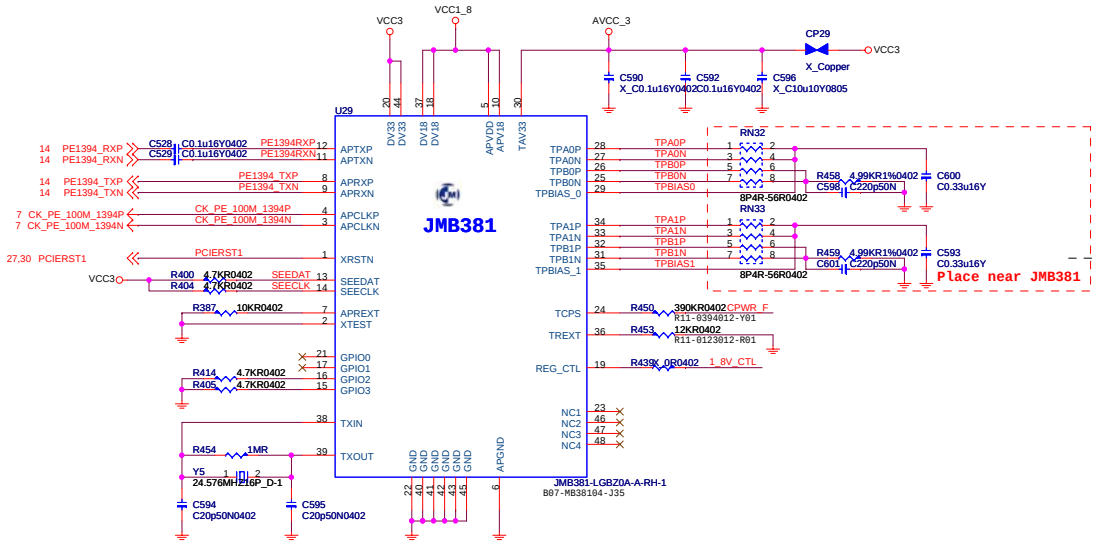


For EMI



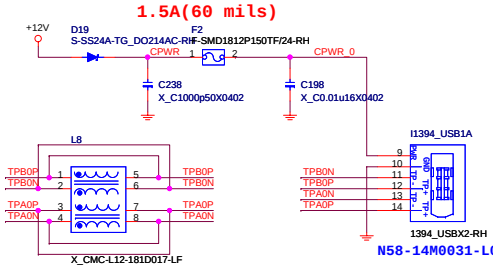
<OrgAddr1>	MICRO-STAR INt'L CO., LTD.	
Title	ALC888 CO-LAY ALC883 CODEC	
Size	Document Number: MS-7379	Rev: 3.0
Date: Tuesday, November 06, 2007	Sheet 28 of 38	

JMICRON JMB381



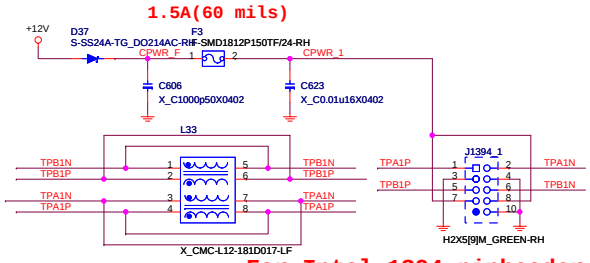
Rear 1394 port

1.5A(60 mils)

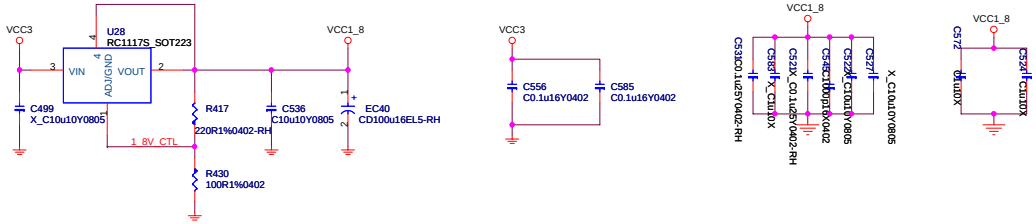


Front 1394 pin header

1.5A(60 mils)



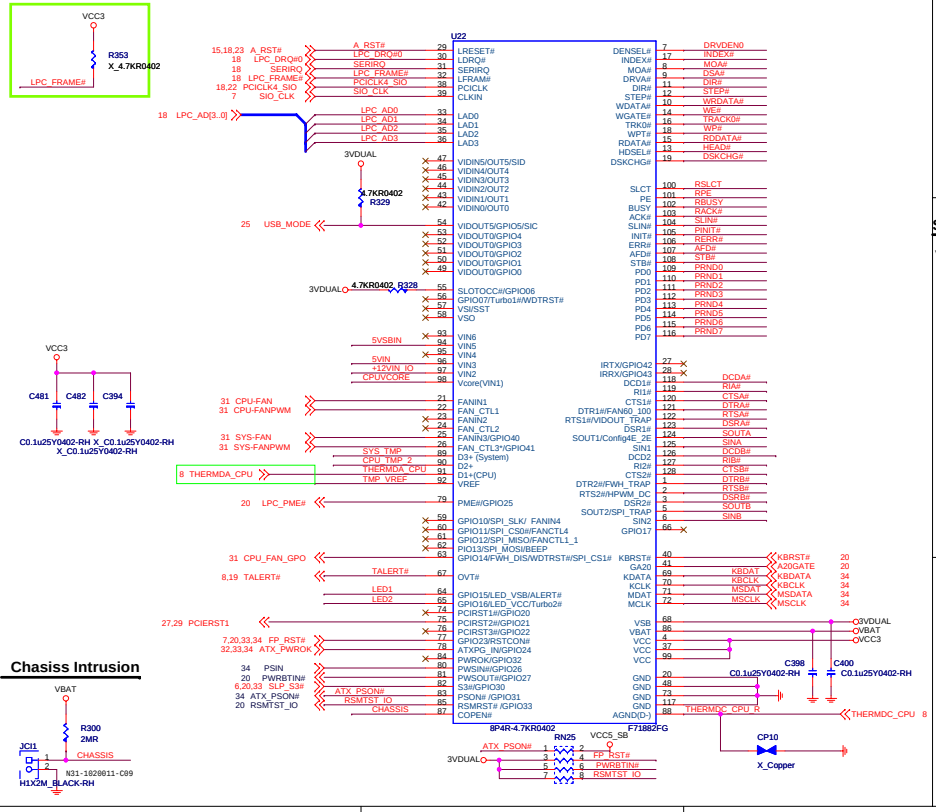
For Intel 1394 pinheader



Title	<Title>		
Size	Document Number <Doc>		Rev <RevCode>
Date: Tuesday, November 06, 2007	Sheet 29 of 38		

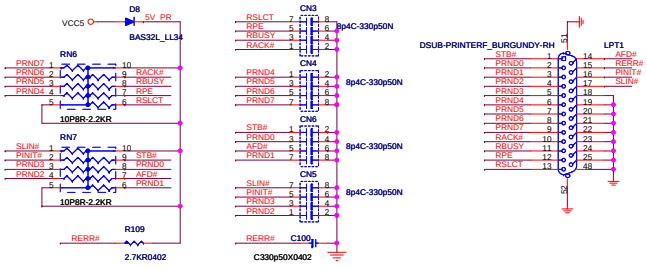
Super I/O

LPC SUPER I/O F71882

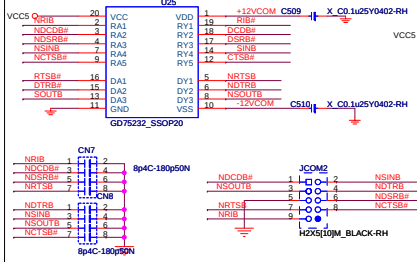


Chassis Intrusion

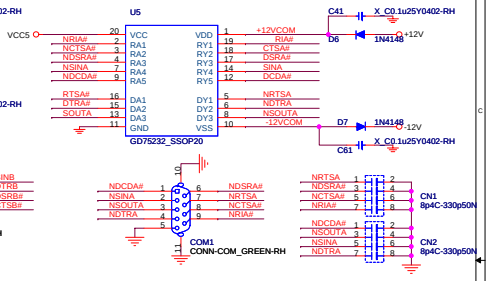
PARALLAL PORT



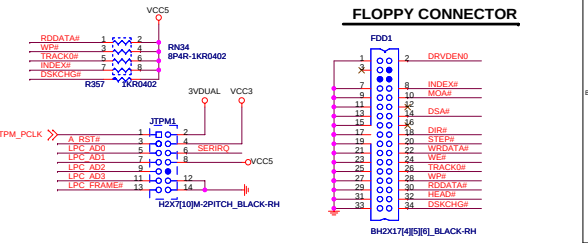
SERIAL PORT 2



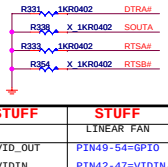
SERIAL PORT 1



FLOPPY CONNECTOR

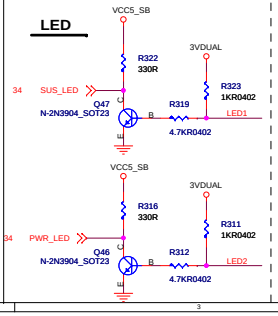


LPC I/O STRAPPING RESISTOR

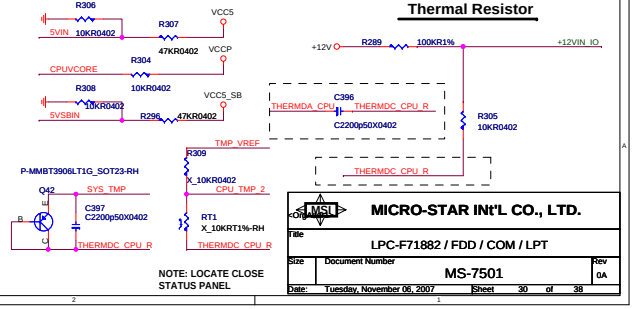


	Don't STUFF	STUFF
RTSB#	PWM FAN	LINEAR FAN
RTSA#	PIN49-54=VID_OUT PIN42-47=VIDIN	PIN49-54=GPIO PIN42-47=VIDIN/OUT
SOUTA	4E	2E
DTRA#	FAN START DUTY 60%	FAN START DUTY 100%

LED



Thermal Resistor



NOTE: LOCATE CLOSE STATUS PANEL

MICRO-STAR INt'L CO., LTD.

Title: LPC-F71882 / FDD / COM / LPT

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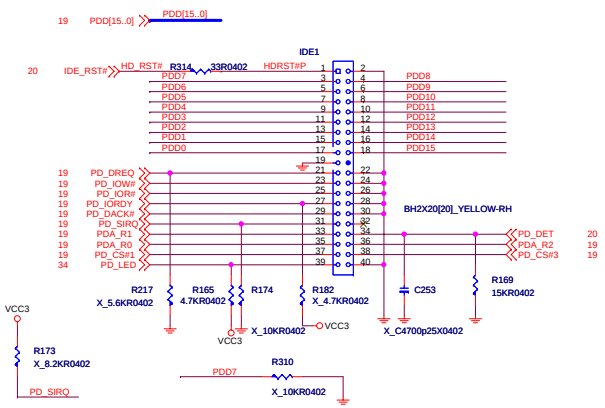
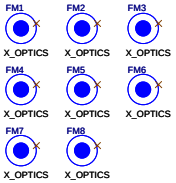
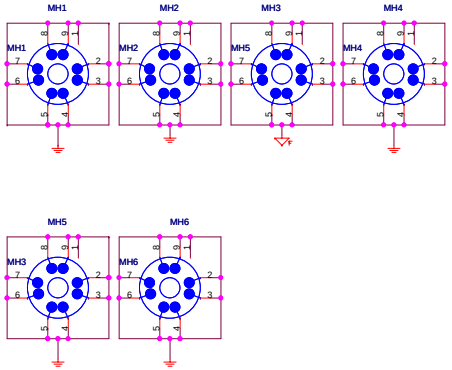
IDE 1



Optics Orientation Holes



Mounting Holes

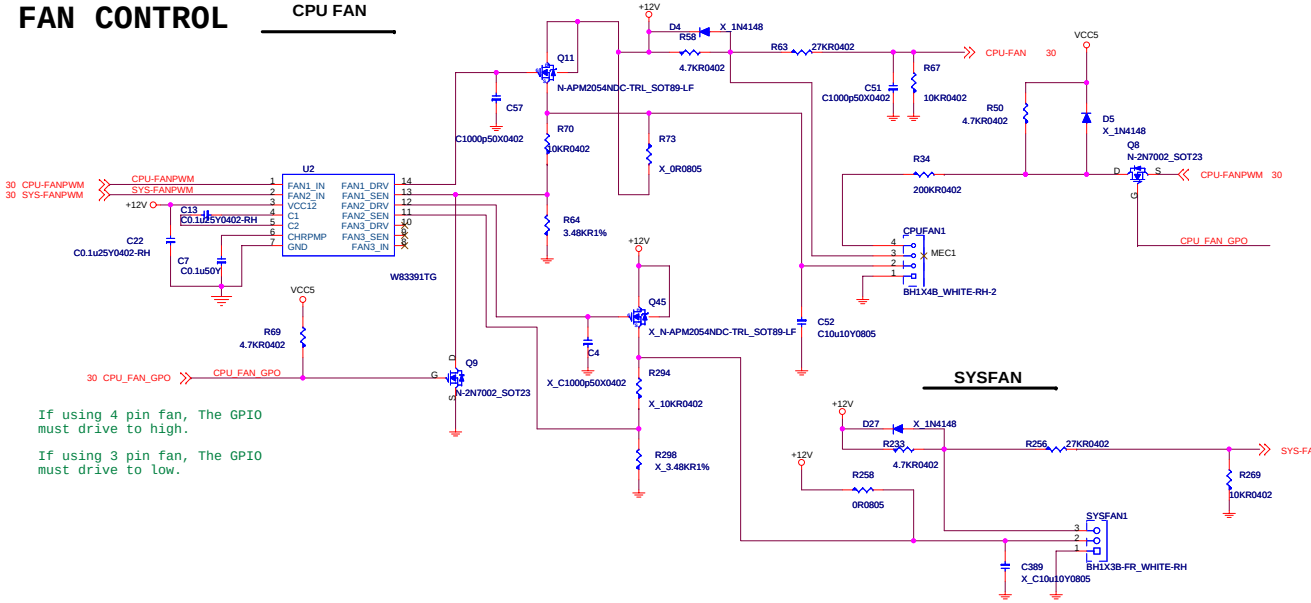


Simulation

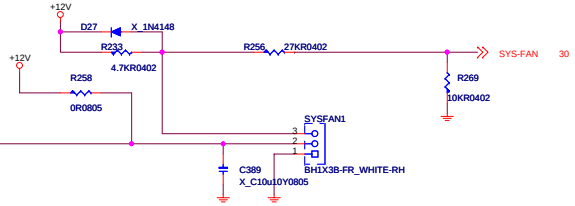
FAN CONTROL

CPU FAN

If using 3 pin fan, The Q40 will turn off to avoid the VCC5(R527) bias to CPU-FANPWM.



SYSFAN



If using 4 pin fan, The GPIO must drive to high.

If using 3 pin fan, The GPIO must drive to low.

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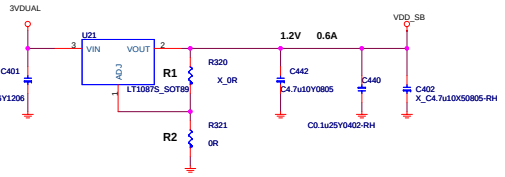
Page 21 : FB10 , FB11

1.25V reference voltage

Vo = Vref (1+R2/R1) + Iadj x R2

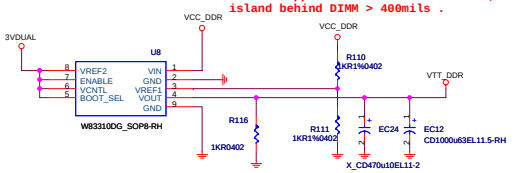


PA_SB700AA1

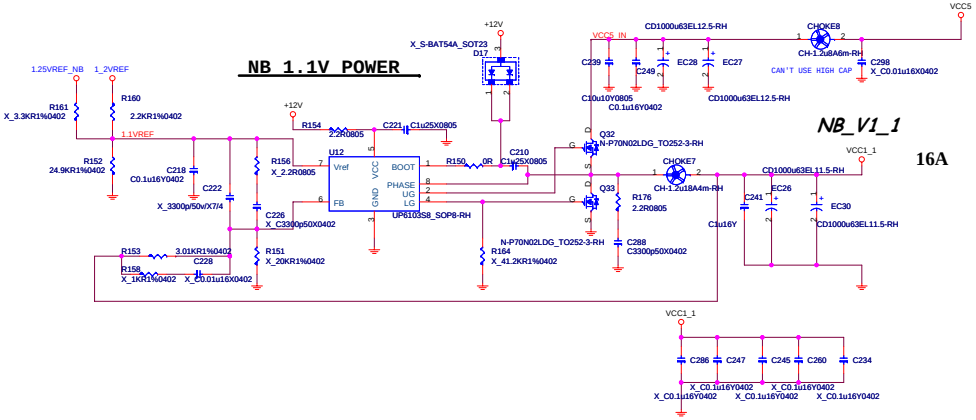
R539 has been un-populated and R541 has been populated for U32 heat.

DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



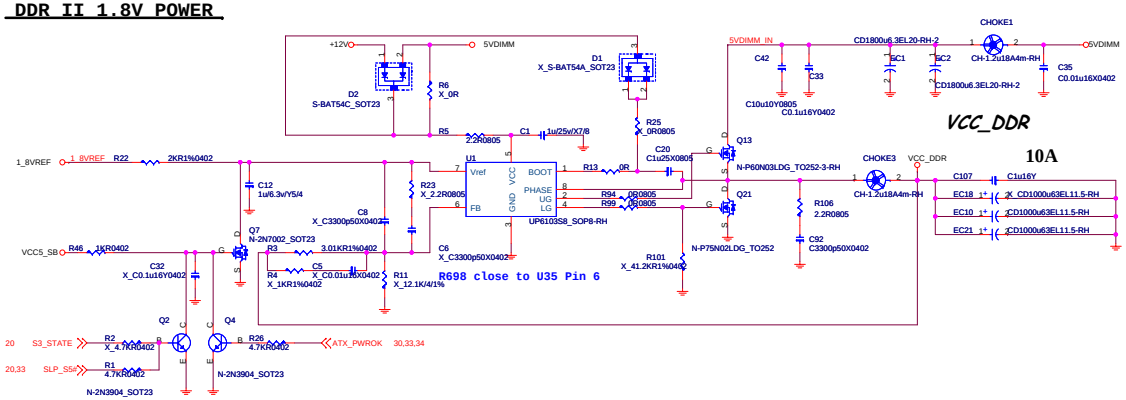
NB 1.1V POWER



NB_V1_1

16A

DDR II 1.8V POWER



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Document Number: MS-7501		
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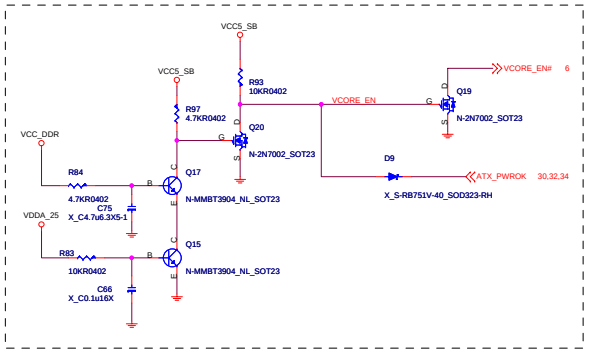
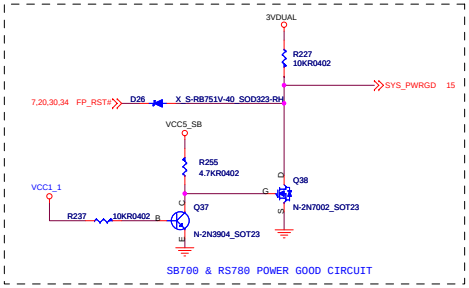
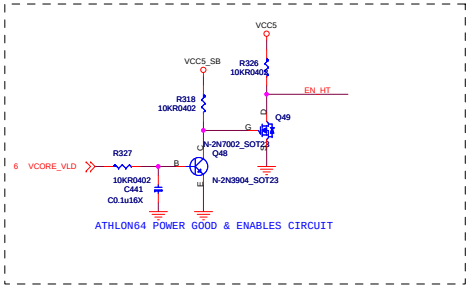
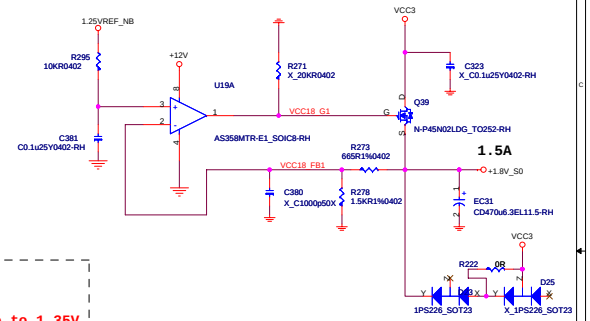
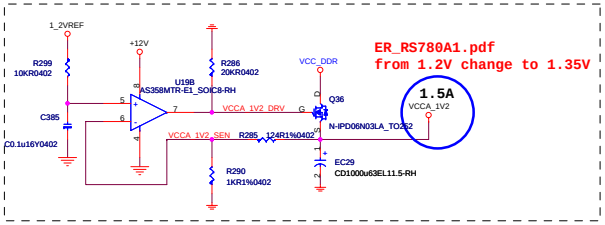
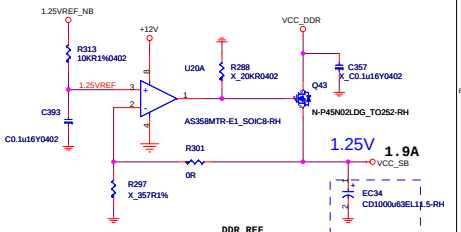


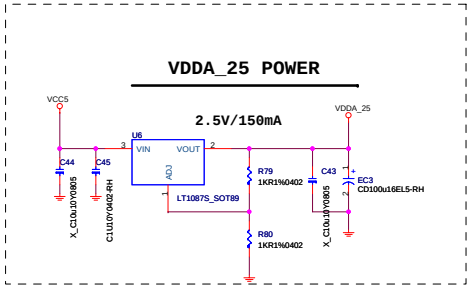


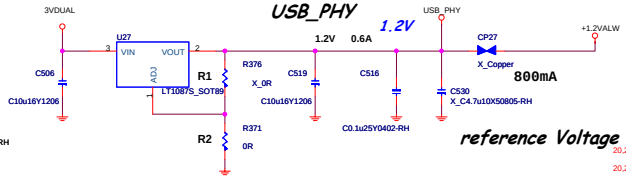


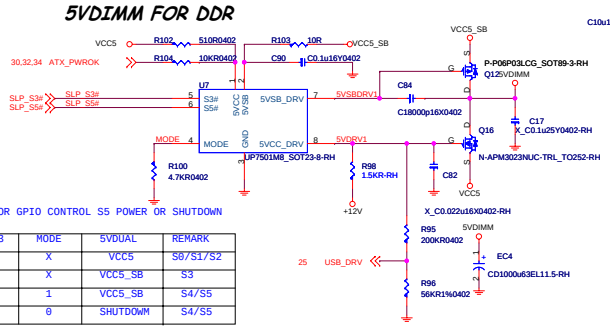


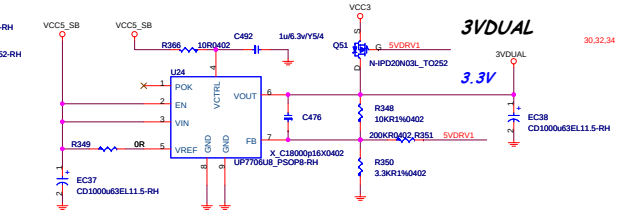




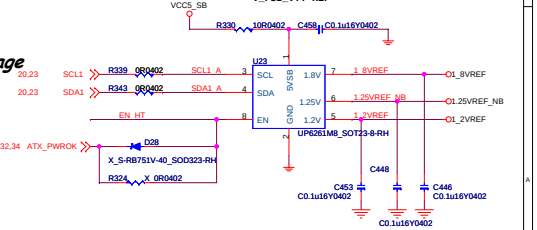








reference Voltage



S5	S3	MODE	5VDUAL	REMARK
1	1	X	VCC5	S0/S1/S2
1	0	X	VCC5_SB	S3
0	X	1	VCC5_SB	S4/S5
0	X	0	SHUTDOWM	S4/S5

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ATX connector / Front Panel

Intel Front Panel

ESD Protect

R465 330R VCC3

SATA_LED 19

PD_LED 31

C618 X_C180p50N0402

S-BAT54A_SOT23 D33

SUS_LED

PWR_LED

C616 C615 X_C0.1u25Y0402-RH

X_C0.1u25Y0402-RH

EMI

EMI For MSI / Intel Front Panel

VCC3 C619 X_C0.1u25Y0402-RH

R471 330R HDD+

JFP1

HDD+ PLED

HDD- SLED

RESET- PWSW+

RESET+ PWSW-

NC

PWR_LED 30

SUS_LED 30

PWSW+

PWSW-

3VDUAL

R460 4.7KR0402

R463 100R1%0402

Near Super I/O

PSIN

7,20,30,33 FP_RST#

R475 33R0402

R476 100R0402

C610 C0.1u25Y0402-RH

H2X5[10]M_COLORS-RH

C617 EMI X_C0.1u25Y0402-RH

PS2 KEYBOARD & MOUSE CONNECTOR

USB_1394

RN4 8P4R-4.7KR0402

C3 X_C0.1u25Y0402-RH

R8 X_1KR0402

JKBMS1

MSDATA R37 0R

MSCLK R48 0R

KBDATA R41 0R

KBCLK R55 0R

MS

KB

C36 C180p50N0402

C23 C180p50N0402

C28 C180p50N0402

C31 C180p50N0402

CONN-KB_MS-RH

BUZZER

VCC5

BAS32L_LL34 D29

BZ1

BUZZER-LF

RN26 8P4R-100R0402

SPK

20 SPKR

R340 2.2KR0402

Q50 N-2N3904_SOT23

C460 C0.1u25Y0402-RH

EMI solution

VCC3 C493 X_C0.1u25Y0402-RH

VCC5 C2 X_C0.1u25Y0402-RH

VCC5 C526 X_C0.1u25Y0402-RH

VCCP

VCC5

C395 C503 C109 C46 C83 C149 C406 C477

X_C0.1u25Y0402-RH

VCC3

C584 C444 C305 C479 C480

X_C0.1u25Y0402-RH

VCC3 C607 X_C0.1u25Y0402-RH

VCC5 C484 X_C0.1u25Y0402-RH

ATX Connector

ATXPWR1

13	3.3V	3.3V	1
14	-12V	3.3V	2
15	GND	GND	3
16	P_ON	5V	4
17	GND	GND	5
18	GND	5V	6
19	GND	GND	7
20	-5V	POK	8
21	5V	5VSB	9
22	5V	+12V	10
23	5V	+12V	11
24	GND	3.3V	12

VCC3 C124 X_C0.1u25Y0402-RH

-12V C219 X_C1000p50X0402

30 ATX_PSON#

C211 C1000p50X0402

C230 X_C0.1u25Y0402-RH

VCC5

EC36 CD1000u63EL11.5-RH

C183 C0.1u25Y0402-RH

VCC5

R133 10KR0402

ATX_PWROK 30,32,33

VCC5_SB

+12V

C164 C0.1u25Y0402-RH

VCC5 C206 X_C0.1u25Y0402-RH

C154 C142 X_C0.1u25Y0402-RH

VCC3 X_C0.1u25Y0402-RH

PWRCONN24P_CREAM-RH-1

3VDUAL C483 X_C0.1u25Y0402-RH

+1.8V_S0 C461 X_C0.1u25Y0402-RH

CP31 CP32 CP33 CP34 CP35 CP36 X_Copper

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