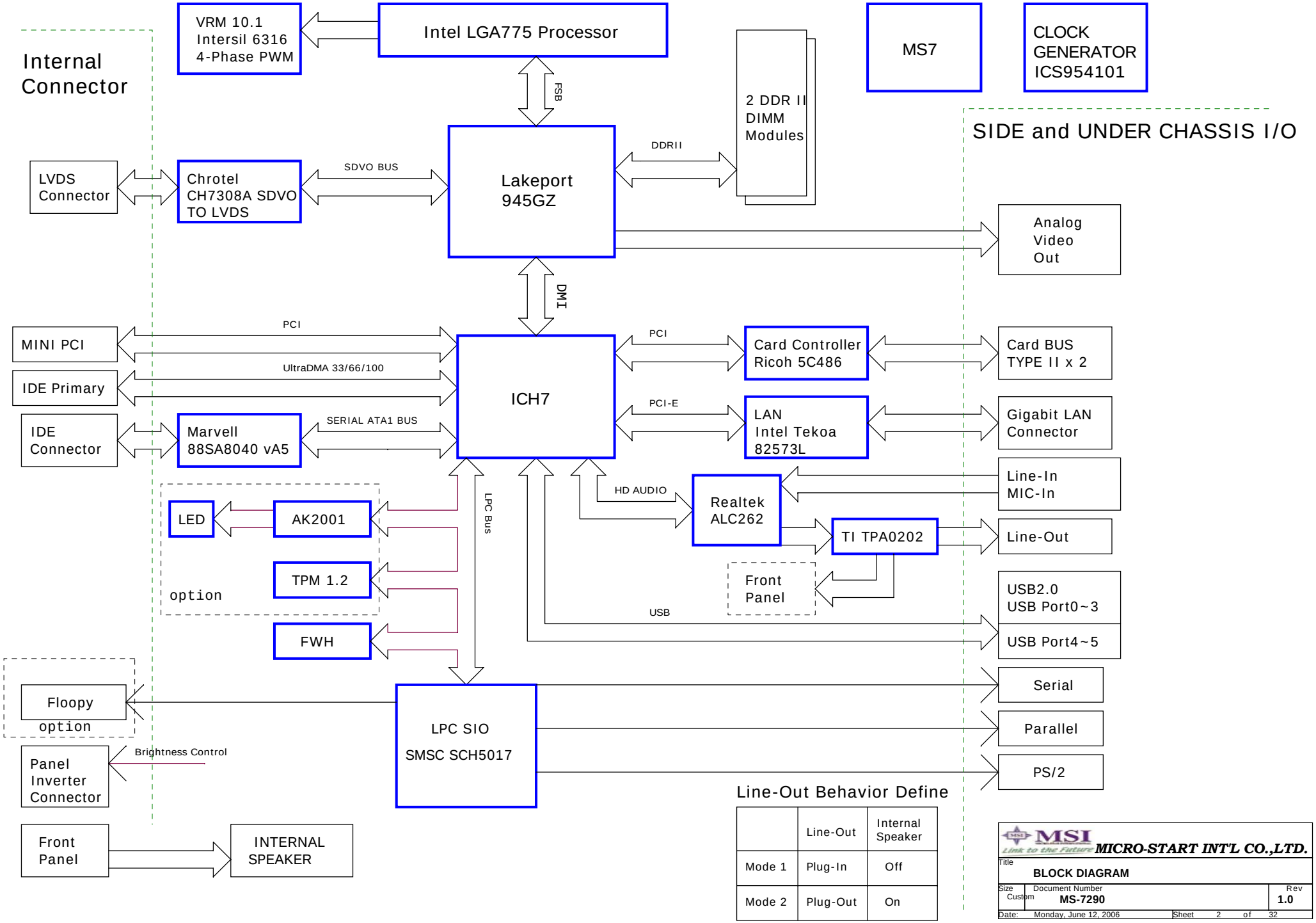
MS-7290 Block Diagram



Line-Out Behavior Define

	Line-Out	Internal Speaker
Mode 1	Plug-In	Off
Mode 2	Plug-Out	On

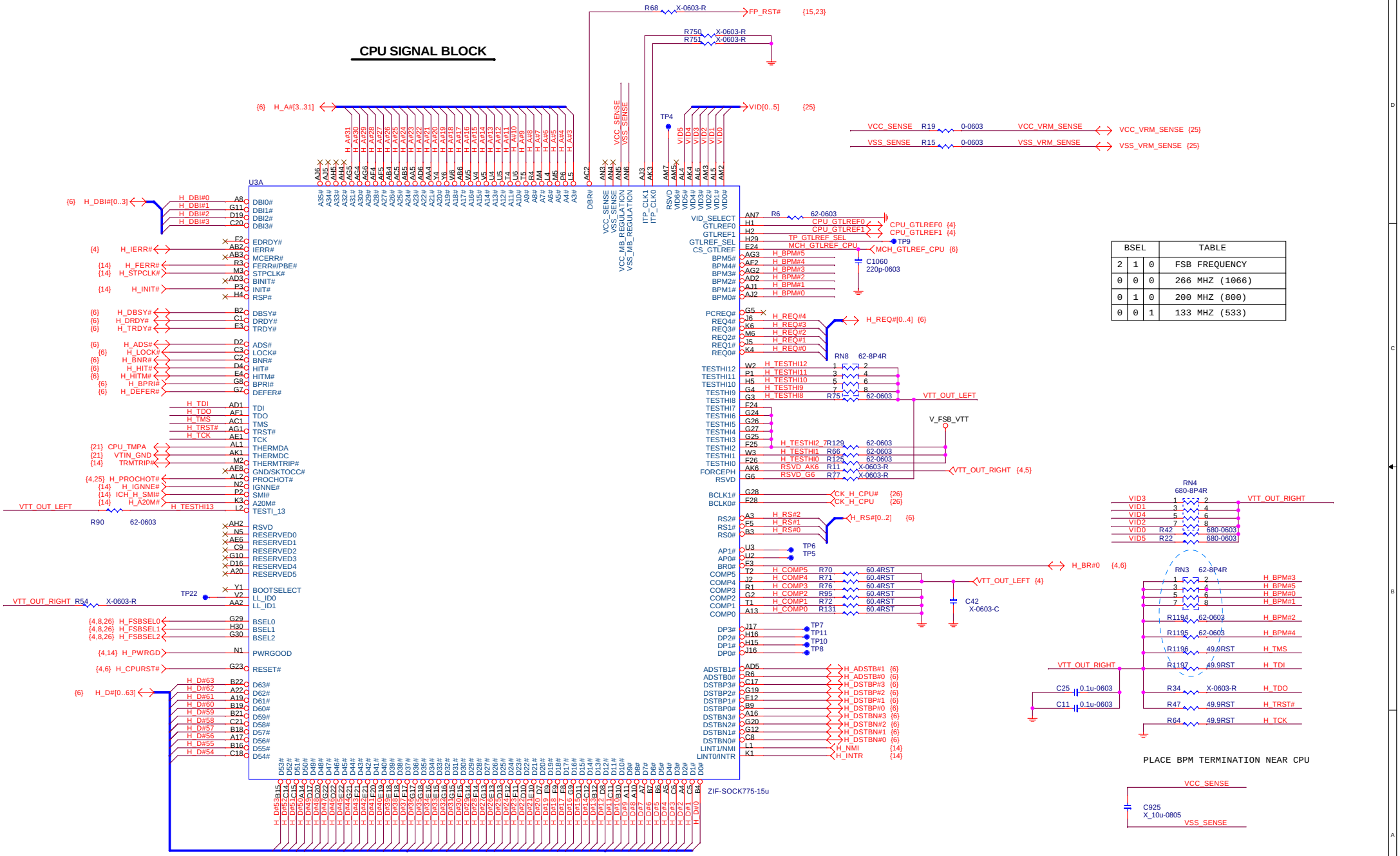
MSI *Link to the Future* **MICRO-START INT'L CO.,LTD.**

Title: **BLOCK DIAGRAM**

Size: Custom | Document Number: **MS-7290** | Rev: **1.0**

Date: Monday, June 12, 2006 | Sheet 2 of 32

CPU SIGNAL BLOCK



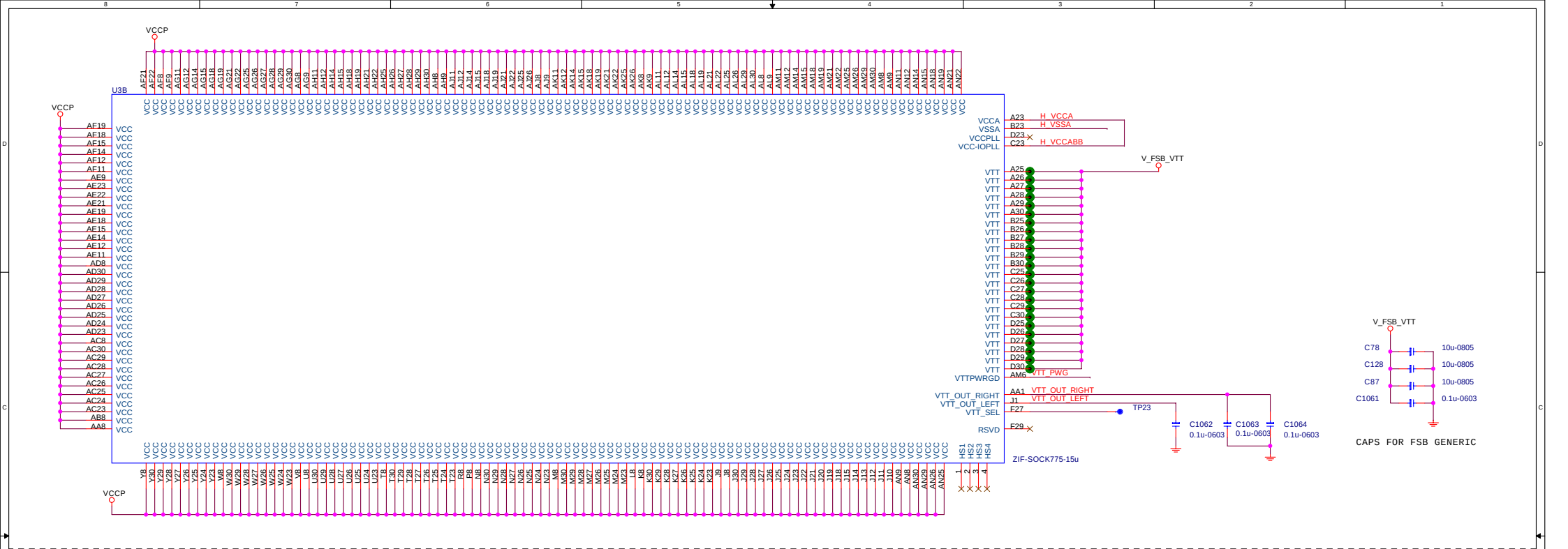
BSEL			TABLE
2	1	0	FSB FREQUENCY
0	0	0	266 MHZ (1066)
0	1	0	200 MHZ (800)
0	0	1	133 MHZ (533)

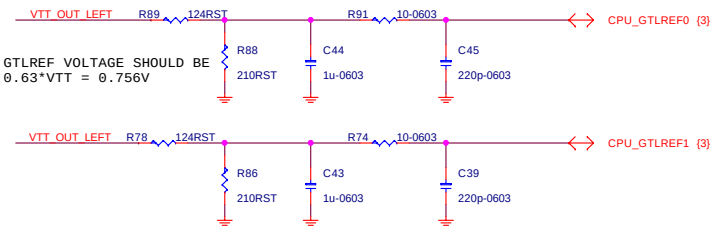
MSI Link to the Future MICRO-START INT'L CO.,LTD.

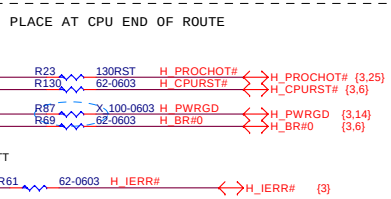
Title: LGA775 Signals

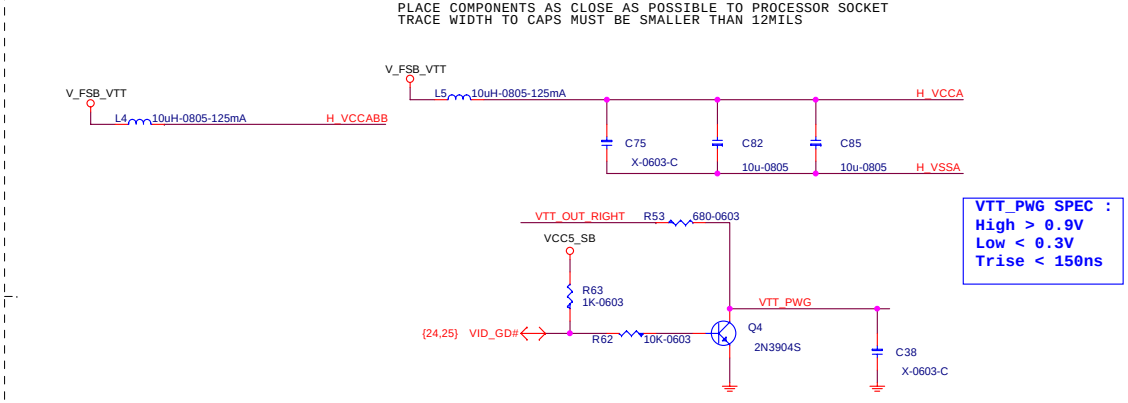
Size: Custom | Document Number: MS-7290 | Rev: 1.0

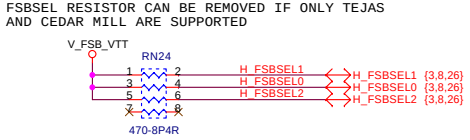
Date: Monday, June 12, 2006 | Sheet 3 of 32







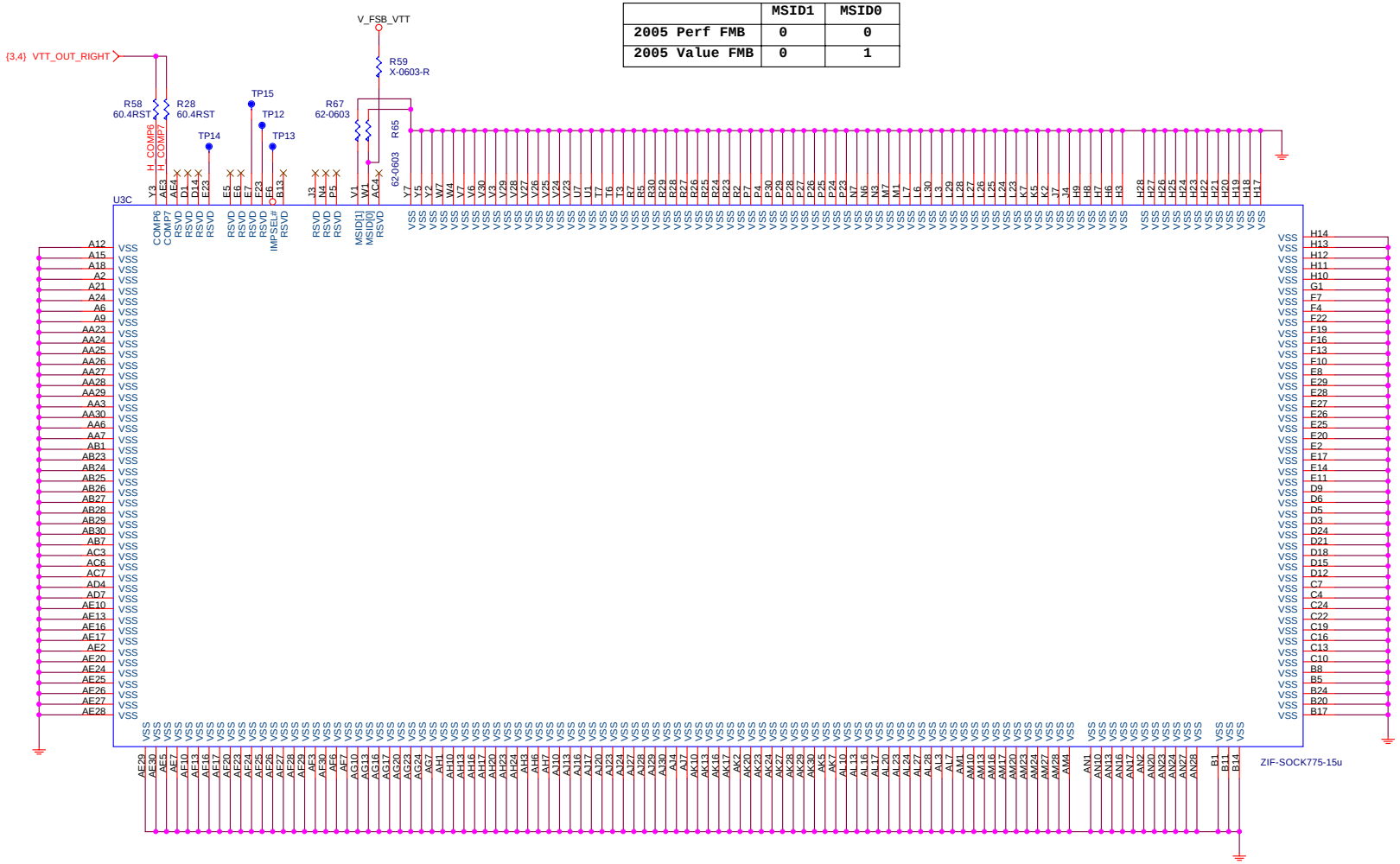




MICRO-START INT'L CO.,LTD.

Title: LGA775 Power		
Size: Custom	Document Number: MS-7290	Rev: 1.0
Date: Monday, June 12, 2006	Sheet 4 of 32	

	MSID1	MSID0
2005 Perf FMB	0	0
2005 Value FMB	0	1

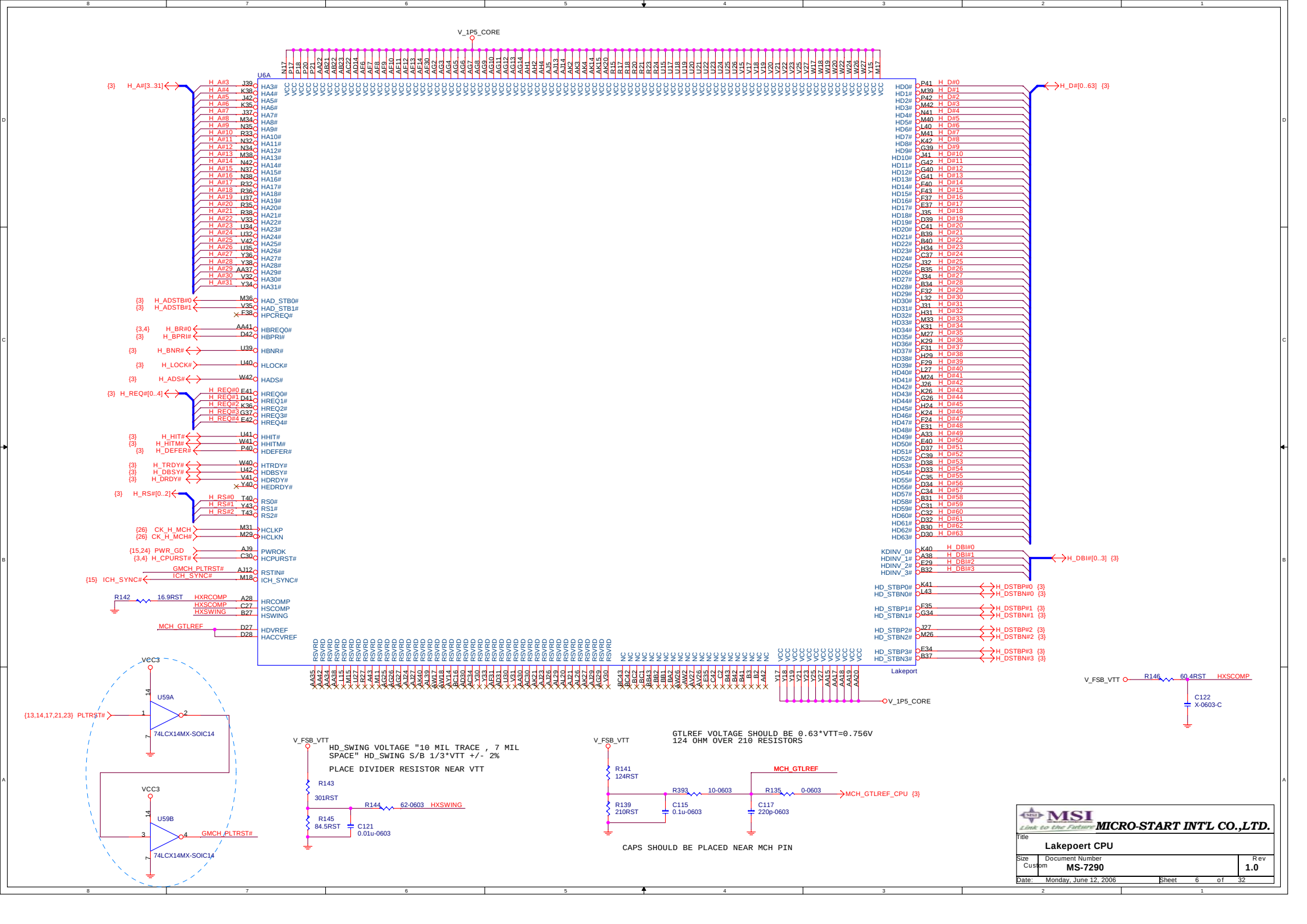


MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: LGA775 GND

Size: Custom | Document Number: MS-7290 | Rev: 1.0

Date: Monday, June 12, 2006 | Sheet 5 of 32


V_1P5_CORE
U6A
H_A#[3..31]
H_ADSTB#0
H_ADSTB#1
H_BR#0
H_BPRI#
H_BNR#
H_LOCK#
H_ADS#
H_REQ#[0..4]
H_HIT#
H_HITM#
H_DEFER#
H_TRDY#
H_DBSY#
H_DRDY#
H_RS#[0..2]
CK_H_MCH
CK_H_MCH#
PWR_GD
H_CPURST#
GMCH_PLTRST#
ICH_SYNC#
ICH_SYNC#
R142
16.9RST
HXRCOMP
HXSCOMP
HXSWING
MCH_GTLREF
H_D#[0..63]
H_DBI#[0..3]
H_DSTBP#0
H_DSTBN#0
H_DSTBP#1
H_DSTBN#1
H_DSTBP#2
H_DSTBN#2
H_DSTBP#3
H_DSTBN#3
Lakeport
V_1P5_CORE
V_FSB_VTT
R146
60.4RST
HXSCOMP
C122
X-0603-C
U59A
U59B
74LCX14MX-SOIC14
PLTRST#
VCC3
HD_SWING VOLTAGE "10 MIL TRACE , 7 MIL SPACE" HD_SWING S/B 1/3*VTT +/- 2%
PLACE DIVIDER RESISTOR NEAR VTT
R143
301RST
R144
62-0603
HXSWING
R145
84.5RST
C121
0.01u-0603
GTLREF VOLTAGE SHOULD BE 0.63*VTT=0.756V
124 OHM OVER 210 RESISTORS
R141
124RST
R139
210RST
C115
0.1u-0603
R393
10-0603
MCH_GTLREF
R135
0-0603
C117
220p-0603
MCH_GTLREF_CPU
CAPS SHOULD BE PLACED NEAR MCH PIN
MICRO-START INT'L CO.,LTD.
Title
Lakepoert CPU
Size
Custom
Document Number
MS-7290
Rev
1.0
Date:
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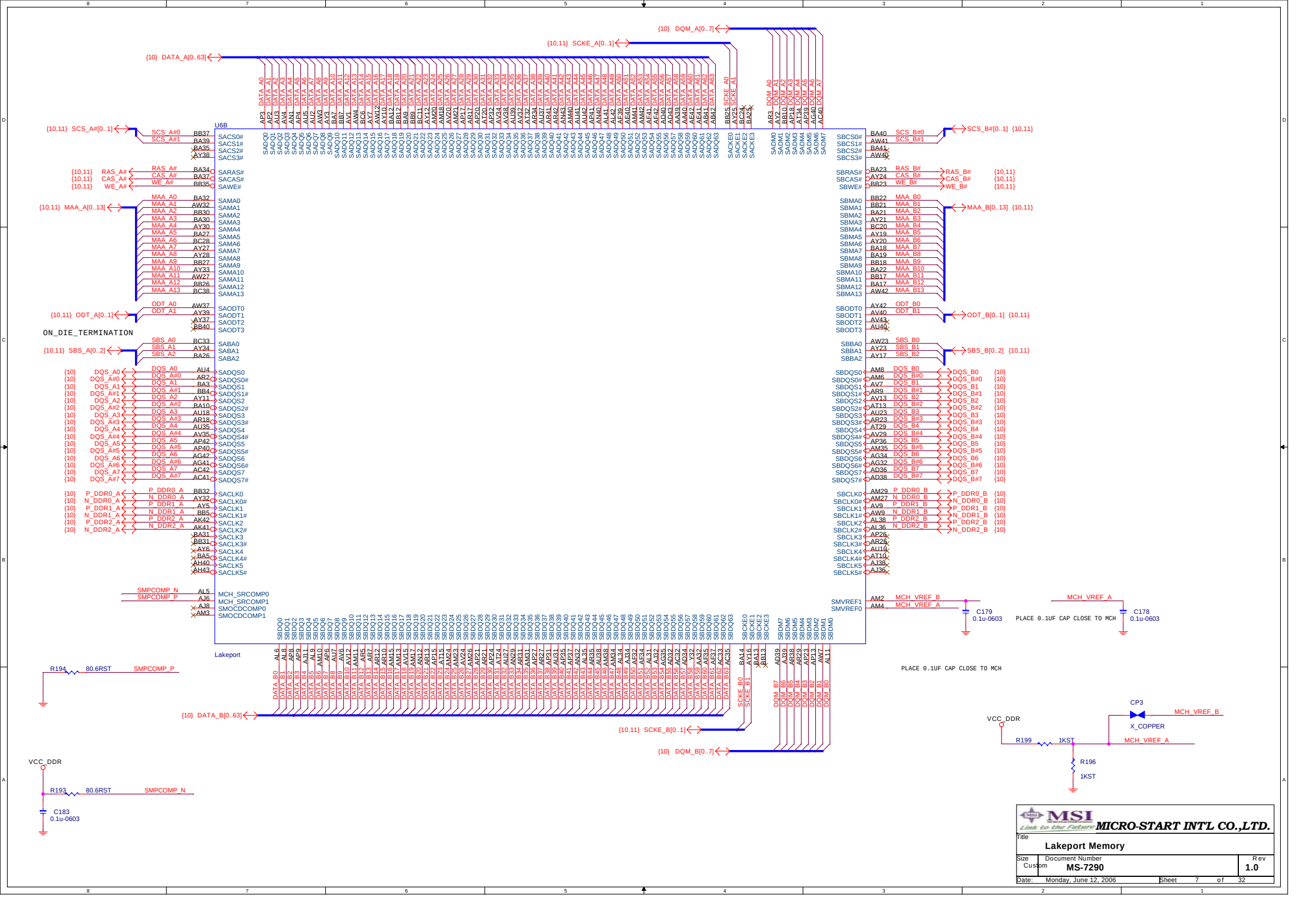
of
32



MICRO-START INT'L CO.,LTD.

Title	Lakeport Memory	
Size: Custom	Document Number: MS-7290	Rev: 1.0
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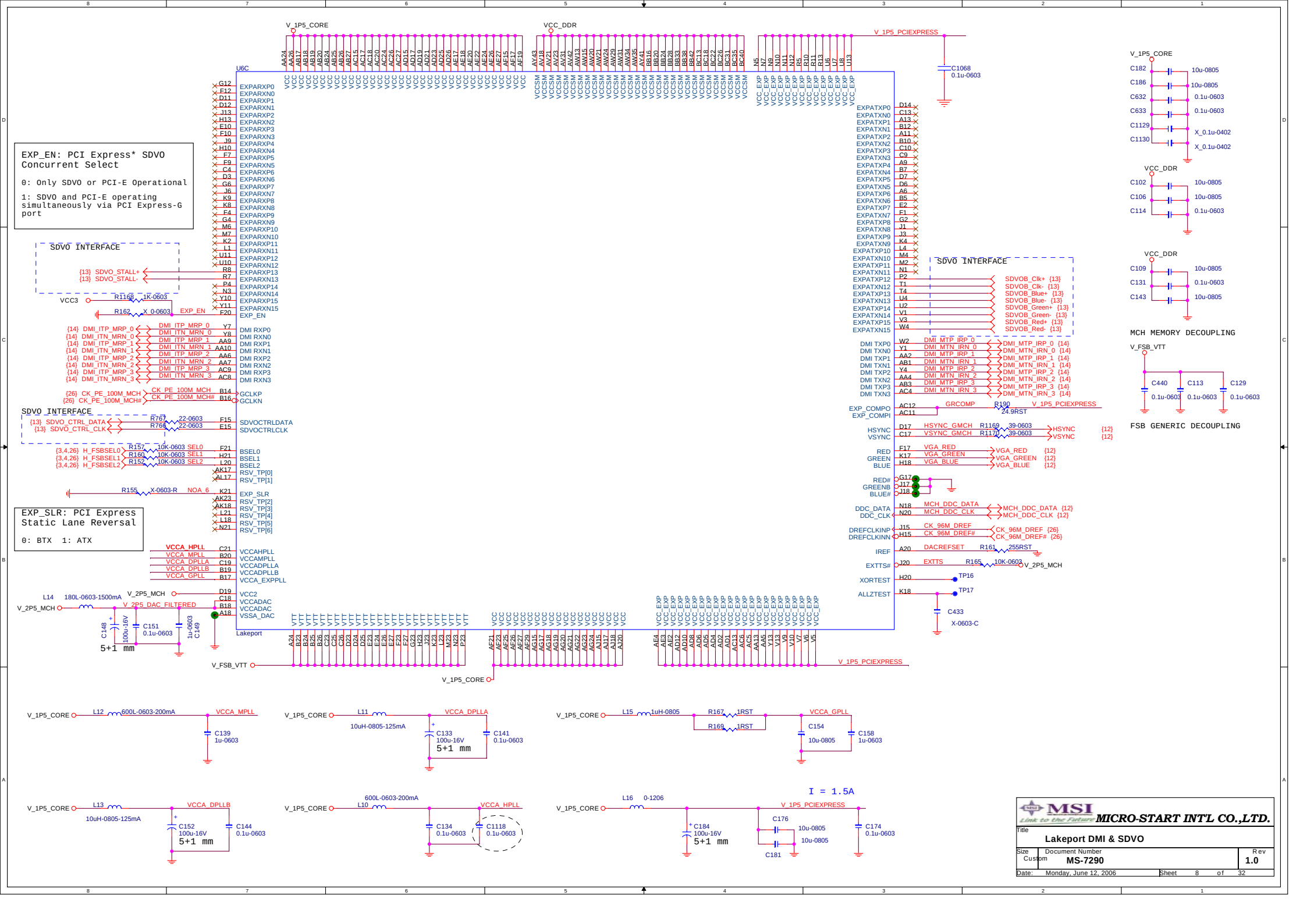
EXP_EN: PCI Express* SDVO Concurrent Select
0: Only SDVO or PCI-E Operational
1: SDVO and PCI-E operating simultaneously via PCI Express-G port
EXP_SLR: PCI Express Static Lane Reversal
0: BTX 1: ATX
U6C
Lakeport
SDVO INTERFACE
SDVO INTERFACE
SDVO INTERFACE
V_1P5_CORE
VCC_DDR
V_1P5_PCIEXPRESS
V_2P5_MCH
V_FSB_VTT
MCH MEMORY DECOUPLING
FSB GENERIC DECOUPLING
I = 1.5A
MSI
MICRO-START INT'L CO.,LTD.
Link to the Future
Title
Lakeport DMI & SDVO
Size
Custom
Document Number
MS-7290
Rev
1.0
Date: Monday, June 12, 2006
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MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: Lakeport GND		
Size: Custom	Document Number: MS-7290	Rev: 1.0
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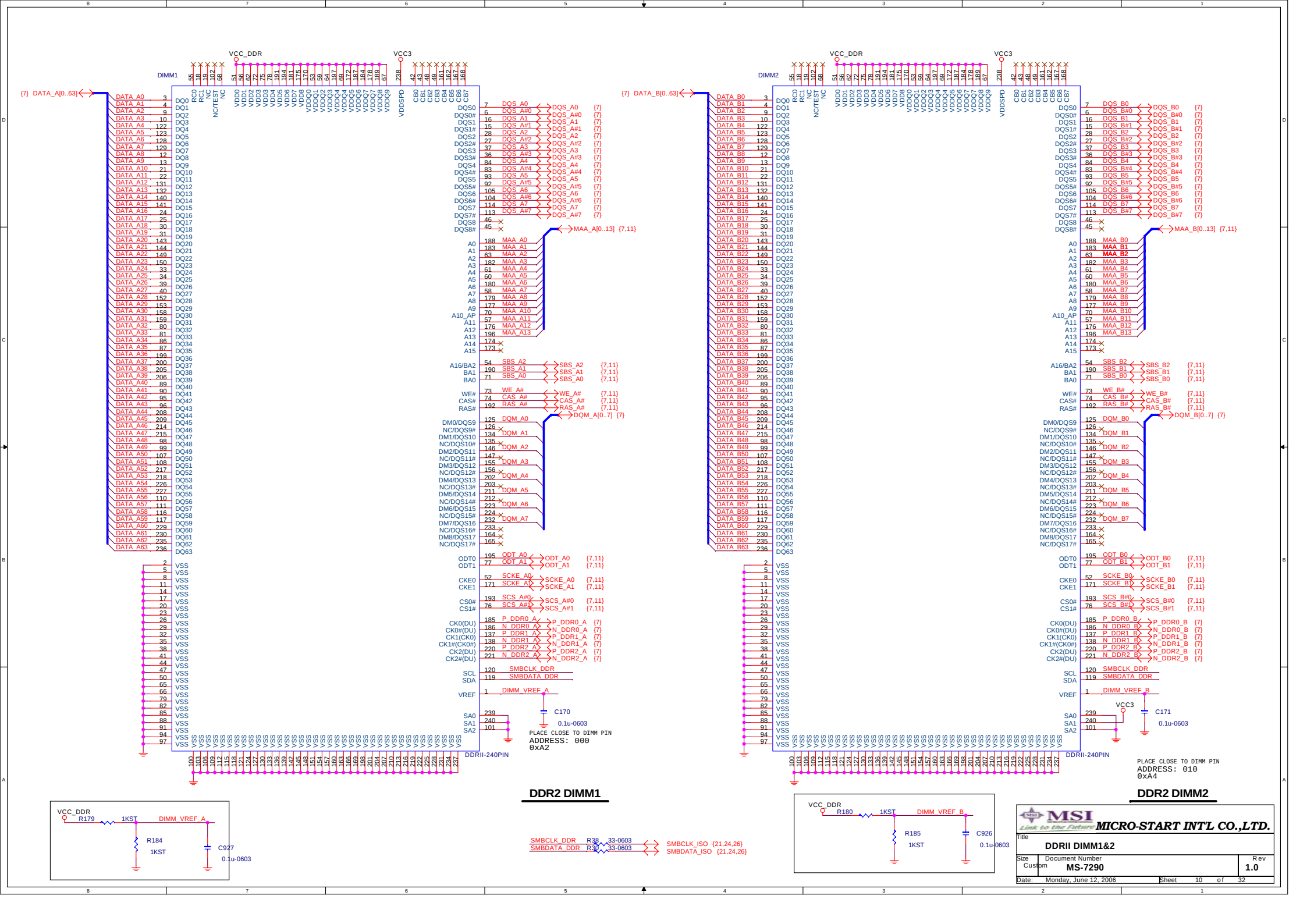
DIMM1
DIMM2
VCC_DDR
VCC3
DDRII-240PIN
DDR2 DIMM1
DDR2 DIMM2
PLACE CLOSE TO DIMM PIN
ADDRESS: 000
0xA2
ADDRESS: 010
0xA4
SMBCLK_DDR
SMBDATA_DDR
SMBCLK_ISO {21,24,26}
SMBDATA_ISO {21,24,26}
MICRO-START INT'L CO.,LTD.
DDRII DIMM1&2
MS-7290
Rev 1.0
Monday, June 12, 2006
Sheet 10 of 32

CHANNEL A V_SM_VTT DECOUPLING CAPS

CHANNEL B V_SM_VTT DECOUPLING CAPS

VTT_DDR

C59 0.1u-0603
C55 X-1206-C

C50 10u-1206
C100 X-1206-C

C103 0.1u-0603
C73 0.1u-0603
C67 0.1u-0603
C60 0.1u-0603
C83 0.1u-0603
C94 0.1u-0603

DIMM1 termination 5020

C71 0.1u-0603
C57 0.1u-0603
C76 0.1u-0603

C53 0.1u-0603
C51 10u-1206
C95 0.1u-0603
C98 0.1u-0603
C89 0.1u-0603
C81 0.1u-0603

VCC_DDR

EC43 470u-4V
EC40 470u-4V
EC155 470u-4V
EC156 470u-4V

SMT 3.8mm

Put between
DIMM1 and DIMM2

C56 1u-0603
C160 1u-0603
C65 1u-0603
C96 1u-0603
C112 1u-0603
C88 1u-0603
C77 1u-0603

C86 1u-0603
C101 1u-0603
C58 1u-0603
C132 1u-0603
C63 1u-0603
C74 1u-0603
C84 1u-0603

C90 1u-0603

VTT_DDR

MAA_A1 MAA_A2 MAA_A3 MAA_A4 MAA_A6 MAA_A8 MAA_A5 MAA_A9 MAA_A7 MAA_A11 MAA_A12 SBS_A2 MAA_A13 RAS_A# WE_A# CAS_A#

RN20 RN22 RN25 33-8P4R-0402

R104 R113 R116 R106 33-0402

{7,10} RAS_A#
{7,10} WE_A#
{7,10} CAS_A#

SBS_A1 SBS_A0 MAA_A10 MAA_A0

RN88 33-8P4R-0402

SCS_A#0 R107 43-0402

ODT_A0 R105 43-0402

SCKE_A0 SCKE_A1 ODT_A1 SCS_A#1

RN27 RN15 43-8P4R-0402

{7,10} MAA_A[0..13]
{7,10} SBS_A[0..2]
{7,10} SCS_A#[0..1]
{7,10} SCKE_A[0..1]
{7,10} ODT_A[0..1]

MAA_B4 MAA_B3 MAA_B2 MAA_B1 MAA_B9 MAA_B5 MAA_B8 MAA_B6 SBS_B2 MAA_B12 MAA_B11 MAA_B7 MAA_B10 MAA_B0 SBS_B0 SBS_B1

RN21 RN23 RN26 RN19 33-8P4R-0402

WE_B# RAS_B# CAS_B#

RN18 33-8P4R-0402

{7,10} WE_B#
{7,10} RAS_B#
{7,10} CAS_B#

SCS_B#0 ODT_B0 SCS_B#1

RN17 43-8P4R-0402

SCKE_B0 SCKE_B1

RN28 43-8P4R-0402

ODT_B1 R760 43-0402

MAA_B13 R761 33-0402

{7,10} MAA_B[0..13]
{7,10} SBS_B[0..2]
{7,10} SCS_B#[0..1]
{7,10} SCKE_B[0..1]
{7,10} ODT_B[0..1]

Grantsdale GMCH Power Sequencing Requirement Between 1.5V Core and 2.5V DAC

VCC3

Q21 NDS351AN-S-SOT23

CT2 X-0805-C

C157 0.1u-0603

+12V

U7A LM358MX-SO8

R168 130RST

R171 120RST

EC45 100u-16V

C147 0.1u-0603

V_2P5_MCH

1P2VREF {13,24}

C153 X-0603-C

V_1P5_CORE V_2P5_MCH

D9 1N4001-S-SM-1

MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: DDRII Termination and MCH2.5V

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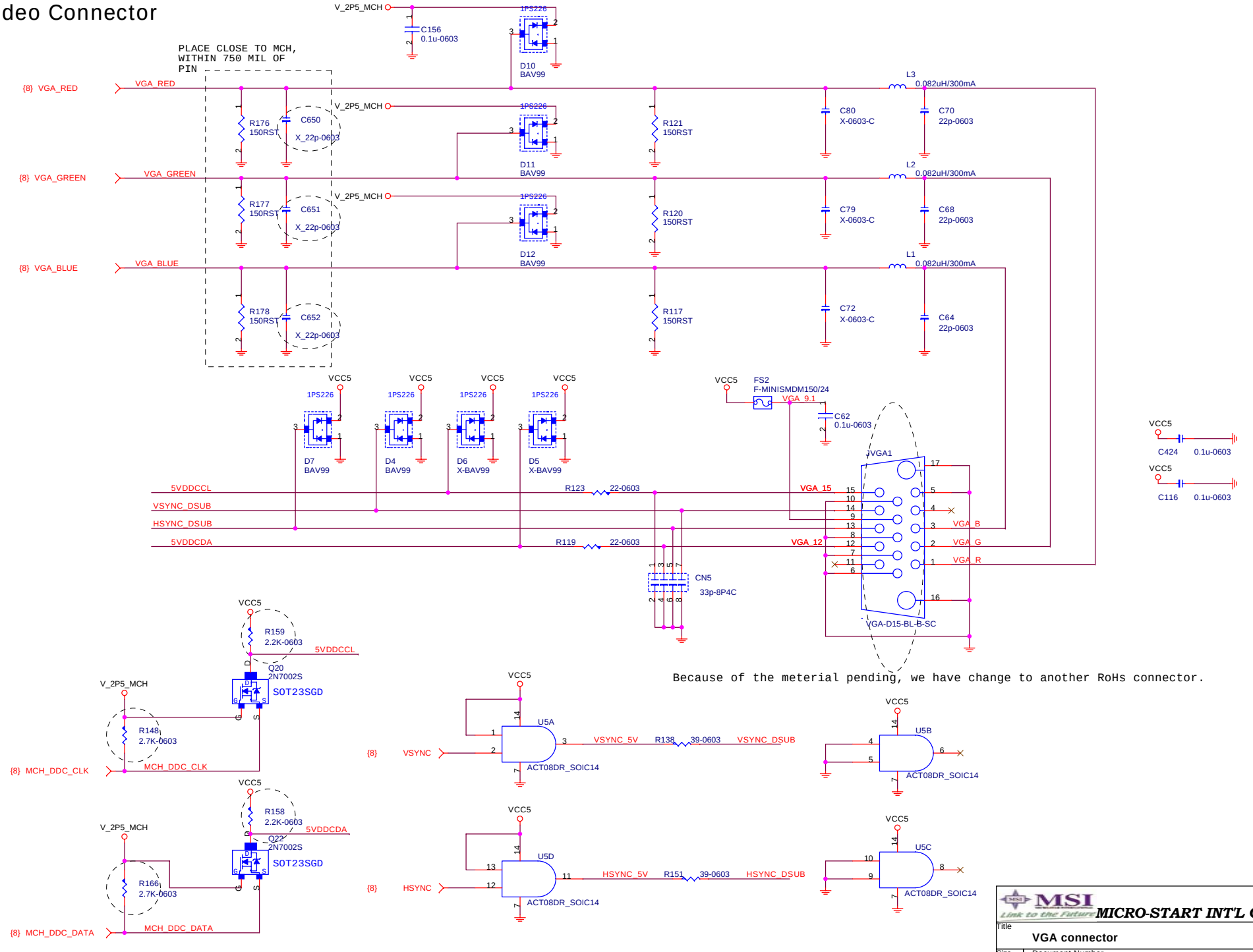
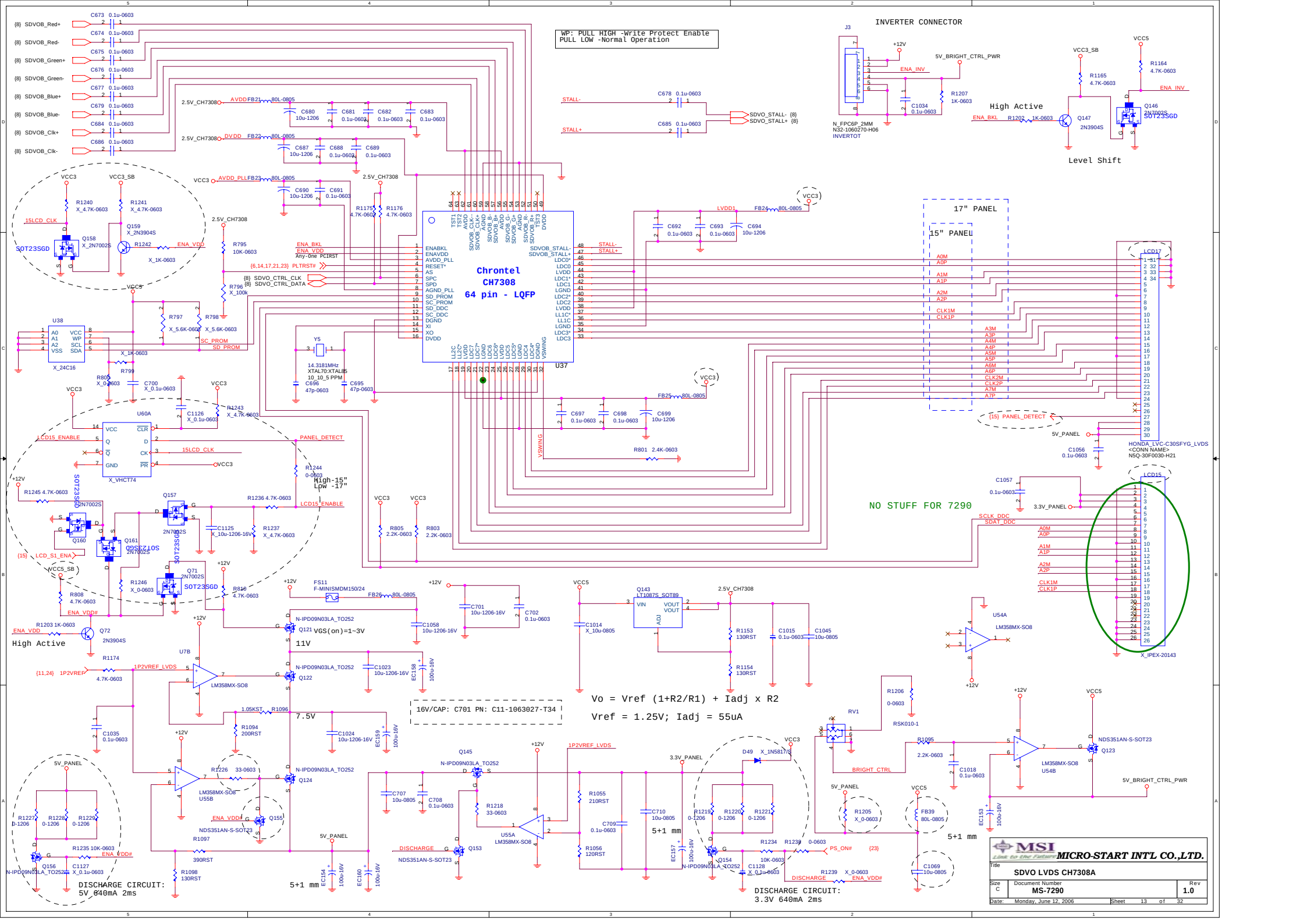
Video Connector



Because of the meterial pending, we have change to another RoHs connector.

MICRO-START INT'L CO.,LTD.

Title	VGA connector	
Size: Custom	Document Number: MS-7290	Rev: 1.0
Date: Monday, June 12, 2006	Sheet 12 of 32	


WP: PULL HIGH -Write Protect Enable
PULL LOW -Normal Operation
INVERTER CONNECTOR
Chrontel
CH7308
64 pin - LQFP
U37
17" PANEL
15" PANEL
NO STUFF FOR 7290
High Active
Level Shift
High-15"
Low -17"
Vo = Vref (1+R2/R1) + Iadj x R2
Vref = 1.25V; Iadj = 55uA
16V/CAP: C701 PN: C11-1063027-T34
DISCHARGE CIRCUIT:
5V 640mA 2ms
DISCHARGE CIRCUIT:
3.3V 640mA 2ms
5+1 mm
MSI MICRO-START INT'L CO.,LTD.
SDVO LVDS CH7308A
MS-7290
1.0
Monday, June 12, 2006

ICH 7
PART 1/3

U19A

PCI INTERFACE

AD0 E18 AD1 C18 AD2 A16 AD3 F18 AD4 E16 AD5 A18 AD6 E17 AD7 A17 AD8 A15 AD9 C14 AD10 E14 AD11 D14 AD12 B12 AD13 C13 AD14 G15 AD15 G13 AD16 E12 AD17 C11 AD18 D11 AD19 A11 AD20 A10 AD21 F11 AD22 F10 AD23 E9 AD24 D9 AD25 B9 AD26 A8 AD27 A6 AD28 C7 AD29 B6 AD30 E6 AD31 D6

{28,29} AD[0..31]

C_BE#0 B15 C_BE#1 C12 C_BE#2 D12 C_BE#3 C15

{28,29} C_BE#[0..3]

C/BE0# C/BE1# C/BE2# C/BE3#

{28,29} DEVSEL# A12
{28,29} FRAME# F16
{28,29} IRDY# A7
{28,29} TRDY# F14
{28,29} STOP# F15
{28,29} PAR E10
{28} LOCK# E11
{28,29} SERR# B10
{28,29} PERR# C9
{28,29} PCI_PME# B19

DEVSEL# FRAME# IRDY# TRDY# STOP# PAR PLOCK# SERR# PERR# PME#

{26} ICH_PCLK
R303 33-0603
{24} PCIRST_ICH6# B18
C241 X-0603-C
A9

PCICLK PCIRST#

{29} PREQ#0 D7
{28} PREQ#2 C16
PREQ#1
PREQ#3 C17
PREQ#4 E13
PREQ#5 R306 0-0603 A13 C8

REQ0# REQ1# REQ2# REQ3# GPIO22/REQ4# GPIO1/REQ5#

{29} PGNT#0 E7
{28} PGNT#2 D16
D17
F13
A14
PGNT#5 R307 0-0603 D8

GNT0# GNT1# GNT2# GNT3# GPIO48/GNT4# GPIO17/GNT5#

INTERRUPT

{28,29} PIRQ#A A3
{28,29} PIRQ#B B4
{28} PIRQ#C C5
PIRQ#D B5
PIRQ#E G8
PIRQ#F E7
PIRQ#G F8
PIRQ#H G7

PIRQA# PIRQB# PIRQC# PIRQD# GPIO2/PIRQE# GPIO3/PIRQF# GPIO4/PIRQG# GPIO5/PIRQH#

{21,23,29} SERIRQ AH21
{17} IDE_IRQ AH16

SERIRQ IDEIRQ

SPI

RN89 10K-8P4R
VCC3_SB

P5 SPI_MOSI
P2 SPI_MISO
P6 SPI_CS#
R2 SPI_CLK
P1 SPI_ARB

{27} SPI_MISO
{27} SPI_CS#
{27} SPI_MOSI
{27} SPI_CLK
{27} SPI_ARB

RN90_X_0-8P4R

Stuff if share SPI.

PREQ#1 PREQ#2 PREQ#4 PREQ#3 PREQ#5 PIRQ#D PIRQ#C PREQ#0
RN44 8.2K-8P4R
RN45 8.2K-8P4R
VCC3

PGNT#5
R313 X-0603-R

VCC3 --- 8.2kOhm
VCC5 --- 2.7kOhm

CPU

A20M# AH28 H_A20M# {3}
CPUSLP# AG27
FERR# AG26 H_FERR# {3}
IGNNE# AG22 H_IGNNE# {3}
INIT# AF22 H_INIT# {3}
INIT3_3V# AG21 FWH_INIT# {17}
INTR AF25 H_INTR {3}
NMI AH24 H_NMI {3}
SMI# AF23 ICH_H_SMI# {3}
STPCLK# AH22 H_STPCLK# {3}
RCIN# AG23 KBRST# {21}
A20GATE AE22 A20GATE {21}
THRMTRIP# AF26 TRMTRIP# {3}
GPO49/CPUPWRGD AG24 H_PWRGD {3,4}

PCI EXPRESS

PLTRST# C26 R247 33-0603 PLTRST# {6,13,17,21,23}

PERN_1 F26 HSI_N1 {27}
PERP_1 F25 HSI_P1 {27}
PETN_1 E28 HSO_N1_C C286 0.1u-0603 HSO_N1 {27}
PETP_1 F27 HSO_P1_C C1013 0.1u-0603 HSO_P1 {27}

PERN_2 H26
PERP_2 H25
PETN_2 G28
PETP_2 G27

PERN_3 K26
PERP_3 K25
PETN_3 J28
PETP_3 J27

PERN_4 M26
PERP_4 M25
PETN_4 L28
PETP_4 L27

PERN_5 P26
PERP_5 P25
PETN_5 N28
PETP_5 N27

PERN_6 T25
PERP_6 T24
PETN_6 R28
PETP_6 R27

DIRECT MEDIA

DMI_0RXN V26 DMI_MTN_IRN_0 {8}
DMI_0RXP V25 DMI_MTP_IRP_0 {8}
DMI_0TXN U28 DMI_ITN_MRN_0 {8}
DMI_0TXP U27 DMI_ITP_MRP_0 {8}

DMI_1RXN Y26 DMI_MTN_IRN_1 {8}
DMI_1RXP Y25 DMI_MTP_IRP_1 {8}
DMI_1TXN W28 DMI_ITN_MRN_1 {8}
DMI_1TXP W27 DMI_ITP_MRP_1 {8}

DMI_2RXN AB26 DMI_MTN_IRN_2 {8}
DMI_2RXP AB25 DMI_MTP_IRP_2 {8}
DMI_2TXN AA28 DMI_ITN_MRN_2 {8}
DMI_2TXP AA27 DMI_ITP_MRP_2 {8}

DMI_3RXN AD25 DMI_MTN_IRN_3 {8}
DMI_3RXP AD24 DMI_MTP_IRP_3 {8}
DMI_3TXN AC28 DMI_ITN_MRN_3 {8}
DMI_3TXP AC27 DMI_ITP_MRP_3 {8}

DMI_CLKN AE28 CK_PE_100M_ICH# {26}
DMI_CLKP AE27 CK_PE_100M_ICH {26}

DMI_ZCOMP C25 R251 24.9RST V_DMI {16}
DMI_IRCOMP D25

LAN

LAN_CLK V3
LAN_RSTSYNC U3
LAN_RXD0 U5
LAN_RXD1 V4
LAN_RXD2 T5

LAN_TXD0 U7
LAN_TXD1 V6
LAN_TXD2 V7

EE_CS W1
EE_DIN W3
EE_DOUT Y2
EE_SHCLK Y1

VSS_0 A4 VSS_1 A23 VSS_2 B1 VSS_3 B8 VSS_4 B11 VSS_5 B14 VSS_6 B17 VSS_7 B20 VSS_8 B26 VSS_9 C2 VSS_10 C6 VSS_11 D10 VSS_12 D13 VSS_13 D18 VSS_14 D21 VSS_15 D24 VSS_16 E1 VSS_17 E2 VSS_18 E8 VSS_19 E15 VSS_20 F3 VSS_21 F4 VSS_22 F5 VSS_23 F22 VSS_24 F27 VSS_25 F28 VSS_26 G1 VSS_27 G2 VSS_28 G5 VSS_29 G6 VSS_30 G9 VSS_31 G14 VSS_32 G18 VSS_33 G21 VSS_34 G24 VSS_35 G25 VSS_36 G26 VSS_37 H3 VSS_38 H4 VSS_39 H5 VSS_40

ICH7

V_FSB_VTT
R384 62-0603 TRMTRIP#

V_FSB_VTT
R387 62-0603 H_FERR#

THERMTRIP# can be routed next to FERR# with 5mil spacing to others 7mil.

PLACE AT ICH END OF ROUTE

SERIRQ R274 10K-0603
KBRST# R270 10K-0603
A20GATE R277 10K-0603
VCC3

MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: ICH7 PCI/DMI/CPU/IRQ

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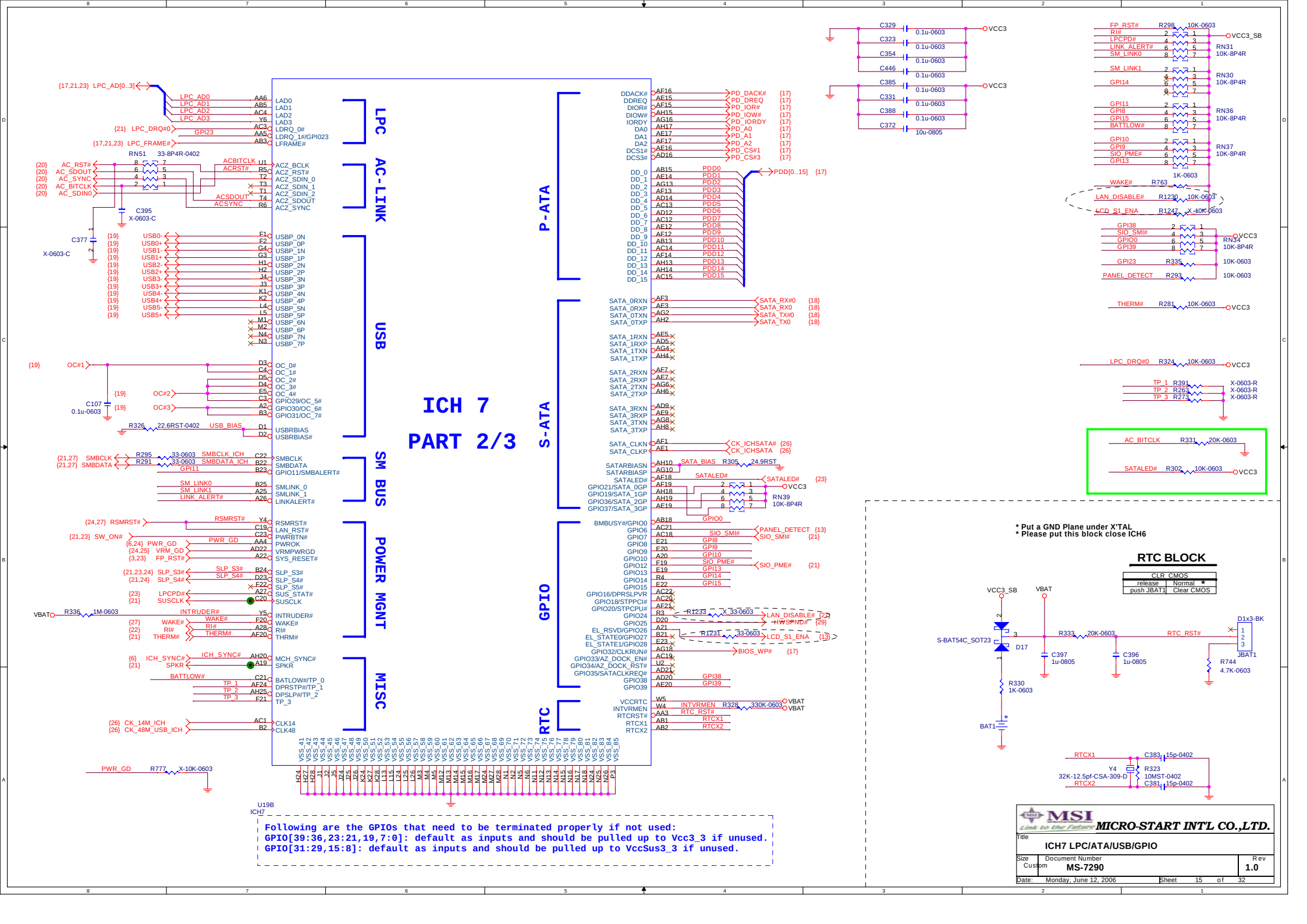
ICH 7
PART 2/3
LPC
AC-LINK
USB
SM BUS
POWER MGNT
MISC
P-ATA
S-ATA
GPIO
RTC
RTC BLOCK
* Put a GND Plane under X'TAL
* Please put this block close ICH6
Following are the GPIOs that need to be terminated properly if not used:
GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3_3 if unused.
GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3_3 if unused.
MSI
MICRO-START INT'L CO.,LTD.
Title
ICH7 LPC/ATA/USB/GPIO
Size
Custom
Document Number
MS-7290
Rev
1.0
Date: Monday, June 12, 2006
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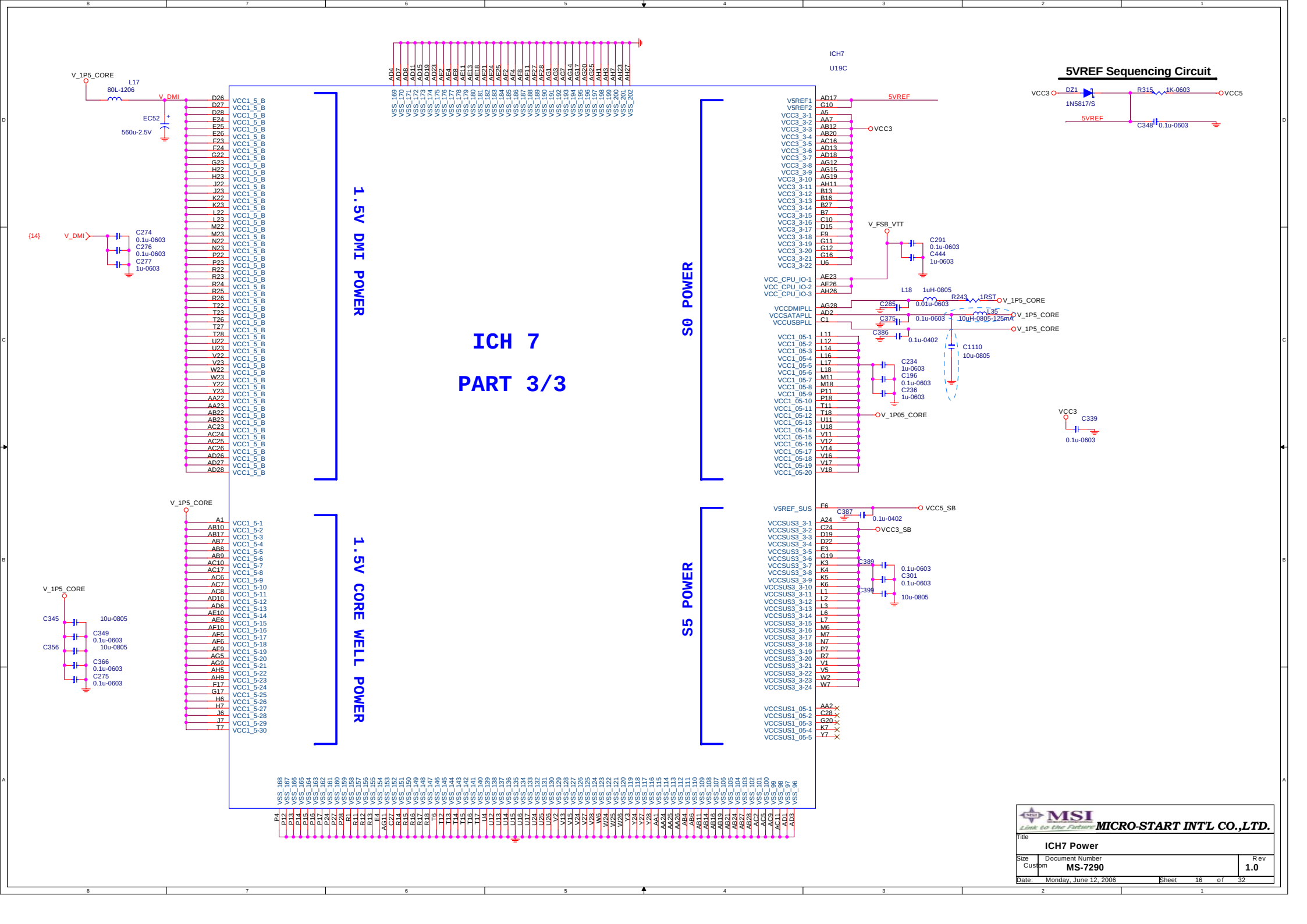
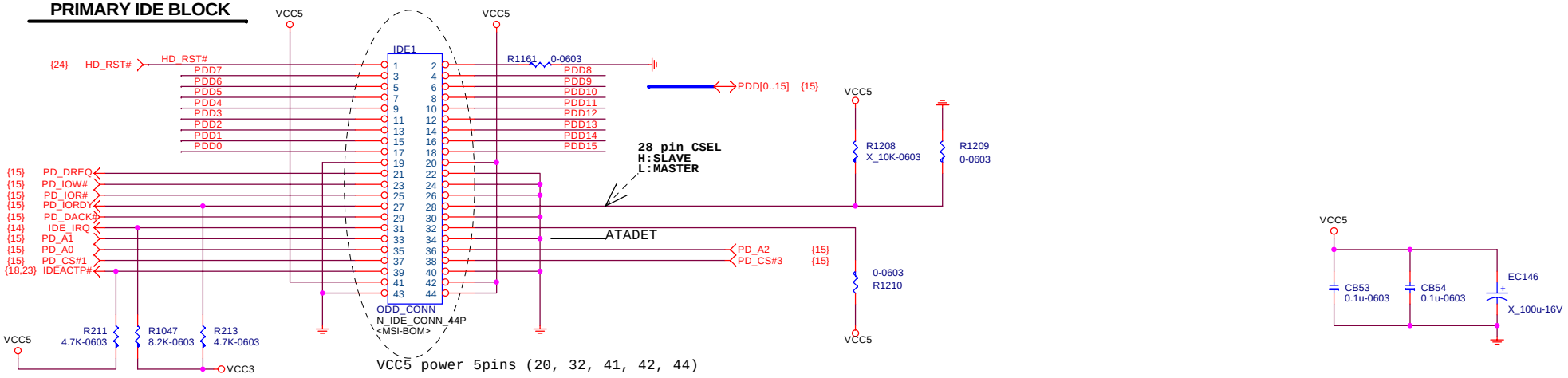
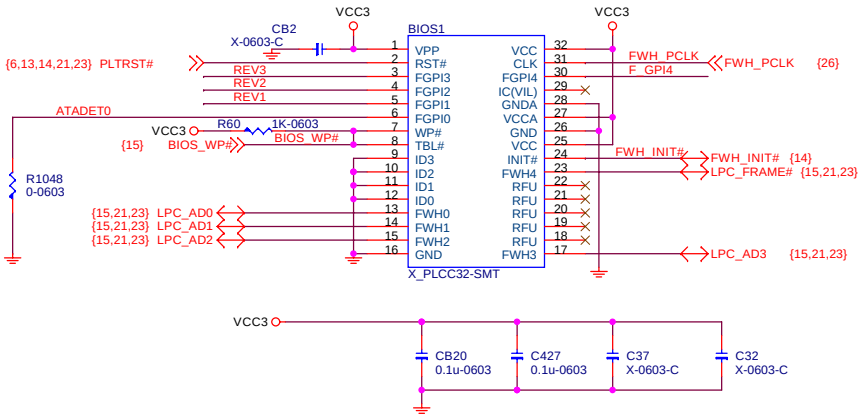

ICH 7
PART 3/3
1.5V DMI POWER
1.5V CORE WELL POWER
S0 POWER
S5 POWER
ICH7
U19C
5VREF Sequencing Circuit
V_1P5_CORE
V_DMI
V_1P05_CORE
V_FSB_VTT
VCC3
VCC5
VCC5_SB
VCC3_SB
5VREF
V_1P5_CORE
V_1P5_CORE
V_1P5_CORE
L17
80L-1206
EC52
560u-2.5V
C274
0.1u-0603
C276
0.1u-0603
C277
1u-0603
C345
10u-0805
C349
0.1u-0603
C356
10u-0805
C366
0.1u-0603
C275
0.1u-0603
C291
0.1u-0603
C444
1u-0603
L18
1uH-0805
C285
0.01u-0603
R243
1RST
L35
10uH-0805-125mA
C375
0.1u-0603
C386
0.1u-0402
C1110
10u-0805
C234
1u-0603
C196
0.1u-0603
C236
1u-0603
C339
0.1u-0603
C387
0.1u-0402
C389
0.1u-0603
C301
0.1u-0603
C399
10u-0805
DZ1
1N5817/S
R315
1K-0603
C348
0.1u-0603
MICRO-START INT'L CO.,LTD.
ICH7 Power
MS-7290
1.0
Monday, June 12, 2006
16
32

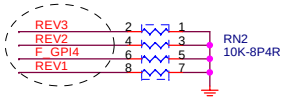
PRIMARY IDE BLOCK

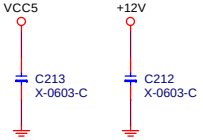


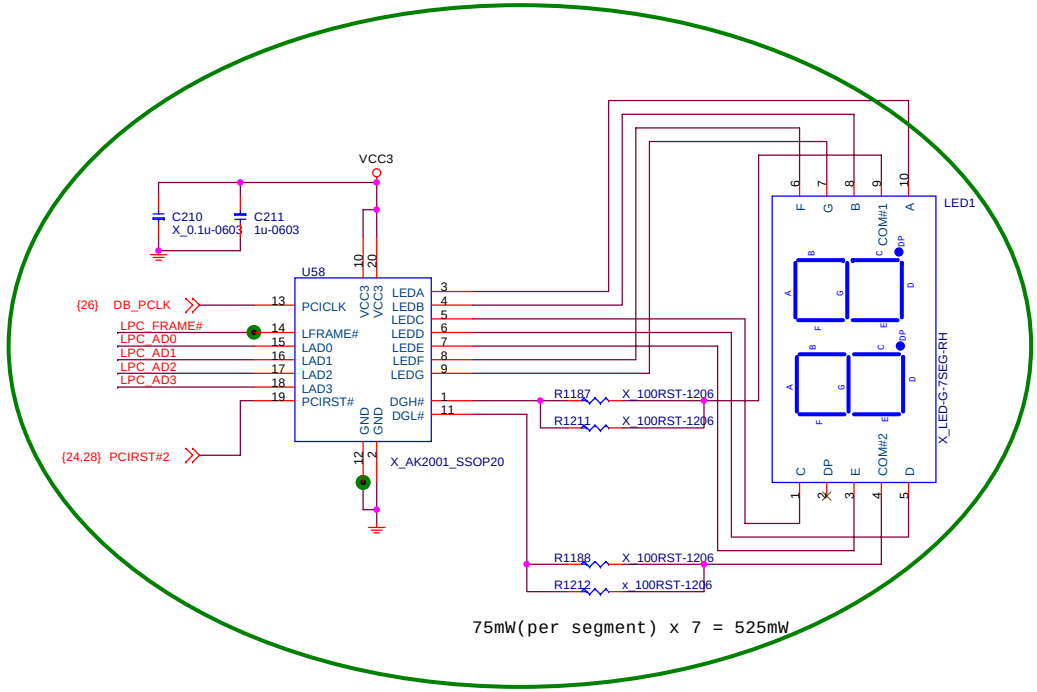
FIRMWARE HUB (FWH)



FWH RESISTORS



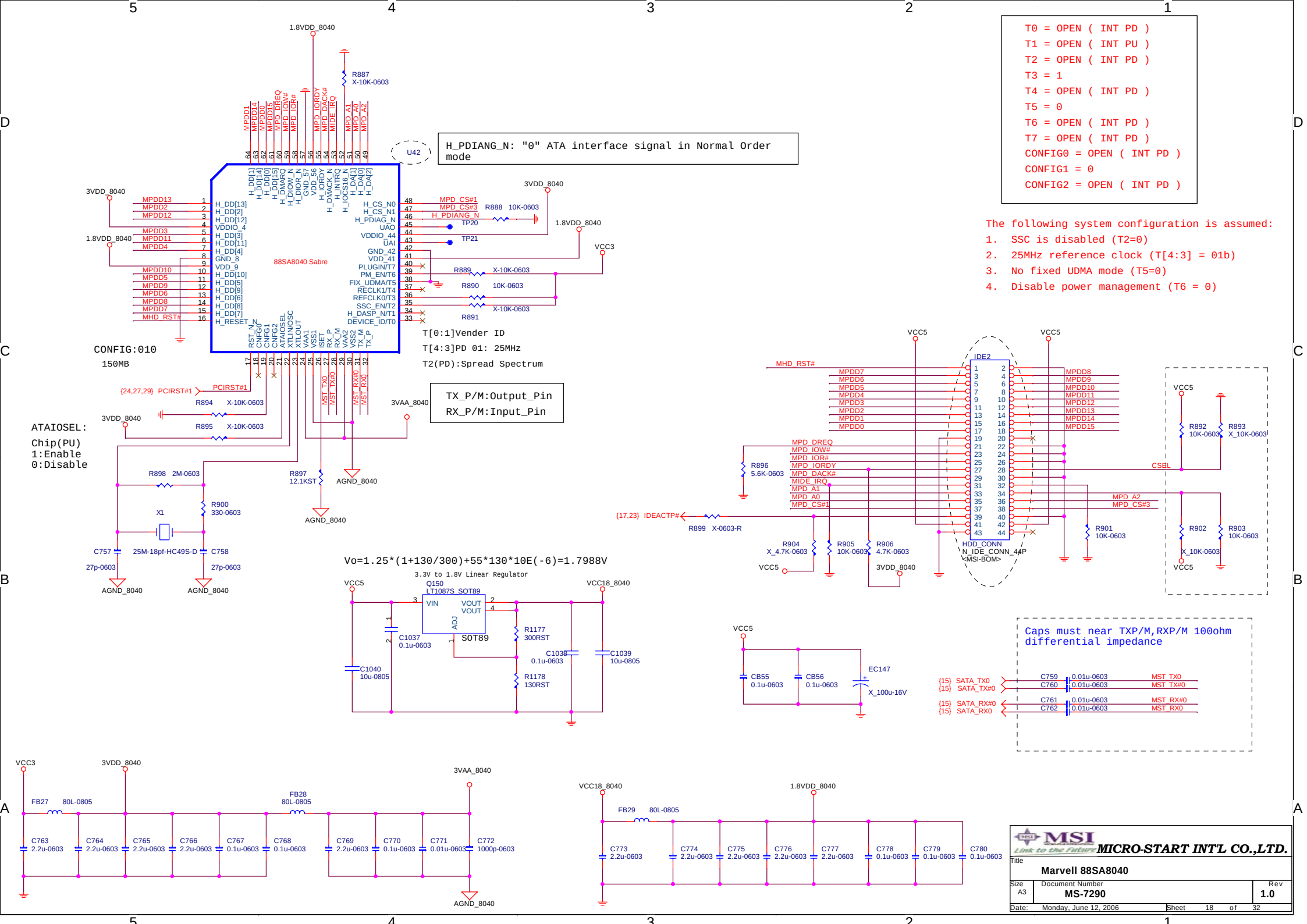




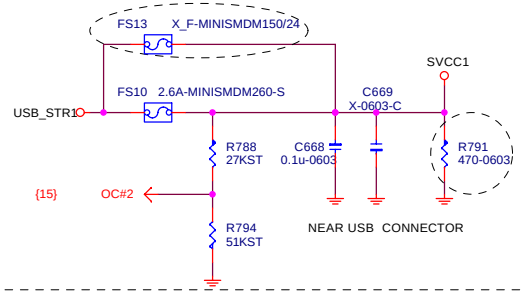
NO STUFF FOR 7290

MSI Link to the Future MICRO-START INT'L CO.,LTD.

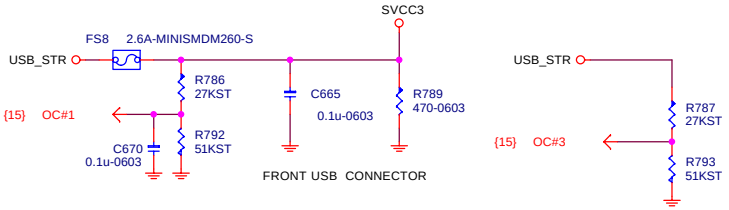
Title	IDE/FWH/AK2001	
Size: Custom	Document Number: MS-7290	Rev: 1.0
Date: Monday, June 12, 2006	Sheet 17 of 32	


T0 = OPEN (INT PD)
T1 = OPEN (INT PU)
T2 = OPEN (INT PD)
T3 = 1
T4 = OPEN (INT PD)
T5 = 0
T6 = OPEN (INT PD)
T7 = OPEN (INT PD)
CONFIG0 = OPEN (INT PD)
CONFIG1 = 0
CONFIG2 = OPEN (INT PD)
The following system configuration is assumed:
1. SSC is disabled (T2=0)
2. 25MHz reference clock (T[4:3] = 01b)
3. No fixed UDMA mode (T5=0)
4. Disable power management (T6 = 0)
H_PDIANG_N: "0" ATA interface signal in Normal Order mode
88SA8040 Sabre
U42
CONFIG:010
150MB
T[0:1]Vender ID
T[4:3]PD 01: 25MHz
T2(PD):Spread Spectrum
TX_P/M:Output_Pin
RX_P/M:Input_Pin
ATAIOSEL:
Chip(PU)
1:Enable
0:Disable
Vo=1.25*(1+130/300)+55*130*10E(-6)=1.7988V
3.3V to 1.8V Linear Regulator
Q150
LT1087S_SOT89
SOT89
IDE2
HDD_CONN_IDE_CONN_44P
<MSI-BOM>
Caps must near TXP/M,RXP/M 100ohm differential impedance
MICRO-START INT'L CO.,LTD.
Title
Marvell 88SA8040
Size A3
Document Number MS-7290
Rev 1.0
Date: Monday, June 12, 2006
Sheet 18 of 32

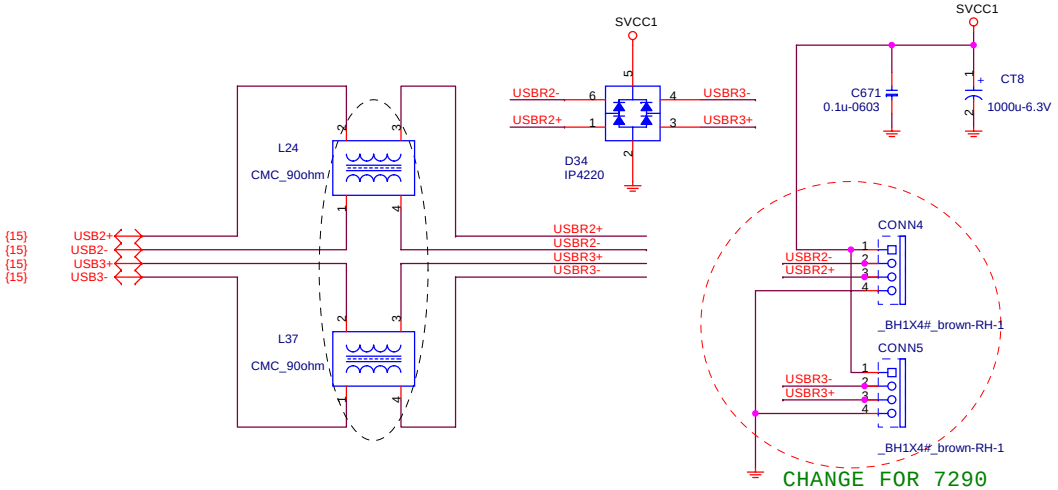
POWER CIRCUIT FOR USB PORT 0,1,2,3

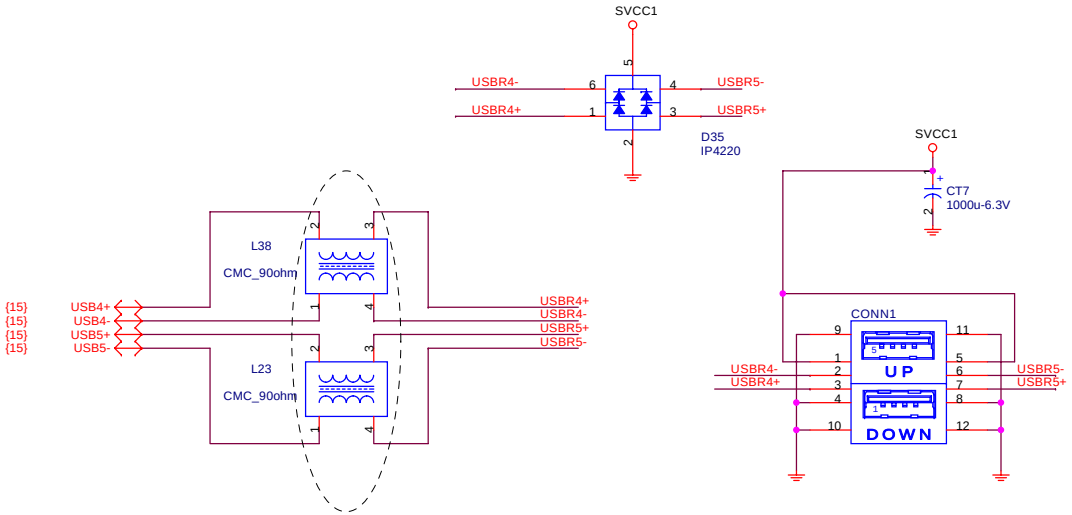


POWER CIRCUIT FOR USB PORT 4,5

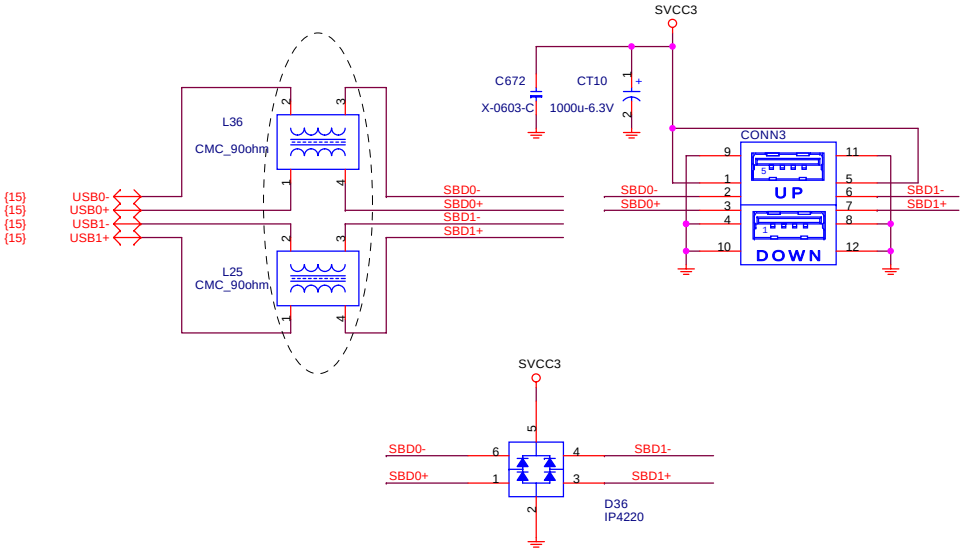


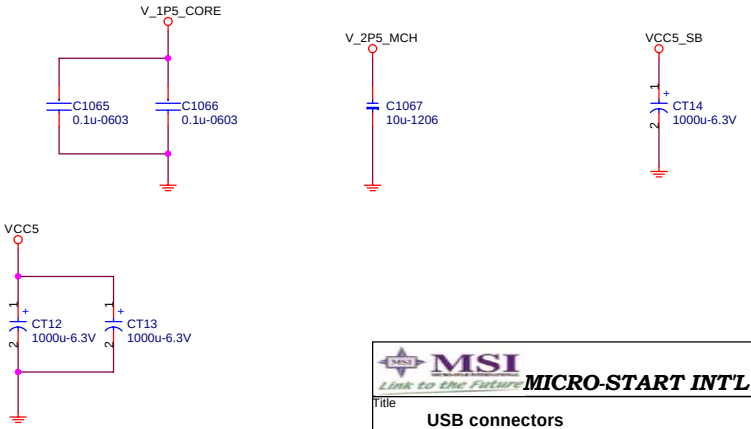
REAR PANEL USB CONNECTOR FOR USB PORT 0,1,2,3





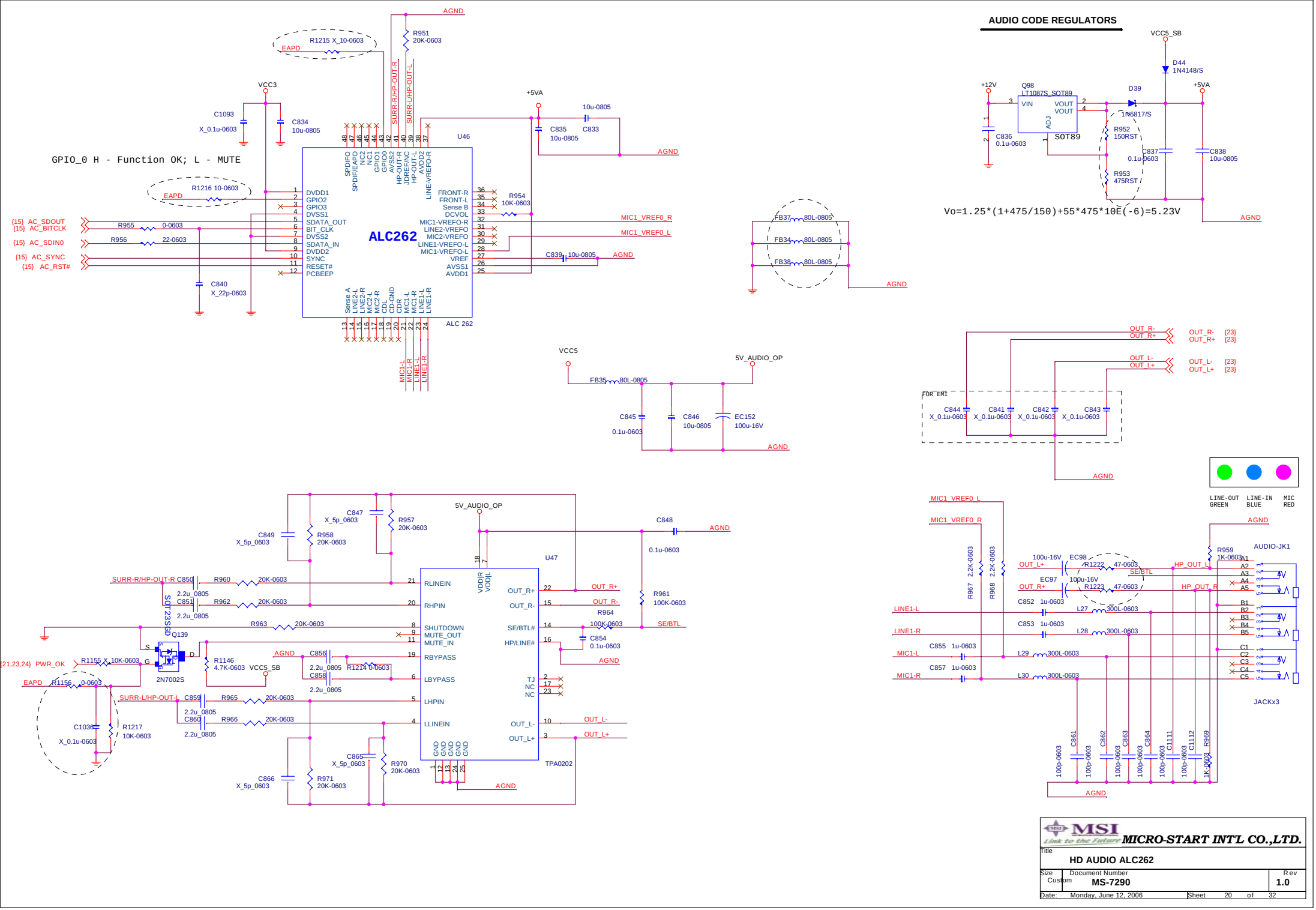
FRONT PANEL USB CONNECTOR FOR USB PORT 4,5

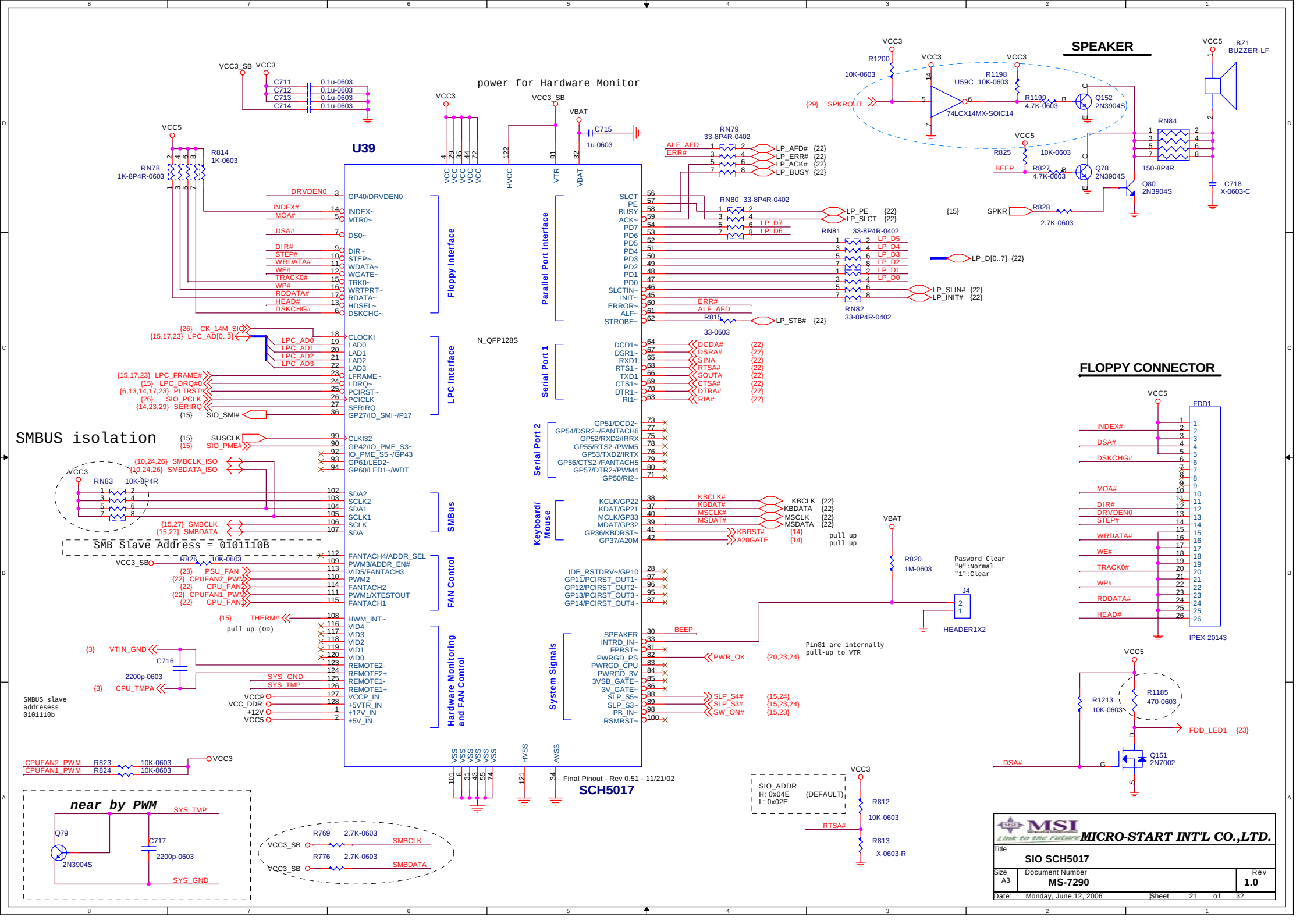




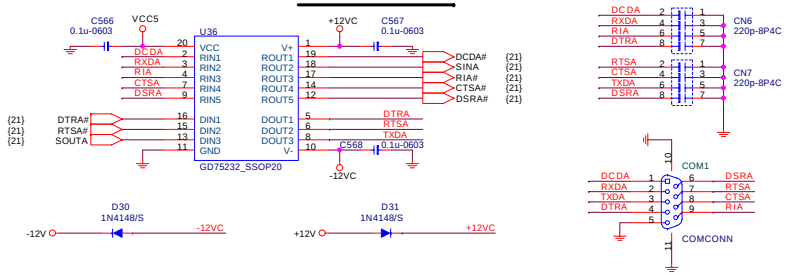
MICRO-START INT'L CO.,LTD.

Title	USB connectors	
Size: Custom	Document Number: MS-7290	Rev: 1.0
Date: Monday, June 12, 2006	Sheet 19 of 32	

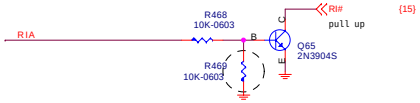

AUDIO CODE REGULATORS
ALC262
ALC 262
U46
U47
GPIO_0 H - Function OK; L - MUTE
Vo=1.25*(1+475/150)+55*475*10E(-6)=5.23V
TPA0202
SOT89
2N7002S
SST23SSD
JACKx3
AUDIO-JK1
LINE-OUT GREEN
LINE-IN BLUE
MIC RED
MICRO-START INT'L CO.,LTD.
HD AUDIO ALC262
MS-7290
Monday, June 12, 2006


power for Hardware Monitor
U39
N_QFP128S
Floppy Interface
LPC Interface
Serial Port 1
Serial Port 2
SMBus
Keyboard/ Mouse
FAN Control
Hardware Monitoring and FAN Control
Parallel Port Interface
System Signals
SMBUS isolation
SMB Slave Address = 0101110B
SMBUS slave addresess 0101110b
near by PWM
SPEAKER
FLOPPY CONNECTOR
Final Pinout - Rev 0.51 - 11/21/02
SCH5017
MICRO-START INT'L CO.,LTD.
SIO SCH5017
MS-7290
1.0
Monday, June 12, 2006

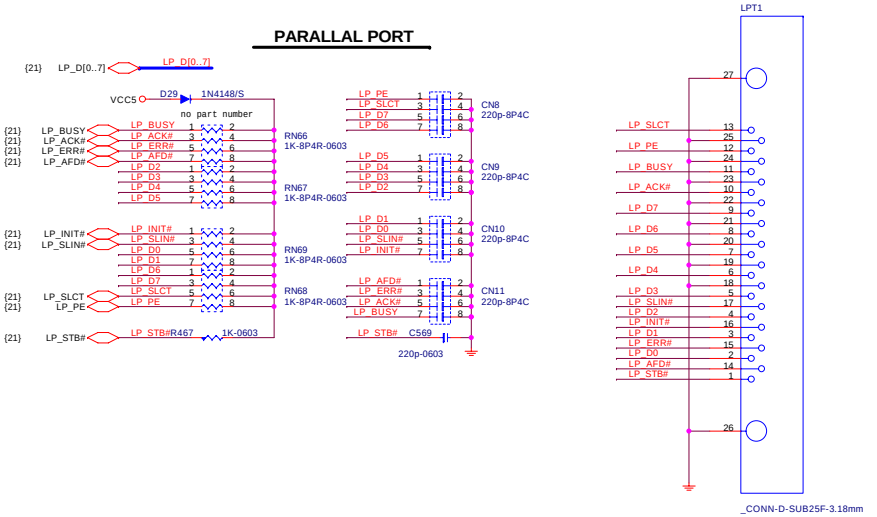
SERIAL PORT 1



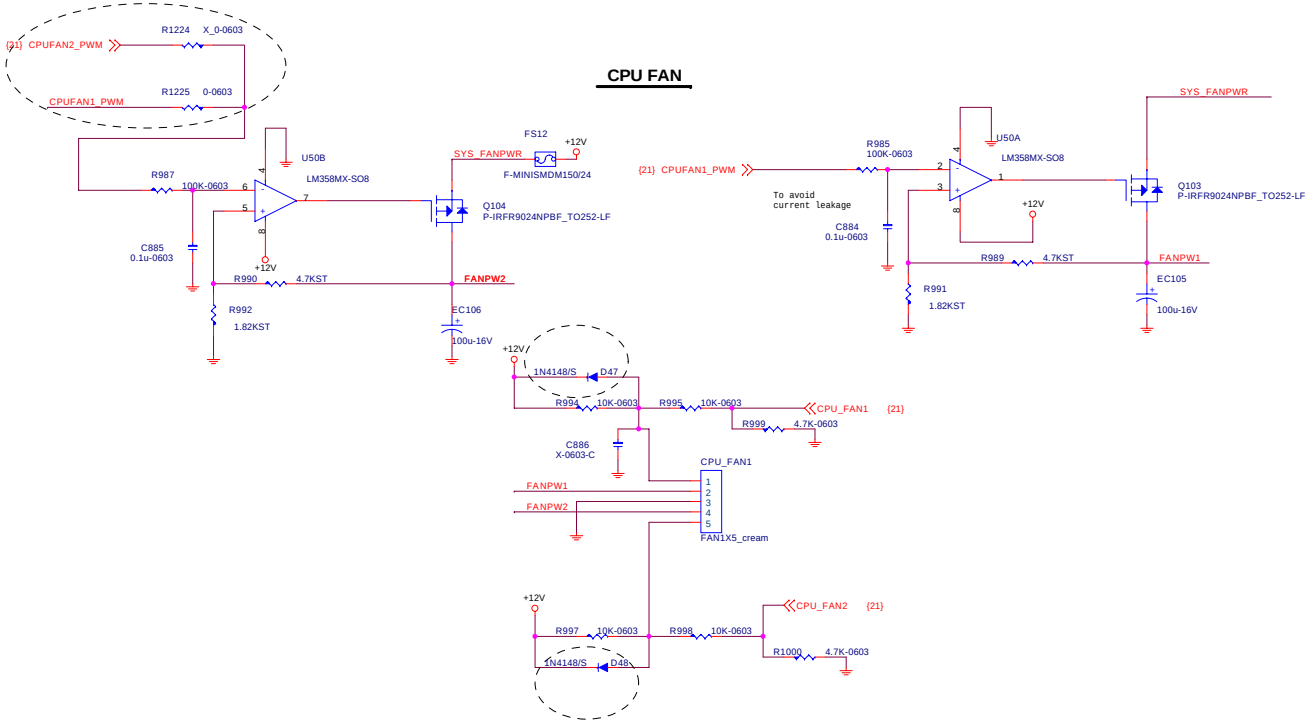
Wake On Modem Header



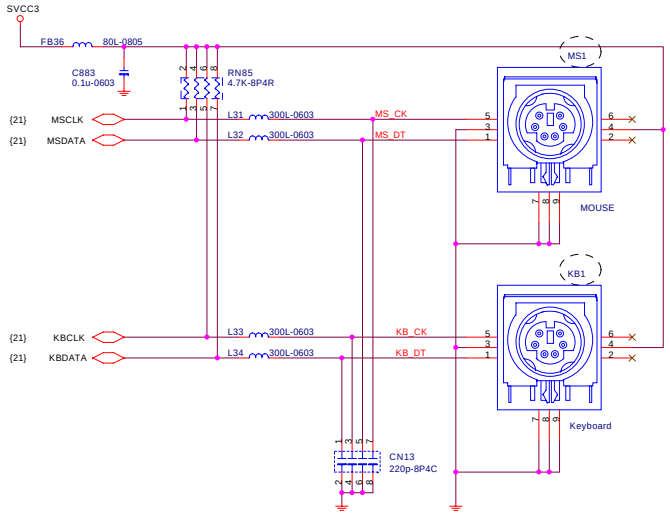
PARALLAL PORT



CPU FAN

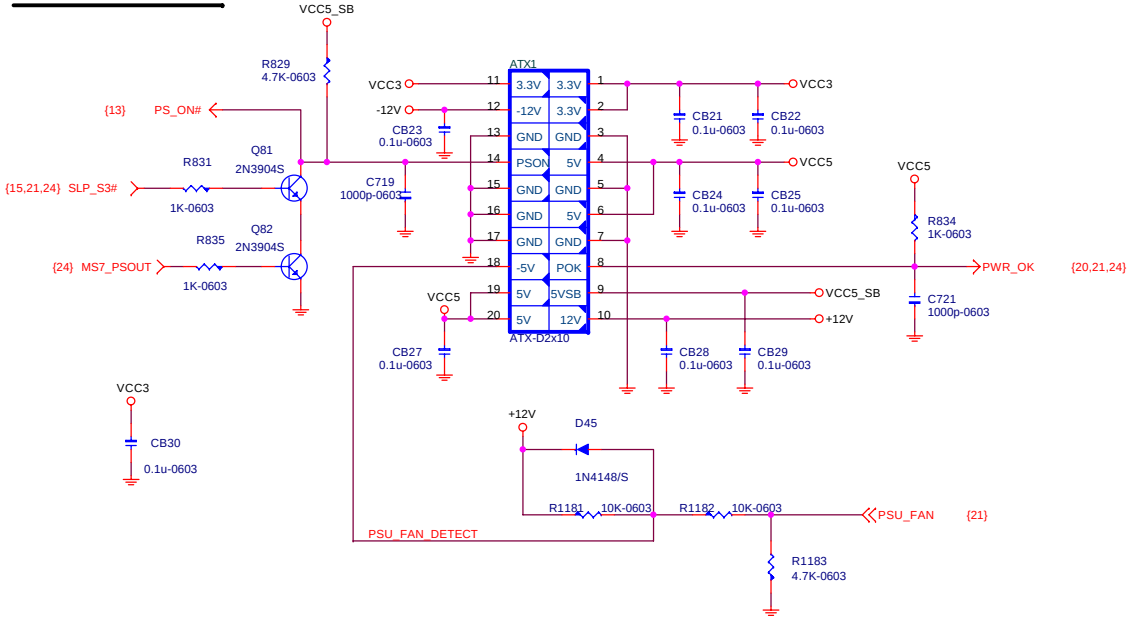


PS2 KEYBOARD & MOUSE CONNECTOR

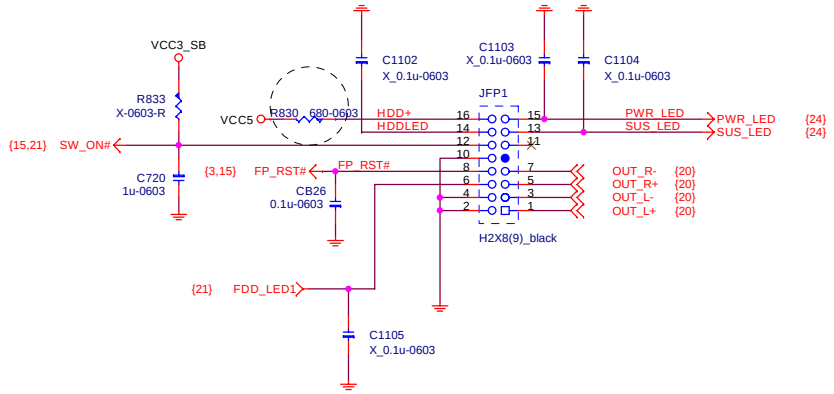


MSI Link for the Future	MICRO-START INT'L CO.,LTD.	
Title: LPT/COM/FAN		
Size: C	Document Number: MS-7290	Rev: 1.0
Date: Monday, June 12, 2006	Sheet 22 of 32	

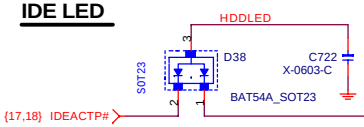
ATX CONNECTOR



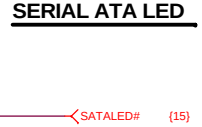
Front Panel

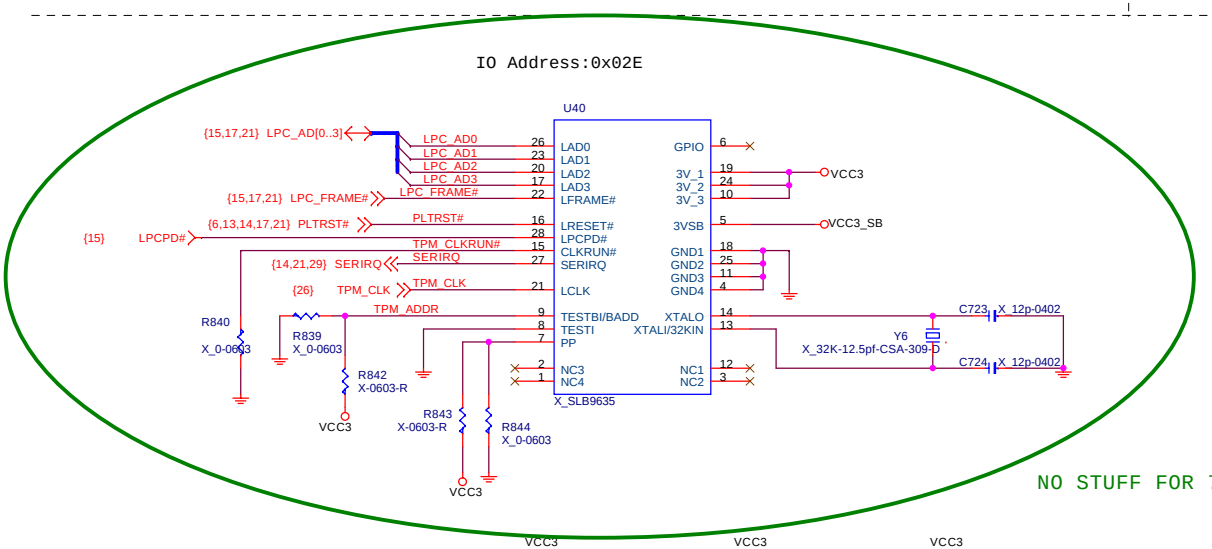


IDE LED

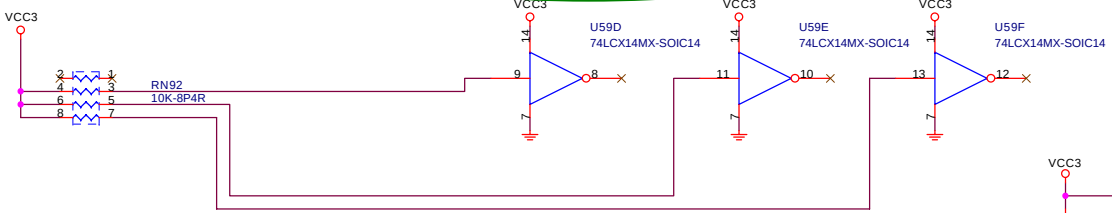


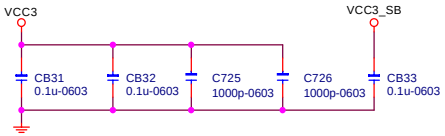
SERIAL ATA LED

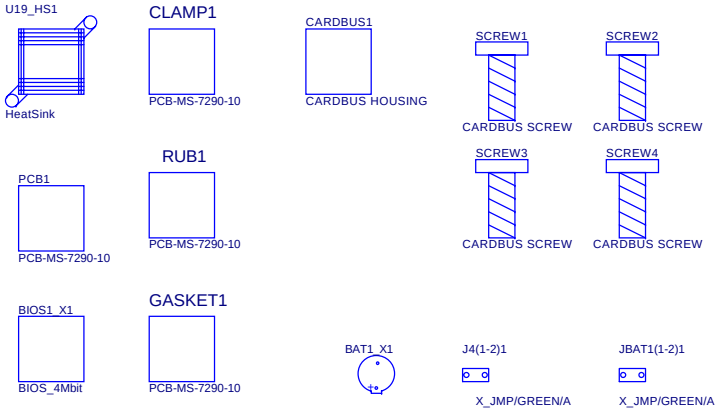




NO STUFF FOR 7290







MSI MICRO-START INT'L CO.,LTD.		
Title: ATX/Front Panel/TPM		
Size: Custom	Document Number: MS-7290	Rev: 1.0
Date: Monday, June 12, 2006	Sheet 23 of 32	

ACPI Controller

3VSB MODE SELECT

3VSB MODE	3VDLDEC#
SINGLE MOSFET	PULL HIGH
DUAL MOSFET	PULL LOW

VDIMM LINEAR OR PWM SELECT

VDIMM MODE	EXTRAM
LINEAR REGULATOR	PULL LOW
PWM REGULATOR	PULL HIGH

DDR AND DDR II VOLT SELECT

DDRTYPE	VDIMM
PULL LOW	2.5V
PULL HIGH	1.8V

1.5V POWER(Height limit 9mm)

22.87A
NB:14A
SB:1A
V_FSB_VTT:6.2A
SB:1.31A

8.58A
CHOKE3 CH-1.2U18A-LF
12.5mm
Cap ripp=10.48A
CH-2.2U25A_D
CHOKE4
14mm
8+1mm
560uF Ripple Current = 4.7A
CLOSE TO CHIP
Iocp=72uA*RISEN/RdsON
40A=72uA*RISEN/8.6m ohm RISEN=4.7k ohm

1.05V POWER

1.31A
15+1mm

5V DUAL Power

FRONT USB
Rear USB

DDR VTT Power

THIS PIN IS OPEN DRAIN OUTPUT
Close to MS6+
Wide Trace
SMT 3.8mm
CHARGE PUMP VOLTAGE OUTPUT

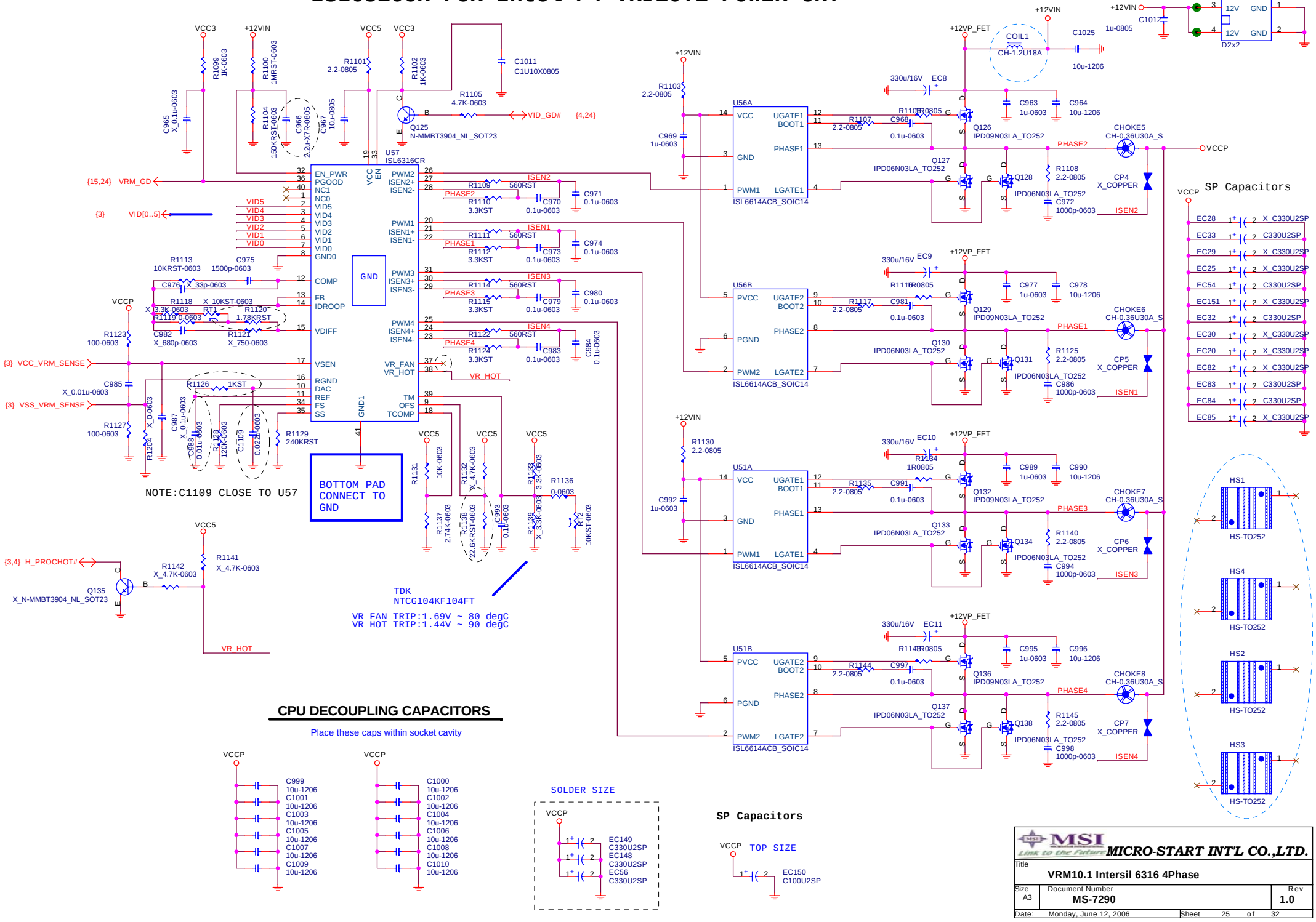
17.46A
VCC_DDR 9.9A = 4A(NB)+4.7A(DDR2*2)+1.2A(VTT)

Iocp=72uA*RISEN/RdsON 20A=72uA*RISEN/8.6m ohm RISEN=2.38k ohm

MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title	MS7 ACPI controller		
Size: Custom	Document Number: MS-7290		Rev: 1.0
Date: Monday, June 12, 2006	Sheet 24 of 32		

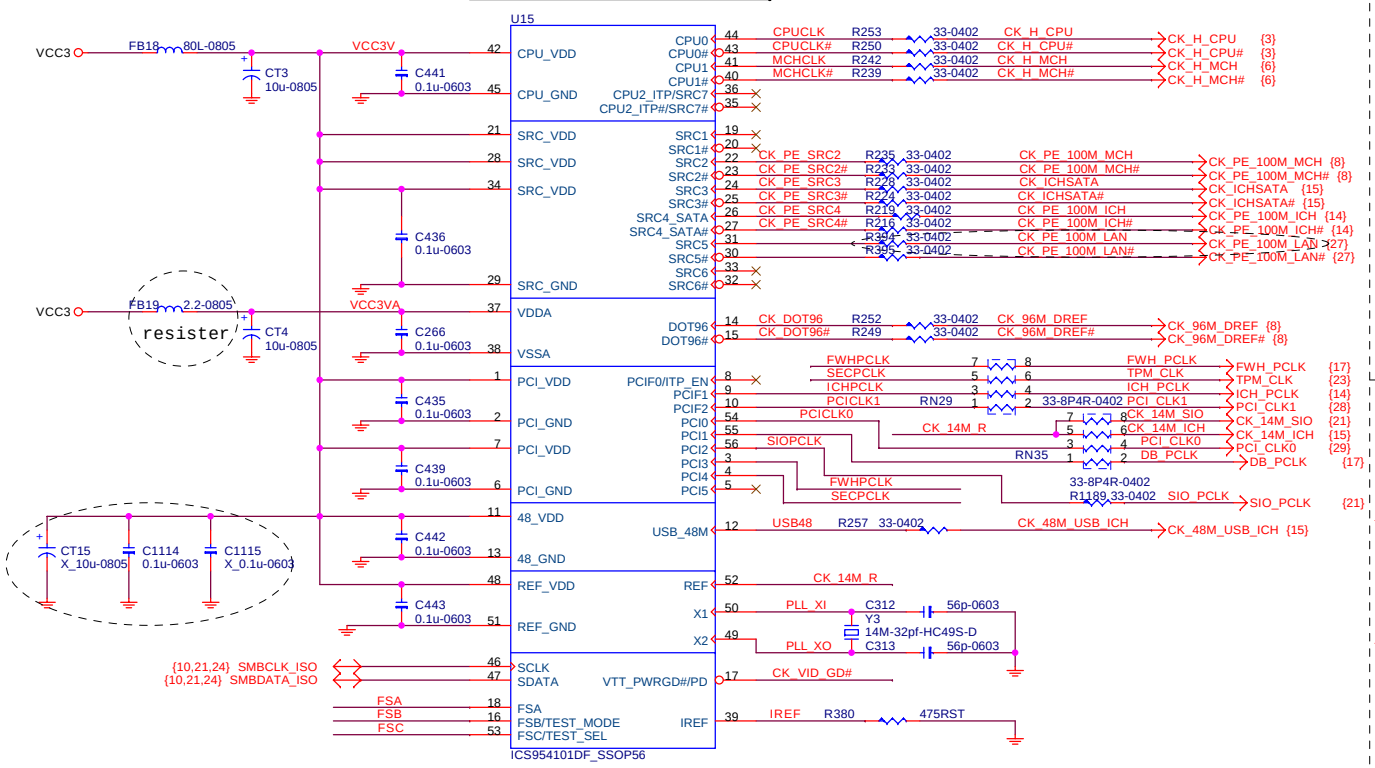
ISL6316CR FOR Intel P4 VRD10.1 POWER CKT

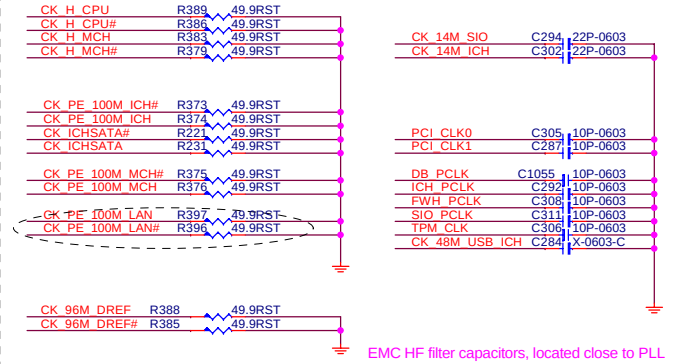


MSI Link to the Future	MICRO-START INT'L CO.,LTD.		
Title	VRM10.1 Intersil 6316 4Phase		
Size A3	Document Number MS-7290		Rev 1.0
Date: Monday, June 12, 2006	Sheet 25 of 32		

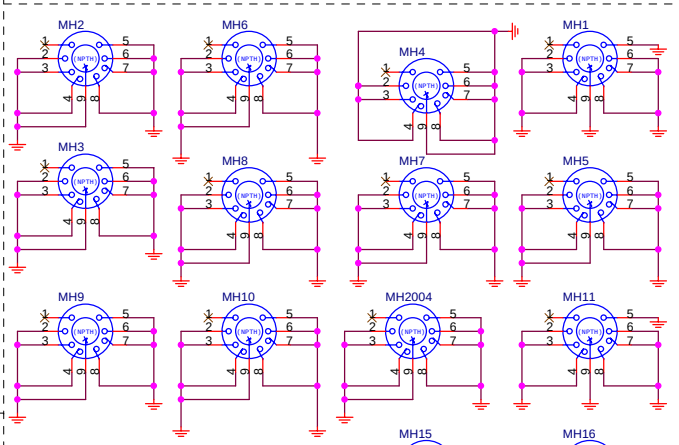
Clock Generator - ICS954101

Trace length less than 0.5inchs

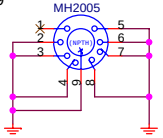




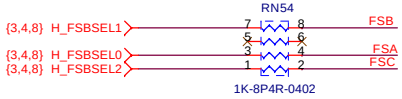
EMC HF filter capacitors, located close to PLL



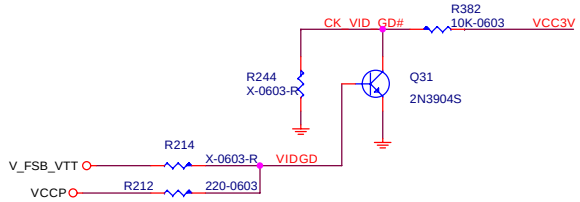
for power cable holder and FP:
HOLES315D189



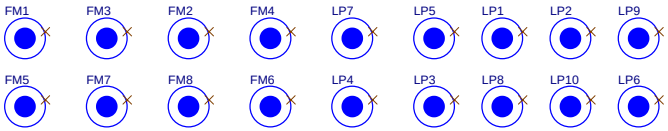
BSEL[0..2] Level Shift



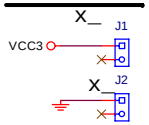
Clock Generator VTT Power Down Block



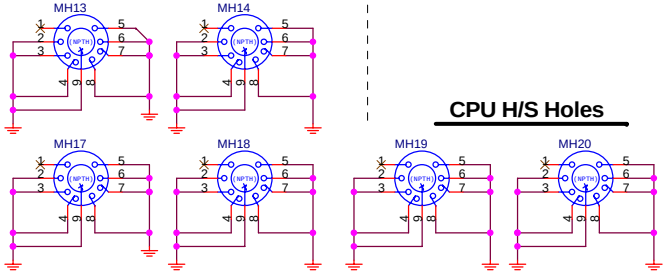
Optics Orientation Holes



Simulation



CPU H/S Holes



MICRO-START INT'L CO.,LTD.

Title: Clock Generator

Size: Custom | Document Number: MS-7290 | Rev: 1.0

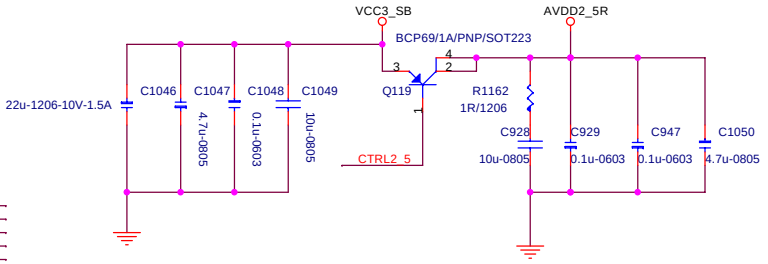
Date: Monday, June 12, 2006 | Sheet 26 of 32

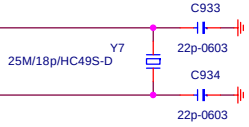
Tekoa(82573L)

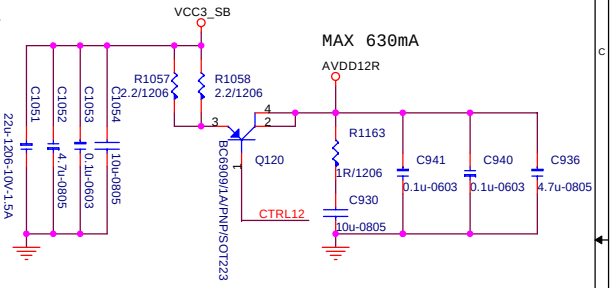
CHANGE TO 82573L FOR 7290

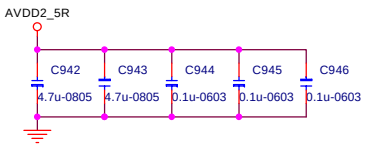
LAN VOLTAGE REGULATION

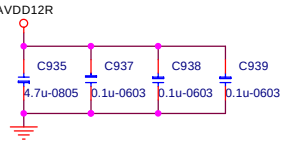
MAX 301mA

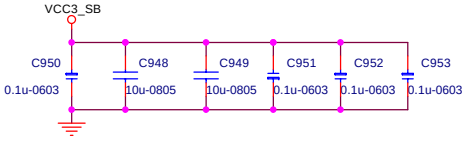


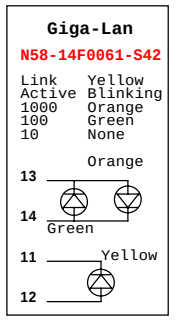


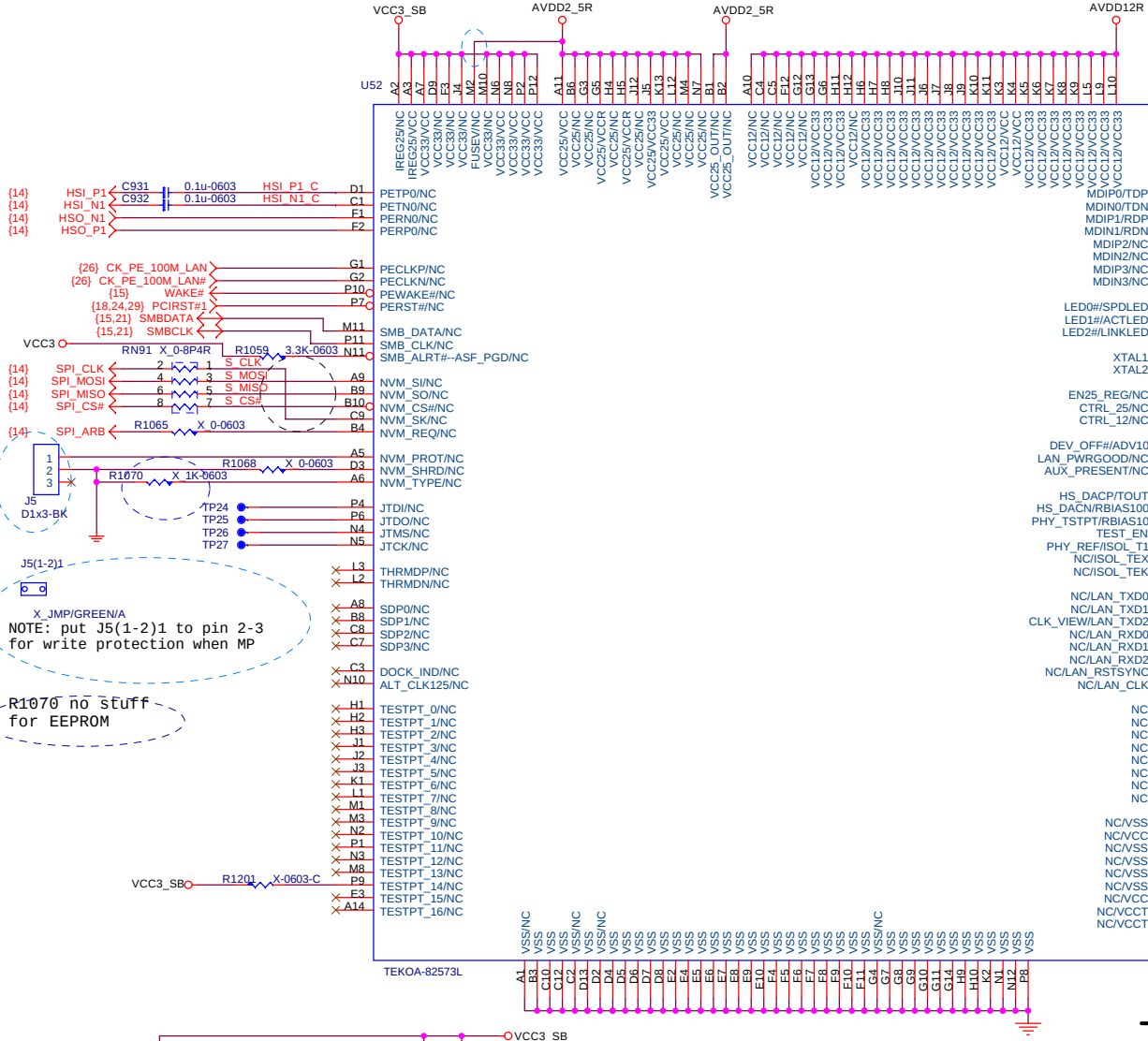


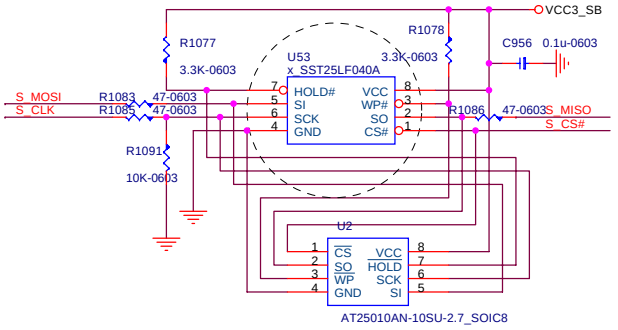




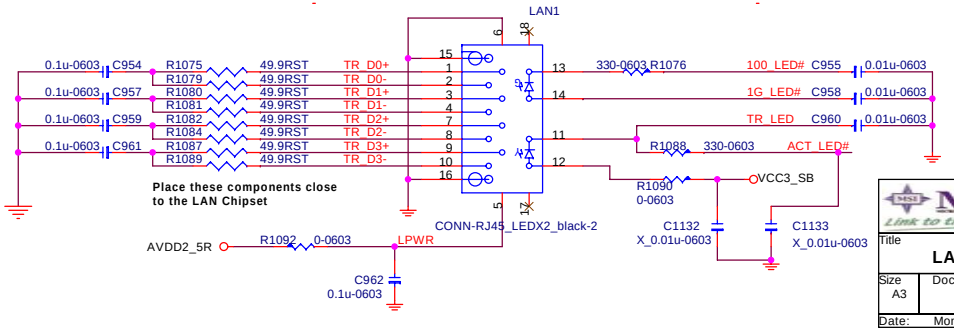








LAN CONNECTOR



MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title	LAN Intel Tekoa 82573L	
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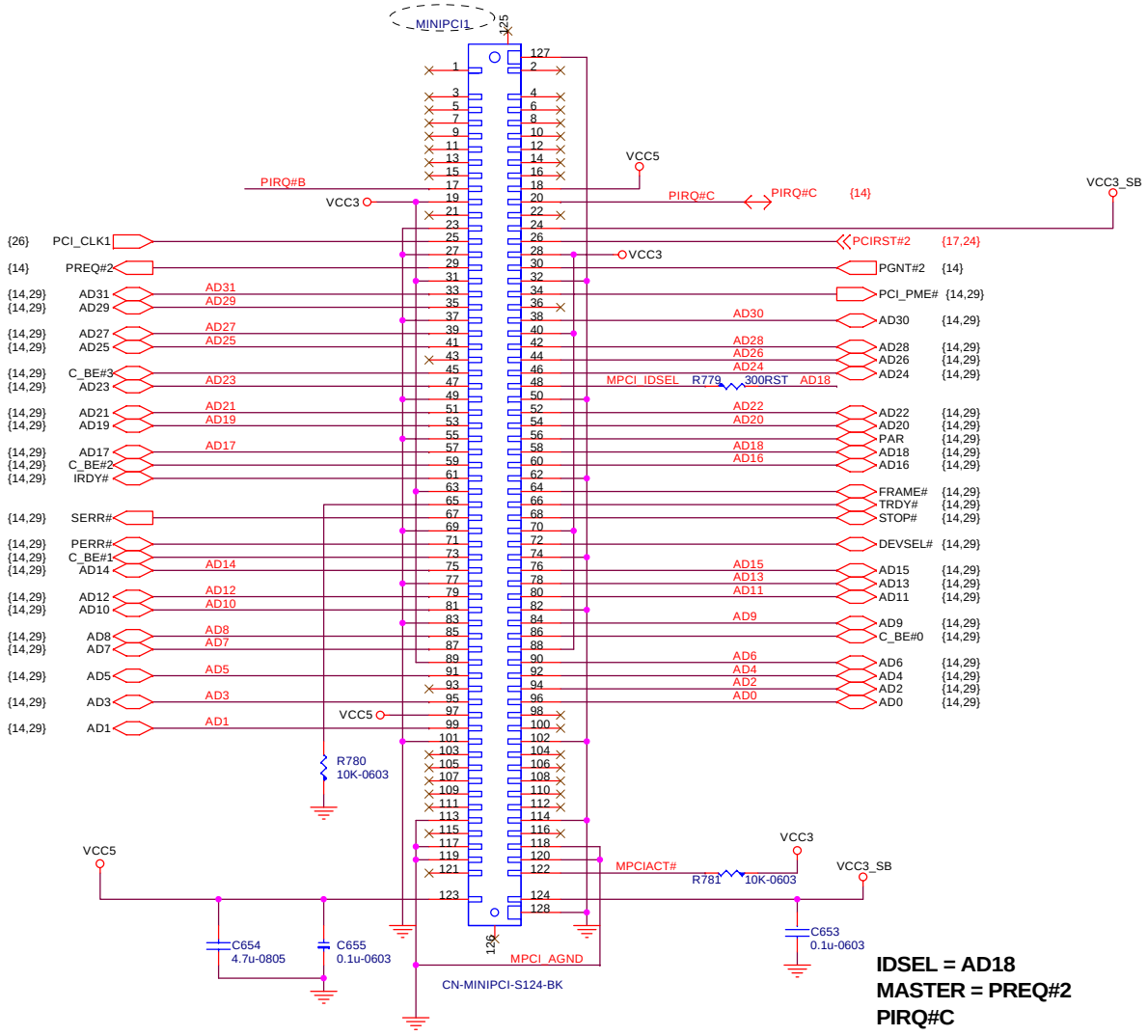
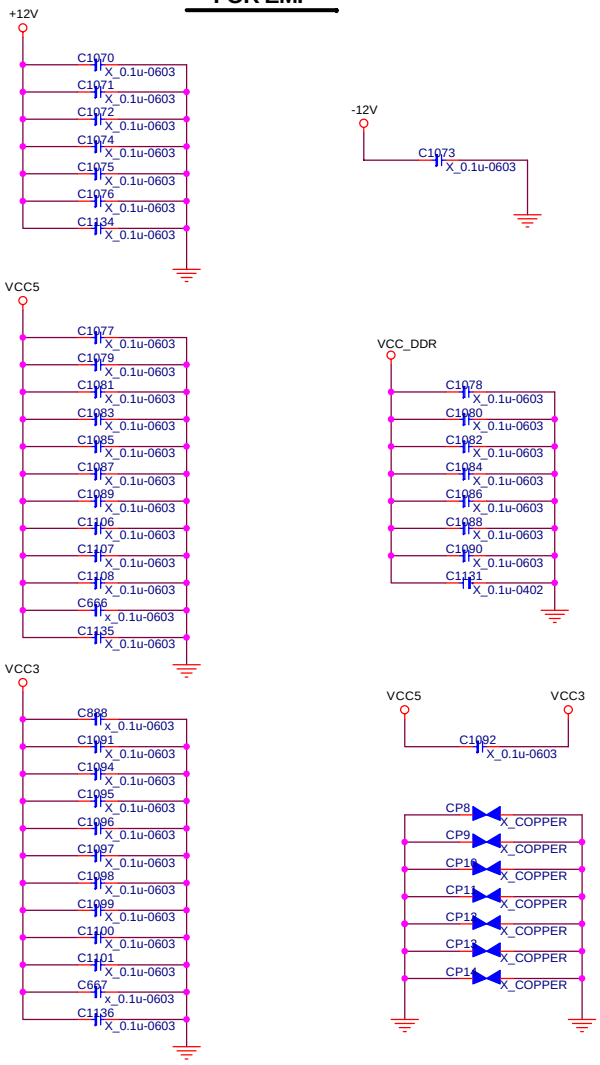
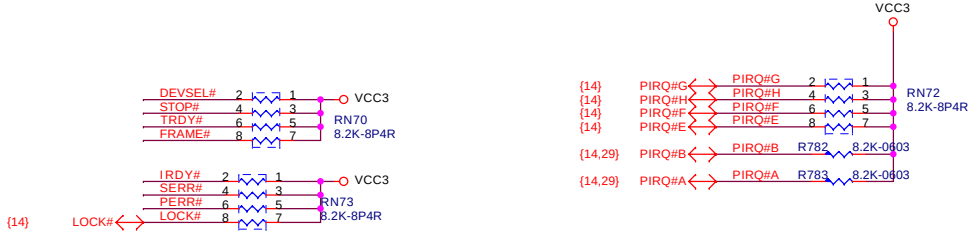


IDSEL = AD18
MASTER = PREQ#2
PIRQ#C

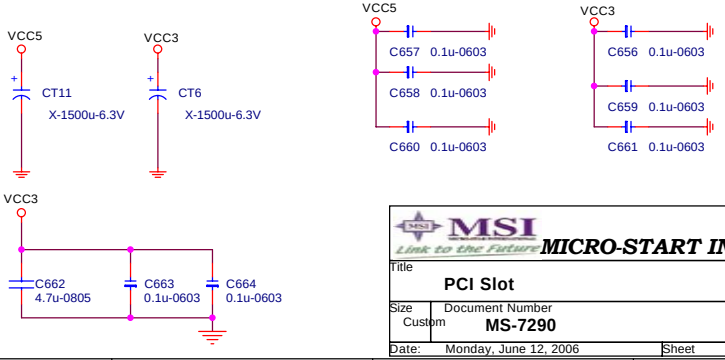
FOR EMI



PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS



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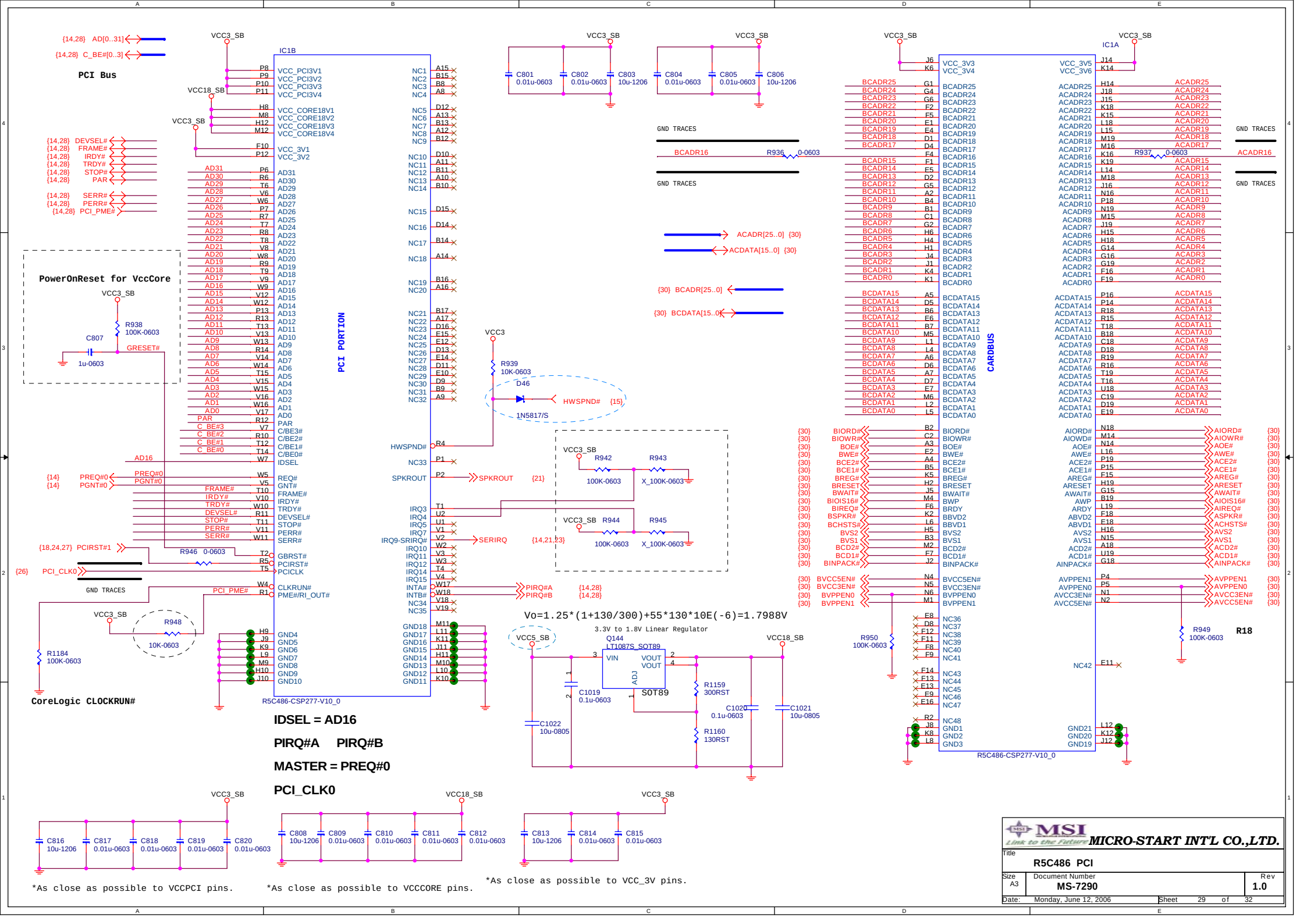
PCI Bus
IC1B
PCI PORTION
R5C486-CSP277-V10_0
PowerOnReset for VccCore
CoreLogic CLOCKRUN#
IDSEL = AD16
PIRQ#A PIRQ#B
MASTER = PREQ#0
PCI_CLK0
Vo=1.25*(1+130/300)+55*130*10E(-6)=1.7988V
3.3V to 1.8V Linear Regulator
LT1087S_SOT89
IC1A
CARDBUS
R5C486-CSP277-V10_0
GND TRACES
*As close as possible to VCCPCI pins.
*As close as possible to VCCCORE pins.
*As close as possible to VCC_3V pins.
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R5C486 PCI
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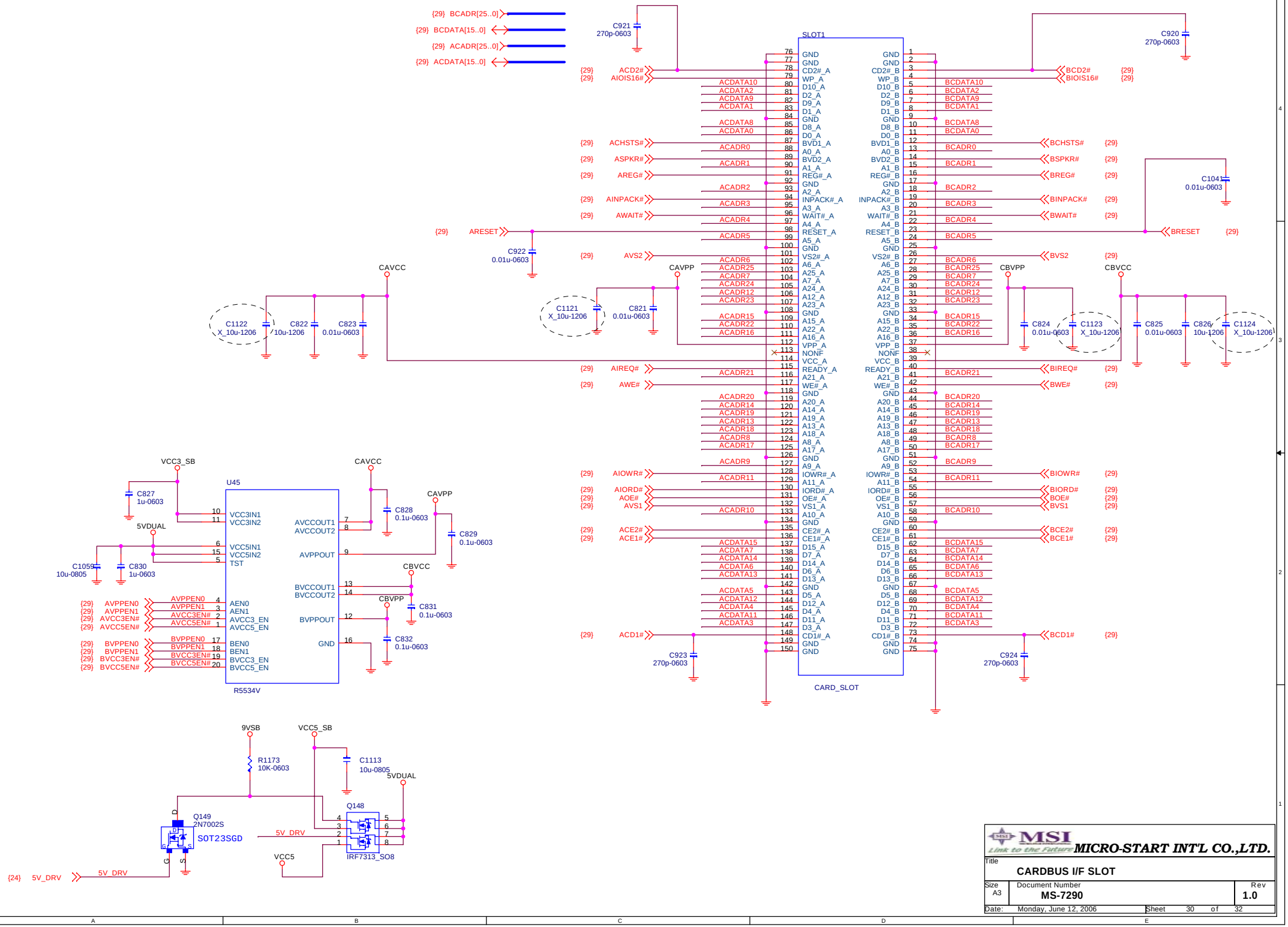
{29} BCADR[25..0]
{29} BCDATA[15..0]
{29} ACADR[25..0]
{29} ACDATA[15..0]
SLOT1
CARD_SLOT
C921 270p-0603
C920 270p-0603
C922 0.01u-0603
C923 270p-0603
C924 270p-0603
C1041 0.01u-0603
CAVCC
CAVPP
CBVPP
CBVCC
C1122 X_10u-1206
C822 10u-1206
C823 0.01u-0603
C1121 X_10u-1206
C821 0.01u-0603
C824 0.01u-0603
C1123 X_10u-1206
C825 0.01u-0603
C826 10u-1206
C1124 X_10u-1206
U45
R5534V
VCC3_SB
5VDUAL
C827 1u-0603
C1059 10u-0805
C830 1u-0603
C828 0.1u-0603
C829 0.1u-0603
C831 0.1u-0603
C832 0.1u-0603
9VSB
VCC5_SB
R1173 10K-0603
C1113 10u-0805
Q149 2N7002S
SOT23SGD
Q148
IRF7313_SO8
5V_DRV
VCC5
{24} 5V_DRV
MSI
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ICH7

GPIO	Alt Func	Pin	I/O/NC	Power	PU	SMI	Tol	Default	Signal Name
GPIO[0]	BM_BUSY#	AB18	I/O	Vcc3p3	N	Y	3.3	Input	strapped hi
GPIO[1]	PCIREQ[5]#	C8	I/O	V5REF	N	Y	5	Input	PREQ#5
GPIO[2]	PIRQE#	G8	I/OD	V5REF	N	Y	5	Input	PIRQ#E
GPIO[3]	PIRQF#	F7	I/OD	V5REF	N	Y	5	Input	PIRQ#F
GPIO[4]	PIRQG#	F8	I/OD	V5REF	N	Y	5	Input	PIRQ#G
GPIO[5]	PIRQH#	G7	I/OD	V5REF	N	Y	5	Input	PIRQ#H
GPIO[6]	unmuxed	AC21	I/O	Vcc3p3	N	Y	3.3	Input	PANEL_DETECT
GPIO[7]	unmuxed	AC18	I/O	Vcc3p3	N	Y	3.3	Input	SIO_SMI#
GPIO[8]	unmuxed	E21	I/O	VccSus3p3	N	Y	3.3	Input	strapped hi
GPIO[9]	unmuxed	E20	I/O	VccSus3p3	N	Y	3.3	Input	strapped hi
GPIO[10]	unmuxed	A20	I/O	VccSus3p3	N	Y	3.3	Input	strapped hi
GPIO[11]	SMBALERT#	B23	I/O	VccSus3p3	N	Y	3.3	Input	strapped hi
GPIO[12]	unmuxed	F19	I/O	VccSus3p3	N	Y	3.3	Input	SIO_PME#
GPIO[13]	unmuxed	E19	I/O	VccSus3p3	N	Y	3.3	Input	strapped hi
GPIO[14]	unmuxed	R4	I/O	VccSus3p3	N	Y	3.3	Input	strapped hi
GPIO[15]	unmuxed	E22	I/O	VccSus3p3	N	Y	3.3	Input	strapped hi
GPIO[16]	unmuxed	AC22	I/O	Vcc3p3	N	N	3.3	0	NC
GPIO[17]	PCIGNT[5]#	D8	I/O	Vcc3p3	N	N	3.3	N/A	NC
GPIO[18]	unmuxed	AC20	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[19]	SATA1GP	AH18	I/O	Vcc3p3	N	N	3.3	Input	strapped hi
GPIO[20]	unmuxed	AF21	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[21]	SATA0GP	AF19	I/O	Vcc3p3	N	N	3.3	Input	strapped hi
GPIO[22]	PCIREQ[4]#	A13	I/O	Vcc3p3	N	N	3.3	Input	PREQ#4
GPIO[23]	LDRQ1#	AA5	I/O	Vcc3p3	N	N	3.3	Input	strapped hi
GPIO[24]	unmuxed	R3	I/O	VccSus3p3	N	N	3.3	1	LAN_DISABLE#
GPIO[25]	unmuxed	D20	I/O	VccSus3p3	Y	N	3.3	1	HWSPND#
GPIO[26]	unmuxed	A21	I/O	VccSus3p3	N	N	3.3	0	LCD_S1_ENA
GPIO[27]	unmuxed	B21	I/O	VccSus3p3	N	N	3.3	0	NC
GPIO[28]	unmuxed	E23	I/O	VccSus3p3	N	N	3.3	0	NC
GPIO[29]	OC5#	C3	I/O	VccSus3p3	N	N	3.3	Input	OC#2
GPIO[30]	OC6#	A2	I/O	VccSus3p3	N	N	3.3	Input	OC#3
GPIO[31]	OC7#	B3	I/O	VccSus3p3	N	N	3.3	Input	OC#3
GPIO[32]	unmuxed	AG18	I/O	Vcc3p3	N	N	3.3	1	BIOS_WP#
GPIO[33]	unmuxed	AC19	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[34]	unmuxed	U2	I/O	Vcc3p3	N	N	3.3	0	NC
GPIO[35]	unmuxed	AD21	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[36]	SATA2GP	AH19	I/O	Vcc3p3	N	N	3.3	Input	strapped hi
GPIO[37]	SATA3GP	AE19	I/O	Vcc3p3	N	N	3.3	Input	strapped hi
GPIO[38]	unmuxed	AD20	I/O	Vcc3p3	N	N	3.3	Input	strapped hi
GPIO[39]	unmuxed	AE20	I/O	Vcc3p3	N	N	3.3	Input	strapped hi
GPIO[48]	GNT4#	A14	I/O	Vcc3p3	N	N	3.3	N/A	NC
GPIO[49]	CPUPWRGD	AG24	I/O	V_CPU_IO	N	N	CPU	N/A	H_PWRGD

Following are the GPIOs that need to be terminated roperly if not used: GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3_3 if unused. GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3_3 if unused.

GPI[15:0] can be configured to cause a SMI# or SCI. Note that a GPI can be routed to either an SMI# or an SCI, but not both.

SIO SCH5017

PIN NAME	PIN#	USAGE	Input/Output
GP42	90	SIO_PME#	OUTPUT
GP27	36	SIO_SMI#	OUTPUT
INTRD_IN-	33	CLEAR PASSWORD	INPUT

SMBus DISTRIBUTION

SMBus	Power	Load
SMBCLK	VCC3_SB	ICH7, LAN
SMBCLK_ISO	VCC3	DIMM, CLK GEN, SIO, MS7

FWH

Note: FWH GPs should only be used for static options, do not put dynamic nets on these

GPIO	Pin#	Power	Tol	Signal Name
FPGI[0]	6	Main	3.3	ATADET0
FPGI[1]	5	Main	3.3	pull-down
FPGI[2]	4	Main	3.3	pull-down
FPGI[3]	3	Main	3.3	pull-down
FPGI[4]	30	Main	3.3	pull-down

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
Ricoh R5C486	PIRQ#A PIRQ#B	PREQ#0 PGNT#0	AD16	PCI_CLK0
mini-PCI	PIRQ#C PIRQ#B	PREQ#2 PGNT#2	AD18	PCI_CLK1

PCI_RST# DISTRIBUTION

SOURCE	PCIRST#	LOAD
ICH7	PCIRST_ICH6#	MS7
	PLTRST#	NB, SIO, FWH, TPM, CH7308A
MS7	PCIRST#1	LAN, CARD_BUS,MARVELL 88SA8040
	PCIRST#2	mini-PCI,AK2001,
	HD_RST#	IDE
NB	H_CPURST#	CPU

DDRII DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	A0H	MCLK_A0/MCLK_A#0 MCLK_A1/MCLK_A#1 MCLK_A2/MCLK_A#2
DIMM 2	A4H	MCLK_B0/MCLK_B#0 MCLK_B1/MCLK_B#1 MCLK_B2/MCLK_B#2

JUMPER SETTING

JBAT1	(1-2)NORMAL	(2-3)CLEAR

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Change Note

Ver:0A

(1) . page 23 : change R830 vaul from 470 ohm to 1K

(2) . page 24 :

1 . change R355 vaul from 470 ohm to 1K

2 . change EC57 vaul from 1000uf to 1800uf

3 . Remove Q162,Q163,C417 and Add R1248,R1249 for USB power rise after PWR_OK

Ver:01S

(3) . page 23 : change R830 vaul from 1K to 680ohm

(4) . page 24 : change R355 vaul from 1K to 680ohm

MICRO-START INT'L CO.,LTD.

Title: Change Note		
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