Compal Confidential

NAV51 Schematics Document

Intel Pineview Processor with Tigerpoint + DDRII

2010-03-31

REV: 1.0

Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.		
Title: Cover Page		
Size: B	Document Number: NAV51 LA-6311P	Rev: 1.0
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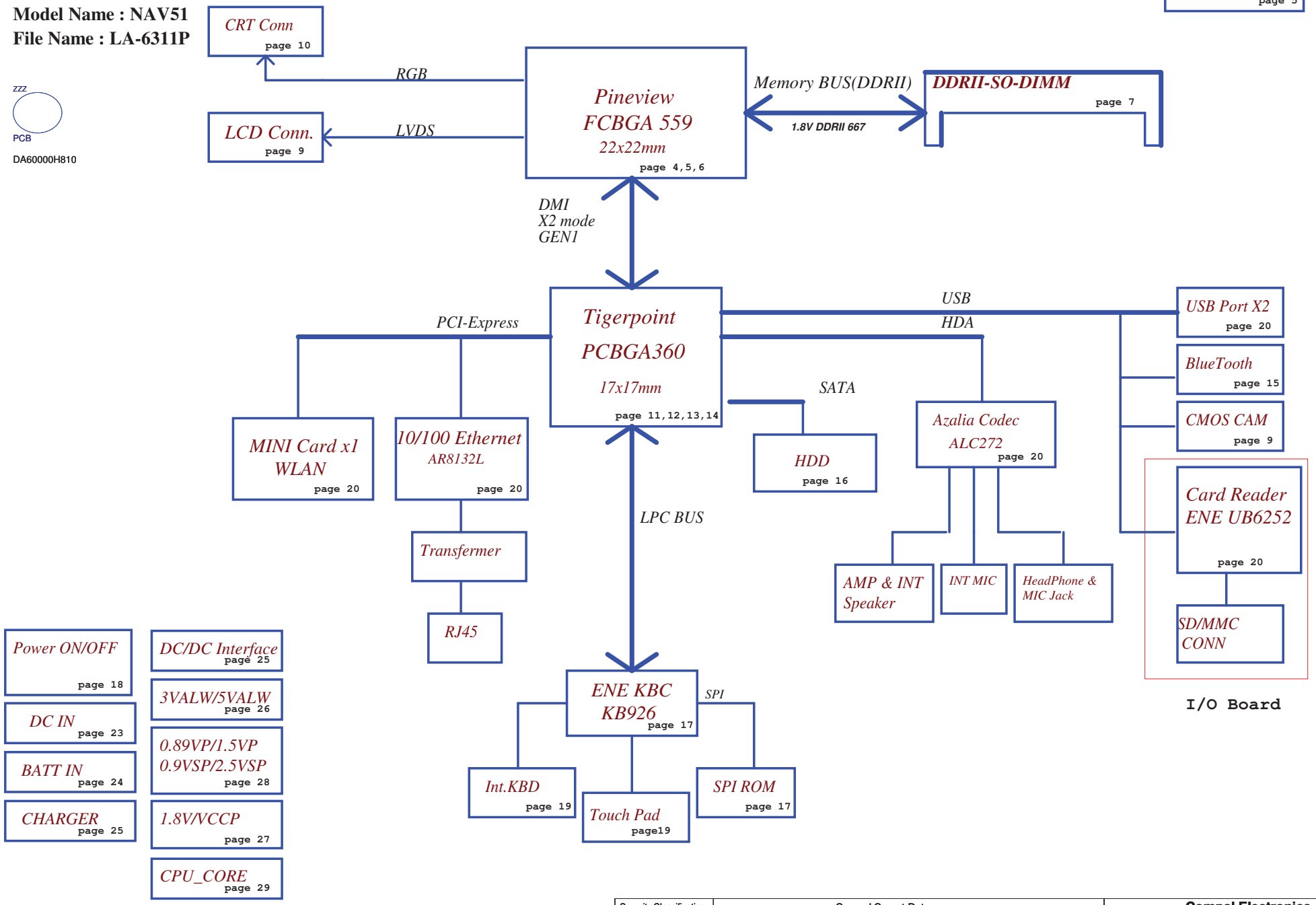
Model Name : NAV51
File Name : LA-6311P

ZZZ
PCB
DA60000H810



Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.			
Title	Block Diagrams		
Size B	Document Number	NAV51 LA-6311P	Rev 1.0
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+VCCP	VCCP switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+0.89V	Graphic core power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table(Page 17)

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0(EVT)	0	0 V	0 V	0 V
1(DVT)	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2(PVT)	18K +/- 5%	0.436 V	0.503 V	0.538 V
3(MP)	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	
3	
4	
5	
6	
7	

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ

No PCI Device

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
EMC1402	100_1100

Tiger Point SM Bus address

Device	Address
Clock Generator (SLG8SP556VTR)	1101 001Xb
DDR DIMMA	1010 000Xb

USB table

EHCI1	UHCI1	Port0	MB USB Conn1.
		Port1	MB USB Conn2.
	UHCI2	Port2	
		Port3	CMOS
	UHCI3	Port4	Card Reader
		Port5	
EHCI2	UHCI4	Port6	BT
		Port7	WLAN
	UHCI5	Port8	
		Port9	
	UHCI6	Port10	
		Port11	

PCIE table

PCIE port1	LAN
PCIE port2	Wireless Card
PCIE port3	
PCIE port4	
PCIE port5	
PCIE port6	

SATA table

SATA port0	HDD
SATA port1	
SATA port2	
SATA port3	
SATA port4	
SATA port5	

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Title	Notes List		
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PINEVIEW_M

U71A

REV = 1.1

DMI_RX0_C
DMI_RX#0_C
DMI_RX1_C
DMI_RX#1_C
F3 DMI_RXP_0
F2 DMI_RXN_0
H4 DMI_RXP_1
G4 DMI_RXN_1

DMI_TXP_0 G2
DMI_TXN_0 G1
DMI_TXP_1 H3
DMI_TXN_1 J2

DMI_TX0 (12)
DMI_TX#0 (12)
DMI_TX1 (12)
DMI_TX#1 (12)

DMI

(8) CLK_CPU_EXP#
(8) CLK_CPU_EXP
N7 EXP_CLKINN
N6 EXP_CLKINP

EXP_RCOMPO L10
EXP_ICOMPI L9
EXP_RBIAS L8

R162
R203 49.9_0402_1%
750_0402_1%

R10 EXP_TCLKINN
R9 EXP_TCLKINP
N10 RSVD
N9 RSVD

RSVD_TP N11
RSVD_TP P11

T38
T39

Must be placed within 500 mils from Pineview-M pins

K2 RSVD
J1 RSVD
M4 RSVD
L3 RSVD

RSVD K3
RSVD L2
RSVD M2
RSVD N2

PINEVIEW-M_FCBGA8559

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(7) DDR_A_DQS#[0..7]
(7) DDR_A_D[0..63]
(7) DDR_A_DM[0..7]
(7) DDR_A_DQS[0..7]
(7) DDR_A_MA[0..14]

U71B

PINEVIEW_M

REV = 1.1

DDR_A_MA0 AH19
DDR_A_MA1 AJ18
DDR_A_MA2 AK18
DDR_A_MA3 AK16
DDR_A_MA4 AJ14
DDR_A_MA5 AH14
DDR_A_MA6 AK14
DDR_A_MA7 AJ12
DDR_A_MA8 AH13
DDR_A_MA9 AK12
DDR_A_MA10 AK20
DDR_A_MA11 AH12
DDR_A_MA12 AJ11
DDR_A_MA13 AJ24
DDR_A_MA14 AJ10

DDR_A_MA0
DDR_A_MA1
DDR_A_MA2
DDR_A_MA3
DDR_A_MA4
DDR_A_MA5
DDR_A_MA6
DDR_A_MA7
DDR_A_MA8
DDR_A_MA9
DDR_A_MA10
DDR_A_MA11
DDR_A_MA12
DDR_A_MA13
DDR_A_MA14

(7) DDR_A_WE#
(7) DDR_A_CAS#
(7) DDR_A_RAS#

DDR_A_WE# AK22
DDR_A_CAS# AJ22
DDR_A_RAS# AK21

DDR_A_WE#
DDR_A_CAS#
DDR_A_RAS#

(7) DDR_A_BS0
(7) DDR_A_BS1
(7) DDR_A_BS2

DDR_A_BS0 AJ20
DDR_A_BS1 AH20
DDR_A_BS2 AK11

DDR_A_BS_0
DDR_A_BS_1
DDR_A_BS_2

(7) DDR_CS#0
(7) DDR_CS#1

DDR_CS#0 AH22
DDR_CS#1 AK25
AJ21
AJ25

DDR_A_CS#_0
DDR_A_CS#_1
DDR_A_CS#_2
DDR_A_CS#_3

(7) DDR_CKE0
(7) DDR_CKE1

DDR_CKE0 AH10
DDR_CKE1 AH9
AK10
AJ8

DDR_A_CKE_0
DDR_A_CKE_1
DDR_A_CKE_2
DDR_A_CKE_3

(7) M_ODT0
(7) M_ODT1

M_ODT0 AK24
M_ODT1 AH26
AH24
AK27

DDR_A_ODT_0
DDR_A_ODT_1
DDR_A_ODT_2
DDR_A_ODT_3

(7) M_CLK_DDR0
(7) M_CLK_DDR#0
(7) M_CLK_DDR1
(7) M_CLK_DDR#1

M_CLK_DDR0 AG15
M_CLK_DDR#0 AF15
M_CLK_DDR1 AD13
M_CLK_DDR#1 AC13

DDR_A_CK_0
DDR_A_CK_0#
DDR_A_CK_1
DDR_A_CK_1#

AC15
AD15
AF13
AG13

DDR_A_CK_3
DDR_A_CK_3#
DDR_A_CK_4
DDR_A_CK_4#

DDR_A_DQS_0
DDR_A_DQS#_0
DDR_A_DM_0

AD3 DDR_A_DQS0
AD2 DDR_A_DQS#0
AD4 DDR_A_DM0

DDR_A_DQ_0
DDR_A_DQ_1
DDR_A_DQ_2
DDR_A_DQ_3
DDR_A_DQ_4
DDR_A_DQ_5
DDR_A_DQ_6
DDR_A_DQ_7

AC4 DDR_A_D0
AC1 DDR_A_D1
AF4 DDR_A_D2
AG2 DDR_A_D3
AB2 DDR_A_D4
AB3 DDR_A_D5
AE2 DDR_A_D6
AE3 DDR_A_D7

DDR_A_DQS_1
DDR_A_DQS#_1
DDR_A_DM_1

AB8 DDR_A_DQS1
AD7 DDR_A_DQS#1
AA9 DDR_A_DM1

DDR_A_DQ_8
DDR_A_DQ_9
DDR_A_DQ_10
DDR_A_DQ_11
DDR_A_DQ_12
DDR_A_DQ_13
DDR_A_DQ_14
DDR_A_DQ_15

AB6 DDR_A_D8
AB7 DDR_A_D9
AE5 DDR_A_D10
AG5 DDR_A_D11
AA5 DDR_A_D12
AB5 DDR_A_D13
AB9 DDR_A_D14
AD6 DDR_A_D15

DDR_A_DQS_2
DDR_A_DQS#_2
DDR_A_DM_2

AD8 DDR_A_DQS2
AD10 DDR_A_DQS#2
AE8 DDR_A_DM2

DDR_A_DQ_16
DDR_A_DQ_17
DDR_A_DQ_18
DDR_A_DQ_19
DDR_A_DQ_20
DDR_A_DQ_21
DDR_A_DQ_22
DDR_A_DQ_23

AG8 DDR_A_D16
AG7 DDR_A_D17
AF10 DDR_A_D18
AG11 DDR_A_D19
AE7 DDR_A_D20
AF8 DDR_A_D21
AD11 DDR_A_D22
AE10 DDR_A_D23

DDR_A_DQS_3
DDR_A_DQS#_3
DDR_A_DM_3

AK5 DDR_A_DQS3
AK3 DDR_A_DQS#3
AJ3 DDR_A_DM3

DDR_A_DQ_24
DDR_A_DQ_25
DDR_A_DQ_26
DDR_A_DQ_27
DDR_A_DQ_28
DDR_A_DQ_29
DDR_A_DQ_30
DDR_A_DQ_31

AH1 DDR_A_D24
AJ2 DDR_A_D25
AK6 DDR_A_D26
AJ7 DDR_A_D27
AF3 DDR_A_D28
AH2 DDR_A_D29
AL5 DDR_A_D30
AJ6 DDR_A_D31

DDR_A_DQS_4
DDR_A_DQS#_4
DDR_A_DM_4

AG22 DDR_A_DQS4
AG21 DDR_A_DQS#4
AD19 DDR_A_DM4

DDR_A_DQ_32
DDR_A_DQ_33
DDR_A_DQ_34
DDR_A_DQ_35
DDR_A_DQ_36
DDR_A_DQ_37
DDR_A_DQ_38
DDR_A_DQ_39

AE19 DDR_A_D32
AG19 DDR_A_D33
AF22 DDR_A_D34
AD22 DDR_A_D35
AG17 DDR_A_D36
AF19 DDR_A_D37
AE21 DDR_A_D38
AD21 DDR_A_D39

DDR_A_DQS_5
DDR_A_DQS#_5
DDR_A_DM_5

AE26 DDR_A_DQS5
AG27 DDR_A_DQS#5
AJ27 DDR_A_DM5

DDR_A_DQ_40
DDR_A_DQ_41
DDR_A_DQ_42
DDR_A_DQ_43
DDR_A_DQ_44
DDR_A_DQ_45
DDR_A_DQ_46
DDR_A_DQ_47

AE24 DDR_A_D40
AG25 DDR_A_D41
AD25 DDR_A_D42
AD24 DDR_A_D43
AC22 DDR_A_D44
AG24 DDR_A_D45
AD27 DDR_A_D46
AE27 DDR_A_D47

DDR_A_DQS_6
DDR_A_DQS#_6
DDR_A_DM_6

AE30 DDR_A_DQS6
AF29 DDR_A_DQS#6
AF30 DDR_A_DM6

DDR_A_DQ_48
DDR_A_DQ_49
DDR_A_DQ_50
DDR_A_DQ_51
DDR_A_DQ_52
DDR_A_DQ_53
DDR_A_DQ_54
DDR_A_DQ_55

AG31 DDR_A_D48
AG30 DDR_A_D49
AD30 DDR_A_D50
AD29 DDR_A_D51
AJ30 DDR_A_D52
AJ29 DDR_A_D53
AE29 DDR_A_D54
AD28 DDR_A_D55

DDR_A_DQS_7
DDR_A_DQS#_7
DDR_A_DM_7

AB27 DDR_A_DQS7
AA27 DDR_A_DQS#7
AB26 DDR_A_DM7

DDR_A_DQ_56
DDR_A_DQ_57
DDR_A_DQ_58
DDR_A_DQ_59
DDR_A_DQ_60
DDR_A_DQ_61
DDR_A_DQ_62
DDR_A_DQ_63

AA24 DDR_A_D56
AB25 DDR_A_D57
W24 DDR_A_D58
W22 DDR_A_D59
AB24 DDR_A_D60
AB23 DDR_A_D61
AA23 DDR_A_D62
W27 DDR_A_D63

DDR_A

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PINEVIEW-M_FCBGA8559

(12) DMI_RX0
(12) DMI_RX#0
(12) DMI_RX1
(12) DMI_RX#1

C435 0.1U_0402_10V7K DMI_RX0_C
C436 0.1U_0402_10V7K DMI_RX#0_C
C437 0.1U_0402_10V7K DMI_RX1_C
C438 0.1U_0402_10V7K DMI_RX#1_C

Close to CPU

JP16 CONN@

(5) XDP_PREQ# XDP_PREQ#
(5) XDP_PRDY# XDP_PRDY#
(5) XDP_BPM#3 XDP_BPM#3
(5) XDP_BPM#2 XDP_BPM#2
(5) XDP_BPM#1 XDP_BPM#1
(5) XDP_BPM#0 XDP_BPM#0
(5,13) H_PWRGD R354 1K_0402_5%
(13) SLPIOVR# R347 1K_0402_5%
(8) CPU_ITP
(8) CPU_ITP#
+VCCP (5,13,16,17,21) PLTRST# PLTRST# R348 1K_0402_1%
(5) XDP_TDO XDP_TDO
(5) XDP_TRST# XDP_TRST#
(5) XDP_TDI XDP_TDI
(5) XDP_TMS XDP_TMS
(5) XDP_TCK XDP_TCK

ACES_87151-24051

XDP Reserve

+VCCP

XDP_TDI R341 51 +-1% 0402
XDP_TMS R342 51 +-1% 0402
XDP_TDO R343 51 +-1% 0402
XDP_PREQ# R344 51 +-1% 0402
XDP_TRST# R345 51 +-1% 0402
XDP_TCK R346 51 +-1% 0402

+1.8V

R369 10K_0402_5%
R370 10K_0402_5% @
T40
T41
R50 1K_0402_1%
R142 1K_0402_1%
C1179 0.1U_0402_16V4Z

DDR_REF AL28
DDR_RPD AK28
DDR_RPU AJ26

RSVD_TP AB11
RSVD_TP AB13
RSVD AB4
RSVD AK8
RSVD AK29

DDR_VREF
DDR_RPD
DDR_RPU

FAN1 Conn

+5VS
C312 2.2U_0603_10V6K
U12
APL5607KI-TRG_SO8
+VCC_FAN1
(21) EN_FAN1
R47 0_0402_5%
C1151 0.1U_0402_16V4Z

+3VS
R256 10K_0402_5%
(21) FAN_SPEED1
C311 100P_0402_50V8J

D19 DAN217_SC59 @
C313 10U_0805_10V4Z
C1150 1000P_0402_50V7K
40mil
JP12
ACES_85204-0300N
CONN@

Update symbol 0111.

Modify D38 D39 D40 Pin define 08/13

XDP_TMS
XDP_TCK
XDP_PREQ#
XDP_TDO
XDP_TRST#
XDP_TDI

D38
D39
D40
PJDLC05C_SOT23-3

Add 2009-6-17

+1.8V
R242 80.6_0402_1% DDR_RPU
C1180 0.01U_0402_16V7K
R243 80.6_0402_1% DDR_RPD

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R249 be placed <750 mils to U71.M30
R247 be placed <750 mils to U71.M29

R201 be placed <500 mils to U71.P28

R151 be placed U71.R22

Modify 08/04

To be placed <250 mils to U71 ball

To be placed <500 mils to U71 ball

Add 470PF on H_SMI# for known issue 07/08

H_THERMDA, H_THERMDC routing together.
Trace width / Spacing = 10 / 10 mil

CPU THERMAL SENSOR

EMC1402-1-ACZL-TR MSOP 8P SENSOR
Address:100_1100

Close to Processor pin

Close to Processor pin

placed within 0.5" of processor pin and 5mils spacing.

placed within 0.5" of processor pin and 5mils spacing.

Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title	Pineview(2/3)	
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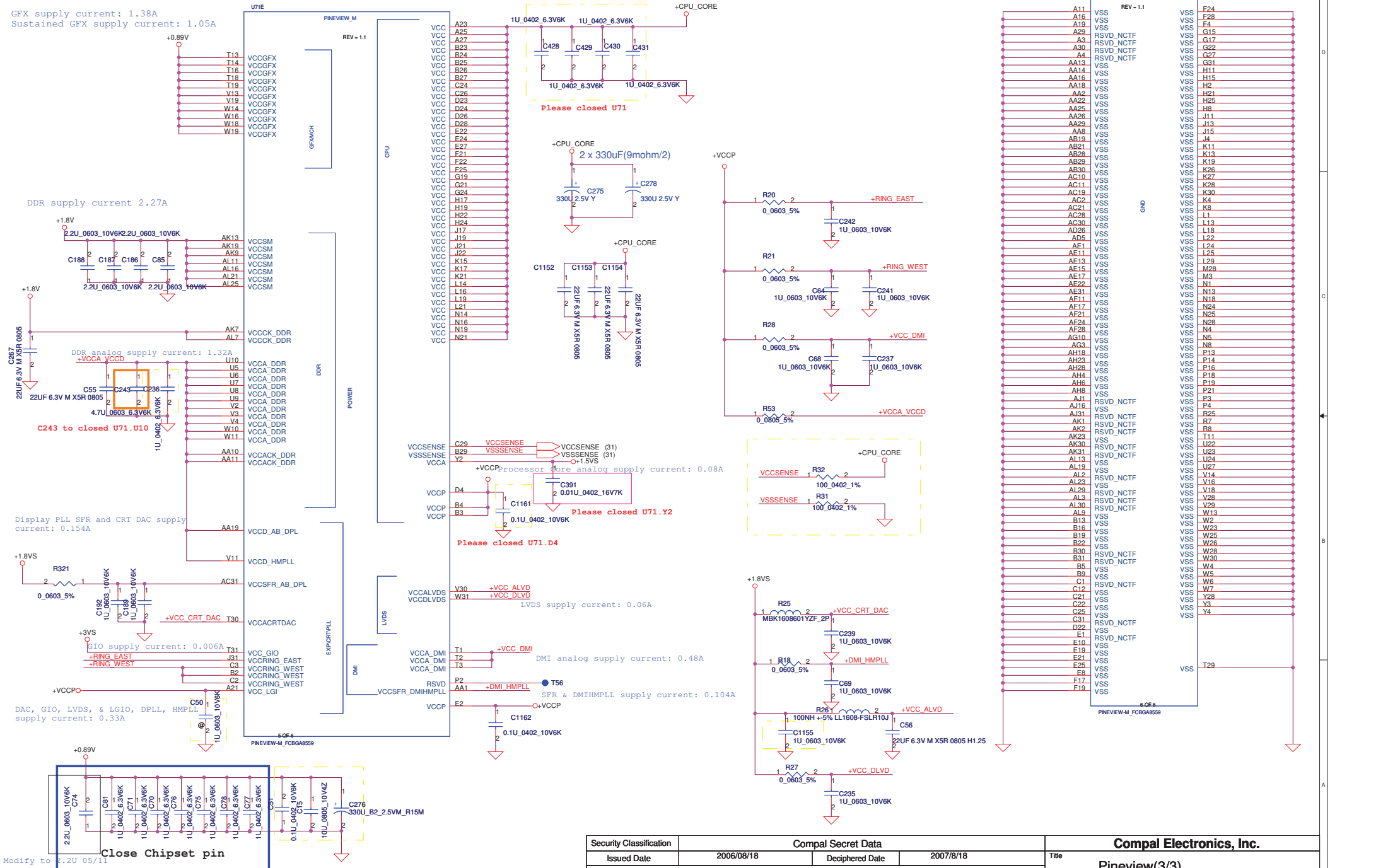

Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: Pineview(3/3)

Size	Document Number	Rev
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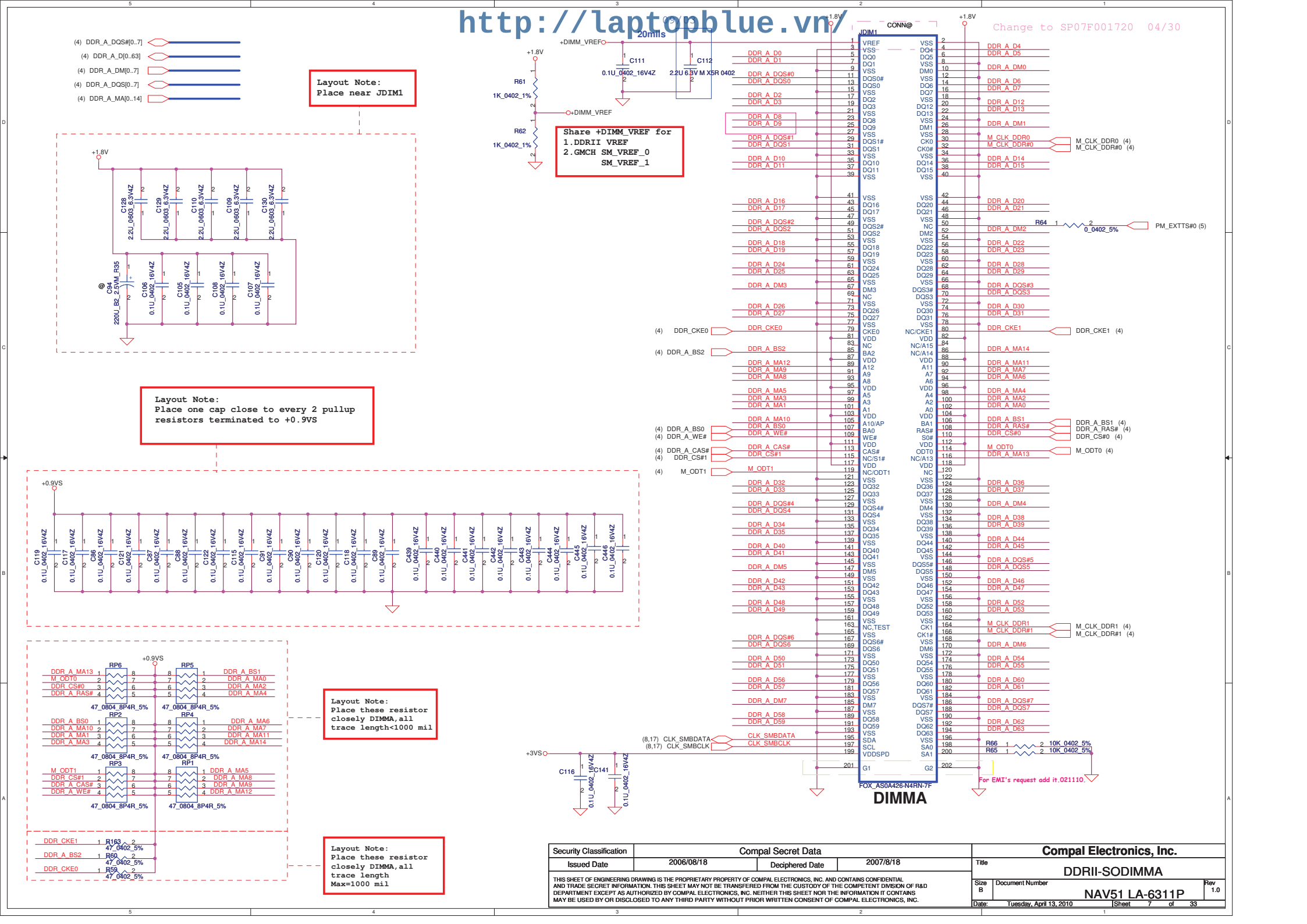

Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.			
Title	DDRII-SODIMMA		
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FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

SA00003H730 (Realtek :RTM890N-397-VC-GRT)

Change co-lay net name to +1.5VM_CK505 07/03

BOM change.012510.

BOM change to use SB000008J00.032310.

For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#
For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS

For PCI2_TME:0=Overclocking of CPU and SRC allowed
(ICS only) 1=Overclocking of CPU and SRC NOT allowed

Routing the trace at least 10mil

U4 SLG8SP556VTR_QFN72_10X10

SRC PORT LIST

PORT	DEVICE
SRC1	CPU_SSCDREFCLK
SRC2	
SRC3	
SRC4	PCIE_WLAN
SRC6	PCIE_SATA
SRC7	PCIE_PCH
SRC8	CPU_ITP
SRC9	CLK_CPU_EXP
SRC10	PCIE_LAN
SRC11	

REQ PORT LIST

PORT	DEVICE
REQ_3#	
REQ_4#	PCIE_WLAN
REQ_6#	
REQ_7#	
REQ_9#	
REQ_10#	PCIE_LAN
REQ_11#	
REQ_A#	

Add LAN_CLKREQ# 0108.

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: Clock Generator CK505

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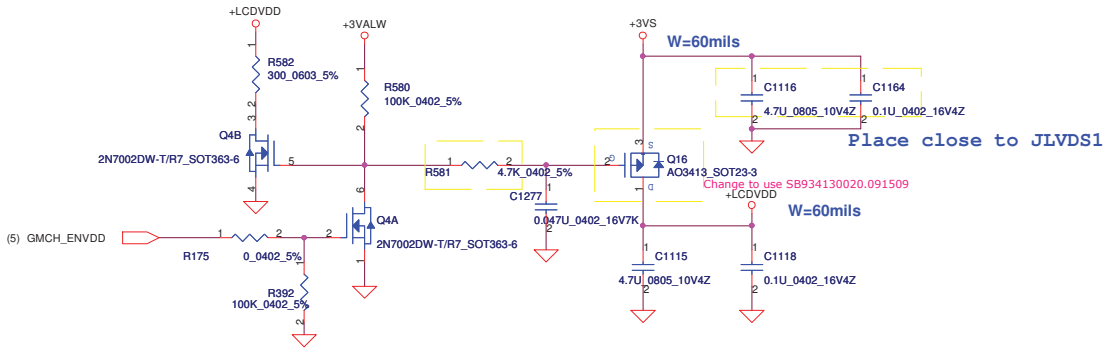
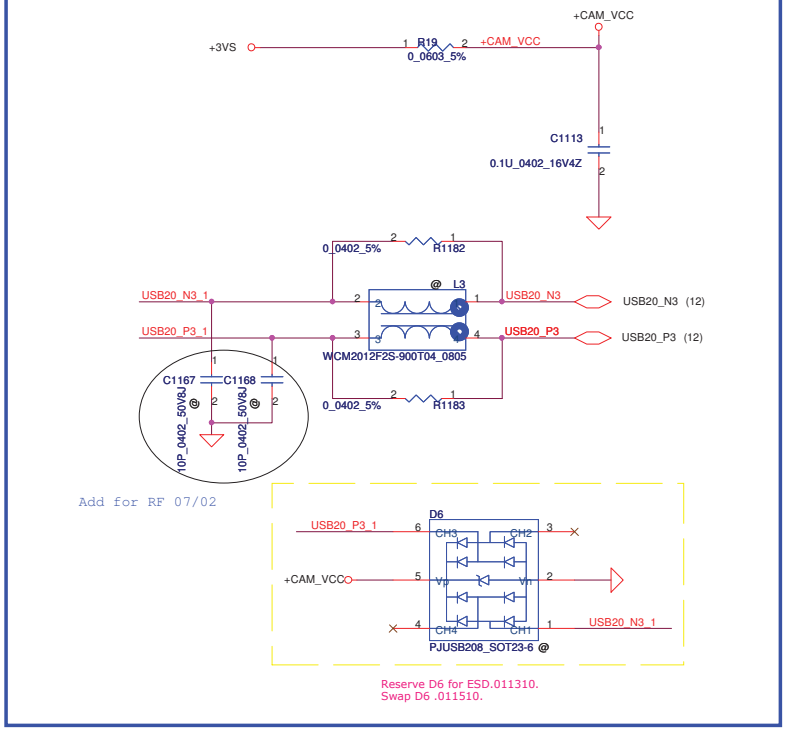
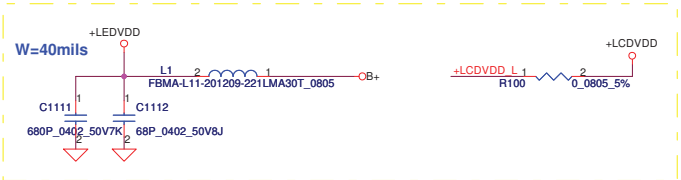
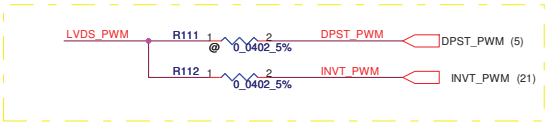
LCD POWER CIRCUIT

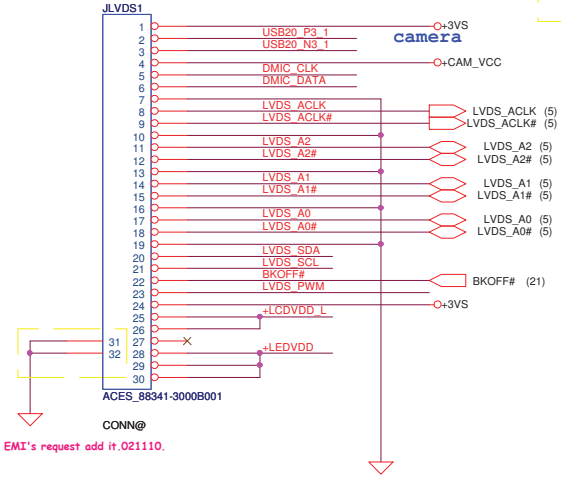


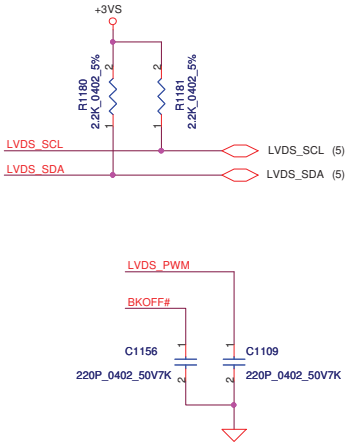


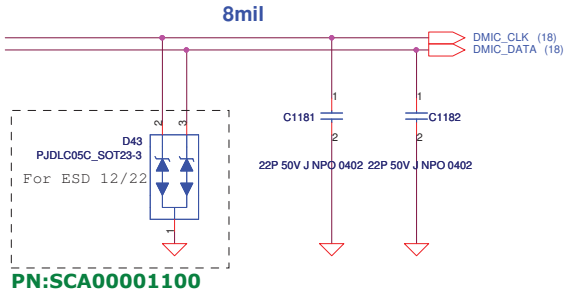
CMOS & LCD/PANEL BD. Conn.











PN:SCA00001100

Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: LVDS /INVERTER

Size	Document Number	Rev
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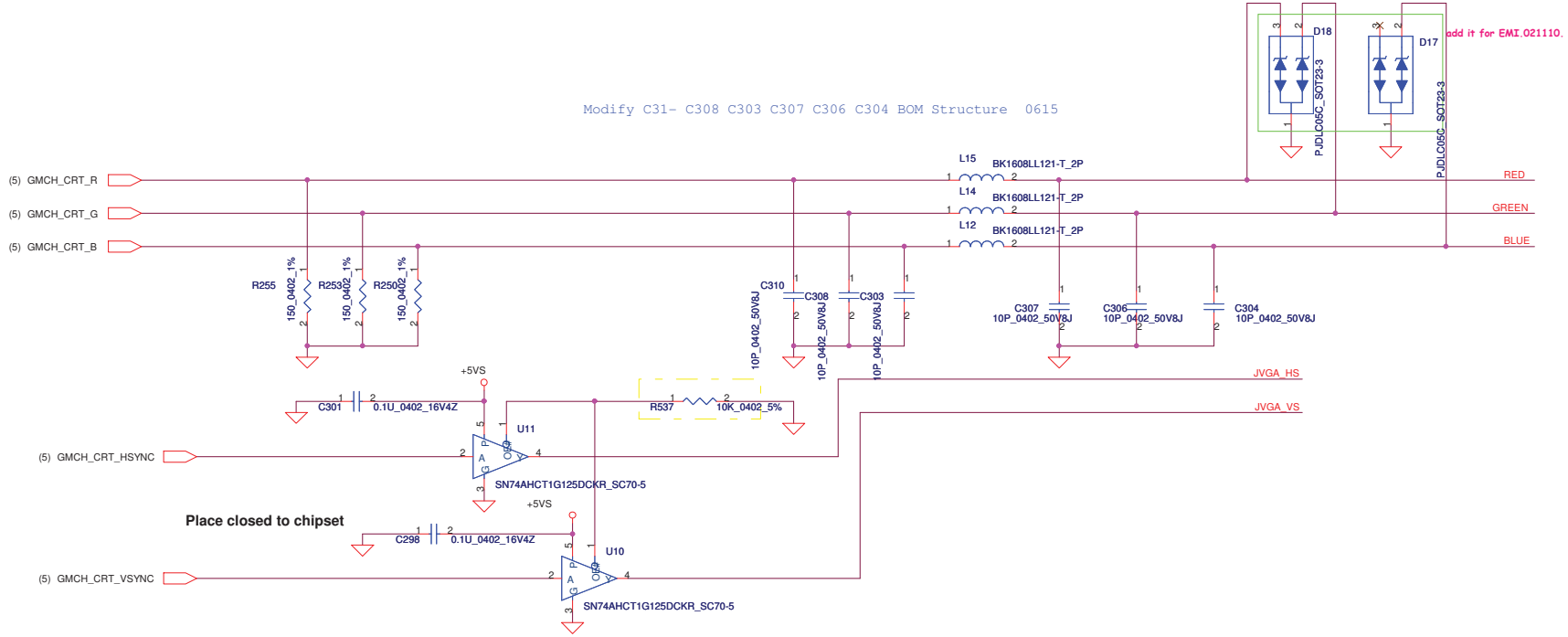
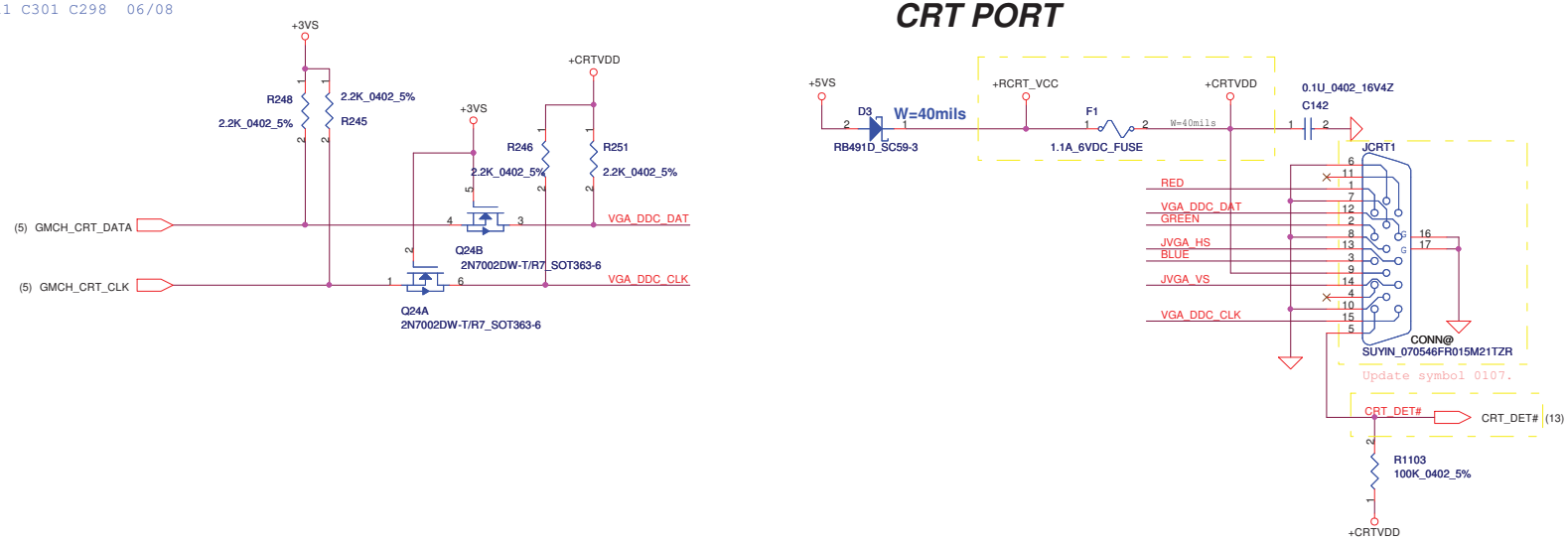
Close to CRT CONN for ESD.

Modify C31- C308 C303 C307 C306 C304 BOM Structure 0615



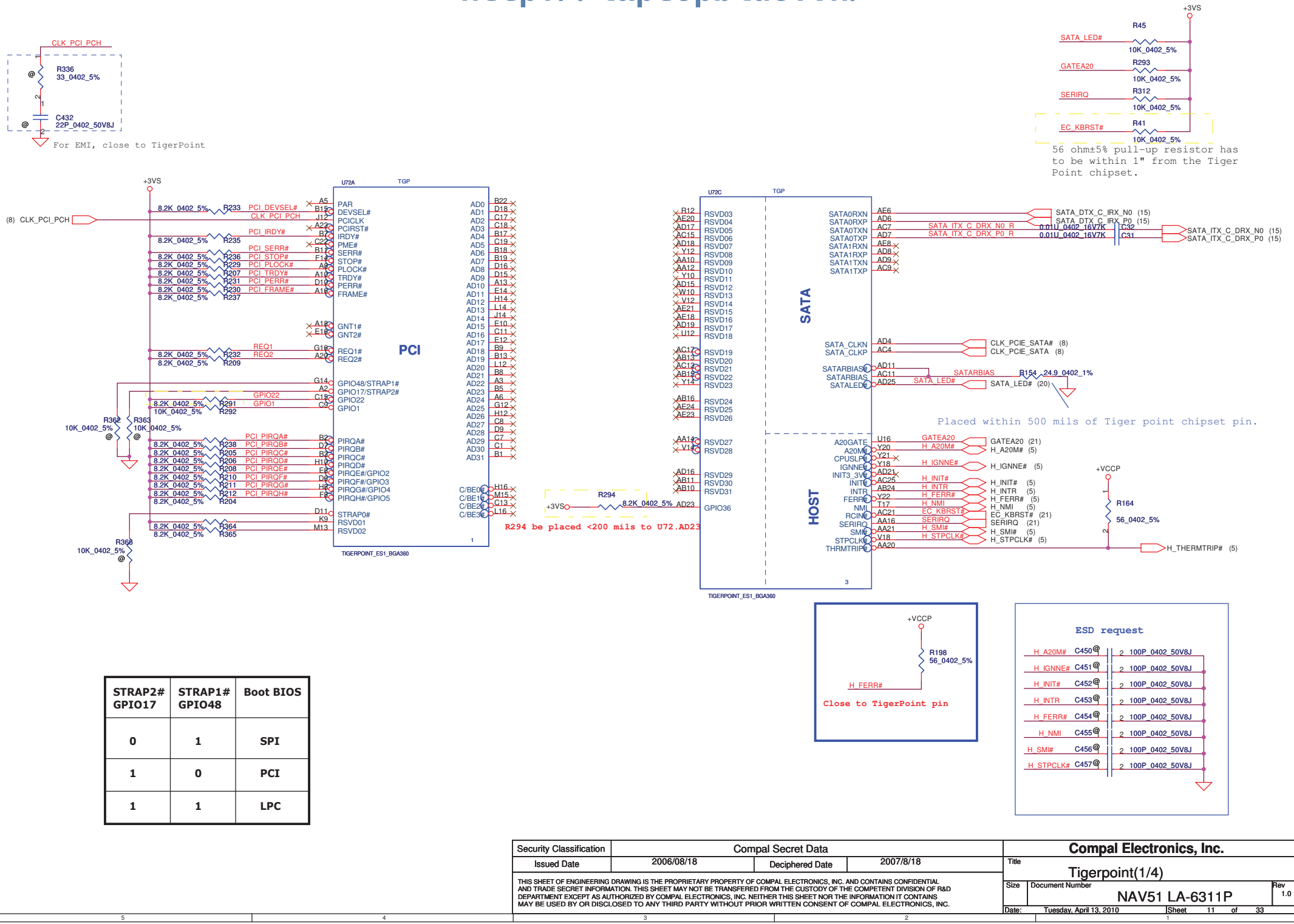
Add R1283 R1284
Change R247 R249 to 10 ohm
Add @ on U10 U11 C301 C298 06/08

CRT PORT



Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.	
Title	CRT PORT
Size B	Document Number NAV51 LA-6311P
Rev	0.2
Date: Tuesday, April 13, 2010	Sheet 10 of 33



STRAP2# GPIO17	STRAP1# GPIO48	Boot BIOS
0	1	SPI
1	0	PCI
1	1	LPC

Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.			
Title	Tigerpoint(1/4)		
Size	Document Number	NAV51 LA-6311P	Rev 1.0
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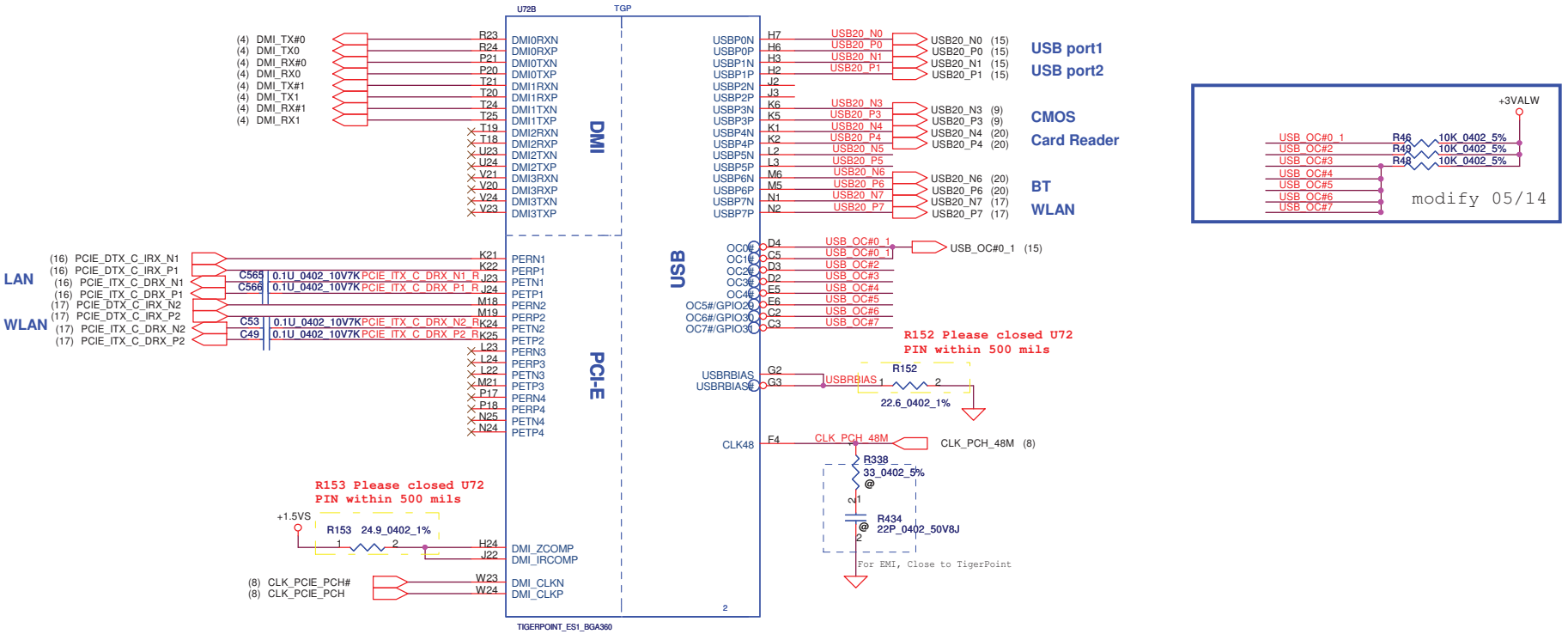
PCIE Port List	
1	LAN
2	WLAN
3	
4	

USB Port List	
0	USB Left1
1	USB Left2
2	
3	CMOS
4	CardReader
5	
6	BT
7	WLAN



Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: Tigerpoint(2/4)

Size	Document Number	Rev
Custom	NAV51 LA-6311P	1.0

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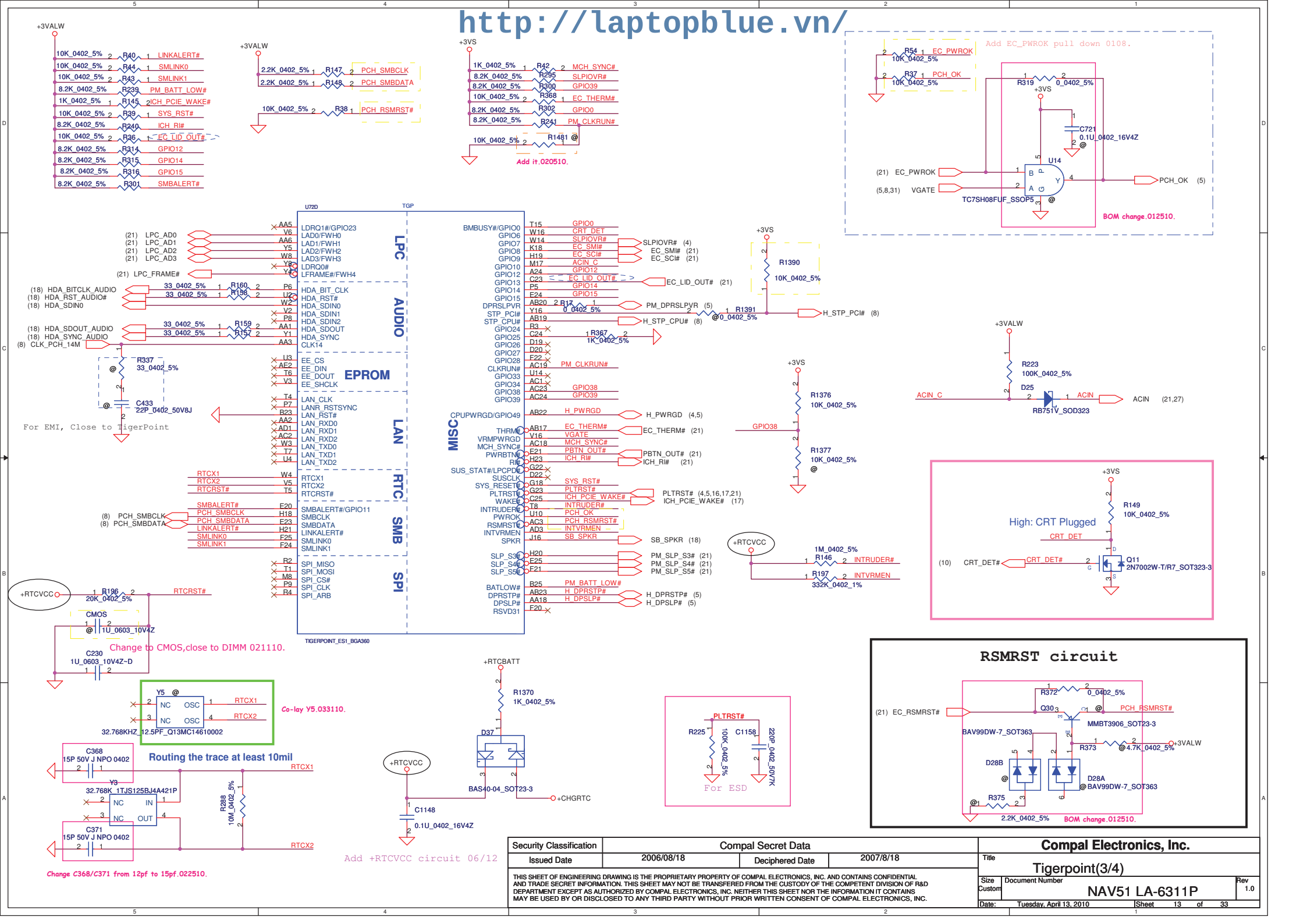

Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.			
Title	Tigerpoint(3/4)		
Size: Custom	Document Number: NAV51 LA-6311P		Rev: 1.0
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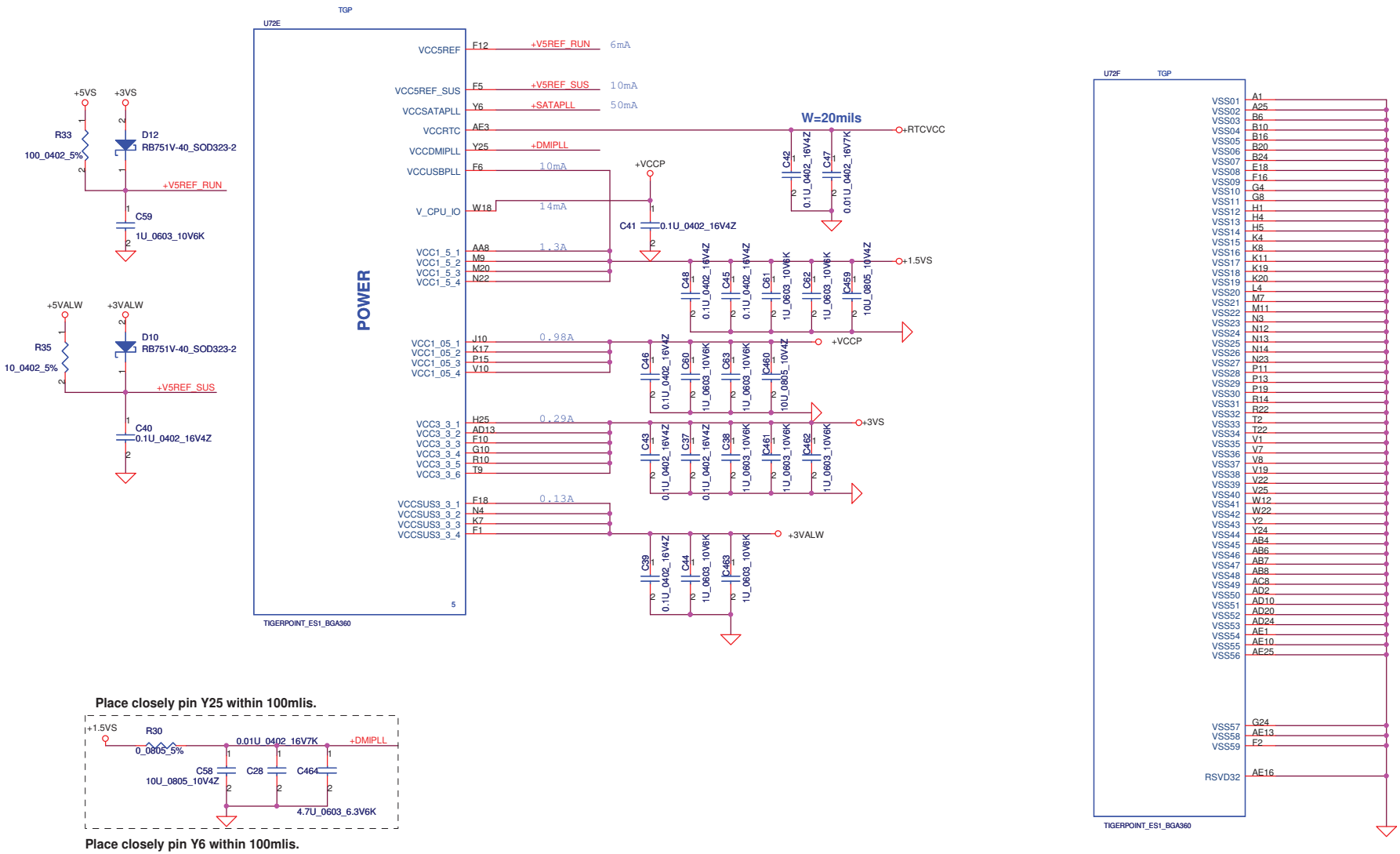
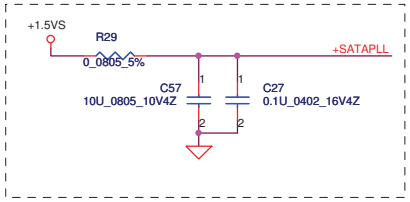




Security Classification	Compal Secret Data		
Issued Date	2009/04/15	Deciphered Date	2010/04/15

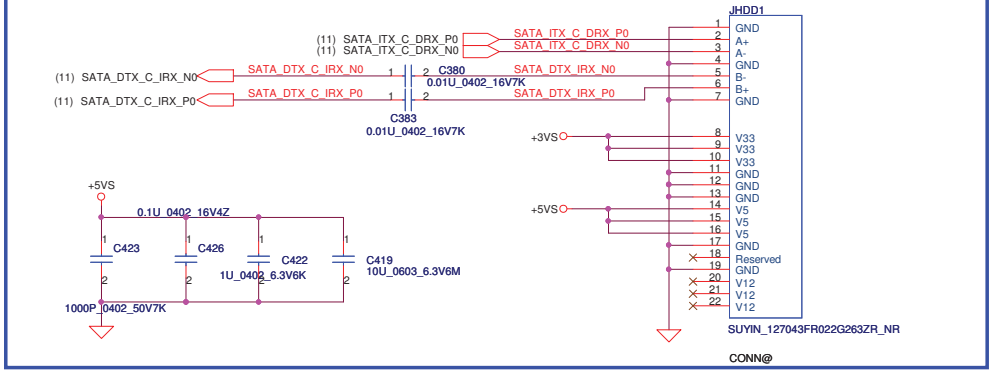
Compal Electronics, Inc.

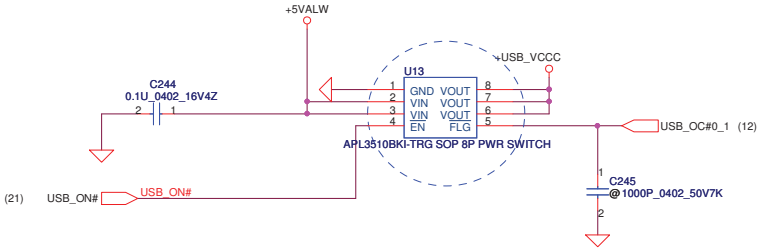
Title: Tigerpoint(4/4)

Size: Custom | Document Number: NAV51 LA-6311P | Rev: 0.1

Date: Tuesday, April 13, 2010 | Sheet 14 of 33

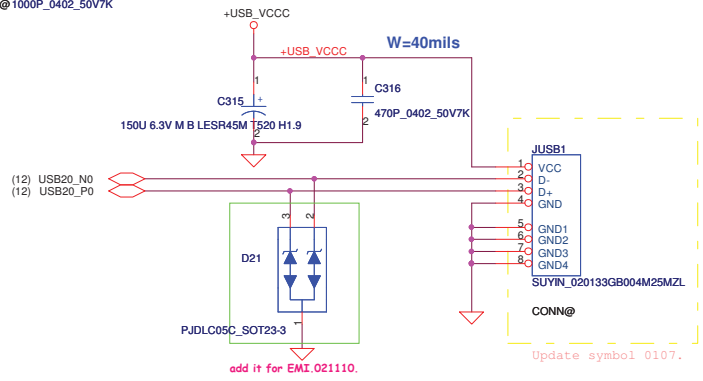
SATA HDD Conn.



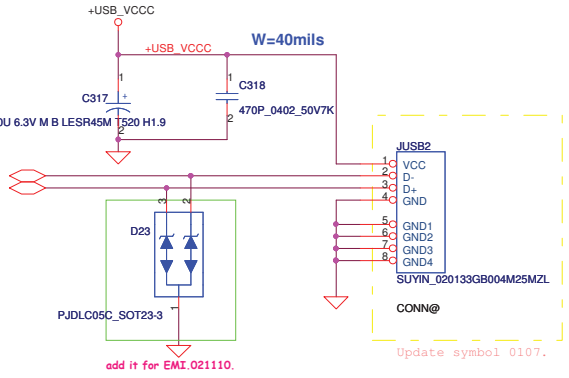


Change JUSB1 JUSB2 to NEW P/N SP010906181 06/23

USB CONN.1



USB CONN.2



Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: SATA,CONN. / USB CONN.

Size	Document Number	Rev
B	NAV51 LA-6311P	0.2

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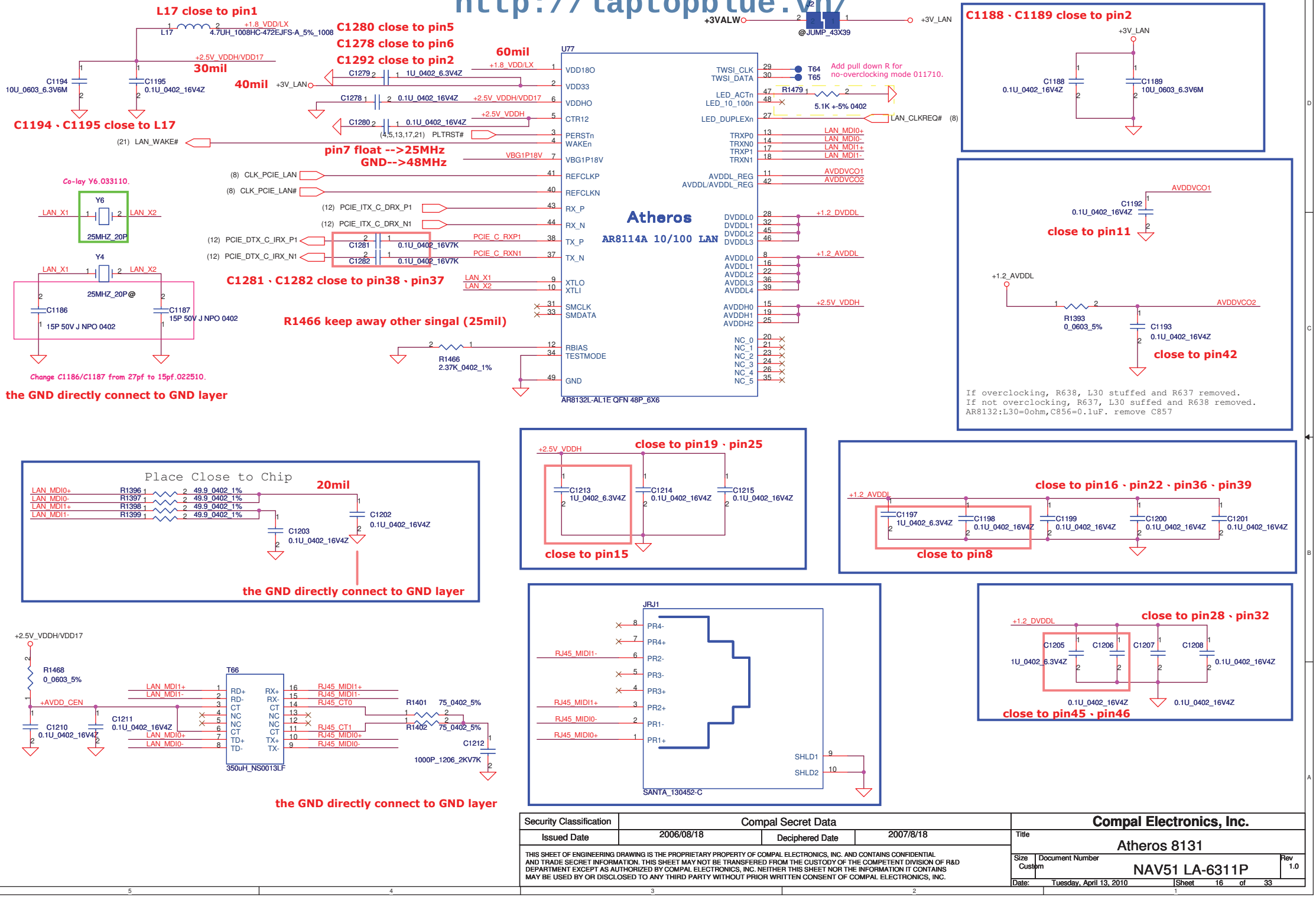

Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title	Atheros 8131		
Size: Custom	Document Number: NAV51 LA-6311P		Rev: 1.0
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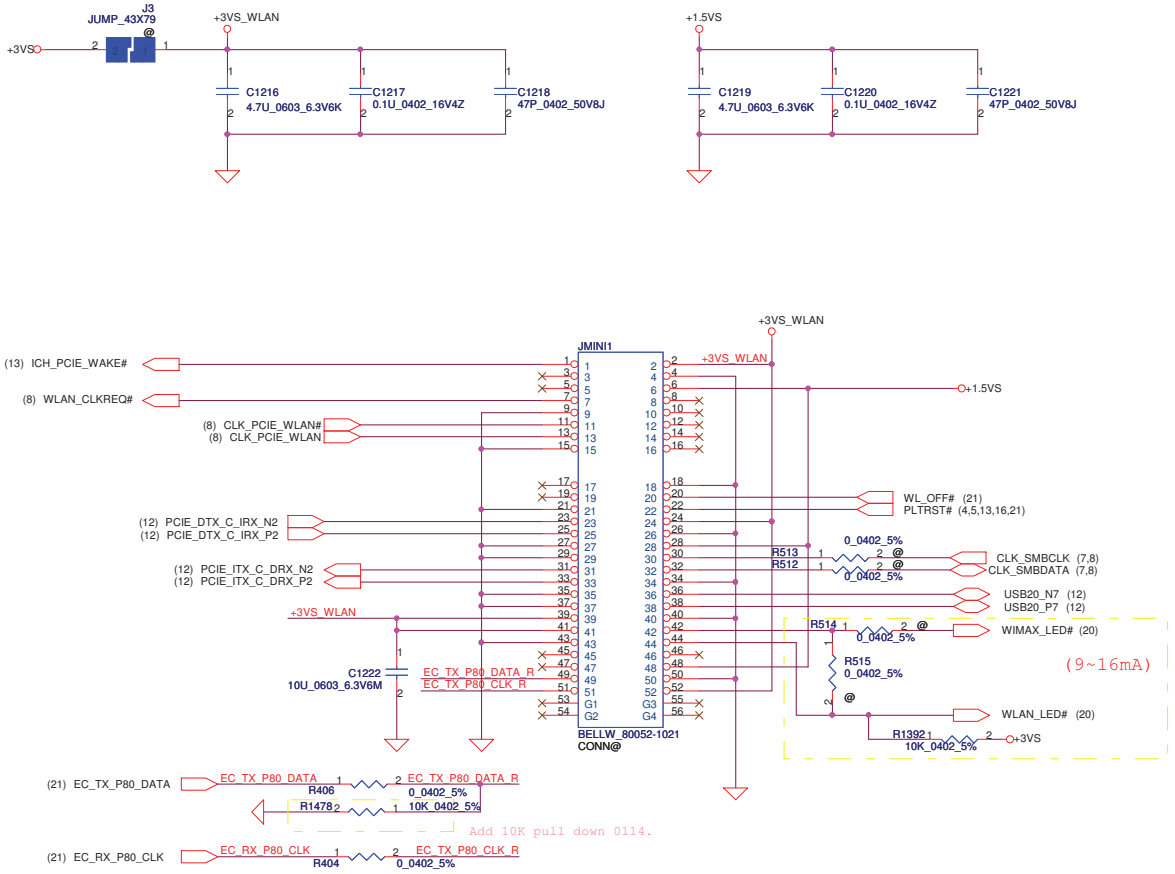
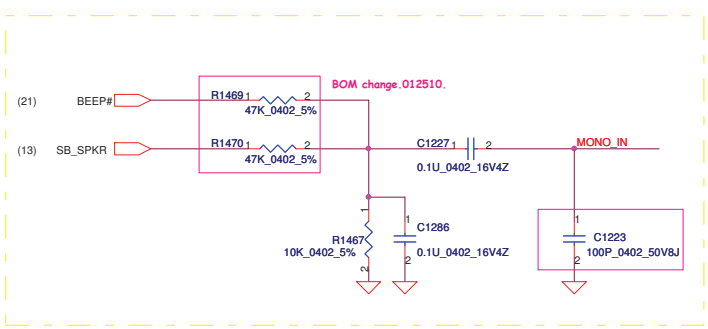
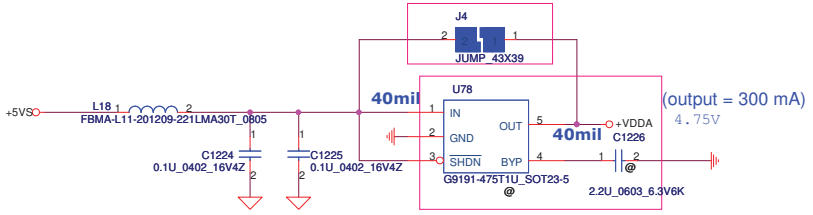
Mini-Express Card for WLAN



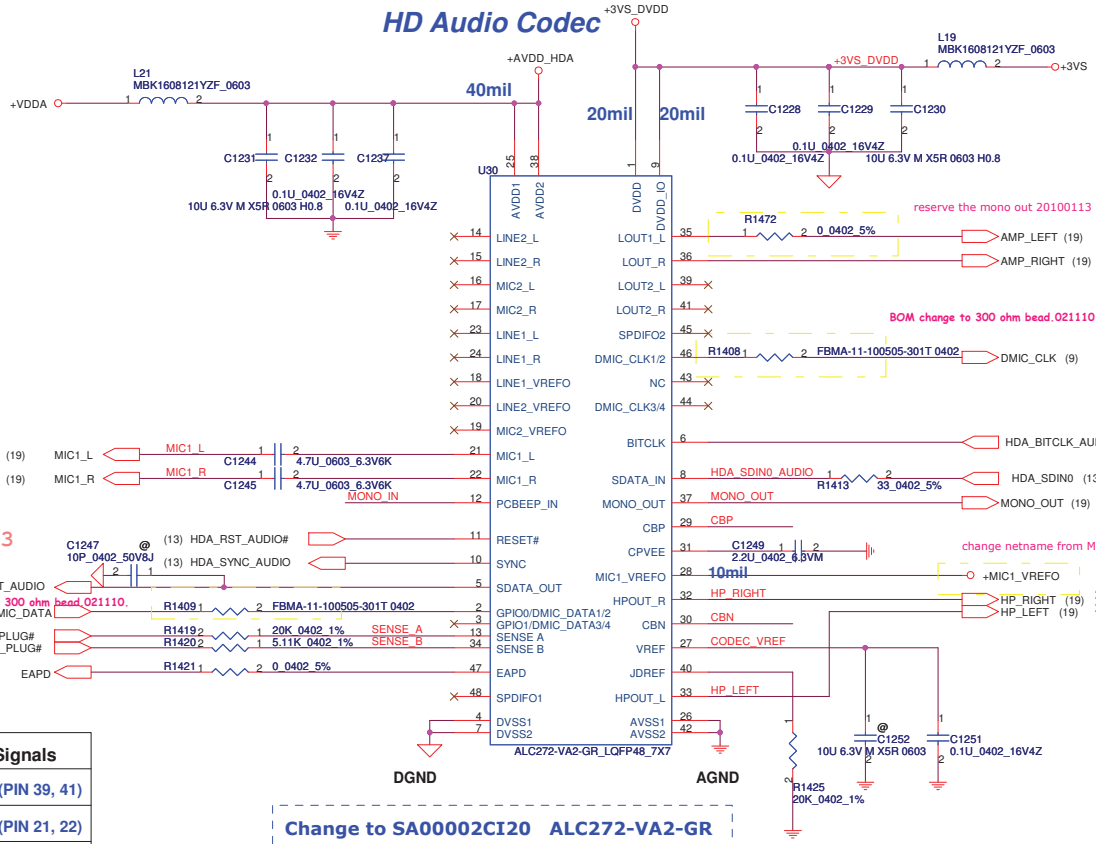
Compal Electronics, Inc.			
Title	<Title>	WLAN	
Size: Custom	Document Number: NAV51 LA-6311P	NAV51 LA-6311P	Rev: 0.1
Date: Tuesday, April 13, 2010	Sheet 17 of 33		

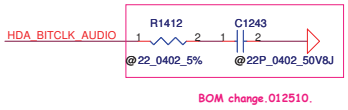


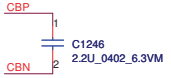
simplify the pcbeep circuit 011410.

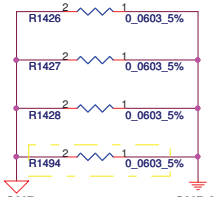


HD Audio Codec









Change to SA00002CI20 ALC272-VA2-GR

Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: HD Audio Codec ALC272

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BOM change.012510.

J5
+5VS — 2 — 1 — +5VAMP_J
JUMP_43X39

change C1255 · C1256 · C1257 · C1258 · C1283 from 0.47uF to 0.1uF
20100113

reserve the mono out 20100113

+5VAMP_J
C1253 10U 6.3V M X5R 0603 H0.8
C1254 0.1U_0402_16V4Z

U80
TPA6017A2_TSSOP20

C1255 0.1U_0603_25V7K — RIN+
C1283 0.1U_0603_25V7K — RIN-
C1257 0.1U_0603_25V7K — AMP_IN+ — LIN+
(18) MONO_OUT — R1473 @ 0_0402_5%
(18) AMP_LEFT — C1256 0.1U_0603_25V7K — R1435 0_0402_5% — AMP_IN- — LIN-
(18) AMP_RIGHT — C1258 0.1U_0603_25V7K — R1438 0_0402_5%
(21) EC_MUTE# — EC_MUTE# — SHUTDOWN

GAIN0 — GAIN1 — ROUT+ — ROUT- — LOUT+ — SPKR/L+ — LOUT- — SPKR/L- — NC — BYPASS — AMP_BYPASS

+5VAMP_J
@ R1429 100K_0402_5%
@ R1430 100K_0402_5%
R1436 100K_0402_5%
R1437 100K_0402_5%

C1259 0.47U_0603_10V7K

Keep 10 mil width

Int. Speaker Conn.

20mil

SPKR/L+ R1431 0_0603_5% SPK_RL+
SPKR/L- R1432 0_0603_5% SPK_RL-
JSPK1
ACES_88266-02001
CONN@

SPK_RL+ — SPK_RL-
D44
PJDLC05C_SOT23-3

R1474 @ 40.2K_0402_1%
+5VAMP_J
U81
EC_MUTE# — AMP_BYPASS — AMP_IN+ R1475 15K_0402_5% @ — AMP_IN- R1476 15K_0402_5% @
SD# BYPASS INP INN GND2 OUTN GND1 VDD OUTP
APA0715QBI-TRG_TDFN8_3X3@
SPKR/L- — SPKR/L+
R1477 @ 40.2K_0402_1%
co-lay TPA6205A1 0112.

Headphone Out

(Use NAL00 PCB Footprint)

20mil
(18) HP_LEFT — HP_LEFT — R1440 56.2_0402_1% — HPOUT_L_1 — L23 FBM-11-160808-700T_0603 — HPOUT_L_2
(18) HP_RIGHT — HP_RIGHT — R1441 56.2_0402_1% — HPOUT_R_1 — L24 FBM-11-160808-700T_0603 — HPOUT_R_2
20mil

C1260 330P_0402_50V7K
C1261 330P_0402_50V7K
(18) HP_PLUG# — HP_PLUG#

JHP1
SINGA_2SJ-0960-C01
CONN@

Follow ACER's request to cheange HP CONN P/N.011410.

MIC JACK

+MIC1_VREFO — +MIC1_VREFO
D26 RB751V-40TE17_SOD323-2
D27 RB751V-40TE17_SOD323-2
R403 4.7K_0402_5%
R402 4.7K_0402_5%
20mil
(18) MIC1_L — R405 1K_0603_1% — MIC2_L_1 — L28 FBM-11-160808-700T_0603 — MIC2_L_2
(18) MIC1_R — R407 1K_0603_1% — MIC2_R_1 — L27 FBM-11-160808-700T_0603 — MIC2_R_2
20mil

C488 220P_0402_50V8J
C489 220P_0402_50V8J
(18) MIC_PLUG# — MIC_PLUG#

JMIC1
SINGA_2SJ-0960-C01
CONN@

Follow ACER's request to cheange MIC CONN P/N.011410.

Compal Electronics, Inc.	
Title	<Title> Amplifier & Audio Jack
Size: Custom	Document Number: NAV51 LA-6311P — NAV51 LA-6311P — Rev: 0.1
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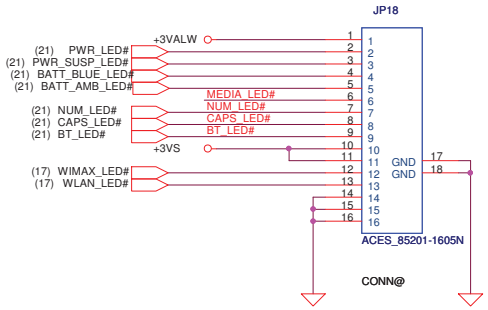
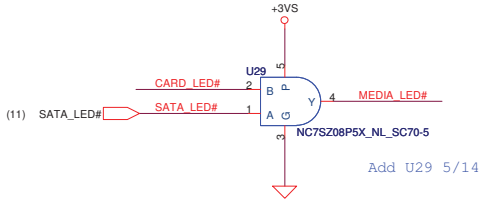
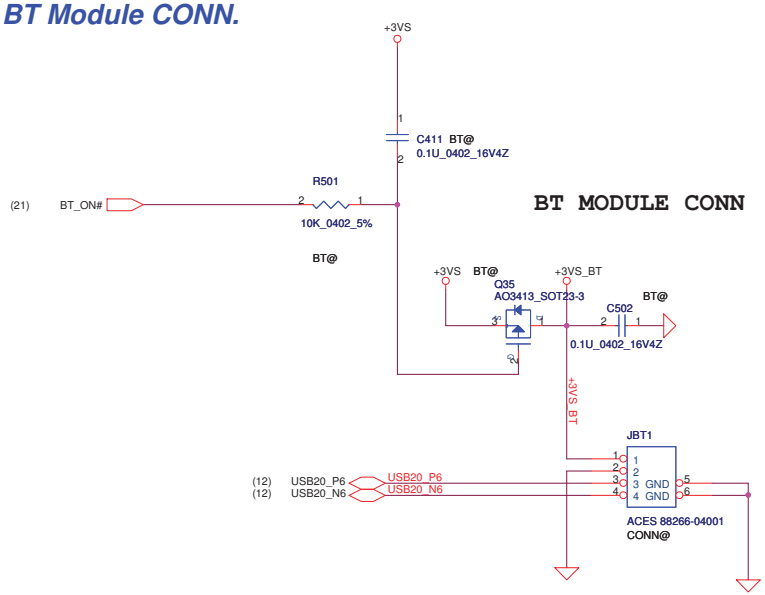
LED PCB CONN.

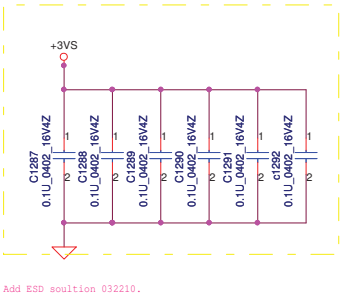




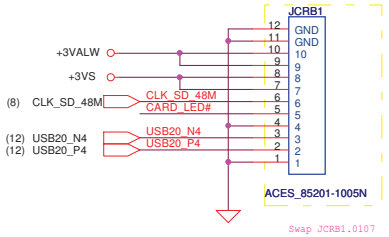
BT Module CONN.



ESD



Card Reader CONN.



Security Classification	Compal Secret Data		
Issued Date	2009/01/22	Deciphered Date	2009/11/20

Compal Electronics, Inc.

Title: **Card reader**

Size: Custom | Document Number: **NAV51 LA-6311P** | Rev: 0.1

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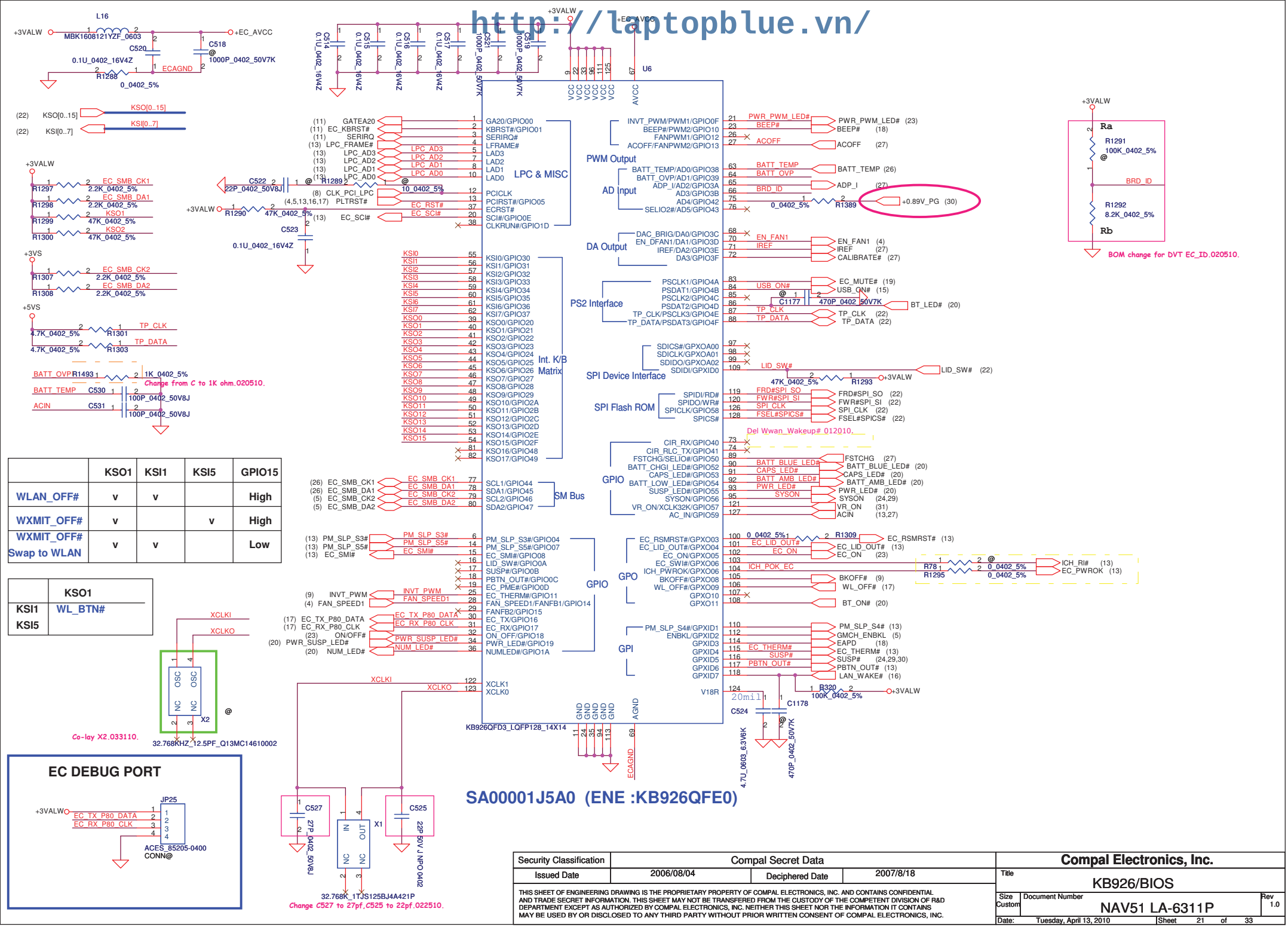


	KSO1	KSI1	KSI5	GPIO15
WLAN_OFF#	v	v		High
WXMIT_OFF#	v		v	High
WXMIT_OFF# Swap to WLAN	v	v		Low

	KSO1
KSI1	WL_BTN#
KSI5	

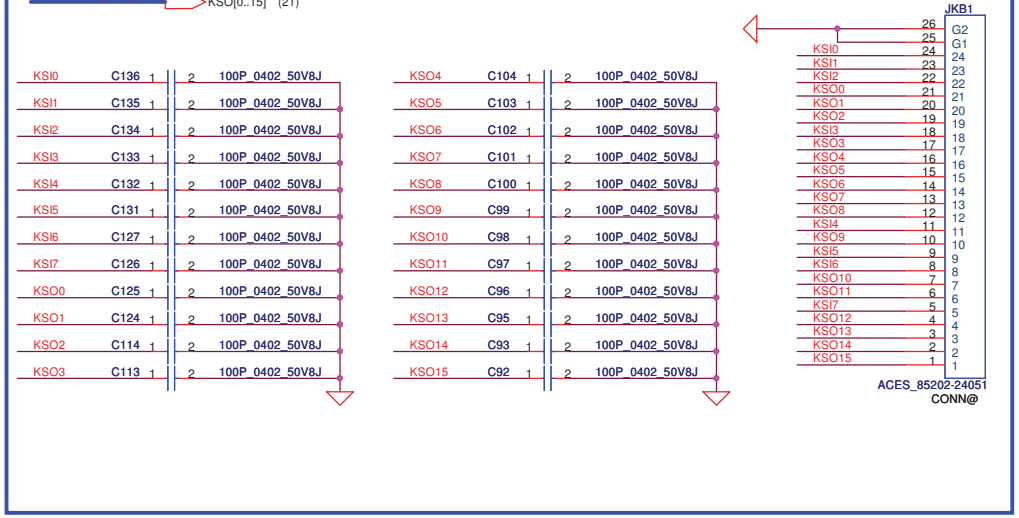
EC DEBUG PORT

Security Classification	Compal Secret Data		
Issued Date	2006/08/04	Deciphered Date	2007/8/18

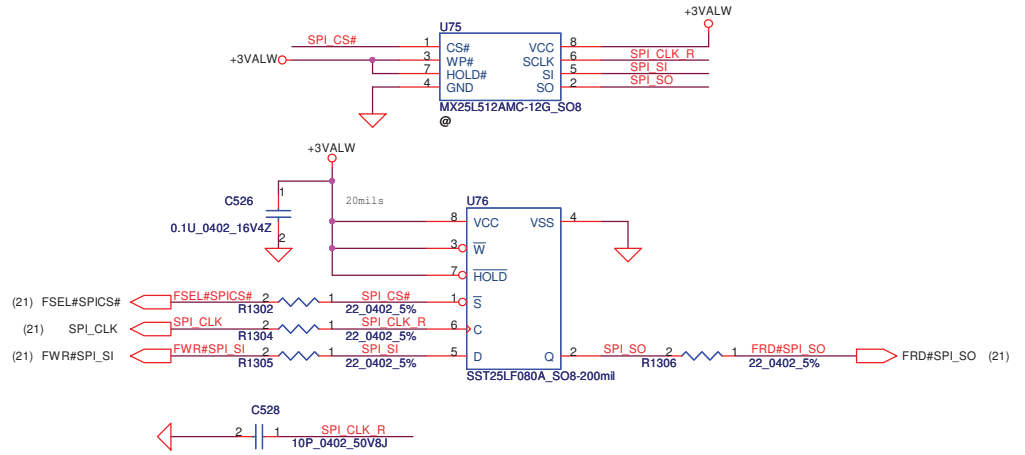
Compal Electronics, Inc.

Title	KB926/BIOS		
Size: Custom	Document Number: NAV51 LA-6311P		Rev: 1.0
Date: Tuesday, April 13, 2010	Sheet 21 of 33		

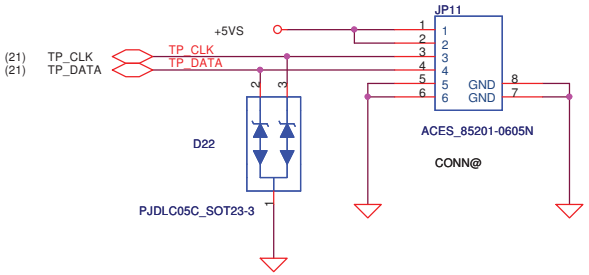
INT_KBD Conn.



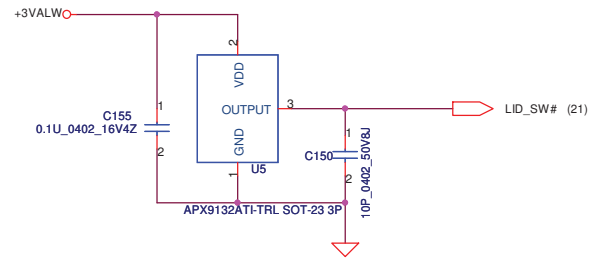
8M SPI ROM



To TP/B Conn.



LID Switch



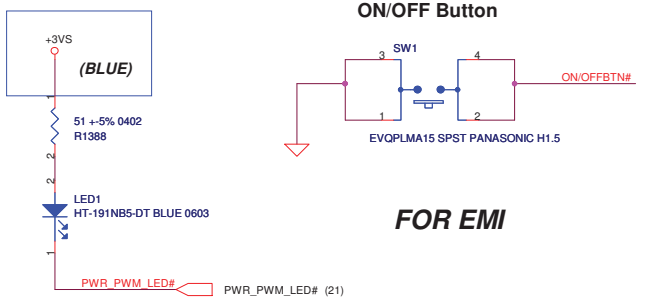
Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

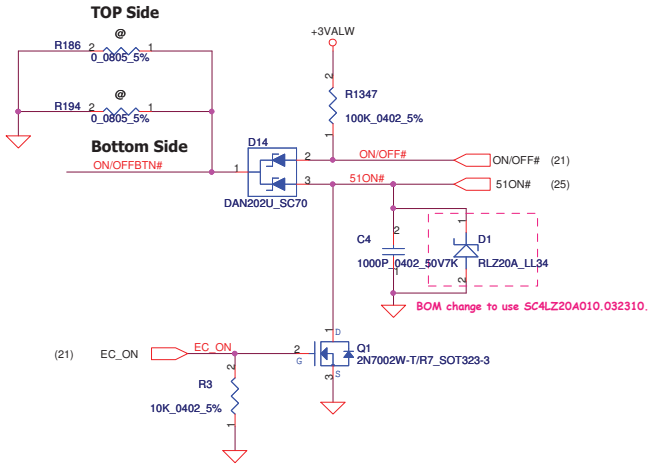
Title	KB CONN/TP/LID SW	
Size: B	Document Number: NAV51 LA-6311P	Rev: 0.2
Date: Tuesday, April 13, 2010	Sheet 22 of 33	

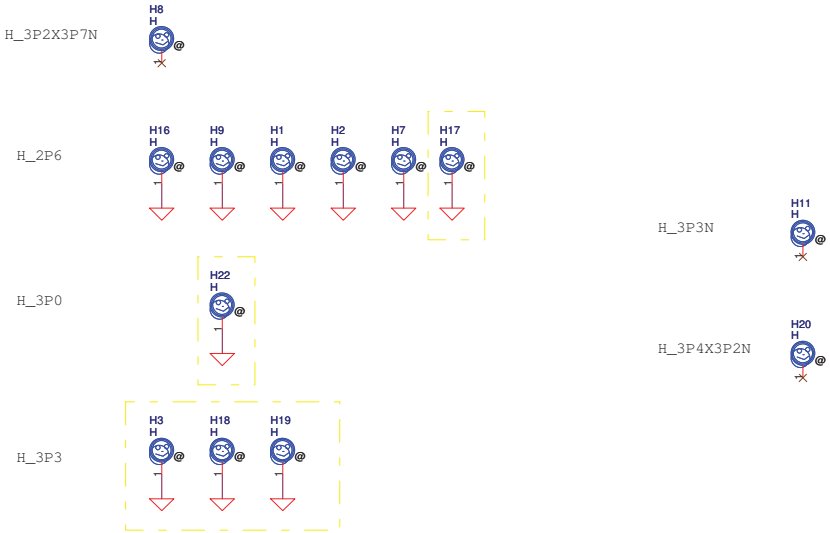
Add For NAV50 07/06
09/03 Change +5VS to +3VS

ON/OFF Button



Power Button Logic





Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: ON/OFF / LID SW

Size	Document Number	Rev
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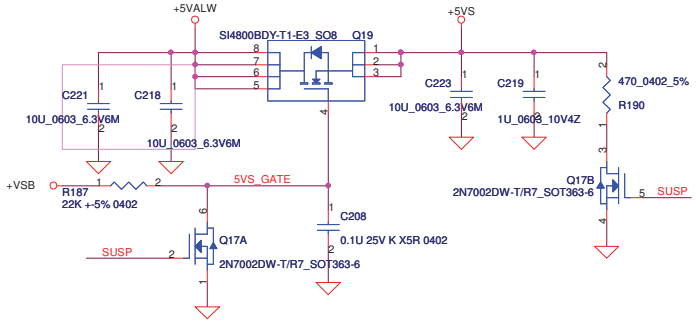
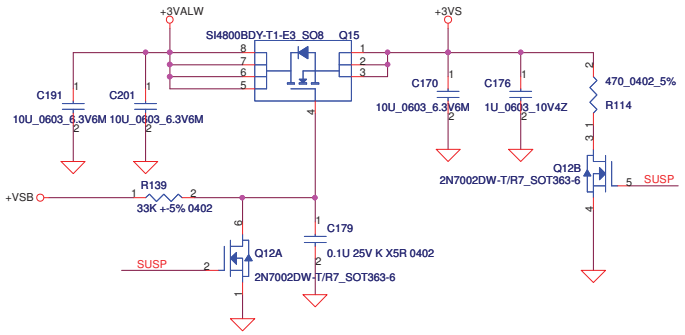
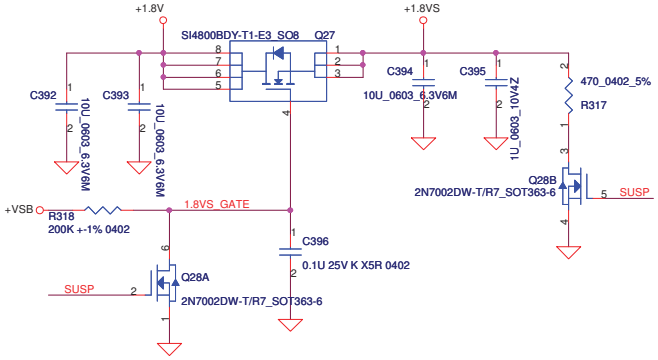
+5VALW TO +5VS

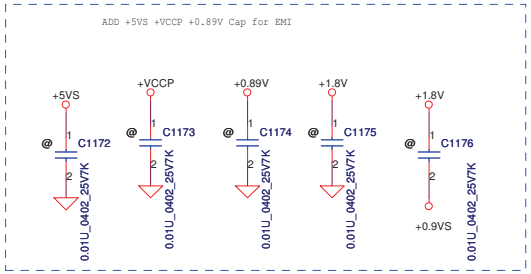


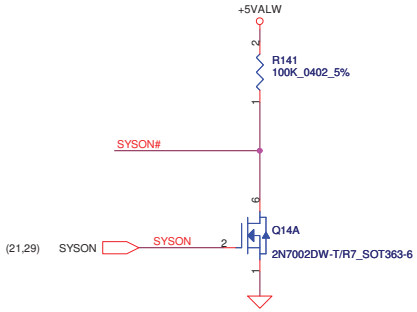
+3VALW TO +3VS

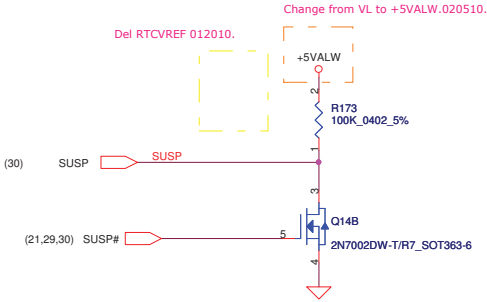


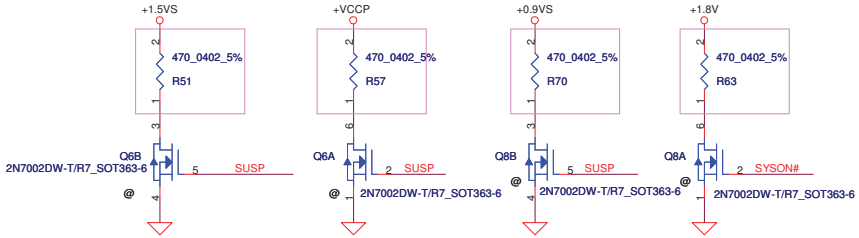
+1.8V to +1.8VS











Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: DC INTERFACE

Size	Document Number	Rev
B	NAV51 LA-6311P	0.2

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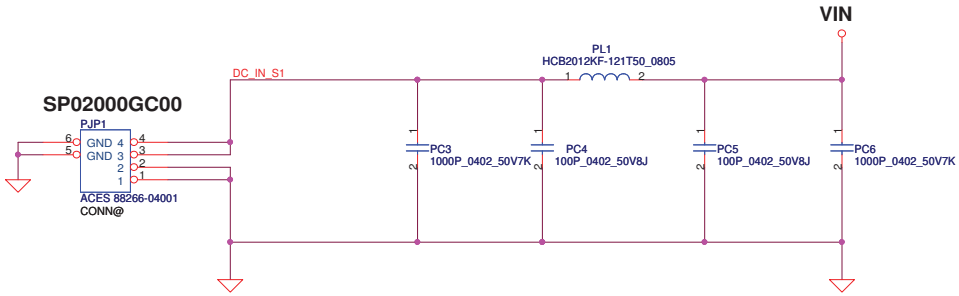

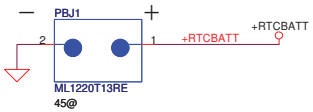

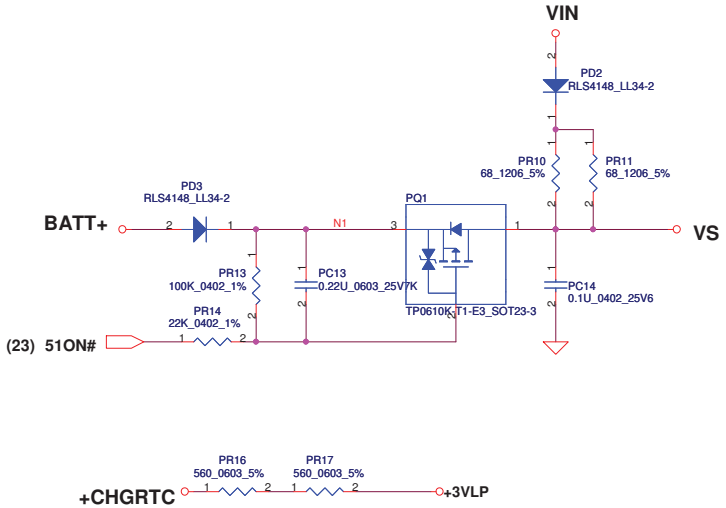

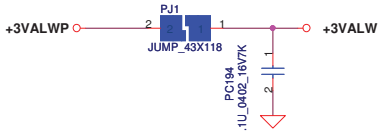

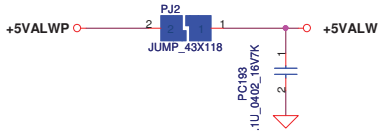

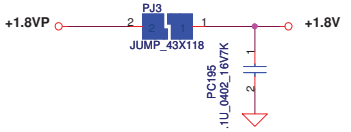

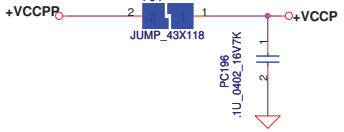

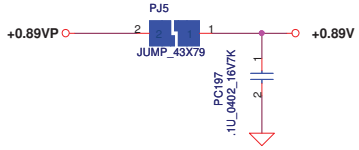

Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Compal Electronics, Inc.

Title: DCIN & DETECTOR

Size	Document Number	Rev
Custom	NAV51 LA-6311P	0.1

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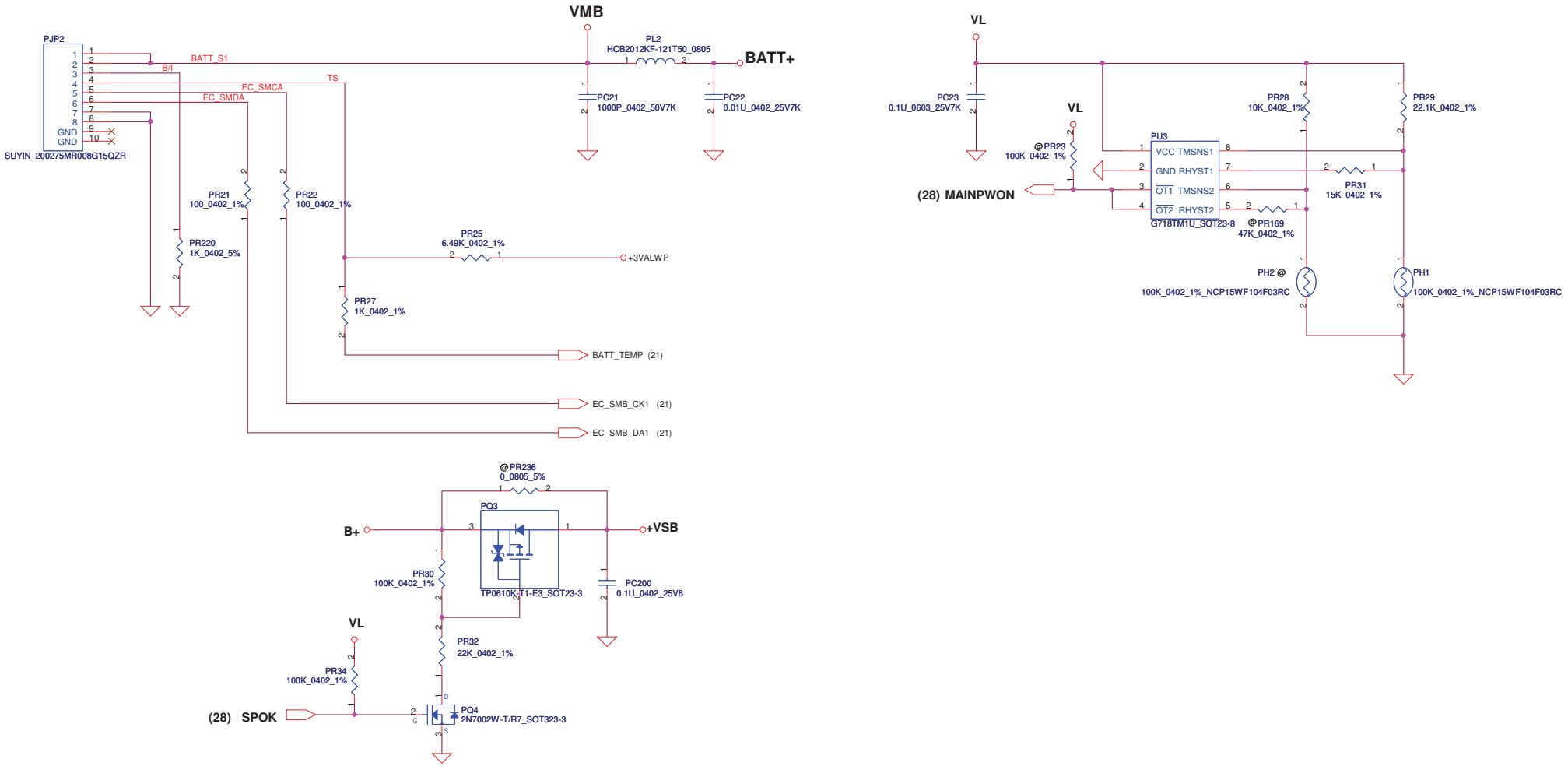
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 72 degree C



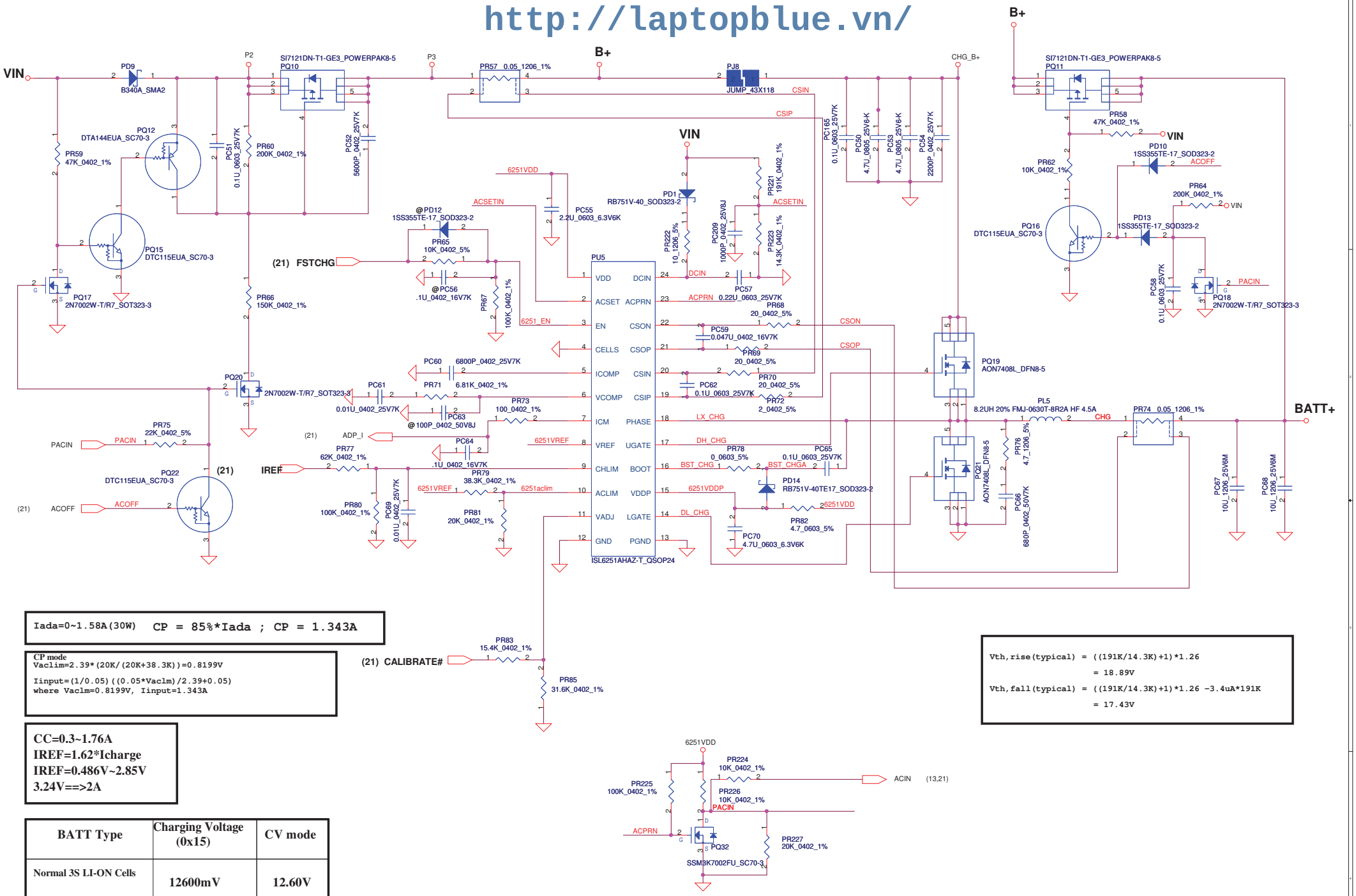
Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size	Document Number	Rev
Custom	NAV51 LA-6311P	0.1

Date: Wednesday, April 14, 2010 | Sheet 26 of 33



Iada=0~1.58A(30W) CP = 85%*Iada ; CP = 1.343A

CP mode
Vaclim=2.39*(20K/(20K+38.3K))=0.8199V

Iinput=(1/0.05)((0.05*Vaclm)/2.39+0.05)
where Vaclm=0.8199V, Iinput=1.343A

CC=0.3~1.76A
IREF=1.62*Icharge
IREF=0.486V~2.85V
3.24V==>2A

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

VADJ-->VREF-->4.41V

VADJ--->Ground--->3.99V

Vcell=(0.175*VADJ+3.99)

Vth,rise(typical) = ((191K/14.3K)+1)*1.26
= 18.89V

Vth,fall(typical) = ((191K/14.3K)+1)*1.26 -3.4uA*191K
= 17.43V

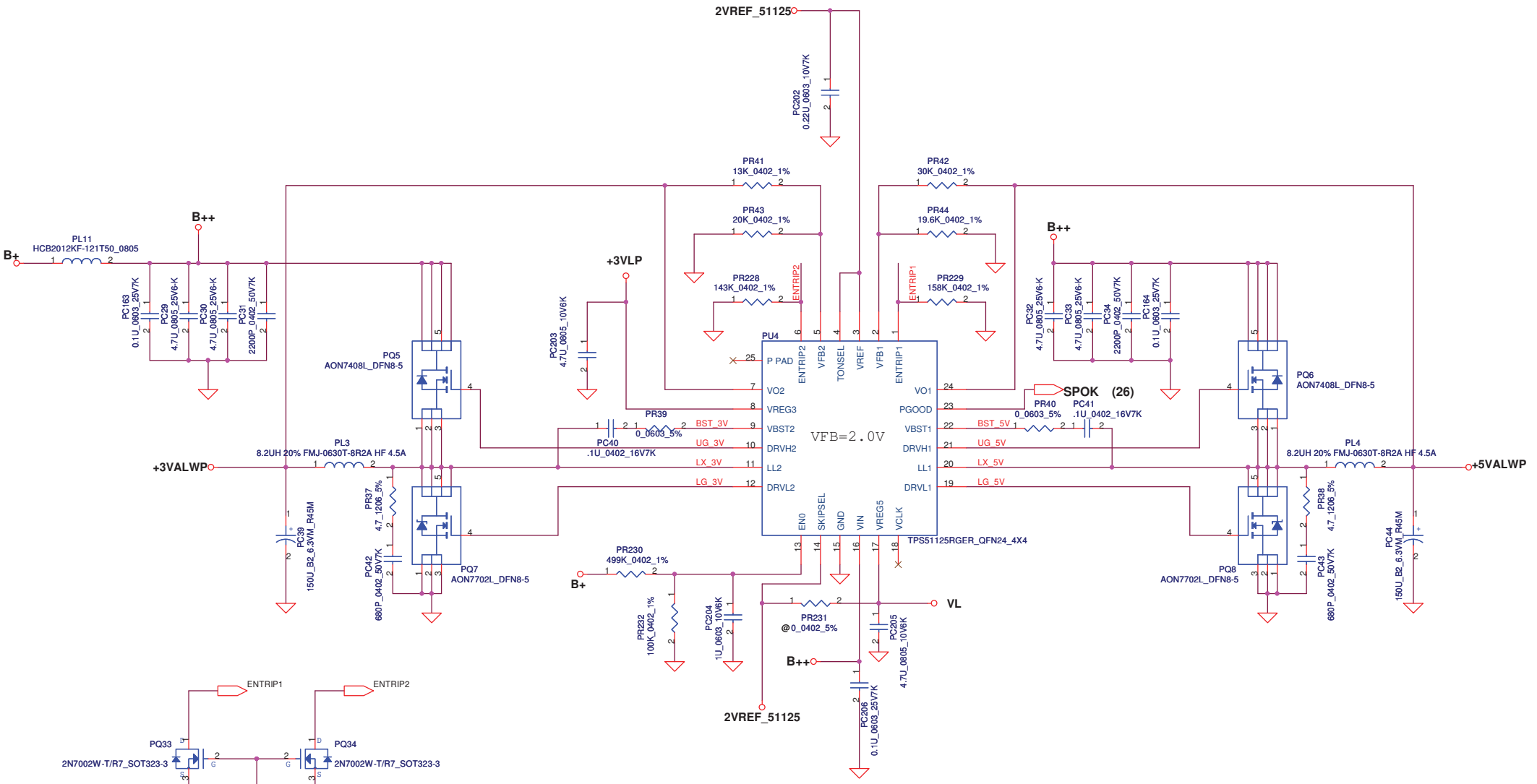
Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Compal Electronics, Inc.

Title: CHARGER

Size: Custom | Document Number: NAV51 LA-6311P | Rev: 0.1

Date: Wednesday, April 14, 2010 | Sheet 27 of 33



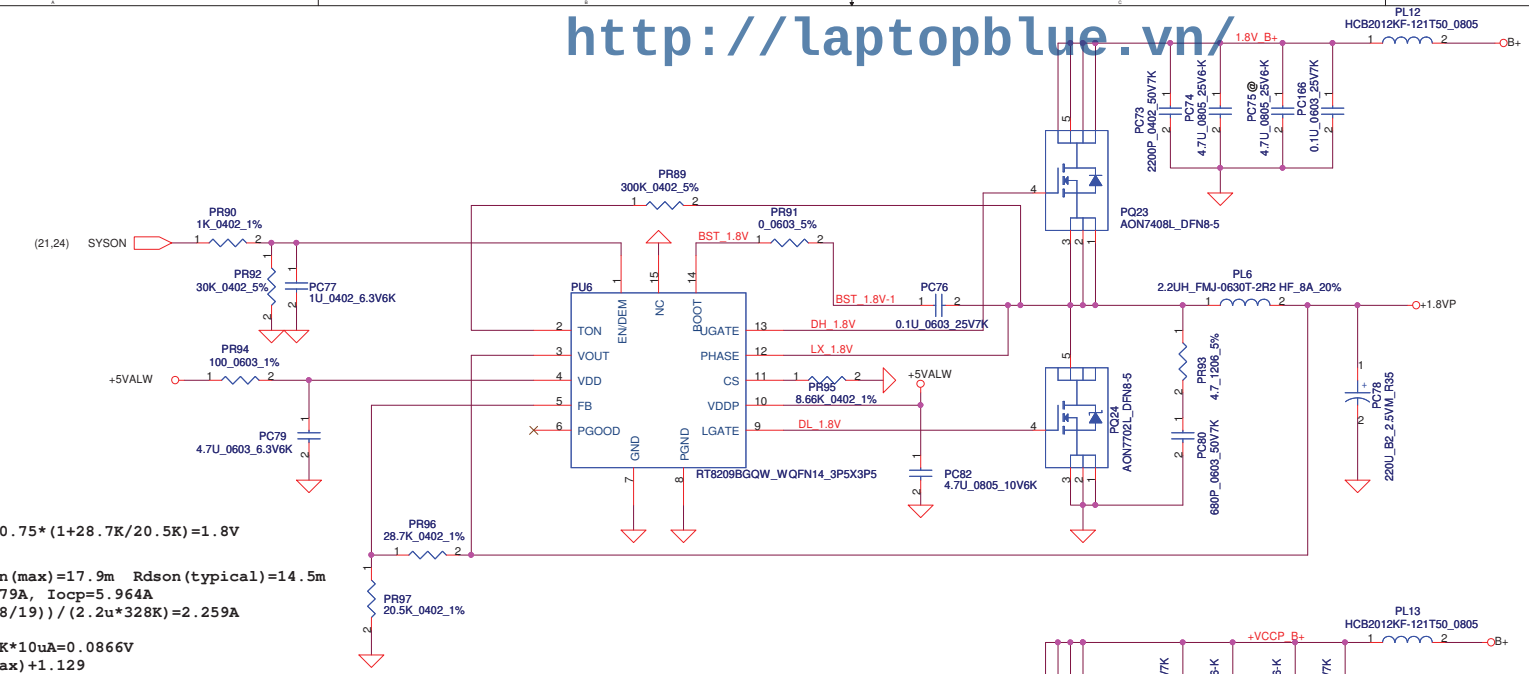
+3.3VALWP Ipeak=5.731A Imax=4.012A
Rds(on)=17.9m ohm(max) ; Rds(on)=14.5m ohm(typical)
Vtrip=(10E-06 * 130K)/9-24mV=134.9mV
Ilimit=134.9mV/17.9m ~134.9mV/14.5m x 1.2
=7.536A ~ 7.752A
Iocp=Ilimit+Delta I/2
=8.081A ~ 8.297A
Delta I=1.090A (Freq=305KHz)

+5VALWP Ipeak=7.0A Imax=4.9A
Rds(on)=17.9m ohm(max) ; Rds(on)=14.5m ohm(typical)
Vtrip=(10E-06 * 147K)/9-24mV=151mV
Ilimit=151mV/17.9m ~151mV/14.5m x 1.2
=8.467A ~ 8.710A
Iocp=Ilimit+Delta I/2
=9.384A ~ 9.627A
Delta I=1.834A (Freq=245KHz)

Security Classification	Compal Secret Data		
Issued Date	2007/11/12	Deciphered Date	2008/11/12

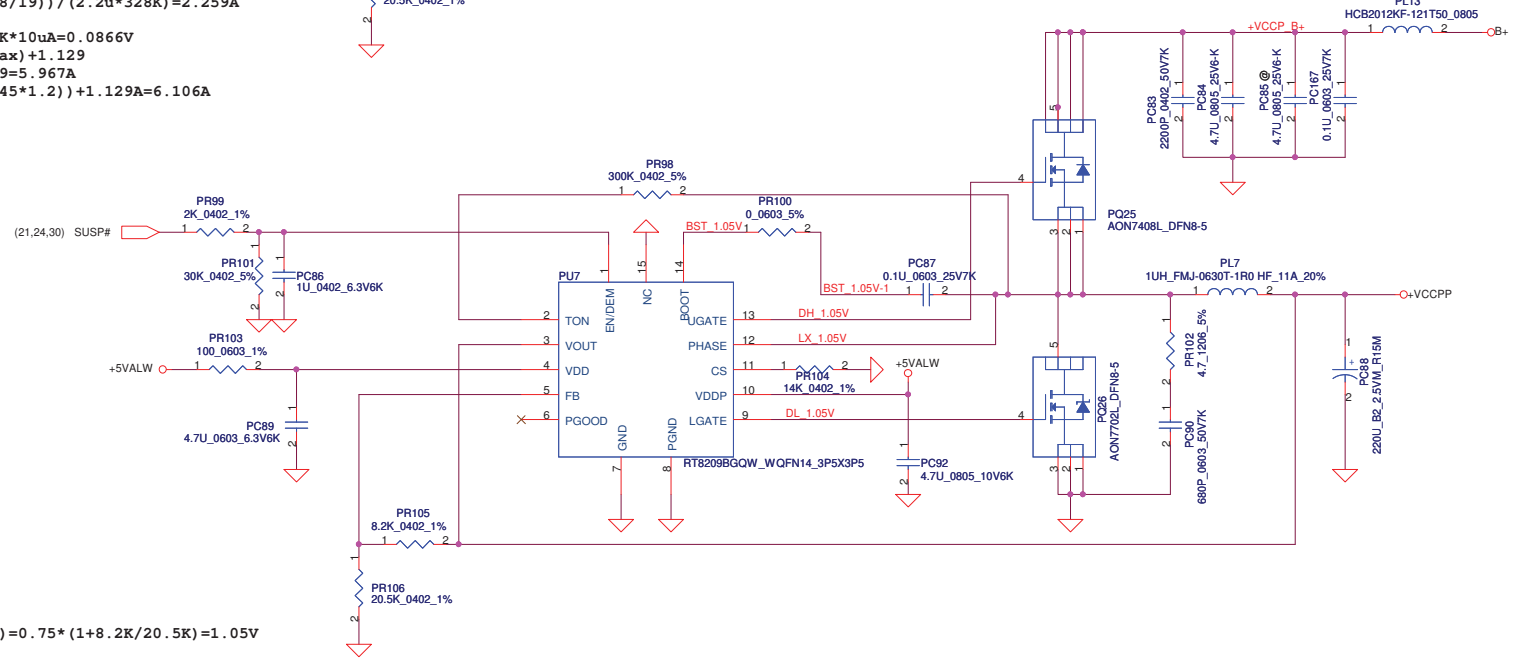
Compal Electronics, Inc.

Title	+5V/+3V	
Size: Custom	Document Number: NAV50	Rev: 0.1
Date: Wednesday, April 14, 2010	Sheet 28 of 33	



<Vo=1.8V> VFB=0.75V
Vo=VFB*(1+PR96/PR97)=0.75*(1+28.7K/20.5K)=1.8V
Fsw=328KHz

Cout ESR=15m ohm Rdson(max)=17.9m Rdson(typical)=14.5m
Ipeak=4.97A, Imax=3.479A, Iocp=5.964A
Delta I=((19-1.8)*(1.8/19))/(2.2u*328K)=2.259A
=>1/2DeltaI=1.129A
Vtrip=Rtrip*10uA=8.66K*10uA=0.0866V
Iocpmin=Vtrip/(Rdsonmax)+1.129
=0.0866/(0.0179)+1.129=5.967A
Iocpmax=(0.0866/(0.0145*1.2))+1.129A=6.106A
Iocp=5.967A~6.106A



<Vo=1.05V> VFB=0.75V
Vo=VFB*(1+PR105/PR106)=0.75*(1+8.2K/20.5K)=1.05V
Fsw=280KHz

Cout ESR=15m ohm Rdson(max)=17.9m Rdson(typical)=14.5m
Ipeak=3.124A, Imax=2.187A, Iocp=3.749A
Delta I=((19-1.05)*(1.05/19))/(1.5u*280K)=3.549A
=>1/2DeltaI=1.774A
Vtrip=Rtrip*10uA=14K*10uA=0.14V
Iocpmin=Vtrip/(Rdsonmax)+1.774
=0.14/(0.0179)+1.774=9.596A
Iocpmax=(0.14/(0.0145*1.2))+1.774A=9.820A
Iocp=9.596A~9.820A

Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Compal Electronics, Inc.

Title: 1.8VP / +VCCPP

Size	Document Number	Rev
Custom	NAV51 LA-6311P	0.1

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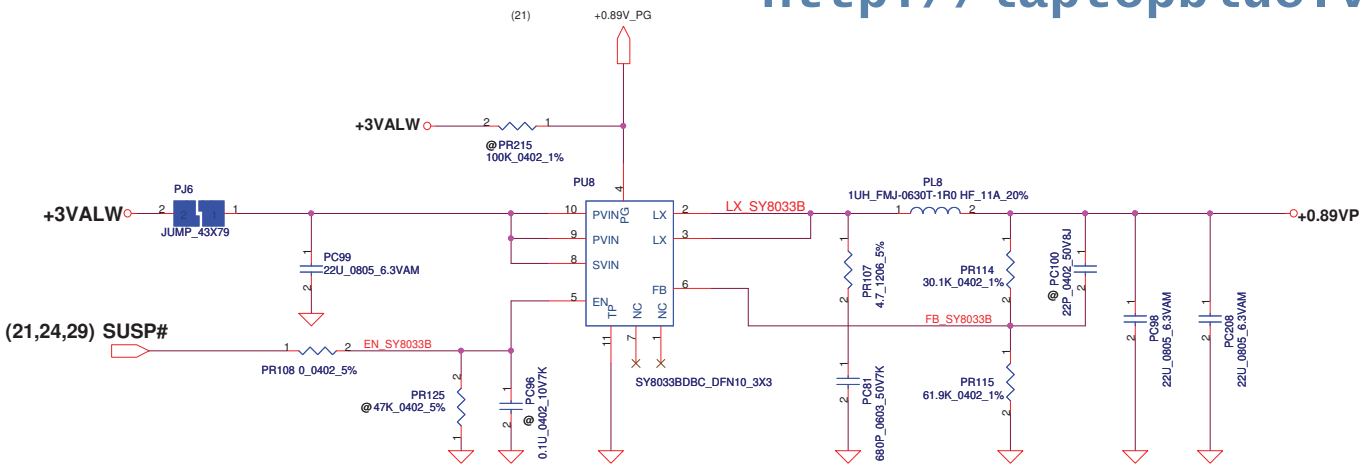
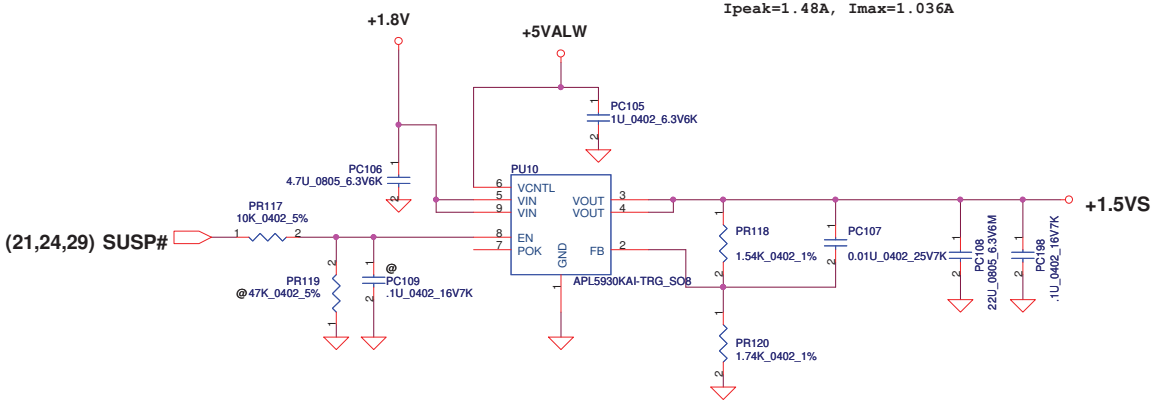
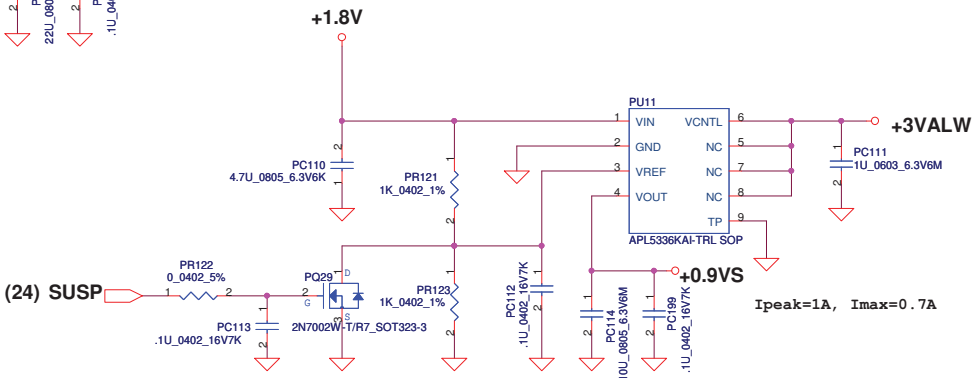


<Vo=0.89V> VFB=0.6V
Vo=VFB*(1+PR114/PR115)=0.6*(1+30.1K/61.9)=0.89V
Ipeak=2.64A, Imax=1.848A

Ipeak=1.48A, Imax=1.036A





Ipeak=1A, Imax=0.7A

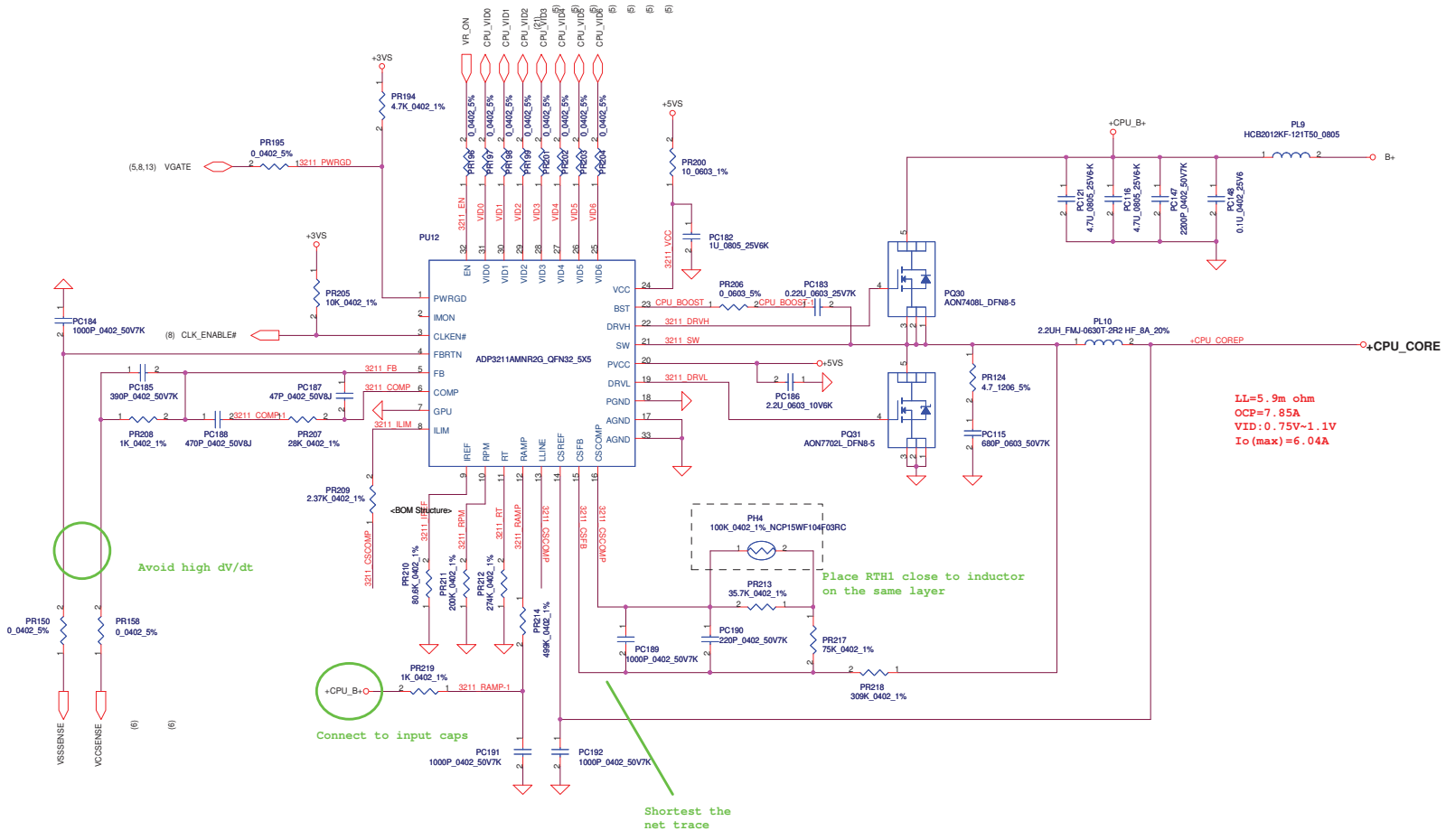
Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Compal Electronics, Inc.

Title: +0.89VP/+1.5VS/+0.9VSP

Size	Document Number	Rev
Custom	NAV51 LA-6311P	0.1

Date: Wednesday, April 14, 2010 | Sheet 30 of 33



Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Compal Electronics, Inc.

Title: +CPU_CORE

Size	Document Number	Rev
C	NAV51 LA-6311P	0.1

Date: Wednesday, April 14, 2010 Sheet 31 of 33

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1						2010.1.8	EVT
2						2010.1.11	EVT
3							
4							
5							
6							
7							
8							
9							
10							
11							
12							
13							
14							
15							
16							
17							
18							
19							
20							
21							
22							
23							

Security Classification	Compal Secret Data		
Issued Date	2006/08/04	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title	PIR_HW	
Size: Custom	Document Number: NAV51 LA-6311P	Rev: 1.0
Date: Wednesday, April 14, 2010	Sheet 32 of 33	

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	PU8 Vin change to +3VALW	modify for HW layout request	0.1	30		2010.1.8	EVT
2	PU4 Pin25 change to no connect	modify for 3/5V load balance(TI FAE request)	0.1	28		2010.1.11	EVT
3							
4							
5							
6							
7							
8							
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21							
22							
23							

Compal Electronics, Inc.		
Title: PIR (PWR)		
Size: Custom	Document Number: NAV51 LA-6311P	Rev: 0.1
Date: Wednesday, April 14, 2010	Sheet 33 of 33	