MS-7510 Version : 0B Diamond Edition

CPU :

Intel Conroe Family and Kentsfield Family Processor
Intel Pentium D Processor 900 and 800 Sequence
Intel Pentium 4 Processor 600 Sequence

System Chipset :

nVidia C72XE [C55 + BR04]
nVidia MCP55P

On Board Chipset :

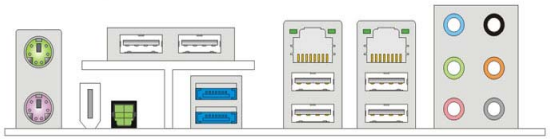
Azalia Codec - RealTek ALC885
GB PHY 1 -- RealTek RTL8211BL
GB PHY 2 -- RealTek RTL8211BL
VRM 11 - Intersil ISL6322
ACPI Controller -- uPI Solution
IEEE 1394a Controller -- JMicron JMB381
eSATA Controller -- JMicron JMB363
Super I/O -- FinTek F71882FG
SPI Flash 8Mb

Main Memory :

2 Channel DDR II * 4 (Max 8GB)

Expansion Slot :

PCI Express x16 Slot * 3
PCI Express x8 Slot * 1
PCI Express x1 Slot * 2
PCI Slot * 1

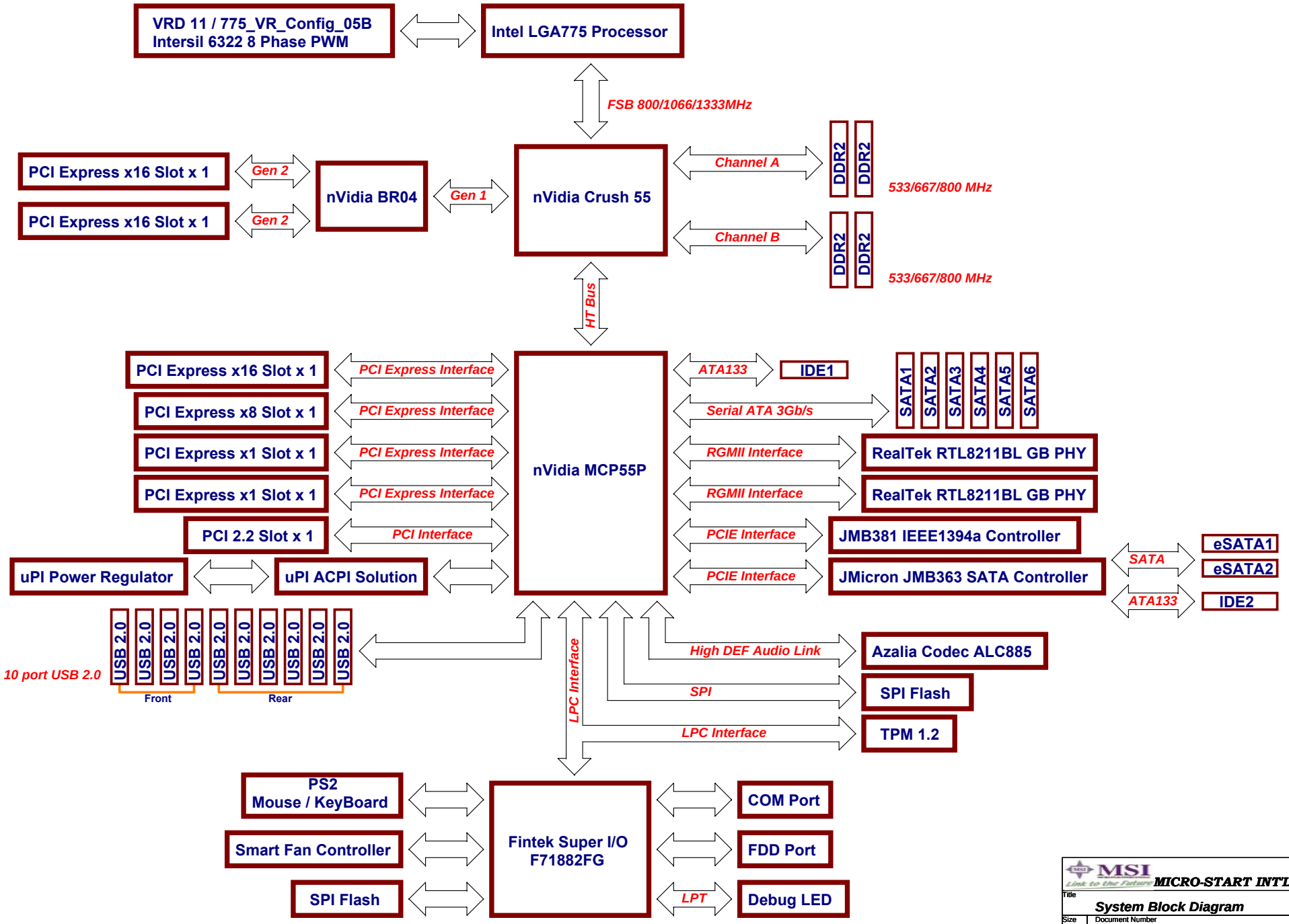


ERP No.	Config Item	PlatForm or Option	Option Select
7510-01S	Cfg-STD	C55 + BR04 + MCP55P + ALC885 + RTL8211BP + JMB381 + JMB363 + F71882FG	STD

MSI MICRO-START INT'L CO.,LTD.
Link to the Future

Title		
Cover Sheet		
Size	Document Number: MS-7510	Rev: 0B
Date: Tuesday, October 30, 2007	Sheet 1 of 41	

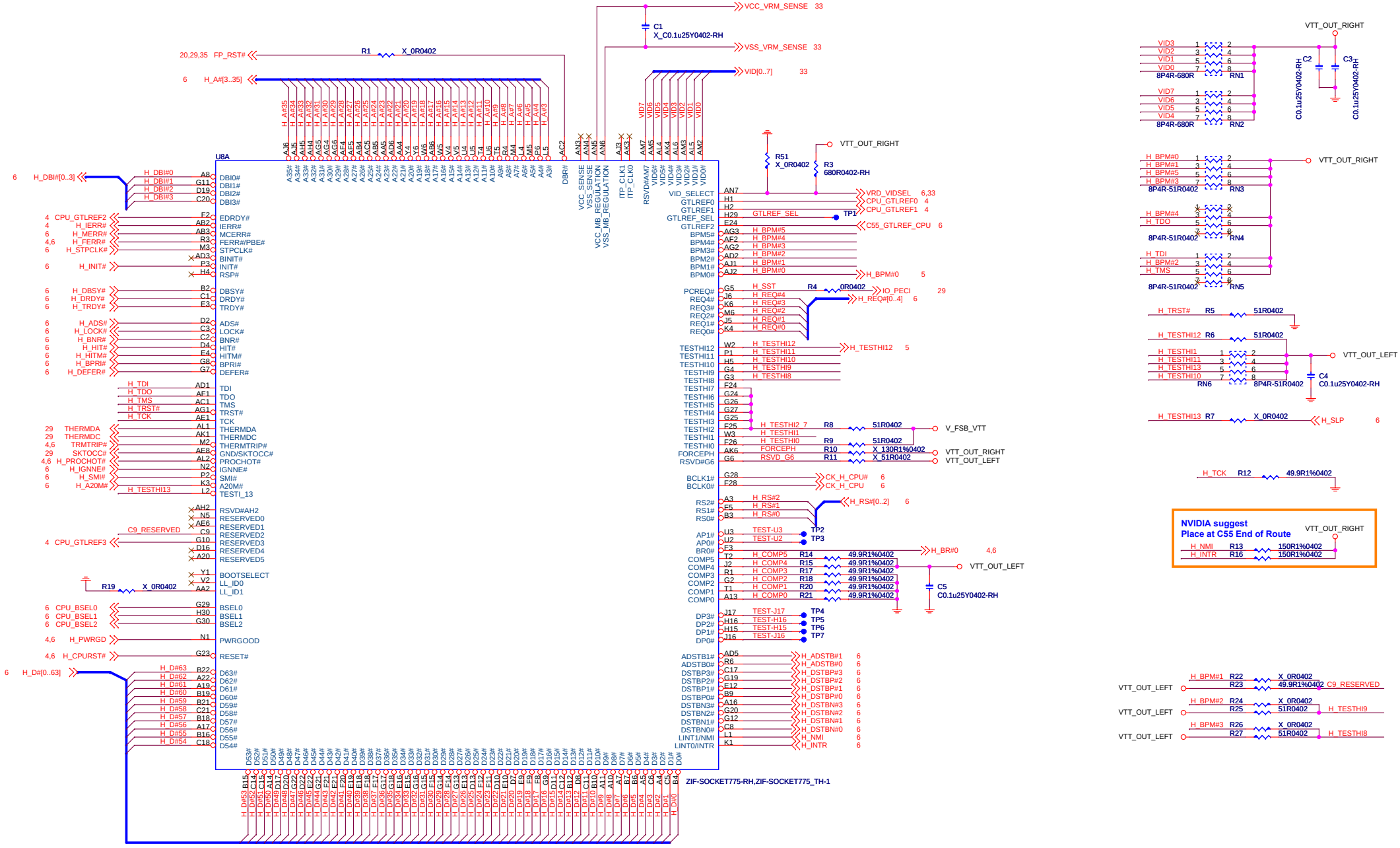
System Block Diagram



MICRO-START INT'L CO.,LTD.

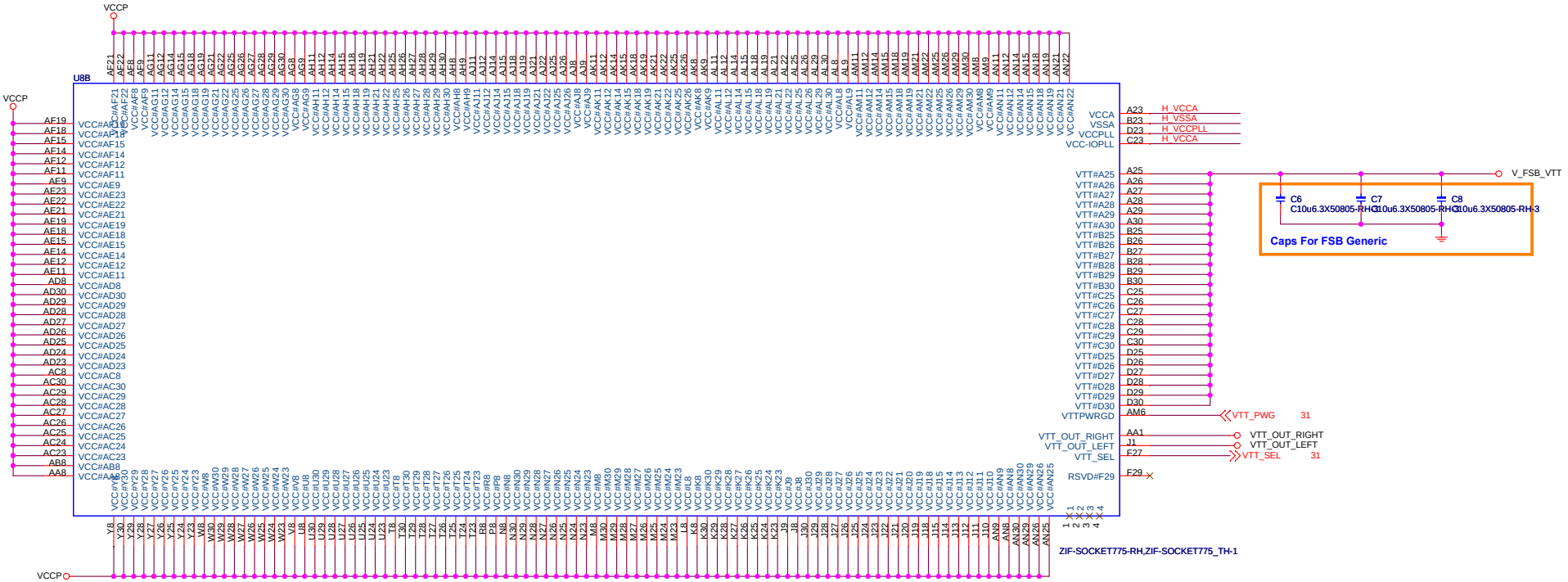
Title: System Block Diagram		
Size	Document Number: MS-7510	Rev: 0B
Date: Tuesday, October 30, 2007	Sheet 2 of 41	

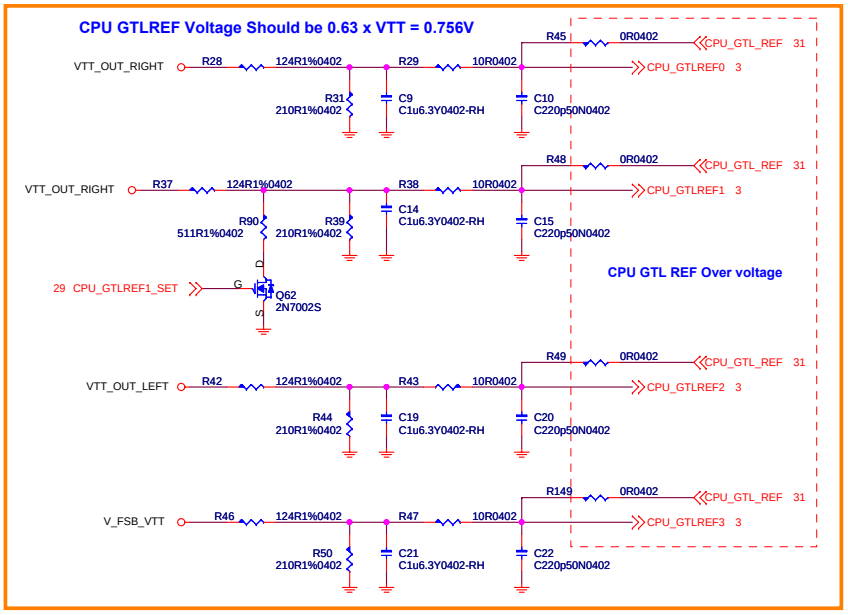
CPU LGA775 - Signals

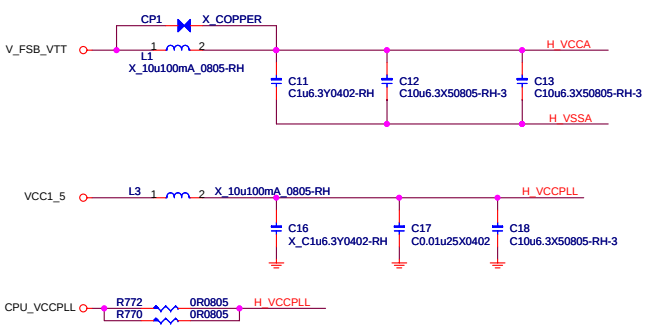


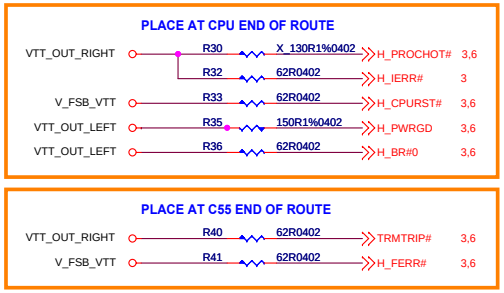
MSI MICRO-START INT'L CO.,LTD.			
Title: CPU LGA775 - Signals			
Size	Document Number: MS-7510		Rev: 0B
Date: Tuesday, October 30, 2007		Sheet 3 of 41	

CPU LGA775 - Power









MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title	CPU LGA775 - Power	
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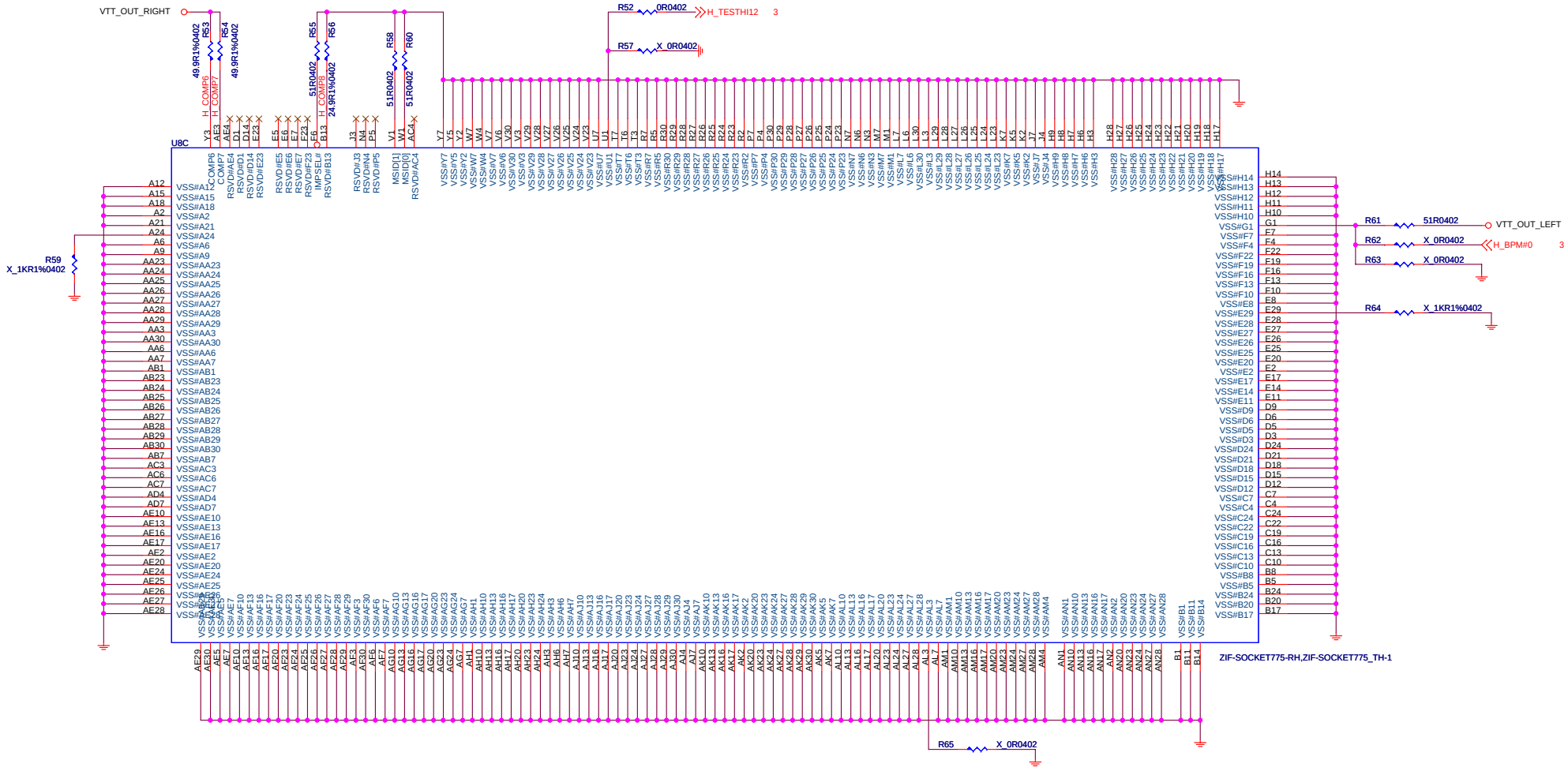
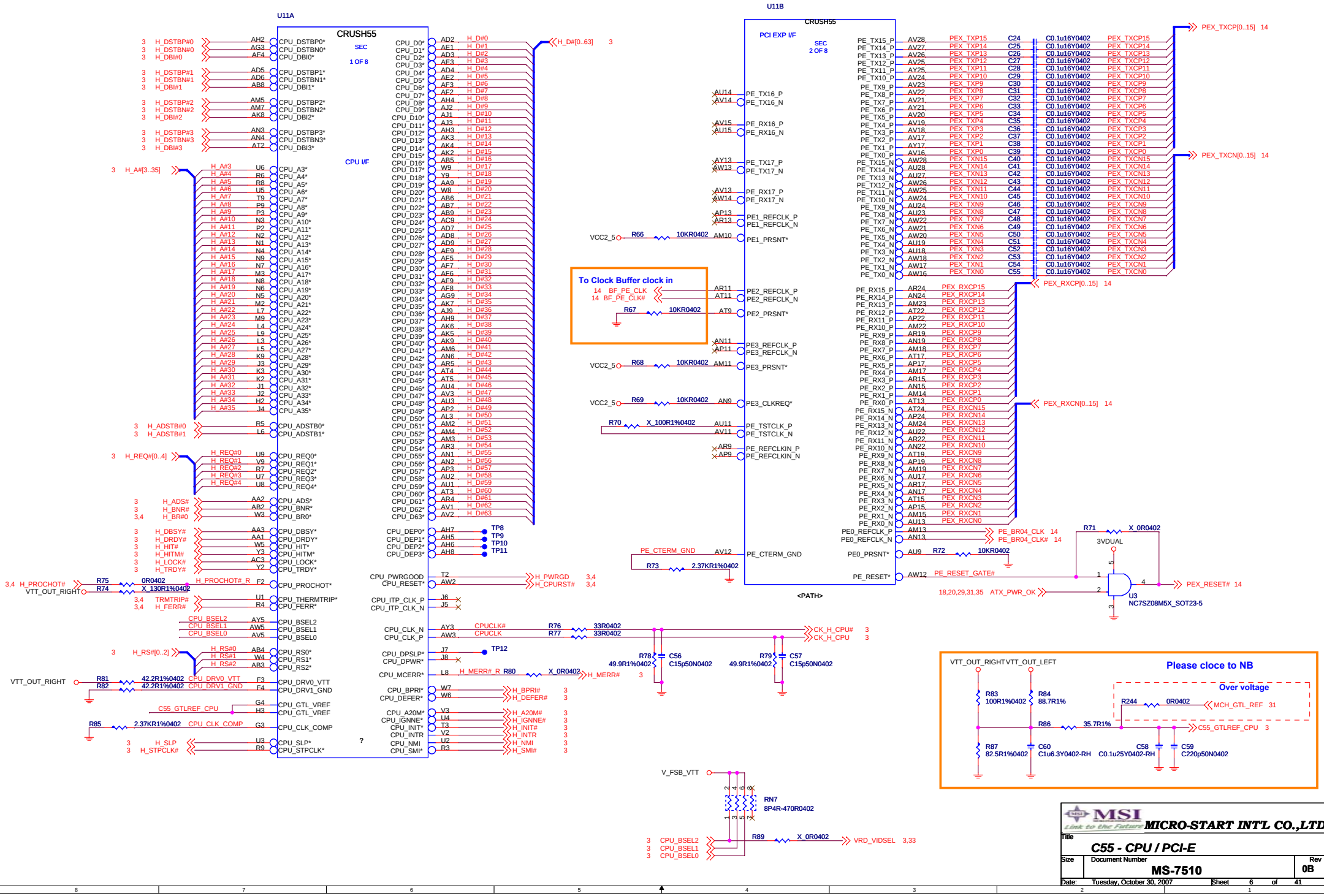
CPU LGA775 - Gnd

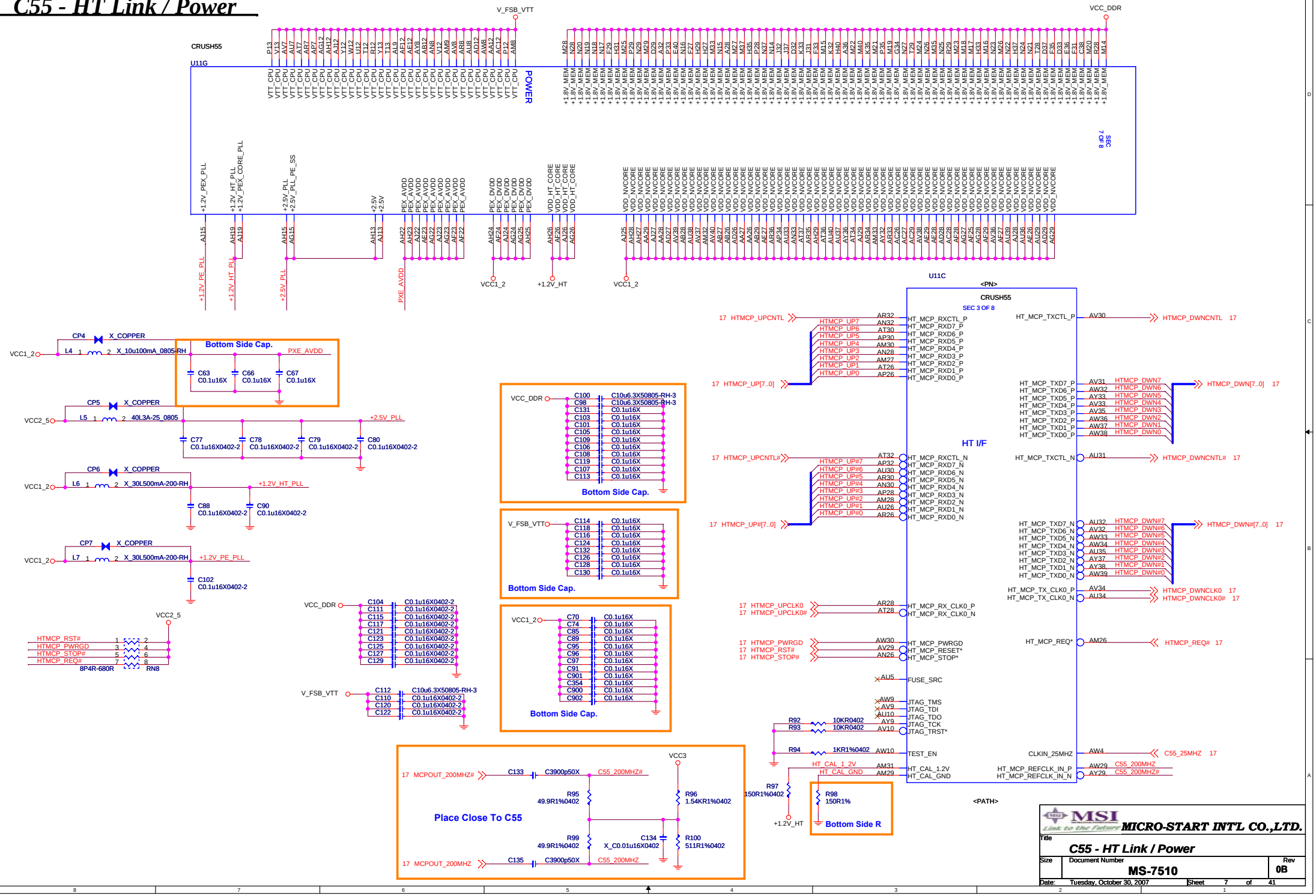


MICRO-START INT'L CO.,LTD.			
Title: CPU LGA775 - Gnd			
Size	Document Number: MS-7510		Rev: 0B
Date: Tuesday, October 30, 2007		Sheet 5 of 41	

C55 - CPU / PCI-E

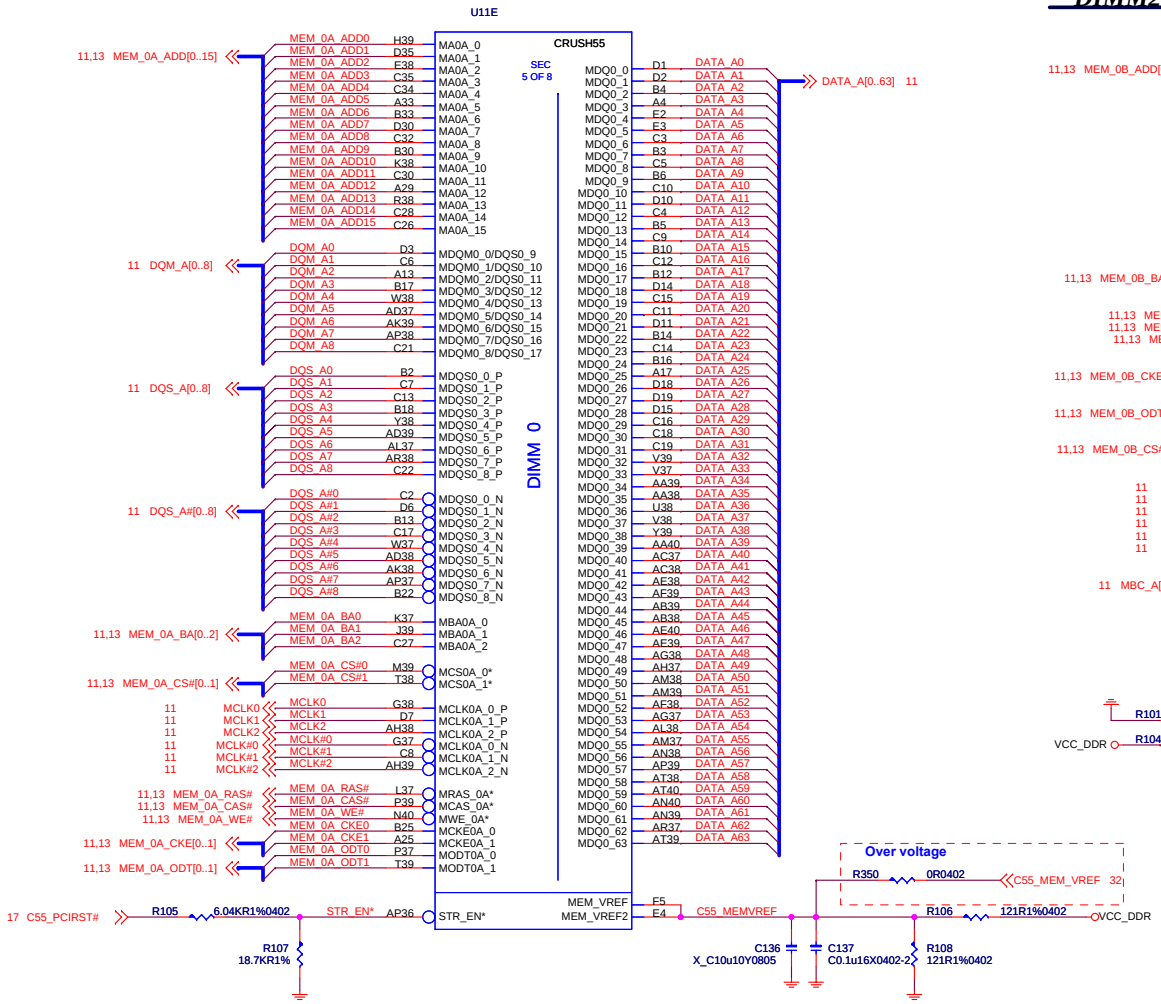

U11A
CRUSH55
SEC
1 OF 8
CPU I/F
U11B
CRUSH55
PCI EXP I/F
SEC
2 OF 8
To Clock Buffer clock in
<PATH>
Please cloce to NB
Over voltage
MICRO-START INT'L CO.,LTD.
C55 - CPU / PCI-E
MS-7510
0B
Tuesday, October 30, 2007

C55 - HT Link / Power

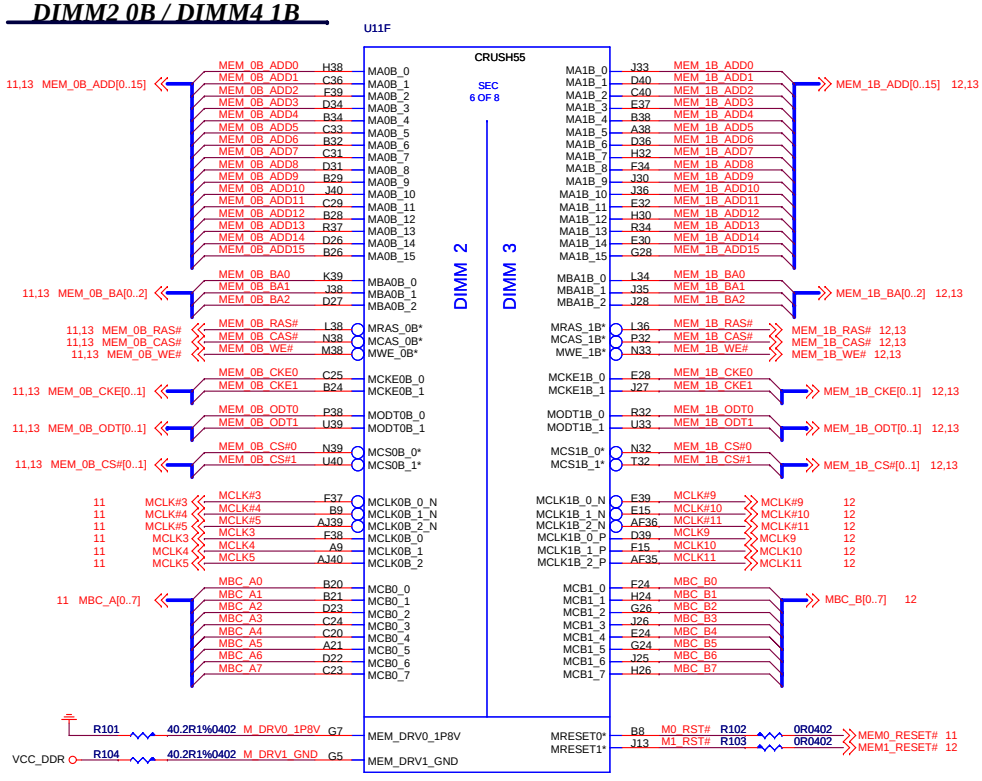


C55 - Memory A0

DIMM1 0A



DIMM2 0B / DIMM4 1B



DATA 0
DATA 1

DIMM 1	ADDR 0A / CNTL 0A	DATA 0
DIMM 2	ADDR 0B / CNTL 0B	DATA 0
DIMM 3	ADDR 1A / CNTL 1A	DATA 1
DIMM 4	ADDR 1B / CNTL 1B	DATA 1

MSI Link to the Future MICRO-START INTL CO.,LTD.

Title	C55 - Memory A0	
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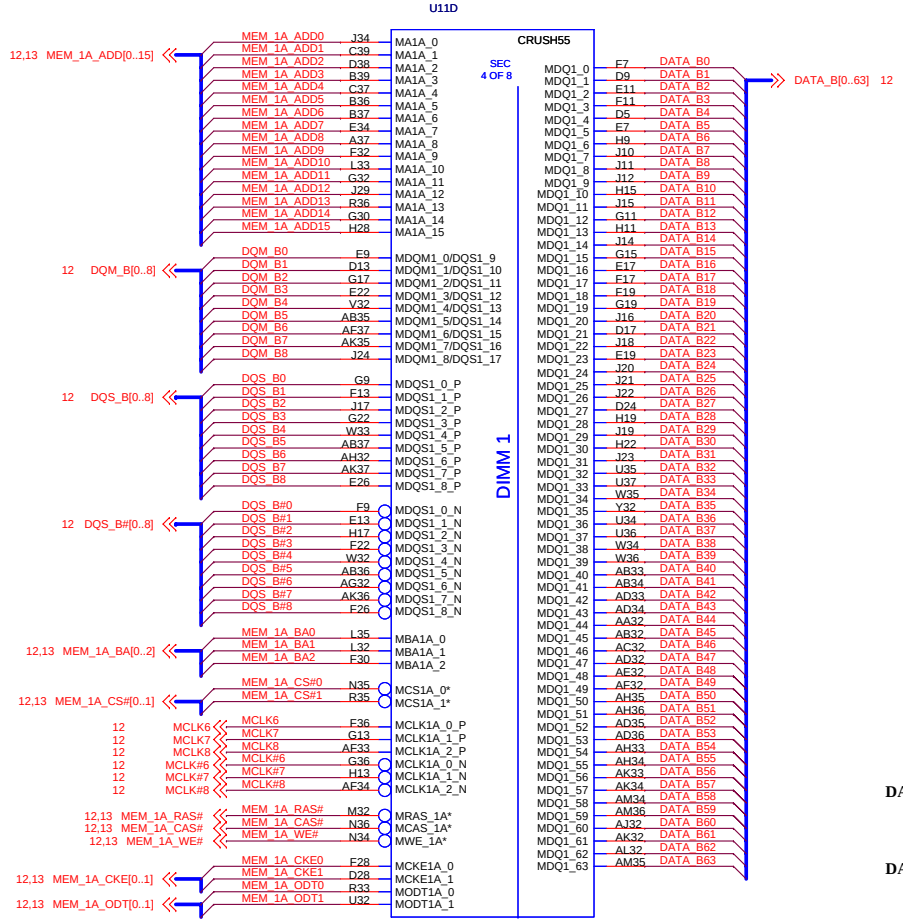
C55 - Memory A1

DIMM3 1A



MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title	C55 - Memory A1	
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C55 - Gnd

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Title: C55 - Gnd			
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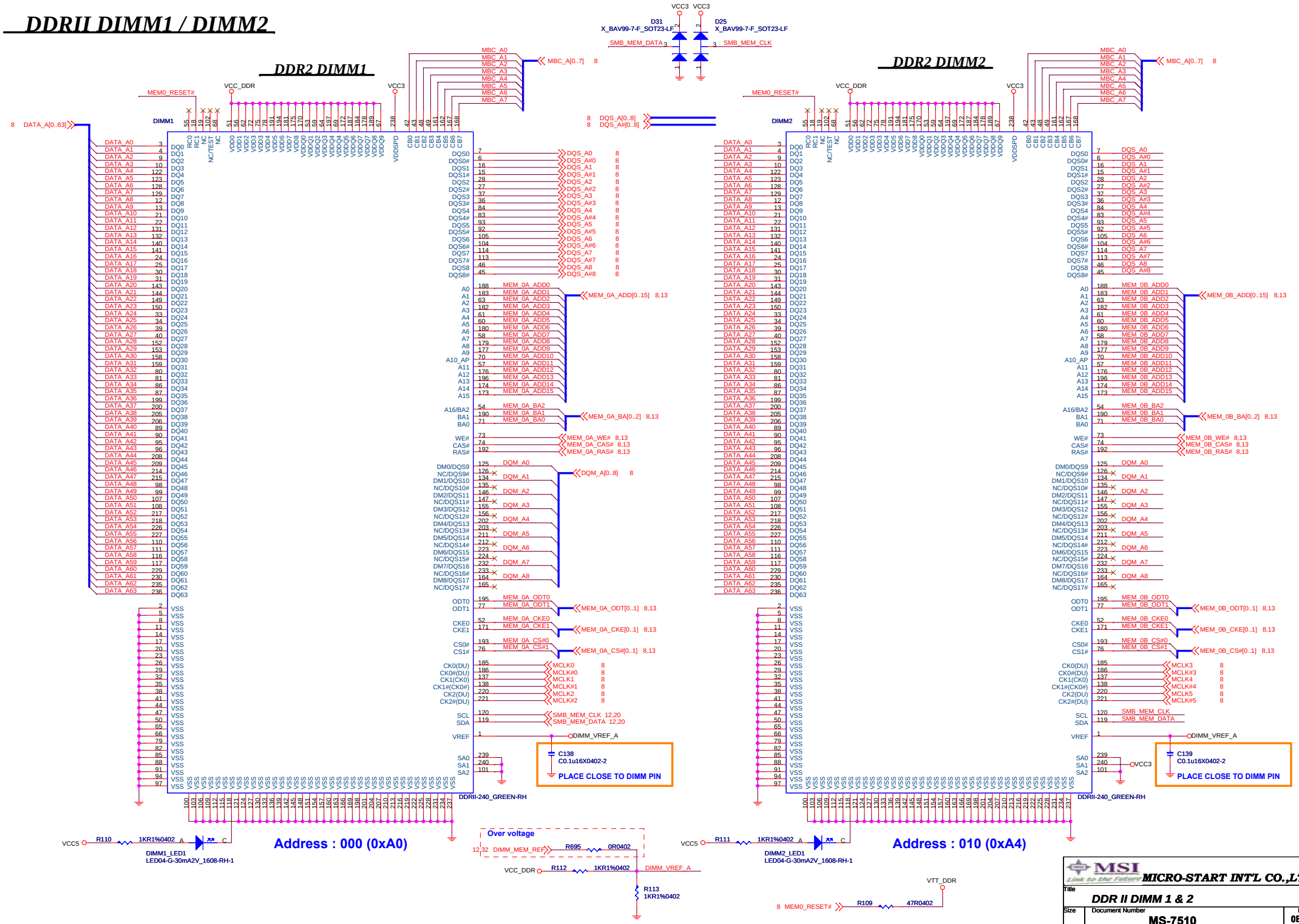
DDRII DIMM1 / DIMM2



MSI Link to the Future **MICRO-START INT'L CO.,LTD.**

Title	DDR II DIMM 1 & 2	
Size	Document Number MS-7510	Rev 0B
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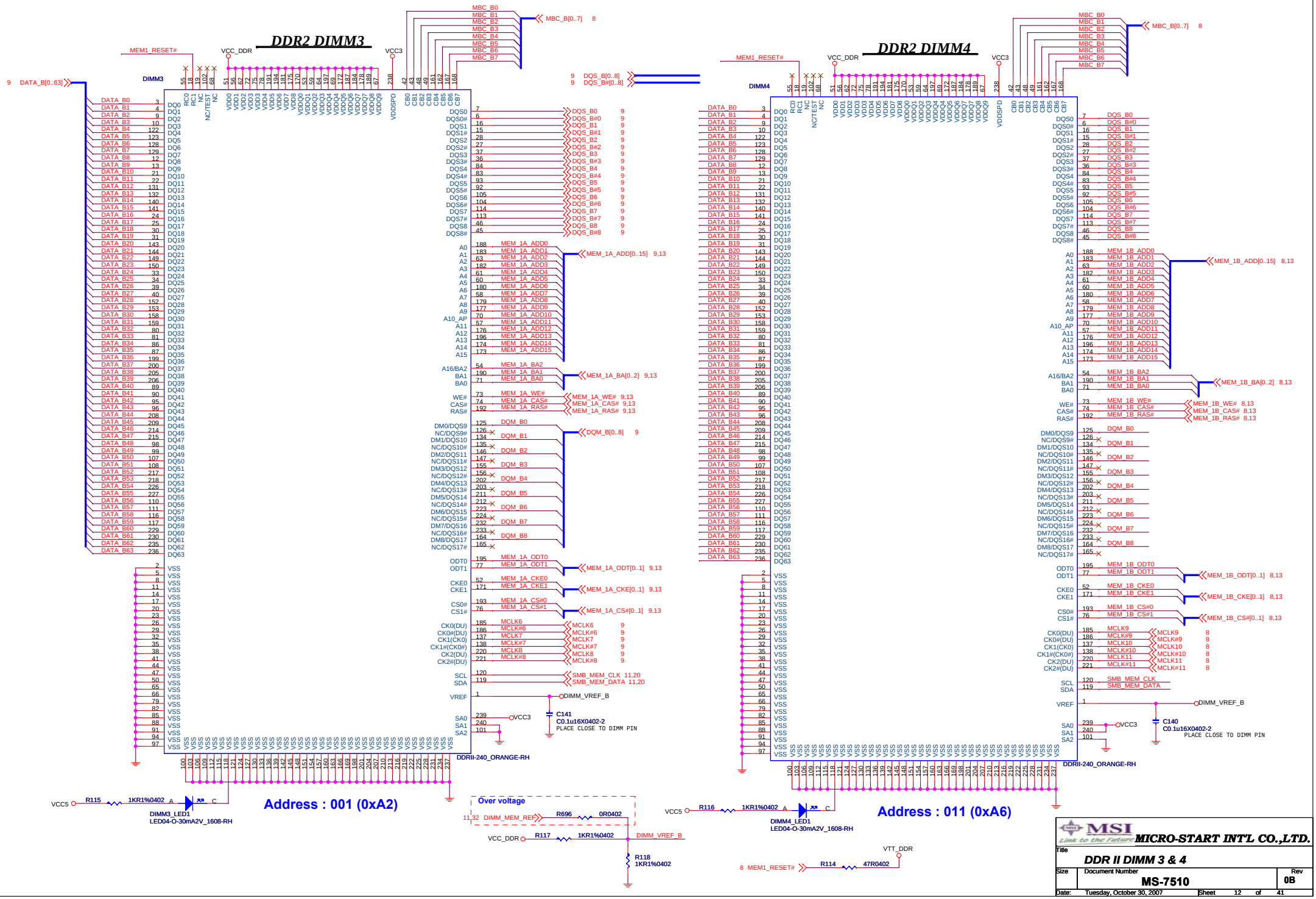
DDRII DIMM3 / DIMM4



MSI Link to the Future **MICRO-START INTL CO.,LTD.**

Title	DDR II DIMM 3 & 4	
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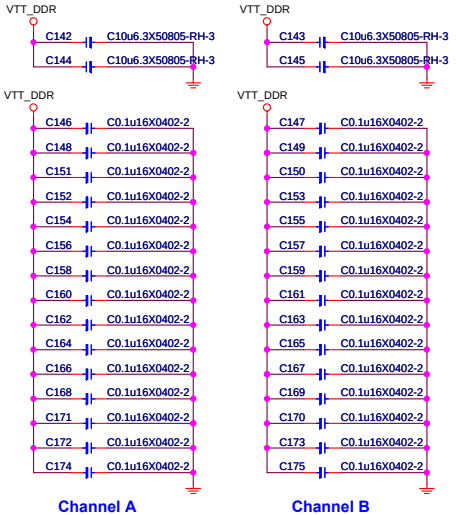
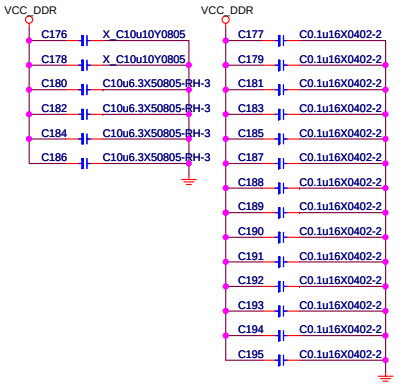
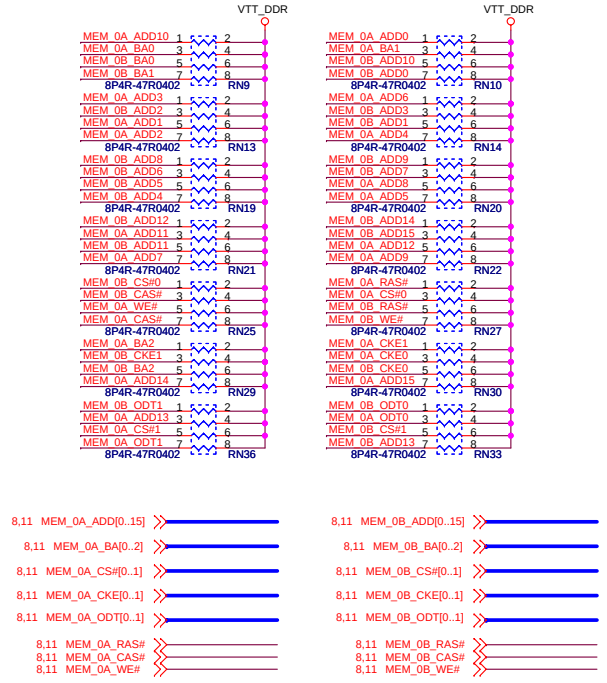
DDR Channel A VTT_DDR Decoulping Caps.



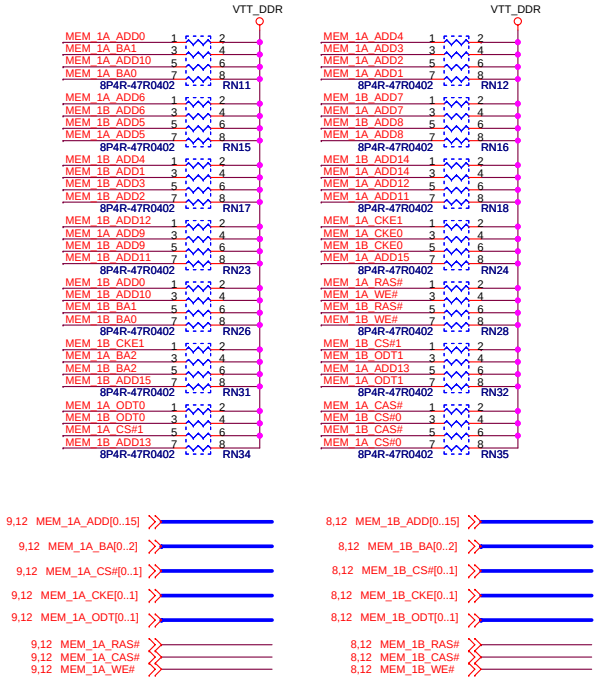
DDR Channel A VCC_DDR Decoulping Caps.



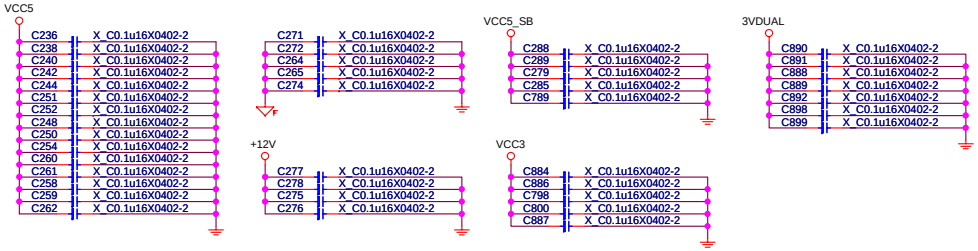
DDR Channel A Termination



DDR Channel B Termination



EMI Solution 2007-10-25



MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: DDR II Termination / EMI		
Size	Document Number: MS-7510	Rev: 0B
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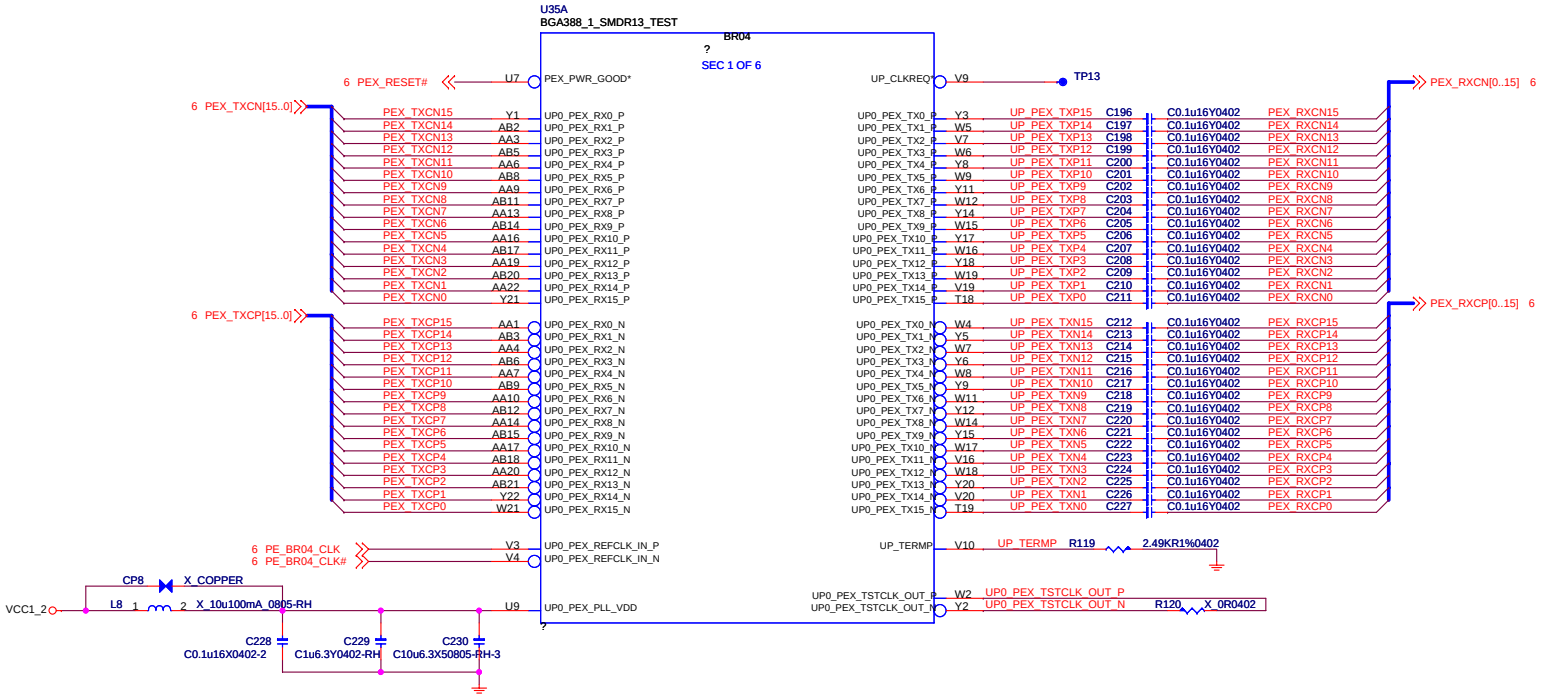
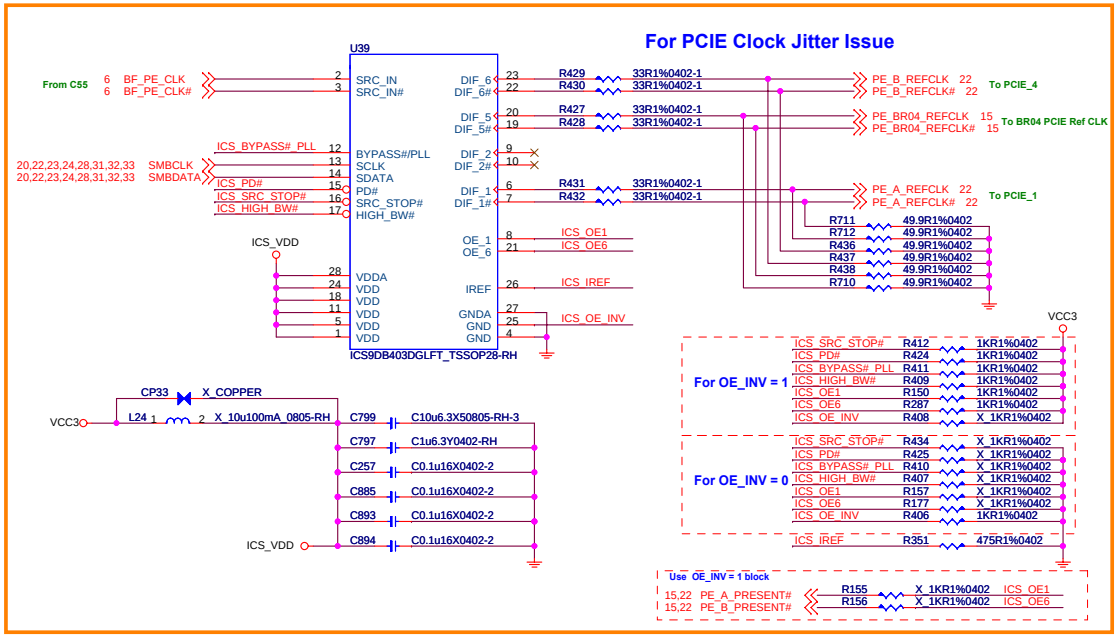
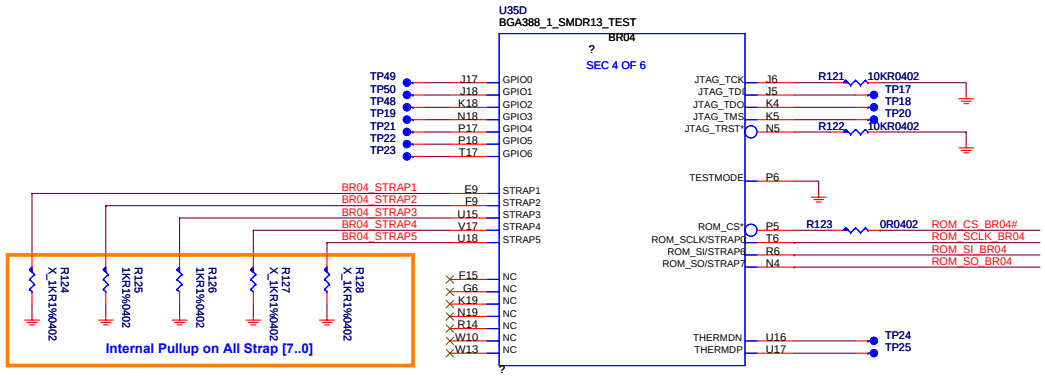
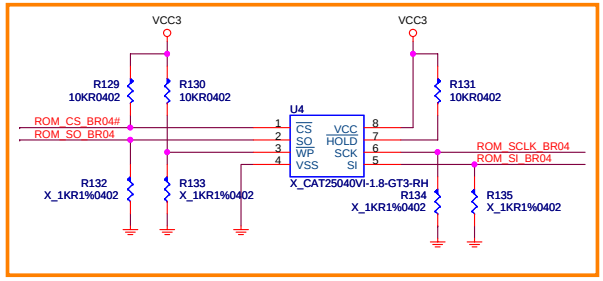
C55 to BR04 PCI-Express Interface









MICRO-START INT'L CO.,LTD.

Title: BR04 - C55 Side

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	MS-7510	0B

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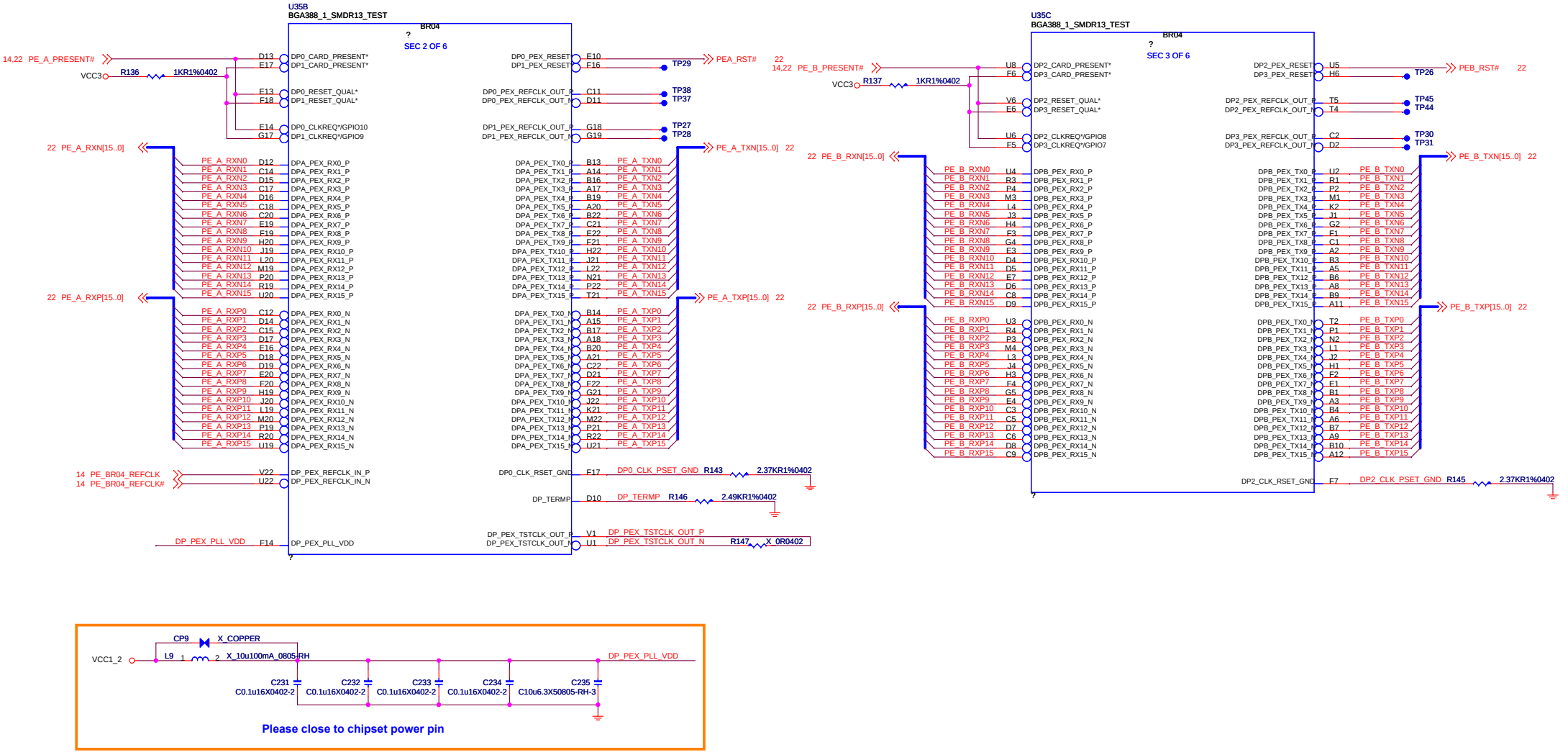
BR04 to PCI-Express Slots



MICRO-START INT'L CO.,LTD.

Title: BR04 - PCIE x16 Slot

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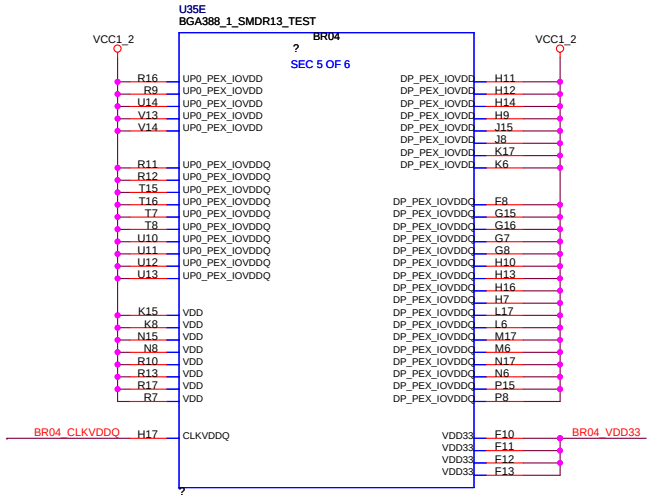
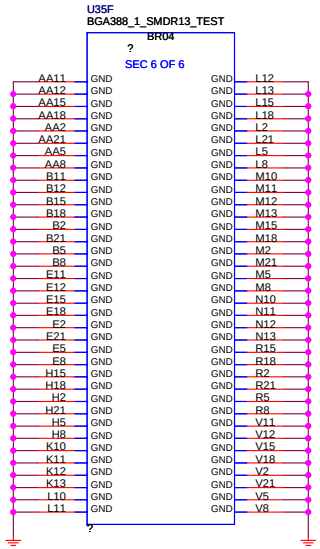
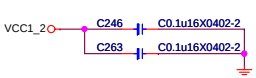
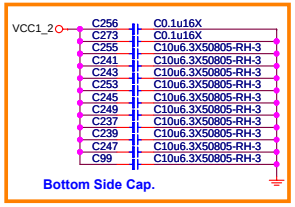
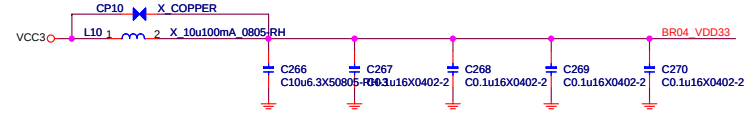
BR04 Power and Gnd Block

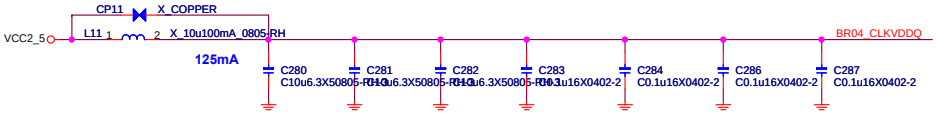












MICRO-START INT'L CO.,LTD.

Title: BR04 - Power / Gnd		
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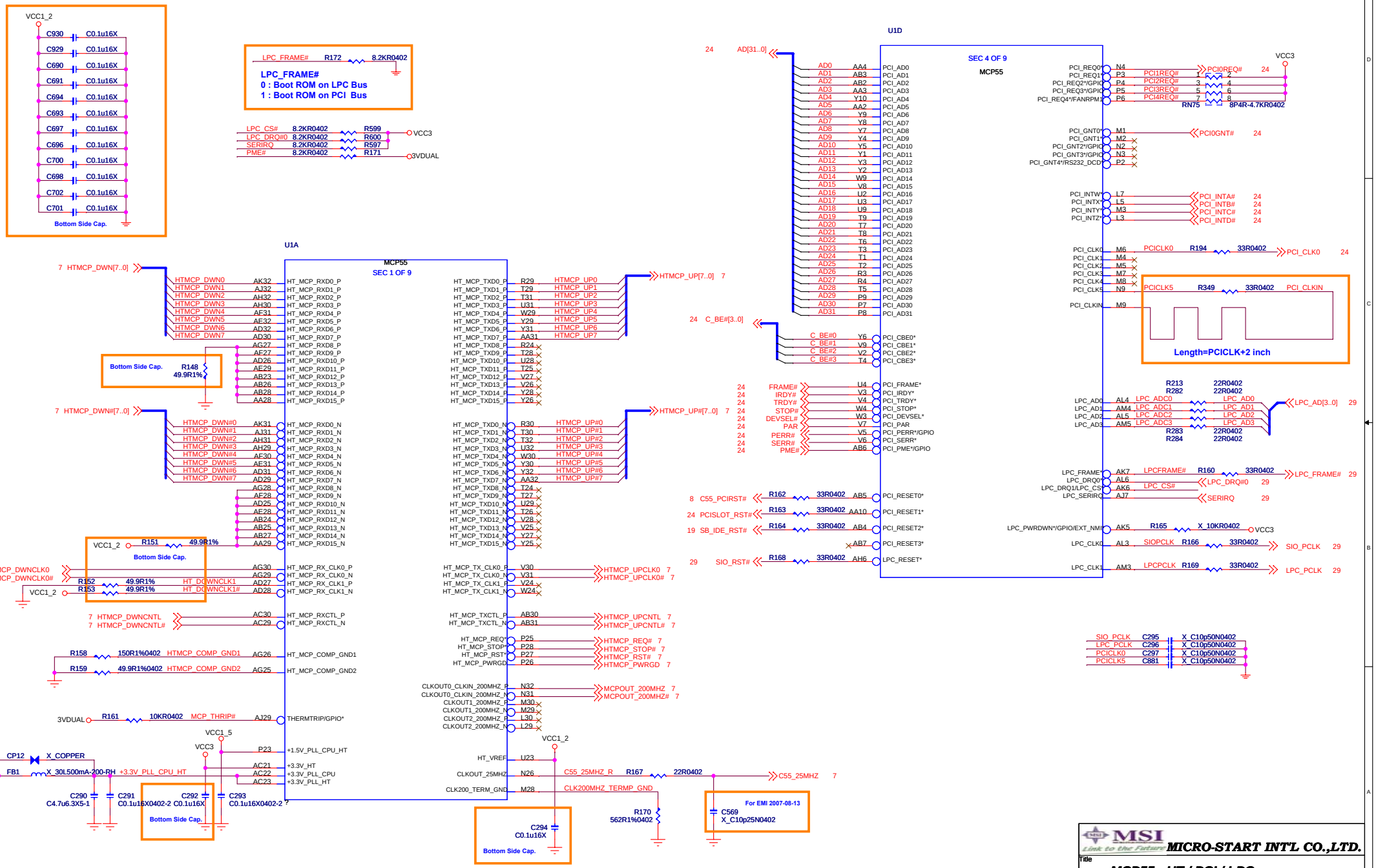
MCP55 - HT / PCI / LPC



MSI MICRO-START INT'L CO.,LTD.		
Title: MCP55 - HT / PCI / LPC		
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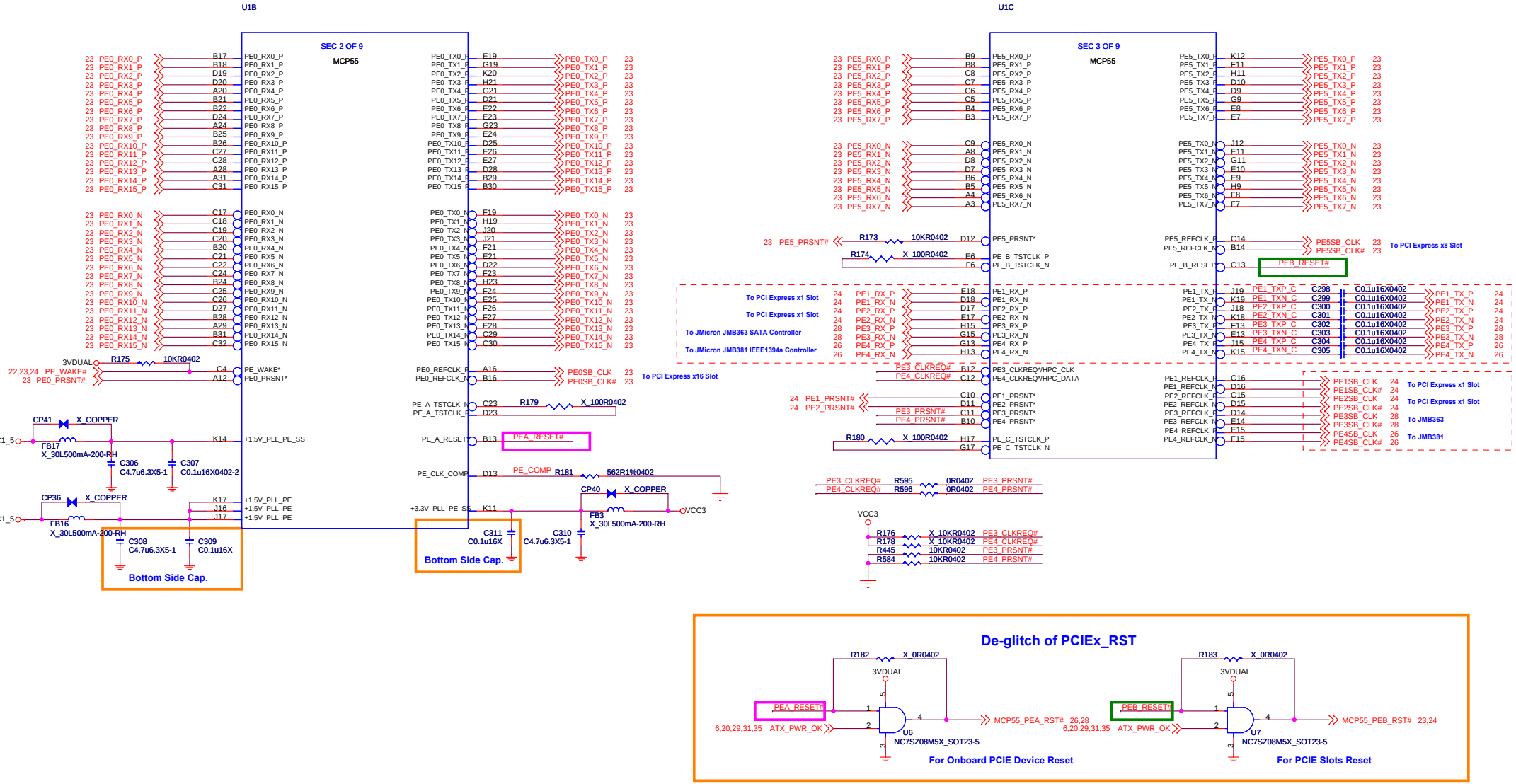
MCP55 - PCI-E



MICRO-START INT'L CO.,LTD.

Title	MCP55 - PCI-E	
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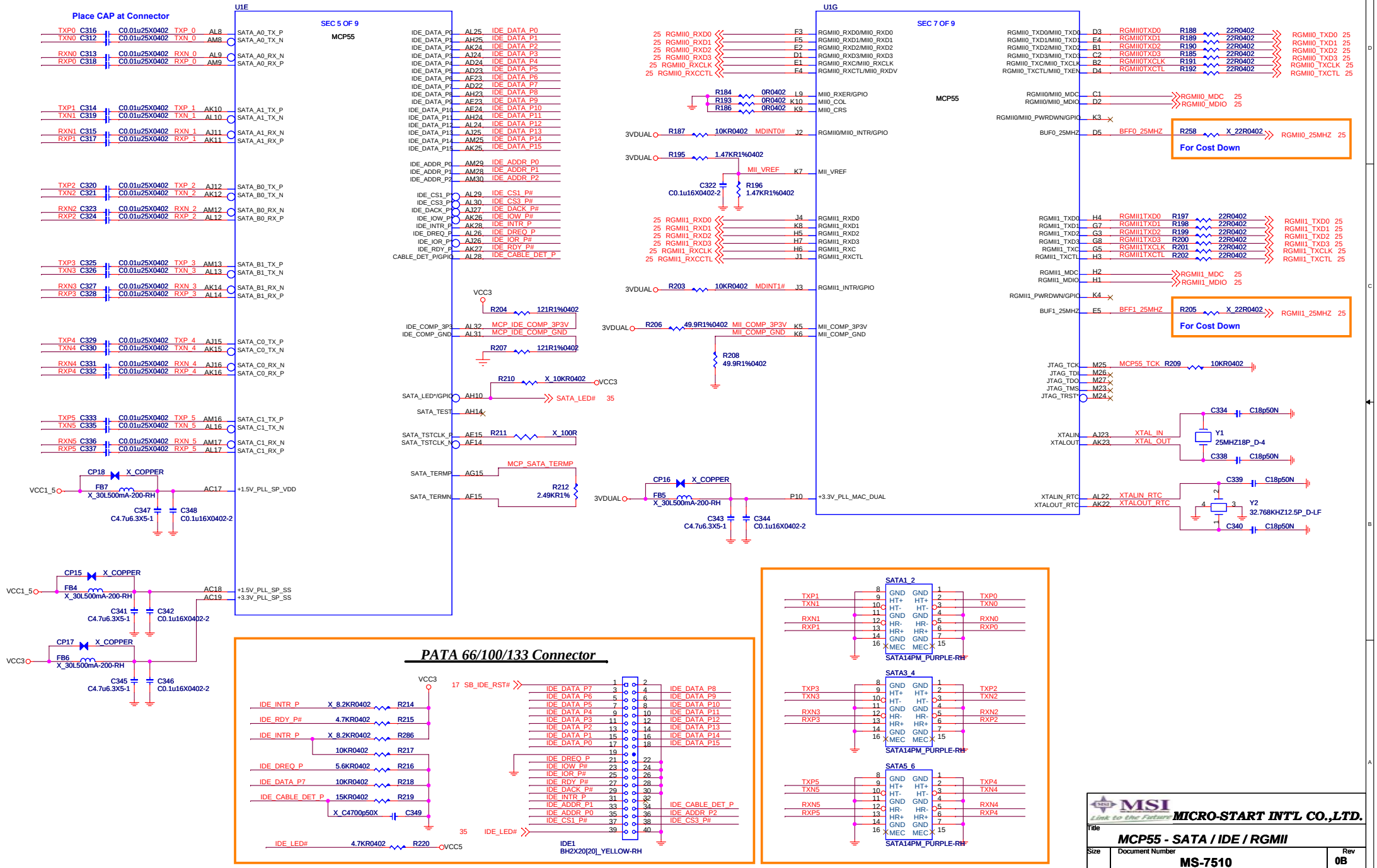
MCP55 - SATA / IDE / RGMII



MICRO-START INT'L CO.,LTD.			
Title: MCP55 - SATA / IDE / RGMII			
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MCP55 - Audio / USB / GPIO

U1F

SEC 6 OF 9

MCP55

27 HD_BCLK — R559 22R0402 — TP32 — AG9 PROG_REFCLK — AJ8 HDA_BCLK

For EMI 2007-08-13 C596 X_C10p25N0402

27 HD_SDOUT — R285 0R0402 — AH7 HDA_SDATA_OUT0/GPIO_45

27 HD_SDIN0 — AF7 HDA_SDATA_IN0/GPIO_22/MGPIO_0

TP33 — AF8 HDA_SDATA_IN1/GPIO_23/MGPIO_1

TP34 — AG8 HDA_SDATA_IN2/GPIO_24/MGPIO_2

27 HD_RESET# — AG7 HDA_RESET*/MGPIO_3

27 HD_SYNC — AH8 HDA_SYNC/GPIO_44

VCC3 — R224 10KR0402 — TP35 — AD19 GPIO_1/SLV_RDY4PWRDWN

TP36 — AE19 GPIO_2/CPU_SLP*/NMI

AH18 GPIO_3/CPU_CLKRUN/SMI*

AE19 GPIO_4/SUS_STAT*/SCI

25 RGMII_RST# — AG17 GPIO_5/SYS_SHUTDOWN*/INIT*

R228 4.7KR0402 nvidia suggest — AD18 GPIO_6/NFERR*/SYS_PERR*

AH17 GPIO_7/FERR*/SYS_SERR*

AF17 GPIO_8/MSMB_CLK

AJ17 GPIO_9/MSMB_DATA

34 GPIO10 — AF24 GPIO_10/THERM_SID1

M32 GPIO_11/CPU_VID0/RS232_SIN*

M31 GPIO_12/CPU_VID1/RS232_SOUT*

P31 GPIO_13/CPU_VID2/RS232_DTR*

N29 GPIO_14/CPU_VID3/RS232_DSR*

N28 GPIO_15/CPU_VID4/RS232_RTS*

P30 GPIO_16/CPU_VID5/RS232_CTS*

SB_MISO — AH20 GPIO_17/SPI_DI

SB_MOSI — AH19 GPIO_18/SPI_DO

SB_SPI_CS0# — AF18 GPIO_19/SPI_CS

SB_SPI_CLK — AM20 GPIO_20/SPI_CLK

3VDUAL — R648 10KR0402 GPIO10

RTC_RST# — AJ22 RTC_RST*

AG11 N/C

AF11 N/C

AH11 N/C

AD11 N/C

AE11 N/C

USB0_P — AL1 — USBP0 34

USB0_N — AL2 — USBN0 34

USB1_P — AK1 — USBP1 34

USB1_N — AK2 — USBN1 34

USB2_P — AJ1 — USBP2 34

USB2_N — AJ2 — USBN2 34

USB3_P — AJ5 — USBP3 34

USB3_N — AJ4 — USBN3 34

USB4_P — AH1 — USBP4 34

USB4_N — AH2 — USBN4 34

USB5_P — AH4 — USBP5 34

USB5_N — AH3 — USBN5 34

USB6_P — AG4 — USBP6 34

USB6_N — AG3 — USBN6 34

USB7_P — AG5 — USBP7 34

USB7_N — AG6 — USBN7 34

USB8_P — AF3 — USBP8 34

USB8_N — AF2 — USBN8 34

USB9_P — AF4 — USBP9 34

USB9_N — AF5 — USBN9 34

RN40: USBN4 USBP4 USBN5 USBP5 — 8P4R-15KR0402

RN39: USBP0 USBN0 USBP1 USBN1 — 8P4R-15KR0402

RN41: USBP3 USBN3 USBP2 USBN2 — 8P4R-15KR0402

RN42: USBP7 USBN7 USBP6 USBN6 — 8P4R-15KR0402

RN43: USBP9 USBN9 USBP8 USBN8 — 8P4R-15KR0402

USB_OC0*/GPIO — AE4 — USB_OCP#0 34

USB_OC1*/GPIO/MGPIO — AF6 — USB_OCP#2 34

USB_OC2*/GPIO/MGPIO — AE3 — USB_OCP#4 34

USB_OC3*/GPIO/MGPIO — AE1 — USB_OCP#6 34

USB_OC4*/GPIO/MGPIO — AE2 — USB_OCP#8 34

USB_RBIAS_GND — AK3 — USB_RBIAS_GND — R232 825R1%

A20GATE/GPIO — AB9 — A20GATE 29

INTRUDER* — AL21 — INTRUDER#

EXT_SMI*/GPIO — AC4 — LPC_SMI# — R236 4.7KR0402 — 3VDUAL

RI*/GPIO — AF9

SPKR — AD9 — SPKR 35

PWRBTN* — AE10 — PWRBTN# 29

SIO_PME*/GPIO — AC3 — SIO_PME# 29

KBRDRSTIN*/GPIO — AB8 — KBRST# 29

SMB_CLK0 — AL20 — SMB_MEM_CLK 11,12

SMB_DATA0 — AK20 — SMB_MEM_DATA 11,12

SMB_CLK1 — AK19 — SMBCLK 14,22,23,24,28,31,32,33

SMB_DATA1 — AJ19 — SMBDATA 14,22,23,24,28,31,32,33

+3.3V_VBAT — AD21 — VBAT

BUF_SIO_CLK — AD3 — SIOCLK_24M — R238 22R0402 — SIO_24M 29

SUS_CLK/GPIO — AD2 — SUS_CLK — C350 X_C10p50N0402

THERM*/GPIO — AD8 — THRM# 29

RSTBTN* — AD10 — R612 22R0402 — FP_RST# 3,29,35

SLP_S5* — AK18 — SLP_S5# 31

SLP_S3* — AJ18 — SLP_S3# 29,31

PWRGD_SB — AK21 — RSMRST# 25,29

PWRGD — AF21 — MCP55_PWRGOOD — R241 0R0402 — ATX_PWR_OK 6,18,29,31,35

FANRPM/GPIO — AD6 — TP47

FANCTL0/GPIO — AD5 — TP46

FANCTL1/GPIO — AD7 — TP39

THERM_SIC/GPIO — AK30 — TP40

THERM_SID0/GPIO — AH27 — TP41

R399 X_10KR0402

TEST_MODE_EN — P24 — SB_TEST — R245 1KR1%

3VDUAL — R646 10KR0402 — SB_SPI_HOLD0#

R643 X_10KR0402 — SB_WP_SIO0#

R645 10KR0402

VCC3

X_C10u10Y0805 C0.1u16X0402-2 — C794 C843

R451 4.7KR0402

U20: SB_SPI_CS0# (1) CE# VDD (8); SB_MISO (2) SO HOLD# (7) SB_SPI_HOLD0#; SB_WP_SIO0# (3) WP# SCK (6) SB_SPI_CLK; VSS (4) SI (5) SB_MOSI

X_MX25L8005M2C-15G-RH

3VDUAL — R239 X_1KR1%0402 — R242 1KR1%0402 — SB_MOSI

3VDUAL — R240 X_1KR1%0402 — R243 1KR1%0402 — SB_SPI_CLK

SPI EEPROM Clock Speed
00: 50 kHz
01: 99 kHz
10: 480 kHz
11: 893 kHz

32 HT_VLD — MEM_VLD — AL18 MEM_VLD

HT_VLD — AE21 HT_VLD

32 HTVDD_EN — HTVDD_EN — AJ21 HTVDD_EN

VCORE_VLD — AH21 CPU_VLD

31,33 VCORE_EN — VCORE_EN — AG21 CPUVDD_EN

Bottom Side Cap.

VCC1_5 — C351 C0.1u16X

CP19 X_COPPER

VCC3 — FB8 X_30L500mA-200-RH — MCP_+3.3V_PLL_USB — AB10 +1.5V_PLL_USB — AD1 +3.3V_PLL_USB

60mA

C352 C4.7u6.3X5-1

C353 C0.1u16X0402-2

NV Recommend

VCC3 — R222 10KR0402 — THRM#

3VDUAL — R225 X_10KR0402

SUS_CLK
MCP55 Model Select
0 : Maeter Mode
1 : Slave Mode

3VDUAL — R223 X_10KR0402 — SUS_CLK — R227 10KR0402

SPKR
0 : User Mode Boot Initial Table
1 : Safe Mode Boot Initial Table

VCC3 — R229 X_1KR1%0402 — SPKR — R230 1KR1%0402

3VDUAL — R221 10KR0402 — HD_RESET#

HD_RESET#
1 : RGMII
0 : MII

VCC3 — R226 10KR0402 — HD_SYNC

HD_SYNC
1 : Super I/O use 24MHz
0 : Super I/O use 14.318MHz

SMB_MEM_CLK — R231 2.7KR0402 — VCC3

SMB_MEM_DATA — R233 2.7KR0402

SMBCLK — R234 2.7KR0402 — 3VDUAL

SMBDATA — R235 2.7KR0402

FP_RST# — R611 10KR0402 — 3VDUAL

INTRUDER# — R510 2MR0402 — VBAT

Vcore Power On Sequence Control Circuit

SLP_S5# — R248 0R0402 — MEM_VLD

C357 X_C0.1u16X0402-2

HTVDD_EN — R253 0R0402 — HT_VLD

C358 X_C0.1u16X0402-2

VCORE_EN — R255 X_0R0402 — VCORE_VLD

C360 X_C0.1u16X0402-2

VCC3

VCC5_SB — R251 X_4.7KR0402

R252 X_4.7KR0402 — 0R0402 — R254 — VRM_GD 33

VCCP — VCORE_VLD

R250 X_1KR1%0402

Q3 X_N-MMBT3904_NL_SOT23

Q2 X_N-MMBT3904_NL_SOT23

C359 X_C0.1u16X0402-2

3VDUAL

VBAT — D1 S-BAT54C_SOT23 — R247 49.9KR1%0402 — RTC_RST#

C355 X_C0.1u25Y0402-RH

C356 C1u6.3Y0402-RH

CLR_CMOS2 — R718 100R1%0402

SW-TACTB1-4P#_BLACK

R249 1KR1%0402

VBAT1 BAT2P_BLACK-RH-1

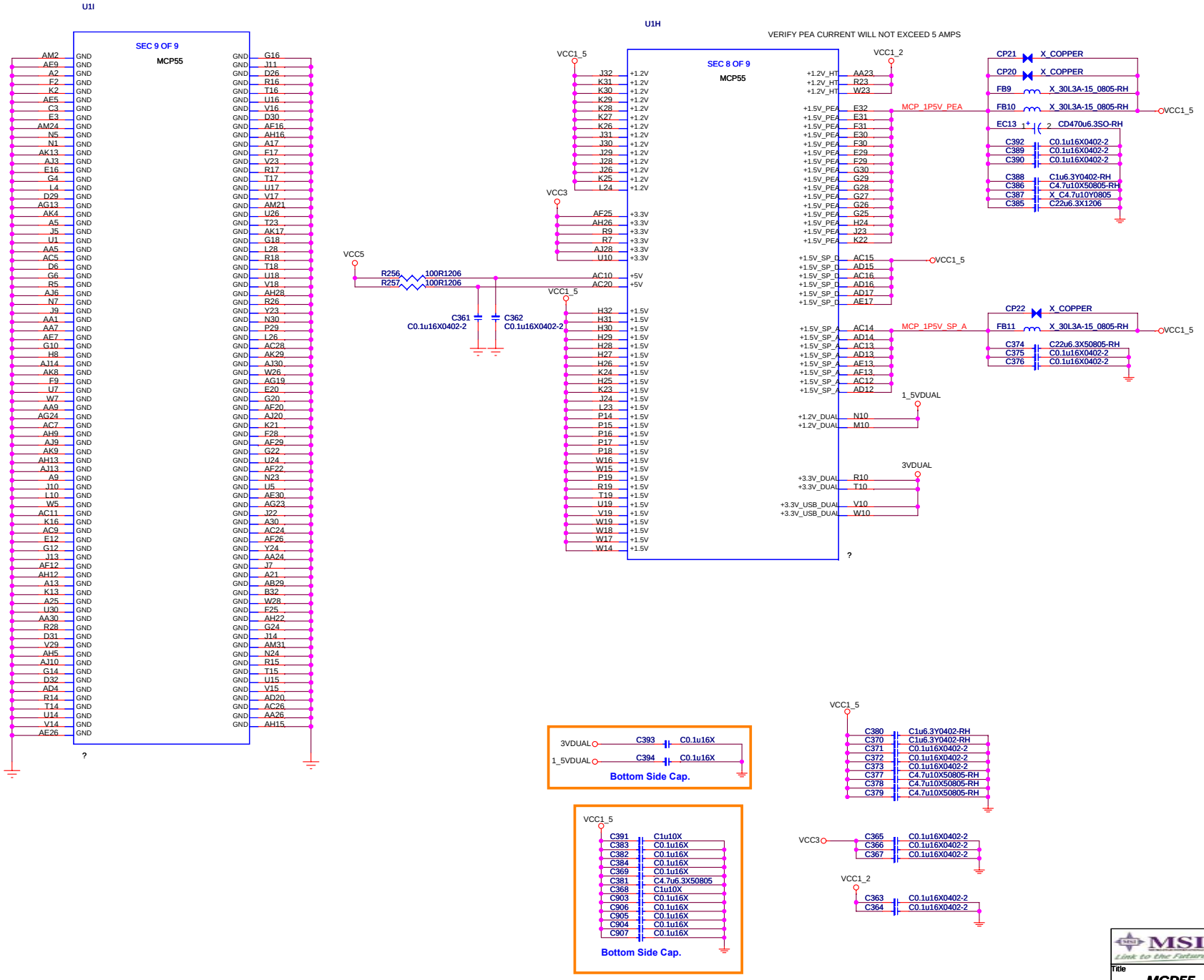
MSI MICRO-START INT'L CO.,LTD.

Title: MCP55 - Audio / USB / GPIO

Size | Document Number: MS-7510 | Rev: 0B

Date: Wednesday, October 31, 2007 | Sheet 20 of 41

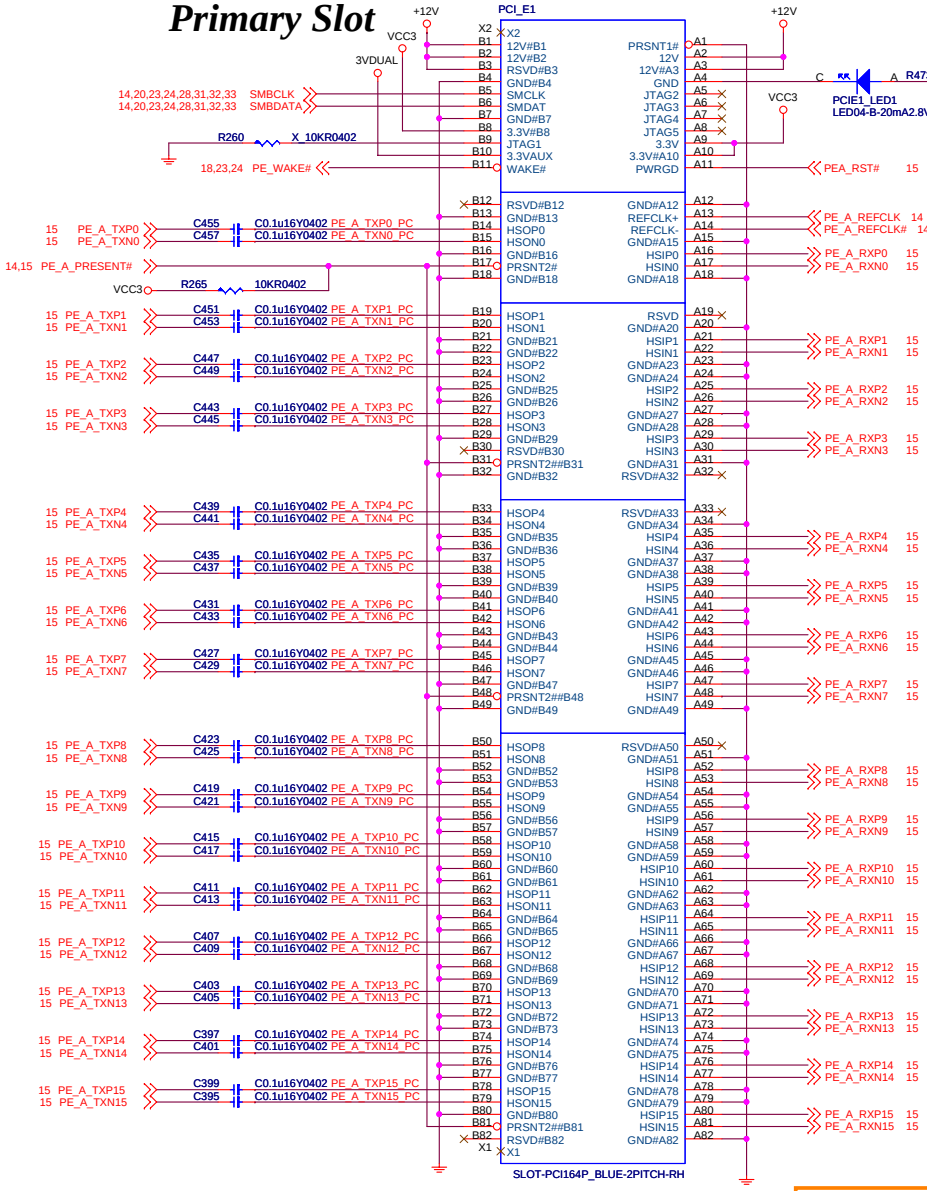
MCP55 - Power & Gnd



MSI Link to the Future	MICRO-START INT'L CO.,LTD.	
Title	MCP55 - Power & Gnd	
Size	Document Number MS-7510	Rev 0B
Date: Tuesday, October 30, 2007	Sheet 21 of 41	

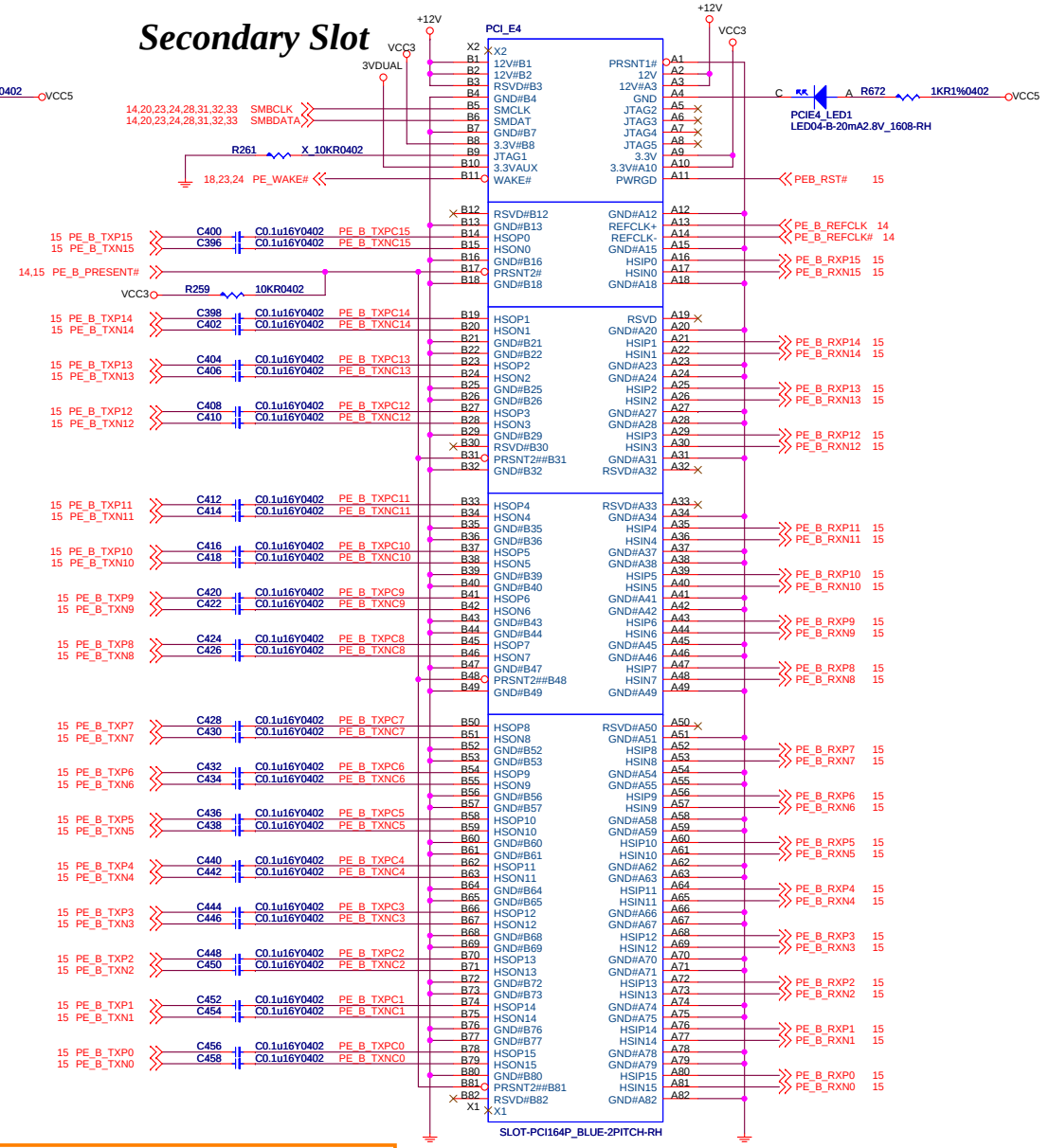
PCI-Express x16 Primary and Secondary Slot

Primary Slot

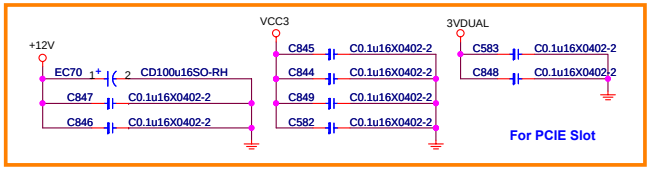


For Layout placement to Reversed

Secondary Slot



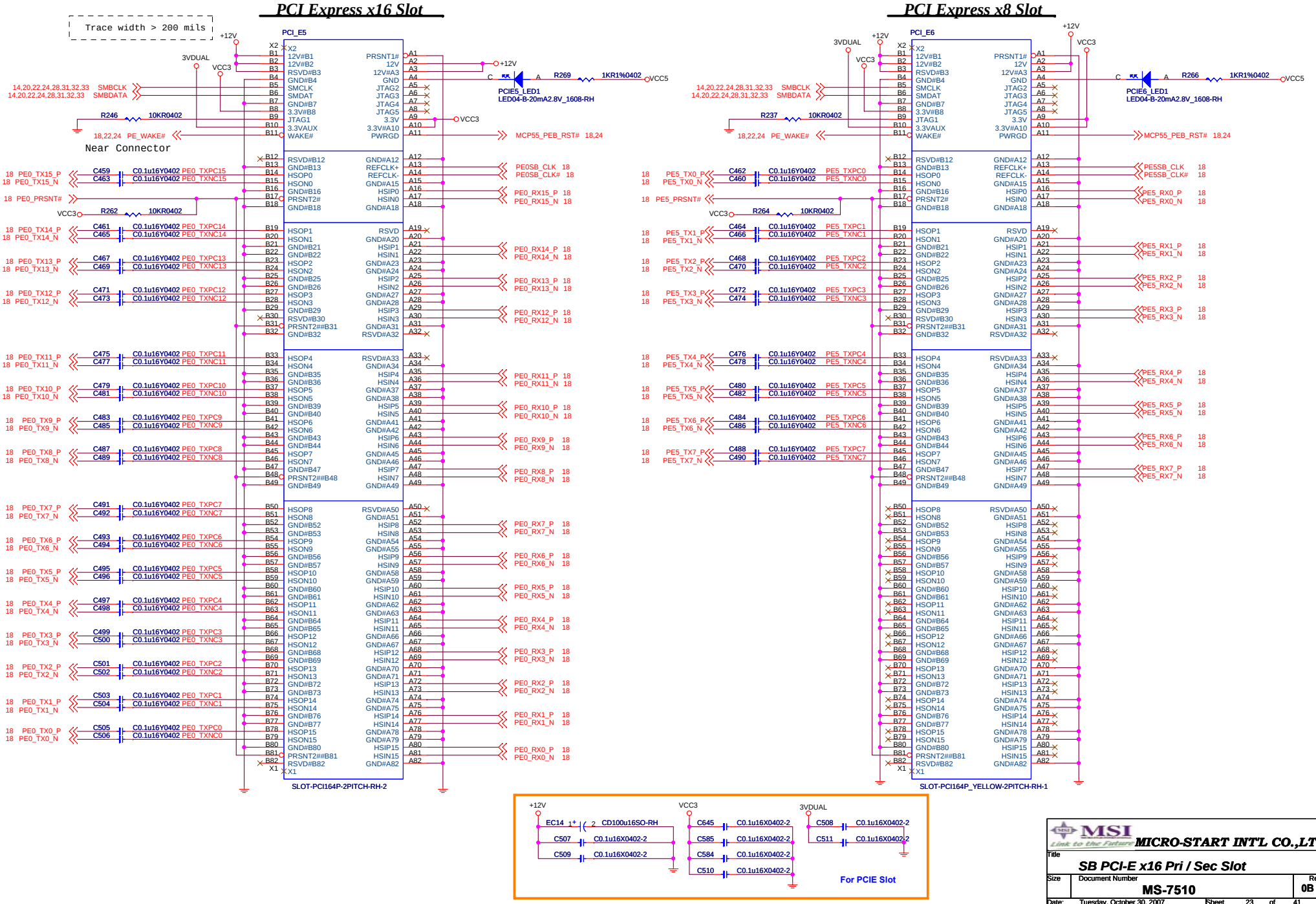
For Layout placement to Reversed



MICRO-START INT'L CO.,LTD.

Title: NB PCI-E x16 Pri / Sec Slot		
Size	Document Number: MS-7510	Rev: 0B
Date: Tuesday, October 30, 2007	Sheet 22 of 41	

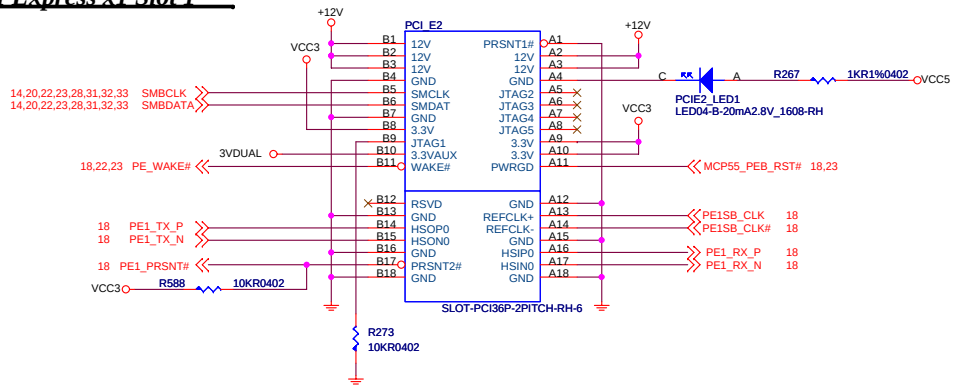
SB PCI Express x16 Slot and PCI Express x8 Slot



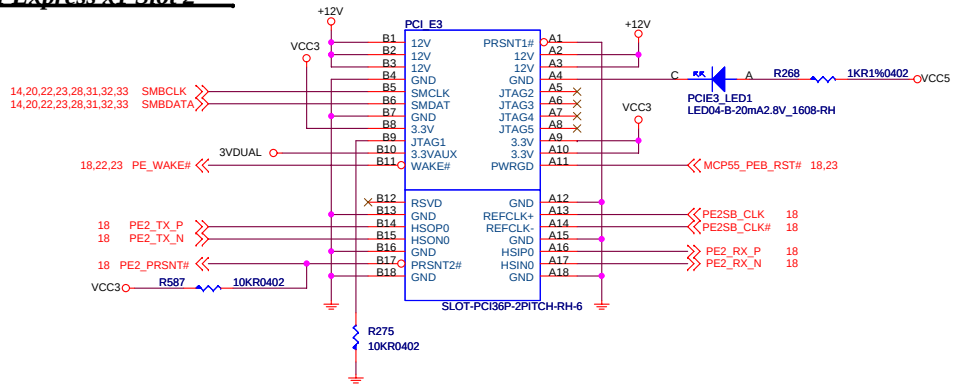
MICRO-START INT'L CO.,LTD.		
Title: SB PCI-E x16 Pri / Sec Slot		
Size	Document Number: MS-7510	Rev: 0B
Date: Tuesday, October 30, 2007	Sheet 23 of 41	

SB PCI-Express x1 Slots and PCI Slot

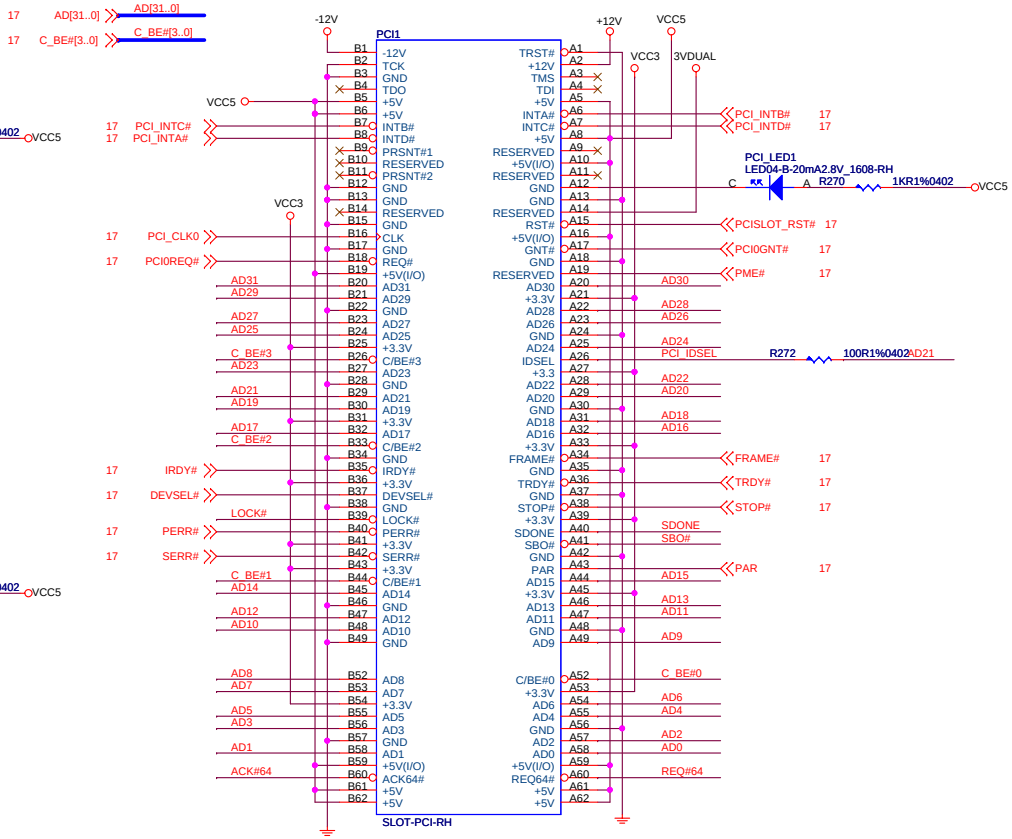
PCI Express x1 Slot 1



PCI Express x1 Slot 2

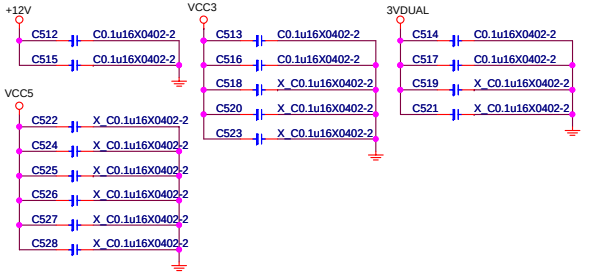


PCI Slot 1 (PCI VER: 2.2 Comply)

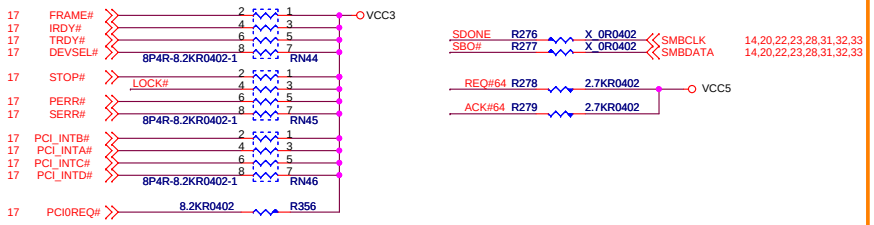


IDSEL = AD21
MASTER = PCI0REQ#
PCI0GNT*

PCI Slot Decoupling Capacitors



PCI Pull Up / Down Resistors



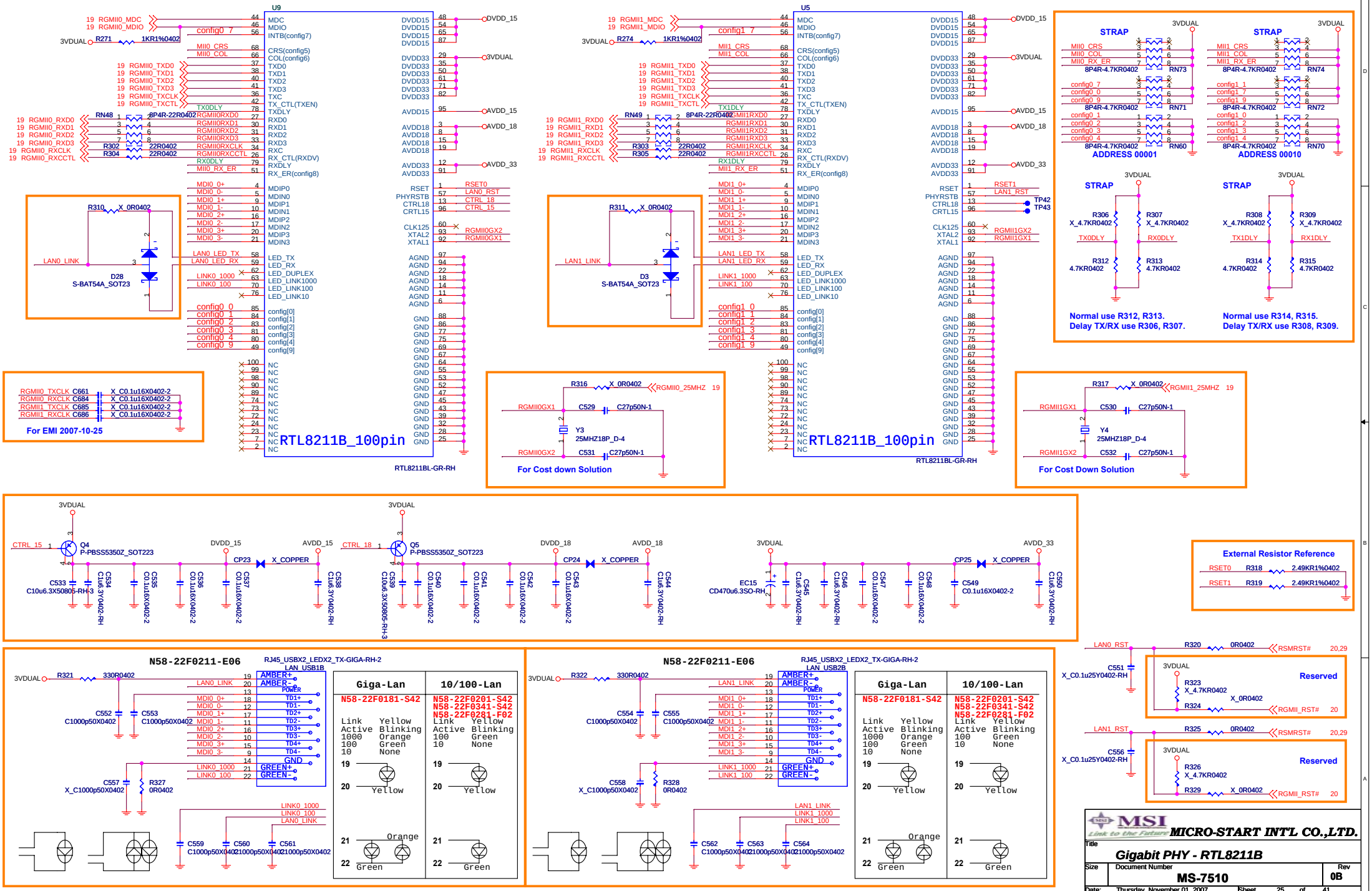
MSI MICRO-START INT'L CO.,LTD.

Title: SB PCI-E x1 / PCI Slot

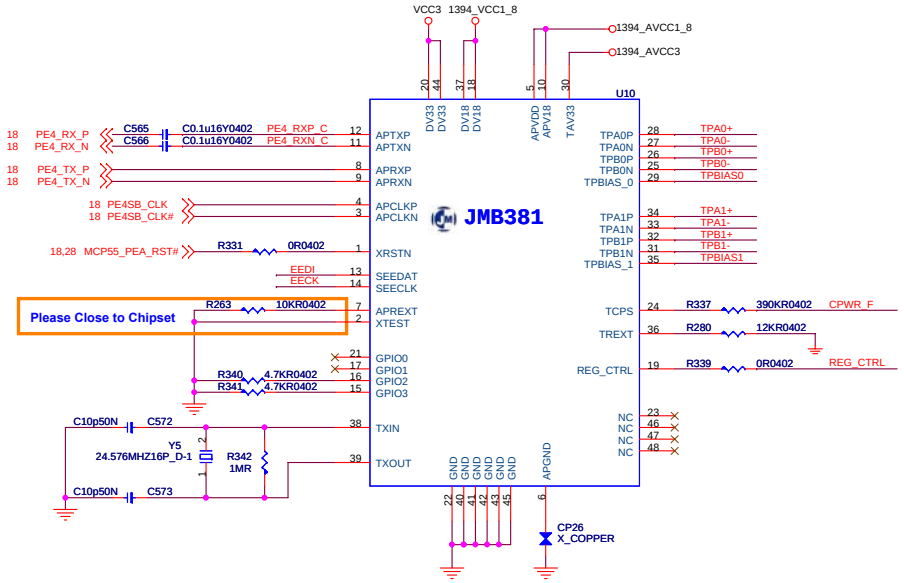
Size | Document Number: MS-7510 | Rev: 0B

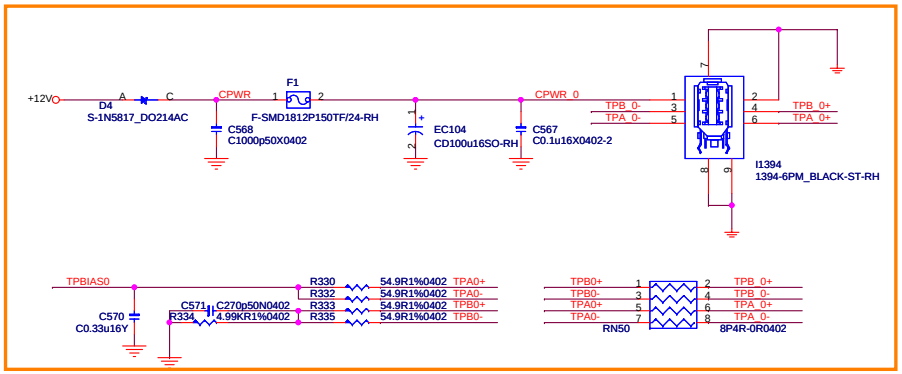
Date: Tuesday, October 30, 2007 Sheet 24 of 41

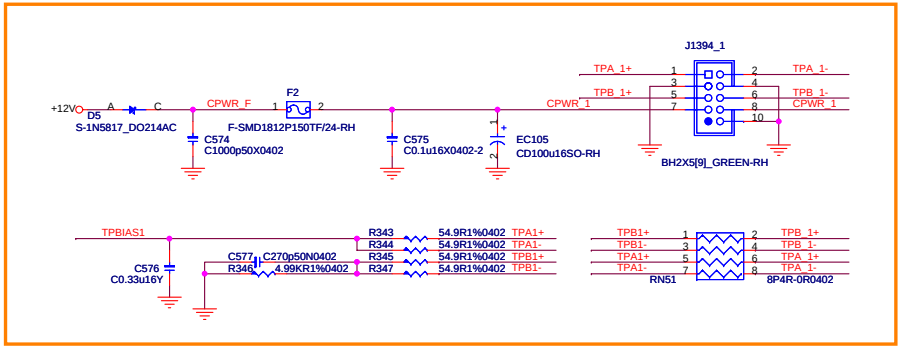
RTL8211B RGMII Gigabit PHY (Lan 1 and Lan 2)

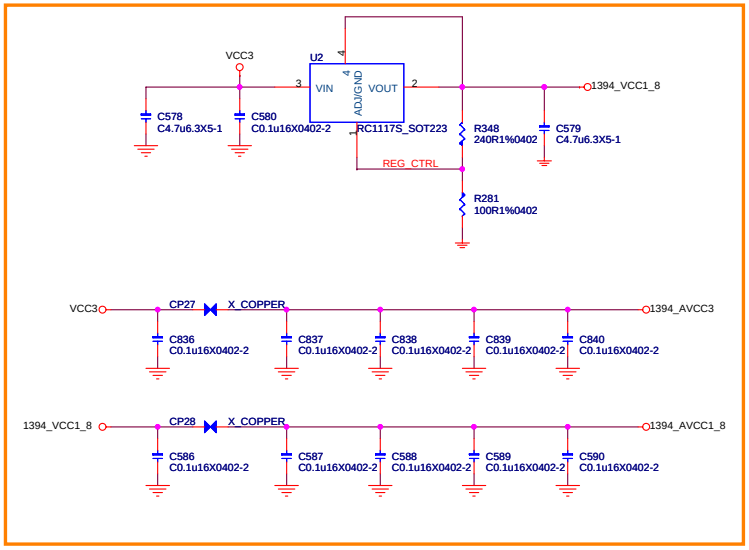


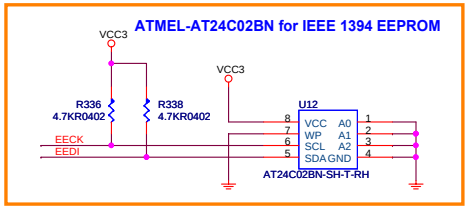
PCIE To 1394a OHCI Host Controller - JMB381







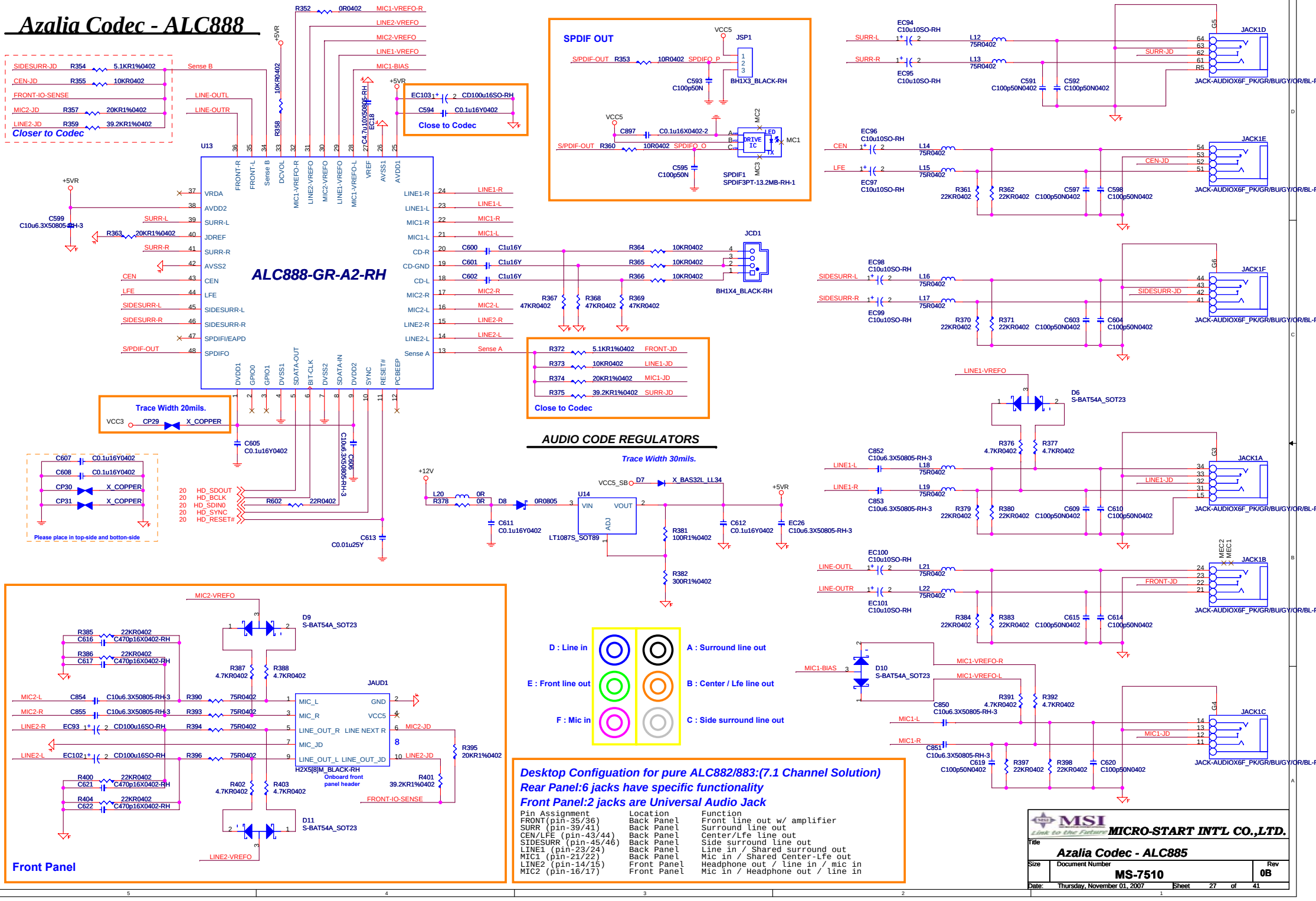




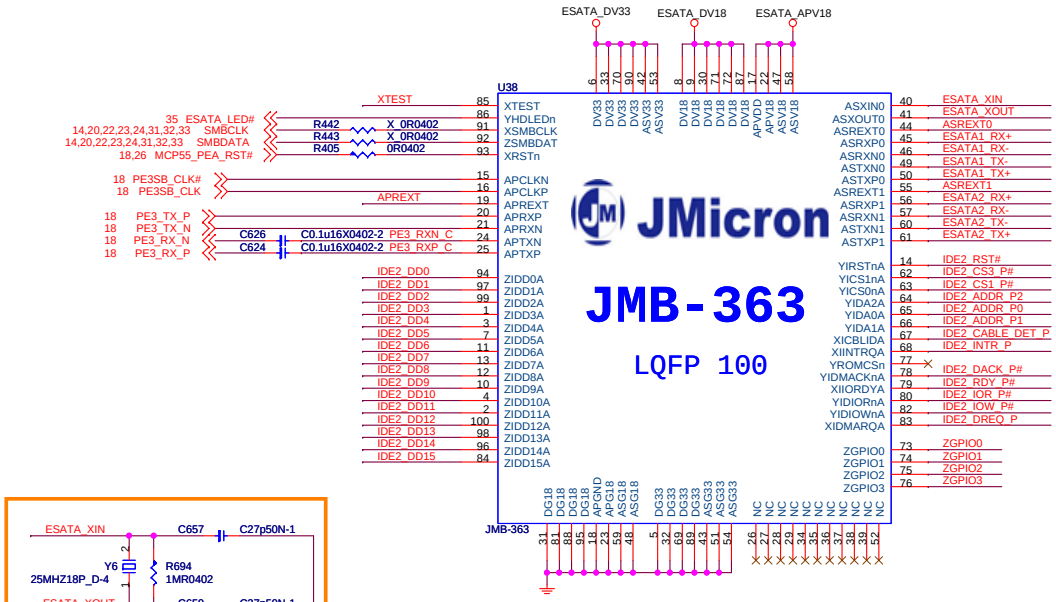
MSI Link to the Future MICRO-START INT'L CO.,LTD.

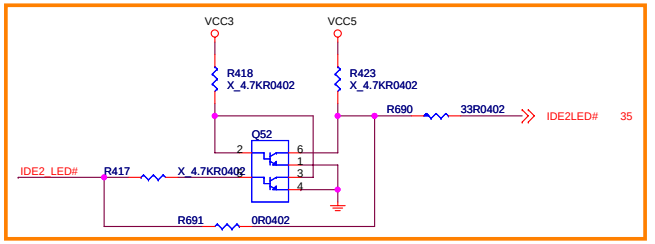
Title	1394 Controller - JMB381	
Size	Document Number MS-7510	Rev 0B
Date: Thursday, November 01, 2007	Sheet 26 of 41	

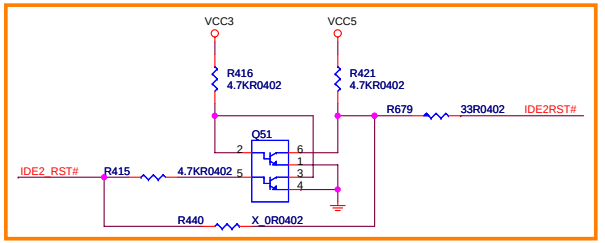
Azalia Codec - ALC888



JMicron JMB363 eSATA Controller



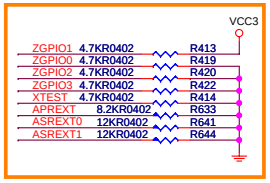


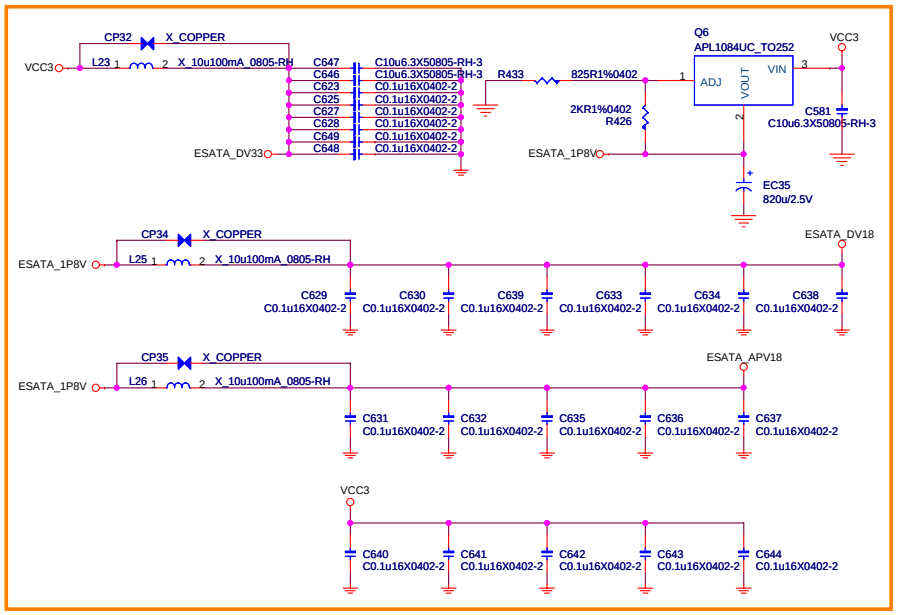


SATA II Port 0 External Reference Resistor.
An external 12KΩ±1%resistor should be connected and bypass to the ground ASG18 (pin#48).

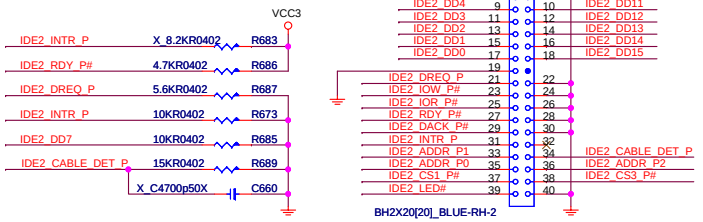
SATA II Port 0 External Reference Resistor.
An external 12KΩ±1%resistor should be connected and bypass to the ground ASG18 (pin#59).

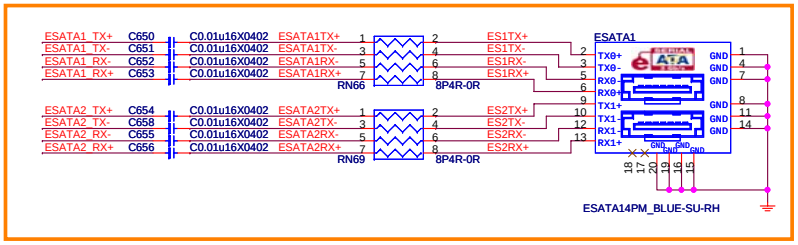
PCI Express External Reference Resistor.
An external 12KΩ±1% resistor should be connected and bypass to the ground APG18 (pin#18).





PATA 66/100/133 Connector



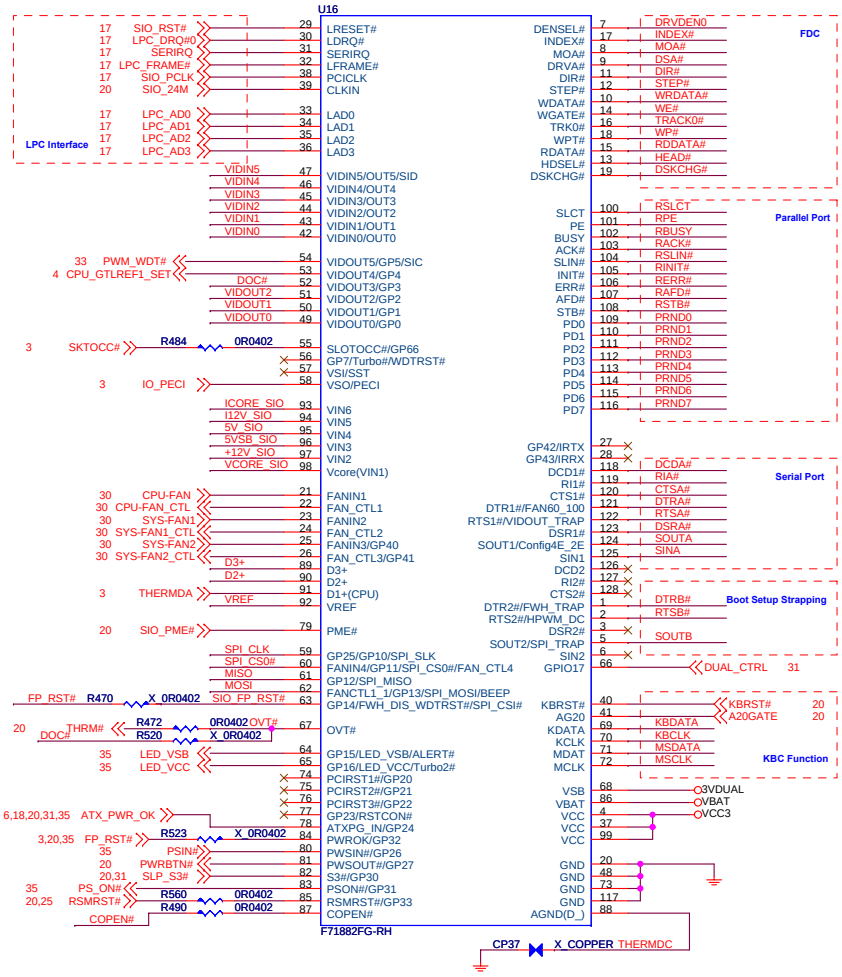


JMB363 GPIO0
It uses to control function# available on JMB363.
0: single function ; 1: multi-function
JMB363 GPIO1
It uses to control clock source of SATA II port 0.
0: from internal clock source from PCI Express clock source
1: from ASXIN0 & ASXOUT0
JMB363 GPIO2
It uses to control interface to access internal debug registers.
0: SMBus I/F ; 1: Reserved for debugging.
JMB363 GPIO3
Reserved for debugging.
JMB363 Test Mode Enable.
High-active signal to enable testing and debug modes of JMB363.

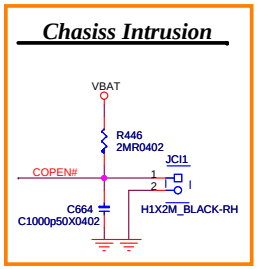
MICRO-START INT'L CO.,LTD.

Title	JMicron JMB363 eSATA Controller	
Size	Document Number: MS-7510	Rev: 0B
Date: Tuesday, October 30, 2007	Sheet 28 of 41	

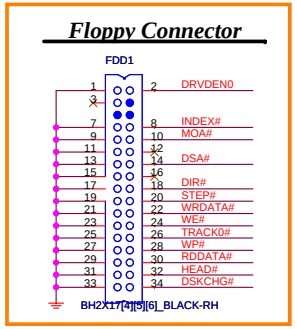
Super I/O FinTek F71882FG



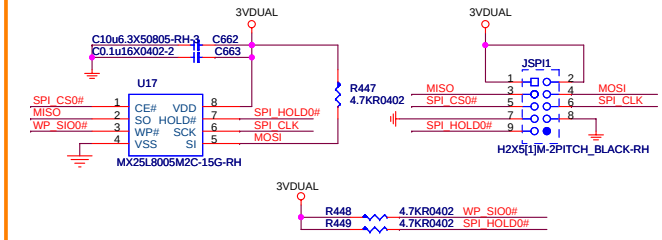
Chasiss Intrusion



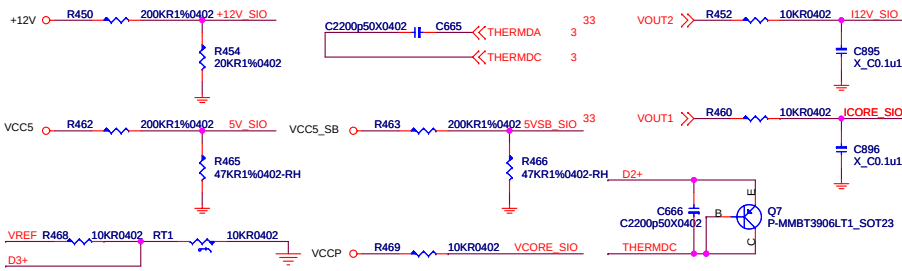
Floppy Connector



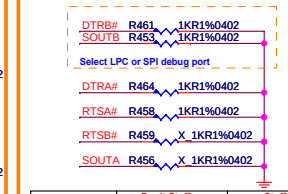
SPI Flash ROM and Debug Port



Voltage and Temperture H/W Monitor Block

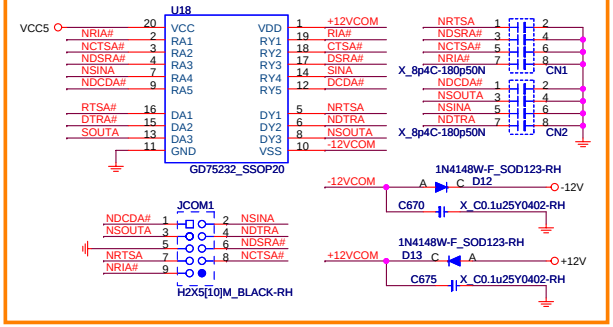


Boot Setup Strapping

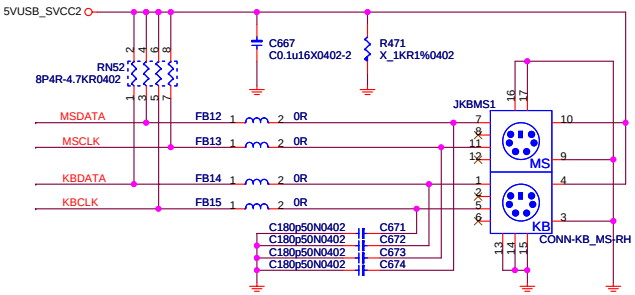


	Don't Stuff	Stuff
RTSB#	PWM FAN	LINEAR FAN
	PIN49_54=VID_OUT	PIN49_54=GPIO
RTSA#	PIN42_47=VIDIN	PIN42_47=VIDIN/OUT
SOUTA	4E / 4F	2E / 2F
SOUTB	SPI_DISABLE	SPI_ENABLE
DTRA#	FAN Start Duty 60%	FAN Start Duty 100%

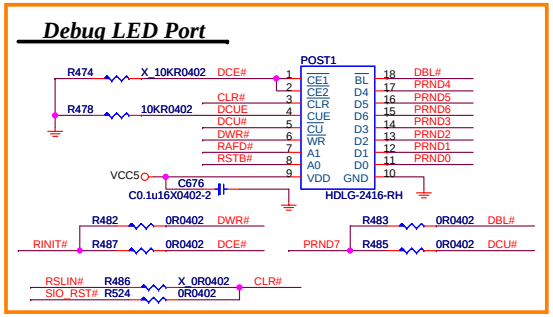
Serial Port (COM1)



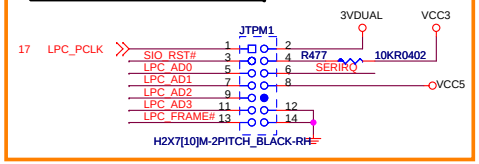
PS2 Keyboard and Mouse Connector

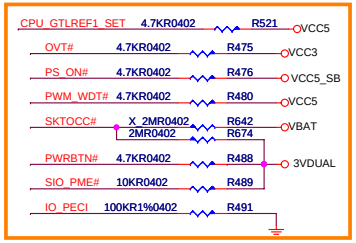


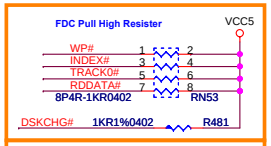
Debug LED Port

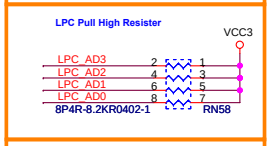


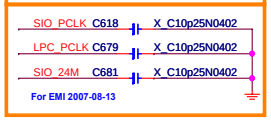
TPM Module Port

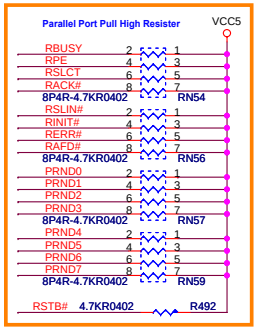


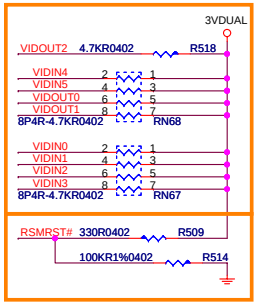


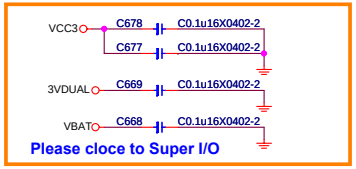












MSI MICRO-START INT'L CO.,LTD.

Title: Super I/O - F71882FG

Size	Document Number	Rev
	MS-7510	0B

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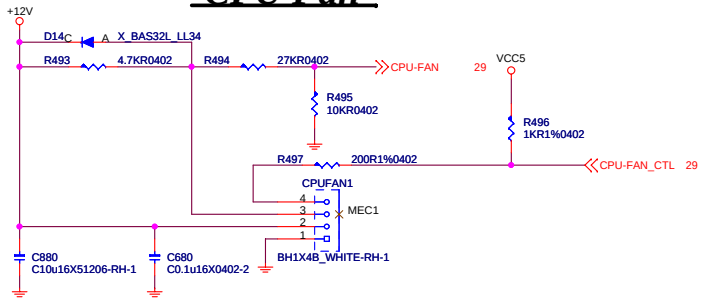
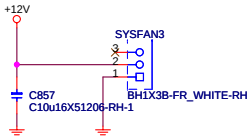
Fan Controller

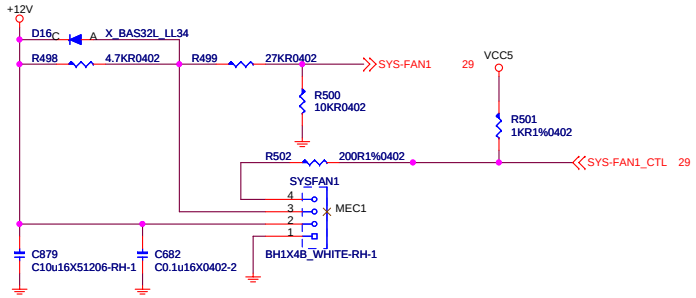
CPU Fan



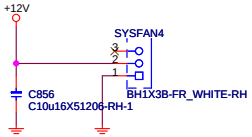
System Fan 3



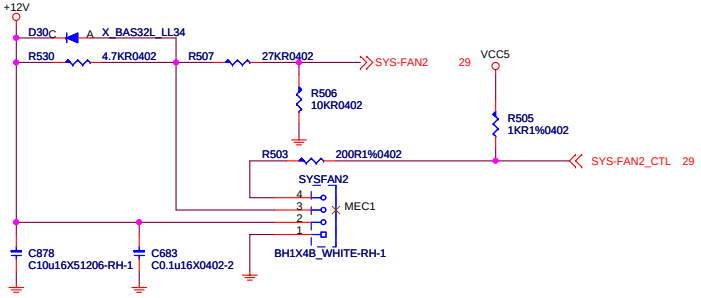
System Fan 1



System Fan 4



System Fan 2



MICRO-START INT'L CO.,LTD.

Title: Fan Controller		
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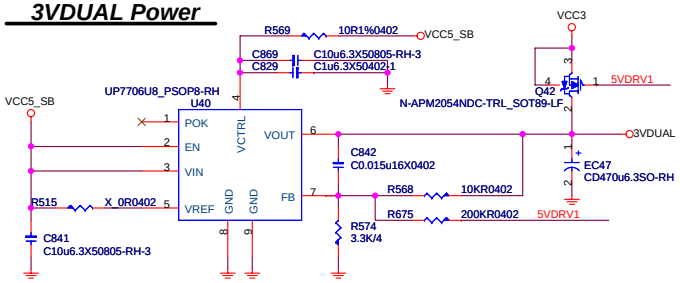
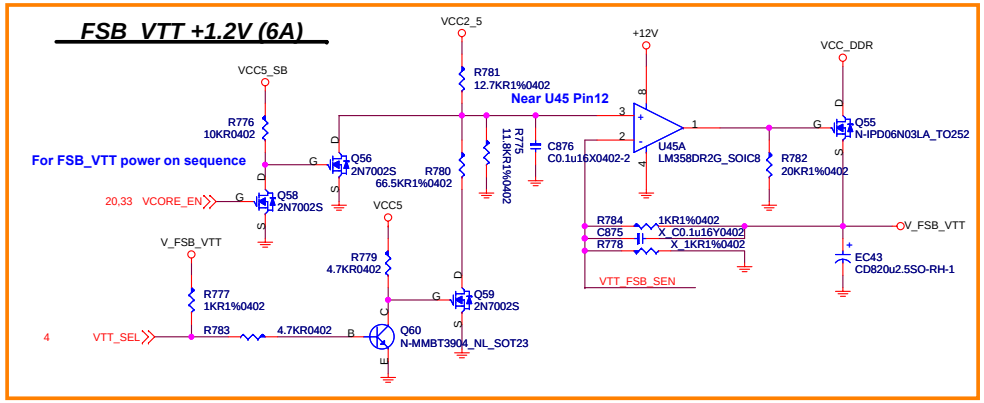
uPI ACPI Solution

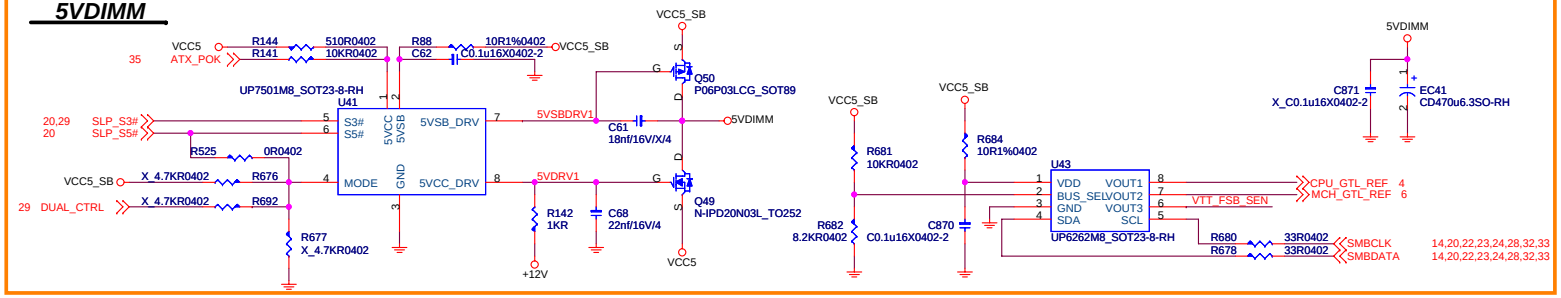
3VDUAL Power



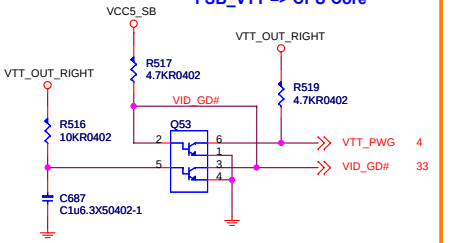
FSB_VTT +1.2V (6A)



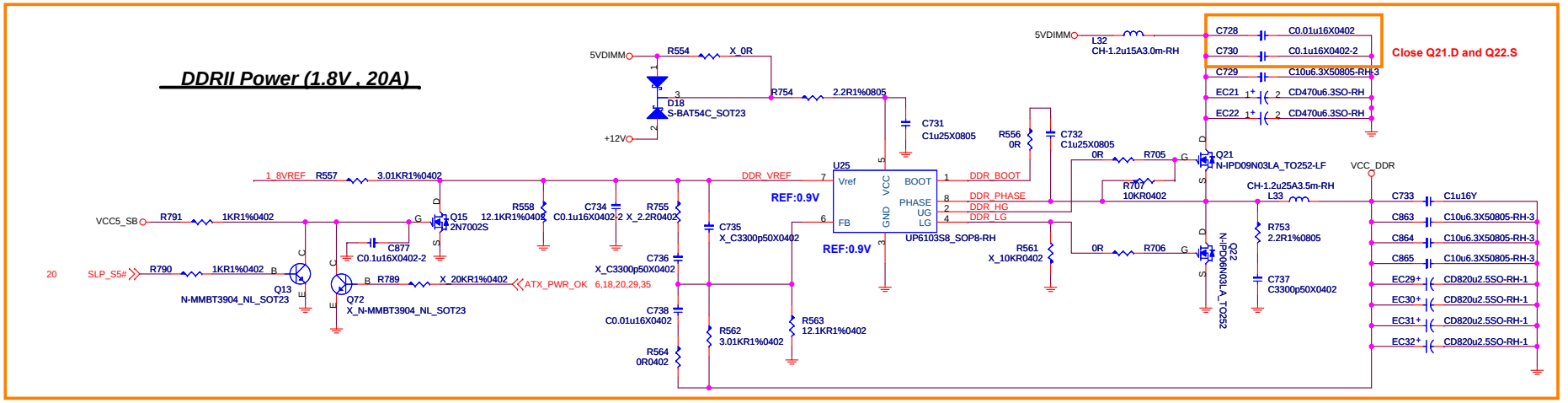
5VDIMM



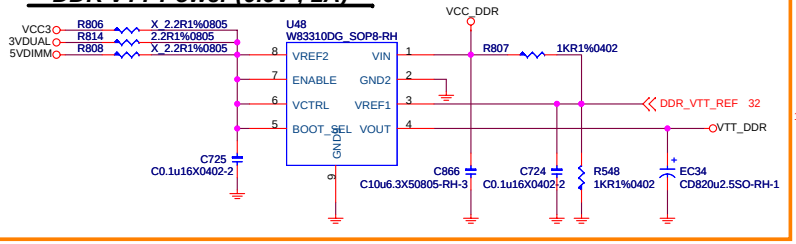
Power on sequence FSB_VTT => CPU Core



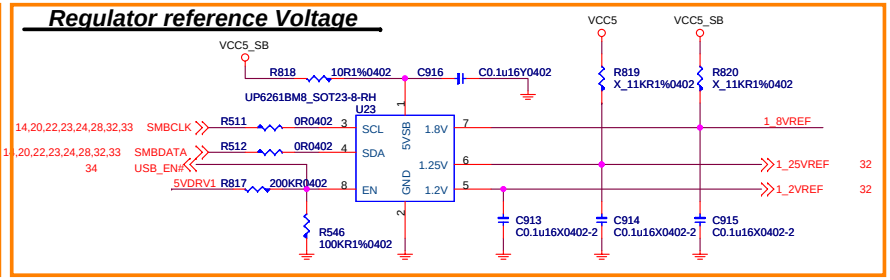
DDRII Power (1.8V , 20A)



DDR VTT Power (0.9V , 1A)



Regulator reference Voltage



MSI MICRO-START INT'L CO.,LTD.

Title: MS12 ACPI Controller

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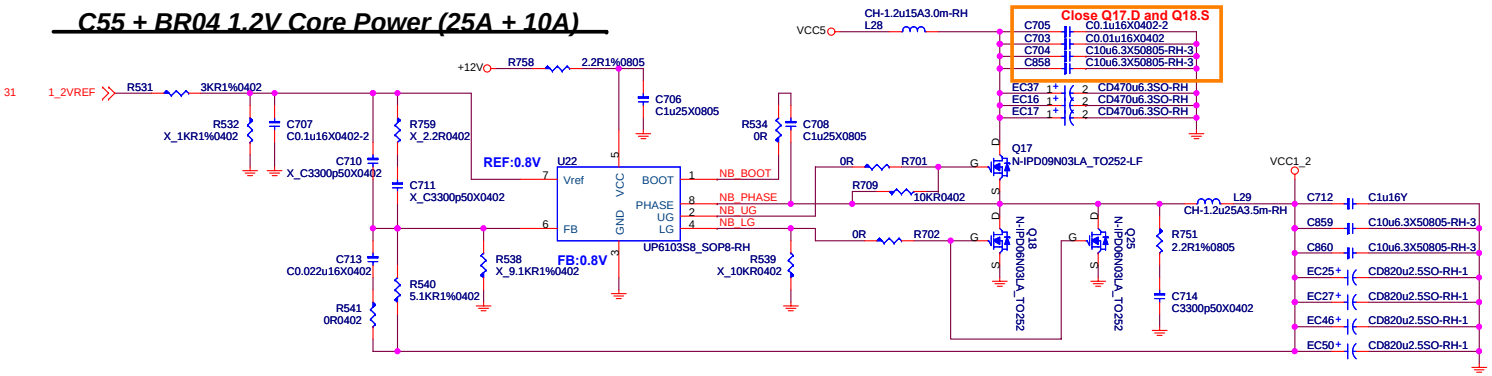
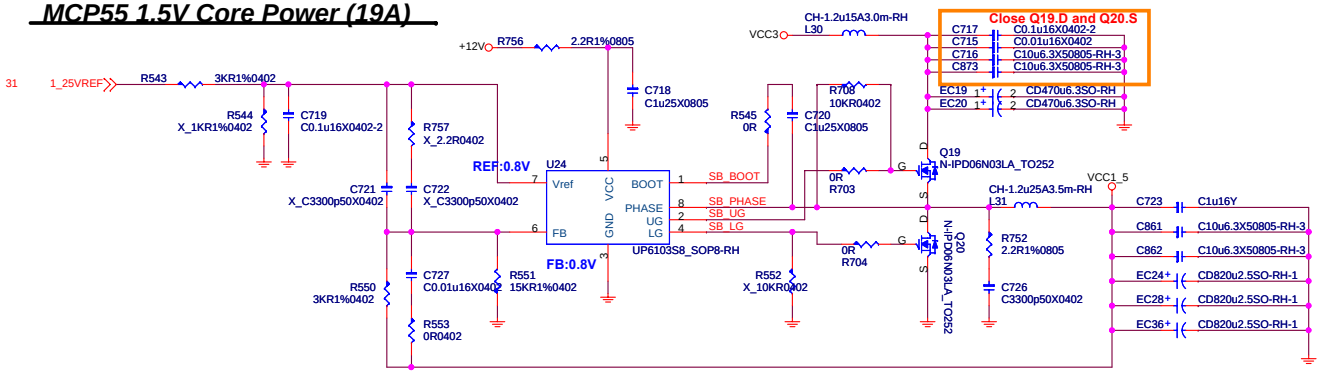
uPI Power Regulator

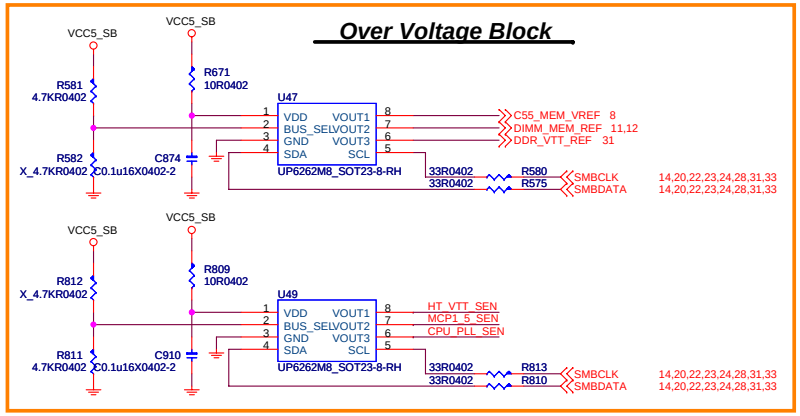
C55 + BR04 1.2V Core Power (25A + 10A)



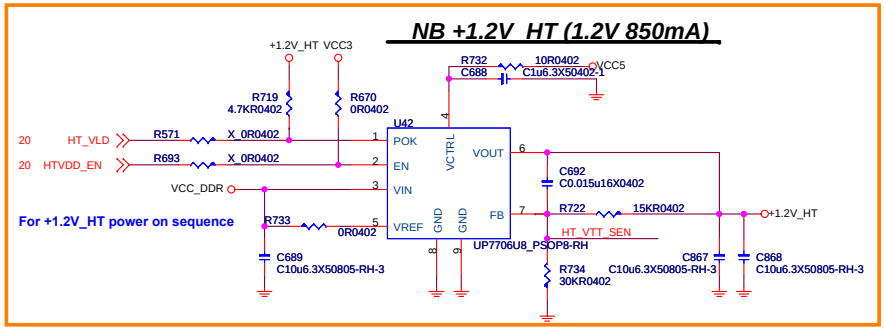
MCP55 1.5V Core Power (19A)



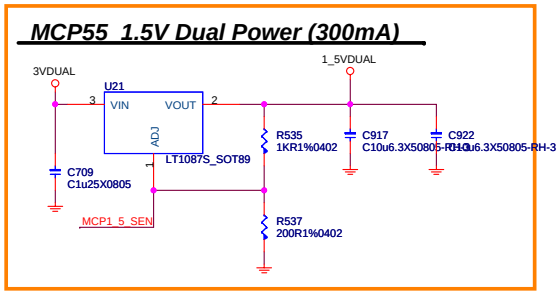
Over Voltage Block



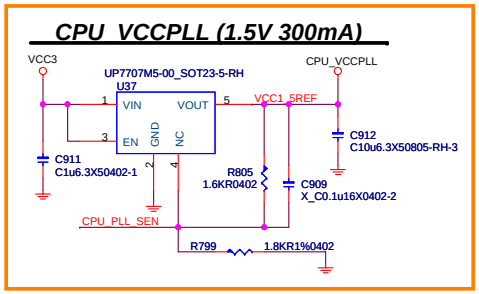
NB +1.2V HT (1.2V 850mA)



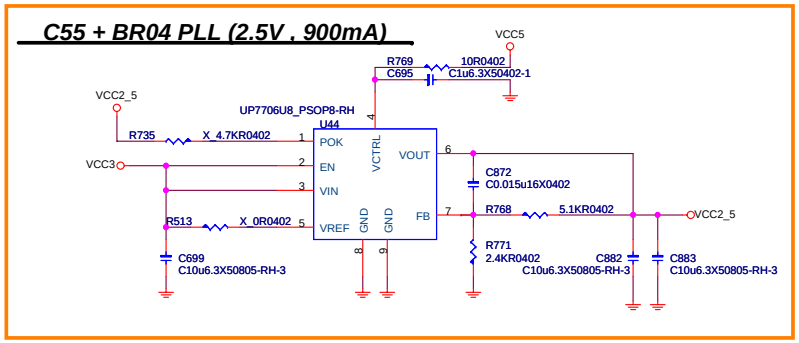
MCP55 1.5V Dual Power (300mA)

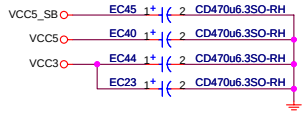


CPU VCCPLL (1.5V 300mA)



C55 + BR04 PLL (2.5V , 900mA)





MICRO-START INT'L CO.,LTD.		
Title: uPI Power Regulator		
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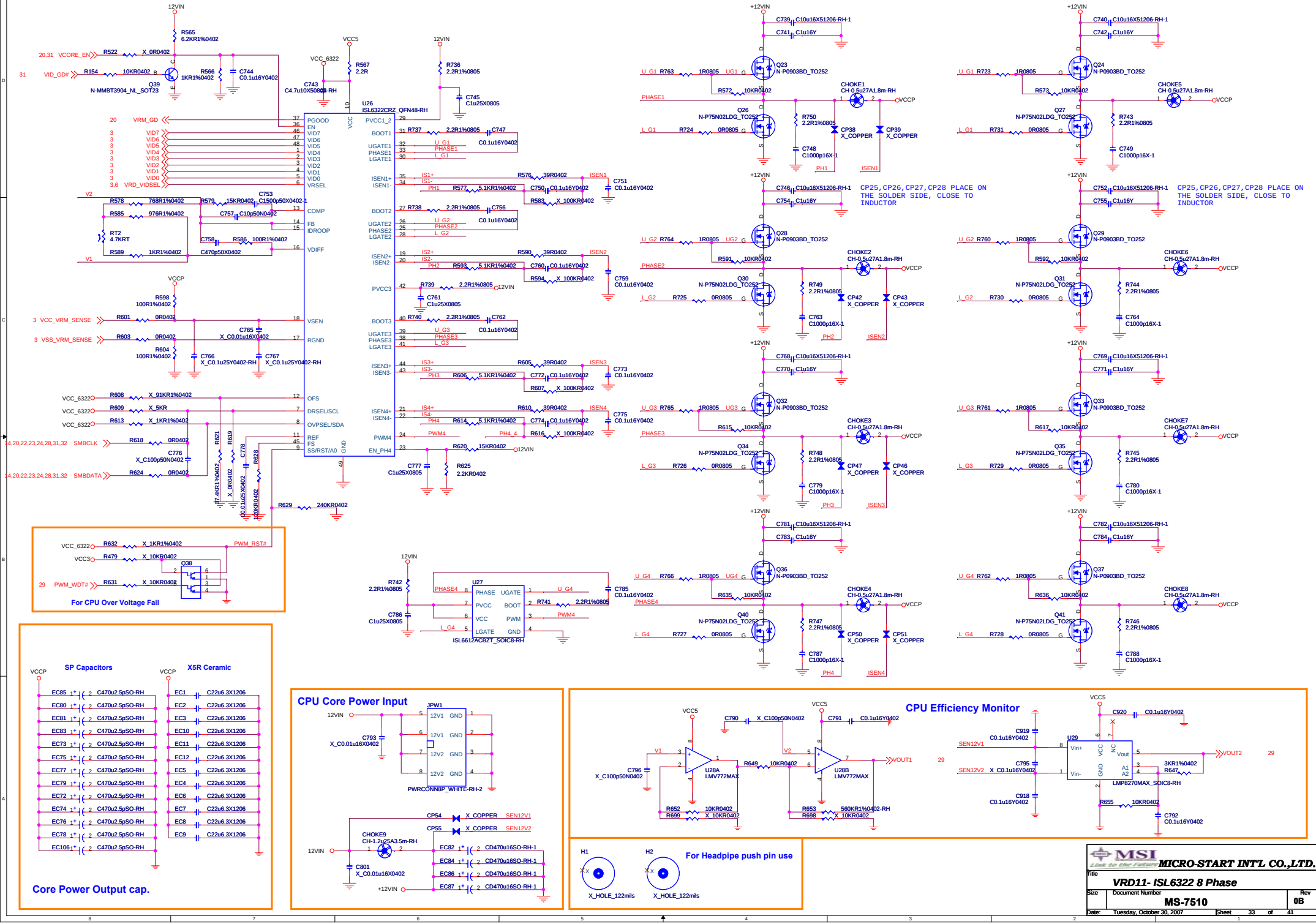
Voltage Regular Module (VRD11)



MSI Link to the Future	MICRO-START INT'L CO.,LTD.		
Title	VRD11- ISL6322 8 Phase		
Size	Document Number	MS-7510	Rev 0B
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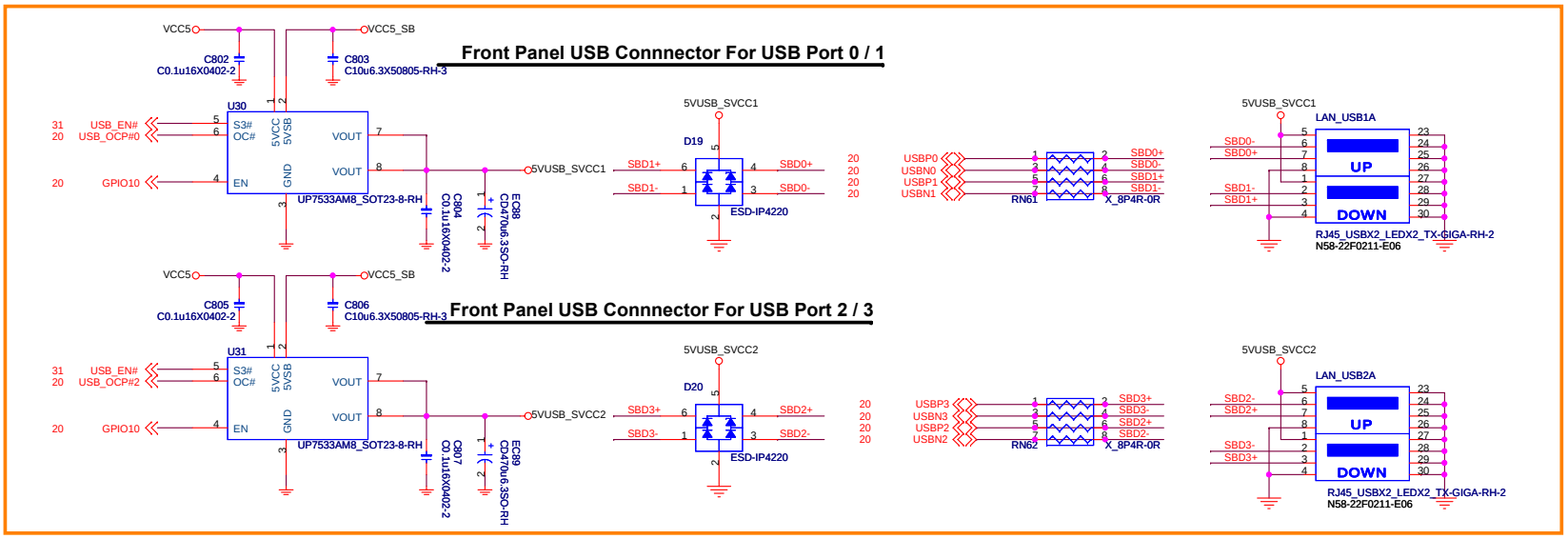
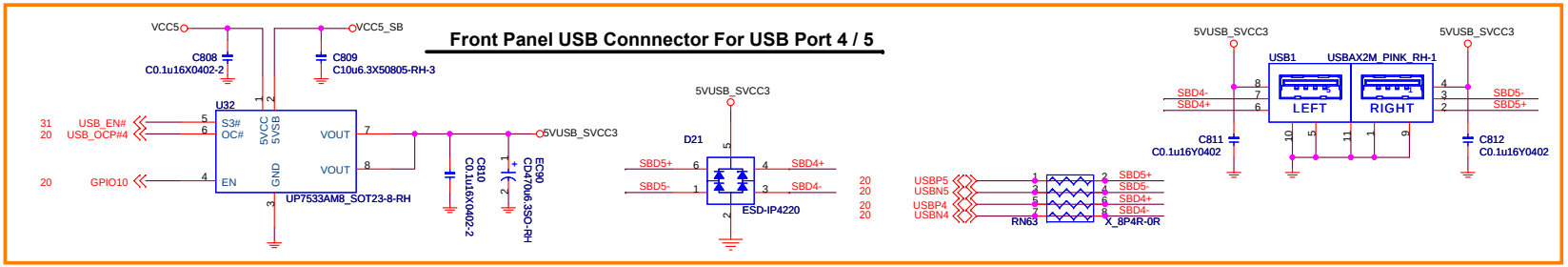
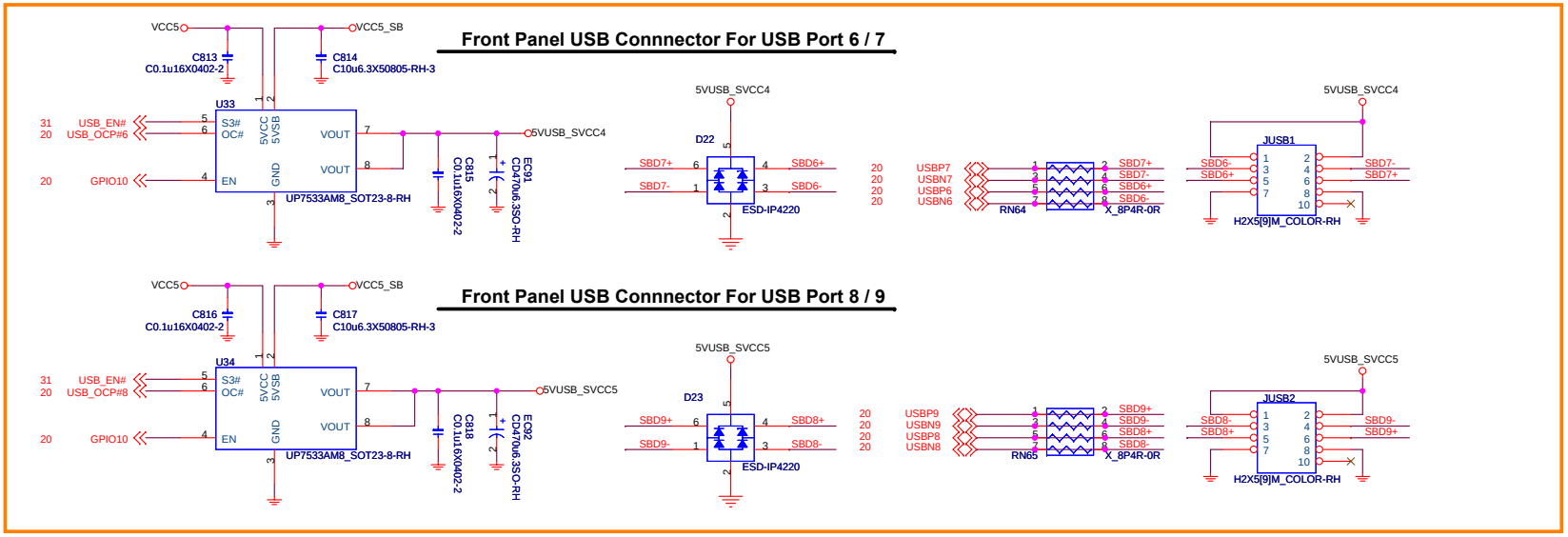
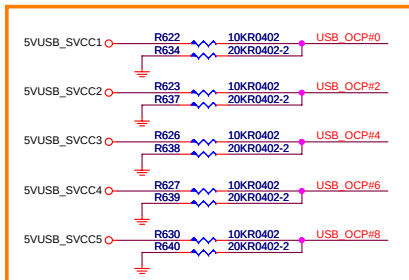
Front Panel and Real I/O USB Connector









MICRO-START INT'L CO.,LTD.

Title: Front / Rear USB Connectors

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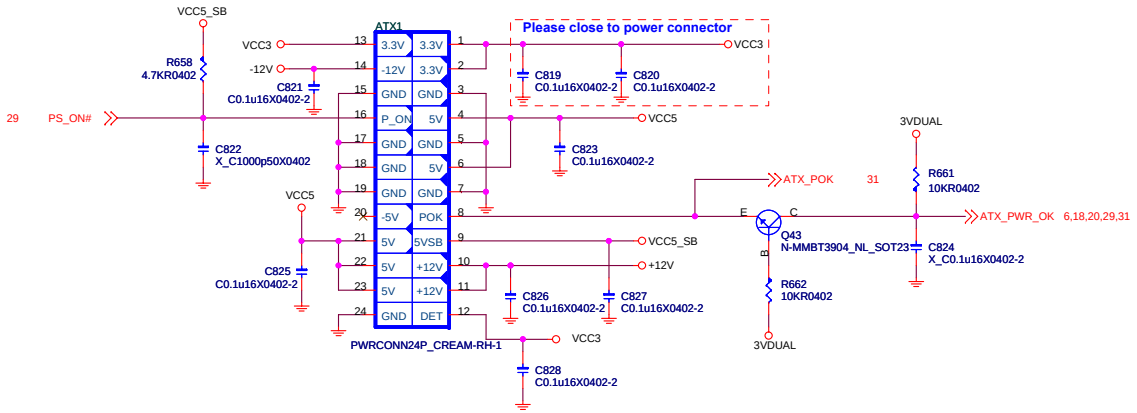
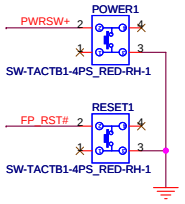
ATX Power Connector / Front Panel / LED

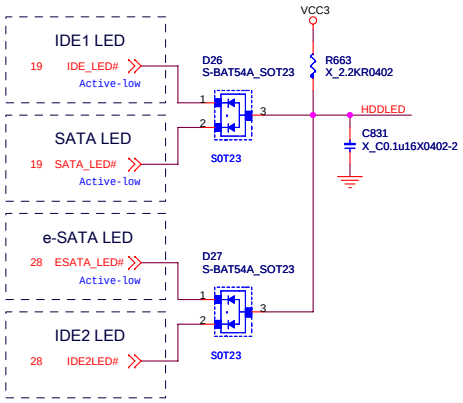
24 Pin ATX Power Connector



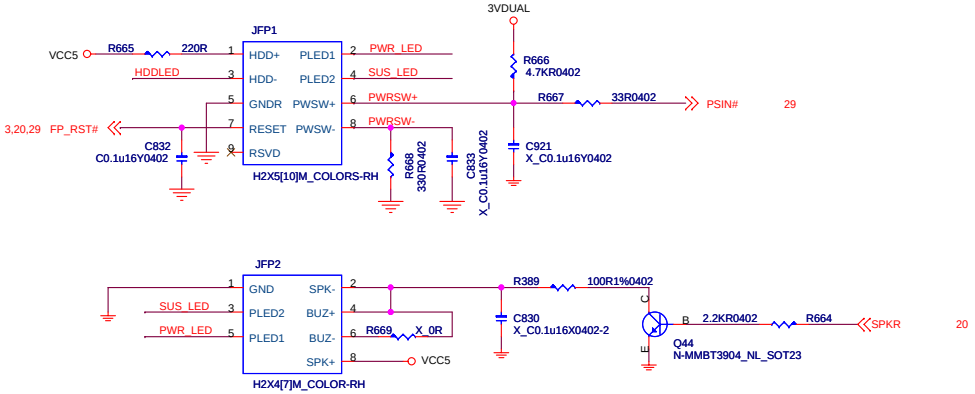
Power and Reset Button

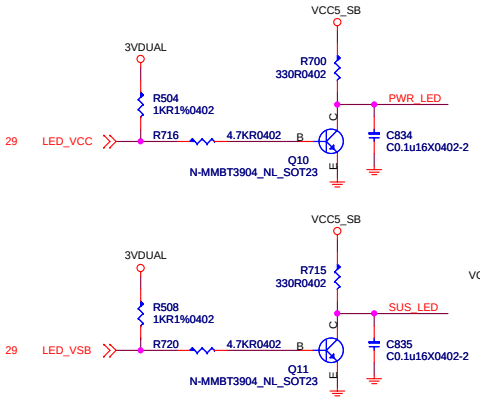


HDD LED

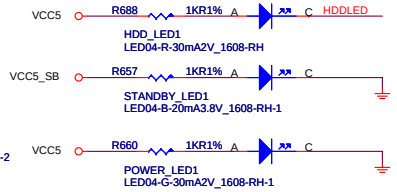


Front Panel





Power State LED



MICRO-START INT'L CO.,LTD.

Title	ATX Connector / Front Panel / LED	
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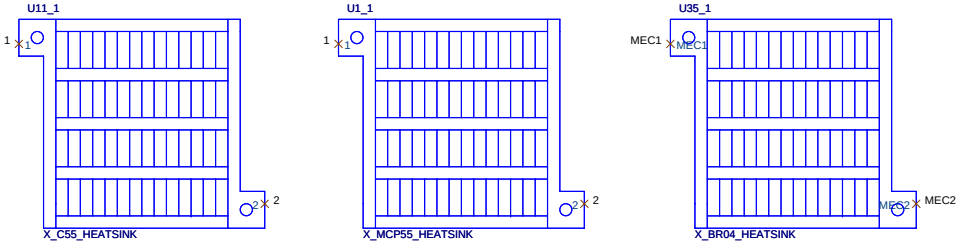
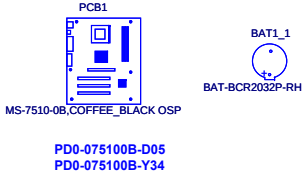
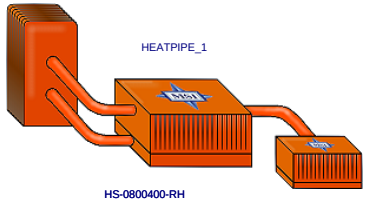
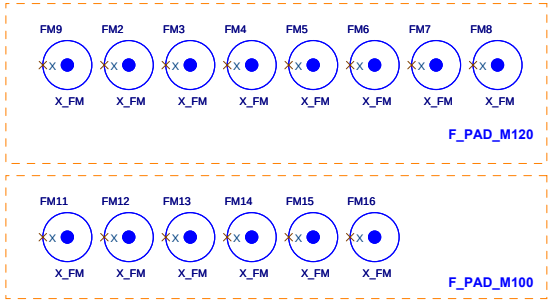


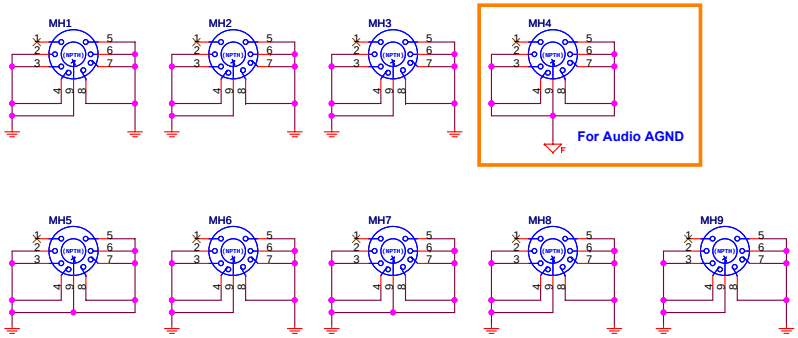




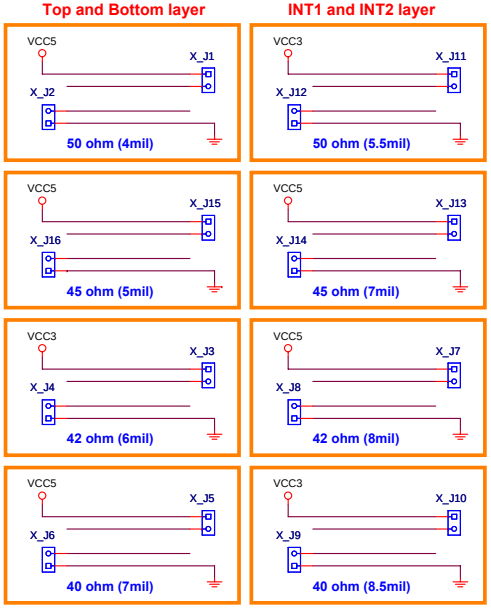
Optics Orientation Holes



PCB Mounting Holes



Simulation



MICRO-START INT'L CO.,LTD.

Title: Manual Parts		
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Power On/Off Sequence

MICRO-START INT'L CO.,LTD.		
Title: Power On/Off Sequence		
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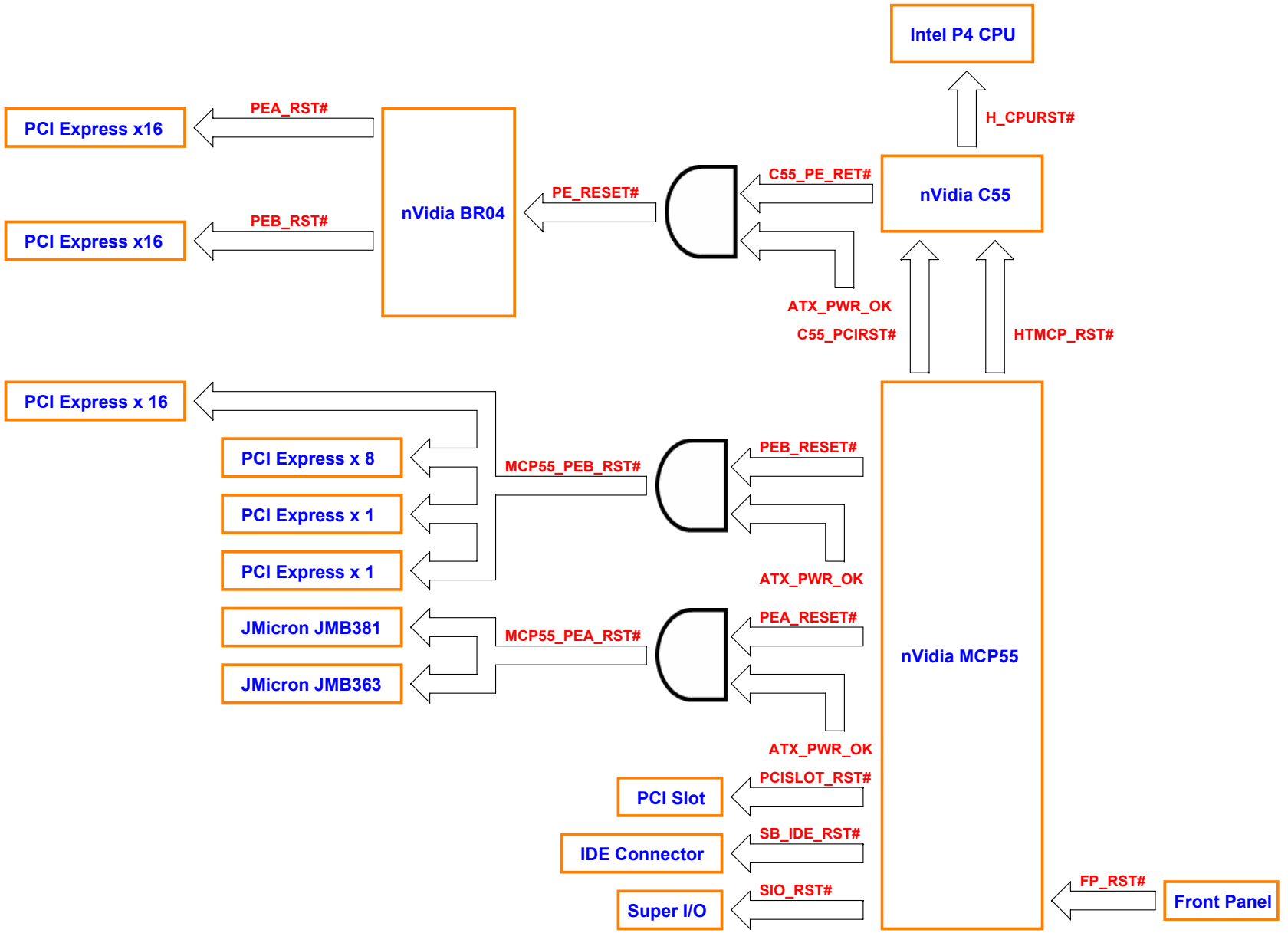
Syatem Reset Map



MICRO-START INT'L CO.,LTD.

Title: Reset Map		
Size	Document Number: MS-7510	Rev: 0B
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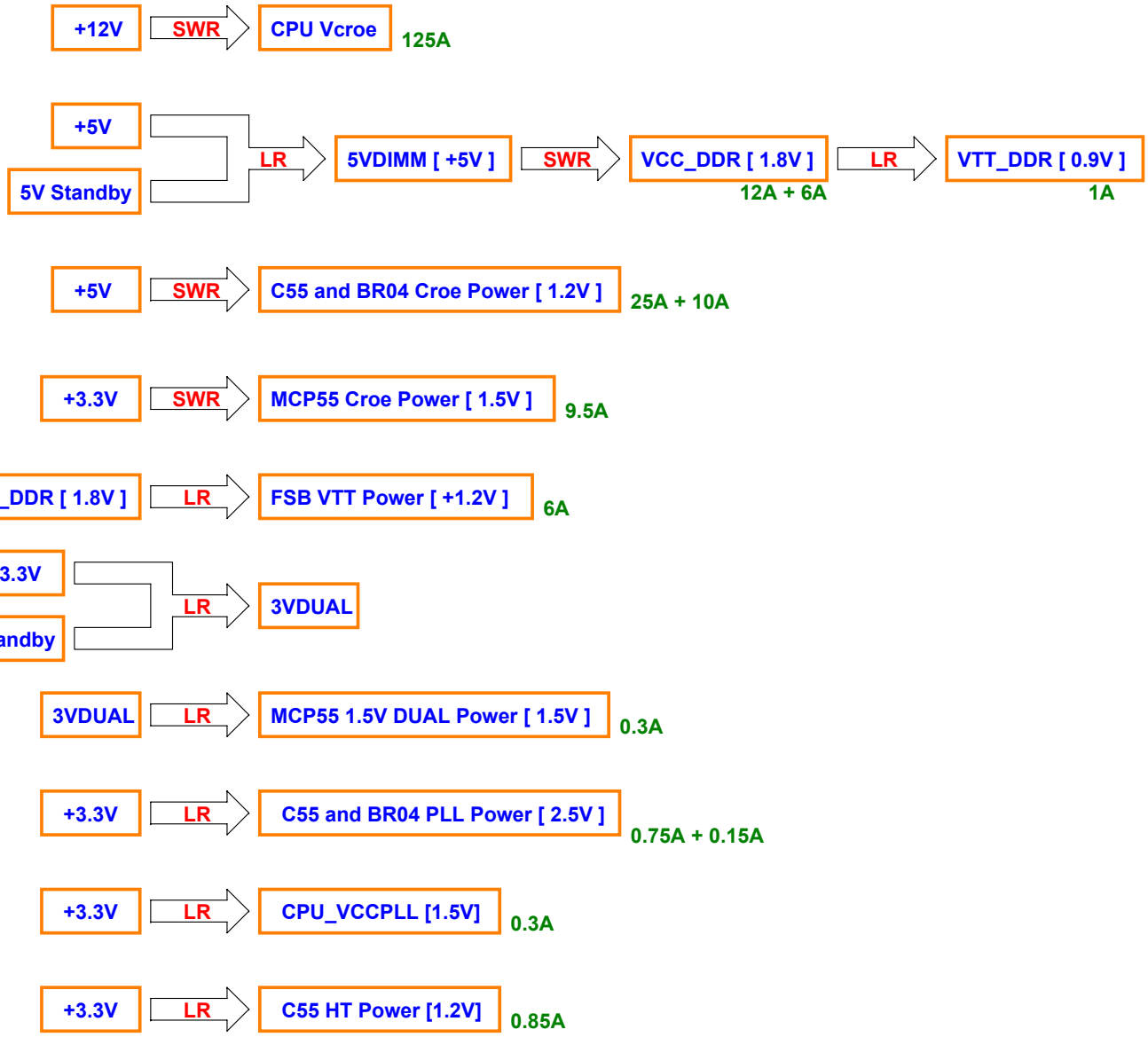
Syatem Power Map



MSI MICRO-START INT'L CO.,LTD.

Title: Cover Sheet

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Configuration & GPIO

PCI Configuration

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK	PCI Reset
PCI slot 1	PIRQ#A	PCI0REQ# PCI0GNT#	AD21	PCI_CLK0	PCISLOT_RST#

DDRII DIMM Configuration

DIMM1	DIMM2	DIMM3	DIMM4
A0 1010000B	A4 1010010B	A2 1010001B	A6 1010011B
0A	0B	1A	1B

SMBus Distribution

SMBus	Power	Load
SMBDATA SMBCLK	VCC3	MCP55 , JM363 , PWM , Super I/O , uPI Power IC PCI Express x16 Slot * 3 , PCI Express x 8 Slot * 1 , PCI Express x 1 Slot * 1 , PCI Slot
SMB_MEM_DATA SMB_MEM_CLK	VCC3_SB	MCP55

System Reset Signal

Signal	Device
PE_RESET#	BR04
H_CPURST#	CPU
HTMCP_RST#	C55
PE_A_RESET#	BR04 PCI Express x 16 Primary Slot
PE_B_RESET#	BR04 PCI Express x 16 Secondary Slot
PEA_RESET#	JMicron JMB363 eSATA Controller JMicron JMB381 IEEE 1394a Host Controller
PEB_RESET#	MCP55 PCI Express x 16 Slot MCP55 PCI Express x 8 Slot MCP55 PCI Express x 1 Slot
PCISLOT_RST#	MCP55 PCI Slot
C55_PCIRST#	C55
SB_IDE_RST#	Master IDE Connector
SIO_RST#	Super I/O

SuperI/O GPIO Function

Pin Name	Function Description
GP4	CPU_GTL_REF Select
GP5	Reset PWM
SLOTOCC#	Detect CPU remove or not
COPEN#	Detect Case Open or not

MCP55 GPIO Function

Pin Name	Function Description
GP10	USB Connector OC# Detect

Device Clock Signal

Signal	Device
CK_H_CPU# CK_H_CPU	C55 to CPU
HTMCP_DWNCLK0 HTMCP_DWNCLK0#	C55 to MCP55
HTMCP_UPCLK0 HTMCP_UPCLK0#	MCP55 to C55
PE_BR04_CLK PE_BR04_CLK#	C55 to BR04
BF_PE_CLK BF_PE_CLK#	C55 to Clock Buffer
PE_BR04_REFCLK PE_BR04_REFCLK#	Clock Buffer to BR04
PE_A_REFCLK PE_A_REFCLK#	Clock buffer to Express x 16 Primary Slot
PE_B_REFCLK PE_B_REFCLK#	Clock Buffer to Express x 16 Secondary Slot
MCPOUT_200MHZ MCPOUT_200MHZ#	MCP55 to C55
C55_25MHZ	MCP55 to C55
PE0SB_CLK PE0SB_CLK#	MCP55 to Express x 16 Slot
PE5SB_CLK PE5SB_CLK#	MCP55 to Express x 8 Slot
PE1SB_CLK PE1SB_CLK# PE2SB_CLK PE2SB_CLK#	MCP55 to PCI Express x 1 Slot
PE3SB_CLK PE3SB_CLK#	MCP55 to JMicron JMB363 eSATA Controller
PE4SB_CLK PE4SB_CLK#	MCP55 to JMicron JMB381 IEEE1394a Controller
PCI_CLK0	MCP55 to PCI Slot
SIO_PCLK	MCP55 to FinTek 71883FG Super I/O
LPC_PCLK	MCP55 to JTPM Pin Header

MICRO-START INT'L CO.,LTD.

Title: GPIO & Jumper Setting

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2007-07-25

Crate First Version Schematic

2007-08-08

7510-0A Net-in

2007-08-22

Update project Spec.
From PDC42819 change to JMB363

2007-09-07

Update nVidia PCI Express clock jitter issue solution

2007-09-12

Gerber Out

2007-09-25

Assembly

2007-10-01

HW gat sample board

2007-10-16

7510-0B Net-in

Update circuit

1. Change ACPI solution from MS12 to uPI

2007-10-30

7510-0B Gerber Out

MICRO-START INT'L CO.,LTD.

Title: History

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