MS-7508Ver:0A

CPU:

AMD AM2 and AM2R2

System Chipset:

NVDIA MCP78U/S

On Board Chipset:

Winbond Super I/O -- FINTEK71882
LAN -- RTL8211BL
HD Codec --ALC888
JIMCRO 1394
BIOS -- SPI ROM

Main Memory:

DDR 2*4(Max4GB)

Expansion Slots:

PCI 2.3 Slot *2

PWM:

ST6740+ST6741

NOTE:

all the 0ohm resistor default not stuff ,change footprint as R0402_6 or R0603_10 ,for costdown request

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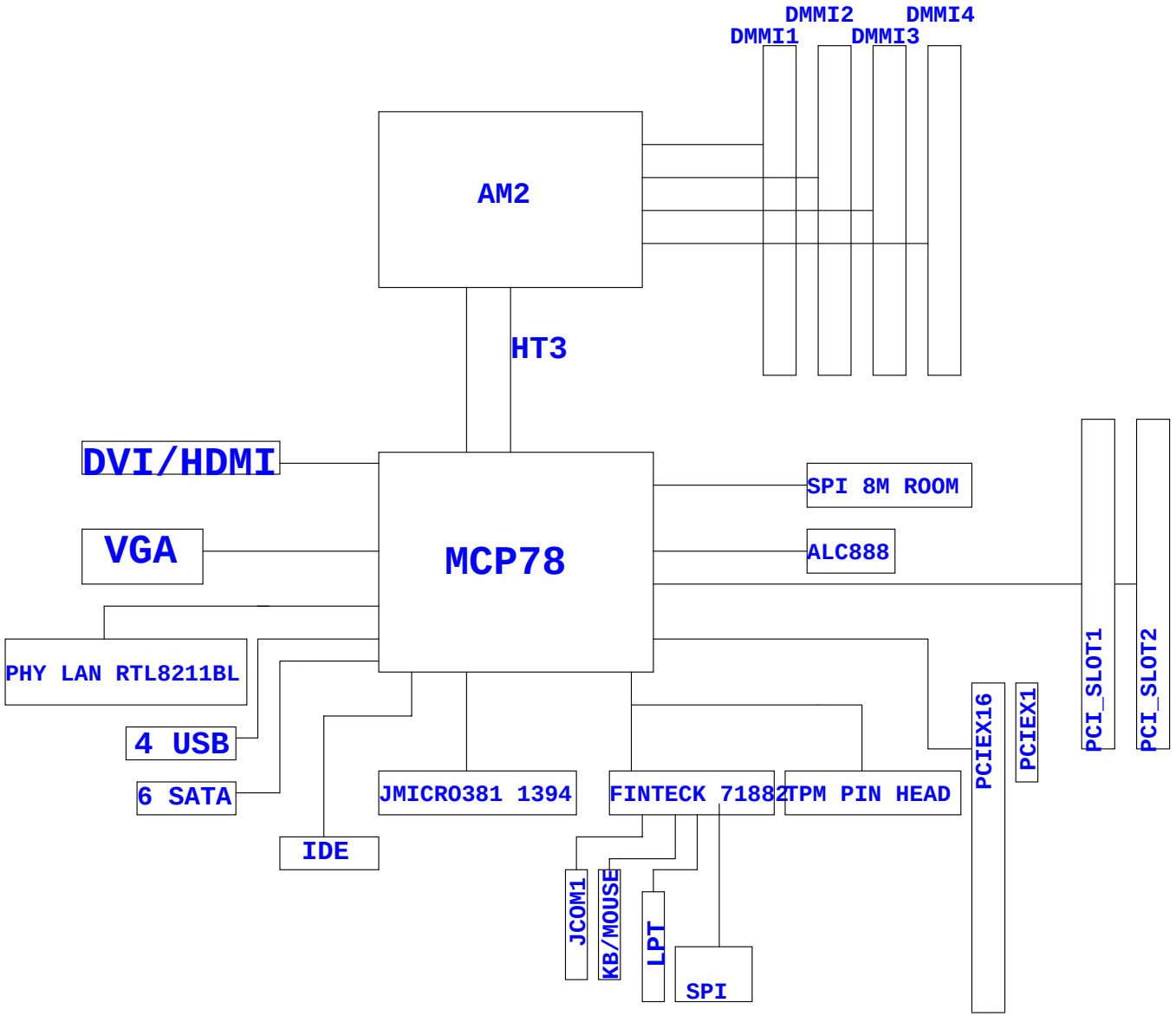

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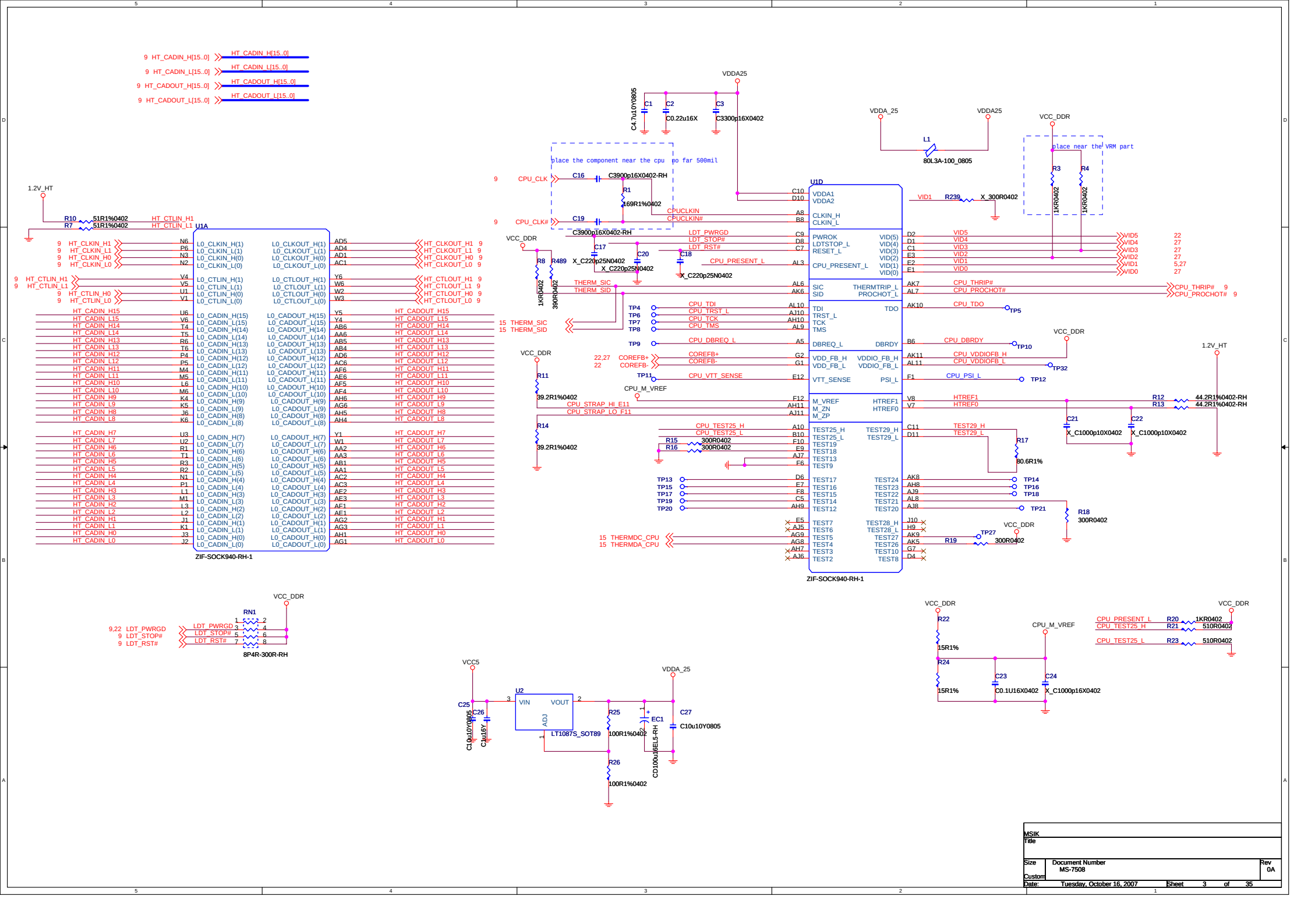
9 HT_CADIN_H[15..0] HT_CADIN_H[15..0]
9 HT_CADIN_L[15..0] HT_CADIN_L[15..0]
9 HT_CADOUT_H[15..0] HT_CADOUT_H[15..0]
9 HT_CADOUT_L[15..0] HT_CADOUT_L[15..0]
1.2V_HT
R10 51R1%0402 HT_CTLIN_H1
R7 51R1%0402 HT_CTLIN_L1
U1A
ZIF-SOCK940-RH-1
VDDA25
C1 C2 C3
C4.7u10Y0805
C0.22u16X
C3300p16X0402
place the component near the cpu no far 500mil
CPU_CLK C16 C3900p16X0402-RH
R1 169R1%0402
CPU_CLK# C19
CPUCLKIN
CPUCLKIN#
C3900p16X0402-RH
VCC_DDR
R8 1KR0402
R489 390R0402
C17 X_C220p25N0402
C20 X_C220p25N0402
C18 X_C220p25N0402
CPU_PRESENT_L
THERM_SIC
THERM_SID
15 THERM_SIC
15 THERM_SID
TP4 TP6 TP7 TP8
CPU_TDI
CPU_TRST_L
CPU_TCK
CPU_TMS
TP9 CPU_DBREQ_L
22,27 COREFB+
22 COREFB-
TP11 CPU_VTT_SENSE
R11 39.2R1%0402
CPU_M_VREF
CPU_STRAP_HI_E11
CPU_STRAP_LO_F11
R14 39.2R1%0402
CPU_TEST25_H
CPU_TEST25_L
R15 300R0402
R16 300R0402
TP13 TP15 TP17 TP19 TP20
15 THERMDC_CPU
15 THERMDA_CPU
U1D
ZIF-SOCK940-RH-1
VDDA_25
L1 80L3A-100_0805
VID1 R239 X_300R0402
place near the VRM part
R3 R4 1KR0402
VID5 VID4 VID3 VID2 VID1 VID0
CPU_THRIP#
CPU_PROCHOT#
CPU_TDO
TP5
VCC_DDR
CPU_DBRDY
TP10
CPU_VDDIOFB_H
CPU_VDDIOFB_L
TP32
CPU_PSI_L
TP12
1.2V_HT
HTREF1
HTREF0
R12 44.2R1%0402-RH
R13 44.2R1%0402-RH
C21 X_C1000p10X0402
C22 X_C1000p10X0402
TEST29_H
TEST29_L
R17 80.6R1%
TP14 TP16 TP18 TP21
R18 300R0402
R19 300R0402
TP27
RN1
9,22 LDT_PWRGD
9 LDT_STOP#
9 LDT_RST#
8P4R-300R-RH
VCC5
U2
VIN VOUT ADJ
LT1087S_SOT89
C25 C10u10Y0805
C26 C4u16Y
R25 100R1%0402
R26 100R1%0402
EC1 CD100u16EL5-RH
C27 C10u10Y0805
R22 15R1%
R24 15R1%
C23 C0.1U16X0402
C24 X_C1000p16X0402
CPU_PRESENT_L R20 1KR0402
CPU_TEST25_H R21 510R0402
CPU_TEST25_L R23 510R0402
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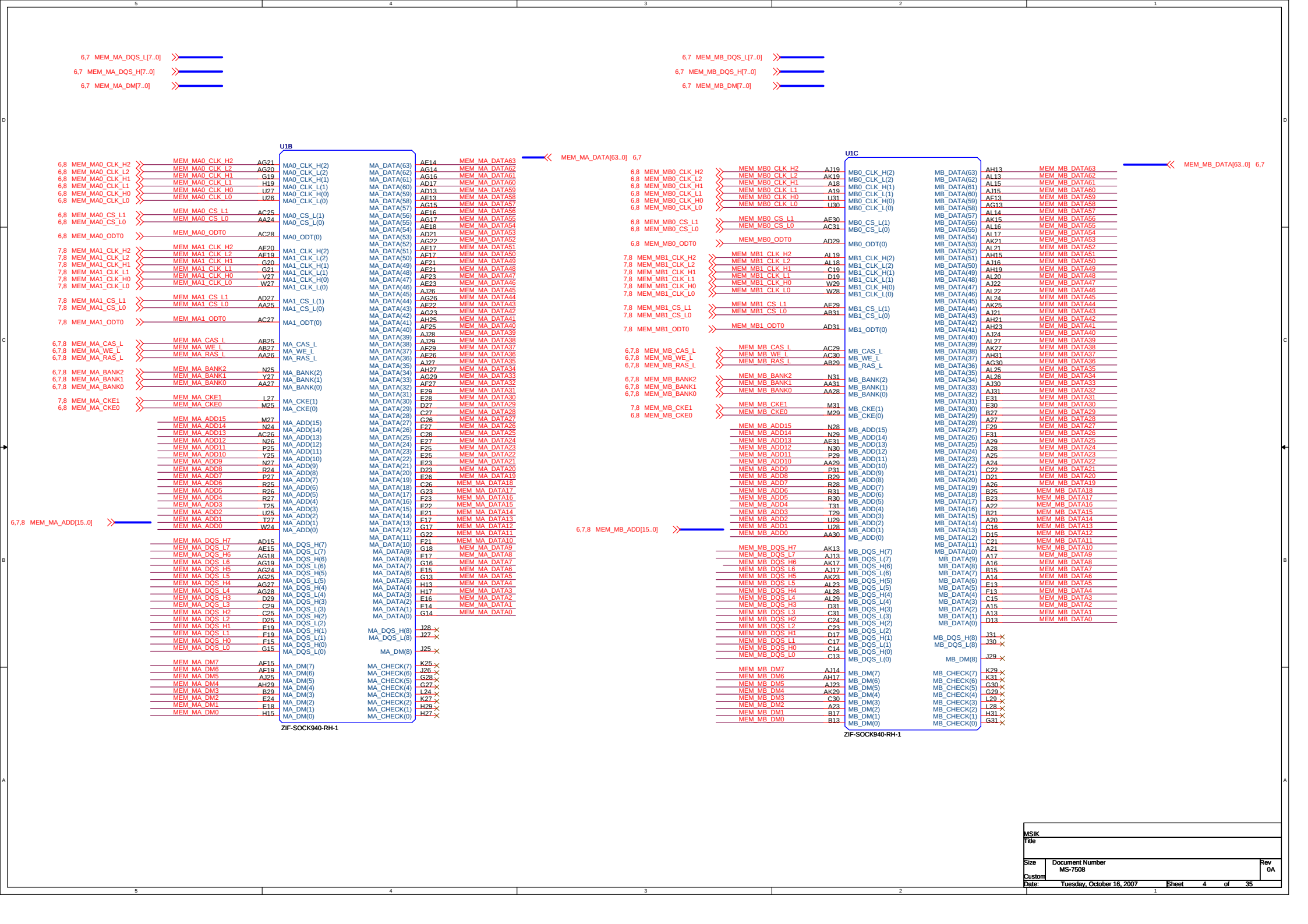
6,7 MEM_MA_DQS_L[7..0]
6,7 MEM_MA_DQS_H[7..0]
6,7 MEM_MA_DM[7..0]
6,7 MEM_MB_DQS_L[7..0]
6,7 MEM_MB_DQS_H[7..0]
6,7 MEM_MB_DM[7..0]
U1B
MEM_MA_DATA[63..0] 6,7
MEM_MB_DATA[63..0] 6,7
U1C
6,7,8 MEM_MA_ADD[15..0]
6,7,8 MEM_MB_ADD[15..0]
ZIF-SOCK940-RH-1
ZIF-SOCK940-RH-1
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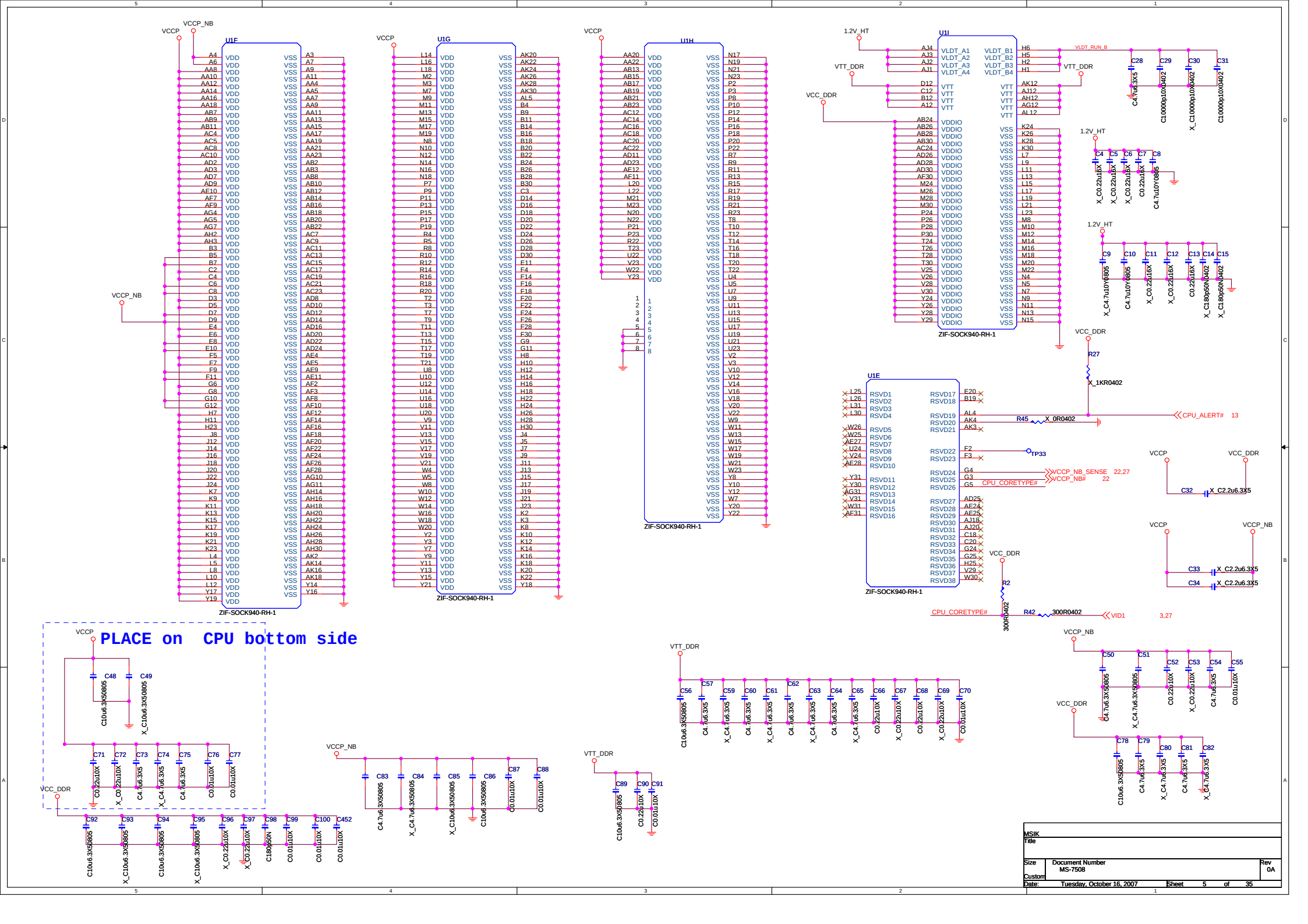
PLACE on CPU bottom side
U1F
U1G
U1H
U1I
U1E
ZIF-SOCK940-RH-1
VCCP
VCCP_NB
VCC_DDR
VTT_DDR
1.2V_HT
CPU_ALERT# 13
CPU_CORETYPE#
VCCP_NB_SENSE 22,27
VCCP_NB# 22
VID1 3,27
TP33
R27 X_1KR0402
R45 X_0R0402
R2 300R0402
R42 300R0402
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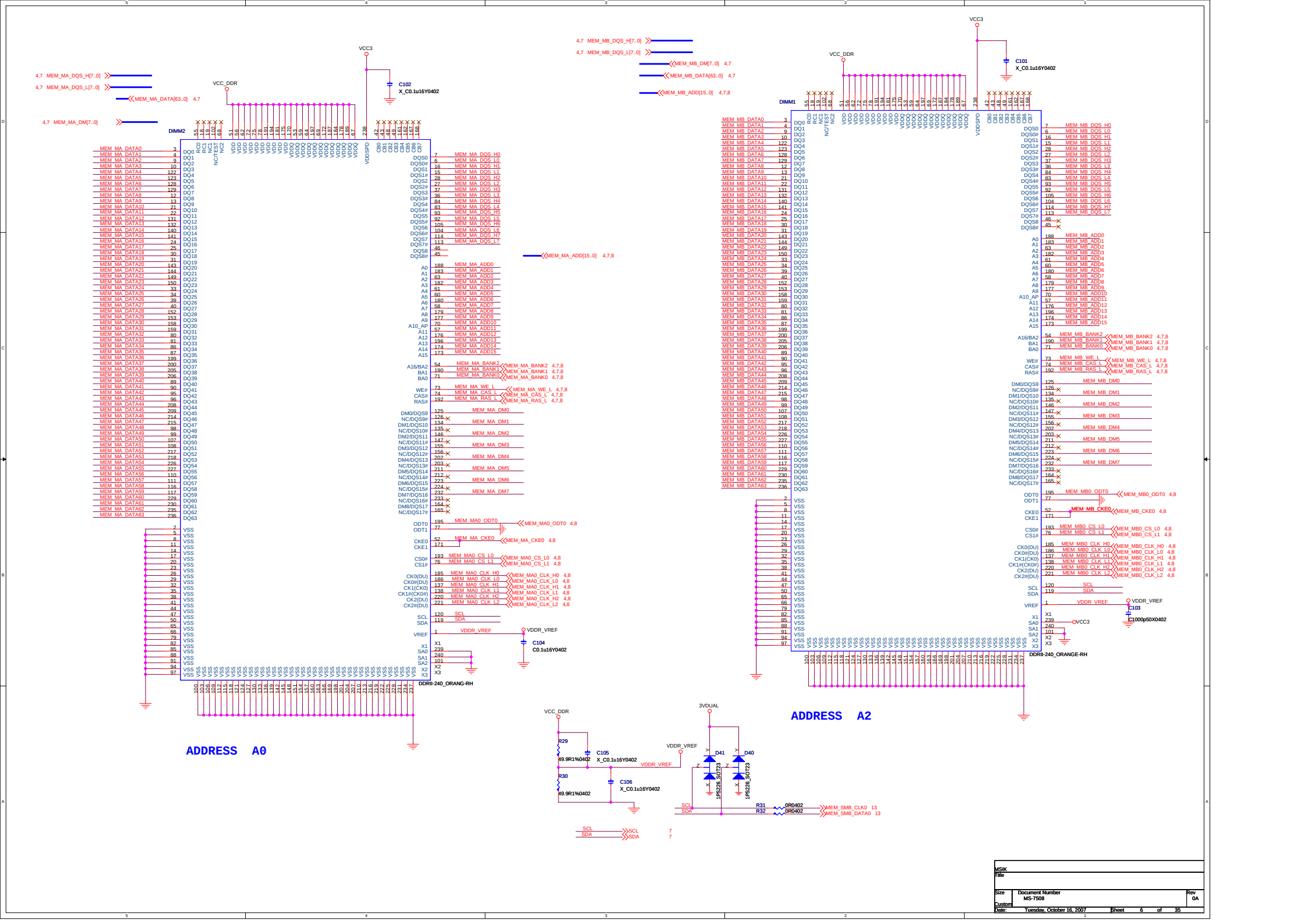
DIMM2
DIMM1
DDRII-240_ORANG-RH
DDRII-240_ORANGE-RH
VCC_DDR
VCC3
3VDUAL
VDDR_VREF
C102
X_C0.1u16Y0402
C101
X_C0.1u16Y0402
C104
C0.1u16Y0402
C103
C1000p50X0402
C105
X_C0.1u16Y0402
C106
X_C0.1u16Y0402
R29
49.9R1%0402
R30
49.9R1%0402
R31
R32
0R0402
D41
D40
1PS226_SOT23
ADDRESS A0
ADDRESS A2
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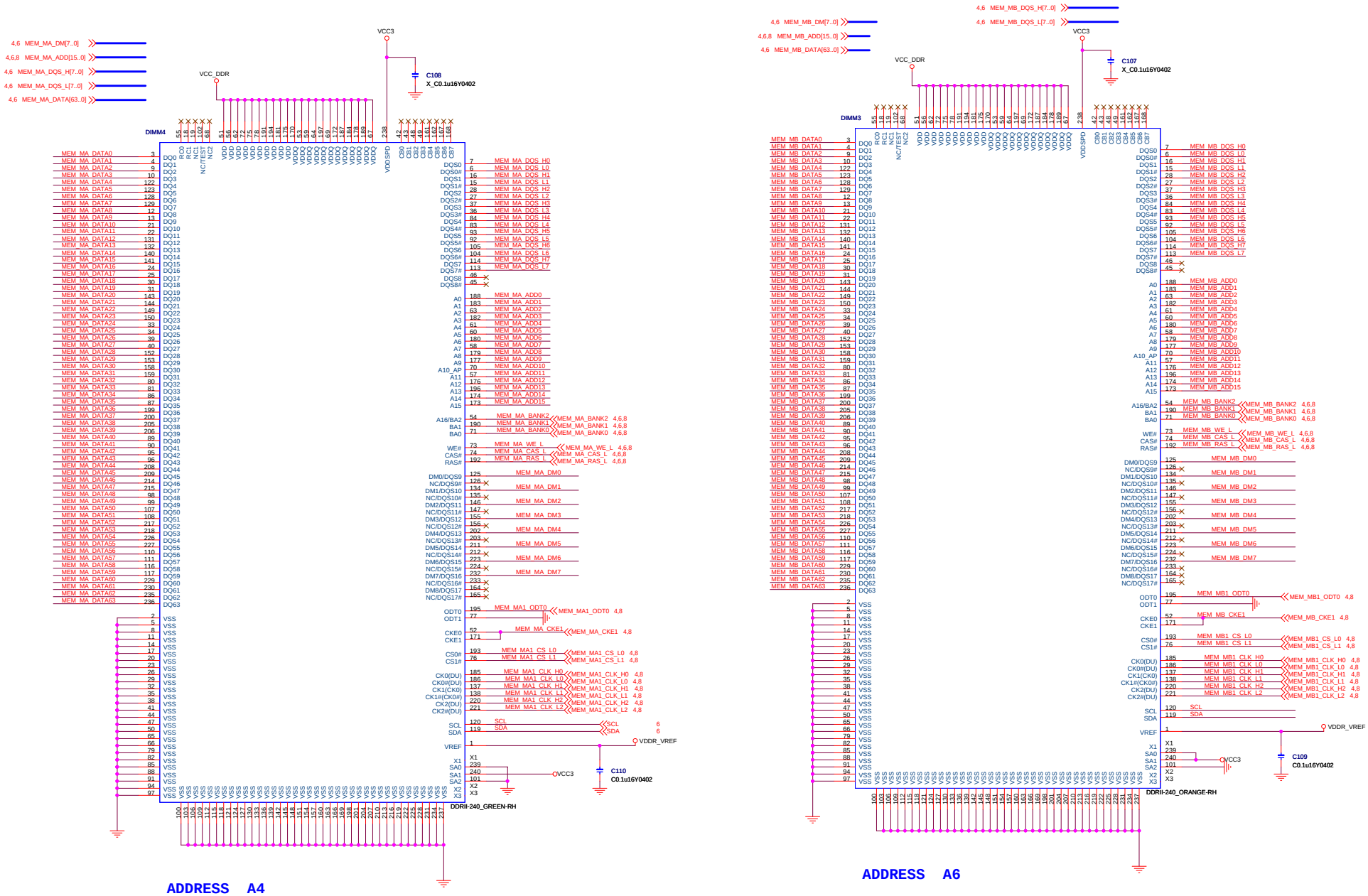
4,6 MEM_MA_DM[7..0]
4,6,8 MEM_MA_ADD[15..0]
4,6 MEM_MA_DQS_H[7..0]
4,6 MEM_MA_DQS_L[7..0]
4,6 MEM_MA_DATA[63..0]
VCC3
VCC_DDR
C108
X_C0.1u16Y0402
DIMM4
MEM_MA_DATA0
MEM_MA_DATA1
MEM_MA_DATA2
MEM_MA_DATA3
MEM_MA_DATA4
MEM_MA_DATA5
MEM_MA_DATA6
MEM_MA_DATA7
MEM_MA_DATA8
MEM_MA_DATA9
MEM_MA_DATA10
MEM_MA_DATA11
MEM_MA_DATA12
MEM_MA_DATA13
MEM_MA_DATA14
MEM_MA_DATA15
MEM_MA_DATA16
MEM_MA_DATA17
MEM_MA_DATA18
MEM_MA_DATA19
MEM_MA_DATA20
MEM_MA_DATA21
MEM_MA_DATA22
MEM_MA_DATA23
MEM_MA_DATA24
MEM_MA_DATA25
MEM_MA_DATA26
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MEM_MA_DATA29
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MEM_MA_DATA43
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MEM_MA_DATA45
MEM_MA_DATA46
MEM_MA_DATA47
MEM_MA_DATA48
MEM_MA_DATA49
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MEM_MA_DATA51
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MEM_MA_DATA53
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MEM_MA_DATA56
MEM_MA_DATA57
MEM_MA_DATA58
MEM_MA_DATA59
MEM_MA_DATA60
MEM_MA_DATA61
MEM_MA_DATA62
MEM_MA_DATA63
MEM_MA_DQS_H0
MEM_MA_DQS_L0
MEM_MA_DQS_H1
MEM_MA_DQS_L1
MEM_MA_DQS_H2
MEM_MA_DQS_L2
MEM_MA_DQS_H3
MEM_MA_DQS_L3
MEM_MA_DQS_H4
MEM_MA_DQS_L4
MEM_MA_DQS_H5
MEM_MA_DQS_L5
MEM_MA_DQS_H6
MEM_MA_DQS_L6
MEM_MA_DQS_H7
MEM_MA_DQS_L7
MEM_MA_ADD0
MEM_MA_ADD1
MEM_MA_ADD2
MEM_MA_ADD3
MEM_MA_ADD4
MEM_MA_ADD5
MEM_MA_ADD6
MEM_MA_ADD7
MEM_MA_ADD8
MEM_MA_ADD9
MEM_MA_ADD10
MEM_MA_ADD11
MEM_MA_ADD12
MEM_MA_ADD13
MEM_MA_ADD14
MEM_MA_ADD15
MEM_MA_BANK2
MEM_MA_BANK1
MEM_MA_BANK0
MEM_MA_WE_L
MEM_MA_CAS_L
MEM_MA_RAS_L
MEM_MA_DM0
MEM_MA_DM1
MEM_MA_DM2
MEM_MA_DM3
MEM_MA_DM4
MEM_MA_DM5
MEM_MA_DM6
MEM_MA_DM7
MEM_MA1_ODT0
MEM_MA_CKE1
MEM_MA1_CS_L0
MEM_MA1_CS_L1
MEM_MA1_CLK_H0
MEM_MA1_CLK_L0
MEM_MA1_CLK_H1
MEM_MA1_CLK_L1
MEM_MA1_CLK_H2
MEM_MA1_CLK_L2
SCL
SDA
VDDR_VREF
C110
C0.1u16Y0402
DDRII-240_GREEN-RH
ADDRESS A4
4,6 MEM_MB_DM[7..0]
4,6,8 MEM_MB_ADD[15..0]
4,6 MEM_MB_DATA[63..0]
4,6 MEM_MB_DQS_H[7..0]
4,6 MEM_MB_DQS_L[7..0]
VCC3
VCC_DDR
C107
X_C0.1u16Y0402
DIMM3
MEM_MB_DATA0
MEM_MB_DATA1
MEM_MB_DATA2
MEM_MB_DATA3
MEM_MB_DATA4
MEM_MB_DATA5
MEM_MB_DATA6
MEM_MB_DATA7
MEM_MB_DATA8
MEM_MB_DATA9
MEM_MB_DATA10
MEM_MB_DATA11
MEM_MB_DATA12
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MEM_MB_DATA27
MEM_MB_DATA28
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MEM_MB_DATA30
MEM_MB_DATA31
MEM_MB_DATA32
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MEM_MB_DATA35
MEM_MB_DATA36
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MEM_MB_DATA38
MEM_MB_DATA39
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MEM_MB_DATA45
MEM_MB_DATA46
MEM_MB_DATA47
MEM_MB_DATA48
MEM_MB_DATA49
MEM_MB_DATA50
MEM_MB_DATA51
MEM_MB_DATA52
MEM_MB_DATA53
MEM_MB_DATA54
MEM_MB_DATA55
MEM_MB_DATA56
MEM_MB_DATA57
MEM_MB_DATA58
MEM_MB_DATA59
MEM_MB_DATA60
MEM_MB_DATA61
MEM_MB_DATA62
MEM_MB_DATA63
MEM_MB_DQS_H0
MEM_MB_DQS_L0
MEM_MB_DQS_H1
MEM_MB_DQS_L1
MEM_MB_DQS_H2
MEM_MB_DQS_L2
MEM_MB_DQS_H3
MEM_MB_DQS_L3
MEM_MB_DQS_H4
MEM_MB_DQS_L4
MEM_MB_DQS_H5
MEM_MB_DQS_L5
MEM_MB_DQS_H6
MEM_MB_DQS_L6
MEM_MB_DQS_H7
MEM_MB_DQS_L7
MEM_MB_ADD0
MEM_MB_ADD1
MEM_MB_ADD2
MEM_MB_ADD3
MEM_MB_ADD4
MEM_MB_ADD5
MEM_MB_ADD6
MEM_MB_ADD7
MEM_MB_ADD8
MEM_MB_ADD9
MEM_MB_ADD10
MEM_MB_ADD11
MEM_MB_ADD12
MEM_MB_ADD13
MEM_MB_ADD14
MEM_MB_ADD15
MEM_MB_BANK2
MEM_MB_BANK1
MEM_MB_BANK0
MEM_MB_WE_L
MEM_MB_CAS_L
MEM_MB_RAS_L
MEM_MB_DM0
MEM_MB_DM1
MEM_MB_DM2
MEM_MB_DM3
MEM_MB_DM4
MEM_MB_DM5
MEM_MB_DM6
MEM_MB_DM7
MEM_MB1_ODT0
MEM_MB_CKE1
MEM_MB1_CS_L0
MEM_MB1_CS_L1
MEM_MB1_CLK_H0
MEM_MB1_CLK_L0
MEM_MB1_CLK_H1
MEM_MB1_CLK_L1
MEM_MB1_CLK_H2
MEM_MB1_CLK_L2
SCL
SDA
VDDR_VREF
C109
C0.1u16Y0402
DDRII-240_ORANGE-RH
ADDRESS A6
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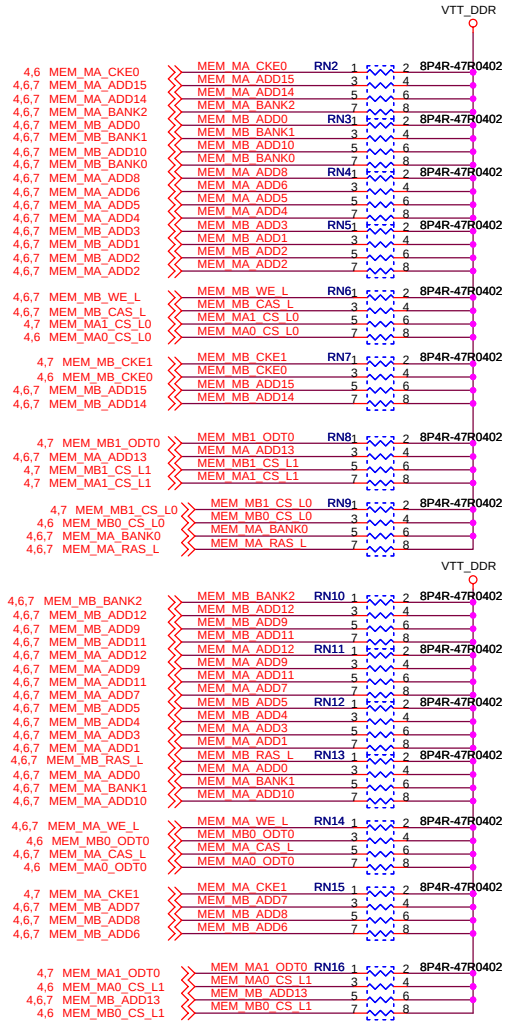
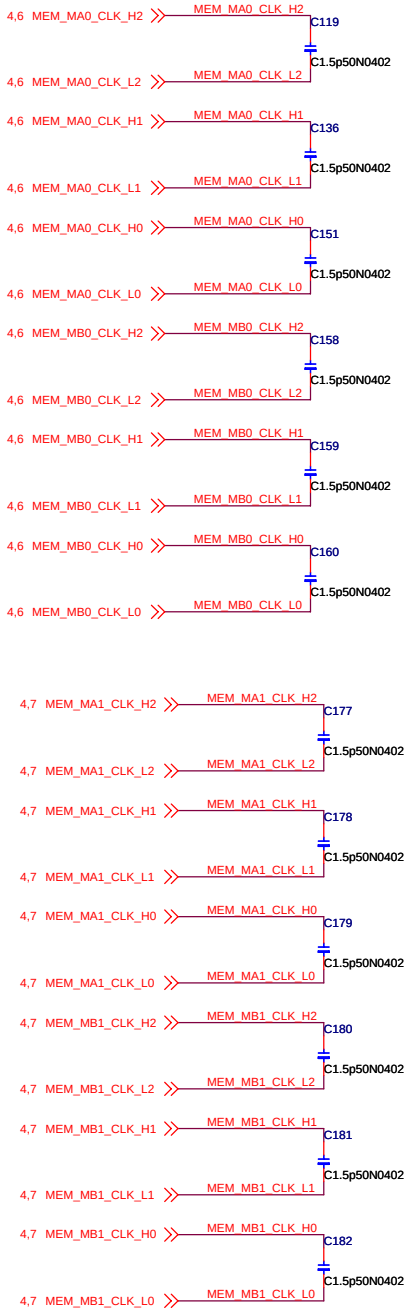
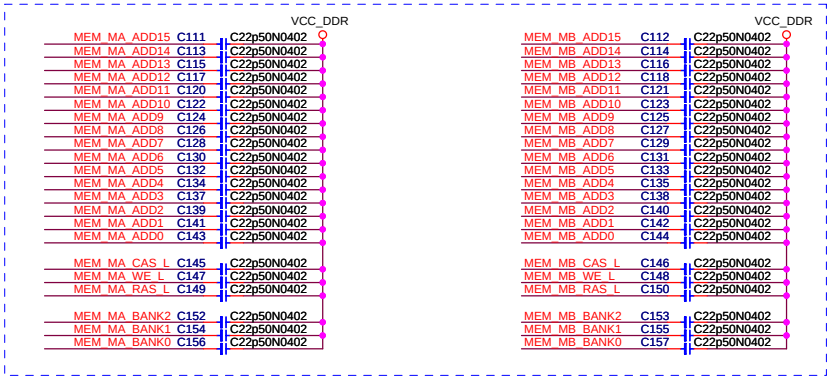
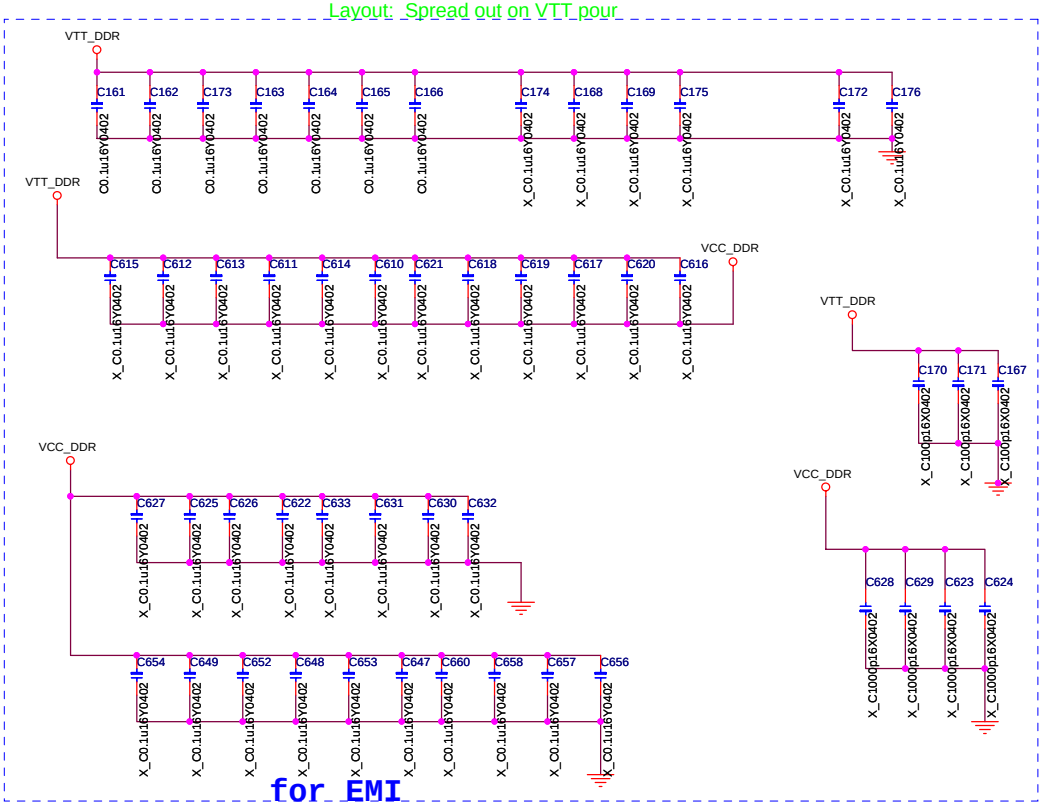






Decoupling Between Processor and DIMMs

Layout: Spread out on VTT pour



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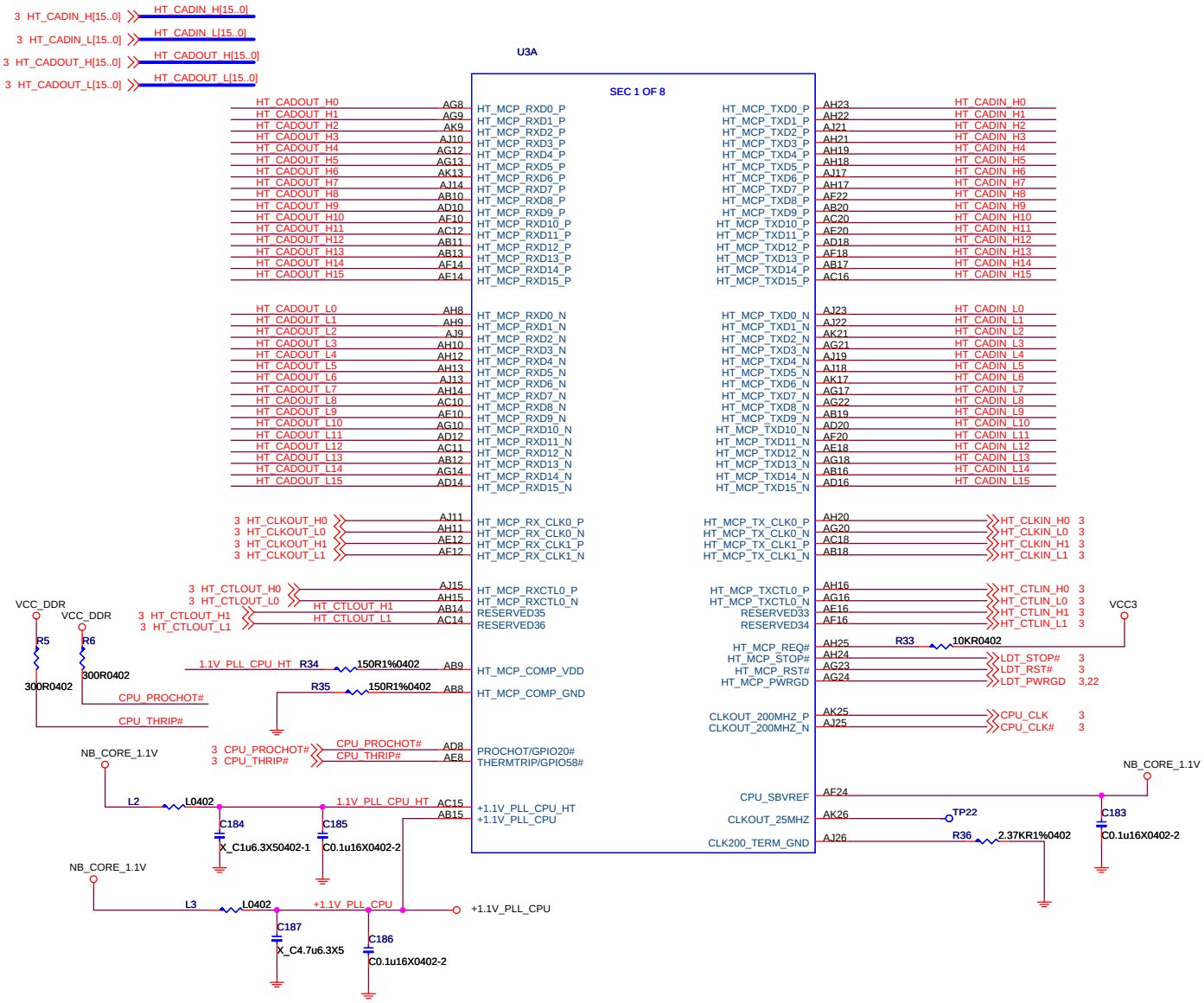

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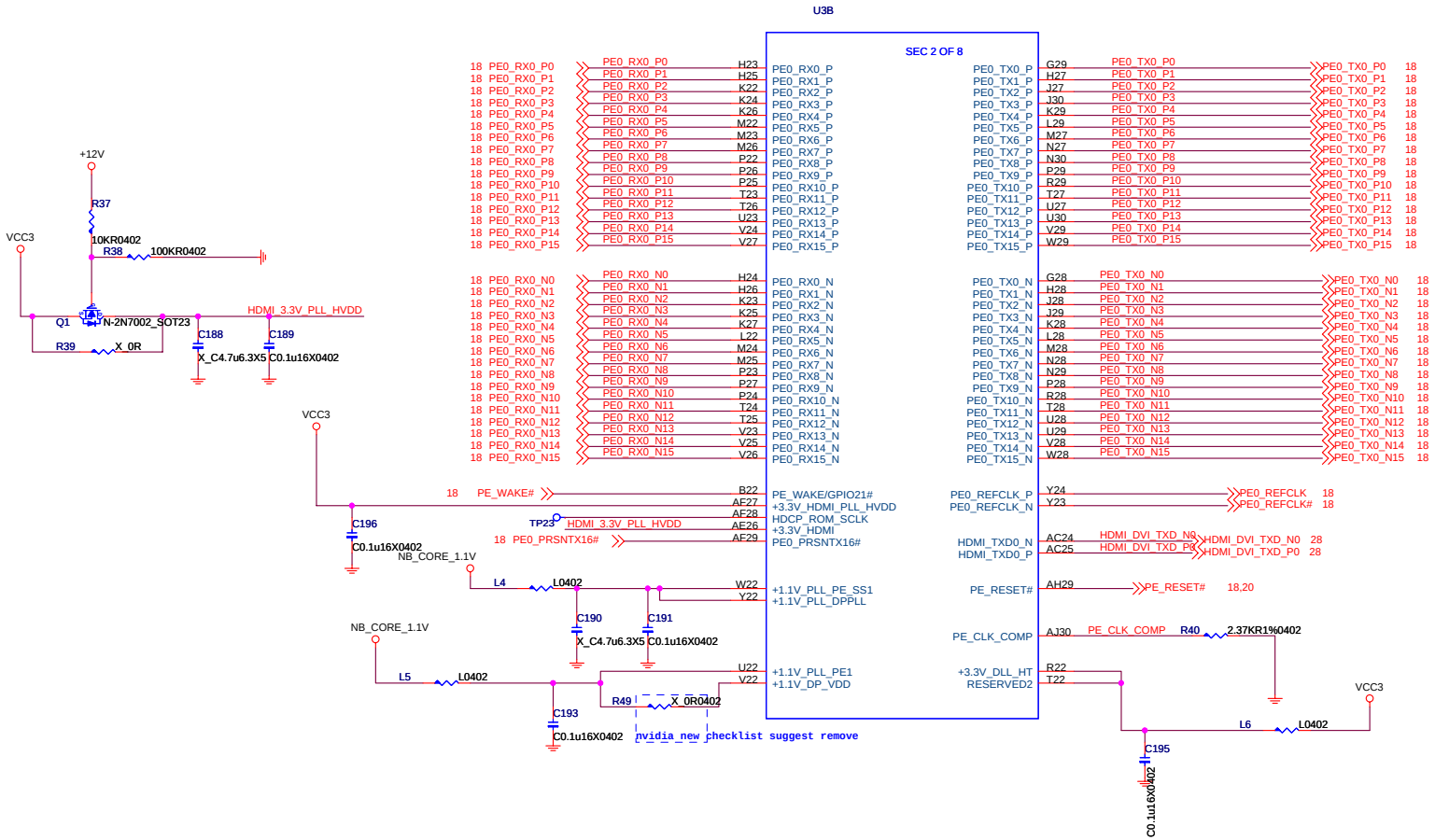

18	PE0_RX0_P0	PE0_RX0_P0	H23	PE0_RX0_P	PE0_TX0_P	G29	PE0_TX0_P0	PE0_TX0_P0	18
18	PE0_RX0_P1	PE0_RX0_P1	H25	PE0_RX1_P	PE0_TX1_P	H27	PE0_TX0_P1	PE0_TX0_P1	18
18	PE0_RX0_P2	PE0_RX0_P2	K22	PE0_RX2_P	PE0_TX2_P	J27	PE0_TX0_P2	PE0_TX0_P2	18
18	PE0_RX0_P3	PE0_RX0_P3	K24	PE0_RX3_P	PE0_TX3_P	J30	PE0_TX0_P3	PE0_TX0_P3	18
18	PE0_RX0_P4	PE0_RX0_P4	K26	PE0_RX4_P	PE0_TX4_P	K29	PE0_TX0_P4	PE0_TX0_P4	18
18	PE0_RX0_P5	PE0_RX0_P5	M22	PE0_RX5_P	PE0_TX5_P	L29	PE0_TX0_P5	PE0_TX0_P5	18
18	PE0_RX0_P6	PE0_RX0_P6	M23	PE0_RX6_P	PE0_TX6_P	M27	PE0_TX0_P6	PE0_TX0_P6	18
18	PE0_RX0_P7	PE0_RX0_P7	M26	PE0_RX7_P	PE0_TX7_P	N27	PE0_TX0_P7	PE0_TX0_P7	18
18	PE0_RX0_P8	PE0_RX0_P8	P22	PE0_RX8_P	PE0_TX8_P	N30	PE0_TX0_P8	PE0_TX0_P8	18
18	PE0_RX0_P9	PE0_RX0_P9	P26	PE0_RX9_P	PE0_TX9_P	P29	PE0_TX0_P9	PE0_TX0_P9	18
18	PE0_RX0_P10	PE0_RX0_P10	P25	PE0_RX10_P	PE0_TX10_P	R29	PE0_TX0_P10	PE0_TX0_P10	18
18	PE0_RX0_P11	PE0_RX0_P11	T23	PE0_RX11_P	PE0_TX11_P	T27	PE0_TX0_P11	PE0_TX0_P11	18
18	PE0_RX0_P12	PE0_RX0_P12	T26	PE0_RX12_P	PE0_TX12_P	U27	PE0_TX0_P12	PE0_TX0_P12	18
18	PE0_RX0_P13	PE0_RX0_P13	U23	PE0_RX13_P	PE0_TX13_P	U30	PE0_TX0_P13	PE0_TX0_P13	18
18	PE0_RX0_P14	PE0_RX0_P14	V24	PE0_RX14_P	PE0_TX14_P	V29	PE0_TX0_P14	PE0_TX0_P14	18
18	PE0_RX0_P15	PE0_RX0_P15	V27	PE0_RX15_P	PE0_TX15_P	W29	PE0_TX0_P15	PE0_TX0_P15	18
18	PE0_RX0_N0	PE0_RX0_N0	H24	PE0_RX0_N	PE0_TX0_N	G28	PE0_TX0_N0	PE0_TX0_N0	18
18	PE0_RX0_N1	PE0_RX0_N1	H26	PE0_RX1_N	PE0_TX1_N	H28	PE0_TX0_N1	PE0_TX0_N1	18
18	PE0_RX0_N2	PE0_RX0_N2	K23	PE0_RX2_N	PE0_TX2_N	J28	PE0_TX0_N2	PE0_TX0_N2	18
18	PE0_RX0_N3	PE0_RX0_N3	K25	PE0_RX3_N	PE0_TX3_N	J29	PE0_TX0_N3	PE0_TX0_N3	18
18	PE0_RX0_N4	PE0_RX0_N4	K27	PE0_RX4_N	PE0_TX4_N	K28	PE0_TX0_N4	PE0_TX0_N4	18
18	PE0_RX0_N5	PE0_RX0_N5	L22	PE0_RX5_N	PE0_TX5_N	L28	PE0_TX0_N5	PE0_TX0_N5	18
18	PE0_RX0_N6	PE0_RX0_N6	M24	PE0_RX6_N	PE0_TX6_N	M28	PE0_TX0_N6	PE0_TX0_N6	18
18	PE0_RX0_N7	PE0_RX0_N7	M25	PE0_RX7_N	PE0_TX7_N	N28	PE0_TX0_N7	PE0_TX0_N7	18
18	PE0_RX0_N8	PE0_RX0_N8	P23	PE0_RX8_N	PE0_TX8_N	N29	PE0_TX0_N8	PE0_TX0_N8	18
18	PE0_RX0_N9	PE0_RX0_N9	P27	PE0_RX9_N	PE0_TX9_N	P28	PE0_TX0_N9	PE0_TX0_N9	18
18	PE0_RX0_N10	PE0_RX0_N10	P24	PE0_RX10_N	PE0_TX10_N	R28	PE0_TX0_N10	PE0_TX0_N10	18
18	PE0_RX0_N11	PE0_RX0_N11	T24	PE0_RX11_N	PE0_TX11_N	T28	PE0_TX0_N11	PE0_TX0_N11	18
18	PE0_RX0_N12	PE0_RX0_N12	T25	PE0_RX12_N	PE0_TX12_N	U28	PE0_TX0_N12	PE0_TX0_N12	18
18	PE0_RX0_N13	PE0_RX0_N13	V23	PE0_RX13_N	PE0_TX13_N	U29	PE0_TX0_N13	PE0_TX0_N13	18
18	PE0_RX0_N14	PE0_RX0_N14	V25	PE0_RX14_N	PE0_TX14_N	V28	PE0_TX0_N14	PE0_TX0_N14	18
18	PE0_RX0_N15	PE0_RX0_N15	V26	PE0_RX15_N	PE0_TX15_N	W28	PE0_TX0_N15	PE0_TX0_N15	18

18	PE_WAKE#		B22	PE_WAKE/GPIO21#					
			AF27	+3.3V_HDMI_PLL_HVDD					
			AF28	HDCP_ROM_SCLK					
	TP23	HDMI_3.3V_PLL_HVDD	AE26	+3.3V_HDMI					
18	PE0_PRSNTX16#		AE29	PE0_PRSNTX16#					
			W22	+1.1V_PLL_PE_SS1					
			Y22	+1.1V_PLL_DPPLL					
			U22	+1.1V_PLL_PE1					
			V22	+1.1V_DP_VDD					
					PE0_REFCLK_P	Y24	PE0_REFCLK	PE0_REFCLK	18
					PE0_REFCLK_N	Y23	PE0_REFCLK#	PE0_REFCLK#	18
					HDMI_TXD0_N	AC24	HDMI_DVI_TXD_N0	HDMI_DVI_TXD_N0	28
					HDMI_TXD0_P	AC25	HDMI_DVI_TXD_P0	HDMI_DVI_TXD_P0	28
					PE_RESET#	AH29	PE_RESET#		18,20
					PE_CLK_COMP	AJ30	PE_CLK_COMP	R40	2.37KR1%0402
					+3.3V_DLL_HT	R22			
					RESERVED2	T22			

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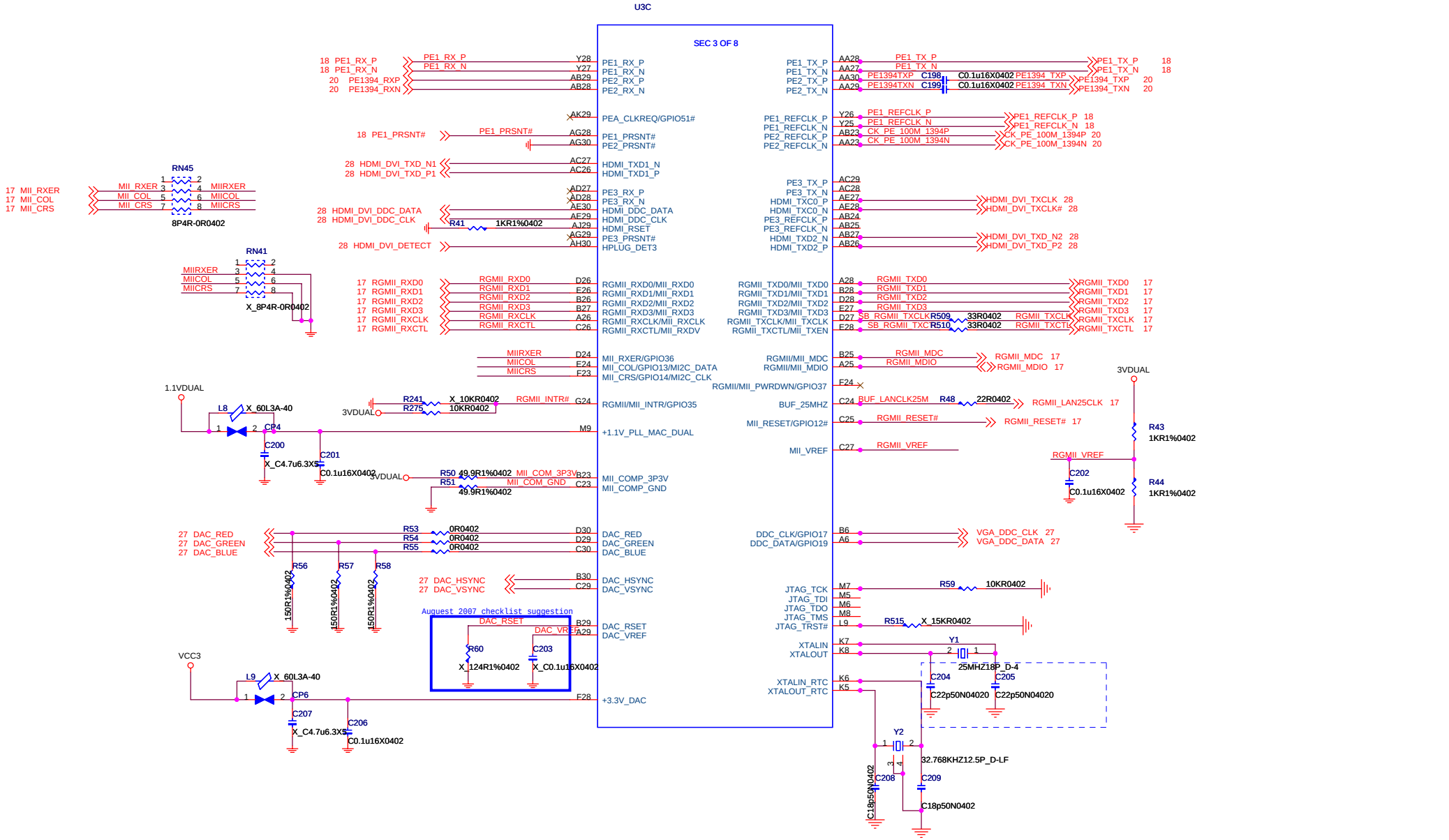

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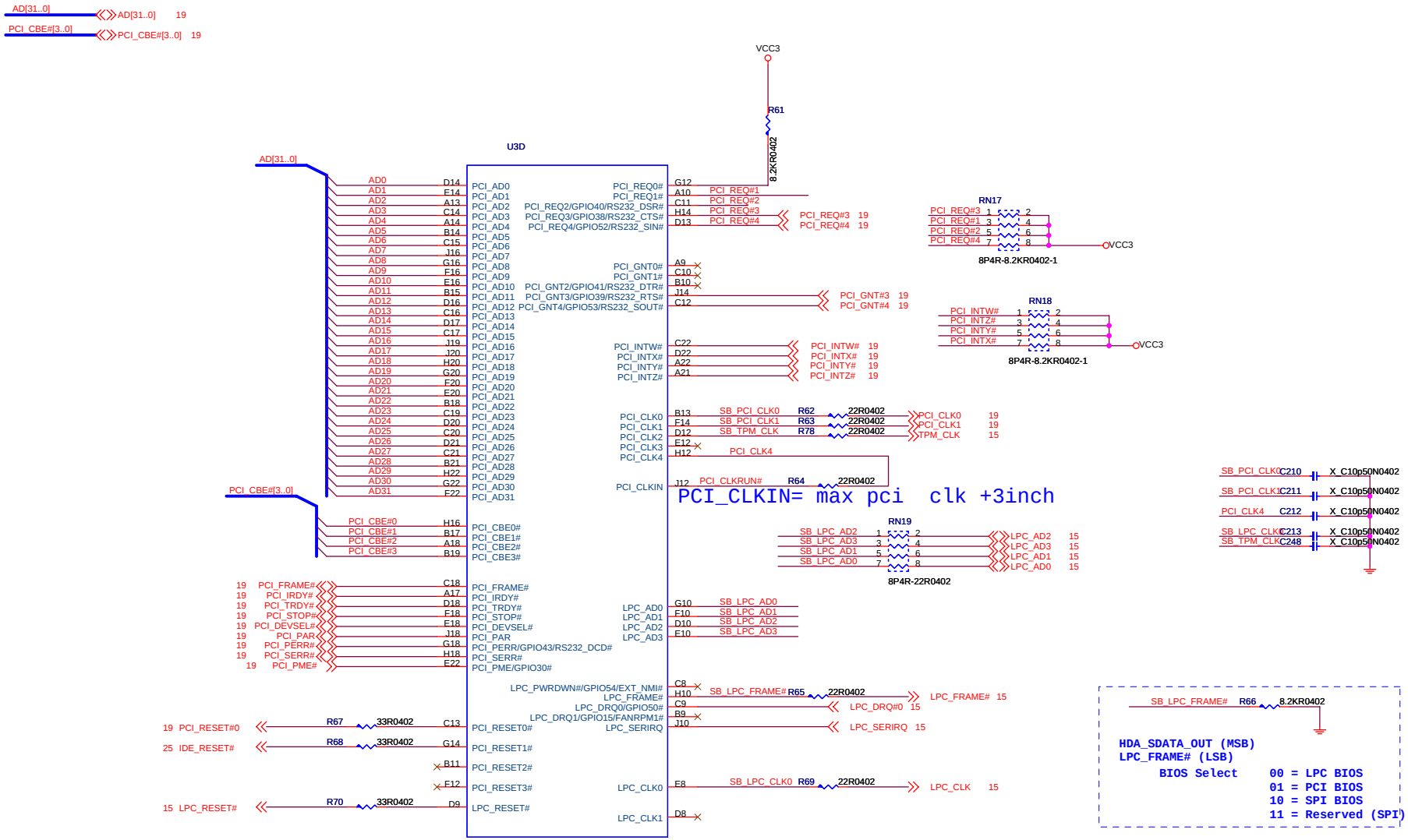
AD[31..0]
AD[31..0] 19
PCI_CBE#[3..0]
PCI_CBE#[3..0] 19
VCC3
R61
8.2KR0402
U3D
PCI_CLKIN= max pci clk +3inch
RN17
8P4R-8.2KR0402-1
RN18
8P4R-8.2KR0402-1
RN19
8P4R-22R0402
HDA_SDATA_OUT (MSB)
LPC_FRAME# (LSB)
BIOS Select 00 = LPC BIOS
01 = PCI BIOS
10 = SPI BIOS
11 = Reserved (SPI)
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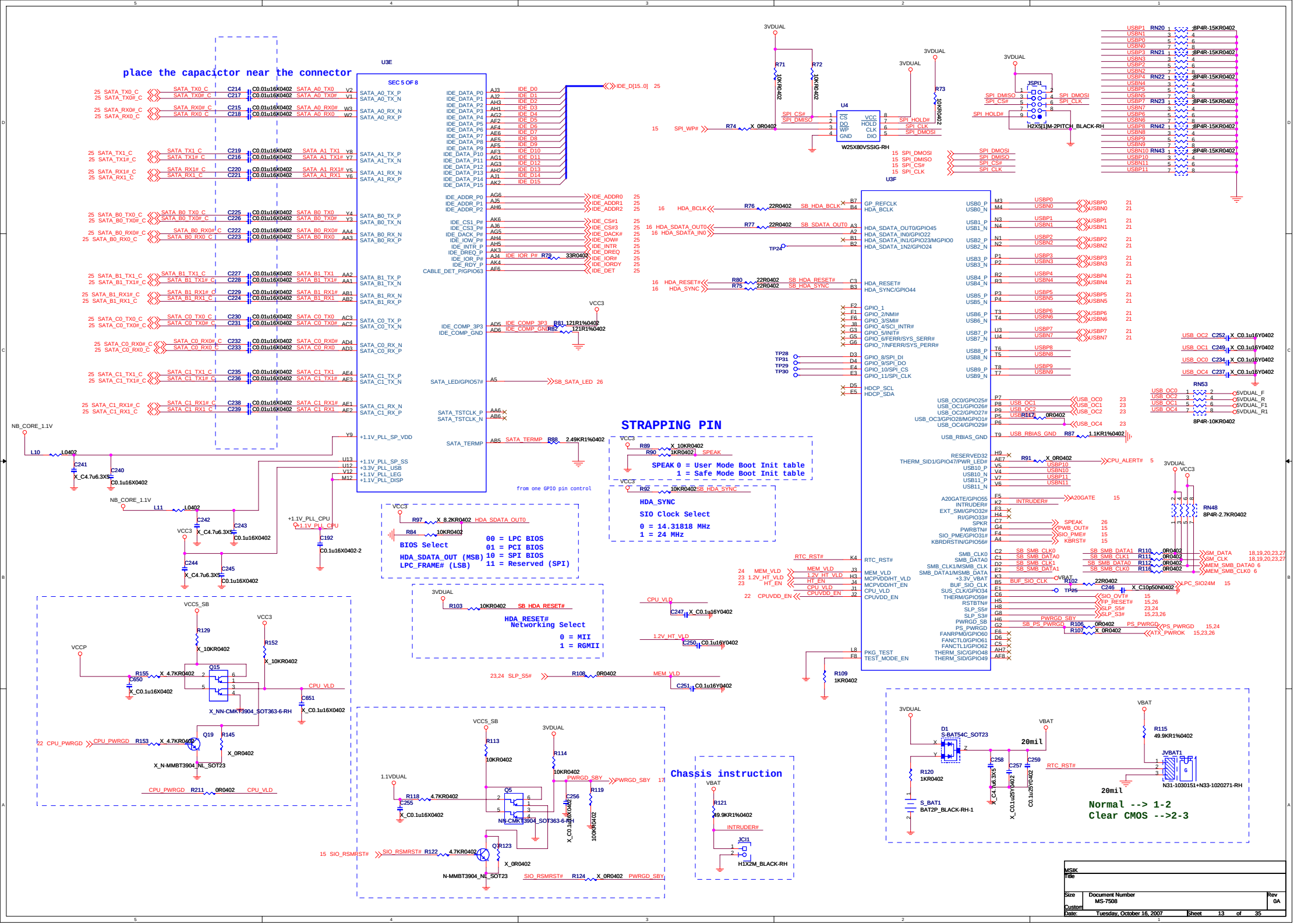
place the capacitor near the connector
U3E
SEC 5 OF 8
STRAPPING PIN
SPEAK 0 = User Mode Boot Init table
1 = Safe Mode Boot Init table
HDA_SYNC
SIO Clock Select
0 = 14.31818 MHz
1 = 24 MHz
BIOS Select
HDA_SDATA_OUT (MSB)
LPC_FRAME# (LSB)
00 = LPC BIOS
01 = PCI BIOS
10 = SPI BIOS
11 = Reserved (SPI)
HDA_RESET# Networking Select
0 = MII
1 = RGMII
from one GPIO pin control
U4
W25X80VSSIG-RH
U3F
JSPI1
H2X5[1]M-2PITCH_BLACK-RH
Chassis instruction
VBAT
JVBAT1
N31-1030151+N33-1020271-RH
20mil
Normal --> 1-2
Clear CMOS -->2-3
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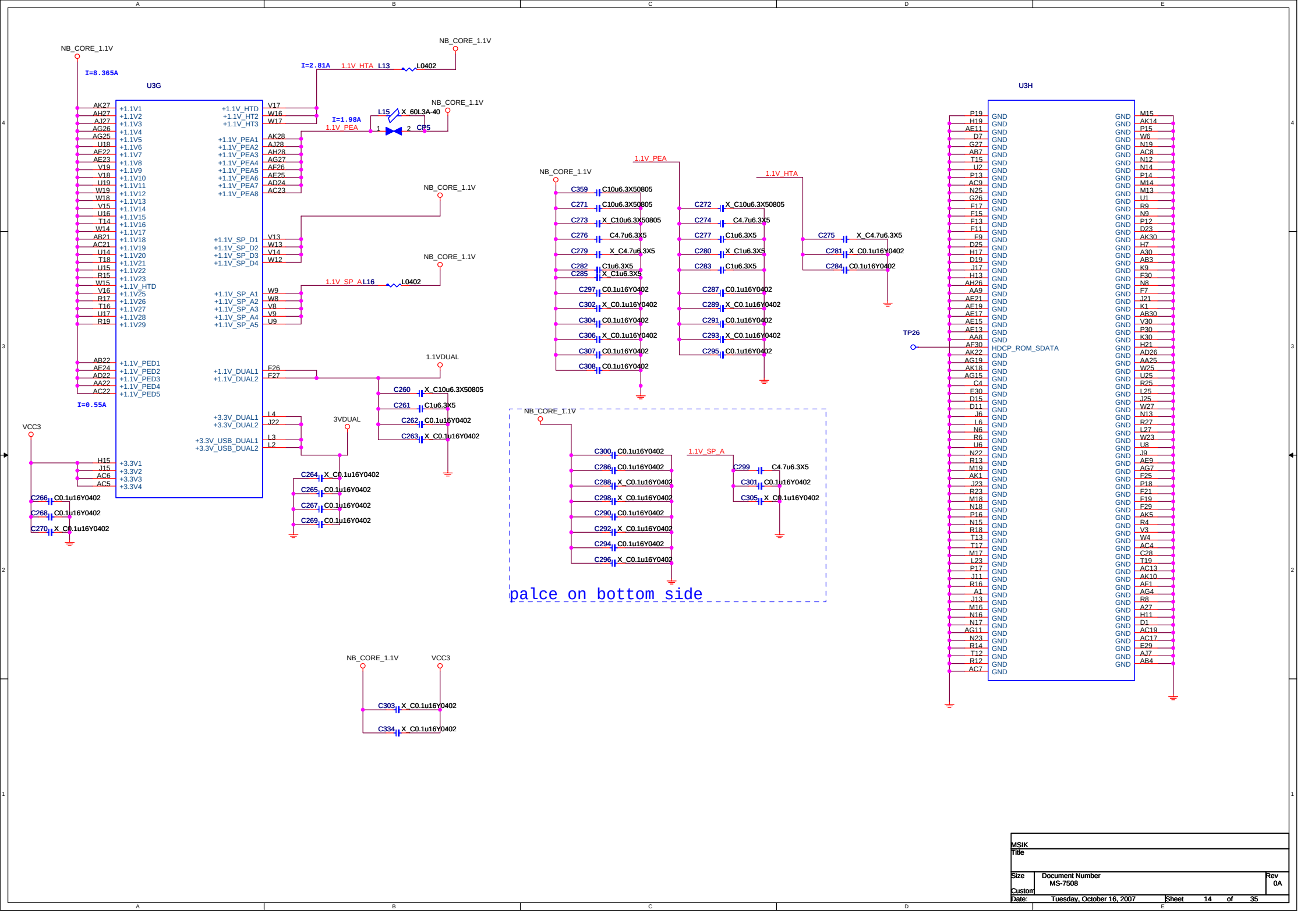
NB_CORE_1.1V
I=8.365A
U3G
I=2.81A
1.1V_HTA
L13
L0402
I=1.98A
1.1V_PEA
L15
X_60L3A-40
CP5
1.1V_SP_A
L16
1.1VDUAL
3VDUAL
VCC3
I=0.55A
U3H
TP26
HDCP_ROM_SDATA
palce on bottom side
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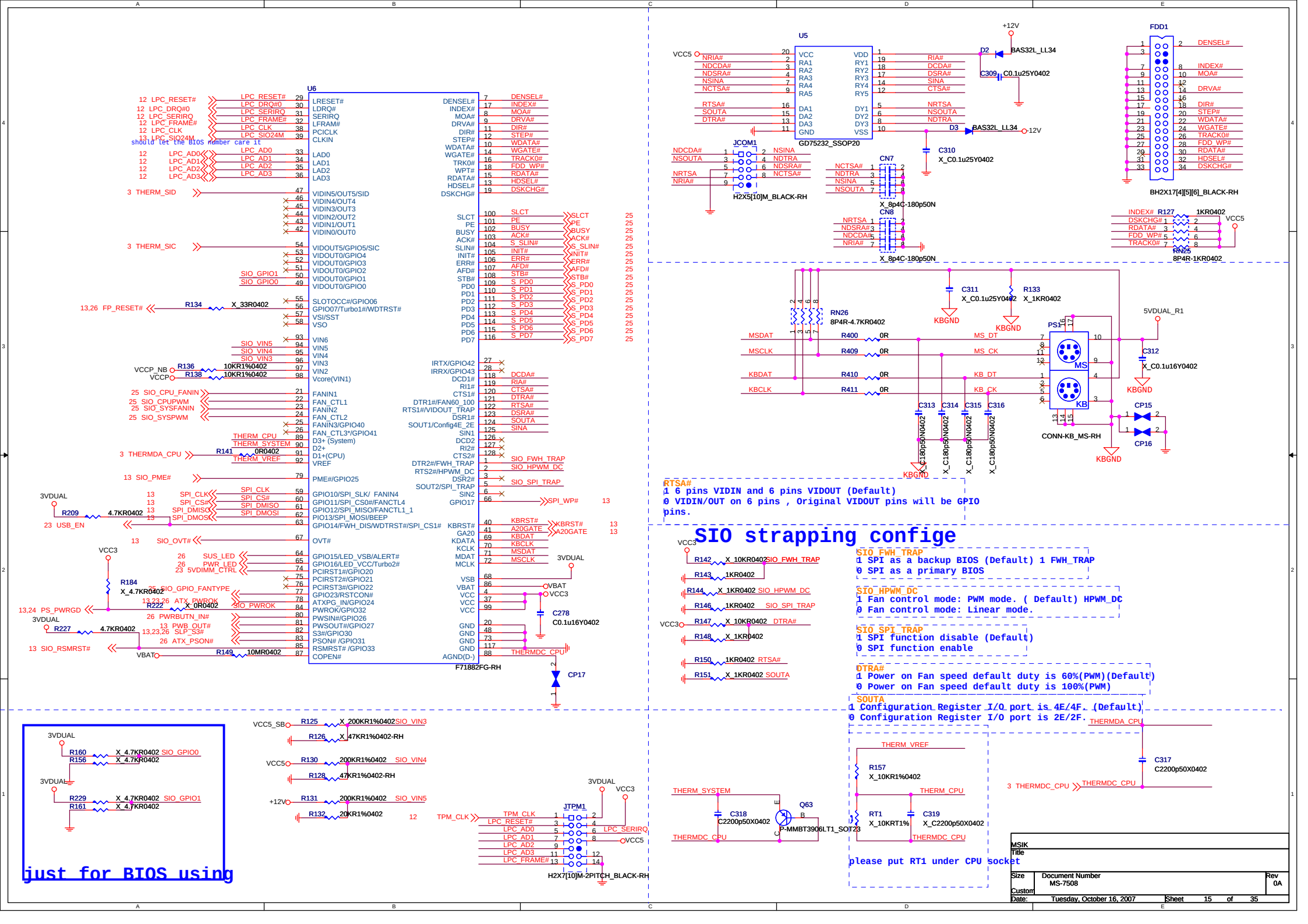
U6
F71882FG-RH
U5
GD75232_SSOP20
FDD1
BH2X17[4][5][6]_BLACK-RH
JCOM1
H2X5[10]M_BLACK-RH
CN7
CN8
X_8p4C-180p50N
RN26
8P4R-4.7KR0402
RN25
8P4R-1KR0402
PS1
MS
KB
CONN-KB_MS-RH
JTPM1
H2X7[10]M-2PITCH_BLACK-RH
Q63
P-MMBT3906LT1_SOT23
RTSA#
1 6 pins VIDIN and 6 pins VIDOUT (Default)
0 VIDIN/OUT on 6 pins , Original VIDOUT pins will be GPIO pins.
SIO strapping confige
SIO_FWH_TRAP
1 SPI as a backup BIOS (Default) 1 FWH_TRAP
0 SPI as a primary BIOS
SIO_HPWM_DC
1 Fan control mode: PWM mode. (Default) HPWM_DC
0 Fan control mode: Linear mode.
SIO_SPI_TRAP
1 SPI function disable (Default)
0 SPI function enable
DTRA#
1 Power on Fan speed default duty is 60%(PWM)(Default)
0 Power on Fan speed default duty is 100%(PWM)
SOUTA
1 Configuration Register I/O port is 4E/4F. (Default)
0 Configuration Register I/O port is 2E/2F.
please put RT1 under CPU socket
just for BIOS using
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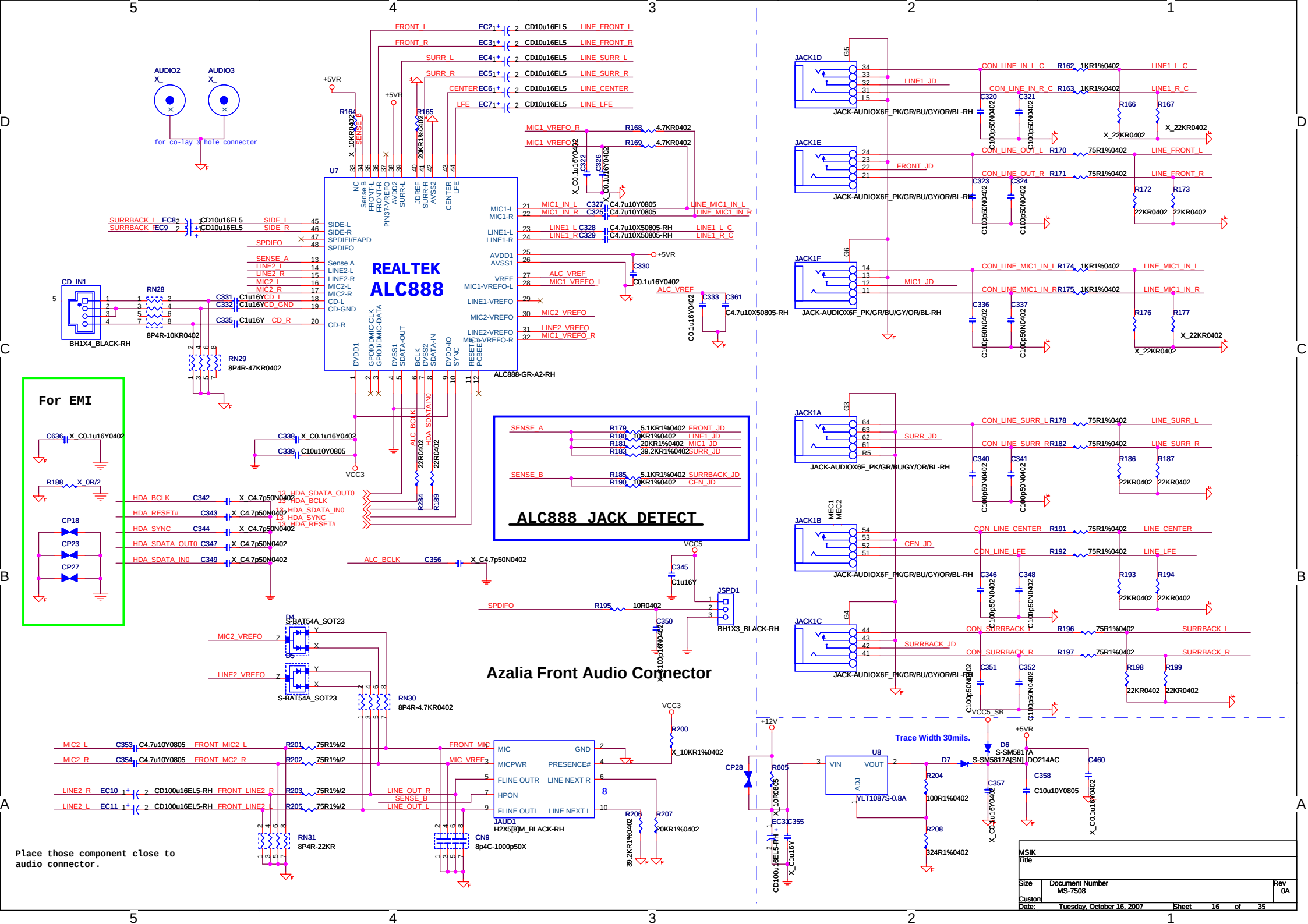
REALTEK
ALC888
ALC888-GR-A2-RH
ALC888 JACK DETECT
Azalia Front Audio Connector
For EMI
Place those component close to audio connector.
Trace Width 30mils.
AUDIO2
AUDIO3
for co-lay 3 hole connector
JACK1D
JACK1E
JACK1F
JACK1A
JACK1B
JACK1C
JACK-AUDIOX6F_PK/GR/BU/GY/OR/BL-RH
BH1X4_BLACK-RH
BH1X3_BLACK-RH
JAUD1
H2X5[8]M_BLACK-RH
CN9
8p4C-1000p50X
U8
YLT1087S-0.8A
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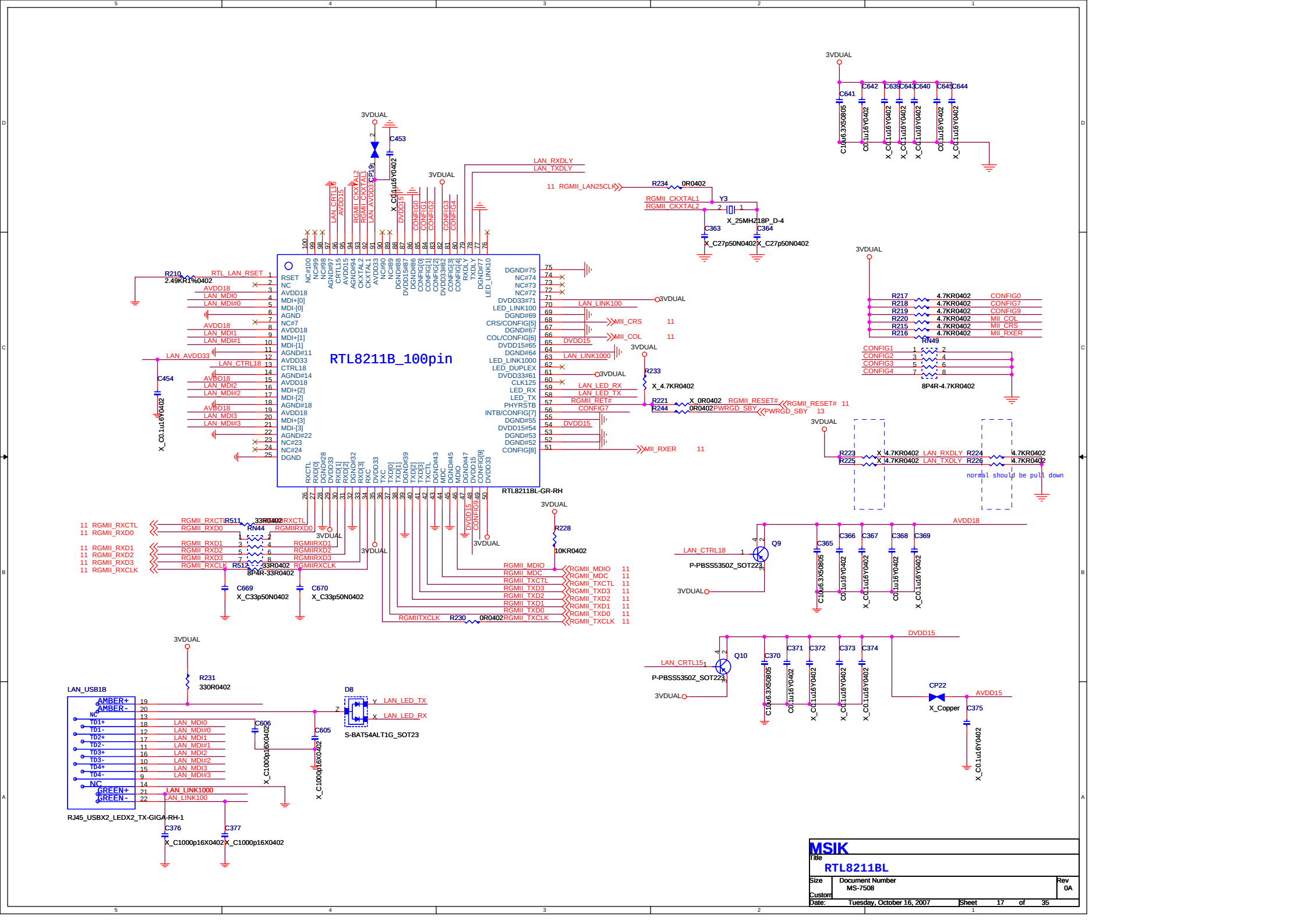
RTL8211B_100pin
RTL8211BL-GR-RH
RJ45_USBX2_LEDX2_TX-GIGA-RH-1
S-BAT54ALT1G_SOT23
P-PBSS5350Z_SOT223
X_25MHZ18P_D-4
8P4R-4.7KR0402
8P4R-33R0402
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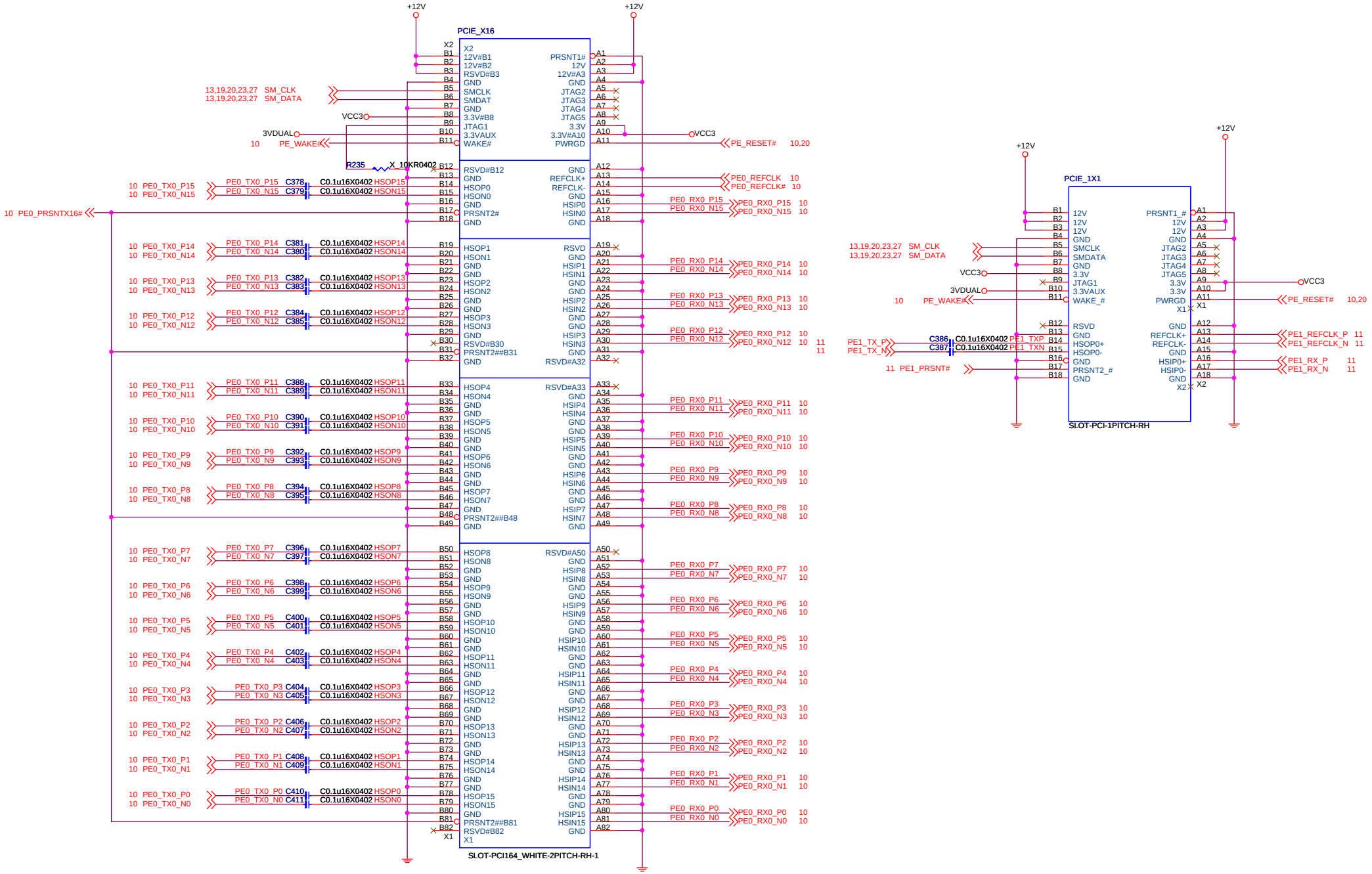
normal should be pull down



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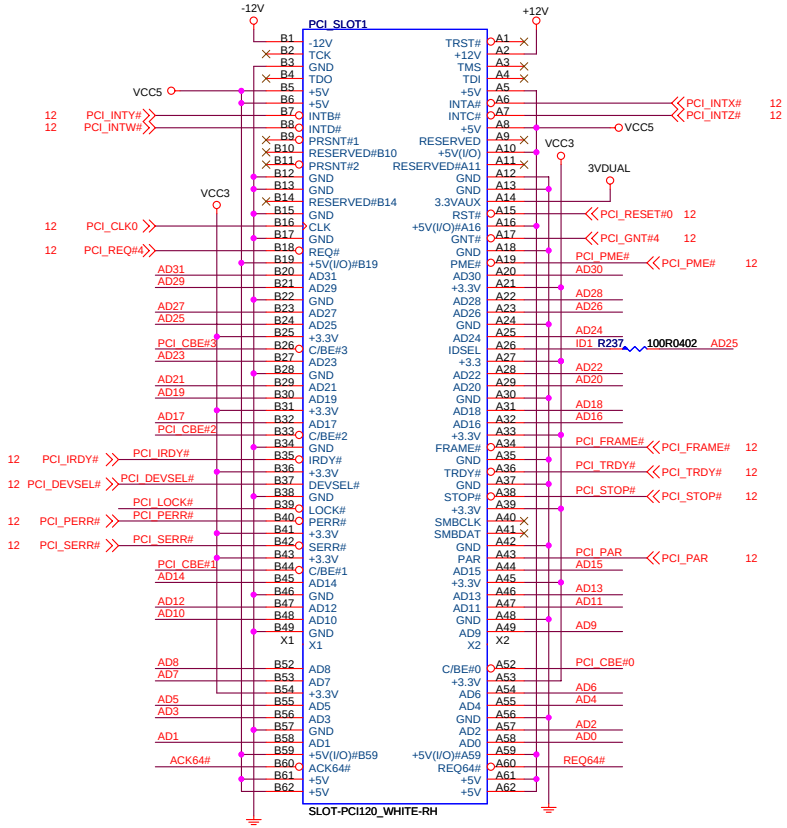
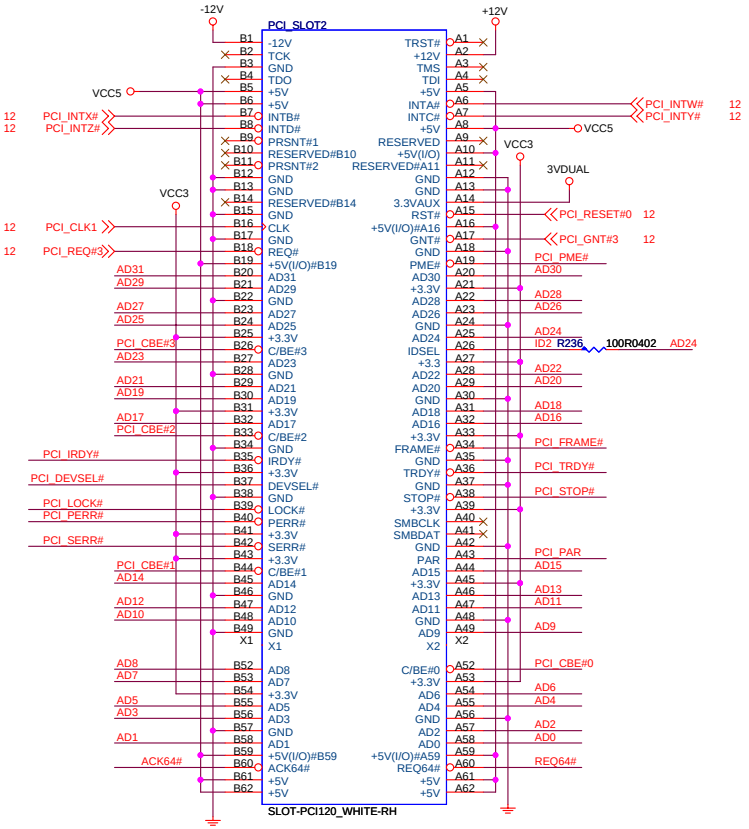
PCI SLOT 1 (PCI VER: 2.3 COMPLY)



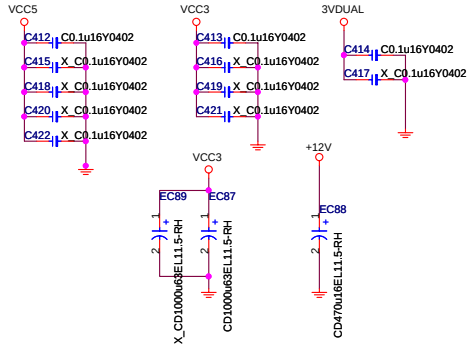
IDSEL = AD25
MASTER = PCI_REQ#4
PCI_GNT#4

PCI SLOT 2 (PCI VER: 2.3 COMPLY)

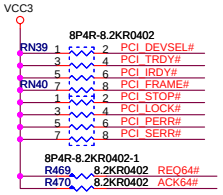


IDSEL = AD24
MASTER = PCI_REQ#3
PCI_GNT#3

PCI SLOT DECOUPLING CAPACITORS



PCI PULL-UP / DOWN RESISTORS



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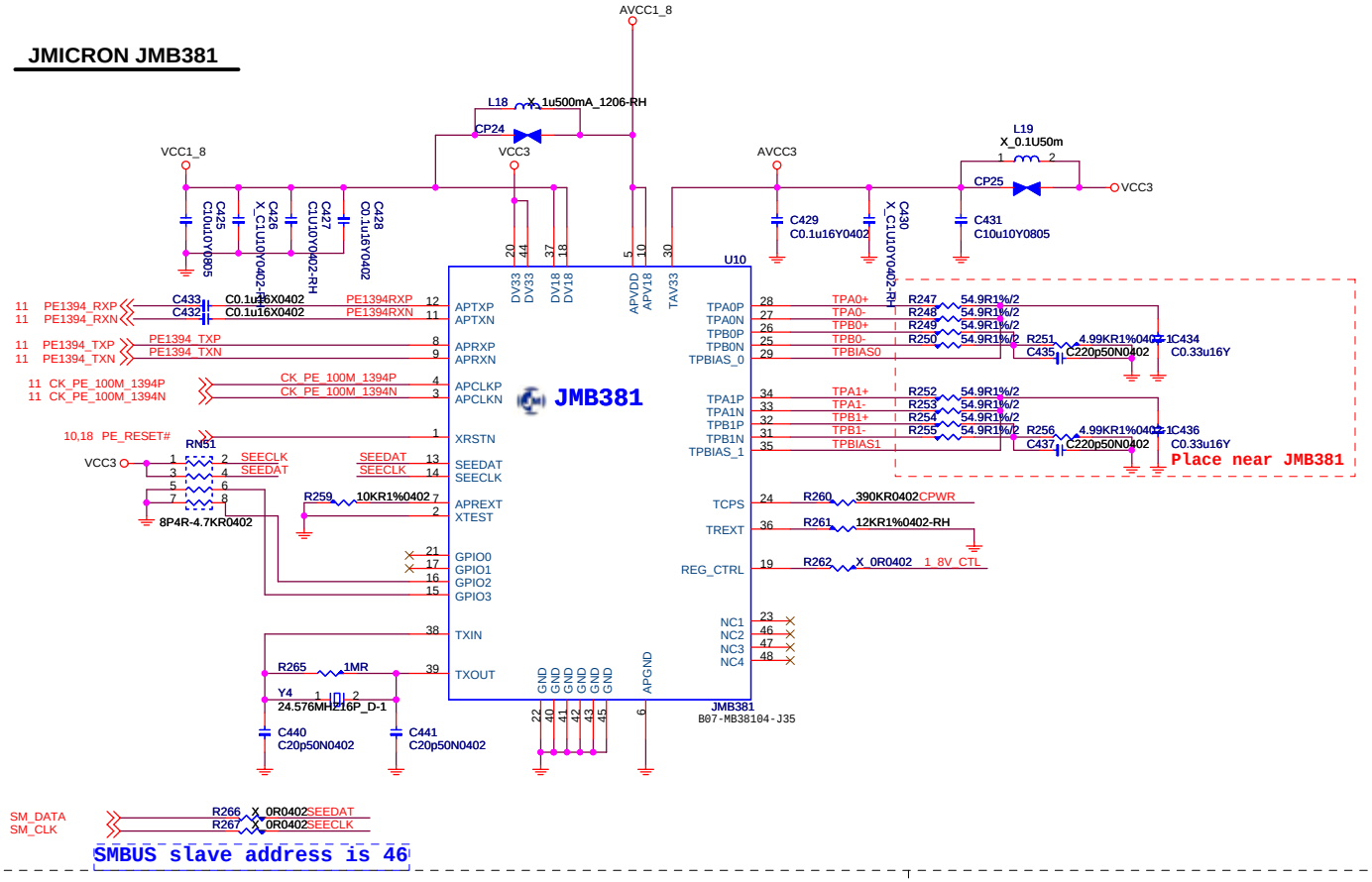
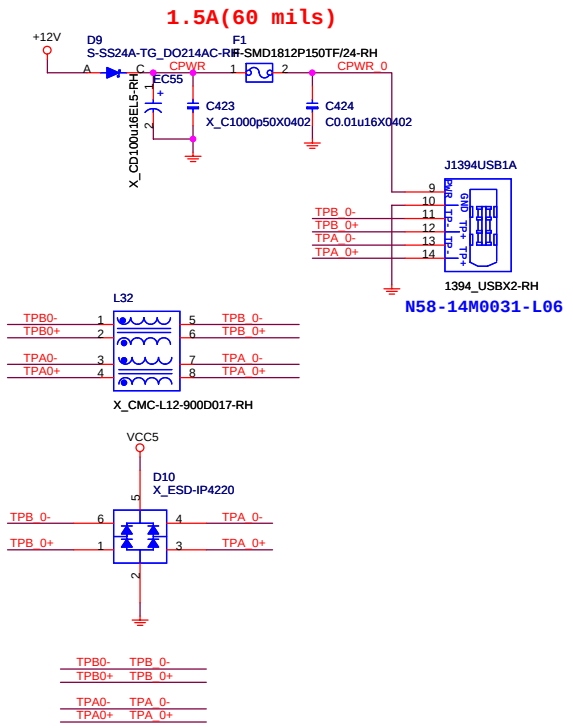
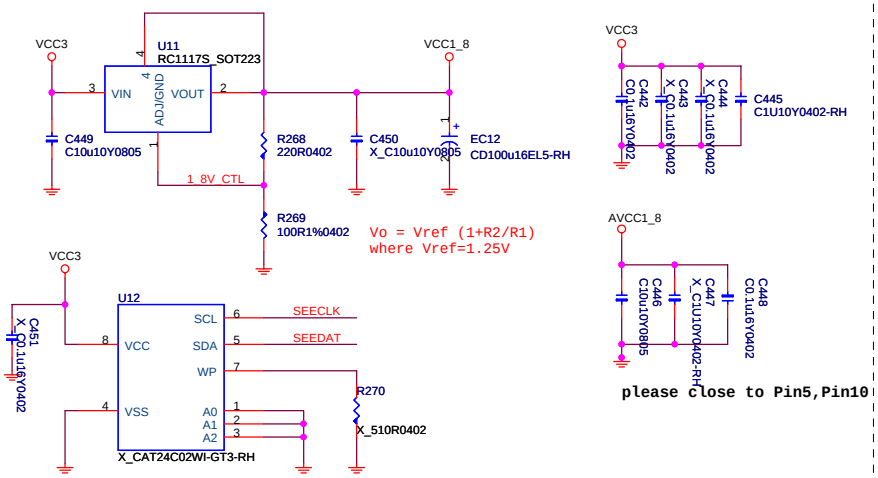
JMICRON JMB381

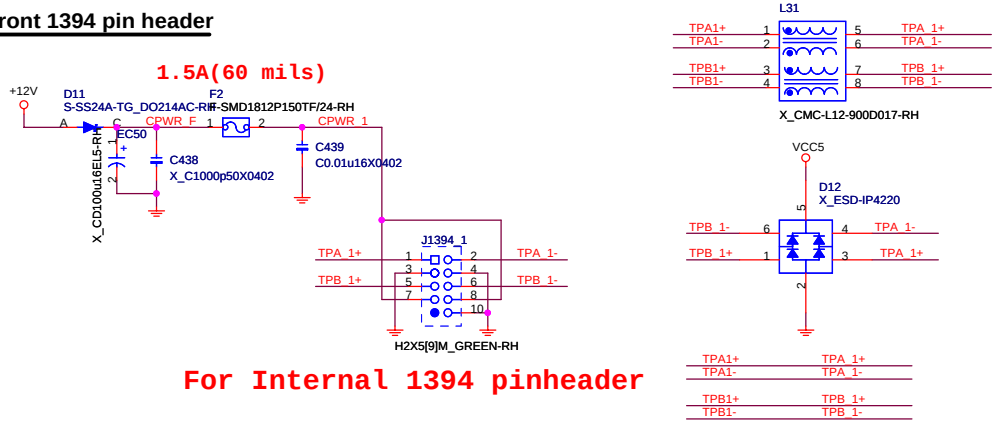


Rear 1394 port





Front 1394 pin header



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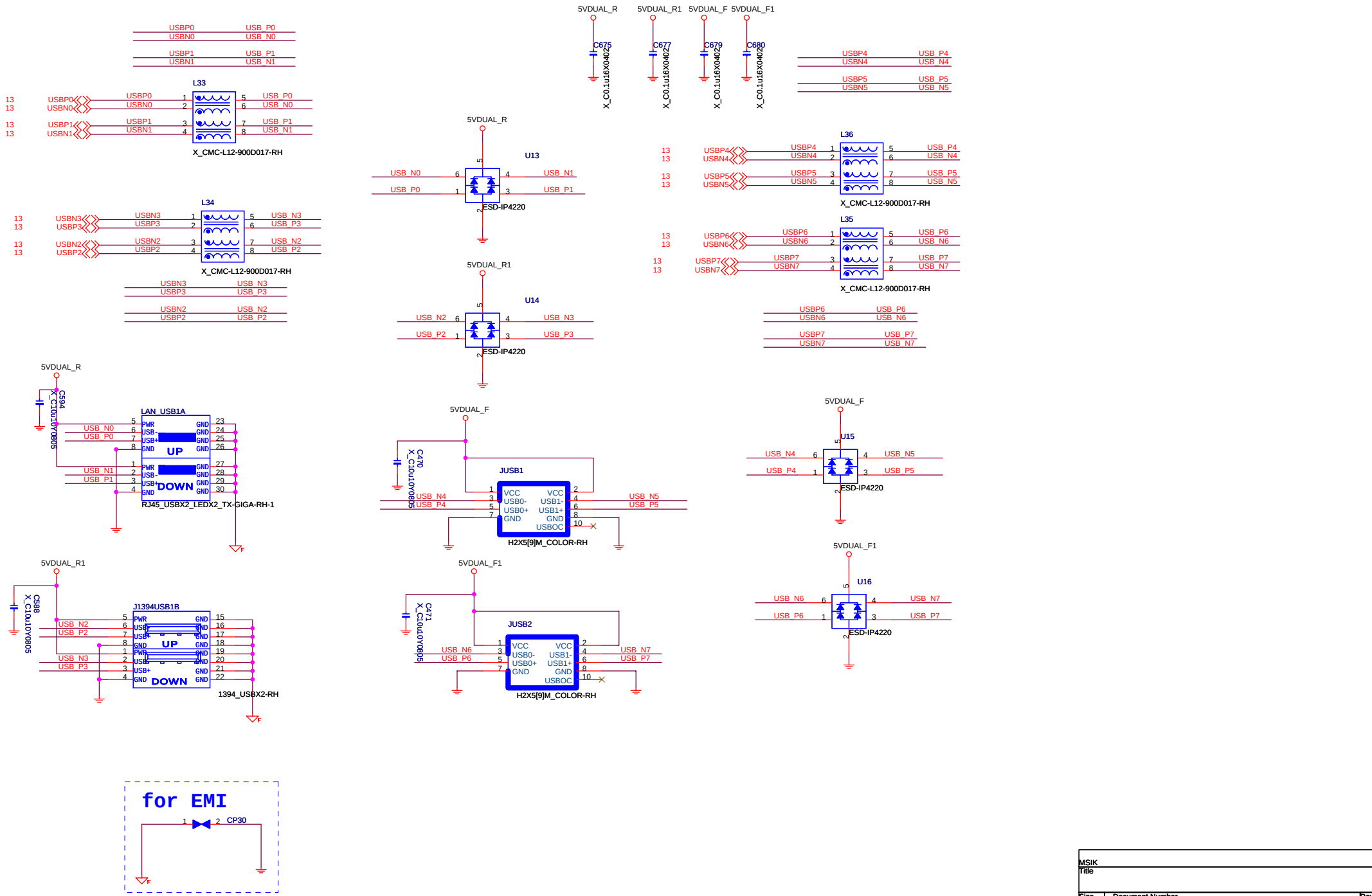
USBP0
USBN0
USB_P0
USB_N0
USBP1
USBN1
USB_P1
USB_N1
L33
X_CMC-L12-900D017-RH
USBN3
USBP3
USBN2
USBP2
USB_N3
USB_P3
USB_N2
USB_P2
L34
X_CMC-L12-900D017-RH
5VDUAL_R
5VDUAL_R1
5VDUAL_F
5VDUAL_F1
C675
C677
C679
C680
X_C0.1u16X0402
USBP4
USBN4
USBP5
USBN5
USB_P4
USB_N4
USB_P5
USB_N5
U13
ESD-IP4220
L36
X_CMC-L12-900D017-RH
U14
USBP6
USBN6
USBP7
USBN7
USB_P6
USB_N6
USB_P7
USB_N7
L35
X_CMC-L12-900D017-RH
C594
X_C10u10Y0805
LAN_USB1A
UP
DOWN
RJ45_USBX2_LEDX2_TX-GIGA-RH-1
C470
JUSB1
H2X5[9]M_COLOR-RH
U15
C588
J1394USB1B
1394_USBX2-RH
C471
JUSB2
U16
for EMI
CP30
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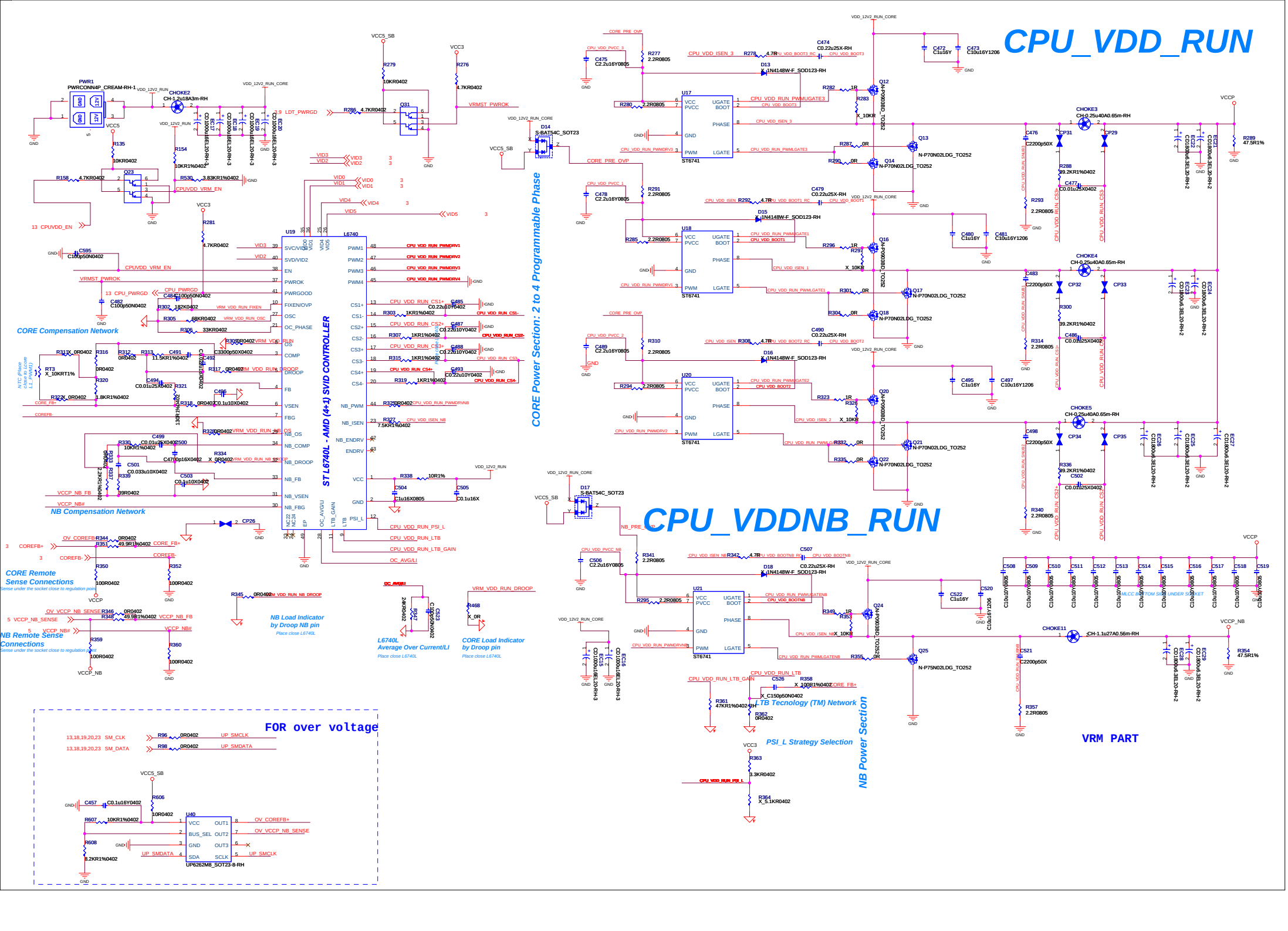
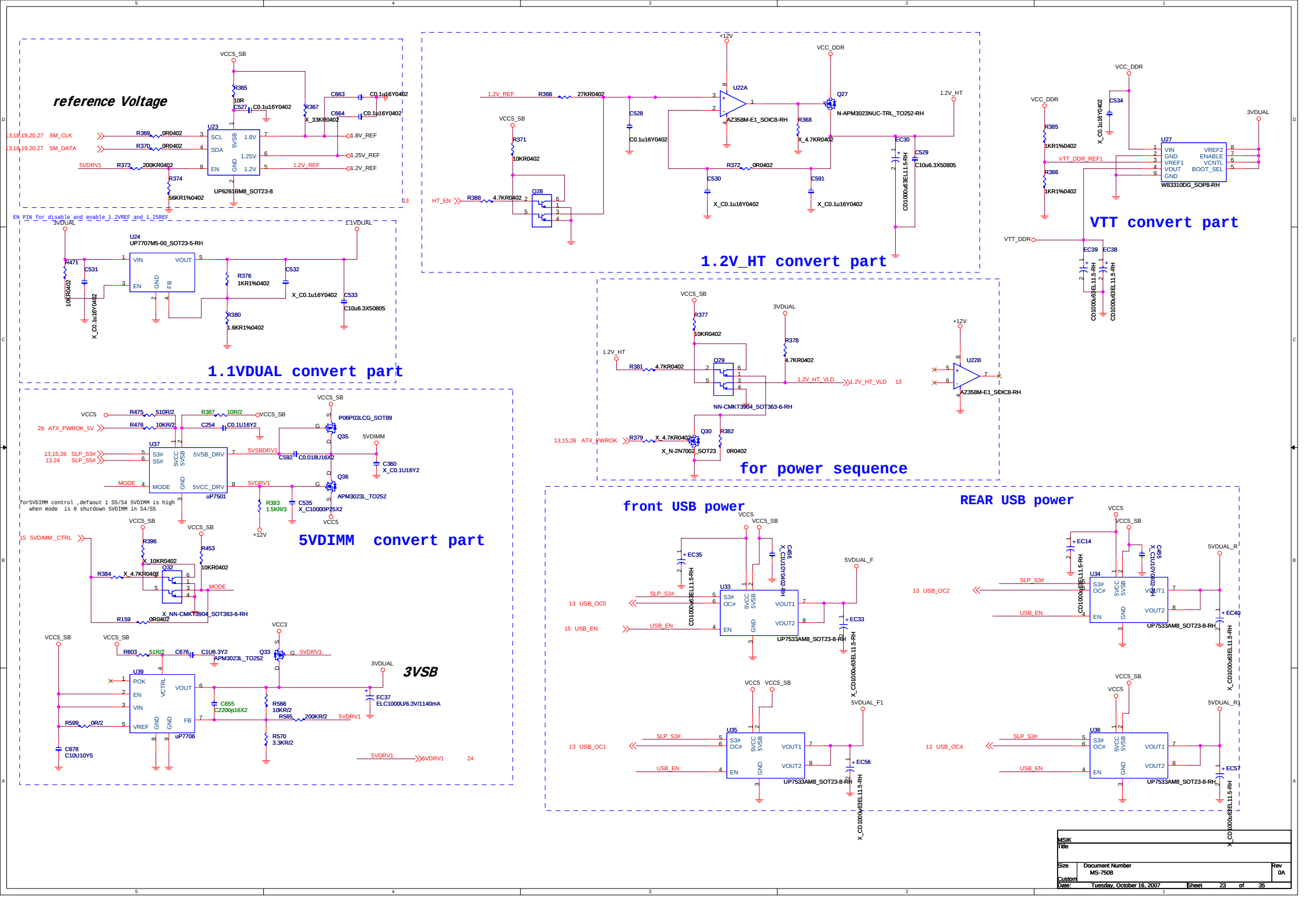

CPU_VDD_RUN
CPU_VDDNB_RUN
ST L6740L - AMD (4+1) SVID CONTROLLER
CORE Power Section: 2 to 4 Programmable Phase
NB Power Section
VRM PART
CORE Compensation Network
NB Compensation Network
CORE Remote Sense Connections
NB Remote Sense Connections
NB Load Indicator by Droop NB pin
L6740L Average Over Current/LI
CORE Load Indicator by Droop pin
LTB Tecnology (TM) Network
PSI_L Strategy Selection
FOR over voltage
UP6262M8_SOT23-8-RH


reference Voltage
VCC5_SB
U23
UP6261BM8_SOT23-8
SM_CLK
SM_DATA
5VDRV1
1.8V_REF
1.25V_REF
1.2V_REF
EN PIN for disable and enable 1.2VREF and 1.25REF
1.1VDUAL convert part
U24
UP7707M5-00_SOT23-5-RH
3VDUAL
1.1VDUAL
1.2V_HT convert part
+12V
VCC_DDR
U22A
AZ358M-E1_SOIC8-RH
Q27
N-APM3023NUC-TRL_TO252-RH
1.2V_HT
Q28
HT_EN
VTT convert part
U27
W83310DG_SOP8-RH
VTT_DDR
VTT_DDR_REF1
U22B
Q29
NN-CMKT3904_SOT363-6-RH
1.2V_HT_VLD
for power sequence
5VDIMM convert part
U37
uP7501
P06P03LCG_SOT89
Q35
Q36
APM3023L_TO252
5VDIMM
5VDIMM _CTRL
Q32
NN-CMKT3904_SOT363-6-RH
3VSB
U39
uP7706
APM3023L_TO252
Q33
front USB power
U33
UP7533AM8_SOT23-8-RH
5VDUAL_F
U35
5VDUAL_F1
REAR USB power
U34
5VDUAL_R
U36
5VDUAL_R1
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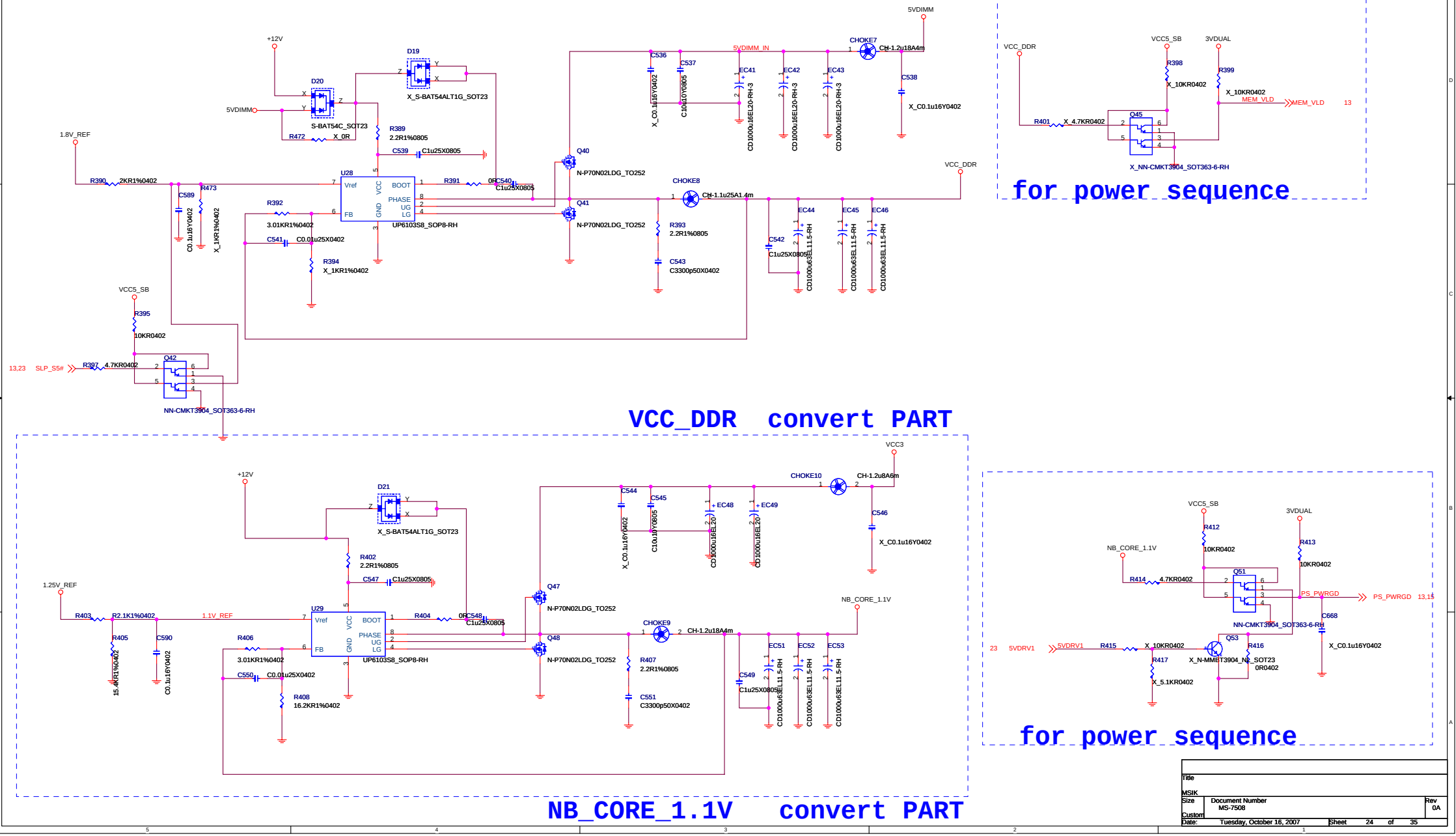
5VDIMM
+12V
D19
D20
X_S-BAT54ALT1G_SOT23
S-BAT54C_SOT23
5VDIMM
R472
X_0R
R389
2.2R1%0805
C539
C1u25X0805
1.8V_REF
R390
2KR1%0402
U28
Vref
VCC
BOOT
PHASE
UG
LG
GND
FB
UP6103S8_SOP8-RH
R391
0RC540
C1u25X0805
Q40
N-P70N02LDG_TO252
Q41
N-P70N02LDG_TO252
5VDIMM_IN
C536
X_C0.1u16Y0402
C537
C10u10Y0805
EC41
EC42
EC43
CD1000u16EL20-RH-3
CHOKE7
CH-1.2u18A4m
C538
X_C0.1u16Y0402
VCC_DDR
CHOKE8
CH-1.1u25A1.4m
EC44
EC45
EC46
CD1000u63EL11.5-RH
C542
C1u25X0805
R393
2.2R1%0805
C543
C3300p50X0402
C589
C0.1u16Y0402
R473
X_1KR1%0402
R392
3.01KR1%0402
C541
C0.01u25X0402
R394
X_1KR1%0402
VCC5_SB
R395
10KR0402
13,23
SLP_S5#
R397
4.7KR0402
Q42
NN-CMKT3904_SOT363-6-RH
VCC_DDR
VCC5_SB
3VDUAL
R398
X_10KR0402
R399
X_10KR0402
MEM_VLD
MEM_VLD
13
R401
X_4.7KR0402
Q45
X_NN-CMKT3904_SOT363-6-RH
for power sequence
VCC_DDR convert PART
VCC3
+12V
D21
X_S-BAT54ALT1G_SOT23
R402
2.2R1%0805
C547
C1u25X0805
1.25V_REF
R403
R2.1K1%0402
1.1V_REF
U29
Vref
VCC
BOOT
PHASE
UG
LG
GND
FB
UP6103S8_SOP8-RH
R404
0RC548
C1u25X0805
Q47
N-P70N02LDG_TO252
Q48
N-P70N02LDG_TO252
C544
X_C0.1u16Y0402
C545
C10u10Y0805
EC48
EC49
CD1000u16EL20
CHOKE10
CH-1.2u8A6m
C546
X_C0.1u16Y0402
NB_CORE_1.1V
CHOKE9
CH-1.2u18A4m
EC51
EC52
EC53
CD1000u63EL11.5-RH
C549
C1u25X0805
R407
2.2R1%0805
C551
C3300p50X0402
R405
15.4KR1%0402
C590
C0.1u16Y0402
R406
3.01KR1%0402
C550
C0.01u25X0402
R408
16.2KR1%0402
NB_CORE_1.1V
3VDUAL
R412
10KR0402
R413
10KR0402
R414
4.7KR0402
Q51
PS_PWRGD
PS_PWRGD
13,15
NN-CMKT3904_SOT363-6-RH
C668
23
5VDRV1
5VDRV1
R415
X_10KR0402
Q53
X_N-MMBT3904_N2_SOT23
R416
0R0402
R417
X_5.1KR0402
X_C0.1u16Y0402
for power sequence
NB_CORE_1.1V convert PART
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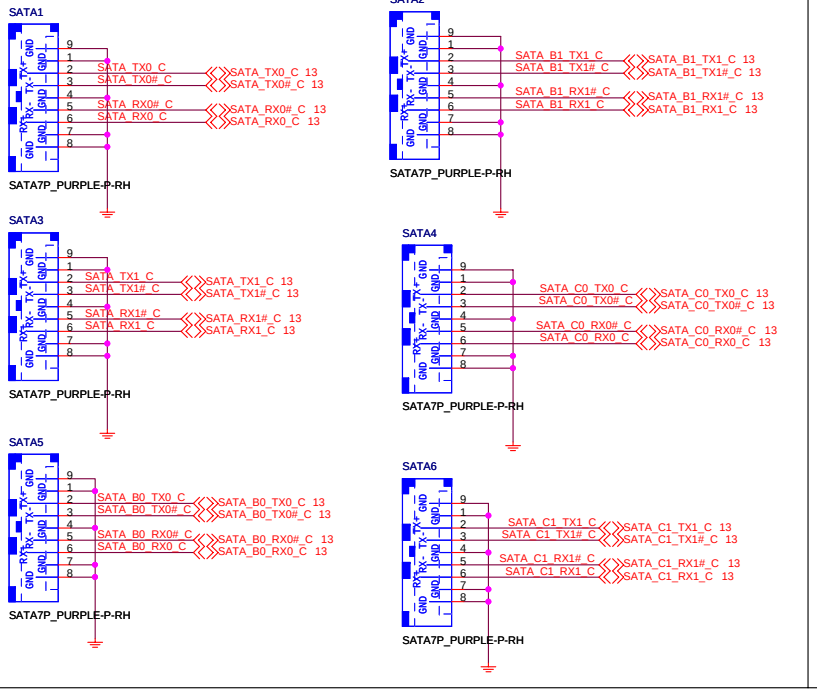

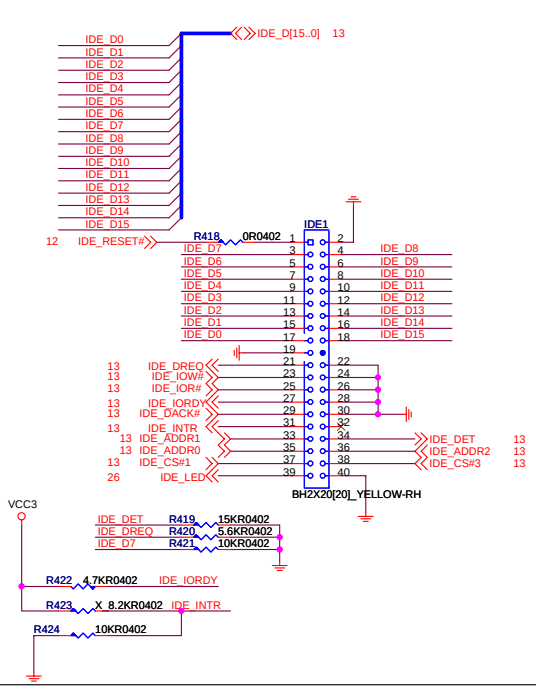

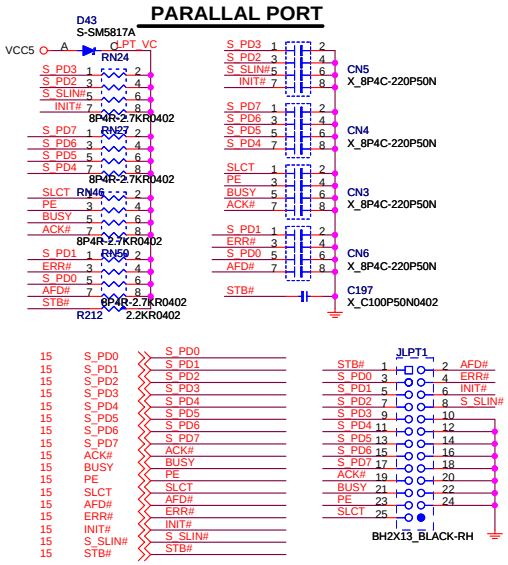

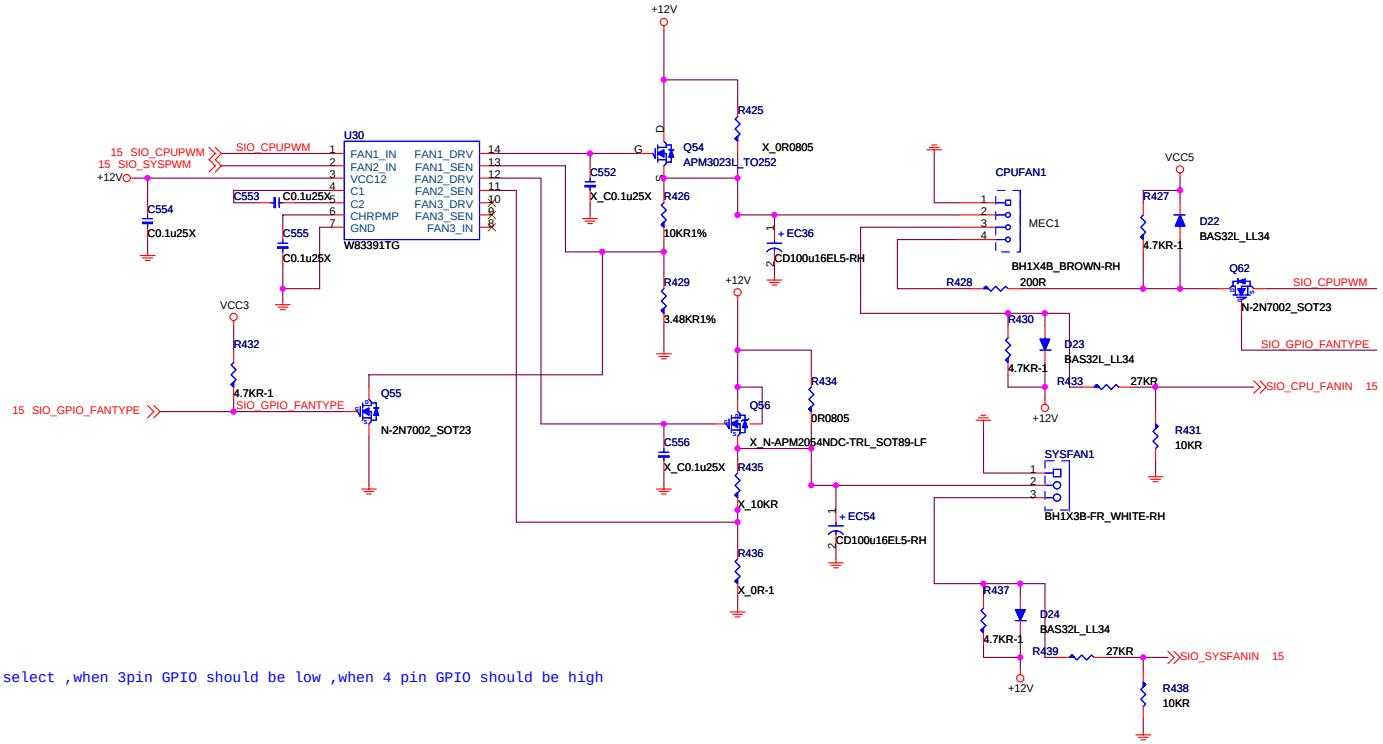

for CPU FAN type select ,when 3pin GPIO should be low ,when 4 pin GPIO should be high

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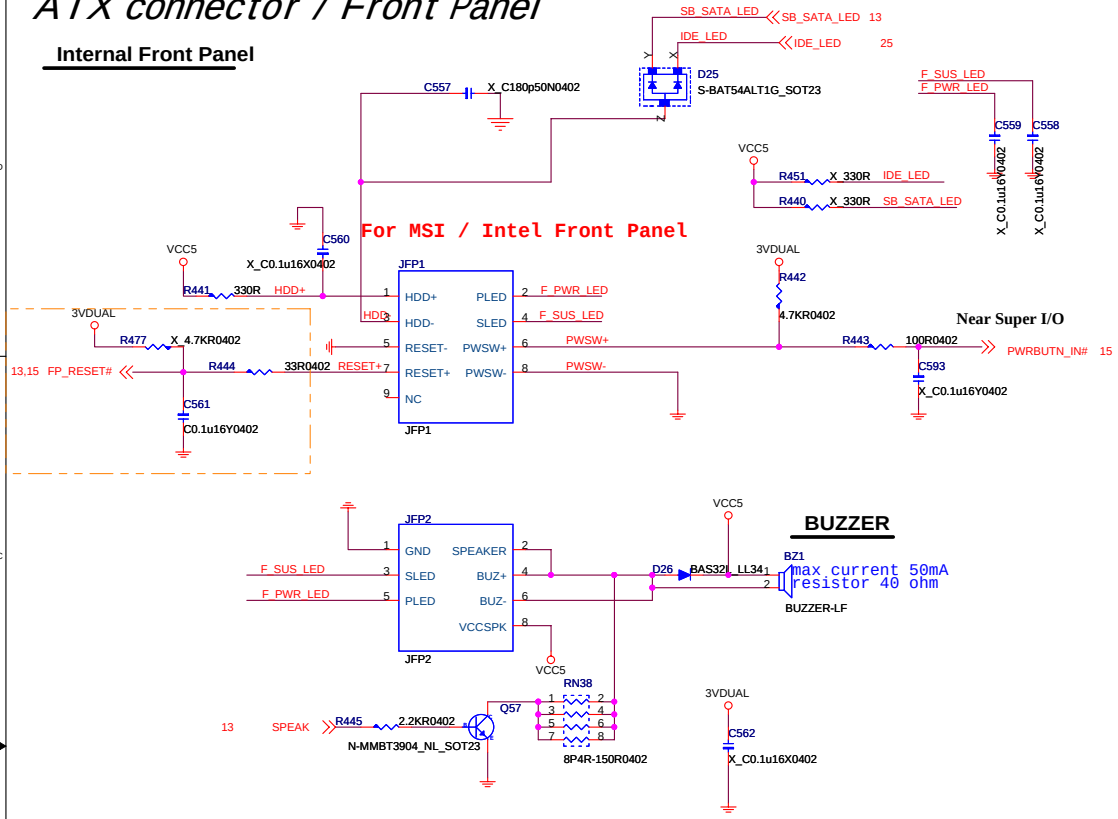
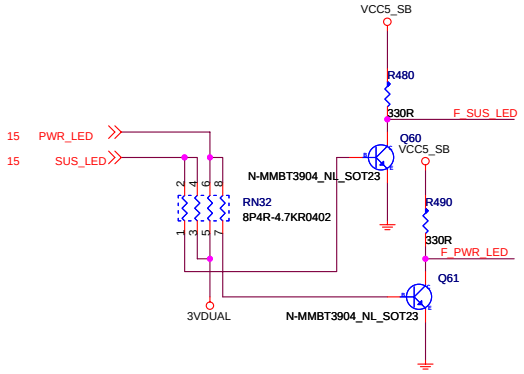
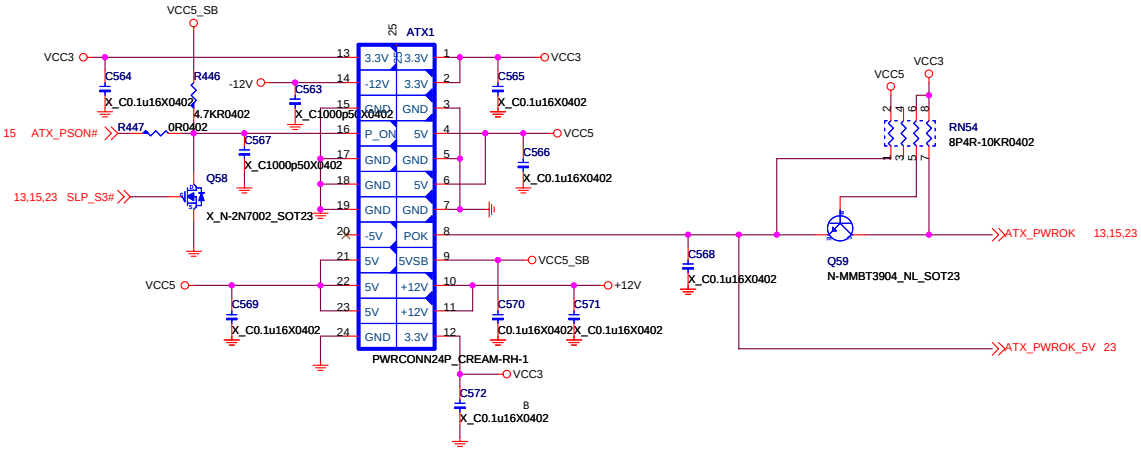
ATX connector / Front Panel

Internal Front Panel

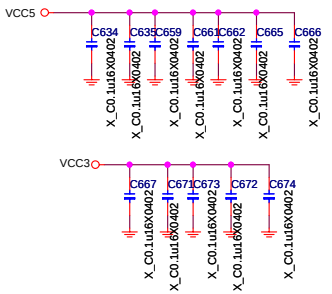




ATX Connector



EMI solution



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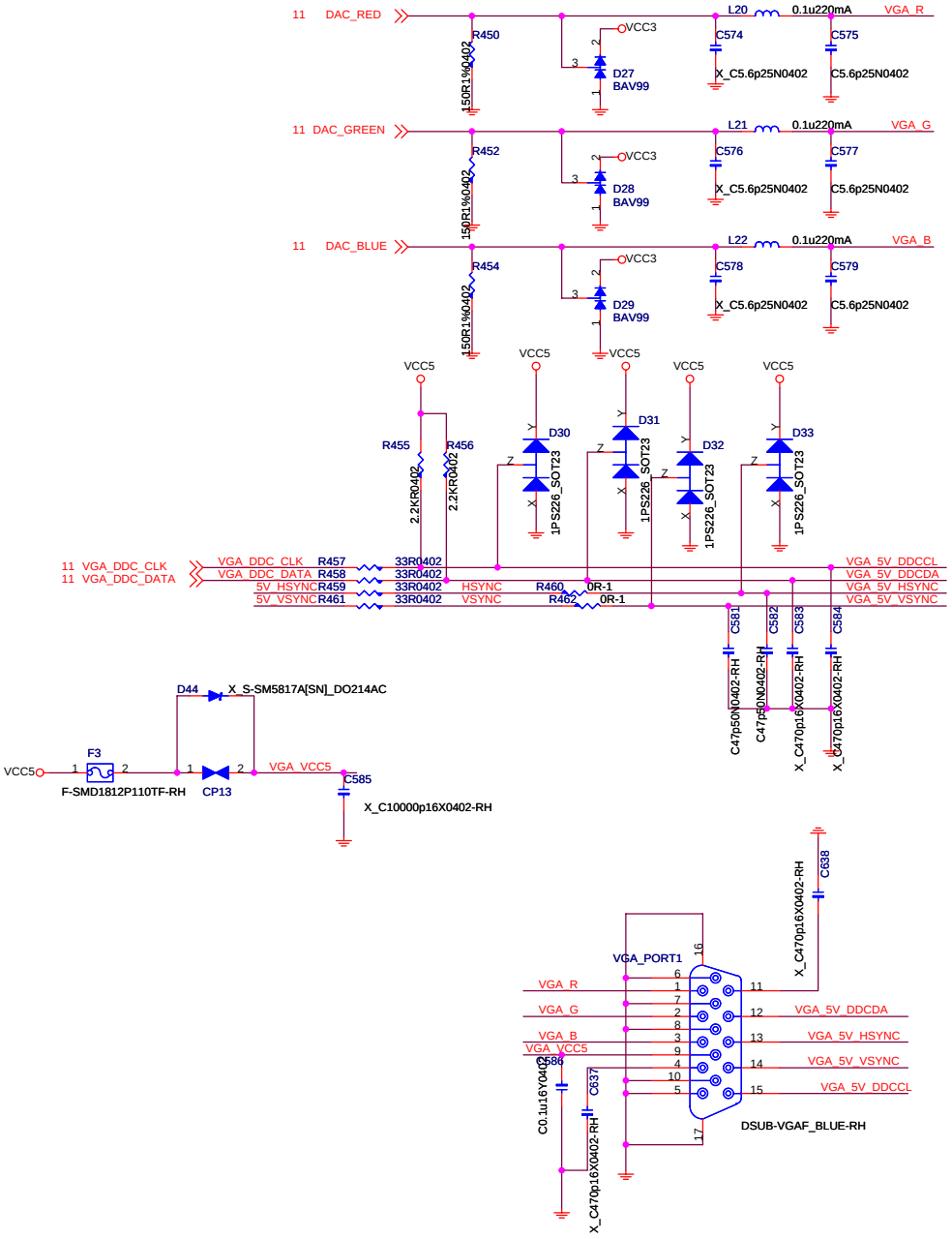
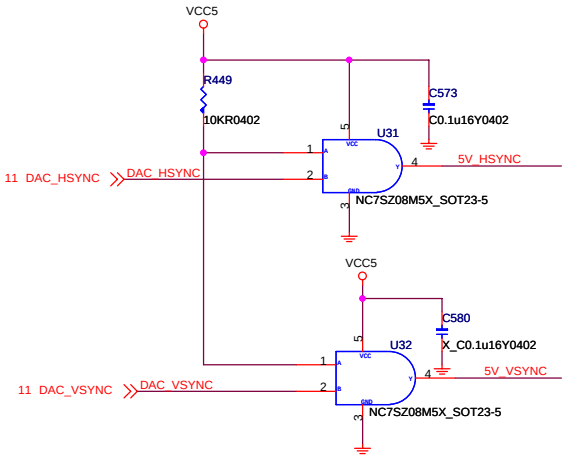
VGA CONNECTOR

Closed NB

close VGA connector For EMI





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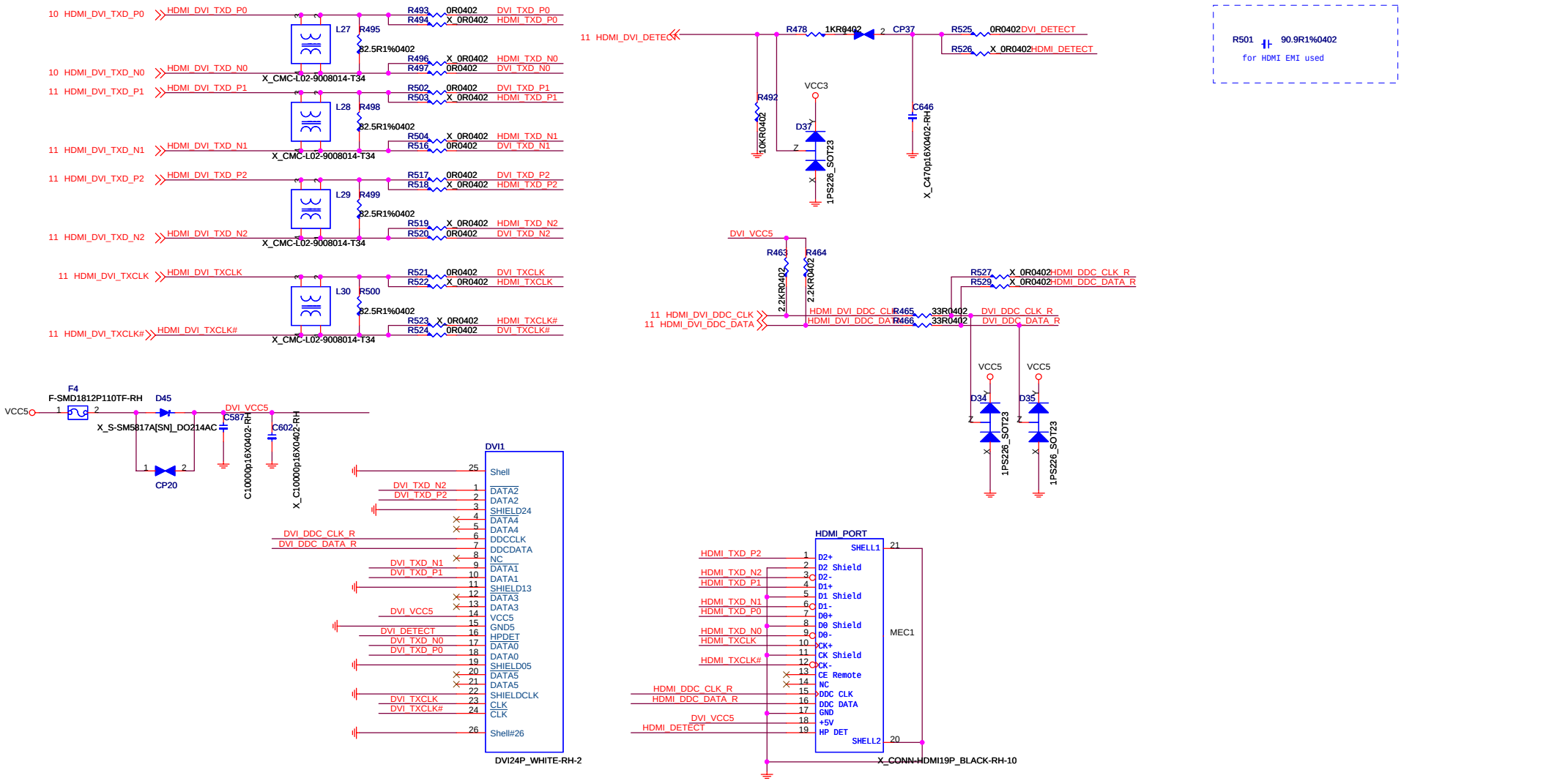
for EMI place near DVI connector



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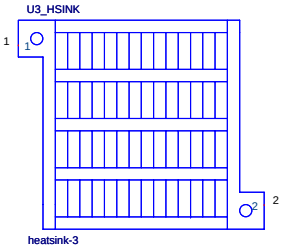
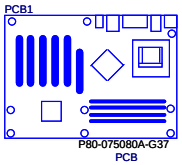
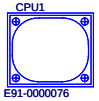
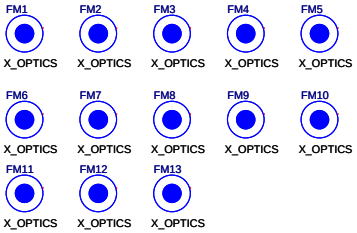


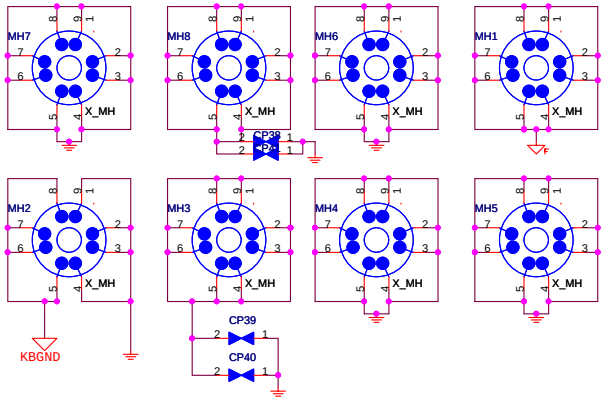




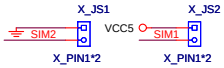
Optics Orientation Holes



Mounting Holes



Simulation



Model option table

Model type	Function	BOM Config	ERP BOM No.
MS-7508	MCP78+RTL8211BL+ALC888+2PCI+1PCIEX16+1PCIEX1 +2PS2+8USB+2COM+HDMI/DVI/VGA+1Audio+RJ45	Cfg-7508VOA	

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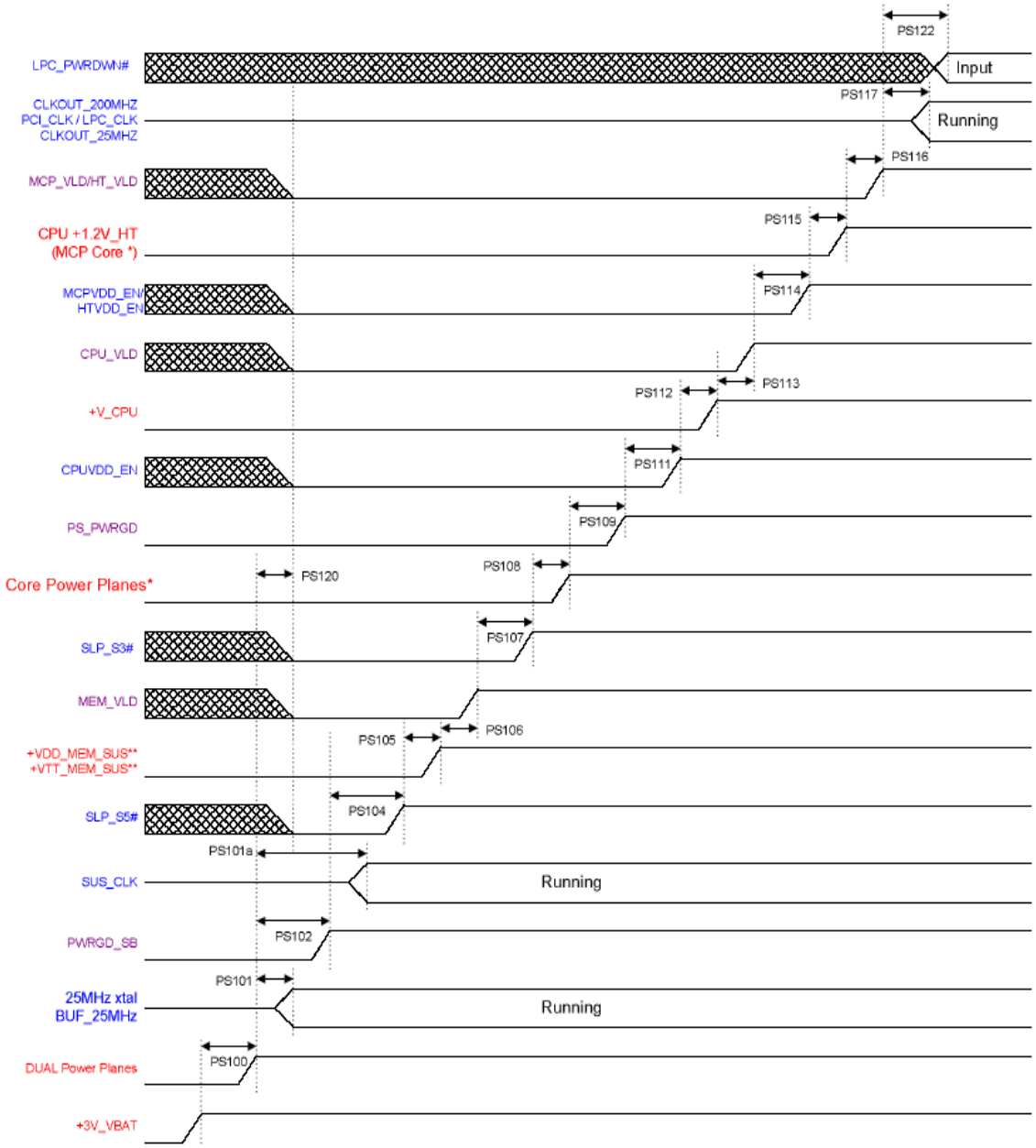

Power Planes are in Red **MCP output signals are in Blue** **Motherboard-generated signals to MCP are in Purple**

* ***Core Power Planes*** include:
All power rails without _DUAL or _SUS in the name except:
- CPU Core Power
- CPU +1.2V_HT
- and optionally, the MCP Core voltage rail

** ***Memory Power Planes*** vary with the memory standard.
- DDR = 2.5, 1.25V
- DDR2 = 1.8, 0.9V
- DDR3 = 1.5, 0.75V

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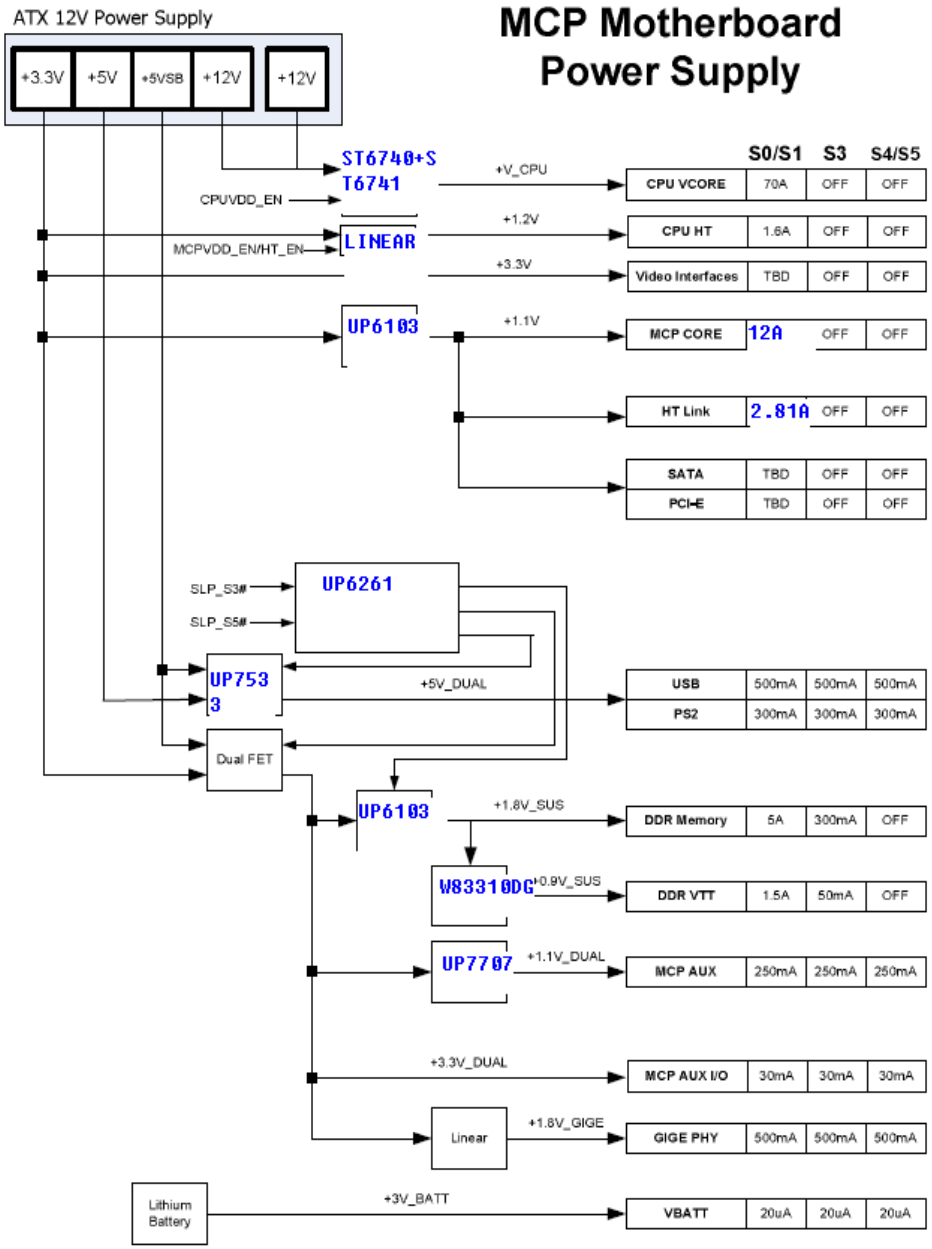
MCP Motherboard Power Supply



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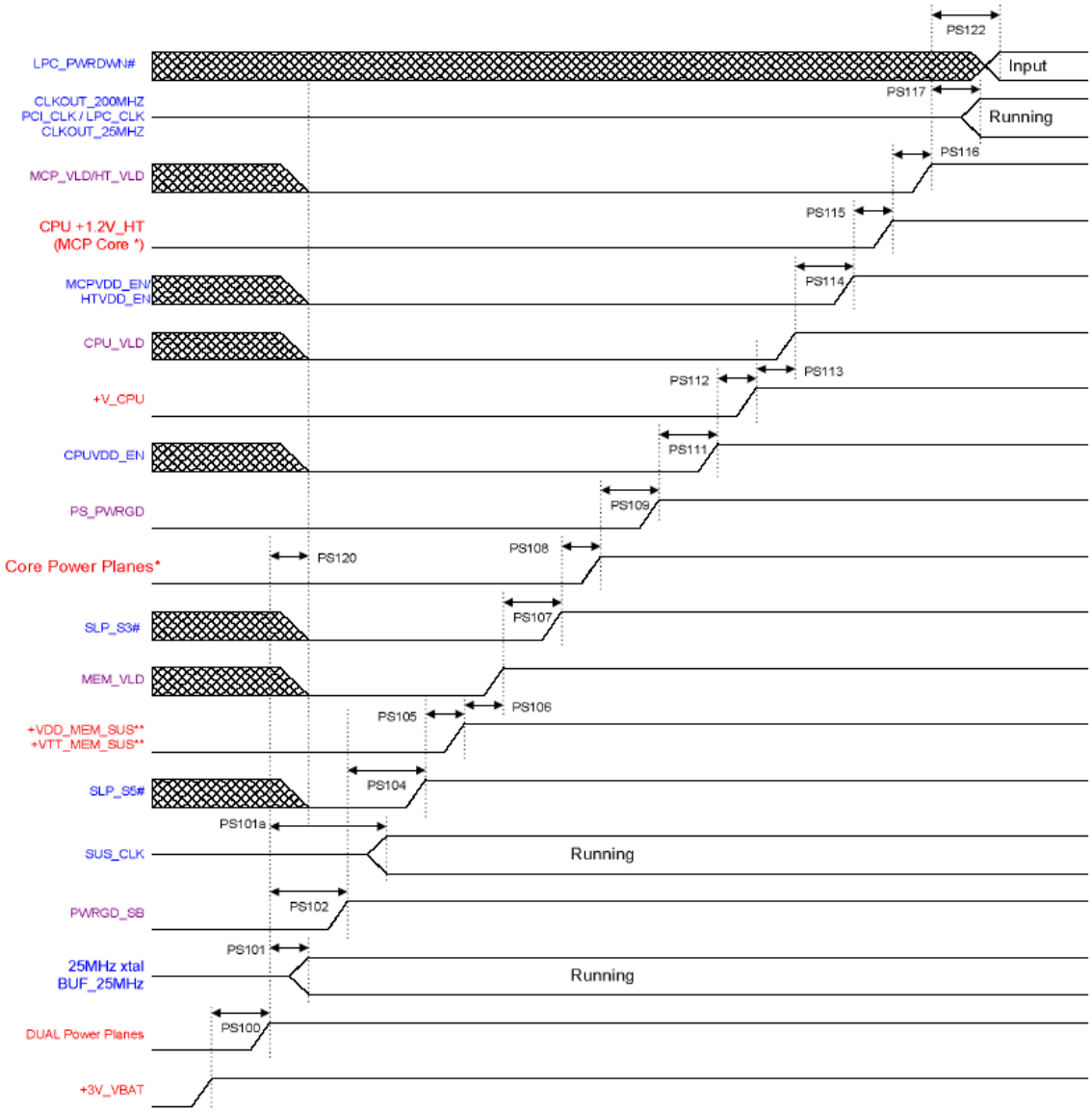

Power Planes are in Red **MCP output signals are in Blue** **Motherboard-generated signals to MCP are in Purple**

* ***Core Power Planes*** include:
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- CPU Core Power
- CPU +1.2V_HT
- and optionally, the MCP Core voltage rail

** ***Memory Power Planes*** vary with the memory standard.
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- DDR3 = 1.5, 0.75V

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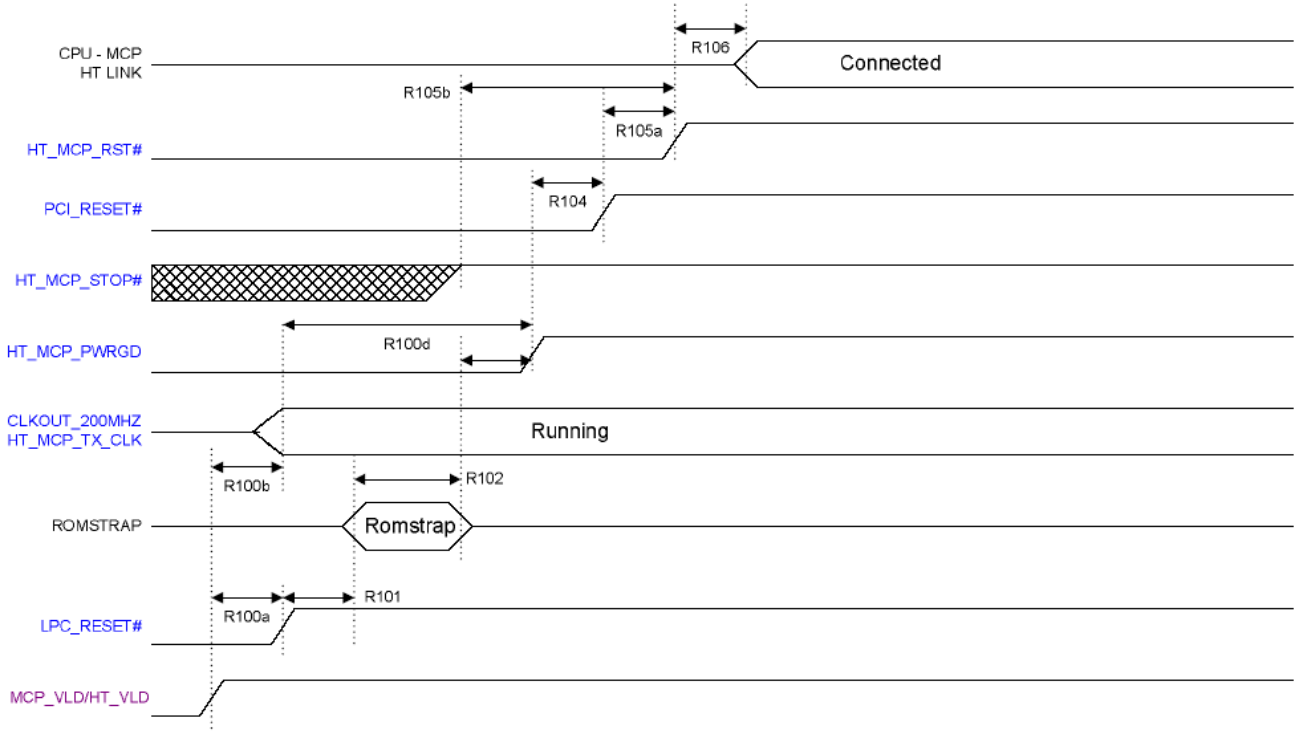
5.2.2. Cold Reset Power-Up Sequence

Figure 5-1 shows the MCP78 cold reset sequence.

This sequence is a continuation of the Power-Up Sequence in the previous chapter.



MCP output signals are in Blue **Motherboard generated inputs to MCP are in Purple**

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MSI	
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