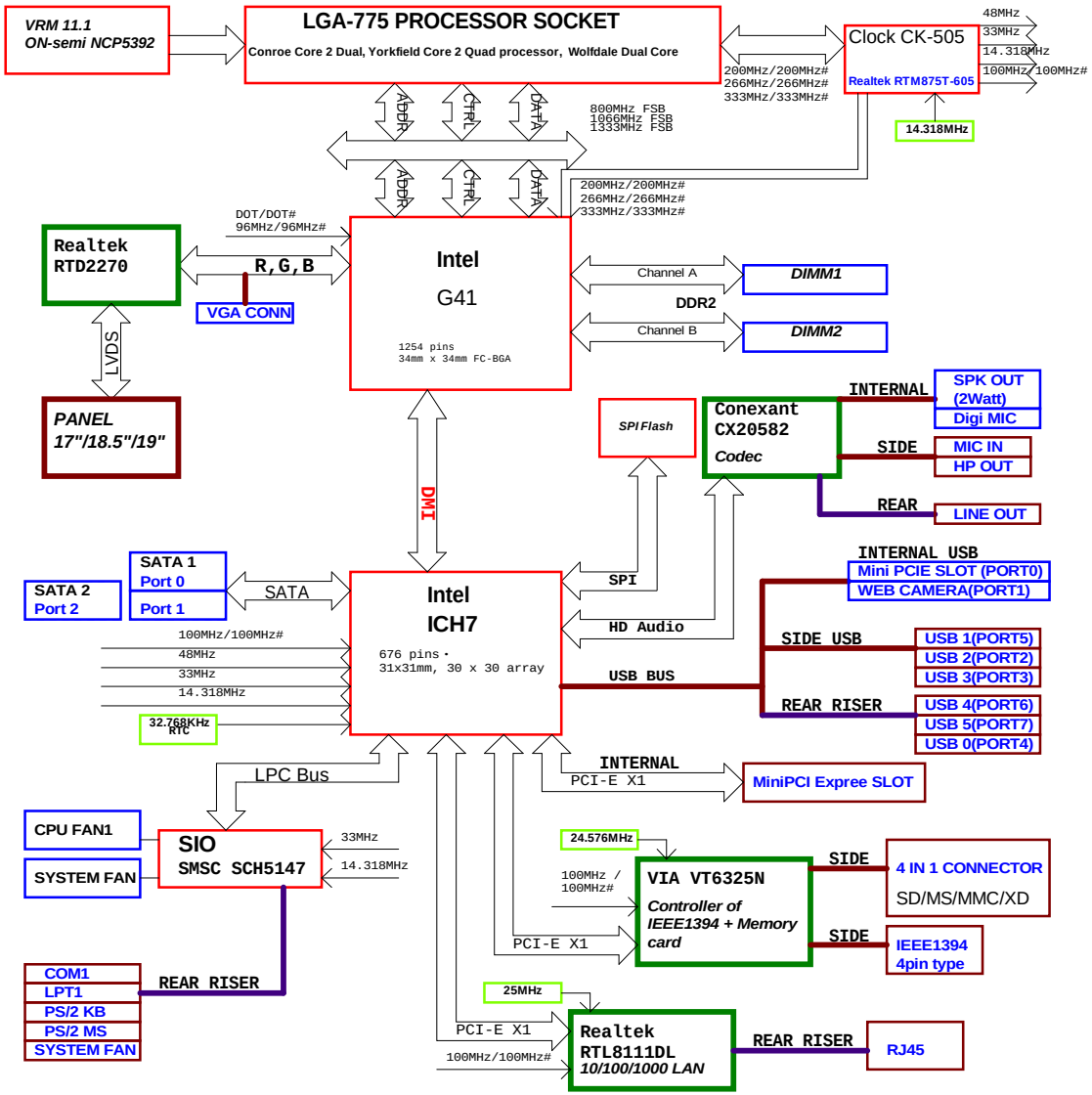
Model: WestLake PCB Ver: A00
PCB: 08174 SCH Ver:01
PCBA: N867P (with 1394/card reader) Board ID[2:1]: 11
PCBA: W099P (w\o 1394/card reader) Board ID[2:1]: 10

4/30



SHEET

BOM Cofiguration
(R): Unmount
(E): EUP circuit
(F): card reader and 1394
(X): remove after MP
(N): For without 1394 and carder sku

<Variant Name>

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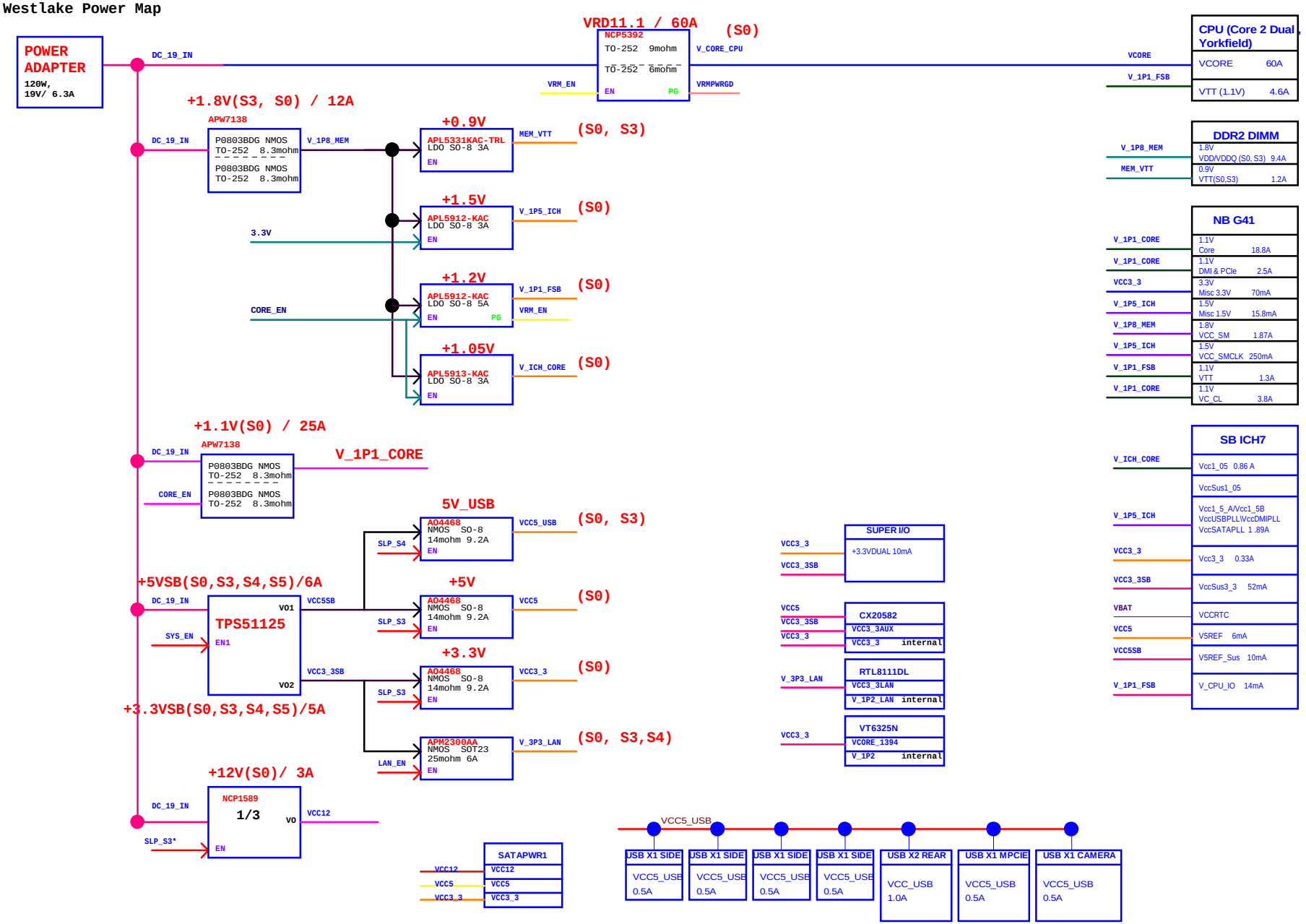
Hsichih, Taipei

Title: COVER PAGE

Size	Document Number	Rev
C	EAGLELAKE	A00

Date: Monday, May 25, 2009 Sheet 1 of 39

Westlake Power Map



<Variant Name>

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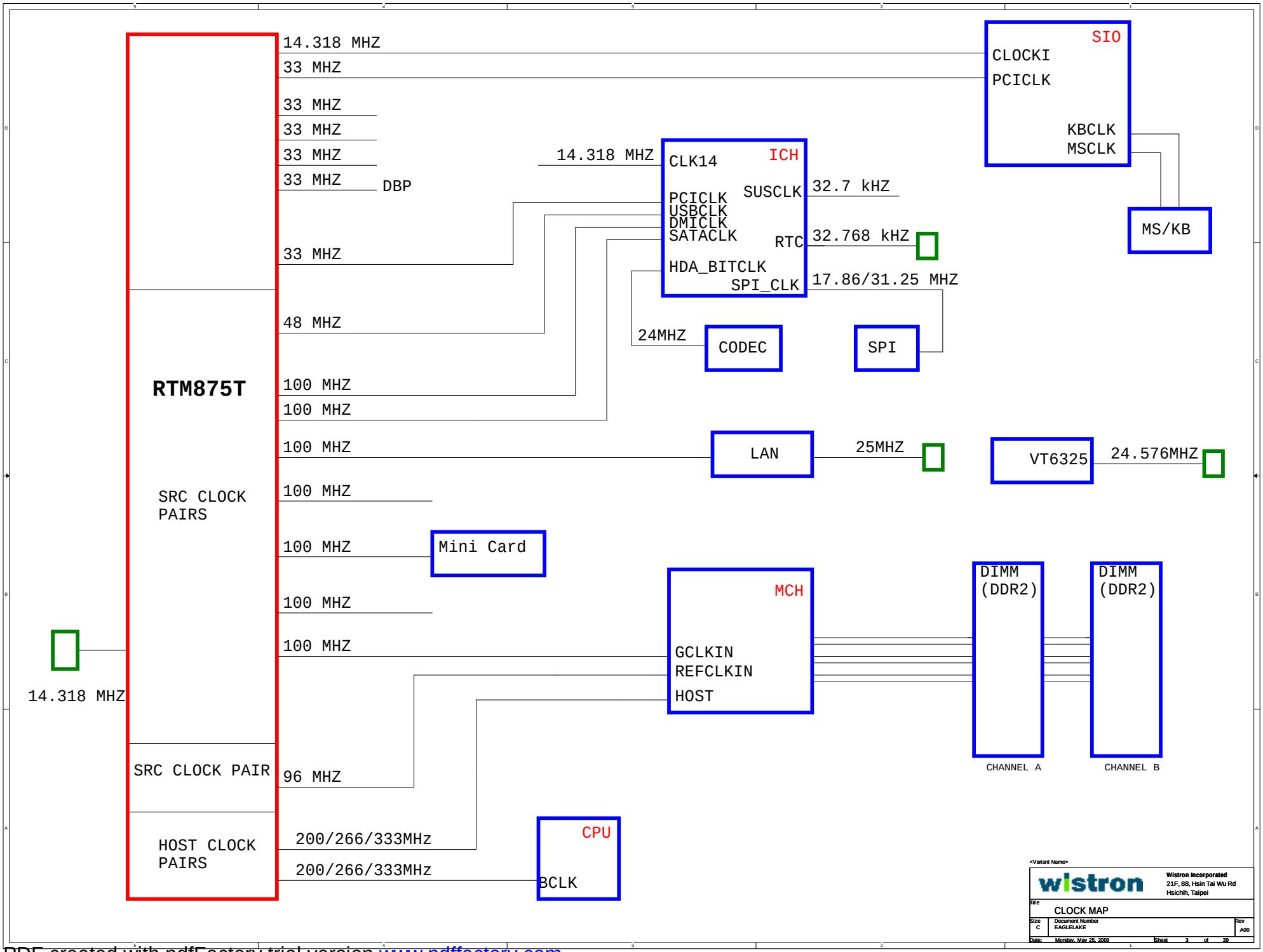
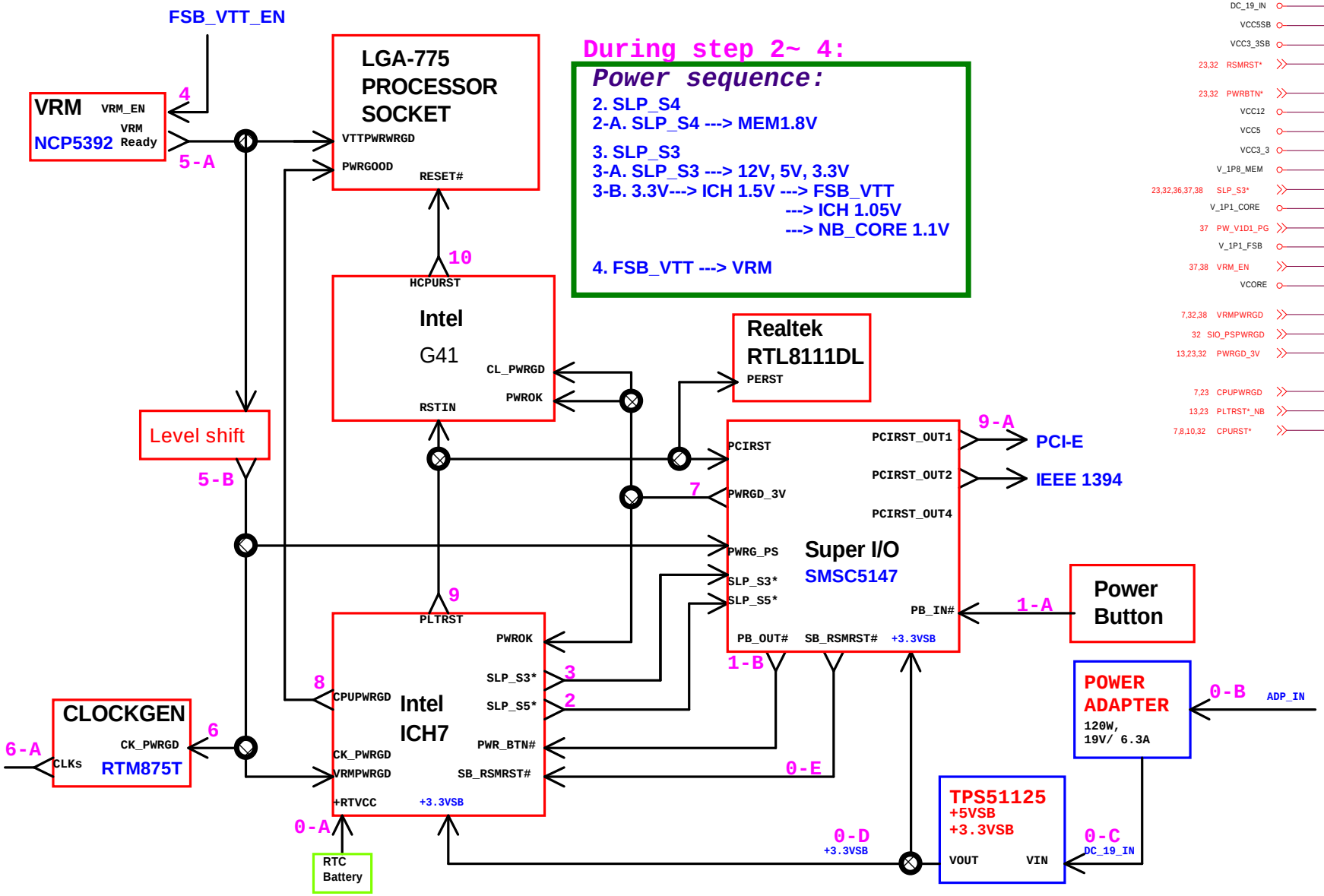
Title: POWER MAP

Size	Document Number	Rev
C	EAGLELAKE	A00

Date: Monday, May 25, 2009 Sheet 2 of 39





<Variant Name>

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Title: SEQUENCE MAP

Size	Document Number	Rev
A3	EAGLELAKE	A00

Date: Monday, May 25, 2009 Sheet 4 of 39

ICH 7

PIN NAME	PIN#	POWER WELL	USAGE	Default Type	DURING RESET	Default Setting	NOTES
GPIO0	AB18	MAIN	ICH_BM_BUSY	GPI	-----	-----	
GPIO1	C8	MAIN	P_REQ_N5	GPI	-----	-----	
GPIO2	G8	MAIN	PIRQJE	GPI	-----	-----	
GPIO3	F7	MAIN	PIRQJF	GPI	-----	-----	
GPIO4	F8	MAIN	PIRQJG	GPI	-----	-----	
GPIO5	G7	MAIN	PIRQJH	GPI	-----	-----	
GPIO6	AC21	MAIN	W_DETECT_N	GPI	-----	-----	For wireless LAN card detected (L: existed)
GPIO7	AC18	MAIN	CB_DET_N	GPI	-----	-----	For PWR BT&LED cable detected (L: existed)
GPIO8	E21	RESUME	non-use	GPI	-----	-----	
GPIO9	E20	RESUME	PANEL_DET	GPI	-----	-----	For ICH7 inform scalar chip function
GPIO10	A20	RESUME	IO_SMI*	GPI	IN	-----	For SIO_SMI* function(low Active)
GPIO11	B23	RESUME	LPC_PME*	Native	IN	-----	For SIO LPC_PME* function(low Active)
GPIO12	F19	RESUME	non-use	GPI	-----	-----	
GPIO13	E19	RESUME	non-use	GPI	-----	-----	
GPIO14	R4	RESUME	AUD_EXPMUTE*	GPI	-----	-----	For AUDIO output Mute function (default : High)
GPIO15	E22	RESUME	non-use	GPI	-----	-----	
GPIO16	AC22	MAIN	AUD_SPKMUTE*	GPO	-----	High	I P/D 20K;For Speaker Mute function (default : High)
GPIO17	D8	MAIN	P_GNT_N5	GPO	-----	-----	INTEGRATED P/U 20K
GPIO18	A20	MAIN	W_DISABLE*	GPO	-----	High	For wireless LAN disable(default : High enable)
GPIO19	AH18	MAIN	INV_DET*	GPI	-----	-----	For Inverter cable detected (L: existed)
GPIO20	AF21	MAIN	non-use	GPO	-----	-----	
GPIO21	AF19	MAIN	LVDS_DET*	GPI	-----	-----	For LVDS cable detected (L: existed)
GPIO22	A13	MAIN	P_REQ_N4	Native	-----	-----	
GPIO23	AA5	MAIN	non-use	Native	-----	-----	Multiplexed with LDRQ1#
GPIO24	R3	RESUME	LAN_EN	GPO	Out	Low	For LAN power enable (Default :Low enable)
GPIO25	D20	RESUME	DMI_MODE	GPO	-----	Low	DMI use AC mode
GPIO26	A21	RESUME	non-use	GPO	-----	-----	
GPIO27	B21	RESUME	SUSLED*	GPO	Out	-----	For Suspend LED function
GPIO28	E23	RESUME	PWRLED*	GPO	Out	-----	For PWR LED function
GPIO29	C3	RESUME	OC*5	Native	-----	-----	
GPIO30	A2	RESUME	OC*67	Native	-----	-----	
GPIO31	B3	RESUME	OC*67	Native	-----	-----	
GPIO32	AG18	MAIN	non-use	GPO	-----	-----	
GPIO33	AC19	MAIN	non-use	GPO	-----	-----	
GPIO34	U2	MAIN	non-use	GPO	-----	High	
GPIO35	AD21	MAIN	CAMERA_EN	GPO	-----	High	For Webcam enable function (default : High enable)
GPIO36	AH19	MAIN	BOARD_ID_1	GPI	-----	-----	Multiplexed with SATA2GP
GPIO37	AE19	MAIN	BOARD_ID_2	GPI	-----	-----	Multiplexed with SATA3GP
GPIO38	AD20	MAIN	RISER1_DET	GPI	-----	-----	For Rear IO cable1 detected (L: existed)
GPIO39	AE20	MAIN	RISER2_DET	GPI	-----	-----	For Rear IO cable2 detected (L: existed)
GPIO48	A14	MAIN	P_GNT_N4	Native	-----	-----	
GPIO49	AG24	CPU	CPUPWRGD	Native	-----	-----	

SCH 5147

GPIO #	Usage	BIOS Post Value	I/O	IN-POWER	OUT-POWER
GP10	PLTRST*_1394	Native(nPCIRST_OUT3)	O	N/A	AUX (VTR)
GP11	PLTRST*_RISER	Native(nPCIRST_OUT1)	O	N/A	AUX (VTR)
GP12	PLTRST*_LAN	Native(nPCIRST_OUT2)	O	N/A	AUX (VTR)
GP14	PLTRST*_DBP	Native(nPCIRST_OUT4)	O	N/A	AUX (VTR)
GP15	non-use	non-use		N/A	MAIN (VCC)
GP16	PROCHOT*_L	PROCHOT* (Processor Hot Function) Default High.Over 85 degree, Enable PROCHOT Function	OD	N/A	AUX (VTR)
GP17	SYS_FAN2_CTRL_SIO	PWM3	O	N/A	AUX (VTR)
GP20	ICH_BM_BUSY	Natice(PECI Request)	I	AUX (VTR)	MAIN (VCC)
GP21	KBDATA	Native(KBDATA)	O	AUX (VTR)	MAIN (VCC)
GP22	KBCLK	Native(KBCLK)	O	AUX (VTR)	MAIN (VCC)
GP27	IO_SMI*	Native (IO_SMI*)	O	AUX (VTR)	AUX (VTR)
GP32	MSDATA	Native(MSDATA)	O	AUX (VTR)	MAIN (VCC)
GP33	MSCLK	Native(MSCLK)	O	AUX (VTR)	MAIN (VCC)
GP36	KBRST*	Native(KBRST*)	O	AUX (VTR)	MAIN (VCC)
GP37	A20GATE	Native(A20GATE)	O	AUX (VTR)	MAIN (VCC)
GP40	non-use	non-use		AUX (VTR)	AUX (VTR)
GP41	non-use	non-use	O	AUX (VTR)	AUX (VTR)
GP42	LPC_PME*	Native(nIO_PME)	O	AUX (VTR)	AUX (VTR)
GP43	AUTO_COLOR_SIO	AUTO_COLOR_SIO(Default: High)	O	AUX (VTR)	MAIN (VCC)
GP50	Panel_FB	Panel_FB	I	AUX (VTR)	AUX (VTR)
GP51	SMBUS_ISP	H:ISP ,L:disable(default)	OD	AUX (VTR)	AUX (VTR)
GP52	CPU_GTLREF_CTRL_1	GPO (Default: Low)	O	AUX (VTR)	AUX (VTR)
GP53	CPU_GTLREF_CTRL_2	GPO(Default: High)	O	AUX (VTR)	AUX (VTR)
GP54	PRT_ISP	L:ISP ,H:disable(default)	OD	AUX (VTR)	AUX (VTR)
GP55	PANEL_SEL1	PANEL type select	OD	AUX (VTR)	AUX (VTR)
GP56	PANEL_SEL2	PANEL type select	OD	AUX (VTR)	AUX (VTR)
GP57	PANEL_SEL3	PANEL type select	OD	AUX (VTR)	AUX (VTR)
GP60	PECI_READY1	Native(PECI Ready)	I	AUX (VTR)	AUX (VTR)
GP61	PECI_SIO_R	Native(PECI IO)	I	AUX (VTR)	AUX (VTR)

3/11

3/11

CN1 DVD-CON2-10-GP

CN2 DVD-CON2-10-GP

21.60695.102
21.60564.102

EMI

VCC3_3SB — EC8 SCD1U16V2ZY-2GP — EC12 SCD1U16V2ZY-2GP

VCC3_3 — EC7 SCD1U16V2ZY-2GP — EC9 SCD1U16V2ZY-2GP

VCC3_3 — EC13 SCD1U16V2ZY-2GP — EC14 SCD1U16V2ZY-2GP

VCC5_USB — EC15 SCD1U16V2ZY-2GP — EC16 SCD1U16V2ZY-2GP

(87.00A52.220) H8 HOLE — (R87.00A52.220) H7 HOLE

5/20

Mini PCIE holder

(R) H4 HOLE — (R) H2 HOLE — (R) H1 HOLE — (R) H5 HOLE

CPU Heatsink screw hole.

NB heatsink

60.3AG10.001

2D label

xx-xxxxxx-xxxxx-xxx-xxxx-X01
Made in xxxxx
DP/N xxxxxx

40.3V302.001

H10 (R) GEN315R140-8-F-A — H6 (R) GEN315R140-8-F-A

H3 (R) GEN315R140-8-F-A — H9 (R) GEN315R140-8-F-A

HLDR-SUPPORT * 4

5/25

42.3AG23.001

SMBUS MAP

ICH7: SMBDATA, SMBCLK

ALERT_DATA
ALERT_CLK

SMSC5147: SDA, SCLK, SDA1, SCLK1

VCC3_3SB — 4.7K — 4.7K

ALERT_DATA
ALERT_CLK
SMBDATA
SMBCLK

4.7K — 4.7K — VCC3_3

DIMM1 Address: 000 A0

DIMM2 Address: 010 A2

XDP connector

RTM875T-605 Address: D2 :WRITE D3 :READ

Mini card Address:

0ohm : optional

<Variant Name>

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Title: GPIO/HOLE/EMI CAP

Size: A2 | Document Number: EAGLELAKE | Rev: A00

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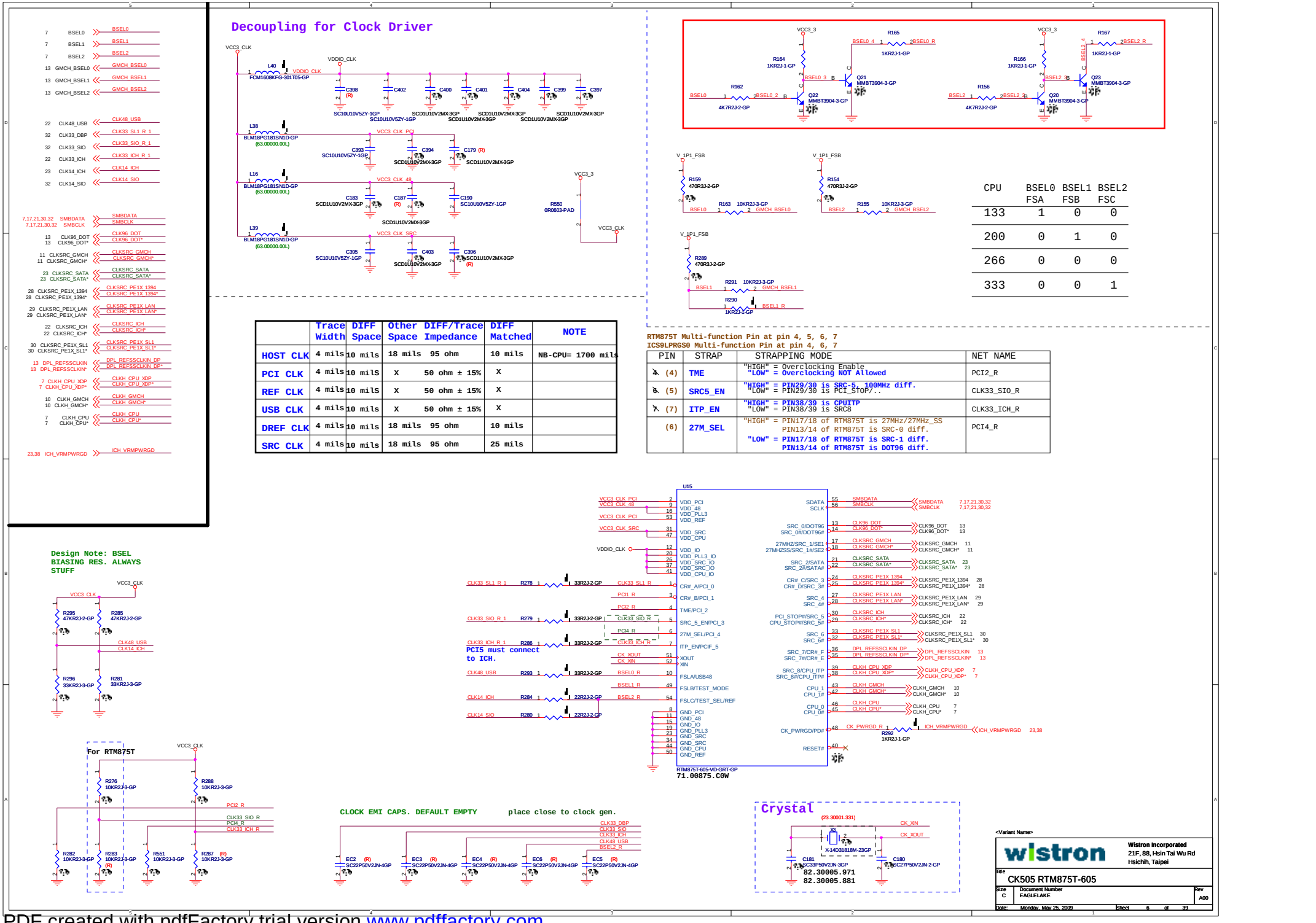

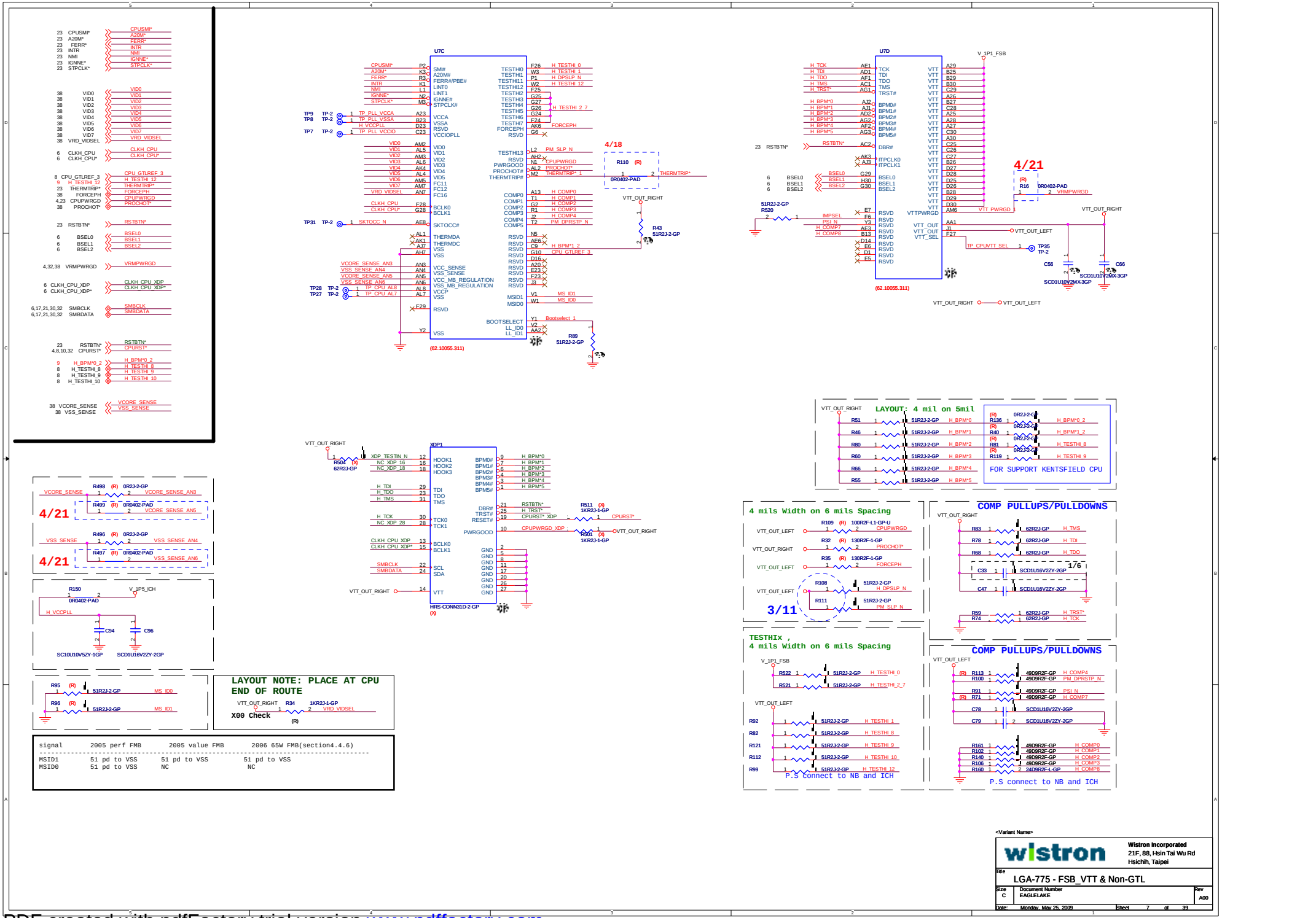

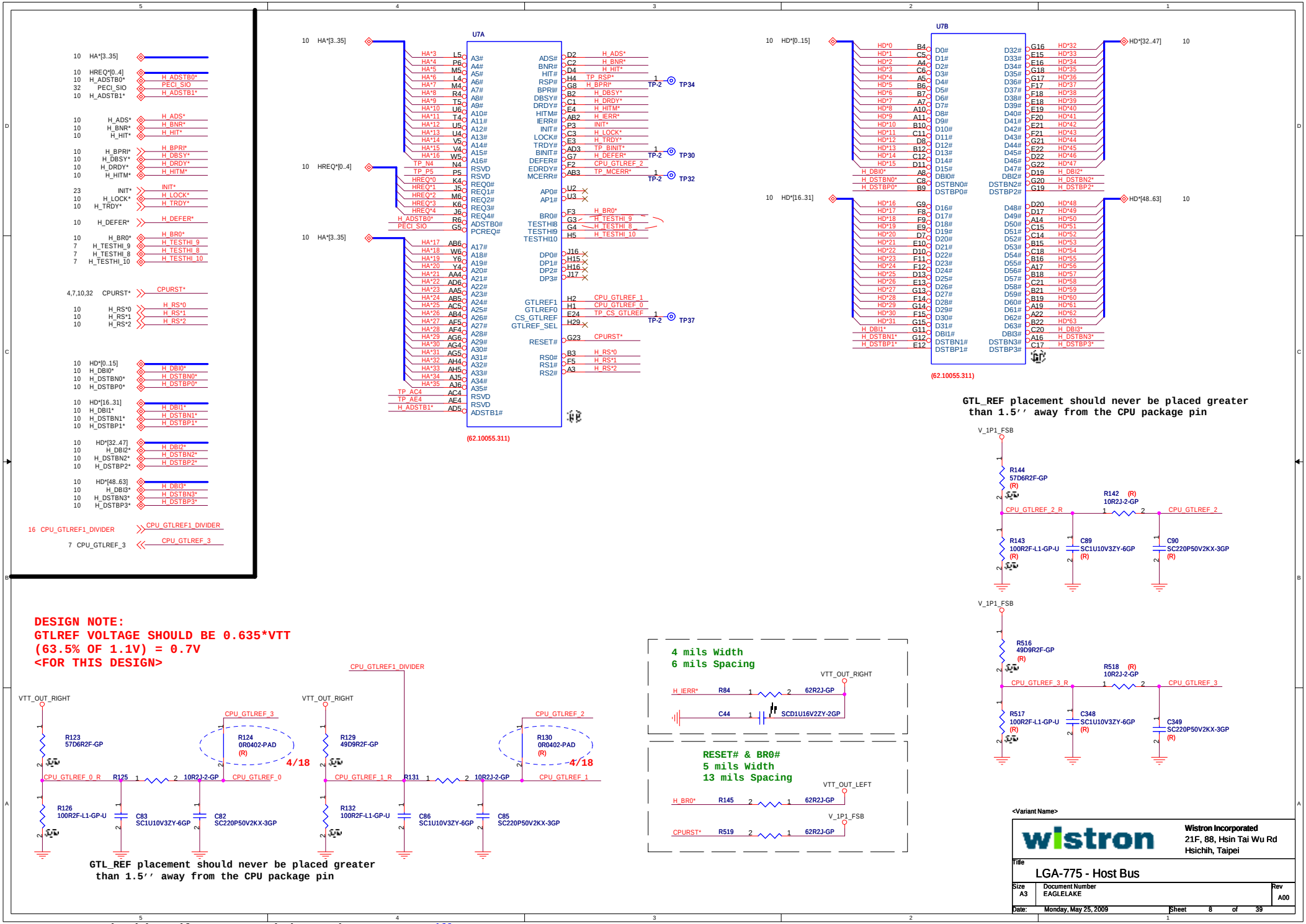

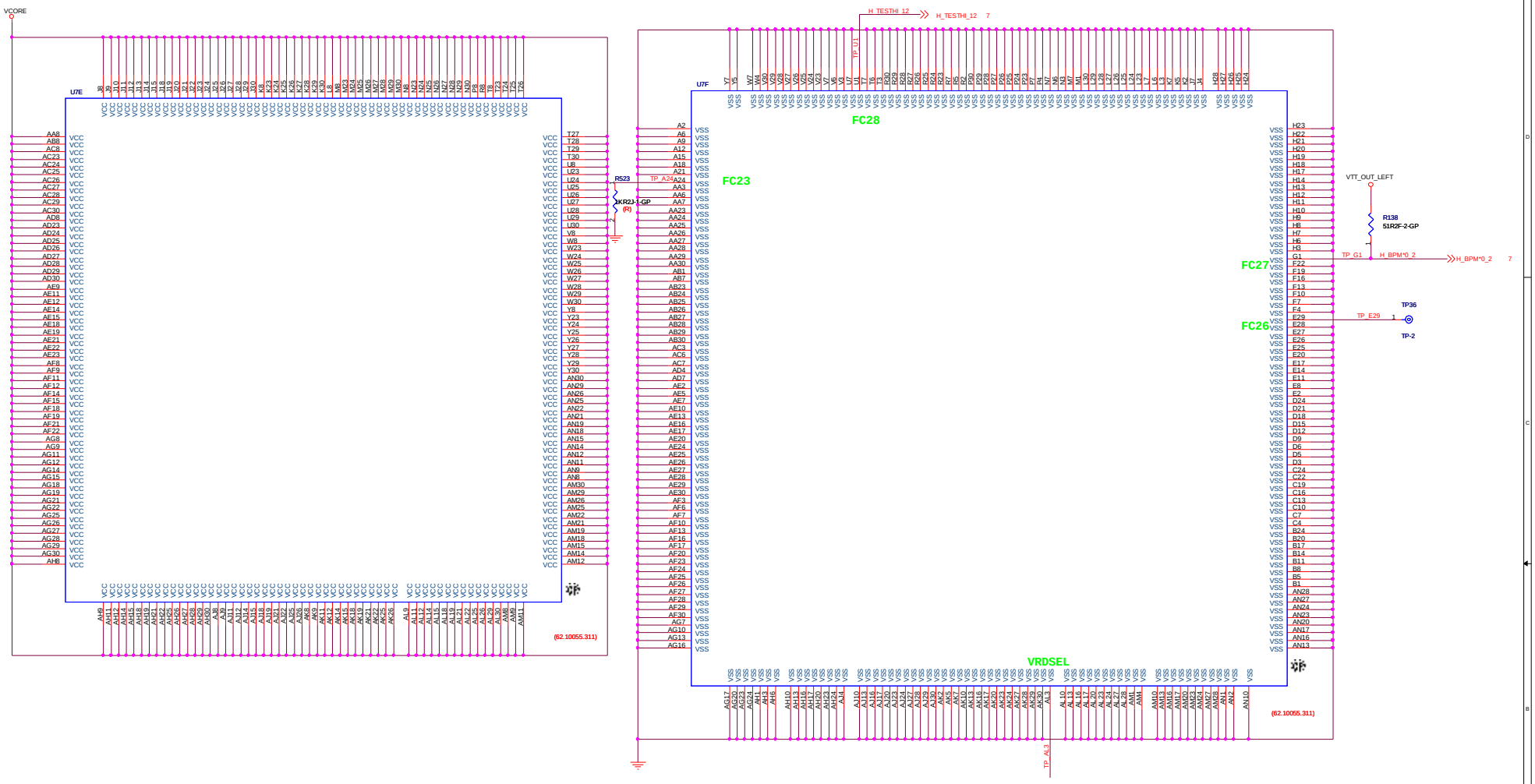

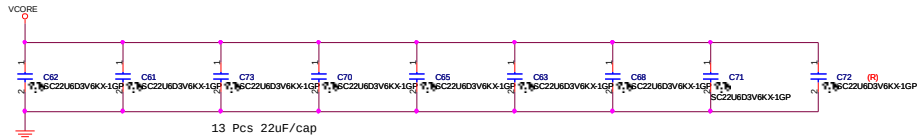

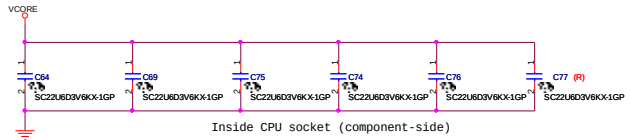

<Variant Name>

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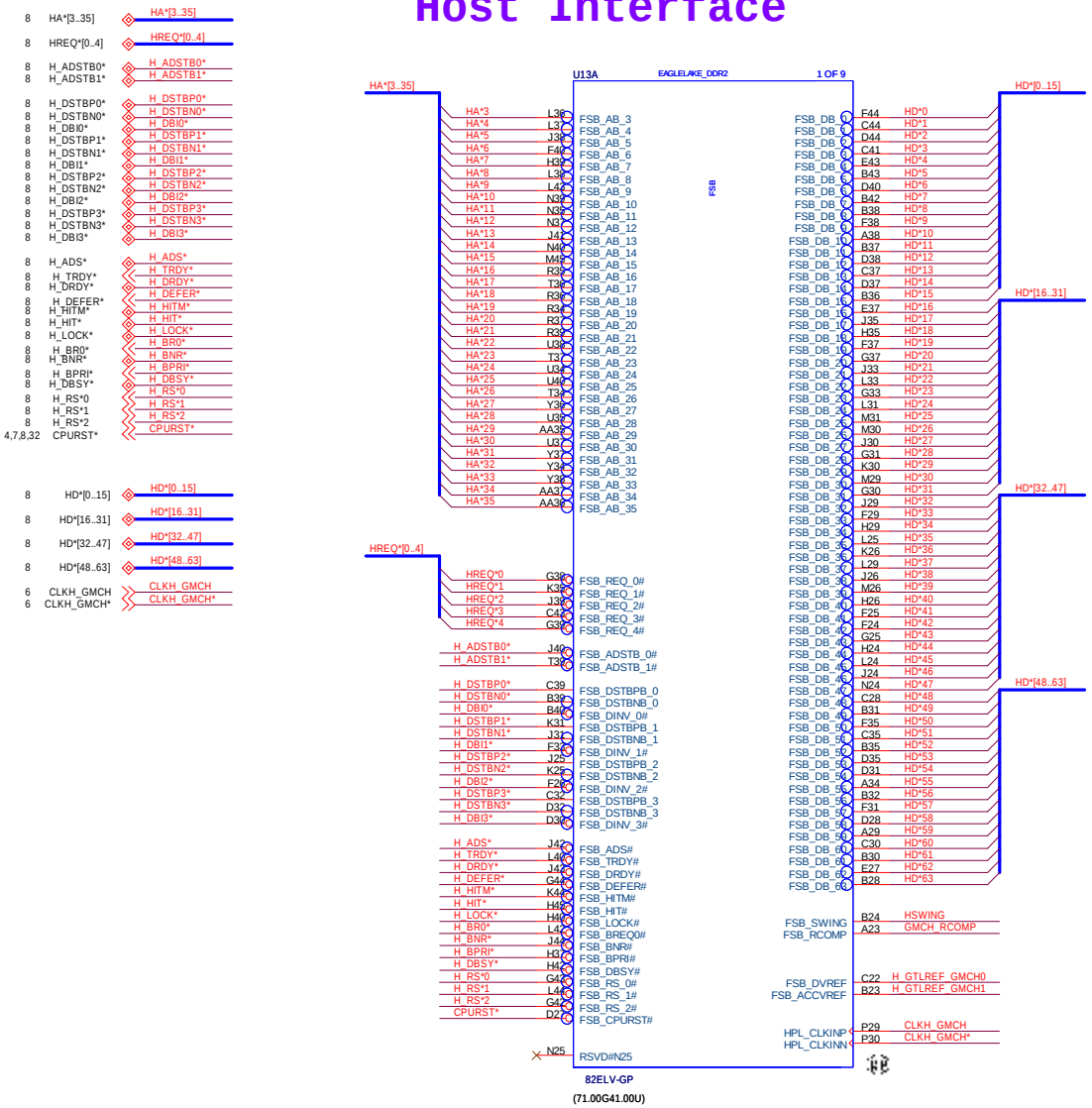
Title: LGA-775 - VCORE & GND

Size	Document Number	Rev
C	EAGLELAKE	A00

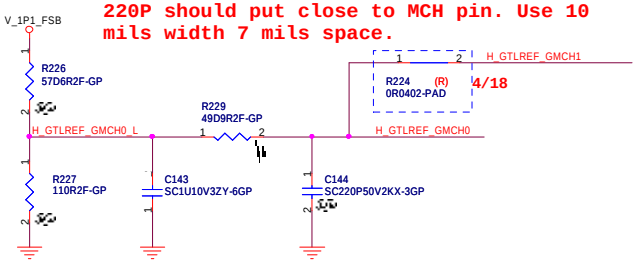
Date: Monday, May 25, 2009 Sheet 9 of 39

Host Interface

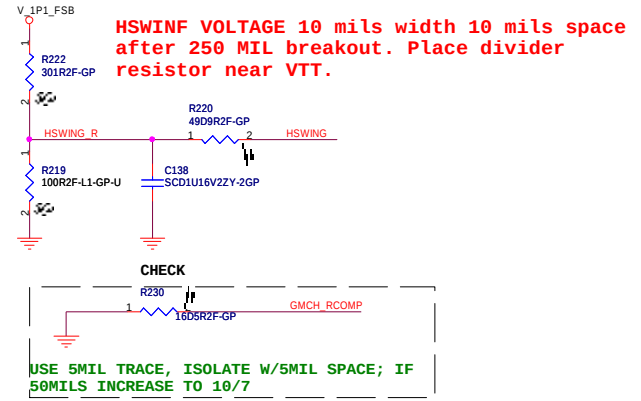


MCH_GTLREF VOLTAGE SHOULD BE
0.635 * VTT = 0.7V

220P should put close to MCH pin. Use 10 mils width 7 mils space.



HSWINF VOLTAGE 10 mils width 10 mils space after 250 MIL breakout. Place divider resistor near VTT.



USE 5MIL TRACE, ISOLATE W/5MIL SPACE; IF 50MILS INCREASE TO 10/7

<Variant Name>

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Title: Eaglelake-G Host Bus

Size	Document Number	Rev
Custom	EAGLELAKE	A00

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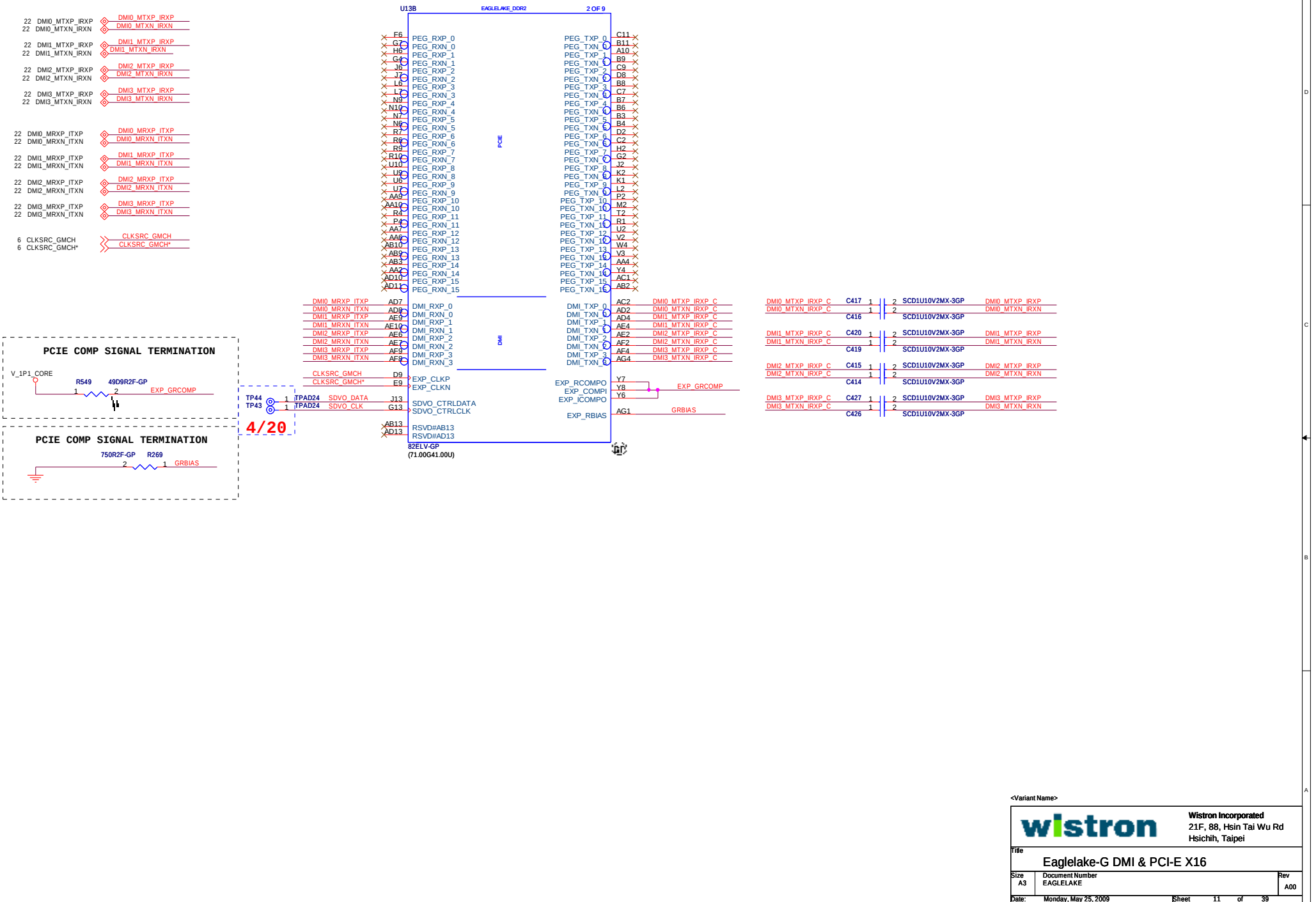

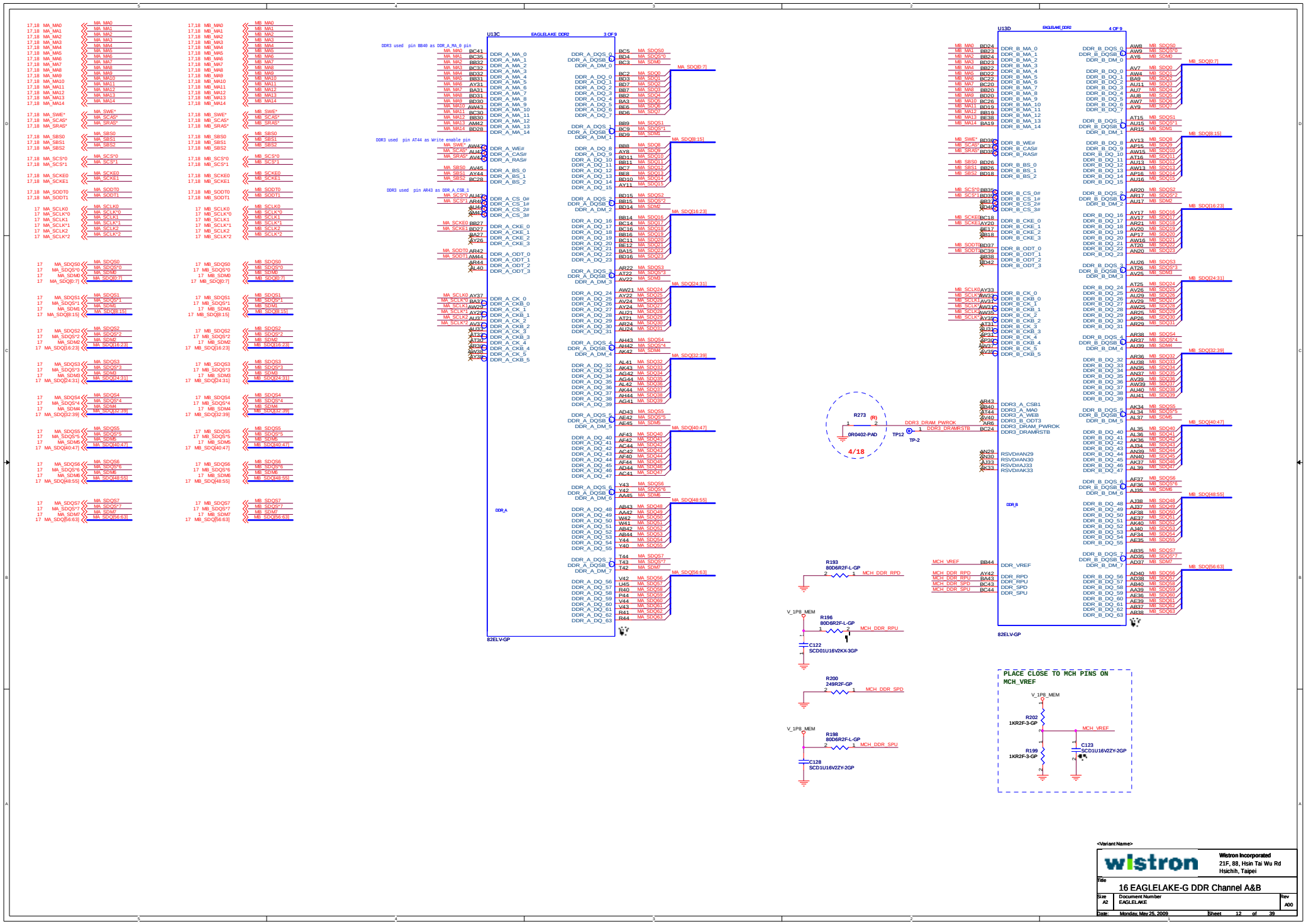

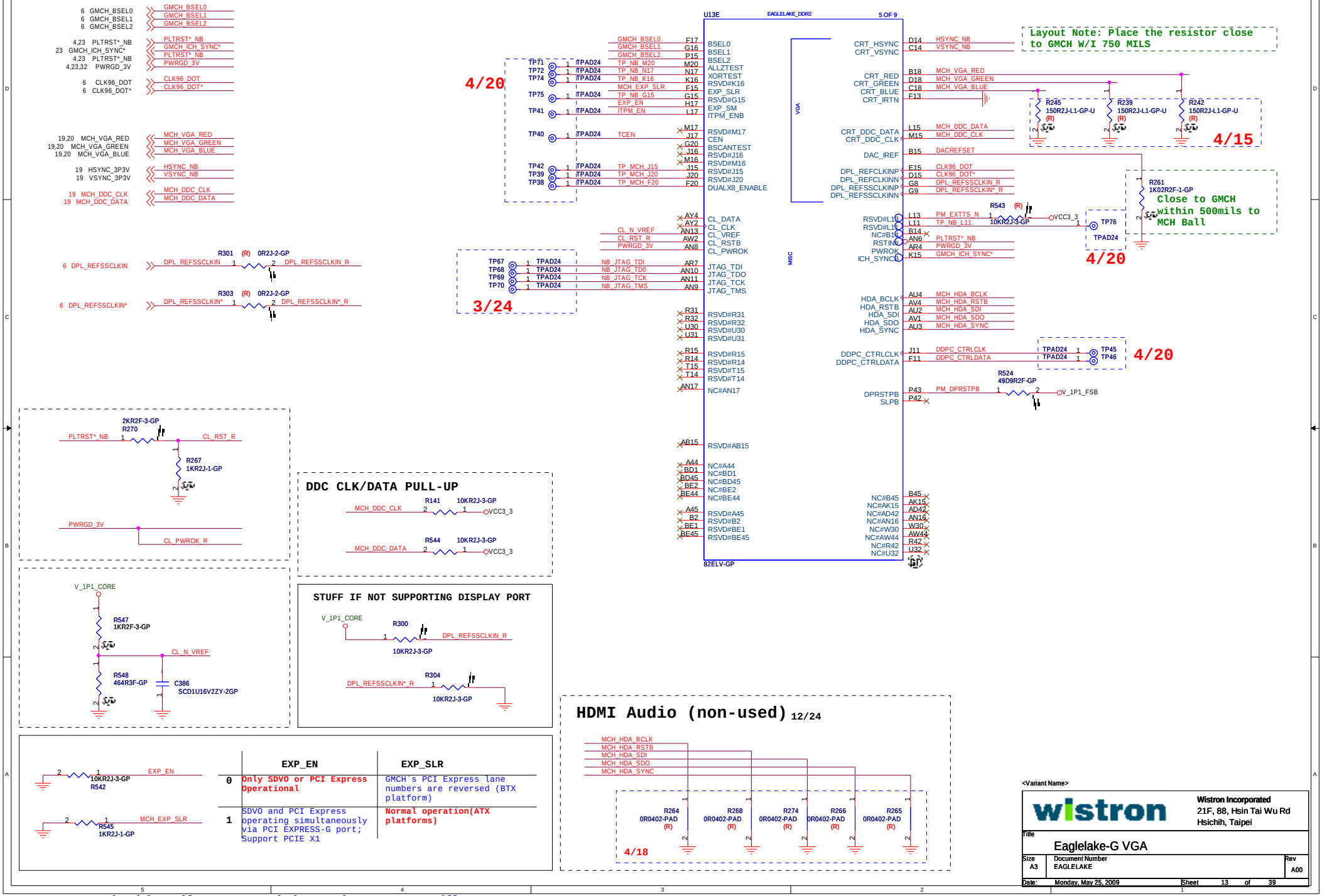

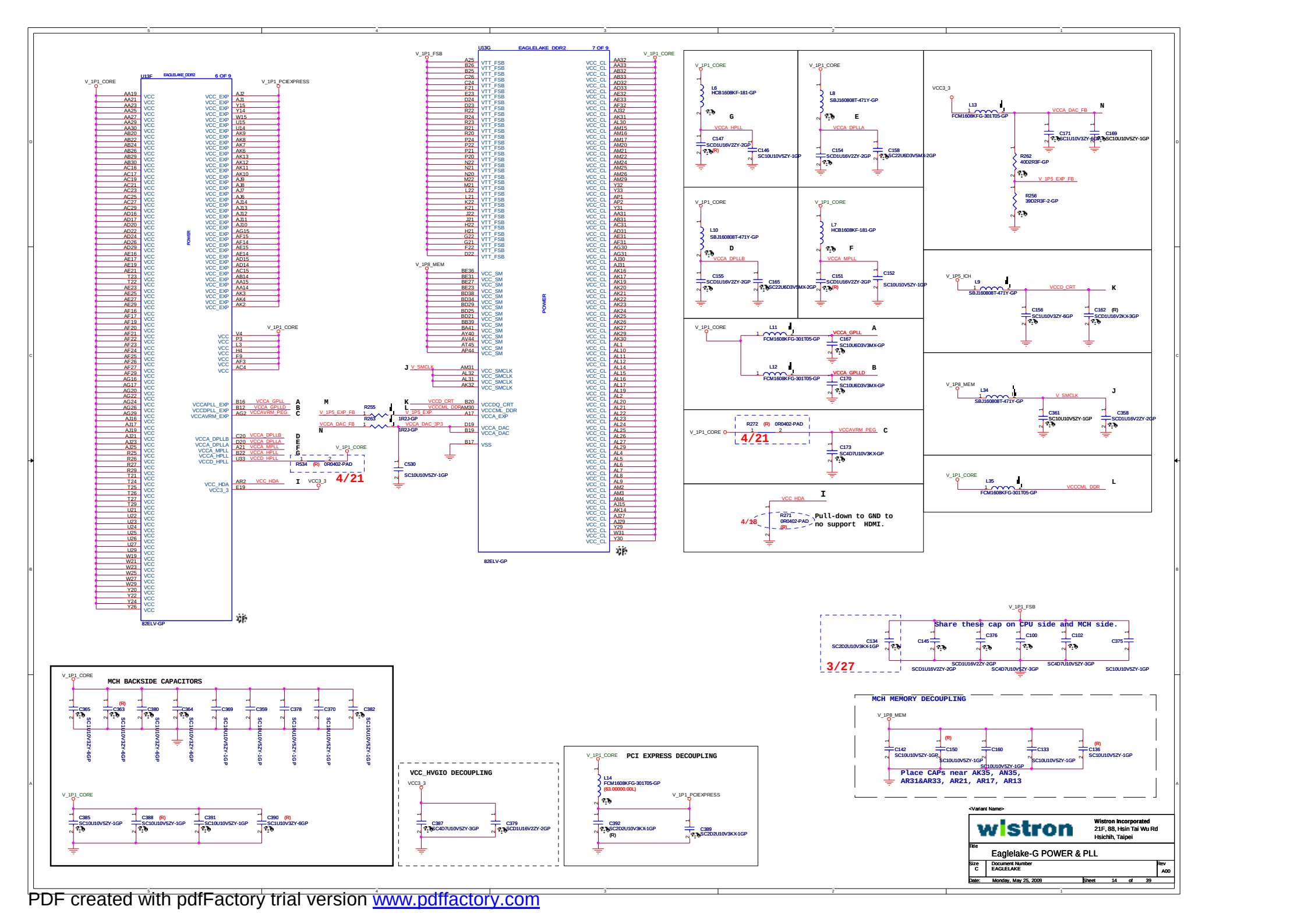

<Variant Name>

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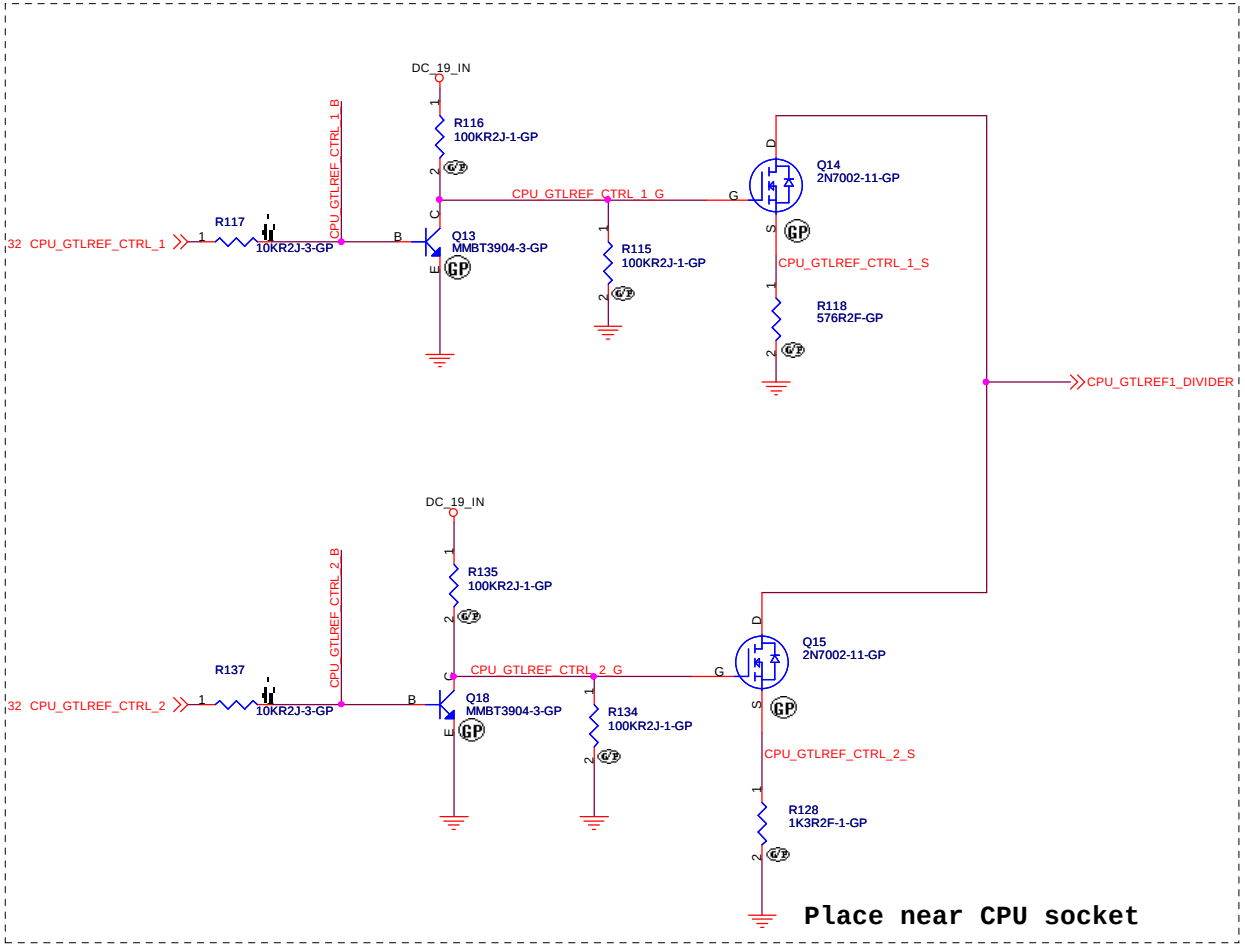
Title: Eaglelake-G GND

Size: Custom | Document Number: EAGLELAKE | Rev: A00

Date: Monday, May 25, 2009 | Sheet 15 of 39



CPU_GTLREF_CTRL_1	CPU_GTLREF_CTRL_2	Ratio
1	1	0.67
1	0	0.65
0	1	0.63 Default value
0	0	0.615

<Variant Name>

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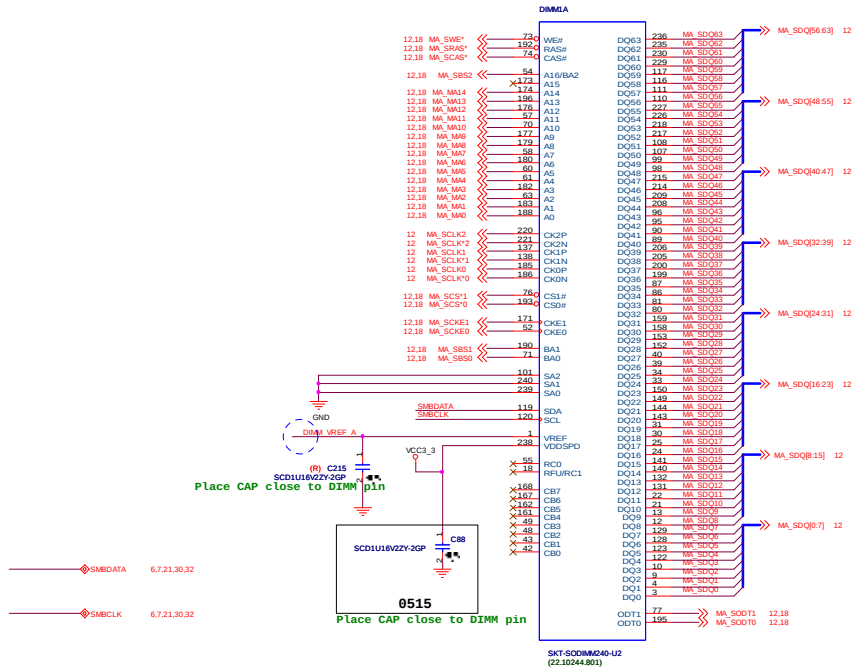
Title: GTL VREF SEL

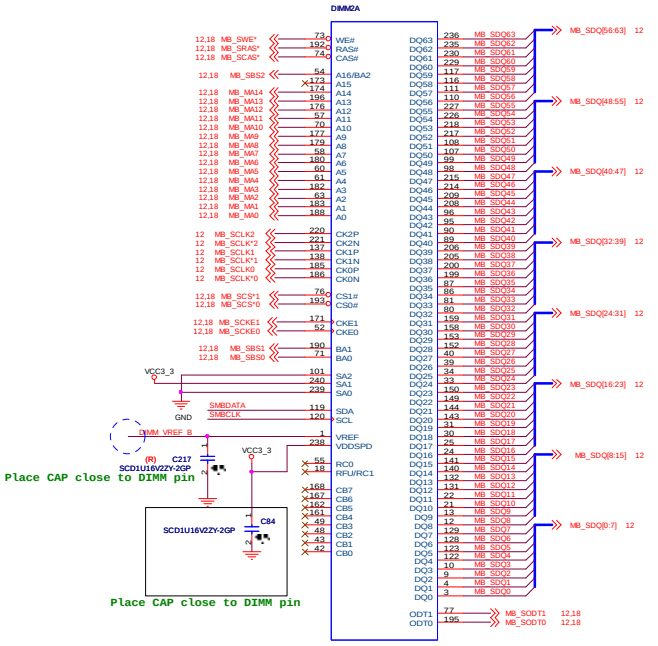
Size	Document Number	Rev
B	EAGLELAKE	A00

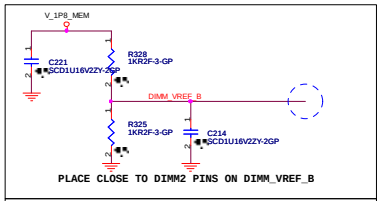
Date: Monday, May 25, 2009 Sheet 16 of 39

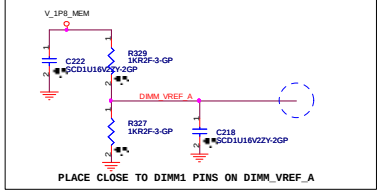
Channel A, Slot 1

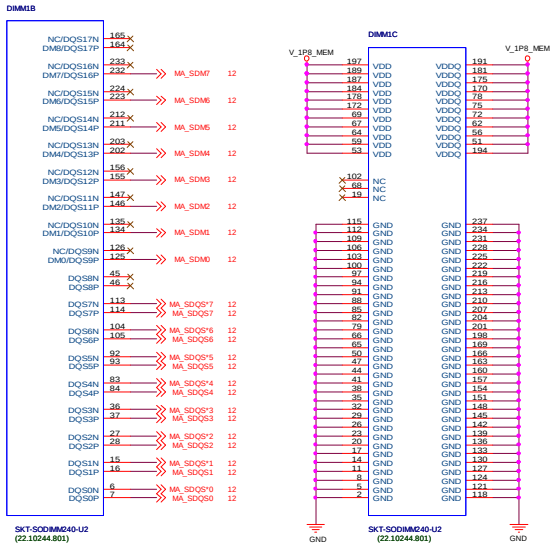


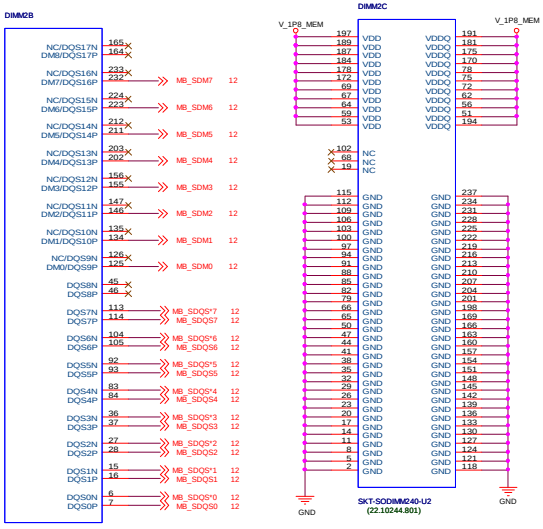
Channel B, Slot 1

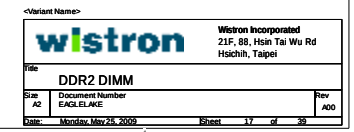




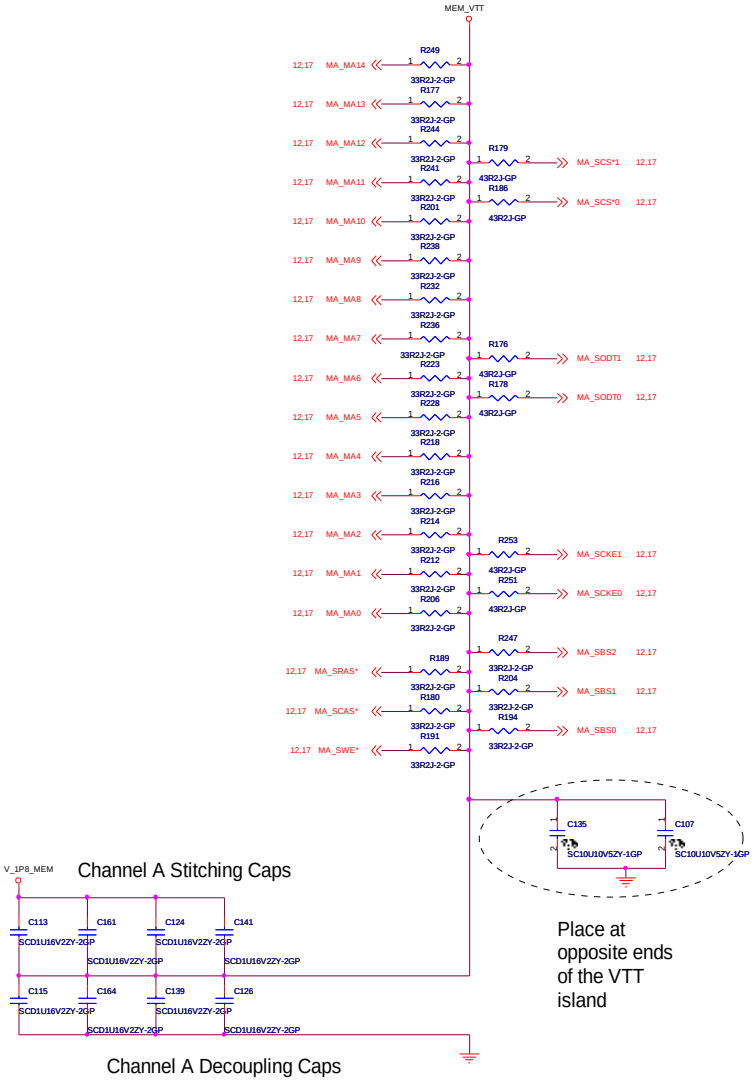








Channel A

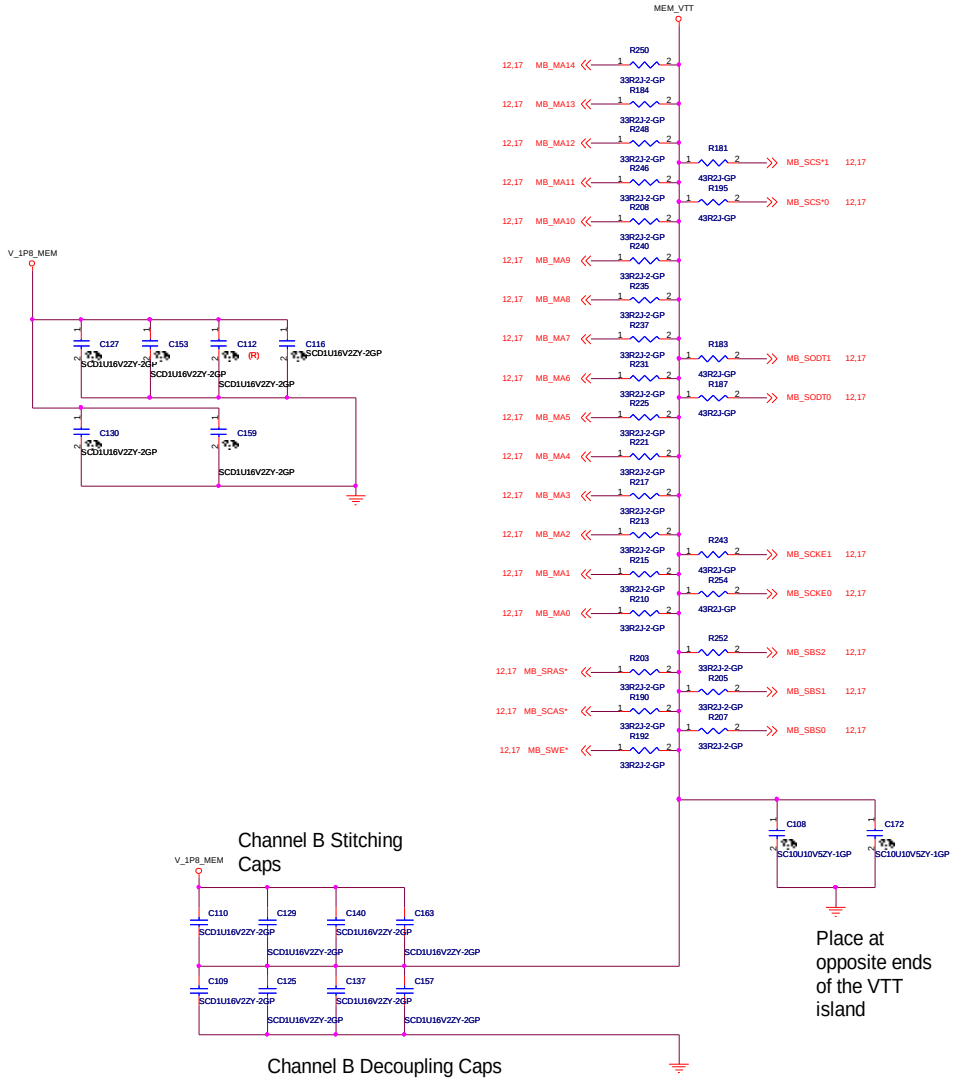


Channel A Stitching Caps

Place at opposite ends of the VTT island

Channel A Decoupling Caps

Channel B



Channel B Stitching Caps

Place at opposite ends of the VTT island

Channel B Decoupling Caps

<variant_name>

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Hsichih, Taipei

Title: DDR2 Terms & Decaps

Size	Document Number	Rev
C	EAGLELAKE	A00

Date: Monday, May 25, 2009 Sheet 18 of 39

From MCH

13 HSYNC_3P3V → HSYNC_3P3V
13 VSYNC_3P3V → VSYNC_3P3V

13 MCH_DDC_CLK → MCH_DDC_CLK
13 MCH_DDC_DATA → MCH_DDC_DATA

HSYNC_3P3V — R114 (R) 0R0402-PAD — HSYNC_5V_CON

VSYNC_3P3V — R120 (R) 0R0402-PAD — VSYNC_5V_CON

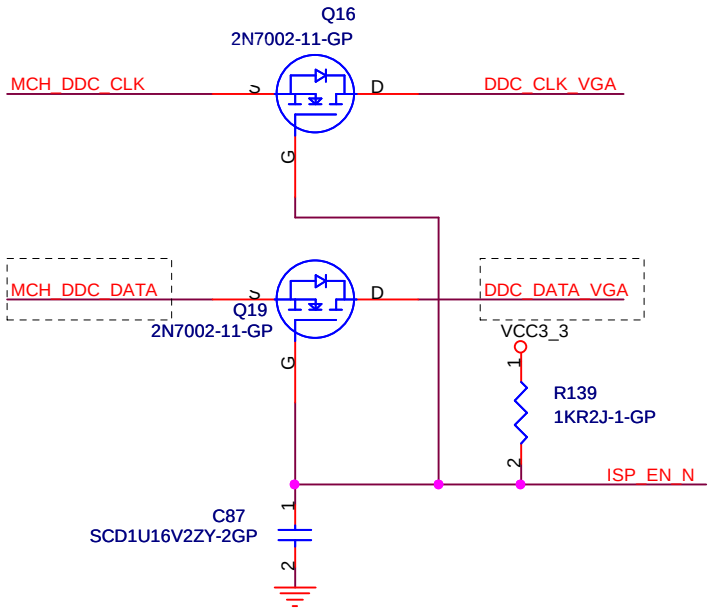
4/18

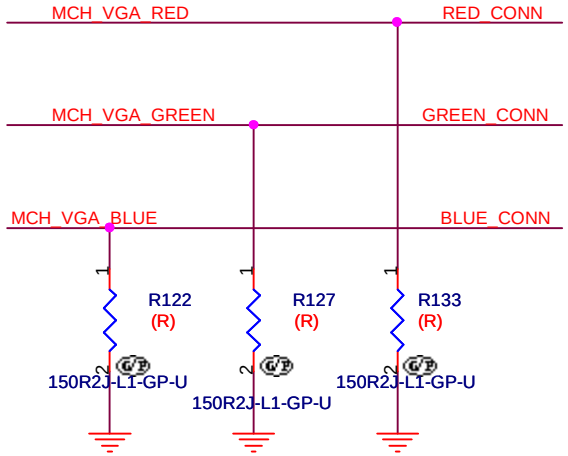
13,20 MCH_VGA_RED → MCH_VGA_RED
13,20 MCH_VGA_GREEN → MCH_VGA_GREEN
13,20 MCH_VGA_BLUE → MCH_VGA_BLUE

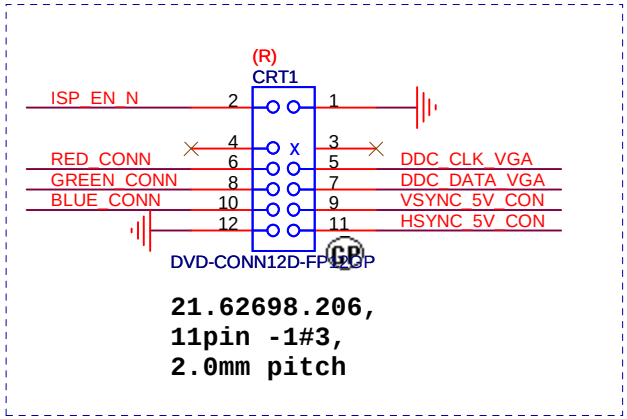
To SCALAR

20 DDC_CLK_VGA → DDC_CLK_VGA
20 DDC_DATA_VGA → DDC_DATA_VGA
20 VSYNC_5V_CON → VSYNC_5V_CON
20 HSYNC_5V_CON → HSYNC_5V_CON

13,20 RED_CONN → RED_CONN
13,20 GREEN_CONN → GREEN_CONN
13,20 BLUE_CONN → BLUE_CONN







<Variant Name>

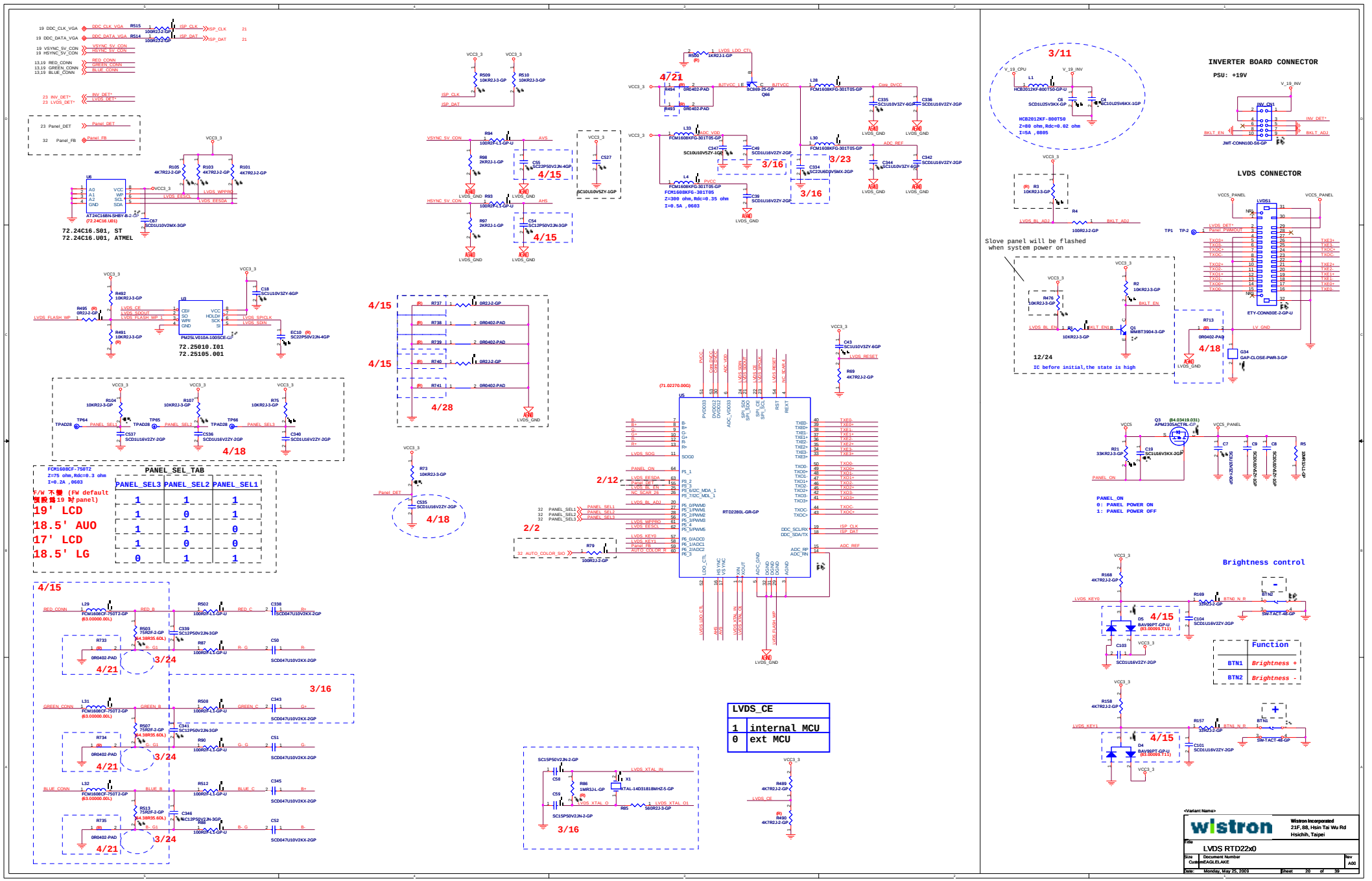
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: VGA CONNECTOR

Size	Document Number	Rev
A	EAGLELAKE	A00

Date: Monday, May 25, 2009 Sheet 19 of 39



PARALLEL PORT

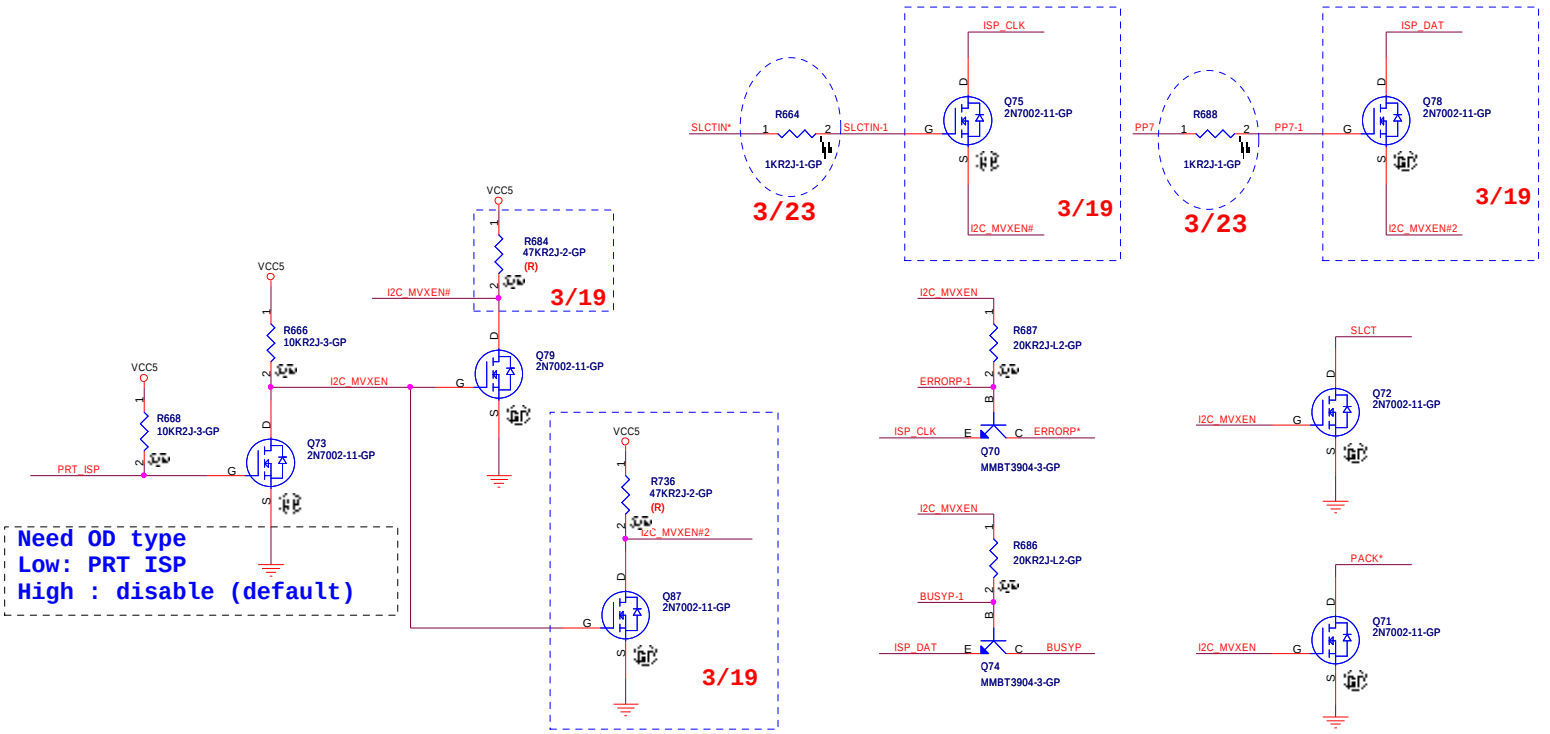
32,33 ERRORP* — ERRORP*
32,33 SLCTIN* — SLCTIN*

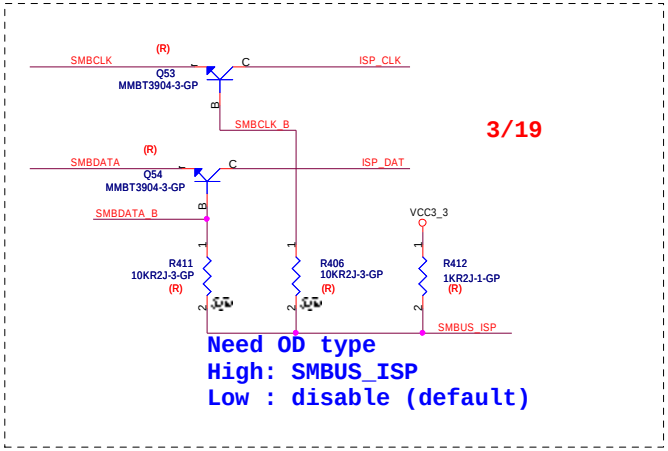
32,33 BUSYP — BUSYP
32,33 PP7 — PP7

32,33 SLCT — SLCT
32,33 PACK* — PACK*

32 PRT_ISP — PRT_ISP
20 ISP_CLK — ISP_CLK
20 ISP_DAT — ISP_DAT

6,7,17,30,32 SMBCLK — SMBCLK
6,7,17,30,32 SMBDATA — SMBDATA
32 SMBUS_ISP — SMBUS_ISP





<Variant Name>

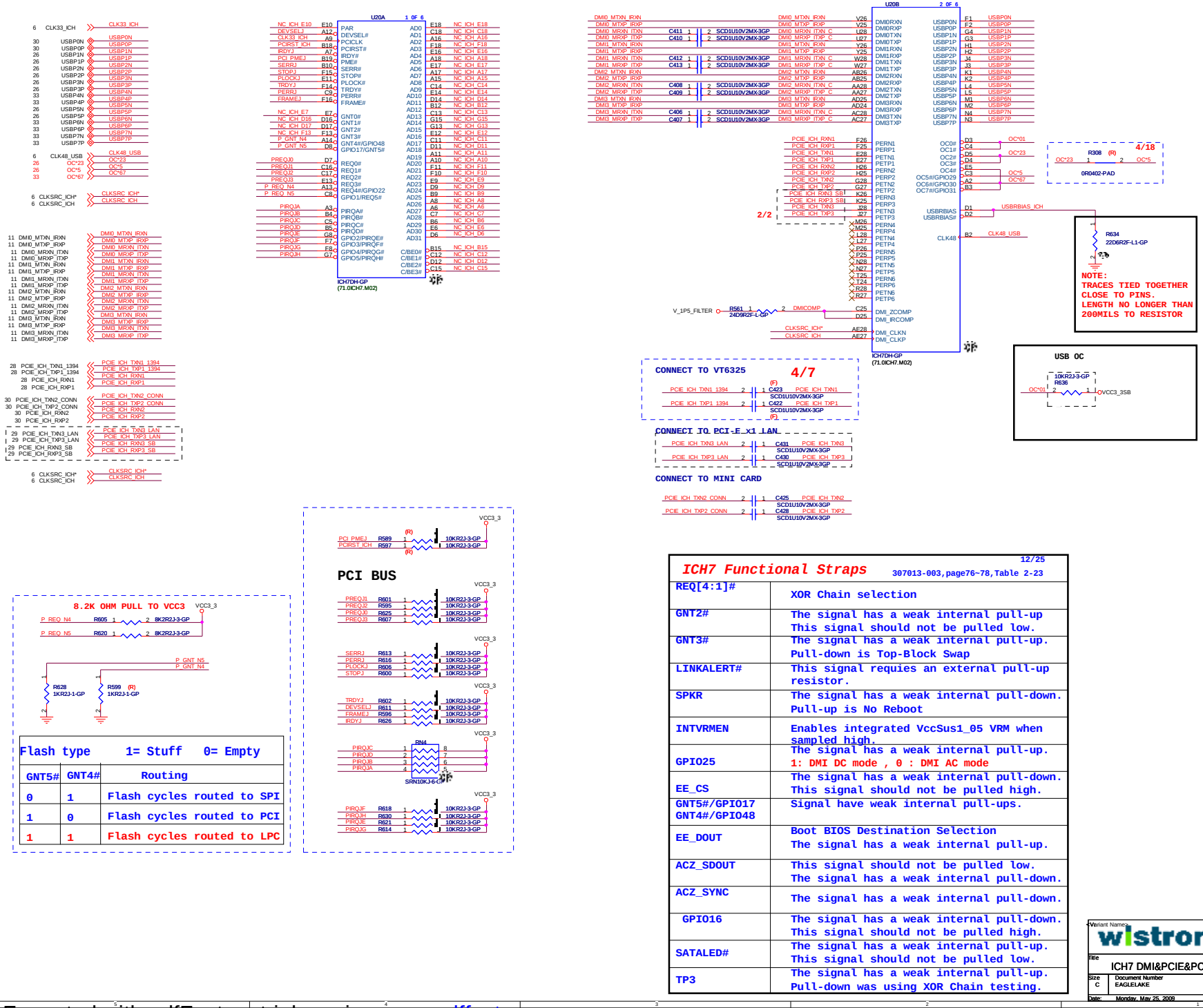
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: PRT and SMBUS ISP

Size	Document Number	Rev
A3	EAGLELAKE	A00

Date: Monday, May 25, 2009 Sheet 21 of 39



ICH7 Functional Straps

12/25

307013-003,page76~78,Table 2-23

REQ[4:1]#	XOR Chain selection
GNT2#	The signal has a weak internal pull-up This signal should not be pulled low.
GNT3#	The signal has a weak internal pull-up. Pull-down is Top-Block Swap
LINKALERT#	This signal requies an external pull-up resistor.
SPKR	The signal has a weak internal pull-down. Pull-up is No Reboot
INTVRMEN	Enables integrated VccSus1_05 VRM when sampled high.
GPIO25	The signal has a weak internal pull-up. 1: DMI DC mode , 0 : DMI AC mode
EE_CS	The signal has a weak internal pull-down. This signal should not be pulled high.
GNT5#/GPIO17 GNT4#/GPIO48	Signal have weak internal pull-ups.
EE_DOUT	Boot BIOS Destination Selection The signal has a weak internal pull-up.
ACZ_SDOUT	This signal should not be pulled low. The signal has a weak internal pull-down.
ACZ_SYNC	The signal has a weak internal pull-down.
GPIO16	The signal has a weak internal pull-down. This signal should not be pulled high.
SATALED#	The signal has a weak internal pull-up. This signal should not be pulled low.
TP3	The signal has a weak internal pull-up. Pull-down was using XOR Chain testing.

Variant Name:

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: ICH7 DMI&PCIE&PCI&USB

Size	Document Number	Rev
C	EAGLELAKE	A00

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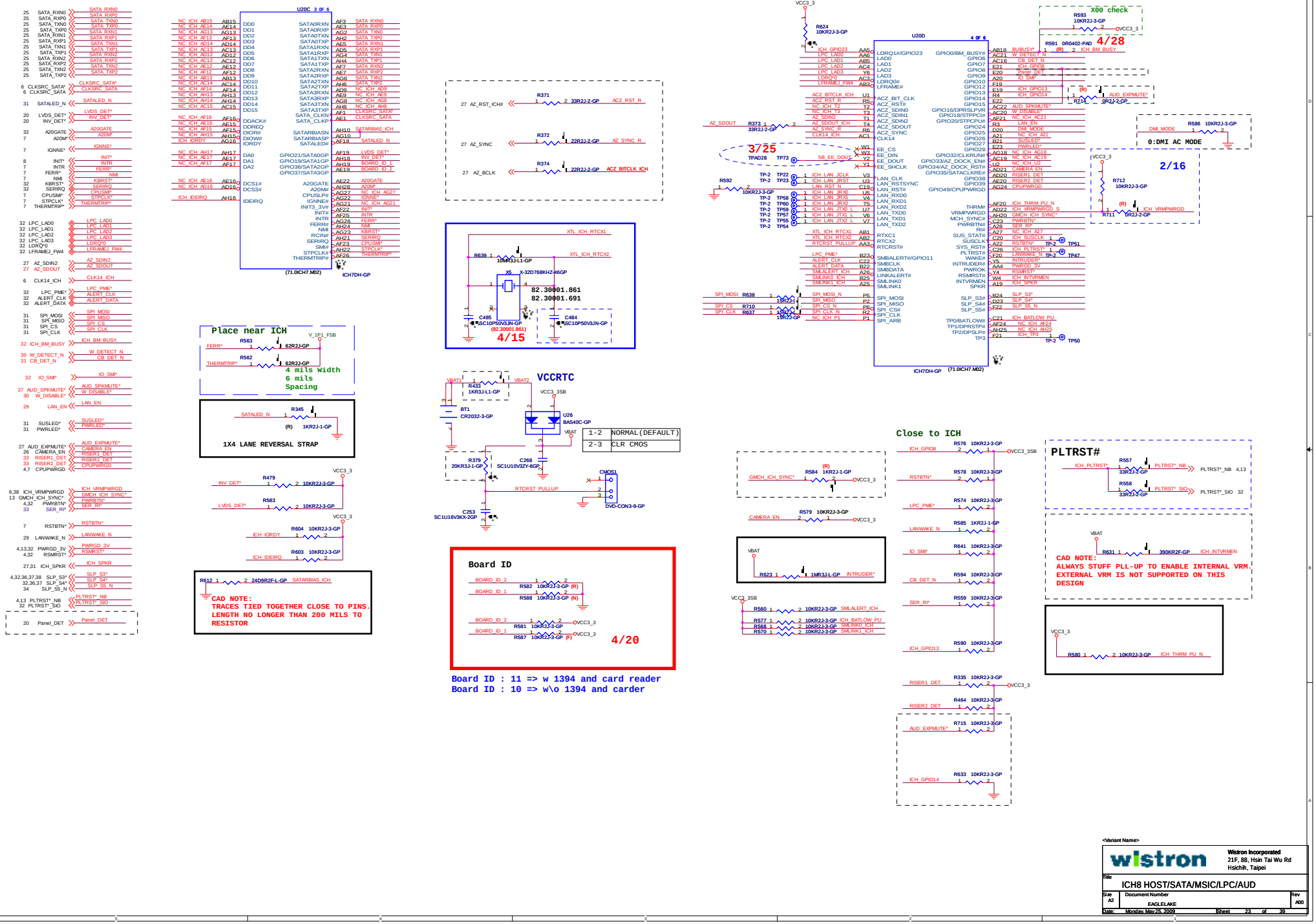
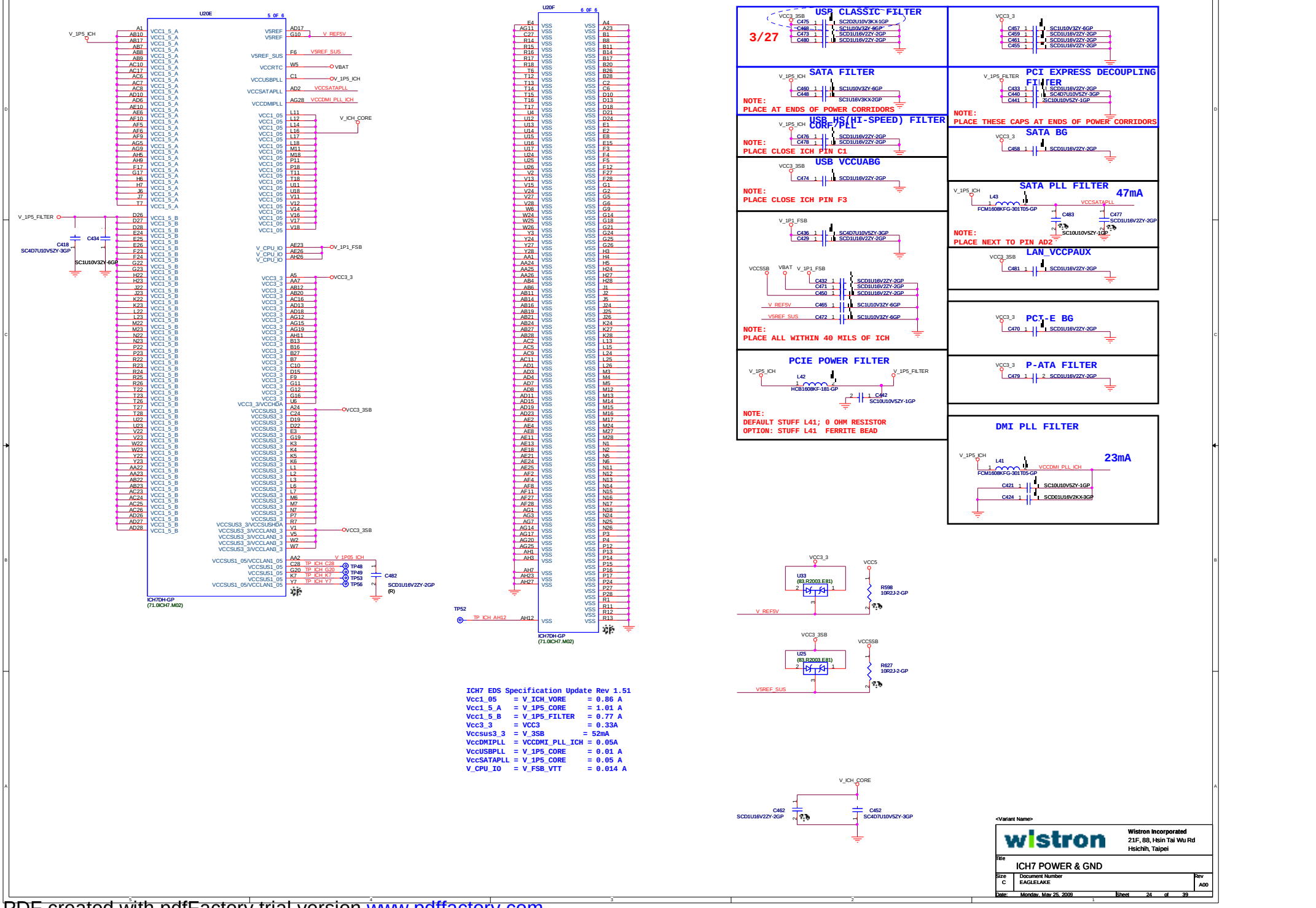
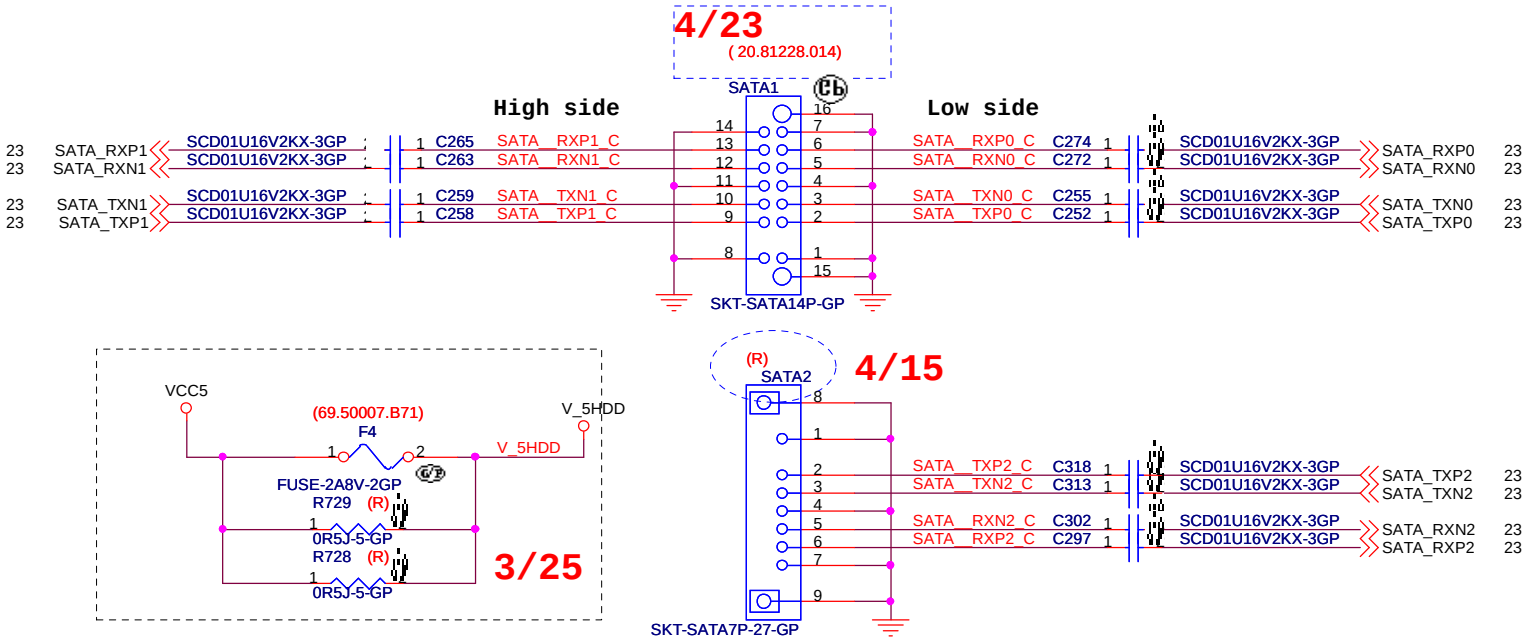


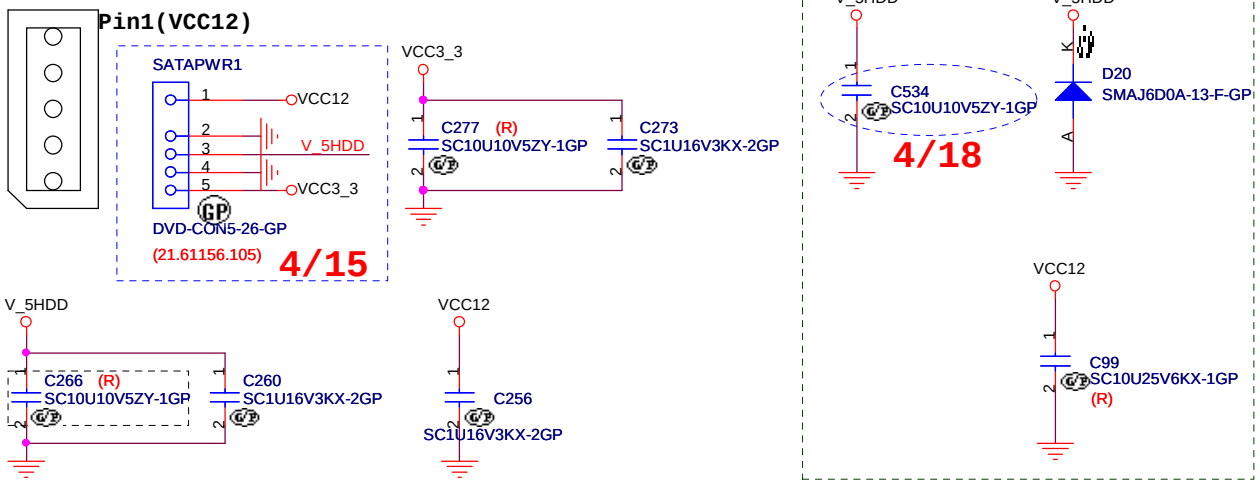


SATA CONNECTORS

SATA 2Port Right angle : 20.81227.014, 20.81228.014



Layout: Please put them together



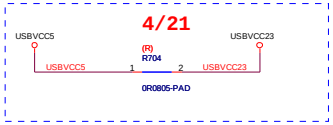
<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

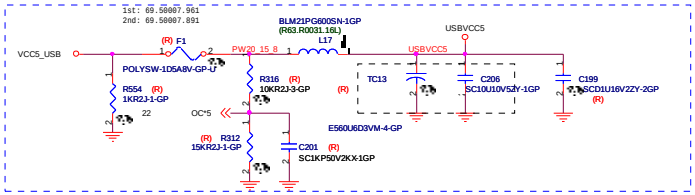
Title	SATA CONN	
Size A4	Document Number EAGLELAKE	Rev A00
Date: Monday, May 25, 2009	Sheet 25 of 39	

Side USB are Port 2, 3, 4,5
Rear USB are Port 6,7
Internal USB, Port 1 for Camera
Internal USB, Port 0 is for Mini PCIE slot

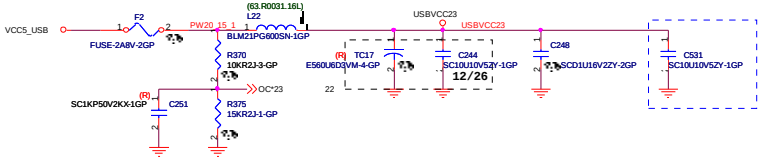


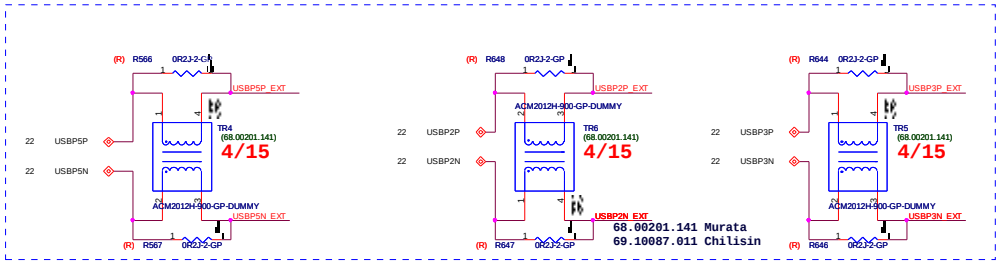
SIDE 2 USB PORT (5)

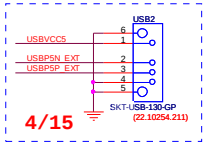
1port USB : 22.10218.N11
2port USB : 22.10218.G71

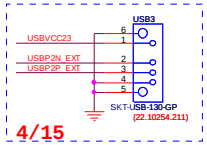


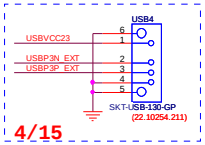
SIDE USB PORT (2/3)



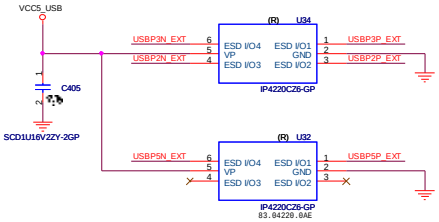




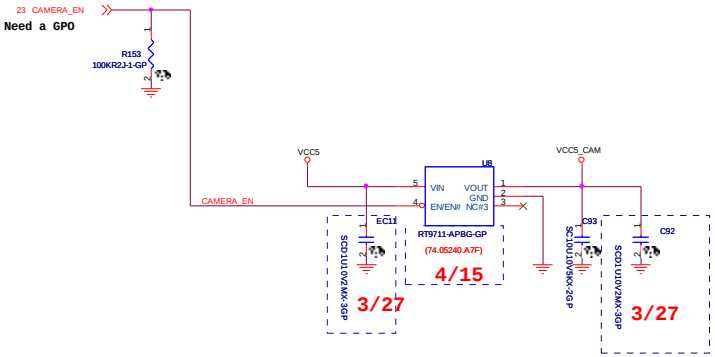




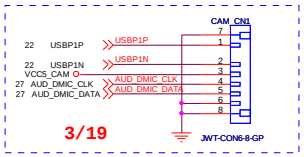
CLOSED TO USB CONNECTOR



INTERNAL USB PORT (1)
for Camera, Digital Mic



Wrong part in X01 ,need to check it



<Variant Name>

wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: USB CONN

Size	Document Number	Rev
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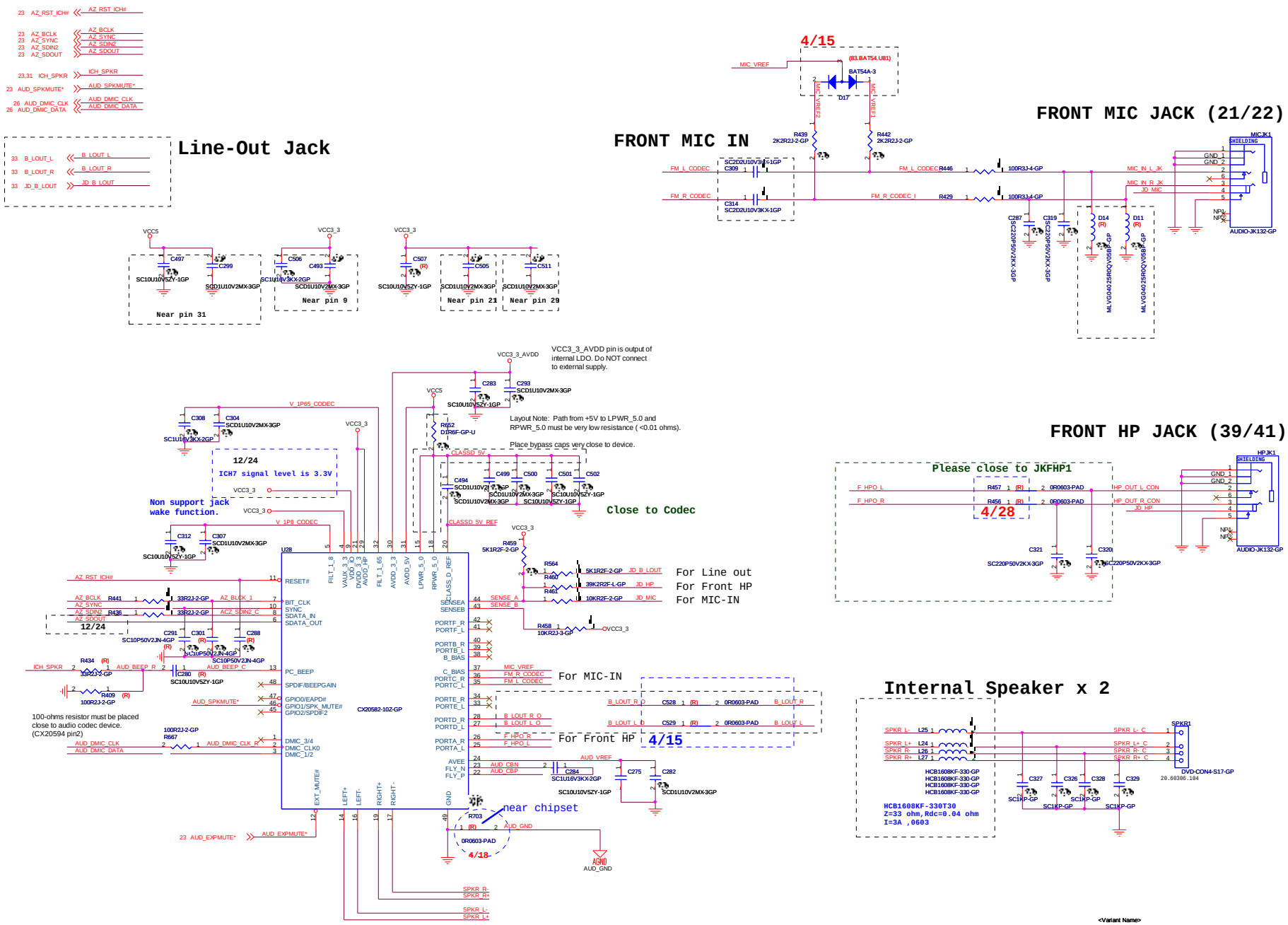
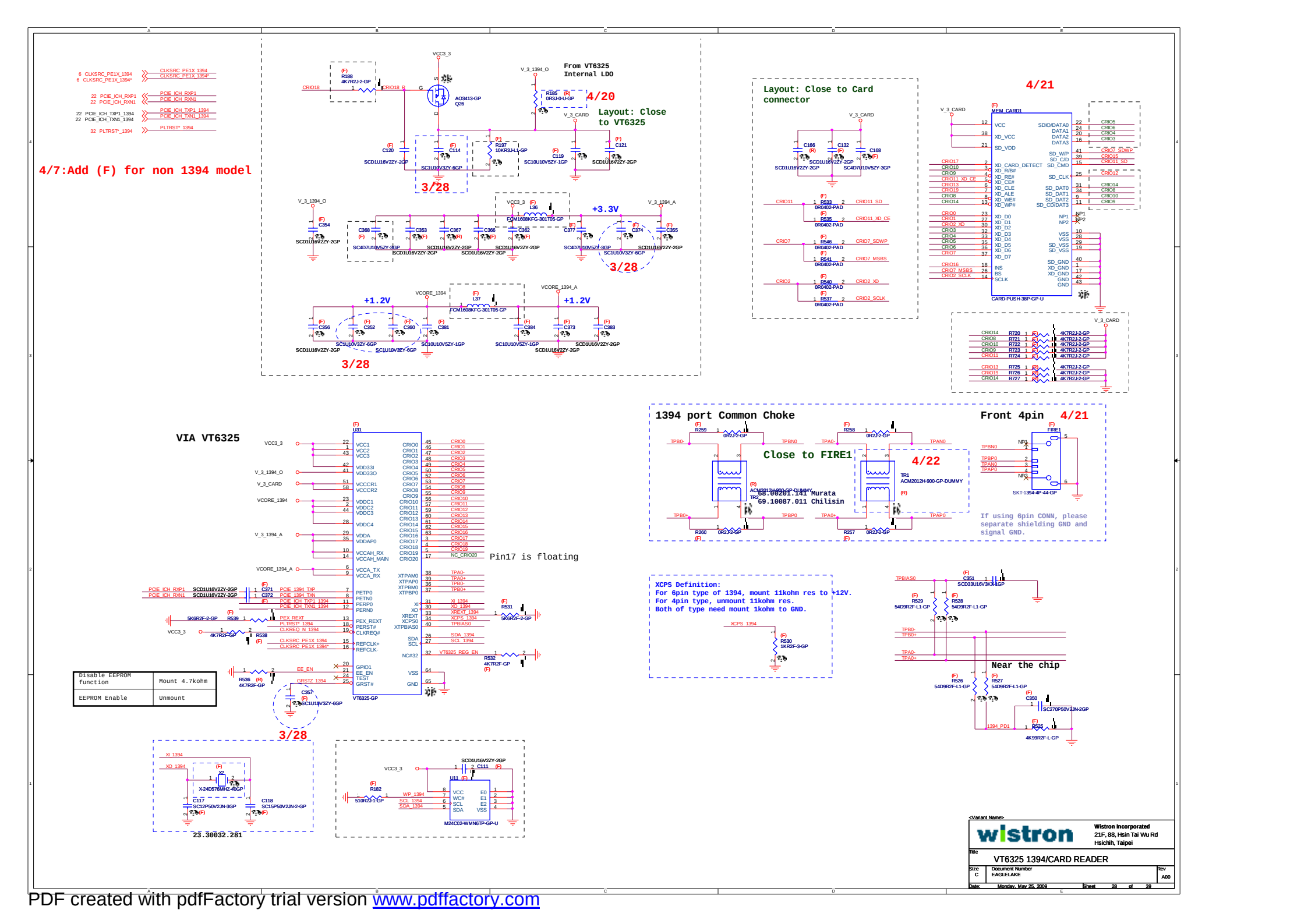
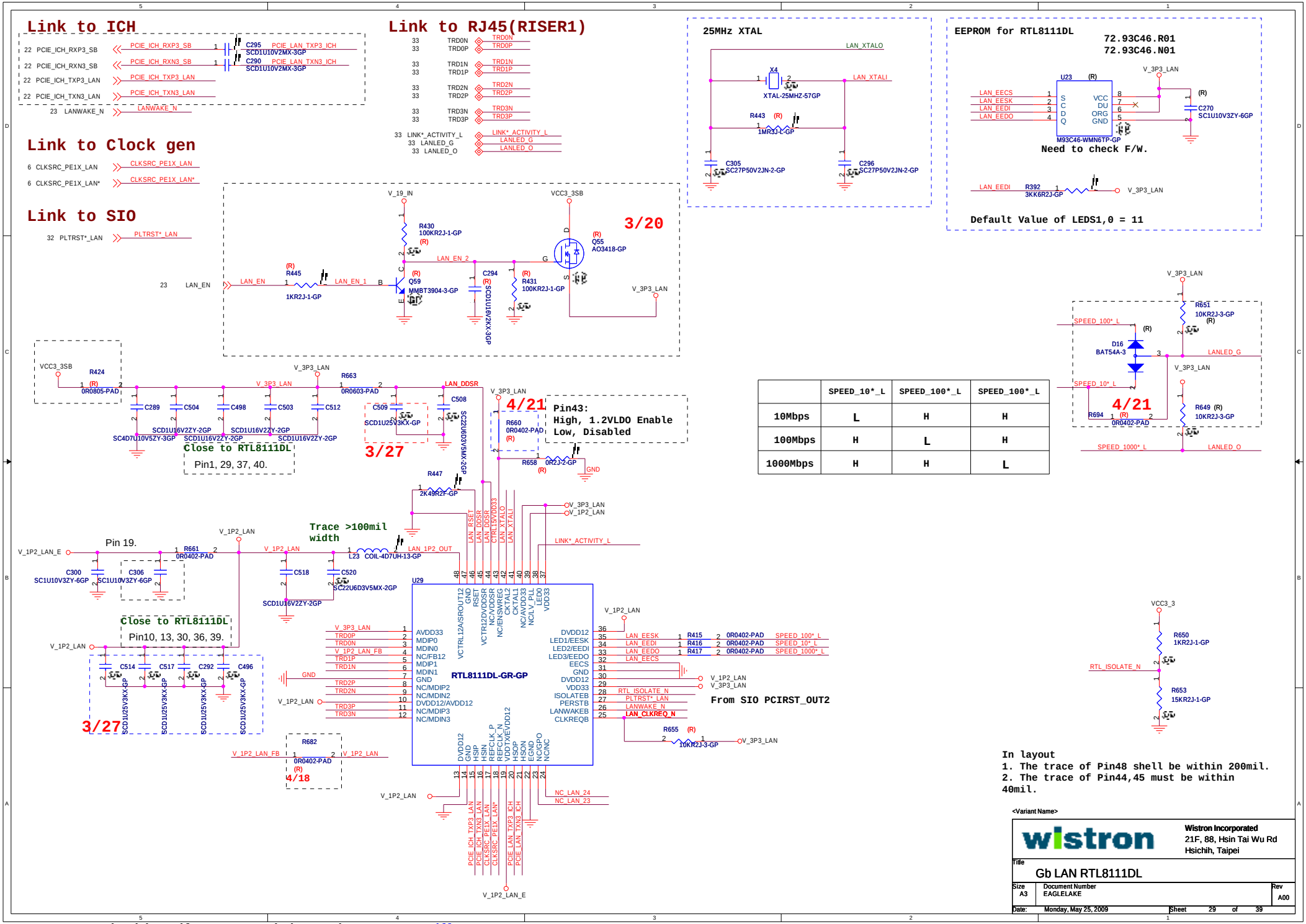
Date: Monday, May 25, 2009 Sheet 26 of 39







	SPEED_10*_L	SPEED_100*_L	SPEED_100*_L
10Mbps	L	H	H
100Mbps	H	L	H
1000Mbps	H	H	L

In layout
1. The trace of Pin48 shell be within 200mil.
2. The trace of Pin44,45 must be within 40mil.

<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Gb LAN RTL8111DL

Size	Document Number	Rev
A3	EAGLELAKE	A00

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Mini PCIE slot 1

INTERNAL USB PORT (0) for Mini PCIE

Please close to MPE1.

V_1P5_ICH

C269 SCD1U16V2ZY-2GP

C286 SCD1U16V2ZY-2GP

C322 SC10U10V5ZY-1GP

Please close to MPE1.

VCC3_3

C495 SCD1U16V2ZY-2GP

C492 SCD1U16V2ZY-2GP

C262 SC10U10V5ZY-1GP

C324 SC10U10V5ZY-1GP

23 W_DISABLE* — W_DISABLE*

23 W_DETECT_N — W_DETECT_N

6 CLKSRC_PE1X_SL1 — CLKSRC_PE1X_SL1

6 CLKSRC_PE1X_SL1* — CLKSRC_PE1X_SL1*

22 PCIE_ICH_RXN2 — PCIE_ICH_RXN2

22 PCIE_ICH_RXP2 — PCIE_ICH_RXP2

22 PCIE_ICH_TXN2_CONN — PCIE_ICH_TXN2_CONN

22 PCIE_ICH_TXP2_CONN — PCIE_ICH_TXP2_CONN

32 PLTRST*_RISER — PLTRST*_RISER

22 USBP0N — USBP0N

22 USBP0P — USBP0P

6,7,17,21,32 SMBCLK — SMBCLK

6,7,17,21,32 SMBDATA — SMBDATA

62.10043.161

MPE1

6	1.5V	REFCLK+	13 CLKSRC_PE1X_SL1
2	3.3V	REFCLK-	11 CLKSRC_PE1X_SL1*
28	+1.5V	PERN0	23 PCIE_ICH_RXN2
48	+1.5V	PERP0	25 PCIE_ICH_RXP2
52	+3.3V	PETN0	31 PCIE_ICH_TXN2_CONN
24	+3.3VAUX	PETP0	33 PCIE_ICH_TXP2_CONN
		USB_D-	36 M_USBP0N — R401 1 (R) 2 0R0402-PAD USBP0N
		USB_D+	38 M_USBP0P — R396 1 (R) 2 0R0402-PAD USBP0P
3	RESERVED#3	SMB_CLK	30 M_SMB_CLK — R413 1 (R) 2 0R2J-2-GP SMBCLK
5	RESERVED#5	SMB_DATA	32 M_SMB_DATA — R402 1 (R) 2 0R2J-2-GP SMBDATA
8	RESERVED#8		
10	RESERVED#10	WAKE#	1 W_WAKE_N — 1 TP-2 TP26
12	RESERVED#12	CLKREQ#	7
14	RESERVED#14	PERST#	22 PLTRST*_RISER — PLTRST*_RISER 32
16	RESERVED#16		
17	RESERVED#17		
19	RESERVED#19		
20	RESERVED#20	GND	4
37	RESERVED#37	GND	9
39	RESERVED#39	GND	15
41	RESERVED#41	GND	18
43	RESERVED#43	GND	21
45	RESERVED#45	GND	26
47	RESERVED#47	GND	27
49	RESERVED#49	GND	29
51	RESERVED#51	GND	34
		GND	35
		GND	40
42	LED_WWAN#	GND	50
44	LED_WLAN#	GND	53
46	LED_WPAN#	GND	54

NP1 NP2

SKT-MINI52P-1-GPU1

VCC3_3

W_DISABLE*

W_DETECT_N

4/21

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: MINI PCIE SLOT

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A4	EAGLELAKE	A00

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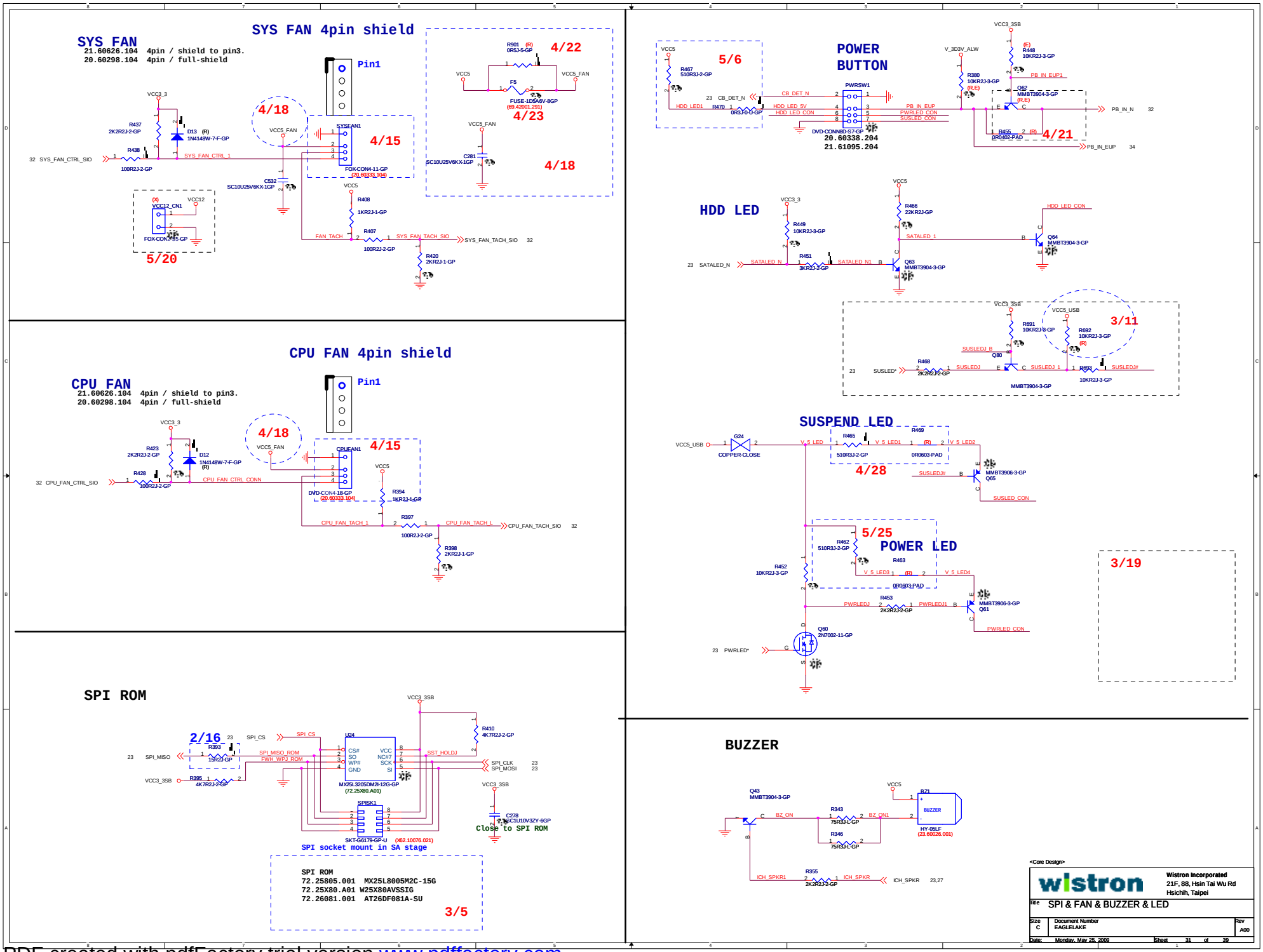

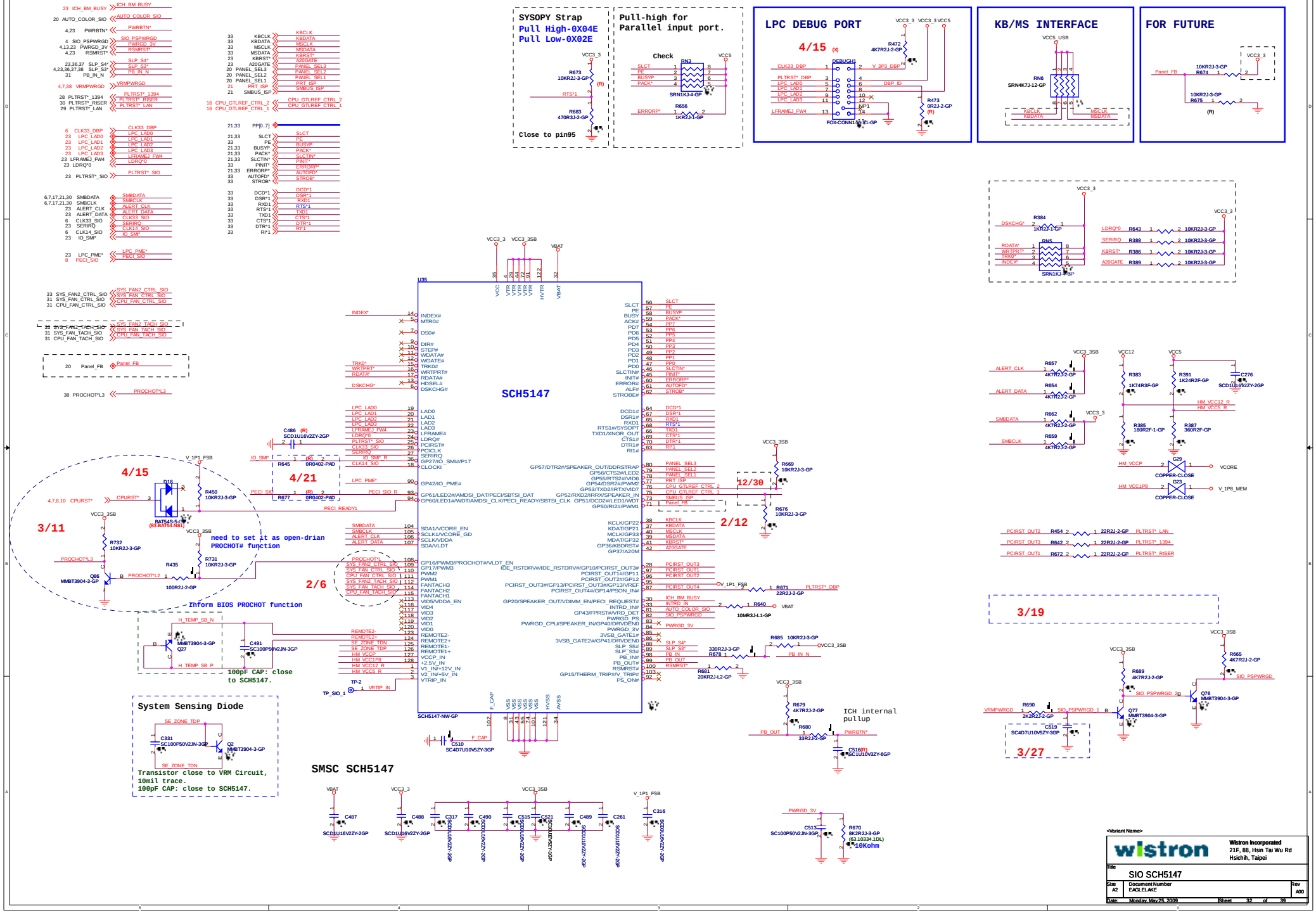

Gb LAN

TRD0N / TRD0P → TRD0N 29 / TRD0P 29
TRD1N / TRD1P → TRD1N 29 / TRD1P 29
TRD2N / TRD2P → TRD2N 29 / TRD2P 29
TRD3N / TRD3P → TRD3N 29 / TRD3P 29
LINK*_ACTIVITY_L → LINK*_ACTIVITY_L 29
LANLED_G → LANLED_G 29
LANLED_O → LANLED_O 29

PARALLEL PORT

32	PINIT*	PINIT*
21,32	SLCTIN*	SLCTIN*
21,32	SLCT	SLCT
32	PE	PE
21,32	BUSYP	BUSYP
21,32	PACK*	PACK*
21,32	ERRORP*	ERRORP*
32	AUTOFD*	AUTOFD*
32	STROB*	STROB*
21,32	PP[0..7]	

32 SYS_FAN2_CTRL_SIO → SYS_FAN2_CTRL_SIO
32 SYS_FAN2_TACH_SIO → SYS_FAN2_TACH_SIO
23 RISER1_DET → RISER1_DET

27 B_LOUT_L → B_LOUT_L
27 B_LOUT_R → B_LOUT_R
27 JD_B_LOUT → JD_B_LOUT

22 USBP4N → USBP4N
22 USBP4P → USBP4P
23 RISER2_DET → RISER2_DET

32 MSDATA → MSDATA
32 MSCLK → MSCLK
32 KBDATA → KBDATA
32 KBCLK → KBCLK

22 USBP6N → USBP6N
22 USBP6P → USBP6P

22 USBP7N → USBP7N
22 USBP7P → USBP7P

RISER1

VCC5_USB	1	2	
	3	4	PP0
MSDATA	5	6	PP1
MSCLK	7	8	PP2
KBDATA	9	10	PP3
KBCLK	11	12	PP4
	13	14	PP5
	15	16	PP6
RCTS*1	17	18	PP7
RDSR*1	19	20	AUTOFD*
RRXD1	21	22	ERRORP*
RDCD*1	23	24	PINIT*
RRI*1	25	26	SLCTIN*
RDTR*1	27	28	SLCT
RRTS*1	29	30	PE
RTXD1	31	32	BUSYP
	33	34	PACK*
SYS_FAN2_CTRL_SIO	35	36	STROB*
SYS_FAN2_TACH_SIO	37	38	VCC5
RISER1_DET	39	40	
		42	

VCC3_3
23 RISER1_DET
Pin1 Pin2 Pin39 Pin40
JWT-CONN40A-GP
20.F1161.040

Pin39 is RISER1_DET

RISER2

V_3P3_LAN	NP1	31	
	16	1	B_LOUT_L
TRD3N	17	2	B_LOUT_R
TRD3P	18	3	AUD_GND
TRD2N	19	4	JD_B_LOUT
TRD2P	20	5	LINK*_ACTIVITY_L
	21	6	LANLED_G
TRD1N	22	7	LANLED_O
TRD1P	23	8	USBP6N
	24	9	USBP6P
TRD0N	25	10	
TRD0P	26	11	USBP7N
RISER2_DET	27	12	USBP7P
USBP4N	28	13	
USBP4P	29	14	USBVCC67
	30	15	
NP2		32	

AGND AUD_GND
23 RISER2_DET
Pin16 Pin1 Pin30 Pin15
JWT-CONN30F-GP
21.D0301.215

Pin30 is RISER2_DET

VCC5_USB → F3 FUSE-2A8V-2GP → USBVCC67
R474 10KR2J-3-GP
22 OC*67
C330 SC1KP50V2KX-1GP
R471 15KR2J-1-GP

VCC5 C325 SC1U10V3ZY-6GP
VCC3_3SB C285 SC1U10V3ZY-6GP
VCC5_USB C323 SC1U10V3ZY-6GP

SERIAL PORT

32	RXD1	RXD1
32	TXD1	TXD1
32	RTS*1	RTS*1
32	CTS*1	CTS*1
32	DTR*1	DTR*1
32	DSR*1	DSR*1
32	DCD*1	DCD*1
32	RI*1	RI*1
23	SER_RI*	SER_RI*

SERIAL PORT

VCC5
C303 SCD047U10V2KX-2GP
C315 SCD33U16V3KX-1GP
COM_B1 COM_B2 COM_B3 COM_B4
U27 MAX3243CAI-GP (74.03243.NF9)
C1+ C1- C2+ C2- T1IN T2IN T3IN R2OUTB R1OUT R2OUT R3OUT R4OUT R5OUT FORCEON FORCEOFF# INVALID# GND
VCC V+ V- T1OUT T2OUT T3OUT R1IN R2IN R3IN R4IN R5IN
DTR*1 RTS*1 TXD1 NC_3243_20 CTS*1 DSR*1 RXD1 DCD*1 RI*1 NC_3243_21
RDTR*1 RRTS*1 RTXD1 RCTS*1 RDSR*1 RRXD1 RDCD*1 RRI*1
C298 SCD1U10V2MX-3GP
C310 SCD33U16V3KX-1GP
C311 SCD33U16V3KX-1GP
COM_B5 COM_B6
3/27

VCC3_3
R421 R427 R422 (R) R432 R419 R426 R414 R403 — 2K2R2J-2-GP
RXD1 TXD1 RTS*1 CTS*1 DTR*1 DSR*1 DCD*1 RI*1
RRI*1
R444 10KR2J-3-GP
RRI*1_SER_B
R440 10KR2J-3-GP
Q58 MMBT3904-3-GP
SER_RI* SER_RI* 23

VCC5 (R) RISER3
SYS_FAN2_CTRL_SIO
SYS_FAN2_TACH_SIO
VCC3_3
DVD-CON5-14-GP
4/23
3/19

<Variant Name>

wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: REAR IO RISER

Size	Document Number	Rev
A3	EAGLELAKE	A00

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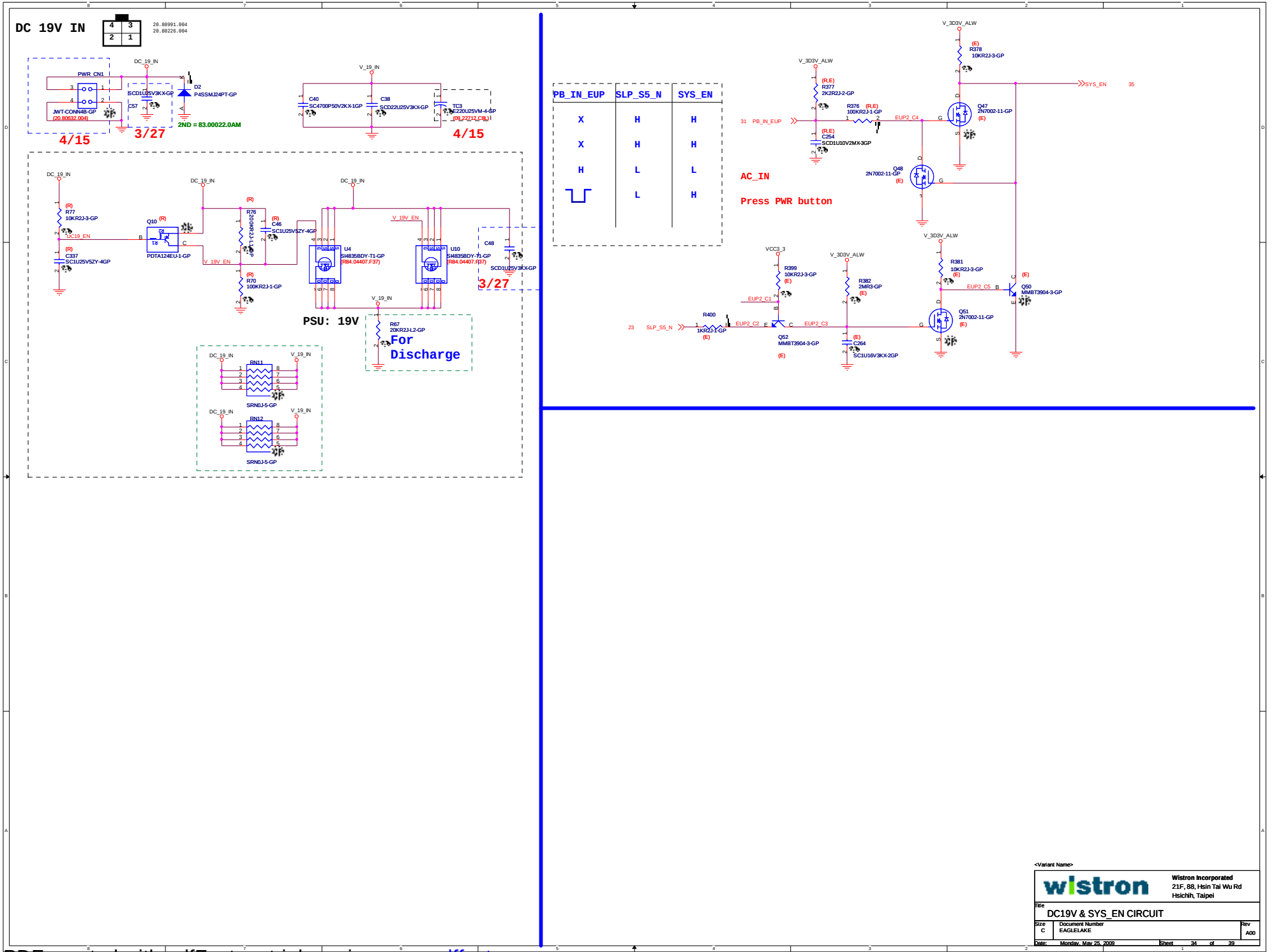
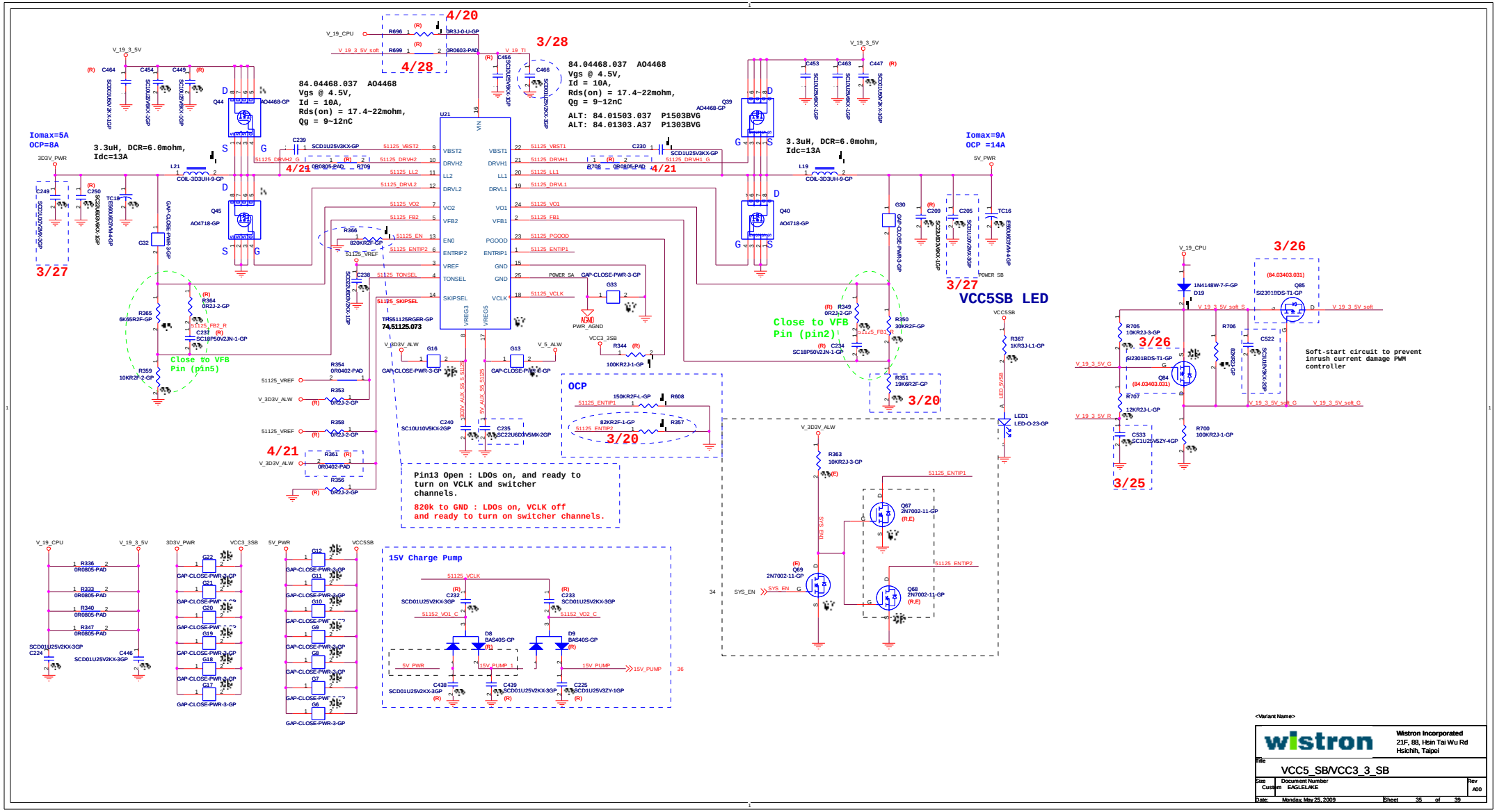
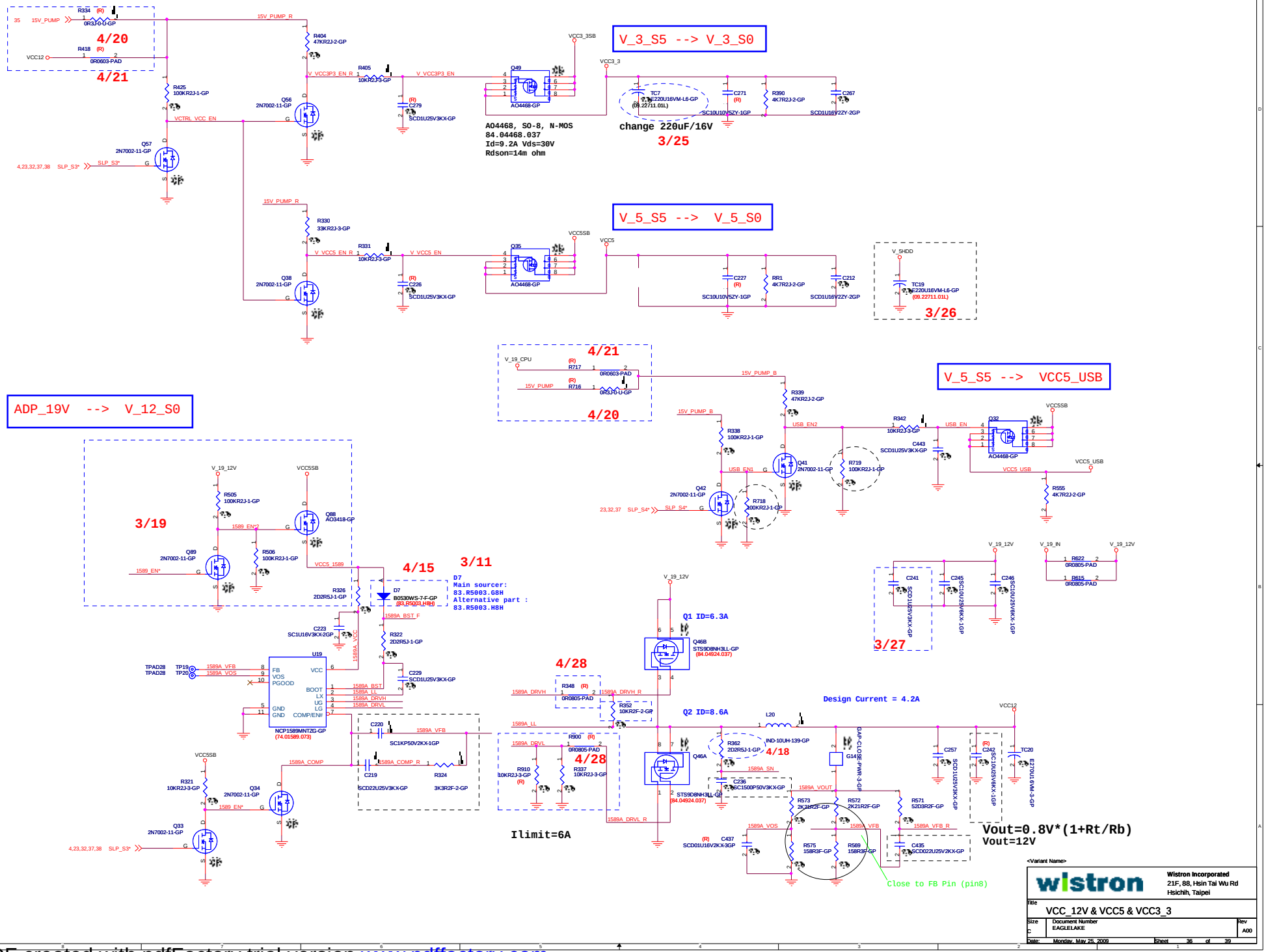
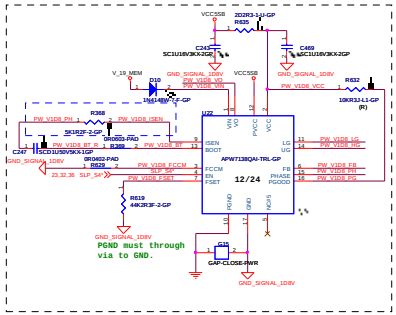


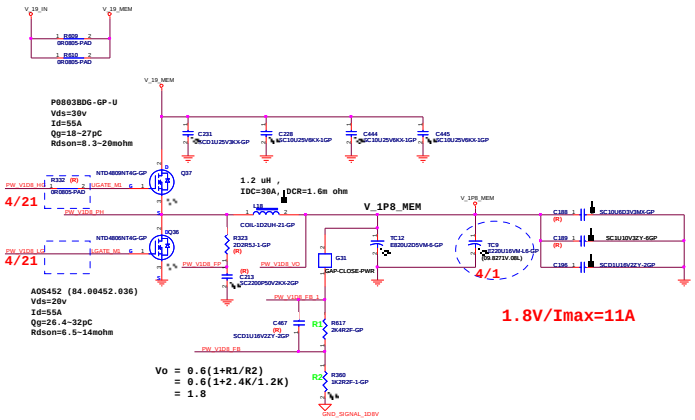




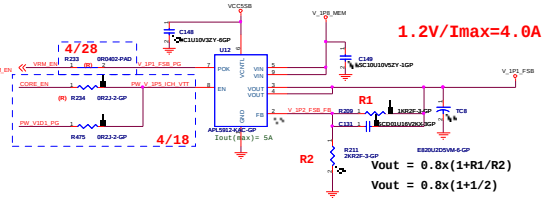
V_19_IN --> V_1P8_MEM



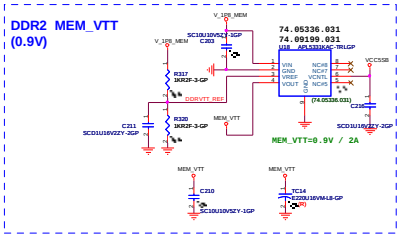
Risen = 5.1k , Rds (on) = 9.4mΩ
OCP = (Ioc * Risen) / Rds(on) = Iocsp
OCP = (26u * 5.1k) / 9.4m = 14.1A



V_FSB_VTT support 65nm Quad-core Processors on Intel 4 series chipset

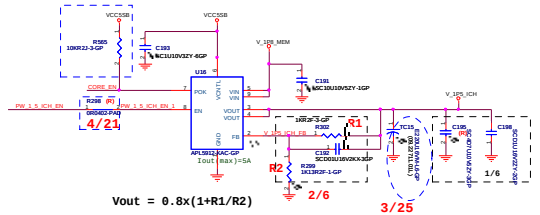


DDR2 MEM_VTT (0.9V)

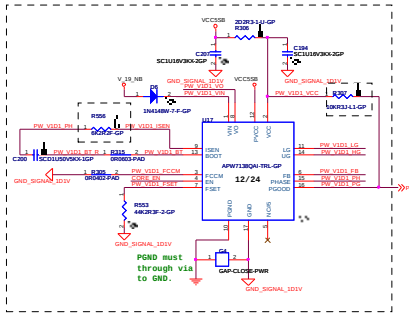


V_1P8_MEM --> V_1P5_ICH

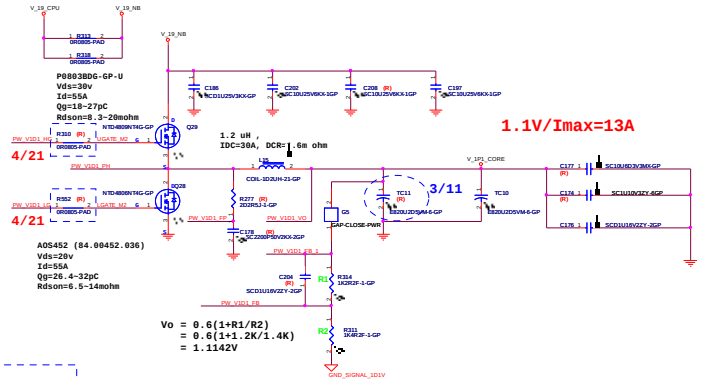
1.5V/Imax=2.8A
2.3A for ICH10,
0.5A for Mini PCIE card.



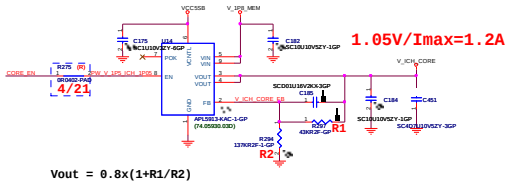
V_19_IN --> V_1P1V

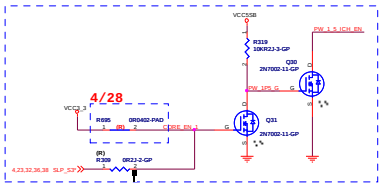


Risen = 6.2k , Rds (on) = 9.4mΩ
OCP = (Ioc * Risen) / Rds(on) = Iocsp
OCP = (26u * 6.2k) / 9.4m = 17.2A



Vout= V_1P05_ICH





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Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
VCC_1_8_DIMM/VCC_1_1_CORE
Size: D
Document Number: EAGLELAKE
Rev: A00
Date: Monday, May 25, 2009
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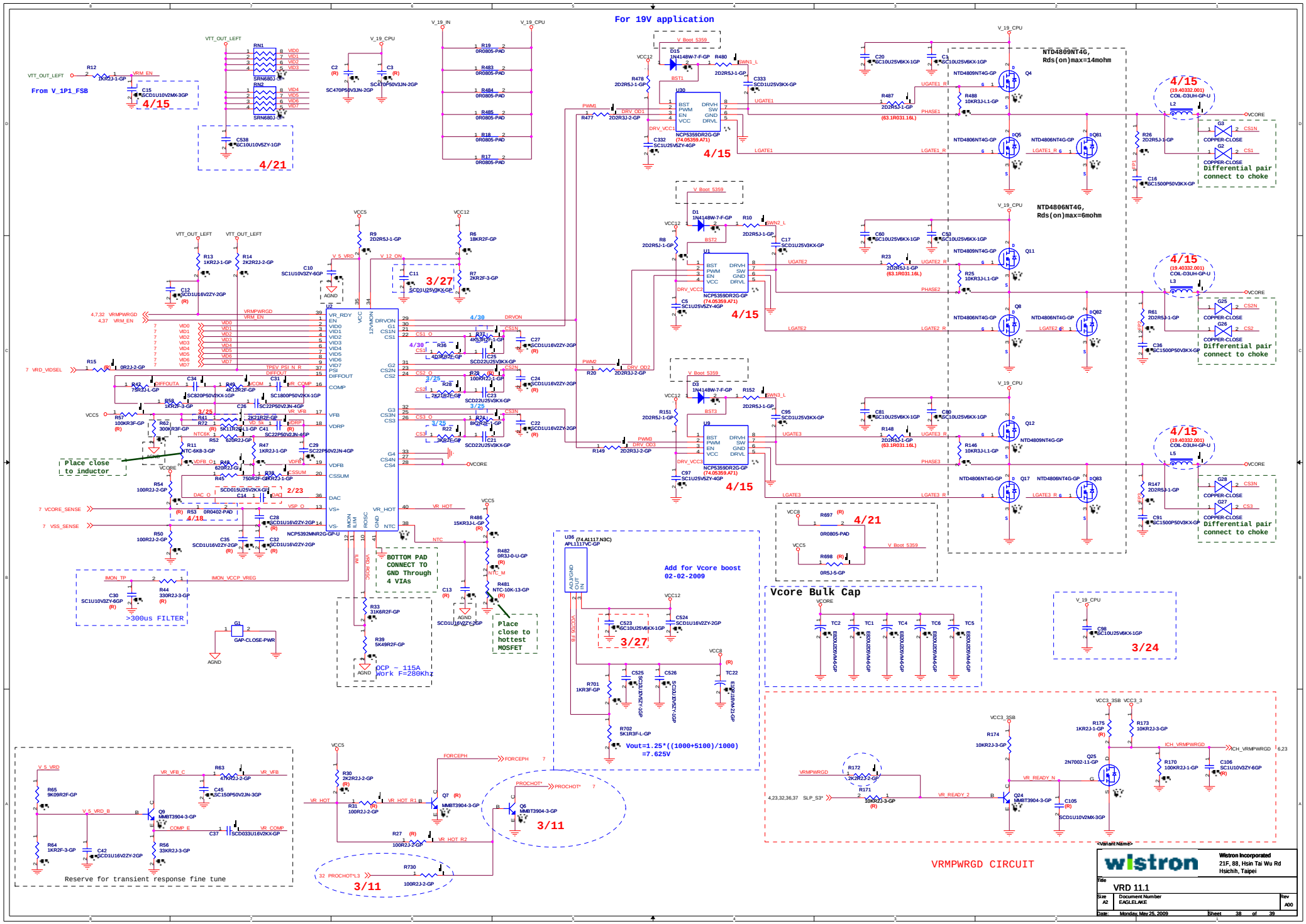
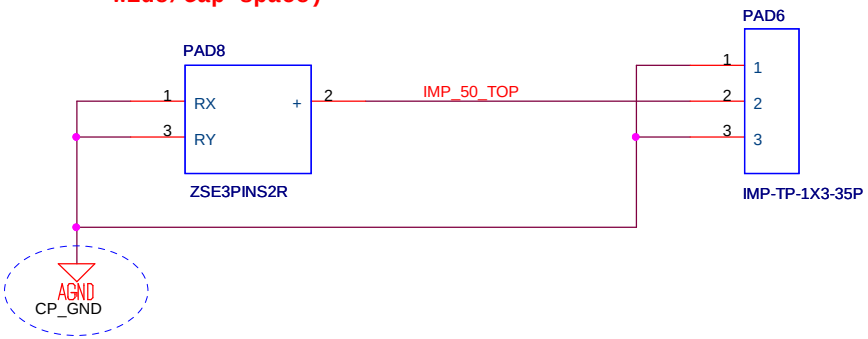


Place these COUPON in V-cut

50 OHM TRACE

The traces rule of TOP and BOT is 4 (Trace wide/Gap space)



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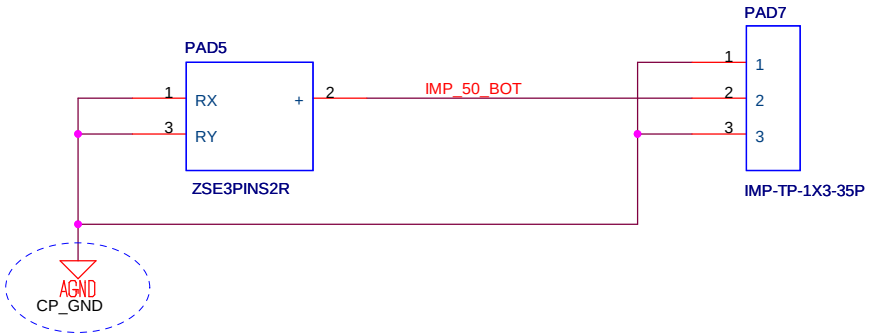

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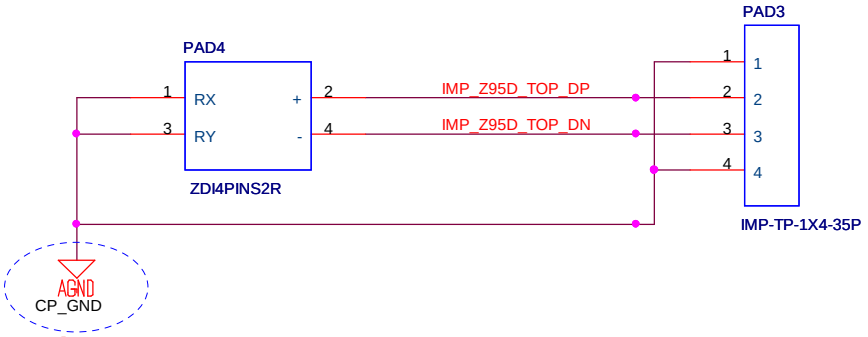
95 OHM TRACE

The traces rule of TOP and BOT is 4/8/4 (Trace wide/Gap space/Trace wide)



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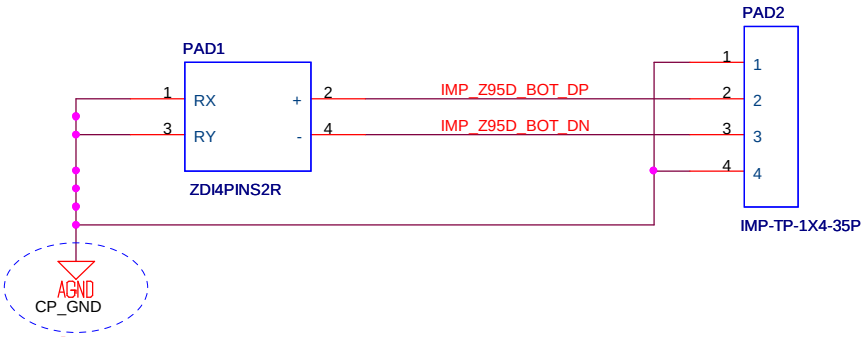

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<Variant Name>

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Title: TEST COUPON		
Size: A4	Document Number: EAGLELAKE	Rev: A00
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