Project Name: PIBTDL/LC AIO
Project Code: 3PD01Z010001
PCB Number : 14060
PCB Size : 150mmx200mm
PCB Name : LC AIO_Intel BT MB

KC.BTD01.29C : Bay Trail-D PENTIUM J2900 4C 2.4G C0
KC.BTD01.19C : Bay Trail-D CELERON J1900 4C 2.0G C0
KC.BTD01.18C : Bay Trail-D CELERON J1800 2C 2.4G C0
KC.29301.BMC : Bay Trail-M CELERON N2930 1.86G

071.00BAY.0C6U : Bay Trail-D PENTIUM J2900 4C 2.4G C0
071.00BAY.0C4U : Bay Trail-D CELERON J1900 4C 2.0G C0
071.00BAY.0C5U : Bay Trail-D CELERON J1800 2C 2.4G C0

XTAL Description

XTAL	Function	Frequency	Spec	Capacitance
X1801	CPU	25M	+/-30ppm CL:12P	C1814=12pF C1815=12pF
X1802	CPU	32.768K	+/-20ppm CL:7P	C1817=4pF C1818=4pF
X3	LAN	25M	+/-30ppm CL:12P	C294=15pF C295=15pF
X3501	HUB	12M	+/-20ppm CL:20P	C4603=18pF C4604=18pF
X5	SCALAR	14.318M	+/-20ppm CL:20P	C532=15pF C533=15pF
X7	GPU	27M	+/-30ppm CL:12P	C738=10pF C734=10pF

BOM Configuration

O_: OCP
O6_: 65W adaptor
O9_: 90W adaptor
R_: Reserve
ECIO_: ITE8732
SIO_: ITE8772
L18_: 18 inch Panel
L19_: 19.5 inch Panel
CMI_: CHIMEI Panel
ODT_:ODT Panel

CMI 19.5"
1.L19_
2.SIO_
3.O_
4.O6_
5.CMI_

ODT 18.5"
1.L18_
2.SIO_
3.O_
4.O6_
5.ODT_

CPU: INTEL BAY TRAIL-D
J2900 - KC.BTD01.29C
J1900 - KC.BTD01.19C
J1800 - KC.BTD01.18C

SIO: IT8732F
BX - 71.08732.00E
CX - 71.08732.A0E
SCALAR: RTD2486
71.02486.D0G
LAN: RTL8111GA
71.08111.Y03
Audio Codec: ALC269Q
71.00269.H03
Amplifier: TAS5707
74.05707.01T
USB3.0 redriver: PS8713
71.08713.003
SATA3.0 redriver: PS8520
71.08520.003
LVDS translator: RTD2136
71.02136.B04

<Variant Name>

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Title: Cover Page
Size: Custom
Document Number: Low Cost AIO
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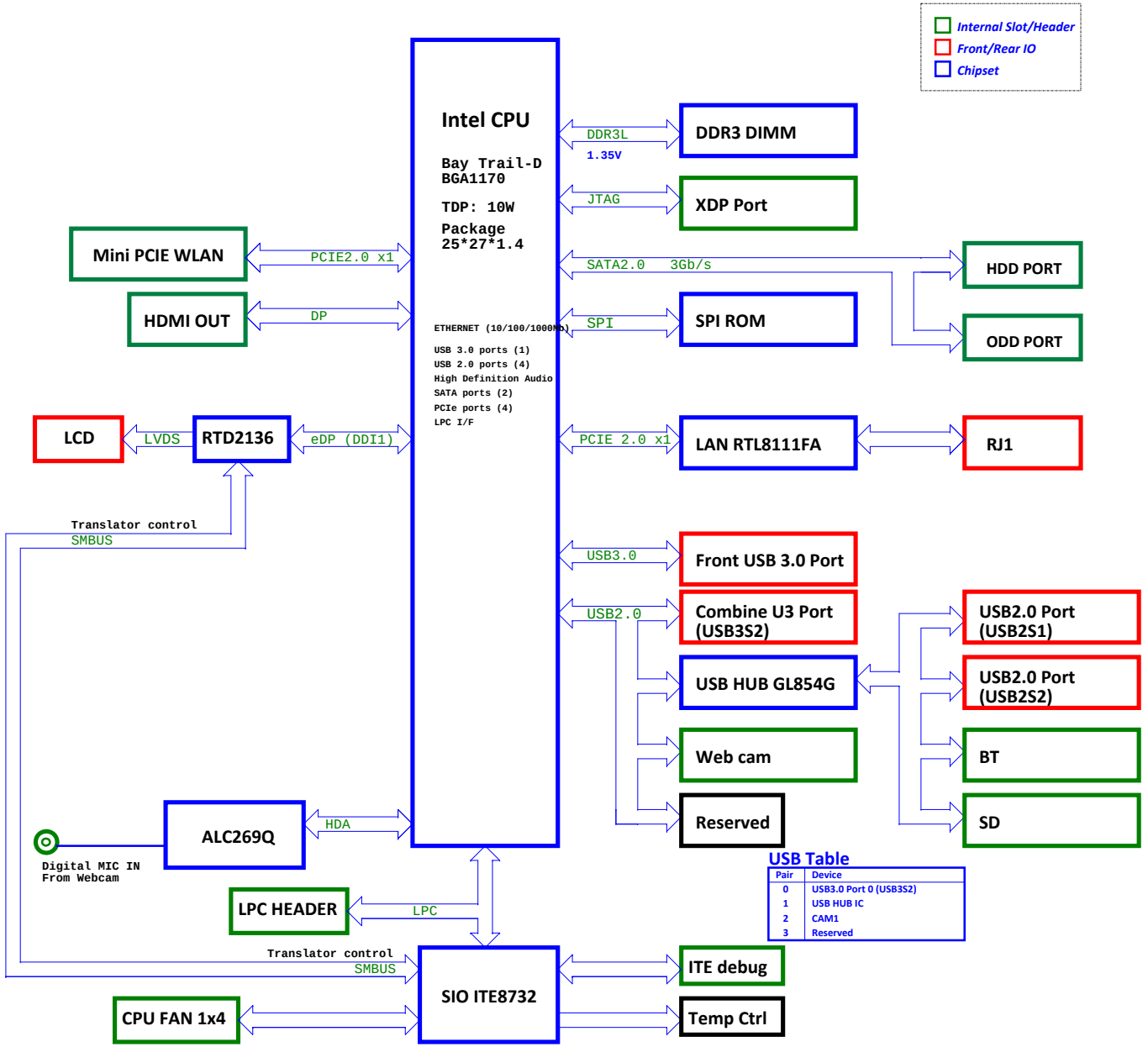
Project Name: PIBTDL/LC AIO
Project Code: 3PD01Z010001
PCB Number : 14060
PCB Size : 150mmx200mm
PCB Name : LC AIO_Intel BT MB



USB Table

Pair	Device
0	USB3.0 Port 0 (USB3S2)
1	USB HUB IC
2	CAM1
3	Reserved

<Variant Name>

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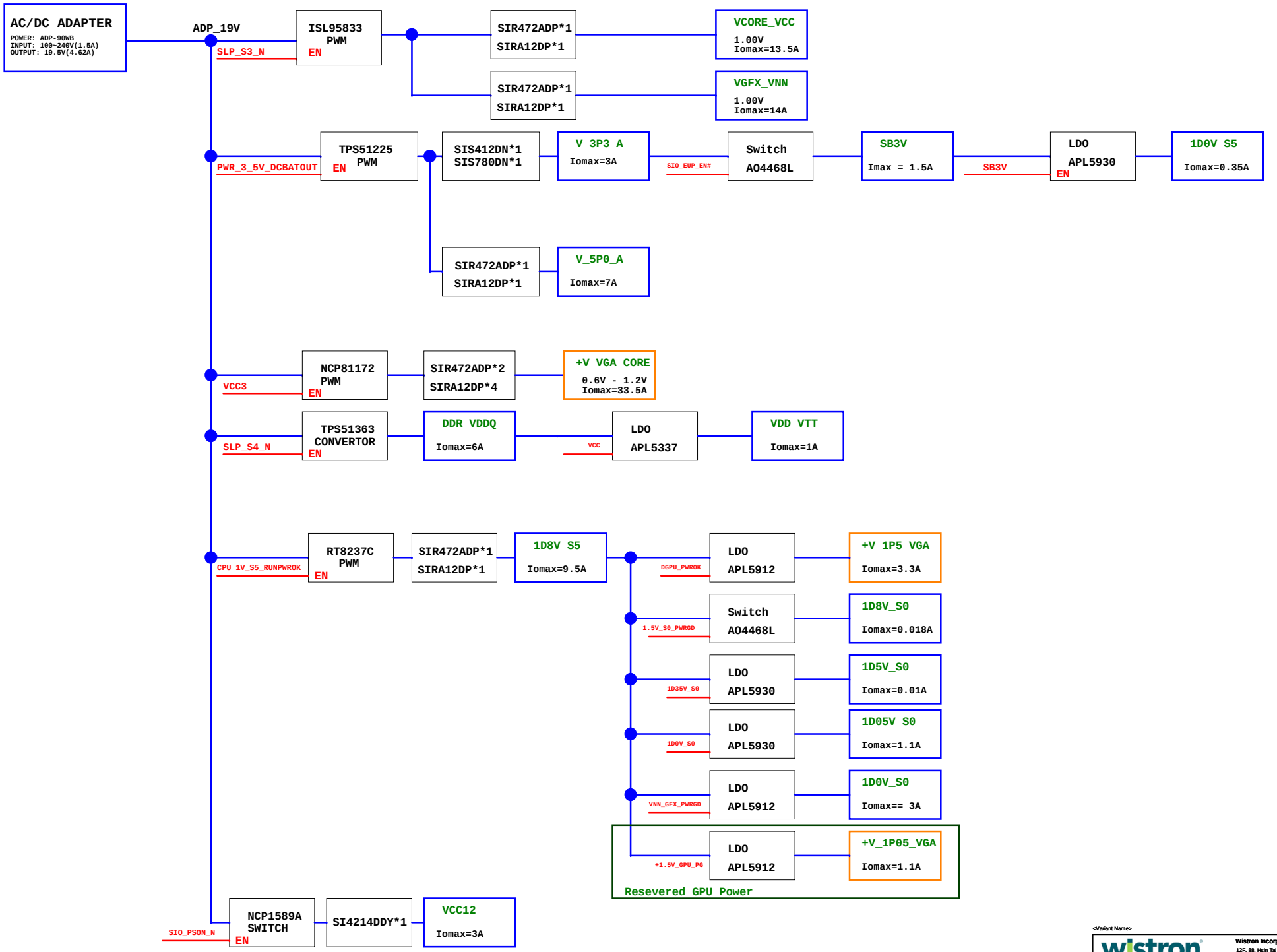
Title: Block Diagram
Size: Custom | Document Number: Low Cost AIO | Rev: 1A
Date: Friday, September 12, 2014 | Sheet 2 of 62



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Title: Power Delivery

Size: Custom | Document Number: Low Cost AIO | Rev: 1A

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Power-up Sequencing for the BAY TRAIL-D Platform

Source	Destination	Signal
RTC Battery	CPU/SIO	RTC_VCC
RTC Battery	CPU/SIO	RTC_TEST# RTC_RST#
Adaptor	MB	DCBATOUT
VRs	CPU/SIO	V_3P3_A
Button	SIO	PWRBTN_N
SIO	VRs	SIO_EUP_EN#
VRs	MB	SB3V/SB5V
VRs	MB	1D0V_S5
VRs	MB	1D8V_S5
SIO	CPU	RSMRST_N
CPU	SIO	PMC_SUSCLK
CPU	MB	PMC_SUSPWRDNACK
SIO	CPU	PMC_PWBTN_N
CPU	SIO / VRs	SLP_S4#
VRs	MB	DDR_VDDQ
MB	CPU	DDR3_DRAM_PWROK
CPU	SIO / VRs	SLP_S3#
SIO	VRs	SIO_PSON#
VRs	MB	VCC12
VRs	CPU	VNN/VCORE
VRs	MB	1D0V_S0
VRs	MB	1D05V_S0
VRs	MB	1D35V_S0
VRs	MB	1D5V_S0
VRs	MB	1D8V_S0
VRs	MB	VCC3/VCC5
VRs	SO-DIMM	V_SM_VTT
SIO	MB	PWRGD_3V
SIO	CPU	PMC_CORE_PWROK
SIO	CPU	DRAM_CORE_PWROK
CPU	MB	PMC_SUS_STAT#
CPU	MB	PMC_PLTRST#

<Variant Name>

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Title: Power Sequence

Size: Custom | Document Number: Low Cost AIO | Rev: 1A

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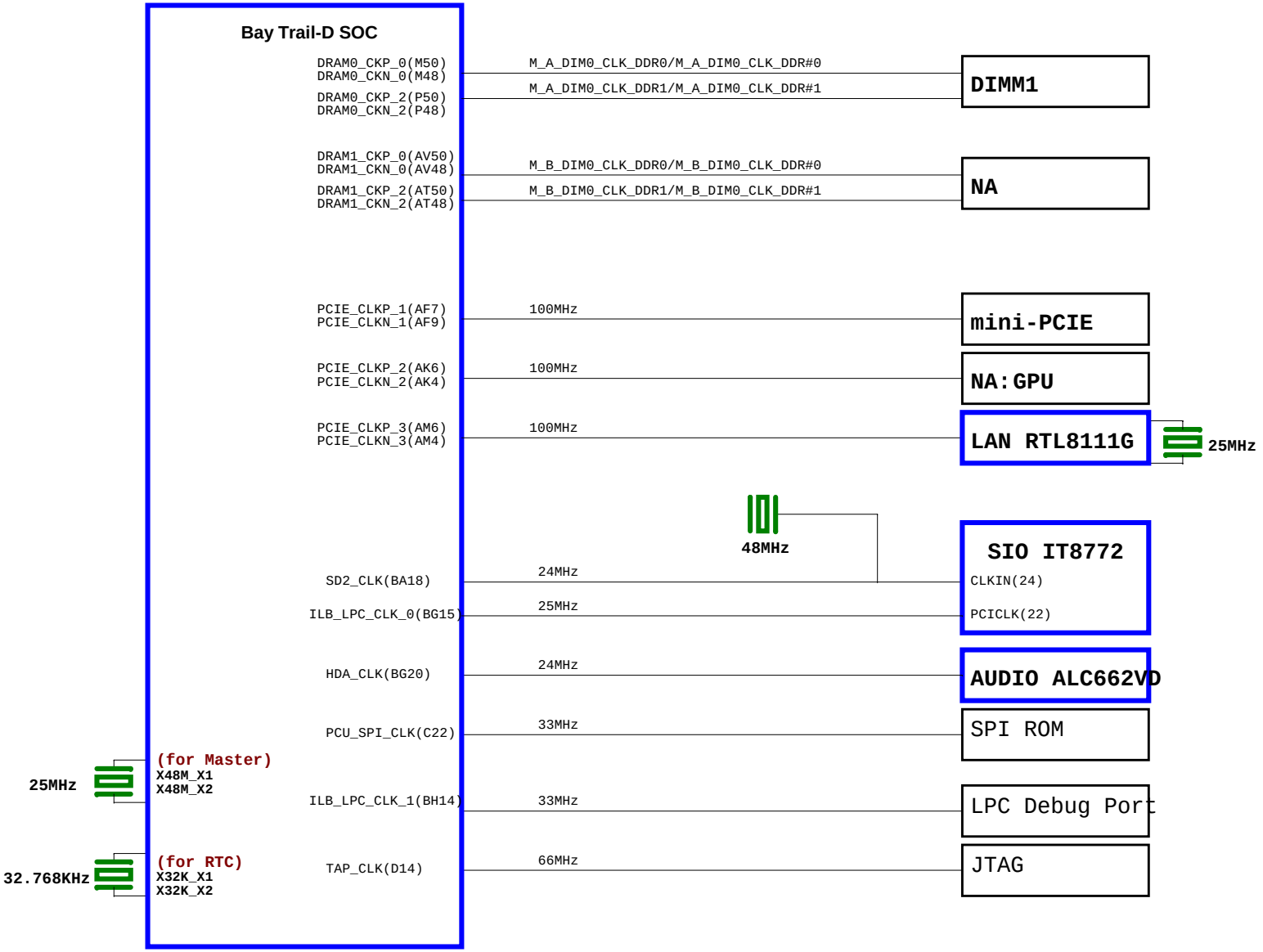

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Title: Clock Map

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Dallas GPIO Table
Version: 2012/11/27

IC Pin Name	Power Well	Default	Default State	Signal Name	Usage	BIOS Programming					Comment
						S0	S1	S3	S4	S5	
GENINT1_L/GPIO32	VDD_33	null	Input, 15K PU	no use	no use						
GENINT2_L/GPIO33	VDD_33	null	Input, 15K PU	no use	no use						
SCL0/GPIO43	VDD_33	null	Input	SMB0_CLK	SMBUS0	Native	Native	Native	Native	Native	2.2K to 3D3V_S0
SD_LED/GPIO45	VDD_33	null	Output	no use	no use						
SDA0/GPIO47	VDD_33	null	Input	SMB0_DATA	SMBUS0	Native	Native	Native	Native	Native	2.2K to 3D3V_S0
SERIRQ/GPIO48	VDD_33	SERIRQ	Input, 15K PU	SERIRQ_N	SERIRQ	Native	Native	Native	Native	Native	10k(R) to 3D3V_S0
GPIO49	VDD_33	GPIO49	Input	no use	no use						
GPIO50	VDD_33	GPIO50	Input, 15K PU	KEY0_TEST	BTN test	GPI	GPI	GPI	GPI	GPI	1K to 3D3V_S0
GPIO51	VDD_33	GPIO51	Input	TP51	no use						
FANOUT0/GPIO52	VDD_33	null	Output, 15K PU	no use	no use						
DEVSLP[0]/GPIO55	VDD_33	GPIO55	Input, 15K PU	TP29	no use						
FANIN0/GPIO56	VDD_33	null	Input, 15K PU	no use	no use						
GPIO57	VDD_33	GPIO57	Input, 15K PU	TP48	no use						
GPIO58	VDD_33	GPIO58	Input, 15K PU	TP49	no use						
DEVSLP[1]/GPIO59	VDD_33	GPIO59	Input, 15K PU	PANEL_OFF_R	panel ON/OFF	GPI	GPI	GPI	GPI	GPI	EC: 10K to 3D3V_A scalar: 10K to P3P3V
CLK_REQ0_L/ SATA_ISO_L/ SATA_ZP0_L/GPIO60	VDD_33	null	Input, 15K PU	BLANCLK_REQ_N_1	clock request (Reserved)						10k(R) to 3D3V_S0
CLK_REQ1_L/GPIO61	VDD_33	null	Input, 15K PU	CLK_PCIE_WLAN_REQ#	clock request (Reserved)						
CLK_REQ2_L/GPIO62	VDD_33	null	Input, 15K PU	no use	no use						
CLK_REQ3_L/ SATA_IS1_L/ SATA_ZP1_L/GPIO63	VDD_33	null	Input, 15K PU	no use	no use						
GPIO64	VDD_33	GPIO64	Input, 15K PU	SMBUS_ISP	scalar FW	GPO L	GPO L	GPO L	GPO L	GPO L	100k to GND controlled by SW tool
CLK_REQG_L/GPIO65/ OSCIN	VDD_33	null	Input, 15K PU	PEG_CLKREQ#	clock request (Reserved)						
SPKR/GPIO66	VDD_33	SPKR	Output	SPKR	beep	Native	Native	Native	Native	Native	
SATA_ACT_L/GPIO67	VDD_33	SATA_ACT_L	Output	no use	no use						
GPIO68	VDD_33	GPIO68	Input, 15K PU	SYS_ID2	SYS ID	GPI	GPI	GPI	GPI	GPI	
GPIO69	VDD_33	GPIO69	Input, 15K PU	SYS_ID3	SYS ID	GPI	GPI	GPI	GPI	GPI	
GPIO70	VDD_33	GPIO70	Input, 15K PU	APU_PROCHOT#_R	thermal (Reserved)						1K to 3D3V_S0
GPIO71	VDD_33	GPIO71	Input	SYS_ID1	SYS ID	GPI	GPI	GPI	GPI	GPI	
SD_CLK/SCLK_2/ GPIO73	VDD_33	null	Input, 50K PU	no use	no use						
SD_CMD/GPIO74	VDD_33	null	Input, 50K PU	no use	no use						
SD_CD/GPIO75	VDD_33	null	Input, 50K PU	no use	no use						
SD_WP/GPIO76	VDD_33	null	Input, 50K PU	no use	no use						
SD_DATA0/ SDATI_2/ GPIO77	VDD_33	null	Input, 50K PU	no use	no use						
SD_DATA1/ SDATO_2/ GPIO78	VDD_33	null	Input, 50K PU	no use	no use						
SD_DATA2/GPIO79	VDD_33	null	Input, 50K PU	no use	no use						
SD_DATA3/GPIO80	VDD_33	null	Input, 50K PU	no use	no use						
SPI_WP_L/GPIO161	VDD_33_ALW	SPI_WP_L	Input	ROM_RST#	SPI	Native	Native	Native	Native	Native	10k to 3D3V_S5
SPI_CLK/GPIO162	VDD _33	SPI_CLK	Input, 15K PD	SPI_CLK	SPI	Native	Native	Native	Native	Native	
SPI_DO/GPIO163	VDD_33_ALW	SPI _ DO	Input, 15K PD	SPI_DATAOUT	SPI	Native	Native	Native	Native	Native	
SPI_DI/GPIO164	VDD_33_ALW	SPI _ DI	Input, 15K PD	SPI_DATAIN	SPI	Native	Native	Native	Native	Native	
SPI_CS1_L/GPIO165	VDD _33	SPI _ CS 1_ L	Input, 15K PU	SPI_CS0_N	SPI	Native	Native	Native	Native	Native	10k to 3D3V_S5
SPI_CS2_L/GPIO166	VDD _33	SPI _ CS 2_ L	Input, 15K PU	EDID_RDY	EDID for APU	GPI	GPI	GPI	GPI	GPI	10k to 3D3V_S5
AZ_SDIN0/GPIO167	VDD_33_ALW	AZ	Input, 13.6K PD	AZ_SDIN0	AZ	Native	Native	Native	Native	Native	10k(R) to GND
AZ_SDIN1/GPIO168	VDD_33_ALW	AZ	Input, 13.6K PD	AZ_SDIN1	AZ	Native	Native	Native	Native	Native	10k(R) to GND
AZ_SDIN2/GPIO169	VDD_33_ALW	AZ	Input, 13.6K PD	AZ_SDIN2	AZ	Native	Native	Native	Native	Native	10k(R) to GND
AZ_SDIN3/GPIO170	VDD_33_ALW	AZ	Input, 13.6K PD	AZ_SDIN3	AZ	Native	Native	Native	Native	Native	10k(R) to GND
GPIO174	VDD_33_ALW	GPIO 174	Input	Wake#_PCIE	wake up	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 3D3V_S5
IR_LED_L/LLB_L/GPIO184	VDD_33_ALW	null	Input, 15K PU	Wake#_LOM	wake up	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 3D3V_S5
SCL1/GPIO227	VDD_33_ALW	null	Input	SMB1_CLK	SMBUS1	Native	Native	Native	Native	Native	2.2K to 3D3V_S5
SDA1/GPIO228	VDD_33_ALW	null	Input	SMB1_DATA	SMBUS1	Native	Native	Native	Native	Native	2.2K to 3D3V_S5
GA20IN/GEVENT0#	VDD_33	GA 20 IN	Input, 15K PU	KA20GATE	GA20IN	Native	Native	Native	Native	Native	10k(R) to 3D3V_S0
GEVENT2#	VDD_33_ALW	null	Input, 15K PU	SPI_SW	only strapping						strap low
LPC_PME#/ GEVENT3#	VDD_33_ALW	null	Input, 15K PU	PME#_M	LPC	Native	Native	Native	Native	Native	2.2k(R) to 3D3V_S5
GEVENT4#	VDD_33_ALW	null	Input	THERMAL_SHUT#	thermal (Reserved)						10k(R) to 3D3V_S5
LPC_PD#/ GEVENT5#	VDD_33_ALW	null	Output	TP_LPC_PD#	no use						
IR_TX1/ GEVENT6#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
GEVENT7#	VDD_33_ALW	null	Input	EC_SMI#	(Reserved)						10k to 3D3V_S5
WAKE#/ GEVENT8#	VDD_33_ALW	null	Input, 15K PU	PCIE_WAKE#	wake up	Native	Native	Native	Native	Native	10k to 3D3V_S5
SPI_HOLD#/ GEVENT9#	VDD_33_ALW	Strap	Input	SST_HOLDJ_1_R	SPI	Native	Native	Native	Native	Native	10k to 3D3V_S5
GEVENT10#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
GEVENT11#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
USB_OC0#/ SPI_TPM_CS#/ TRST#/ GEVENT12#	VDD_33_ALW	USB_OC0#	Input, 15K PU	USB_OC_01	USB OCP	Native	Native	Native	Native	Native	10k to 3D3V_S5
USB_OC1#/TDI/ GEVENT13#	VDD_33_ALW	null	Input, 15K PU	USB_OC_23	USB OCP	Native	Native	Native	Native	Native	10k to 3D3V_S5
USB_OC2#/TCK/ GEVENT14#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
USB_OC3#/TDO/ GEVENT15#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
AC_PRES/IR_RX0/ GEVENT16#	VDD_33_ALW	null	Input, 15K PU	AC_PRES	no use						
GEVENT17#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
BLINK/ GEVENT18#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
SYS_RESET#/ GEVENT19#	VDD_33_ALW	SYS_RESET_L	Input, 15K PU	FP_RST_N	no use						
IR_RX1/ GEVENT20#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
IR_TX0/ GEVENT21#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
GEVENT22#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
LPC_SMI#/ GEVENT23#	VDD_33_ALW	null	Input, 15K PU	no use	no use						

IC Pin Name	Power Well (GPIO)	Default	Default State	Signal Name	Usage	Open Drain / Push Pull	BIOS Programming					Comment
							S0	S1	S3	S4	S5	
PCIRST3#/GP10	3VSB	PCIRST3#	Native	AMP_PDN#	mute	DO/DIOD	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 3D3V_A controlled by EC H: ON, L: OFF/mute
PCIRST2#/GP11	3VSB	PCIRST2#	Native	PCIRST2#	RESET	DO/DIOD	Native	Native	Native	Native	Native	10k(R) to 3D3V_A
PCIRST1#/GP12	3VSB	PCIRST1#	Native	PCIRST1#	RESET	DO/DIOD	Native	Native	Native	Native	Native	10k(R) to 3D3V_A
PWROK1/GP13	3VSB	PWROK1	Native	PWROK3_1	PWROK	DOD/DIOD	Native	Native	Native	Native	Native	1k to 3D3V_S0 set delay to 200ms
VCORE_EN/PCH_C1/GP14	3VSB	VCORE_EN	Native	LAN_PWR_EN	LAN power (reserved)	DOD/DIOD/DIOD	GPO H	GPO H	GPO H	GPO H	GPO H	390k to 3D3V_S5
PCIRSTIN#/CIRTX2/GP15/CPU_PG	3VSB	CIRTX2	Native	SIO_PCIRSTIN#	RESET	DI/DOD/DIOD/DOD	Native	Native	Native	Native	Native	10k to 3D3V_A
5VSB_CTRL#/ CIRRX2/GP16	3VSB	5VSB_CTRL#	Native	EC_EUP	EUP	DOD/DI/DIOD	Native	Native	Native	Native	Native	10k to 3D3V_A
RI2#/GP17	3VSB	null		SPI_WP_R_N	SPI WP	DI/DIOD	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 3D3V_A H: can be write L: write protect
CTS2#/GP20	3VSB	GP20		PANEL_SW_EC	panel ON/OFF	DI/DIOD	GPI	GPI	GPI	GPI	GPI	10k to 3D3V_A controlled by EC
DCD2#/GP21	3VSB	GP21		PANEL_CTRL	panel ctrl (reserved)	DI/DIOD	GPI	GPI	GPI	GPI	GPI	10k to 3D3V_A controlled by EC
SCK/GP22	3VSB	GP22		SIO_SCK_R	EC EPROM	DO/DIOD	Native	Native	Native	Native	Native	1k to 3D3V_A
SI/GP23	3VSB	GP23		SIO_SI	EC EPROM	DO/DIOD	Native	Native	Native	Native	Native	1k to 3D3V_A
RTS2#/GP24	3VSB	GP24		THERMAL_SHUT#_SIO	thermal (reserved)	DO/DIOD	GPO H	GPO H	GPO H	GPO H	GPO H	10k(R) to 3D3V_S5
DSR2#/GP25	3VSB	GP25		SIO_Audio_Mute	mute (reserved)	DI/DIOD	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 3D3V_A
SOUT2/GP26	3VSB	GP26		SIO_UART1_TX	UART	DO/DIOD	Native	Native	Native	Native	Native	10k to 3D3V_A
SIN2/GP27	3VSB	GP27		SIO_UART1_RX	UART	DI/DIOD	Native	Native	Native	Native	Native	10k to 3D3V_A
ATXPG/GP30	3VSB	ATXPG	Native	SIO_ATXPG	sequence	DI/DIOD	Native	Native	Native	Native	Native	10k to 3D3V_S0
PWMOUT/GP31	3VSB	PWMOUT	Native	W3_DISABLE_N	wake up	DOD/DIOD	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 3D3V_S5 L: disable
DPWROK/GP32	3VSB	DPWROK	Native	W1_DISABLE_N	wake up	DOD/DIOD	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 3D3V_S5 L: disable
SUSACK#/GP33	3VSB	SUSACK#	Native	SIO_BOARD_ID3	board ID	DOD/DIOD	GPI	GPI	GPI	GPI	GPI	controlled by EC H: scalar, L: non-scalar
SUSWARN#/GP34	3VSB	SUSWARN#	Native	SIO_BOARD_ID2	board ID	DOD/DIOD	GPI	GPI	GPI	GPI	GPI	board stage
FAN_TAC4/GP35	3VSB	FAN_TAC4	Native	SIO_BOARD_ID1	board ID	DI/DIOD	GPI	GPI	GPI	GPI	GPI	board stage
FAN_CTL3/GP36	3VSB	FAN_CTL3	Native	no use	no use	DOD/DIOD	GPO H	GPO H	GPO H	GPO H	GPO H	
FAN_TAC3/GP37	3VSB	FAN_TAC3	Native	EC_AMP_RST	mute	DI/DIOD	GPO L	GPO L	GPO L	GPO H	GPO H	10k to 3D3V_A controlled by EC H: reset/mute, L: normal
3VSBSW#/GP40	3VSB	3VSBSW#	Native	SLP_S3_N_R3	sequence	DOD/DIOD	GPI	GPI	GPI	GPI	GPI	10k to 3D3V_S5 controlled by EC
PWROK2/GP41	3VSB	PWROK2	Native	PWROK3_2	PWROK (reserved)	DOD/DIOD	Native	Native	Native	Native	Native	10k to 3D3V_S5
PSON#/GP42	3VSB	PSON#	Native	SIO_PSON_N	S0 power (reserved)	DOD/DIOD	Native	Native	Native	Native	Native	4.7k to 3D3V_A
PANSWH#/GP43	3VSB	PANSWH#	Native	PB_IN_N_1	PWR BTN	DI/DIOD	Native	Native	Native	Native	Native	330k to 3D3V_A
PWRON#/GP44	3VSB	PWRON#	Native	SW_ON_N_SIO	sequence	DOD/DIOD	Native	Native	Native	Native	Native	10k to 3D3V_S5
D_RX0/SMCLK2/ GP46	3VSB	null		SMBCLK2_SIO	SIO SMBUS2	DI/DIO/DIOD	Native	Native	Native	Native	Native	10k to 3D3V_A controlled by EC
D_TX0/SMDAT2/ GP47	3VSB	null		SMBDAT2_SIO	SIO SMBUS2	DO/DIO/DIOD	Native	Native	Native	Native	Native	10k to 3D3V_A controlled by EC
SO/GP50	3VSB	SO	Native	SIO_SO	EC EPROM	DI/DIOD	Native	Native	Native	Native	Native	1k to 3D3V_A
FAN_CTL2/GP51	3VSB	FAN_CTL2	Native	SUSLED_R_N	LED	DOD/DIOD	Native	Native	Native	Native	Native	10k to USB30_VCCA
FAN_TAC2/GP52	3VSB	FAN_TAC2	Native	EC_SMI#	(Reserved)	DI/DIOD	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 3D3V_S5
SUSC#/GP53	3VSB	SUSC#	Native	SLP_S5_N_R	sequence	DI/DIOD	Native	Native	Native	Native	Native	10k to 3D3V_S5
PME#/GP54	3VSB	PME#	Native	LPC_PME_N	LPC	DOD/DIOD	Native	Native	Native	Native	Native	2.2k(R) to 3D3V_S5
RSMRST#/CIRRX1/GP55	3VSB	RSMRST#	Native	ICH_RSMRST_N_R	sequence	DOD/DI/DIOD	Native	Native	Native	Native	Native	10k to 3D3V_S5
MCLK/GP56	3VSB	MCLK	Native	MCLK	no use	DIOD/DIOD	Native	Native	Native	Native	Native	10k to 5V_S5
MDAT/GP57	3VSB	MDAT	Native	MDAT	no use	DIOD/DIOD	Native	Native	Native	Native	Native	10k to 5V_S5
KCLK/GP60	3VSB	KCLK	Native	KBCLK	no use	DIOD/DIOD	Native	Native	Native	Native	Native	10k to 5V_S5
KDAT/GP61	3VSB	KDAT	Native	KDAT	no use	DIOD/DIOD	Native	Native	Native	Native	Native	10k to 5V_S5
KRST#/GP62	3VSB	KRST#	Native	KBRST_N	KBRST	DO/DIOD	Native	Native	Native	Native	Native	10k(R) to 3D3V_S0
SLP_SUS#/VLDT_EN/GP63	3VSB	SLP_SUS#	Native	APU_PROCHOT#	(Reserved)	DI/DOD/DIOD	GPI	GPI	GPI	GPI	GPI	1k to 3D3V_S0 controlled by EC
GP70/KSI0	3VSB	KSI0	Native	DET_HDMI	scalar/HDMI	DIOD/DI	GPI	GPI	GPI	GPI	GPI	10k to 3D3V_A controlled by EC
GP71/KSI1	3VSB	KSI1	Native	SCALAR_EN	scalar/HDMI	DIOD/DI	GPO H	GPO H	GPO H	GPO L	GPO L	10k to 3D3V_A controlled by EC H: enable scalar
GP72/KSO0	3VSB	KSO0	Native	EUP_DSW_SEL	strap	DIOD/DO	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 3D3V_A ?
GP73/KSO1	3VSB	KSO1	Native	SIO_PANEL_ON	panel ON/OFF	DIOD/DO	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 3D3V_A controlled by EC L: panel ON
GP74/KSO2	3VSB	KSO2	Native	SIO_PANEL_OFF	panel ON/OFF	DIOD/DO	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 3D3V_A controlled by EC L: panel OFF
GP75/KSO3	3VSB	KSO3	Native	LVDS_BL_EN_1	panel ON/OFF	DIOD/DO	GPI	GPI	GPI	GPI	GPI	10k to 3D3V_A controlled by EC
GP76/KSO4	3VSB	KSO4	Native	no use	no use	DIOD/DO	GPO H	GPO H	GPO H	GPO H	GPO H	
GP77/KSO5	3VSB	KSO5	Native	SIO_MEM_EVENT_L	power consum. (reserved)	DIOD/DO	GPO H	GPO H	GPO H	GPO H	GPO H	controlled by EC
IO_SCI#/GP85/SMDAT0	3VSB			SIO_SMDAT0	SIO SMBUS0	DO/DIOD/DIOD	Native	Native	Native	Native	Native	4.7k to 3D3V_S0 controlled by EC
GP86/SMCLK0	3VSB			SIO_SMCLK0	SIO SMBUS0	DIOD/DIOD	Native	Native	Native	Native	Native	4.7k to 3D3V_S0 controlled by EC

<Core Design>

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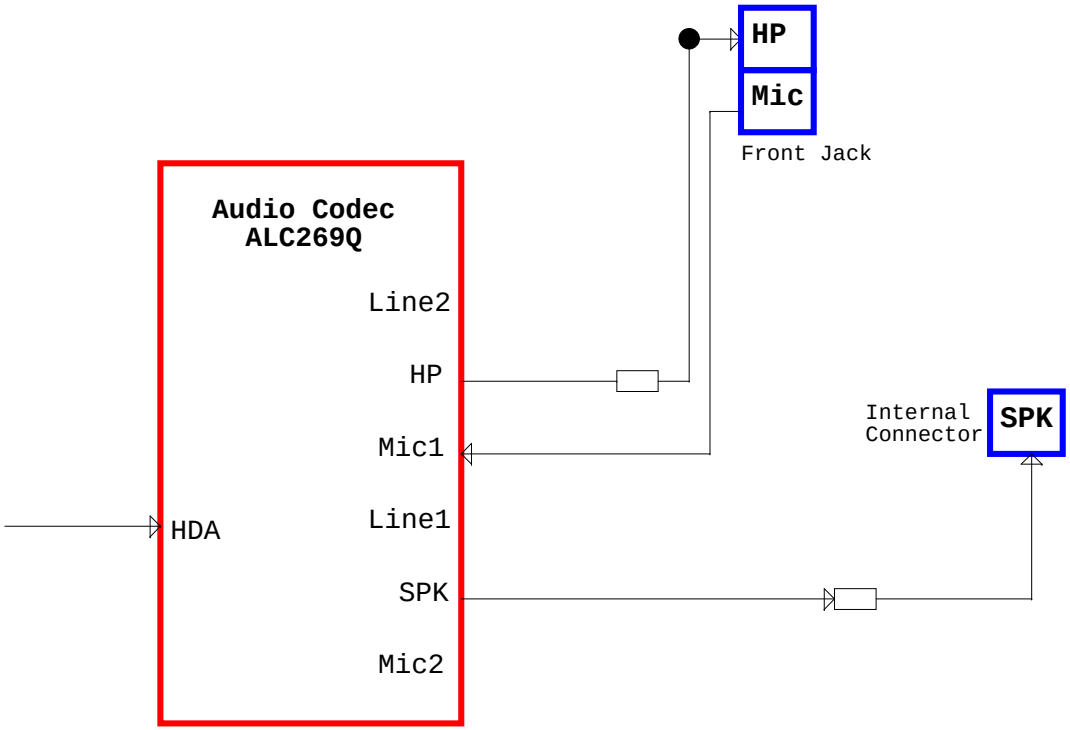
Hsichih, Taipei

Title: GPIO Table

Size: Custom | Document Number: Low Cost AIO | Rev: 1A

Date: Friday, September 12, 2014 | Sheet 7 of 62



<Variant Name>

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Title: Audio Block Diagram

Size: C | Document Number: Low Cost AIO | Rev: 1A

Date: Friday, September 12, 2014 | Sheet 8 of 62

<Core Design>

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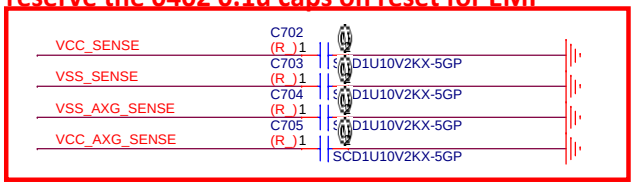
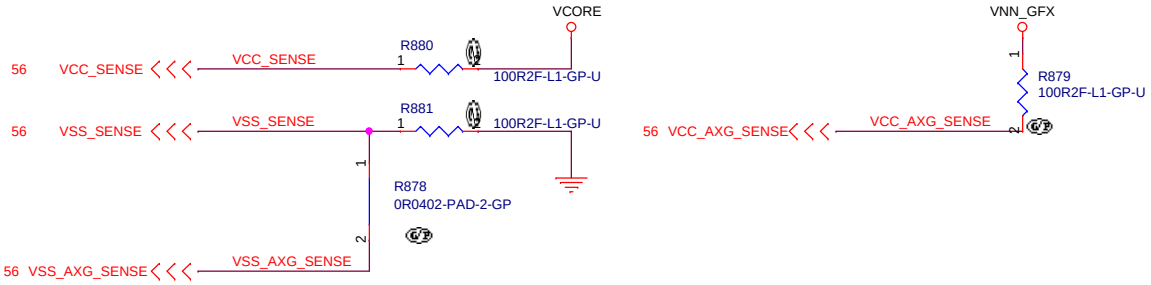
Title: CPU (DDR)

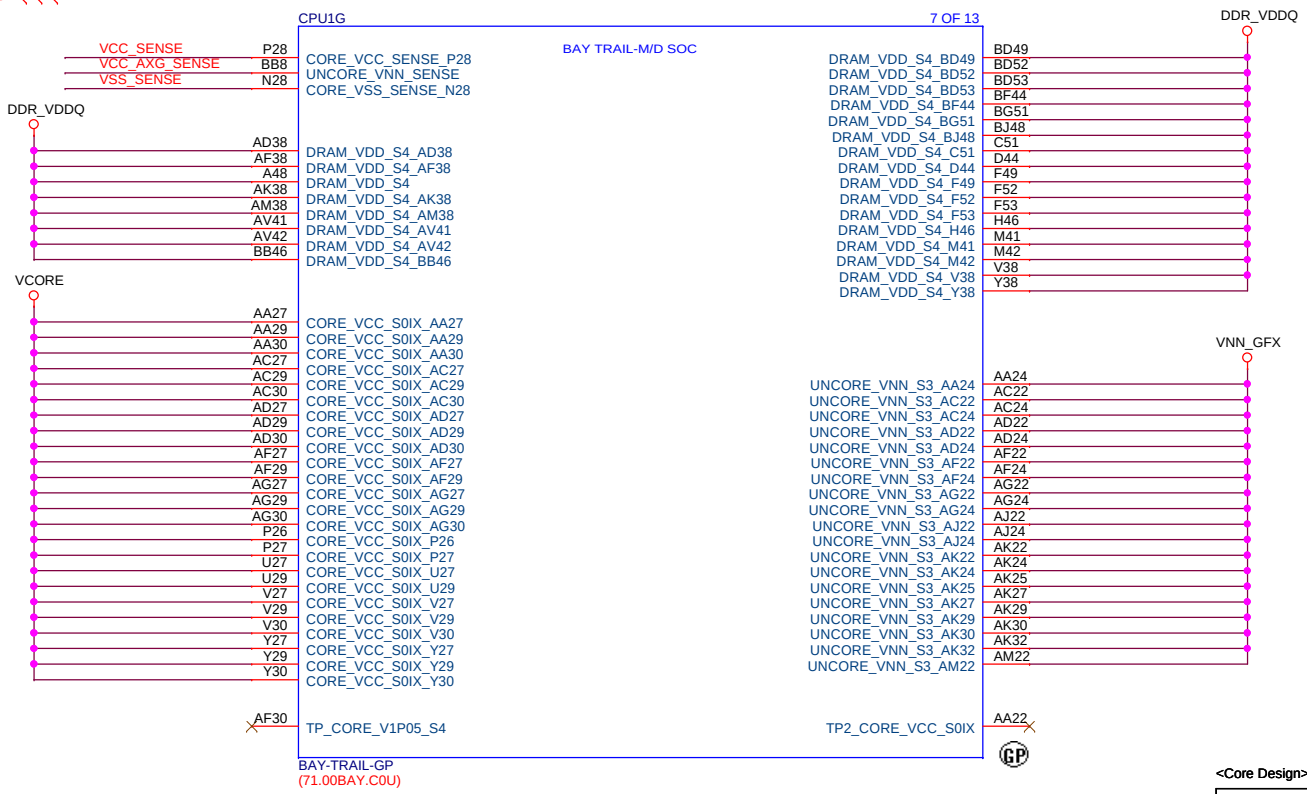
Size: Custom | Document Number: Low Cost AIO | Rev: 1A

Date: Friday, September 12, 2014 | Sheet 9 of 62

reserve the 0402 0.1u caps on reset for EMI







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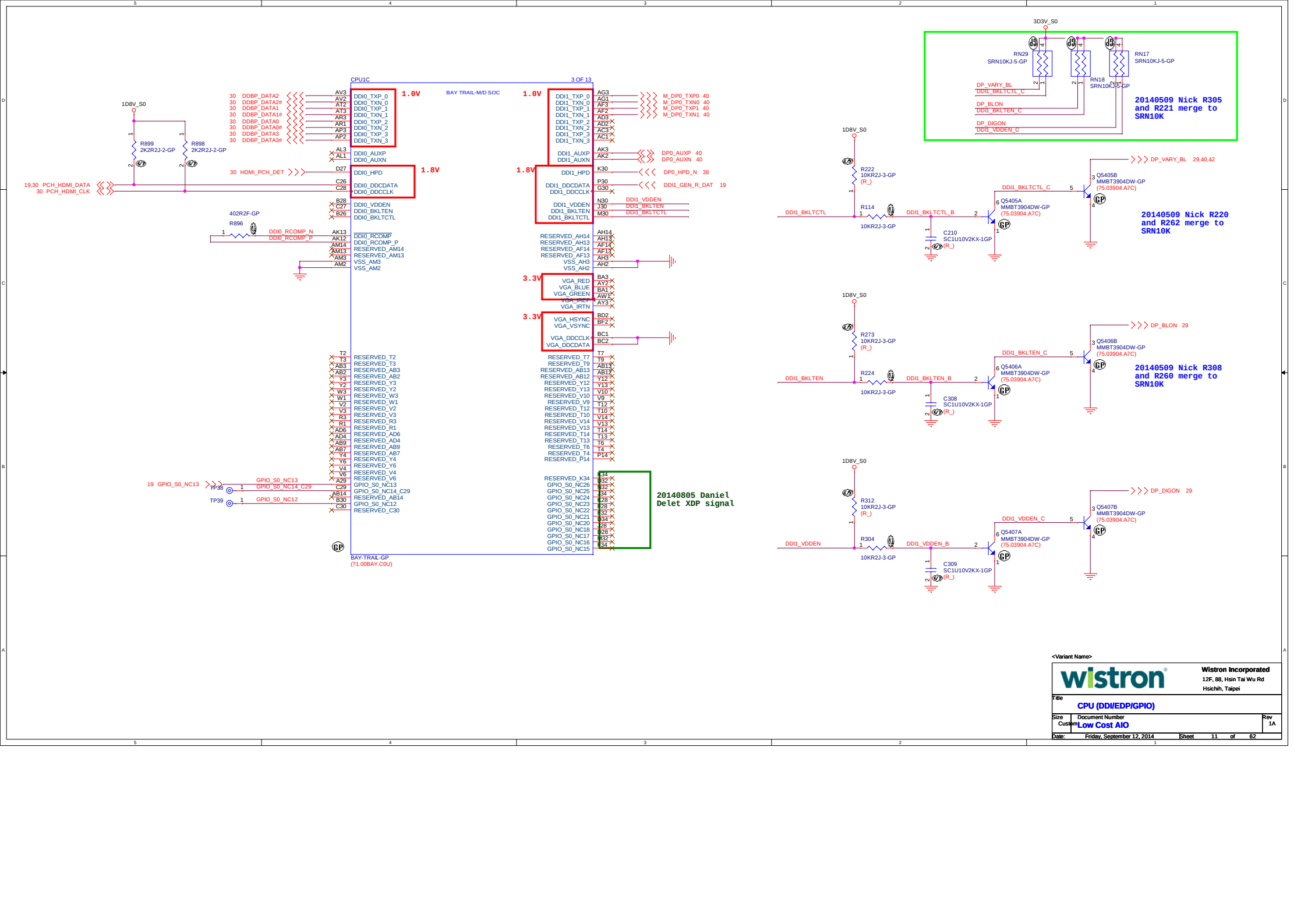
Hsichih, Taipei

Title: CPU (VCC CORE)

Size: Custom | Document Number: Low Cost AIO | Rev: 1A

Date: Friday, September 12, 2014 | Sheet 10 of 62


CPU1C
3 OF 13
BAY TRAIL-M/D SOC
BAY-TRAIL-GP
(71.00BAY.C0U)
1.0V
1.8V
3.3V
1D8V_S0
3D3V_S0
R899 2K2R2J-2-GP
R898 2K2R2J-2-GP
402R2F-GP
R896
DDI0_TXP_0
DDI0_TXN_0
DDI0_TXP_1
DDI0_TXN_1
DDI0_TXP_2
DDI0_TXN_2
DDI0_TXP_3
DDI0_TXN_3
DDI0_AUXP
DDI0_AUXN
DDI0_HPD
DDI0_DDCDATA
DDI0_DDCCLK
DDI0_VDDEN
DDI0_BKLTEN
DDI0_BKLTCTL
DDI0_RCOMP
DDI0_RCOMP_P
RESERVED_AM14
RESERVED_AM13
VSS_AM3
VSS_AM2
DDI1_TXP_0
DDI1_TXN_0
DDI1_TXP_1
DDI1_TXN_1
DDI1_TXP_2
DDI1_TXN_2
DDI1_TXP_3
DDI1_TXN_3
DDI1_AUXP
DDI1_AUXN
DDI1_HPD
DDI1_DDCDATA
DDI1_DDCCLK
DDI1_VDDEN
DDI1_BKLTEN
DDI1_BKLTCTL
RESERVED_AH14
RESERVED_AH13
RESERVED_AF14
RESERVED_AF13
VSS_AH3
VSS_AH2
VGA_RED
VGA_BLUE
VGA_GREEN
VGA_IRTN
VGA_HSYNC
VGA_VSYNC
VGA_DDCCLK
VGA_DDCDATA
RESERVED_T2
RESERVED_T3
RESERVED_AB3
RESERVED_AB2
RESERVED_Y3
RESERVED_Y2
RESERVED_W3
RESERVED_W1
RESERVED_V2
RESERVED_V3
RESERVED_R3
RESERVED_R1
RESERVED_AD6
RESERVED_AD4
RESERVED_AB9
RESERVED_AB7
RESERVED_Y4
RESERVED_Y6
RESERVED_V4
RESERVED_V6
GPIO_S0_NC13
GPIO_S0_NC14_C29
RESERVED_AB14
GPIO_S0_NC12
RESERVED_C30
RESERVED_T7
RESERVED_T9
RESERVED_AB13
RESERVED_AB12
RESERVED_Y12
RESERVED_Y13
RESERVED_Y10
RESERVED_V10
RESERVED_V9
RESERVED_T12
RESERVED_T10
RESERVED_V14
RESERVED_V13
RESERVED_T14
RESERVED_T13
RESERVED_T6
RESERVED_T4
RESERVED_P14
RESERVED_K34
GPIO_S0_NC26
GPIO_S0_NC25
GPIO_S0_NC24
GPIO_S0_NC23
GPIO_S0_NC22
GPIO_S0_NC21
GPIO_S0_NC20
GPIO_S0_NC18
GPIO_S0_NC17
GPIO_S0_NC16
GPIO_S0_NC15
M_DP0_TXP0 40
M_DP0_TXN0 40
M_DP0_TXP1 40
M_DP0_TXN1 40
DP0_AUXP 40
DP0_AUXN 40
DP0_HPD_N 38
DDI1_GEN_R_DAT 19
DDI1_VDDEN
DDI1_BKLTEN
DDI1_BKLTCTL
DDBP_DATA2
DDBP_DATA2#
DDBP_DATA1
DDBP_DATA1#
DDBP_DATA0
DDBP_DATA0#
DDBP_DATA3
DDBP_DATA3#
HDMI_PCH_DET
PCH_HDMI_DATA
PCH_HDMI_CLK
GPIO_S0_NC13
GPIO_S0_NC14_C29
GPIO_S0_NC12
TP38
TP39
20140805 Daniel
Delet XDP signal
RN29 SRN10KJ-5-GP
RN18 SRN10KJ-5-GP
RN17 SRN10KJ-5-GP
DP_VARY_BL
DDI1_BKLTCTL_C
DP_BLON
DDI1_BKLTEN_C
DP_DIGON
DDI1_VDDEN_C
20140509 Nick R305
and R221 merge to
SRN10K
R222 10KR2J-3-GP (R_)
R114 10KR2J-3-GP
C210 SC1U10V2KX-1GP (R_)
Q5405A MMBT3904DW-GP (75.03904.A7C)
Q5405B MMBT3904DW-GP (75.03904.A7C)
DDI1_BKLTCTL_B
20140509 Nick R220
and R262 merge to
SRN10K
R273 10KR2J-3-GP (R_)
R224 10KR2J-3-GP
C308 SC1U10V2KX-1GP (R_)
Q5406A MMBT3904DW-GP (75.03904.A7C)
Q5406B MMBT3904DW-GP (75.03904.A7C)
DDI1_BKLTEN_B
20140509 Nick R308
and R260 merge to
SRN10K
R312 10KR2J-3-GP (R_)
R304 10KR2J-3-GP
C309 SC1U10V2KX-1GP (R_)
Q5407A MMBT3904DW-GP (75.03904.A7C)
Q5407B MMBT3904DW-GP (75.03904.A7C)
DDI1_VDDEN_B
<Variant Name>
wistron
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
CPU (DDI/EDP/GPIO)
Size
Custom
Document Number
Low Cost AIO
Rev
1A
Date: Friday, September 12, 2014
Sheet 11 of 62

USB Table

Pair	Device
0	USB3.0 Port 0 (USB3S2)
1	USB HUB IC
2	CAM1
3	Delete TOUCH1

Make sure the signal routing is as short as possible
and isolated from high speed data signal.
Parasitic resistance for the overall routing should be less than 100 Ω.

CPU1F — BAY TRAIL-M/D SOC — 6 OF 13

BAY-TRAIL-GP
(71.00BAY.C0U)

PANEL OFF

KEY TEST

LPC DEBUG PORT

Pin height 2.3mm

Layout Close SIO

09/12 Daniel modify

09/12 CM modify

20140509 Nick R1225 and R1226 merge to SRN2.2K

20140909 Daniel Reserved For EMI

Variant Name	<Variant Name>
Company	Wistron Incorporated
Address	12F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	CPU (USB/LPC/GPIO)
Size	C
Document Number	Low Cost AIO
Rev	1A
Date	Friday, September 19, 2014
Sheet	12 of 62

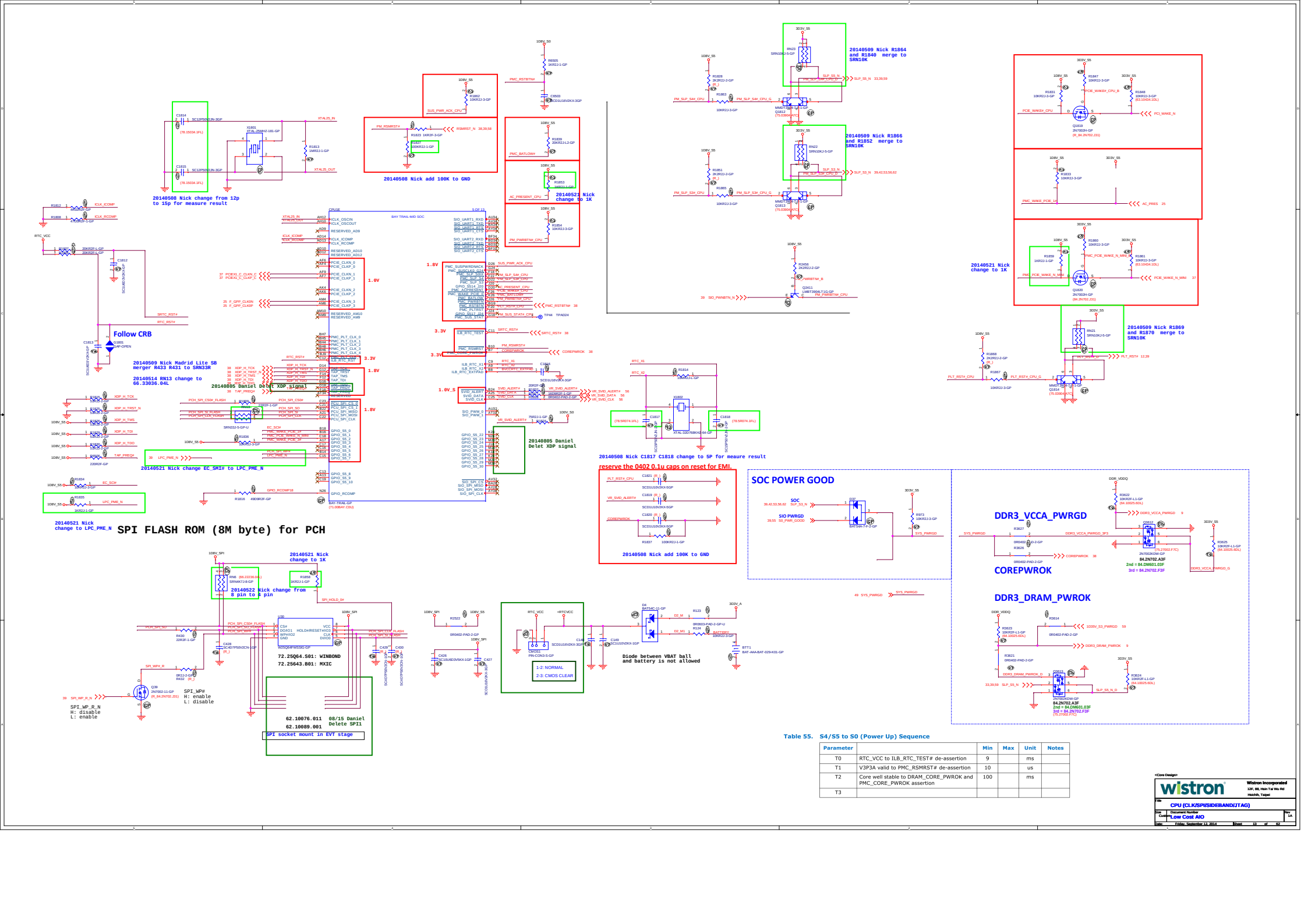


Table 55. S4/S5 to S0 (Power Up) Sequence

Parameter		Min	Max	Unit	Notes
T0	RTC_VCC to ILB_RTC_TEST# de-assertion	9		ms	
T1	V3P3A valid to PMC_RSMRST# de-assertion	10		us	
T2	Core well stable to DRAM_CORE_PWROK and PMC_CORE_PWROK assertion	100		ms	
T3					

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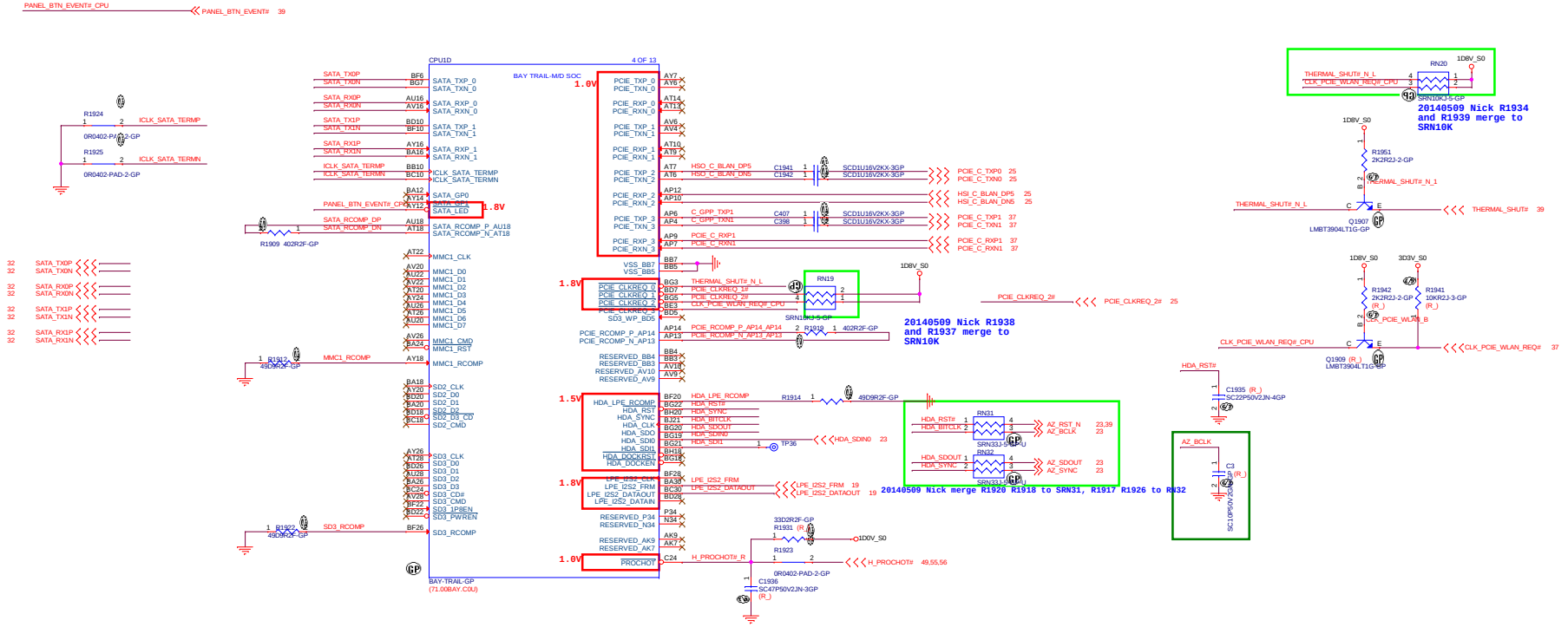
20140807 Daniel
Short PANEL_BTN_EVENT# to PANEL_BTN_EVENT#_CPU
Delete Q1816, R1856, R1855"



<Variant Name>

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12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU (SATA/PCIE/IHDA)

Size	Document Number	Rev
Custom	Low Cost AIO	1A

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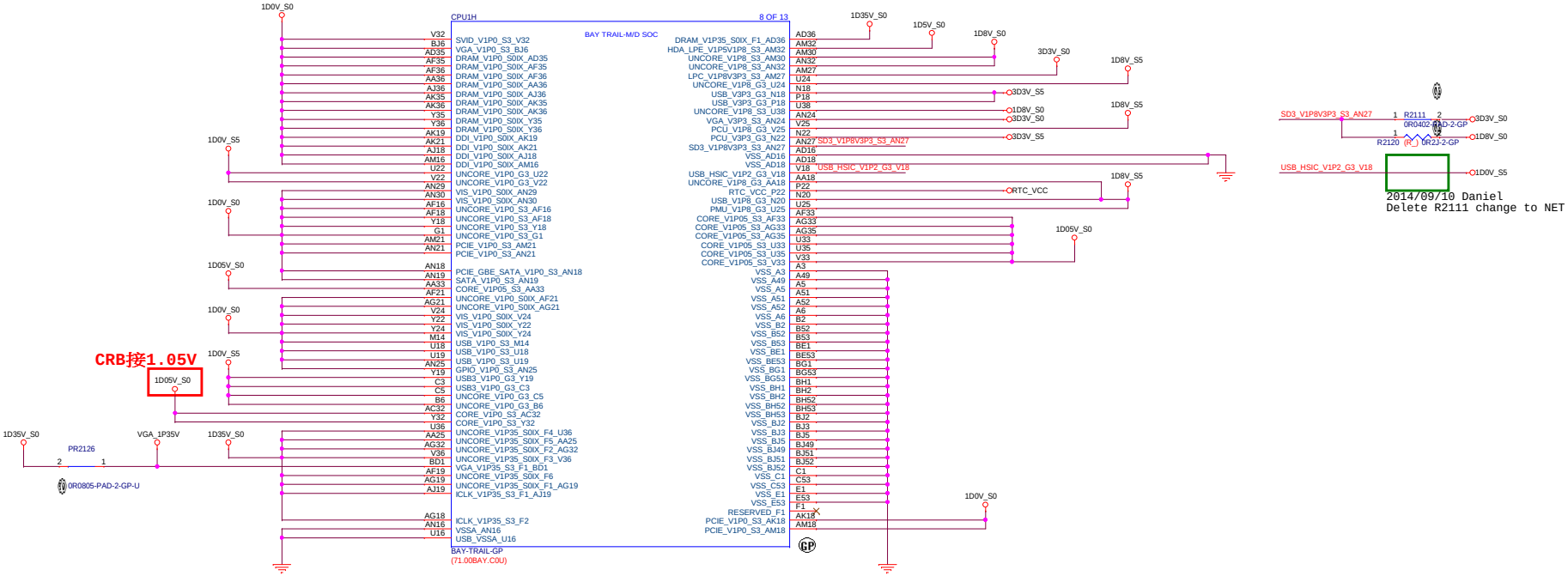

<Core Design>

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12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU (POWER)

Size: C | Document Number: Low Cost AIO | Rev: 1A

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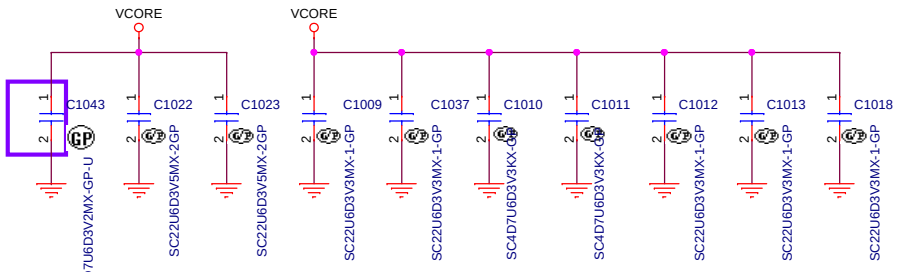
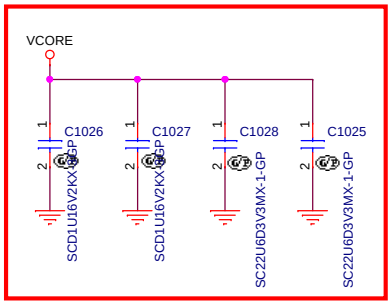
VCORE

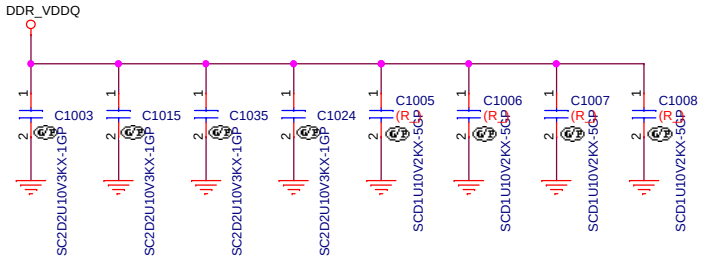


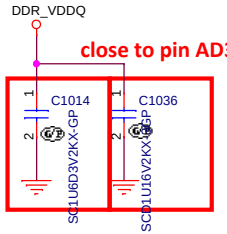
reserve the 0402 0.1u caps on reset for EMI(5/9).



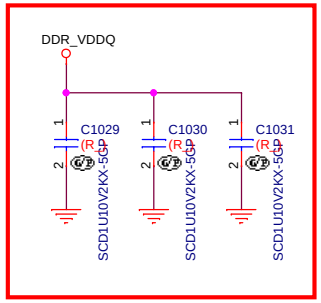
20150515 Nick add for power request

DDR_VDDQ

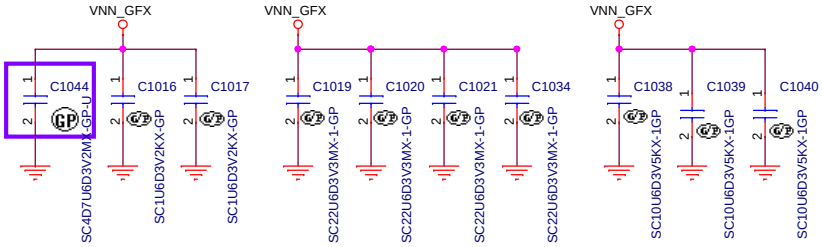




reserve the 0402 0.1u caps on reset for EMI(5/9).

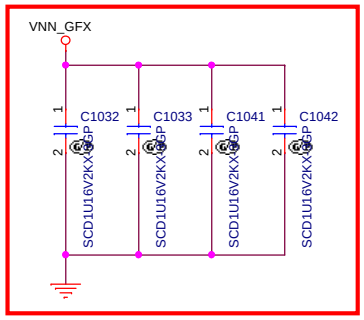


VNN_GFX



20150515 Nick add for power request

reserve the 0402 0.1u caps on reset for EMI(5/9).



<Core Design>

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12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU (POWER CAP1)

Size: B | Document Number: Low Cost AIO | Rev: 1A

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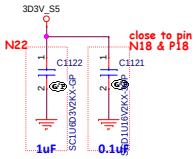
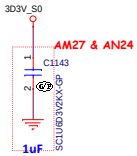
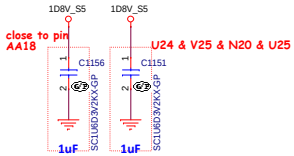
3D3V_S5



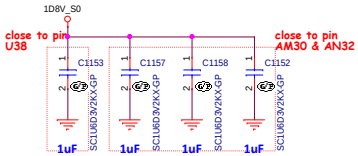
3D3V_S0



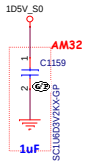
1D8V_S5



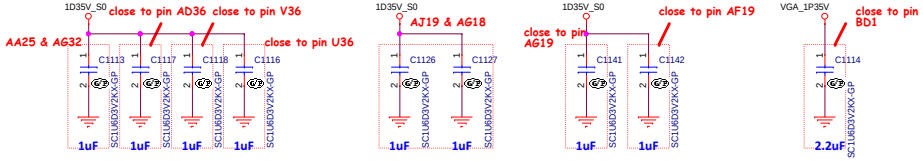
1D8V_S0



1D5V_S0

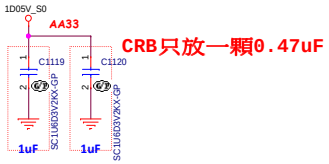


1D35V_S0

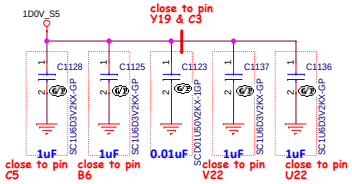


VGA_1P35V

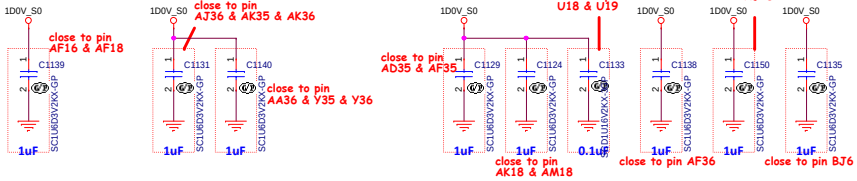
1D05V_S0

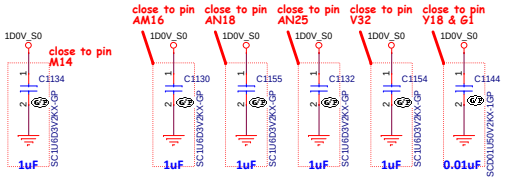


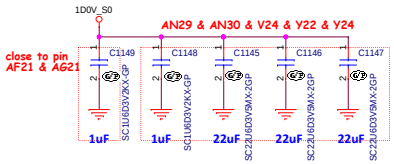
1D0V_S5



1D0V_S0







<Core Design>

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12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU (POWER CAP2)

Size: Custom | Document Number: Low Cost AIO | Rev: 1A

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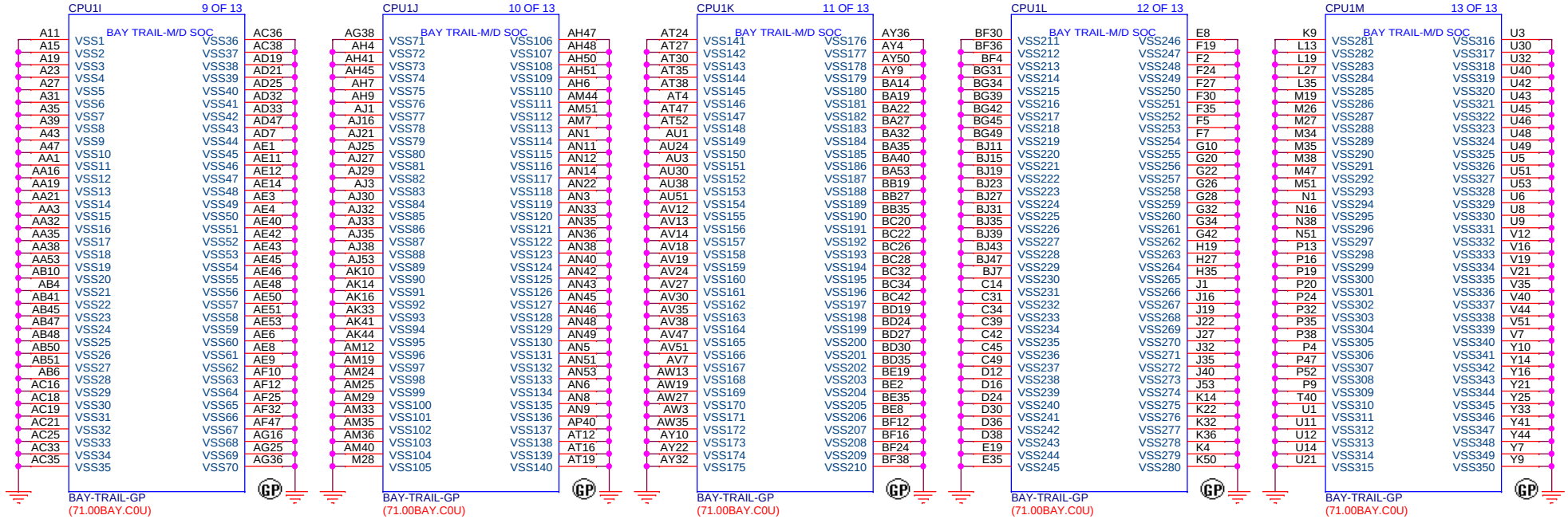

<Core Design>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: **CPU (VSS)**

Size	Document Number	Rev
Custom	Low Cost AIO	1A

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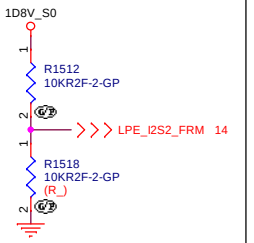
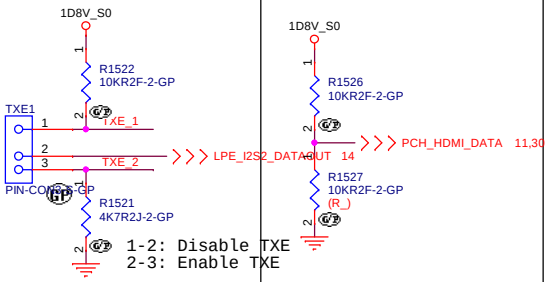
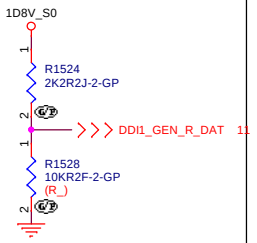
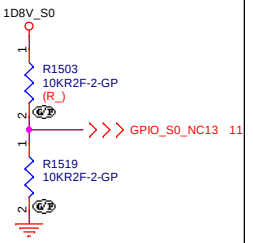
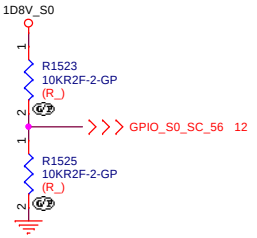
STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC
SHOULD BE PLACED OUTSIDE KOZ AREA

Description	BIOS Boot Selection	Security Flash Descriptors	DDI0 Detect	DDI1 Detect	DDI1 Detect	Top swap
GPIO	GPIO_S0_SC[063]	GPIO_S0_SC[065]	DDI0_DDCDATA	DDI1_DDCDATA	MDSI_DDCDATA	GPIO_S0_SC [56]
Schematic						
High	SPI	Normal Operation	DDI0 detected	DDI1 detected	DDI1 detected	
Low	LPC	Override	DDI0 not detected	DDI1 not detected	DDI1 not detected	

2.25 Hardware Straps

All straps are sampled on the rising edge of PMC_CORE_PWROK.

Table 27. Straps

Signal Name	Function	Default	Strap Exit	Strap Description
GPIO_S0_SC[63]	Legacy	1b	PMC_CORE_PWROK de-asserted	BIOS Boot Selection 0 = LPC 1 = SPI
GPIO_S0_SC[65]	Legacy	1b	PMC_CORE_PWROK de-asserted	Security Flash Descriptors 0 = Override 1 = Normal Operation
DDI0_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
DDI1_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected
MDSI_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected

27.1.1.2 Hardware Controlled

System hardware, external to the SoC, can be used to assert or de-assert the Top-Swap strapping input signal. If the signal is sampled as being asserted during power-up then Top-Swap is active.

Note: The Top-Swap strap is an active high signal and is multiplexed with the GPIO_S0_SC[56] signal.

<Core Design>

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Hsichih, Taipei

Title: CPU (STRAP)

Size: A3 | Document Number: Low Cost AIO | Rev: 1A

Date: Friday, September 12, 2014 | Sheet 19 of 62

TBD

<Core Design>

Wistron Incorporated
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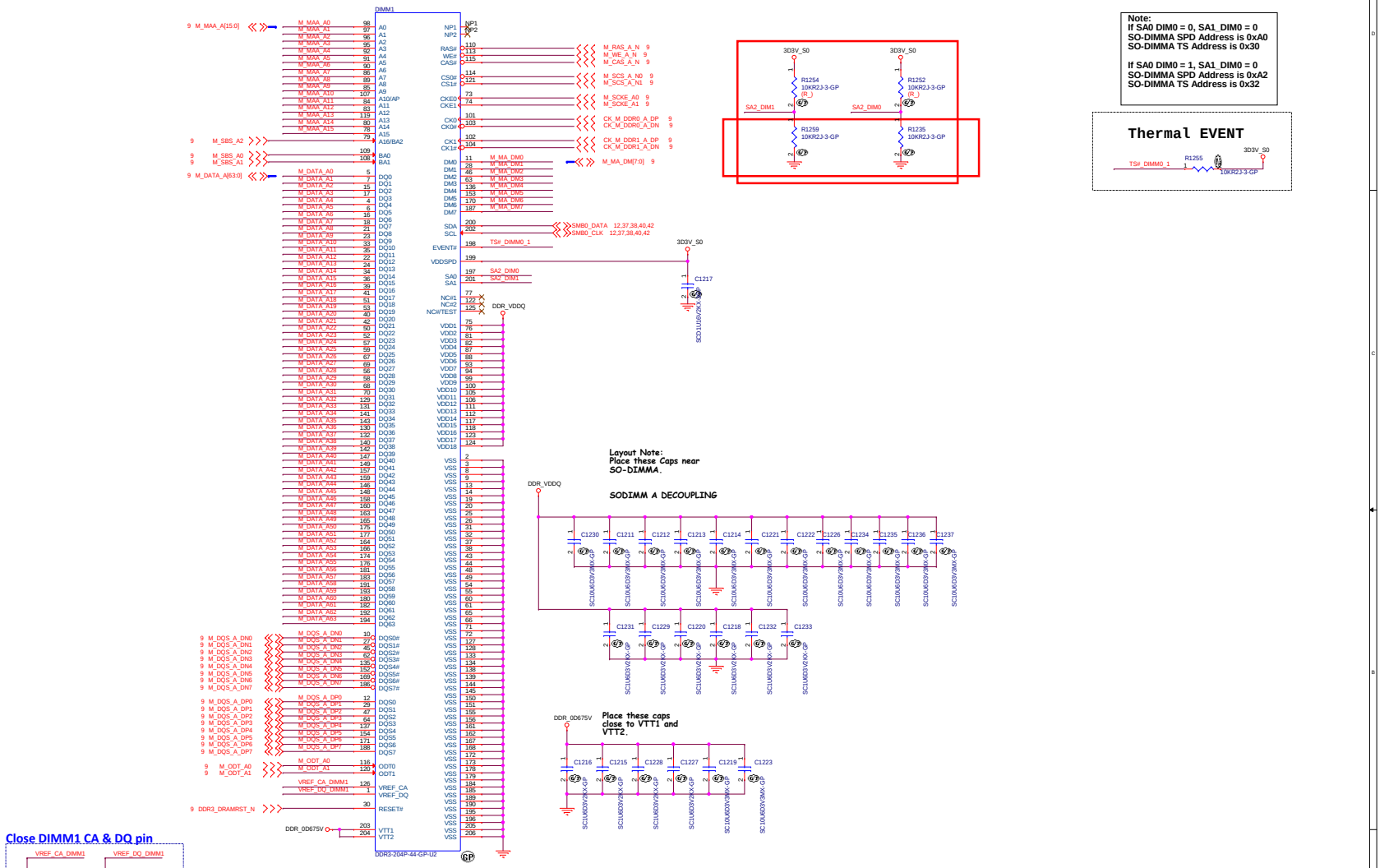
Hsichih, Taipei

Title: DDR3L-SODIMM1

Size: Custom | Document Number: Low Cost AIO | Rev: 1A

Date: Friday, September 12, 2014 | Sheet 20 of 62



<Core Design>

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Hsichih, Taipei

Title: DDR3L-SODIMM2

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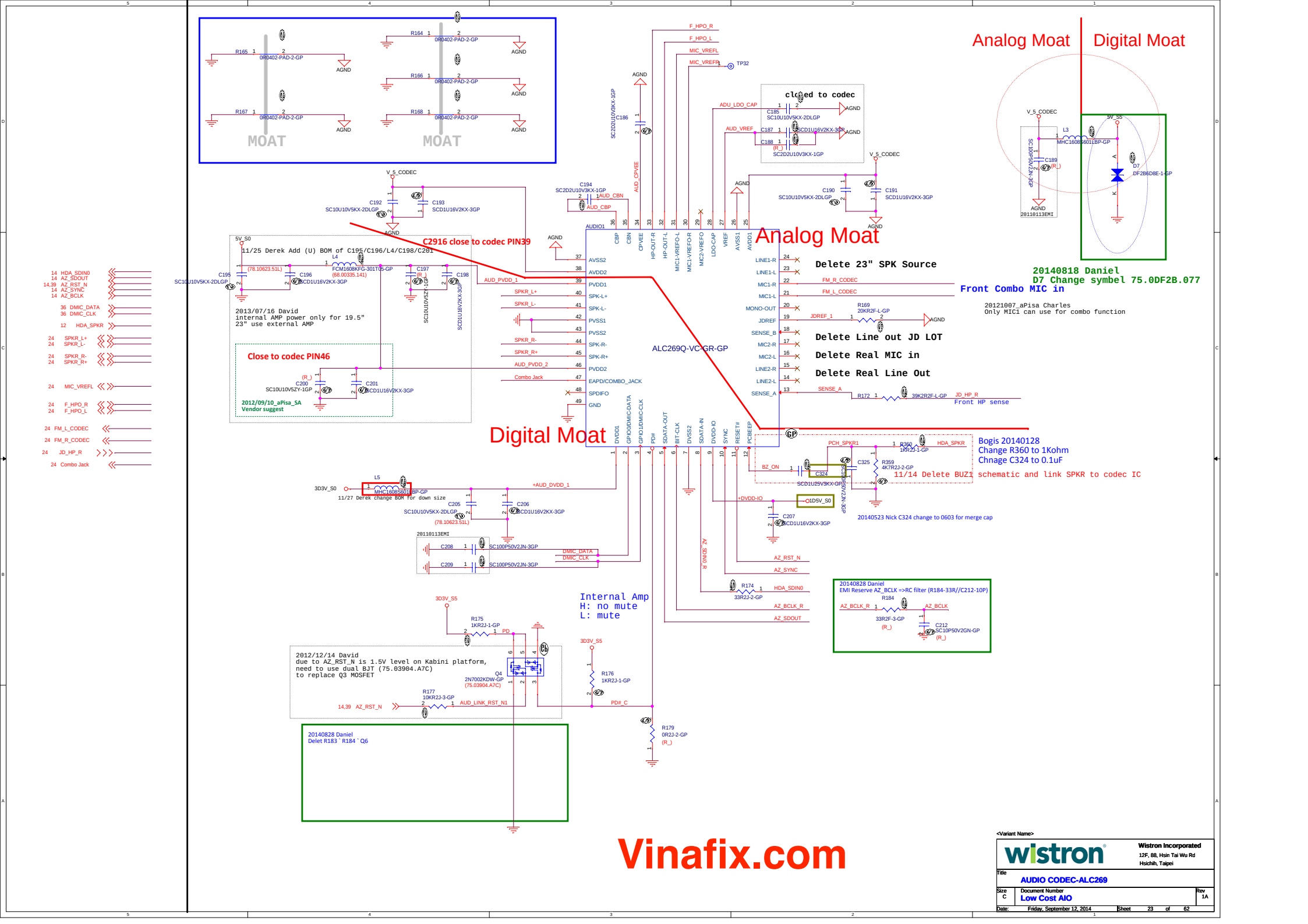
Date: Friday, September 12, 2014 | Sheet 21 of 62

TBD

<Core Design>

wistron®	**Wistron Incorporated** 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title: **Front BD Connector**		
Size: A	Document Number: **Low Cost AIO**	Rev: 1A
Date: Friday, September 12, 2014	Sheet 22 of 62	


MOAT
MOAT
Analog Moat
Digital Moat
closed to codec
C2916 close to codec PIN39
11/25 Derek Add (U) BOM of C195/C196/L4/C198/C201
2013/07/16 David
internal AMP power only for 19.5"
23" use external AMP
Close to codec PIN46
2012/09/10_aPisa_SA
Vendor suggest
Analog Moat
Delete 23" SPK Source
Front Combo MIC in
20121007_aPisa Charles
Only MIC1 can use for combo function
Delete Line out JD LOT
Delete Real MIC in
Delete Real Line Out
Front HP sense
ALC269Q-VC-GR-GP
Digital Moat
20140818 Daniel
D7 Change symbel 75.0DF2B.077
Bogis 20140128
Change R360 to 1Kohm
Chnage C324 to 0.1uF
11/14 Delete BUZ1 schematic and link SPKR to codec IC
20140523 Nick C324 change to 0603 for merge cap
11/27 Derek change BOM for down size
20140828 Daniel
EMI Reserve AZ_BCLK =>RC filter (R184-33R//C212-10P)
Internal Amp
H: no mute
L: mute
2012/12/14 David
due to AZ_RST_N is 1.5V level on Kabini platform,
need to use dual BJT (75.03904.A7C)
to replace Q3 MOSFET
20140828 Daniel
Delet R183 `R184 `Q6
Vinafix.com
Wistron Incorporated
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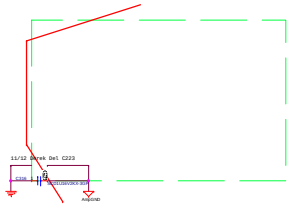
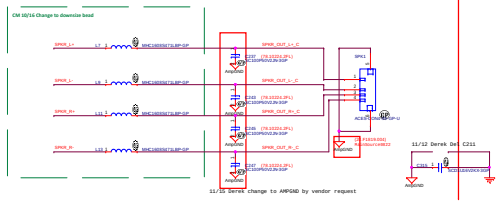
Hsichih, Taipei
AUDIO CODEC-ALC269
Low Cost AIO
Friday, September 12, 2014

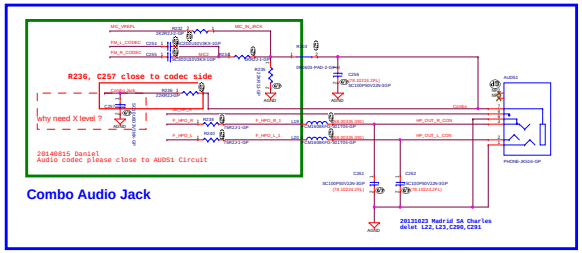
The ADAM1278C is integrated +8Y ESD protection of system level up to +/- 8KV and offers a high-performance, low-cost solution for signals switching.

Support iPhone ~ Mount R3018,R3020
unMount R3019,R3021

Support Nokia ~ Mount R3019,R3021
unMount R3018,R3020







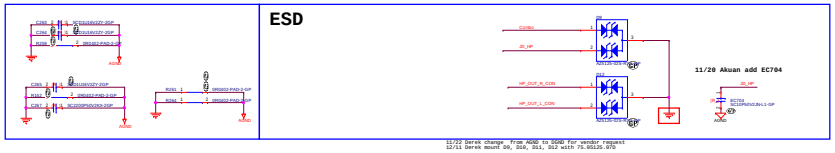
SHDN_MUTE_AP_CTL

When the PC mode and Monitor mode are being switched

MUTE_AP_CTL should be low in order to avoid the noise

MUTE_AP_CTL also control when select MUTE in the PC mode or Monitor mode

MUTE_AP_CTL also control when system wake from S3 to S0



Control
23 JD_HP_R

Enable Control
Low: Mute
High: No-MUTE
23 PH_L_CODEC
23 PH_R_CODEC
23 MIC_VREF1
23 F_HPO_R
23 F_HPO_L
14,23,39 AZ_RST_N

23 SPKR_L+
23 SPKR_L-
23 SPKR_R-
23 SPKR_R+

23 Combo Jack

2013/08/28_aPlus_SA

IC	P/N	L21	R269	C270
RTL8111GA	71.08111.Y03	M	R	M
RTL8111GS	71.08111.T03	M	R	M
RTL8111G	71.08111.U03	R	M	R

M:Mount
R:Reserved

IC	P/N	C288	C289
RTL8111GA	71.08111.Y03	M	M
RTL8111GS	71.08111.T03	M	M
RTL8111G	71.08111.U03	R	R

M:Mount
R:Reserved

CLOCK

13 F_GPP_CLKOP
13 F_GPP_CLKON

PCI-E

14 PCIE_C_TXP0
14 PCIE_C_TXN0
14 HSI_C_BLAN_DP5
14 HSI_C_BLAN_DN5
14 PCIE_CLKREQ_2#

LAN

LAN wake
13 AC_PRES
39 PLTRST_LAN
39 LAN_PWR_EN

Colse to the AVDD33 pin location

C302 close to Pin11 (AVDD33)

Colse to the AVDD10 pin location

Colse to the pin22

Reserve for RTL8111G/GS/GA

Reserve for RTL8111GA

Close to LAN chipset

Mount for RTL8111G ONLY

Mount for RTL8111GS/RTL8111GA ONLY

20140514 Nick L21 change to 68.4R750.20C

Michael 2012/2/15 SB XF1 horizontal and swap pair for layout routing

20140512 Nick SB follow Seattle change to 68.89241.30A

2014/09/01 Daniel
Follow Lijiang LAN Surge Solution Cost Down

11/18 Akuan dummy

Lan Power

The V_3P3_LAN rise time must be controlled between 0.5ms and 100ms

AO3419 PMOS 3.5A

12/4 Derek remove R273 short pad

20140827 Daniel
Report 0603 R278
Delete Lan Power function

ESD

20140514 Nick mount U9 U10 for EMI
20140519 Nick change U9 U10 to (75.09904.07C)

LAN wake

2014/08/15 Daniel
ME ask change to 022.10001.0041

Lan Surge

2014/09/01 Daniel
Follow Lijiang LAN Surge Solution Cost Down

Xtal accuracy: +/- 30ppm

CLKREQ Level shift

SOC

IC

	Giga	100	10
Link	Orange	Green	X
Act	Blink	Blink	Blink

PCB

2011/06/26

<Variant Name>

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Title: LAN-RTL8111GA
Size: Custom
Document Number: *Low Cost AIO
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Date: Friday, September 19, 2014
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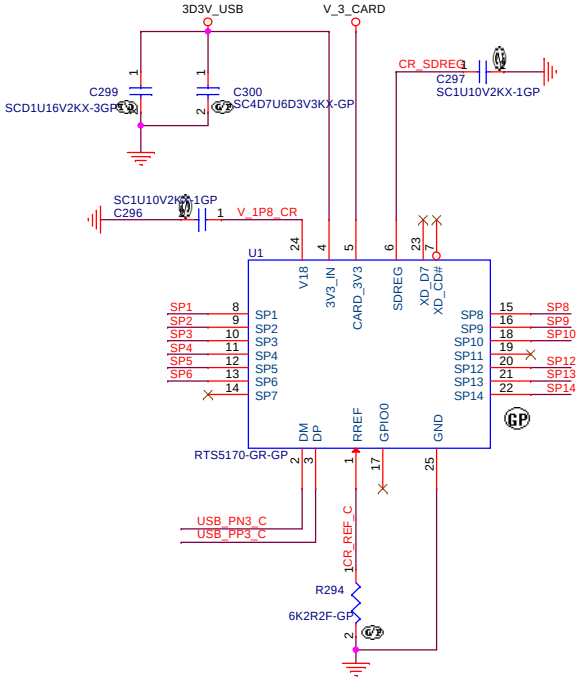
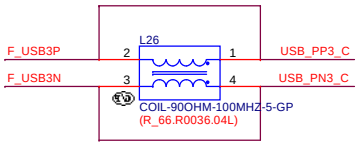
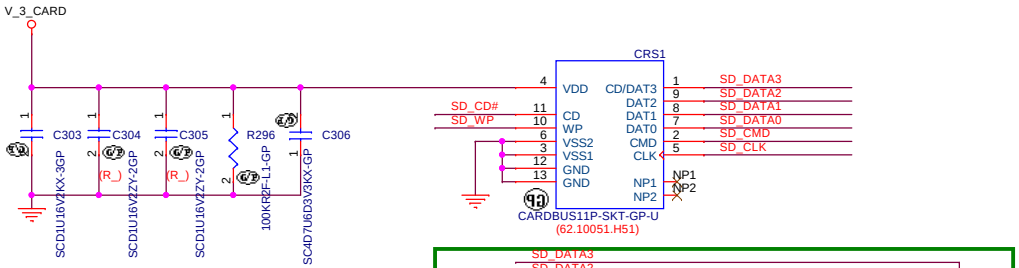
(SD only)

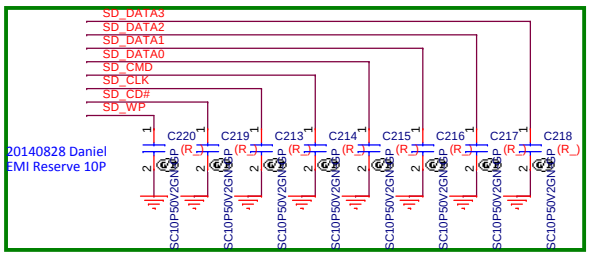
35 F_USB3P
35 F_USB3N



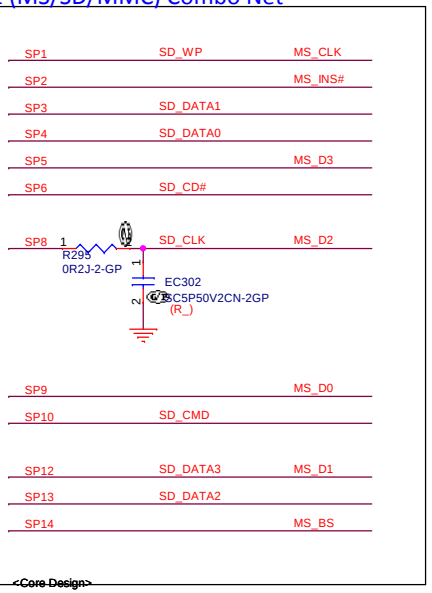




Without card	CD, WP, GND
Inserted card(lock)	CD, WP, GND
Inserted card(unlock)	CD, WP, GND



3IN1 (MS/SD/MMC) Combo Net



<Core Design>

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Title: RTS5170 (CARD READER)

Size: Custom | Document Number: Low Cost AIO | Rev: 1A

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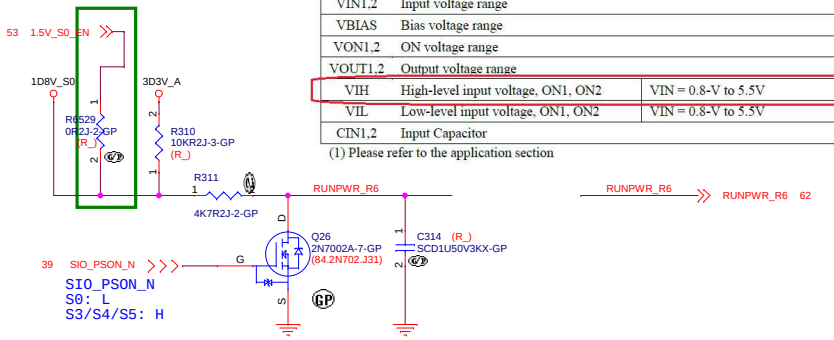
ANNIE Run Power

		MIN	MAX	UNIT
VIN1,2	Input voltage range	0.8	5.5	V
VBIAS	Bias voltage range	4.75	5.25	V
VON1,2	ON voltage range	0	5.5	V
VOUT1,2	Output voltage range		VIN1,2	V
VIH	High-level input voltage, ON1, ON2	VIN = 0.8-V to 5.5V	1.05	5.5	V
VIL	Low-level input voltage, ON1, ON2	VIN = 0.8-V to 5.5V		0.6	V
CIN1,2	Input Capacitor		0.1 (1)		µF

(1) Please refer to the application section

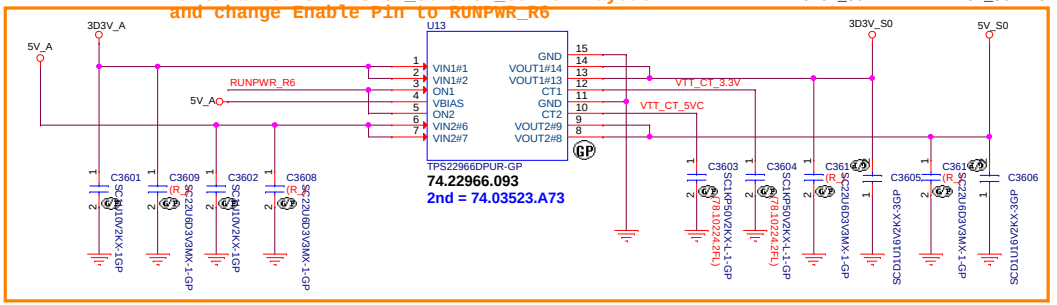


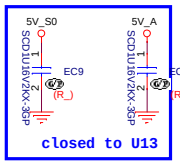
RUNPWR_R6 → RUNPWR_R6 62

12/25 Derek
Delete U13/U15 power MOS
Add TPS22966 for 3V/5V_S0 power
1/14 Daniel Change EN pin from 12V_S0_PG
1/16 Daniel SWAP 3D3V_S0 & 5V_S0 for Layout and change Enable Pin to RUNPWR_R6

Dallas 3D3V_S0=2A

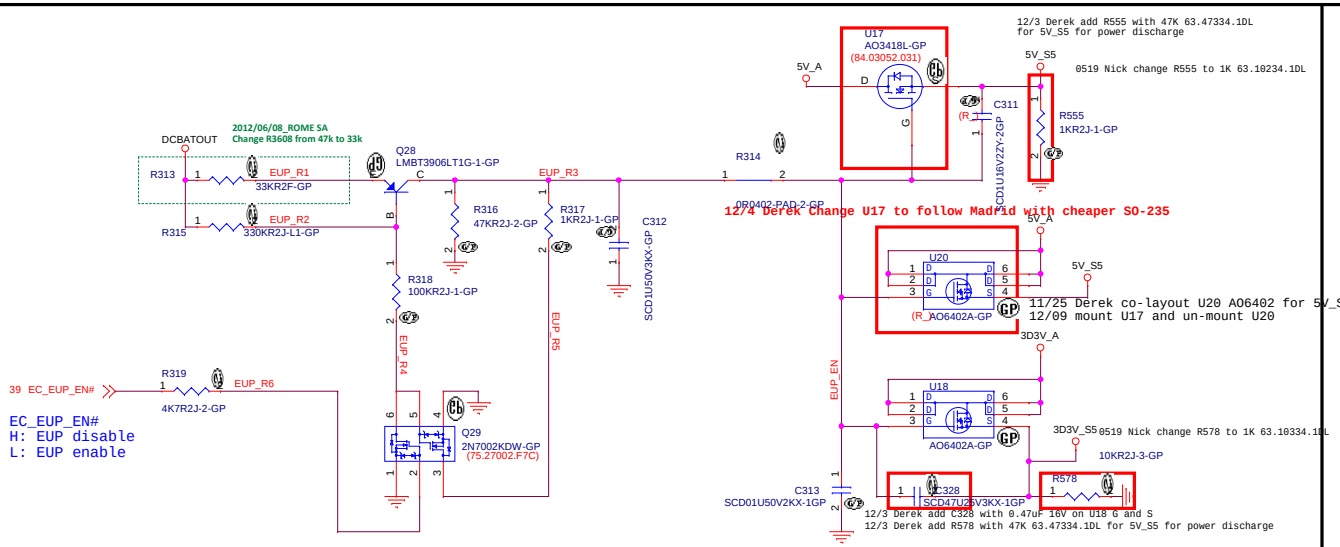
Dallas 5V_S0=4.5A





2012/10/19 David
change from 84.04468.A37(11.6A)
to 84.06402.B3D(7A)

EUP Power



2012/10/21 David
Removed PS_S3CNTRL

<Core Design>

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Title: RUN POWER & SEQUENCE

Size: Custom | Document Number: Low Cost AIO | Rev: 1A

Date: Friday, September 12, 2014 | Sheet 27 of 62

AspireLink

TBD

<Core Design>

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Title: AspireLink

Size: A | Document Number: Low Cost AIO | Rev: 1A

Date: Friday, September 12, 2014 | Sheet 28 of 62

SSID = VIDEO

Modified by Kenyon. Use CMC to choose signal source. 2012/11/07

For UMA
Low: Disable
High: Enable

2012/10/5 David
change to polysw

01/14 Daniel change U59 symbel to 74.00554.073

09/12 CM add

2012/12/26 David
add for EC to do
panel control

2013/12/3 Derek
Delete Q31/R370/R371
without ECIO BL_EN

CNVBD1 Co-Layout with CNVBD2

20mils

EC LCD ID GPIO

PCH LCD ID GPIO

09/12 CM modify
09/12 Daniel modify

20140116 EMI ISSUE Daniel mont 1000P

CNVBD3 Co-Layout & close with CNVBD2 Pin1

Roger modify 2013/2/4

11/27 Jimmy change to 32 25V

11/26 Derek Change U59 net name from AGND to LEDGND

19V boost to 50V

12/4 Derek Change L27 to P/N 68.33010.20J ; Q78 to P/N 84.04468.A37 with smaller size

1st source: 83.3R010.08M
2rd source: 83.3R010.A8M

12/13 Derek change Q78 to 084.PA010.0037

20140819 Daniel
LVDS18 LVDS19 from 20.K0683.030 change to 20.K0386.030

LVDS18 Co-Layout & close with LVDS19

20140818 Daniel
Change Power to 5V_S0

High: Enable
Low: Disable

20140522 Nick change R377 to 499ohm

2012/10/15 David
Reserved for EMI
Closed to LVDS1

2012/10/15 David
Down size to 1210
Symbol: 68.01210.20G(higher)
0 ohm: 66.R0036.04L
EMI: Murata 68.00396.001

Change to 20113018 type
20131023 Kenyon
20131113 Derek delete L27~L39

11/27 Jimmy update Cable Spec

Panel Model	Cable Spec			
	ID0	ID1	ID2	Vout
LG LM230WF3-SLK1	0	0	0	3,4 Vout 1,6 RTN 2,5 N.C
LG LM230WF5-TLF1	0	0	1	3,4 Vout 1,6 RTN 2,5 N.C
LG LM230WF3-SLL1	0	1	0	3,4 Vout 1,6 RTN 2,5 N.C
CMI M195FGE-L23 C1	1	0	0	1,2,5,6 Vout 3,4 RTN
CMI M195FGE-L20 C3	1	1	0	1,2,5,6 Vout 3,4 RTN
CMI M195FGE-L20 C1	1	1	1	1,2,5,6 Vout 3,4 RTN

<Variant Name>

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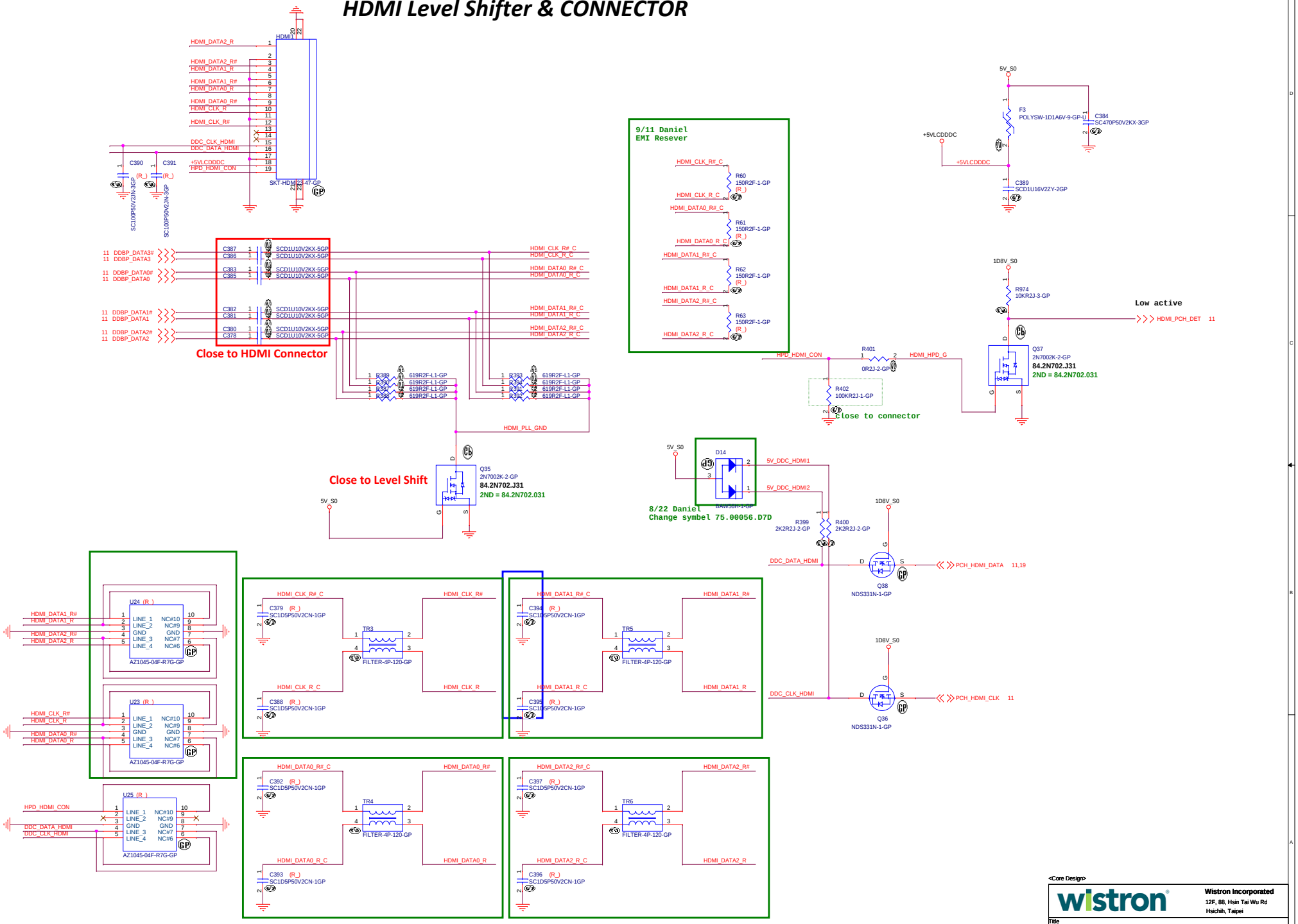
Hsichih, Taipei

Title: LCD CONN/CVR
Size: Custom | Document Number: Low Cost AIO | Rev: 1A
Date: Friday, September 12, 2014 | Sheet 29 of 62

HDMI Level Shifter & CONNECTOR



<Core Design>

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Hsichih, Taipei

Title	HDMI OUT	
Size C	Document Number Low Cost AIO	Rev 1A
Date: Friday, September 12, 2014	Sheet 30 of 62	

TBD

<Core Design>

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Hsichih, Taipei

Title: HDMI IN

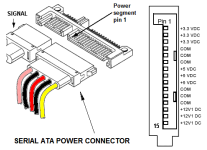
Size	Document Number	Rev
C	Low Cost AIO	1A

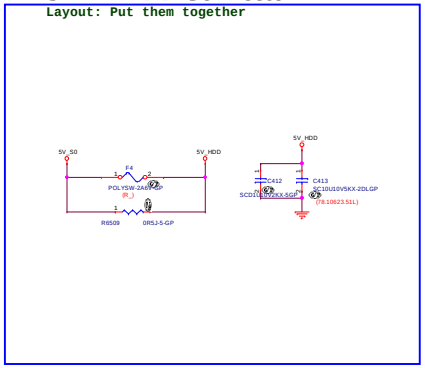
Date: Friday, September 12, 2014 Sheet 31 of 62

SSID = SATA

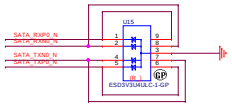
SATA HDD Connector

Layout: Put them together

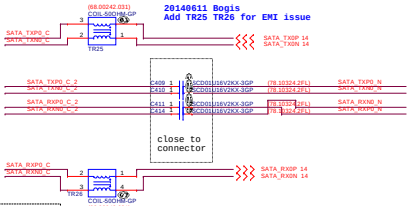


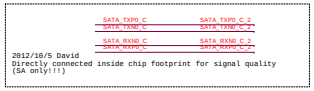


20140514 Nick add U15 TVS for EMI
20140516 Nick swap U15 net name



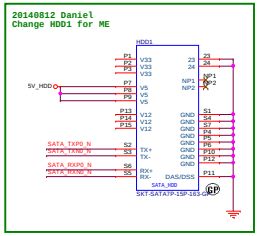
20140611 Bogis
Add TR25 TR26 for EMI issue

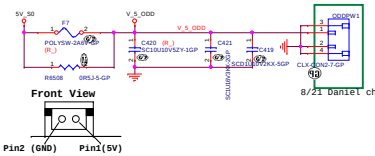




2012/10/10 David
SA create a temporary symbol (ZZ.08520.003) for re-driver co-lay,
If confirm that re-driver is required, need change symbol to
normal type (71.08520.003) , and cut short-pad inside the IC

20140812 Daniel
Change HDD1 for ME

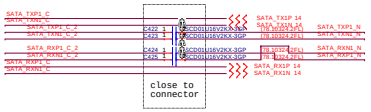


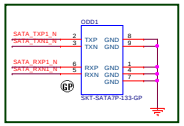


8/21 Daniel changes to 020.D0007.0102

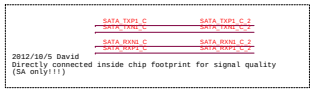
2012/10/23 David
change to PS8520 for SATA gen3

2013/05/21 David
Deleted SATA re-driver since
test PASS and to fix P/R issue

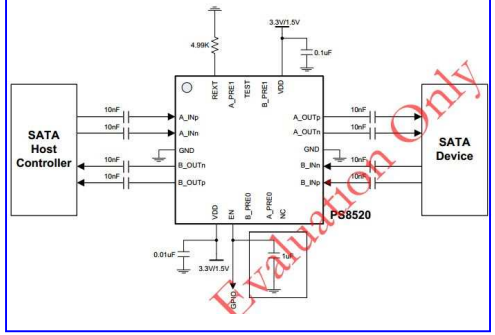


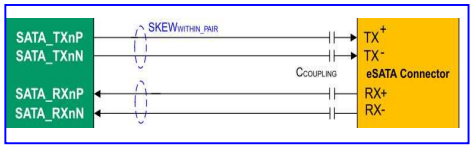


2012/10/24 David
EN pin and TEST pin can be floating for normal working.
Pin20 (REXT) should be connect to 4.99K ohm to GND



2012/10/10 David
SA create a temporary symbol (ZZ.08520.003) for re-driver co-lay,
If confirm that re-driver is required, need change symbol to
normal type (71.08520.003) , and cut short-pad inside the IC



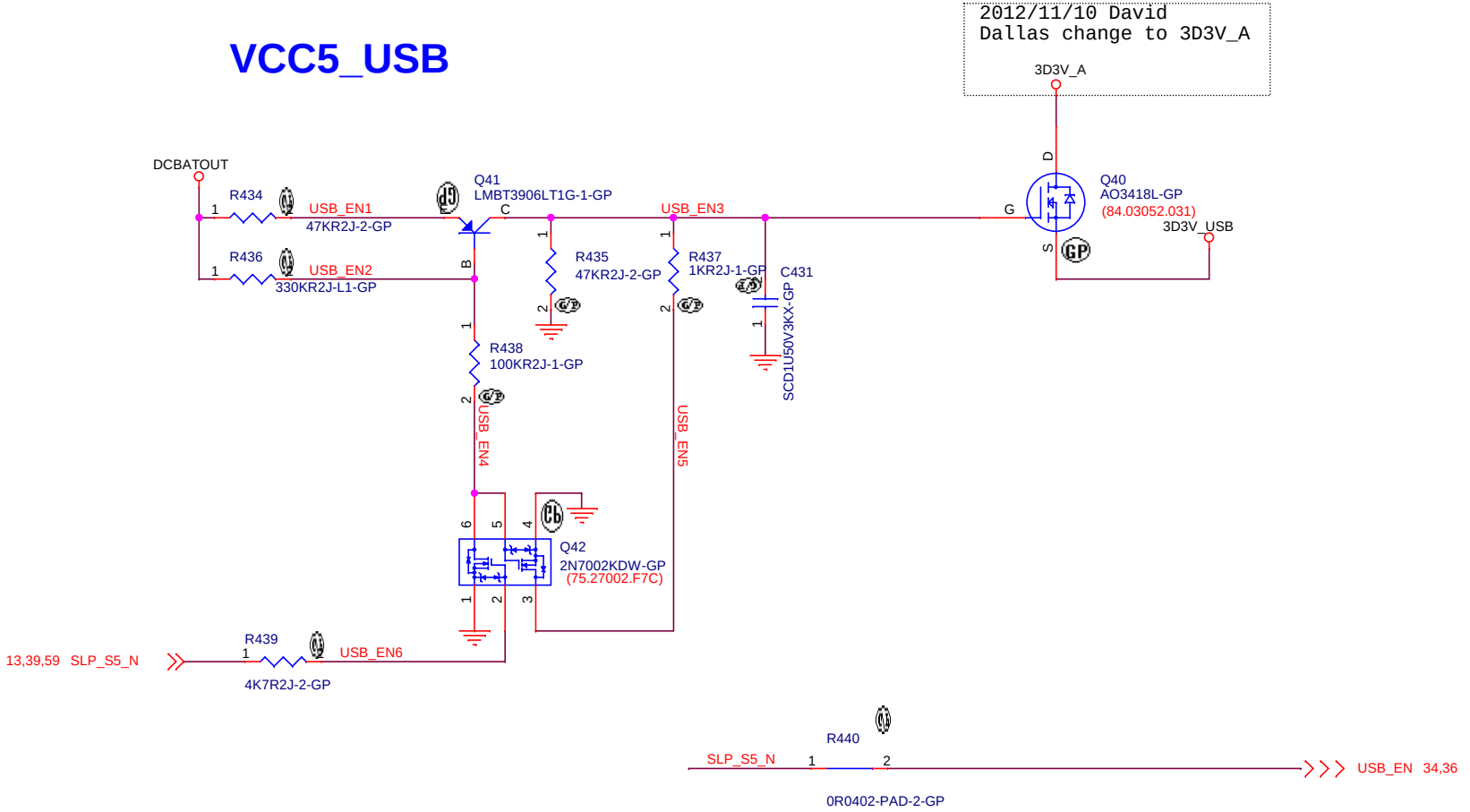


<Variant Name>
wistron
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
File
HDD/ODD
Size D
Document Number
Low Cost AIO
Rev 1A
Date: Friday, September 12, 2014
Sheet 32 of 63

SSID = USB

VCC5_USB

2012/11/10 David
Dallas change to 3D3V_A

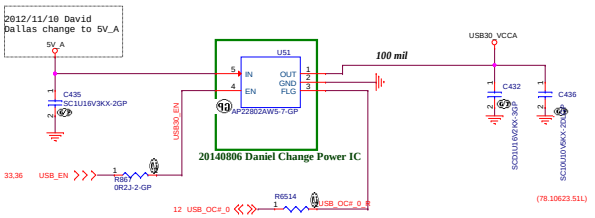


<Core Design>

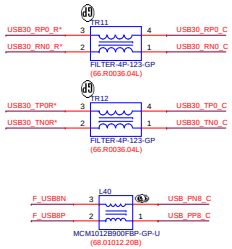
wistron	Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	USB 2.0 Power SW
Size: Custom	Document Number: Low Cost AIO
Rev	1A
Date: Friday, September 12, 2014	Sheet 33 of 62

20140508 Nick change F7 to 074.07549.0099

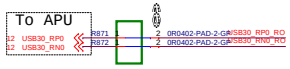
2012/11/10 David
Dallas change to 5V_A



0ohm: 66.R0036.04L



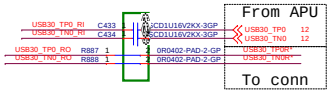
To APU

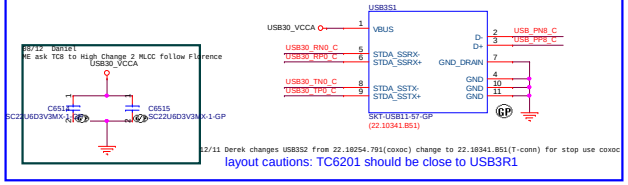


2012/07/12
If use NXP
R126,R136= 0ohm
R81=NC

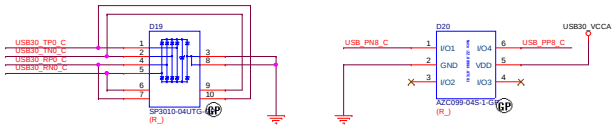
If use TI
R126,R136,R81= 0ohm

2012/10/5 David
Directly connected inside chip footprint for signal quality
(SA only!!!)

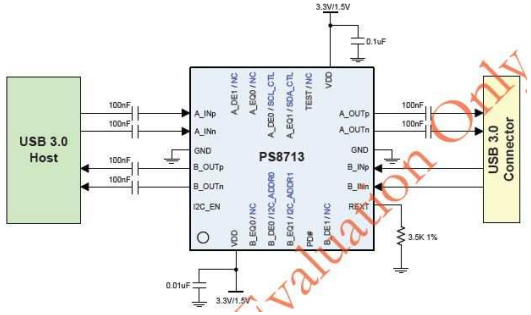




layout cautions: TC6201 should be close to USB3R1



USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	



<Core Design>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

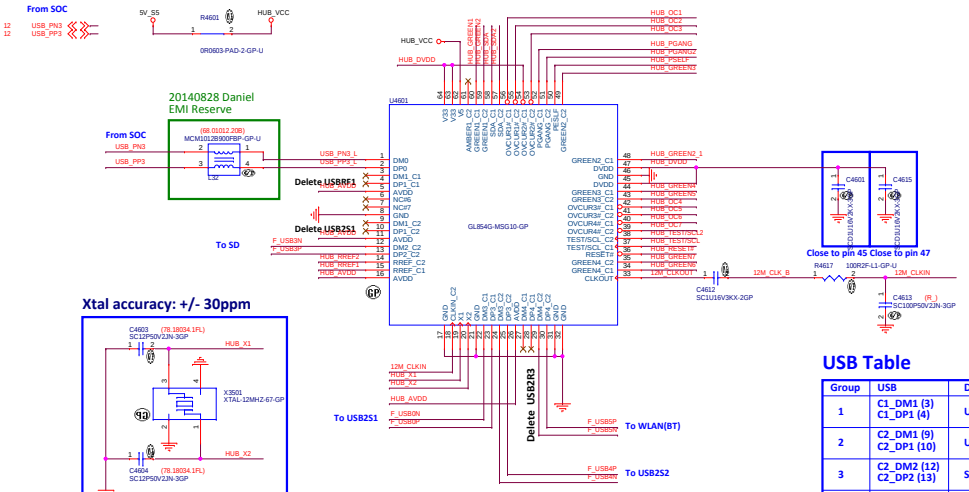
Title: USB 3.0 Port

Size: Custom | Document Number: Low Cost AIO | Rev: 1A

Date: Friday, September 12, 2014 | Sheet 34 of 62

GL850G
Enable/Disable USB output port: D+/D- pull high 1K to disable USB port
Set USB port to be internal (non-removable): set OC pin is floating
Set USB port to be external (removable): set OC pin is non-floating (pull high 10K to 3.3V or USB OC#)

GL852G
Enable/Disable USB output port: setting by EEPROM
Set USB port to be internal (non-removable) or external (removable): setting by EEPROM



Xtal accuracy: +/- 30ppm

Close to GL854G pin19/20

1st: 82.30006.641
2nd: 82.30006.501

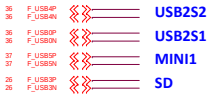
Any Green#=1 -> Non-Removable (Compound device)

	PGreen1	PGreen2	PGreen3	PGreen4	PGreen5	PGreen6	PGreen7
Non-Removable	X	1	1	1	1	1	1

Note -- x : Not support
1 : Pull up 15K to DVDD
PGreen2 & PGreen3 do not set to 1 concurrently

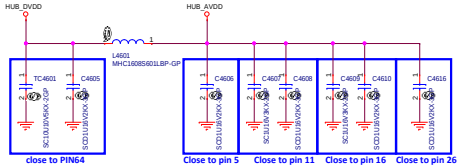
USB Table

Group	USB	Device	
1	C1_DM1 (3) C1_DP1 (4)	USBRF1	Delete
2	C2_DM1 (9) C2_DP1 (10)	USB2S1	Delete
3	C2_DM2 (12) C2_DP2 (13)	SD	internal
4	C1_DM3 (22) C1_DP3 (23)	USB2S1	external
5	C2_DM3 (24) C2_DP3 (25)	USB2S2	external
6	C1_DM4 (27) C1_DP4 (28)	USB2R3	Delete
7	C2_DM4 (29) C2_DP4 (30)	MINI1	internal

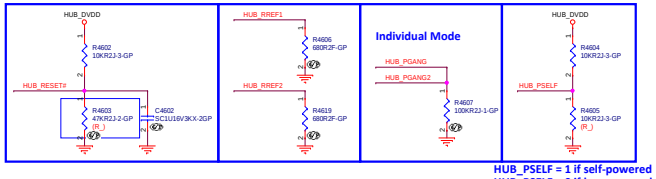


Internal Power

(Hub Internal VR output from pin 63/64 V33 = HUB_DVDD)



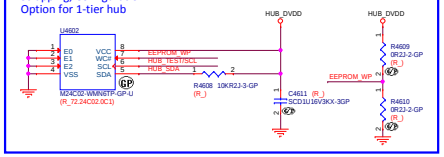
Fine tune resistor value for USB driving
590ohm: 64.59005.6DL



HUB_PSELF = 1 if self-powered
HUB_PSELF = 0 if bus-powered

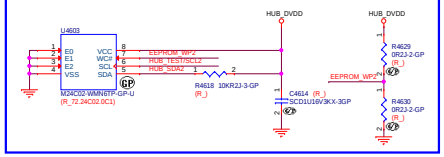
EEPROM

Option:
24C02 for VID, PID,
Strapping, Configuration.
Option for 1-tier hub

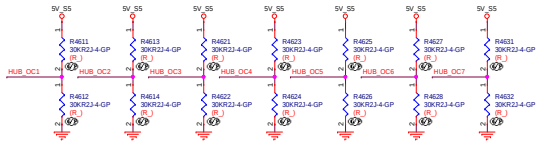


EEPROM

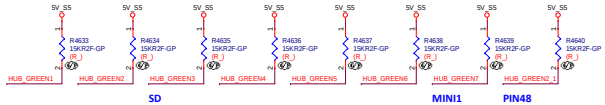
Option for 2-tier hub



Over Current



Green LED



<Core Design>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: USB HUB IC
Size: Custom
Document Number: Low Cost AIO
Rev: 1A
Date: Friday, September 12, 2014
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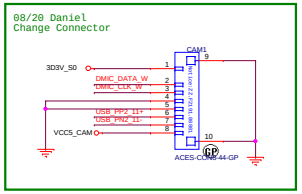
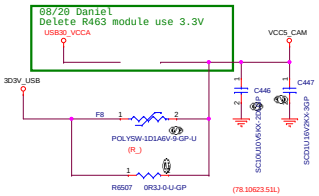
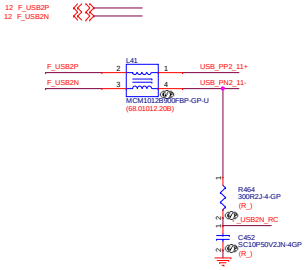
SSID =USB2.0

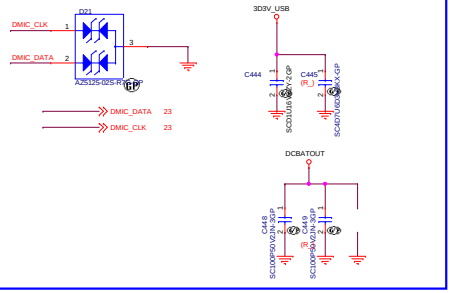


USB Port2 -> WEB CAM





DMIC Connector



USB Port 1 -> Delete TOUCH

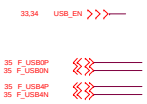
Mas touch Connector Pin Define

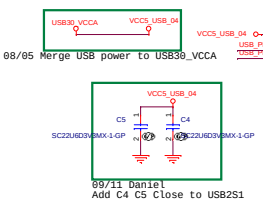
PIN NO.	PIN Name
1	VUSB
2	D-
3	D+
4	GND
5	Shield

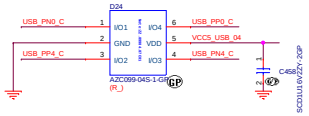
TPK touch Connector Pin Define

PIN NO.	PIN Name
1	VUSB
2	D-
3	D+
4	GND
5	Shield

USB Port -> Side I/O







<variant_name>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

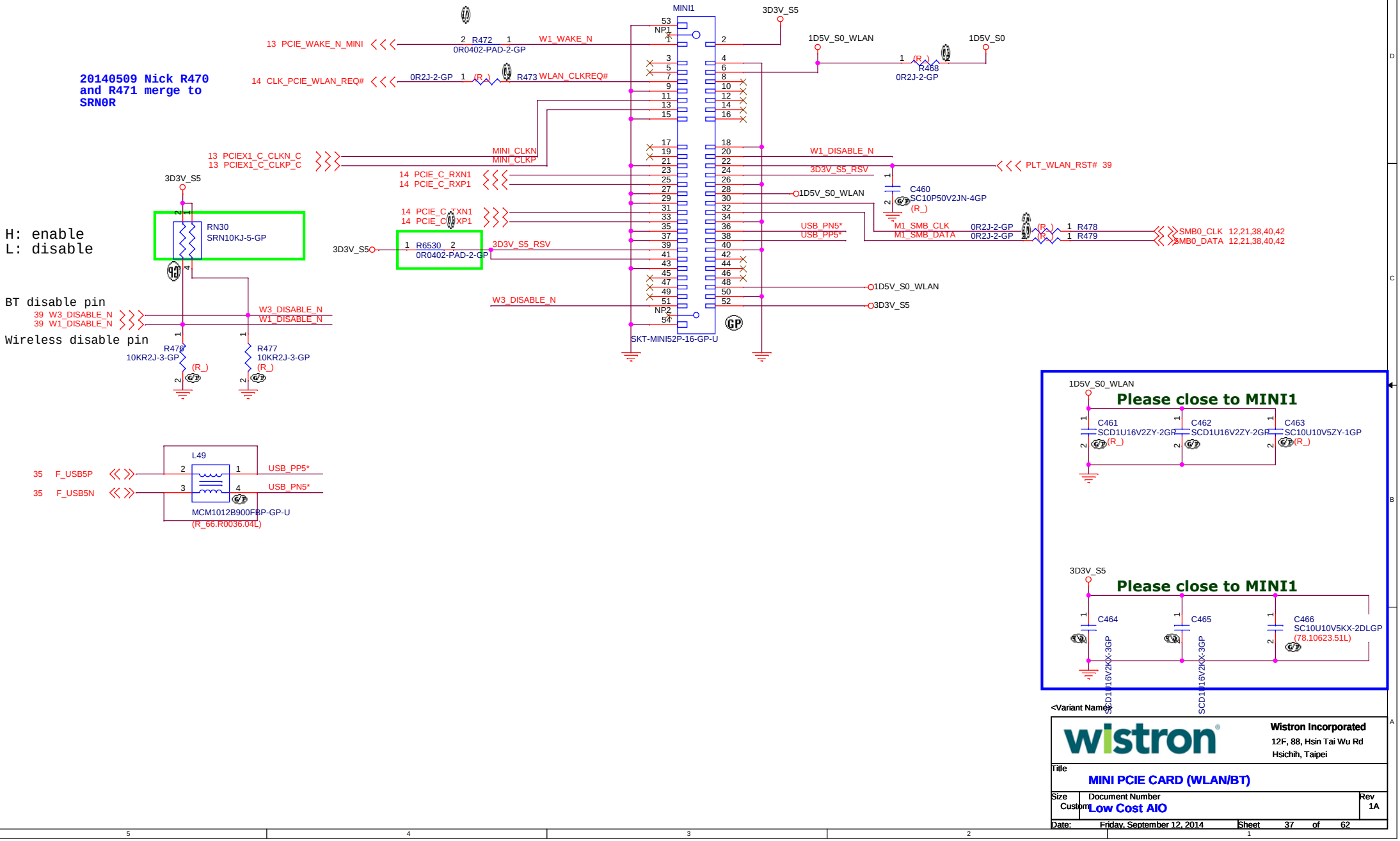
Title: REAR USB / TOU / WEBCAM

Size: Custom | Document Number: Low Cost AIO | Rev: 1A

Date: Friday, September 12, 2014 | Sheet 36 of 62

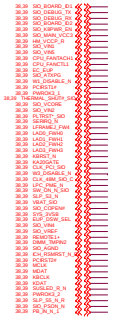
SSID = Wireless and Bluetooth

Mini Card Connector(Wireless LAN+BT)



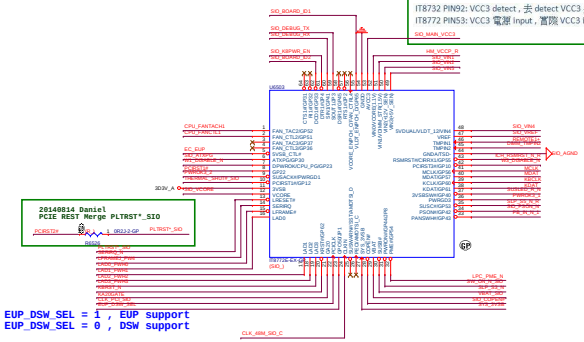
Wistron Incorporated	12F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	MINI PCIE CARD (WLAN/BT)
Size: Custom	Document Number: Low Cost AIO
Rev	1A
Date: Friday, September 12, 2014	Sheet 37 of 62

Colay to ITE8732

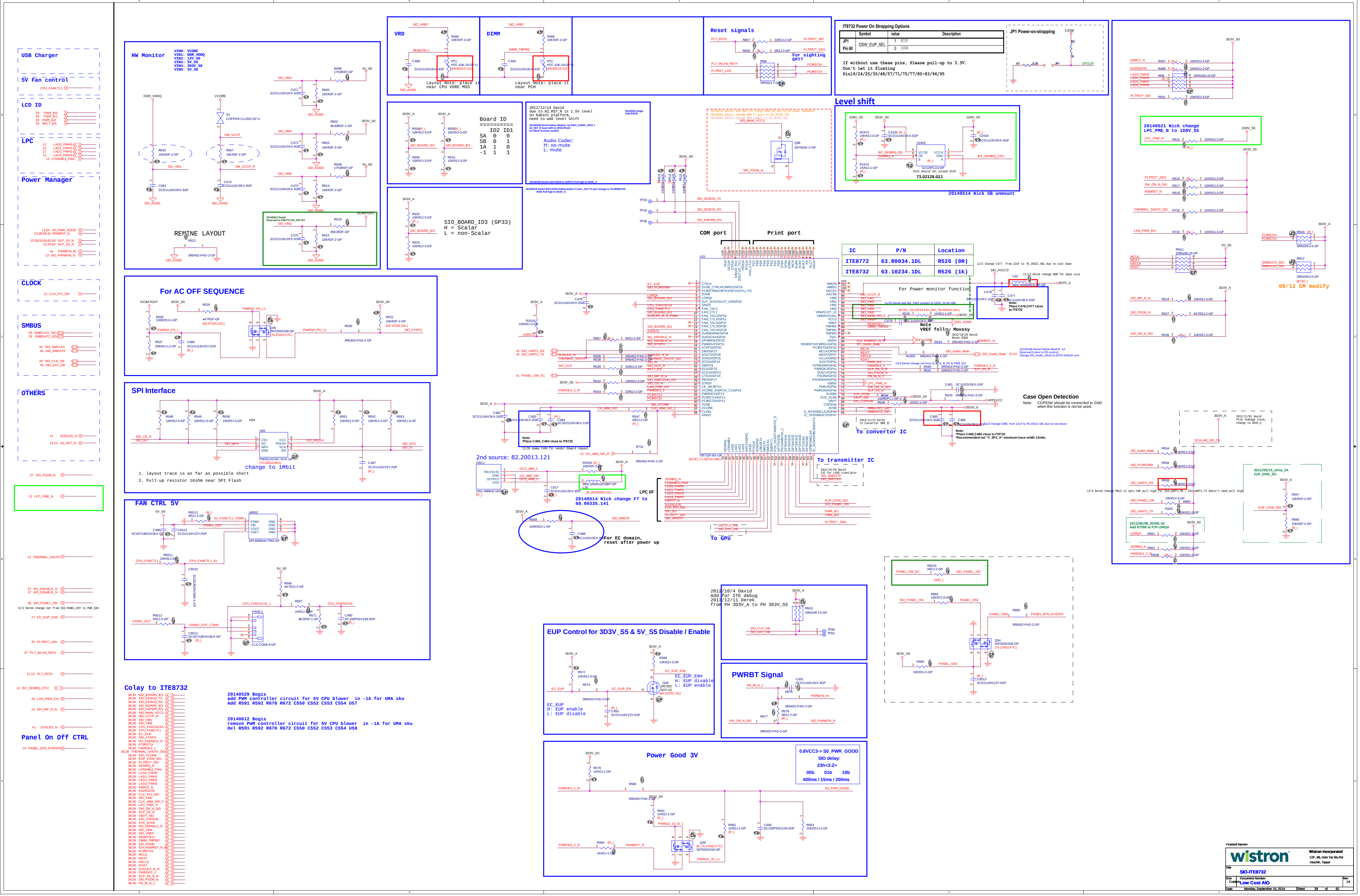


IC	P/N	Location
ITE8772	63.R0034.1DL	R526 (0R)
ITE8732	63.10234.1DL	R526 (1k)

IT8732 PIN92: VCC3 detect , 去 detect VCC3 是否有 in ,IC 內部有電路去做偵測 , 需接 1K 電阻
IT8772 PIN53: VCC3 電源 input , 實際 VCC3 in , 外部不用接 1K 電阻



Wistron Incorporated 13F, 88, Hsin Tai Wu Rd Hsichih, Taipei		
File: SCALAR-RTD2486		
Size: Custom	Document Number: PLow Cost AIO	Rev: 1A
Date: Friday, September 19, 2014	Sheet 38 of 63	



USB Charger
5V Fan control
LCD ID
LPC
Power Manager
CLOCK
SMBUS
OTHERS
Panel On Off CTRL
HW Monitor
VIN0: VCORE
VIN1: DDR_VDDQ
VIN2: 12V_S0
VIN3: 5V_S5
VIN4: 3D3V_S0
VIN5: 5V_S0
REMINE LAYOUT
VRD
Layout Note: place it near CPU VCORE MOS
DIMM
Layout Note: place it near PCH
Reset signals
For sighting GP77
IT8732 Power On Strapping Options
JP1 Power-on-strapping
If without use these pins, Please pull-up to 3.3V.
Don't let it floating
Pin19/24/25/30/48/57/71/75/77/80~83/96/95
Board ID
SIO_BOARD_ID3 (GP33)
H = Scalar
L = non-Scalar
Audio Codec:
H: no-mute
L: mute
Level shift
20140521 Nick change
LPC_PME_N to 1D8V_S5
20140514 Nick SB unmount
For AC OFF SEQUENCE
COM port
Print port
IC
P/N
Location
ITE8772
63.R0034.1DL
R526 (0R)
ITE8732
63.10234.1DL
R526 (1k)
For Power monitor function
Case Open Detection
SPI Interface
change to 1Mbit
1. layout trace is as far as possible short
2. Pull-up resistor 1Kohm near SPI Flash
2nd source: 82.20013.121
20140514 Nick change F7 to 68.00335.141
LPC I/F
To convertor IC
To transmitter IC
To GPU
For EC domain, reset after power up
FAN CTRL 5V
09/12 CM modify
Colay to IT8732
20140529 Bogis
add PWM controller circuit for 5V CPU blower in -1A for UMA sku
Add R591 R592 R670 R672 C550 C552 C553 C554 U57
20140612 Bogis
remove PWM controller circuit for 5V CPU blower in -1A for UMA sku
Del R591 R592 R670 R672 C550 C552 C553 C554 U58
EUP Control for 3D3V_S5 & 5V_S5 Disable / Enable
EC_EUP
H: EUP enable
L: EUP disable
EC_EUP_EN#
H: EUP disable
L: EUP enable
2013/10/4 David
Add for ITE debug
2013/12/11 Derek
from PH 3D3V_A to PH 3D3V_S5
PWRBT Signal
Power Good 3V
0.8VCC3-> S0_PWR_GOOD
SIO delay:
23h<3:2>
00b 01b 10b
400ms / 15ms / 200ms
wistron
Wistron Incorporated
SIO-ITE8732
Low Cost AIO
Monday, September 15, 2014
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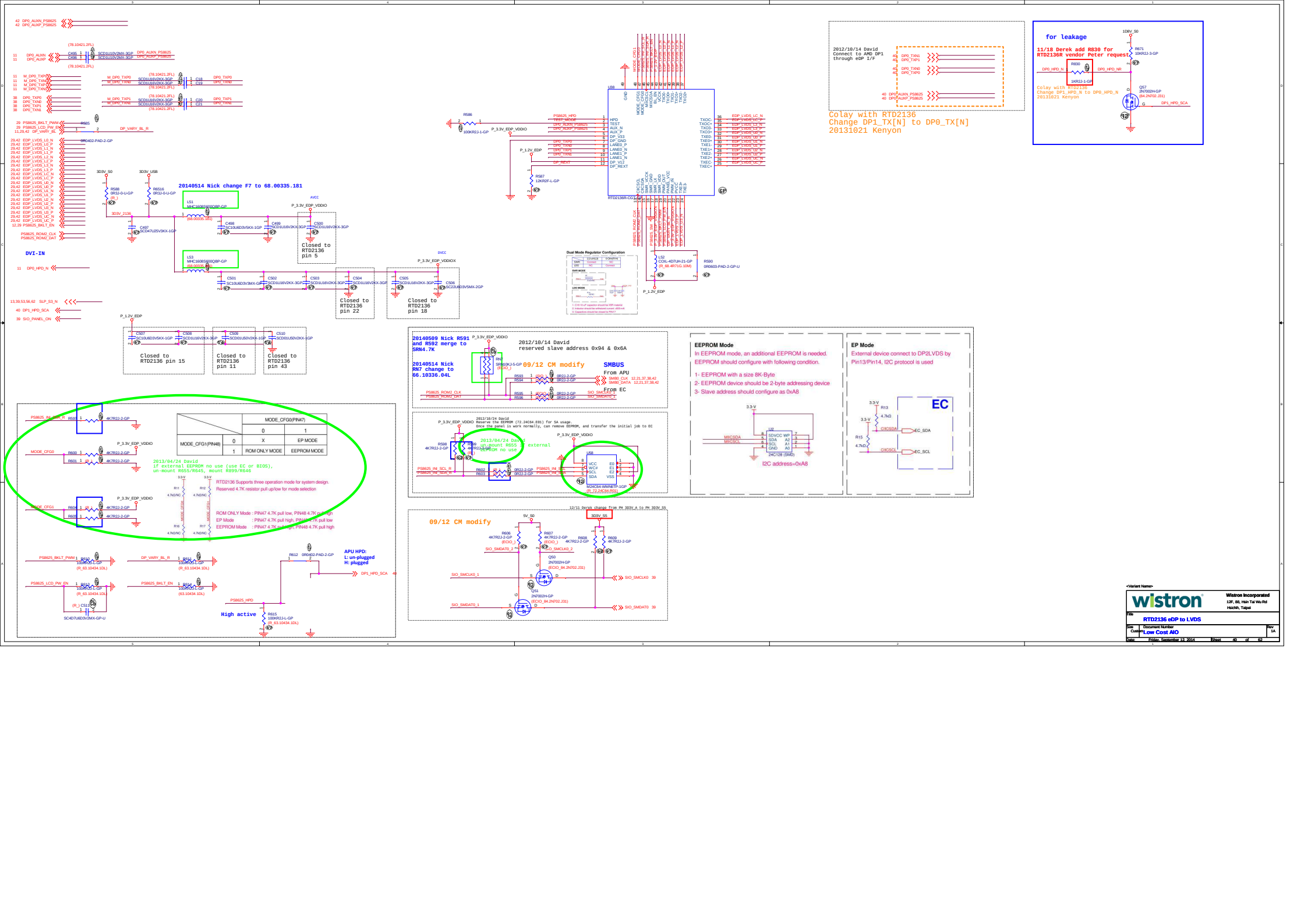
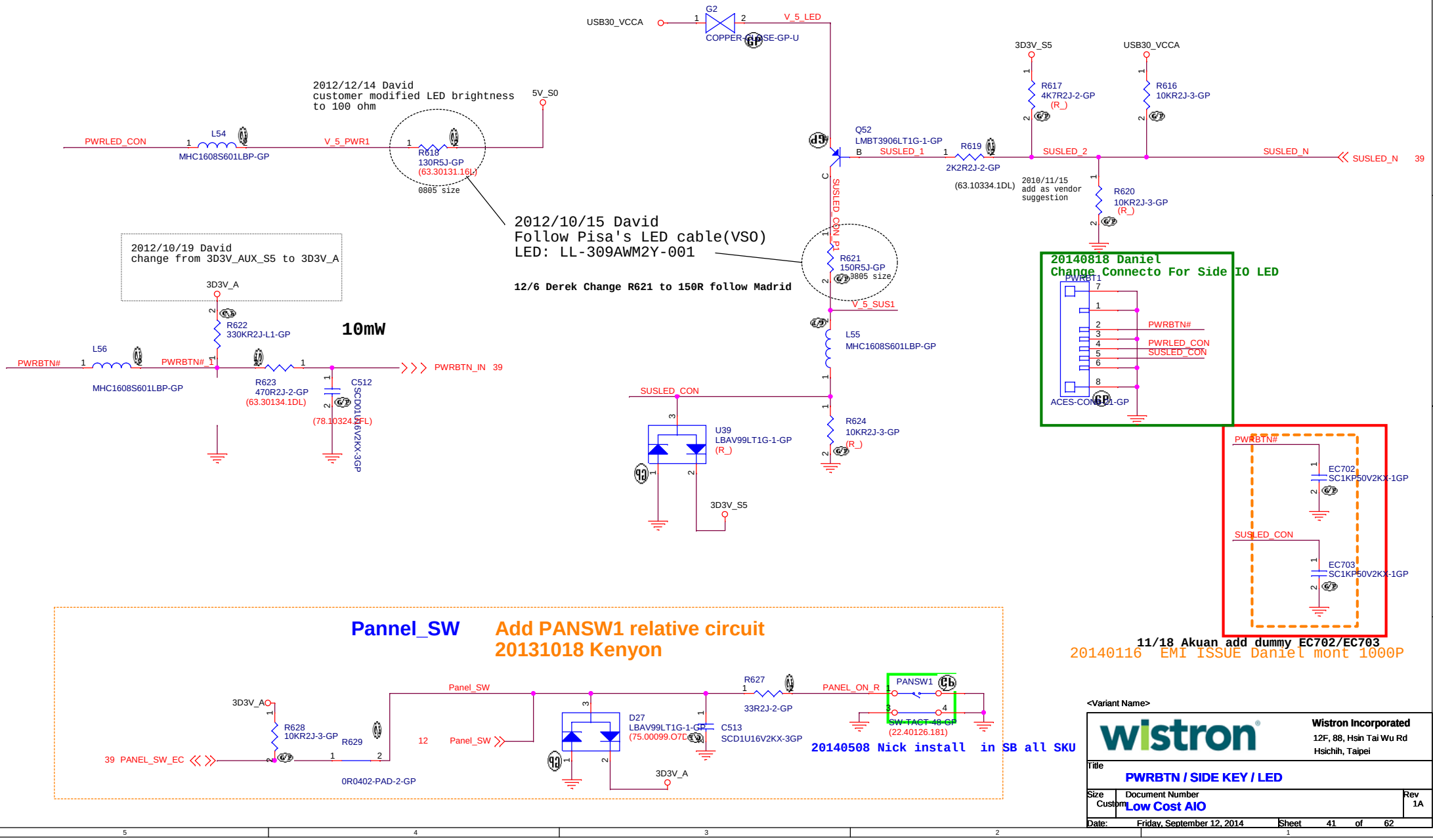

DVI-IN
20140514 Nick change F7 to 68.00335.181
Closed to RTD2136 pin 5
Closed to RTD2136 pin 22
Closed to RTD2136 pin 18
Closed to RTD2136 pin 15
Closed to RTD2136 pin 11
Closed to RTD2136 pin 43
2012/10/14 David Connect to AMD DP1 through eDP I/F
Colay with RTD2136 Change DP1_TX[N] to DP0_TX[N] 20131021 Kenyon
for leakage
11/18 Derek add R830 for RTD2136R vendor Peter request
Colay with RTD2136 Change DP1_HPD_N to DP0_HPD_N 20131021 Kenyon
20140509 Nick RS91 and R592 merge to SRN4.7K
20140514 Nick RN7 change to 86.10336.04L
2012/10/14 David reserved slave address 0x94 & 0x6A
09/12 CM modify
SMBUS
From APU
From EC
EEPROM Mode
In EEPROM mode, an additional EEPROM is needed.
EEPROM should configure with following condition.
1- EEPROM with a size 8K-Byte
2- EEPROM device should be 2-byte addressing device
3- Slave address should configure as 0xA8
I2C address=0xA8
EP Mode
External device connect to DP2LVDS by Pin13/Pin14, I2C protocol is used
EC
2013/04/24 David
if external EEPROM no use (use EC or BIOS), un-mount R655/R645, mount R899/R646
RTD2136 Supports three operation mode for system design.
Reserved 4.7K resistor pull up/low for mode selection
ROM ONLY Mode : PIN47 4.7K pull low, PIN48 4.7K pull high
EP Mode : PIN47 4.7K pull high, PIN48 4.7K pull low
EEPROM Mode : PIN47 4.7K pull high, PIN48 4.7K pull high
MODE_CFG(PIN47)
MODE_CFG1(PIN48)
EP MODE
ROM ONLY MODE
EEPROM MODE
APU HPD:
L: un-plugged
H: plugged
High active
09/12 CM modify
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
RTD2136 eDP to LVDS
Low Cost AIO
Friday, September 12, 2014


USB30_VCCA
G2
COPPER-BASE-GP-U
V_5_LED
3D3V_S5
USB30_VCCA
R617
4K7R2J-2-GP
(R_)
R616
10KR2J-3-GP
2012/12/14 David
customer modified LED brightness
to 100 ohm
5V_S0
PWRLED_CON
L54
MHC1608S601LBP-GP
V_5_PWR1
R618
130R5J-GP
(63.30131.16L)
0805 size
Q52
LMBT3906LT1G-1-GP
B
SUSLED_1
R619
2K2R2J-2-GP
(63.10334.1DL)
2010/11/15
add as vendor
suggestion
SUSLED_2
SUSLED_N
SUSLED_N 39
R620
10KR2J-3-GP
(R_)
2012/10/15 David
Follow Pisa's LED cable(VSO)
LED: LL-309AWM2Y-001
12/6 Derek Change R621 to 150R follow Madrid
SUSLED_CON_P1
R621
150R5J-GP
0805 size
20140818 Daniel
Change Connecto For Side IO LED
PWRBT1
PWRBTN#
PWRLED_CON
SUSLED_CON
ACES-CON2-GP
2012/10/19 David
change from 3D3V_AUX_S5 to 3D3V_A
3D3V_A
R622
330KR2J-L1-GP
10mW
L56
PWRBTN#
PWRBTN#_1
MHC1608S601LBP-GP
R623
470R2J-2-GP
(63.30134.1DL)
C512
SCD01U16V2KX-3GP
(78.10324.1FL)
PWRBTN_IN 39
V_5_SUS1
L55
MHC1608S601LBP-GP
SUSLED_CON
U39
LBAV99LT1G-1-GP
(R_)
R624
10KR2J-3-GP
(R_)
3D3V_S5
PWRBTN#
EC702
SC1KP50V2KX-1GP
SUSLED_CON
EC703
SC1KP50V2KX-1GP
11/18 Akuan add dummy EC702/EC703
20140116 EMI ISSUE Daniel mont 1000P
Pannel_SW
Add PANSW1 relative circuit
20131018 Kenyon
3D3V_A
R628
10KR2J-3-GP
R629
0R0402-PAD-2-GP
39 PANEL_SW_EC
12
Panel_SW
Panel_SW
D27
LBAV99LT1G-1-GP
(75.00099.07D)
C513
SCD1U16V2KX-3GP
3D3V_A
R627
33R2J-2-GP
PANEL_ON_R
PANSW1
SW-TACT-48-GP
(22.40126.181)
20140508 Nick install in SB all SKU
<Variant Name>
wistron
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
PWRBTN / SIDE KEY / LED
Size
Custom
Document Number
Low Cost AIO
Rev
1A
Date:
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62

TBD

<Variant Name>

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Hsichih, Taipei

Title: XDP

Size: B

Document Number: Low Cost AIO

Rev: 1A

Date: Friday, September 12, 2014

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Hsichih, Taipei

Title: SCALAR POWER

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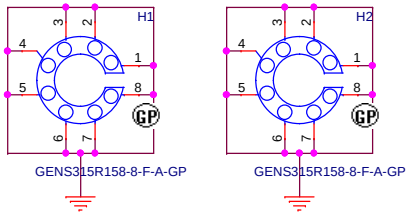
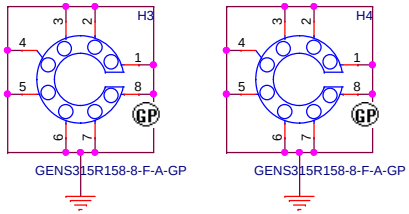
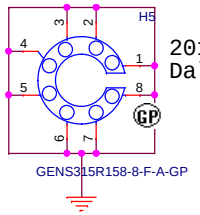
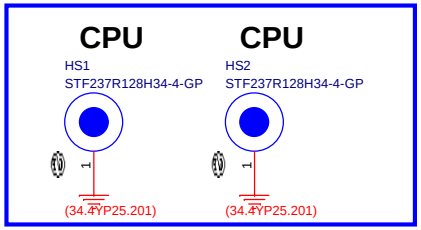


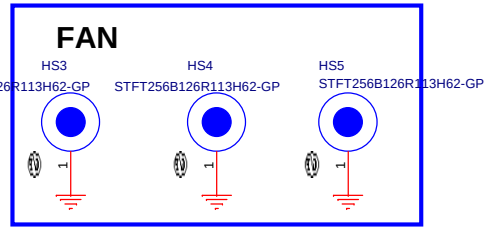
ZZ.SCREW.541





2012/10/2 David
Dallas no Chrome OS





<Core Design>

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Hsichih, Taipei

Title: STAND OFF / HOLE / EMI CAP

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Material part

LGA115x CPU SOCKET Symbol

Vendor:LOTES
P/N:22.78003.011

Vendor:FOXCONN
P/N:22.78006.001

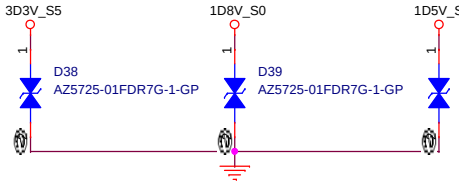
Vendor: LOTES
P/N:22.78002.011
Thickness: max 2.2mm (含mylar及螺孔高)

Vendor: FOXCONN
P/N:22.78006.011
Thickness:2.0mm(含mylar)

Vendor:LOTES
P/N: 22.78005.171

Vendor:FOXCONN
P/N: 22.78005.161

2013/03/19 David
Removed CPU socket & back plate & cover



20140618 Bogis
add ESD component
D38 for 3D3V_S5
D39 for 1D8V_S0
D40 for 1D5V_S0

Vendor:LOTES
P/N: 22.78005.171

Vendor:FOXCONN
P/N: 22.78005.161

LABEL

LBL1
LABEL
(40.3BZ24.001)

LBL2
LABEL
(R_)

LBL3
LABEL
(R_)

MB serial NO# and MAC address
40.3KP03.001 -> 35 x 15mm
45.41107.011 -> 70 x 8mm
45.41115.001 -> 34 x 13.5mm for aDallas
40.3BZ24.001 -> 30 x 15mm
09/24 Daniel
Change to 30x15 mm

HeatSink Symbol

2013/03/19 David
Removed HeatSink

Vendor
P/N:
60.3ET05.001
60.3ET05.011
60.3ET05.021

Stand-off

2013/03/19 David
Removed Stand-off
since already exist

34.3KF01.001 for 5.2mm slot 62.10043.G11
34.3HJ03.001 for 9.0mm slot 62.10043.E41

Battery Symbol

BTT2
BATTERY CR2032
(23.20068.001)

Vendor
P/N:
23.20068.001
23.20023.311
23.22063.001

PCB Symbol

<Core Design>

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Title: HeatSink/Battery/etc

Size: B | Document Number: Low Cost AIO | Rev: 1A

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TBD

<Core Design>

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Title: GPU(1/5): PCI Express

Size: C | Document Number: Low Cost AIO | Rev: 1A

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TBD

<Core Design>

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12F, 88, Hsin Tai Wu Rd
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Title: GPU(2/5): IFB(IO)

Size: Custom | Document Number: Low Cost AIO | Rev: 1A

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TBD

<Core Design>

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Hsichih, Taipei

Title: GPU(3/5): MEMORY FBA

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TBD

GPIO	GF117
GPIO 0	FAN_PWM/FB_CLAMP/DEBUG Service
GPIO 1	MEM_VDD_CTL
GPIO 2	UNUSED
GPIO 3	UNUSED
GPIO 4	UNUSED
GPIO 5	Reserved
GPIO 6	FB_CLAMP_TGL_REQ
GPIO 7	3DVision(UNUSED)
GPIO 8	GPU Overtemp
GPIO 9	GPU Thermal Alert
GPIO 10	FB Vref Control
GPIO 11	NVVDD PWM_VID
GPIO 12	PWR_Level AC Detect
GPIO 13	UNUSED(No Need to Set in VBIOS)
GPIO 14	N/A on Package
GPIO 15	N/A on Package
GPIO 16	N/A on Package
GPIO 17	N/A on Package
GPIO 18	N/A on Package
GPIO 19	N/A on Package
GPIO 20	N/A on Package
GPIO 21	N/A on Package

Table 115. GB2-64 and GB4-128 GPIO Description

Pin Name	Normal Function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	FB_CLAMP_WOH	I	FB Clamp monitor	
GPIO1	MEM_VDD_CTL	O	Memory VDD VID	MEM VID: Strap to boot FBVDD/Q
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100 K pull-down
GPIO3	LCD_VCC	O	Panel Power Enable	LCD_VCC: 100k pull-down
GPIO4	LCD_BLEN	O	Panel Backlight Enable	100 K pull-down
GPIO5	Reserved			
GPIO6	FB_CLAMP_TGL_REQ	O	Active low FB Clamp toggle request	
GPIO7	3DVision	O	3D Vision L/R signal	100 K pull-down
GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature	100 K pull-up
GPIO9	ALERT	I/O	Active Low Thermal Alert	100 K pull-up
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 K pull-down
GPIO11	PWM_VID	O	GPU Core VDD PWM control signal	
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100 K pull-up
GPIO13	PSI	O	Phase Shedding	PSI: 10k pull-up to enable two phase.
GPIO14	HPD_A		Hot Plug Detect for IFPA used as DisplayPort or for IFPAB when used as Dual Link DVI	See Figure 78
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	See Figure 78
GPIO16	FRM_LCK	O	JT Frame Lock signal	
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	See Figure 78
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	See Figure 78
GPIO19	HPD_F or HPD_B	I	Hot Plug Detect for IFPF or for IFPB used as DisplayPort	See Figure 78
GPIO20	Reserved			
GPIO21	Reserved			

+ GPIO20 and GPIO21 are only available on N14M-LP/-GS/-WE/-WS & N14P-GV/-GV2
+ The greyed out section of Table 107 indicates GPIOs that are not available for N14M-GE/-GL

GPIO0, GPIO6 is for GC6 feature, no need to connect since this project won't support GC6.
GPIO1 is for FB voltage control, no need to connect since the FBVDDQ is 1.5V for all P-States.
GPIO12 : High->AC Mode;Low->Battery Mode enter slow down functionpull for power saving.Recommand:Pull-High for AC mode.
GPIO13 PSI :Change Phase from two to one, and thean enter slow down functionpull for power saving.

STRAP

QVL1: Hynix (KN.2GB0G.038)+R488, R490, R489, R925(64.10025.6DL)
QVL2: Micron (KN.2GB04.022)+R483, R490, R929, R934 (64.10025.6DL)

STRAP PIN MODE TABLE	
PIN NAME	BINARY BRINGUP
STRAP0	3GIO_PADCFG_LUT_ADR0
STRAP1	3GIO_PADCFG_LUT_ADR1
STRAP2	3GIO_PADCFG_LUT_ADR2
STRAP3	3GIO_PADCFG_LUT_ADR3
STRAP4	PCI_MAX_SPEED
ROM_SCLK	SMB_ALT_ADDR
ROM_SI	SUB_VENDOR
ROM_SO	VGA_DEVICE

NOTE 2: See table 1 for the correct value/location of the strap resistor for the desired modes

NOTE 3: Bring-up SKU(s) have jumper configurable subvendor and DEVID_4 settings see the ROM_SCLK STRAP

Table 1. N14M-GE/GL DDR3 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
128M×16 DDR3	Micron	0x1	1.5 V/ 1.5 V	MT41J128M16JT-093G:K	1000	1150	Production Candidate
				MT41J128M16JT-107G:K	900	1150	Production Candidate
	Samsung	0x5	1.5 V/ 1.5 V	K4W2G1646E-BC1A	1000	1204	Production Candidate
				K4W2G1646E-BC11	900	1204	Production Candidate
	Hynix	0x6	1.5V/ 1.5V	H5TQ2G63DFR-H0C	1000	N/A	Production Candidate
				H5TQ2G63DFR-11C	900	N/A	Production Candidate

Table 2. N14M-GE/GL DDR3 Recommended Memories 256Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
256M×16 DDR3	Samsung	0xB	1.5 V/ 1.5 V	K4W4G1646B-HC11	900	N/A	Production Candidate
	Micron	0xD	1.5 V/ 1.5 V	MT41K256M16HA-107G:E	900	N/A	Production Candidate
	Hynix	0x3	1.5V/ 1.5V	H5TQ4G63MFR-11C	900	N/A	Production Candidate
		0x4		H5TQ4G63AFR-11C		N/A	Post-Production Candidate

Table 122 Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10k Ω	Pull-down to GND
ROM_SI	SUB_VENDOR	10k Ω	Pull-up to 3V3 if VBIOS ROM exists Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10k Ω	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10k Ω	See Note below
STRAP1	RAM_CFG[1]	10k Ω	See Note below
STRAP2	RAM_CFG[2]	10k Ω	See Note below
STRAP3	RAM_CFG[3]	10k Ω	See Note below
STRAP4	PCIE_MAX_SPEED	10k Ω	Pull-down to GND

Refer to the latest version of N14M-GE/-GL *Memory Recommended Vendor List* for the specific setting for each memory type and configuration. Pull-up to 3V3 for binary '1' and pull-down to GND for binary '0'.

XTAL

THERMAL PROTECTION

VRAM ID [0-3]:

Mount	Un-mount	VRAM Type	P/N
R488、R490、R489、R924	R483、R486、R929、R934	Hynix 1GHz H5TC2G63FFR-11C	KN.2GB0G.038
R483、R490、R929、R934	R488、R486、R489、R924	MICRON 1GHz MT41J128M16JT-093G:K	KN.2GB04.022
R488、R486、R489、R924	R483、R490、R929、R934	SAMSUNG 1G K4W2G1646Q-BC1A	KN.2GB0B.040

Mount 10K 64.10025.6DL

VRAM ID [0-3]:

VRAM Type	P/N	0	1	2	3
Hynix 1G H5TC2G63FFR-11C	KN.2GB0G.038			V	V
	72.52G63.N0U	V	V		

VRAM ID [0-3]:

VRAM Type	P/N	0	1	2	3
Micron 1G MT41J128M16JT-093G:K	KN.2GB04.022	V			
	72.41128.10U		V	V	V

VRAM ID [0-3]:

VRAM Type	P/N	0	1	2	3
SAMSUNG 1G K4W2G1646Q-BC1A	KN.2GB0B.040		V	V	V
		V			

KN.2GB0B.041

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GPU(4/5): GPIO/STRAP

Low Cost AIO

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<Core Design>

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: GPU(5/5): PWR/GND

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VRAM Type	P/N
Hynix 1G H5TC2G63FFR-11C	KN.2GB0G.038

QVL1: Hynix (KN.2GB0G.038)+R221, R220, R231, R238 (64.10025.6DL)
QVL2: Micron (KN.2GB04.022)+R234, R238, R228, R219 (64.10025.6DL)

VRAM Type	P/N
Micron 1G MT41J128M16JT-093G:K	KN.2GB04.022

CHANNEL A:1GB DDR3

KN.2GB0G.038	2Gb DDR3 128M*16 900MHz SDRAM FBGA96P	Hynix - H5TC2G63FFR-11C
KN.2GB04.022	2Gb DDR3 128M*16 900MHz SDRAM FBGA96P	Micron - MT41J128M16JT-093G:K

TBD

FBCLK Termination place on VRAM side

128M*16 VRAM
KN.2GB0B.040 - Samsung K4W2G1646Q-BC1A
KN.2GB0G.038 - Hynix H5TC2G63FFR-11C

ORDERING INFORMATION

Part No.	Power Supply	Clock Frequency	Data Rate	Interface	Package
H5TC2G63FFR-11C	VDD/VDDQ=1.35V	900MHz	1.8Gbps/pin	SSTL-15	96ball FBGA
	VDD/VDDQ=1.5V	1.0GHz	2.0Gbps/pin		
H5TQ2G63FFR-N1C	VDD/VDDQ=1.5V	1.1GHz	2.2Gbps/pin		

Note) 1.35v speed part provides backward compatibility with the 1.5V DDR3.

1. Ordering Information

[Table 1] Samsung 2Gb gDDR3 Q-die ordering information table

Organization	gDDR3-1600(11-11-11)	gDDR3-1866(13-13-13)[3]	gDDR3L-1866(13-13-13)[3]	gDDR3-2133(14-14-14)[2]	Package
VDD	1.5V	1.5V	1.35V	1.5V	
128Mx16	K4W2G1646Q-BC12	K4W2G1646Q-BC11	K4W2G1646Q-BC1A		96 FBGA

NOTE
1. Speed bin is in order of CL-tRCD-tRP
2. Backward Compatible to gDDR3-1866(13-13-13), gDDR3-1600(11-11-11)
3. Backward Compatible to gDDR3-1600(11-11-11)

RMA_CFG [3:0]
Samsung - K4W2G1646E-BC11 (1000MHz) [0101]
Micron - MT41J128M16JT-093G:K (1000MHz) [0001]

<Core Design>

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Hsichih, Taipei

Title: GPU_DDR3 128MX16

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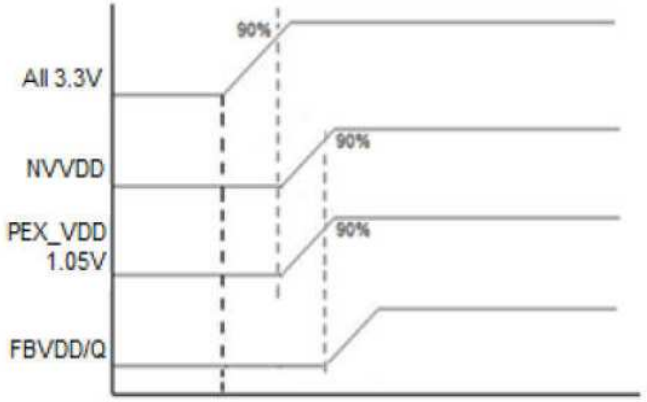
3.3V-->NVVDD&PEX_VDD(+V_VGA_CORE&+V_1P05_VGA)-->FBVDD/Q(+V_1P5_VGA)



Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

<Core Design>

wistron	Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title: GPU_POWER Sequence		
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3D3V_S0 to 3D3V_DELAY Transfer

TBD

2014/4/29 Nick change from 5V_S0 to 5V_S5

<Core Design>

Wistron Incorporated
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Hsichih, Taipei

Title: GPU_CTF/PPLAY/LDO/MVDD

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TBD

<Core Design>

Wistron Incorporated
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Title: GPU_VDDC_NCP81172

Size: D | Document Number: Low Cost AIO | Rev: 1A

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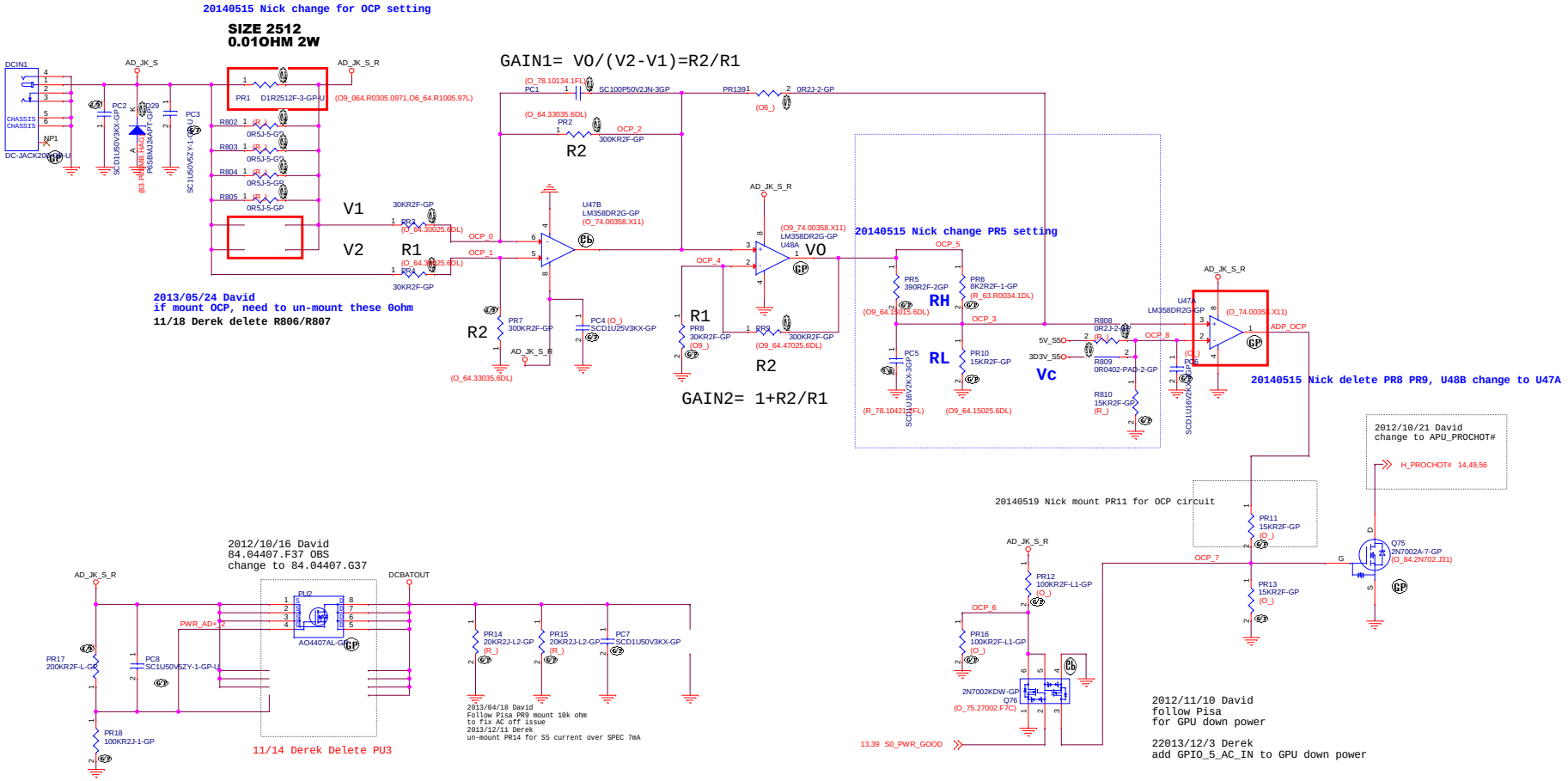
ANNIE solution



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wistron	Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title: PWR_DCIN JACK		
Size: Custom	Document Number: Low Cost AIO	Rev: 1A
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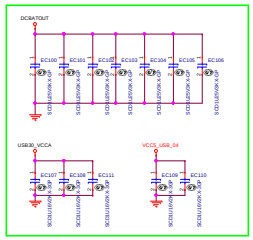

20140514 Nick SB add for EMI
20140516 Nick SB add for EMI

084.04378.0037 SM4378N
Vgs @ 4.5V,
Id = 20A,
Rds(on) = 9.2~12mohm,

084.04504.0037 SM4504N
Vgs @ 4.5V,
Id = 20A,
Rds(on) = 4.8~6.3mohm,

20140709 PTC2 can unmount and co-layout and change to 3pcs MLCC 78.10622.51L

VIN RIPPLE CURRENT Imax=2.46A

0.33uH, DCR=3.5~3.9 mohm, Idc=20A

Iomax=11A

47uF/25V, ESR=30mohm
Ripple Current=2800mA

B2buF/2.5V
ESR= 7mohm
Ripple Current =5000mA

1.0V
L=0.36uH
ΔI=((Vin-Vout)*Vout)/(Vin*L*Fsw)
ΔI=((19 - 1.0)*1.0)/(19*0.33u*450K)=6.38A

20150515 Nick add for power request

NTC PLACE NEAR H/S MOSFET

VBOOT=1.1V, and AND ICCMAX_CORE = 18A

20140515 Nick Change PC134=330P
POWER request

20140515 Nick Change PR191=120K (64.12035.6DL) POWER request

PR38 place near to choke PL1

PR37 place near to choke PL2

20140515 Nick Change PR190=402
POWER request

FSW=450K and AND ICCMAX_GT = 18A

20140515 Nick Change PR192=47K
POWER request

20140515 Nick Change PR196=330
POWER request

20140515 Nick Change PR211=3.09k
POWER request

20140515 Nick
Change PC143=4700P
POWER request

VIN RIPPLE CURRENT Imax=3.16A

0.33uH, DCR=3.5~3.9 mohm, Idc=20A

Iomax=13.5A

47uF/25V, ESR=30mohm
Ripple Current=2800mA

47uF/2.5V
ESR= 7mohm
Ripple Current =5000mA

1.0V
L=0.36uH
ΔI=((Vin-Vout)*Vout)/(Vin*L*Fsw)
ΔI=((19 - 1.0)*1.0)/(19*0.33u*450K)=6.38A

20150515 Nick add for power request

<Core Design>

wistron

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Hsichih, Taipei

Title: PWR_CPU CORE&VNN

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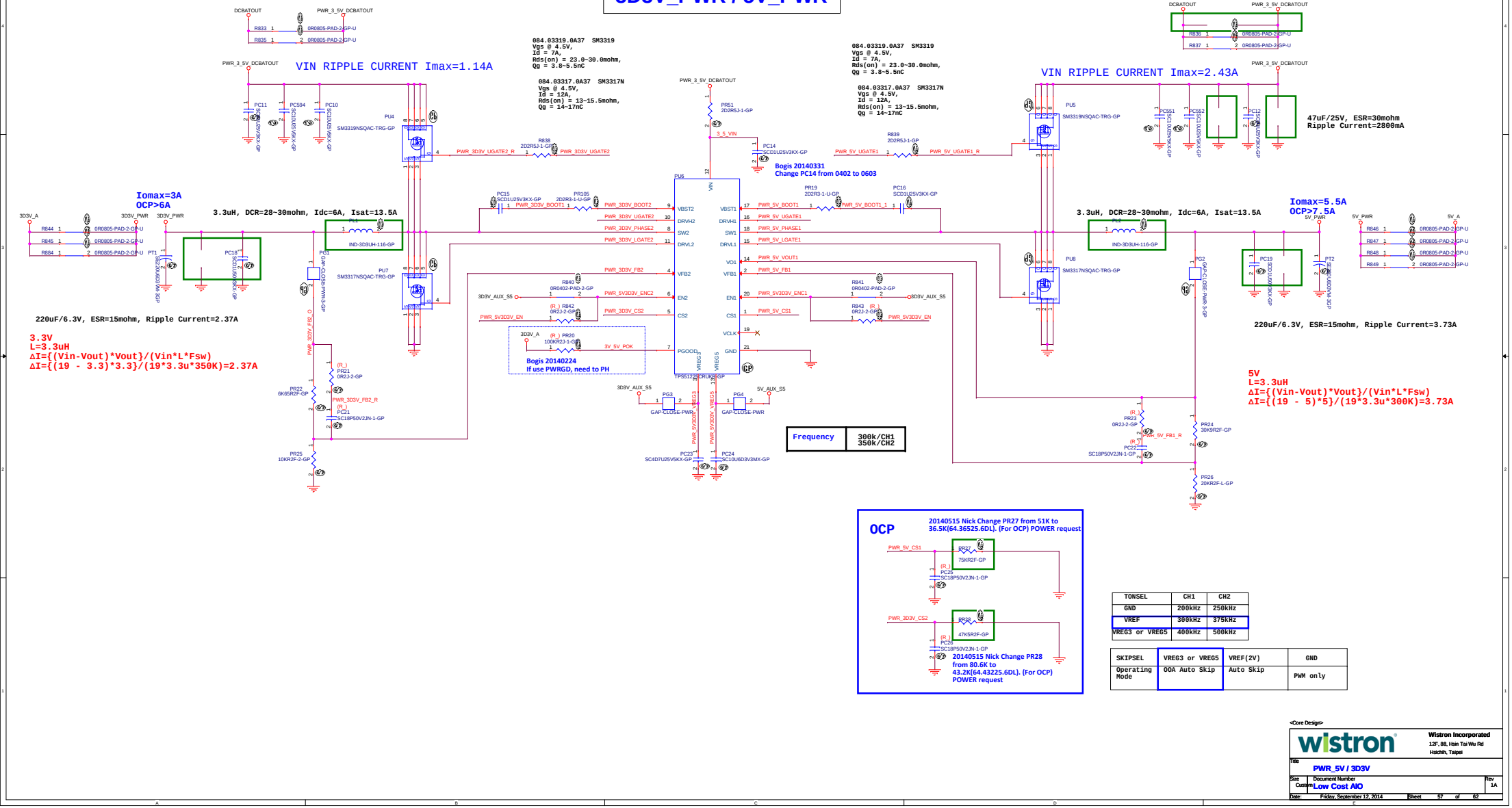
3D3V_PWR / 5V_PWR



TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3 or VREG5	400kHz	500kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

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Title: PWR_5V / 3D3V
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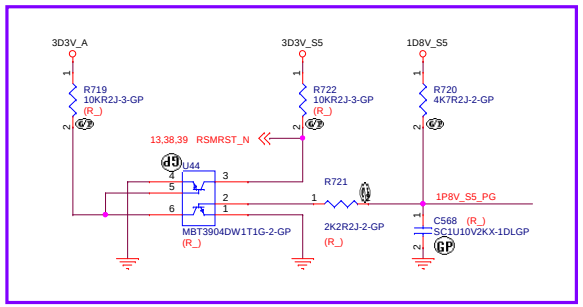
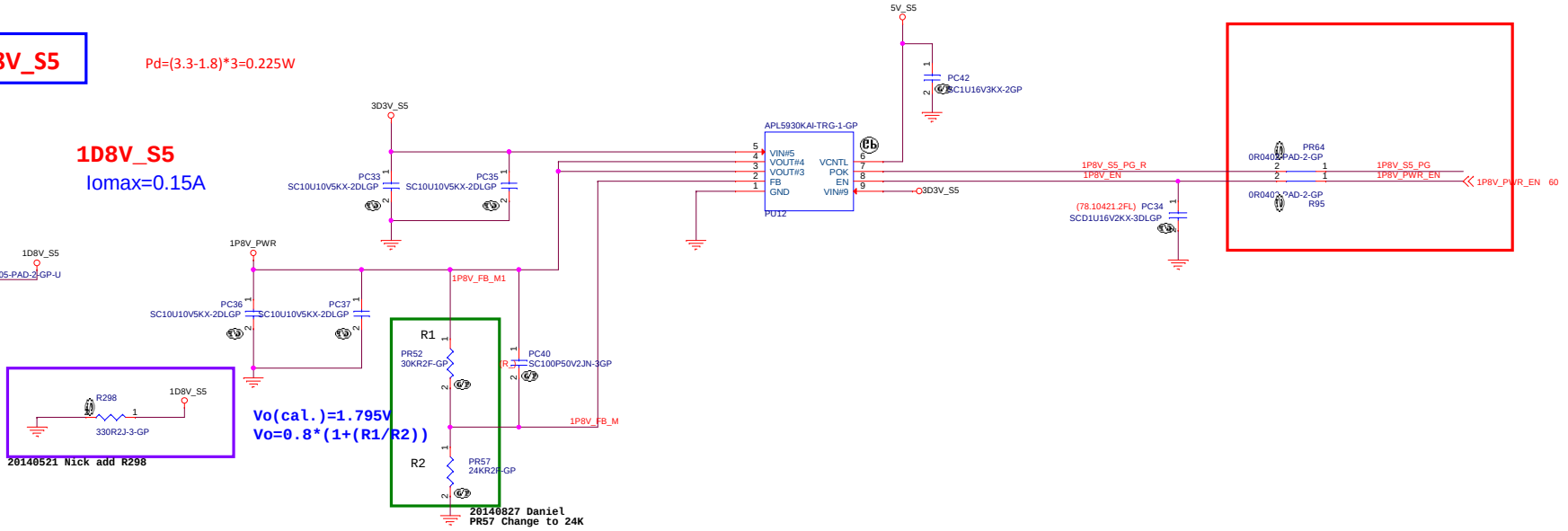


3D3V_S5 -> 1D8V_S5

Pd=(3.3-1.8)*3=0.225W

1D8V_S5

Iomax=0.15A



Vo(cal.)=1.795V
Vo=0.8*(1+(R1/R2))

20140521 Nick add R298

20140827 Daniel
PR57 Change to 24K

<Core Design>

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Hsichih, Taipei

Title: PWR_1D8V_RT8237

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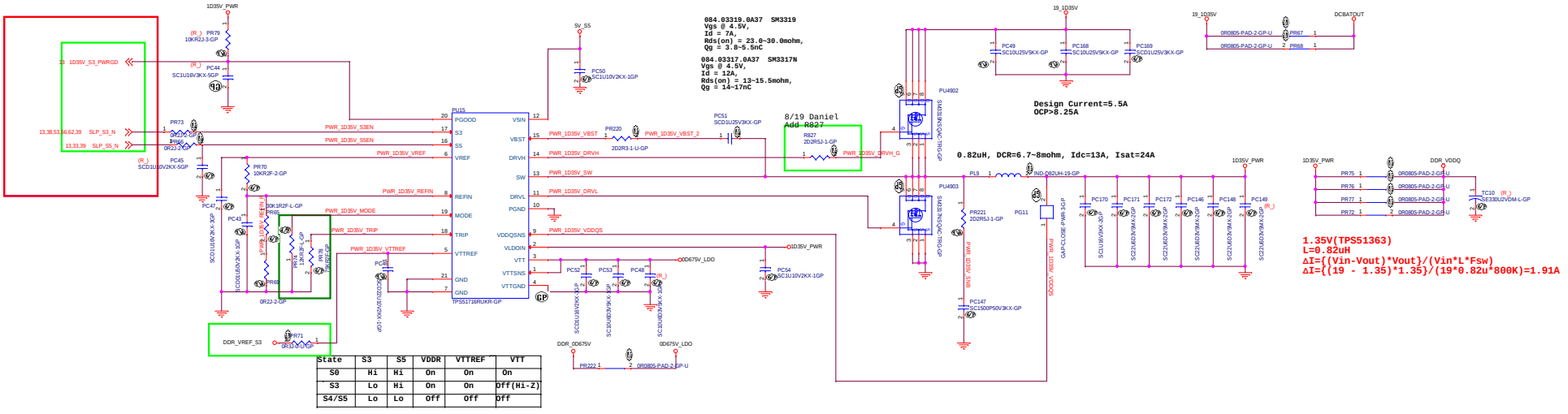
DDR_1.35V

V_SM_VTT

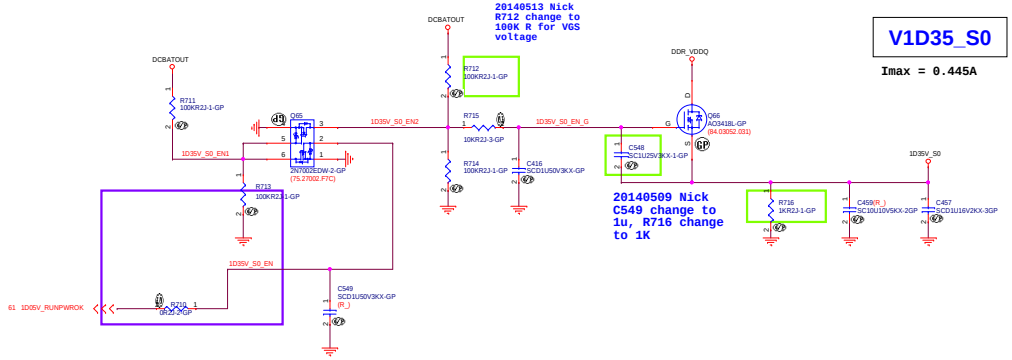
EE need check

VIN RIPPLE CURRENT Imax=1.42A



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

20140513 Nick
R712 change to
100K R for VGS
voltage



20140509 Nick
C549 change to
1u, R716 change
to 1K

V1D35_S0

Imax = 0.445A

20140515 Nick PR145 move to page 53

2014/4/28 Nick change from
1D05V_RUNPWROK to
+V_3P3_VGA

<Core Design>

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Title: PWR_1D35V_0D675_TPS51363

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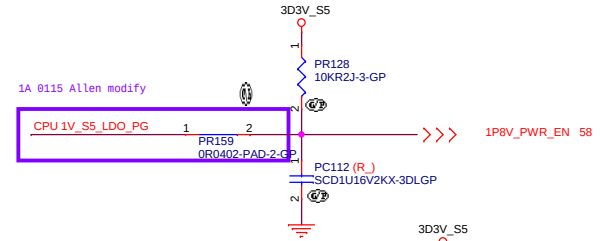
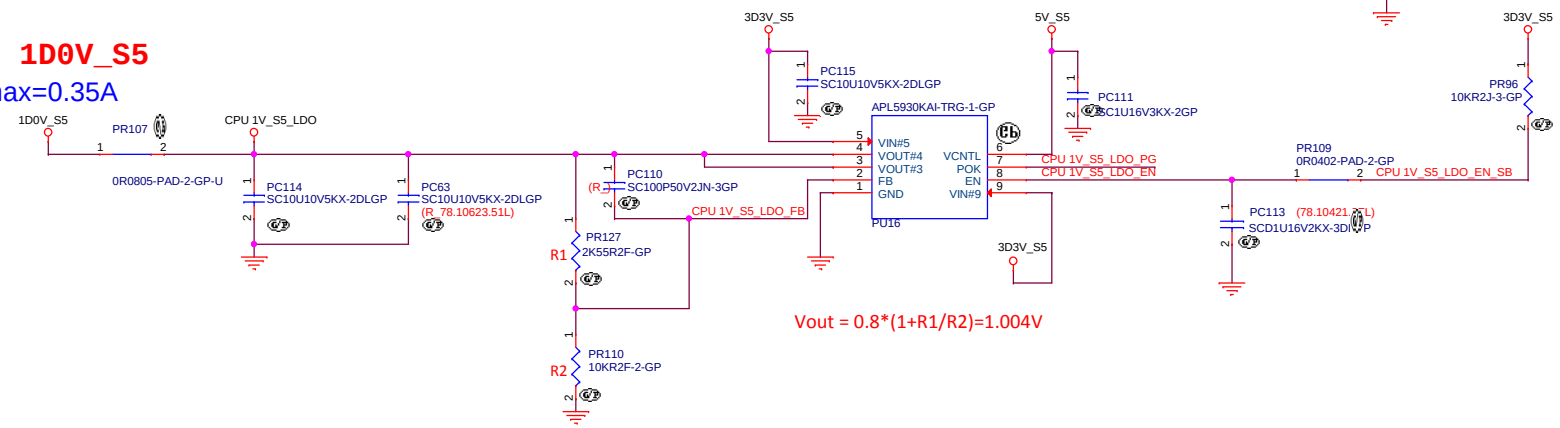
3D3V_S5 -> 1D0V_S5



CPU 1D0V_S5

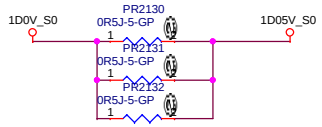
Iomax=0.35A

Pd=(3.3-1.0)*0.35=0.805W



Vout = 0.8*(1+R1/R2)=1.004V

Merger 1D05V_S0 -> 1D0V_S0



<Core Design>

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Title: PWR_CPU 1V_S0&CPU 1V_S5

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20140814 Daniel
1D5V_EN

20140814 Daniel
3D3V_S5 LDO to 1D5V_S0

20140519 Nick add for 1.5V_S0
power sequence follow Seattle

20140617 Bogis Add PR148

1D8V_S5 -> 1D8V_S0

20140513 Nick
R727 change to
100K R for VGS
voltage

Iomax=0.018A

20140509 Nick
C97 change to
1u, R717 change
to 1K

2014/4/29 Nick move C100 to page 61 and connect with 1.5V_S0_PWRGD

Merger 1D8V_S5 to 1D5V_S0

1.05V
EE need check

09/12 CM modify

EE need check

Float : 800KHz
GND: 400KHz

Iomax=4.5A
OCP=8A

0.82uH, DCR=6.7~8mohm, Idc=13A, Isat=24A

TRIP=GND, OCP=8A
TRIP= 5V, OCP=12A

VIN RIPPLE CURRENT Imax=1.1A

Bogis 20140312
Del PTC10、add PC168 to PC172

1.05V(TPS51363)
L=0.82uH
ΔI={(Vin-Vout)*Vout}/(Vin*L*Fsw)
ΔI={(19 - 1.05)*1.05}/(19*0.82u*800K)=1.52A

Connect GSNS to output capacitor
ground and VSNS to positive terminal
of output capacitor, run these two
trace as differential

<Core Design>

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Title: PWR_1P5_S0&1P05_S0&1P8V_S0

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<Variant Name>

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Title
PWR_12V

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