MS-7984

ATX

Ver: 1.1

Intel -Skylake plamform Z170

CPU:

Skylake-S

System Chipset:

Z170

Onboard Chip:

HD Audio Codec:ALC1150
LAN:Intel I219V
SIO:Nuvoton 6793D
Flash ROM: SPI 64MB /128MB(For H170/B150)

Main Memory:

*DDRIV (800/1066/1333/1600/2133MHz) * 4 (Dual Channel)*

ACPI:

NIKO/UPI

PWM:

IMVP8 -ISL95856

Expansion Slots:

*PCI Express (X16) Slot *1*
*PCI Express (X8) Slot * 1*
*PCI Express (X4) Slot * 1*
*PCI Express (X1) Slot * 3*
*PCI Slot * 1*
*M2 * 1*
SATAe 1*
SATA3.0 x6

Other:

*REAR USB2.0 *2*
*REAR USB3.0 *4*
*REAR USB3.1 *2*
*FRONT USB2.0 *4*
*FRONTUSB3.0 *2*

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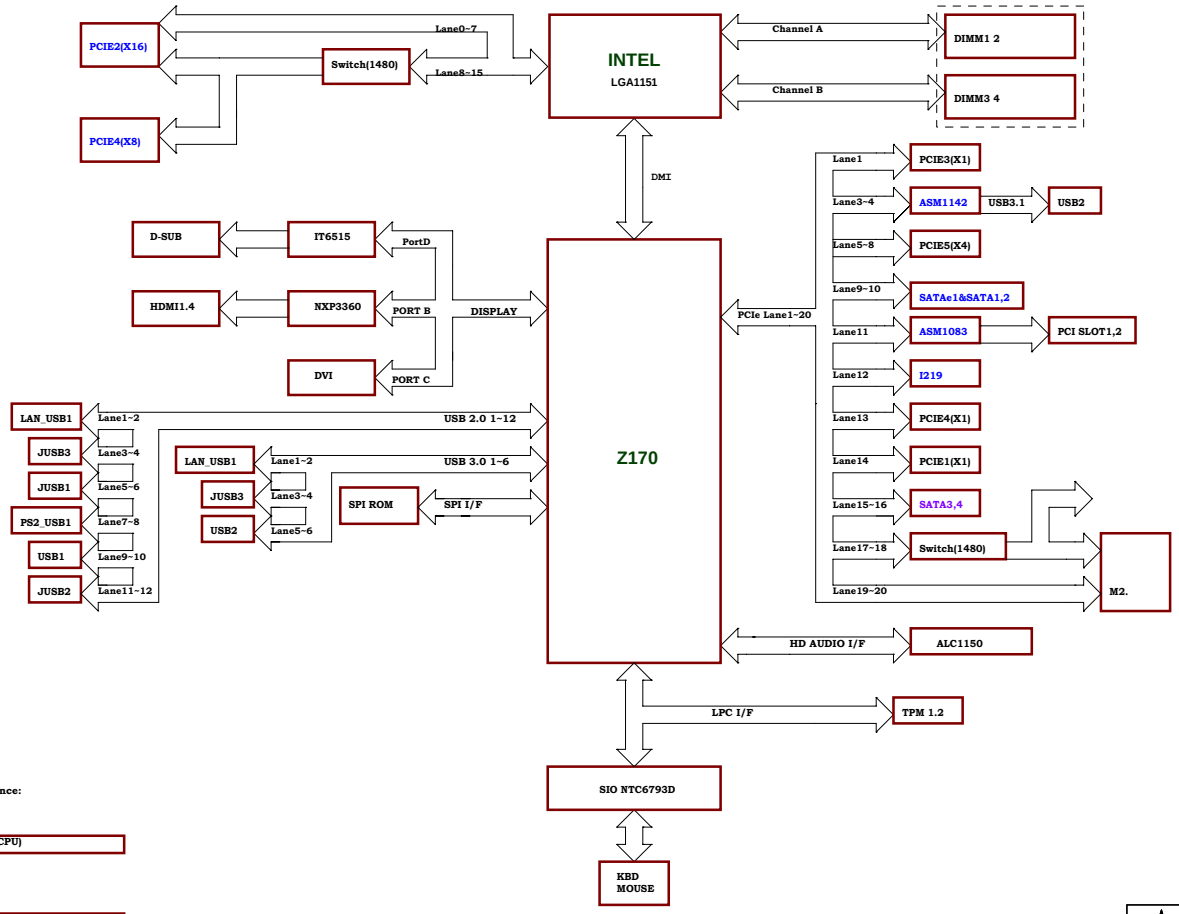
MS-7922 Block Diagram



Slot Sequence:

- PCIE X1
- PCIE X16(CPU)
- PCIE X1
- PCIE X1
- PCIE X8(CPU)
- PCI
- PCIE X4(PCH)

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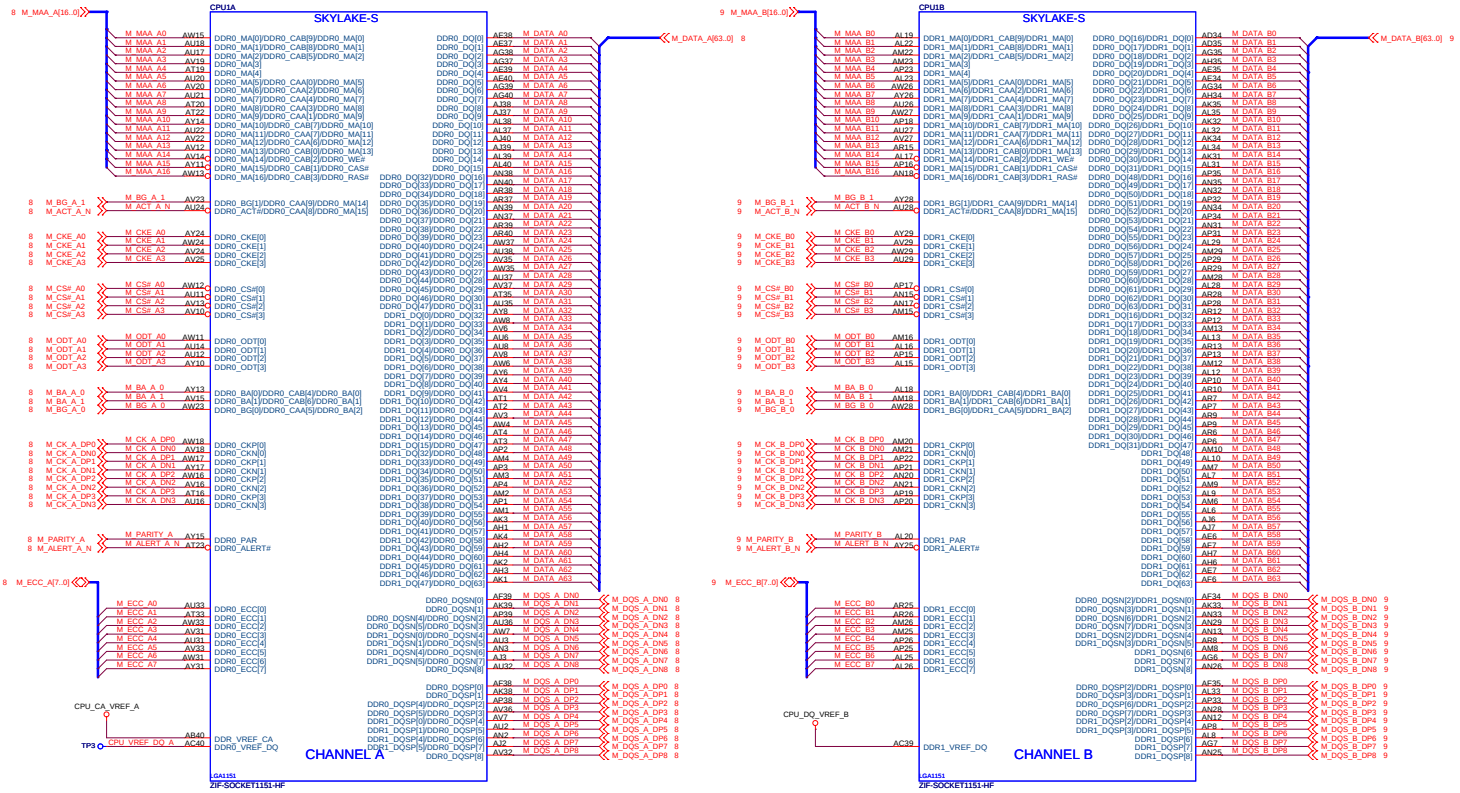
SOCKET PN N12-151A010-L06



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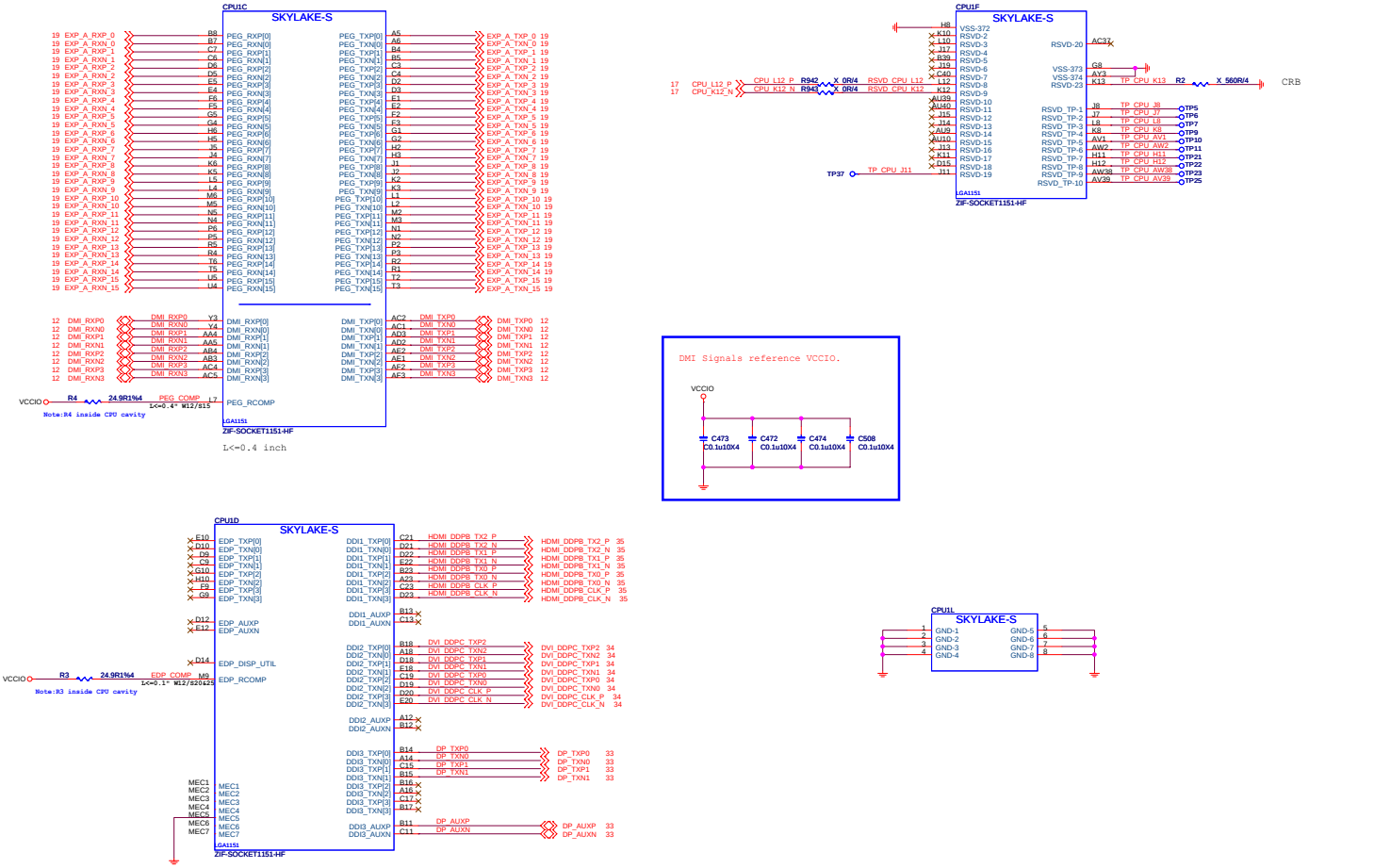

CPU Socket MEC5 Hole top layer add Soldermask,bot layer not add Soldermask.
1.MEC5 connect to GND.
2.Add CPU1L.
3.Footprint change to ZIF_SOCK1151_TEST_7978.

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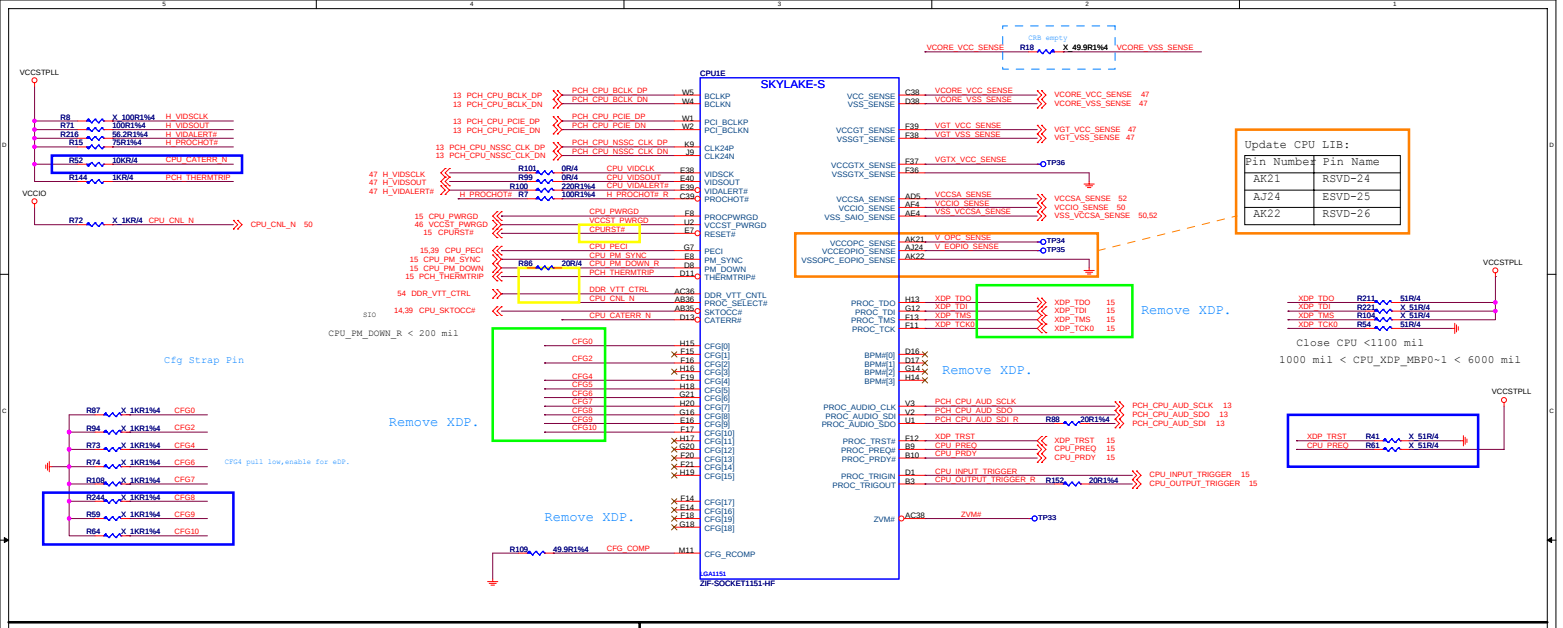

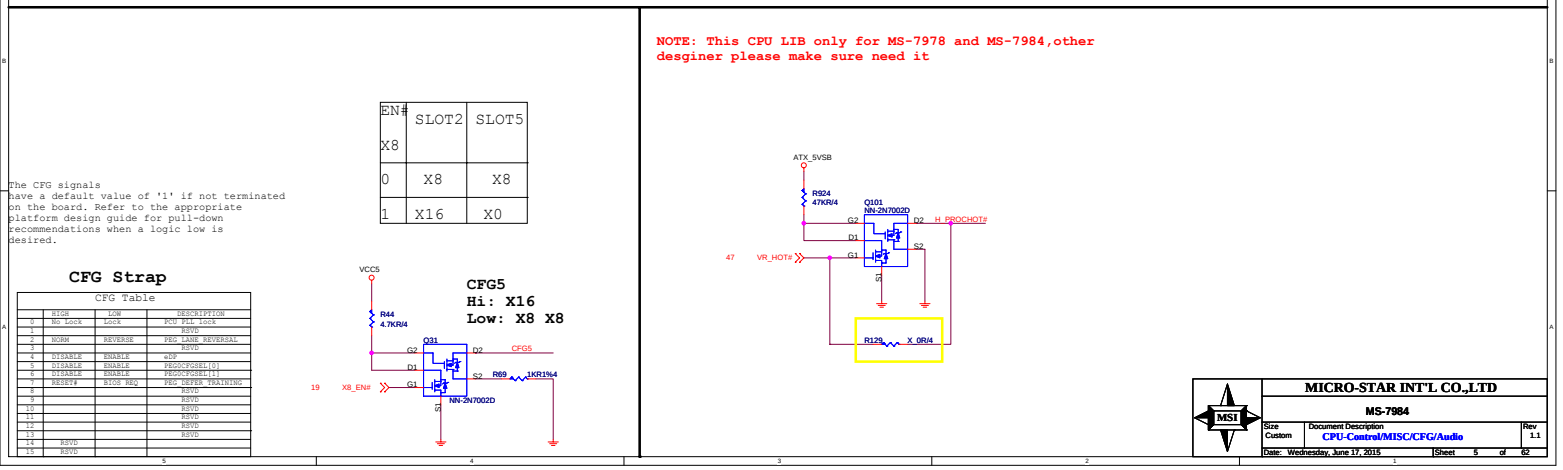

The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.

EN# X8	SLOT2	SLOT5
0	X8	X8
1	X16	X0

CFG Strap

CFG Table

	BIT	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL lock
1			RSVD
2	NORM	REVERSE	PEG LANE REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG2CFGSEL[0]
6	DISABLE	ENABLE	PEG3CFGSEL[1]
7	RESET#	BIOS REQ	PEG DEFER TRAINING
8			RSVD
9			RSVD
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14	RSVD		
15	RSVD		

NOTE: This CPU LIB only for MS-7978 and MS-7984,other desginer please make sure need it

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MS-7984	
Size: Custom	Document Description: CPU-Control/MISC/CFG/Audio
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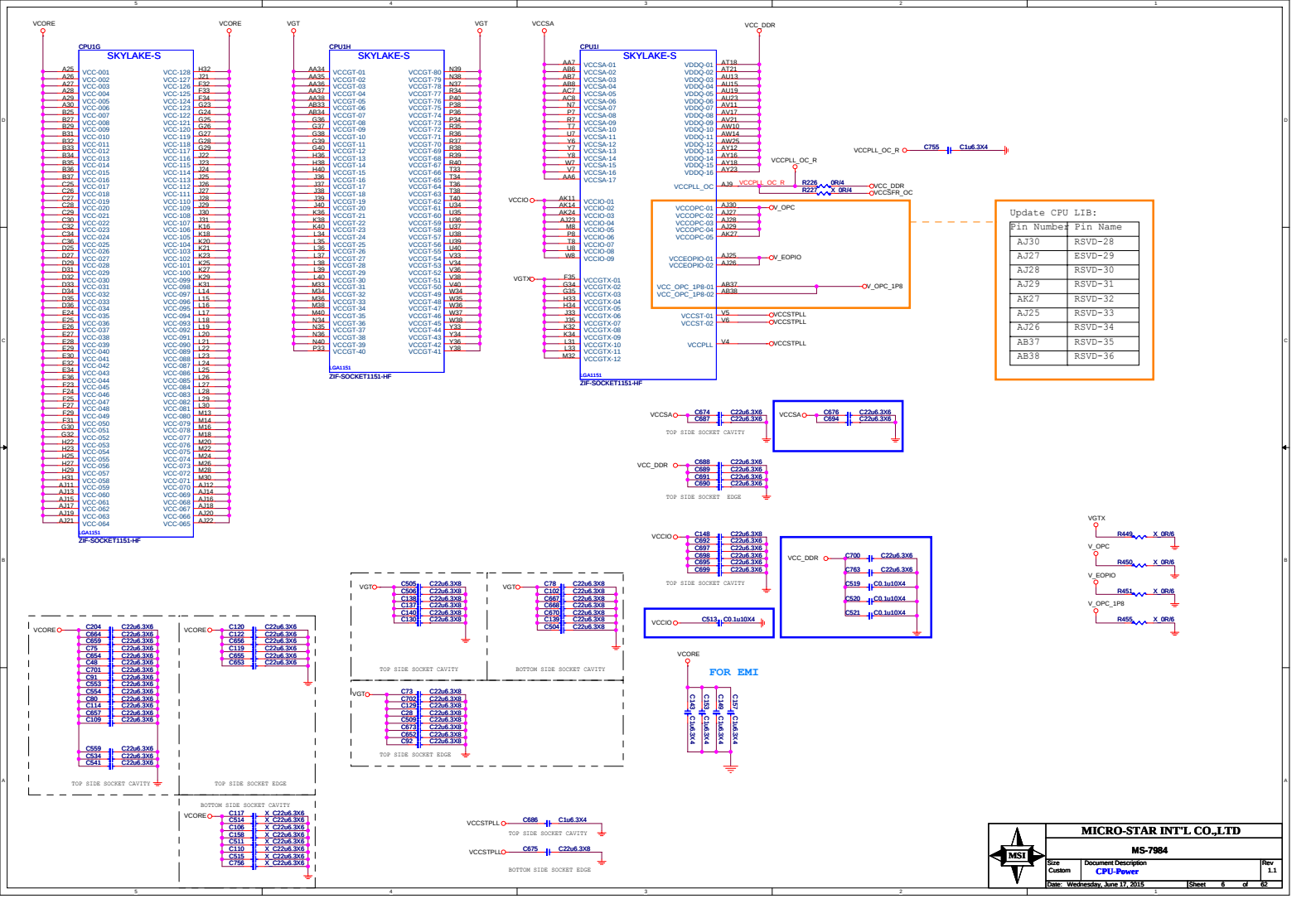

MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: CPU-Power	Rev: 1.1
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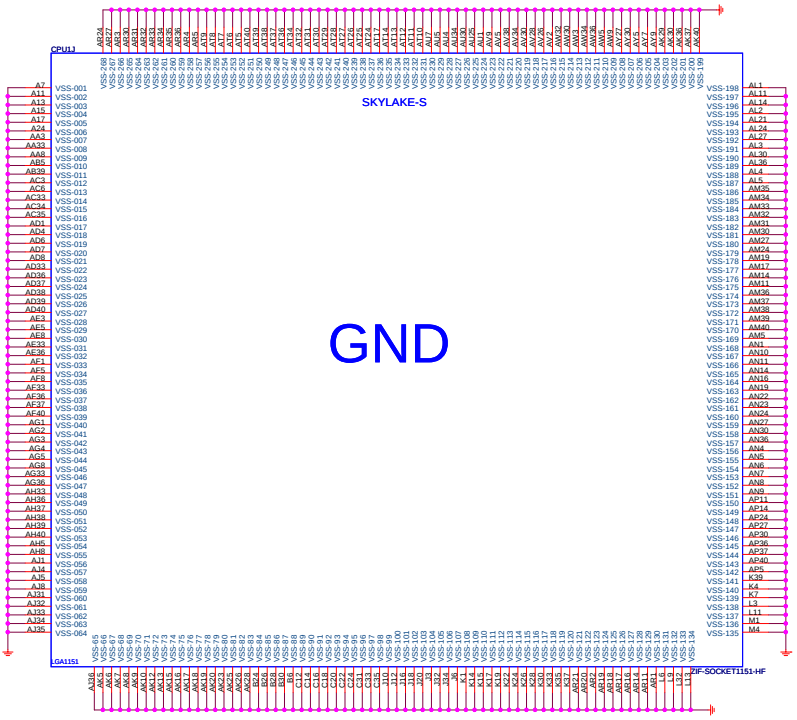

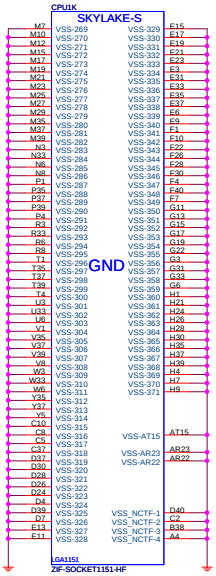

MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: CPU-GND	Rev: 1.1
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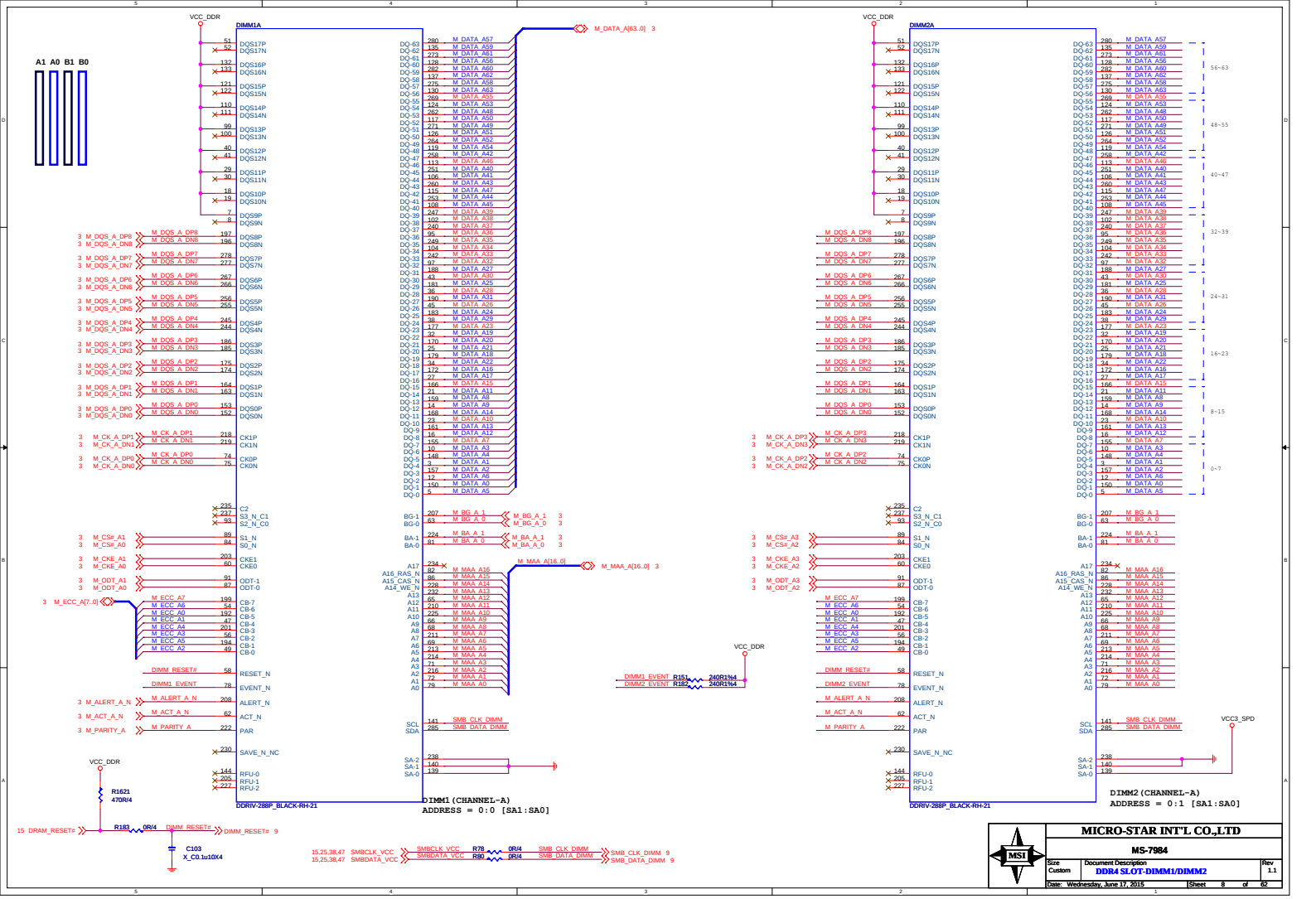

MICRO-STAR INT'L CO.,LTD		
MS-7984		
Size: Custom	Document Description: DDR4 SLOT-DIMM1/DIMM2	Rev: 1.1
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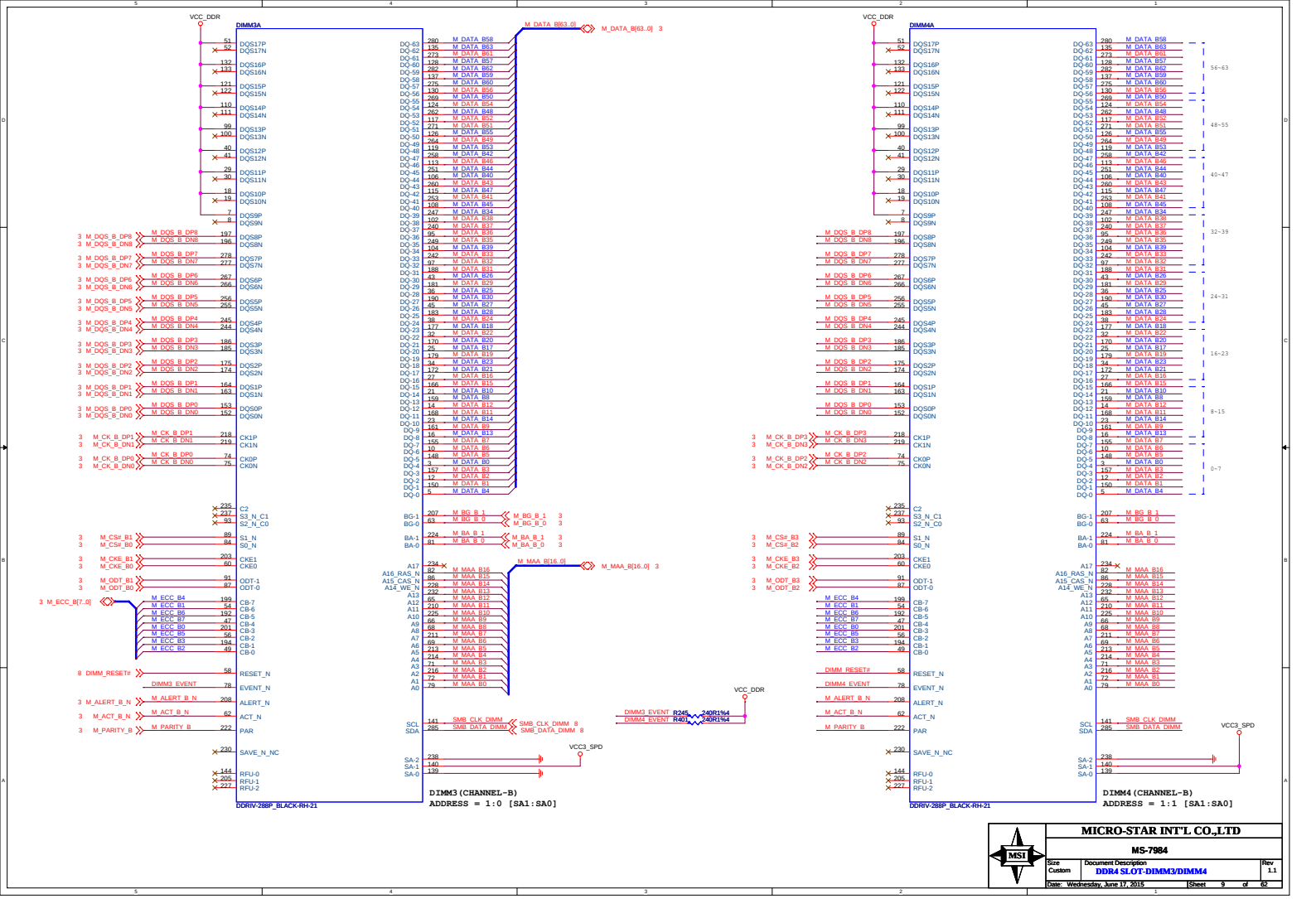

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7984	
Size: Custom	Document Description: DDR4 SLOT-DIMM3/DIMM4	Rev: 1.1
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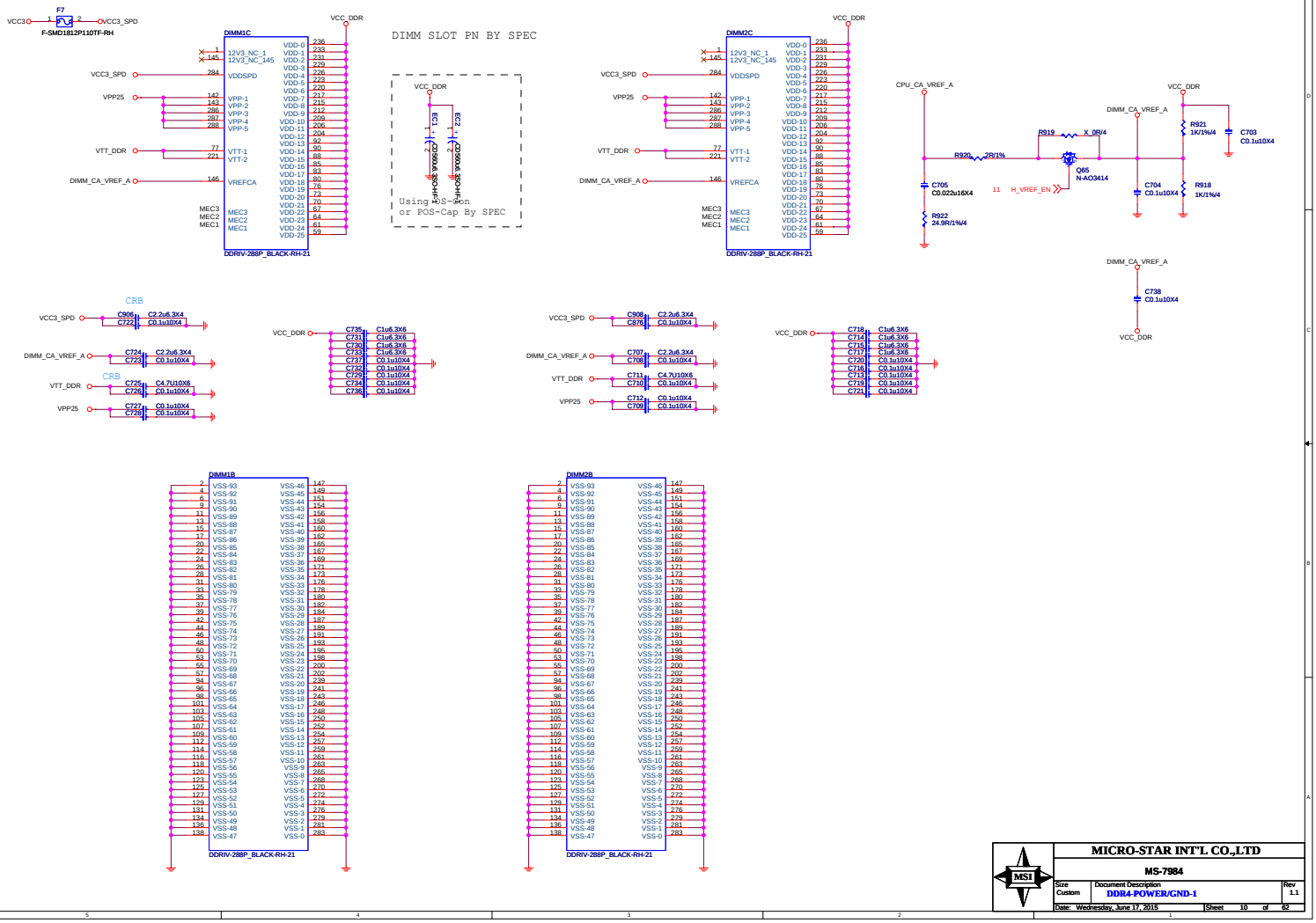

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MS-7984		
Size: Custom	Document Description: DDR4-POWER/GND-1	Rev: 1.1
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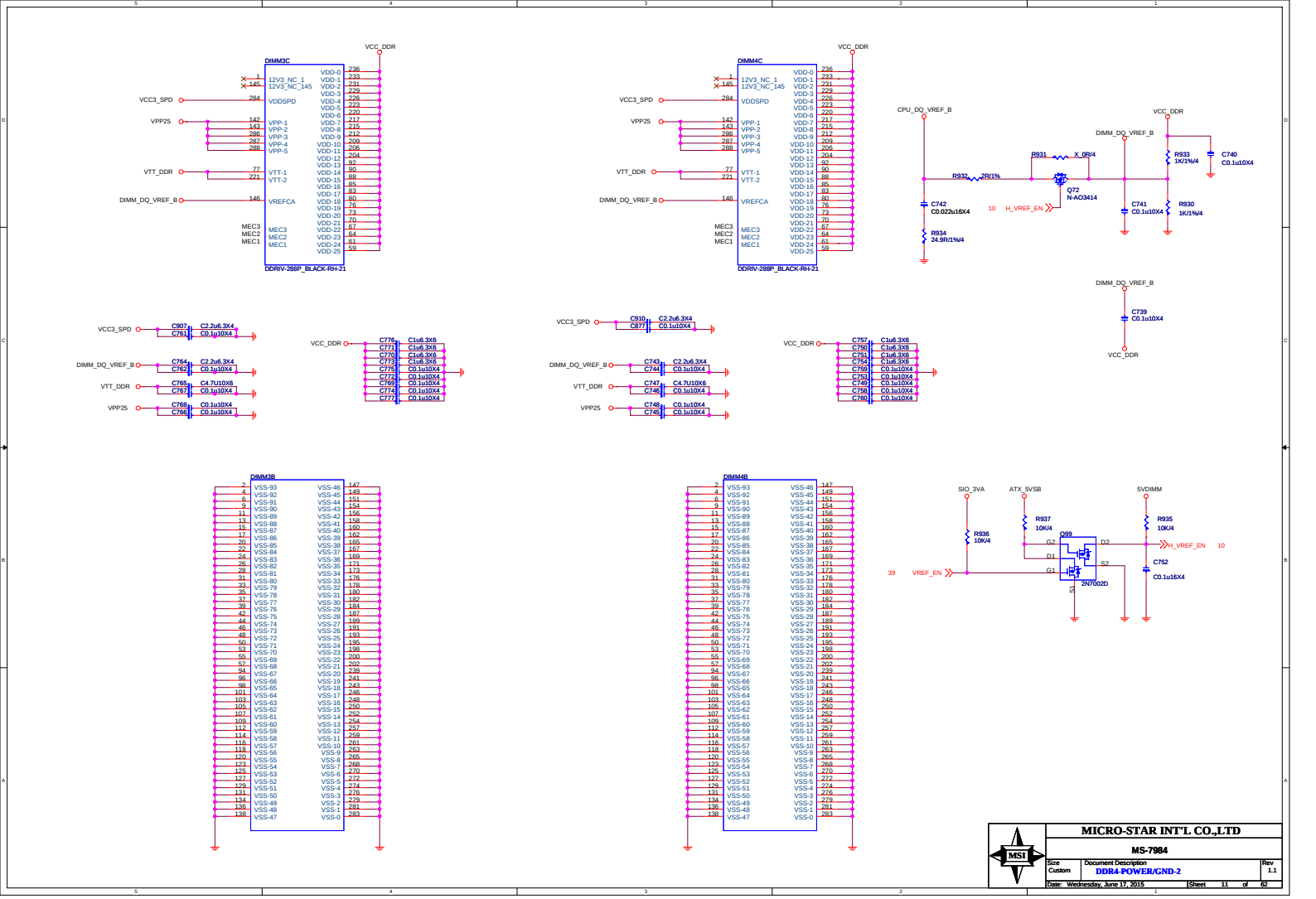

DDRIV-288P_BLACK-RH-21

DDRIV-288P_BLACK-RH-21

MSI	MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: DDR4-POWER/GND-2	Rev: 1.1
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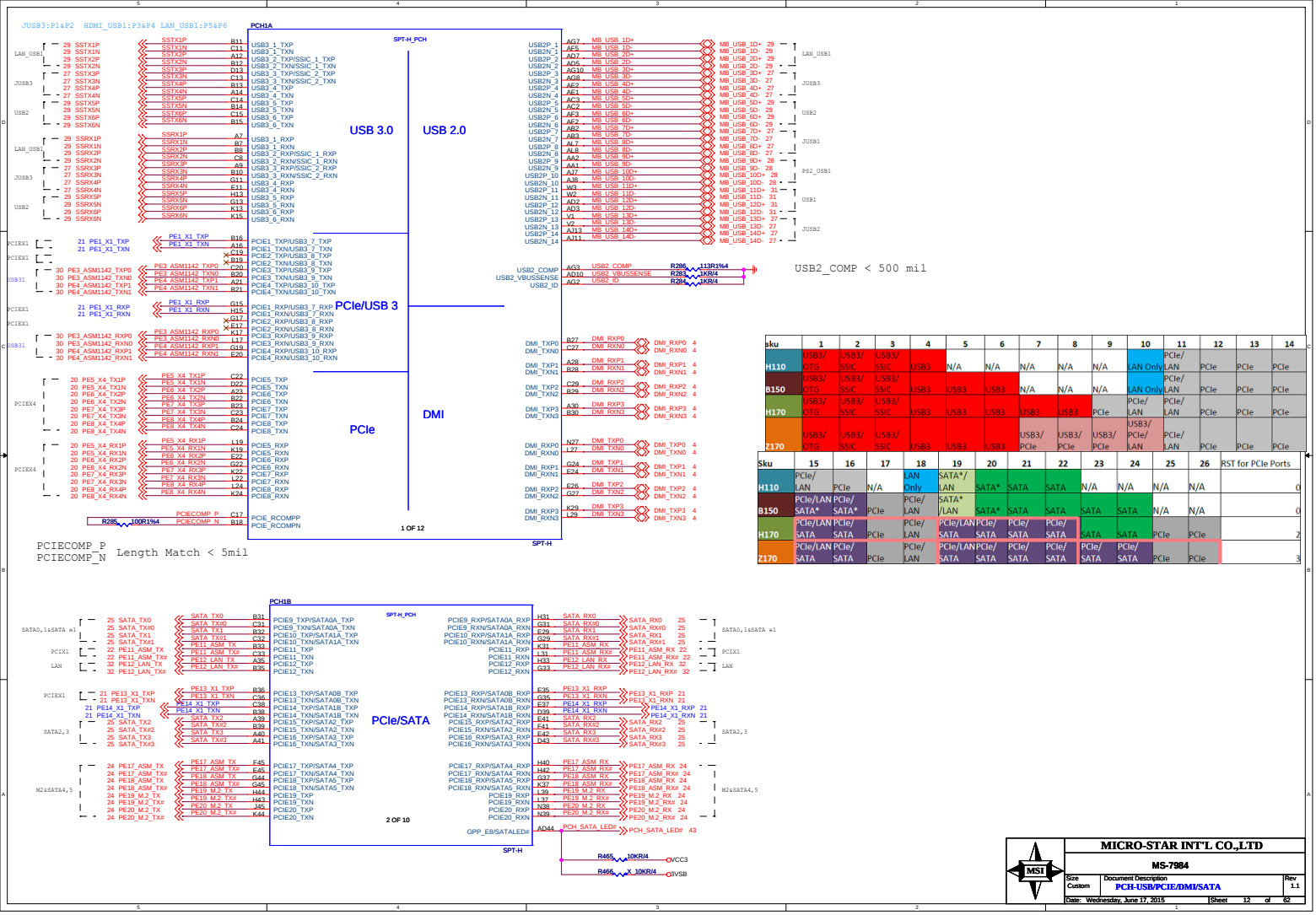

sku	1	2	3	4	5	6	7	8	9	10	11	12	13	14
H110	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	N/A	N/A	N/A	N/A	N/A	LAN Only	PCIe/ LAN	PCIe	PCIe	PCIe
B150	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	N/A	N/A	N/A	LAN Only	PCIe/ LAN	PCIe	PCIe	PCIe
H170	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	USB3	USB3	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe	PCIe
Z170	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	USB3/ PCIe	USB3/ PCIe	USB3/ PCIe	USB3/ PCIe/ LAN	PCIe/ LAN	PCIe	PCIe	PCIe

Sku	15	16	17	18	19	20	21	22	23	24	25	26	RST for PCIe Ports
H110	PCIe/ LAN	PCIe	N/A	LAN Only	SATA*/ LAN	SATA*	SATA	SATA	N/A	N/A	N/A	N/A	0
B150	PCIe/LAN SATA*	PCIe/ SATA*	PCIe	PCIe/ LAN	SATA* /LAN	SATA*	SATA	SATA	SATA	SATA	N/A	N/A	0
H170	PCIe/LAN SATA	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	SATA	SATA	PCIe	PCIe	2
Z170	PCIe/LAN SATA	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe	PCIe	3

Project	MICRO-STAR INT'L CO.,LTD
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Document Description	PCH-USB/PCIE/DMI/SATA
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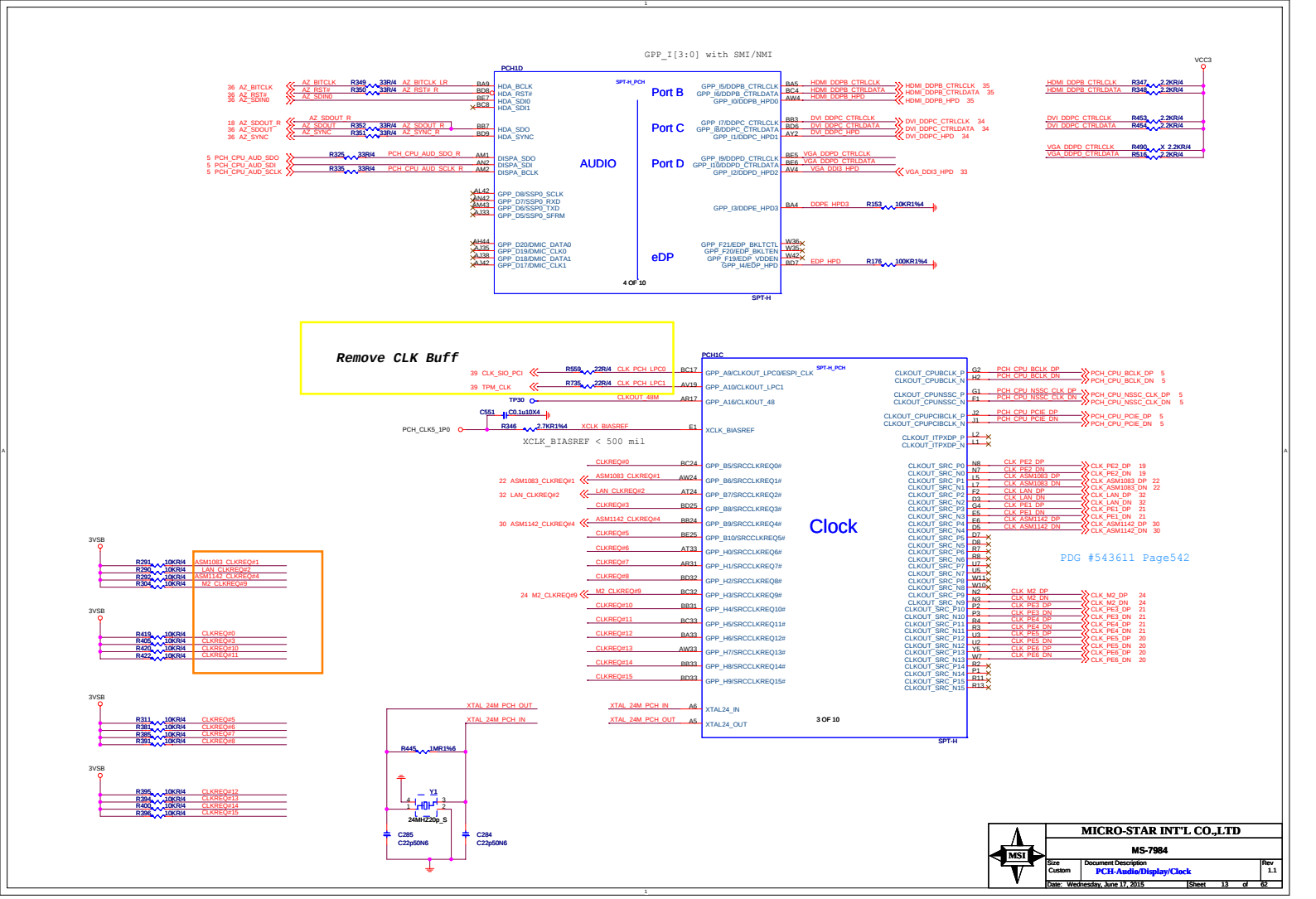
GPP_I[3:0] with SMI/NMI
PCH1D
SPT-H_PCH
AUDIO
Port B
Port C
Port D
eDP
4 OF 10
SPT-H
Remove CLK Buff
PCH1C
Clock
3 OF 10
XCLK_BIASREF < 500 mil
PDG #543611 Page542
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PCH-Audio/Display/Clock
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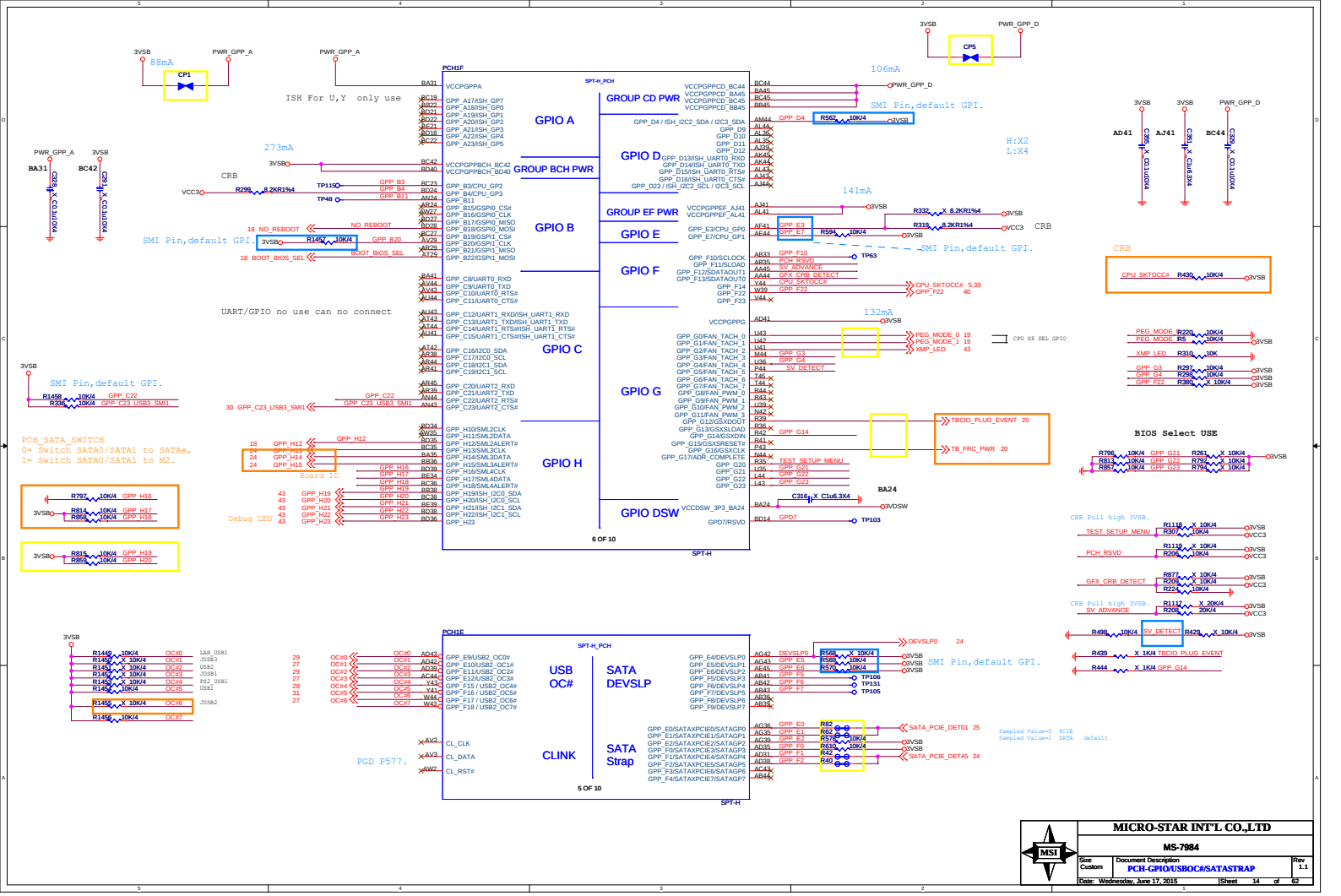
PCH1F
SPT-H_PCH
GROUP CD PWR
GROUP BCH PWR
GROUP EF PWR
GPIO A
GPIO D
GPIO B
GPIO E
GPIO F
GPIO C
GPIO G
GPIO H
GPIO DSW
6 OF 10
SPT-H
ISH For U,Y only use
UART/GPIO no use can no connect
SMI Pin,default GPI.
CRB
PCH_SATA_SWITCH
0= Switch SATA0/SATA1 to SATAe,
1= Switch SATA0/SATA1 to M2.
Board ID
Debug LED
BIOS Select USE
TBCIO_PLUG_EVENT
TB_FRC_PWR
PCH1E
USB OC#
SATA DEVSLP
CLINK
SATA Strap
5 OF 10
PGD P577.
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PCH-GPIO/USBOC#/SATASTRAP
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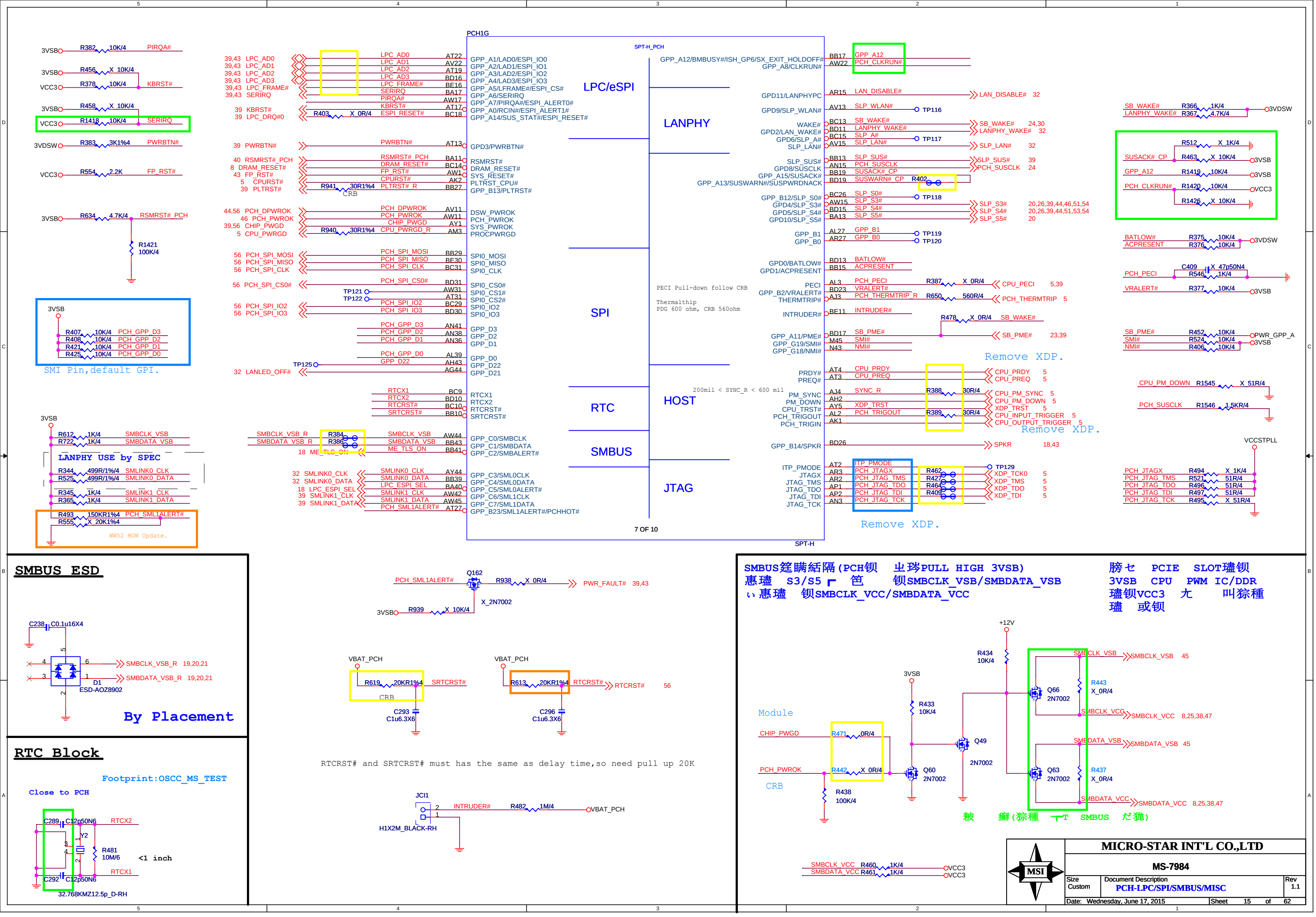

PCH1G
SPT-H_PCH
LPC/eSPI
LANPHY
SPI
RTC
HOST
SMBUS
JTAG
7 OF 10
SPT-H
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_FRAME#
SERIRQ
PIRQA#
KBRST#
ESPI_RESET#
PWRBTN#
RSMRST#_PCH
DRAM_RESET#
FP_RST#
CPURST#
PLTRST#_R
PCH_DPWROK
PCH_PWROK
CHIP_PWGD
CPU_PWRGD_R
PCH_SPI_MOSI
PCH_SPI_MISO
PCH_SPI_CLK
PCH_SPI_CS0#
PCH_SPI_IO2
PCH_SPI_IO3
PCH_GPP_D3
PCH_GPP_D2
PCH_GPP_D1
PCH_GPP_D0
GPP_D22
RTCX1
RTCX2
RTCRST#
SRTCRST#
SMBCLK_VSB
SMBDATA_VSB
ME_TLS_ON
SMLINK0_CLK
SMLINK0_DATA
LPC_ESPI_SEL
SMLINK1_CLK
SMLINK1_DATA
PCH_SML1ALERT#
GPP_A12
PCH_CLKRUN#
LAN_DISABLE#
SLP_WLAN#
SB_WAKE#
LANPHY_WAKE#
SLP_A#
SLP_LAN#
SLP_SUS#
PCH_SUSCLK
SUSACK#_CP
SUSWARN#_CP
SLP_S0#
SLP_S3#
SLP_S4#
SLP_S5#
GPP_B1
GPP_B0
BATLOW#
ACPRESENT
PCH_PECI
VRALERT#
PCH_THERMTRIP_R
INTRUDER#
SB_PME#
SMI#
NMI#
CPU_PRDY
CPU_PREQ
SYNC_R
XDP_TRST
PCH_TRIGOUT
CPU_PM_SYNC
CPU_PM_DOWN
CPU_INPUT_TRIGGER
CPU_OUTPUT_TRIGGER
SPKR
ITP_PMODE
PCH_JTAGX
PCH_JTAG_TMS
PCH_JTAG_TDO
PCH_JTAG_TDI
PCH_JTAG_TCK
XDP_TCK0
XDP_TMS
XDP_TDO
XDP_TDI
PECI Pull-down follow CRB
Thermalthip
PDG 600 ohm, CRB 560ohm
200mil < SYNC_R < 600 mil
Remove XDP.
SMI Pin,default GPI.
LANPHY USE by SPEC
MW52 MOW Update.
CRB
SMBUS ESD
ESD-AOZ8902
By Placement
RTC Block
Footprint:OSCC_MS_TEST
Close to PCH
32.768KMZ12.5p_D-RH
<1 inch
PCH_SML1ALERT#
PWR_FAULT#
X_2N7002
VBAT_PCH
RTCRST# and SRTCRST# must has the same as delay time,so need pull up 20K
JCI1
H1X2M_BLACK-RH
INTRUDER#
Module
CHIP_PWGD
PCH_PWROK
SMBCLK_VSB
SMBCLK_VCC
SMBDATA_VSB
SMBDATA_VCC
2N7002
+12V
3VSB
VCC3
3VDSW
VCCSTPLL
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Size Custom
Document Description
PCH-LPC/SPI/SMBUS/MISC
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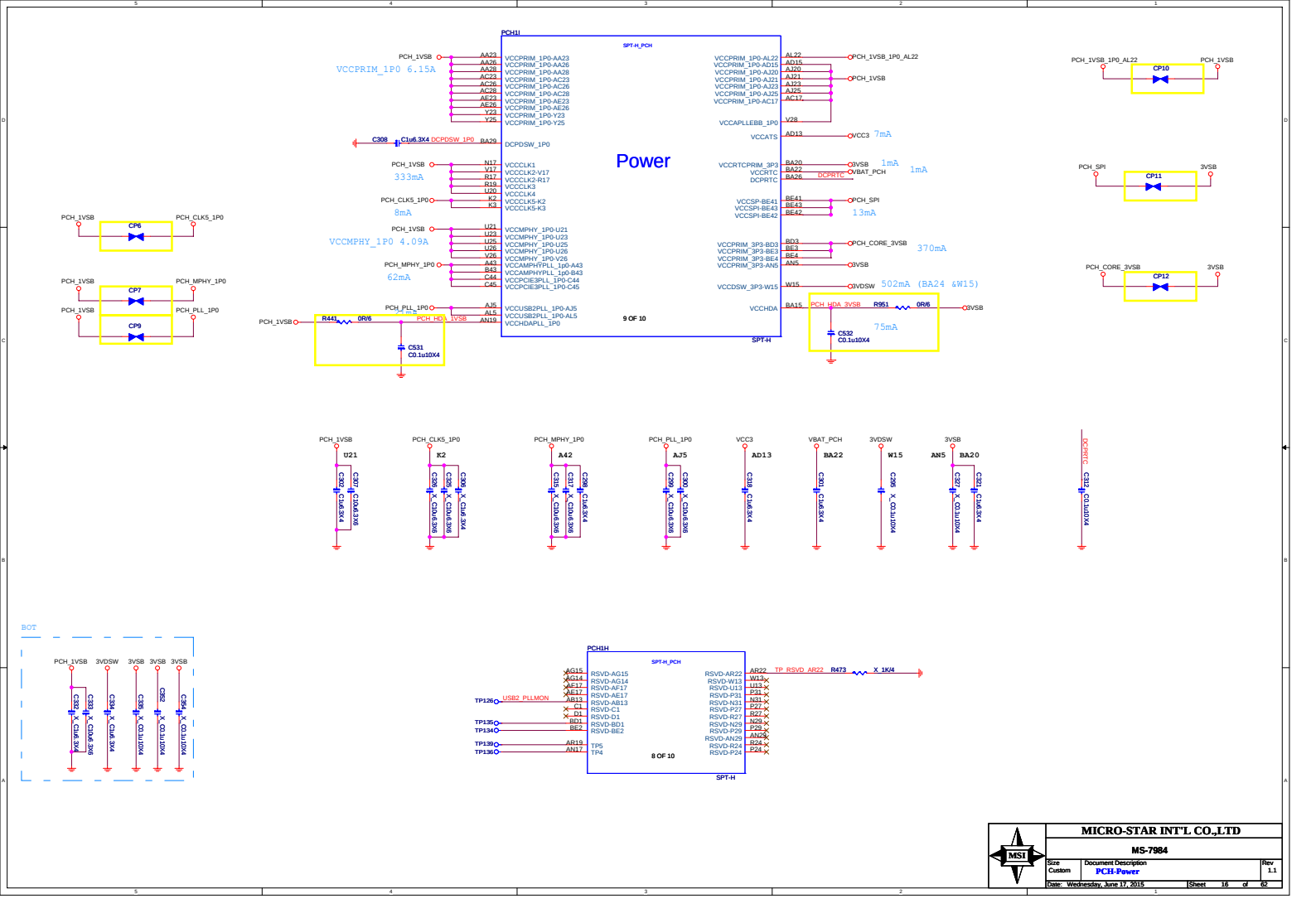

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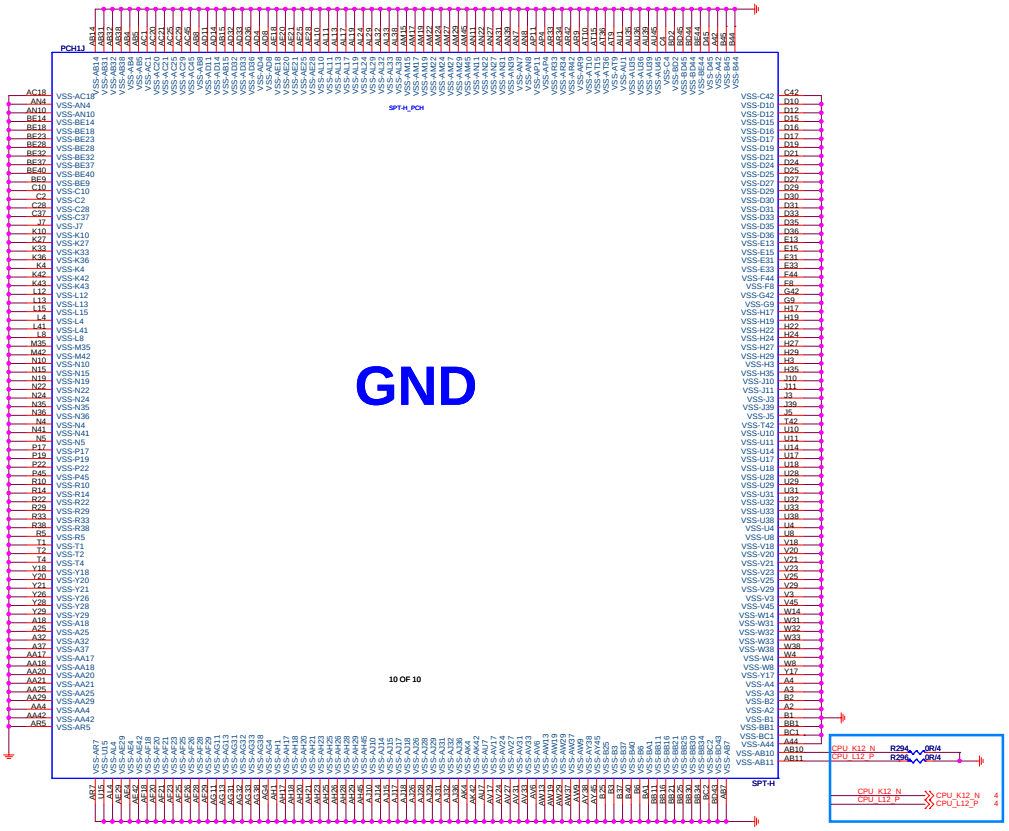

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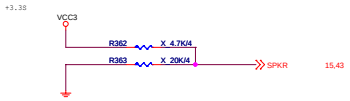
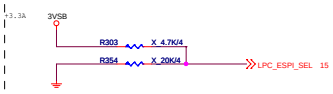
TOP Swap



Internal pull-down is disabled after PLTRST#

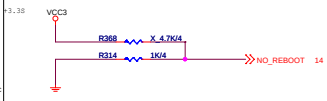
LPC eSPI Mode



0 : LPC
1 : eSPI

Internal pull-down is disabled after RSMRST

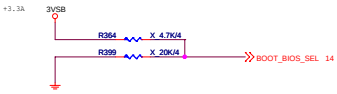
No Reboot



0 : DISABLE (Default)
1 : ENABLE

Internal pull-down is disabled after PLTRST#

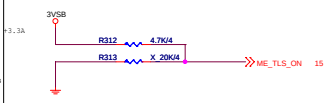
Boot BIOS



0 : SPI
1 : LPC

Internal pull-down is disabled after PLTRST

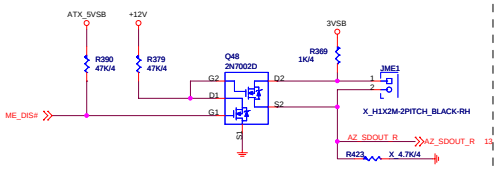
AMT and SBA with confidentiality



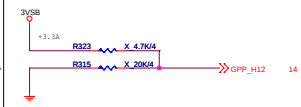
0 : DISABLE
1 : ENABLE (Default)

Internal pull-down is disabled after RSMRST

HDA_SDO



ESPI FLASH SHARING MODE



0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

Internal pull-down is disabled after RSMRST

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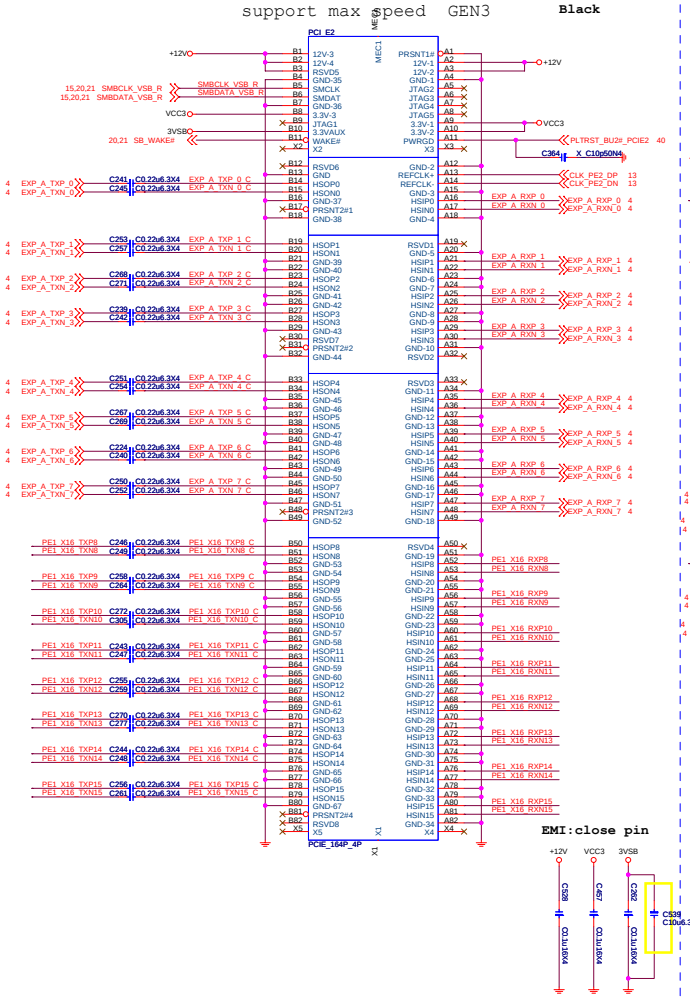
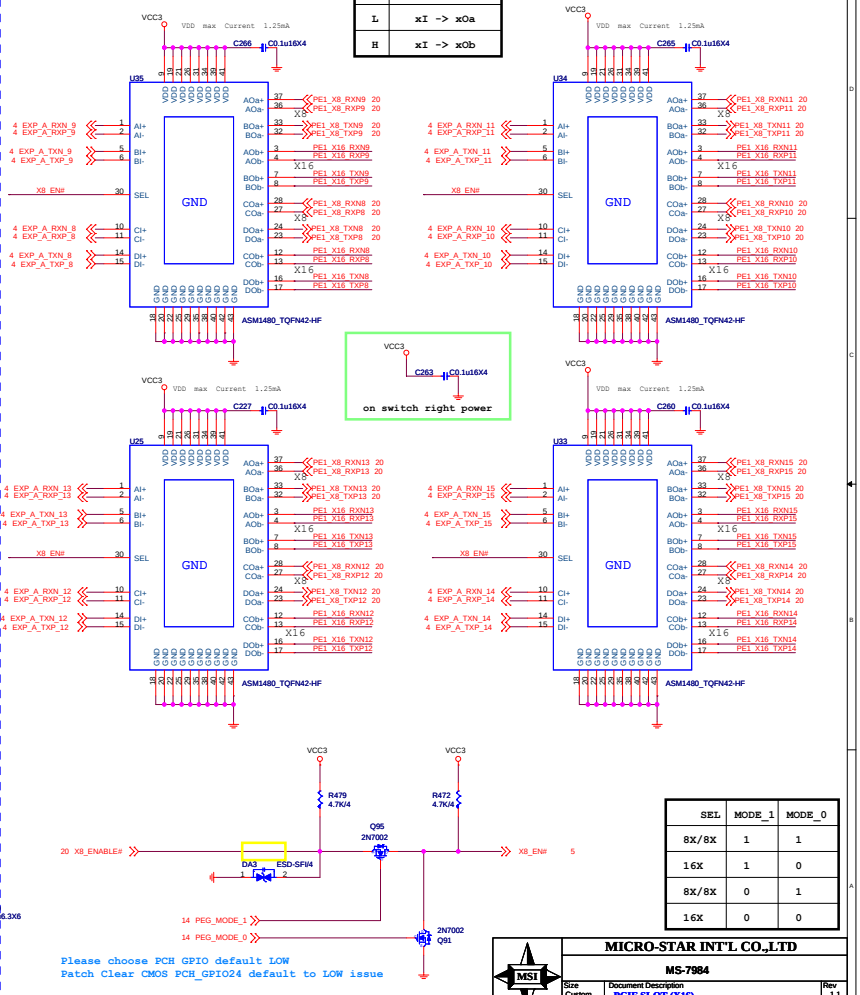
PCI Express X16 Slot

support max speed GEN3

Black



SEL	Function
L	xI -> xOa
H	xI -> xOb



Please choose PCH GPIO default LOW

Patch Clear CMOS PCH_GPIO24 default to LOW issue

SEL	MODE_1	MODE_0
8X/8X	1	1
16X	1	0
8X/8X	0	1
16X	0	0

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Custom	PCIE SLOT (X16)	1.1

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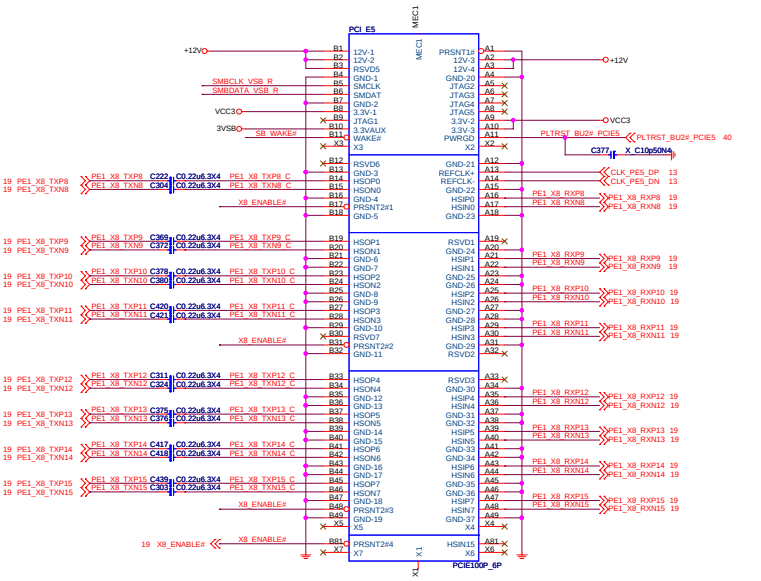
15,19,21 SMBCLK_VSB_R
15,19,21 SMBDATA_VSB_R
19,21 SB_WAKE#

SMBCLK_VSB_R
SMBDATA_VSB_R
SB_WAKE#

PCI_Express X8 Slot

support max speed GEN3 **Black**

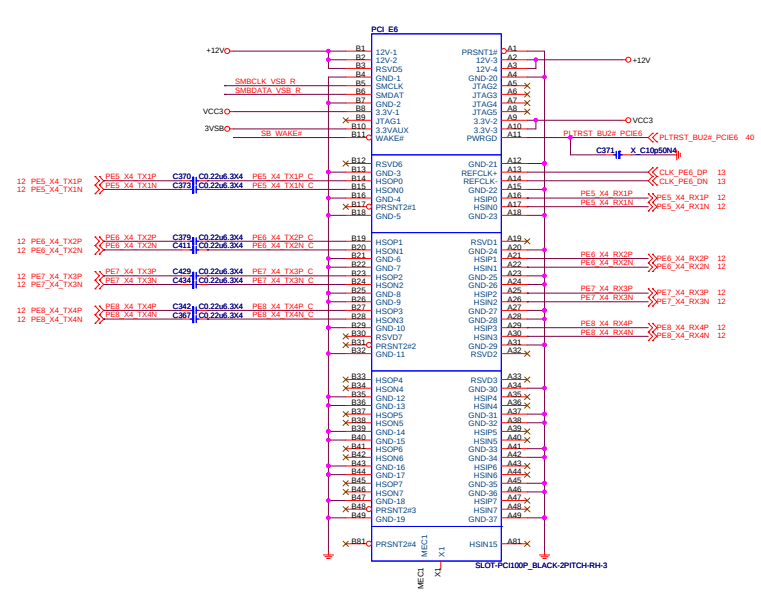
PCI E5



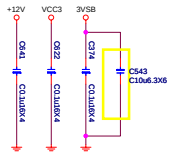
PCI_Express X4 Slot

support max speed GEN3 **Black**

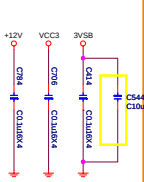
PCI E6



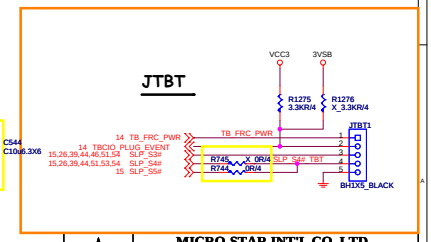
EMI:close pin



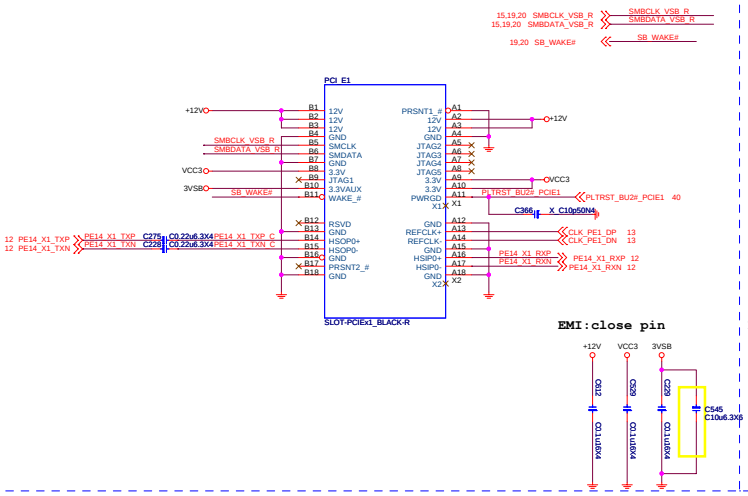
EMI:close pin



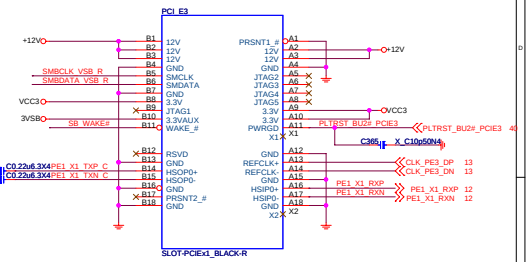
JTBT



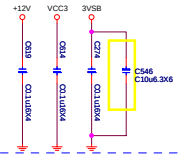
MICRO-STAR INT'L CO.,LTD		
MS-7984		
Size: Custom	Document Description: PCIE SLOT (X4)	Rev: 1.1
Date: Wednesday, June 17, 2015	Sheet 20 of 62	



EMI:close pin

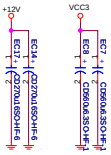


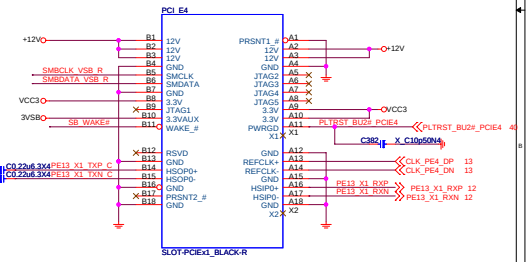
EMI:close pin



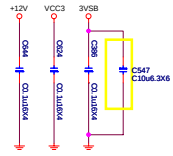
PCIE(X1) *3 PCIE(X4)*1 PCIE(X8)*1 PCIE(X16)*1

3.3Vaux:0.375*5=2.25A(wake)
0.02*5=0.12A(no wake)
VCC3:3*6=18A
+12V:0.5*3+2.1+2.1+5.5=11.2A

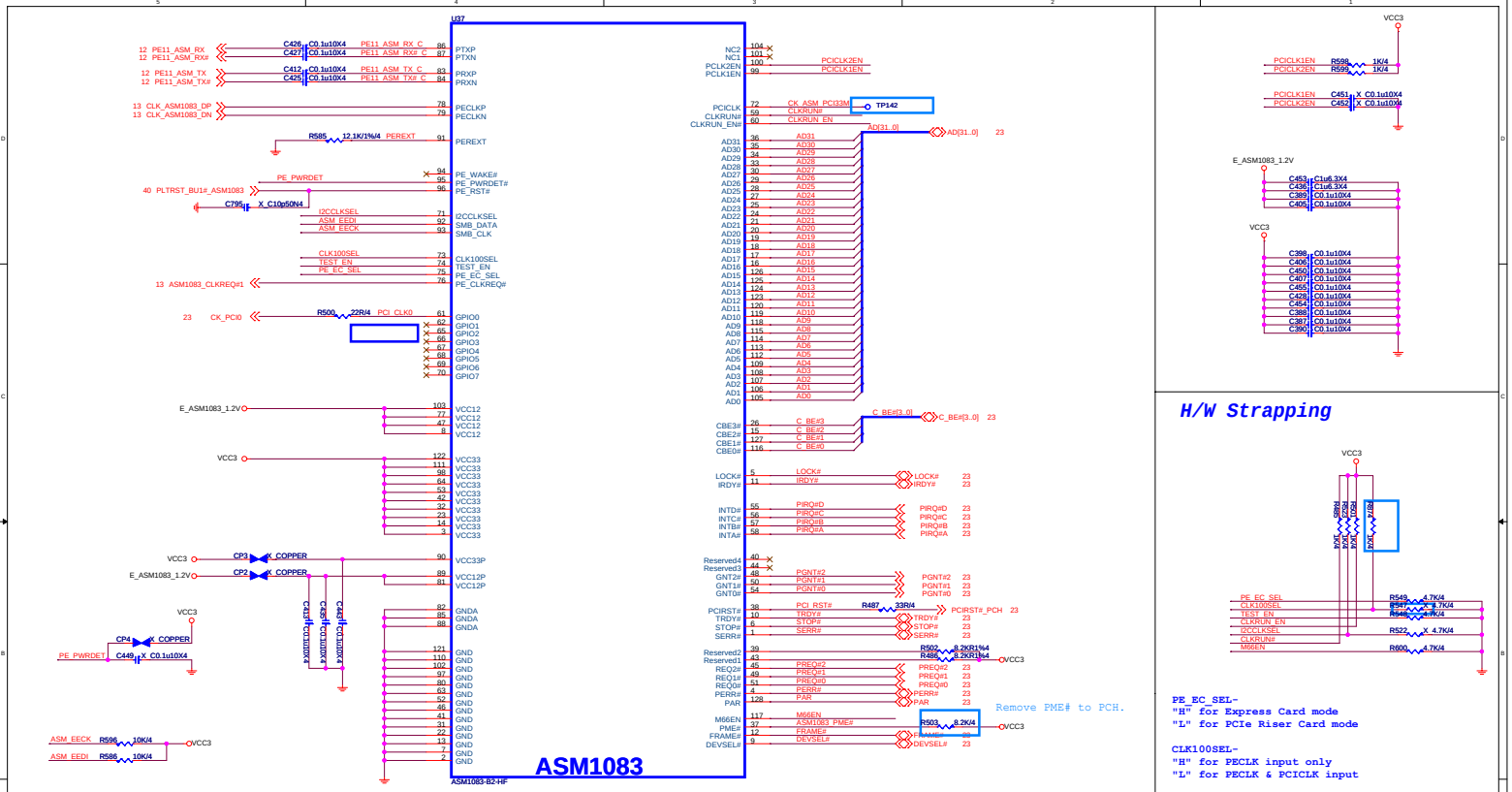




EMI:close pin



MICRO-STAR INT'L CO.,LTD		
MS-7984		
Size: Custom	Document Description: PCIE SLOT (X1)	Rev: 1.1
Date: Wednesday, June 17, 2015	Sheet 21 of 62	



H/W Strapping

PE_EC_SEL-
"H" for Express Card mode
"L" for PCIe Riser Card mode

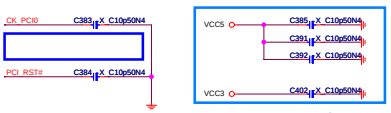
CLK100SEL-
"H" for PECLK input only
"L" for PECLK & PCICLK input

TEST_EN-
"H" for Test Mode Enable
"L" for Test Mode Disable

CLKRUN_EN-
"H" for CLKRUN Mode Disable
"L" for CLKRUN Mode Enable

I2CCLKSEL-
"H" is 135KHz I2CCLK
"L" is 67.5KHz I2CCLK

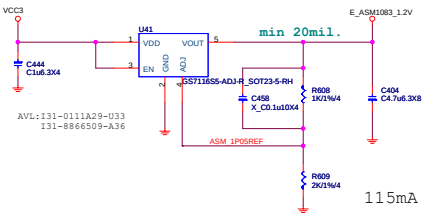
EMI



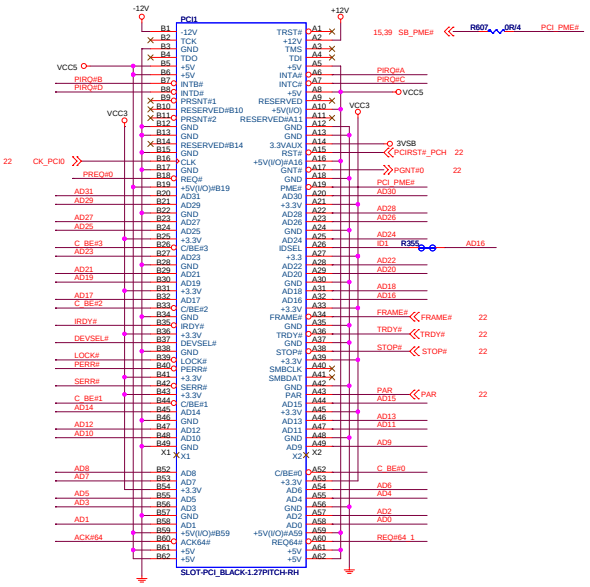
By Layout ,CK_PCI Reference Layer changed.

VCC3
90mA+115mA

Remove Cut Power.



MICRO-STAR INT'L CO.,LTD	
MS-7984	
Size: Custom	Document Description: PCIE to PCI-ASM1083
Rev: 1.1	
Date: Wednesday, June 17, 2015	Sheet 22 of 62

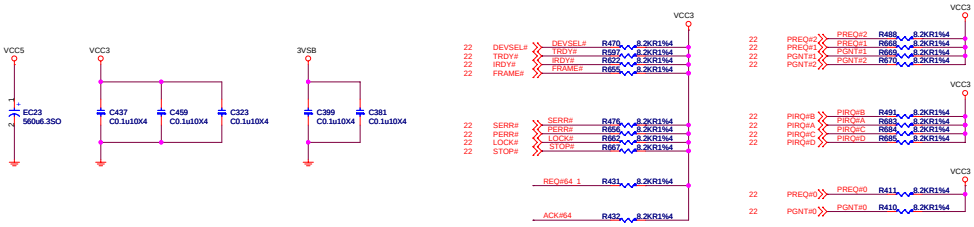


IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

AD[31..0] AD[31..0] 22

C_BE#[3..0] C_BE#[3..0] 22

PCI PULL-UP / DOWN RESISTORS



PCI slot (X3)	
+3.3Vaux (wake)	- 1125mA
+3.3Vaux (no wake)	- 60mA
+3.3V	- 7.6A
+5V	- 15A
+12V	- 1.5A

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7984	
Size: Custom	Document Description: PCI SLOT	Rev: 1.1
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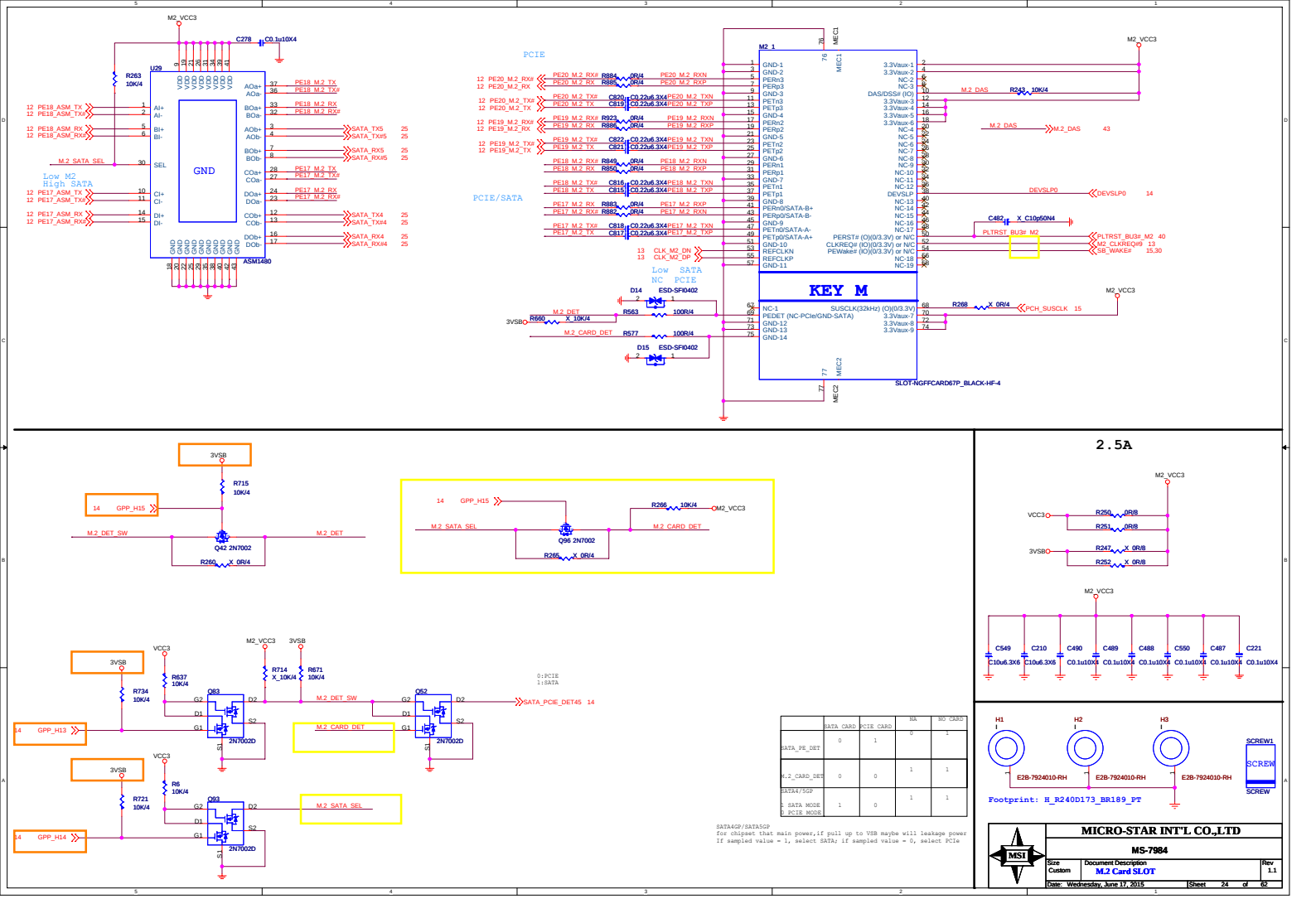
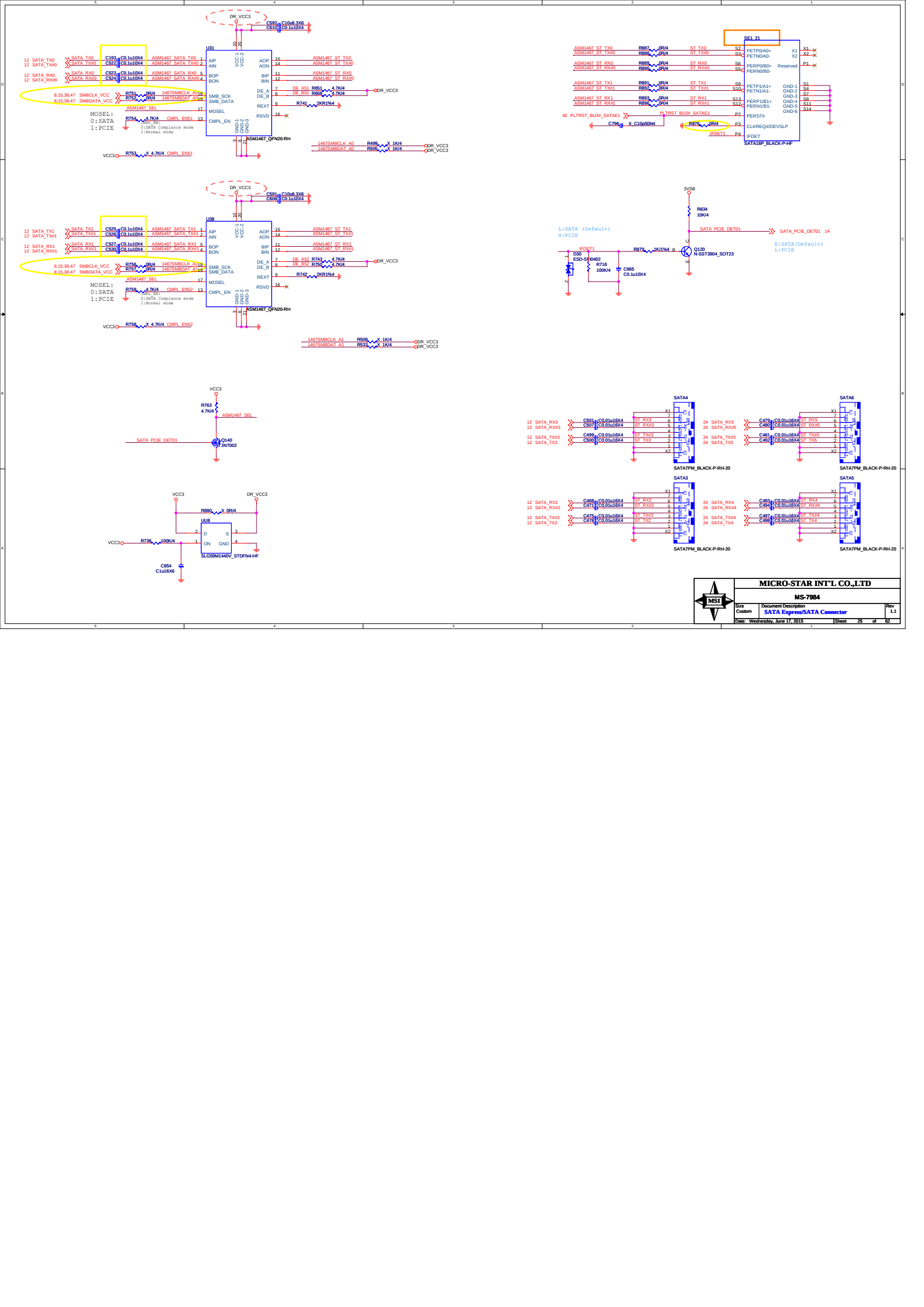


	SATA_CARD	PCIE_CARD	NA	NO_CARD
SATA_PE_DET	0	1	0	1
M.2_CARD_DET	0	0	1	1
SATA4/5GP			1	1
1 SATA MODE	1	0		
0 PCIE MODE				

SATA4GP/SATA5GP
for chipset that main power,if pull up to VSB maybe will leakage power
If sampled value = 1, select SATA; if sampled value = 0, select PCIe

2.5A

MICRO-STAR INT'L CO.,LTD		
MS-7984		
Size: Custom	Document Description: M.2 Card SLOT	Rev: 1.1
Date: Wednesday, June 17, 2015	Sheet 24 of 62	



Company	MICRO-STAR INT'L CO.,LTD
Model	MS-7984
Size	Custom
Document Description	SATA Express/SATA Connector
Rev	1.1
Date	Wednesday, June 17, 2015
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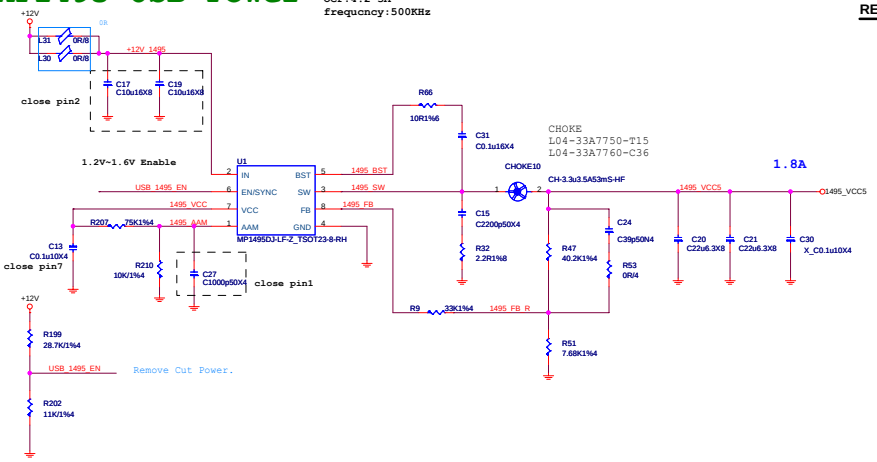
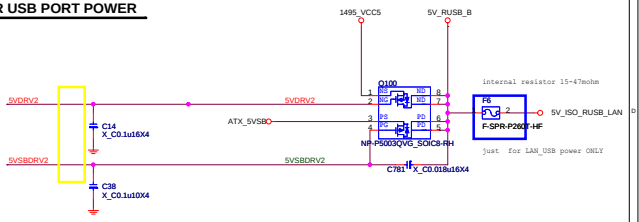
MP1495 USB Power

OCP:4.2~5A
frequcncy:500KHz



REAR USB PORT POWER

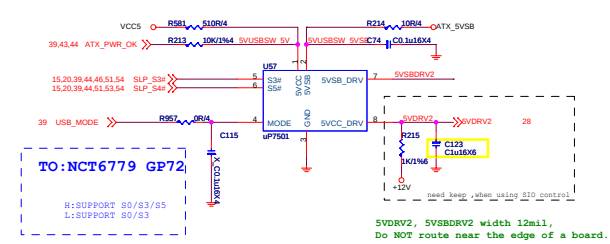


P-MOS
D03-06P0319-N03

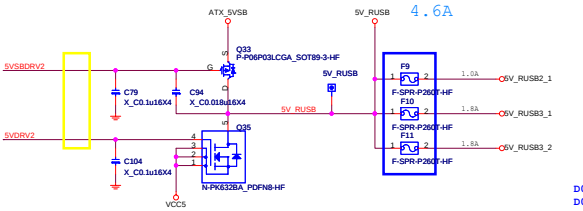
N-MOS
D03-510BA0C-N03
D03-3056M00-U47
D03-4C05N03-O05
D03-3830D09-N47
D03-632BA0C-N03

2A Fuse (1812)
D08-040022A-P16
D08-040020A-B07
D08-040021A-R02
2A Fuse (1206)
D08-0400800-B07
D08-0400900-L07

(D03-P500303-N03 N/P MOS can replace Q1/Q2)



5VDRV2, 5VSBDRV2 width 12mil,
Do NOT route near the edge of a board.

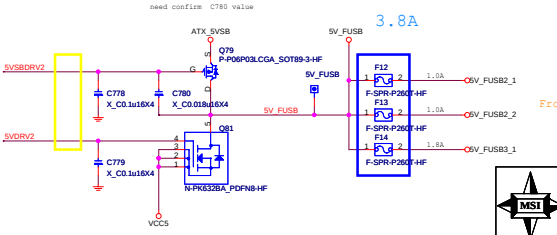


P-MOS
D03-06P0319-N03

N-MOS
D03-510BA0C-N03
D03-3056M00-U47
D03-4C05N03-O05
D03-3830D09-N47
D03-632BA0C-N03

D08-2000300-P16 (Itrip=3.5A; 0.003ohm)
D08-0300700-P16 (Itrip=2.6A; 0.015ohm)

need confirm C780 value



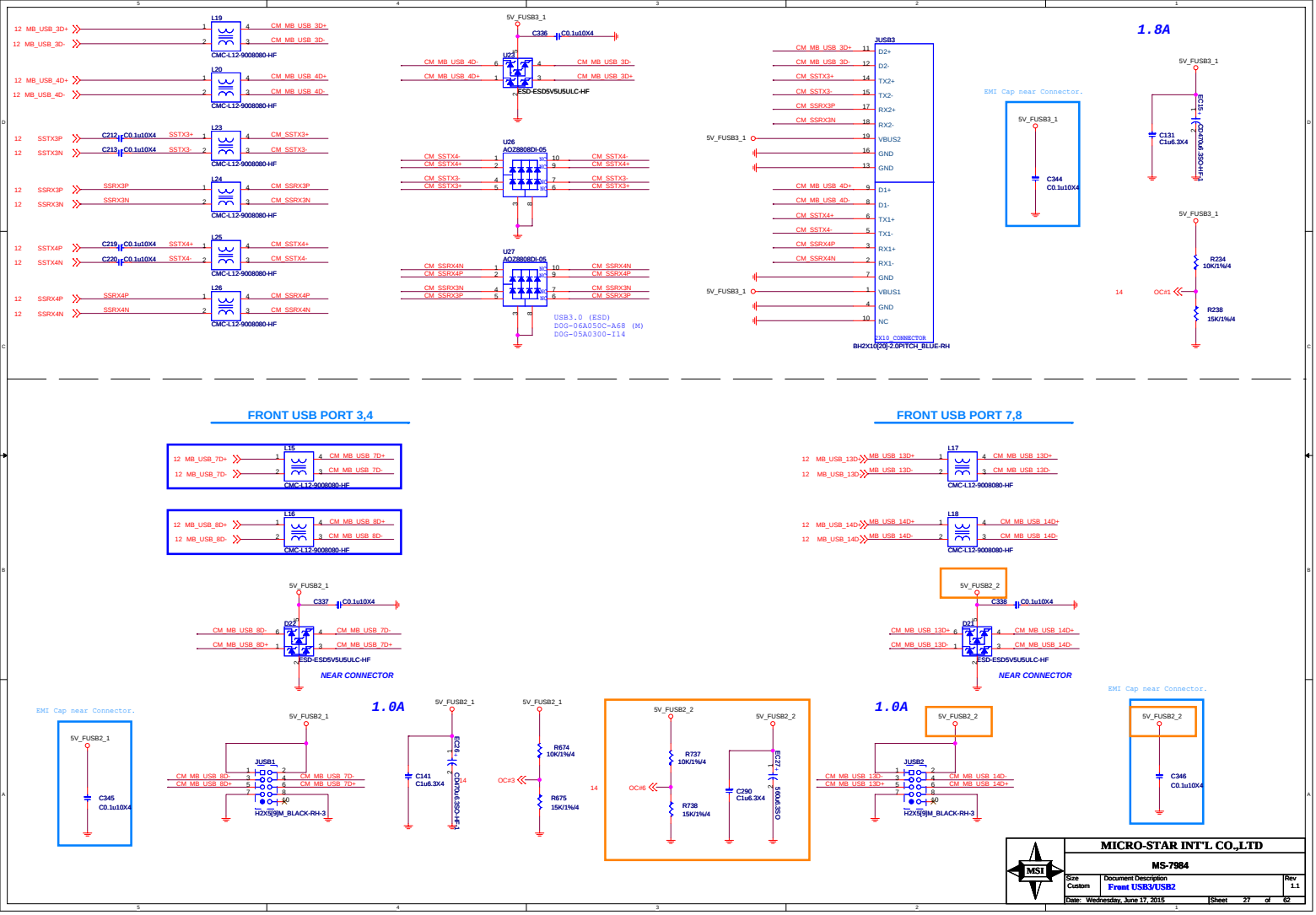
Front USB2.0 Voltage Drop Fail.

MICRO-STAR INT'L CO.,LTD

MS-7984

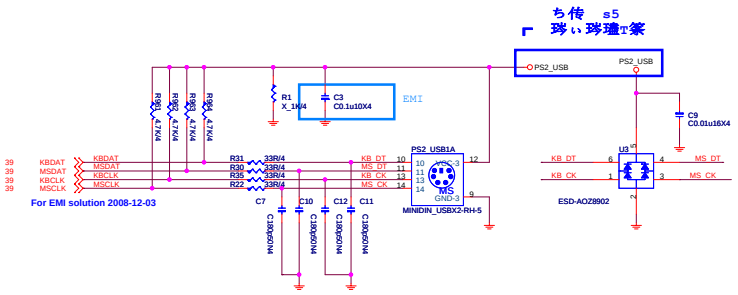
Size	Document Description	Rev
Custom	USB POWER-MP1495/UP7501	1.1

Date: Wednesday, June 17, 2015 | Sheet 26 of 62

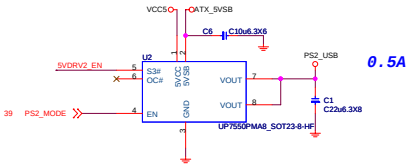


MICRO-STAR INT'L CO.,LTD		
MS-7984		
Size: Custom	Document Description: Front USB3/USB2	Rev: 1.1
Date: Wednesday, June 17, 2015	Sheet 27 of 62	

PS2 KEYBOARD & MOUSE CONNECTOR

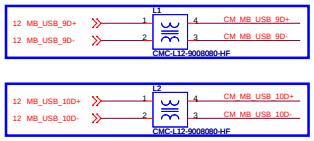


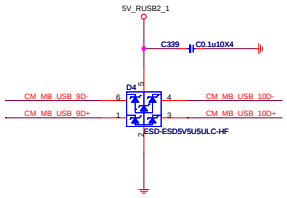
PS2 Power

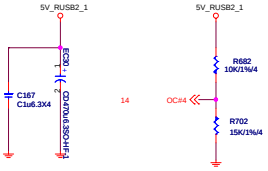


USB MODE

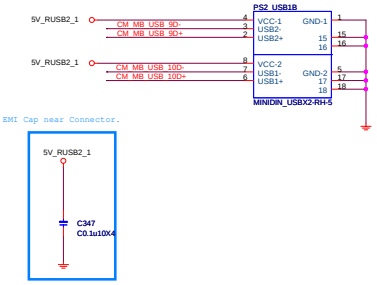
REAR USB PORT 2,3 (W/ PS2)



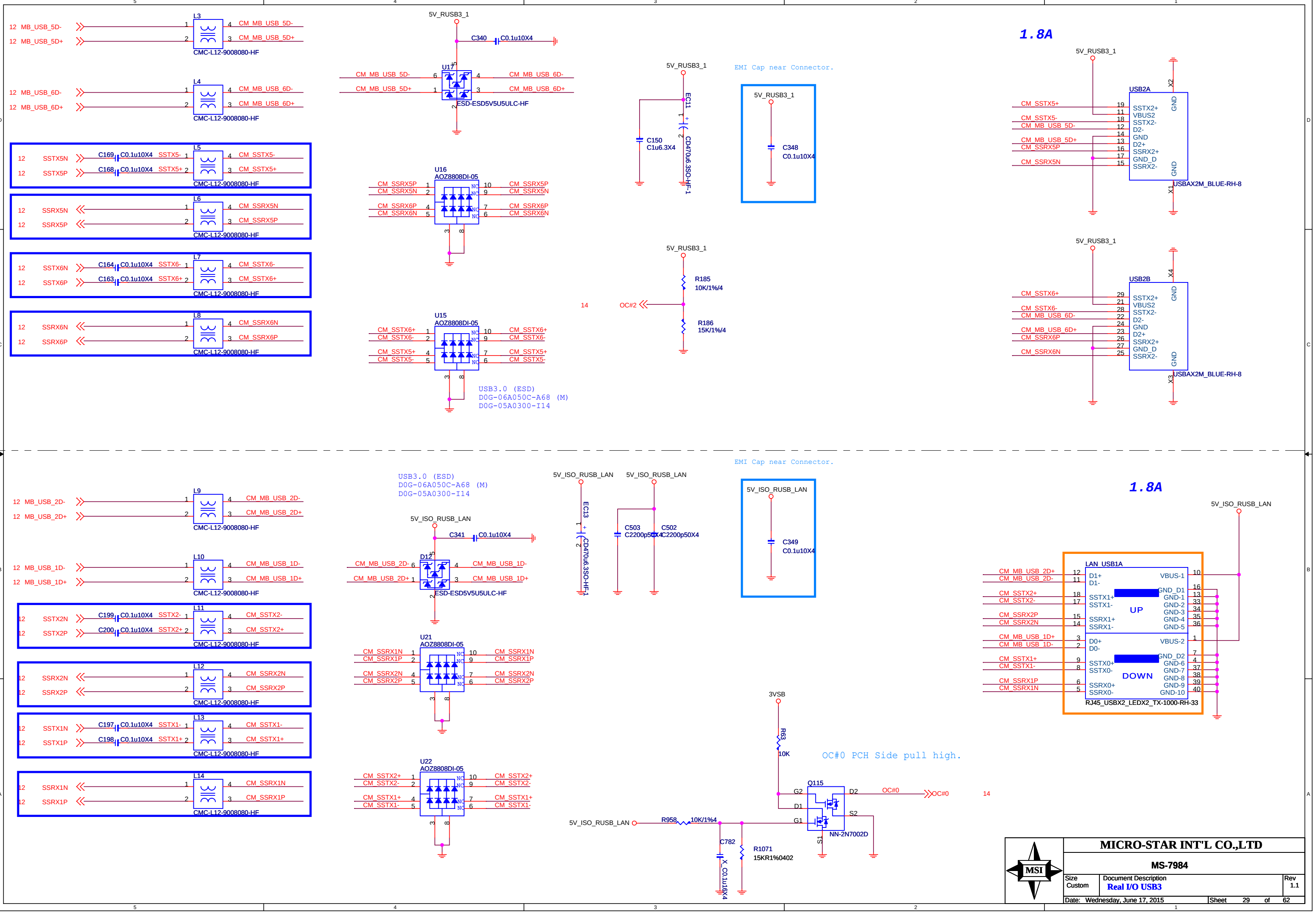




1.0A



MICRO-STAR INT'L CO.,LTD		
MS-7984		
Size: Custom	Document Description: Rear I/O PS2/USB2	Rev: 1.1
Date: Wednesday, June 17, 2015	Sheet 28 of 62	



MICRO-STAR INT'L CO.,LTD

MS-7984

Size	Document Description	Rev
Custom	Real I/O USB3	1.1

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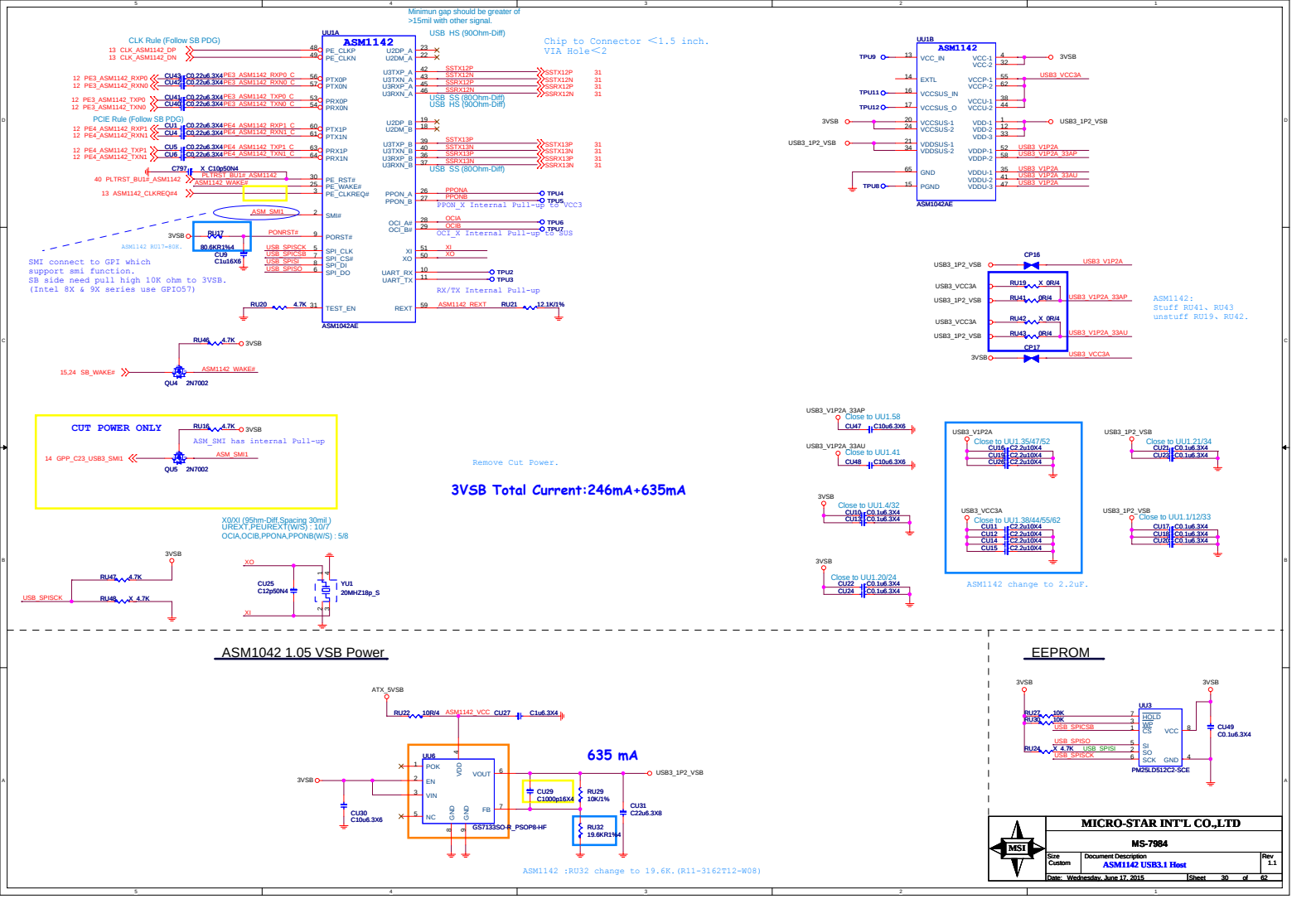

MICRO-STAR INT'L CO.,LTD		
MS-7984		
Size: Custom	Document Description: ASM1142 USB3.1 Host	Rev: 1.1
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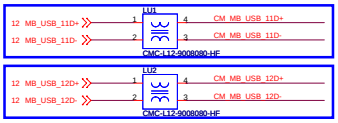
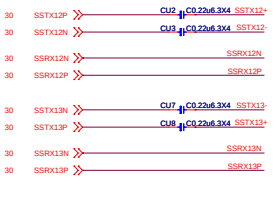
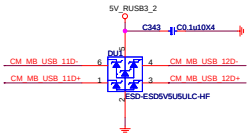
Rear USB3 CONN

Important~~
If USB3.0 signal conect to front pin header,
please must less than 1.5 inch,short trace
has better eye diagram with some bad fly cable by SI customer.

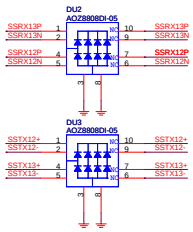




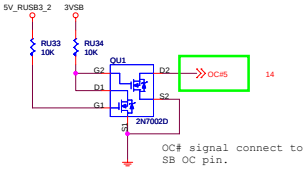
USB2.0
D0G-0200529-A68 Main
D0G-0100619-I05 AVL



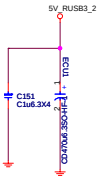
ESD Protection
NEAR CONNECTOR



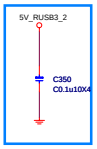
USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL



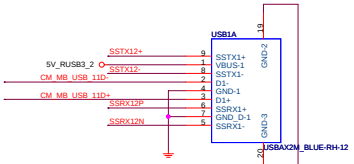
min 80mil.
1.8 A



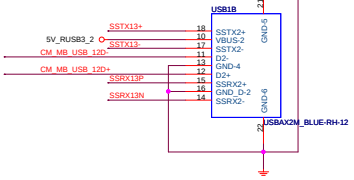
EMI Cap near Connector.



From PCH.

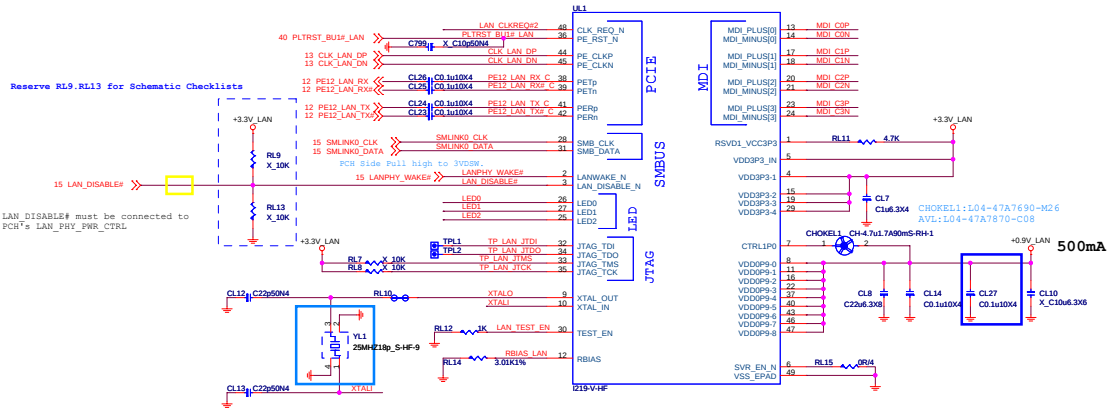


From PCH.

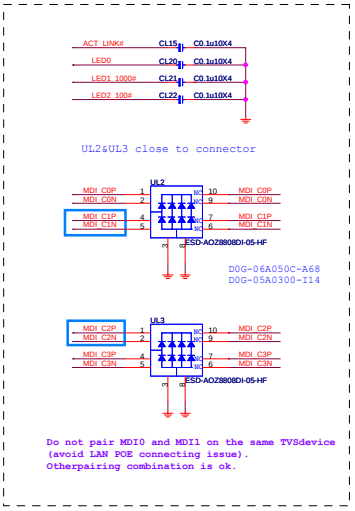


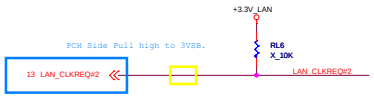
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7984	
Size: Custom	Document Description: Rear USB3.1 Connector	Rev: 1.1
Date: Wednesday, June 17, 2015	Sheet 31 of 62	

Intel I219V / I218V PHY



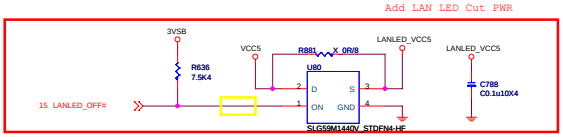
For EMI



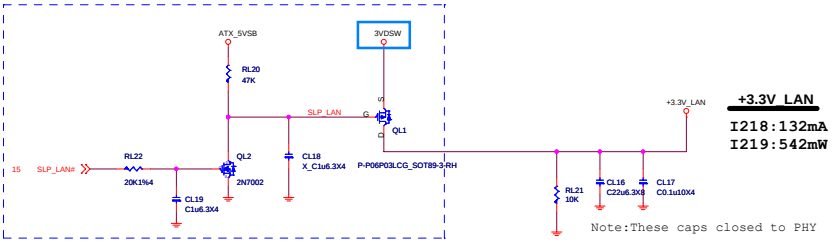


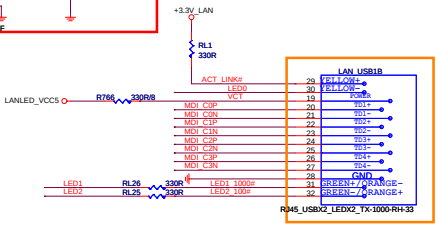
The 10Kohm pull-up resistor (RL18) of CLK_REQ_N is connected to 3.3V Suspend/Core/etc. power well, depending on the power well of PCH's input PCIECLKRQ<n> buffer.

Add LAN LED Cut PWR



support WOL from Deep Sx:
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218/i219.





MICRO-STAR INT'L CO.,LTD		
MS-7984		
Size: Custom	Document Description: LAN Killer E2205	Rev: 1.1
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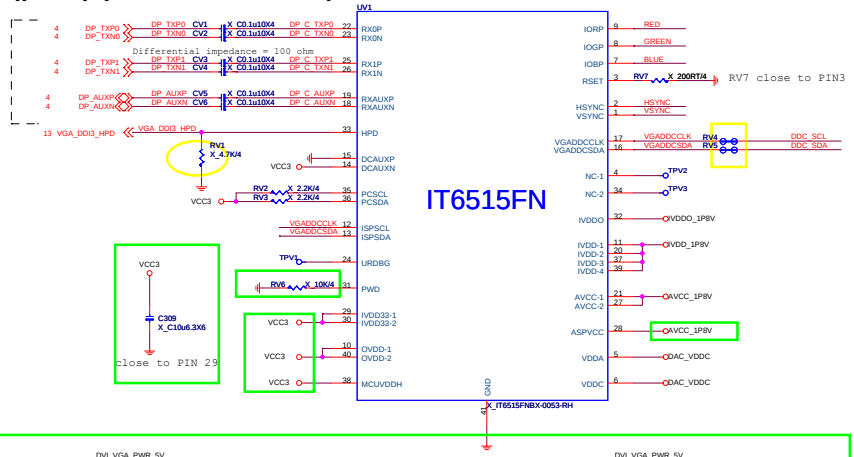
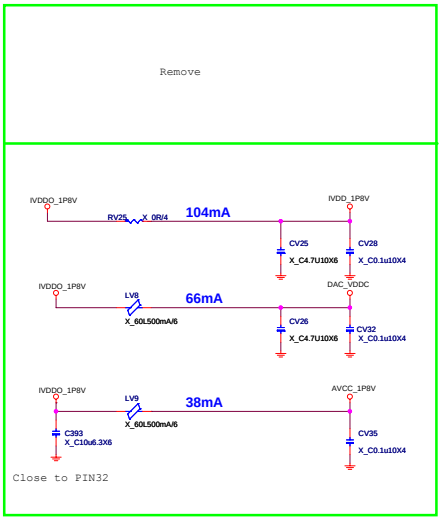
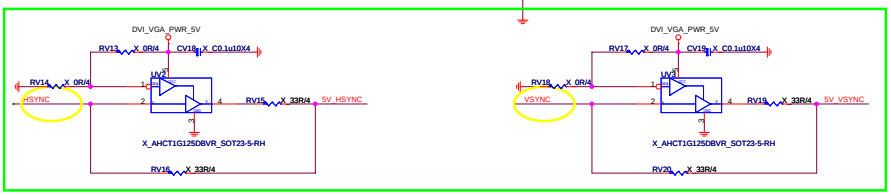
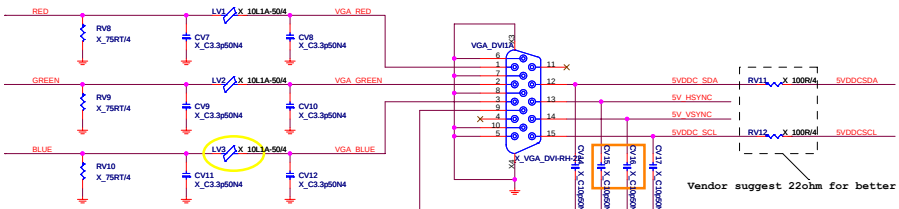
Note:

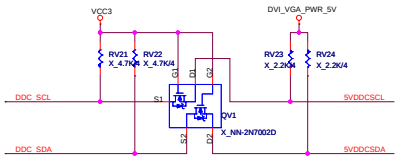
If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining











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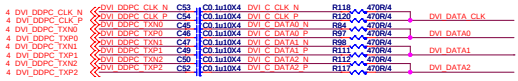
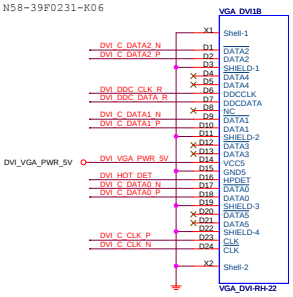
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

Check MSI PN
N58-39F0231-K06





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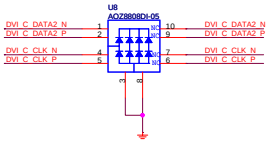

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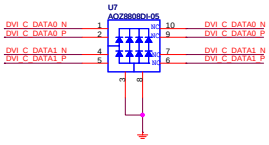

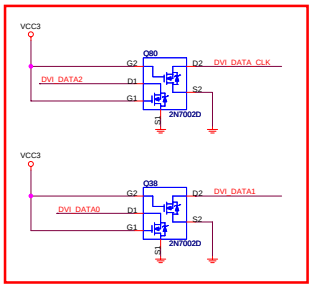

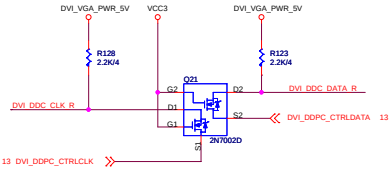

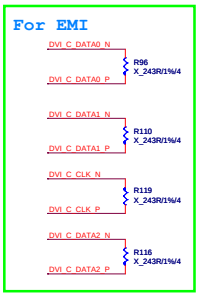

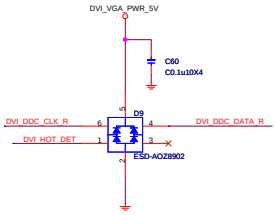

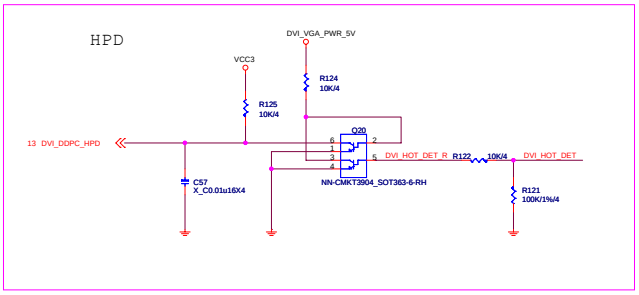

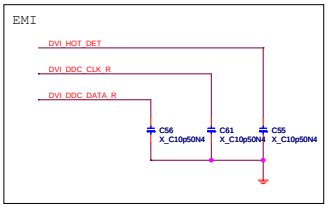

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HDMI level shifter

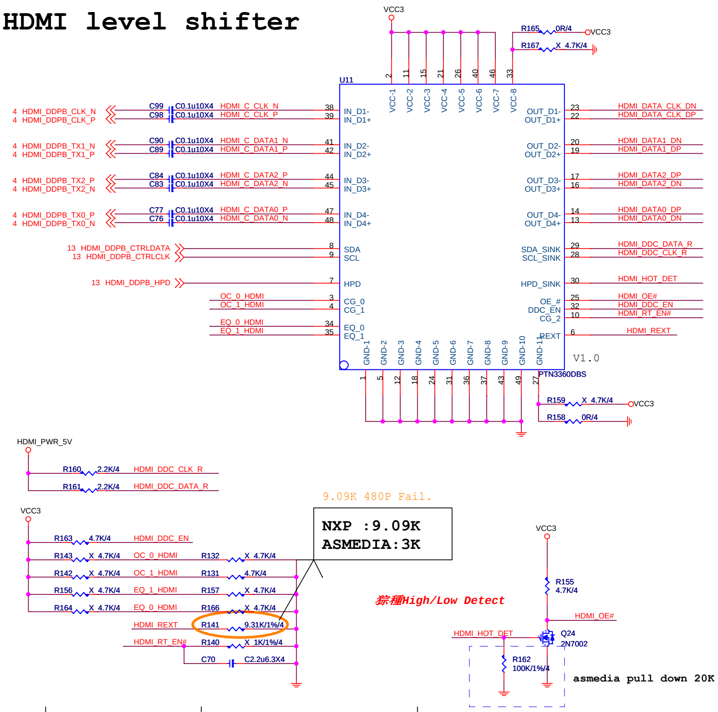
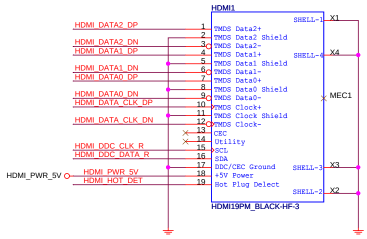
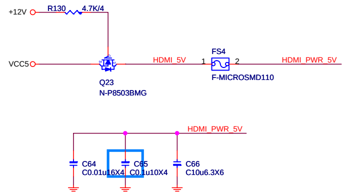


Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMDSB_DATA2#	DDPB_0N
	DDSP_B_TX0_DP	TMDSB_DATA2	DDPB_0P
	DDSP_B_TX1_DN	TMDSB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMDSB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMDSB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMIB_CTRL_CLK	HDMI DDC lines for Port B
	SDVO_CTRLDATA	HDMIB_CTRL_DATA	



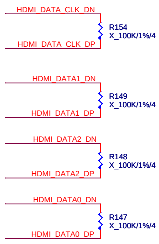


	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant
DDCBUF_EN	For DDC level shifitng configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

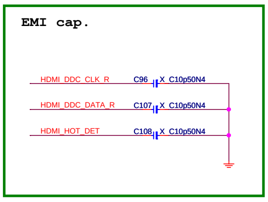
[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

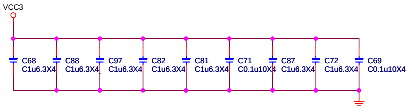
PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

EMI



EMI cap.





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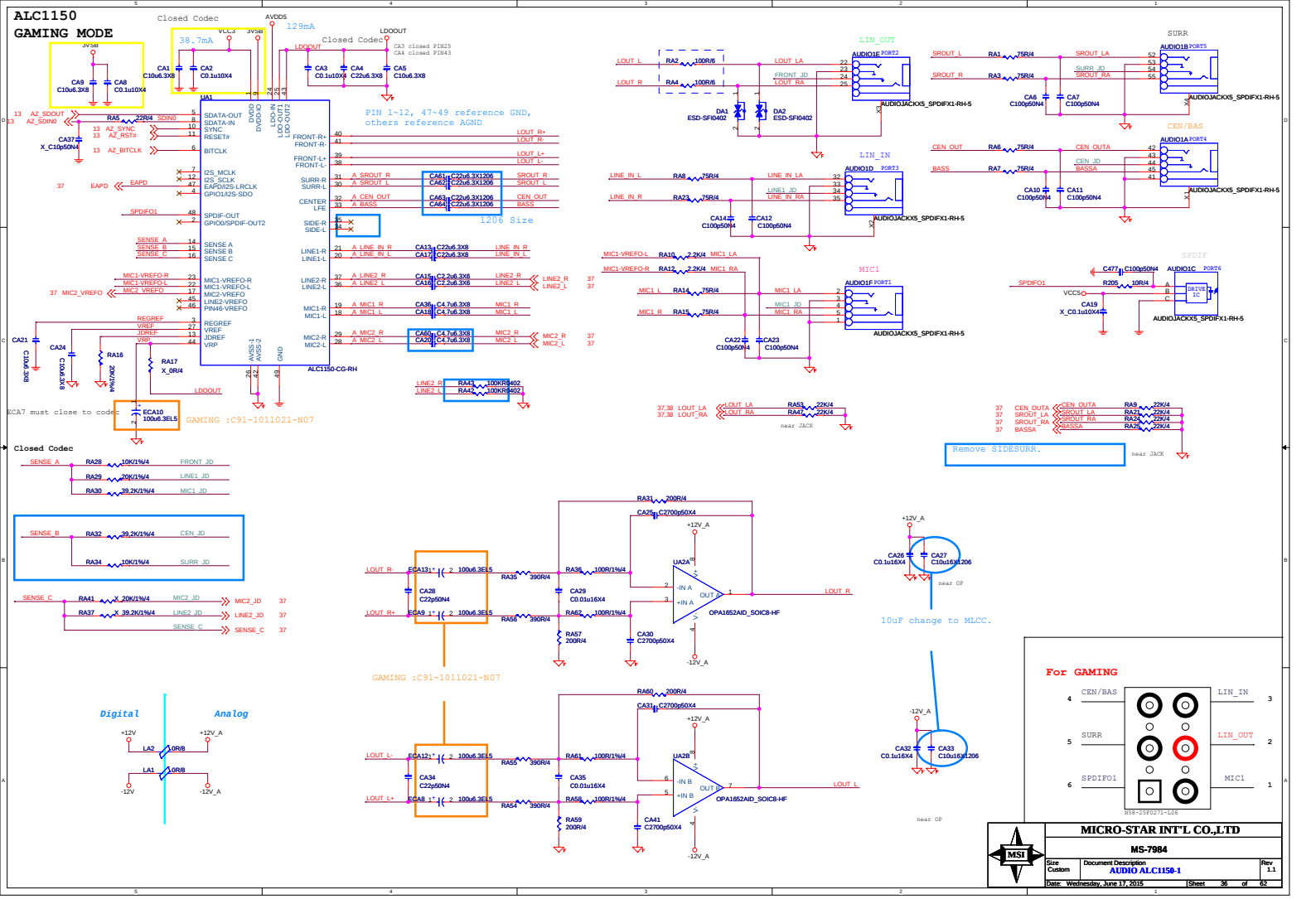
ALC1150
GAMING MODE



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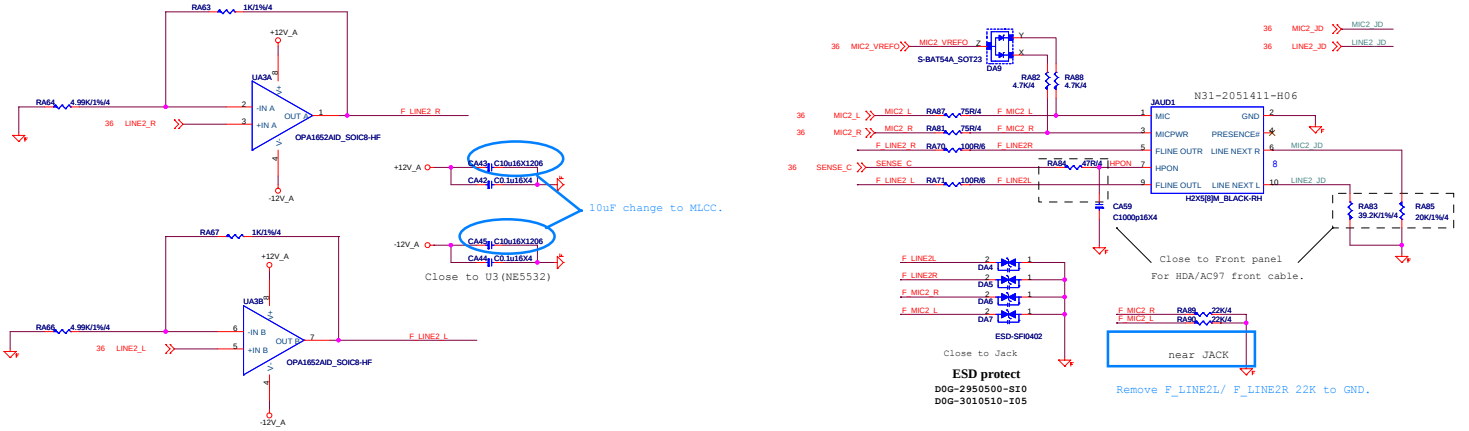
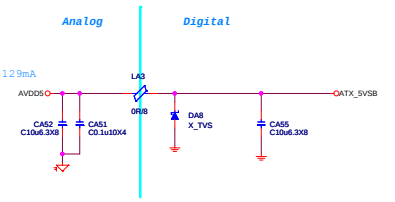
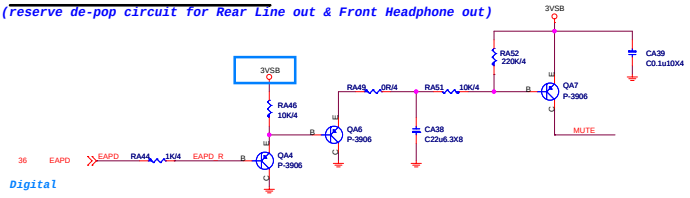


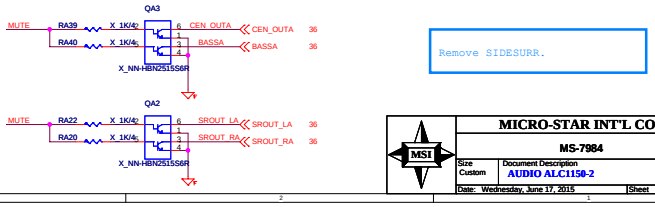


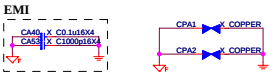
Rear Line OUT De-POP circuit

(reserve de-pop circuit for Rear Line out & Front Headphone out)



(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change CA6,CA7, CA12, CA13, CA23, CA24 to TVS)





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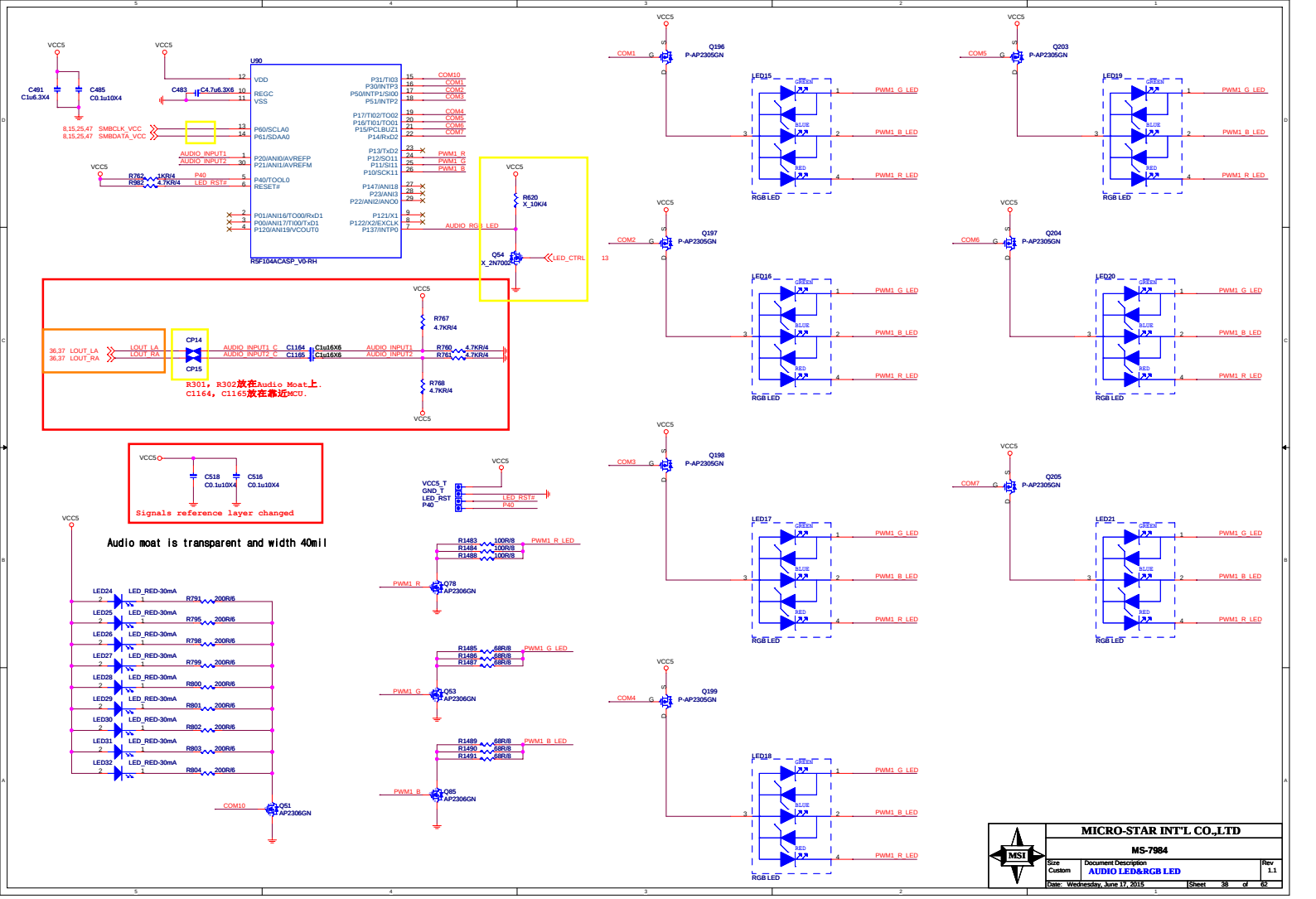
U90
R5F104ACASP_V0-RH
R620
X_10K/4
Q54
X_2N7002
LED_CTRL
AUDIO_RGB_LED
CP14
CP15
C1164
C1165
C1u16X6
R760
R761
R767
R768
4.7KR/4
R301, R302放在Audio Moat上.
C1164, C1165放在靠近MCU.
Signals reference layer changed
Audio moat is transparent and width 40mil
Q196
Q197
Q198
Q199
Q202
Q204
Q205
P-AP2305GN
LED15
LED16
LED17
LED18
LED19
LED20
LED21
RGB LED
PWM1_G_LED
PWM1_B_LED
PWM1_R_LED
Q78
Q53
Q85
AP2306GN
R1483
R1484
R1488
R1485
R1486
R1487
R1489
R1490
R1491
100R/8
68R/8
LED24
LED25
LED26
LED27
LED28
LED29
LED30
LED31
LED32
LED_RED-30mA
R791
R795
R798
R799
R800
R801
R802
R803
R804
200R/6
Q51
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AUDIO LED&RGB LED
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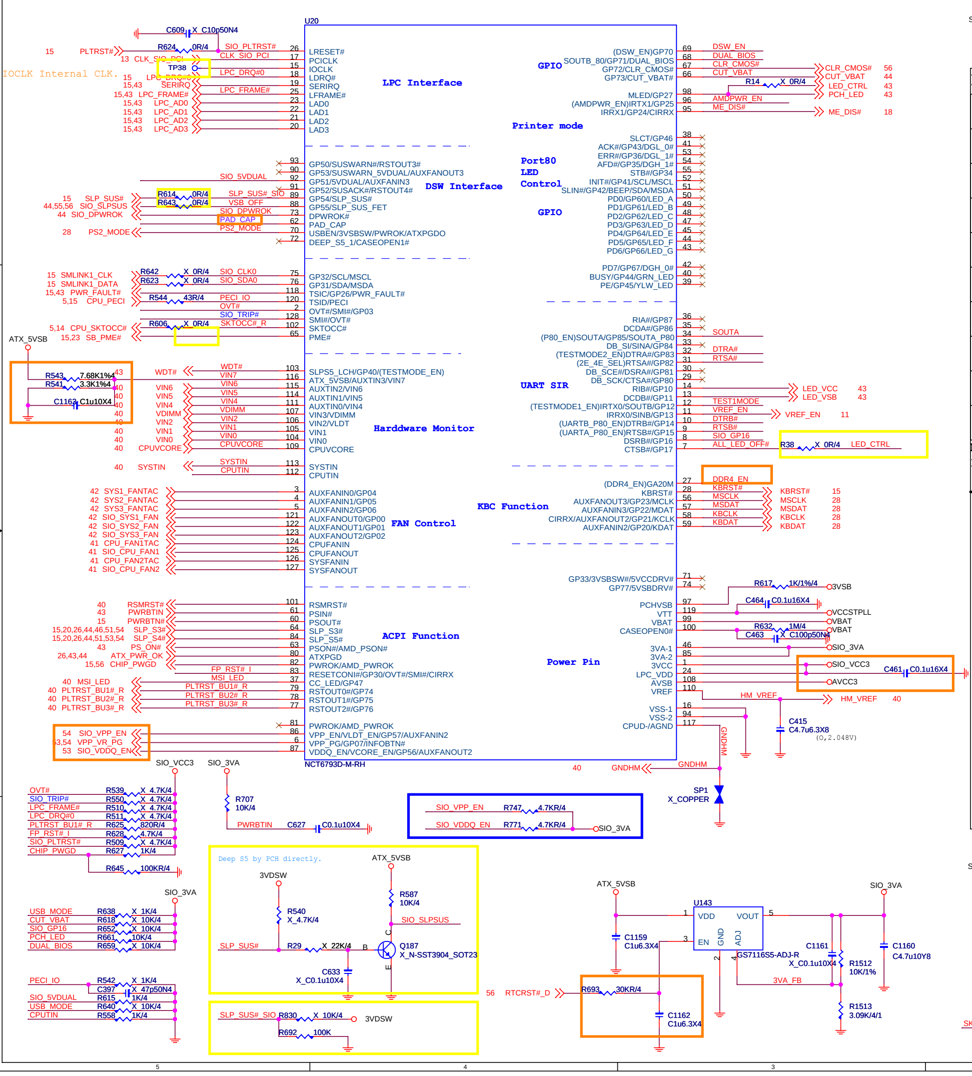


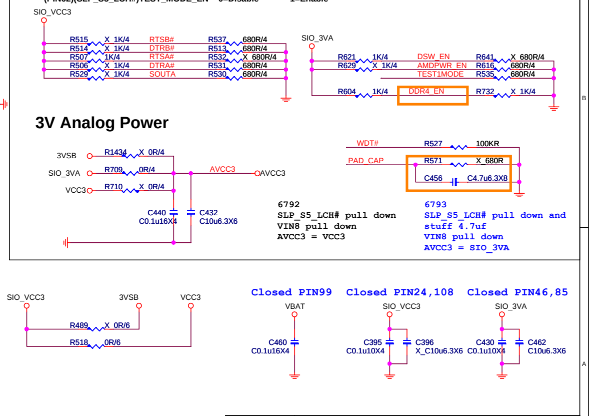
POWER ON STRAPPING PIN FOR NCT6792

PIN	6792 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	24_48_SEL	DTRA#	24M CLOCK SOURCE	48M CLOCK SOURCE	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
62	TESTMODE_EN	SLP_S5_LCH#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST

Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO

SIO Pin Strap

(PIN31)RTSA# 0=2E 1=4E
(PIN32)DTRA# 0=24MHz 1=48MHz
(PIN34)SOUTA 0=Port80 Enable 1=PRT Enable
(PIN69)DSW_EN 0=Disable 1=Enable
(PIN9))(RTSB#)ORT80_EN 0=Disable 1=Enable
(PIN96)AMDPWR_EN 0=Disable 1=Enable
(PIN62)(SLP_S5_LCH#)TEST_MODE_EN 0=Disable 1=Enable



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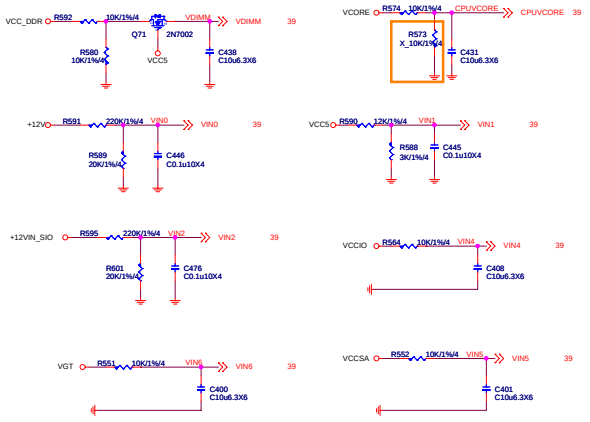
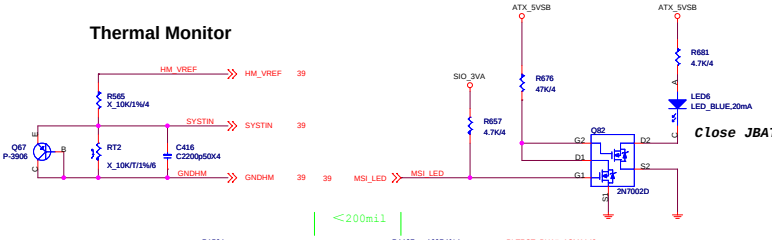
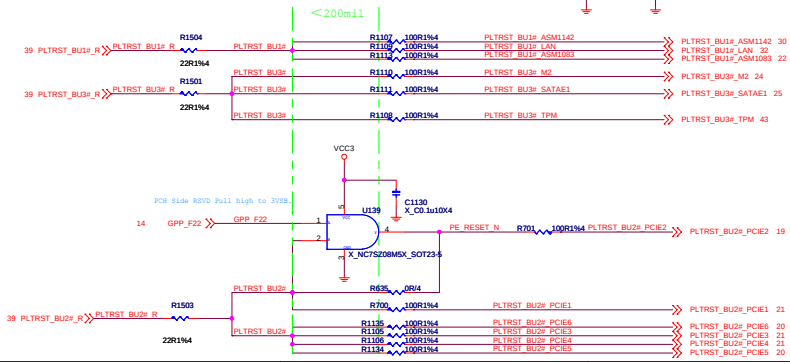
HW Monitor - Voltage

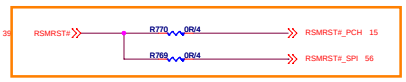
SIO HW Voltage voer 2V will not detect



Thermal Monitor







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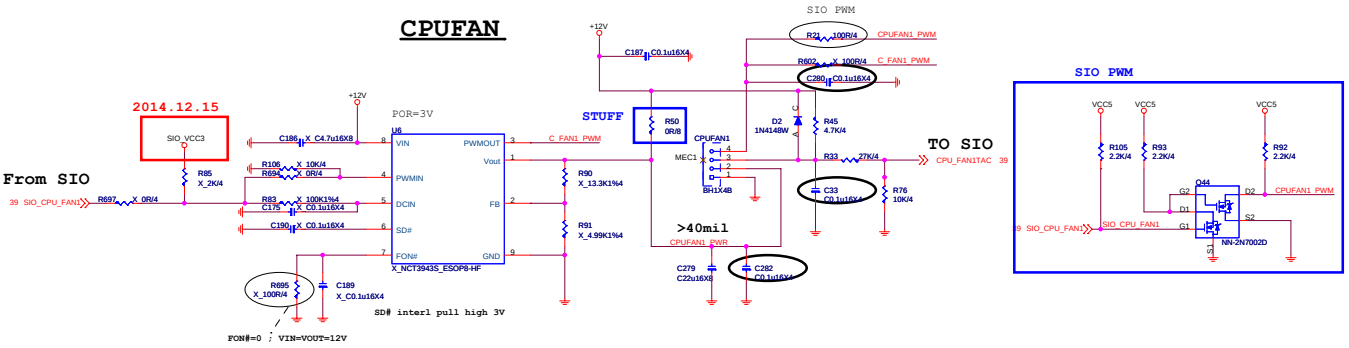
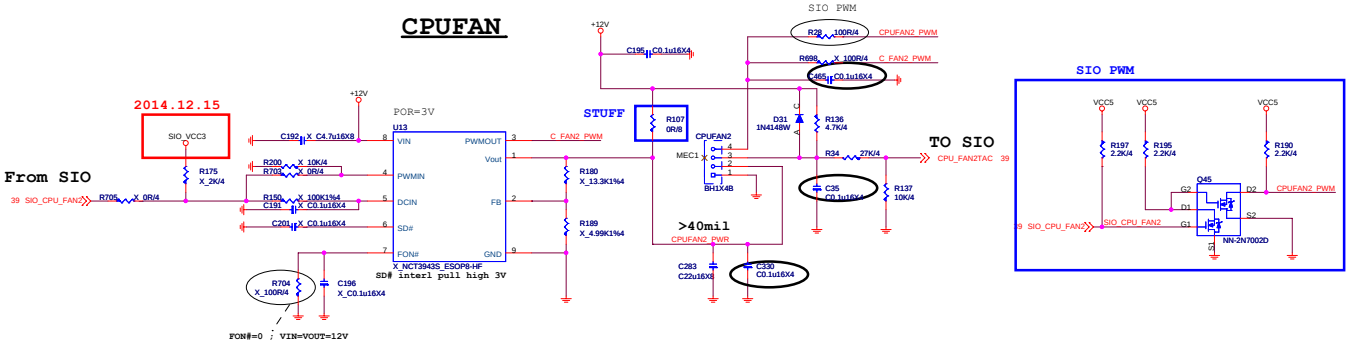
Type G : 4 PIN CPU FAN USE SIO PWM (Reserve NCT3943S & WITHOUT CUT POWER)



WITHOUT CUT POWER

BOM OPT	R602	R21	R105	R93	R92	Q44	R697	R85	R106	R694	R83	C175	R695	C186	U6	R90	R91	R50
SIO PWM	X	O	O	O	O	O	X	X	X	X	X	X	X	X	X	X	X	O

Type G : 4 PIN CPU FAN USE SIO PWM (Reserve NCT3943S & WITHOUT CUT POWER)



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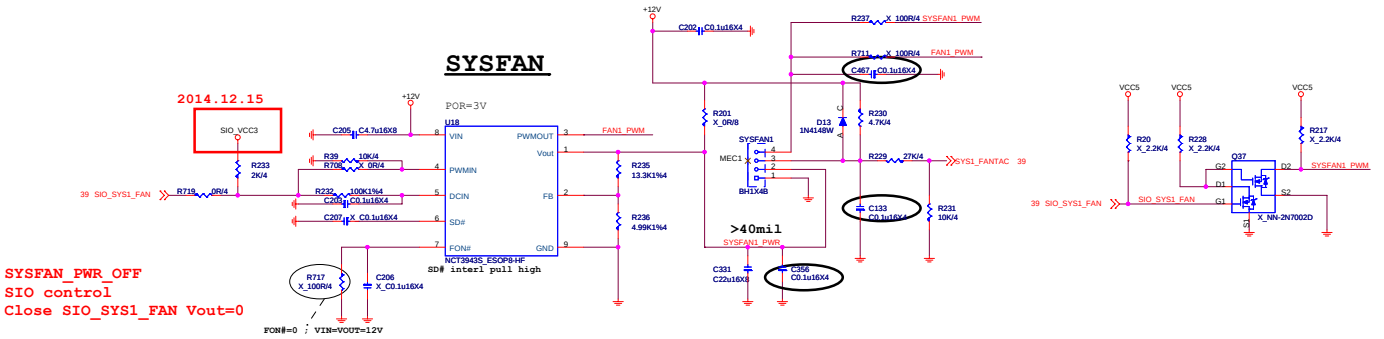
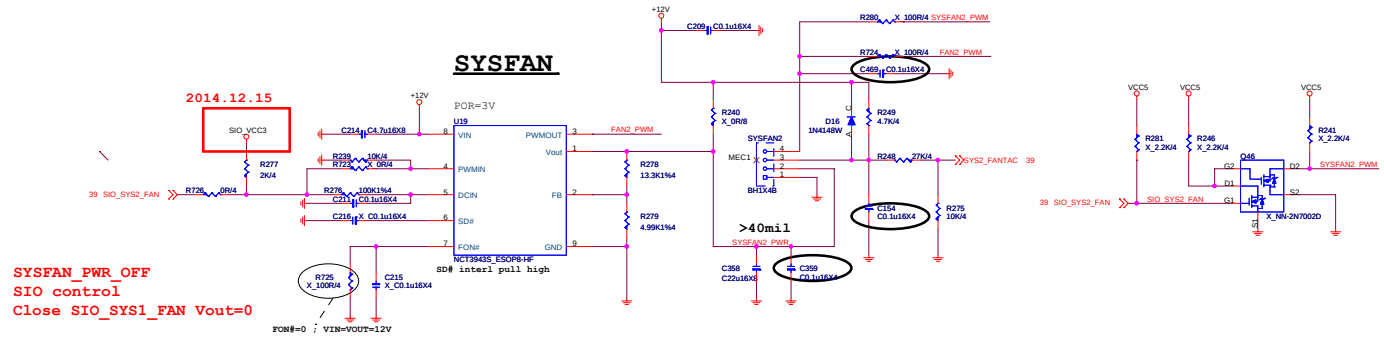
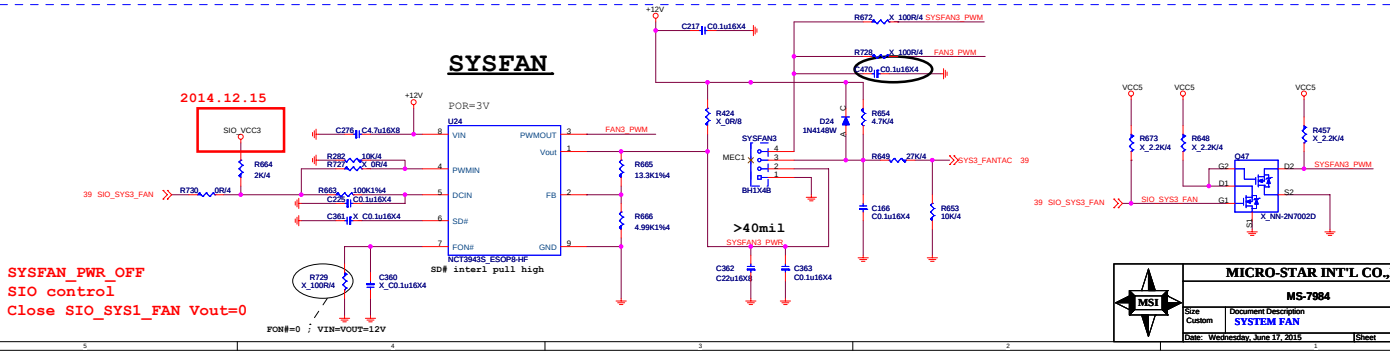
Type H : 4/3 PIN SYS FAN FROM NCT3943S(USE SIO CUT POWER)







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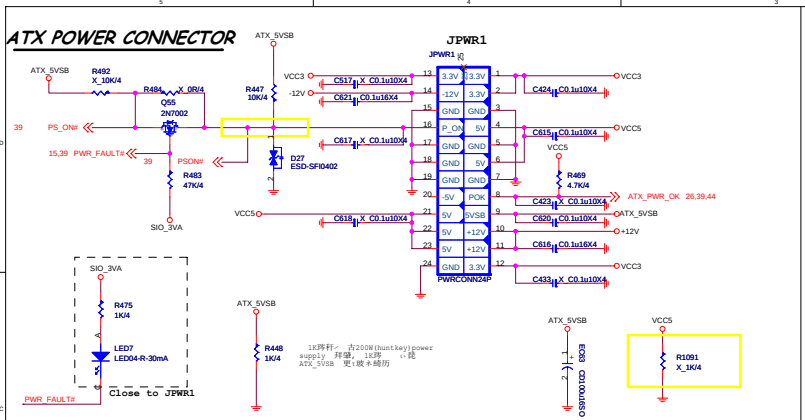

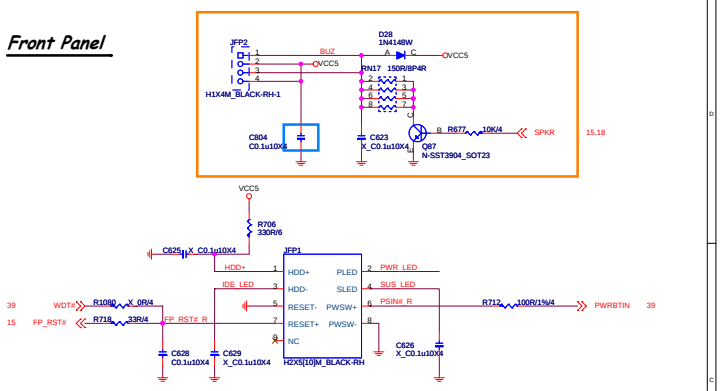

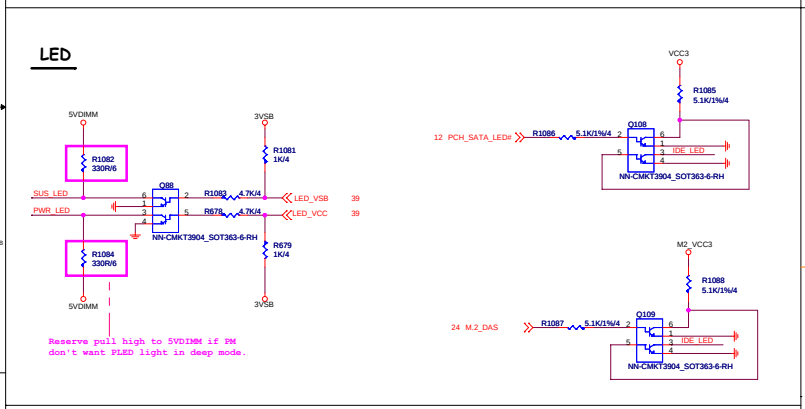

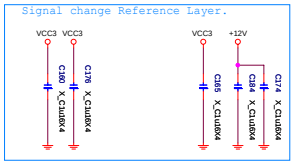

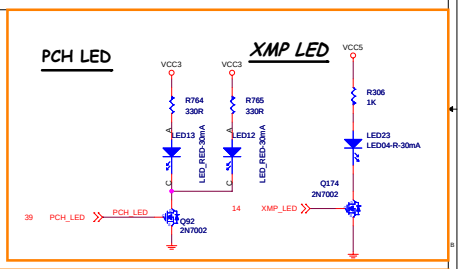

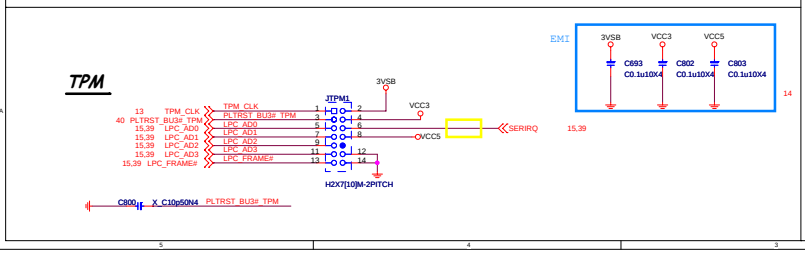

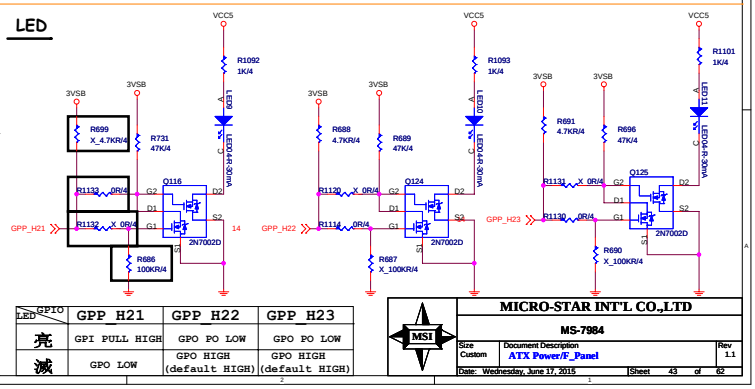

GPIO / LED	GPP_H21	GPP_H22	GPP_H23
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

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Size: Custom | Document Description: ATX Power/F_Panel | Rev: 1.1

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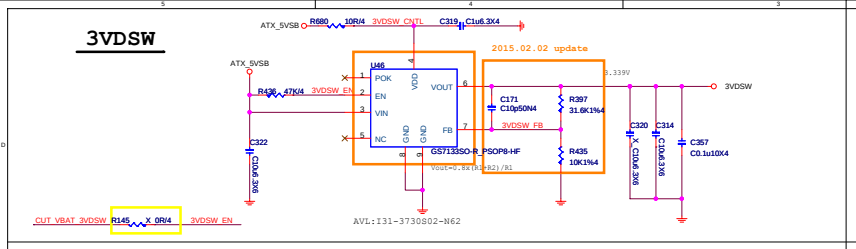

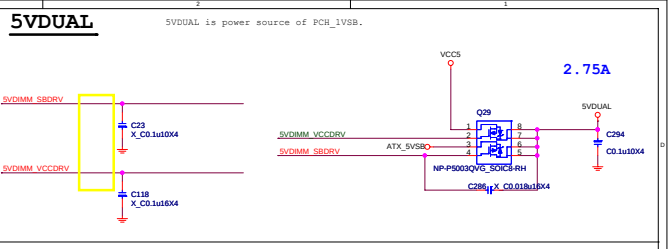

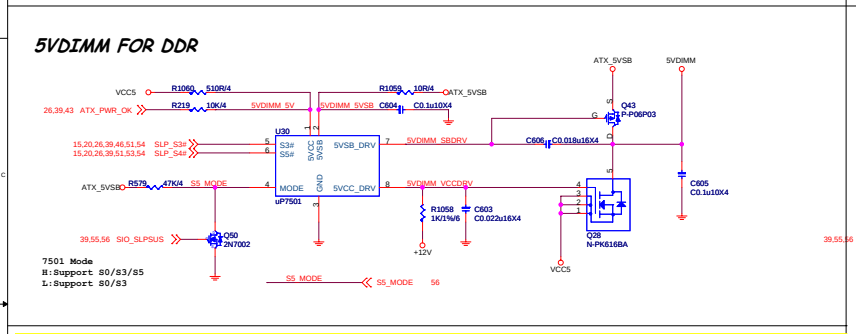

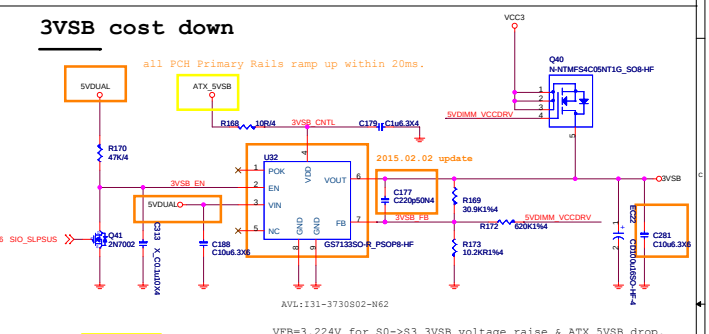

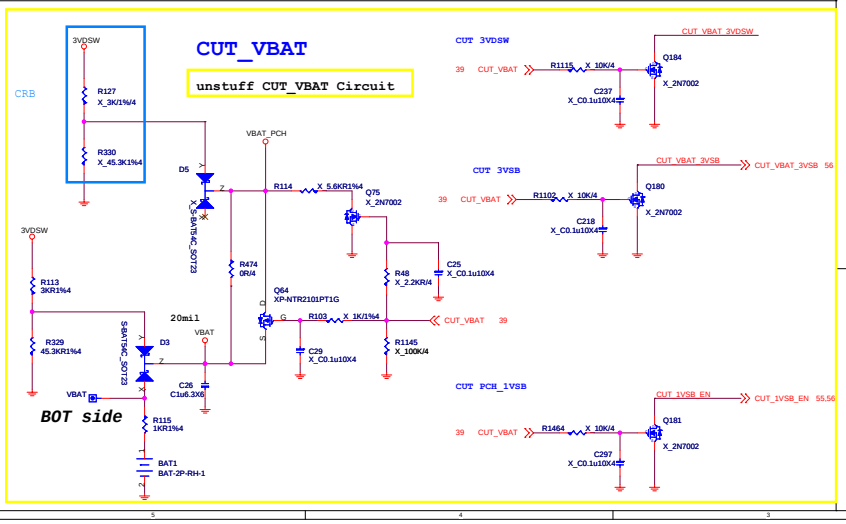

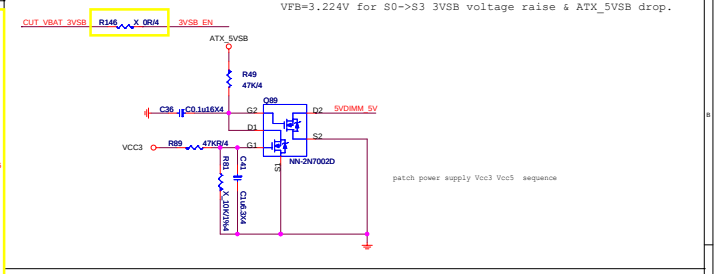

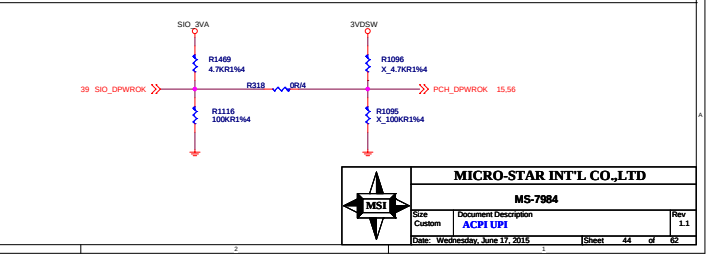

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Custom	ACPI UP1	1.1

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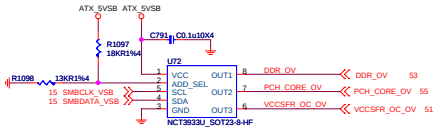
Remove Cut Power.

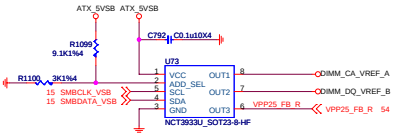
UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=13K



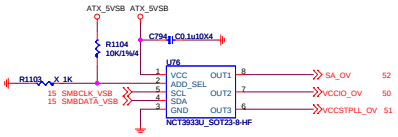
UPI VOLTAGE CONSOLE

0x28:RH=9.1K,RL=3K



UPI VOLTAGE CONSOLE

0x20:RH=10K,RL=OPEN



ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

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Custom	OV-NCT3933/GPIO-NCT5605	1.1

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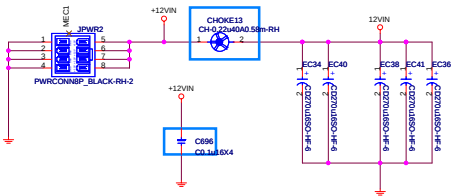
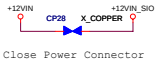
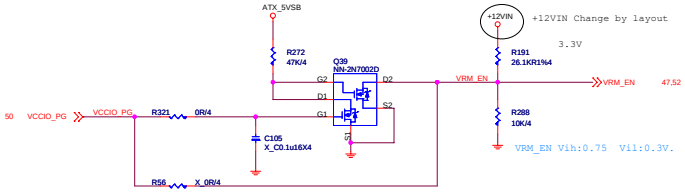


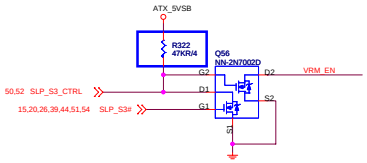
Iripple=30.95A
VCORE 18.101A
VGT 8.457A
VCCSA 4.392A



Close Power Connector

VRM_EN Control from VCCIO_PG

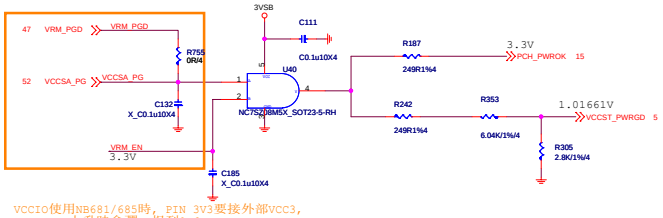




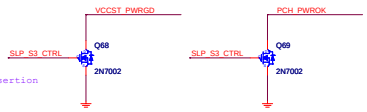
PCH_PWROK Control from VCCIO_PG&VCCSA

VCCST_PWRGD Control from VRM_PGD

VCCSA&Vcore use same PWM IC, pull up VCC3
VCCSA&Vcore use different PWM IC,pull up VCCSA
VCCST_PWRGD can assert before or equal to PCH_PWROK, but must never lag it.



VCCIO使用NB681/685時, PIN 3V3要接外部VCC3,
VCCIO_PG上升時會彈一根到0.6V,
所以PCH_PWROK前端控制的VCCIO_PG改接VRM_EN.



For VCCST_PWRGD deassertion
max:1us

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The total Length of Data and Clock (from CPU to each VR) must be equal (≯ 0.1 inch).data & clk mismatch

Route the Alert signal between the Clock and the Data signals.

Constraint: 5/10/15

SVID Addr 00h : VCORE
SVID Addr 01h : VGT
SMBus Addr: XXh

Vcore Iccmax=100A
VGT Iccmax =48A

TDP: 95W

VGT Total OCP: 90A

4+3 Application: VCORE+VGT

PWM1~PWM3	For VCORE 79A
PWM4~PWM5	For VGT 51A

close to VRM < 0.1"

close to VRM <0.1"

RC22 change 0603 to 0402

CLOSE Q194

CLOSE Q212

CLOSE L38 or L39 PIN2

VCORE

VGT

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MS-7984	
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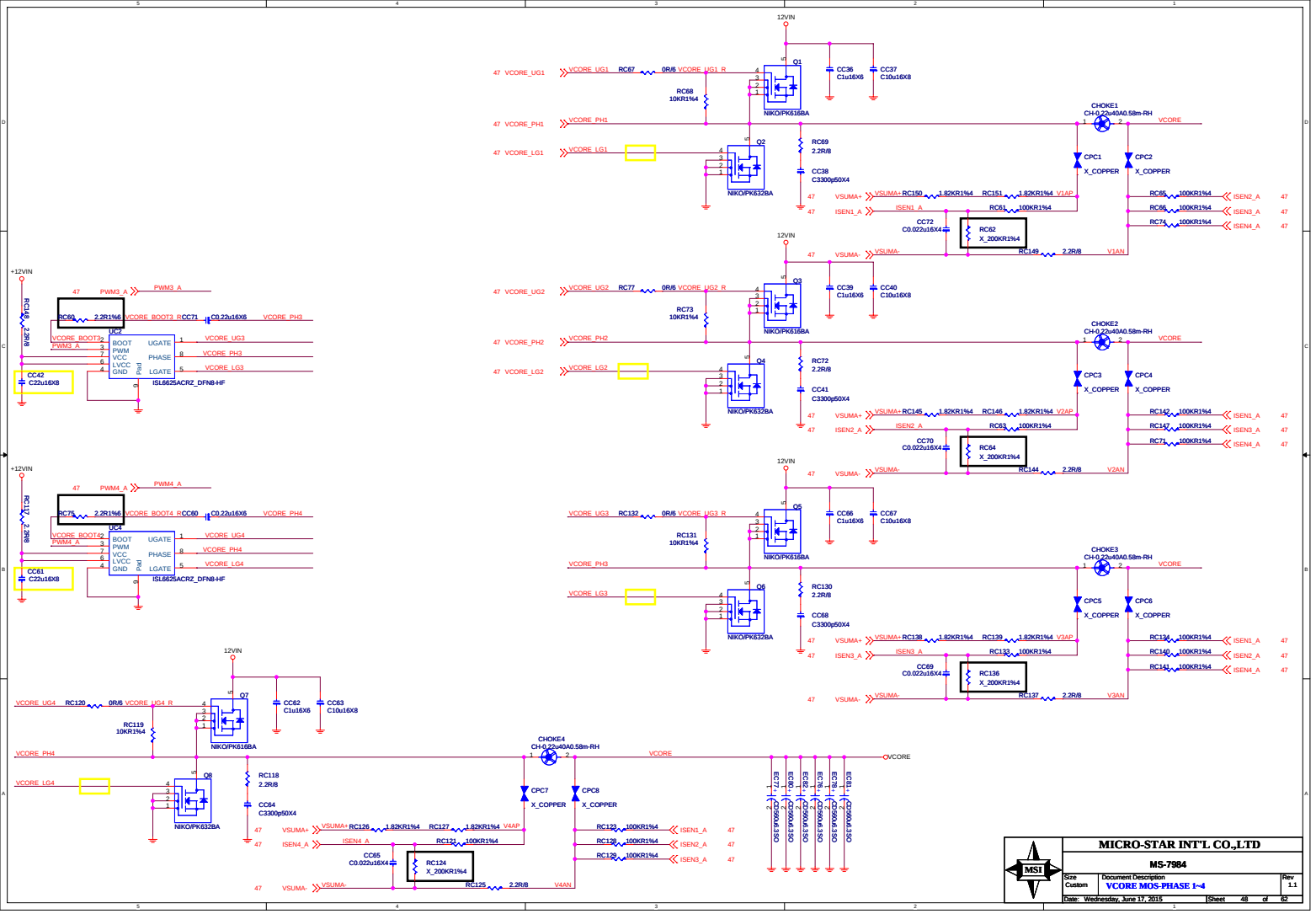

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Size: Custom	Document Description: VCORE MOS-PHASE 1~4	Rev: 1.1
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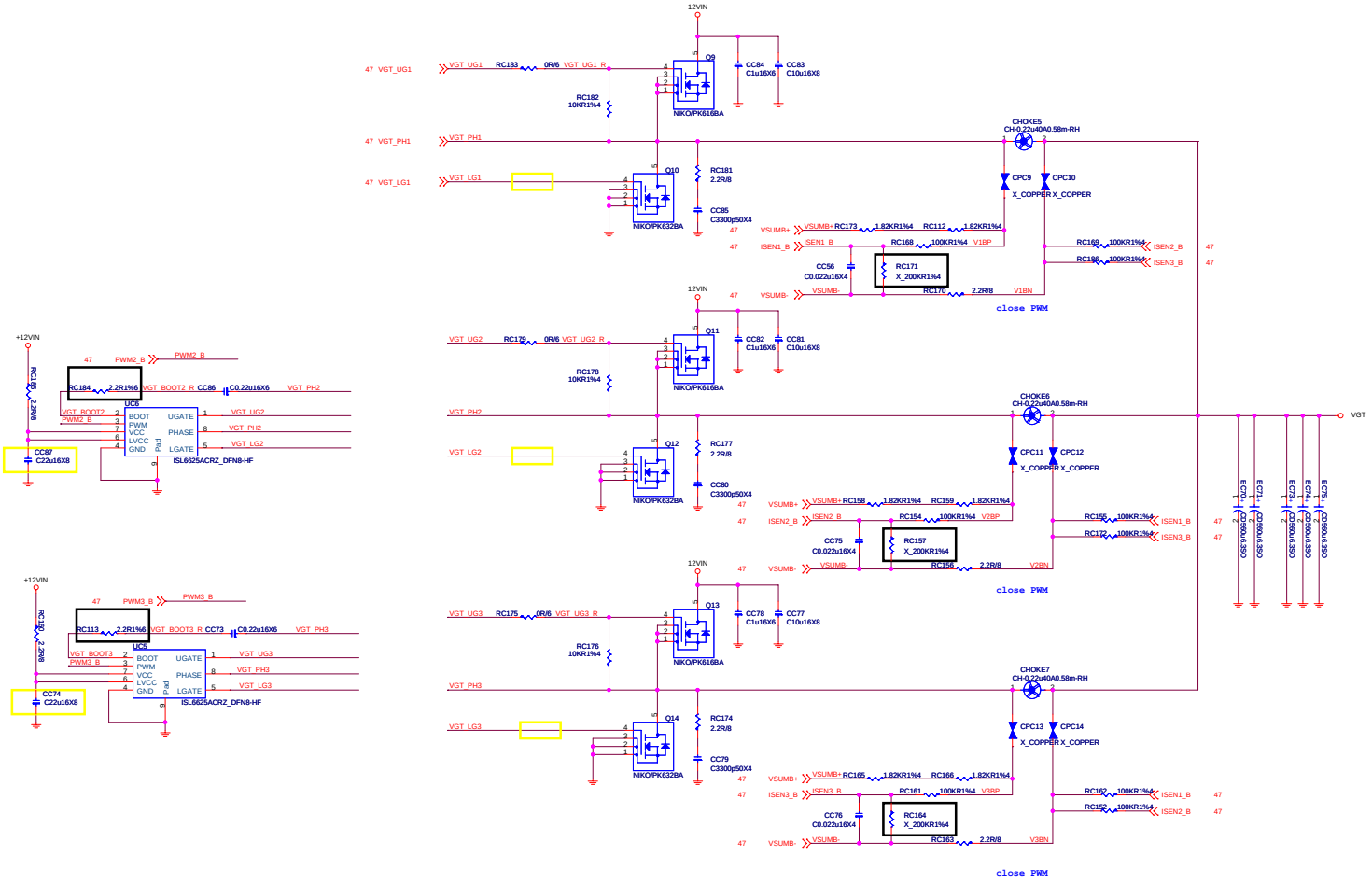

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Size: Custom	Document Description: VGT MOS-PHASE 1~3	Rev: 1.1
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VCCIO

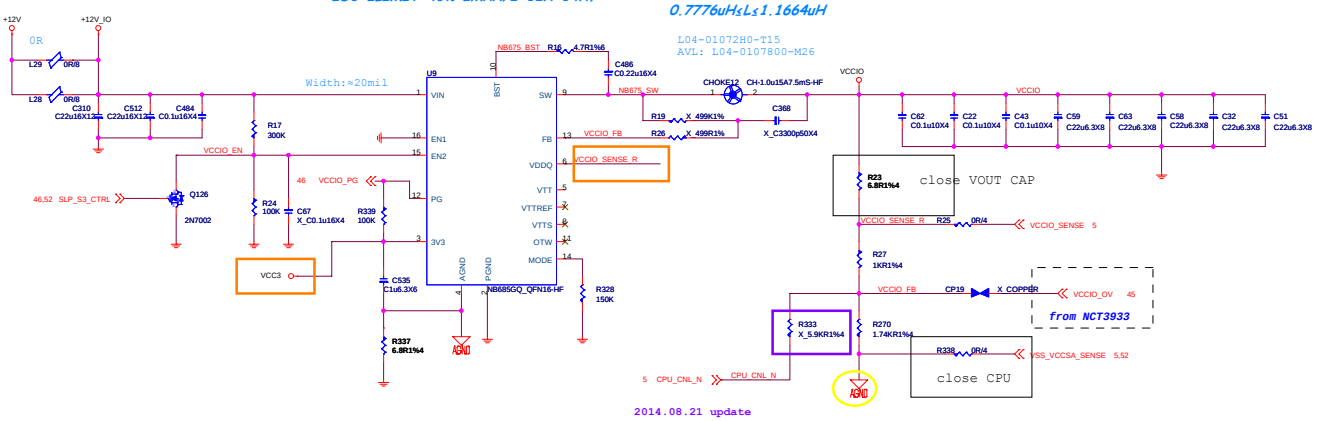
0.95V; 5.5A

(H110 VCCIO=VCCSA)

IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.

0.7776uH≤L≤1.1664uH

L04-01072H0-T15
AVL: L04-0107800-M26

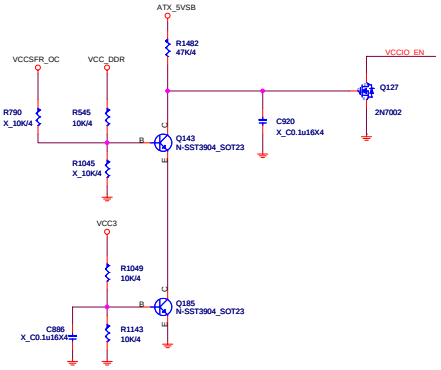


2014.08.21 update
RSVD for CRB

CPU_CNL_N come from CPU PROC_SELECT#

SLP_S3# assertion to VCCIO VR disabled ≦1uS.

SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off. <500ms



MICRO-STAR INT'L CO.,LTD

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Custom	CPU PWR_VCCIO	1.1

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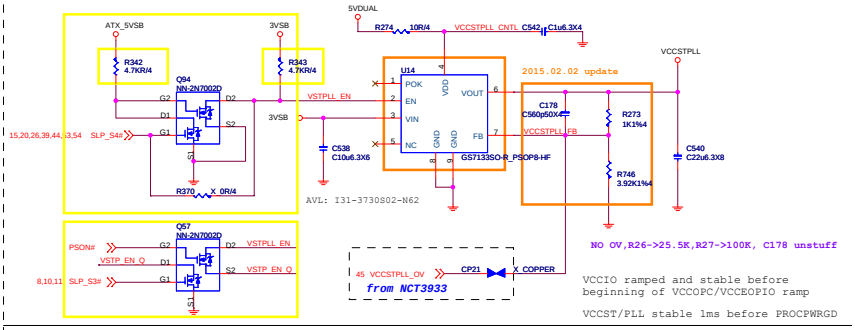
VCCSTPLL

for Gaming3/5, Classic, ECO and H110

1.0V; 250mA(0.12A+0.13A)

For Cost down VCCST&VCCPLL merge

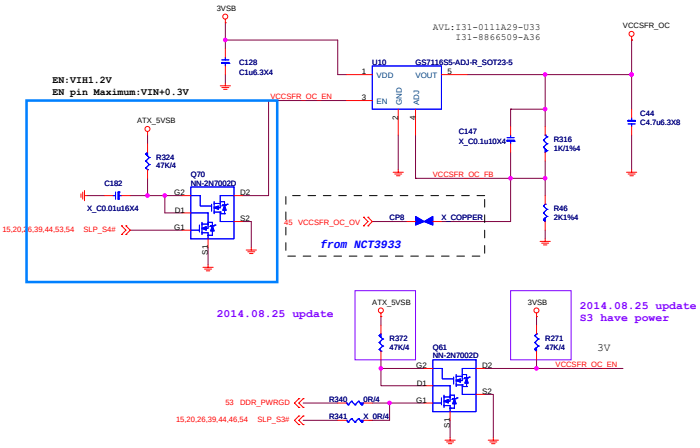


To solve CPU hotplug and lake current

VCCPLL OC

1.2V; 110mA(0.1A)

2014.08.21 update



2014.08.25 update

2014.08.25 update
S3 have power

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SA Power:1.05V,12.3A(11A)

*OCP =12.3A*1.4=17.22A*
*Rocs(R15)=OCP*Rdson(Low side)3.4mohm]/10uA*
=17.22(3.4)mohm/10uA*
=5.854Kohm

Rocs:5.76K,OCP:
D03-4C05N03-O05 : 16.94A
D03-632BA0C-N03 : 17.45A
use UBIQ MOS need Check

Rdson(low)10V
D03-4C05N03-O05 : 3.4mohm
D03-632BA0C-N03 : 3.3mohm
D03-3056M00-U47 : 4.2mohm

RT8125C R413->10R
up1540 R413->2.2R

2014.08.25 update

EN:VIH2.4V
EN pin Maximum:6.5V

RT8125C C5->1000pf;R415->768R
up1540 C5&R415 NC

RT8125C C39->1000pF.
For up1540 :C39->5.36K, OCP 15.76A
5K is min

RT8125C R194->stuff;R179->NC
up1540 R194->NC;R179->stuff

RT8125C R426->3.24K
up1540 R426->3.16K

FB:0.8V

RT8125C C100&R225&C85 ->NC
up1540 C100->NC;R225->36K;C85->10nf

2014.08.21 update

Pull up by layout&Check level

EN:VIH2.4V
EN pin Maximum:6.5V

SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.

SLP_S3# assertion to VR disabled
max:1us

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 18* 0.2825
= 5.086A

Footprint:CHK_D2_10_5X7_2_H9_6

1.05V,12.3A

OCPSET:min 5Kohm

RT8125C R417->5.76K
up1540 R417->NC

Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.5914uH (K = 30%)

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DDR4_1.2V 2.5A+9.5A+1.2A+0.1A=13.3A

2.5A FOR CPU

9.5A FOR 4DIMM

1.2A FOR DDR VTT

0.1A FOR VccPLL(OC)

OCP =13.2A*1.5=19.8A

Rocs(R95)=OCP*Rdson[(Low side)/2]/10uA

=19.8A*(4.6/2)mohm/10uA

=4.95Kohm≦5K

Rocpset:5.1K

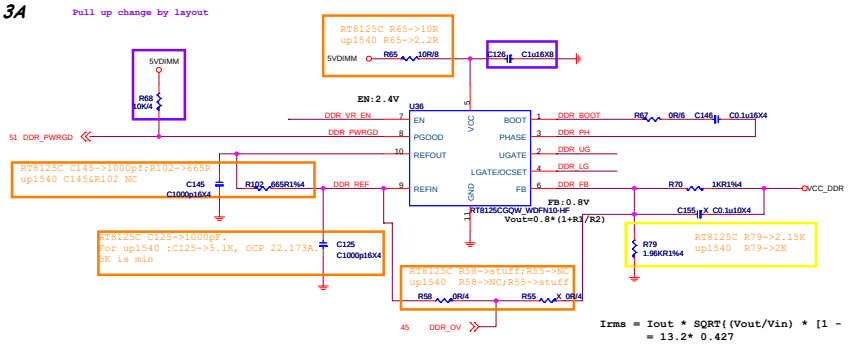
OCP=Rocset*Rdson[(Low side)/2]/10uA

=5.1K*(5/2)mohm/10uA

=22.173A

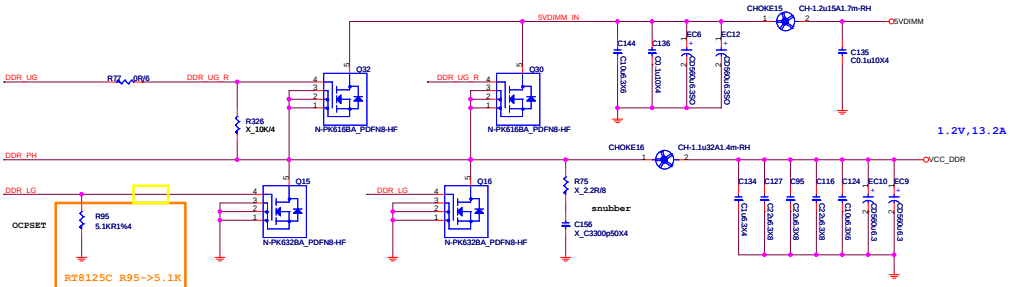
use UBIQ MOS need Check

Pull up change by layout

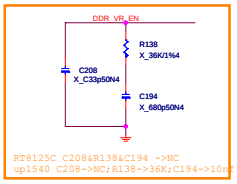


Irms = Iout * SQRT{(Vout/Vin) * [1 - (Vout/Vin)]}
= 13.2* 0.427
= 5.636A

(OS-CON CAP)



1.2V,13.2A



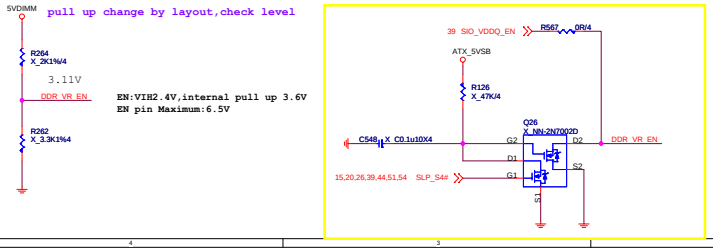
RT8125C R95->5.1K
up1540 R95->NC

DatasheetぞA項衡

Lmin = ((Vin - 1.2V)/(Fsw * k * Iout_max)) * (Vout/Vin)

= 0.7677uH (K = 30%)

項眩 CAP ESR項衡,0.2432uH≦L≦1.2897uH



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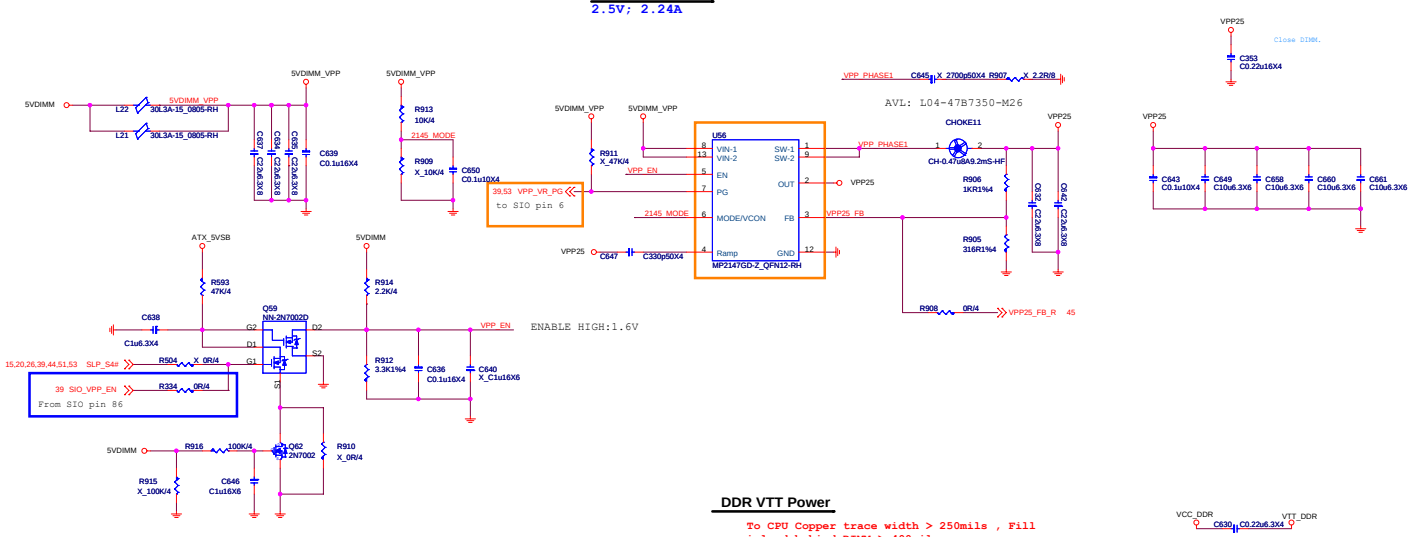
4DIMM :2.24A FOR DDR VPP2.5V

VPP25 Power

2.5V; 2.24A

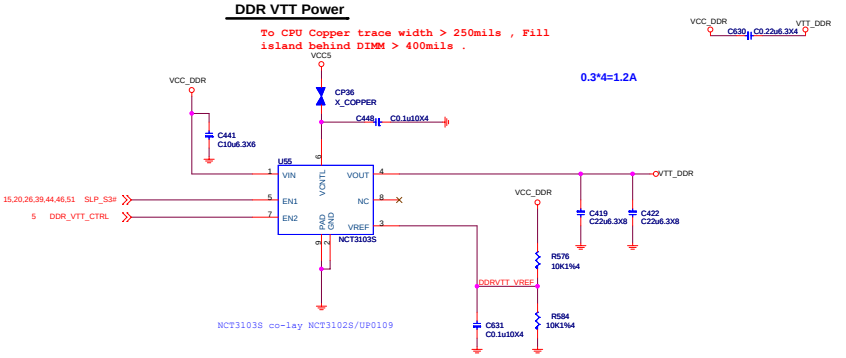


To make sure VPP EN after 5VDIMM stable

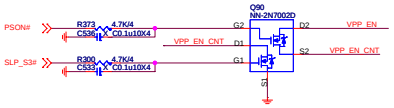
DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

0.3*4=1.2A



IF PCH & DDR power share with the same UP7501, add circuit to keep DDR power OFF when G3 to S5



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PCH_1VSB

1.0V; 11A (11.334A)

6.54+0.7+0.132*6+0.154*15+0.054+0.132*6+0.102+0.044=11.334A

OCP = 11.334*1.5=17.001A

Rocset = 1.5 * Imax * Rdson(low) / Iocset
= 1.5 * 11.334 * 4.6mohm / 10uA
= 7.821K

Rdson(low)4.5V

D03-4C05N03-O05 : 5 mohm
D03-632BA0C-N03 : 4.6mohm
D03-3056M00-U47 : 6.2mohm

Rocs:7.87K,OCP:
D03-4C05N03-O05 : 15.74A
D03-632BA0C-N03 : 17.1A Default
use UBIQ MOS need Check

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 10.664 * 0.4
= 4.2656A < 5000mA

L04-47B7730-T15 for OC, Gaming 10, 9, 7, 5
L04-12A7321-L65 for Gaming 3, SLI, ECO
L04-12A7721-T15 for cost down

CHOKE8 CH-1.2u15A1.7m-RH too Big

MAX:10.664A

L04-01072H0-T15
AVL: L04-0107800-M26

CHOKE9 CH-1.0u15A7.5mS-HF

U28 RT8125CGQW_WDFN10-HF

2014.08.21 update

2014.08.25:Change 1u/0603

RT8125C R65->10R
up1540 R65->2.2R

RT8125C C236->100upF;R204->665R
up1540 C236&R204 NC

RT8125C C180->1000pF.
For up1540 :C180->7.87K, OCP 15.74A.
5K is min

RT8125C R177->7.87K
up1540 R177->NC

RT8125C R287->stuff;R188->NC
up1540 R287->NC;R188->stuff

RT8125C C170&R192&C142 ->NC
up1540 C170->NC;R192->36K;C142->3.3nF

0728: add

0728: Change net name

Vout = Vref * (1 + R821/R822)
= 0.8 * (1 + 1K/3.92K)
= 0.8 * 1.2551
= 1.004V

Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.8335uH (K = 30%)

PLACE UNDER THE PCH

0302 : Stuff R when NO PCH_1P8 & V_OPC_1P8

PCH_1P8

Remove circuit

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Size: Custom	Document Description: PCH Core Power-RT8125C
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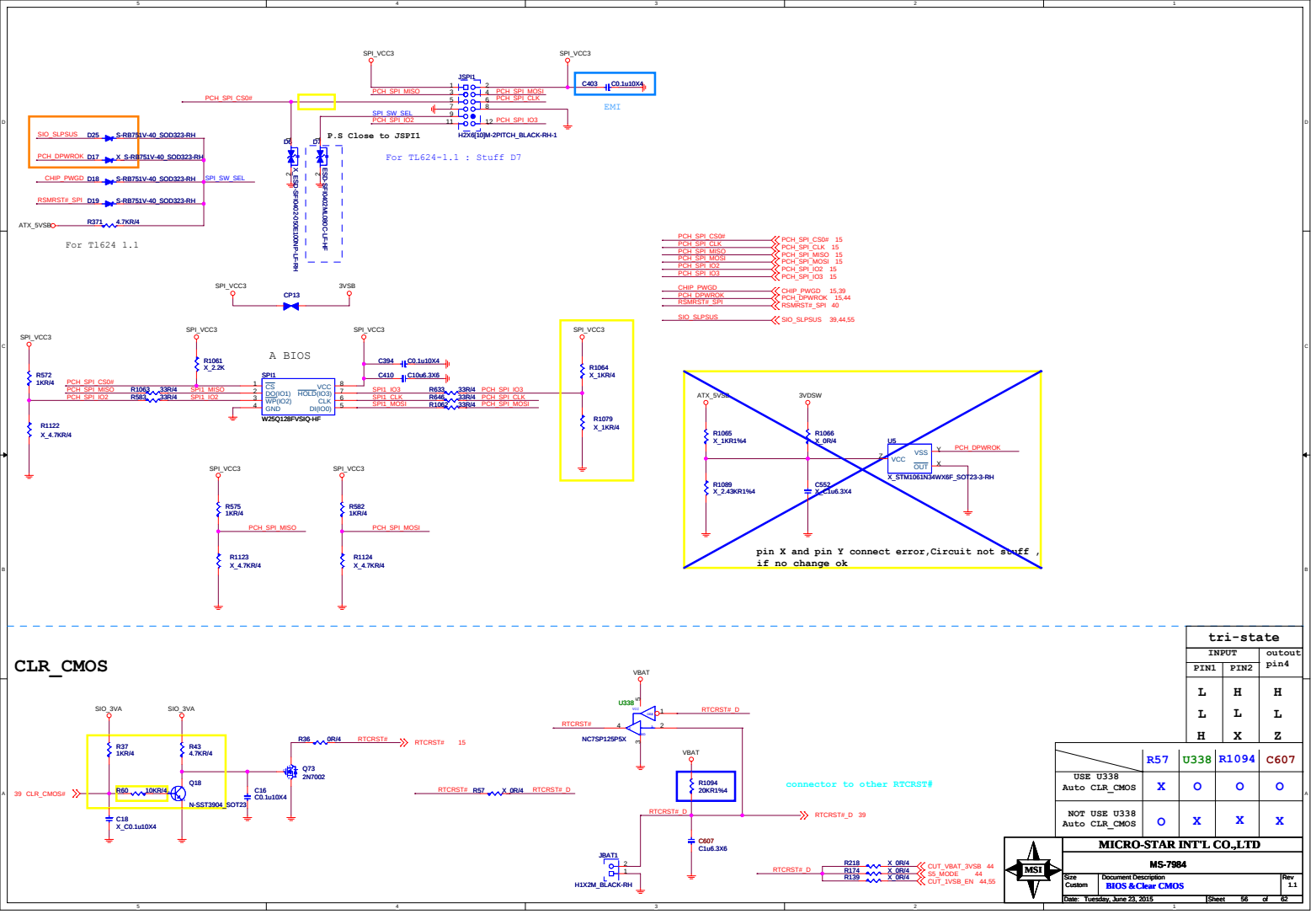

CLR_CMOS

tri-state		
INPUT		outout
PIN1	PIN2	pin4
L	H	H
L	L	L
H	X	Z

	R57	U338	R1094	C607
USE U338 Auto CLR_CMOS	X	O	O	O
NOT USE U338 Auto CLR_CMOS	O	X	X	X

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PCB

P/N:PD0-0798411-G37
PD0-0798411-E48

PCB

7978_1.0

CPU Socket

CPU_H1

CPU_H1

SBC Label

SBC_LA1

Label

SBC

SBC LABEL

Battery

BAT1_X1

BAT-BCR2032P-RH

HDMI Label

HDMI_LA1

Label

HDMI

HDMI LABEL

Audio Small Cover

COVER1

Audio Cover

E21-7978010-RH

BIOS Label

AMI_LA1

AMI_BIOS LABLE

BIOS_LABLE

LAN Cover

COVER2

Audio Cover

E21-7976010-RH

Marketing Label

Z170_LA1

Label

Z97-Gaming3

MKT-LABEL

USB3.1 Label

USB31_LA1

Label

HDMI

U3.1 LABEL

PCH Heatsink

HS_PCH1

MEC1

MEC2

HS-0407560-RH

MOS1 Heatsink

HS_MOS1

MEC1

MEC2

HS-0503400-RH

MOS2 Heatsink

HS_MOS2

MEC1

MEC2

HS-0503390-RH

Gaming Network Manager

NET_LA1

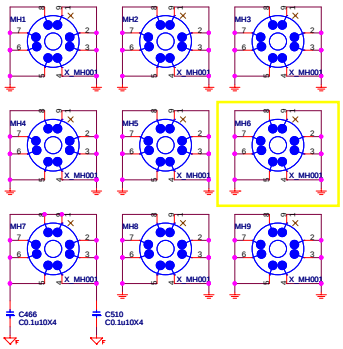
Label

Z97-Gaming3

Y02-MU00170-CFO

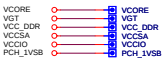
for GAMING Pro sku+Krait sku

Mounting Holes

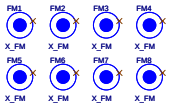


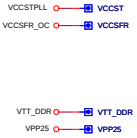
Simulation

Test point



Optical Fiducial Marks-120





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