H81H3-AD

Rev:V1.0

ECS CONFIDENTIAL

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REVISION HISTORY:

Rev	Date	Notes
A	2013/01/23	Modified Q87H3-AM to Sargo project.
B	2013/05/10	Swap BIOS_WP and CMOS header, combine bottom side of GND plane VGA and PS2.
C	2013/05/30	Cancel sparate line of Vcore in GND layer.
V1.0	2013/06/07	modified for MP.

Title: Cover Page			
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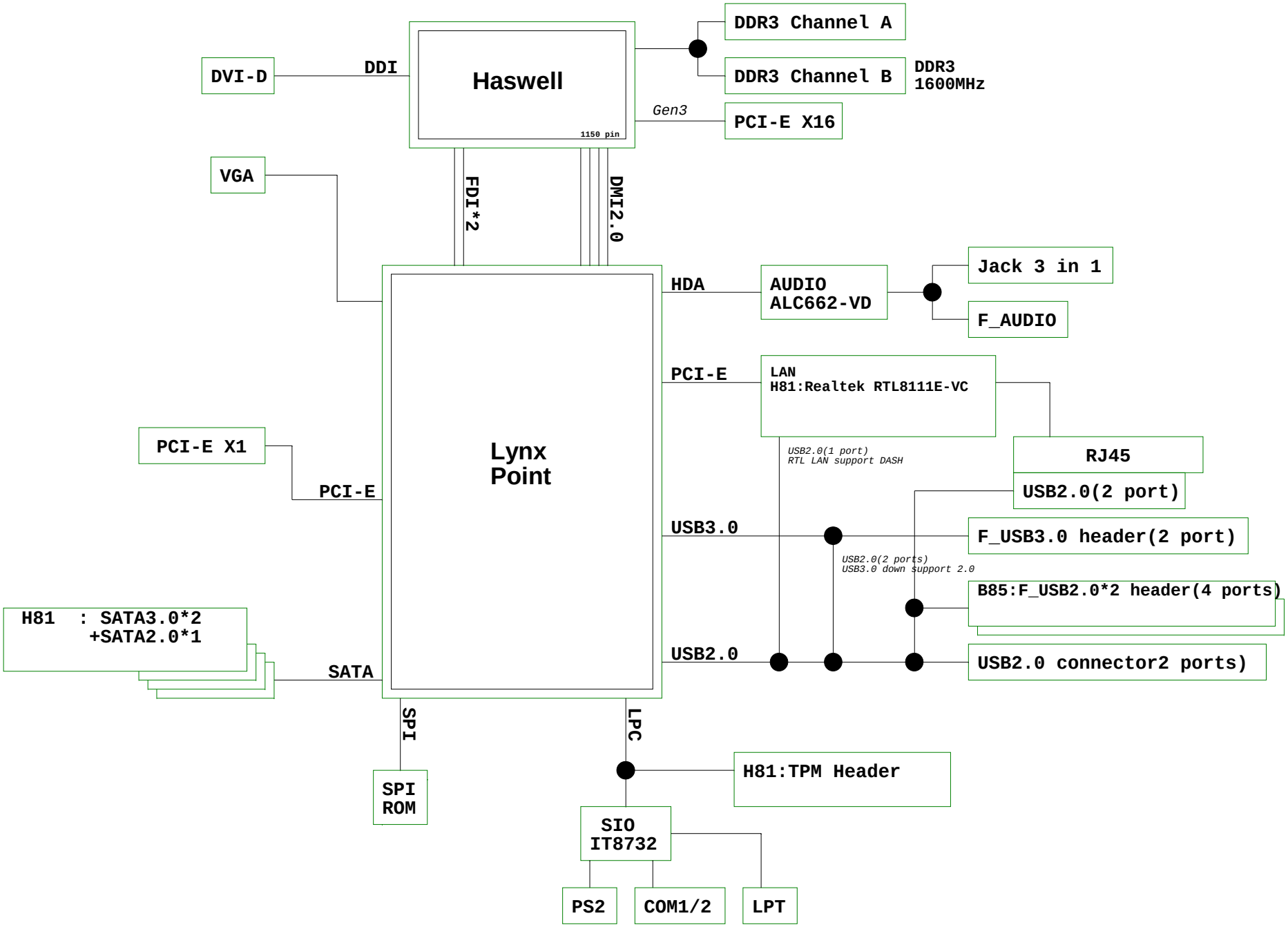

Title	Block Diagram	
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PCH-GPIO function

Pin Name	Power Well	Usage	Default Status	
GPIO13	3VSB	LPC_PME	GPI	
GPIO40	3VSB	USB_5VDUAL control	Native	S0/S3/S4/S5:High
GPIO72	3VSB	USB_5VDUAL control (reserve)	Native	S0/S3/S4/S5:High
GPIO45	3VSB	BIOS WP	Native	OUTPUT Low/BIOS WP, High/Normal
GPIO57	3VSB	BIOS WP	GPI	INPUT Low/Normal, High/BIOS WP
GPIO46	3VSB	WLAN_DIS_L	Native	
GPIO61	3VSB	LPCPD_L	Native	INPUT Low/Active
GPIO27	ATX_3VSB	ILAN_WAKE_L	GPI	INPUT Low/Active
GPIO1	VCC3	OBR	GPI	INPUT Low/Active
GPIO6	VCC3	Thermal_SD	GPI	INPUT Low/Active
GPIO68	VCC3	TP_VGA	GPI	INPUT Low/On VGA output
GPIO23	VCC3	HDPANEL_DETECT	Native	INPUT Low/Active
GPIO15	3VSB	PEX16_RST	GPO	S0:High S3/S4/S5:Low
DL,BIOS must be pro				
GPIO73	3VSB	case open(reserve)	PCIECLKRQ0#	
GPIO24	3VSB	ME_Disable	GPO	OUTPUT Low/Normal, High/ME disable
GPIO19	VCC3	BOOT device detect	GPI	
GPIO51	VCC3	BOOT device detect	GPO	

Interrupt mapping

Function	INT# port	PCIe*1 port	Device
LAN	INTC#	port 3	RTL8111E-VC
PCIEX1	INTD#	port 4	LPT integrate
SATA	INTB#	NA	LPT integrate

SIO-GPIO function

Pin Name	Power Well	Usage	Default Status	
GP16	VCC3	Beep(reserve)	CIRRX2	
GP36	3VSB	Thermal_SD	FAN_CTL3	OUTPUT Low/Thermal SD, High/Normal
GP35	3VSB	LED0	FAN_TAC4	
GP37	3VSB	LED1	FAN_TAC3	
GP70	VCC3	TPM Onboard detect	GPIO	INPUT Low/TMP Header, High/TMP CHIP
GP71	VCC3	BOM detect	GPIO	
GP73	VCC3	BOM detect	GPIO	
GP74	VCC3	BOM detect	GPIO	
GP76	3VSB	Changer enable	GPIO	S0/S3/S4/S5:High
GP46	3VSB	Acer Header	GPIO	
GP47	3VSB	Acer Header	GPIO	
GP40	3VSB	5VDUAL Switch	3VSBSW	
RI1#	3VSB	LAN on MB wake up	RI1	INPUT Low/Active

BIOS must be pro to Native 3VSBSW

Title	GPIO Function & INT# Mapping		
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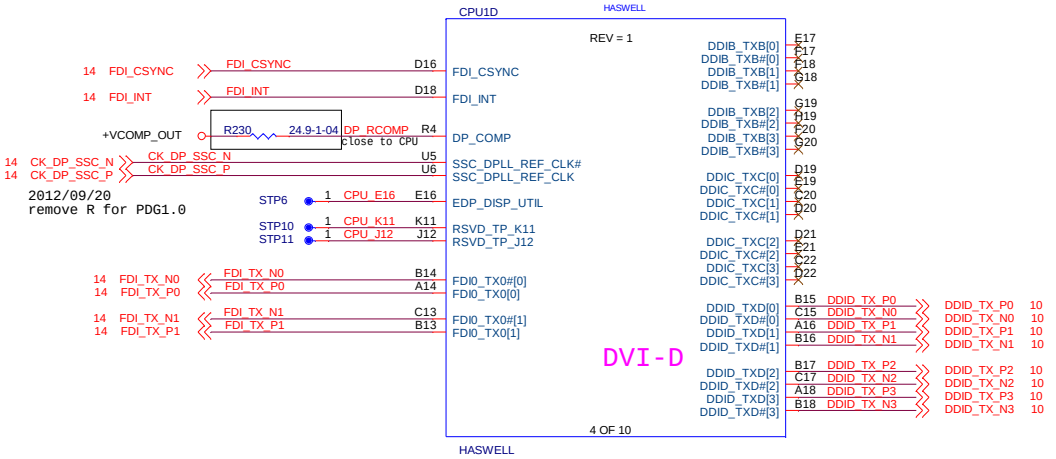
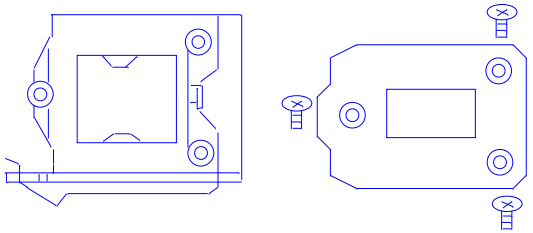


2012/09/20
remove R for PDG1.0

CPU1
CPU_SUBASSY_STEEL



CPU steel (T/U pahse)
PN:20-800-005711 CPU SOCKET STEEL SUBASSY.STEEL....LGA 1155/1156P.W/BACK PLATE,CAP.LOTES

CPU socket (SMD phase)
PN:11-018-115128 SOCKET.CPU..LGA 1150P SMD..15u...BLACK.ACA-ZIF-138-P01...HF.LEAD-FREE.LOTES

Title	CPU-PEG/DMI/FDI/DDI		
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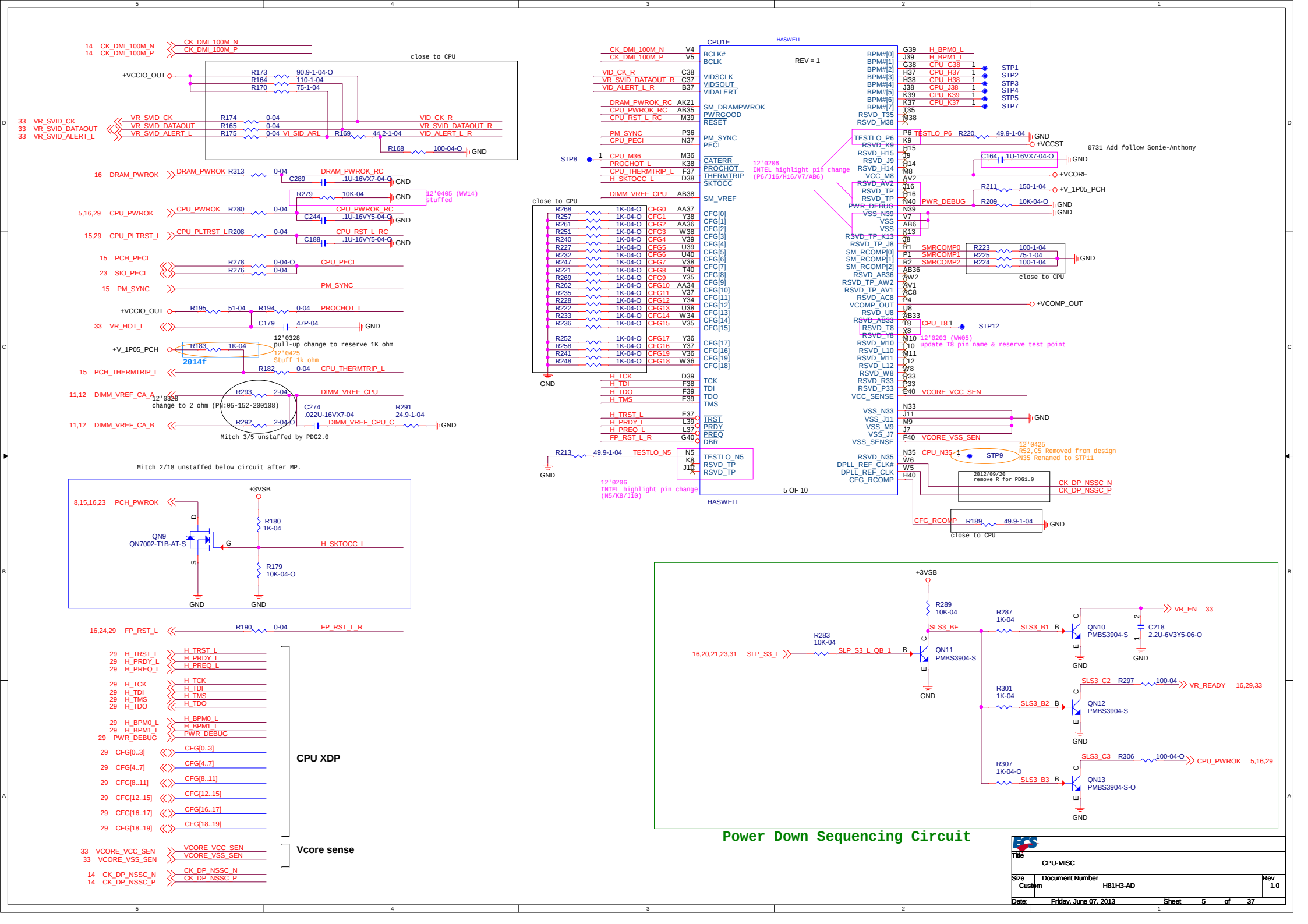
CPU1E
HASWELL
REV = 1
5 OF 10
close to CPU
Mitch 2/18 unstaffed below circuit after MP.
Mitch 3/5 unstaffed by PDG2.0
CPU XDP
Vcore sense
Power Down Sequencing Circuit
0731 Add follow Sonie-Anthony
Title
CPU-MISC
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**Attention

**Attention

DDR3 CH.A

DDR3 CH.B

CPU1A

CPU1B

HASWELL

REV = 1

1 OF 10

2 OF 10

R446 0-04

C366 .1U-16VX7-04-O

close to DIMM slot

C257 .022U-16VX7-04

C252 .022U-16VX7-04

R286 24.9-1-04

R285 24.9-1-04

Title	CPU-DDR3
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12'0425
SC12 change to 0.1UF
SC14 change to 4.7UF

+VCCST

C193 .1U-16VX7-04

C194 4.7U-25VX5-08

GND GND

R234 0-04-O

VCCIO_OUT

CPU_AB8

2014b

R229 0-04

2014a

+VCCIO_PCH

R304 0-04

+V_1P05_PCH

12'0425
Added new caps for VCCIO_OUT

+V_1P05_PCH +VCCIO_OUT

R201 0-04-O

R199 0-04 VCCIO_OUT

C182 4.7U-6.3VX6S-O

GND

09/04 reserve for power quality

+VCORE +VCORE

CPU1F HASWELL

REV = 1

P8	VCC_P8	VCC_C31	C31
L40	VCCIO_OUT	VCC_C33	C33
AB8	VCCIO2PCH	VCC_L16	L16
		VCC_L15	L15
		VCC_J35	J35
L31	VCC_L31	VCC_H33	H33
L18	VCC_L18	VCC_H35	H35
L17	VCC_L17	VCC_J21	J21
J33	VCC_J33	VCC_J22	J22
A24	VCC_A24	VCC_J23	J23
A25	VCC_A25	VCC_J24	J24
A26	VCC_A26	VCC_J25	J25
A27	VCC_A27	VCC_J26	J26
A28	VCC_A28	VCC_J27	J27
A29	VCC_A29	VCC_J28	J28
A30	VCC_A30	VCC_J29	J29
G33	VCC_G33	VCC_J30	J30
B25	VCC_B25	VCC_J32	J32
B27	VCC_B27	VCC_J34	J34
B29	VCC_B29	VCC_K19	K19
B31	VCC_B31	VCC_K21	K21
J31	VCC_J31	VCC_K23	K23
B33	VCC_B33	VCC_K25	K25
G31	VCC_G31	VCC_K27	K27
B35	VCC_B35	VCC_K29	K29
C24	VCC_C24	VCC_K31	K31
C25	VCC_C25	VCC_M13	M13
C26	VCC_C26	VCC_K33	K33
C27	VCC_C27	VCC_K35	K35
C28	VCC_C28	VCC_L19	L19
C29	VCC_C29	VCC_L20	L20
C30	VCC_C30	VCC_L21	L21
C32	VCC_C32	VCC_L22	L22
C34	VCC_C34	VCC_L23	L23
C35	VCC_C35	VCC_L24	L24
D25	VCC_D25	VCC_L25	L25
D27	VCC_D27	VCC_L26	L26
D29	VCC_D29	VCC_L27	L27
D31	VCC_D31	VCC_L28	L28
E33	VCC_E33	VCC_L29	L29
D33	VCC_D33	VCC_L30	L30
E31	VCC_E31	VCC_L32	L32
D35	VCC_D35	VCC_L33	L33
E24	VCC_E24	VCC_M17	M17
E25	VCC_E25	VCC_M15	M15
E26	VCC_E26	VCC_M19	M19
E27	VCC_E27	VCC_M21	M21
E28	VCC_E28	VCC_M23	M23
E29	VCC_E29	VCC_M25	M25
E30	VCC_E30	VCC_M27	M27
E32	VCC_E32	VCC_M29	M29
E34	VCC_E34	VCC_M33	M33
F23	VCC_F23		
F25	VCC_F25	VDDQ_AJ12	AJ12
F27	VCC_F27	VDDQ_AJ13	AJ13
F29	VCC_F29	VDDQ_AJ15	AJ15
F31	VCC_F31	VDDQ_AJ17	AJ17
E35	VCC_E35	VDDQ_AJ20	AJ20
F33	VCC_F33	VDDQ_AJ21	AJ21
F35	VCC_F35	VDDQ_AJ24	AJ24
G22	VCC_G22	VDDQ_AJ25	AJ25
G23	VCC_G23	VDDQ_AJ28	AJ28
G24	VCC_G24	VDDQ_AJ29	AJ29
G25	VCC_G25	VDDQ_AJ9	AJ9
G26	VCC_G26	VDDQ_AT17	AT17
G27	VCC_G27	VDDQ_AT22	AT22
G28	VCC_G28	VDDQ_AU15	AU15
G29	VCC_G29	VDDQ_AU20	AU20
G30	VCC_G30	VDDQ_AU24	AU24
G32	VCC_G32	VDDQ_AV10	AV10
G34	VCC_G34	VDDQ_AV11	AV11
G35	VCC_G35	VDDQ_AV13	AV13
H23	VCC_H23	VDDQ_AV18	AV18
H25	VCC_H25	VDDQ_AV23	AV23
H27	VCC_H27	VDDQ_AV8	AV8
H29	VCC_H29	VDDQ_AW16	AW16
H31	VCC_H31	VDDQ_AY12	AY12
L34	VCC_L34	VDDQ_AY14	AY14
		VDDQ_AY9	AY9

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HASWELL

+VDIMM

+VCORE

C247 C161 C160 C246 C239 C226
22U-6V3X5-08

C237 C208 C207 C225 C206 C238
22U-6V3X5-08

C248 C240 C227 C162 C163 C224
22U-6V3X5-08-O

GND

12'0405
stuff 18pcs

07/19 change to 15pcs-Anthony

+VDIMM

C264 C263 C262 C261 C260
22U-6V3X5-08-O

C259 C265 C266 C267
22U-6V3X5-08

12'1217
Intel spec. cost down VDDQ cap

GND

place caps in CPU socket cavity

+VCORE

C205 C223 C236 C209
22U-6V3X5-08-O

GND

12'0405
unstuff

place caps at top CPU socket edge

+VDIMM

C417 C387 C388 C419
22U-6V3X5-08-O

GND

place caps between CHA/CHB DIMM

Title	CPU-POWER	
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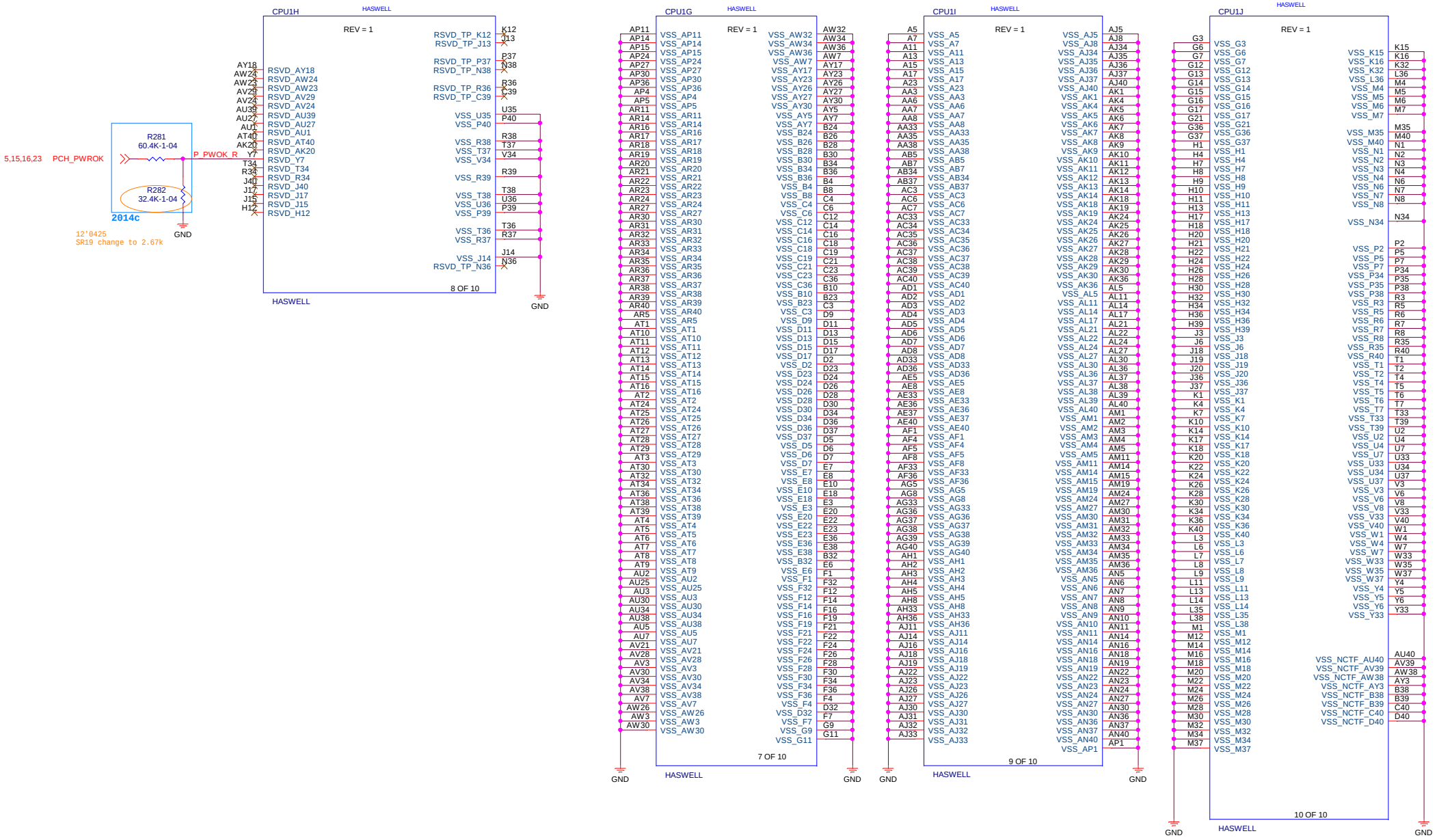

Title	CPU-GND	
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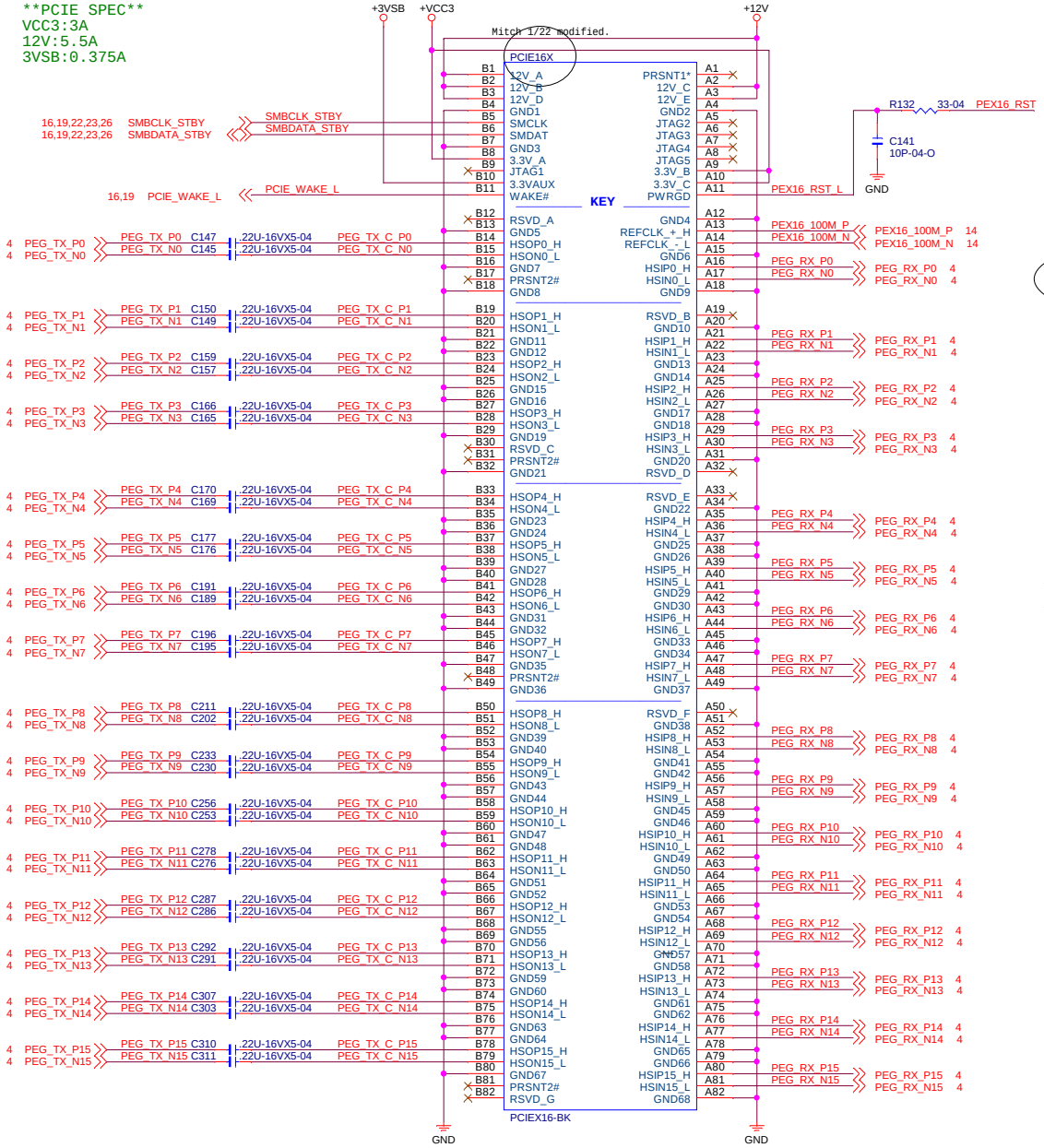
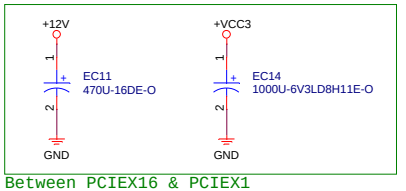
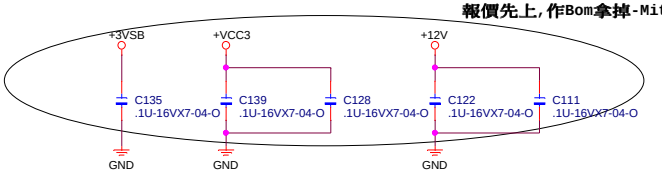
PCIE SPEC
VCC3:3A
12V:5.5A
3VSB:0.375A

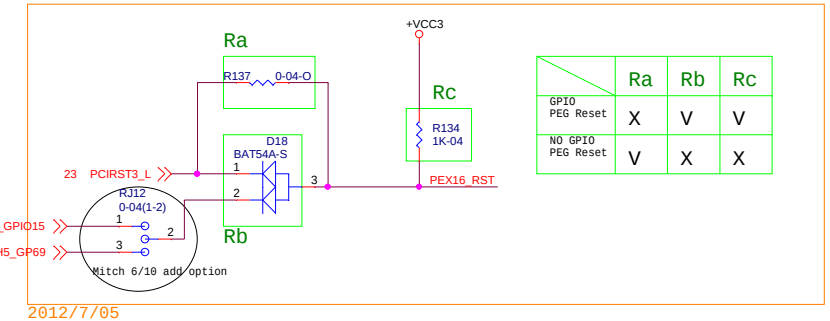




Between PCIEX16 & PCIEX1

報價先上,作Bom拿掉-Mitch





	Ra	Rb	Rc
GPIO PEG Reset	X	V	V
NO GPIO PEG Reset	V	X	X

2012/7/05
PCIe Gen3 slot reset circuit update .

Title	PCIE*16		
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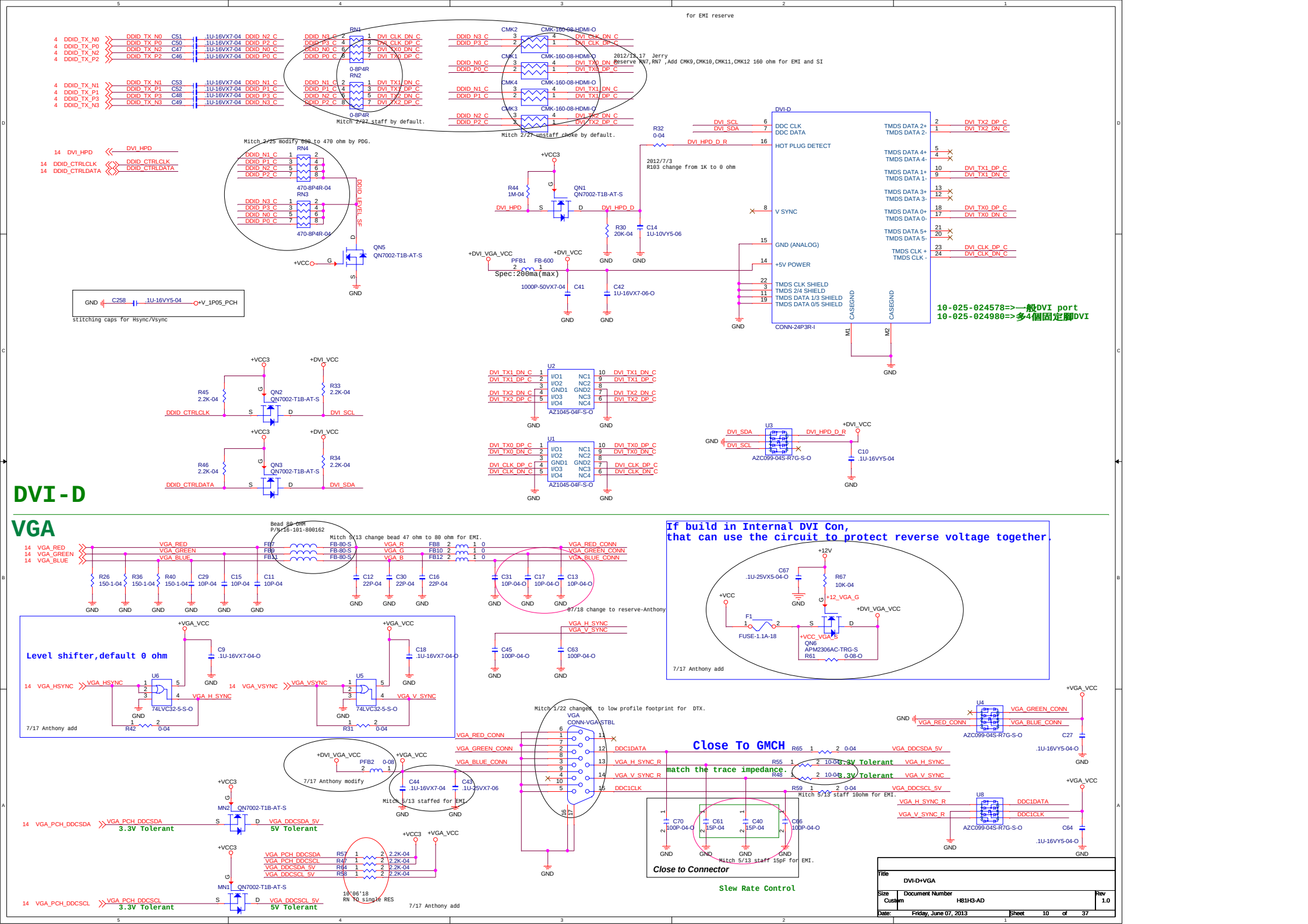
DVI-D

VGA



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CHANNEL A DIMMs

2013/1/8 by nick change remove DIMM

CHANNEL B DIMMs

Mitch 2/26 swap DIMM number.

close to CHA-DIMM0

close to CHB-DIMM0

close to CHA-DIMM2

close to CHB-DIMM1

stiching caps for CMD,CTL,ADDR

place between CHA&CHB
Don't punch VIAS

CH.A	SA1	SA0
DIMM0	L	L
DIMM1	L	H

CH.B	SA1	SA0
DIMM0	H	L
DIMM1	H	H

Title	DDR3-CHA
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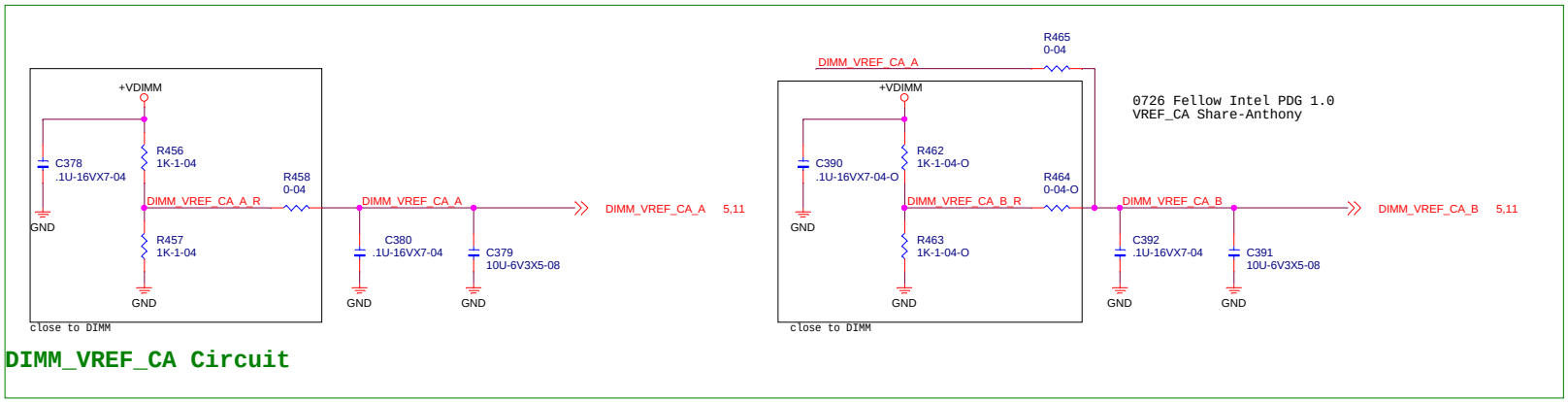
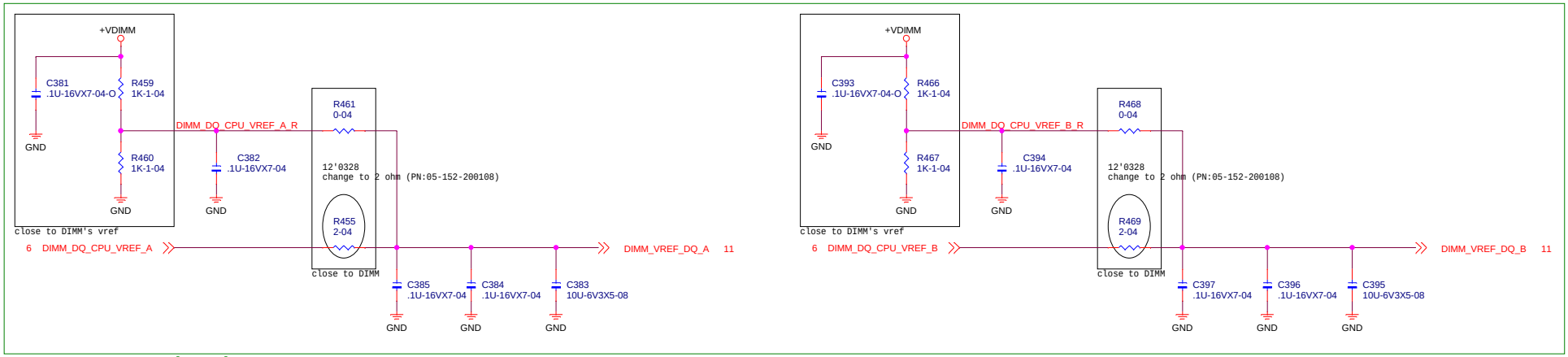


DIMM_VREF_CA Circuit



DIMM_VREF_DQ Circuit

Title: DDR3-Vref		
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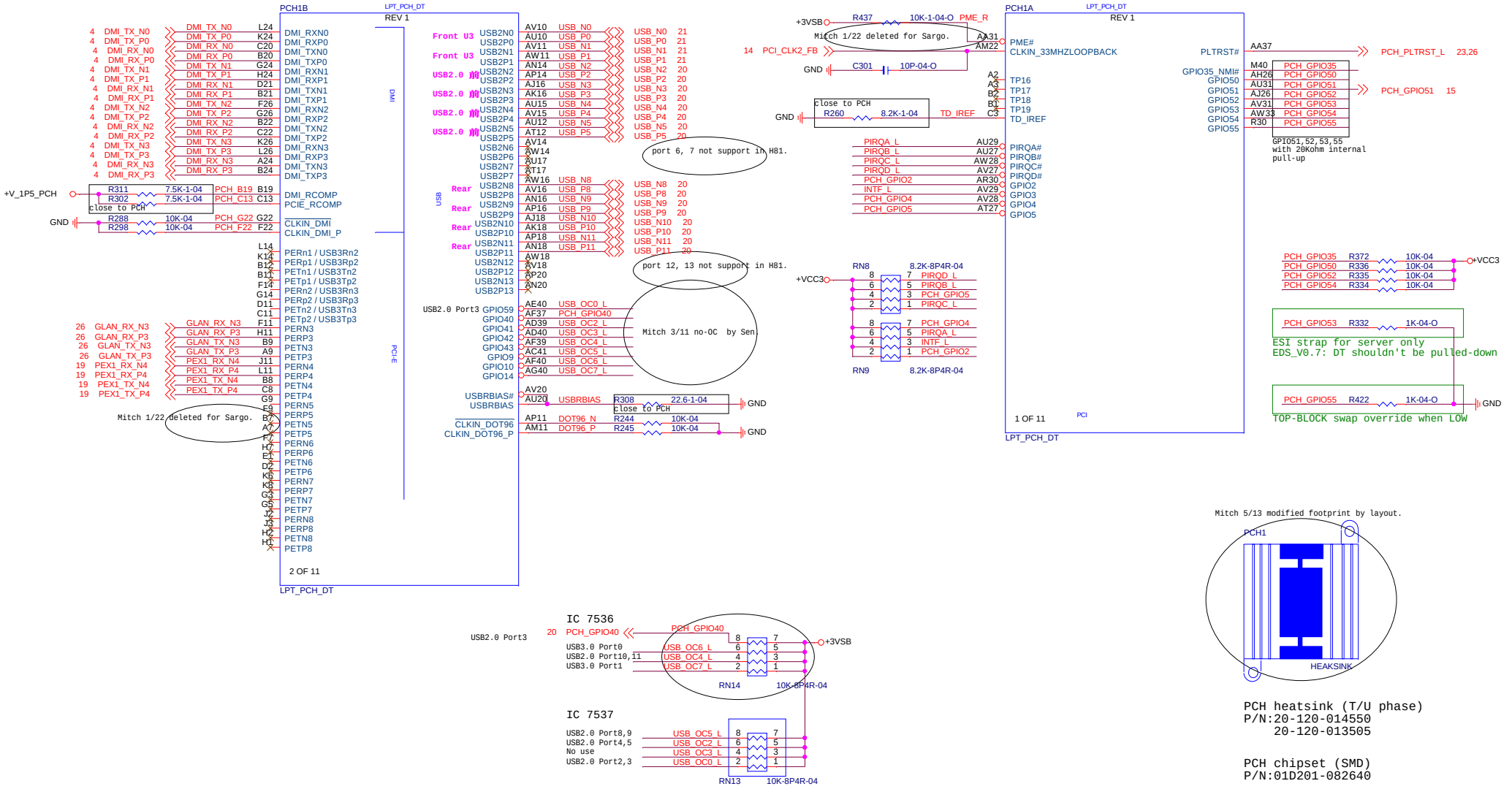
PCH1B
LPT_PCH_DT
REV 1
DMI_TX_N0 L24
DMI_TX_P0 K24
DMI_RX_N0 C20
DMI_RX_P0 B20
DMI_TX_N1 G24
DMI_TX_P1 H24
DMI_RX_N1 D21
DMI_RX_P1 B21
DMI_TX_N2 F26
DMI_TX_P2 G26
DMI_RX_N2 B22
DMI_RX_P2 C22
DMI_TX_N3 K26
DMI_TX_P3 L26
DMI_RX_N3 A24
DMI_RX_P3 B24
DMI_RXN0
DMI_RXP0
DMI_TXN0
DMI_TXP0
DMI_RXN1
DMI_RXP1
DMI_TXN1
DMI_TXP1
DMI_RXN2
DMI_RXP2
DMI_TXN2
DMI_TXP2
DMI_RXN3
DMI_RXP3
DMI_TXN3
DMI_TXP3
DMI
+V_1P5_PCH
R311 7.5K-1-04 PCH_B19 B19
R302 7.5K-1-04 PCH_C13 C13
close to PCH
GND
R288 10K-04 PCH_G22 G22
R298 10K-04 PCH_F22 F22
DMI_RCOMP
PCIE_RCOMP
CLKIN_DMI
CLKIN_DMI_P
PERn1 / USB3Rn2
PERp1 / USB3Rp2
PETn1 / USB3Tn2
PETp1 / USB3Tp2
PERn2 / USB3Rn3
PERp2 / USB3Rp3
PETn2 / USB3Tn3
PETp2 / USB3Tp3
PERN3
PERP3
PETN3
PETP3
PERN4
PERP4
PETN4
PETP4
PERN5
PERP5
PETN5
PETP5
PERN6
PERP6
PETN6
PETP6
PERN7
PERP7
PETN7
PETP7
PERN8
PERP8
PETN8
PETP8
PCIE
GLAN_RX_N3
GLAN_RX_P3
GLAN_TX_N3
GLAN_TX_P3
PEX1_RX_N4
PEX1_RX_P4
PEX1_TX_N4
PEX1_TX_P4
Mitch 1/22 deleted for Sargo.
2 OF 11
LPT_PCH_DT
USB2.0 前
USB2N0 AV10 USB_N0
USB2P0 AU10 USB_P0
USB2N1 AV11 USB_N1
USB2P1 AW11 USB_P1
USB2N2 AN14 USB_N2
USB2P2 AP14 USB_P2
USB2N3 AJ16 USB_N3
USB2P3 AK16 USB_P3
USB2N4 AU15 USB_N4
USB2P4 AV15 USB_P4
USB2N5 AU12 USB_N5
USB2P5 AT12 USB_P5
USB2N6 AV14
USB2P6 AW14
USB2N7 AU17
USB2P7 AT17
USB2N8 AW16 USB_N8
USB2P8 AV16 USB_P8
USB2N9 AN16 USB_N9
USB2P9 AP16 USB_P9
USB2N10 AJ18 USB_N10
USB2P10 AK18 USB_P10
USB2N11 AP18 USB_N11
USB2P11 AN18 USB_P11
USB2N12 AW18
USB2P12 AV18
USB2N13 AP20
USB2P13 AN20
USB
Front U3
Rear
port 6, 7 not support in H81.
port 12, 13 not support in H81.
USB_N0 21
USB_P0 21
USB_N1 21
USB_P1 21
USB_N2 20
USB_P2 20
USB_N3 20
USB_P3 20
USB_N4 20
USB_P4 20
USB_N5 20
USB_P5 20
USB_N8 20
USB_P8 20
USB_N9 20
USB_P9 20
USB_N10 20
USB_P10 20
USB_N11 20
USB_P11 20
USB2.0 Port3 GPIO59 AE40 USB_OC0_L
GPIO40 AF37 PCH_GPIO40
GPIO41 AD39 USB_OC2_L
GPIO42 AD40 USB_OC3_L
GPIO43 AF39 USB_OC4_L
GPIO9 AC41 USB_OC5_L
GPIO10 AF40 USB_OC6_L
GPIO14 AG40 USB_OC7_L
Mitch 3/11 no-OC by Sen.
USBRBIAS# AV20
USBRBIAS AU20 USBRBIAS
R308 22.6-1-04
close to PCH
CLKIN_DOT96 AP11 DOT96_N
CLKIN_DOT96_P AM11 DOT96_P
R244 10K-04
R245 10K-04
GND
+3VSB
R437 10K-1-04-O PME_R
Mitch 1/22 deleted for Sargo.
14 PCI_CLK2_FB
C301 10P-04-O
close to PCH
R260 8.2K-1-04 TD_IREF
PIRQA_L AU29
PIRQB_L AU27
PIRQC_L AW28
PIRQD_L AV27
PCH_GPIO2 AR30
INTF_L AV29
PCH_GPIO4 AV28
PCH_GPIO5 AT27
RN8 8.2K-8P4R-04
PIRQD_L
PIRQB_L
PCH_GPIO5
PIRQC_L
PCH_GPIO4
PIRQA_L
INTF_L
PCH_GPIO2
RN9 8.2K-8P4R-04
+VCC3
PCH1A
LPT_PCH_DT
REV 1
PME# AA31
CLKIN_33MHZLOOPBACK AM22
TP16 A2
TP17 A3
TP18 B2
TP19 B1
TD_IREF C3
PIRQA#
PIRQB#
PIRQC#
PIRQD#
GPIO2
GPIO3
GPIO4
GPIO5
1 OF 11
PCI
LPT_PCH_DT
PLTRST# AA37
GPIO35_NMI# M40 PCH_GPIO35
GPIO50 AH26 PCH_GPIO50
GPIO51 AU31 PCH_GPIO51
GPIO52 AJ26 PCH_GPIO52
GPIO53 AV31 PCH_GPIO53
GPIO54 AW33 PCH_GPIO54
GPIO55 R30 PCH_GPIO55
PCH_PLTRST_L 23,26
PCH_GPIO51 15
GPIO51,52,53,55
with 20Kohm internal
pull-up
PCH_GPIO35 R372 10K-04 +VCC3
PCH_GPIO50 R336 10K-04
PCH_GPIO52 R335 10K-04
PCH_GPIO54 R334 10K-04
PCH_GPIO53 R332 1K-04-O
ESI strap for server only
EDS_V0.7: DT shouldn't be pulled-down
PCH_GPIO55 R422 1K-04-O GND
TOP-BLOCK swap override when LOW
IC 7536
USB2.0 Port3 20 PCH_GPIO40
PCH_GPIO40
USB3.0 Port0 USB_OC6_L
USB2.0 Port10,11 USB_OC4_L
USB3.0 Port1 USB_OC7_L
+3VSB
RN14 10K-8P4R-04
IC 7537
USB2.0 Port8,9 USB_OC5_L
USB2.0 Port4,5 USB_OC2_L
No use USB_OC3_L
USB2.0 Port2,3 USB_OC0_L
RN13 10K-8P4R-04
0727 If no use usb OC#
need pull up 3VSB by 10KΩ-Anthony
Mitch 5/13 modified footprint by layout.
PCH1
HEAKSINK
PCH heatsink (T/U phase)
P/N:20-120-014550
20-120-013505
PCH chipset (SMD)
P/N:01D201-082640
Title
PCH-DMI/PE/USB2.0
Size
Custom
Document Number
H81H3-AD
Rev
1.0
Date:
Friday, June 07, 2013
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of
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PCH1E
LPT_PCH_DT
REV 1

10 DVI_HPD
DVI_HPD
AJ2 DDPB_HPD
AH5 DDPC_HPD
AJ4 DDPD_HPD
AK6 DDPB_AUXN
AK8 DDPB_AUXP
AG7 DDPC_AUXN
AG6 DDPC_AUXP
AG11 DDPD_AUXN
AG10 DDPD_AUXP

VGA_HSYNC
VGA_VSYNC
VGA_RED
VGA_GREEN
VGA_BLUE
VGA_IRTN
VGA_DDC_DATA
VGA_DDC_CLK
DAC_IREF
close to PCH R272 649-1-04

AH3 PCH_VGA_HSYNC R255 33-04 VGA_HSYNC
AH2 PCH_VGA_VSYNC R254 33-04 VGA_VSYNC
VGA_HSYNC 10
VGA_VSYNC 10
AC2 VGA_RED
AE2 VGA_GREEN
AC3 VGA_BLUE
VGA_RED 10
VGA_GREEN 10
VGA_BLUE 10
AG4 GND
AL3 VGA_PCH_DDCSDA 10
AL2 VGA_PCH_DDCSCL 10
AF5 PCH_AF5
R274 150-1-04
R273 150-1-04
R275 150-1-04
GND GND GND

DDPC_CTRLCLK
DDPC_CTRLDATA
DDPB_CTRLCLK
DDPB_CTRLDATA
DDPD_CTRLCLK
DDPD_CTRLDATA
AN3
AM2
AM1
AJ5
AN4 DDID_CTRLCLK
AN2 DDID_CTRLDATA
DDID_CTRLCLK 10
DDID_CTRLDATA 10

Layout note:
DDC_DATA要長於DDC_CLK約1inch.
越接近越好但不要超過.

5 OF 11
LPT_PCH_DT

VGA_RED C220 5P-04
VGA_GREEN C219 5P-04
VGA_BLUE C221 5P-04
GND
For EMI, close to chipset.

VGA_HSYNC C204 10P-04-O
VGA_VSYNC C203 10P-04-O
GND
2012/07/09
Reserved Cap for Slew rate control

GND C294 .1U-16VY5-04-O +VCC3
stitching caps for PCI_CLK2_FB

GND C241 .1U-16VY5-04-O +V_1P05_PCH
stitching caps for PEX16_100M

Mitch 5/9 modified for SI.
R299 47 to 56 ohm, R284 33 to 47 ohm
R303 43 to 56 ohm.

PCH1G
LPT_PCH_DT
REV 1

25 TCM_33M R295 22-04 PCH_TCM_33M AV5
23 SIO_33M R299 56-1-04 PCH_SIO_33M AV7
13 PCI_CLK2_FB R284 47-04 PCH_PCI_CLK2_FB AU2
GND C283 10P-04-O
GND C275 10P-04-O
GND C249 10P-04-O
CLKOUT_33MHZ0
CLKOUT_33MHZ1
CLKOUT_33MHZ2
AN9 CLKOUT_33MHZ3
AU5 CLKOUT_33MHZ4

23 SIO_48M R303 56-1-04 PCH_SIO_48M AU8
GND C285 10P-04-O
AV8 CLKOUTFLEX0 / GPIO64
AT9 CLKOUTFLEX1 / GPIO65
AV9 CLKOUTFLEX2 / GPIO66
CLKOUTFLEX3 / GPIO67

+V_1P5_PCH R256 7.5K-1-04 close to PCH DIFFCLK_BIASREF R11
DIFFCLK_BIASREF
GND R296 10K-04 REFCLK14IN AR7
REFCLK14IN

CLKIN_GND0
CLKIN_GND0_P
G16 CLKIN_GND_N R290 10K-04 GND
F16 CLKIN_GND_P R294 10K-04 GND
CLKOUT_DMI
CLKOUT_DMI_P
R2 CK_DMI_100M_N CK_DMI_100M_N 5
T2 CK_DMI_100M_P CK_DMI_100M_P 5
CLKOUT_DP
CLKOUT_DP_P
T3 CK_DP_SSC_N CK_DP_SSC_N 4
T5 CK_DP_SSC_P CK_DP_SSC_P 4
CLKOUT_DPNS
CLKOUT_DPNS_P
W2 CK_DP_NSSC_N CK_DP_NSSC_N 5
U2 CK_DP_NSSC_P CK_DP_NSSC_P 5
CLKOUT_ITPXDP
CLKOUT_ITPXDP_P
U6 CK_H_XDP_N CK_H_XDP_N 29
U7 CK_H_XDP_P CK_H_XDP_P 29
CLKOUT_PEG_A
CLKOUT_PEG_A_P
AA3 PEX16_100M_N PEX16_100M_N 9
AA2 PEX16_100M_P PEX16_100M_P 9
CLKOUT_PEG_B
CLKOUT_PEG_B_P
AE6
AE7
CLKOUT_PCIE_N0
CLKOUT_PCIE_P0
AE10
AE11
CLKOUT_PCIE_N1
CLKOUT_PCIE_P1
AC6
AC7
CLKOUT_PCIE_N2
CLKOUT_PCIE_P2
AC11 RLAN_CLKN RLAN_CLKN 26
AC10 RLAN_CLKP RLAN_CLKP 26
CLKOUT_PCIE_N3
CLKOUT_PCIE_P3
W11
W10
CLKOUT_PCIE_N4
CLKOUT_PCIE_P4
Y4
Y2
CLKOUT_PCIE_N5
CLKOUT_PCIE_P5
W7
W6
CLKOUT_PCIE_N6
CLKOUT_PCIE_P6
AA7
AA6
CLKOUT_PCIE_N7
CLKOUT_PCIE_P7
R6 PEX1_100M_N PEX1_100M_N 19
R7 PEX1_100M_P PEX1_100M_P 19

07/18 del mini pcie
Wilson: 1/9 del LAN
Mitch 1/22 deleted for Sargo.

12'0203 (WW05)
N6/N7 pin swap
XTAL_25M_PCH_IN N7 XTAL25_IN
XTAL_25M_PCH_OUT N6 XTAL25_OUT
R249 1M-1
X1 X-25M
C200 27P-04
C199 27P-04
GND

7 OF 11
LPT_PCH_DT

+VCC3 C341 .1U-16VY5-04-O GND
C305 .1U-16VY5-04-O
stitching caps for single end clock

+VCC C487 .1U-16VY5-04-O GND
stitching caps for TCM 33M clock

PCH1F
LPT_PCH_DT
REV 1

21 USB3_RX_N0 F20 USB3RN0
21 USB3_RX_P0 G20 USB3RP0
21 USB3_TX_N0 B18 USB3TN0
21 USB3_TX_P0 C18 USB3TP0
21 USB3_RX_N1 G18 USB3RN1
21 USB3_RX_P1 H18 USB3RP1
21 USB3_TX_N1 B15 USB3TN1
21 USB3_TX_P1 B16 USB3TP1
K20 USB3RN4
L20 USB3RP4
D15 USB3TN4
C15 USB3TP4
L18 USB3RN5
K18 USB3RP5
B14 USB3TN5
A14 USB3TP5
USB3
FDILINK

+VCC3 R341 10K-04 PCH_TACH6 AK28 TACH6 / GPIO70
R347 10K-04 PCH_TACH7 AT34 TACH7 / GPIO71
R345 10K-04-O
GND R348 10K-04-O

Soft strap
GPIO70->USB3_port4
GPIO71->USB3_port5
To determine native function

FDI_RXN0 N1 FDI_TX_N0 FDI_TX_N0 4
FDI_RXP0 N2 FDI_TX_P0 FDI_TX_P0 4
FDI_RXN1 P2 FDI_TX_N1 FDI_TX_N1 4
FDI_RXP1 P3 FDI_TX_P1 FDI_TX_P1 4
FDI_CSYNC L2 FDI_CSYNC FDI_CSYNC 4
FDI_INT L3 FDI_INT FDI_INT 4
FDI_RCOMP K2 K2_PCH R246 7.5K-1-04 close to PCH +V_1P5_PCH

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LPT_PCH_DT

Title	PCH-FDI/DDI/USB3.0/CLK		
Size	Document Number		Rev
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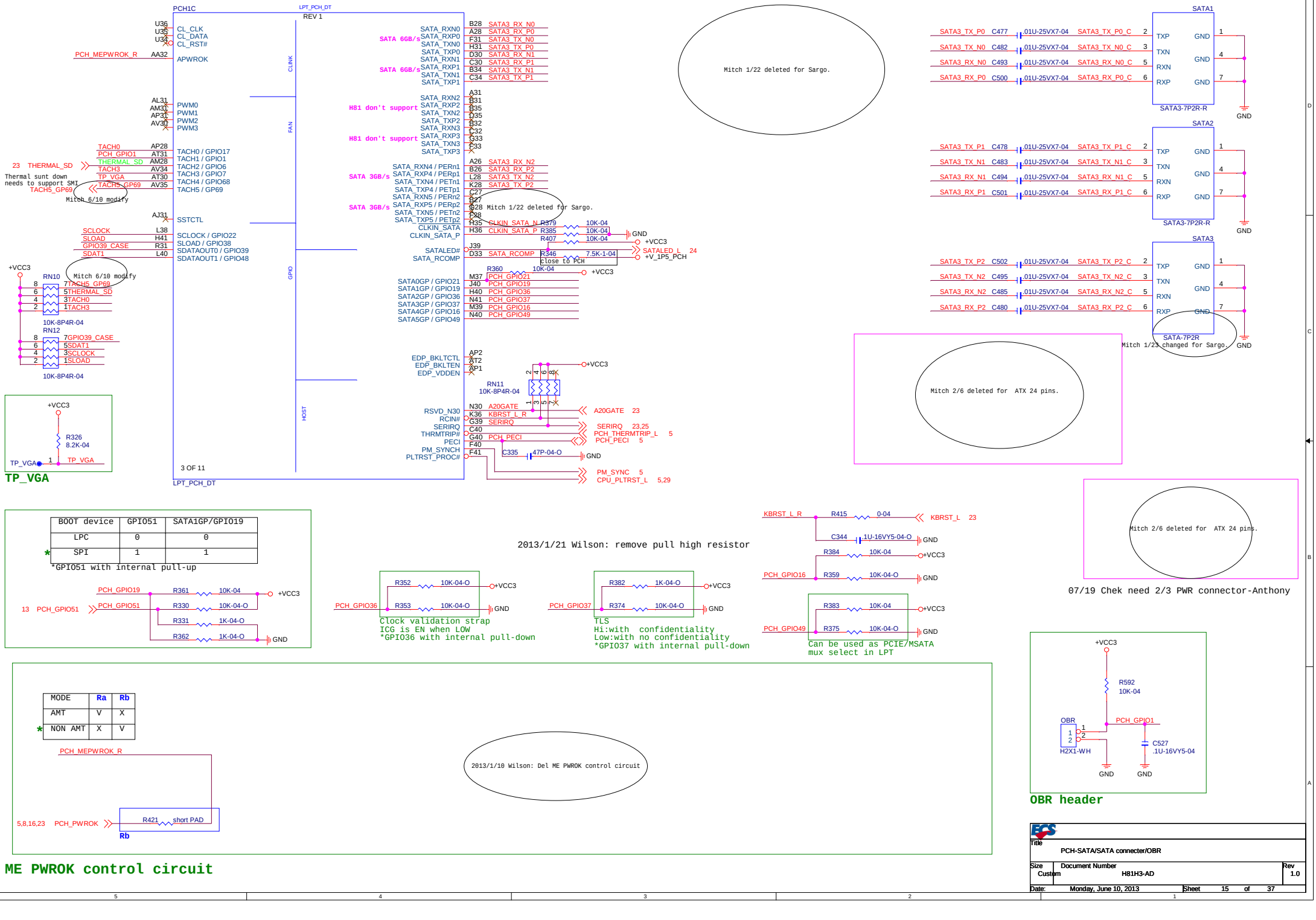
PCH1C
LPT_PCH_DT
REV 1
3 OF 11
LPT_PCH_DT
CLINK
FAN
GPIO
HOST
PCH_MEPWROK_R
APWROK
PWM0
PWM1
PWM2
PWM3
TACH0 / GPIO17
TACH1 / GPIO1
TACH2 / GPIO6
TACH3 / GPIO7
TACH4 / GPIO68
TACH5 / GP69
SSTCTL
SCLOCK / GPIO22
SLOAD / GPIO38
SDATAOUT0 / GPIO39
SDATAOUT1 / GPIO48
SATA 6GB/s
SATA 3GB/s
H81 don't support
CLKIN_SATA
SATALED#
SATA_RCOMP
SATA0GP / GPIO21
SATA1GP / GPIO19
SATA2GP / GPIO36
SATA3GP / GPIO37
SATA4GP / GPIO16
SATA5GP / GPIO49
EDP_BKLTCTL
EDP_BKLTEN
EDP_VDDEN
RSVD_N30
RCIN#
SERIRQ
THRMTRIP#
PECI
PM_SYNCH
PLTRST_PROC#
THERMAL_SD
Thermal sunt down
needs to support SMI
Mitch 6/10 modify
Mitch 1/22 deleted for Sargo.
RN10
RN12
RN11
10K-8P4R-04
R326
8.2K-04
TP_VGA
TP_VGA
R379
R385
R407
R346
7.5K-1-04
close to PCH
R360
10K-04
SATALED_L
+V_1P5_PCH
A20GATE
SERIRQ
PCH_PECI
PCH_THERMTRIP_L
PM_SYNC
CPU_PLTRST_L
C335
47P-04-O
Mitch 1/22 deleted for Sargo.
SATA1
SATA2
SATA3
SATA-7P2R
SATA3-7P2R-R
SATA3_TX_P0_C
SATA3_TX_N0_C
SATA3_RX_N0_C
SATA3_RX_P0_C
SATA3_TX_P1_C
SATA3_TX_N1_C
SATA3_RX_N1_C
SATA3_RX_P1_C
SATA3_TX_P2_C
SATA3_TX_N2_C
SATA3_RX_N2_C
SATA3_RX_P2_C
.01U-25VX7-04
Mitch 1/23 changed for Sargo.
Mitch 2/6 deleted for ATX 24 pins.
Mitch 2/6 deleted for ATX 24 pins.
07/19 Chek need 2/3 PWR connector-Anthony
BOOT device | GPIO51 | SATA1GP/GPIO19
LPC | 0 | 0
SPI | 1 | 1
*GPIO51 with internal pull-up
2013/1/21 Wilson: remove pull high resistor
Clock validation strap
ICG is EN when LOW
*GPIO36 with internal pull-down
TLS
Hi:with confidentiality
Low:with no confidentiality
*GPIO37 with internal pull-down
Can be used as PCIE/MSATA
mux select in LPT
MODE | Ra | Rb
AMT | V | X
NON AMT | X | V
2013/1/10 Wilson: Del ME PWROK control circuit
R421
short PAD
OBR
H2X1-WH
R592
10K-04
C527
.1U-16VY5-04
TP_VGA
ME PWROK control circuit
OBR header
Title
PCH-SATA/SATA connecter/OBR
Size
Custom
Document Number
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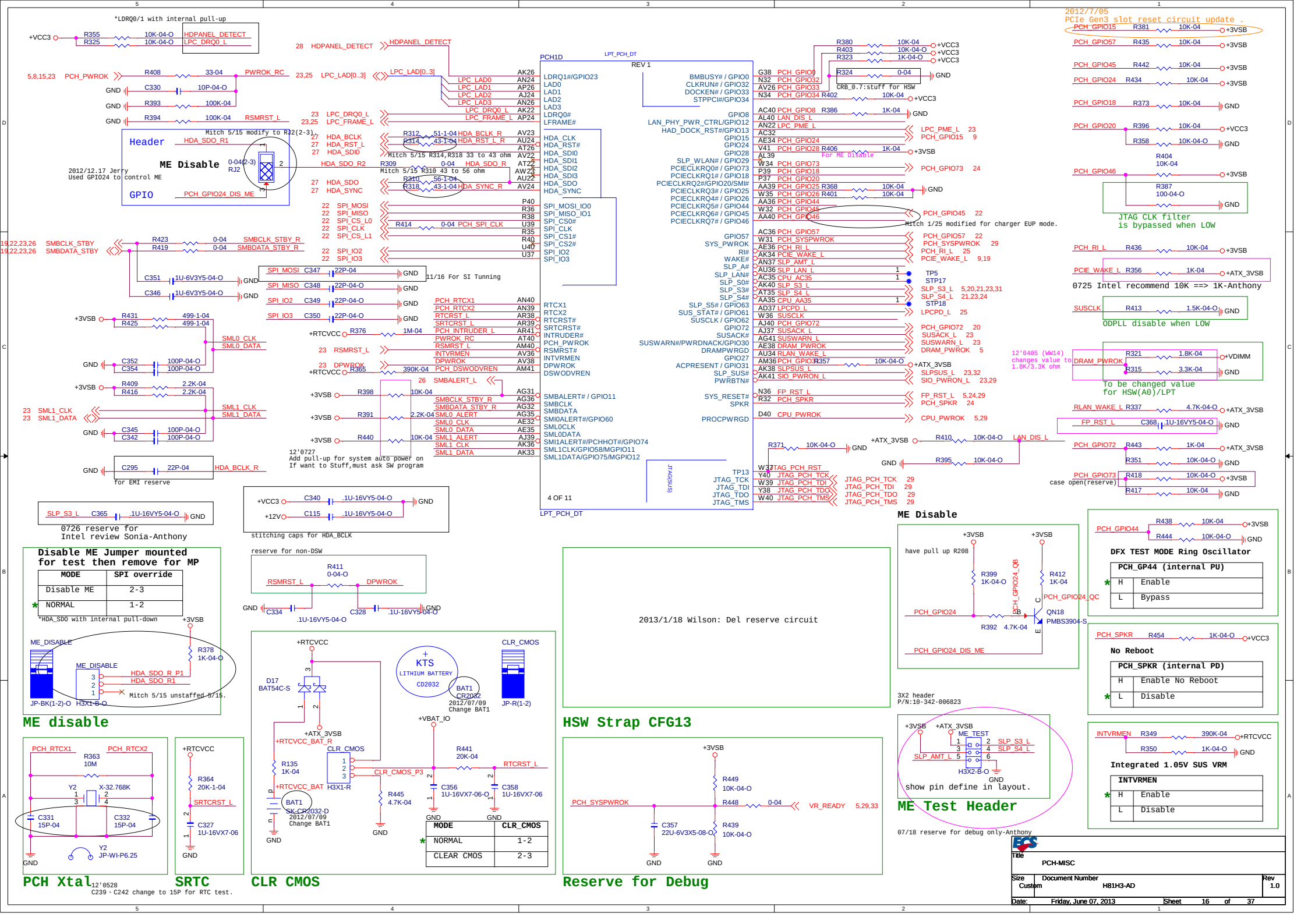
*LDRQ0/1 with internal pull-up
+VCC3
R355 10K-04-O
R325 10K-04-O
HDPANEL_DETECT
LPC_DRQ0_L
28 HDPANEL_DETECT
HDPANEL_DETECT
5,8,15,23 PCH_PWROK
R408 33-04
PWROK_RC
23,25 LPC_LAD[0..3]
LPC_LAD[0..3]
GND
C330 10P-04-O
R393 100K-04
R394 100K-04
RSMRST_L
23 LPC_DRQ0_L
23,25 LPC_FRAME_L
LPC_LAD0
LPC_LAD1
LPC_LAD2
LPC_LAD3
LPC_DRQ0_L
LPC_FRAME_L
Mitch 5/15 modify to R12(2-3).
Header
HDA_SDO_R1
ME Disable
0-04(2-3)
RJ2
2012/12.17 Jerry
Used GPIO24 to control ME
GPIO
PCH_GPIO24_DIS_ME
27 HDA_BCLK
27 HDA_RST_L
27 HDA_SDI0
R312 51-1-04
R314 43-1-04
HDA_BCLK_R
HDA_RST_L_R
Mitch 5/15 R314,R318 33 to 43 ohm
HDA_SDO_R2
R309 0-04
HDA_SDO_R
Mitch 5/15 R310 43 to 56 ohm
27 HDA_SDO
27 HDA_SYNC
R310 56-1-04
R318 43-1-04
HDA_SYNC_R
22 SPI_MOSI
22 SPI_MISO
22 SPI_CS_L0
22 SPI_CLK
22 SPI_CS_L1
22 SPI_IO2
22 SPI_IO3
R414 0-04 PCH_SPI_CLK
19,22,23,26 SMBCLK_STBY
19,22,23,26 SMBDATA_STBY
R423 0-04
R419 0-04
SMBCLK_STBY_R
SMBDATA_STBY_R
C351 1U-6V3Y5-04-O
C346 1U-6V3Y5-04-O
SPI_MOSI C347 22P-04
SPI_MISO C348 22P-04-O
SPI_IO2 C349 22P-04-O
SPI_IO3 C350 22P-04-O
11/16 For SI Tunning
+3VSB
R431 499-1-04
R425 499-1-04
SML0_CLK
SML0_DATA
C352 100P-04-O
C354 100P-04-O
R409 2.2K-04
R416 2.2K-04
23 SML1_CLK
23 SML1_DATA
SML1_CLK
SML1_DATA
C345 100P-04-O
C342 100P-04-O
C295 22P-04
HDA_BCLK_R
for EMI reserve
+RTCVCC
R376 1M-04
23 RSMRST_L
RSMRST_L
23 DPWROK
R365 390K-04
DPWROK
PCH_DSWODVREN
26 SMBALERT_L
R398 10K-04
R391 2.2K-04
R440 10K-04
SMBCLK_STBY_R
SMBDATA_STBY_R
SMLO_ALERT
SMLO_CLK
SMLO_DATA
SML1_ALERT
SML1_CLK
SML1_DATA
12'0727
Add pull-up for system auto power on
If want to Stuff,must ask SW program
PCH_RTCX1
PCH_RTCX2
RTCRST_L
SRTCRST_L
PCH_INTRUDER_L
PWROK_RC
RSMRST_L
INTVRMEN
DPWROK
PCH_DSWODVREN
PCH1D
LPT_PCH_DT
REV 1
LDRQ1#/GPIO23
LAD0
LAD1
LAD2
LAD3
LDRQ0#
LFRAME#
HDA_CLK
HDA_RST#
HDA_SDI0
HDA_SDI1
HDA_SDI2
HDA_SDI3
HDA_SDO
HDA_SYNC
SPI_MOSI_IO0
SPI_MISO_IO1
SPI_CS0#
SPI_CLK
SPI_CS1#
SPI_CS2#
SPI_IO2
SPI_IO3
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
PCH_PWROK
RSMRST#
INTVRMEN
DPWROK
DSWODVREN
SMBALERT# / GPIO11
SMBCLK
SMBDATA
SMI0ALERT#/GPIO60
SML0CLK
SML0DATA
SMI1ALERT#/PCHHOT#/GPIO74
SML1CLK/GPIO58/MGPIO11
SML1DATA/GPIO75/MGPIO12
4 OF 11
LPT_PCH_DT
BMBUSY# / GPIO0
CLKRUN# / GPIO32
DOCKEN# / GPIO33
STPPCI#/GPIO34
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
HAD_DOCK_RST#/GPIO13
GPIO15
GPIO24
GPIO28
SLP_WLAN# / GPIO29
PCIECLKRQ0# / GPIO73
PCIECLKRQ1# / GPIO18
PCIECLKRQ2#/GPIO20/SMI#
PCIECLKRQ3# / GPIO25
PCIECLKRQ4# / GPIO26
PCIECLKRQ5# / GPIO44
PCIECLKRQ6# / GPIO45
PCIECLKRQ7# / GPIO46
GPIO57
SYS_PWROK
RI#
WAKE#
SLP_A#
SLP_LAN#
SLP_S0#
SLP_S3#
SLP_S4#
SLP_S5# / GPIO63
SUS_STAT# / GPIO61
SUSCLK / GPIO62
GPIO72
SUSACK#
SUSWARN#/PWRDNACK/GPIO30
DRAMPWRGD
GPIO27
ACPRESENT / GPIO31
SLP_SUS#
PWRBTN#
SYS_RESET#
SPKR
PROCPWRGD
TP13
JTAG_TCK
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG(SUS)
R380 10K-04
R403 10K-04-O
R323 1K-04-O
+VCC3
R324 0-04
GND
CRB_0.7:stuff for HSW
R402 10K-04
+VCC3
G38 PCH_GPIO0
N32 PCH_GPIO32
AV26 PCH_GPIO33
N34 PCH_GPIO34
AC40 PCH_GPIO8
R386 1K-04
GND
AL40 LAN_DIS_L
AN22 LPC_PME_L
AC32
AE34 PCH_GPIO24
V41 PCH_GPIO28
R406 1K-04
+3VSB
For ME Disable
AL39
W34 PCH_GPIO73
P39 PCH_GPIO18
P37 PCH_GPIO20
AA39 PCH_GPIO25
R368 10K-04
GND
W35 PCH_GPIO26
R401 10K-04
AA36 PCH_GPIO44
W32 PCH_GPIO45
AA40 PCH_GPIO46
Mitch 1/25 modified for charger EUP mode.
LPC_PME_L 23
PCH_GPIO15 9
PCH_GPIO73 24
PCH_GPIO45 22
AC36 PCH_GPIO57
W31 PCH_SYSPWROK
AE36 PCH_RI_L
AK34 PCIE_WAKE_L
AN37 SLP_AMT_L
AU36 SLP_LAN_L
AC35 CPU_AC35
AK40 SLP_S0_L
AT35 SLP_S4_L
AA35 CPU_AA35
AD37 LPCPD_L
W36 SUSCLK
AJ40 PCH_GPIO72
AJ37 SUSACK_L
AG41 SUSWARN_L
AE38 DRAM_PWROK
AU34 RLAN_WAKE_L
AM36 PCH_GPIO37
R357 10K-04-O
+ATX_3VSB
AK38 SLPSUS_L
AK41 SIO_PWRON_L
N36 FP_RST_L
R32 PCH_SPKR
D40 CPU_PWROK
PCH_GPIO57 22
PCH_SYSPWROK 29
PCH_RI_L 25
PCIE_WAKE_L 9,19
TP5
STP17
SLP_S3_L 5,20,21,23,31
SLP_S4_L 21,23,24
STP18
LPCPD_L 25
PCH_GPIO72 20
SUSACK_L 23
SUSWARN_L 23
DRAM_PWROK 5
SLPSUS_L 23,32
SIO_PWRON_L 23,29
FP_RST_L 5,24,29
PCH_SPKR 24
CPU_PWROK 5,29
R371 10K-04-O
GND
+ATX_3VSB
R410 10K-04-O
LAN_DIS_L
GND
R395 10K-04-O
JTAG_PCH_RST
JTAG_PCH_TCK 29
JTAG_PCH_TDI 29
JTAG_PCH_TDO 29
JTAG_PCH_TMS 29
201277/05
PCIe Gen3 slot reset circuit update .
PCH_GPIO15 R381 10K-04 +3VSB
PCH_GPIO57 R435 10K-04 +3VSB
PCH_GPIO45 R442 10K-04 +3VSB
PCH_GPIO24 R434 10K-04 +3VSB
PCH_GPIO18 R373 10K-04 GND
PCH_GPIO20 R396 10K-04 +VCC3
R358 10K-04-O GND
R404 10K-04
PCH_GPIO46 +3VSB
R387 100-04-O GND
JTAG CLK filter
is bypassed when LOW
PCH_RI_L R436 10K-04 +3VSB
PCIE_WAKE_L R356 1K-04 +ATX_3VSB
0725 Intel recommend 10K ==> 1K-Anthony
SUSCLK R413 1.5K-04-O GND
ODPLL disable when LOW
12'0405 (WW14)
changes value to
1.8K/3.3K ohm
DRAM_PWROK
R321 1.8K-04 +VDIMM
R315 3.3K-04 GND
To be changed value
for HSW(A0)/LPT
RLAN_WAKE_L R337 4.7K-04-O +ATX_3VSB
FP_RST_L C368 1U-16VY5-04-O GND
PCH_GPIO72 R443 1K-04 +ATX_3VSB
R351 10K-04-O GND
PCH_GPIO73 R418 10K-04-O +3VSB
case open(reserve)
R417 10K-04 GND
SLP_S3_L C365 .1U-16VY5-04-O GND
0726 reserve for
Intel review Sonia-Anthony
+VCC3 C340 .1U-16VY5-04-O GND
+12V C115 .1U-16VY5-04-O
stitching caps for HDA_BCLK
Disable ME Jumper mounted
for test then remove for MP
MODE | SPI override
Disable ME | 2-3
NORMAL | 1-2
*HDA_SDO with internal pull-down
+3VSB
ME_DISABLE
R378 1K-04-O
HDA_SDO_R_P1
HDA_SDO_R1
Mitch 5/15 unstaffed 5/15.
JP-BK(1-2)-O H3X1-B-O
ME disable
reserve for non-DSW
R411 0-04-O
RSMRST_L
DPWROK
GND
C334 .1U-16VY5-04-O
C328 .1U-16VY5-04-O
GND
2013/1/18 Wilson: Del reserve circuit
HSW Strap CFG13
+RTCVCC
D17 BAT54C-S
KTS LITHIUM BATTERY CD2032
BAT1 CR2032
2012/07/09 Change BAT1
CLR_CMOS
JP-R(1-2)
+VBAT_IO
+ATX_3VSB
+RTCVCC_BAT_R
R135 1K-04
CLR_CMOS
R441 20K-04
RTCRST_L
CLR_CMOS_P3
+RTCVCC_BAT
H3X1-R
BAT1
SK-CR2032-D
2012/07/09
Change BAT1
R445 4.7K-04
C356 1U-16VX7-06-O
C358 1U-16VX7-06
GND
MODE | CLR_CMOS
NORMAL | 1-2
CLEAR CMOS | 2-3
have pull up R208
+3VSB
R399 1K-04-O
PCH_GPIO24_QB
R412 1K-04
PCH_GPIO24_QC
PCH_GPIO24
QN18 PMBS3904-S
R392 4.7K-04
PCH_GPIO24_DIS_ME
ME Disable
PCH_GPIO44 R438 10K-04 +3VSB
R444 10K-04-O GND
DFX TEST MODE Ring Oscillator
PCH_GP44 (internal PU)
H Enable
L Bypass
PCH_SPKR R454 1K-04-O +VCC3
No Reboot
PCH_SPKR (internal PD)
H Enable No Reboot
L Disable
3X2 header
P/N:10-342-006823
+3VSB
+ATX_3VSB
ME_TEST
SLP_S3_L
SLP_S4_L
SLP_AMT_L
H3X2-B-O
GND
show pin define in layout.
ME Test Header
INTVRMEN R349 390K-04 +RTCVCC
R350 1K-04-O GND
Integrated 1.05V SUS VRM
INTVRMEN
H Enable
L Disable
PCH_RTCX1
PCH_RTCX2
R363 10M
Y2 X-32.768K
C331 15P-04
C332 15P-04
Y2 JP-WI-P6.25
PCH Xtal
12'0528
C239、C242 change to 15P for RTC test.
+RTCVCC
R364 20K-1-04
SRTCRST_L
C327 1U-16VX7-06
SRTC
PCH_SYSPWROK
+3VSB
R449 10K-04-O
R448 0-04
VR_READY 5,29,33
C357 22U-6V3X5-08-O
R439 10K-04-O
Reserve for Debug
07/18 reserve for debug only-Anthony
Title
PCH-MISC
Size Custom
Document Number H81H3-AD
Rev 1.0
Date: Friday, June 07, 2013
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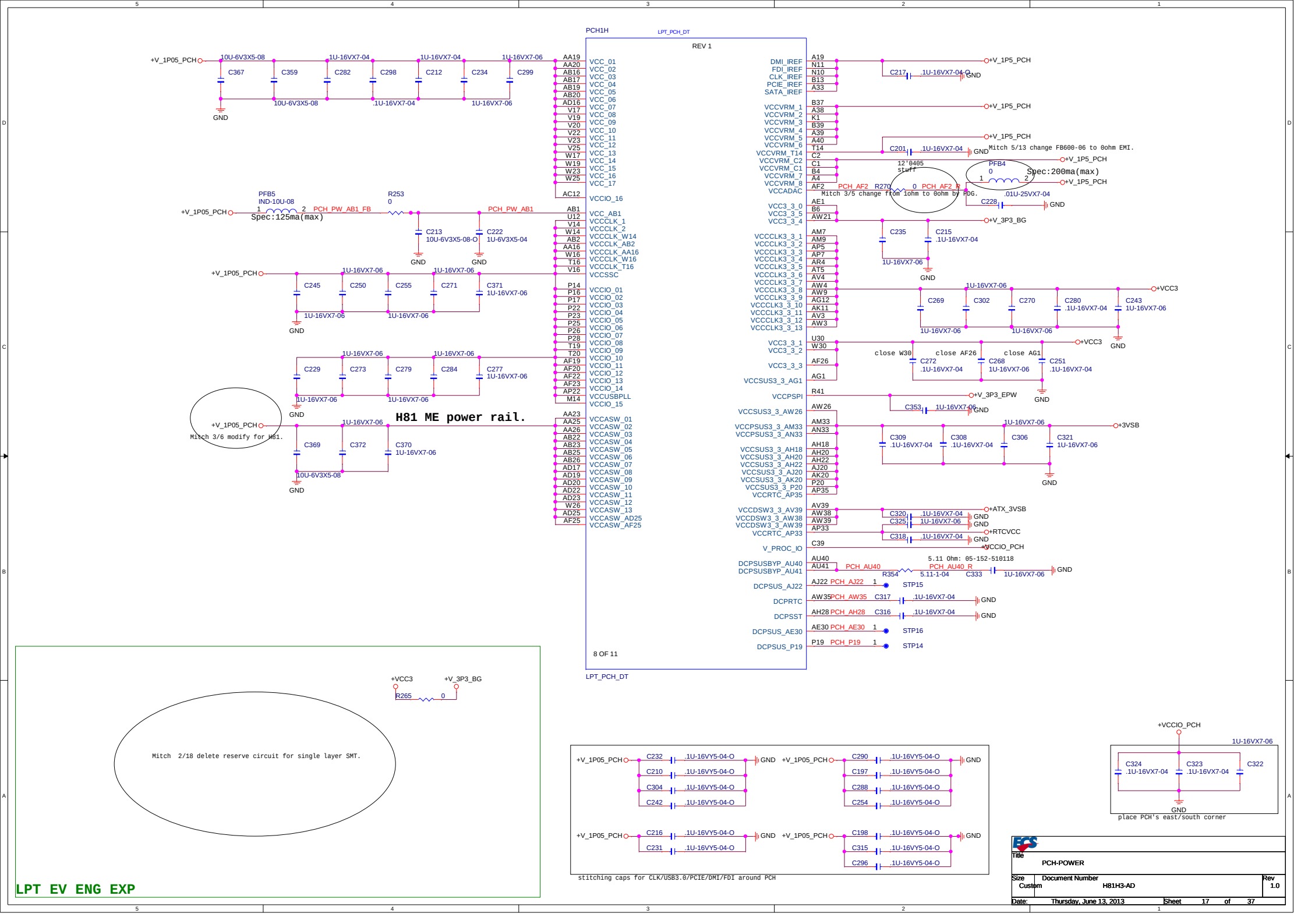
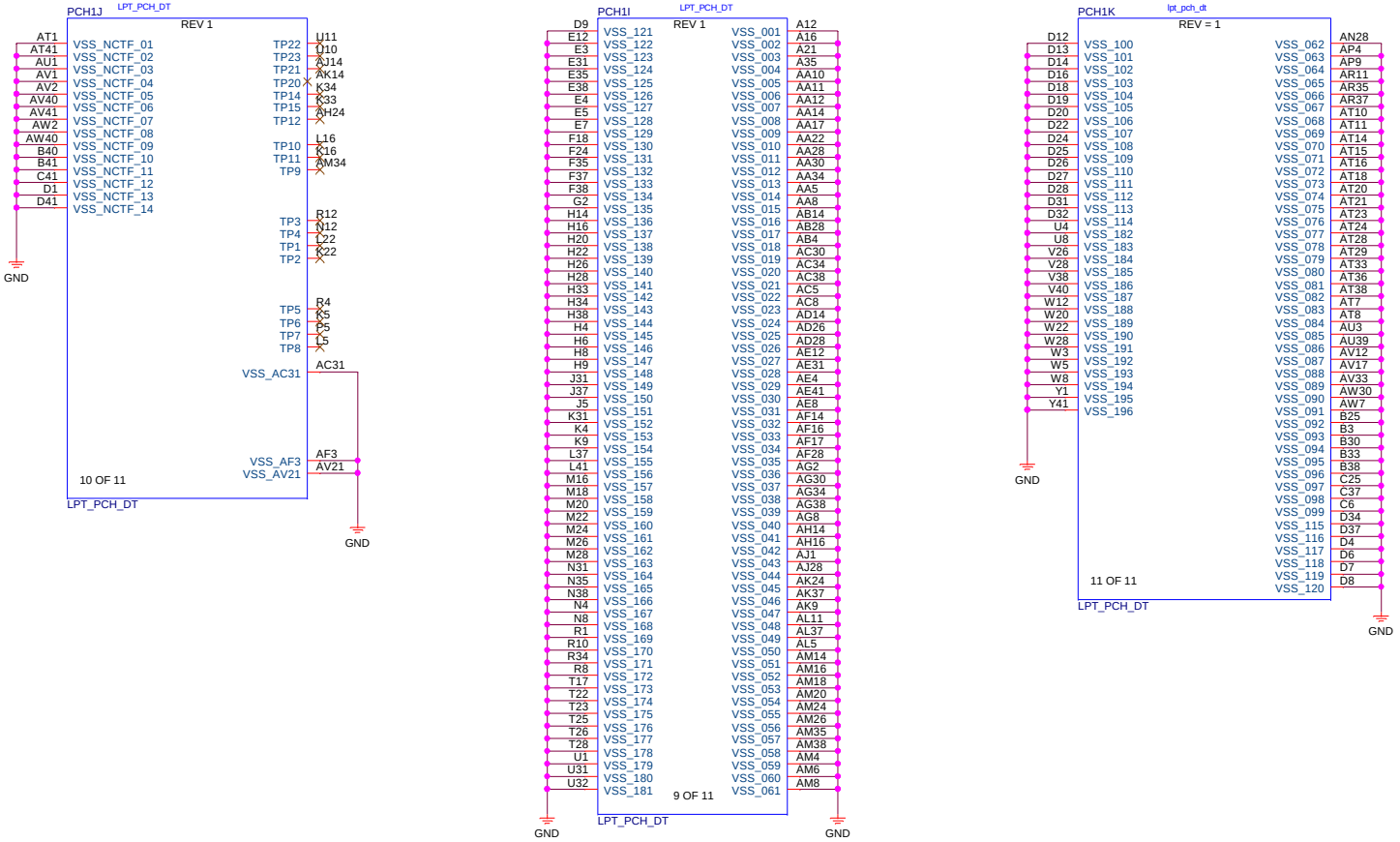

PCH1H
LPT_PCH_DT
REV 1
8 OF 11
LPT_PCH_DT
H81 ME power rail.
Mitch 3/6 modify for H81.
Mitch 2/18 delete reserve circuit for single layer SMT.
LPT EV ENG EXP
Spec:125ma(max)
Spec:200ma(max)
Mitch 5/13 change FB600-06 to 0ohm EMI.
Mitch 3/5 change from 1ohm to 0ohm by RDG.
close W30
close AF26
close AG1
5.11 Ohm: 05-152-510118
stitching caps for CLK/USB3.0/PCIE/DMI/FDI around PCH
place PCH's east/south corner
PCH-POWER
H81H3-AD
Thursday, June 13, 2013
17 of 37
1.0



Title	PCH-GND		
Size	Document Number		Rev
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9,16,22,23,26 SMBCLK_STBY
9,16,22,23,26 SMBDATA_STBY
9,16 PCIE_WAKE_L

SMBCLK_STBY
SMBDATA_STBY
PCIE_WAKE_L

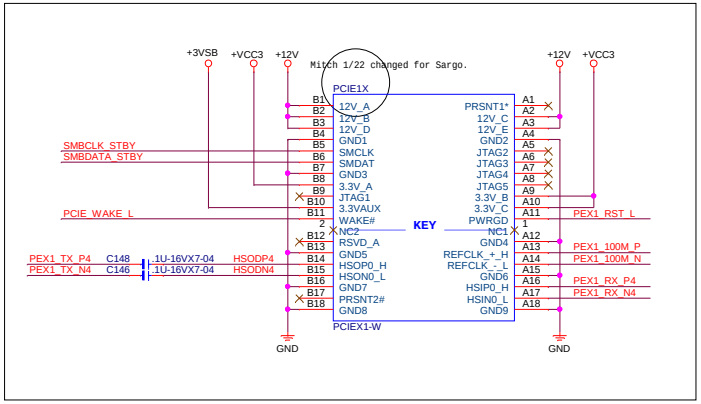
Mitch 1/22 deleted for Sargo.

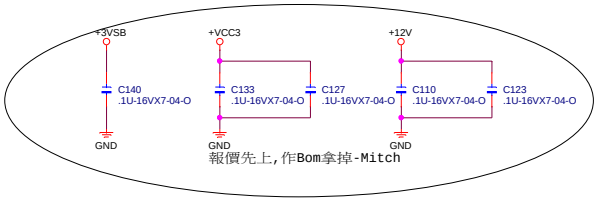
14 PEX1_100M_P
14 PEX1_100M_N
13 PEX1_TX_P4
13 PEX1_TX_N4
13 PEX1_RX_P4
13 PEX1_RX_N4

PEX1_100M_P
PEX1_100M_N
PEX1_TX_P4
PEX1_TX_N4
PEX1_RX_P4
PEX1_RX_N4

Mitch 1/22 deleted for Sargo.

2013/1/8 by nick change

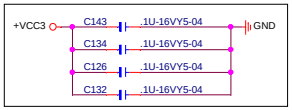




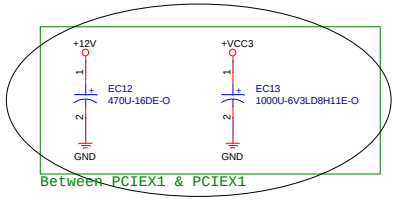
Mitch 1/22 deleted for Sargo.

close to PCIE*1

23 PCIRST1_L
R138 33-04 PEX1_RST_L
C144 10P-04-O
GND



stitching caps for 4X change reference layer



Between PCIEX1 & PCIEX1

2013/1/18 報價不上-Mitch

報價先上,作Bom拿掉-Anthony

Mitch 1/22 deleted for Sargo.

Title	PCIE*4/PCIE*1		
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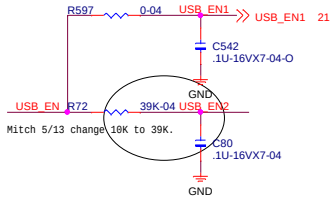
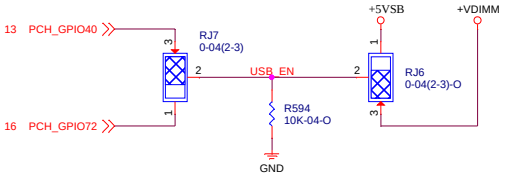
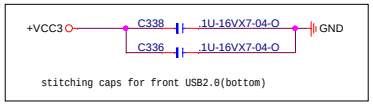
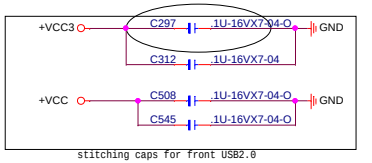




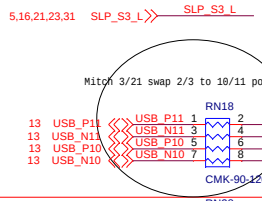
	uP7536 Enable use	RJ?	RJ?	S4/S5 USB_5V_DUAL	Customer
	VDIMM	0ohm (1-2)	NA	0 Volt	Acer S4 w/o S5 w/ USB_5VDUAL
	5VSB	0ohm (2-3)	NA	5 Volt	
*	GPIO	NA	0 ohm	S4 : 0 Volt S5 : 5 Volt	

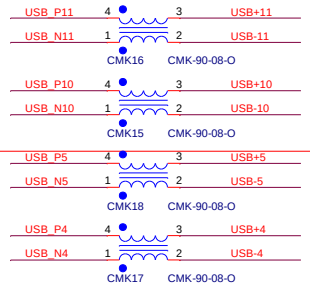


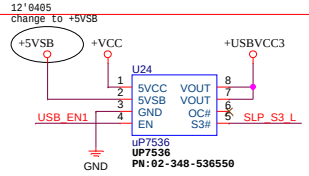


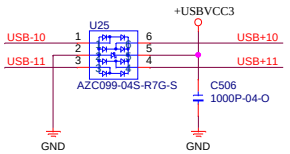
2013/1/9 Wilson Del F_USB3,1#port

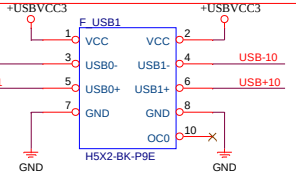
USB2.0 header

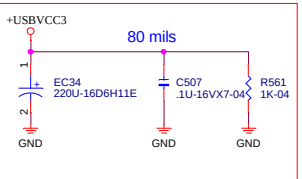


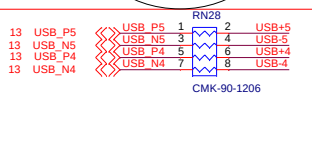


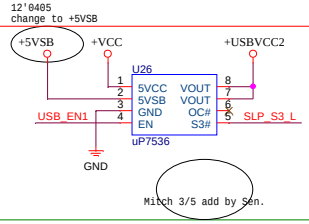


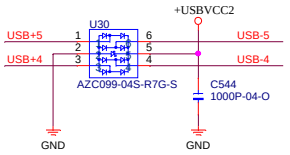


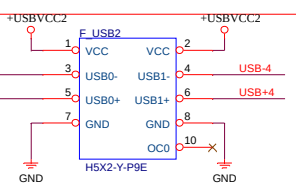


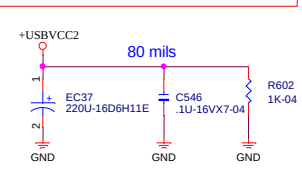




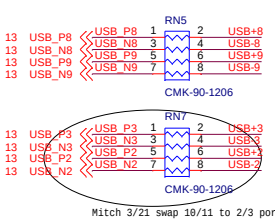


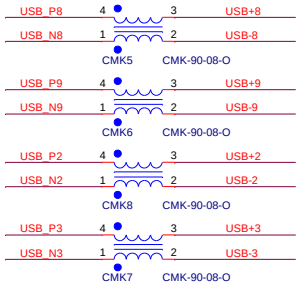


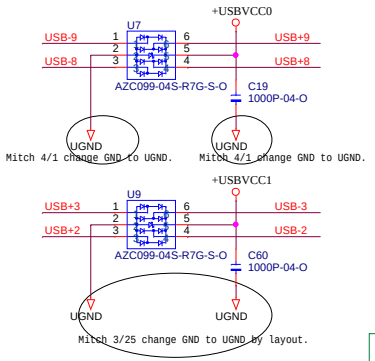


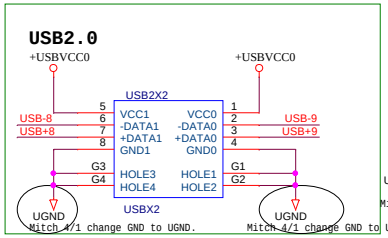


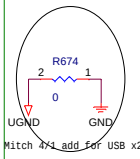
USB2.0 connecter

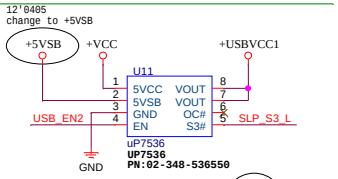


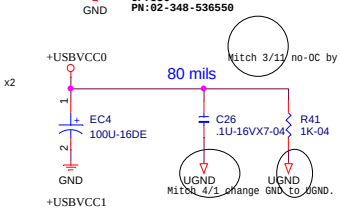


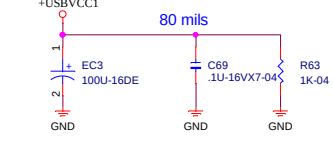


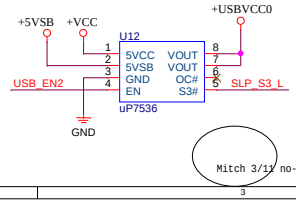


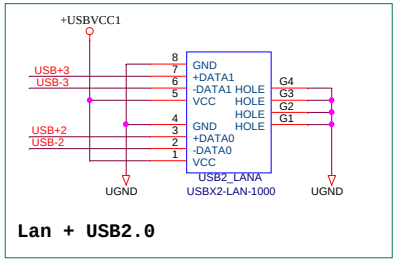












3. OC[3:0]# should be connected with USB 2.0 ports 0 - 7 and any 4 of USB 3.0 ports 1 - 6.
4. OC[7:4]# should be connected with USB 2.0 ports 8 - 13 and any 4 of USB 3.0 ports 1 - 6.

Title	USB2.0 CONN & Header		
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Date: Friday, June 07, 2013	Sheet 20 of 37		

Front USB3-2

need to measure SI

13 USB_N0
13 USB_P0
13 USB_N1
13 USB_P1

7536 — USB_N0_X — USB_N0 2 — RJ4 0-04(1-2) — 2543 — USB_N0_2543_OUT
USB_N0_2543_IN — R471 0-04-O — USB_N0_X
Mitch 6/11 change to no charger function.

7536 — USB_P0_X — USB_P0 2 — RJ3 0-04(1-2) — 2543 — USB_P0_2543_OUT
USB_P0_2543_IN — R470 0-04-O — USB_P0_X

RN15 (CMK-90-12-06): USB_N0_X / USB_P0_X / USB_N1 / USB_P1 → USB_N0_R / USB_P0_R / USB_N1_R / USB_P1_R
CMK10 (CMK-90-08-O): USB_P0_X / USB_N0_X → USB_P0_R / USB_N0_R
CMK9 (CMK-90-08-O): USB_P1 / USB_N1 → USB_P1_R / USB_N1_R

CMK12 (CMK-50-08-USB3.0-O): USB3_TX_N0_C → USB3_TX_N0_R; USB3_TX_P0_C → USB3_TX_P0_R
CMK11 (CMK-50-08-USB3.0-O): USB3_TX_N1_C → USB3_TX_N1_R; USB3_TX_P1_C → USB3_TX_P1_R
CMK14 (CMK-50-08-USB3.0-O): USB3_RX_N0 → USB3_RX_N0_R; USB3_RX_P0 → USB3_RX_P0_R
CMK13 (CMK-50-08-USB3.0-O): USB3_RX_N1 → USB3_RX_N1_R; USB3_RX_P1 → USB3_RX_P1_R

14 USB3_RX_N0
14 USB3_RX_P0
14 USB3_RX_N1
14 USB3_RX_P1
RN17 (0-8P4R): USB3_RX_N0_R / USB3_RX_P0_R / USB3_RX_N1_R / USB3_RX_P1_R

14 USB3_TX_N0
14 USB3_TX_P0
14 USB3_TX_N1
14 USB3_TX_P1
C429 .1U-16VX7-04 USB3_TX_N0_C
C428 .1U-16VX7-04 USB3_TX_P0_C
C420 .1U-16VX7-04 USB3_TX_N1_C
C405 .1U-16VX7-04 USB3_TX_P1_C
RN16 (0-8P4R): USB3_TX_N0_C / USB3_TX_P0_C / USB3_TX_N1_C / USB3_TX_P1_C → USB3_TX_N0_R / USB3_TX_P0_R / USB3_TX_N1_R / USB3_TX_P1_R

Mitch 3/11 no-OC by Sen.

Mitch 5/13 combine power net.
+USB3_2543_2 +USB3VCC2_1 Mitch 5/13 delete R528 for SI.
Mitch 6/11 change to no charger function.
+USB3VCC2_2 +USB3VCC2
80 Mils
Mitch 10/18 rename F_USB2 to USB3_F1
7536 R481 0-08 — 2543 R529 0-08
USB3_F1 H10X2-P20E-BK: VBUS1 SSRX1- SSRX1+ GND16 SSTX1- SSTX1+ GND13 D1- D1+ VBUS0 SSRX0- SSRX0+ GND4 SSTX0- SSTX0+ GND7 D0- D0+ KEY
EC28 220U-16DE — C454 1U-16VX7-04
D20 ESD3V3U4ULC-O: I/O1 I/O2 GND I/O3 I/O4 NC NC NC NC
D21 ESD3V3U4ULC-O: I/O1 I/O2 GND I/O3 I/O4 NC NC NC NC
U17 AZC099-04S-R7G-S: USB_N0_R / USB_N1_R → USB_P0_R / USB_P1_R
C402 1000P-04-O
Mitch 5/13 combine power net.
+USB3_2543_2

12'0405 change to +5VSB
7536
+VCC +5VSB +USB3VCC2_2 +USB3VCC2_1
5,16,20,21,23,31 SLP_S3_L
20 USB_EN1
U22 UP7537BSUB: S3# EN 5VCC GND VOUT1 VOUT2 VOUT3 5VSB
C486 1U-6V3X5-04
C481 1U-6V3X5-04
EC29 220U-16DE — C491 1U-16VX7-04 — R533 1K-04 — C503 1U-16VX7-04 — R545 1K-04
80 Mils
Mitch 12/26 added.
UP7537 PN:02-345-537551
12'9328 GND
Mitch 12/26 added.
In order to safety criterion, UP7537 only use two output.

Input Logic Level				Logic Output 2543	
INPUT1 S4	INPUT2 Pull high	INPUT3 Pull High	ILIM_SEL S3/ S4	Charging Mode	WAKE Output (active low)
0	0	0	X	OUT discharge, power switch off	off
0	0	1	0	Dedicated charging port, auto-detect	off
0	1	0	X	Dedicated charging port, auto-detect, w/ Mouse/Keyboard detect + pass through enabled (back to auto detect when detached)	active low if DCP load present
X	1	0	X	Standard downstream port, USB 2.0 Mode	off
1	0	0	X	Dedicated charging port, BC1.2 only	off
0	1	1	1	Auto mode, keyboard/mouse wakeup, no load detection	off
1	1	1	0	Standard downstream port, USB 2.0 Mode,no discharge	off
1	1	1	1	Charging downstream port, BC1.2	active low if CDP load present

S4/S5
S3
S0

5,16,20,21,23,31 SLP_S3_L
16,23,24 SLP_S4_L
Mitch 3/20 modify for Nokia N8 SDP issue.
R480 0-04-O — Q8 2N7002-S-O
+USB_5VDUAL1
R490 20K-04-O — R496 80.6K-1-04-O — R504 100K-04-O
Mitch 3/11 no-OC by Sen.
TPS2543_PG TPS2543_ILIM TPS2543_FLT

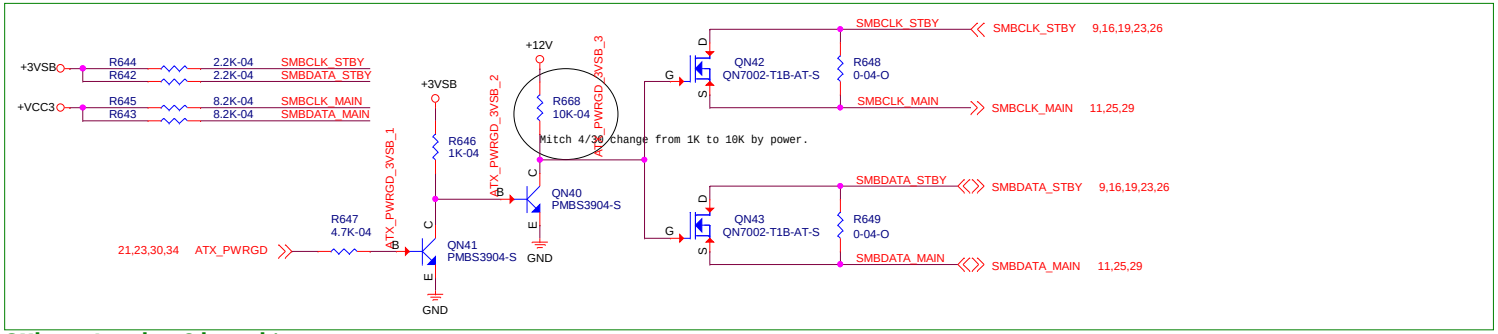
U19 TPS2546-O: PAD ILIM_HI ILIM_LO GND1 FAULT# IN DM_OUT DP_OUT ILIM_SEL OUT DM_IN DP_IN WAKE# EN CTL1 CTL2 CTL3
+USB3_2543_2 80 Mils
USB_N0_2543_OUT USB_P0_2543_OUT C2_ILIM_SEL
USB_N0_2543_IN USB_P0_2543_IN TPS2543_PG
R513 100K-04-O — +USB_5VDUAL1
RJ5 10K-04(1-2)-O
C445 10U-10VY5-08-O — C446 1U-16VX7-04-O
Mitch 10/9 change value of R579 from 0 --> 10K ohm.
Mitch 2/23 modify for S3 SDP and S4/S5 DCP.
GNDGND GND

Mitch 10/9 modified
23 SIO_GP76
3VSB +ATX_3VSB
R515 0-04-O — R511 0-04-O 3VSB_R
Mitch 1/25 modified for charger
SLP_S3_L R489 0-04-O — R488 0-04-O — R493 0-04-O
R494 10K-04-O — R501 10K-04-O — R507 10K-04-O — R512 10K-04-O
Mitch 2/23 modify for S3 SDP and S4/S5 DCP.
R500 10K-04-O — R506 10K-04-O — R516 10K-04-O
Mitch 6/11 change to no charger function.
Mitch 12/25 modified for H81.

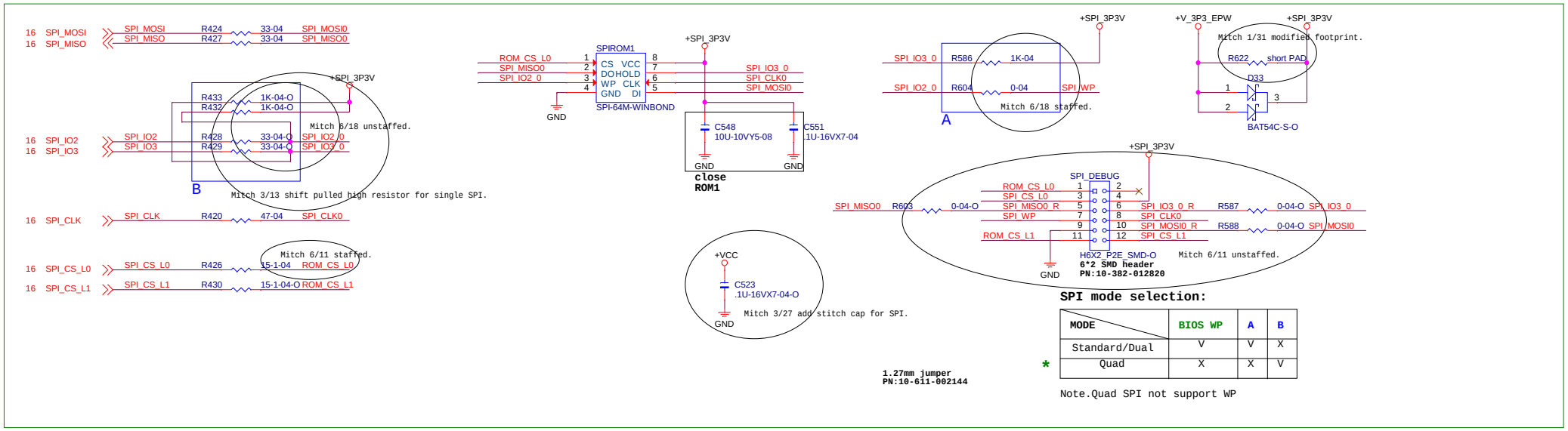
5V_DUAL

Mitch 6/7 change to +ATX_5VSB
Mitch 6/7 delete R563, R559-O for charger issue.
+ATX_5VSB — R563 4.7K-04-O — +ATX_5VSB
R575 4.7K-04-O
SLP_S3 — ATX_D — R576 1K-04-O — Q12 2N3904-S-O — C519 .1U-16VX7-04-O
SLP_S3_L_ATX_D1
R570 10K-04-O — 80 Mils — +USB_5VDUAL1
Q9 APM4500AKC-O: APM4500_P4 APM4500_P2 +VCC
22,23,30,34 ATX_PWRGD — Q10 2N7002-S-O
Mitch 6/7 change to +ATX_5VSB
Mitch 6/11 change to no charger function.
+12V
R567 0-04-O — +ATX_5VSB — R568 4.7K-04-O — R590 1K-04-O
SLP_S3_L_ATX_D2
R566 1K-04-O — Q11 2N3904-S-O — C509 1U-16VX7-04-O
SLP_S3_L_ATX_D3
SLP_S3_L_ATX_AND
SLP_S3_L_ATX_D4
5,16,20,21,23,31 SLP_S3_L — R693 0-04-O — Q13 2N7002-S-O

Title	USB3.0 Header
Size: Custom	Document Number: H81H3-AD — Rev: 1.0
Date: Thursday, June 13, 2013	Sheet 21 of 37

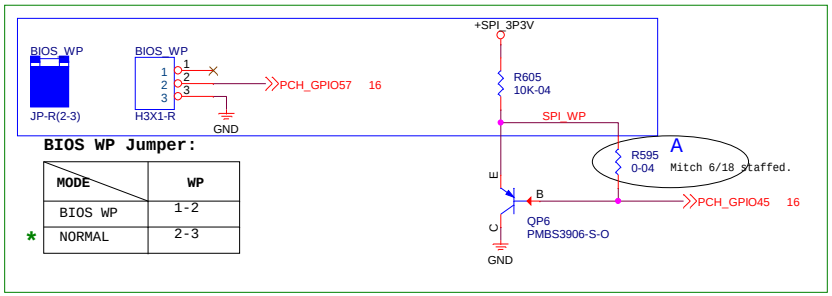


SMbus Logic Circuit



MODE	BIOS WP	A	B
Standard/Dual	V	V	X
* Quad	X	X	V

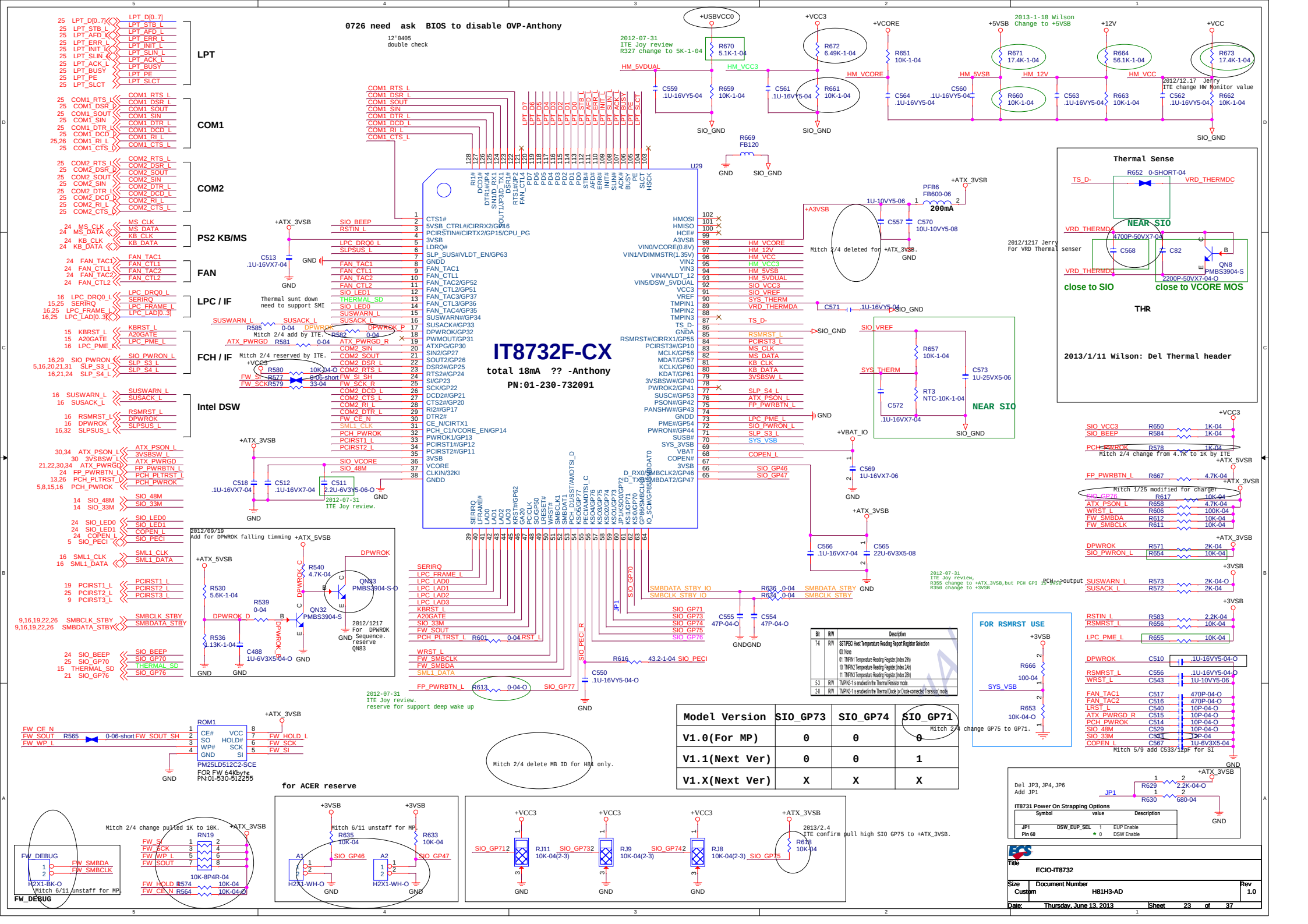
SPI ROM

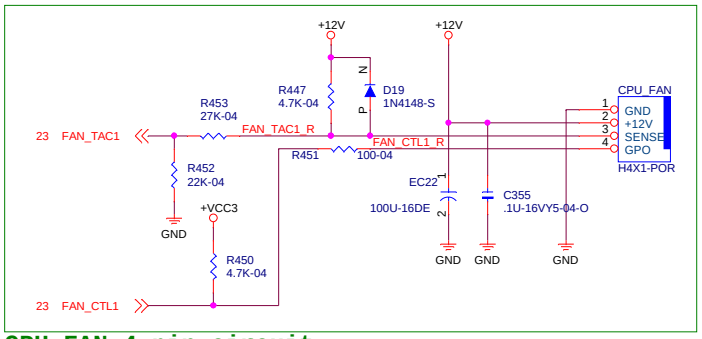


MODE	WP
BIOS WP	1-2
* NORMAL	2-3

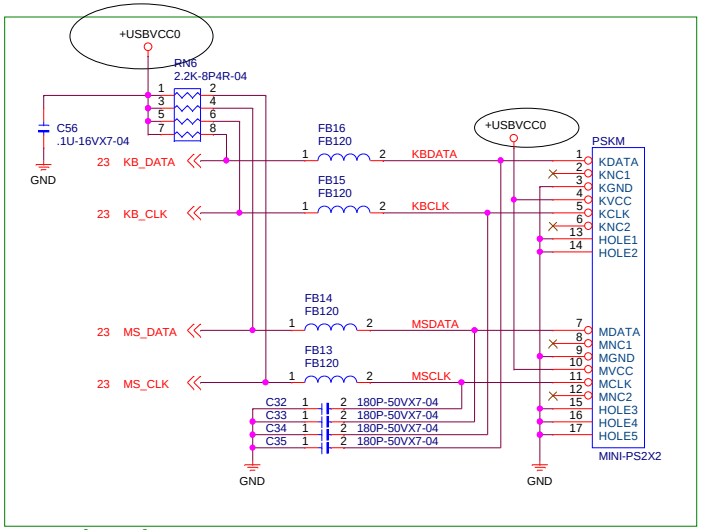
BIOS WP

Title	SPI/SMbus		
Size	Document Number		Rev
Custom	H81H3-AD		1.0
Date:	Tuesday, June 18, 2013	Sheet 22 of 37	

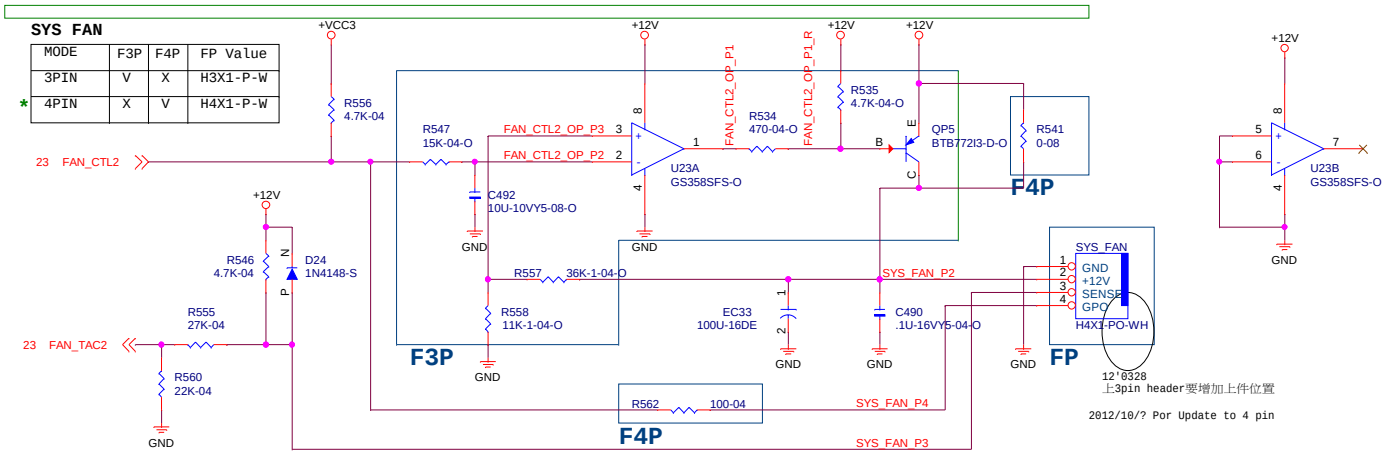

0726 need ask BIOS to disable OVP-Anthony
12'0405
double check
IT8732F-CX
total 18mA ?? -Anthony
PN:01-230-732091
LPT
COM1
COM2
PS2 KB/MS
FAN
LPC / IF
FCH / IF
Intel DSW
Thermal Sense
NEAR SIO
close to SIO
close to VCORE MOS
THR
2013/1/11 Wilson: Del Thermal header
FOR RSMRST USE
for ACER reserve
FW_DEBUG
ECIO-IT8732
Model Version | SIO_GP73 | SIO_GP74 | SIO_GP71
V1.0(For MP) | 0 | 0 | 0
V1.1(Next Ver) | 0 | 0 | 1
V1.X(Next Ver) | X | X | X



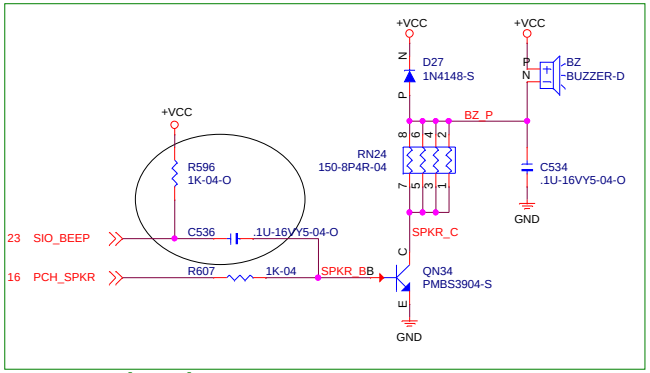
CPU_FAN 4 pin circuit



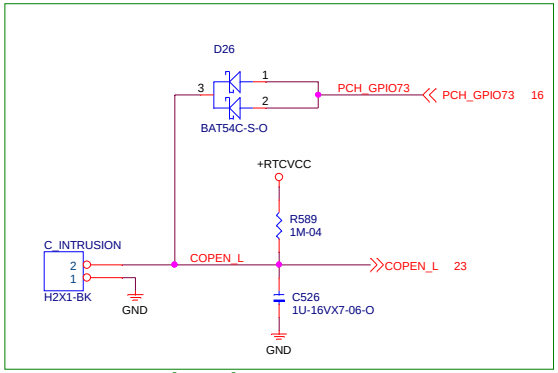
PS2 circuit



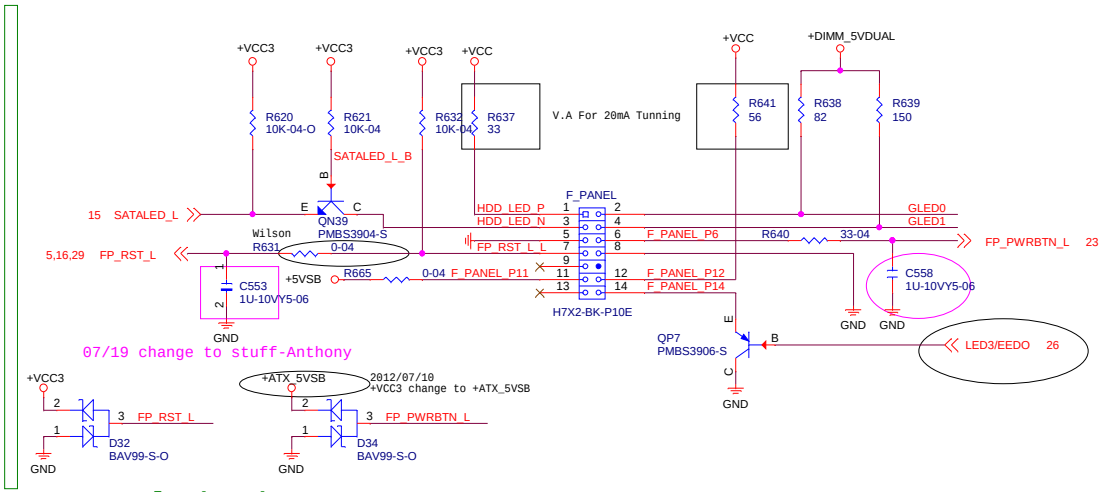
SYS_FAN 3/4 pin co-layout circuit



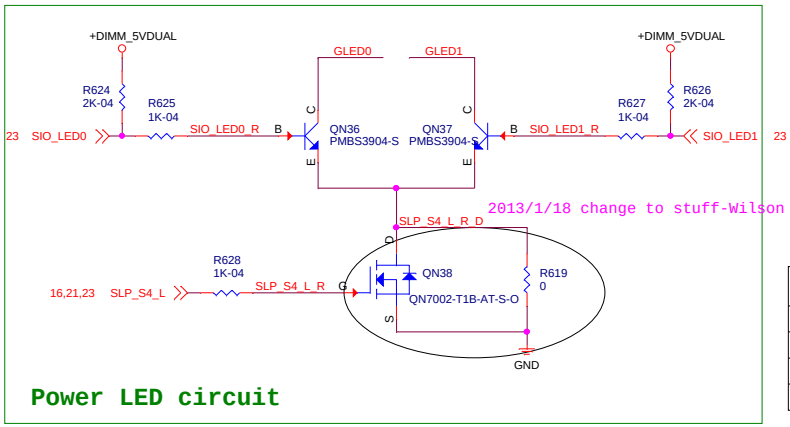
Buzzer circuit



Case open circuit



Front Panel circuit



Power LED circuit

SIO_LED1 SIO_GP37	SIO_LED0 SIO_GP35	POWER LED
0(low)	0(low)	OFF
0(low)	1(High)	OFF
1(High)	0(low)	ON
1(High)	1(High)	OFF

Title	FAN/PS2/Buzzer/F_Panel	
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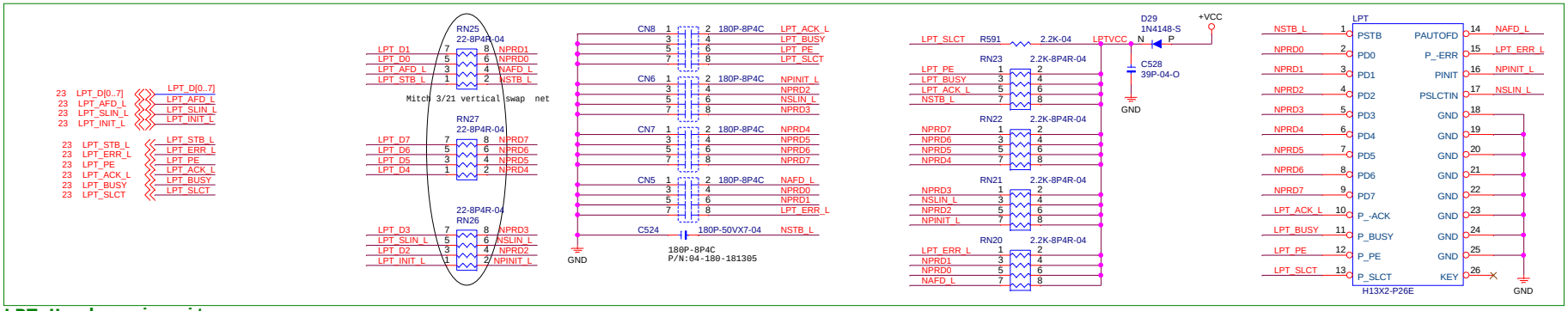
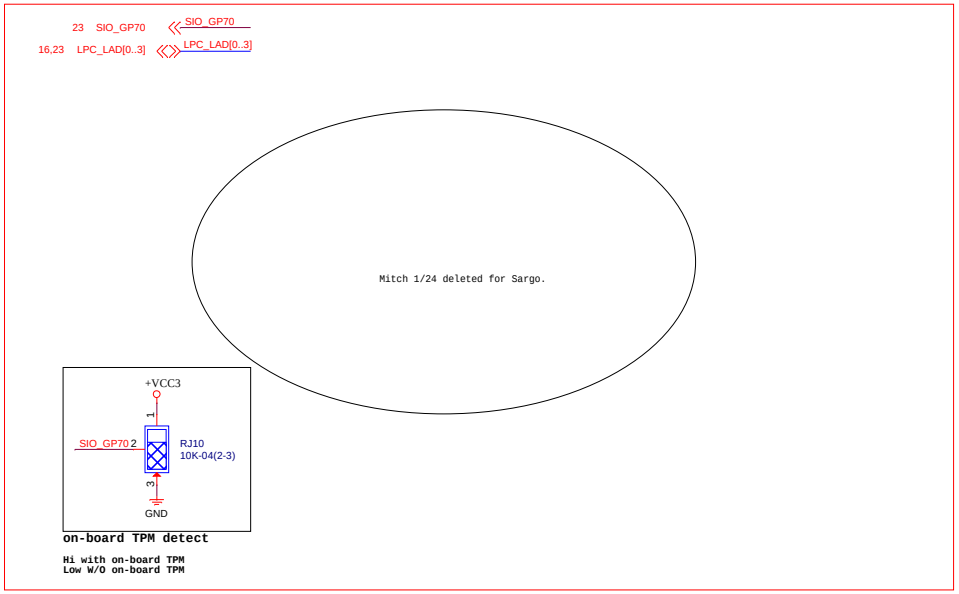
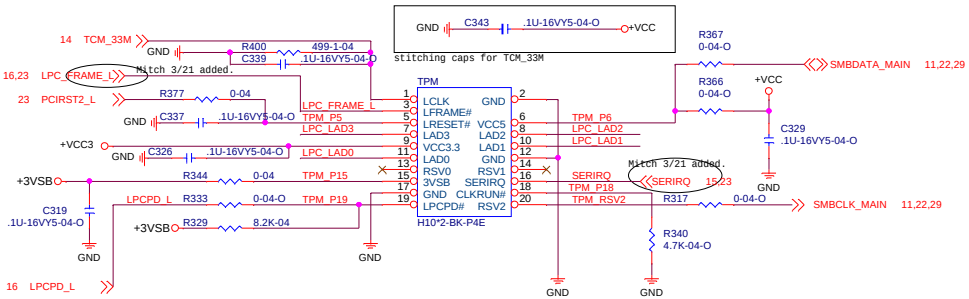
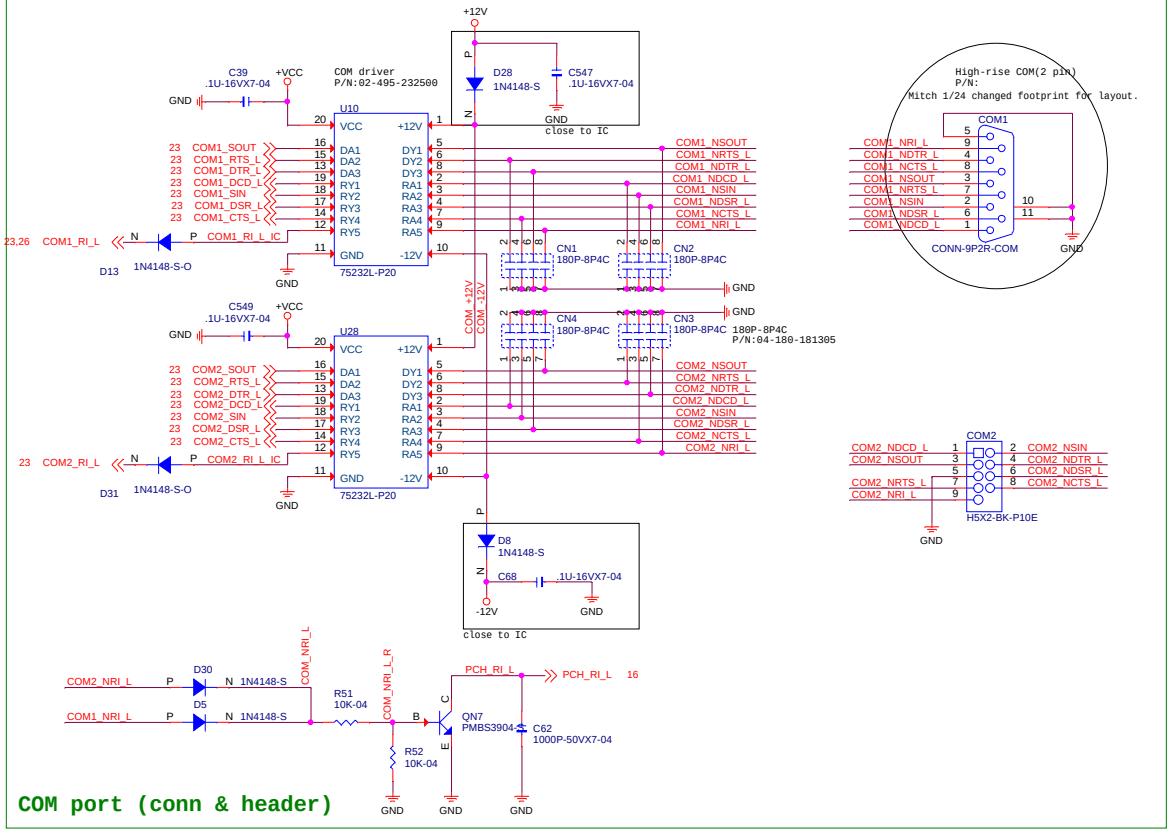


LPT Header circuit





TPM chip/header circuit



COM port (conn & header)

Title	LPT/COM/TPM	
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2013/1/18 報價先上,作Bom上0 ohm -Mitch

For RTL8111E
* Bellow CAP are for VDD33 pins-- 12, 27, 39, 42, 47, 48.

+VDD33

Imax=200mA

Mitch 5/7 modify for LAN PWR SI.

LAN 3.3V rise time > 1ms, < 100ms.

200mils

Use External 1.05V Supply When Disable Switch Regulator.
If Using External 1.2V Supply Pls. Contact With FAE.

Pls. refer to 8111E Layout Guide for Lx, Cout1, Cout2 selection criteria.

Imax=300mA

For RTL8111E
* Bellow CAPs are for VDD10 pins-- 3, 6, 9, 13, 29, 41, 45.

1.05V

* Bellow CAPs are for EVD1D10 pins--21.

The power inductor SPEC.

L(uH)/ toerance	ESR(ohm) @ 1MHz	
2.2 or 4.7 / <=20%	Below 0.8	

40mils

Remove For Disable Switch Regulator (Accept External 1.05V Power Supply)

Acer/FDR request:
1:default use e-FUSE;
2:only reserve External EEPROM;

e-Fuse pull low

Pull high in PCH

93C46 P/N:01-530-046157
93C66 P/N:01-530-066020

R684 value should be 2.49K (1%) for all application.

More Detail Layout
Pls. Refer to Layout Guide

R677 For Enable Switch Regulator.
R679 For Disable Switch Regulator.

+VCC3

RTL8105E/8111E

Mitch 5/16 change C114, C120 for SI.
(主)07-135-250024
(替)07-135-250031

Mitch 2/5 change to ATX_3VSB.

Stuff R when use RTL LAN and support G3~S5 WOL

2013/1/18 Wilson: Link to RI to support G3 to S5

Place above two CAP near LAN chip.

Close to LAN side

Near to RJ45 conn.

Place 3/1 deleted 1UF cap.

Mitch 3/1 adjust wired net of +VDD3 .

Acer Lan LED Status

Wake on LAN (WOL) set to ON ==> In BIOS and OS

	LED		S0	S1	S3	S4	S5	G3 to S5 unplug and plug power cord
Rear Side	ACTIVE-LED (Single Color)	Access:Blink	Blink	Blink	Blink	Blink	Blink	OFF
		Others:OFF	OFF	OFF	OFF	OFF	OFF	OFF
	SPEED-LED (Dual Color)	Disconnected:OFF	OFF	OFF	OFF	OFF	OFF	OFF
		1000:ON with A color:Amber	Amber	OFF	OFF	OFF	OFF	OFF
		100:ON with B color:Green	Green	OFF	OFF	OFF	OFF	OFF
		10:OFF	OFF	OFF	OFF	OFF	OFF	OFF
Front Side	(Single Color)	Access: Blinking Others: OFF	Access: Blinking Others: OFF	Access: Blinking Others: OFF	OFF	OFF	OFF	OFF

Wake on LAN (WOL) set to OFF ==> In BIOS and OS

	LED	S0	S0	S1	S3	S4	S5	G3 to S5 unplug and plug power cord
Rear Side	ACTIVE-LED (Single Color)	Access:Blink	Blink	OFF	OFF	OFF	OFF	OFF
		Others:OFF	OFF	OFF	OFF	OFF	OFF	OFF
	SPEED-LED (Dual Color)	Disconnected:OFF	OFF	OFF	OFF	OFF	OFF	OFF
		1000:ON with A color:Amber	Amber	OFF	OFF	OFF	OFF	OFF
		100:ON with B color:Green	Green	OFF	OFF	OFF	OFF	OFF
		10:OFF	OFF	OFF	OFF	OFF	OFF	OFF
Front Side	(Single Color)	Access: Blinking Others: OFF	Access: Blinking Others: OFF	OFF	OFF	OFF	OFF	OFF

Acer Spec:

LAN LED	
Active	Green
LINK1000	Orange
LINK100	Green
LINK10	OFF

Title	LAN RTL8111E
Size	Custom
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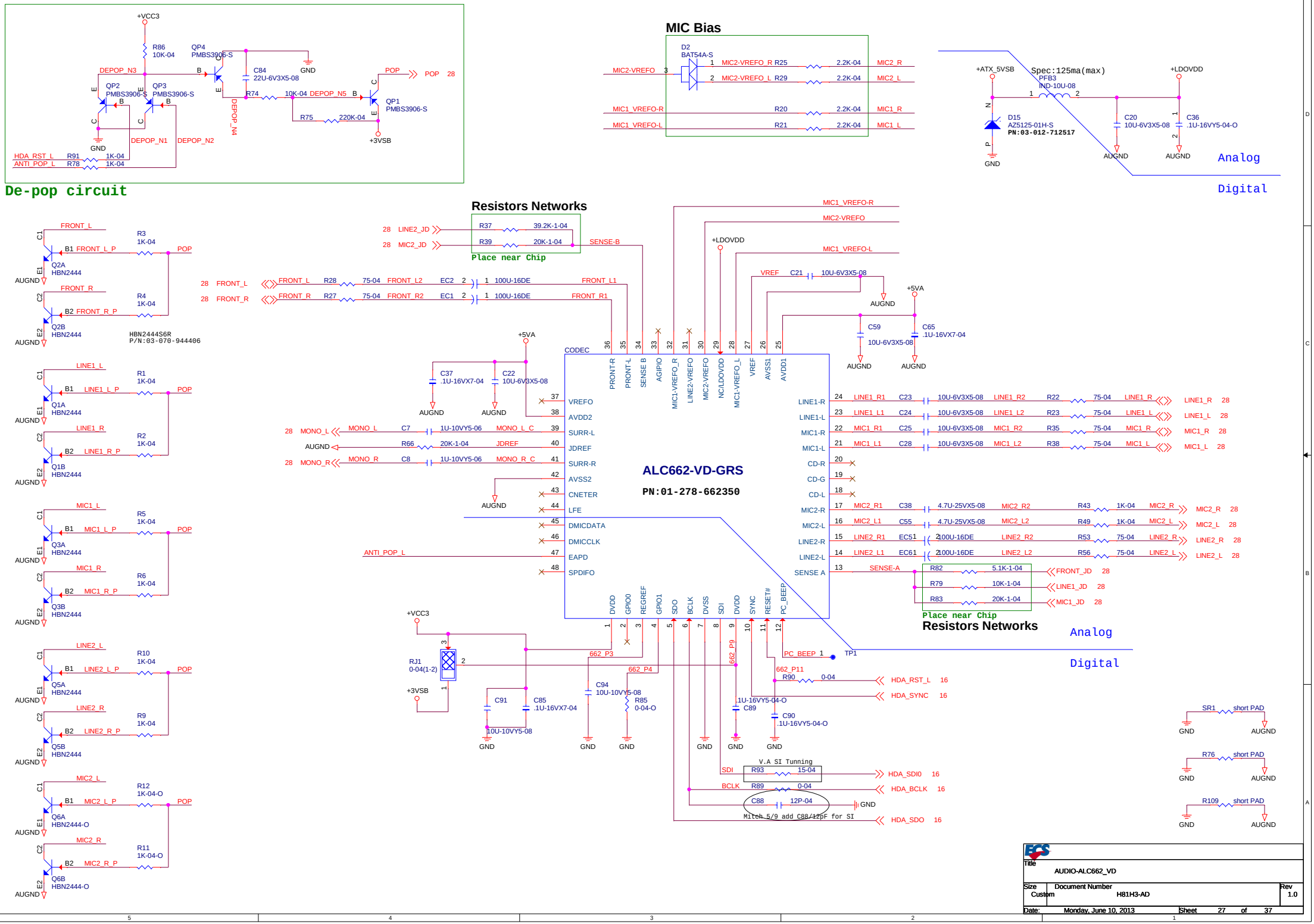
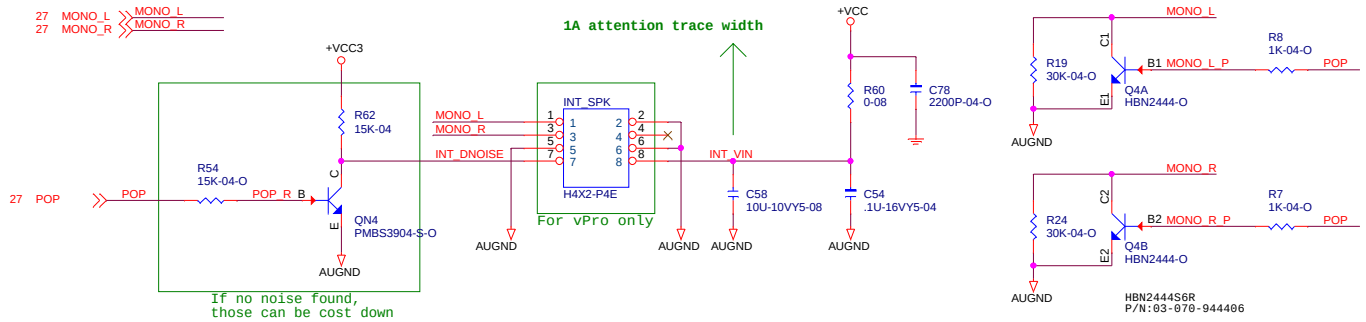
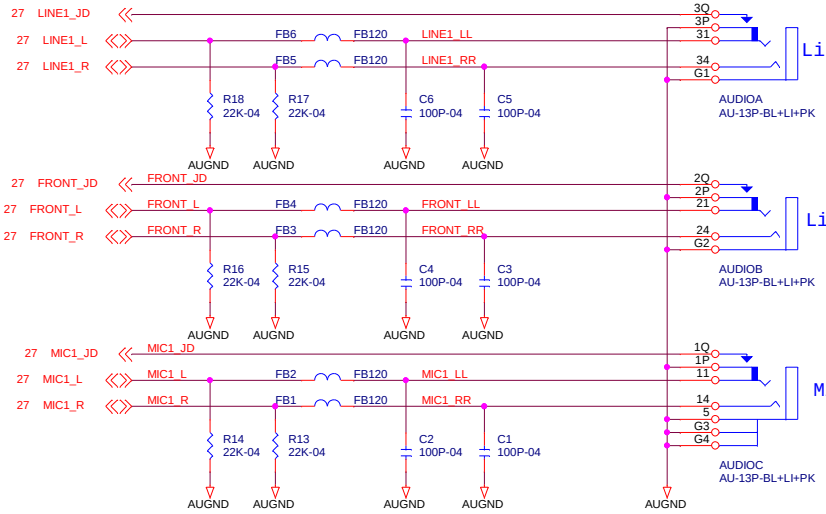
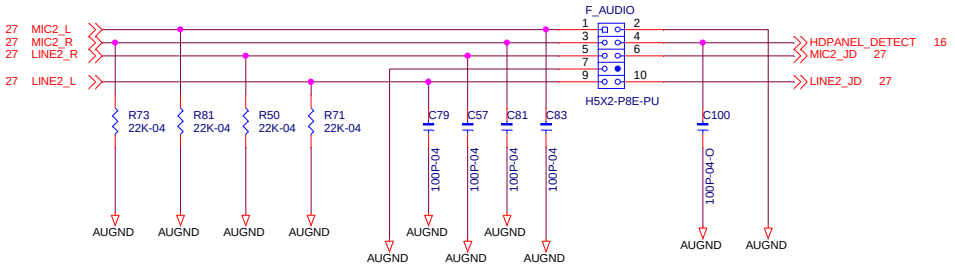
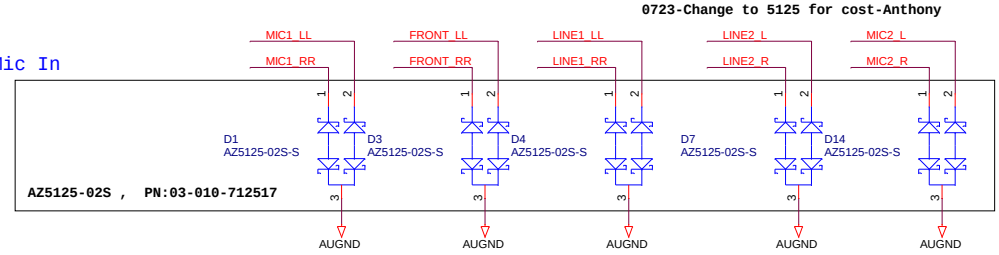
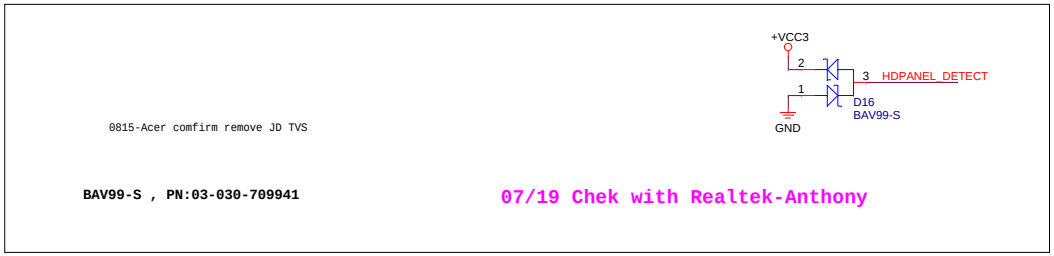

De-pop circuit
MIC Bias
Resistors Networks
Place near Chip
ALC662-VD-GRS
PN:01-278-662350
Analog
Digital
HBN2444S6R
P/N:03-070-944406
V.A SI Tunning
Mitch 5/9 add C88/12pF for SI
AUDIO-ALC662_VD
H81H3-AD
Monday, June 10, 2013



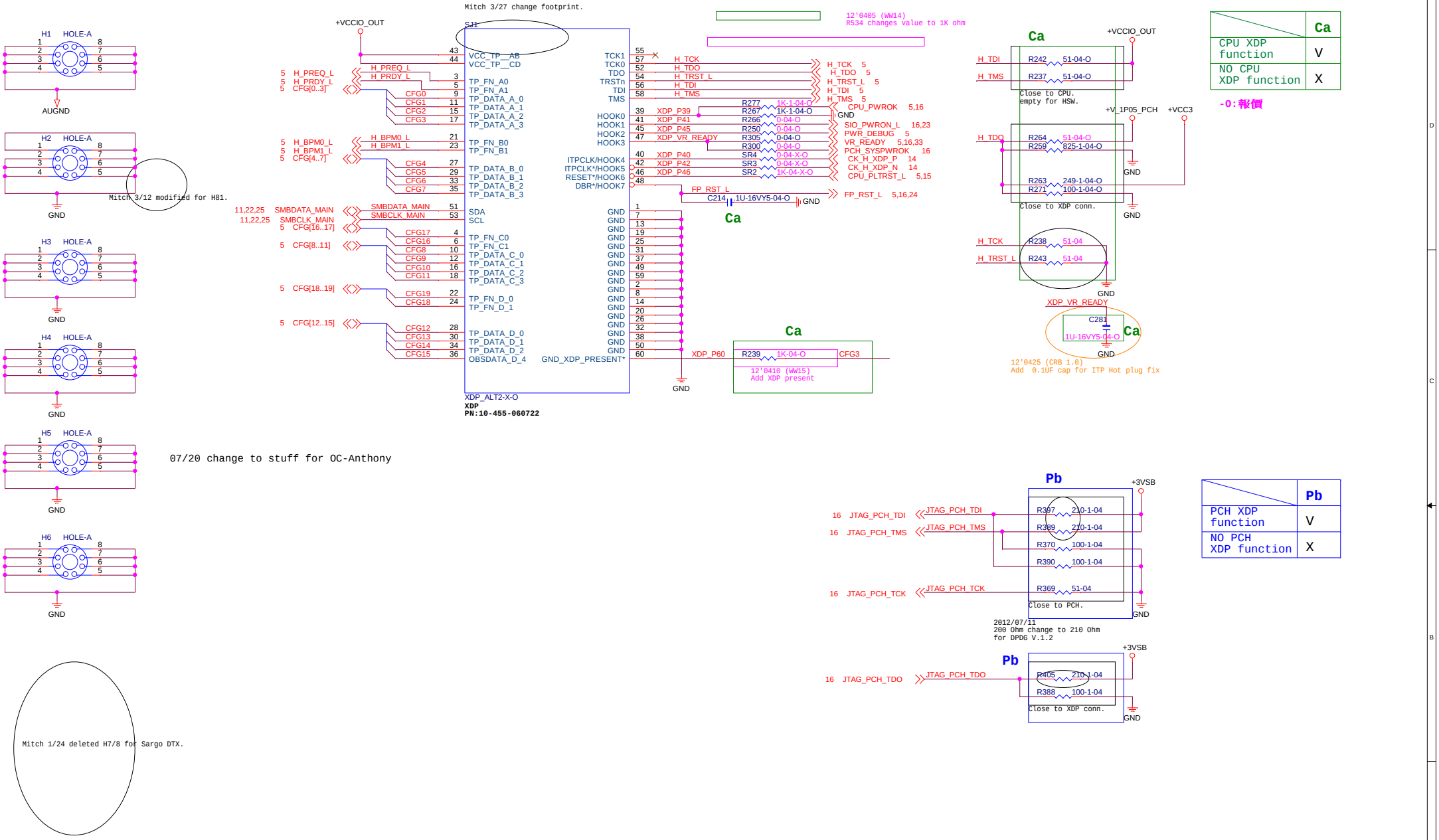








Title	AUDIO-CONN & Header		
Size	Document Number		Rev
Custom	H81H3-AD		1.0
Date:	Friday, June 07, 2013	Sheet 28 of 37	



Title	XDP-CPU/PCH		
Size: Custom	Document Number: H81H3-AD		Rev: 1.0
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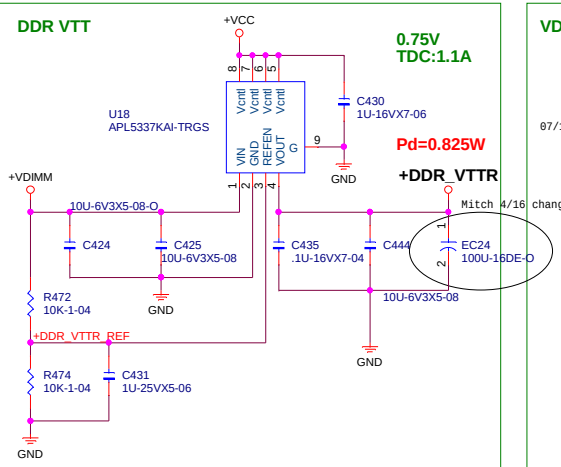
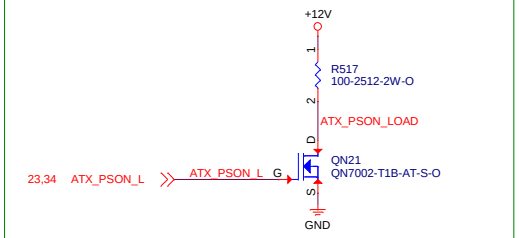
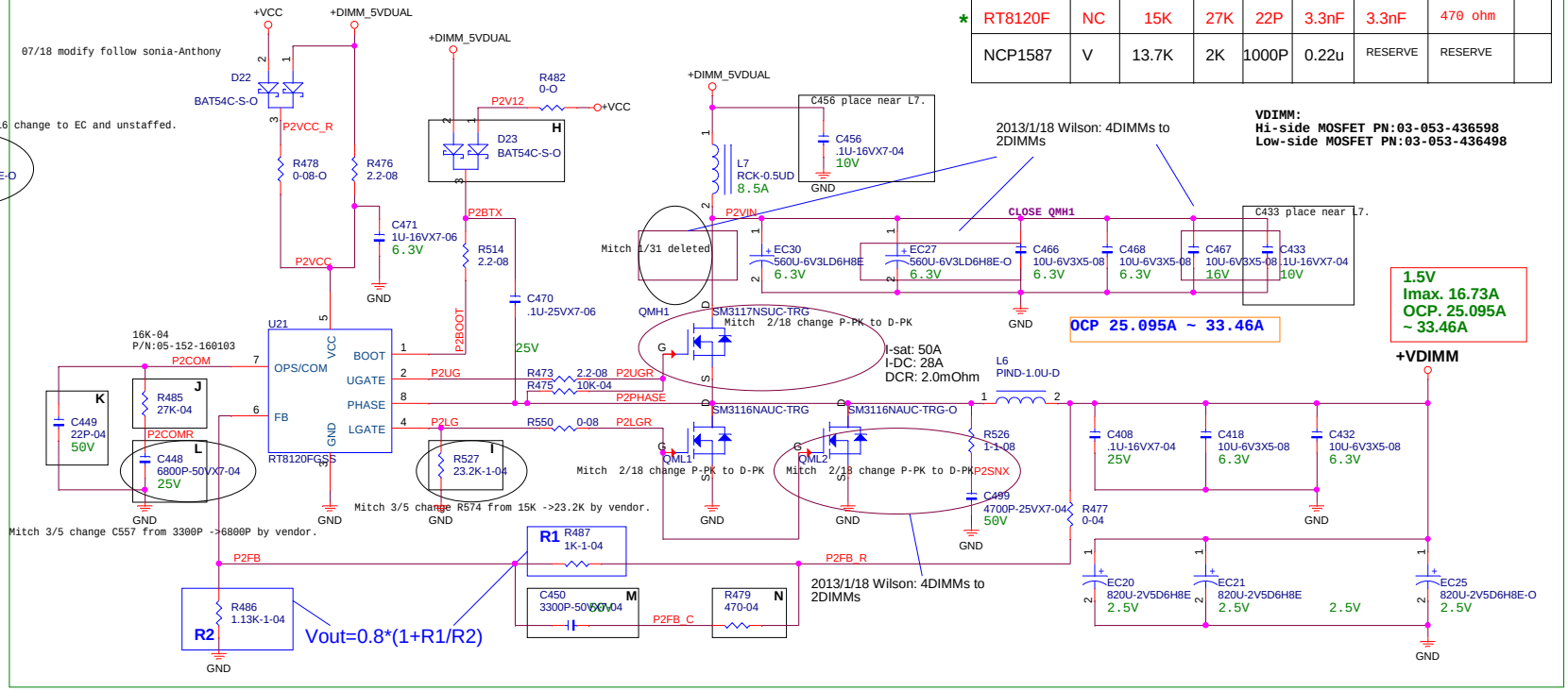
DDR VTT



Dummy Load for ATX power

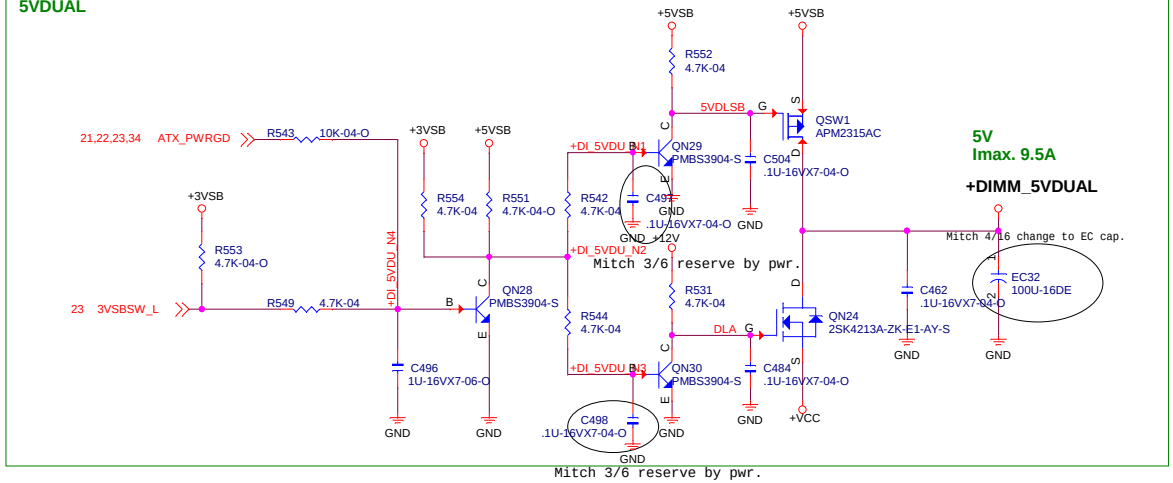


VDIMM



	H	I	J	K	L	M	N	
* RT8120F	NC	15K	27K	22P	3.3nF	3.3nF	470 ohm	
NCP1587	V	13.7K	2K	1000P	0.22u	RESERVE	RESERVE	

5VDUAL



Title	DC/DC VDIMM/DDR_VTT/5VDUAL		
Size: Custom	Document Number: H81H3-AD		Rev: 1.0
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PCH core power

12'0328
update pull-up(change to 1.2K)/pull-down(change to 560 ohm) value
of 1.05PCH's reference voltage.

Power sequence control

+5VSB, +VCC3, R522 10K-04, R502 1K-04, R491 10K-04-O, R492 1K-04, C464 .1U-16VX7-04-O, 5,16,20,21,23 SLP_S3_L, PCH_1P05_N1, QN22 PMBS3904-S, QN23 PMBS3904-S, C479 .1U-16VX7-04-O, PCH_1P05_N2

Mitch 3/6 reserve by pwr.

+3VSB, R508 1.2K-1-04, R509 562-1-04, C473 2.2U-6V3X5-08, Mitch 3/31 change to 0603.

+1P05V_REF, +12V, R484 4.7K-O, U20A GS358SFS, R483 4.7K-04, R495 4.7K-04-O, C461 2200p-04-O, C465 .1U-16VY5-04-O, PCH_1P05_N4, PCH_1P05_N5, +1P05V_FB

12'0328
reserve R to GND

R497 0-04, C460 .1U-16VY5-04-O

+VDIMM, QN20 STD60N3LH5, Pd: 2.7W, C436 .1U-16VX7-04, C447 4.7U-25VX5-08-O, C451 .1U-16VY5-04-O

1.05V
Imax:5.24A(non-include ME power)
Imax:5.91A(include ME power)

+V_1P05_PCH

Mitch 3/6 combined PCH 1.05V power for H81.

C443 22U-6V3X5-08, C442 22U-6V3X5-08, EC26 1000U-6V3LD8H11E

Mitch 3/6 change to EC by power.

CRB:820UF X 1PCS
22UF X 2PCS

PCH DAC power

add 上件

+3VSB, R525 2.2K-04, PCH_1P5_N3, R538 10K-04, SLP_S3_L, 1U-16VX7-04-O, C489, QN25 PMBS3904-S, R548 10K-04, .1U-16VX7-04-O, C505, QN31 PMBS3904-S, PCH_1P5_N1, PCH_1P5_N11

+V_1P05_PCH

R532 20K-04, QN26 QN7002-T1B-AT-S, PCH_1P5_N9, PCH_1P5_N4, R519 0-04

+VREF25, R518 10K-1-04, R520 15K-1-04, C475 2.2U-6V3X5-08, Mitch 3/31 change to 0603.

+1P5V_REF, +12V, R498 4.7K-O, U20B GS358SFS, R499 4.7K-04, C465 2200p-04-O, C474 .1U-16VY5-04-O, PCH_1P5_N8, PCH_1P5_N12, +1P5V_FB

R537 20K-04-O, QN27 APM2306AC-TRG-S-O, PCH_1P5_N10, PCH_1P5_N5, R523 10K-08-O

R521 0-04, C476 .1U-16VY5-04-O

+VCC3, C434 1U-16VX7-06, QN19 APM2306AC-TRG-S, Mitch 3/1 recovery to SOT253.

Mitch 3/4 change Imax from 0.65A to 0.253A.

Pd: 0.46W

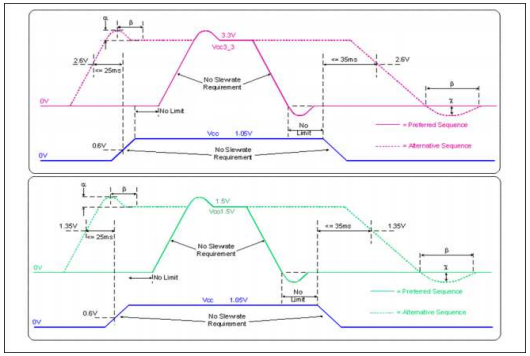
1.5V
Imax:0.253A

+V_1P5_PCH

C422 10U-6V3X5-08, C421 10U-6V3X5-08-O, EC23 100U-16DE

Mitch 13'0218 change one 22uF to 10uF MLCC by power.
reserve one MLCC.

Mitch 3/6 reserve by pwr.



PCH ME power

2013/1/10 Wilson: Del ME POWER circuit

Mitch 3/6 change to +V_1P05_PCH power for H81 ME power.

+V_1P05_PCH

1.05V
Imax:0.67A

C439 22U-6V3X5-08, C441 22U-6V3X5-08, C440 10U-6V3X5-08, C438 1U-16VX7-06-O, C437 .1U-16VY5-04-O

0726 reserve for
Acer review Sonia-Anthony

Title	DC/DC PCH_1.5V/PCH,ME_1.05V		
Size: Custom	Document Number: H81H3-AD		Rev: 1.0
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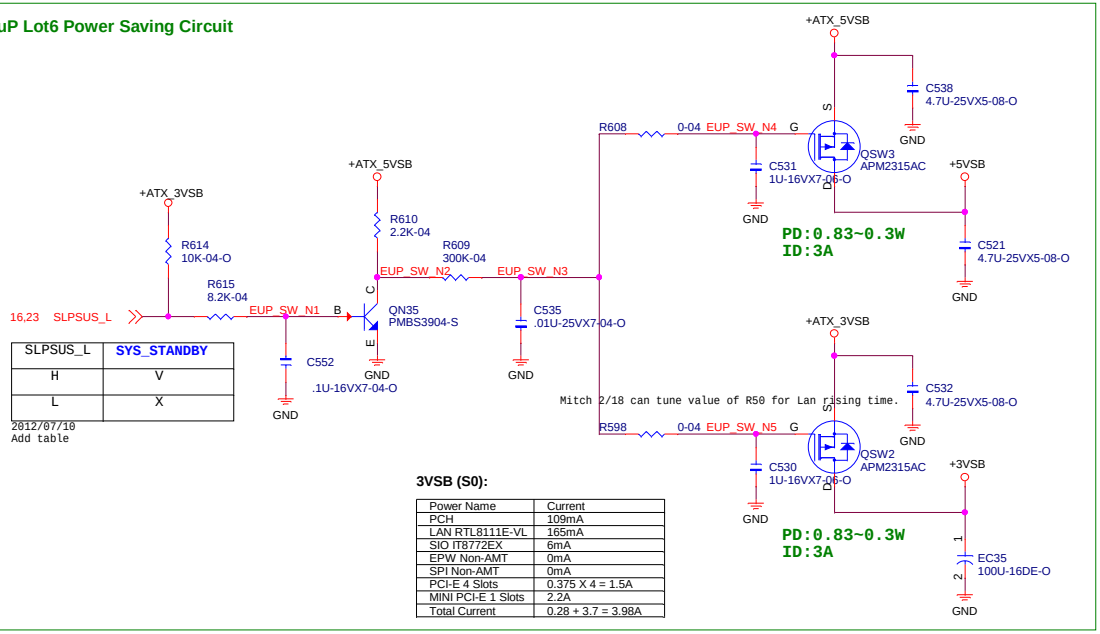
EuP Lot6 Power Saving Circuit



SLPSUS_L	SYS_STANDBY
H	V
L	X

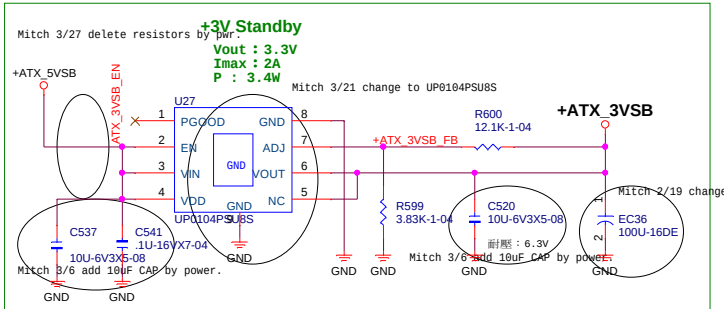
2012/07/10
Add table

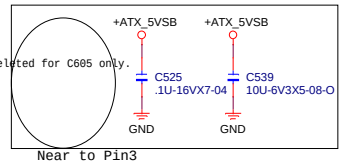
3VSB (S0):

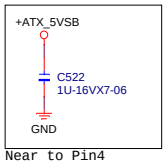
Power Name	Current
PCH	109mA
LAN RTL8111E-VL	165mA
SIO IT8772EX	6mA
EPW Non-AMT	0mA
SPI Non-AMT	0mA
PCI-E 4 Slots	0.375 X 4 = 1.5A
MINI PCI-E 1 Slots	2.2A
Total Current	0.28 + 3.7 = 3.98A

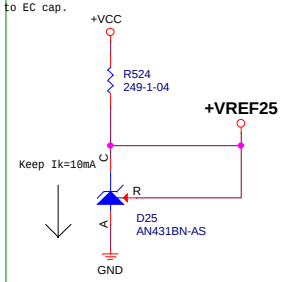
+3V Standby

Vout : 3.3V
Imax : 2A
P : 3.4W

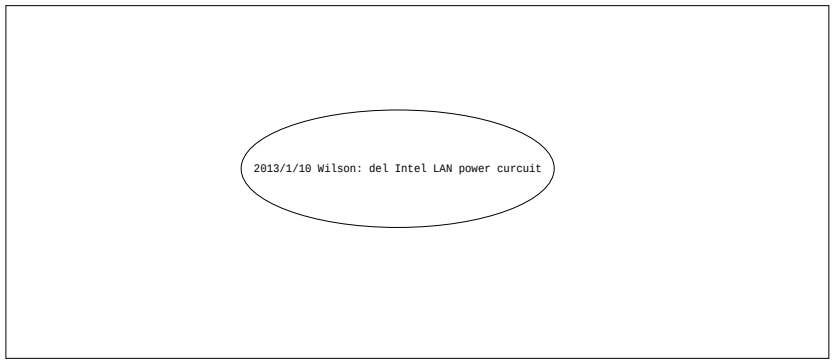


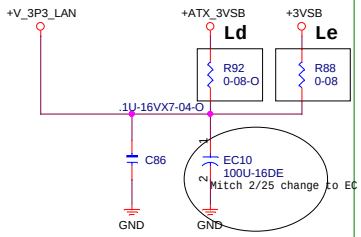






LAN Power Circuit



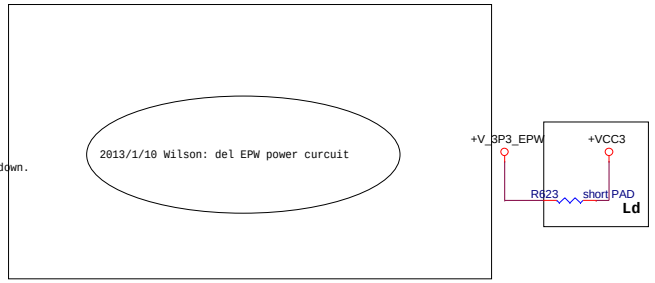


LAN Power Source

	EUP Enable G3-->S5,S5	La	Lb	Lc	Ld	Le
Intel LAN	can wake up	V	V	X		
	can't wake up	V	X	V		
Realtek LAN *	can wake up				V	X
	can't wake up				X	V

del mini

SPI ROM & PCH Power Circuit



+VCC3_EPW	Ld	Le	Lf
Intel LAN	X	V	X
Realtek LAN	V	X	X
Intel LAN(Cost down)	X	X	V

*

Title	DC/DC ATX_3VSB/3VDUAL		
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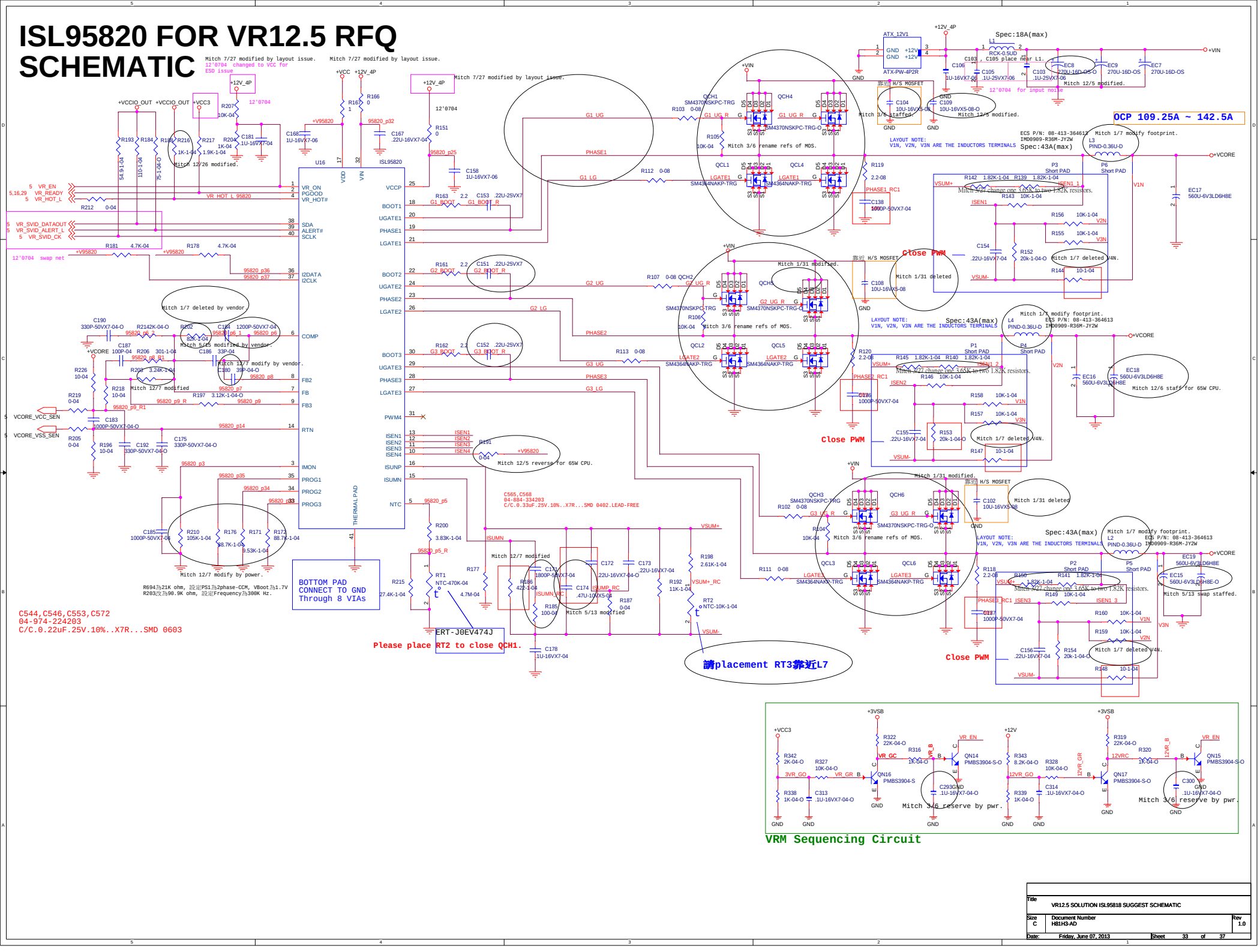
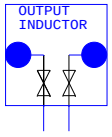
ISL95820 FOR VR12.5 RFQ SCHEMATIC



Mitch 3/21 deleted for multi rail PSU.

SPxx PLACE ON THE SOLDER SIDE, CLOSE INDUCTOR



The Rs1, Rs2 and C can be calculated as:

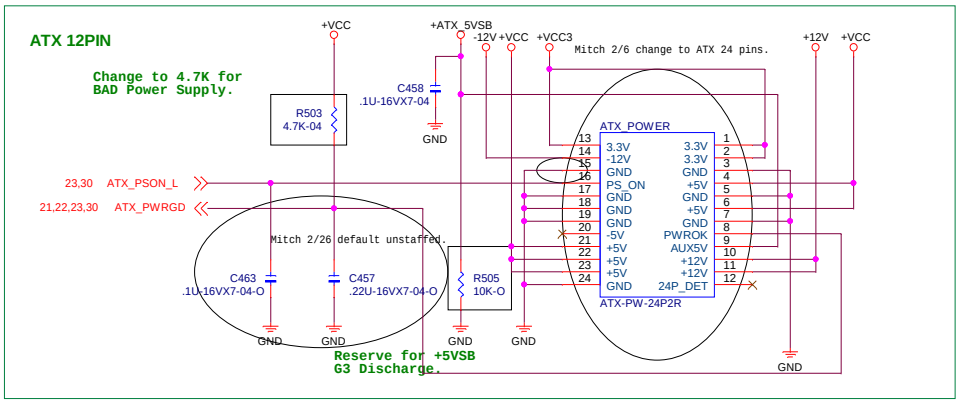
$$C \cdot \left(R_{S1} // R_{S2}\right) = \frac{L}{DCR}$$

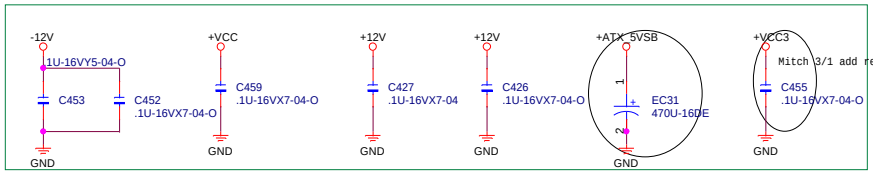
The inductor peak current limit is:

$$I_{LIM(Peak)} = \frac{V_{th\_DC}}{k \cdot DCR}, \text{where } k = \frac{R_{S2}}{R_{S1} + R_{S2}}$$

The DC current limit is:

$$I_{LIM} = I_{LIM(Peak)} - \frac{V_O \cdot (V_{in} - V_O)}{2 \cdot V_{in} \cdot f_{SW} \cdot L}$$





Mitch 5/20 staff for drop issue on S5 to S0.

Title: DC/DC VDIMM/DDR_VTT/5VDUAL		
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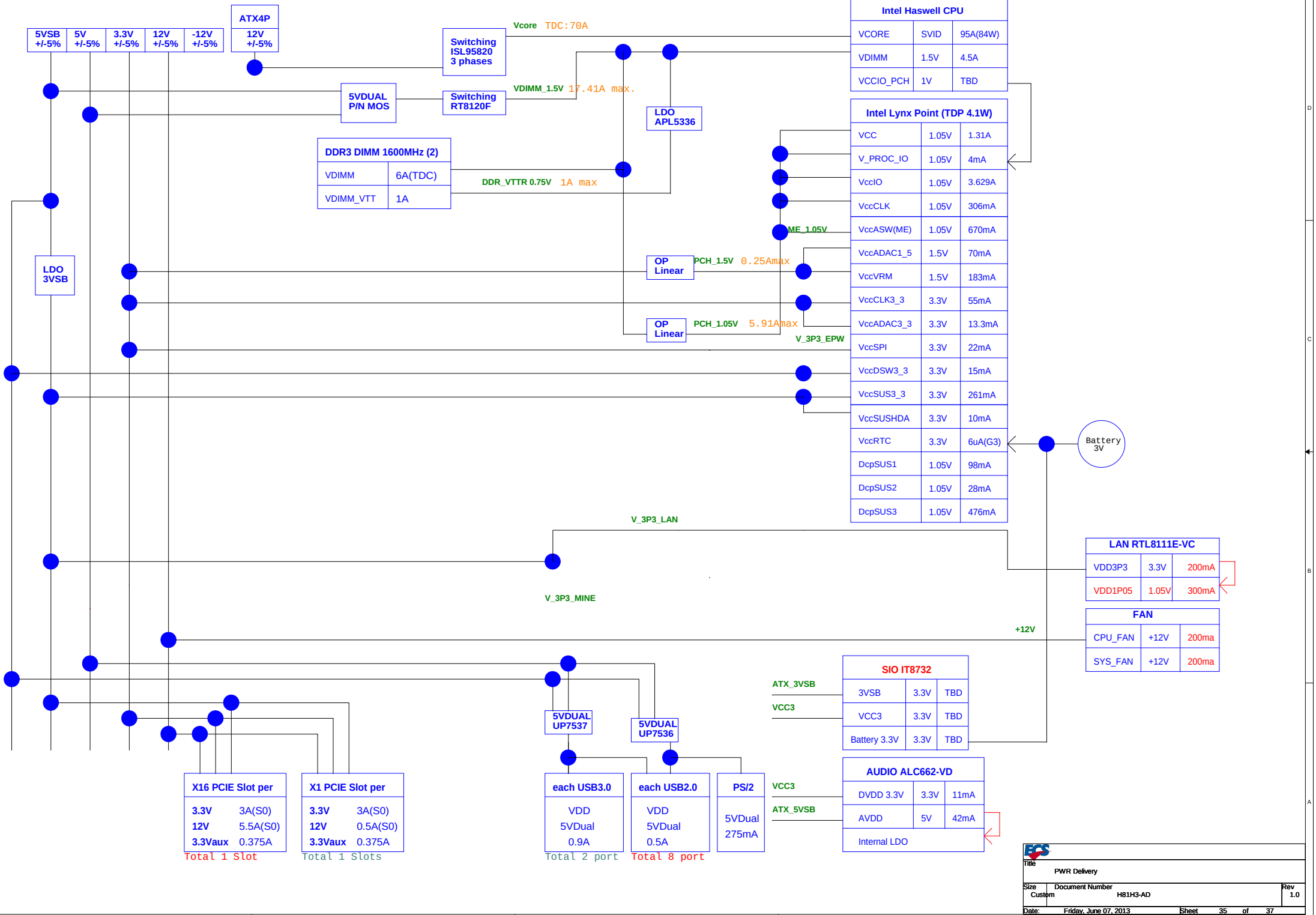
5VSB +/-5%
5V +/-5%
3.3V +/-5%
12V +/-5%
-12V +/-5%
ATX4P
12V +/-5%
Switching ISL95820 3 phases
Vcore TDC:70A
Intel Haswell CPU
VCORE SVID 95A(84W)
VDIMM 1.5V 4.5A
VCCIO_PCH 1V TBD
5VDUAL P/N MOS
Switching RT8120F
VDIMM_1.5V 17.41A max.
LDO APL5336
DDR3 DIMM 1600MHz (2)
VDIMM 6A(TDC)
VDIMM_VTT 1A
DDR_VTTR 0.75V 1A max
Intel Lynx Point (TDP 4.1W)
VCC 1.05V 1.31A
V_PROC_IO 1.05V 4mA
VccIO 1.05V 3.629A
VccCLK 1.05V 306mA
VccASW(ME) 1.05V 670mA
ME_1.05V
VccADAC1_5 1.5V 70mA
VccVRM 1.5V 183mA
VccCLK3_3 3.3V 55mA
VccADAC3_3 3.3V 13.3mA
V_3P3_EPW
VccSPI 3.3V 22mA
VccDSW3_3 3.3V 15mA
VccSUS3_3 3.3V 261mA
VccSUSHDA 3.3V 10mA
VccRTC 3.3V 6uA(G3)
DcpSUS1 1.05V 98mA
DcpSUS2 1.05V 28mA
DcpSUS3 1.05V 476mA
LDO 3VSB
OP Linear
PCH_1.5V 0.25Amax
OP Linear
PCH_1.05V 5.91Amax
Battery 3V
V_3P3_LAN
V_3P3_MINE
LAN RTL8111E-VC
VDD3P3 3.3V 200mA
VDD1P05 1.05V 300mA
FAN
CPU_FAN +12V 200ma
SYS_FAN +12V 200ma
+12V
SIO IT8732
3VSB 3.3V TBD
VCC3 3.3V TBD
Battery 3.3V 3.3V TBD
ATX_3VSB
VCC3
5VDUAL UP7537
5VDUAL UP7536
X16 PCIE Slot per
3.3V 3A(S0)
12V 5.5A(S0)
3.3Vaux 0.375A
Total 1 Slot
X1 PCIE Slot per
3.3V 3A(S0)
12V 0.5A(S0)
3.3Vaux 0.375A
Total 1 Slots
each USB3.0
VDD 5VDual 0.9A
Total 2 port
each USB2.0
VDD 5VDual 0.5A
Total 8 port
PS/2
5VDual 275mA
VCC3
ATX_5VSB
AUDIO ALC662-VD
DVDD 3.3V 3.3V 11mA
AVDD 5V 42mA
Internal LDO
ECS
Title
PWR Delivery
Size Custom
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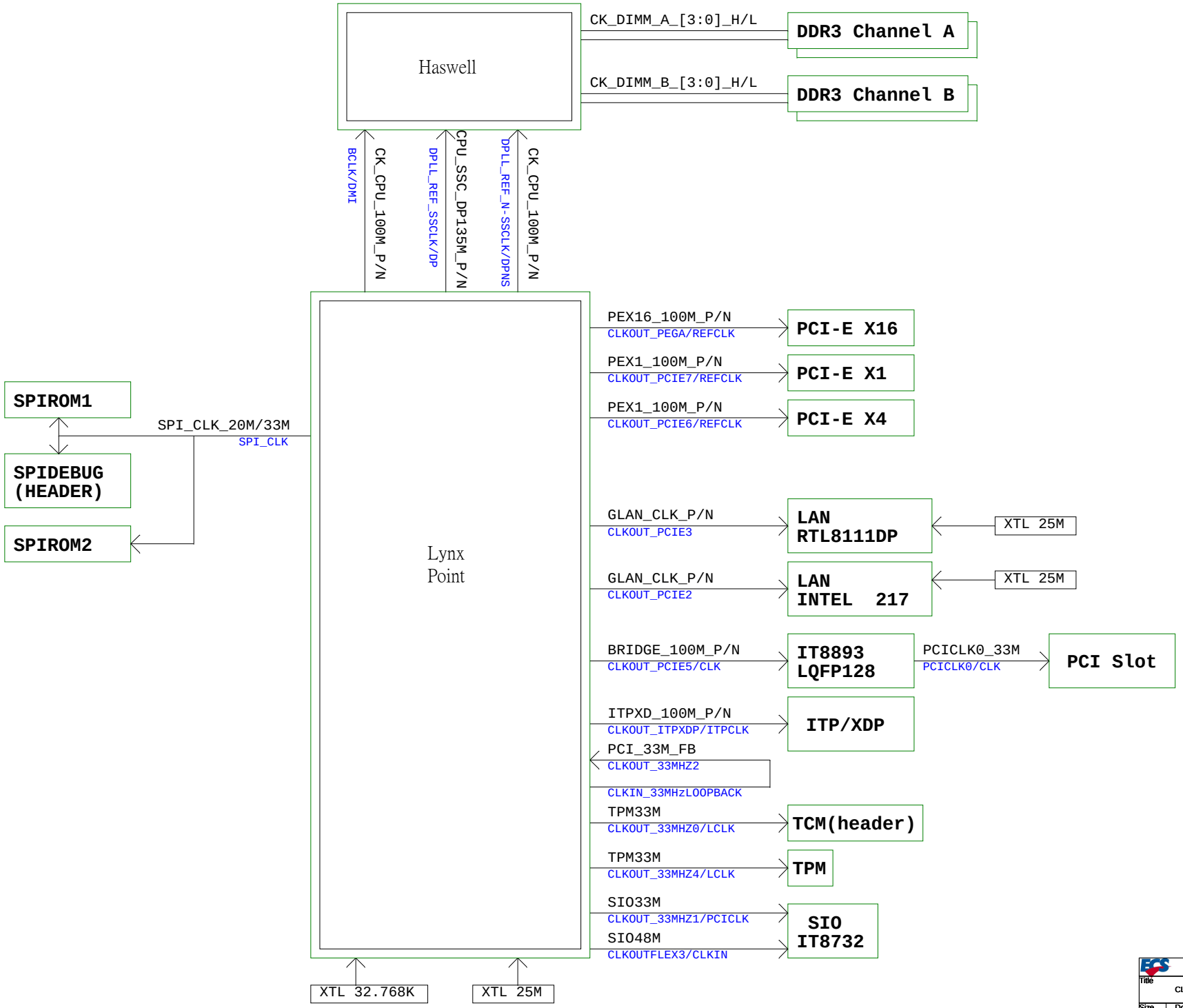

Title	CLK Distribution	
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