Hadley15" Schematics Document

Haswell ULT

2013-06-28
REV : A00

DY : None Installed
UMA: UMA only installed
OPS: Optimus solution installed.
eDP: Support eDP Panel installed.
LVDS: Support LVDS Panel installed.

<Core Design>

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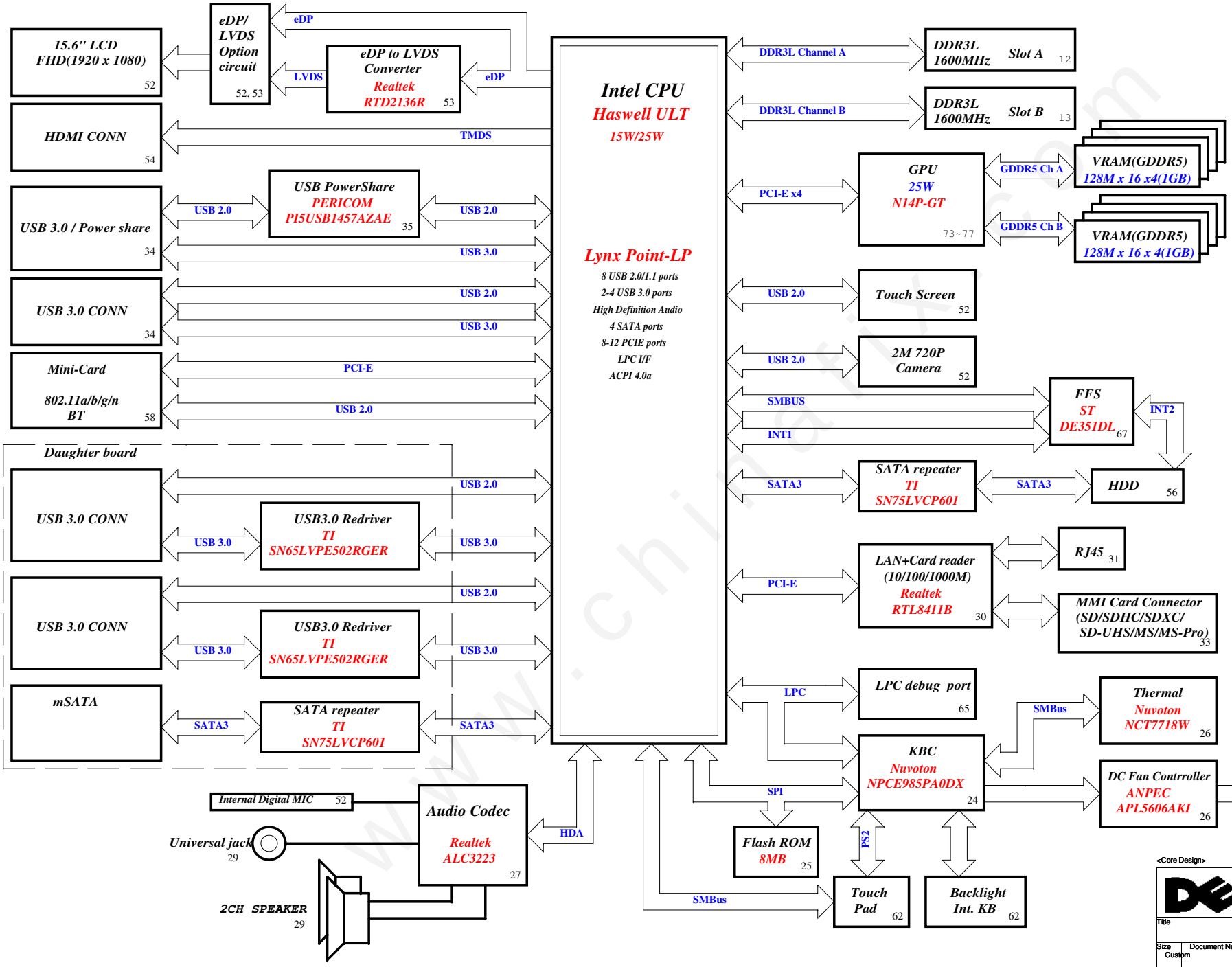
Hadly15 Block Diagram

Project code : 91.47L01.001
PCB P/N : 12311-1
Revision : A00



CHARGER BQ24717 34	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC TPS51225 45	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_CHARGER 3D3V_PWR

CPU DC/DC TPS51622 46~47	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51363 48	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

SYSTEM DC/DC TPS51216 49	
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D675V_S0

SYSTEM DC/DC NCP81172 82	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

Switches 36, 83	
INPUTS	OUTPUTS
5V_S5 3D3V_S5 3D3V_S0 1D05V_S0 1D35V_S3	5V_S0 3D3V_S0 3D3V_VGA_S0 1D05V_VGA_S0 1D35V_VGA_S0

LDO TLV70215DBVR 51	
INPUTS	OUTPUTS
3D3V_S5	

PCB LAYER
L1 : TOP
L2 : GND
L3 : Signal
L4 : Signal
L5 : VCC
L6 : Signal
L7 : GND
L8 : Bottom

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Title: *(Reserved)*

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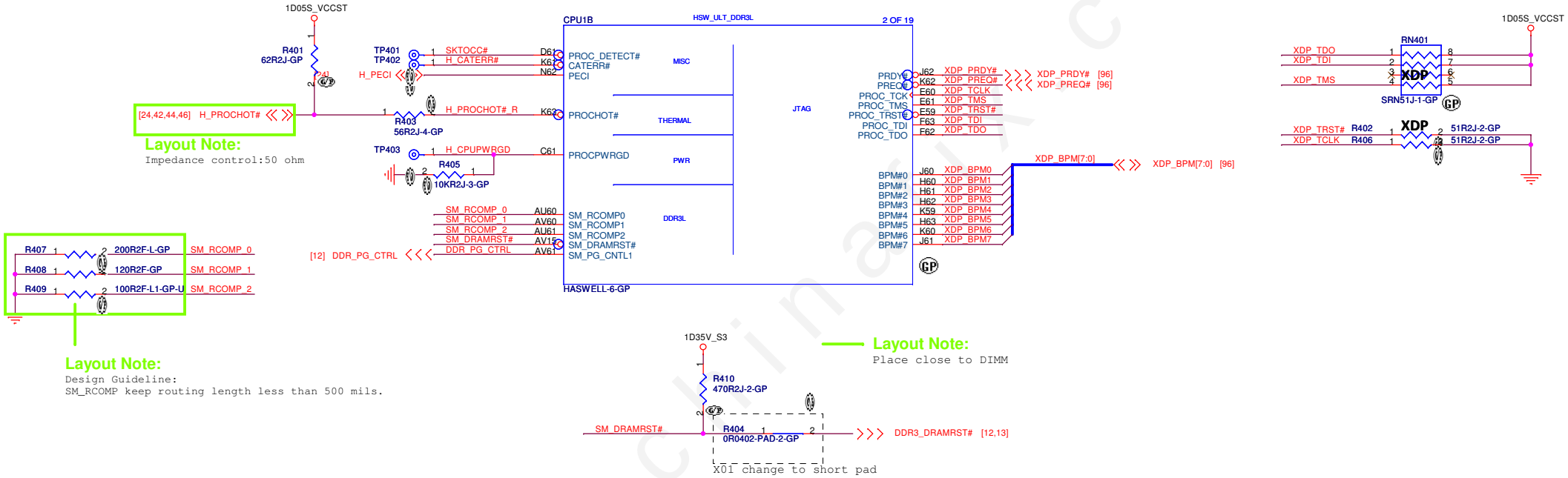
SSID = CPU



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Title: CPU (THERMAL/CLOCK)

Size	Document Number	Rev
A3	Hadley 15"	X02

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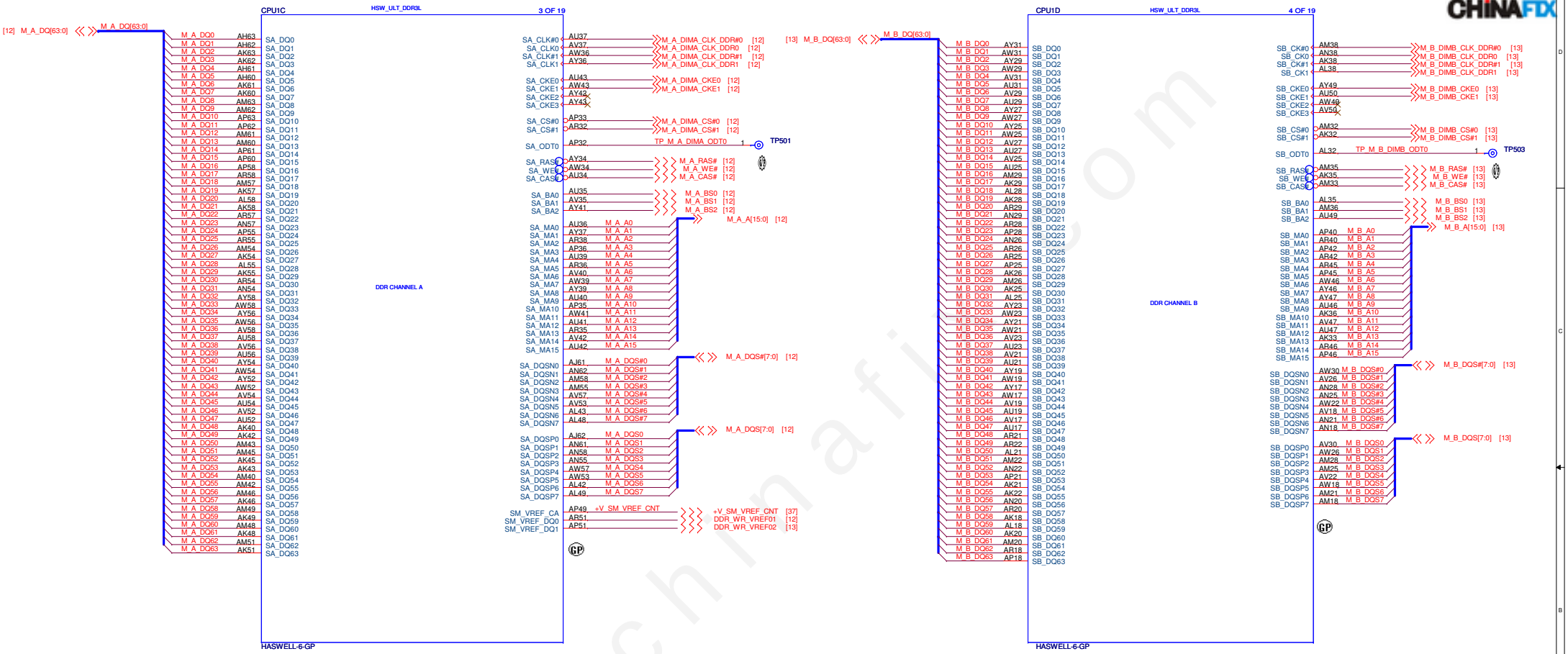
SSID = CPU



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Title: CPU (DDR)

Size	Document Number	Rev
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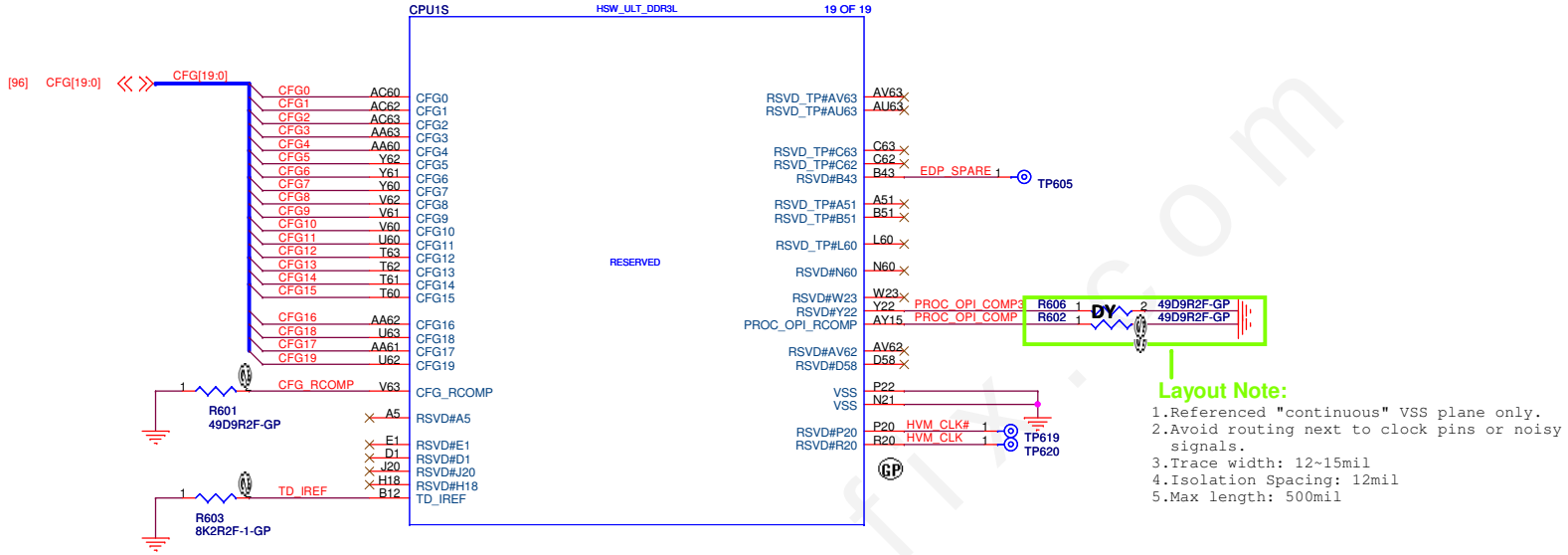
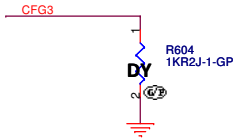
SSID = CPU

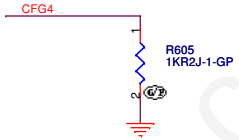


Layout Note:

1.Referenced "continuous" VSS plane only.
2.Avoid routing next to clock pins or noisy signals.
3.Trace width: 12~15mil
4.Isolation Spacing: 12mil
5.Max length: 500mil



PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED



DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT 1 : DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

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Title: CPU (RESERVED)

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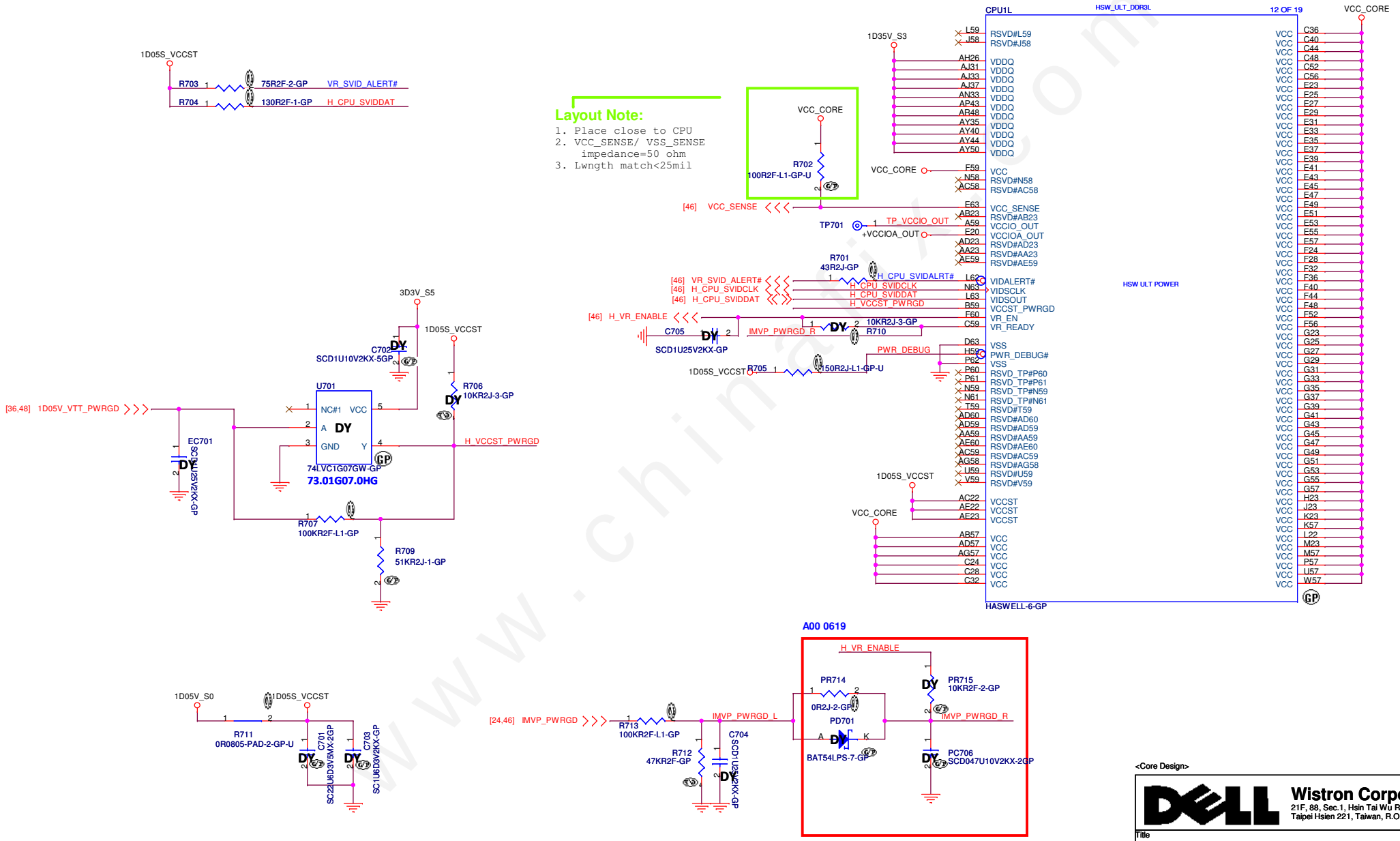
SSID = CPU



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Title: CPU (VCC_CORE)

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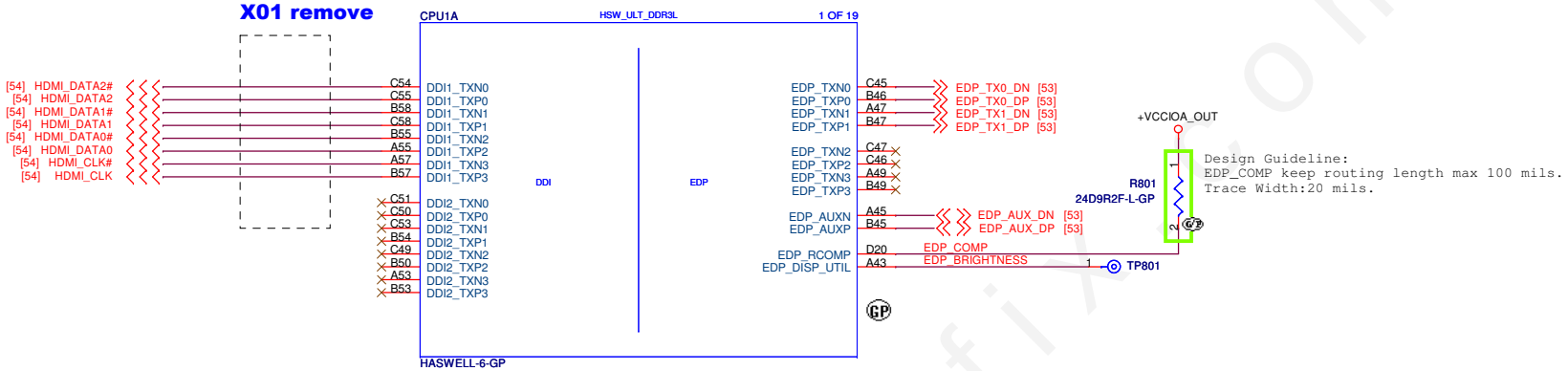
SSID = CPU

HDMI

X01 remove



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Title: CPU (DDI/EDP)

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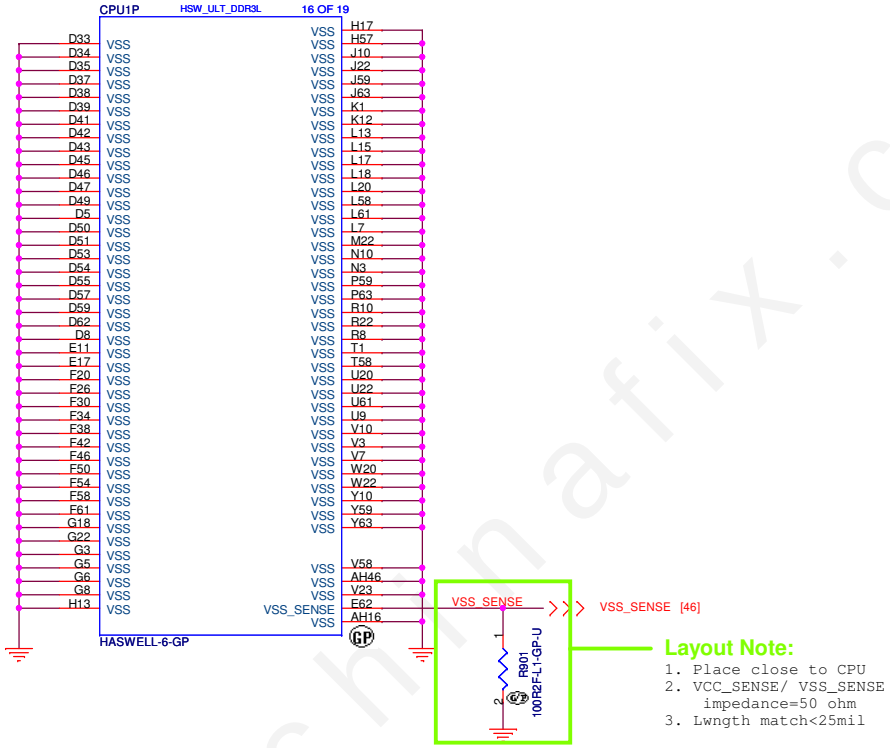
SSID = CPU



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Title: CPU (VSS)

Size: A3 | Document Number: Hadley 15" | Rev: X02

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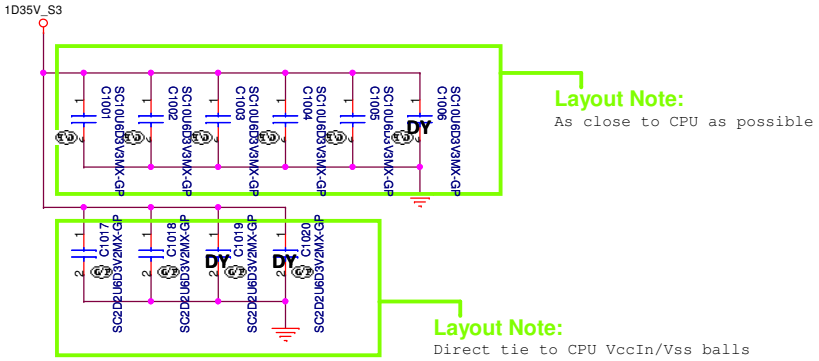
SSID = CPU



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Title: CPU(Power CAP1)

Size: A3 | Document Number: Hadley 15" | Rev: X02

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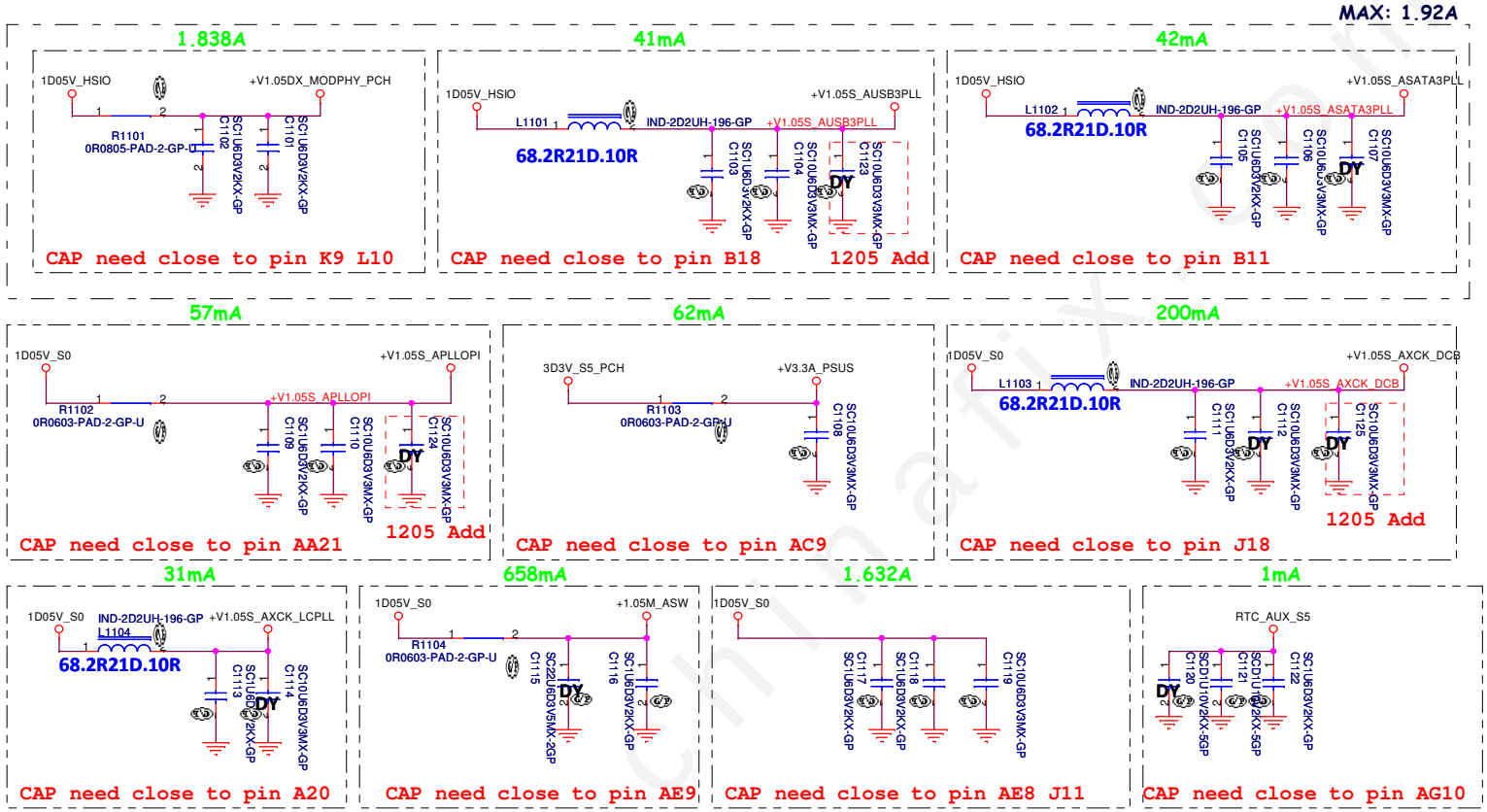
SSID = CPU



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Title: CPU(Power CAP2)

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SSID = MEMORY

Note:
SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

Layout Note:
Place these caps close to VREF_CA

Layout Note:
Place these caps close to VREF_DQ

Layout Note:
Place these caps close to VTT1 and VTT2.

Layout Note:
All VREF traces should have width=20mil; spacing=20 mil

Layout Note:
Place Close SO-DIMMA.

Layout Note:
Place these Caps near SO-DIMMA.

X01 change to short pad

Q1201 Need check Vth=1V

84.05067.031

DDR3-204P-122-GP-U1

62.10017.Z51

close to dimm

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Title: DDR3L-SODIMM1

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SSID = MEMORY

CHINAFDX

DM2

M_B_A[15:0] [5]

[5] M_B_BS2
[5] M_B_BS0
[5] M_B_BS1
[5] M_B_DQ[63:0]

M_B_A0 M_B_A1 M_B_A2 M_B_A3 M_B_A4 M_B_A5 M_B_A6 M_B_A7 M_B_A8 M_B_A9 M_B_A10 M_B_A11 M_B_A12 M_B_A13 M_B_A14 M_B_A15

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12 A13 A14 A15 A16/BA2 BA0 BA1

M_B_DQ8 M_B_DQ14 M_B_DQ10 M_B_DQ11 M_B_DQ12 M_B_DQ9 M_B_DQ13 M_B_DQ15 M_B_DQ28 M_B_DQ29 M_B_DQ26 M_B_DQ27 M_B_DQ25 M_B_DQ24 M_B_DQ30 M_B_DQ31 M_B_DQ40 M_B_DQ41 M_B_DQ46 M_B_DQ42 M_B_DQ45 M_B_DQ44 M_B_DQ47 M_B_DQ43 M_B_DQ56 M_B_DQ57 M_B_DQ59 M_B_DQ58 M_B_DQ61 M_B_DQ60 M_B_DQ63 M_B_DQ62 M_B_DQ4 M_B_DQ1 M_B_DQ3 M_B_DQ7 M_B_DQ5 M_B_DQ0 M_B_DQ2 M_B_DQ6 M_B_DQ21 M_B_DQ20 M_B_DQ22 M_B_DQ23 M_B_DQ16 M_B_DQ17 M_B_DQ19 M_B_DQ18 M_B_DQ36 M_B_DQ33 M_B_DQ35 M_B_DQ39 M_B_DQ37 M_B_DQ32 M_B_DQ34 M_B_DQ38 M_B_DQ52 M_B_DQ49 M_B_DQ48 M_B_DQ53 M_B_DQ51 M_B_DQ55 M_B_DQ54 M_B_DQ50

DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31 DQ32 DQ33 DQ34 DQ35 DQ36 DQ37 DQ38 DQ39 DQ40 DQ41 DQ42 DQ43 DQ44 DQ45 DQ46 DQ47 DQ48 DQ49 DQ50 DQ51 DQ52 DQ53 DQ54 DQ55 DQ56 DQ57 DQ58 DQ59 DQ60 DQ61 DQ62 DQ63

M_B_DQS#1 M_B_DQS#3 M_B_DQS#5 M_B_DQS#7 M_B_DQS#0 M_B_DQS#2 M_B_DQS#4 M_B_DQS#6

DQS0# DQS1# DQS2# DQS3# DQS4# DQS5# DQS6# DQS7#

M_B_DQS#[7:0] [5]

M_B_DQS1 M_B_DQS3 M_B_DQS5 M_B_DQS7 M_B_DQS0 M_B_DQS2 M_B_DQS4 M_B_DQS6

DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7

M_B_DQS[7:0] [5]

[12] M_B_DIMB_ODT0
[12] M_B_DIMB_ODT1

ODT0 ODT1

M_VREF_CA_DIMMB
M_VREF_DQ_DIMMB

VREF_CA VREF_DQ

[4,12] DDR3_DRAMRST#

RESET#

0D675V_S0

VTT1 VTT2

SKT_DDR_204P_SMD

DDR3-204P-122-GP-U1

62.10017.Z51

M_B_RAS# [5]
M_B_WE# [5]
M_B_CAS# [5]

RAS# WE# CAS#

M_B_DIMB_CS#0 [5]
M_B_DIMB_CS#1 [5]

CS0# CS1#

M_B_DIMB_CKE0 [5]
M_B_DIMB_CKE1 [5]

CKE0 CKE1

M_B_DIMB_CLK_DDR0 [5]
M_B_DIMB_CLK_DDR#0 [5]

CK0 CK0#

M_B_DIMB_CLK_DDR1 [5]
M_B_DIMB_CLK_DDR#1 [5]

CK1 CK1#

DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7

PCH_SMBDATA [12,18,58,62,67]
PCH_SMBCLK [12,18,58,62,67]

SDA SCL

EVENT#

VDDSPD

SA0_DIMB
SA1_DIMB

SA0 SA1

NC#1 NC#2 NC#/TEST

1D35V_S3

VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 VDD9 VDD10 VDD11 VDD12 VDD13 VDD14 VDD15 VDD16 VDD17 VDD18

VSS

3D3V_S0

R1301 10KR2J-3-GP

SA1_DIMB
SA0_DIMB

R1302 0R0402-PAD-2-GP

C1303 SCD1U10V2KX-5GP

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

M_VREF_CA_DIMMB

C1301 SCD1U10V2KX-5GP
EC1302 SCD1U10V2KX-5GP
C1302 SCD1U10V2KX-5GP

Layout Note:
Place these caps close to VREF_CA

M_VREF_DQ_DIMMB

C1305 SC2D2U6D3V2MX-GP
C1304 SCD1U10V2KX-5GP
C1306 SCD1U10V2KX-5GP

Layout Note:
Place these caps close to VREF_DQ

0D675V_S0

C1316 SC1U6D3V2KX-GP
C1317 SC1U6D3V2KX-GP
C1318 SC1U6D3V2KX-GP

Layout Note:
Place these caps close to VTT1 and VTT2.

Layout Note:
All VREF traces should have width=20mil; spacing=20 mil

C1319 SCD1U10V2KX-5GP

close to dimm

1D35V_S3

C1312 SC1U10V6A3VMX-GP
C1311 SC1U10V6A3VMX-GP
C1310 SC1U10V6A3VMX-GP
C1309 SC1U10V6A3VMX-GP
C1308 SC1U6D3V3MX-GP
C1307 SC1U6D3V3MX-GP

C1313 SCD1U10V2KX-5GP
C1314 SCD1U10V2KX-5GP
C1315
EC1301 SCD1U10V2KX-5GP

Layout Note:
Place these Caps near SO-DIMMA.

Layout Note:
Place Close SO-DIMMA.

[5] DDR_WR_VREF02

0D675V_VTTREF 1D35V_S3

R1308 0R2J-2-GP
R1306 1K8R2F-GP
2R2F-GP R1304
R1303 1K8R2F-GP
M_VREF_DQ_DIMMB
C1320 SCD022U16V2JX-GP
+V_VREF_PATH2
R1307 24D9R2F-L-GP

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Title: DDR3L-SODIMM2

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Title: M1&M3

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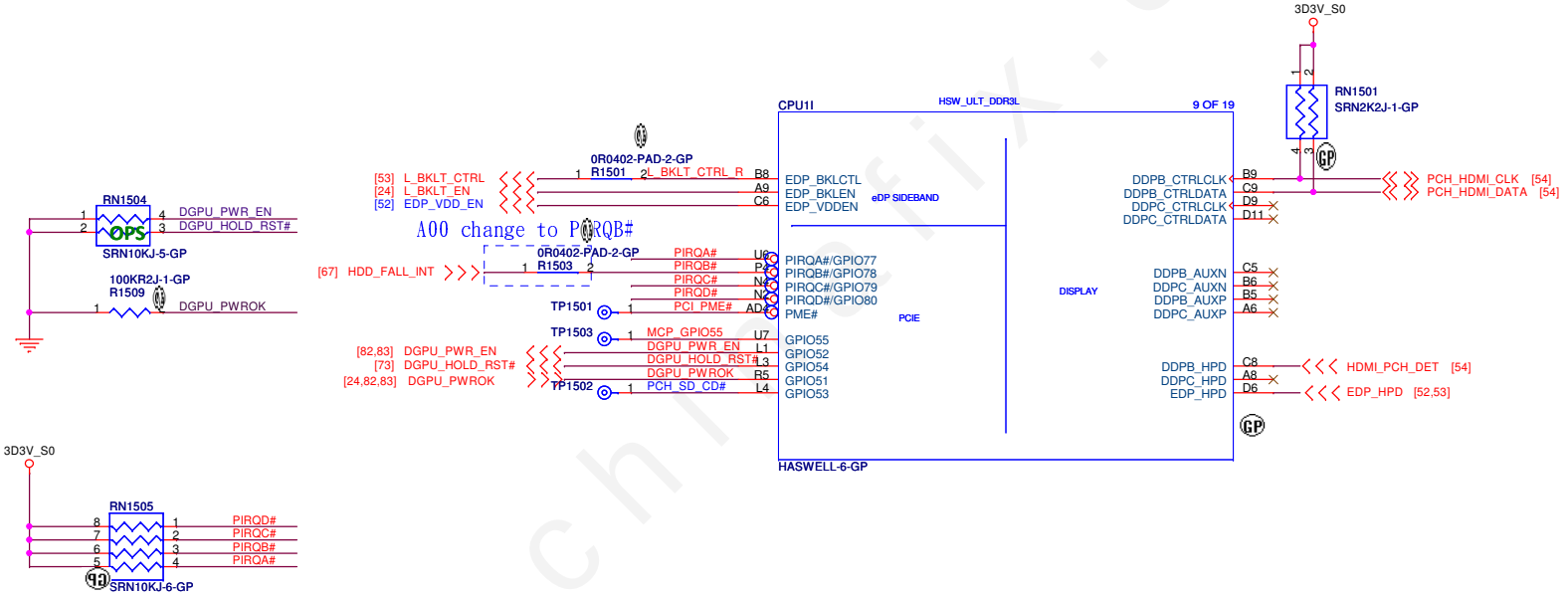
SSID = CPU



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Title: CPU (EDP SIDEBAND/GPIO/DDI)

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SSID = CPU

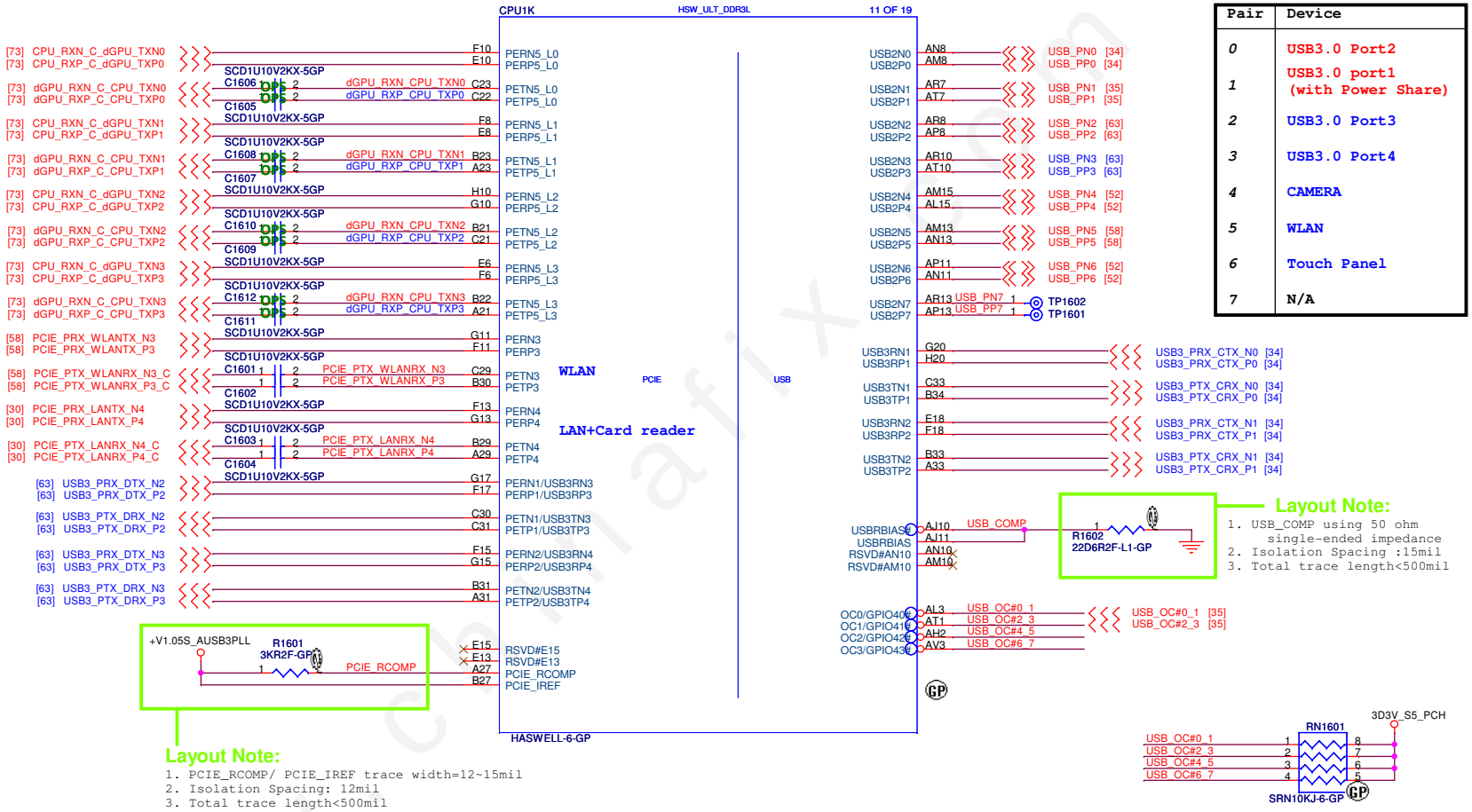
CHINAFDX

PCIE Table

Port	Device	Share BUS
1	N/A	USB3.0_3
2	N/A	USB3.0_4
3	WLAN	
4	LAN+ Card reader	
5(4lane)	GPU	
6(4lane)	N/A	SATA0~3

USB 2.0 Table

Pair	Device
0	USB3.0 Port2
1	USB3.0 port1 (with Power Share)
2	USB3.0 Port3
3	USB3.0 Port4
4	CAMERA
5	WLAN
6	Touch Panel
7	N/A



Layout Note:

1. PCIE_RCOMP/ PCIE_IREF trace width=12~15mil
2. Isolation Spacing: 12mil
3. Total trace length<500mil

Layout Note:

1. USB_COMP using 50 ohm single-ended impedance
2. Isolation Spacing :15mil
3. Total trace length<500mil

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Title	CPU (PCIE/USB)	
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SSID = CPU

On Die DSW VR Enable	
DSWODVREN	Low = Disable High = Enable (default) ★

DSWODVREN — R1720 330KR2J-L1-GP (RTC_AUX_S5) — DY — R1721 330KR2J-L1-GP

RN1703 SRN10KJ-5-GP: PM_RSMRST#, PM_PCH_PWROK, SYS_PWROK — R1717 DY 10KR2J-3-GP

3D3V_S0 — RN1704 SRN8K2J-3-GP (GP): XDP_DBRESET#, PM_CLKRUN#

CPU1H — HSW_ULT_DDR3L — 8 OF 19 — SYSTEM POWER MANAGEMENT

[24,96] SYS_PWROK
[24,26,36] PCH_PWROK
R1706 0R0402-PAD-2-GP
R1707 0R0402-PAD-2-GP
PM_SUSACK# AK2 → SUSACK#
XDP_DBRESET# AC2 → SYS_RESET#
SYS_PWROK AG2 → SYS_PWROK
PM_PCH_PWROK AY7 → PCH_PWROK
MPWROK AB5 → APWROK
PCI_PLTRST# AG7 → PLTRST#

PM_RSMRST# AW8 → RSMRST#
PM_SUSWARN# AV8 → SUSWARN#/SUSPWRDNACK#/GPIO30
PM_PWRBTN# AL → PWRBTN#
AC_PRESENT AJ8 → ACPRESENT/GPIO31
BATLOW# AN4 → BATLOW#/GPIO72
PCH_SLP_S0# AE2 → SLP_S0#
PCH_SLP_WLAN# AM5 → SLP_WLAN#/GPIO29

[24,96] PM_PWRBTN#
[24,76] AC_PRESENT
[48] PCH_SLP_S0#
TP1705 0R0402-PAD-2-GP

[24,30,58,65,73] PLT_RST# — R1713 — PCI_PLTRST#
R1715 100KR2J-1-GP DY — C1701 SC220P50V2KX-3GP DY

DSWVRMEN AW7 → DSWODVREN
DPWROK AV5 → PCH_DPWROK
WAKE# AJ5 → PCH_WAKE# — R1703 — PM_RSMRST# — 3D3V_S5

NON DS3
R1704 0R2J-2-GP — R1709 0R0402-PAD-2-GP — A00 0618
0311 PCH WAKE# pin PH 1K

CLKRUN#/GPIO32 V5 → PM_CLKRUN# — PM_CLKRUN#_EC [24]
SUS_STAT#/GPIO61 AG4 → PM_SUS_STAT# — TP1702
SUSCLK/GPIO62 AE6 → SUS_CLK — R1710 0R0402-PAD-2-GP — PCH_SUSCLK_KBC [24]
SLP_S5#/GPIO63 AP5 → PM_SLP_S5# — TP1703

SLP_S4# AJ6 → PM_SLP_S4# — PM_SLP_S4# [24,49]
SLP_S3# AT4 → PM_SLP_S3# — PM_SLP_S3# [24,36,48,49,51]
SLP_A# AL5 → PM_SLP_A# — TP1704
SLP_SUS# AP4 → PM_SLP_SUS# — PM_SLP_SUS# [24,38]
SLP_LAN# AJ7 → PM_SLP_LAN# — TP1707

HASWELL-6-GP

3D3V_S5 — RN1701 SRN10KJ-5-GP: BATLOW#, AC_PRESENT

[24] PM_SUSACK#
[24] PM_SUSWARN#
A00 0618 — RN1702 0R4P2R-PAD: PM_SUSACK#_R, PM_SUSWARN#_R

A00 0618
PCH_DPWROK — R1718 0R0402-PAD-2-GP — KBC_DPWROK [24]
R1725 100KR2F-L1-GP DS3

3D3V_AUX_S5 — NON DS3 — R1708 100KR2J-1-GP — R1726 10KR2J-3-GP

Q1701 2N7002KDW-GP
3V_5V_POK# — 3V_5V_POK
PM_RSMRST# — R1702 1KR2J-1-GP — RSMRST#_KBC [24]
3V_5V_POK — R1728 0R2J-2-GP — 3V_5V_POK [45]
NON DS3 — R1729 0R0402-PAD-2-GP — PM_SLP_SUS#
A00 0618

PCH_SUSCLK_KBC — EC1701 SC4D7P50V2CN-1GP DY

3D3V_S5_PCH — R1724 DY 10KR2J-3-GP — PM_SUS_STAT#
R1727 10KR2J-3-GP — PM_SUSWARN#

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Title		
CPU (PM)		
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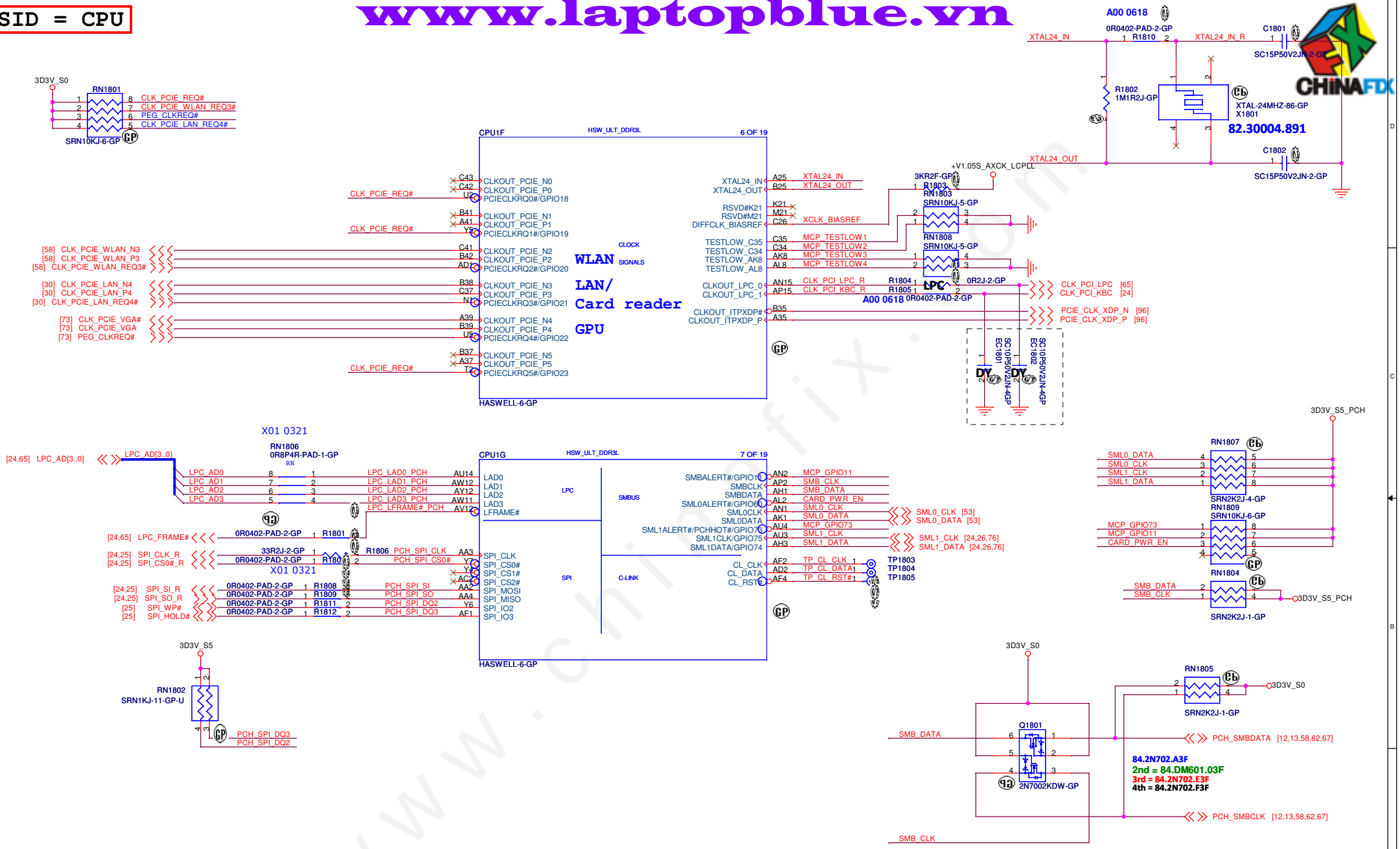

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CLK/SMB/LPC/SPI)

Size	Document Number	Rev
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X02 0502 change C1903 C1904 from 18pF to 15 pF

RTC_X1 RTC_X2 R1915 10MR2J-L-GP X1901 X-32D768KHZ-65-GP C1903 SC15P50V2JN-2-GP C1904 SC15P50V2JN-2-GP

82.30001.A41
2nd = 82.30001.841

RTC_AUX_S5 R1903 330KR2J-L1-GP R1901 1M1R2J-GP RN1901 SRN20KJ-1-GP

[24] RTCRST_ON Q1901 2N7002K-2-GP R1902 10KR2J-3-GP C1901 SC1U6D3V2KX-GP G1901 GAP-OPEN C1902 SC1U6D3V2KX-GP

84.2N702.J31
2ND = 84.2N702.031
3rd = 84.07002.I31

CPU1E HSW_ULT_DDR3L 5 OF 19

RTC_X1 RTC_X2 SM_INTRUDER# PCH_INTVRMEN SRTC_RST# RTC_RST#

AW5 RTCX1
AY5 RTCX2
AU8 INTRUDER#
AV7 INTVRMEN
AV8 SRTCRST#
AU7 RTCRST#

RTC

HDA_BITCLK HDA_SYNC HDA_RST# HDA_SDIN0 HDA_SDOUT TP_HDA_DOCK_EN#

AW8 HDA_BCLK/I2S0_SCLK
AV11 HDA_SYNC/I2S0_SFRM
AU9 HDA_RST#/I2S_MCLK#
AY10 HDA_SDI0/I2S0_RXD
AU12 HDA_SDI1/I2S1_RXD
AU11 HDA_SDO/I2S0_TXD
AW10 HDA_DOCK_EN#/I2S1_TXD#
AV10 HDA_DOCK_RST#/I2S1_SFRM#
AY8 I2S1_SCLK

AUDIO

[27] HDA_SDIN0 TP1902

[27] HDA_CODEC_BITCLK R1907 33R2J-2-GP HDA_BITCLK

TP1901 PCH_JTAG_TRST# PCH_JTAG_TCK PCH_JTAG_TDI PCH_JTAG_TDO PCH_JTAG_TMS XDP_TCK_JTAGX

AU62 PCH_TRST#
AE62 PCH_TCK
AD61 PCH_TDI
AE61 PCH_TDO
AD62 PCH_TMS
AL11 RSVD#AL11
AC4 RSVD#AC4
AE63 JTAGX
AV2 RSVD#AV2

JTAG

[27] HDA_CODEC_SYNC R1905 0R0402-PAD-2-GP HDA_SYNC
[27,29] HDA_CODEC_RST# R1908 0R0402-PAD-2-GP HDA_RST#
[27] HDA_CODEC_SDOUT R1910 0R0402-PAD-2-GP HDA_SDOUT
[24] ME_UNLOCK R1909 1KR2J-1-GP

SATA_RN0/PERN6_L3 SATA_RP0/PERP6_L3 SATA_TN0/PETN6_L3 SATA_TP0/PETP6_L3
SATA_RN1/PERN6_L2 SATA_RP1/PERP6_L2 SATA_TN1/PETN6_L2 SATA_TP1/PETP6_L2
SATA_RN2/PERN6_L1 SATA_RP2/PERP6_L1 SATA_TN2/PETN6_L1 SATA_TP2/PETP6_L1
SATA_RN3/PERN6_L0 SATA_RP3/PERP6_L0 SATA_TN3/PETN6_L0 SATA_TP3/PETP6_L0

SATA

J5 H5 B15 A15 SATA3_PRX_DTX_N0 [56] SATA3_PRX_DTX_P0 [56] SATA3_PTX_DRX_N0 [56] SATA3_PTX_DRX_P0 [56]

HDD1

J8 H8 A17 B17 SATA3_PRX_DTX_N1 [63] SATA3_PRX_DTX_P1 [63] SATA3_PTX_DRX_N1 [63] SATA3_PTX_DRX_P1 [63]

mSATA

J6 H6 B14 C15
F5 E5 C17 D17

V1 EC_SMI# EC_SMI# [24]
U1 MCP_GPIO35
V6 SATA_ODD_PRSNT#
AC1 MSATA_DET# [63]
A12 SATA_IREF
L11
K10
C12 SATA_RCOMP
U3 SATA_LED# SATA_LED# [61]

SATA0GP/GPIO34 SATA1GP/GPIO35 SATA2GP/GPIO36 SATA3GP/GPIO37 SATA_IREF RSVD#L11 RSVD#K10 SATA_RCOMP SATALED#

+V1.05S_ASATA3PLL

0R0402-PAD-2-GP R1904
R1906 3KR2F-GP

HASWELL-6-GP

Layout Note:
4mil trace at break-out and 3 12-15mil trace with <0.2 ohms and length total <= 500mils.

Flash Descriptor Security Overide/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

The internal pull-down is disabled after PLTRST# deasserts

R1913 DY PCH_INTVRMEN 330KR2J-L1-GP

Integrated SUS 1V VRM Enable	
INTVRMEN	Low = External VRs High = Internal VRs*

1D05S_VCCST

R1916 DY PCH_JTAG_TDI 51R2J-2-GP
R1917 DY PCH_JTAG_TDO 51R2J-2-GP
R1918 DY PCH_JTAG_TMS 51R2J-2-GP
R1919 DY XDP_TCK_JTAGX 1KR2J-1-GP

R1920 DY PCH_JTAG_TCK 51R2J-2-GP

3D3V_S0

RN1902 SRN10KJ-6-GP

EC_SMI# MCP_GPIO35 MSATA_DET# SATA_ODD_PRSNT#

<Core Design>

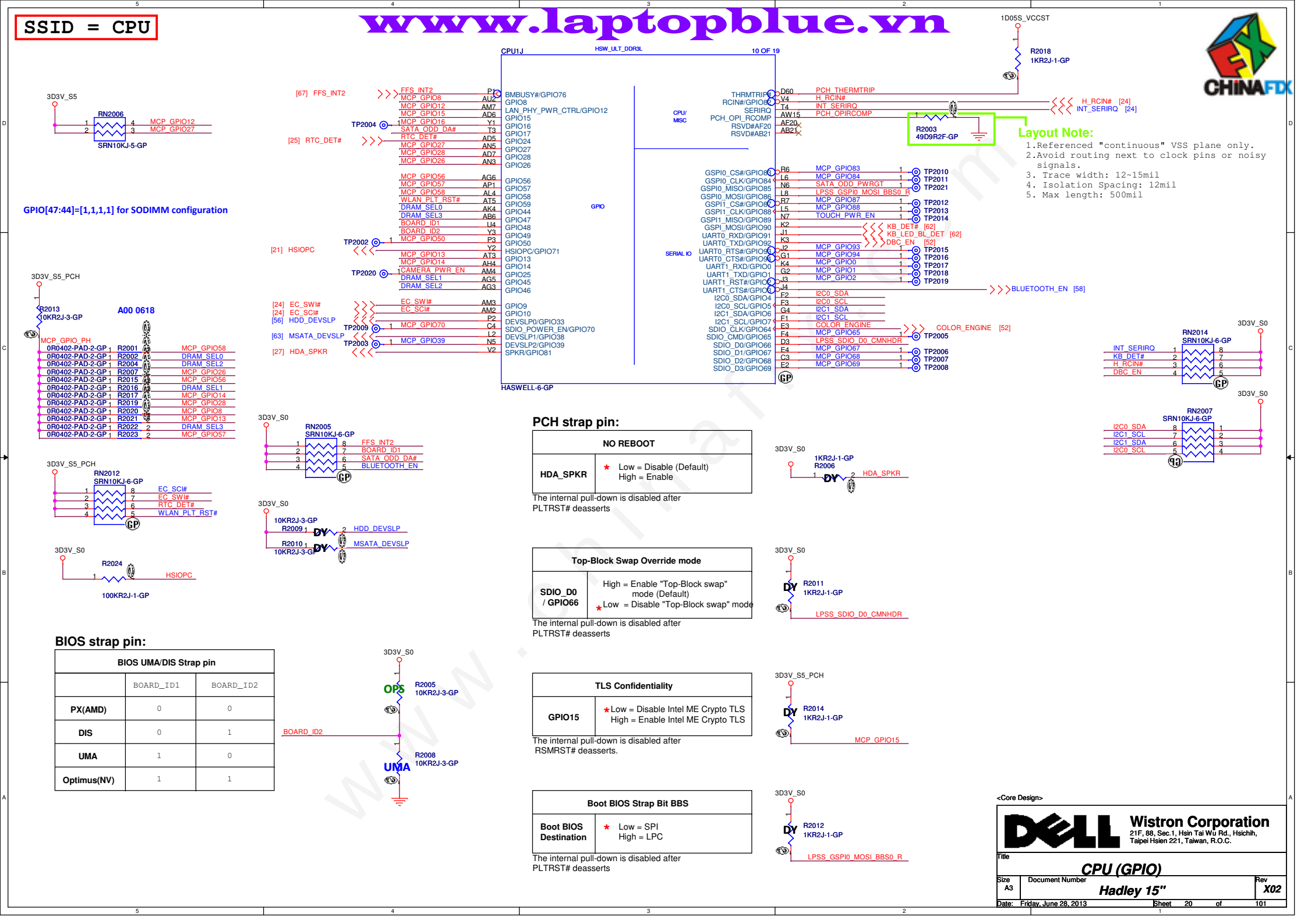
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (RTC/SATA/HDA/JTAG)

Size	Document Number	Rev
A3	Hadley 15"	X02

Date: Friday, June 28, 2013 Sheet 19 of 101

SSID = CPU



<Core Design>

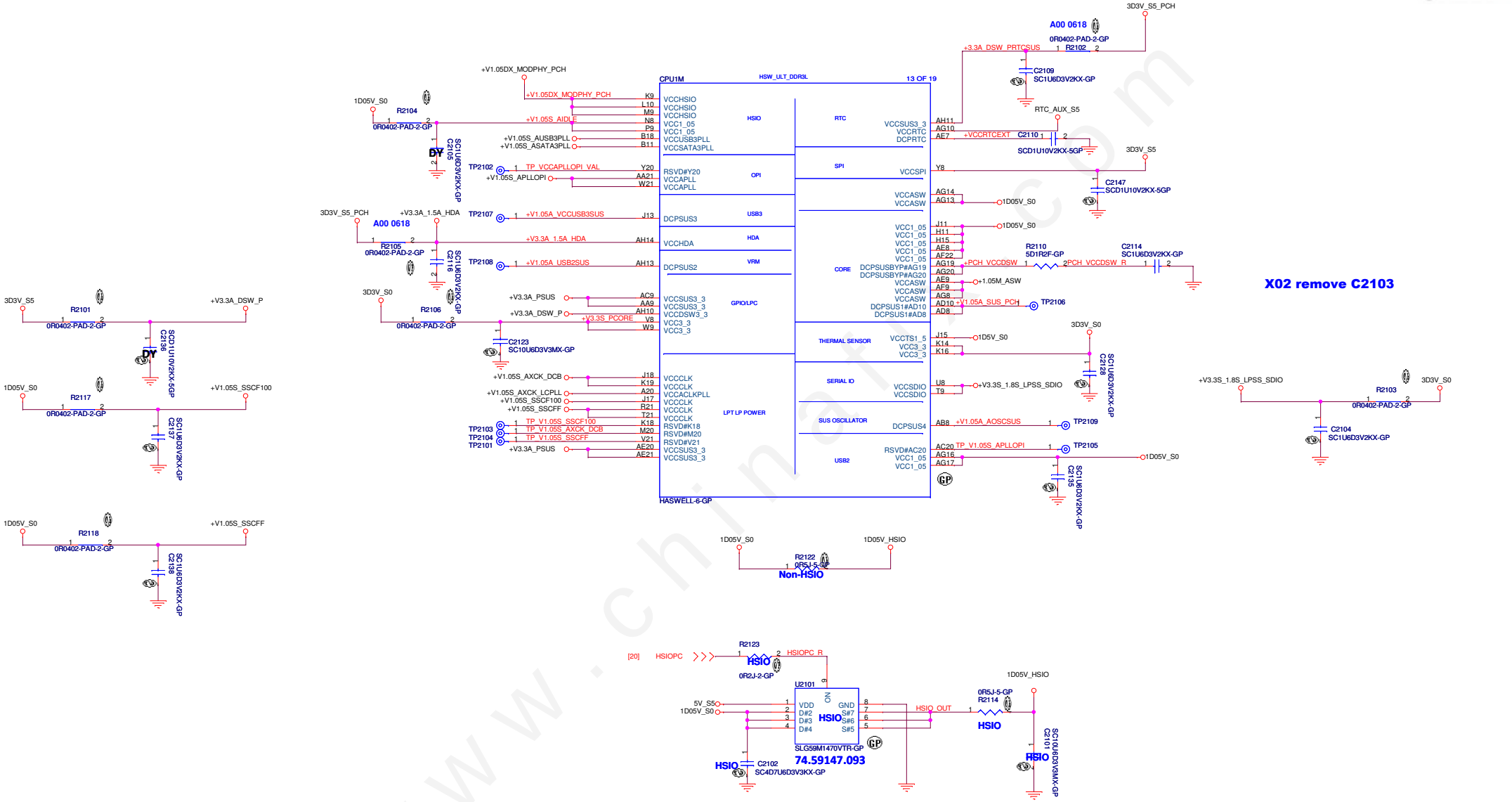
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (GPIO)

Size	Document Number	Rev
A3	Hadley 15"	X02

Date: Friday, June 28, 2013 Sheet 20 of 101

SSID = CPU



<Core Design>

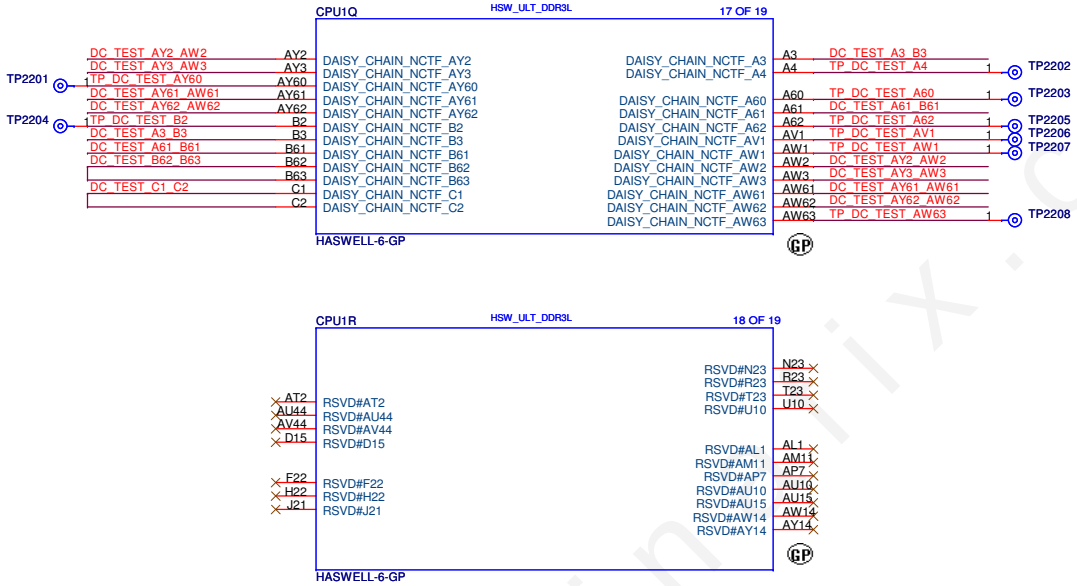
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (POWER2)

Size: Custom | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 21 of 101

SSID = CPU



<Core Design>

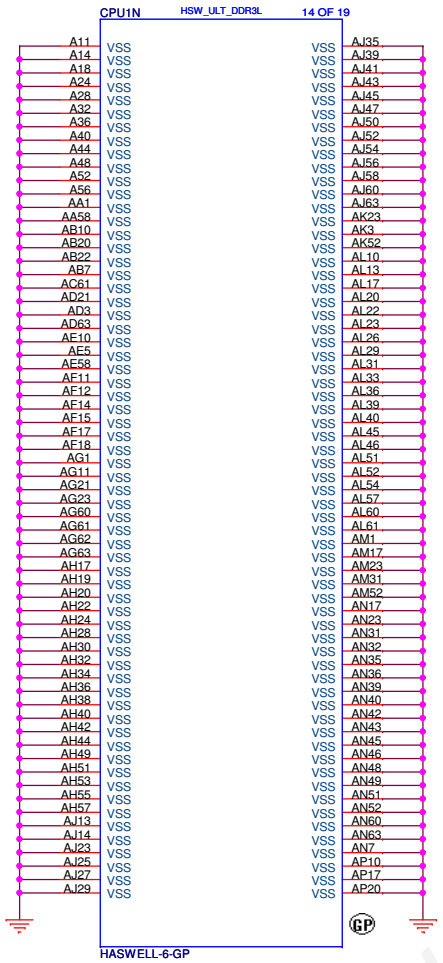
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

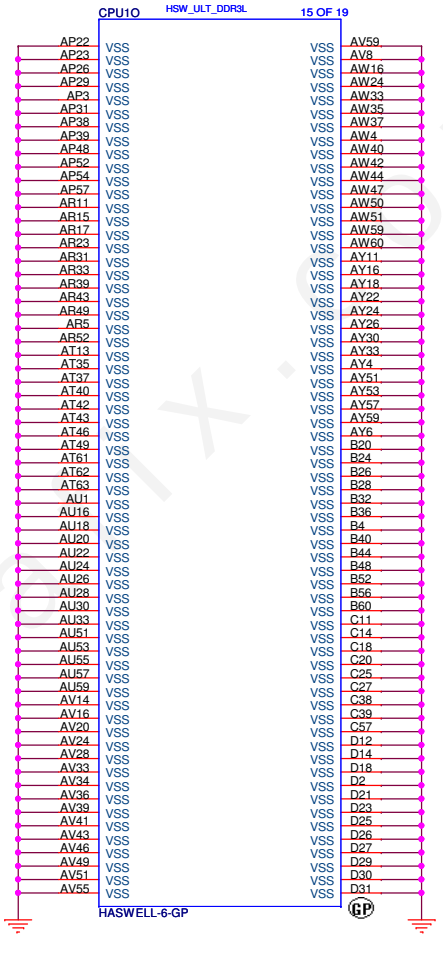
Title: RSVD

Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 22 of 101

SSID = CPU





<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (VSS)	
Size: A3	Document Number: Hadley 15"	Rev: X02
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SSID = KBC

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.0V
X01	100.0K	20.0K	2.75V
X02	100.0K	33.0K	2.48V
X03	100.0K	47.0K	2.24V
A00	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

MODEL_ID_DET(GPIO07)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
(DOH70)UMA	100.0K	10.0K(64.10025.6DL)	3.0V
(DOH50)UMA/eDP	100.0K	13.7K(64.13725.6DL)	2.852V
TBD	100.0K	17.8K(64.17825.6DL)	2.681V
(DOH70)DIS	100.0K	22.1K(64.22125.6DL)	2.5V
TBD	100.0K	27.0K(64.27025.6DL)	2.5V
TBD	100.0K	32.4K(64.32425.6DL)	2.402V
TBD	100.0K	37.4K(64.37425.6DL)	2.402V
TBD	100.0K	43.2K(64.43225.6DL)	2.402V
(DOH50)UMA/LVDS	100.0K	49.9K(64.49925.6DL)	2.402V
(DOH50)DIS/eDP	100.0K	57.6K(64.57625.6DL)	2.003V
TBD	100.0K	64.9K(64.64925.6DL)	2.001V
TBD	100.0K	73.2K(64.73225.6DL)	1.905V
TBD	100.0K	82.5K(64.82525.6DL)	1.808V
TBD	100.0K	93.1K(64.93125.6DL)	1.709V
TBD	100.0K	107K(64.10735.6DL)	1.594V
TBD	100.0K	120K(64.12035.6DL)	1.499V
TBD	100.0K	137K(64.13735.6DL)	1.392V
TBD	100.0K	154K(64.15435.6DL)	1.299V
TBD	100.0K	200K(64.20035.6DL)	1.099V
TBD	100.0K	232K(64.23236.6DL)	0.994V

Layout Note:
Need very close to EC

Layout Note:
Need very close to EC

Layout Note:
Need very close to EC
C2422 PDG is 47p

Layout Note:
Connect GND and AGND planes via either
0R resistor or connect directly.

Don't PD

ALL_SYS_PWRGD assert, delay 10ms;
PCH_PWROK assert.

ALL_SYS_PWRGD assert, delay 100ms;
SYS_PWROK assert.

LVDS backlight Control from PS8625

eDP backlight Control from PCH

Backlight Control from LVDS Converter

AOAC Ambient temperature detect

EC_GPIO47 High Active

KBC24

NPCE985PA0DX-1-GP
71.00985.C0G

CH751H-40PT-GP
83.R0304.A8F

D2401
BAT54CPT-2-GP
75.00054.K7D

Q2401 2N7002K-2-GP
84.2N702.I31
2ND = 84.2N702.031
3rd = 84.07002.I31
4th = 84.2N702.W31

Q2402 DMP2130L-7-GP
84.02130.031
2ND = 84.03413.A31

Q2403 2N7002K-2-GP
84.2N702.I31
2ND = 84.2N702.031
3rd = 84.07002.I31
4th = 84.2N702.W31

Q2404 MMBT3906-4-GP
84.T3906.A11
2nd = 84.03906.F11

R2441 NTC-10K-26-GP
69.60037.011

X01 0321

A00 0618

<Core Design>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

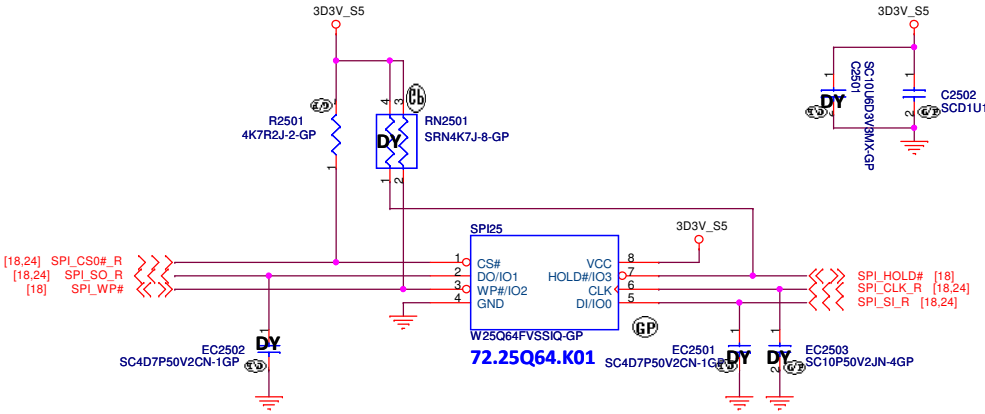
Title: KBC Nuvoton NPCE985

Size: A2 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 24 of 101

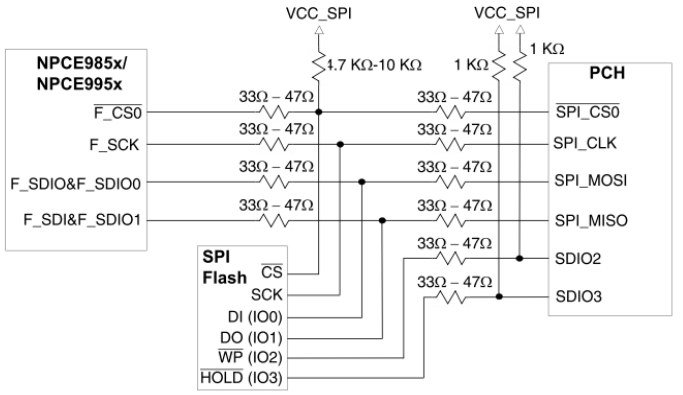
SSID = Flash.ROM

SPI Flash ROM(8M) for PCH



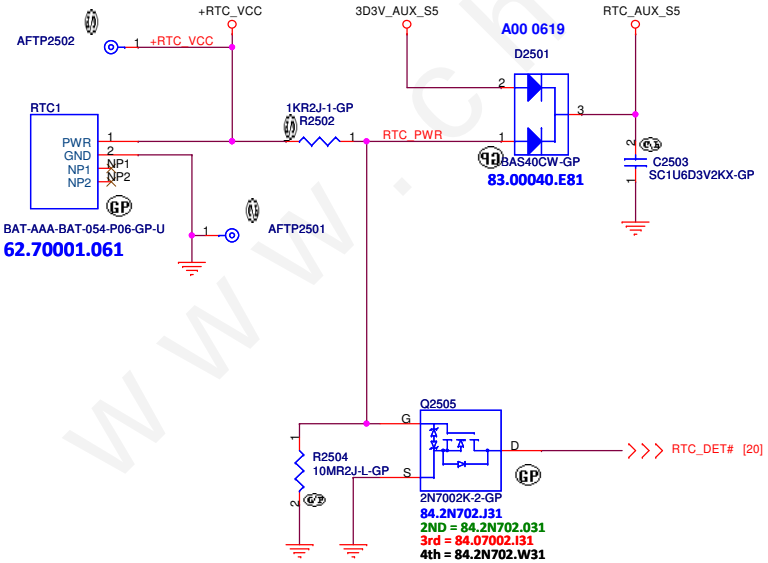
Source	QUAD/DUAL fast read	DUAL fast read
72.25Q64.K01	O	O
72.25647.00A	O	O

Single SPI shared flash connection (SPI Quad I/O mode)



Refer to "NCPE985x/ NPCE995x board design reference guide"

SSID = RBATT

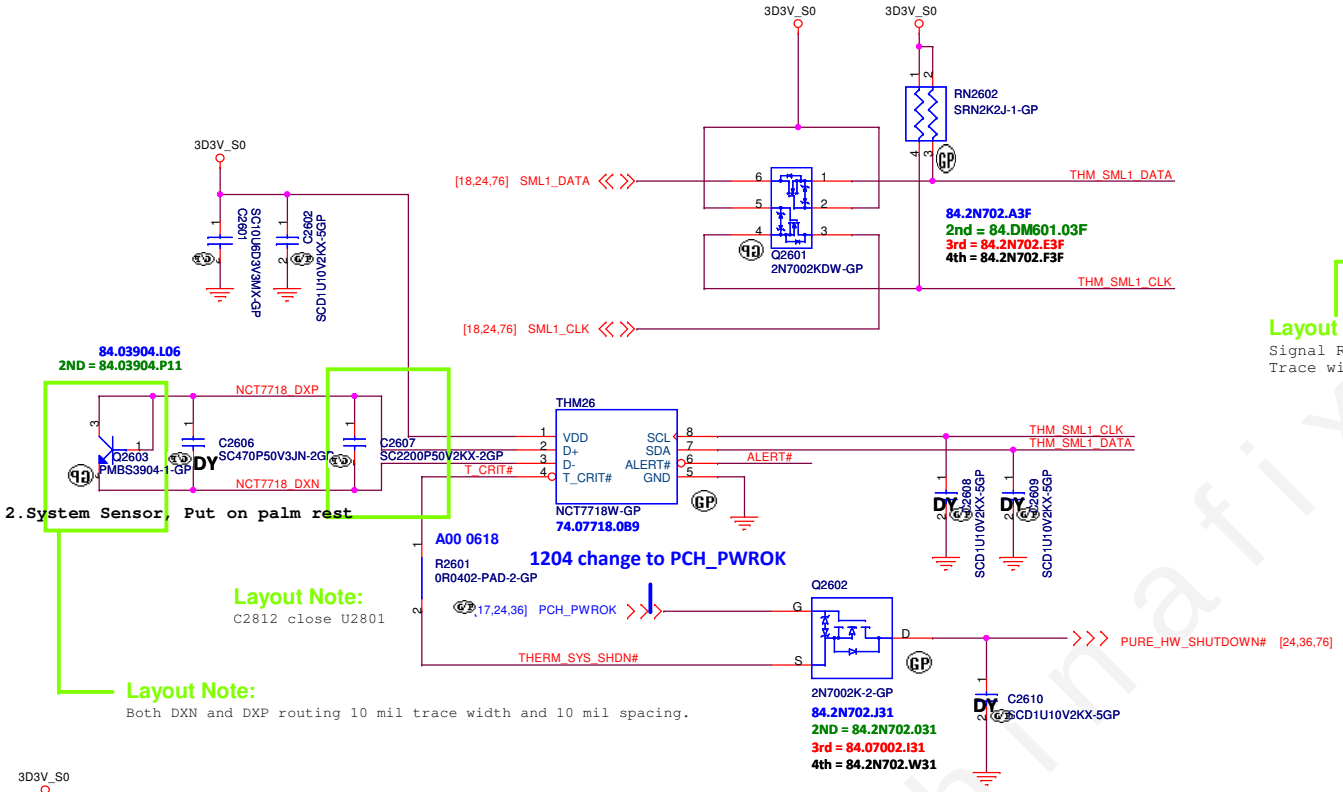


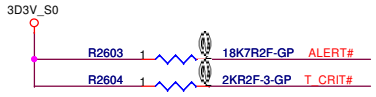
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC		
Size: A3	Document Number: Hadley 15"	Rev: X02
Date: Friday, June 28, 2013	Sheet 25 of 101	

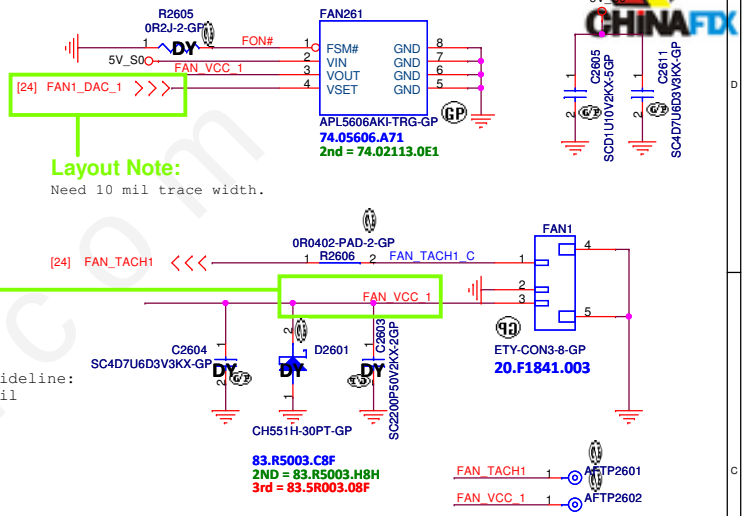
SSID = Thermal





TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

Fan controller1



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal NCT7718W/Fan

Size: A3 | Document Number: Hadley 15" | Rev: X02

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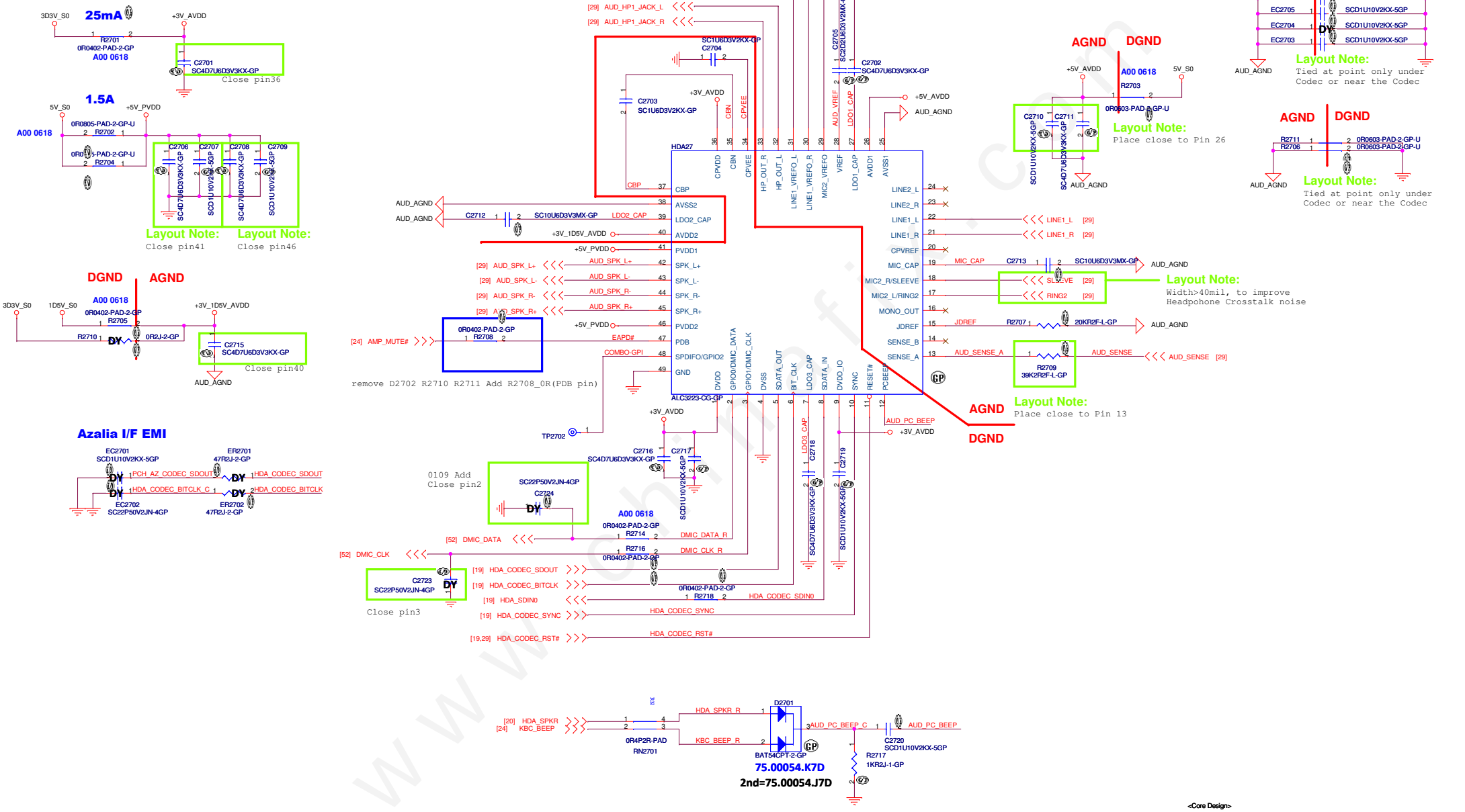
SSID = AUDIO



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec ALC3223

Size: Custom | Document Number: Hadley 15" | Rev: X02

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<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

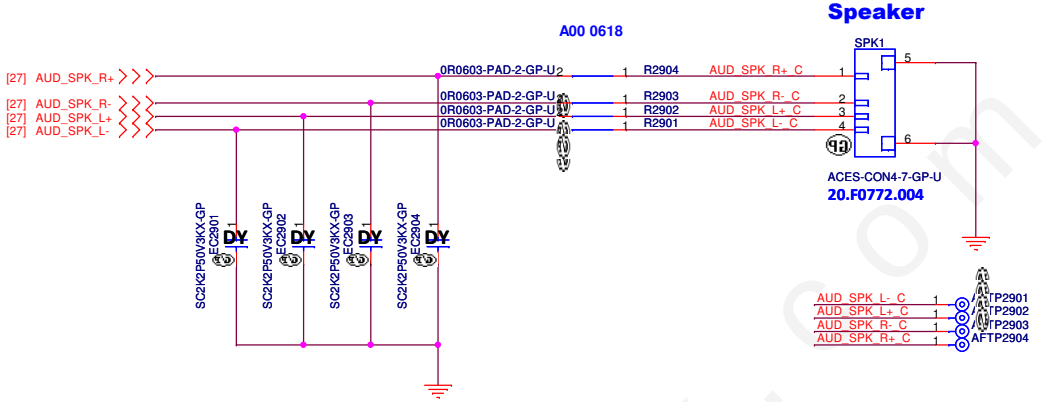
Title: Reserved

Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 28 of 101

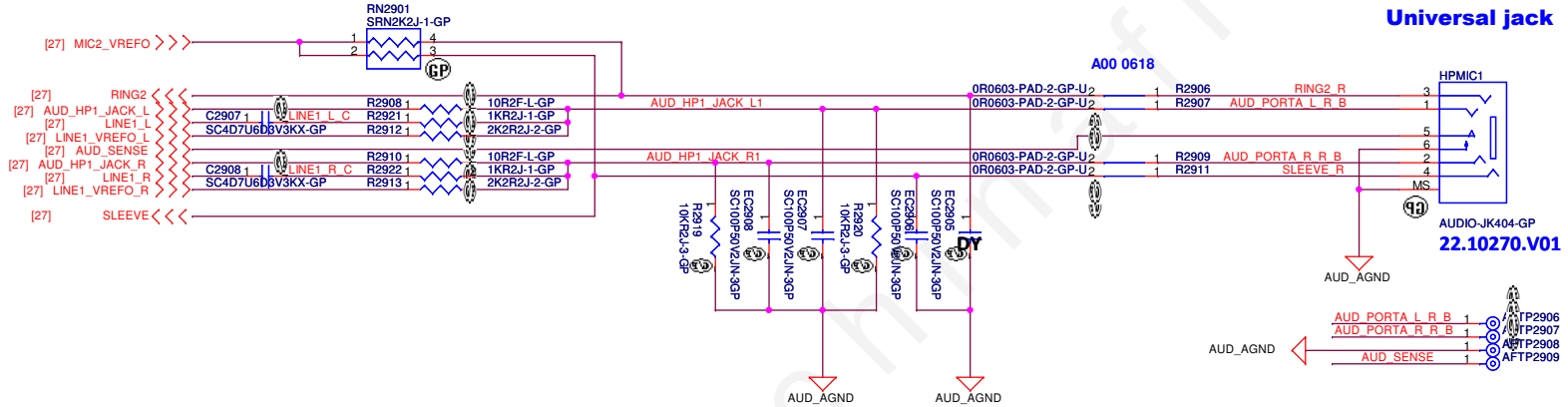
SSID = AUDIO

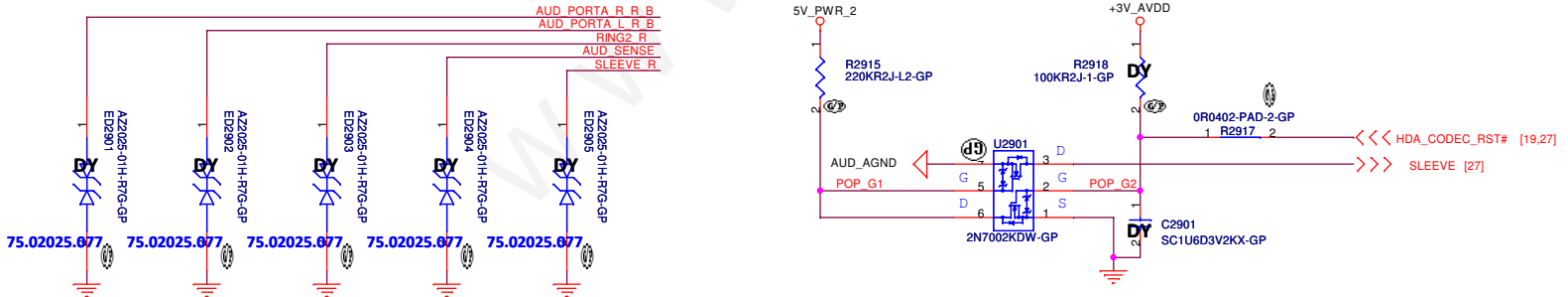
Speaker



CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L_

Universal jack





<Core Design>

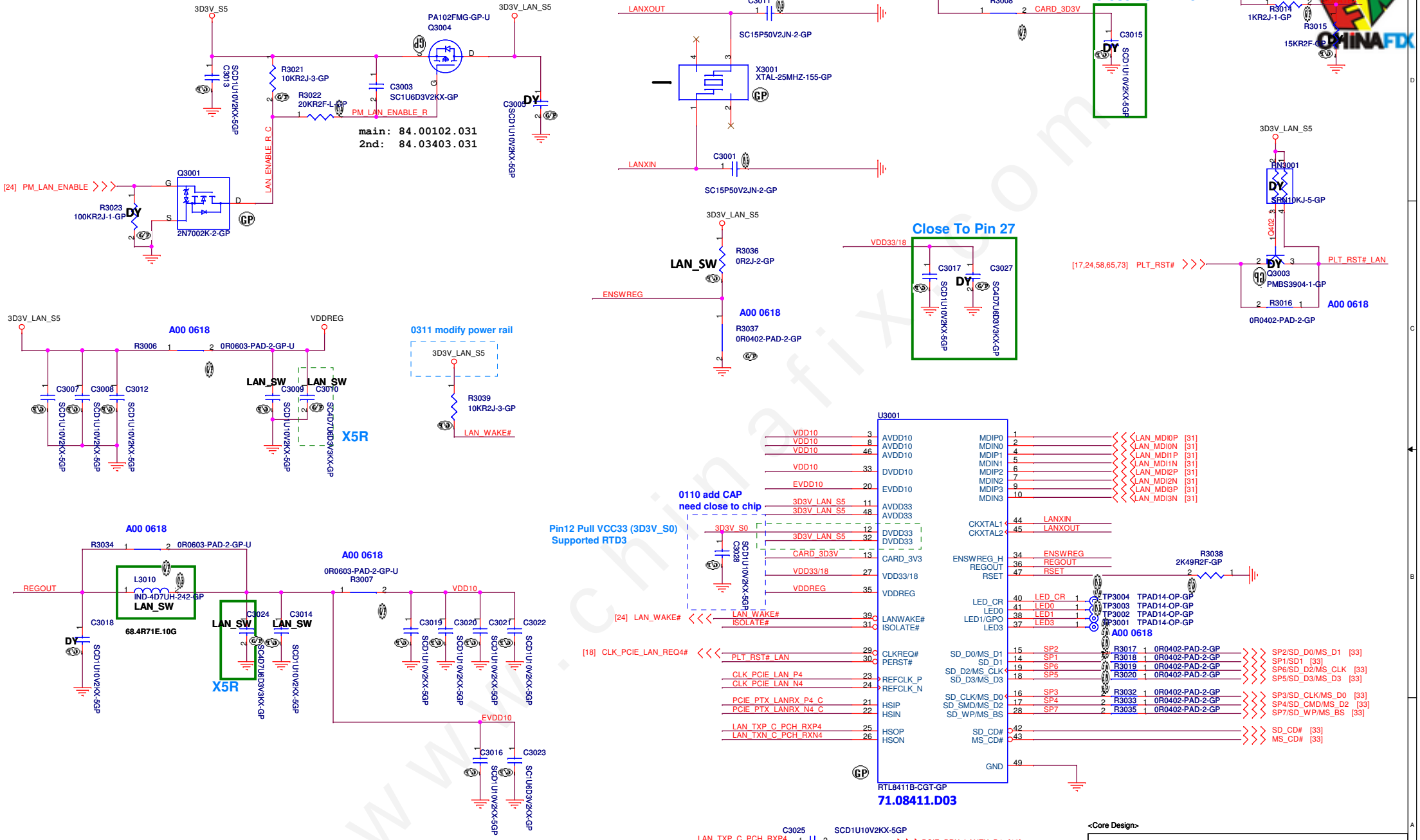
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Speaker/HPMIC CONN

Size	Document Number	Rev
A3	Hadley 15"	X02

Date: Friday, June 28, 2013 Sheet 29 of 101

SSID = LOM



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

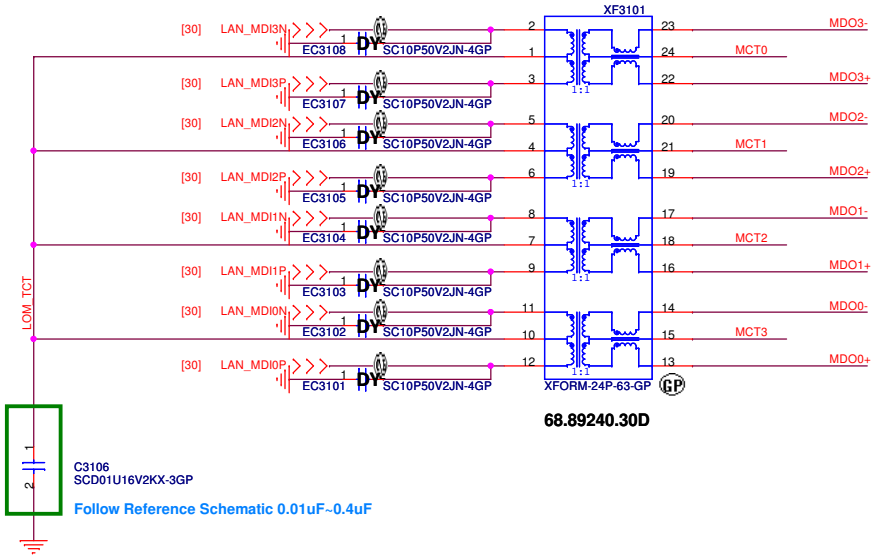
Title: **LOM(RTL8411B)**

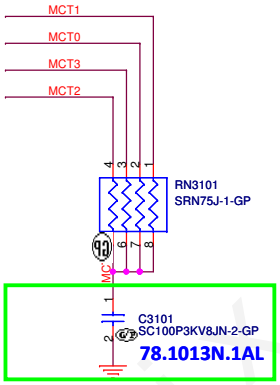
Size	Document Number	Rev
A3	Hadley 15"	X02

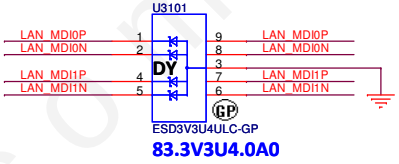
Date: Friday, June 28, 2013 Sheet 30 of 101

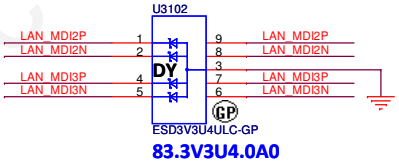
SSID = LOM

GIGA LAN TransFormer

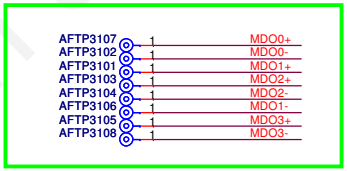


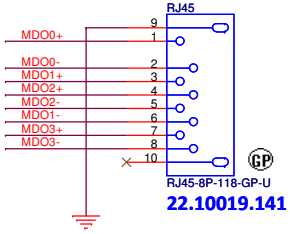






Layout:
Place near RJ45





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RJ45+Transformer

Size	Document Number	Rev
A3	Hadley 15"	X02

Date: Friday, June 28, 2013 Sheet 31 of 101

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Hadley 15" | Rev: X02

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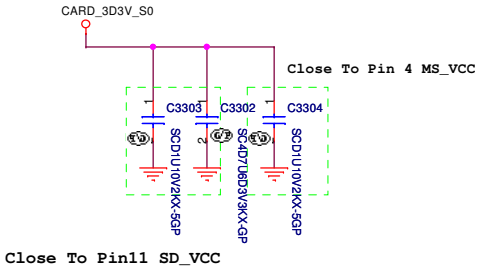
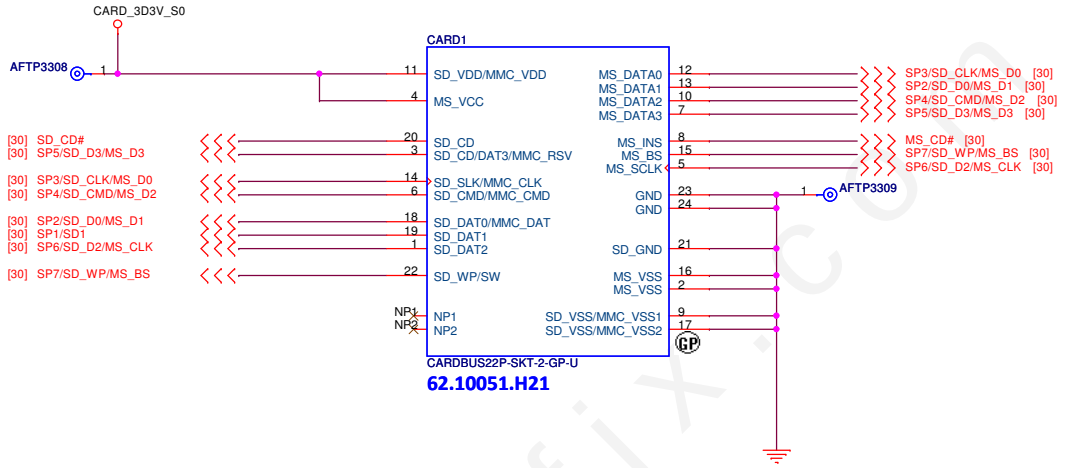
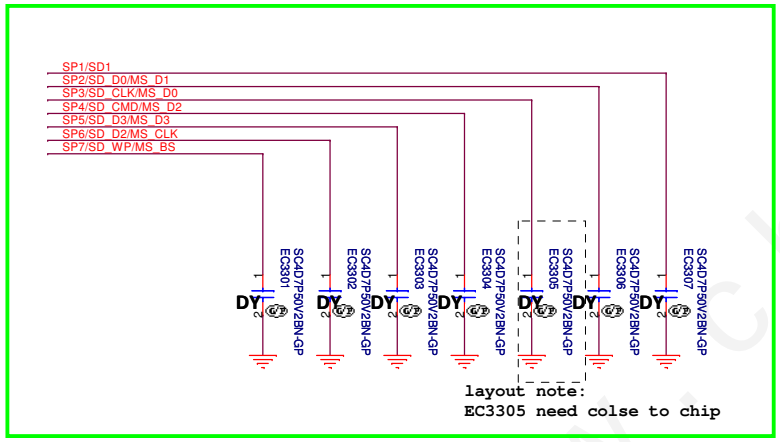
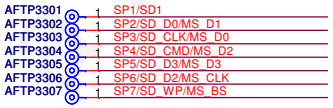
SSID = SDIO





Reserve EMI Cap, 0107 CLK Cap DY





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

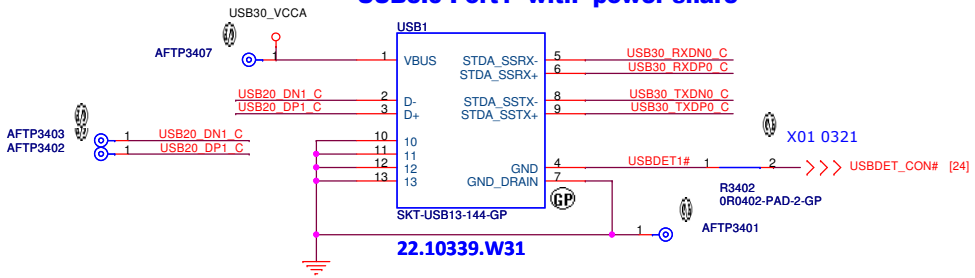
Title: Card Reader CONN

Size	Document Number	Rev
A3	Hadley 15"	X02

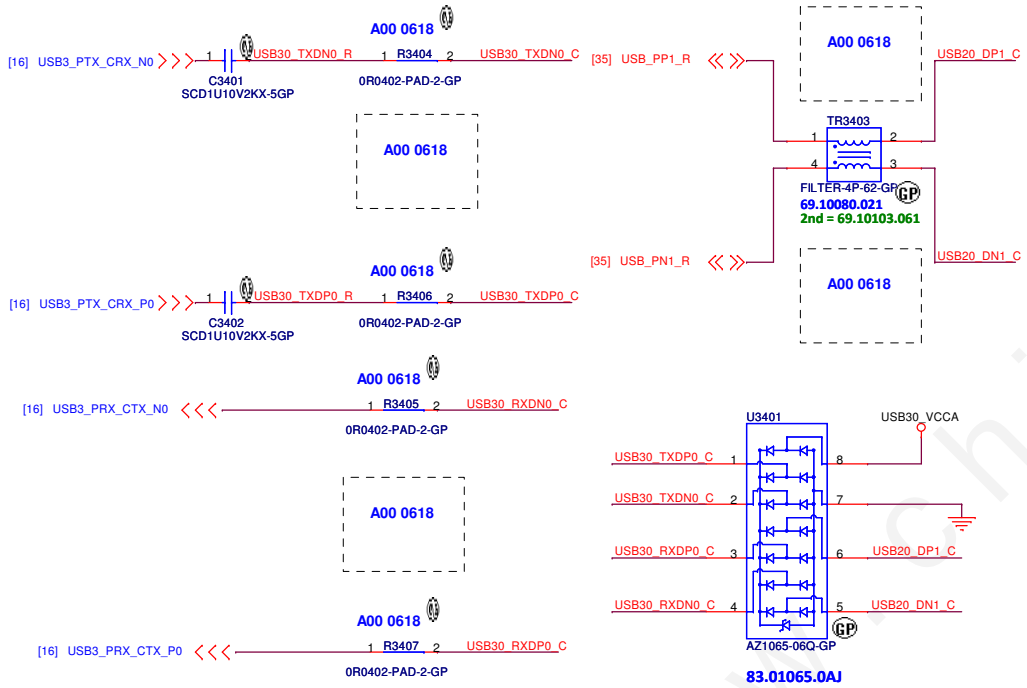
Date: Friday, June 28, 2013 Sheet 33 of 101

SSID = USB

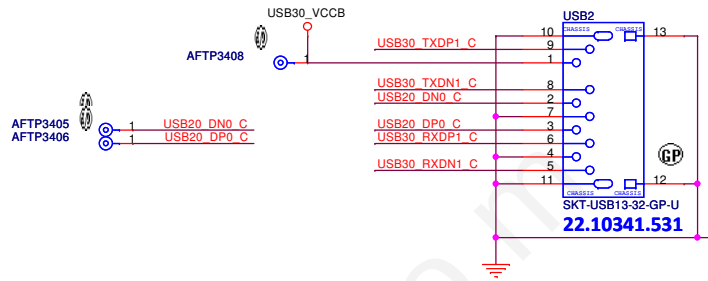
USB3.0 Port1 with power share



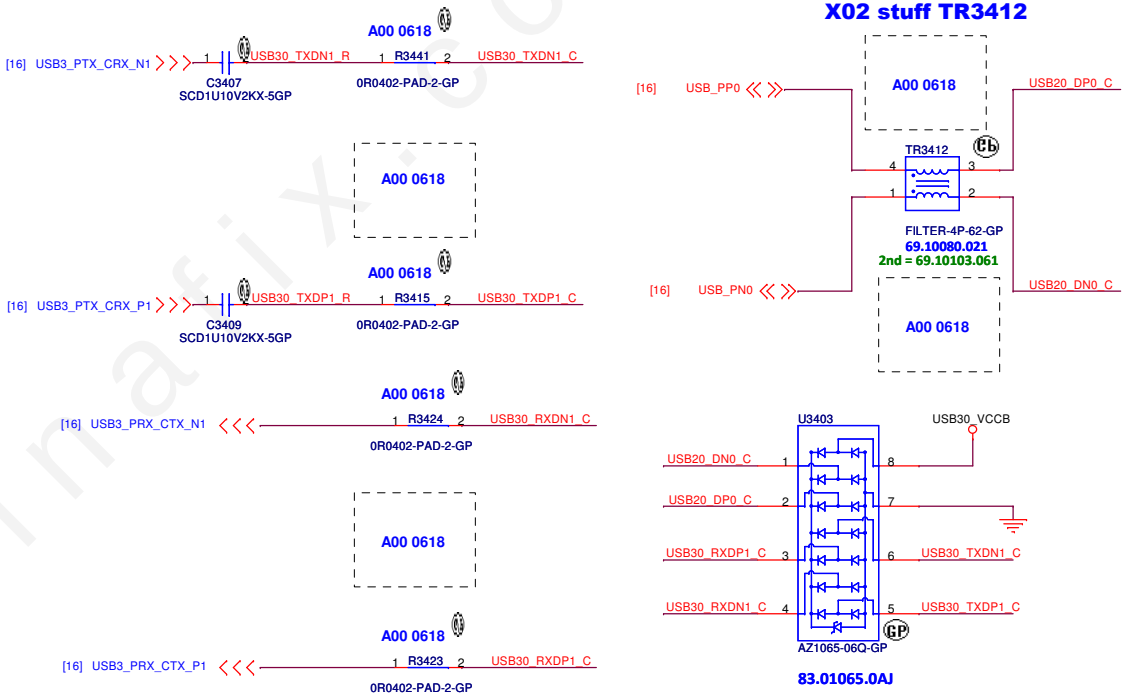
X02 stuff TR3403



USB3.0 Port2



X02 stuff TR3412



<Core Design>

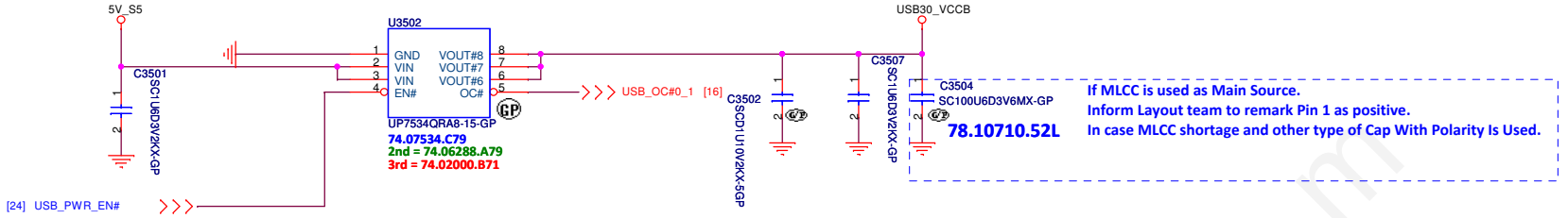
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

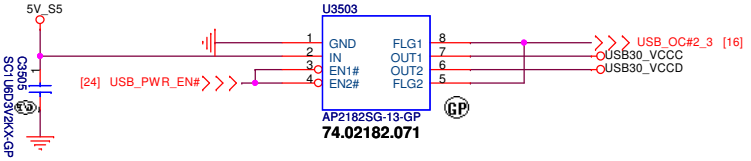
Title: USB3.0(1)

Size	Document Number	Rev
A3	Hadley 15"	X02

Date: Friday, June 28, 2013 Sheet 34 of 101

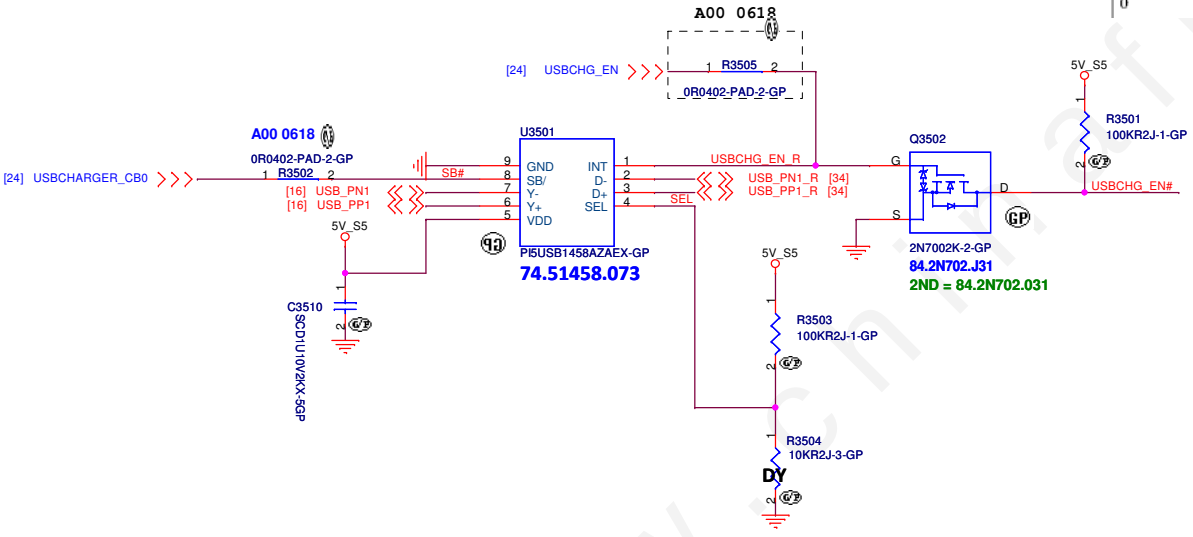
SSID = USB

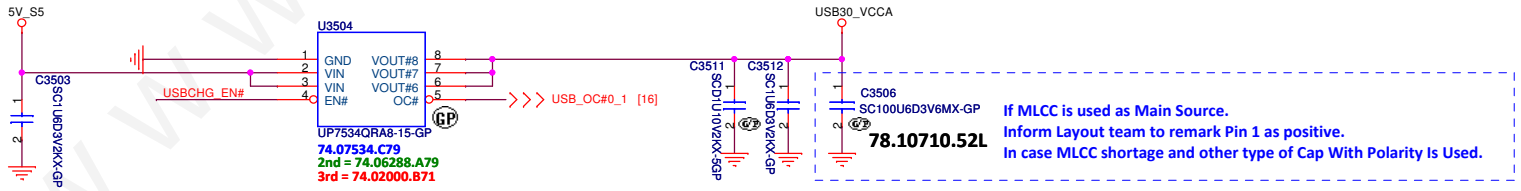




SB/ (pin 8)	SEL(pin 4)	Feature	pin 1 role (INT or INT/)
0	0	Auto S & C without mouse/keyboard pass through	INT or INT/
0	1	Auto S & C with mouse/keyboard pass through	INT or INT/
1	0	S0 charging with SDP only	INT or INT/
1	1	S0 charging with CDP or SDP only (depending on external device)	INT or INT/
0	M= (1/2)*V_{DD}	Test Mode, M = $V_{DD/2}$ = (1/2)*V_{DD}	

0319 modify USB Charger circuit





USB Power SW (U3504)

Vendor	Vendor P/N	Wistron P/N	Priority
Silergy	SY6288DCAC	74.06288.A79	1ST
DII (Diodes)	AP2301MPG-13	74.02301.071	2ND
GMT	G547I2P81U	74.00547.F79	3RD

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB Power SW

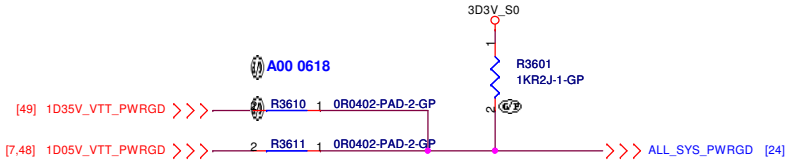
Size | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 35 of 101

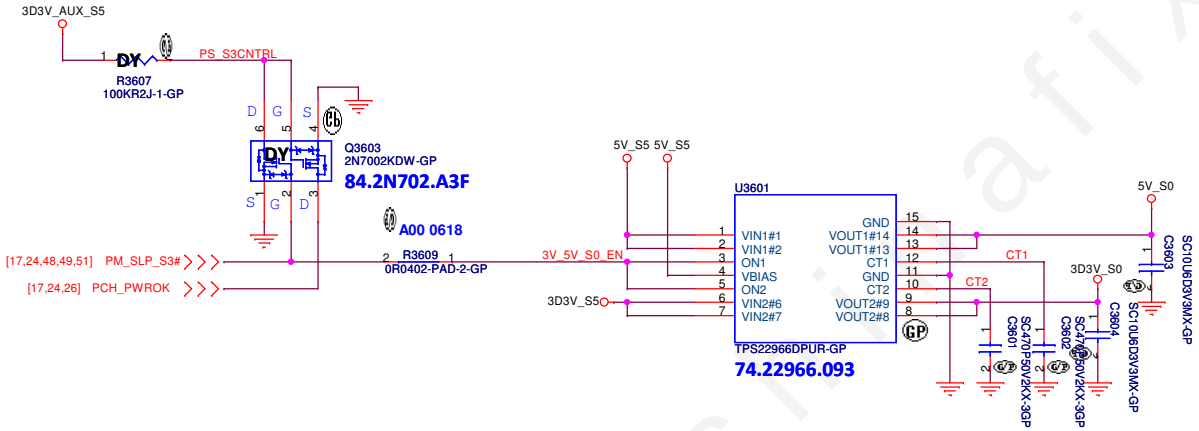
SSID = Reset.Suspend

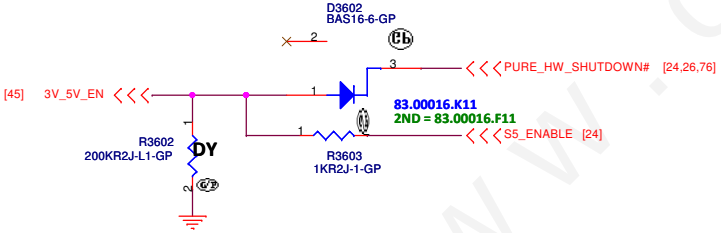
CHINAFDX

Power Good



ROSA Run Power





5V_S0

5V_S0 Comsumption
Peak current 4.033A

3D3V_S0

3D3V_S0 Comsumption
Peak current 3A

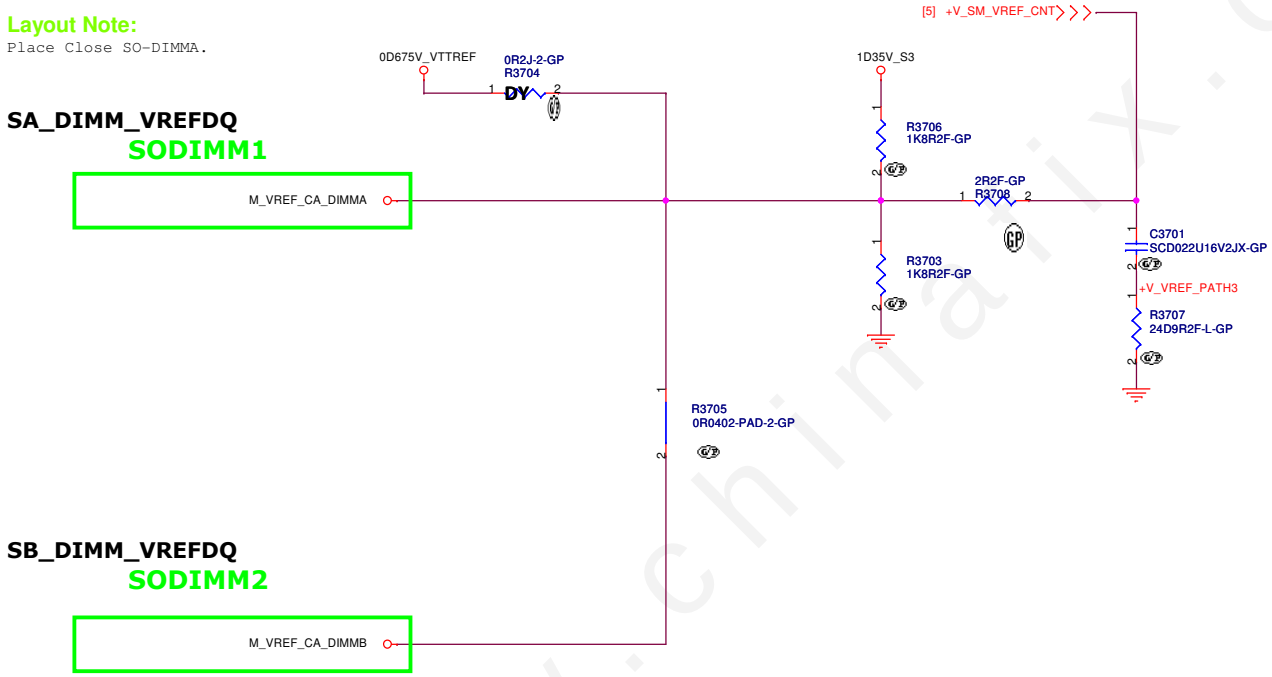
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable		
Size: A3	Document Number: Hadley 15"	Rev: X02
Date: Friday, June 28, 2013	Sheet 36 of 101	

SSID = Reset.Suspend

Layout Note:
Place Close SO-DIMMA.



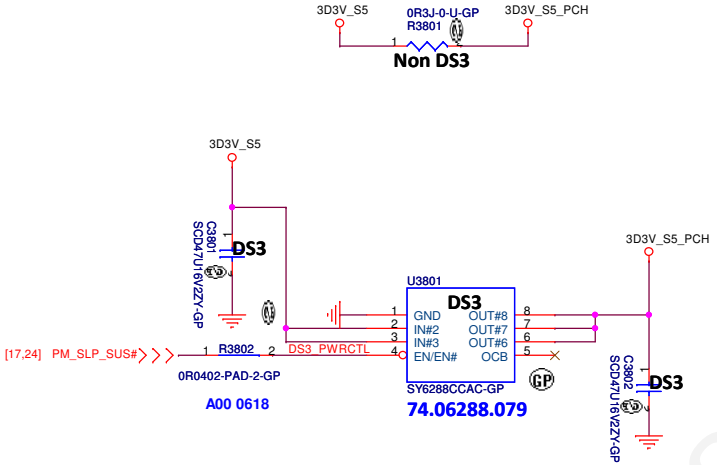
Close to DIMM
S3 Power Reduction Circuit PM_DRAM_PWRGD

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	S3 Power Reduction	
Size A3	Document Number Hadley 15"	Rev X02
Date: Friday, June 28, 2013	Sheet 37 of 101	

SSID = Reset.Suspend



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DSW	
Size A3	Document Number Hadley 15"	Rev X02
Date: Friday, June 28, 2013	Sheet 38 of 101	

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 39 of 101

(Blanking)

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: Reserved

Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 40 of 101

(Blanking)

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

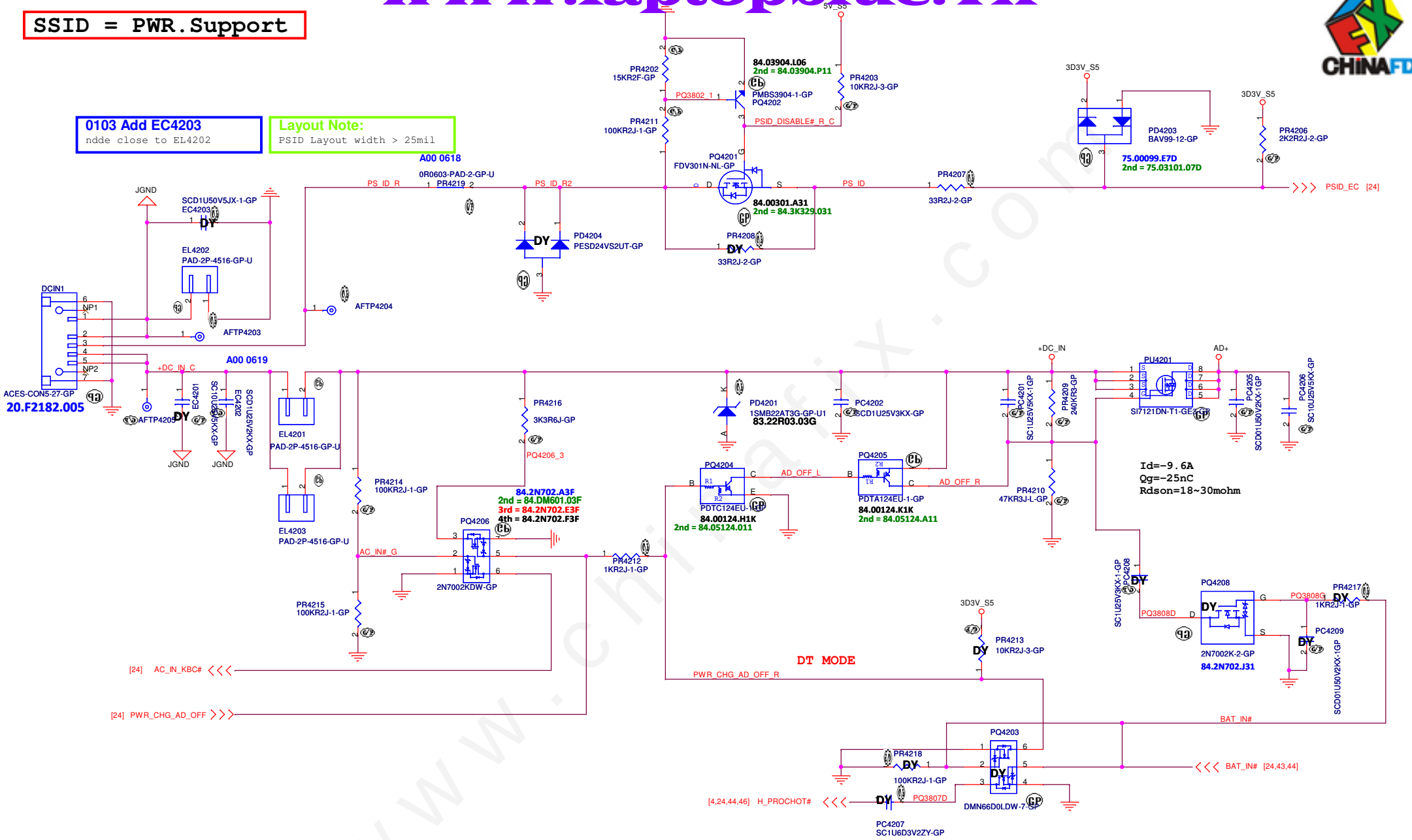
Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 41 of 101

SSID = PWR.Support

0103 Add EC4203
ndde close to EL4202

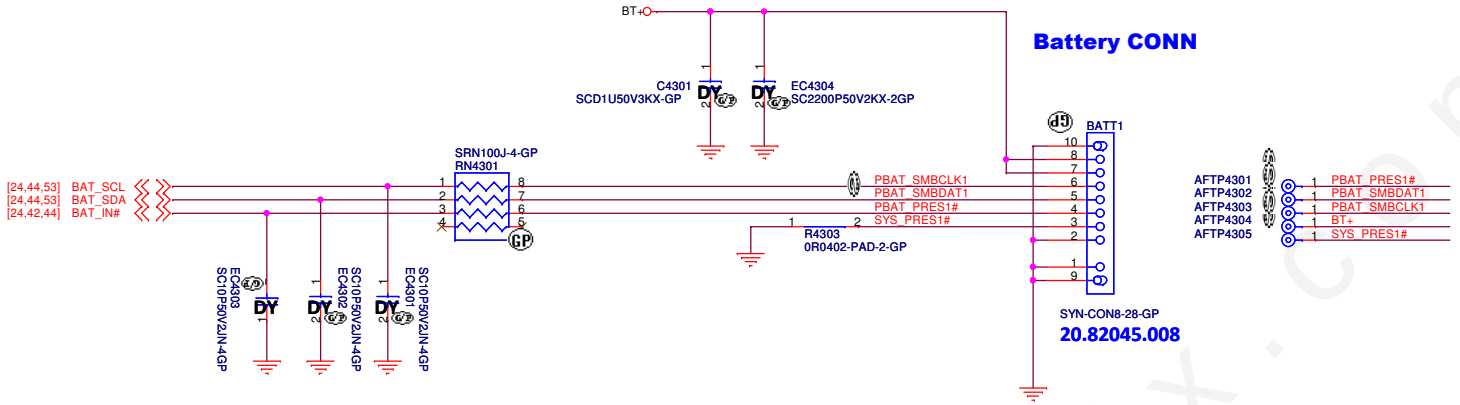
Layout Note:
PSID Layout width > 25mil



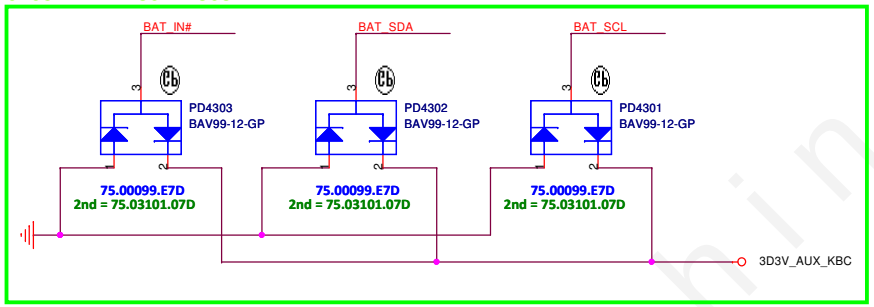
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DCIN	
Size A3	Document Number Hadley 15"	Rev X02
Date: Friday, June 28, 2013	Sheet 42 of 101	



0109 DY PD4301~4303



Layout Note:

Place near Battery CONN

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: BATT CONN

Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 43 of 101

SSID = Charger

KBC FOR DT MODE
CHECK EE PULL HIGH

VacDET=2.4V
Acok setting=2.4*((PR4444+PR4411)/PR4411)
Setting=18.178v

PU4406 and PU4407:
main source: 84.03660.037

ZZ.00215.037

DIS_DTM:
H= cell is plus to GND. (reset charger ic)
L=nornal

Follow custormer circuits

ACAV_IN
H=ACIN
L=UNAC

Close PR4443

CHECK PM BATTERY TYPE
CHECK CELL for DT mode

CHECK EE

BATTERY MON

PWR_CHG_ACOK:
PWR_CHG_REGN=6V
V+=6*(PR4404/(PR4410+PR4404))=3.27V

PWR_CHG_CMPIN:
V-=3.3*(PR4402/(PR4428+PR4402))=1.1099V

DIS_DTM_HW:
PWR_CHG_REGN=6V
V+=6*(PR4440/(PR4441+PR4440))=3.27V
Setting=3.27*((PR4442+PR4447)/PR4447)=9V

CHECK PM ADAPTER TYPE
And setting adapter type

(AD_IA_HW)
(AD_IA_HW_2)

ADAPTER TYPE	AD_IA_HW	AD_IA_HW_2	SETTING
90W	L	L	1.099V
65W	H	L	0.862329V
45W	L	H	0.659648V

CHECK EE
follow custormer circuits.

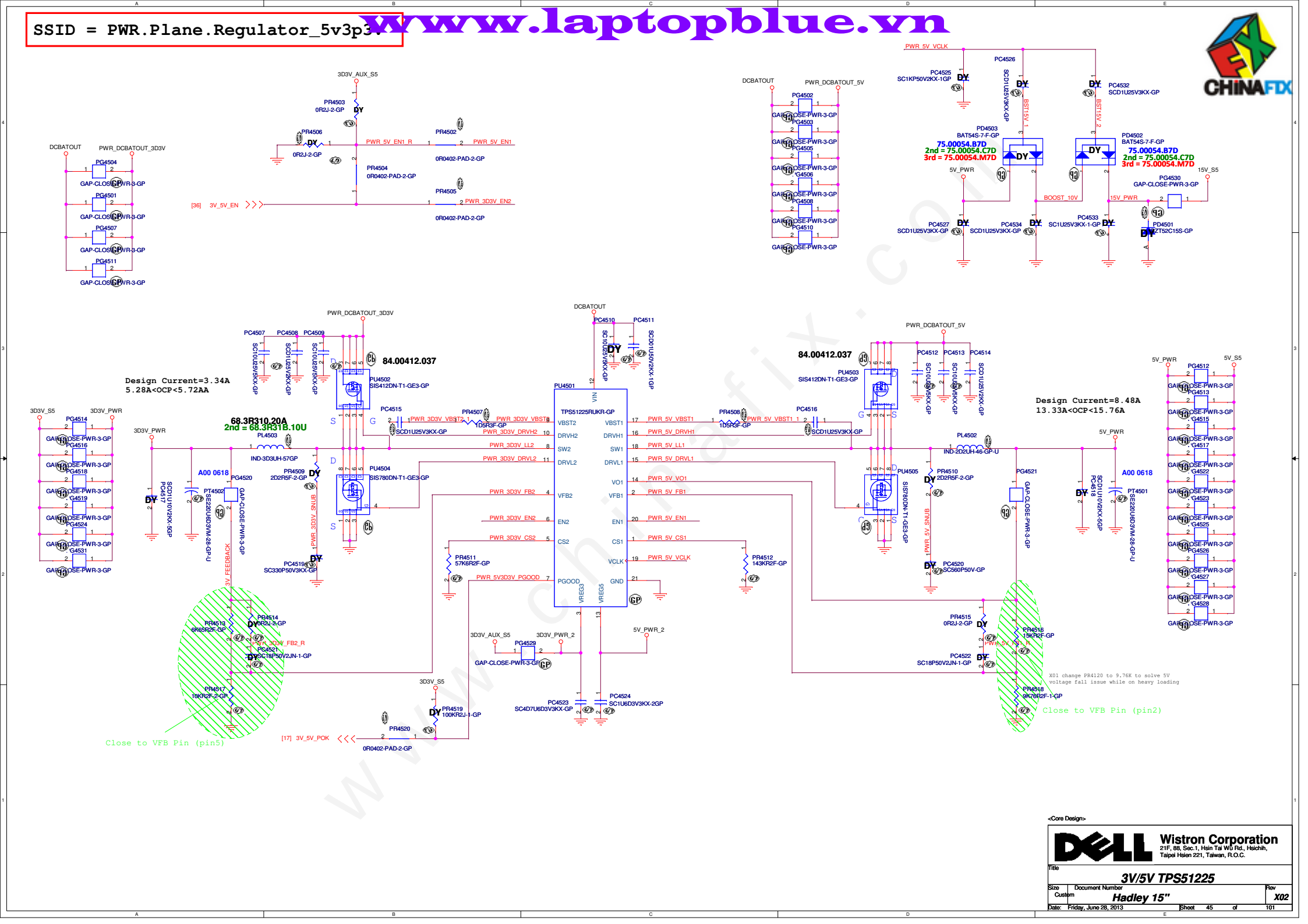
REGN REGULATOR

VREGN_REG	REGN Regulator Voltage	VVCC > 6.5V, VACDET>0.6V (0-50mA load)	5.5	6	6.5	V

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGE(BQ24715)
Size: Custom | Document Number | Rev: X02
Date: Friday, June 28, 2013 | Sheet 44 of 101

SSID = PWR.Plane.Regulator_5v3p3v



<Core Design>

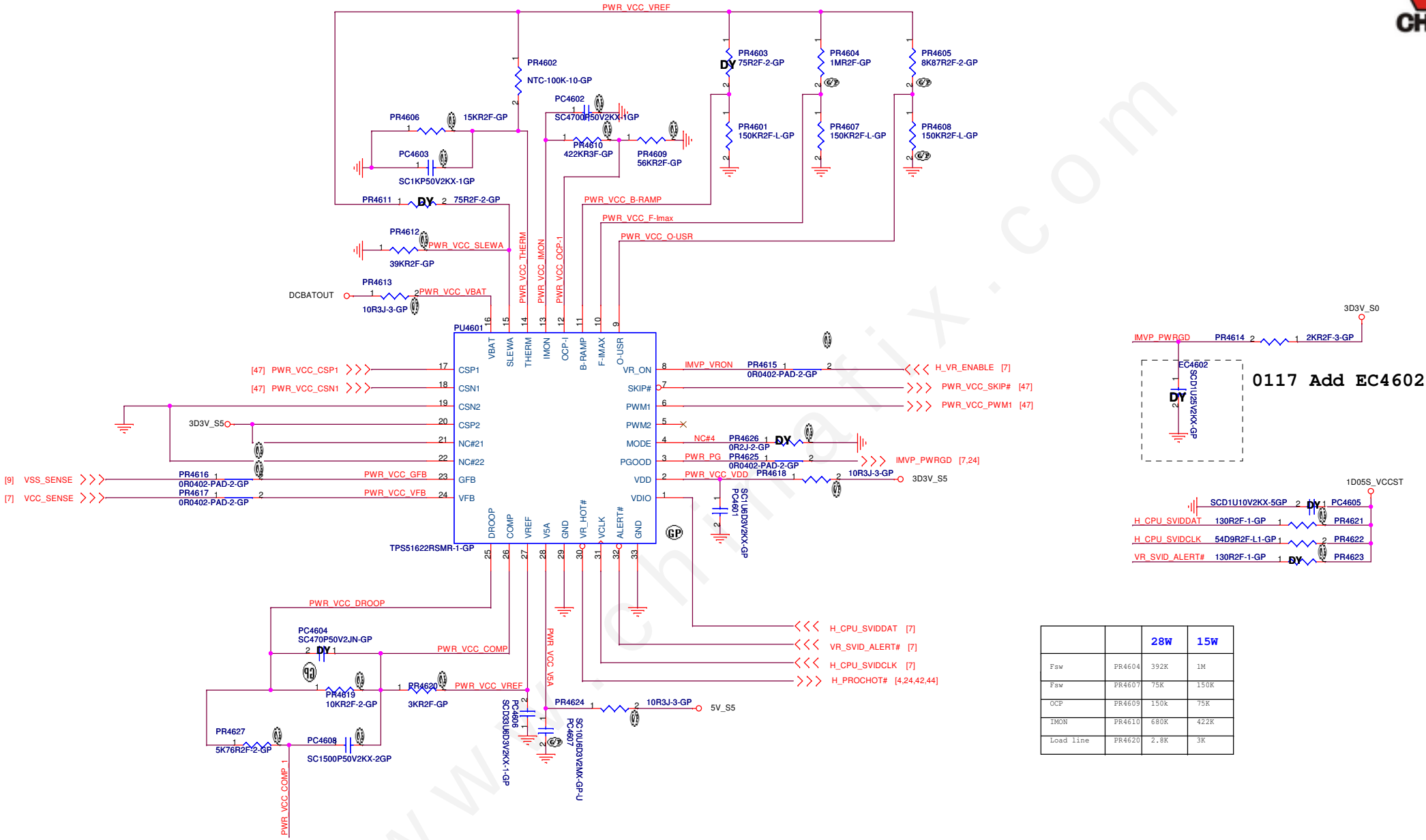
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 3V/5V TPS51225

Size	Document Number	Rev
Custom	Hadley 15"	X02

Date: Friday, June 28, 2013 Sheet 45 of 101

SSID = CPU.Regulator



		28W	15W
Fsw	PR4604	392K	1M
Fsw	PR4607	75K	150K
OCP	PR4609	150k	75K
IMON	PR4610	680K	422K
Load line	PR4620	2.8K	3K

<Core Design>

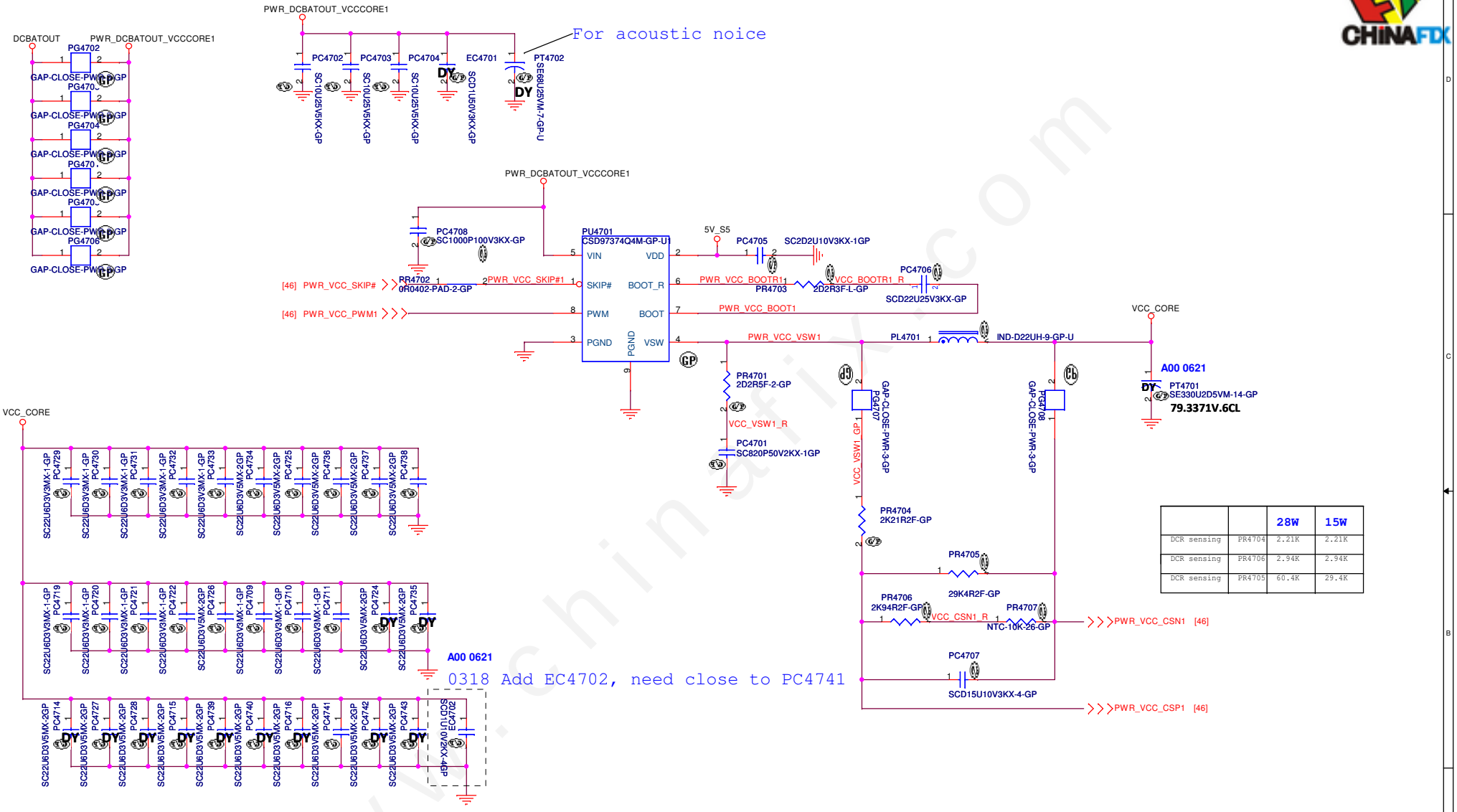
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51622_CPUCORE(1/2)

Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 46 of 101

SSID = CPU.Regulator



		28W	15W
DCR sensing	PR4704	2.21K	2.21K
DCR sensing	PR4706	2.94K	2.94K
DCR sensing	PR4705	60.4K	29.4K

<Core Design>

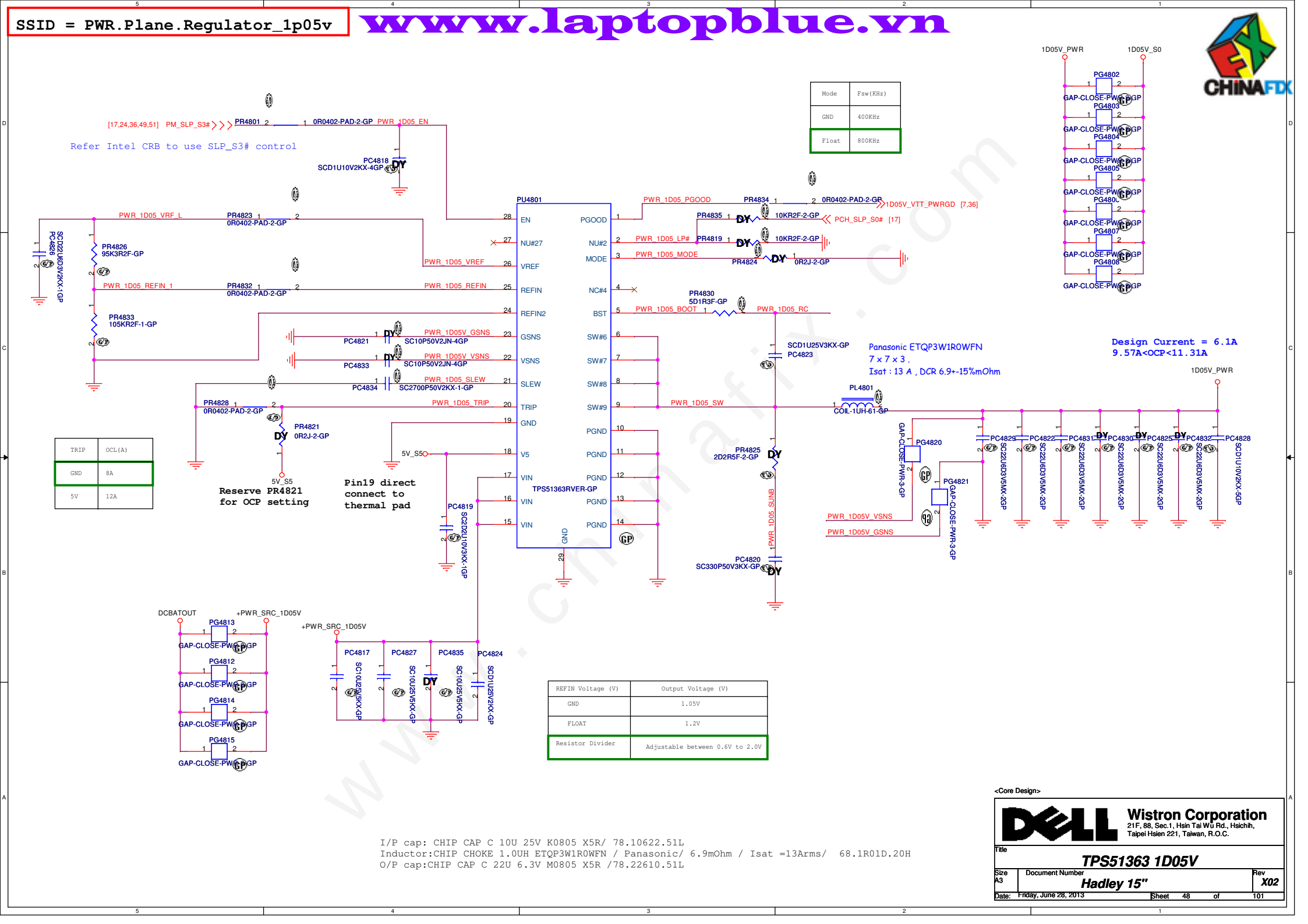
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51622_CPUCORE(2/2)

Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 47 of 101

SSID = PWR.Plane.Regulator_1p05v



Mode	Fsw(KHz)
GND	400KHz
Float	800KHz

TRIP	OCL(A)
GND	8A
5V	12A

REFIN Voltage (V)	Output Voltage (V)
GND	1.05V
FLOAT	1.2V
Resistor Divider	Adjustable between 0.6V to 2.0V

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor:CHIP CHOKE 1.0UH ETQP3W1R0WFN / Panasonic/ 6.9mOhm / Isat =13Arms/ 68.1R01D.20H
O/P cap:CHIP CAP C 22U 6.3V M0805 X5R /78.22610.51L

<Core Design>

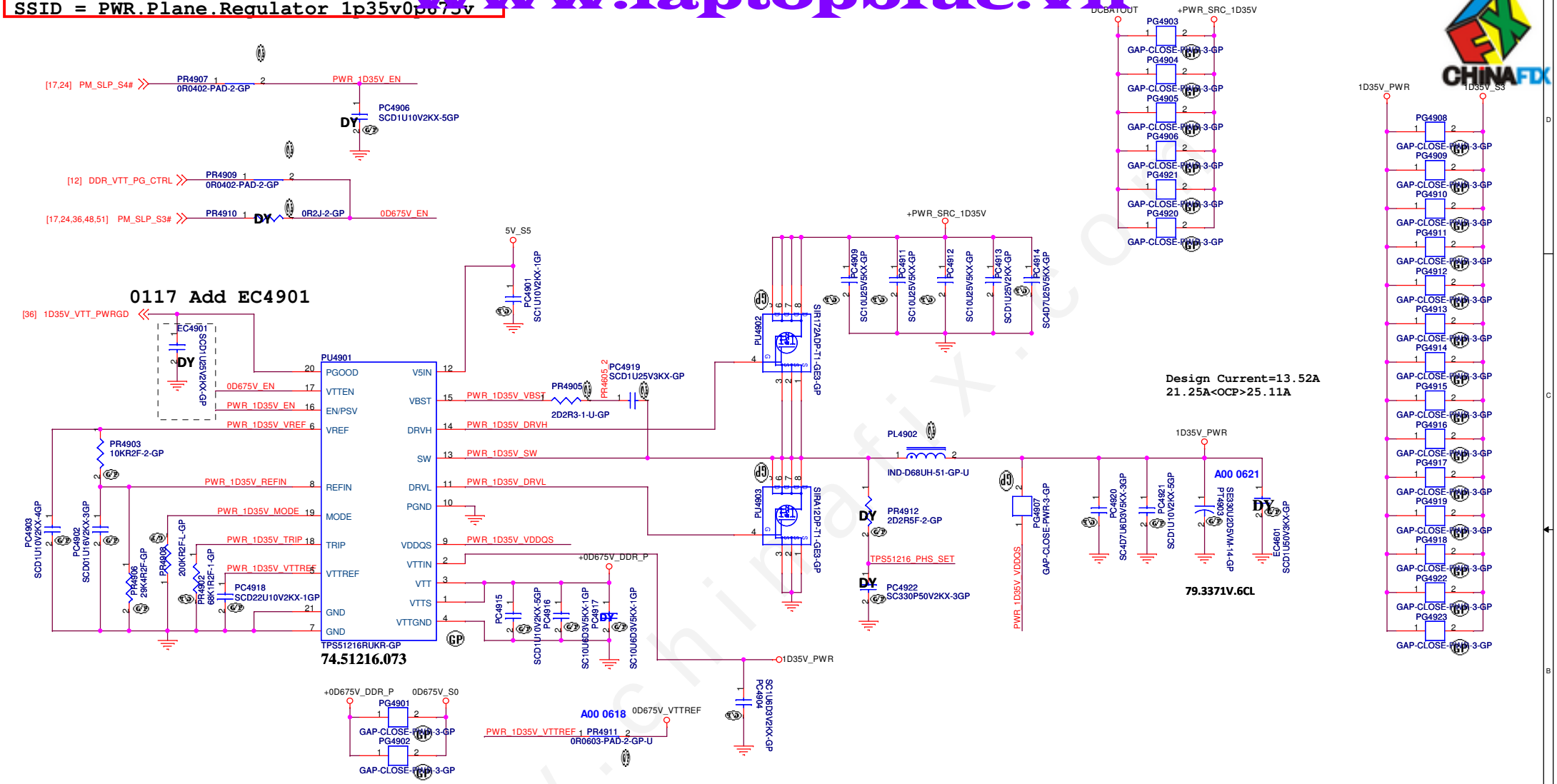
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51363 1D05V

Size	Document Number	Rev
A3	Hadley 15"	X02

Date: Friday, June 28, 2013 Sheet 48 of 101

SSID = PWR.Plane.Regulator 1p35v0p675v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE

PR4608	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 1.0UH PCMB104T-1R0M/ 3.3mohm/ Isat =28A rms /68.1R01C.10Q
O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L
H/S: SIR172ADP-T1-GE3 / 8.5mohm/10.5mOhm@4.5Vgs/ 84.00172.A37
L/S: SIRA12DP-T1-GE3 / 4.4mohm/6mOhm@4.5Vgs/ 84.SRA12.037

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51216_+1.35V_SUS
Size: A3
Document Number: Hadley 15"
Rev: X02
Date: Friday, June 28, 2013
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

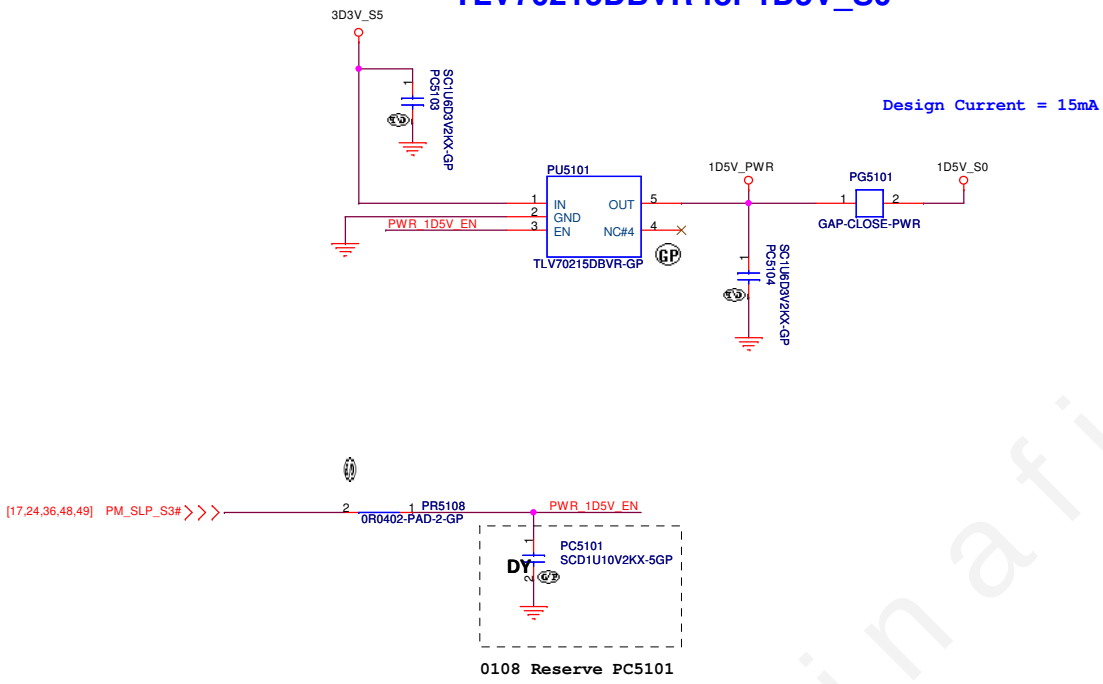
Title: (Reserved)TPS51312 1D8V

Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 50 of 101

SSID = PWR.Plane.Regulator_1p5v

TLV70215DBVR for 1D5V_S0



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RT9198-15PU5R_1D5V	
Size A3	Document Number Hadley 15"	Rev X02
Date: Friday, June 28, 2013	Sheet 51 of 101	

SSID = VIDEO

Pin	eDP	LVDS	Pin	eDP	LVDS
1	LCDVDD	LCDVDD	16	NC	LVDS_DATA2#
2	LCDVDD	LCDVDD	17	NC	LVDS_DATA2
3	LCDVDD	LCDVDD	18	GND	GND
4	LCDVDD	LCDVDD	19	NC	LVDS_CLK#_R
5	EDP_HP	3D3V_ROM	20	NC	LVDS_CLK_R
6	LCD_TST_C	LCD_TST_C	21	GND	GND
7	EDP_AUX	LVDS_DDC_CLK	22	GND	GND
8	EDP_AUX#	LVDS_DDC_DAT	23	GND	GND
9	GND	GND	24	DBC_EN	DBC_EN
10	EDP_TX0N	LVDS_DATA0#	25	BRIGHTNESS	BRIGHTNESS
11	EDP_TX0P	LVDS_DATA0	26	BLON_OUT	BLON_OUT
12	GND	GND	27	Color_Engine	Color_Engine
13	EDP_TX1N	LVDS_DATA1#	28	NC	NC
14	EDP_TX1P	LVDS_DATA1	29	DCBATOUT_LCD	DCBATOUT_LCD
15	GND	GND	30	DCBATOUT_LCD	DCBATOUT_LCD

LVDS / EDP Colay Page 53
PL Page 53.

EC (BIST MODE)

eDP/ LVDS select circuit

INVERTER POWER

800mA

Touch panel

X02 remove TPNL1

0307 modify

CAMERA

Camera Power

303mA

69.50007.921

need close to connector

LCDVDD

LCD Power

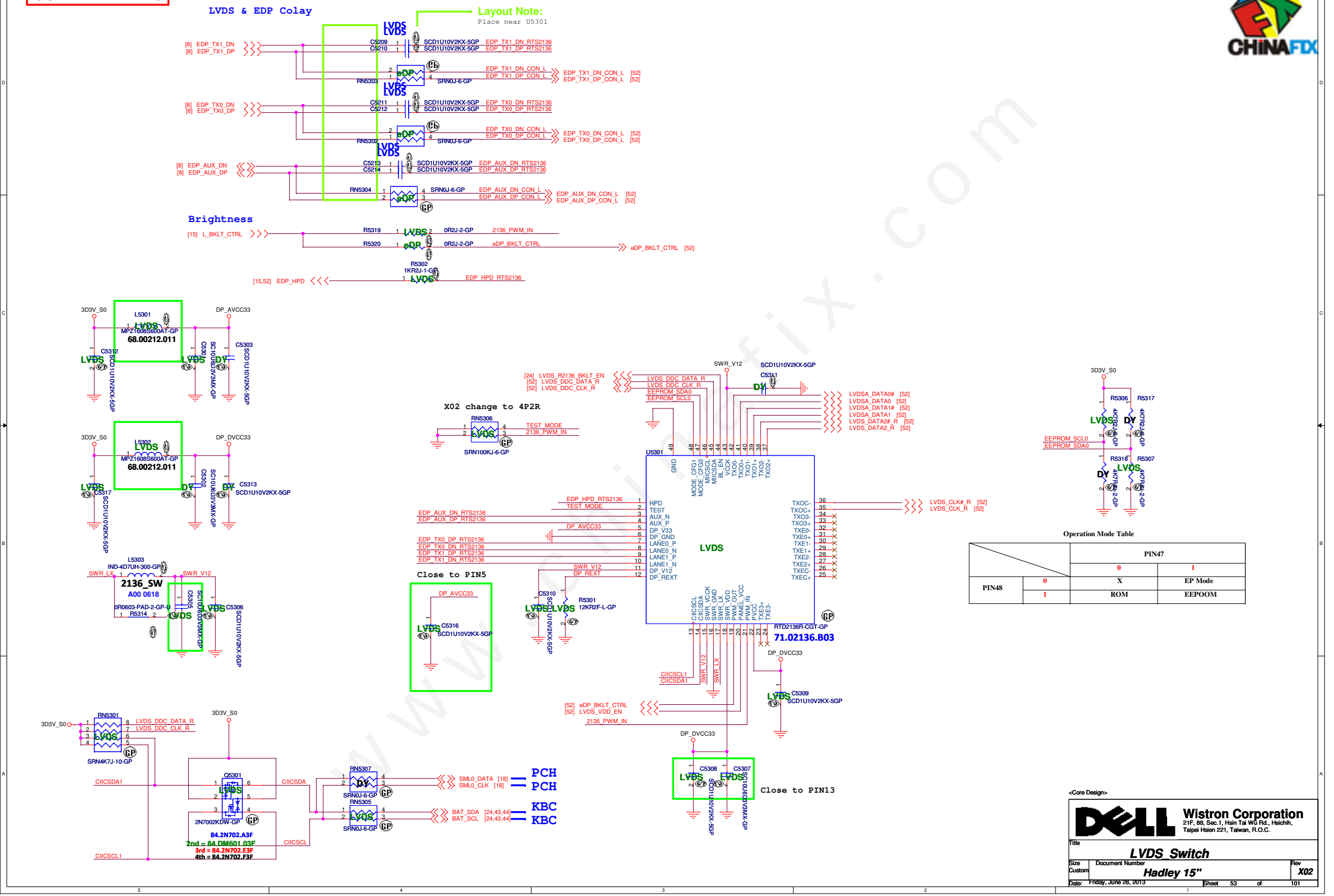
600mA

Layout Note:
Trace width = 80mil

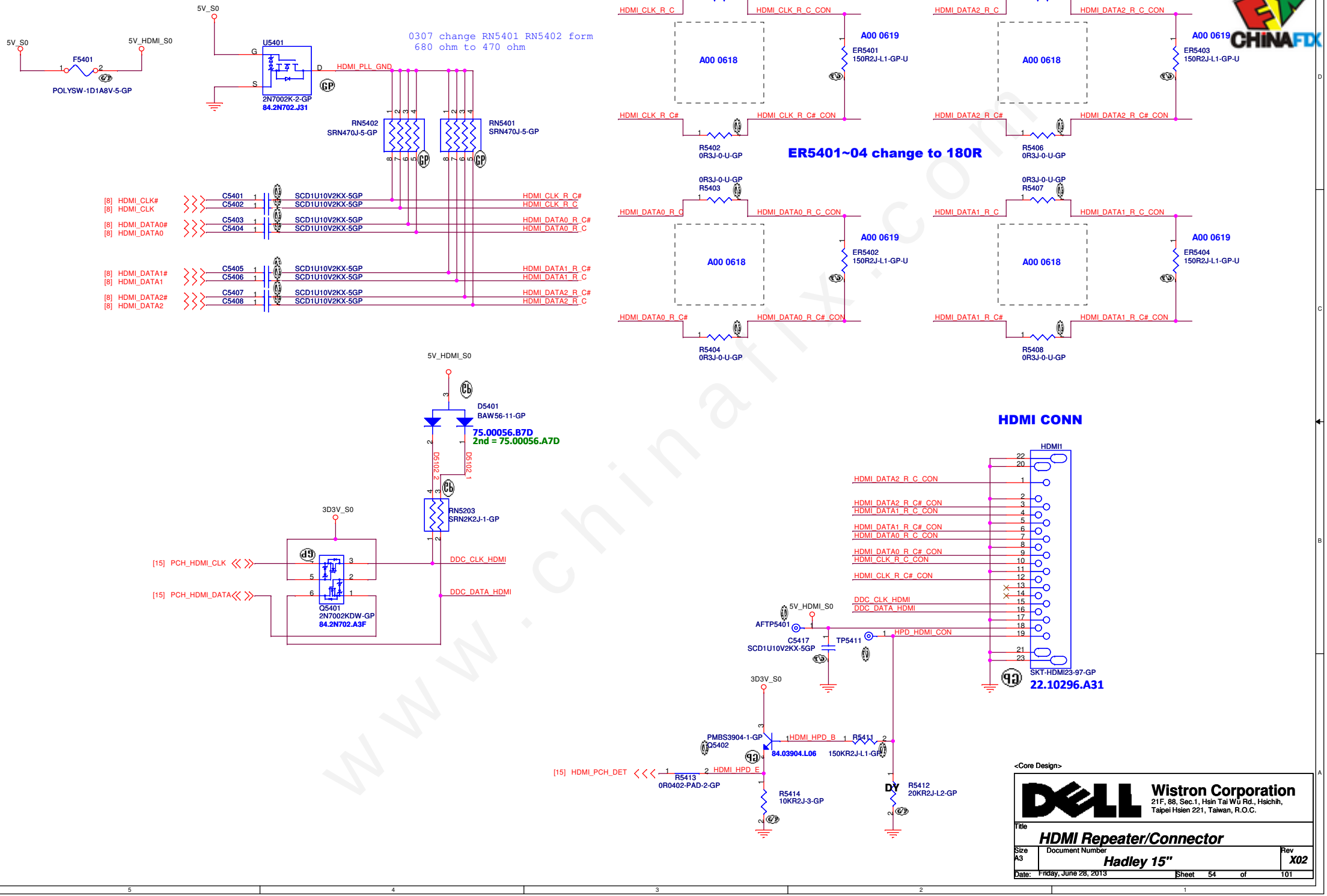
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD Connector
Size: Custom | Document Number: Hadley 15" | Rev: X02
Date: Friday, June 28, 2013 | Sheet 52 of 101

SSID = VIDEO



SSID = VIDEO



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Repeater/Connector

Size	Document Number	Rev
A3	Hadley 15"	X02

Date: Friday, June 28, 2013 Sheet 54 of 101

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<Core Design>

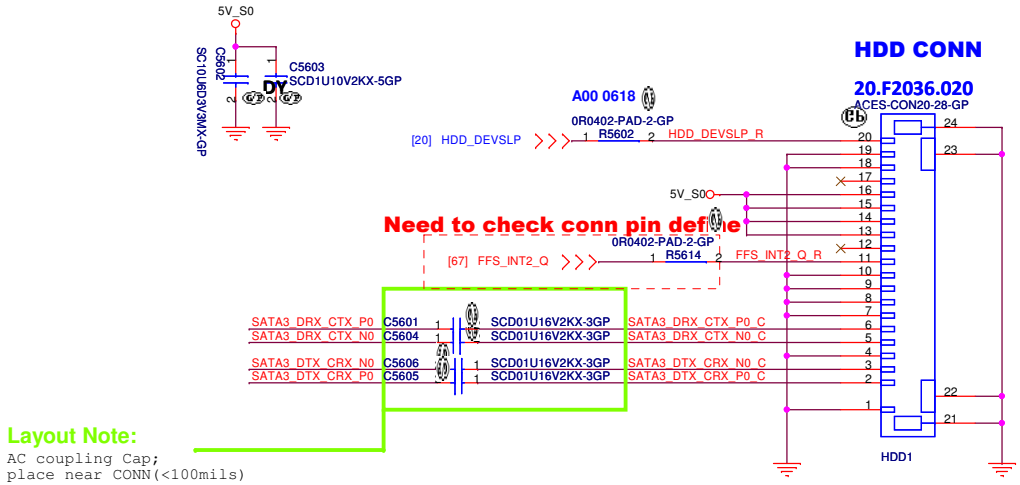
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 55 of 101

SSID = SATA



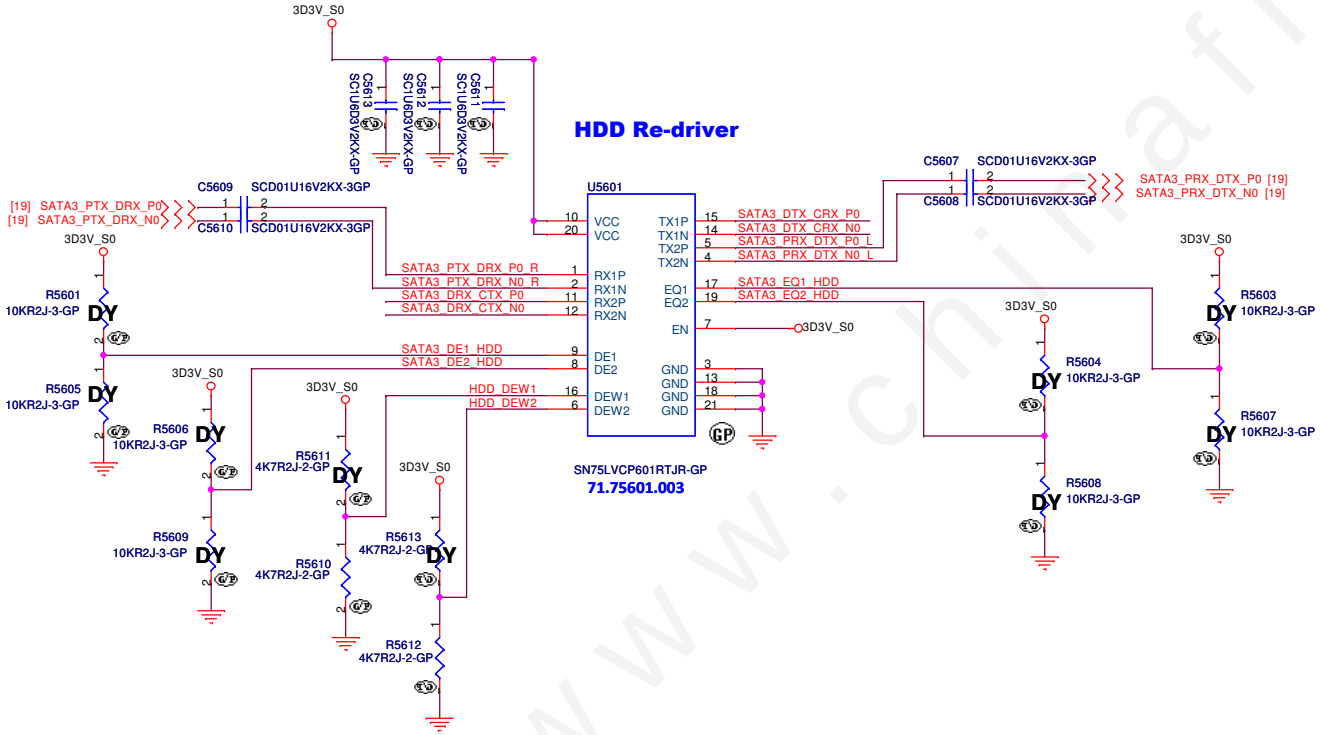


Table 1: Tx/Rx EQ & DE Pulse Width Settings

DE1/DE2	CH1/CH2De-Emphasis dB(@6Gbps
NC (*default*)	-6
0	0
1	-3

EQ1/EQ2	CH1/CH2Equalization dB (@6Gbps)
NC (*default*)	0
0	7
1	14

DEW1/DEW2	Device Function→ DE Width for CH1/CH2
0	De-Emphasis Pulse Width Short (recommended setting when link operates at SATA 1.5/3.0/6.0 Gbps)
1 (*default*)	De-Emphasis Pulse Width Long (recommended setting when link operates at SATA 1.5/3.0 Gbps speed only)

<Core Design>

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Title: HDD

Size: A3 | Document Number: Hadley 15" | Rev: X02

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<Core Design>

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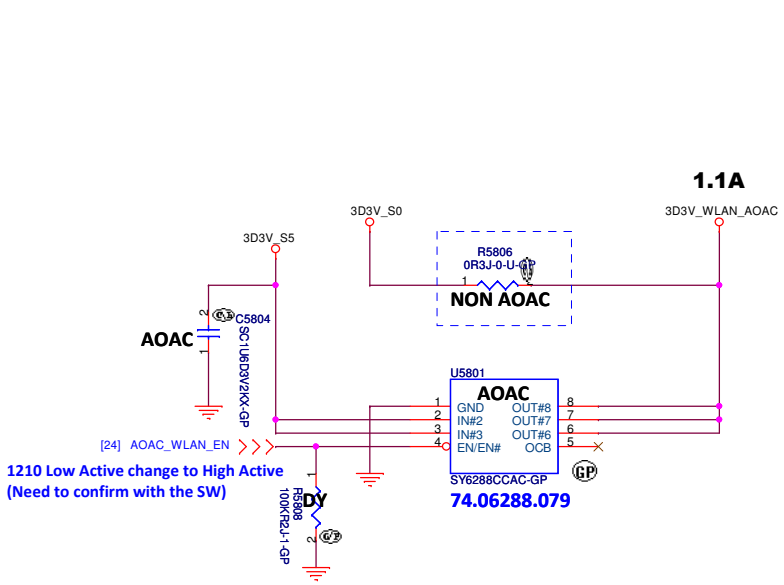
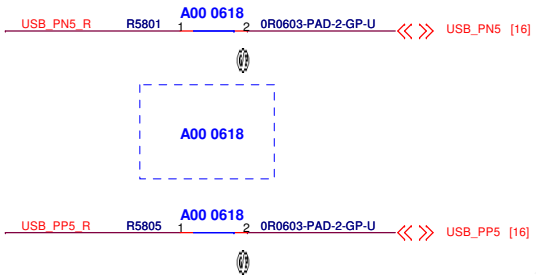
Title: Reserved

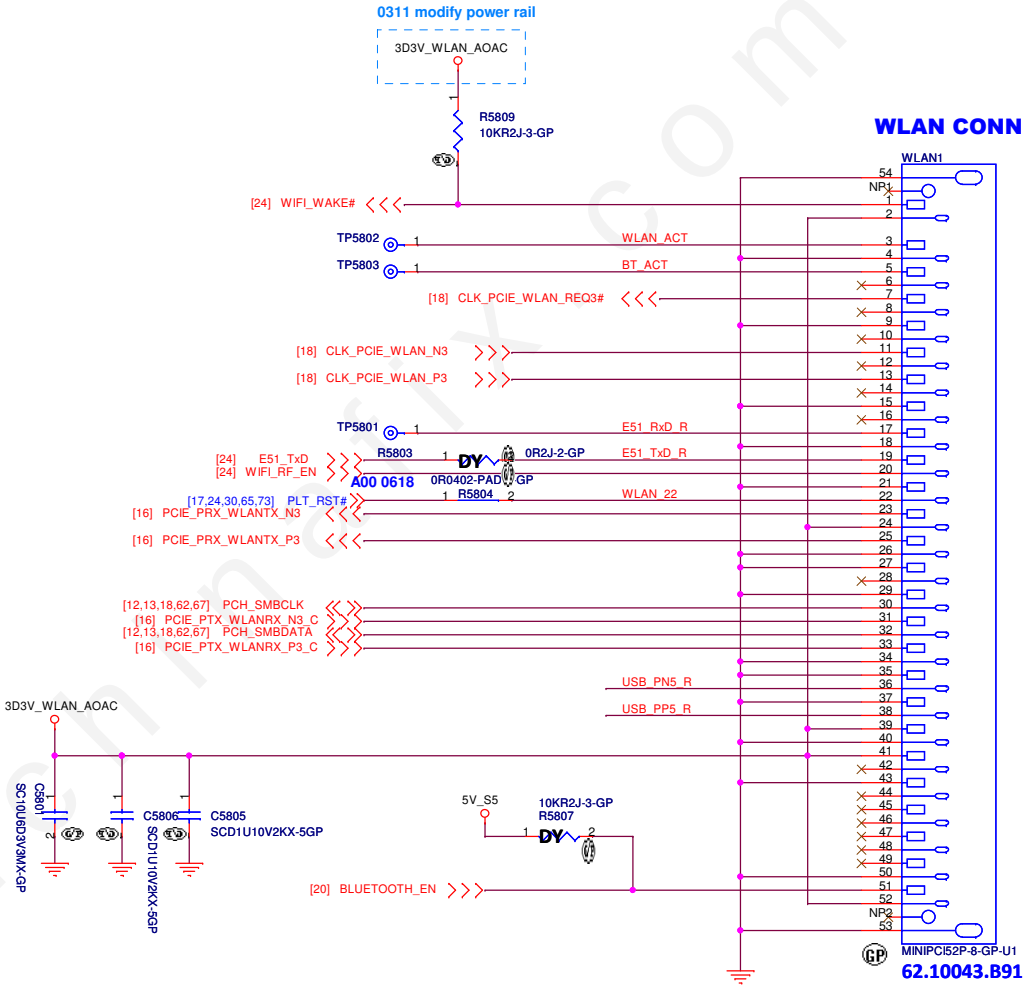
Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 57 of 101

SSID = Wireless







<Core Design>

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Title: WLAN/BT

Size	Document Number	Rev
A3	Hadley 15"	X02

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Title: Reserved

Size: A3 | Document Number: Hadley 15" | Rev: X02

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Title: Reserved

Size: A3 | Document Number: Hadley 15" | Rev: X02

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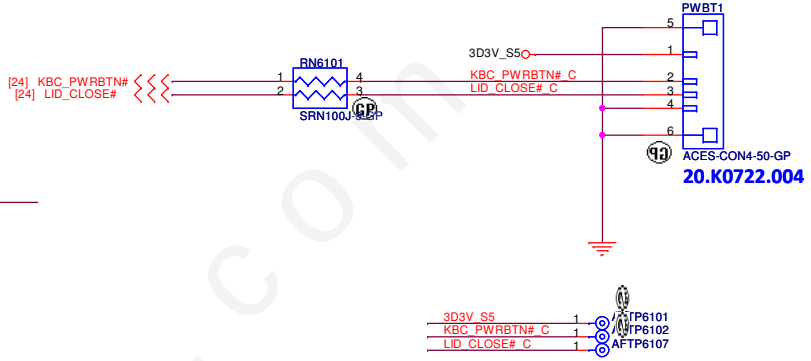
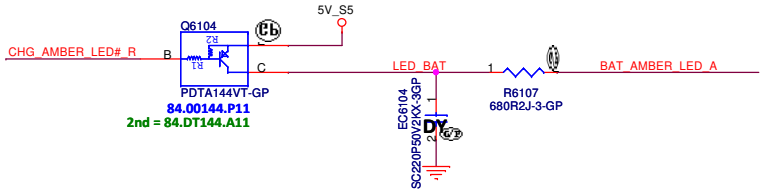
SSID = User.Interface

PWRBTN CONN



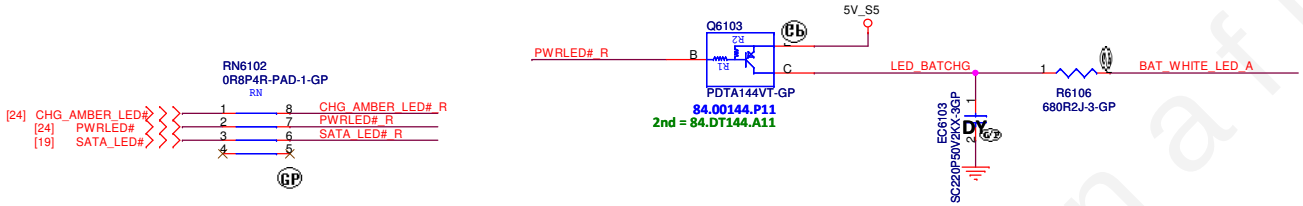
Battery LED1(Amber_LED)

LOW actived from KBC GPIO

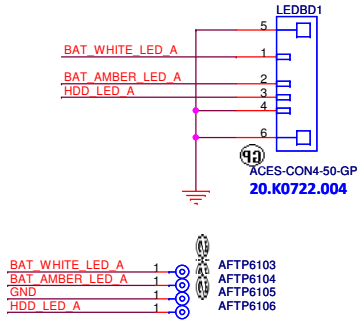


Power & Battery LED2(White_LED)

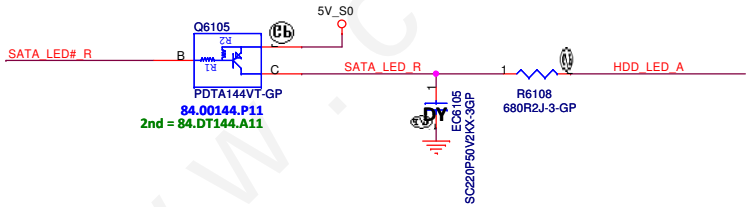
LOW actived from KBC GPIO



LED board CONN



SATA HDD LED



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Title	LED Bar/Power Button	
Size A3	Document Number: Hadley 15"	Rev: X02
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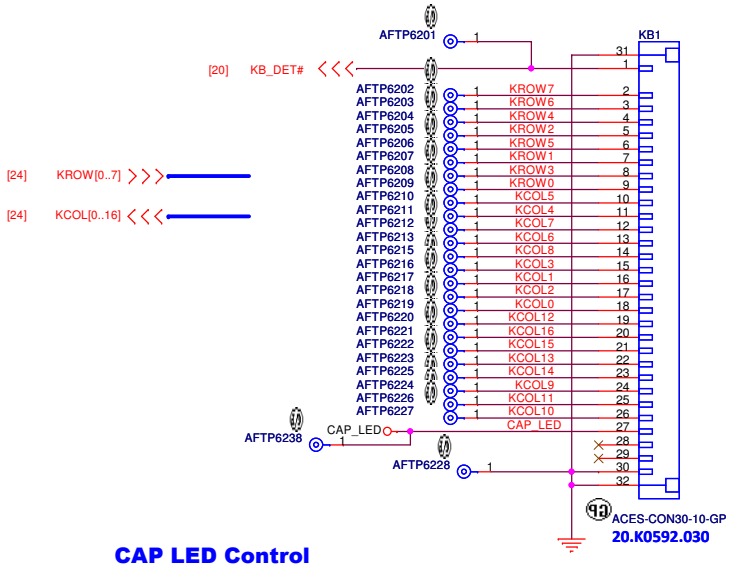
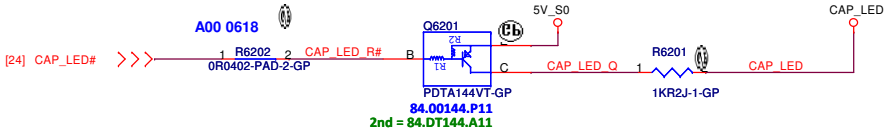
SSID = KBC

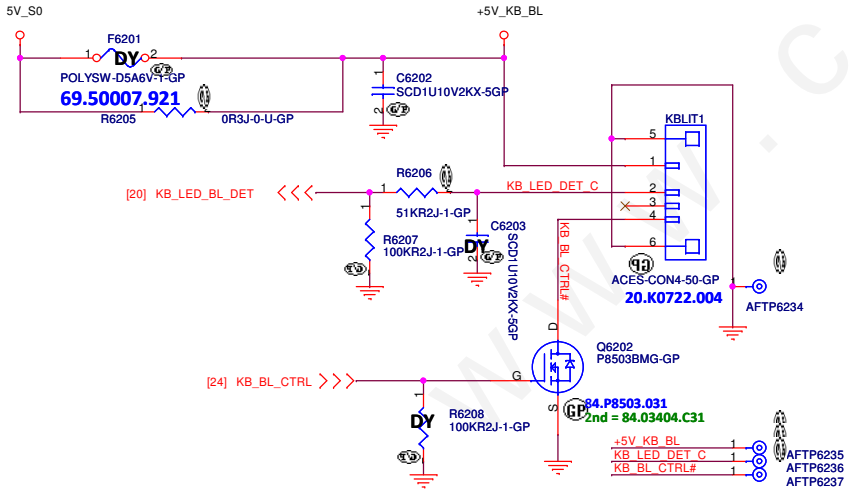
Internal Keyboard Connector



CAP LED Control

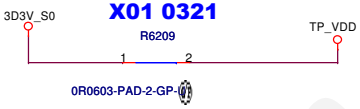
LOW actived from KBC GPIO



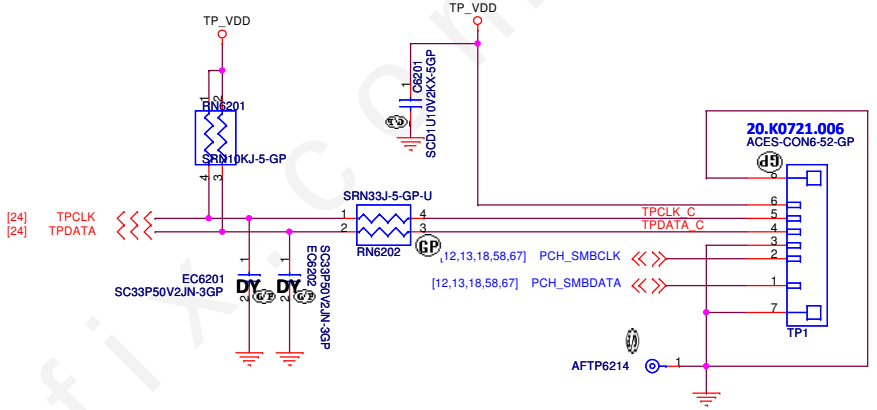


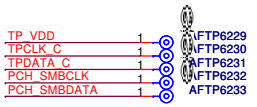
SSID = Touch.Pad

X01 0321



Touch Pad Connector





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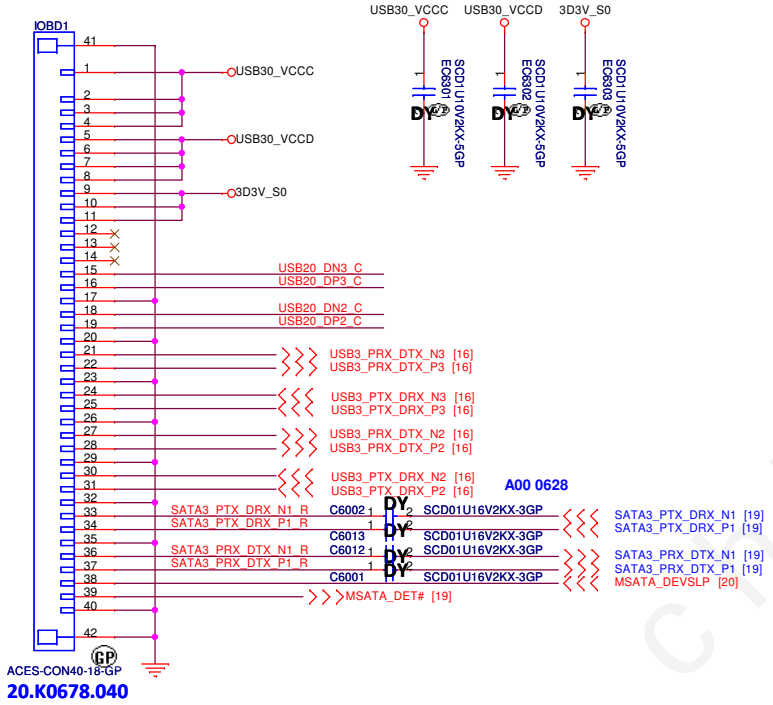
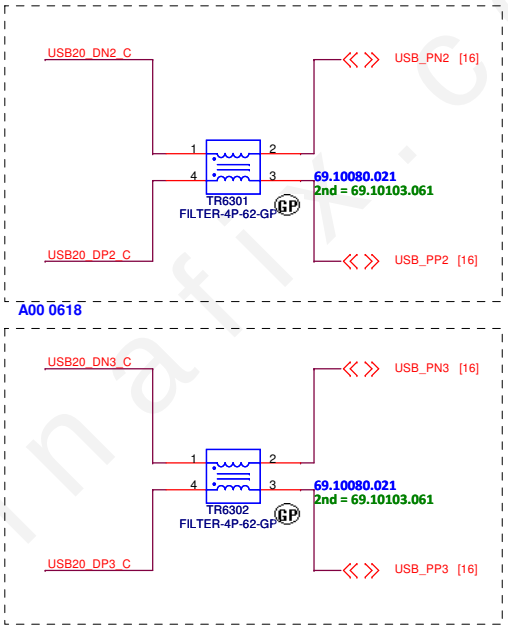
Title	Reserved	
Size A3	Document Number Hadley 15"	Rev X02
Date: Friday, June 28, 2013	Sheet 62 of 101	

SSID = User.Interface





<Core Design>

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Title: IO Board Connector

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<Core Design>

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Title: Reserved

Size: A3 | Document Number: Hadley 15" | Rev: X02

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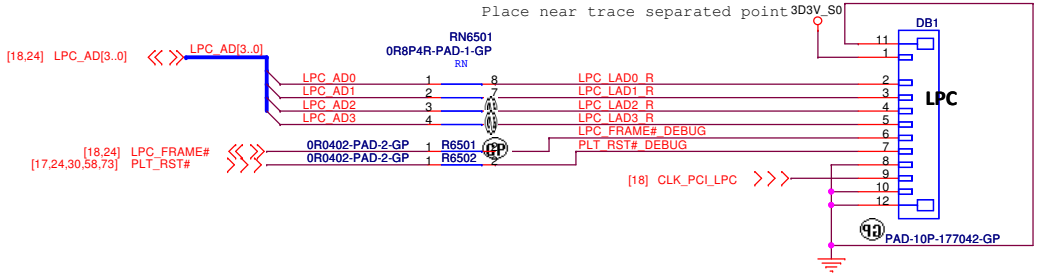
SSID = DEBUG PORT

Debug Connector

A00 0625



ZZ.00PAD.Y41

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Title	Dubug connector	
Size A3	Document Number Hadley 15"	Rev X02
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<Core Design>

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Title
Reserved

Size	Document Number	Rev
A4	Hadley 15"	X02

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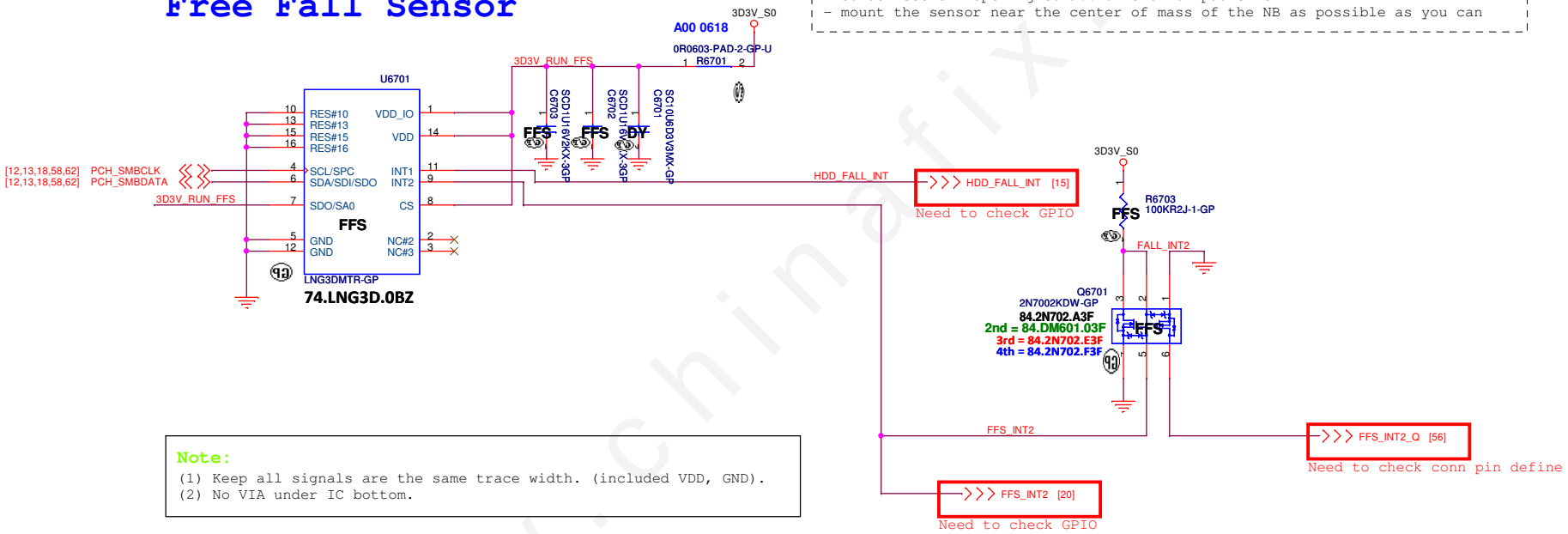
SSID = User.Interface

Free Fall Sensor

Note:
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



Note:
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

<Core Design>

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Title: FFS		
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Title: Reserved

Size: A3 | Document Number: Hadley 15" | Rev: X02

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Title: Reserved

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Title: Reserved

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Title: Reserved

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SSID = VIDEO

dGPU Reset

D7301 1SS400GPT-GP
83.00400.C1F
2ND = 83.27101.01F
3RD = 83.01426.01F
A00 0618
0R0402-PAD-2-GP

[17,24,30,58,65] PLT_RST#
[15] DGPU_HOLD_RST#
R7304
VGA_RST# [76]

3D3V_VGA_S0
Q7301 2N7002K-2-GP
84.2N702.J31
R7308 10KR2J-3-GP
R7305 0R2J-2-GP
[18] PEG_CLKREQ#

GPU1A 1 OF 17
1/17 PCI_EXPRESS

GK107/GF108 GK208/GF117
NC

PEX_WAKE# AJ11
PEX_RST# AJ12 ← VGA_RST#
PEX_CLKREQ# AK12 ← GPU_CLKREQ#
PEX_REFCLK AL13 ← [18] CLK_PCIE_VGA
PEX_REFCLK# AK13 ← [18] CLK_PCIE_VGA#

[16] CPU_RXP_C_dGPU_TXP0	C7301 SCD22U10V2KX-1GP	dGPU_TXP_CPU_RXP0	PEX_TX0 AK14
[16] CPU_RXN_C_dGPU_TXN0	C7302 SCD22U10V2KX-1GP	dGPU_TXN_CPU_RXN0	PEX_TX0# AJ14
[16] dGPU_RXP_C_CPU_TXP0			PEX_RX0 AN12
[16] dGPU_RXN_C_CPU_TXN0			PEX_RX0# AM12
[16] CPU_RXP_C_dGPU_TXP1	C7303 SCD22U10V2KX-1GP	dGPU_TXP_CPU_RXP1	PEX_TX1 AH14
[16] CPU_RXN_C_dGPU_TXN1	C7304 SCD22U10V2KX-1GP	dGPU_TXN_CPU_RXN1	PEX_TX1# AG14
[16] dGPU_RXP_C_CPU_TXP1			PEX_RX1 AN14
[16] dGPU_RXN_C_CPU_TXN1			PEX_RX1# AM14
[16] CPU_RXP_C_dGPU_TXP2	C7305 SCD22U10V2KX-1GP	dGPU_TXP_CPU_RXP2	PEX_TX2 AK15
[16] CPU_RXN_C_dGPU_TXN2	C7306 SCD22U10V2KX-1GP	dGPU_TXN_CPU_RXN2	PEX_TX2# AJ15
[16] dGPU_RXP_C_CPU_TXP2			PEX_RX2 AP14
[16] dGPU_RXN_C_CPU_TXN2			PEX_RX2# AP15
[16] CPU_RXP_C_dGPU_TXP3	C7307 SCD22U10V2KX-1GP	dGPU_TXP_CPU_RXP3	PEX_TX3 AL16
[16] CPU_RXN_C_dGPU_TXN3	C7308 SCD22U10V2KX-1GP	dGPU_TXN_CPU_RXN3	PEX_TX3# AK16
[16] dGPU_RXP_C_CPU_TXP3			PEX_RX3 AN15
[16] dGPU_RXN_C_CPU_TXN3			PEX_RX3# AM15

PEX_TX4 AK17
PEX_TX4# AJ17
PEX_RX4 AN17
PEX_RX4# AM17
PEX_TX5 AH17
PEX_TX5# AG17
PEX_RX5 AP17
PEX_RX5# AP18
PEX_TX6 AK18
PEX_TX6# AJ18
PEX_RX6 AN18
PEX_RX6# AM18
PEX_TX7 AL19
PEX_TX7# AK19
PEX_RX7 AN20
PEX_RX7# AM20
PEX_TX8 AK20
PEX_TX8# AJ20
PEX_RX8 AP20
PEX_RX8# AP21
PEX_TX9 AH20
PEX_TX9# AG20
PEX_RX9 AN21
PEX_RX9# AM21
PEX_TX10 AK21
PEX_TX10# AJ21
PEX_RX10 AN23
PEX_RX10# AM23
PEX_TX11 AL22
PEX_TX11# AK22
PEX_RX11 AP23
PEX_RX11# AP24
PEX_TX12 AK23
PEX_TX12# AJ23
PEX_RX12 AN24
PEX_RX12# AM24
PEX_TX13 AH23
PEX_TX13# AG23
PEX_RX13 AN26
PEX_RX13# AM26
PEX_TX14 AK24
PEX_TX14# AJ24
PEX_RX14 AP26
PEX_RX14# AP27
PEX_TX15 AL25
PEX_TX15# AK25
PEX_RX15 AN27
PEX_RX15# AM27

PEX LANES 8 TO 15 NC FOR GF117/GK208

OPS

N14P-GS-A1-GP
71.0N14P.00U

GF108	GK208/GK107/GF117
NC	PEX_PLL_HVDD AH12
	PEX_SVDD_3V3 AG12

PEX_IOVDD_1 AG19
PEX_IOVDD_2 AG21
PEX_IOVDD_3 AG22
PEX_IOVDD_4 AG24
PEX_IOVDD_5 AH21
PEX_IOVDD_6 AH25

1D05V_VGA_S0
C7323 SC10U6D3V3MX-GP
C7310 SC10U6D3V3MX-GP
C7322 SC10U6D3V3MX-GP
C7312 SC1U6D3V2KX-GP
C7313 SC1U6D3V2KX-GP
C7325 SC10U6D3V3MX-GP
C7326 SC10U6D3V3MX-GP

1.05V +/- 30mV
3.3A

PEX_IOVDDQ_1 AG13
PEX_IOVDDQ_2 AG15
PEX_IOVDDQ_3 AG16
PEX_IOVDDQ_4 AG18
PEX_IOVDDQ_5 AG25
PEX_IOVDDQ_6 AH15
PEX_IOVDDQ_7 AH18
PEX_IOVDDQ_8 AH26
PEX_IOVDDQ_9 AH27
PEX_IOVDDQ_10 AJ27
PEX_IOVDDQ_11 AK27
PEX_IOVDDQ_12 AL27
PEX_IOVDDQ_13 AM28
PEX_IOVDDQ_14 AN28

1D05V_VGA_S0
C7320 SC10U6D3V3MX-GP
C7321 SC10U6D3V3MX-GP
C7309 SC4D7U6D3V3KX-GP
C7311 SC1U6D3V2KX-GP
C7314 SC1U6D3V2KX-GP
C7327 SC10U6D3V3MX-GP
C7328 SC4D7U6D3V3KX-GP

3.3V +/- 5%
210mA

3D3V_VGA_S0
C7316 SC1U10V2KX-5GP
C7315 SC4D7U6D3V3KX-GP
C7324 SC4D7U6D3V3KX-GP

X7R, Under GPU.

POWER IC

VDD_SENSE L4 → VGA_SENSE [82]
GND_SENSE L5 → GND_SENSE [82]
NC_3V3AUX P8

R7303 200R2F-L-GP
PEX_TSTCLK_OUT AJ26 PEXTSTCLK_OUT
PEX_TSTCLK_OUT# AK26 PEXTSTCLK_OUT#

1.05V +/- 30mV
150mA

1D05V_VGA_S0
PEX_PLLVDD AG26
C7318 SC1U10V2KX-5GP
C7317 SC4D7U6D3V3KX-GP
C7319 SC1U6D3V2KX-GP

0102 remove R7307

TESTMODE AK11 TESTMODE
R7302 10KR2J-3-GP
PEX_TERMP AP29 PEX_TERMP
R7301 2K49R2F-GP

<Core Design>

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Title: GPU_PCIE/STRAPPING(1/5)
Size: Custom | Document Number: Hadley 15" | Rev: X02
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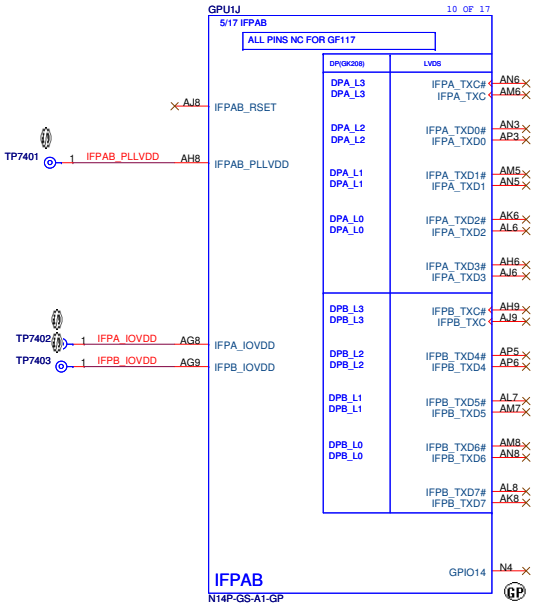
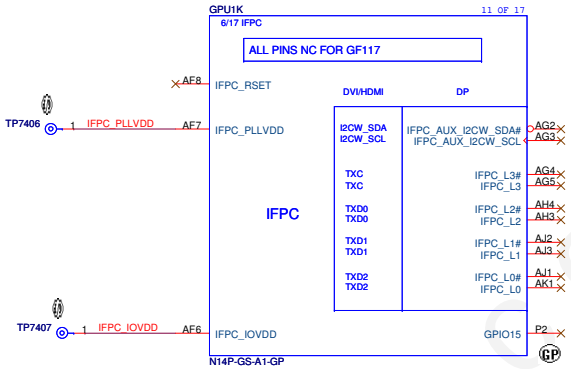
SSID = VIDEO



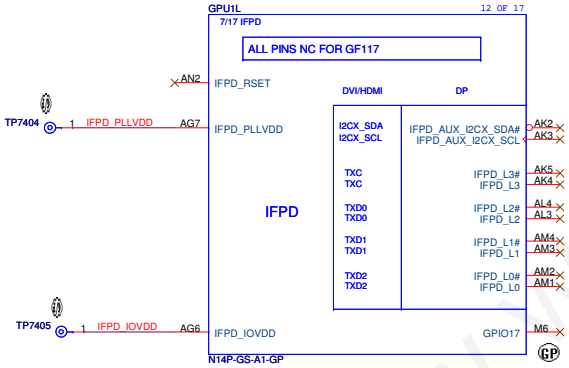
71.0N14P.00U

OPS



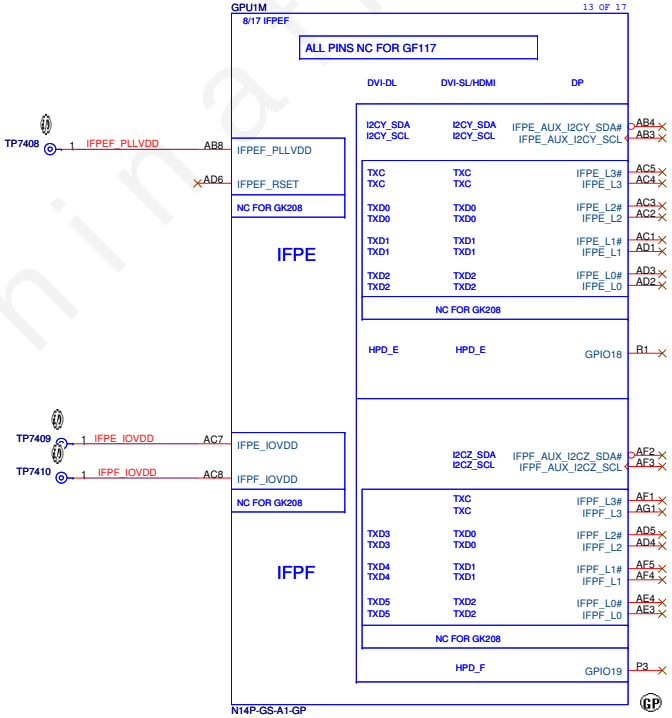
71.0N14P.00U

OPS



71.0N14P.00U

OPS



71.0N14P.00U

OPS

<Core Design>

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Title: GPU Memory(2/5)

Size	Document Number	Rev
Custom	Hadley 15"	X02

Date: Friday, June 28, 2013 Sheet 74 of 101

SSID = VIDEO

A00 0618

0102 remove L7502
change K27 pin net name

Layout note:FBA_PLL_AVDD=16mil
Place close to Ball

0102 remove L7503
change C7506 to 0603 package

Place under GPU near

THE FBA_WCKBxx PINS ARE USED ONLY ON GK107 THEY ARE NC FOR GK208/GF108 /GF117

THE FBB_WCKBxx PINS ARE USED ONLY ON GK107 THEY ARE NC FOR GF108

ALL PINS NC FOR GF117/GK208

1.35V +/- 3%
4.88A

GPU FBVDDQ Decoupling
PLACE CLOSE TO GPU BALLS

PLACE CLOSE TO GPU BALLS

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DP/LVDS/CRT/GPIO(3/5)

Size: A2 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 28, 2013 | Sheet 75 of 101

SSID = VIDEO

NV request to need to be keeped

Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

GPU Product Name	N14P-GT
NV-Internal Chip Part# (used on labels of packaging bag/box materials)	GK107-750
Device ID	0x0FE4
Memory interface	GDDR5
Package	GB4-128

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed WCK (MHz)	Memory Date Code Minimum	Status
128Mx16 GDDR5	Hynix	0x6	1.35V/ 1.35V	H5GQ2H24AFR-T2C	2000	N/A	Production candidate
	Samsung	0x7	1.35V/ 1.35V	K4G20325FD-FC04	2000	1219	Post-production candidate

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	0	0	1	0
15K PD	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
Hynix 35K PD	0	1	1	0
Samsung 45K PD	0	1	1	1
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
5K PH	1	0	0	0
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
45K PH	1	1	1	1
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
5K PD	0	0	0	0
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
25K PD	0	1	0	0
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
5K PD	0	0	0	0
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
45K PD	0	1	1	1
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

0102 remove 0R

DA-05691-001_V05 P15
GPIO20/21 NC : for ALL

DA-05691-001_V05 P6
NC : N13P-GS

EA40-HW SC

N14P-GT

71.0N14P.00U

OPS

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Title: Reserved

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SSID = VIDEO

VGA_CORE

Under GPU **N14P-GT : 45A**

C7709 C7707 C7708 C7706 C7702 C7701 — OPS — SC4D7U6D3V3KX-GP

C7725 C7722 C7723 C7724 C7721 C7720 C7719 — OPS — SC4D7U6D3V3KX-GP

C7716 C7715 C7718 C7717 C7714 C7713 C7712 C7711 — OPS — SC1U6D3V2KX-GP

NEAR TO GPU

C7703 C7705 C7710 — OPS — SC010U6D3V3MX-GP

R7701 — UMA — 0R0J-0U-GP

GPU1H 8 OF 17 — 13/17 NVVDD

VDD_1 … VDD_72

N14P-GS-A1-GP

71.0N14P.00U

OPS

GPU1F 6 OF 17 — 15/17 GND_1/2

GND_1 … GND_140

N14P-GS-A1-GP

71.0N14P.00U

OPS

GPU1G 7 OF 17 — 16/17 GND_2/2

GND_141 … GND_198

AG11 GND_F GND_H AH11

GND_OPT_1 GND_OPT_2 C16 W32

Optional CMD GNDs (2)
NC for 4-Lyr cards

N14P-GS-A1-GP

71.0N14P.00U

OPS

GPU1I 9 OF 17 — 9/17 XVDD

CONFIGURABLE POWER CHANNELS

XVDD_1 … XVDD_38

N14P-GS-A1-GP

71.0N14P.00U

OPS

GPU1E 5 OF 17 — 17/17 NC/VDD33

DA-05691-001_V05 P20
3V3MISC : N13P-GS

GK107	GK208 GF117
3V3MISC	3V3MISC_1
3V3MISC	3V3MISC_2

VDD33_1 VDD33_2

NC#AJ28 NC#C15 NC#D19 NC#D20 NC#D23 NC#D26 NC#H31 NC#V32

DNU#AC6 DNU#AJ4 DNU#AJ5 DNU#AL11 DNU#T8 — DO NOT CONNECT THESE PINS

N14P-GS-A1-GP

71.0N14P.00U

OPS

3.3V +/- 5%
85mA

3D3V_VGA_S0

C7704 C7729 C7727 C7728 — X7R — OPS — SC1U10V2KX-5GP / SC1U6D3V2KX-GP

0.1U Under GPU

4.7U NEAR TO GPU

1U NEAR TO GPU

<Core Design>

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Title: GPU_POWER(4/5)

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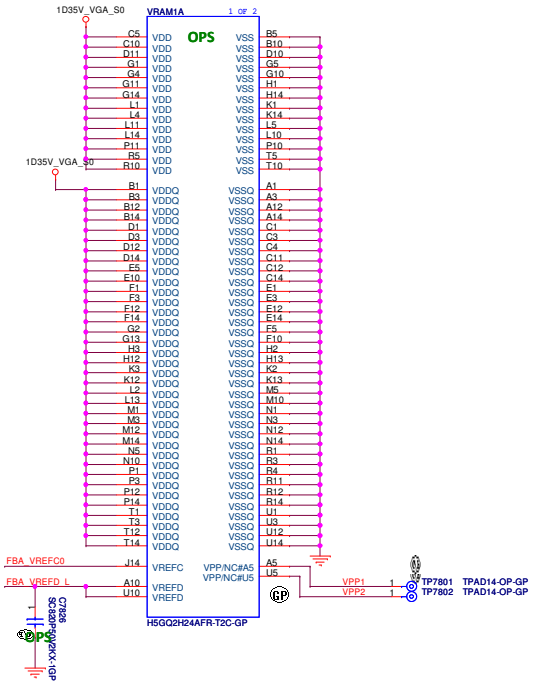
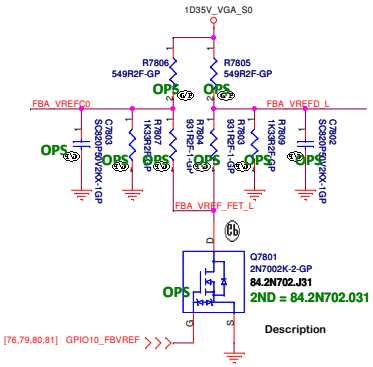
SSID = VIDEO

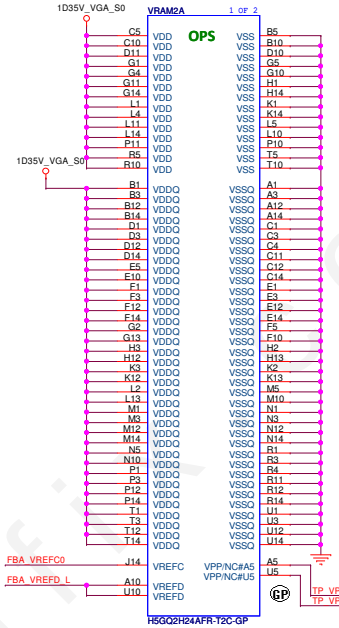


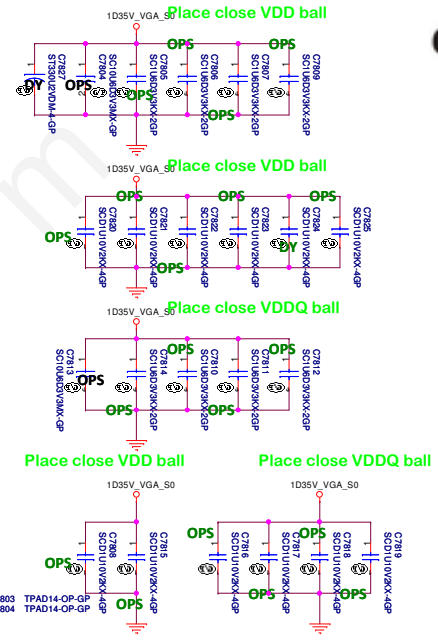
Frame Buffer Patition A-Lower Half



FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

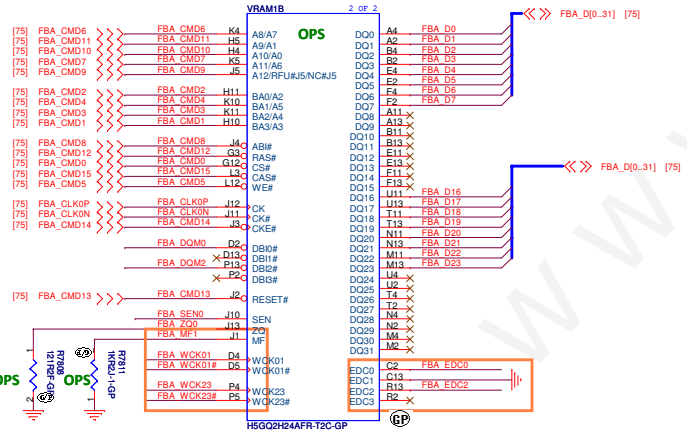




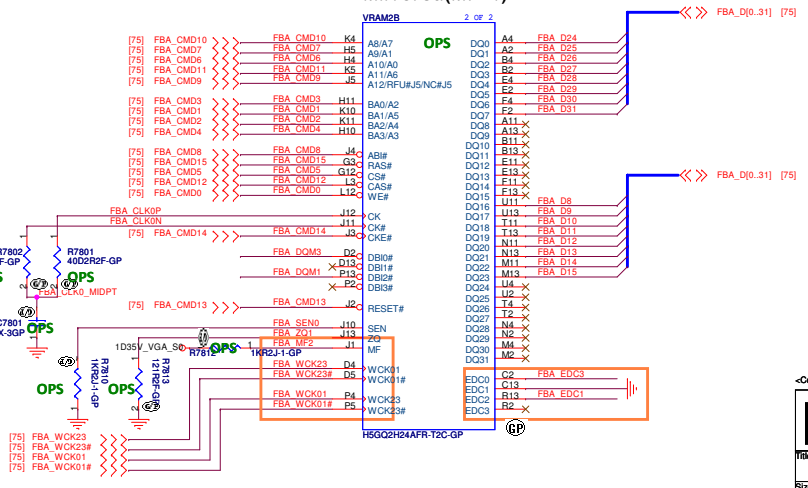
[75] FBA_EDC[0..3] FBA_EDC0 FBA_EDC1 FBA_EDC2 FBA_EDC3

FBA_DQM0 FBA_DQM1 FBA_DQM2 FBA_DQM3 FBA_DQM[0..3] [75]

Normal(MF=0)



Mirrored(MF=1)



<Core Design>

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Title: GPU-VRAM1,2 (1/4)

Size: Custom | Document Number: Hadley 15" | Rev: X02

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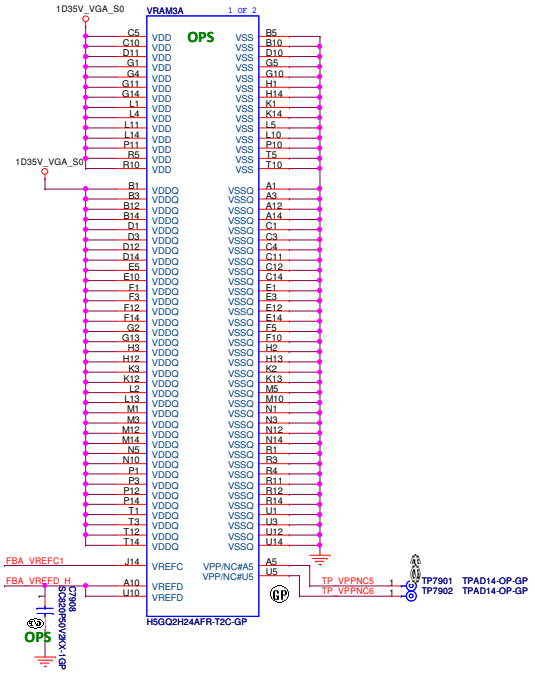
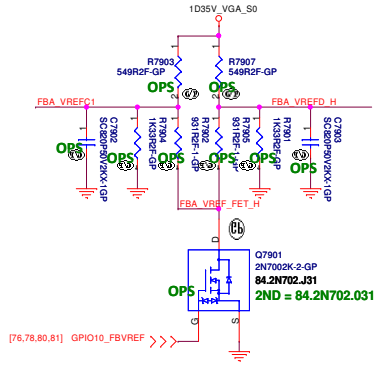
SSID = VIDEO

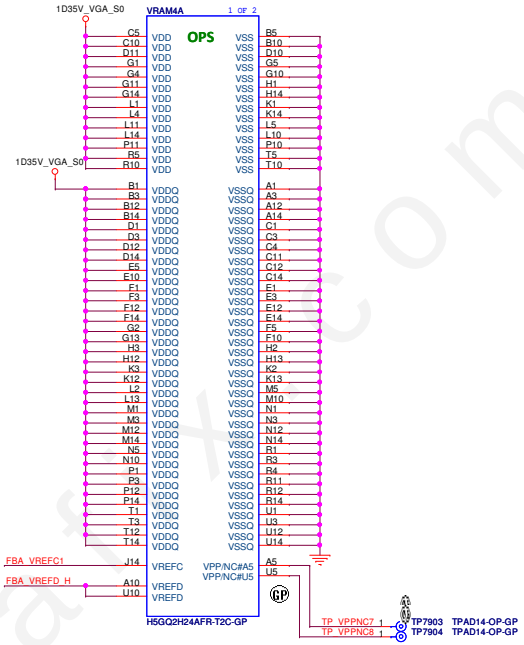


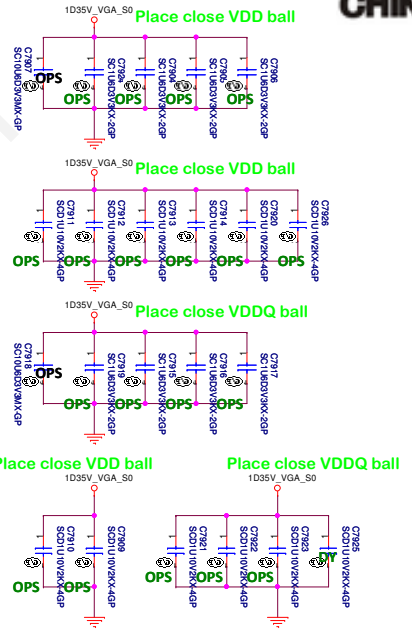
Frame Buffer Patition A-Upper Half

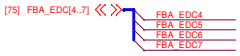


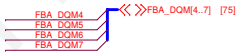
FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low









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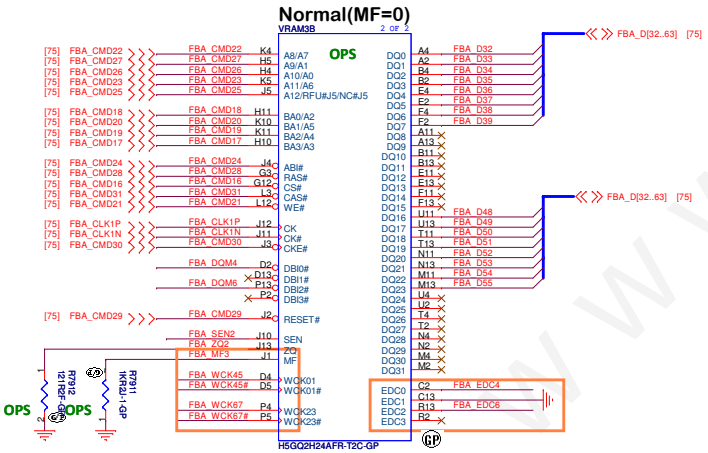

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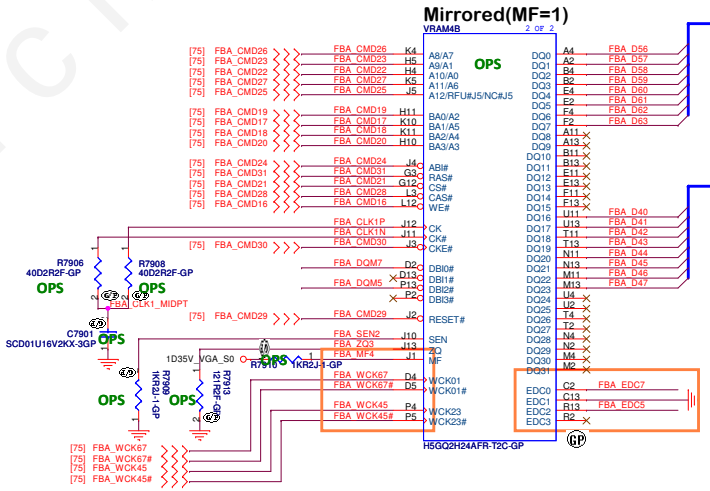

<Core Design>

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Title: GPU-VRAM3,4 (2/4)

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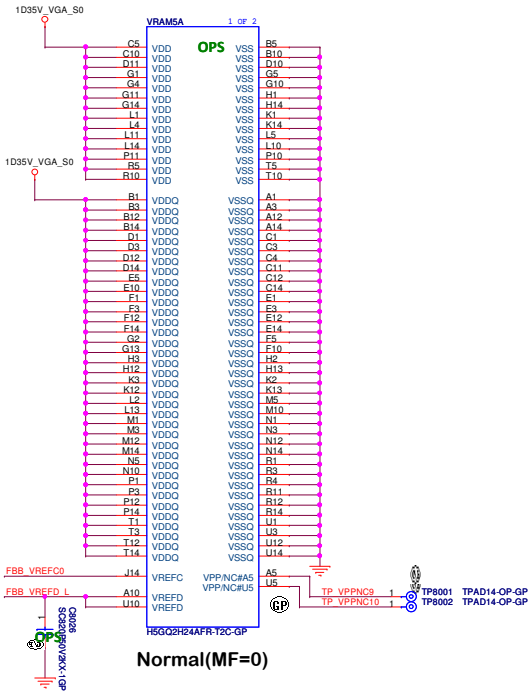
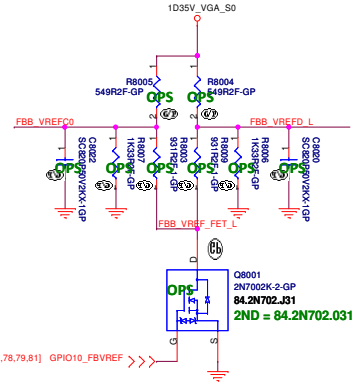
SSID = VIDEO



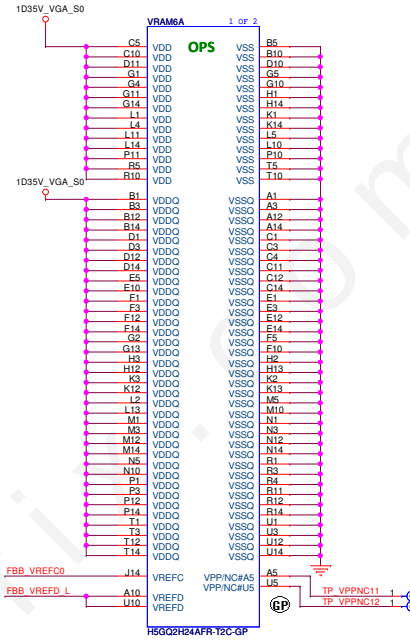
Normal(MF=0)

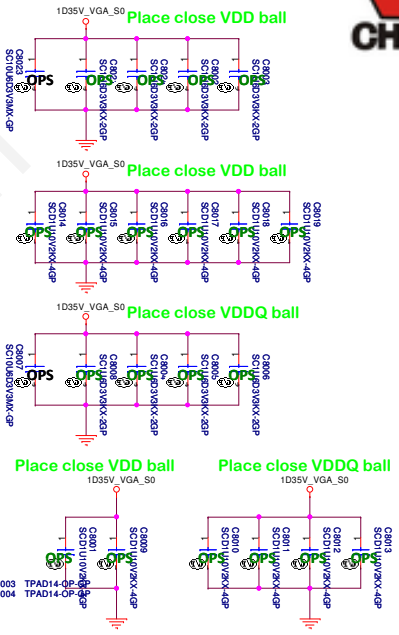
Frame Buffer Patition B-Lower Half

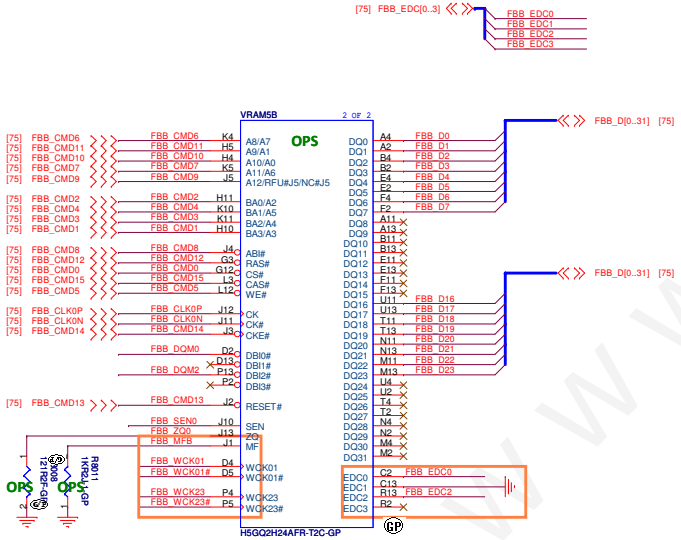


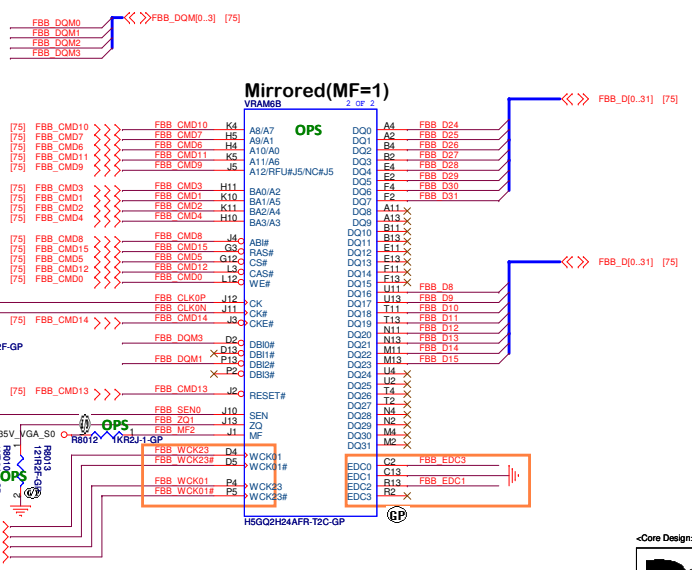
FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low









<Core Design>

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Title: GPU-VRAM5,6 (3/4)

Size	Document Number	Rev
Custom	Hadley 15"	X02

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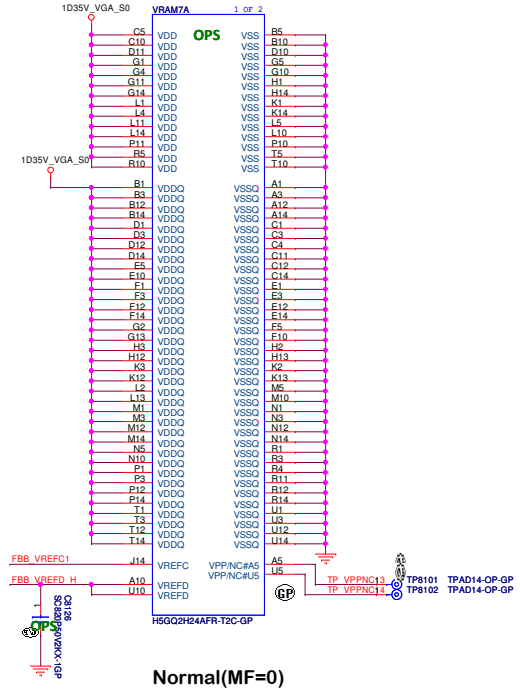
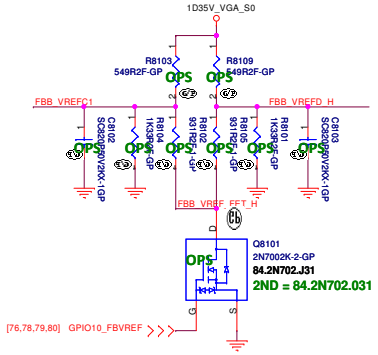
SSID = VIDEO



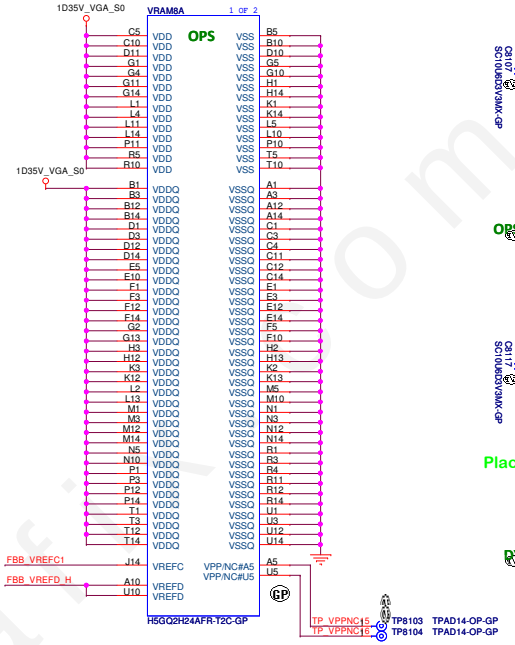
Normal(MF=0)

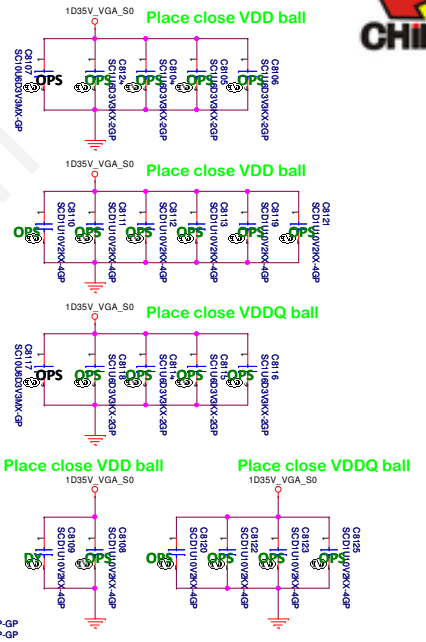
Frame Buffer Patition B-Upper Half



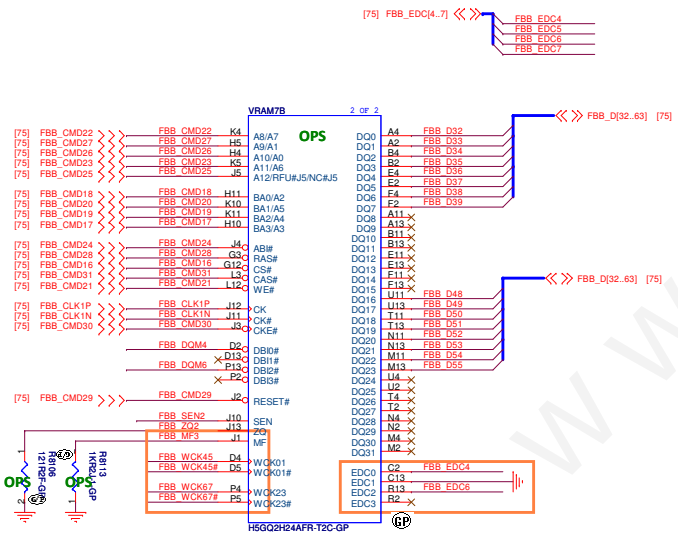
FBVREF Termination

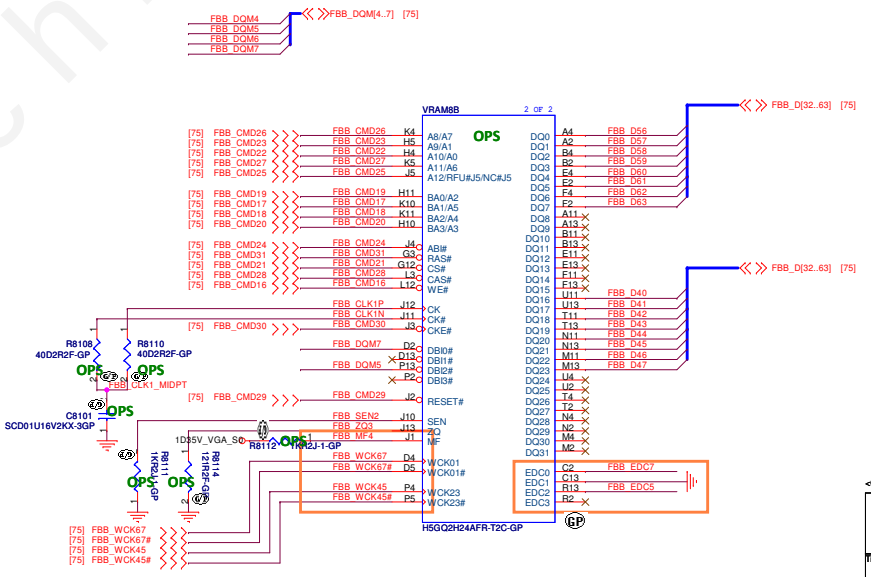
Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low





Mirrored(MF=1)





<Core Design>

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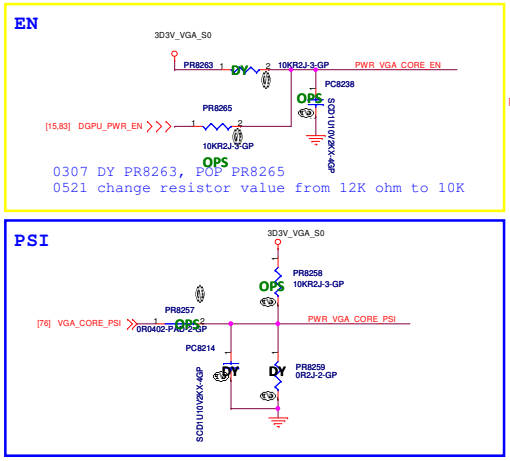
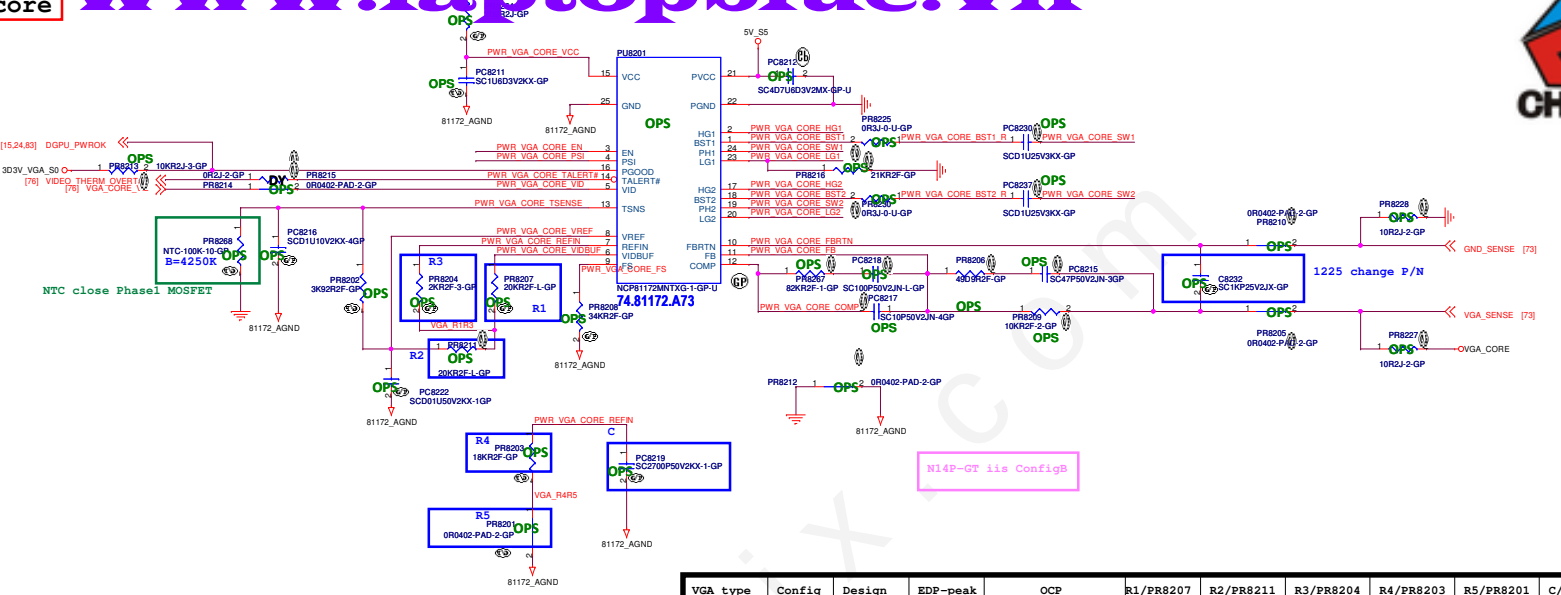
Title: GPU-VRAM7,8 (4/4)

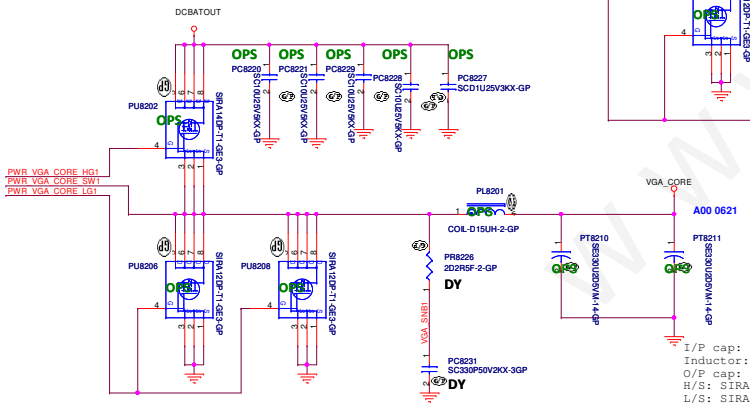
Size: Custom | Document Number: Hadley 15" | Rev: X02

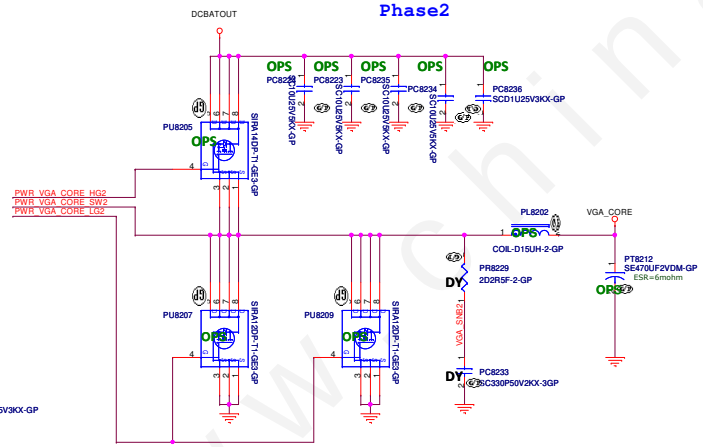
Date: Friday, June 28, 2013 | Sheet 81 of 101

SSID = PWR.Plane.Regulator_vga_core









VGA type	Config	Design Current	EDP-peak	OCP	R1/PR8207	R2/PR8211	R3/PR8204	R4/PR8203	R5/PR8201	C/PC8219
N14P-LP	B	25A	35A	38.5A<OCP<45.5A	20K	20K	2K	18K	0	2.7nF
N14P-GE	B	27A	40A	44A<OCP<52A	20K	20K	2K	18K	0	2.7nF
N14P-GS	B	38A	60A	66A<OCP<78A	20K	20K	2K	18K	0	2.7nF
N14P-GT	B	45A	75A	82.5A<OCP<97.5A	20K	20K	2K	18K	0	2.7nF
N14P-GV	B	24A	35A	38.5A<OCP<45.5A	20K	20K	2K	18K	0	2.7nF
N14P-GV2	B	32A	55A	60.5A<OCP<71.5A	20K	20K	2K	18K	0	2.7nF
N14M-GS	B	26A	45A	49.5A<OCP<58.5A	20K	20K	2K	18K	0	2.7nF
N14M-LP	B	22A	35A	38.5A<OCP<45.5A	20K	20K	2K	18K	0	2.7nF
N14M-GL	C	24.33A	35.42A	38.96A<OCP<46.04A	39K	30K	3K	24K	3K	1.8nF
N14M-GE	C	35A	40.89A	44.98A<OCP<53.16A	39K	30K	3K	24K	3K	1.8nF
N14E-GTX	A	95A	125A	137.5A<OCP<162.5A	39K	39K	1.5K	30K	1.5K	1.5nF
N14E-GS	B	65.16A	87.87A	96.66A<OCP<114.2A	20K	20K	2K	18K	0	2.7nF
N14E-GE-B	B	65.37A	98.6A	108.5A<OCP<128.2A	20K	20K	2K	18K	0	2.7nF
N14E-GE	B	65.37A	98.6A	108.5A<OCP<128.2A	20K	20K	2K	18K	0	2.7nF
N14E-GL	B	46.35A	71.83A	79.01A<OCP<93.98A	20K	20K	2K	18K	0	2.7nF

Table 1. PWM-VID Spec and Component Values

PWM-VID Spec				
		Config A	Config B	Config C
Vmin	V	0.6	0.6	0.65
Vmax	V	1.2	1.2	1.15
Vboot	V	0.875	0.9	0.9
Voltage Step Vstep	mV	6.25	6.25	25
Number of Voltage Levels N	level	96	96	20
PWM Frequency F_{PWM}	MHz	1.125	1.125	0.676
PWM Minimum Pulse Width T_{DMIN}	ns	9.26	9.26	74
VID Transient Time T	us	<100	<100	<100
Component Value				
R1 (1%)	KΩ	39	20	39
R2 (1%)	KΩ	39	20	30
R3 (1%)	KΩ	1.5	2	3
R4 (1%)	KΩ	30	18	24
R5 (1%)	KΩ	1.5	0	3
C	nF	1.5	2.7	1.8

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 0.22UH M PCMC063T-R22MN/ 2.8mohm/ Isat =40A rms /68.R22M-10V
O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L
H/S: SIRA14DP-T1-GE3 / 6.8mohm/8.5mOhm@4.5Vgs/ 84.A14DP.037
L/S: SIRA12DP-T1-GE3 / 4.4mohm/6mOhm@4.5Vgs/ 84.SRA12.037

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: NCP81172_VGA_CORE

Size: A2 | Document Number: Hadley 15" | Rev: X02

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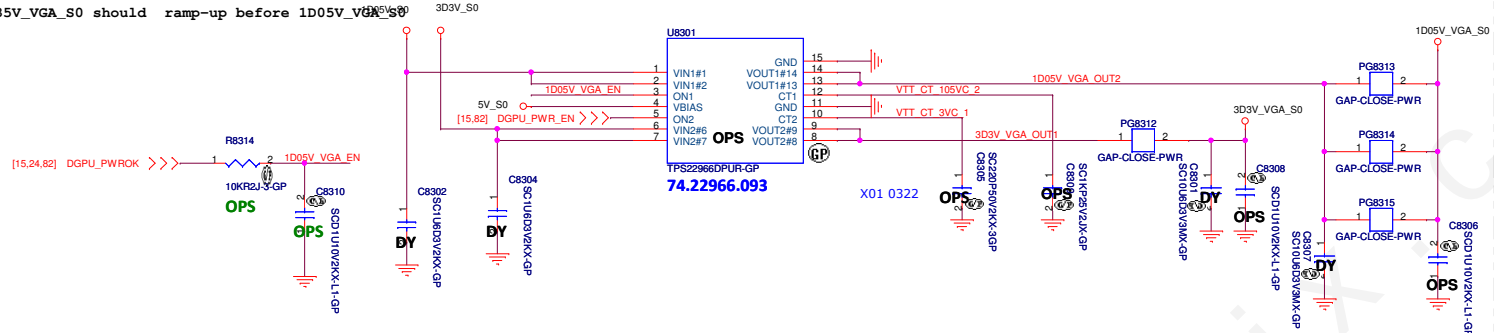
SSID = PWR.Plane.Regulator_3p3v_vga, 1p35v_vga, 1p05v_vga

3D3V_VGA_S0

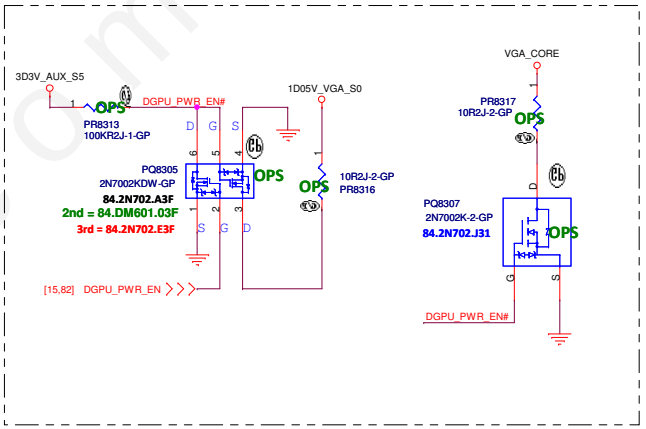
1D05V_VGA_S0

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1D5V_VGA_S0
1D35V_VGA_S0 should ramp-up before 1D05V_VGA_S0

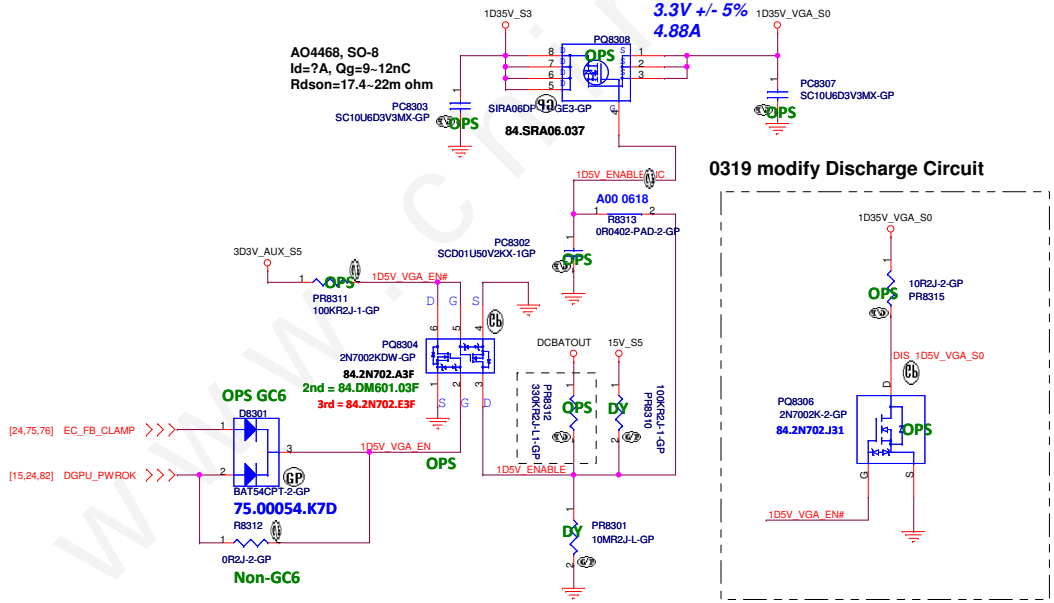
3D3V_S0 to 3D3V_VGA_S0
1D05V_S0 to 1D05V_VGA_S0



0307 Add Discharge Circuit



1D35V_VGA_S0



0319 modify Discharge Circuit

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Title: DISCRETE VGA POWER

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SSID = User.Interface

SO1 SO2 SO3
OPS
STF217R128H83-2-GP
34.4Y702.301

S1 S2 S3 S4
SPRING-52-GP
34.4T025.001

H2 H3 H4
HOLET256B315R111-GP
ZZ.00PAD.M01
HT85BE85R29-U-5-GP
ZZ.00PAD.D41

0116 Add RF CAP

DCBATOUT
EC8601 EC8602 EC8603 EC8604 EC8605
SCD1U25V2KX-GP
DY

C1 C2 C3
HOLE197R166-1-GP
ZZ.00PAD.V71

0528 Add NPTH hole

PAD1
PAD-3P-GP

0117 Add EMC CAP

DCBATOUT
EC8606 EC8607 EC8608 EC8609 EC8610 EC8611 EC8612
SCD1U25V2KX-GP
DY

5V_S0 3D3V_S0 VGA_CORE 1D05V_S0
EC8613 EC8614 EC8615 EC8616 EC8620 EC8621 EC8622
SCD1U25V2KX-GP
DY

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Title: UNUSED PARTS/EMI Capacitors
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Title: *Reserved*

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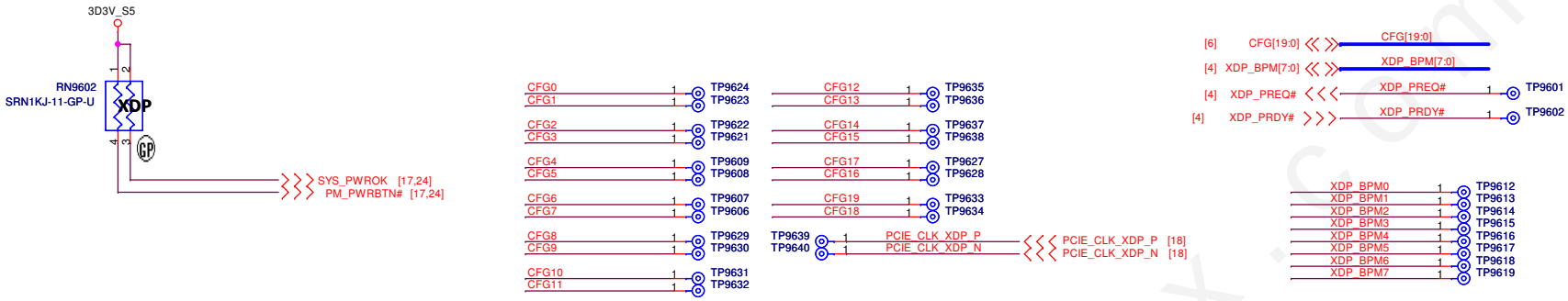
SSID = XDP

CPU XDP



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Title	CPU XDP	
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PCH Strapping

Name	Schematics Notes

Processor Strapping

Bit	Name	Strap Description	Strap Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION

SMBus ADDRESSES

I²C / SMBus Addresses	CHIEF RIVER ORB	
Device	Address	Bus
EC SMBus 1		
Battery 0	0x16	BAT_SCL/BAT_SDA
CHARGER	0x12	BAT_SCL/BAT_SDA
PS8122(HDMI Switch) (Bottom Dock)	0x9E	BAT_SCL/BAT_SDA
USB3.0 redriver PS8710 (Bottom Dock)	0x40	BAT_SCL/BAT_SDA
EC SMBus 2		
Battery 1	0x16	SML1_CLK/SML1_DATA
PCH	0x96 & 0x94	SML1_CLK/SML1_DATA
Discrete VGA Thermal	0x9C or 0x9E	SML1_CLK/SML1_DATA
PS8321 HDMI level shifter	0x96 & 0X97	SML1_CLK/SML1_DATA
NCT7718W	0x98 or 0x99	SML1_CLK/SML1_DATA
EC SMBus 3		SMB2_CLK/SMB2_DATA
NCT5605Y-0	0x30	SMB2_CLK/SMB2_DATA
NCT5605Y-1	0x32	SMB2_CLK/SMB2_DATA
PCH SMBus		
SO-DIMMA		PCH_SMBDATA/PCH_SMBCLK
SO-DIMMB		PCH_SMBDATA/PCH_SMBCLK
Intel LAN 82579		PCH_SMBDATA/PCH_SMBCLK
G-Sensor		PCH_SMBDATA/PCH_SMBCLK
MINI WWAN		PCH_SMBDATA/PCH_SMBCLK
INTEL LAN82579		PCH_SMBDATA/PCH_SMBCLK

PCIE Routing

LANE1	X
LANE2	X
LANE3	Mini Card1(WLAN)
LANE4	X
LANE5	X
LANE6	X
LANE7	X
LANE8	X

SATA Table

SATA	
Pair	Device
0	HDD1
1	mSATA
2	
3	
4	
5	

USB Table

Pair	Device
0	USB port 1,with Power Share
1	USB 2.0 HDMI
2	USB port2 (usb redriver)
3	X
4	Touch Panel
5	Card Reader
6	BLUETOOTH
7	CAMERA

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DELL

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Title: Change History

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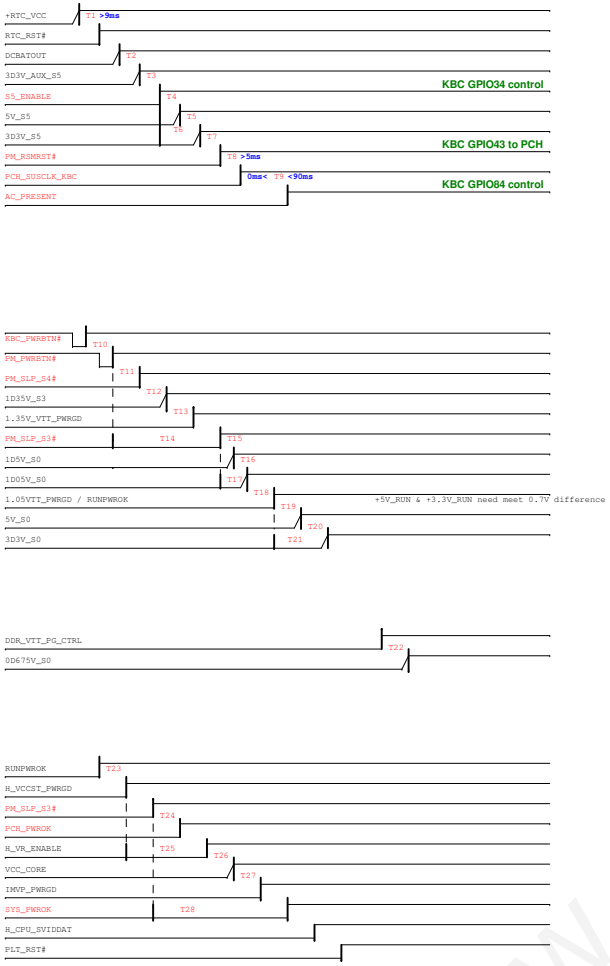
Intel Power Up Sequence

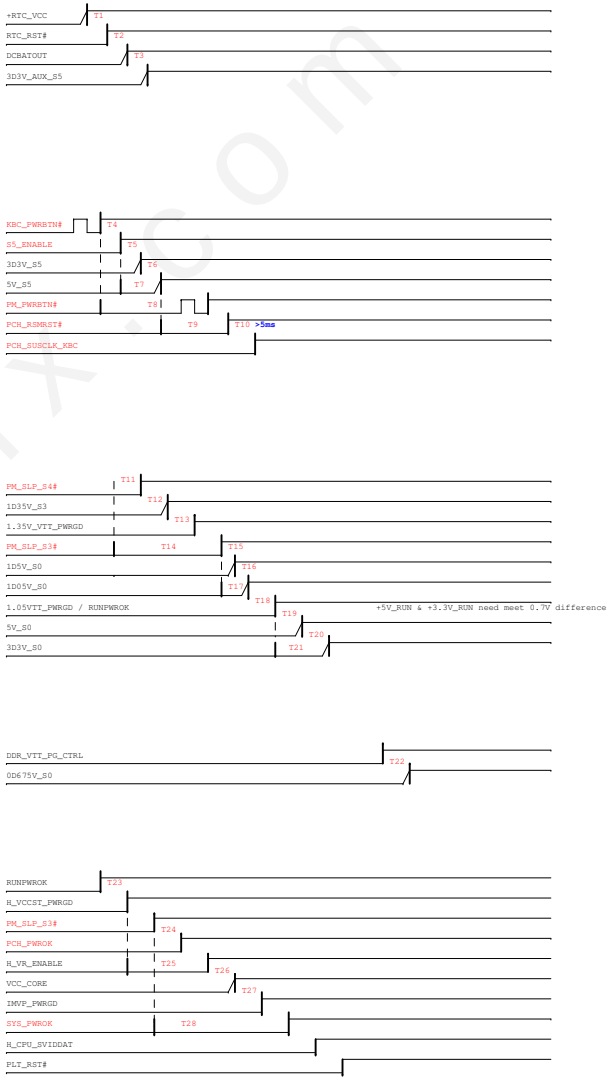
(AC mode)

Red printings:KBC GPIO involved



(DC mode)

Red printings:KBC GPIO involved



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Title: Power Sequence

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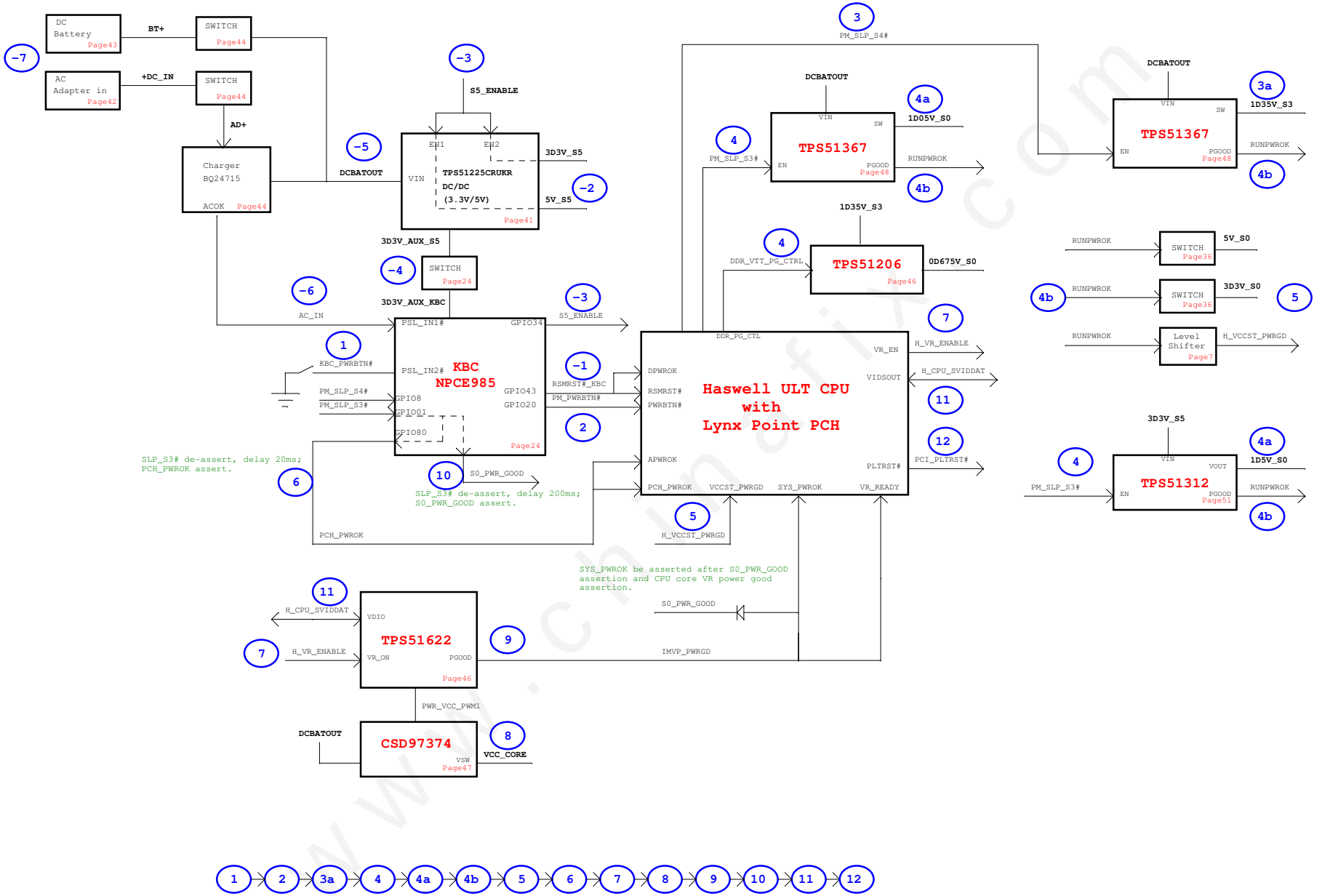
Wistron SHARK BAY POWER UP SEQUENCE DIAGRAM



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Title: Power Block Diagram
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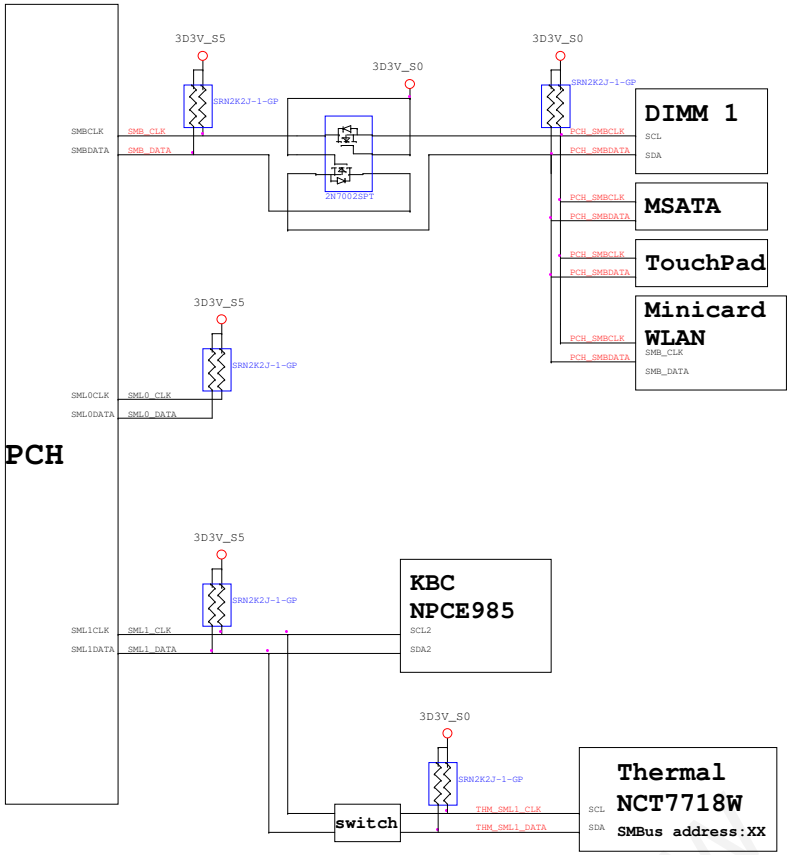
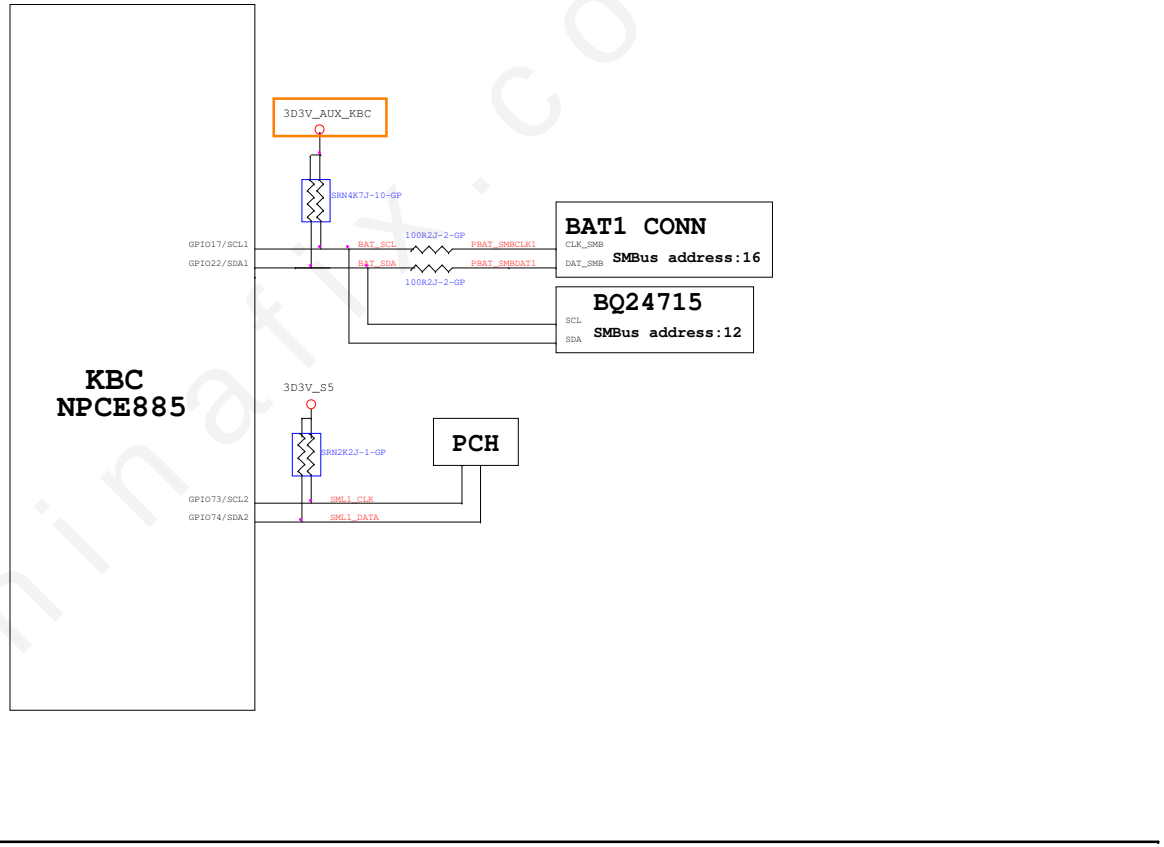
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

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