Starload Schematics
Skylake-U

2016-02-18

REV : A00

DY : None Installed
UMA: UMA only installed
OPS: DISCRTE OPTIMUS installed

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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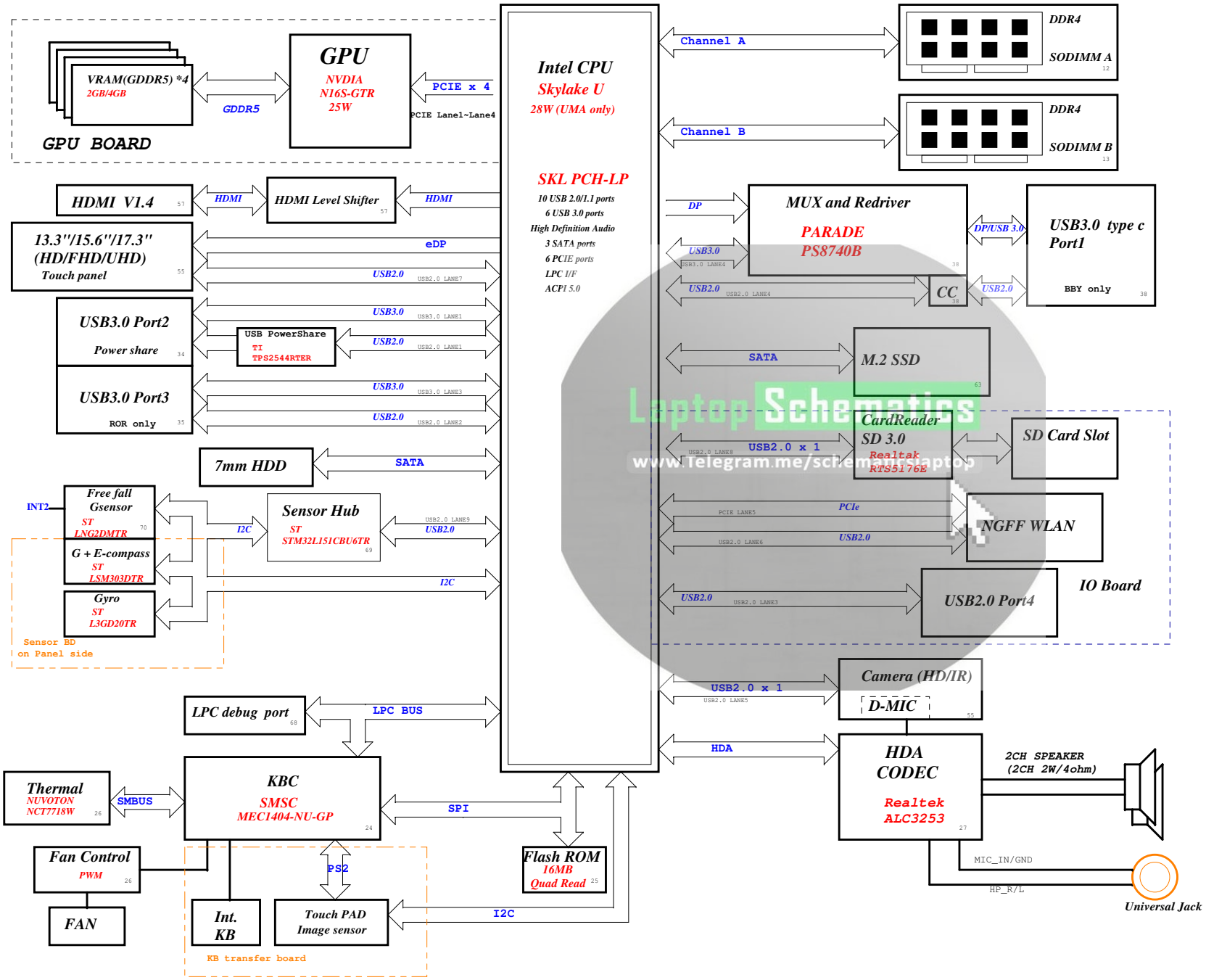
Title: *Cover Page*		
Size: A3	Document Number: Starload SKL-U	Rev: A00
Date: Thursday, February 18, 2016	Sheet 1 of 106	

Project code: 4PD07S010001
PCB P/N: 15264
Revision: A00

Star lord SKL-U Block Diagram



CHARGER — ISL95521HRZ-T — 44

INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC — SY8288CRAC-GP — 45

INPUTS	OUTPUTS
DCBATOUT	PWR_5V 5V_S5 5V_AUX_S5

CPU Core Power — NCP81208MNTXG-GP — 46~50
NCP81382MNTXG-1-GP
NCP81382MNTXG-1-GP
NCP81253MNTBG-GP

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
DCBATOUT	+VCCGT
DCBATOUT	+VCCSA_VR

DDR4 — SY8288RAC-GP / APL5338XAI-TRG-GP — 51

INPUTS	OUTPUTS
DCBATOUT	1D2V_S3 0D675V_S0

CPU DCDC-V1D00A — AOZ1268QI-02-GP — 52

INPUTS	OUTPUTS
DCBATOUT	1D0V_S5

LDO-V1D5V — S-1339D15-M5001-GP — 54

INPUTS	OUTPUTS
3D3V_S5	1D5V_S0

LDO-V1D8V — APL5930KAI-TRG-GP — 54

INPUTS	OUTPUTS
3D3V_S5	1D8V_S5

5V/3V S0 — G5016KD1U — 40

INPUTS	OUTPUTS
5V_S5 3D3V_S5	5V_S0 3D3V_S0

VCCSTG — M5938ARD1U-GP-U — 40

INPUTS	OUTPUTS
1D0V_S5	+VCCSTG

VCCST — TPS22965DSGR-GP-U — 40

INPUTS	OUTPUTS
1D0V_S5	+V1.00U_CPU

SYSTEM DC/DC — TPS51225RUKR-GP — 45

INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 3D3V_S5 PWR_3D3V

<Core Design>

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Title: Block Diagram
Size: C | Document Number: Starload SKL-U | Rev: A00
Date: Thursday, February 18, 2016 | Sheet 2 of 106

Main Func = CPU

(Blanking)

<Core Design>

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Title: (Reserved)

Size: A3 | Document Number: Starload SKL-U | Rev: A00

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Main Func = CPU

#544669 CRB Rev0.52

+VCCSTG = 1.0 V

[PECI] and [PROCHOT#]
Impedance control: 50 ohm

[24] H_PECI
[24,44,46] H_PROCHOT#

R401 1KR2J-1-GP
499R2F-2-GP R403 Ra
TPAD14-OP-GP

TP401 TPAD14-OP-GP
TP402 TPAD14-OP-GP
TP403 TPAD14-OP-GP
TP404 TPAD14-OP-GP
TP405 TPAD14-OP-GP
TP406 TPAD14-OP-GP
TP407 TPAD14-OP-GP
TP408 TPAD14-OP-GP

H_CATERR# D63
H_PROCHOT# R C65
PCH_THERMTRIP# C63
SKTOCC# A65
XDP_BPM0 C55
XDP_BPM1 D55
XDP_BPM2 B54
XDP_BPM3 C56
GPP_E3/CPU_GP0 A6
TOUCHPAD_INTR# A7
GPP_B4/CPU_GP3 BA5
CPU_POPIRCOMP AY5
PCH_POPIRCOMP AT16
EDRAM_OPIO_RCOMP AU16
EOPIO_RCOMP H66
H65

49D9R2F-GP R412
49D9R2F-GP R413
49D9R2F-GP R414
49D9R2F-GP R415

[24,55] TOUCH_PANEL_INTR#

3D3V_S5_PCH
R404 DY 100KR2J-1-GP
3D3V_S0
R405 DS3 100KR2J-1-GP

R410 NON DS3 0R2J-2-GP
[24,65] INT_TP#
DS3 D401 RB751V-40H-GP
K A

83.R2004.G8F

Add resistor by NON DS3 function

CPU1D 4 OF 20
SKYLAKE_ULT

CPU MISC
CATERR#
PECI
PROCHOT#
THERMTRIP#
SKTOCC#
BPM#[0]
BPM#[1]
BPM#[2]
BPM#[3]
GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3
PROC_POPIRCOMP
PCH_OPIRCOMP
OPCE_RCOMP
OPC_RCOMP

JTAG
PROC_TCK B61 XDP_TCLK
PROC_TDI D60 XDP_TDI
PROC_TDO A61 XDP_TDO_CPU
PROC_TMS C60 XDP_TMS
PROC_TRST# B59 XDP_TRST#
PCH_JTAG_TCK B56 PCH_JTAG_TCK
PCH_JTAG_TDI D59 PCH_JTAG_TDI
PCH_JTAG_TDO A56 PCH_JTAG_TDO
PCH_JTAG_TMS C59 PCH_JTAG_TMS
PCH_TRST# C61 XDP_TRST#
JTAGX A59 XDP_TCK_JTAGX

SKYLAKE-U-GP

071.SKYLA.000U

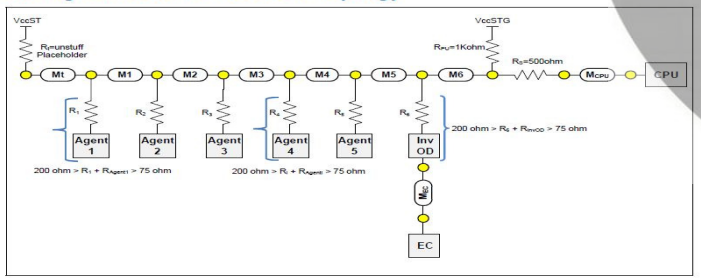
+VCCST_CPU
R419 1KR2J-1-GP
PCH_THERMTRIP#
EC401 AZ5725-01FDR7G-GP
EMI DVT1 0210

+VCCSTG = 1.0 V

XDP_TMS 1 DY 2 R421 51R2J-2-GP
XDP_TDI 1 DY 2 R422 51R2J-2-GP
XDP_TDO_CPU 1 DY 2 R423 51R2J-2-GP
PH in P.99
PCH_JTAG_TDI 1 R408 51R2J-2-GP
PCH_JTAG_TDO 1 R409 51R2J-2-GP
PCH_JTAG_TMS 1 R416 51R2J-2-GP
XDP_TCK_JTAGX 1 DY 2 R417 1KR2J-1-GP
XDP_TRST# R402 1 DY 2 51R2J-2-GP
XDP_TCLK R406 1 DY 51R2J-2-GP
PCH_JTAG_TCK R407 1 DY 51R2J-2-GP

(#543016) PROCHOT# Routing Guidelines

Figure 10-1. Routing Illustration for PROCHOT# Topology



M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt <0.3 mils
Main route(M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

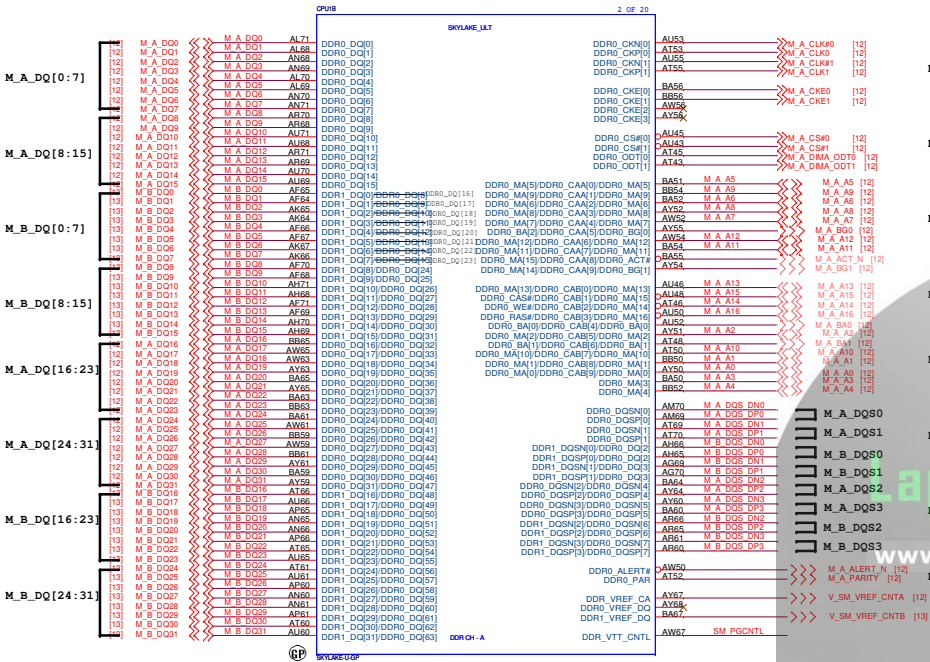
Title: CPU_(JTAG/CPU SIDE BAND)

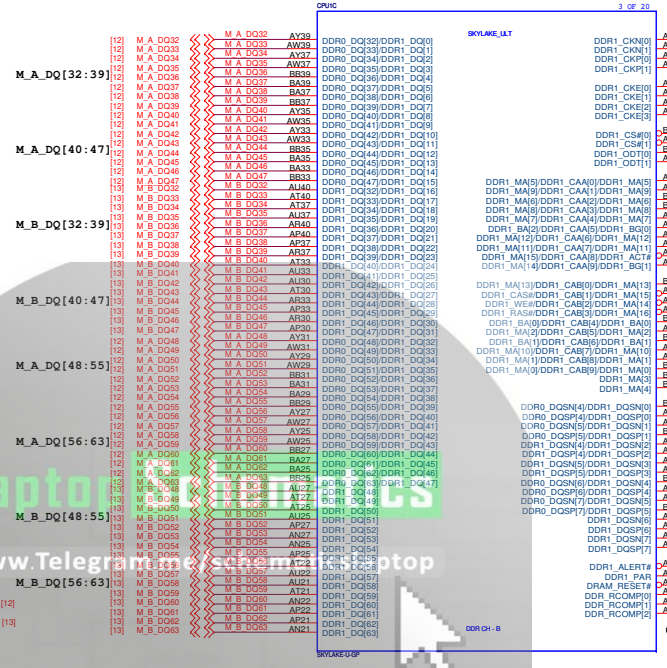
Size: A3 | Document Number: Starload SKL-U | Rev: A00

Date: Thursday, February 25, 2016 | Sheet 4 of 106

Main Func = CPU

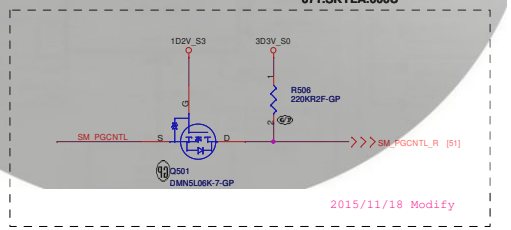
DDR4 ball type: Interleaved Type





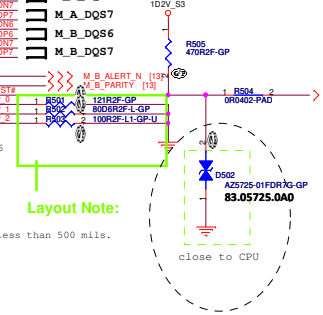
071.SKYLA.000U

DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel.
Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.



071.SKYLA.000U

Design Guideline:
SM_RCOMP keep routing length less than 500 mils.



Layout Note:

PDG: DDR/ODT

4.17 SKL U and SKL Y System Memory ODT Signal Connectivity Details

Table 4-41. ODT Signals Connectivity table

Processor	Memory type	Side	Signal	Rule	Notes
SKL-Y	LPDDR3 Memory Down	Processor	DDR0_ODT[0] DDR1_ODT[0]	Processor's ODT[0] connected to DRAMs' ODT. T-topology connection	1,2
		DRAMs	One ODT per x32 DRAM PKG Two ODT per x64 DRAM PKG		
SKL-U	LPDDR3 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' ODT. T-topology connection. Processor's ODT[1] not connected.	1,2
		DRAMs	One ODT per x32 DRAM PKG Two ODT per x64 DRAM PKG		
	DDR3L Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT. If Rank1 not used, Processor ODT[1] not connected.	3,4
		DRAMs	ODT[1:0]		
	DDR3L SO-DIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] connected to DIMMs ODT[1:0].	1,3
		DIMMs	ODT[1:0]		
	DDR3L Mixed Memory Down and SO-DIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's SODIMM Channel ODT[1:0] connected to DIMM. Processor's Memory Down channel - ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT. If rank1 not used, ODT[1] not connected.	3,4
		DIMM	ODT[1:0]		
		DRAMs	ODT[1:0]		
	DDR4 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT balls. If Rank1 not used, Processor ODT[1] not connected.	
		DRAMs	ODT[1:0]		
	DDR4 SO-DIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] balls connected to DIMM ODT[1:0] balls.	
		DIMMs	ODT[1:0]		

Notes:
1. For additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files (RVP3 - SKL-Y LPDDR3, RVP5 - SKL-U LPDDR3)
2. LPDDR3 Rank1 ODT is always disabled by BIOS/MRC. ODT signal is controlling only Rank0 ODT.
3. DDR3L ODT input is held high (Active), RTT NOM is defined by BIOS as High-Z in both ranks, when a Rank receives write command it enables RTT WR (set by BIOS after power training). Otherwise ODT gets RTT NOM (High-Z).
4. These guidelines are related to DDR3L supported Memory down topologies only. 2R x16 DDP single side, 2R x16 SDP dual sided and 2Rx8 dual side.

<Core Design>

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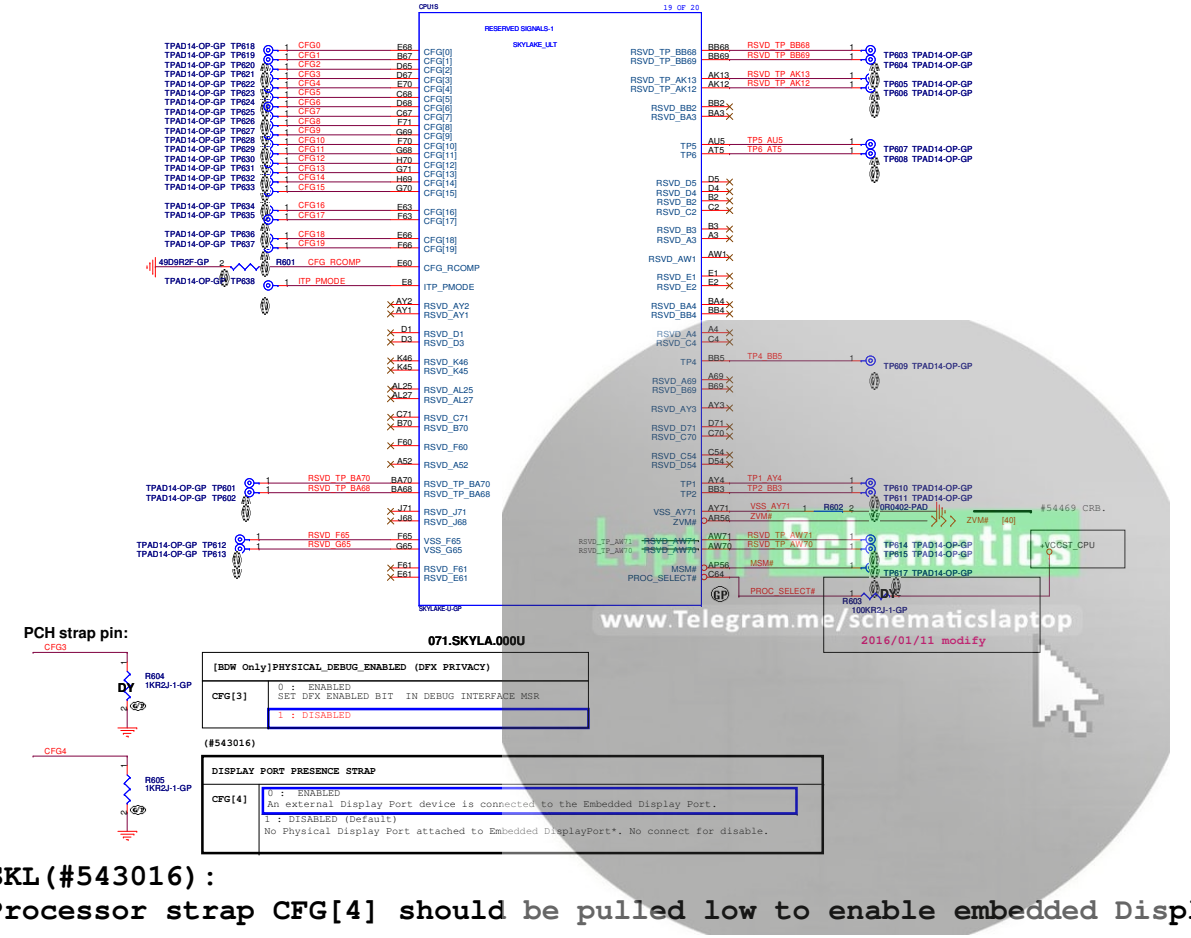
Title: CPU_(DDR)
Size: A2 | Document Number: Starload SKL-U | Rev: X02
Date: Thursday, February 25, 2016 | Sheet 5 of 106

Main Func = CPU



PCH strap pin:

071.SKYLA.000U

CFG3

R604 1KR2J-1-GP

[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED

(#543016)

CFG4

R605 1KR2J-1-GP

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port. 1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.

SKL(#543016):

Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(RESERVED)

Size: A2 | Document Number: Starload SKL-U | Rev: A00

Date: Thursday, February 25, 2016 | Sheet 6 of 106

Main Func = CPU

140mA

3A

3A

071.SKYLA.000U

071.SKYLA.000U

#544669 CRB.

2016/02/16 modify

071.SKYLA.000U

Layout Note:
1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE Impedance=50 ohm
3. Length match<25mil

SVID_543016:

Figure 10-7. Routing Illustration for SVID Topology

SVID DATA

Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
Route the Alert signal between the Clock and the Data signals.

SVID CLOCK

CPU

VR 1

VR 2

VR 3

VR 4

Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{pu} [Ω]	R_{pu2} [Ω]	R_{s1} [Ω]	R_{s2} [Ω]	VCCprr [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT #							56	Empty	220	0	

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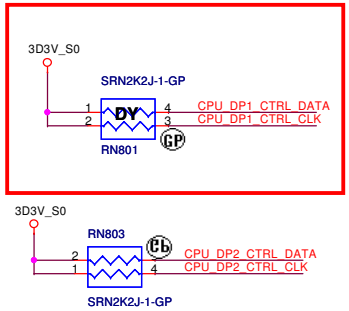
CPU(VCC_CORE)

Starload SKL-U

A00

Main Func = CPU

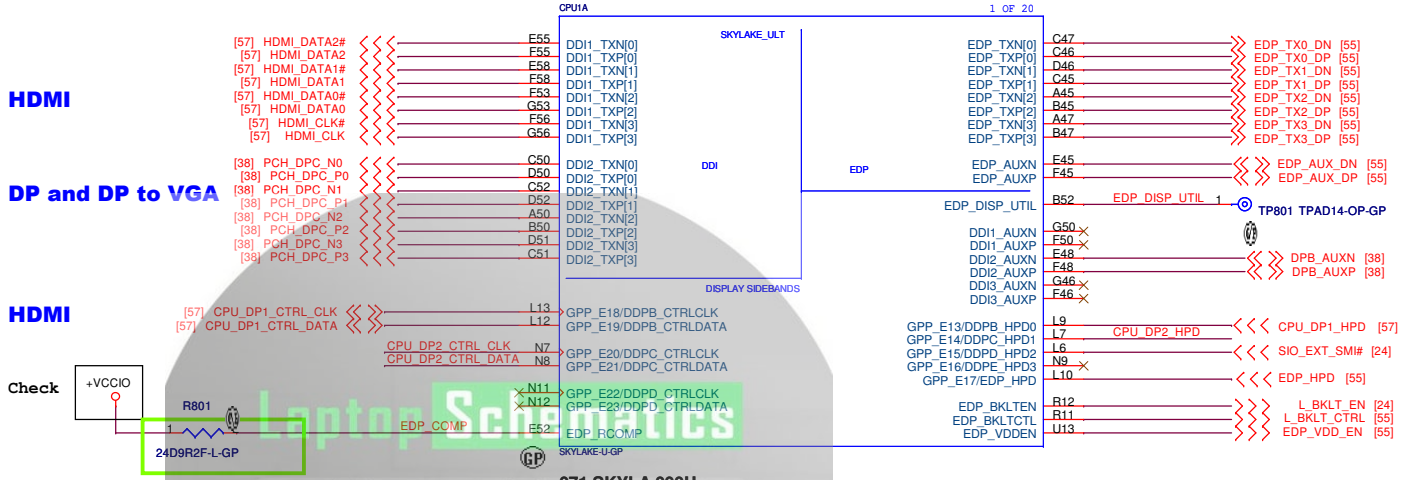
Dummy, Vendor suggest
20141117



HDMI

DP and DP to VGA

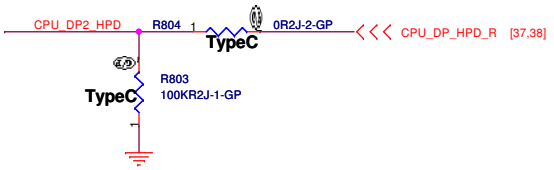
HDMI

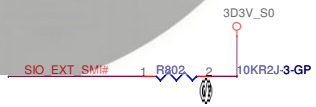


Check

071.SKYLA.000U

(#543016) The Skylake U/Y processor supports only two DDI ports – Port 1 and Port 2.





(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils

(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 ±1% Ω resistor.

<Core Design>

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Title: CPU_(DISPLAY)

Size: A3 | Document Number: Starload SKL-U | Rev: A00

Date: Thursday, February 25, 2016 | Sheet 8 of 106

Main Func = CPU

<Core Design>

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Title: *(Reserved)*

Size: A3 | Document Number: *Starload SKL-U* | Rev: *A00*

Date: Thursday, February 18, 2016 | Sheet 9 of 106

Main Func = CPU

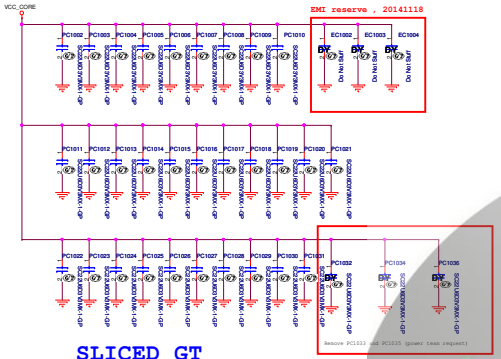
(#543016 PDG)

20140814 DAVID

CORE

U-line 23e 28W
IccMax current-10ms max = 34 A

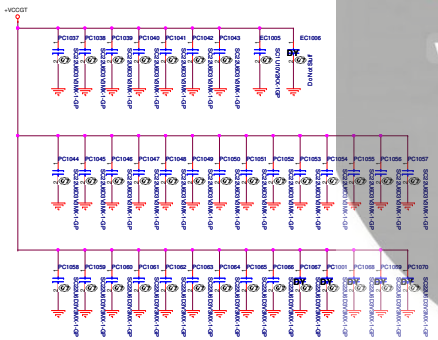
22U 0603 x 35(5 DY)



SLICED GT

U-line 23e 28W
IccMax current-10ms max[A] = 67 A

22U 0603 x35 (5 DY)



VCCSA

22U 0603 x13 (5 DY)

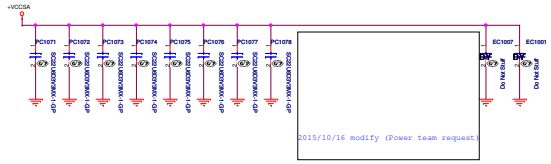


Table 53-3. SKL U Bulk Decoupling Requirements

Bulk Decoupling Locations	Requirements	Notes
VCC Power Plane at VR output	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
	1x 220uF (@4.5mO ESR)	Placed at backside side near to VR output
VCCGT Power Plane at VR output	2x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output Additional components needed when supporting 23e
VCCGTx Power Plane at VR output	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output Only needed when supporting 23e
VCCIO Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output
VCCSA Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output

Note: These requirements are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 1 of 2)

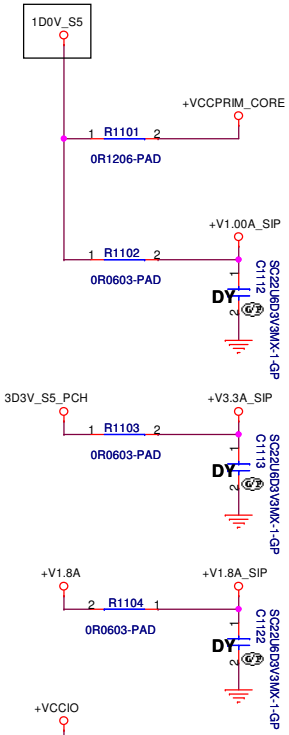
Domain	Backside cap	Primary side cap	Placement guideline
VCC	9x 22uF 0603		Place on secondary side, underneath the package
	7x 10uF 0402		
	15x 1uF 0201		
		8x 47uF 0805 (6.3V)[1]	Place as close to the package as possible
		8x 10uF 0402	
VCCGT	10x 10uF 0402		Place on secondary side, underneath the package
	12x 1uF 0201		
		3x 47uF 0805 (6.3V)[1]	Place as close to the package as possible
		7x 22uF 0603	
		3x 47uF 0805	Place as close to the package as possible Additional components needed when supporting 23e
		5x 22uF 0603	
VCCGTx	8x 10uF 0402		Place on secondary side, underneath the package Only needed when supporting 23e
		8x 22uF 0603	Only needed when supporting 23e
VCCSA	7x 10uF 0402		Place on secondary side, underneath the package
	7x 1uF 0201		
		6x 10uF 0402	Place as close to the package as possible
VCCIO	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 1uF 0402	Place as close to the package as possible
VDDQ	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 10uF 0402	Place as close to the package as possible
VDDQC	1x 1uF 0201		Place on secondary side, underneath the package
VCCPLL		1x 1uF 0402	Place as close to the package as possible
VCCST		1x 1uF 0402	Place as close to the package as possible

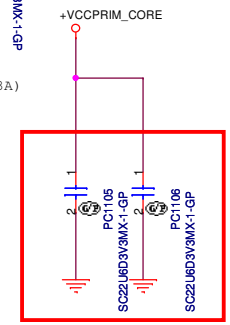
Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 2 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCCSTG	1x 1uF 0402		Place on secondary side, underneath the package Placeholder only
VCCEOPIO	2x 10uF 0402		Place on secondary side, underneath the package
VCCOPC	1x 10uF 0402		Place on secondary side, underneath the package
	6x 1uF 0201		

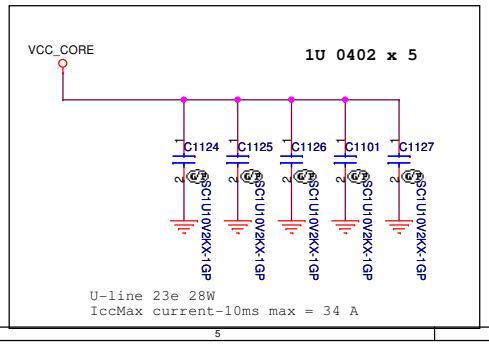
Main Func = CPU

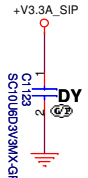
PCH DERIVED RAILS



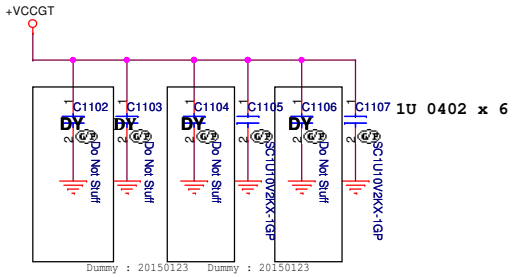


Size:0805 change to 0603
20141117

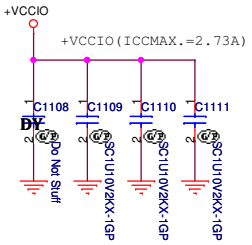


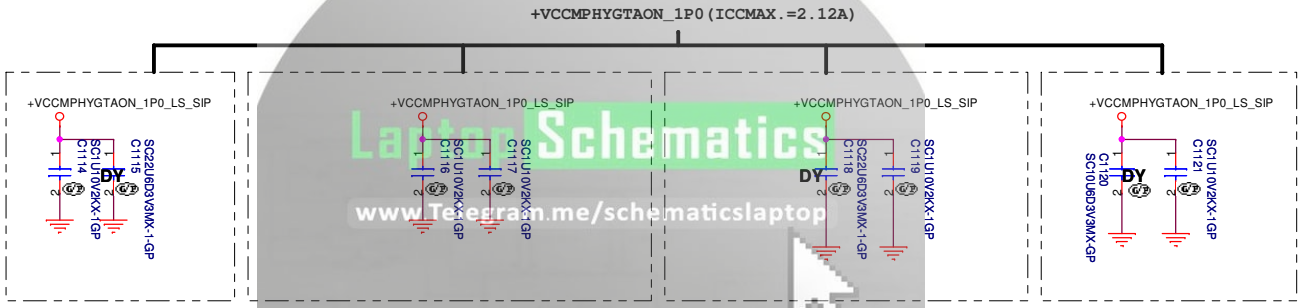


UNSLICED GT



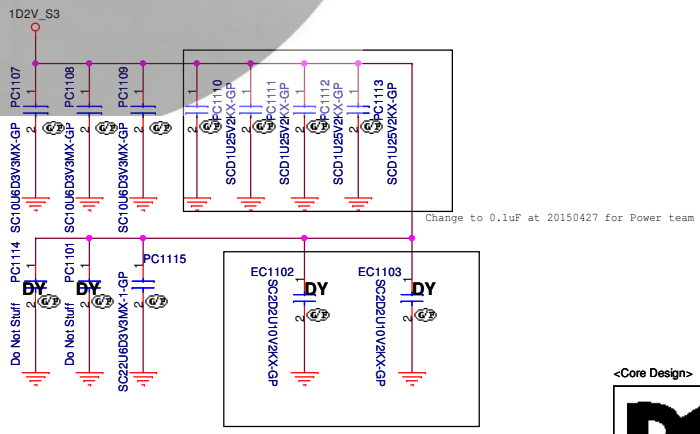
VCCIO





Layout Note:

1uF:
C1174 near N15
C1180 near K15
C1173 near AF20
C1172 near N18
C1175 near AB19
22uF :
C1182 C1184 near N15
10uF:
C1176 near N15



RF request 2016/01/12 modify

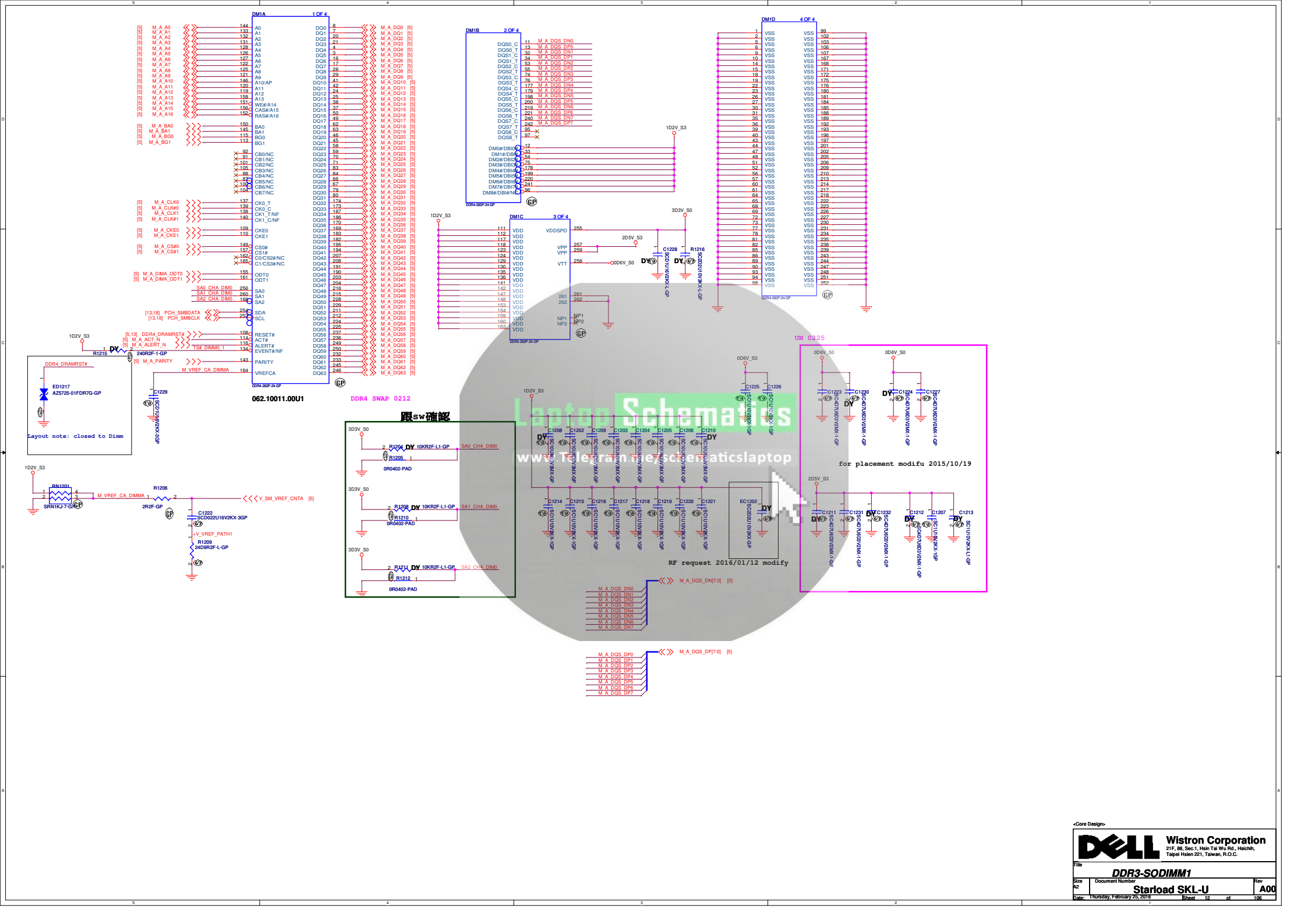
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (Power CAP2)

Size	Document Number	Rev
A3	Starload SKL-U	A00

Date: Thursday, February 18, 2016 Sheet 11 of 106



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1

Size	Document Number	Rev
A2	Starload SKL-U	A00

Date: Thursday, February 25, 2016 Sheet 12 of 106

By layou modify 20150916

By layou modify 20150916

DDR4 SWAP 0212

跟sw確認

062.10011.00T1

UN 0225

RF request 2016/01/12 modify

RF request 2016/01/12 modify

Layout note: closed to Dimm

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1

Size: X2 | Document Number: Starload SKL-U | Rev: A00

Date: Thursday, February 25, 2016 | Sheet 13 of 106

(Blanking)

<Core Design>

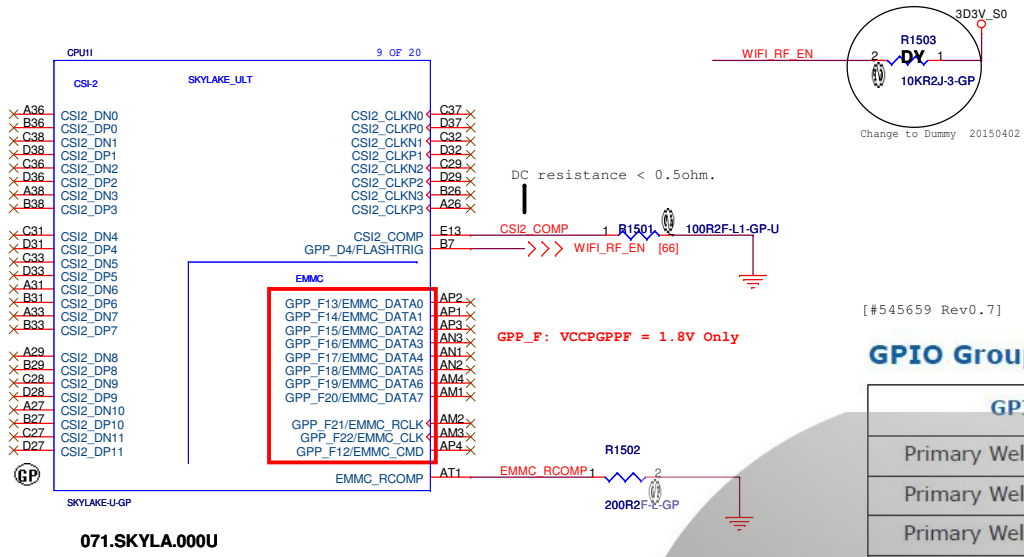
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)_SODIMM _SODIMM4*

Size	Document Number	Rev
A4	*Starload SKL-U*	*A00*

Date: Thursday, February 18, 2016 Sheet 14 of 106

Main Func = PCH



071.SKYLA.000U

Table 8-1. Switchable Graphics GPIO Requirements

GPIO	Usage
DGPU_PWR_EN#	BIOS drives to turn on/off the discrete graphics power.
DGPU_PWROK	dGPU voltage regulator drives to indicate power status to the PCH. It enables clocks to dGPU.
DGPU_HOLD_RST#	Discrete Graphics Enable signal. BIOS controls and a PCH GPIO drives. It gates Platform Reset to enable Reset for the dGPU.
DGPU_PRSNT#	Used only by the CRB or if Graphic Cards requiring AC caps on the motherboard or add-in card is supported on the platform to indicate that a card is present.

[#545659 Rev0.7]

GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V

<Core Design>

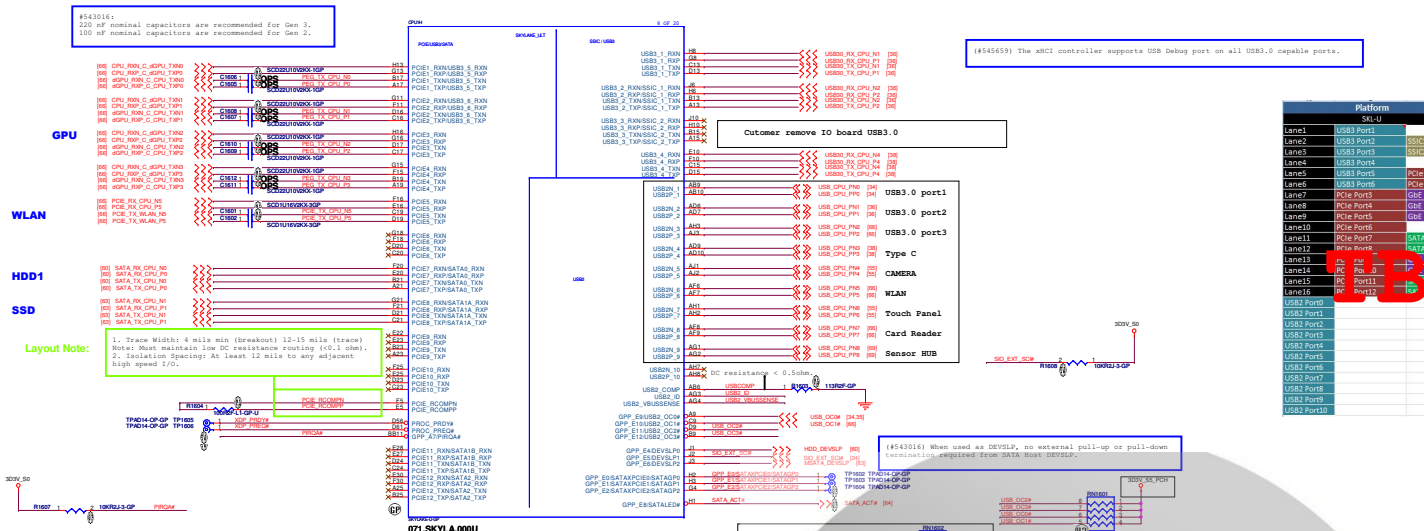
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(CS-2/EMMC)

Size: A3 | Document Number: Starload SKL-U | Rev: A00

Date: Thursday, February 25, 2016 | Sheet 15 of 106

Main Func = PCH



Platform			Project
SKL-U			Tulip
Lane1	USB3 Port1		USB 3 (I/O) Port 1
Lane2	USB3 Port2	SSIC1	NC
Lane3	USB3 Port3	SSIC2	NC
Lane4	USB3 Port4		NC
Lane5	USB3 Port5	PCIe Port1	dGPU
Lane6	USB3 Port6	PCIe Port2	
Lane7	PCIe Port3	GbE	
Lane8	PCIe Port4	GbE	
Lane9	PCIe Port5	GbE	WLAN
Lane10	PCIe Port6		LAN
Lane11	PCIe Port7	SATA0	HDD
Lane12	PCIe Port8	SATA1	ODD
Lane13	PCIe Port9		
Lane14	PCIe Port10		
Lane15	PCIe Port11		
Lane16	PCIe Port12		
USB2 Port0			USB 3 (I/O) Port 1
USB2 Port1			USB 2 Port 2
USB2 Port2			USB 2 Port 3
USB2 Port3			NC
USB2 Port4			Camera
USB2 Port5			WLAN
USB2 Port6			Touch Panel
USB2 Port7			Card Reader
USB2 Port8			NC
USB2 Port9			NC
USB2 Port10			NC

USB 2.0 Table

Pair	Device
0	USB3.0 port1
1	USB3.0 Port2 (Debug Port/IOBD)
2	USB3.0 Port3 (IOBD)
3	Sensor HUB
4	CAMERA
5	WLAN
6	Touch Panel
7	Card Reader

#545659 (SKL_PCH_U_Y_EDS Rev0.7)

Figure 3-1. HSIO Muxing on SKL PCH-LP (U Series)

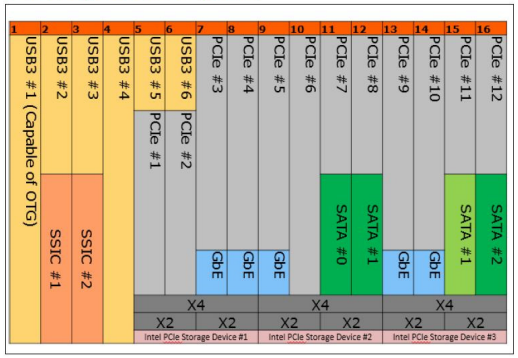


Table 24-2. PCI Express* Port Feature Details

SKL	Max Device (Ports)	Max Lanes	PCIe* Gen Type	Encoding	Transfer Rate (MT/s)	Theoretical Max Bandwidth (GB/s) x1	x2	x4
U	6	12	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00
			3	128b/130b	8000	1.00	2.00	3.94
Y	5	10	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00

Table 24-3. PCI Express* Link Configurations Supported

SKL	PCIe Link Config	PCI Express* Lanes 1	2	3	4	5	6	7	8	9	10	11	12
U	1x4	Port1				Port5				Port9			
	2x2	Port1		Port3		Port5		Port7		Port9		Port11	
	1x2 + 2x1	Port1		Port3	Port4	Port5		Port7	Port8	Port9		Port11	Port12
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9	Port10	Port11	Port12
Y	1x4	Port1				Port5							
	2x2	Port1		Port3		Port5		Port7					
	1x2 + 2x1	Port1		Port3	Port4	Port5		Port7	Port8				
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8				
	1x2									Port9			
	2x1									Port9	Port10		

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCIE/SATA/USB)

Size	Document Number	Rev
A1	Starload SKL-U	A00

Date: Thursday, February 25, 2016 Sheet 18 of 186

Main Func = PCH

Remove Power rail +V3.3A_SIP and R1712(DY), 20141118

R1709,R1723,R1703,R1724 merge to RN1704

RN1704 SRN10KJ-6-GP

AC_PRESENT
PCH_WAKE#
PCH_BATLOW#
GPD11/LANPHYPC

GPD11 pull high by Intel PDG1.3 request

3D3V_S5 R1711 0R0603-PAD +VCCPDSW_3P3

Layout note: 3 PAD SHARING

RTC_AUX_S5 R1730 330KR2J-L1-GP SM_INTRUDER#

#544669 (CRB): 330k.

+V3.3A_SIP R1731 20KR2J-L2-GP EXT_PWR_GATE#

[#543016 Rev0.7]
EXT_PWR_GATE#: Due to a bug on A0, a temporary pull-up resistor will be required to overcome the internal 20k pull-down that is active during the early portion of the power up sequence

#544669 Rev0.52 CRB:
No PL resistor on THERMTRIP#.

H_CPUPWRGD R1714 10KR2J-3-GP DY EC1701 AZ5725-01F6RG-GP EMI DVT1 0210

RN1703 SRN10KJ-5-GP
PM_RSMRST#
PM_PCH_PWROK
R1717 10KR2J-3-GP DY SYS_PWROK

[24] EC_WAKE# R1732 0R0402-PAD GPD2/LAN_WAKE#

+V3.3A_SIP R1701 10KR2J-3-GP

TP1709 TPAD14-OP-GP PCH_PLTRST#
TP1705 TPAD14-OP-GP H_CPUPWRGD
[24] SYS_PWROK
[24,26] RESET_OUT#
PM_RSMRST# R1706 0R0402-PAD R1704 0R2J-2-GP NON DS3
[20] ME_SUS_PWR_ACK_R
+VCCPDSW_3P3 R1707 10KR2J-3-GP

XDP_DBRESET#
SYS_RESET#
RSMRST#
PROCPWRGD
VCCST_PWRGD
SYS_PWROK
PCH_PWROK
DSW_PWROK
ME_SUS_PWR_ACK_R
SUSACK#_R
PCH_WAKE#
GPD2/LAN_WAKE#
GPD11/LANPHYPC
GPD7/USB2_WAKEOUT#

(PDG#543016)
WAKE#: Ensure that WAKE# signal rise (Maximum) is <100 ns.

CPU1K 11 OF 20
SYSTEM POWER MANAGEMENT
SKYLAKE_ULT
SKYLAKE-U-GP
071.SKYLA.000U

GPP_B12/SLP_S0#
GPD4/SLP_S3#
GPD5/SLP_S4#
GPD10/SLP_S5#
SLP_SUS#
SLP_LAN#
GPD9/SLP_WLAN#
GPD6/SLP_A#
GPD3/PWRBTN#
GPD1/ACPRESENT
GPD0/BATLOW#
GPP_A11/PME#
INTRUDER#
GPP_B11/EXT_PWR_GATE#
GPP_B2/VRALERT#

SIO_SLP_S0# [24,60]
SIO_SLP_S3# [24,27,40,51,54]
SIO_SLP_S4# [24,40,54]
SIO_SLP_S5#
SIO_SLP_SUS# [52,54]
SLP_LAN#
AUX_EN_WOWL
SIO_SLP_A#
SIO_PWRBTN# [24]
AC_PRESENT
PCH_BATLOW#
PME#
SM_INTRUDER#
EXT_PWR_GATE#

TP1703 TPAD14-OP-GP
TP1704 TPAD14-OP-GP
TP1710 TPAD14-OP-GP
TP1706 TPAD14-OP-GP
TP1707 TPAD14-OP-GP
TP1708 TPAD14-OP-GP

BATLOW#:
Pull-up required even if not implemented.

AC_PRESENT EC1707 DY SCD1U16V2KX-3GP

AOZ Power switch, P/N: 074.01334.0093
Low Rds(on)= 5m Ohm
Turn on rise time = 10us

3D3V_S5 C1703 SCD1U16V2KX-3GP DY
U1703 NC#1 VCC A DY GND Y 74LVC1G07GW-GP
[24,27,40,51,54] SIO_SLP_S3#
[24,40] ALL_SYS_PWRGD R1733 0R2J-2-GP

For sequence fine tune 2016/01/04

3D3V_S5 C1702 SCD1U16V2KX-3GP +VCCSTG
U1701 NC#1 VCC A DY GND Y 74LVC1G07GW-GP 73.01G07.0HG
R1722 100KR2J-1-GP DY Dis-wire with XDP_PM_RSMRST_PWRGD_XDP
H_VCCST_PWRGD
EC1708 AZ5725-01F6RG-GP
C1701 SCD01U50V2KX-1GP DY
EMI DVT1 0210

R722 & EC1708 modify to 100k and 0.01uF at DVT1

[24,66,68] PLT_RST#
R1713 0R0402-PAD PCH_PLTRST#
R1715 100KR2J-1-GP DY
C1701 SC220P50V2KX-3GP DY

3D3V_S5 EC1713 SCD1U16V2KX-3GP DY
EC1709 AZ5725-01F6RG-GP
R1710 100KR2F-L1-GP
R1719 47KR2F-GP
EMI DVT1 0210

RF request 2016/01/12 modify

#543016 Rev0.7
1. VCCST_PWRGD is only 1.0 V tolerant.
2. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST

+VCCMPHYGTAON_1P0
SKL: 1.0V
+VCCMPHYGTAON_1P0(ICCMAX.=3.5A)

1D0V_S5 EC1710 SCD1U16V2KX-3GP DY R1724 0R0805-PAD R1735 0R0805-PAD +VCCMPHYGTAON_1P0_LS_SIP C1704 SC10U6D3V3MX-GP

RF request 2016/01/12 modify
Follow Iris SKL 2015/11/30 modify

XDP_DBRESET#
SYS_PWROK
PLT_RST#
RESET_OUT#
3V_5V_POK
EC1706 SC1KP50V2KX-1GP
EC1702 EC1703 EC1704 EC1705 AZ5725-01F6RG-GP
EMI DVT1 0210

4th = 84.DMN66.03F
3rd = 75.00601.07C
2nd = 84.2N702.E3F
84.2N702.A3F
D1701 RB751V-40H-GP
ACOK_IN_M [43,44]
Q1702 2N7002KDW-GP
83.R2004.G8F
3D3V_AUX_S5 R1737 100KR2J-1-GP NON DS3 PM_RSMRST#_M
PM_RSMRST#_R NON DS3 R1720 0R2J-2-GP PM_RSMRST#
AC_PRESENT

Reserve by NON DS3 function 20150413

DS3 BOM Option

NON DS3 R1708 0R2J-2-GP ME_SUS_PWR_ACK_R SUSACK#_R
TPAD14-OP-GP TP1711 SUSACK#
TPAD14-OP-GP TP1712 ME_SUS_PWR_ACK
RN1702 DS3 SRN0J-6-GP ME_SUS_PWR_ACK_R

[24] PCH_DPWROK R1718 DY 0R2J-2-GP 3V_5V_POK [40,45,52,54]

Change dummy property from DS3 to DY

EC1711 AZ5725-01F6RG-GP

Change location to net PCH_DPWROK

3D3V_AUX_S5 R1727 100KR2J-1-GP NON DS3
R1726 10KR2J-3-GP
Q1701 2N7002KDW-GP
3V_5V_POK#
PM_RSMRST#
R1702 1KR2J-1-GP R1729 0R2J-2-GP
3V_5V_POK_C
3V_5V_POK [40,45,52,54]
PCH_RSMRST# [24]
NON DS3 DS3 R1729 0R2J-2-GP SIO_SLP_SUS#
C1710 SCD47U10V2KX-GP DY
EC1712 SCD1U16V2KX-3GP DY

Dummy C1710 by it's useless

84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 75.00601.07C
4th = 84.DMN66.03F

EC1711 modify to 100k and 0.01uF at DVT1 20150203

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(POWER MANAGEMENT)
Size: A2 | Document Number: Starload SKL-U | Rev: A00
Date: Thursday, February 25, 2016 | Sheet 17 of 106

Main Func = PCH

PCH strap pin:

eSPI or LPC	Sampled at rising edge of RSMRST#
SML0ALERT# / GPP_C5	This signal has a weak internal pull-down. 0 = LPC Is selected for EC. 1 = eSPI Is selected for EC.

This signal has a weak internal pull-down.

PCH strap pin:

BOOT HALT	
SPI0_MOSI	0 = ENABLED 1 = DISABLED WEAK INTERNAL PU

This signal has a weak internal pull-up.

R1835 and R1834 merge to RN1802
2015/10/06 modify

R1806,R1807,R1808,R1809 merge to RN1803
2015/10/06 modify

RCIN#:
Frequency to Avoid: 33 MHz

SERIRQ PH:
PDG: 8.2k
CRB: 10k

WLAN

071.SKYLA.000U

071.SKYLA.000U

Layout: Place at the open door area.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(LPC/SPI/SMBUS/CL/CLK)

Size: A2 | Document Number: Starload SKL-U | Rev: A00

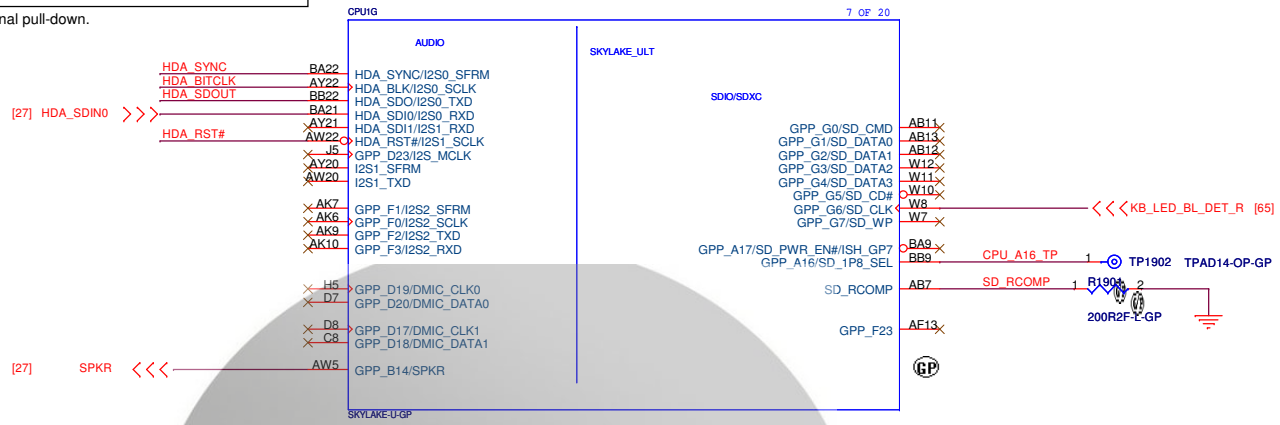
Date: Thursday, February 25, 2016 | Sheet 18 of 106

Main Func = PCH

Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. ★ 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. ★ 1 = Port C is detected.

These two signals have weak internal pull-down.



PCH strap pin:

Flash Descriptor Security Overide/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default ★ High = Enable

The internal pull-down is disabled after PLTRST# deasserts

PCH strap pin:

NO REBOOT	
HDA_SPKR	★ Low = Enable (Default) High = Disable

The internal pull-down is disabled after PLTRST# deasserts

071.SKYLA.000U

3D3V_S0
1KR2J-1-GP
R2006
DY
SPKR

[27] HDA_CODEC_SYNC R1908 0R0402-PAD HDA_SYNC
TPAD14-OP-GP TP1903 HDA_RST#_R R1911 0R0402-PAD HDA_RST#

EC1901
DY
HDA_CODEC_BITCLK
SC10P50V2JN-4GP

HDA_RST#
EC1902
SCD1U16V2KX-3GP

SRN33J-5-GP-U
[27] HDA_CODEC_BITCLK
[27] HDA_CODEC_SDOUT
HDA_BITCLK
HDA_SDOUT
RN1902
[24] ME_FWP_EC R1909 1KR2J-1-GP

R1907,R1912 merge to RN1902
2015/10/06 modify

<Core Design>

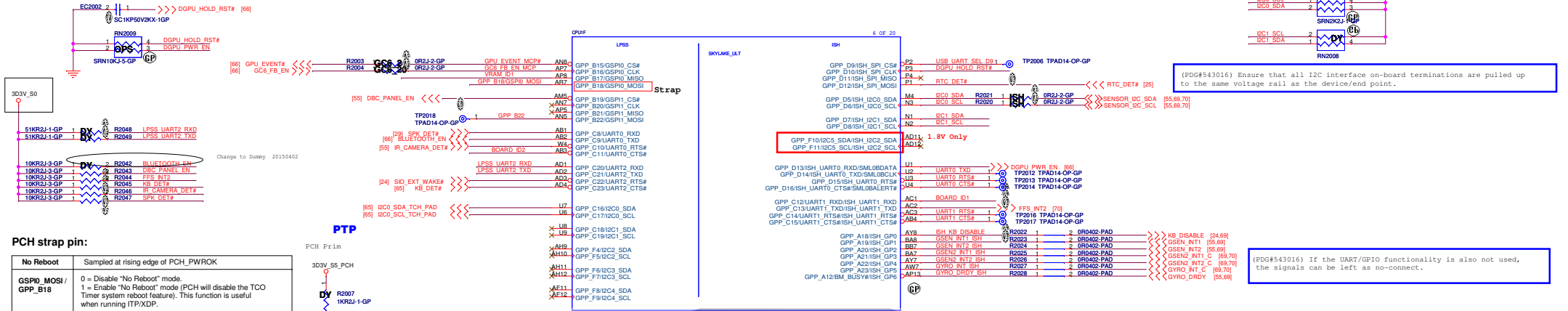
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(AUDIO/SDIO/SDXC)

Size	Document Number	Rev
A3	Starload SKL-U	A00

Date: Thursday, February 25, 2016 Sheet 19 of 106

Main Func = PCH



(PDG#543016) Ensure that all I2C interface on-board terminations are pulled up to the same voltage rail as the device/end point.

(PDG#543016) If the UART/GPIO functionality is also not used, the signals can be left as no-connect.

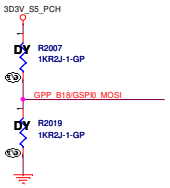
PCH strap pin:

No Reboot	Sampled at rising edge of PCH_PWROK
GSPI0_MOSI / GPP_B18	0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

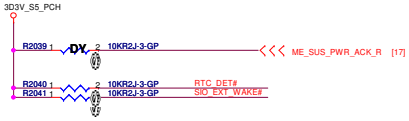
The signal has a weak internal pull-down.

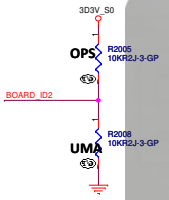
PTP

PCH Prim



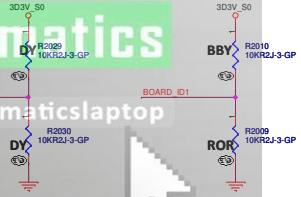
071.SKYLA.000U





BIOS strap pin:

BIOS UMA/DIS Strap pin	BOARD_ID2
UMA	0
DIS	1



<Core Design>

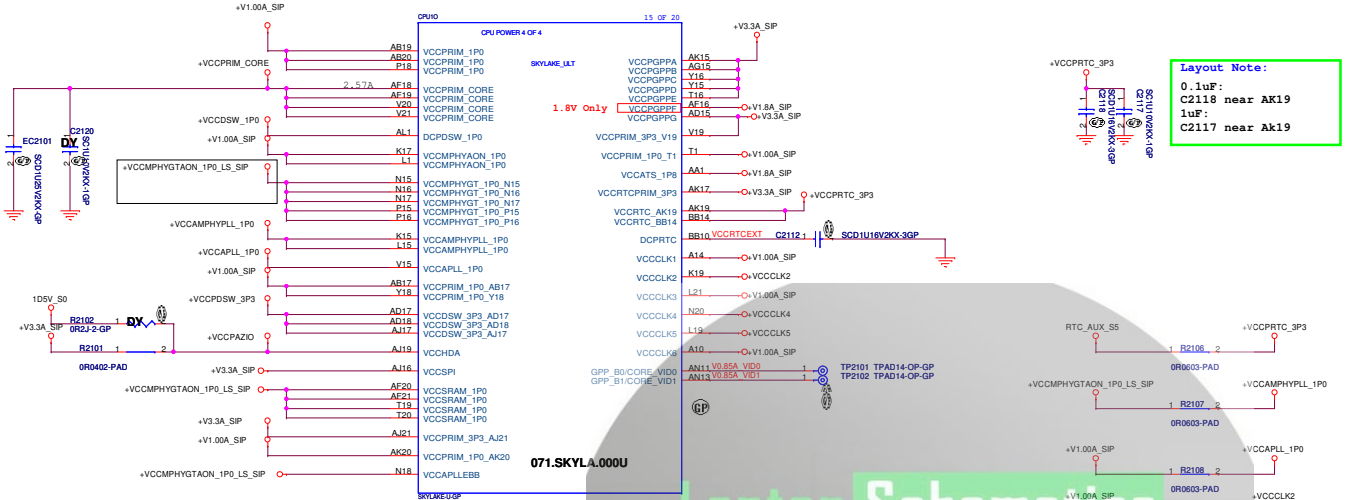
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(LPSS/ISH)

Size: A2 | Document Number: Starload SKL-U | Rev: A00

Date: Thursday, February 25, 2016 | Sheet 20 of 106

Main Func = PCH



Layout Note:
0.1uF:
C2118 near AK19
1uF:
C2117 near Ak19

Layout Note:
1uF:
C2105 near V19
C2106 near AK17
C2107 near AG15
C2109 near Y16
C2110 near T16
C2111 near AJ19

Layout Note:
1uF:
C2101 near AB19
C2104 near K17
C2116 near A10
C2121 near AL1

Layout Note:
22uF:
C2113 near K15

Layout Note:
22uF:
C2113 near K15

Layout Note:
1uF:
C2116 near A10
22uF:
C2115 near K19
C2119 near N20
C2122 near L19

<Core Design>

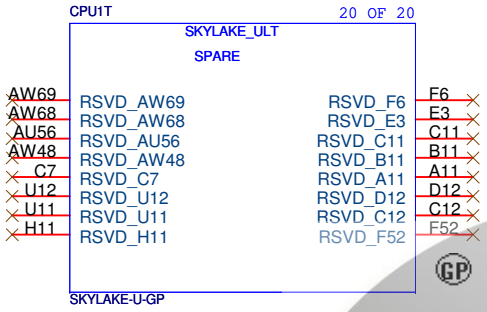
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(POWER1)

Size: A2 | Document Number: Starload SKL-U | Rev: A00

Date: Thursday, February 18, 2016 | Sheet 21 of 106

Main Func = PCH



071.SKYLA.000U

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

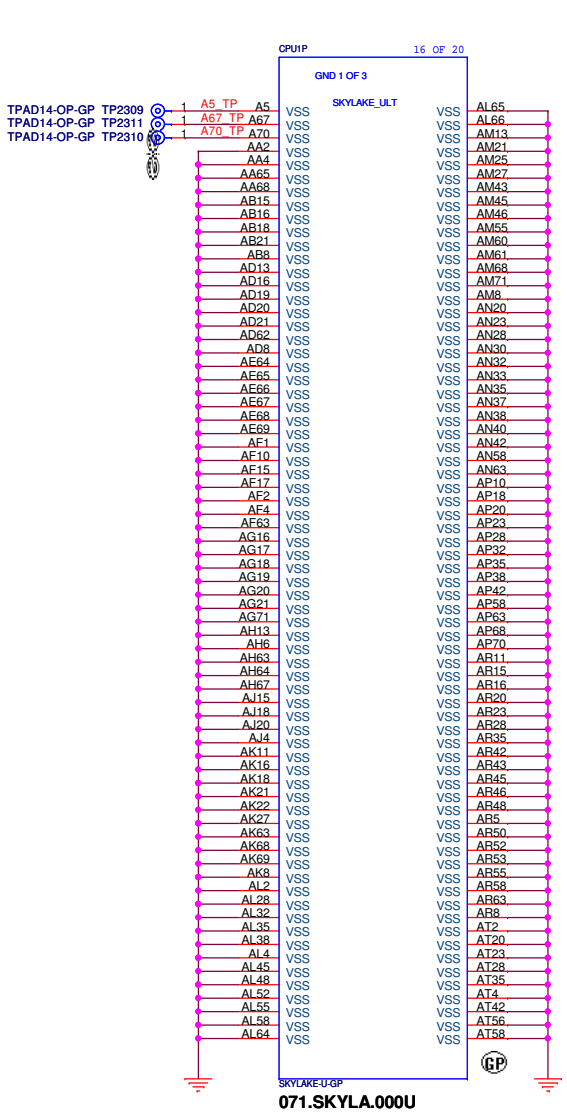
Title

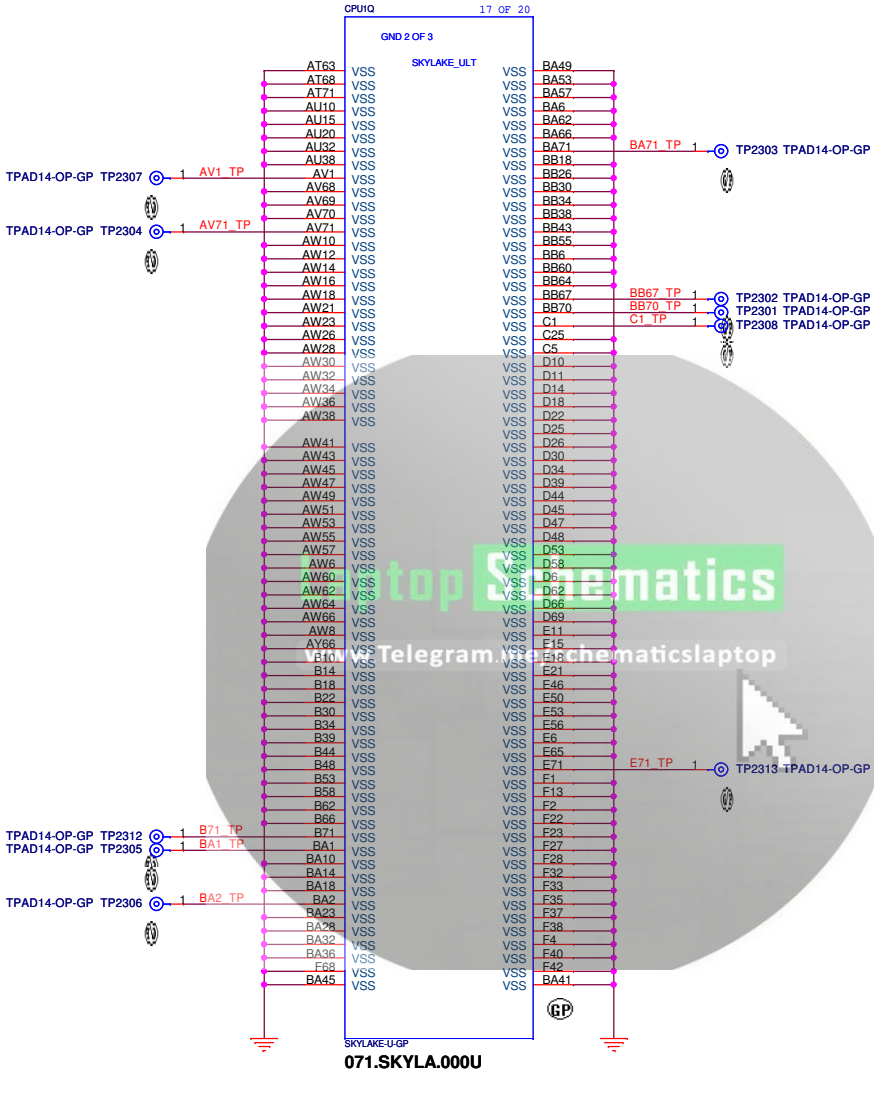
CPU_(RSVD)

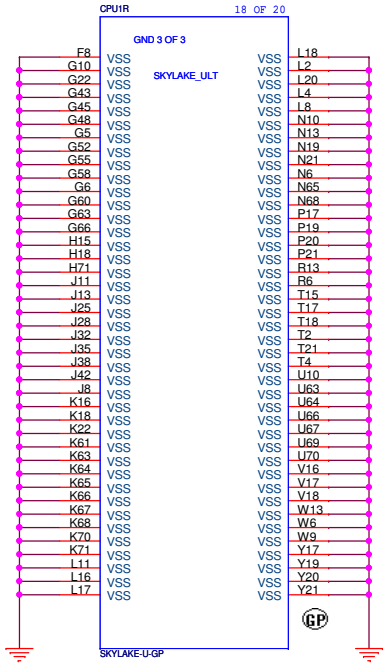
Size	Document Number	Rev
A4	***Starload SKL-U***	***A00***

Date: Thursday, February 18, 2016 Sheet 22 of 106

Main Func = PCH







Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	
BA1	NCTFVSS	Test Point (TP)	Corner BB1
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	
C1	NCTFVSS	Test Point (TP)	Corner A1
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(VSS)

Size: A3 | Document Number: Starload SKL-U | Rev: A00

Date: Thursday, February 18, 2016 | Sheet 23 of 106

Main Func = KBC

BOARD_ID VERSION A/D	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
EVT (SA)	100.0K	10.0K	3.0V
DVT1 (SB)	100.0K	20.0K	2.75V
DVT2 (SC)	100.0K	33.0K	2.48V
DVT3 (SD)	100.0K	47.0K	2.24V
X-build (1)	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

MODEL_ID_DET(GPIO97)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
Starlord UMA_BOM	100.0K	16.0K/64.1002X-GD(1)	3.0V
TBD	100.0K	23.1K/64.2312X-GD(1)	2.782V
Starlord UMA_BRV	100.0K	32.4K/64.3242X-GD(1)	2.492V
TBD	100.0K	47.5K/64.4752X-GD(1)	2.201V
Starlord DIS_BRV	100.0K	64.9K/64.6492X-GD(1)	2.001V
Starlord_ET_EMA	100.0K	93.1K/64.9312X-GD(1)	1.798V
TBD	100.0K	126K/64.1263X-GD(1)	1.493V
TBD	100.0K	200K/64.2003X-GD(1)	1.097V

Just for Starload placement
2015/09/23 modify

Layout Note:
Need very close to EC

Just for Starload placement
2015/09/23 modify

Layout Note:
Need very close to EC

2015/09/22 modify

Layout Note:
Need very close to EC

R2404,R2406 merge to RN2406
2015/10/06 modify

ALL_SYS_PWRGD assert, delay 10ms; PCH_PWROK assert.

071.01404.0B0E

2015/09/22 modify

082.30003.0131

Layout Note:
Connect GND and AGND planes via either 0R resistor or connect directly.

For Typec SMBUS

Change symbol part number, because origin symbol is DELL OBS part

83.R2004.G8F

eDP backlight Control from PCH

Q2412 and Q2413 merge
24014/12/23 modify

84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 75.00601.07C
4th = 84.DMN66.03F

Dummy R2422 & C2427
by EC control PCH_DPWROK
20150416

2015/09/15 modify

Move schematic, 20141118

For Typec charge detect modfy
2016/01/04

Reserve resistor, 20141118

Reserve by NON DS3 function 20150413

2015/09/22 modify

20.K0691.006

R2498,R2499 merge to RN2407
2015/10/06 modify

Just for Starload placement
2015/09/23 modify

Change symbol part number, because origin symbol is DELL OBS part
20150116 2040

83.R2004.G8F

Power Switch Logic(PSL)

X00_0804

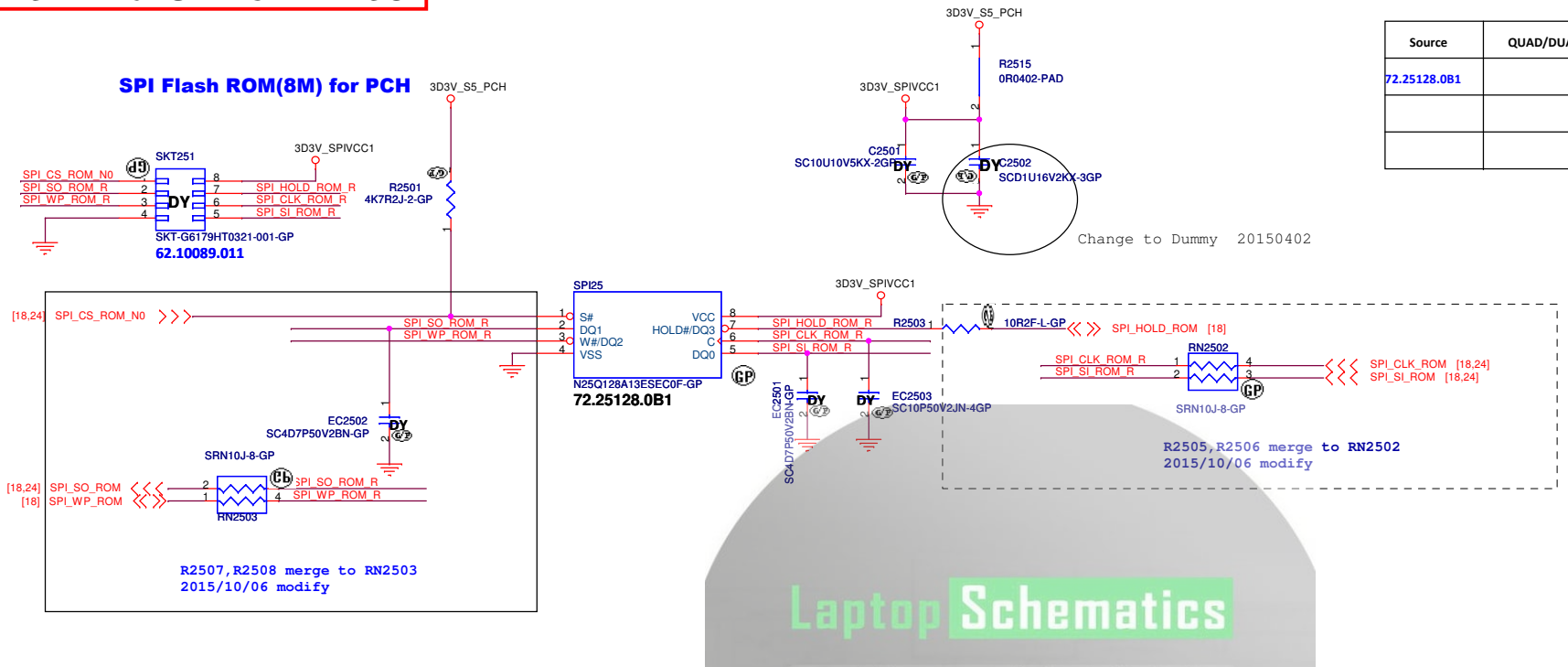
Just for Starload placement
2015/09/23 modify

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

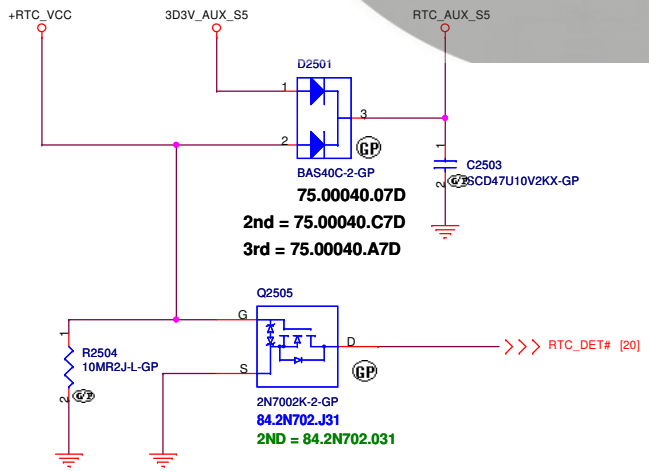
Title: KBC Nuvoton NPCE285PA0DX
Size: A1 | Document Number: Starload SKL-U | Rev: A00
Date: Thursday, February 25, 2016 | Sheet 24 of 156

Main Func = SPI Flash



Source	QUAD/DUAL fast read	DUAL fast read	SFDP
72.25128.0B1	O	O	O
	O	O	O
	O	O	O

Main Func = RTC



<Core Design>

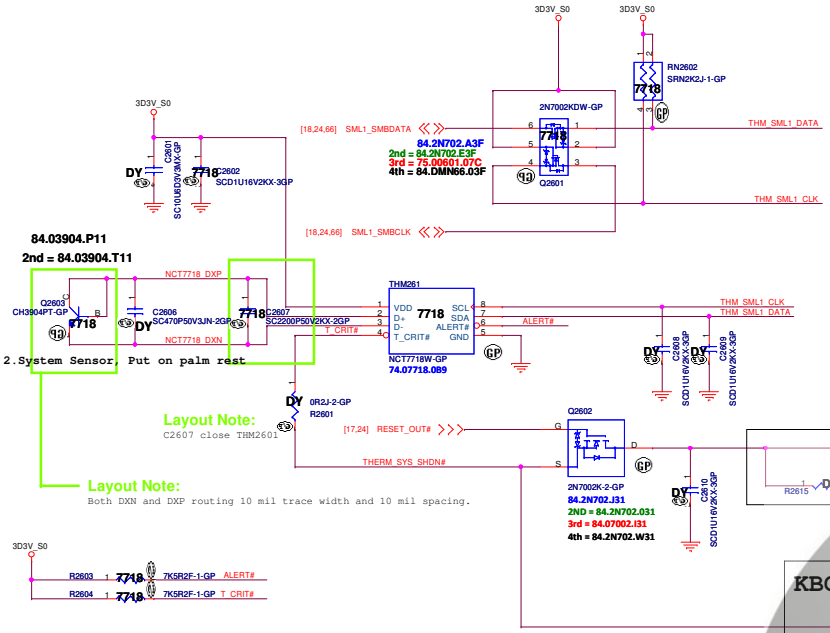
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC

Size: A3 | Document Number: Starload SKL-U | Rev: A00

Date: Thursday, February 25, 2016 | Sheet 25 of 106

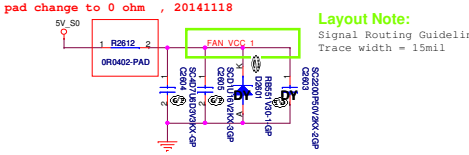
Main Func = Thermal Sensor

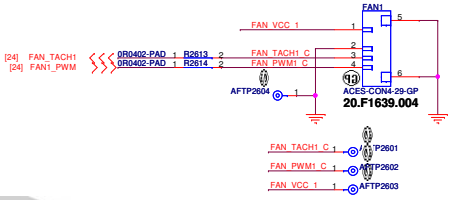


PWM FAN1

Short pad change to 0 ohm , 20141118

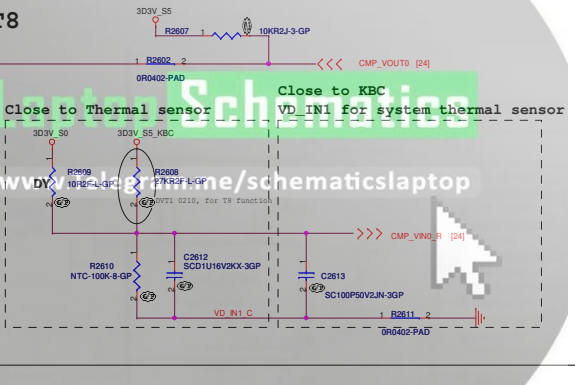
Layout Note:
Signal Routing Guideline:
Trace width = 15mil





TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

KBC T8

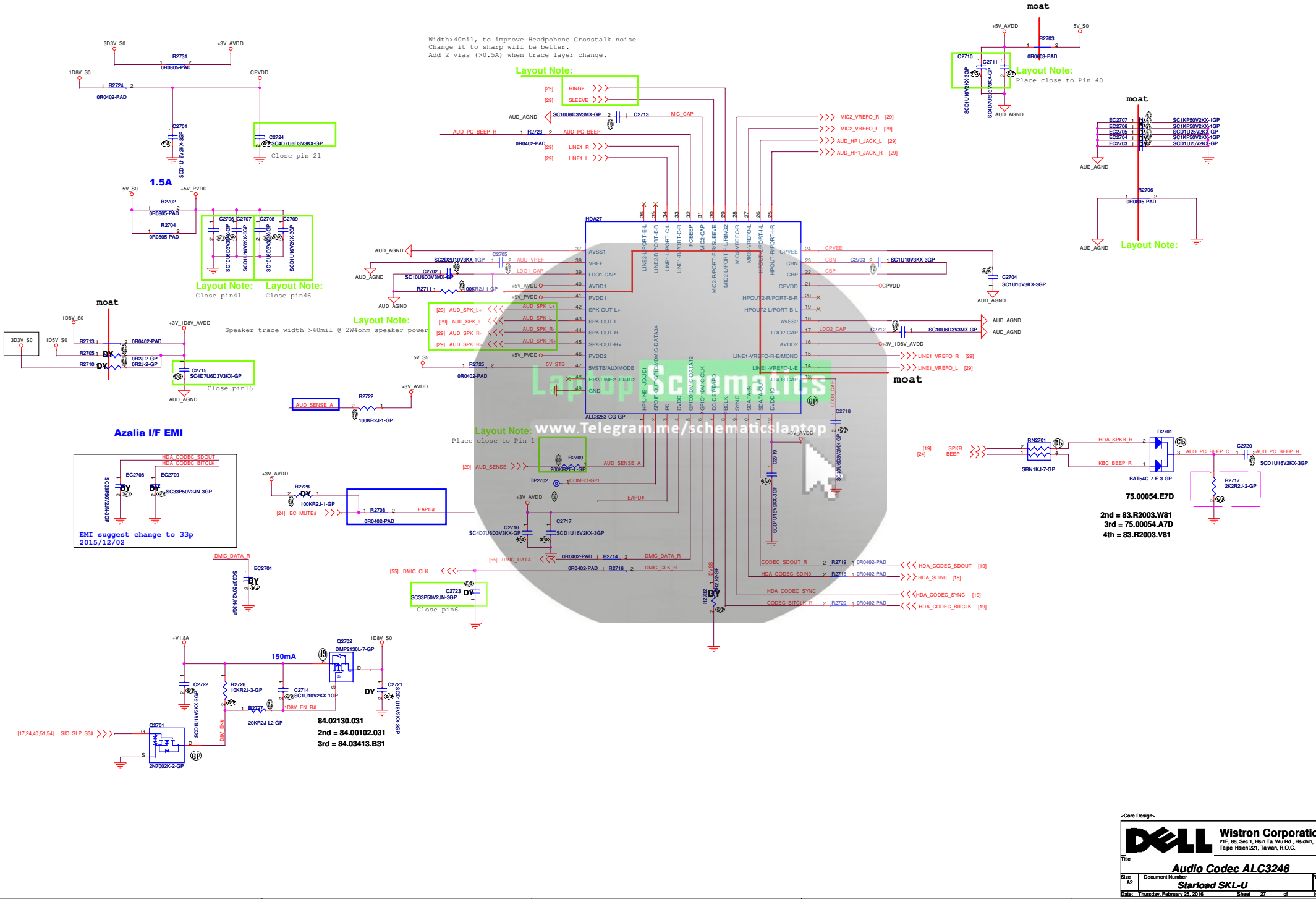


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL NCT7718W/Fan
Size: A2
Document Number: Starload SKL-U
Rev: A00
Date: Thursday, February 25, 2016
Sheet 26 of 106

Main Func = Audio



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio Codec ALC3246**

Size: A2 | Document Number: Starload SKL-U | Rev: A00

Date: Thursday, February 25, 2016 | Sheet 27 of 106

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserved)

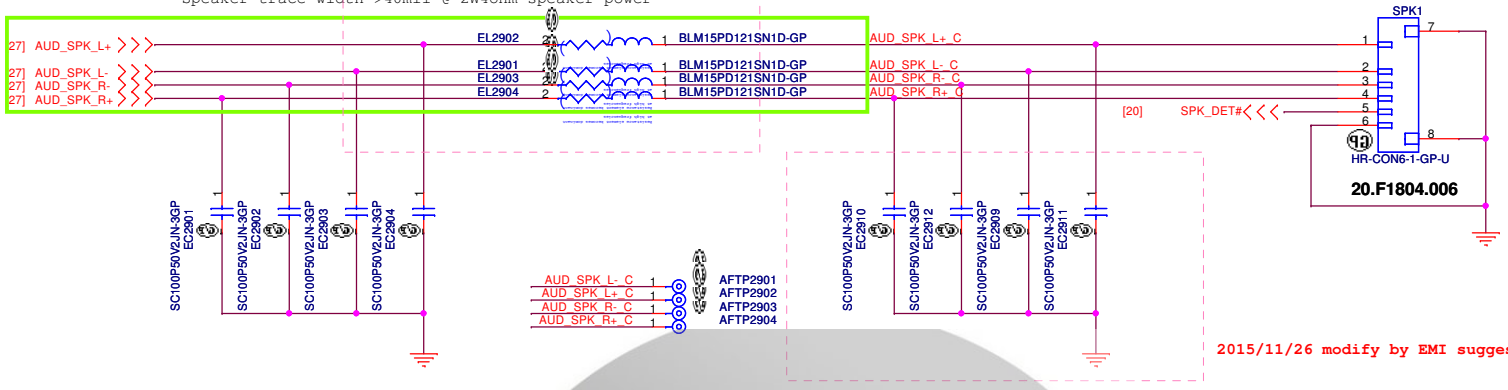
Size	Document Number	Rev
A1	Starload SKL-U	A00

Date: Thursday, February 19, 2015 Sheet 28 of 156

Main Func = Audio

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

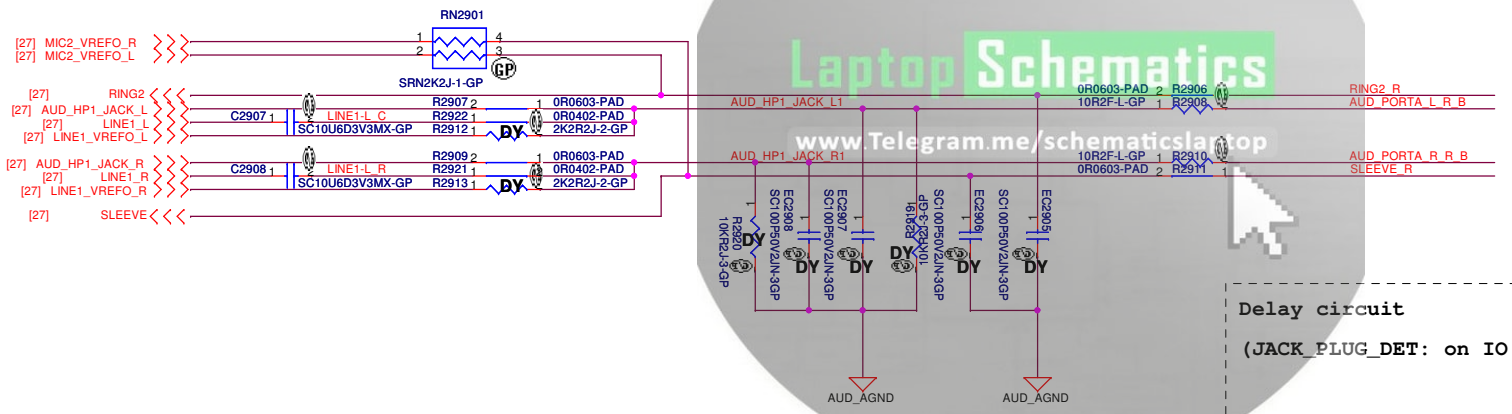
Speaker

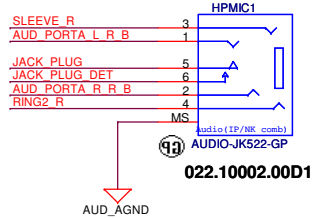


CONN Pin	Net name
Pin1	SPK_L+
Pin2	SPK_L-
Pin3	SPK_R-
Pin4	SPK_R+
Pin5	SPK_DET#
Pin6	GND

2015/11/26 modify by EMI suggest

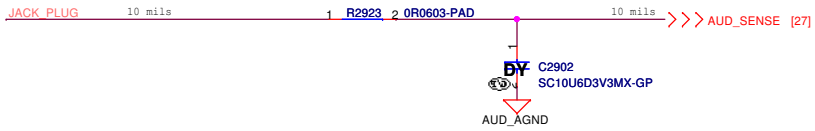
Universal Jack (Moved to I/O Board)

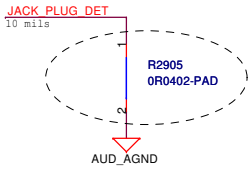




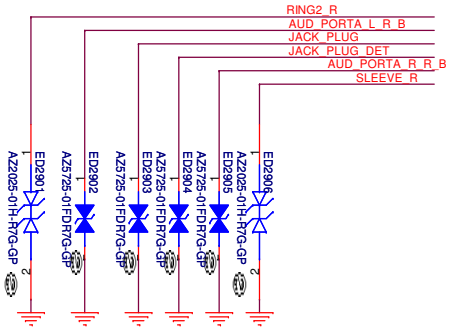
Delay circuit

(JACK_PLUG_DET: on IO Board)





CLOSS TO HPMIC1



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio IO**

Size: A3 | Document Number: **Starload SKL-U** | Rev: **A00**

Date: Thursday, February 25, 2016 | Sheet 29 of 106

Main Func = Audio

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)

Size	Document Number	Rev
A4	Starload SKL-U	A00

Date: Thursday, February 18, 2016 Sheet 30 of 106

Main Func = LAN

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN RTL8106

Size: A2 | Document Number: Starload SKL-U | Rev: A00

Date: Thursday, February 18, 2016 | Sheet 31 of 106

Main Func = LAN

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: XFOM&RJ45

Size: A3 | Document Number: Starload SKL-U | Rev: A00

Date: Thursday, February 18, 2016 | Sheet 32 of 106

Main Func = Card Reader

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

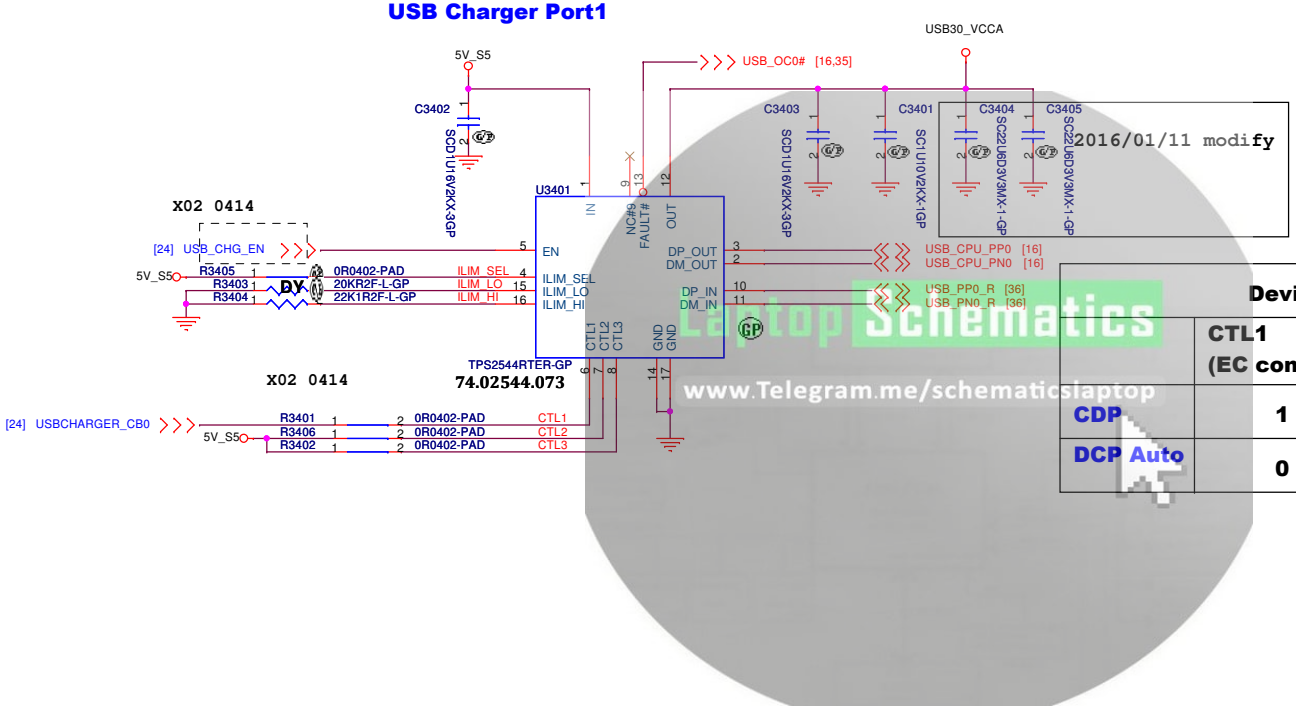
Title: Card Reader-RTS5170

Size: A2 | Document Number: Starload SKL-U | Rev: A00

Date: Thursday, February 18, 2016 | Sheet 33 of 106

Main Func = USB3.0 Port1

USB Charger Port1



Device Control Pins				
	CTL1 (EC control)	CTL2	CTL3	ILIM_SEL
CDP	1	1	1	1
DCP Auto	0	1	1	X

<Core Design>

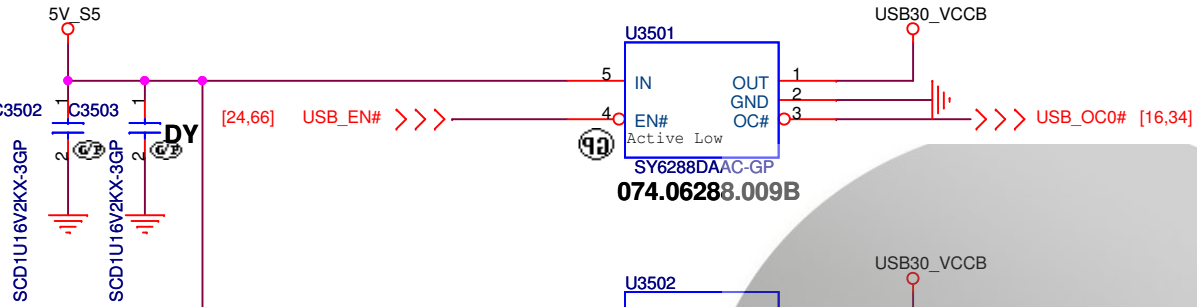
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserved)

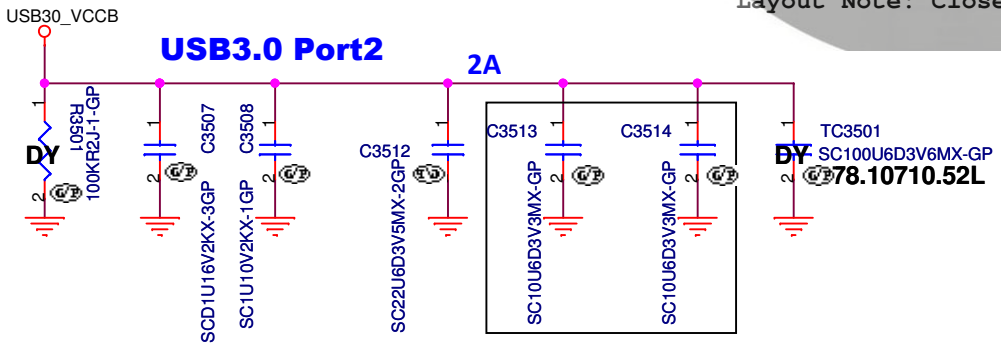
Size: A3 | Document Number: Starload SKL-U | Rev: A00

Date: Thursday, February 25, 2016 | Sheet 34 of 106

Main Func = USB3.0 Port1



Layout Note: Close USB3



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB switch**

Size	Document Number	Rev
	Starload SKL-U	A00

Date: Thursday, February 25, 2016 Sheet 35 of 106

Main Func = USB3.0 Port1

USB3.0 Port1

[16] USB30_TX_CPU_N1 → C3601 SCD1U16V2KX-3GP → USB30_TXDN1_R → R3605 0R0402-PAD → USB30_TXDN1_C

[16] USB30_RX_CPU_N1 → R3609 0R0402-PAD → USB30_RXDN1_C

[16] USB30_TX_CPU_P1 → C3602 SCD1U16V2KX-3GP → USB30_TXDP1_R → R3606 0R0402-PAD → USB30_TXDP1_C

[16] USB30_RX_CPU_P1 → R3610 0R0402-PAD → USB30_RXDP1_C

[34] USB_PP0_R ↔ DLP11SN900HL2L-GP TR3602 ↔ USB20_DP0_C

[34] USB_PN0_R ↔ DLP11SN900HL2L-GP TR3602 ↔ USB20_DN0_C

USB2.0 Port2 and USB2.0 Port3 are on IOBD

EU3601
USB30_RXDN1_C / USB30_RXDP1_C → USB30_RXDN1_C / USB30_RXDP1_C
USB30_TXDN1_C / USB30_TXDP1_C → USB30_TXDN1_C / USB30_TXDP1_C
ESD3V3U4ULC-GP
83.3V3U4.0A0

USB30_VCCA

EU3602
USB20_DN0_C → I/O1 … USB20_DP0_C
GND, VDD, I/O2, I/O3, I/O4
AZC099-04S-1-GP
75.09904.07C
2nd = 75.02304.07C

EMI for DVT1 0212

USB30_VCCA

USB2
VBUS, D-, D+ → USB20_DN0_C / USB20_DP0_C
STDA_SSRX-, STDA_SSRX+ ← USB30_RXDN1_C / USB30_RXDP1_C
STDA_SSTX-, STDA_SSTX+ ← USB30_TXDN1_C / USB30_TXDP1_C
GND_DRAIN, GND, GND, GND, CHASSIS#12, CHASSIS#13
SKT-USB13-221-GP
022.10005.01P1

USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

USB3.0 Port2

ROR

[16] USB30_TX_CPU_N2 → C3603 SCD1U16V2KX-3GP → USB30_TXDN2_R → R3611 0R0402-PAD → USB30_TXDN2_C

[16] USB30_RX_CPU_N2 → R3612 0R0402-PAD → USB30_RXDN2_C

[16] USB30_TX_CPU_P2 → C3604 SCD1U16V2KX-3GP → USB30_TXDP2_R → R3614 0R0402-PAD → USB30_TXDP2_C

[16] USB30_RX_CPU_P2 → R3613 0R0402-PAD → USB30_RXDP2_C

[16] USB_CPU_PP1 ↔ DLP11SN900HL2L-GP TR3603 ↔ USB20_DP1_C

[16] USB_CPU_PN1 ↔ DLP11SN900HL2L-GP TR3603 ↔ USB20_DN1_C

EU3603
USB30_RXDN2_C / USB30_RXDP2_C → USB30_RXDN2_C / USB30_RXDP2_C
USB30_TXDN2_C / USB30_TXDP2_C → USB30_TXDN2_C / USB30_TXDP2_C
ESD3V3U4ULC-GP
83.3V3U4.0A0

USB30_VCCB

EU3604
USB20_DN1_C → I/O1 … USB20_DP1_C
GND, VDD, I/O2, I/O3, I/O4
AZC099-04S-1-GP
75.09904.07C
2nd = 75.02304.07C

EMI for DVT1 0212

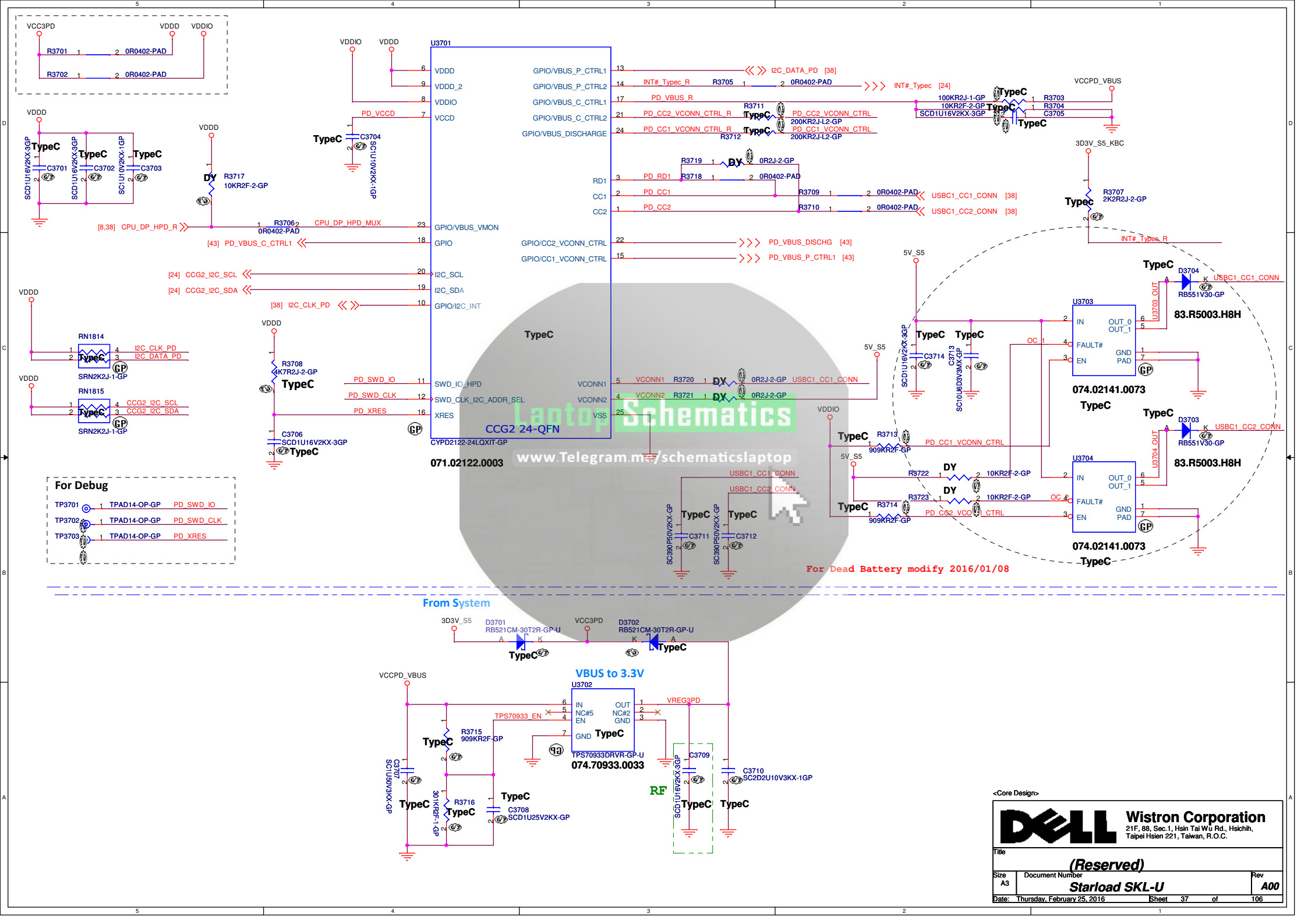
USB30_VCCB

USB3
VBUS, D-, D+ → USB20_DN1_C / USB20_DP1_C
STDA_SSRX-, STDA_SSRX+ ← USB30_RXDN2_C / USB30_RXDP2_C
STDA_SSTX-, STDA_SSTX+ ← USB30_TXDN2_C / USB30_TXDP2_C
GND_DRAIN, GND, GND, GND, CHASSIS#12, CHASSIS#13
SKT-USB13-221-GP
022.10005.01P1

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB30
Size: A3 | Document Number: Starload SKL-U | Rev: A00
Date: Thursday, February 25, 2016 | Sheet 36 of 106



<Core Design>

Wistron Corporation
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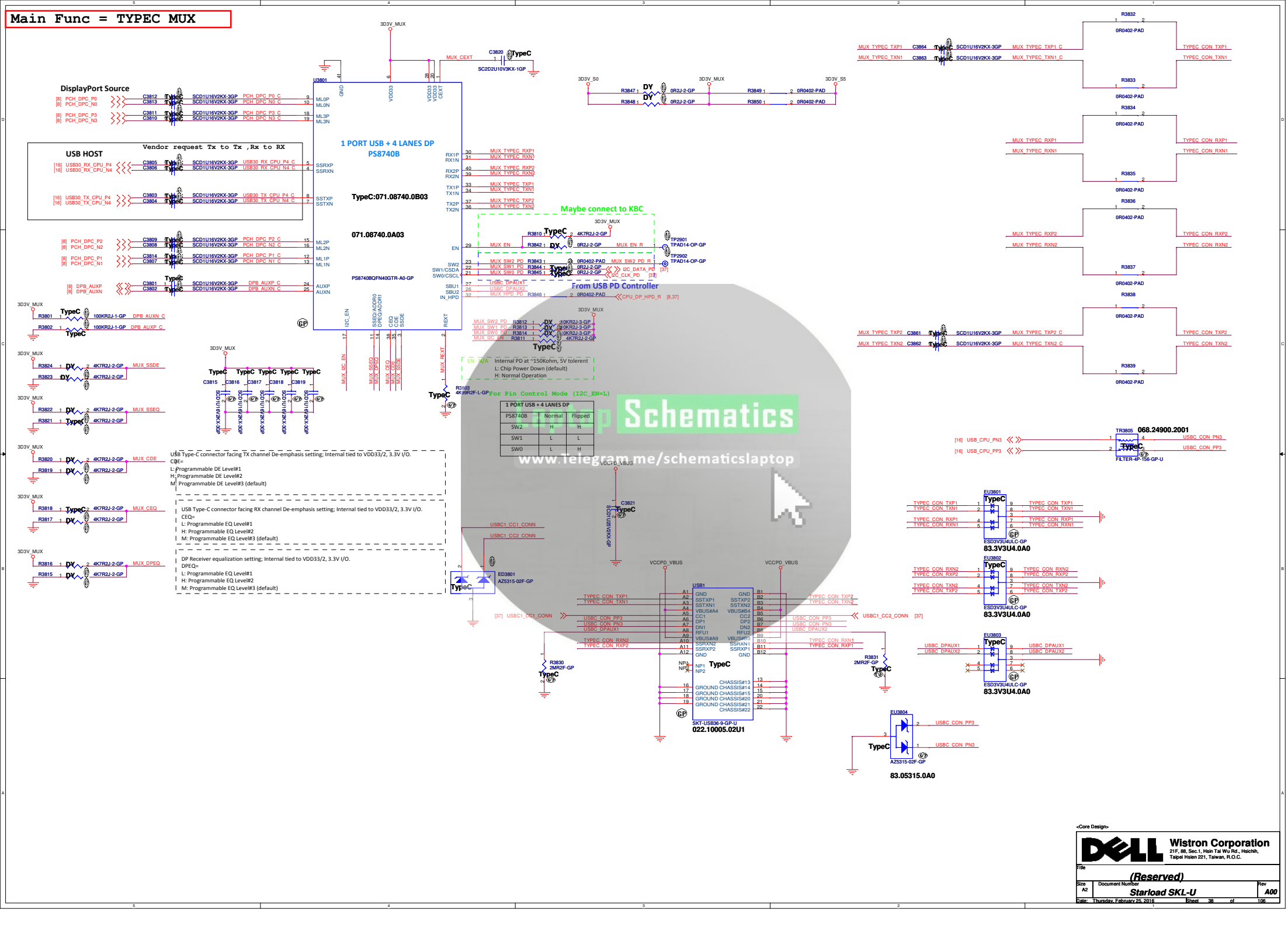
Title: *(Reserved)*

Size	Document Number	Rev
A3	*Starload SKL-U*	*A00*

Date: Thursday, February 25, 2016 Sheet 37 of 106

Main Func = TYPEC MUX



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Title: (Reserved)

Size: A2 | Document Number: Starload SKL-U | Rev: A00

Date: Thursday, February 25, 2016 | Sheet 38 of 106

Main Func = USB3.0 Port1

<Core Design>

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Title: (Reserved)

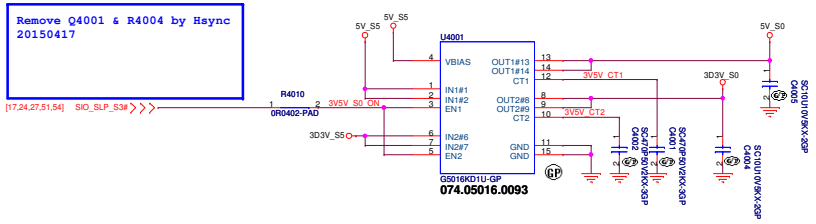
Size	Document Number	Rev
A2	Starload SKL-U	A00

Date: Thursday, February 18, 2016 Sheet 39 of 106

Main Func = Power Plane & Sequence

ROSA Run Power

Remove Q4001 & R4004 by Hsync
20150417

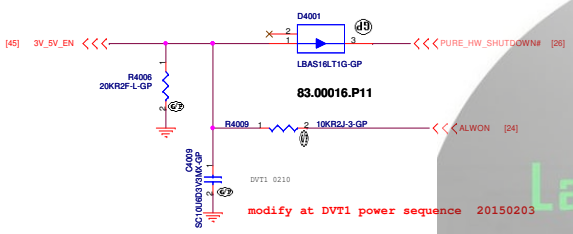


5V_S0

5V_S0 Comsumption
Peak current 5A

3D3V_S0

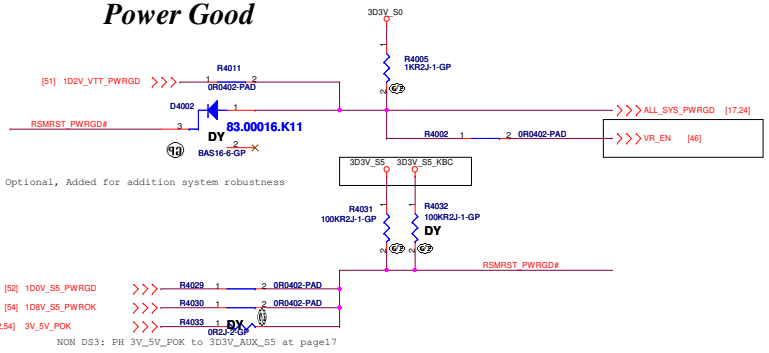
3D3V_S0 Comsumption
Peak current 2.5A



modify at DVT1 power sequence 20150203

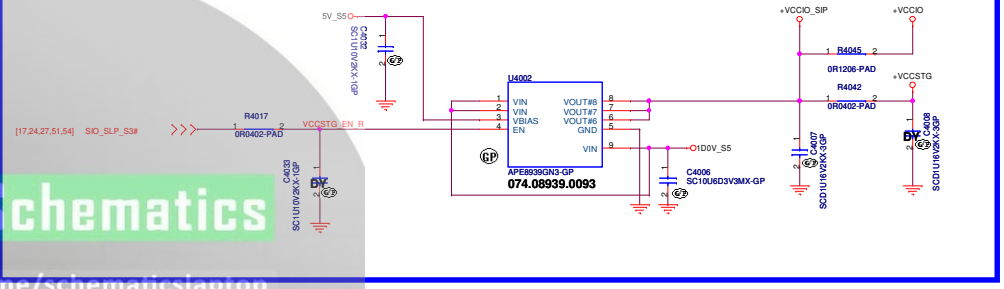
20150116 2032

Power Good



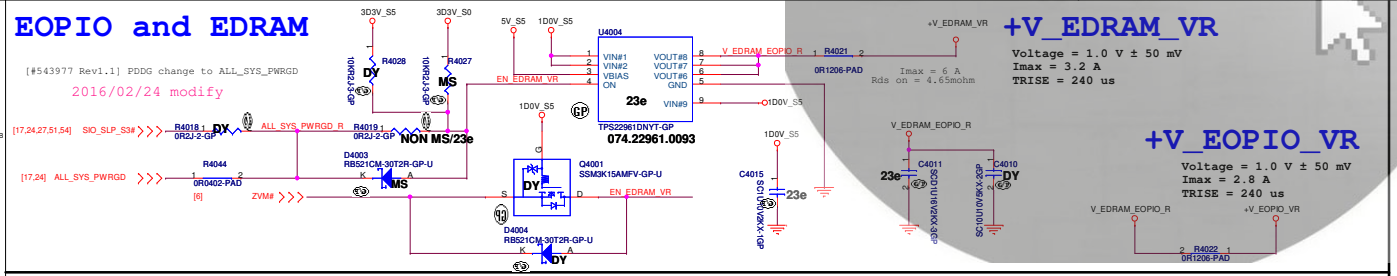
VCCIO and VCCSTG

Modify power switch IC and relate schematic
2016/01/07



EOPIO and EDRAM

[#543977 Rev1.1] PDDG change to ALL_SYS_PWRGD
2016/02/24 modify



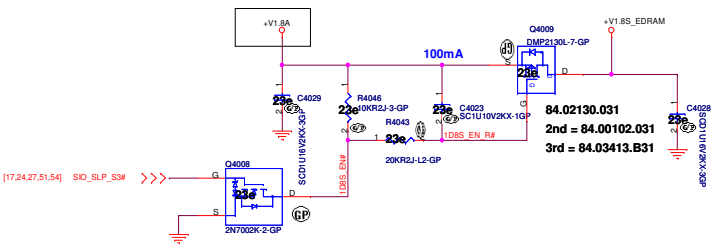
+V_EDRAM_VR

Voltage = 1.0 V ± 50 mV
Imax = 3.2 A
TRISE = 240 us

+V_EOPIO_VR

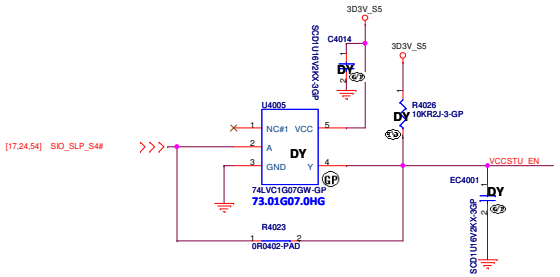
Voltage = 1.0 V ± 50 mV
Imax = 2.8 A
TRISE = 240 us

V1.8S

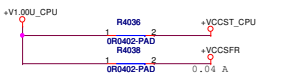


MANAGEMENT RAIL POWER GENERATION

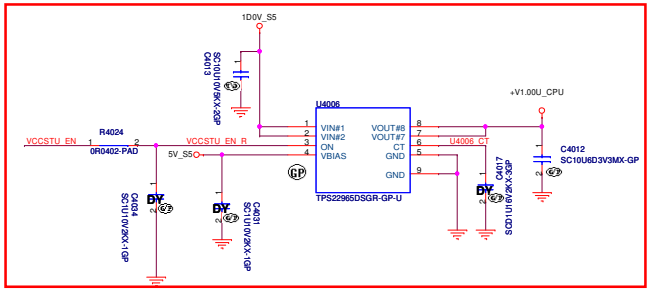
VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization.



VCCST



Modify power switch IC and relate schematic ,DVT1 20150204



<Core Design>

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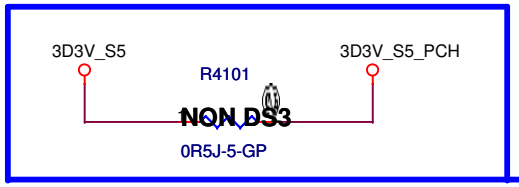
Title: Power Plane Enable

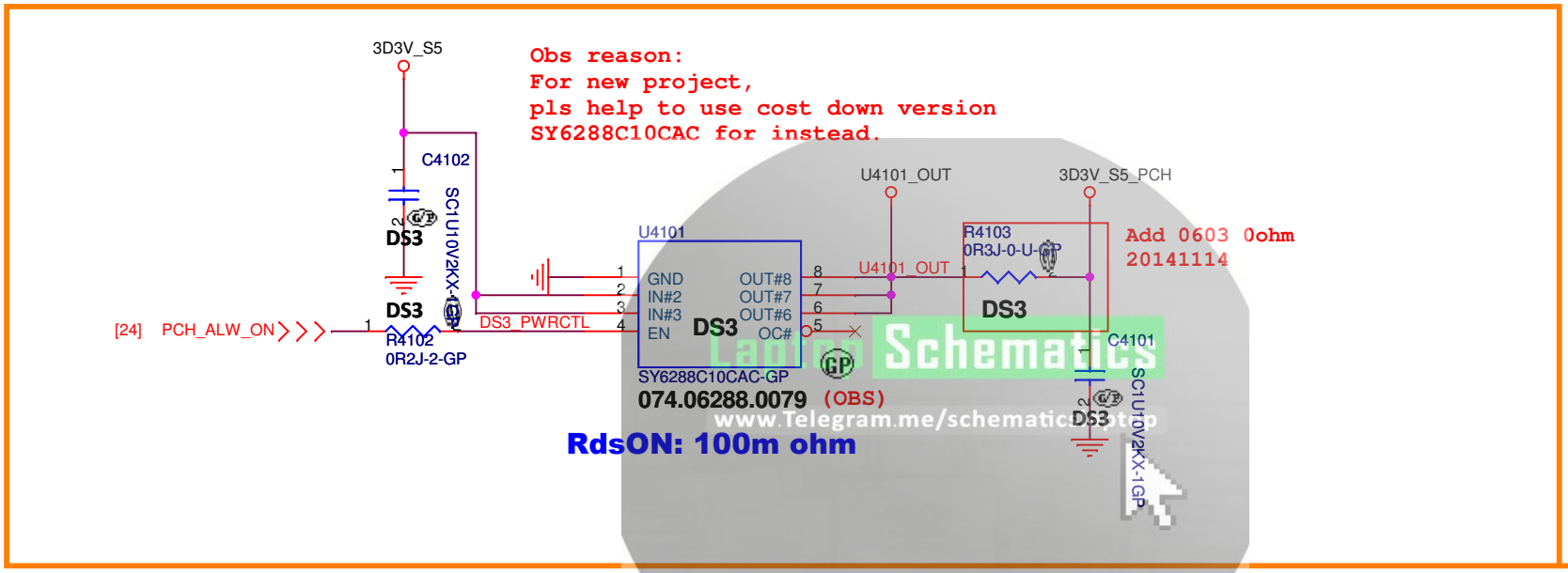
Size	Document Number	Rev
A2	Starload SKL-U	A00

Date: Thursday, February 25, 2016 Sheet 40 of 106

Main Func = Power Plane & Sequence



Reserve by NON DS3 function 20150413



DS3

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Connected_Standby(1/2)+DS3

Size	Document Number	Rev
A4	Starload SKL-U	A00

Date: Thursday, February 25, 2016 Sheet 41 of 106

Main Func = DIMM1
Main Func = DIMM2

<Core Design>

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Title: *Connected_Standby(2/2)*

Size	Document Number	Rev
A3	Starload SKL-U	A00

Date: Thursday, February 18, 2016 Sheet 42 of 106

Main Func = ADT Input

Layout Note:
PSID Layout width > 25mil

Pin Definition: TBD

60ohm@100MHz
DCR=0.02 ohm
Max current = 6000mA

2016/01/07 mofiy

DY discharge schematic AC_DIS change to SATA LED function 2016/02/03 modify

Id=-9.6A
Qg=-25nC
Rdson=18~30mohm

PD_VBUS_C_CTRL1 = 1 (Consumer Path OFF)
PD_VBUS_C_CTRL1 = 0/Z (Consumer Path ON)

PD_VBUS_P_CTRL1 = 1 (Provider Path ON)
PD_VBUS_P_CTRL1 = 0/Z (Provider Path OFF)

PD_VBUS_DISCHG = 1 (VBUS Discharging)
PD_VBUS_DISCHG = 0/Z (VBUS not discharging)

Main Func = M-BAT Input

Batt Connecter

Placement: Close to Batt Connector

2nd = 75.00099.K7D	2nd = 75.00099.K7D	2nd = 75.00099.K7D
3rd = 75.00099.Q7D	3rd = 75.00099.Q7D	3rd = 75.00099.Q7D
4th = 75.00099.D7D	4th = 75.00099.D7D	4th = 75.00099.D7D

TypeC Protect circuit
2015/11/26 modify

<Core Design>

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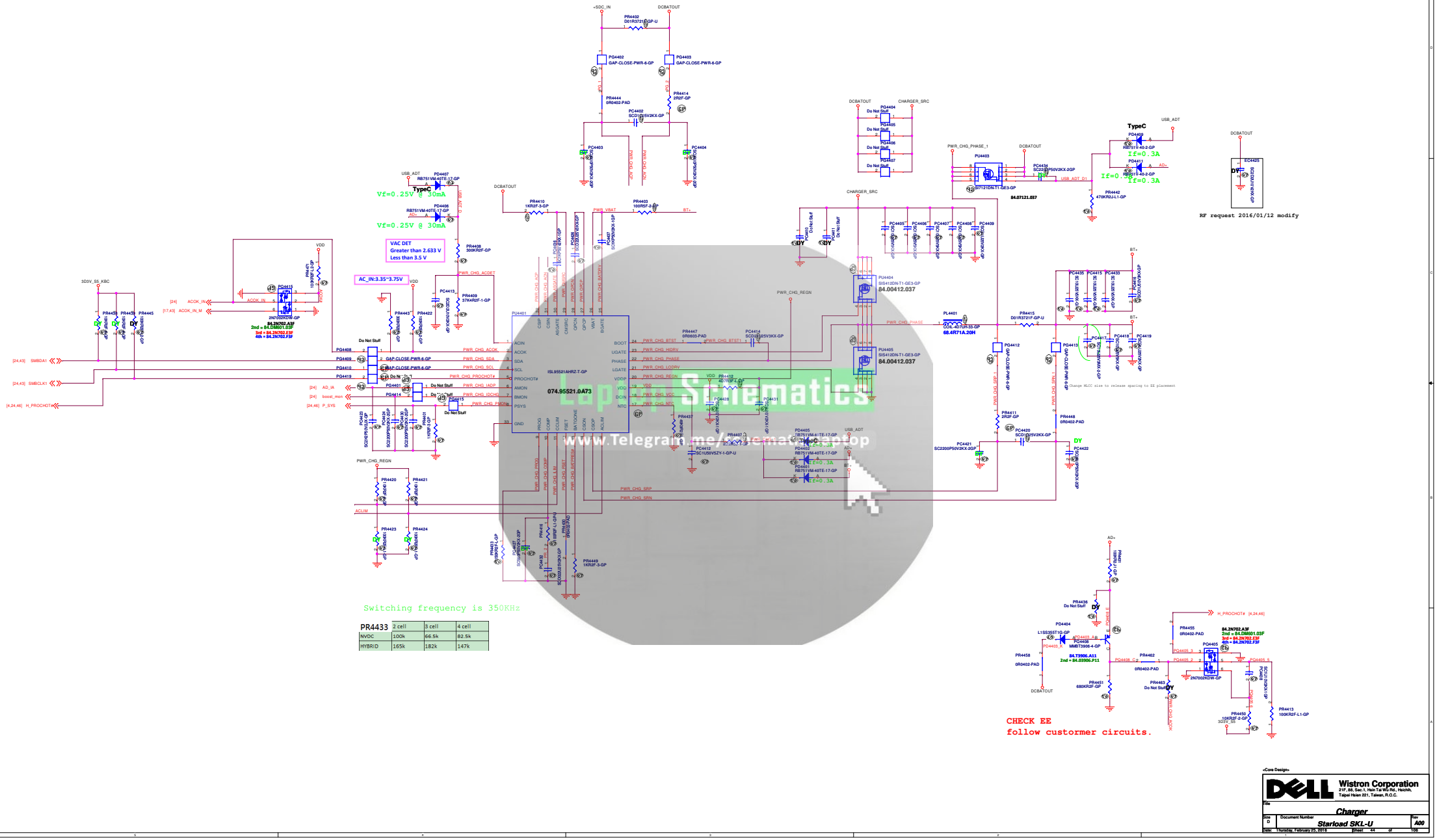
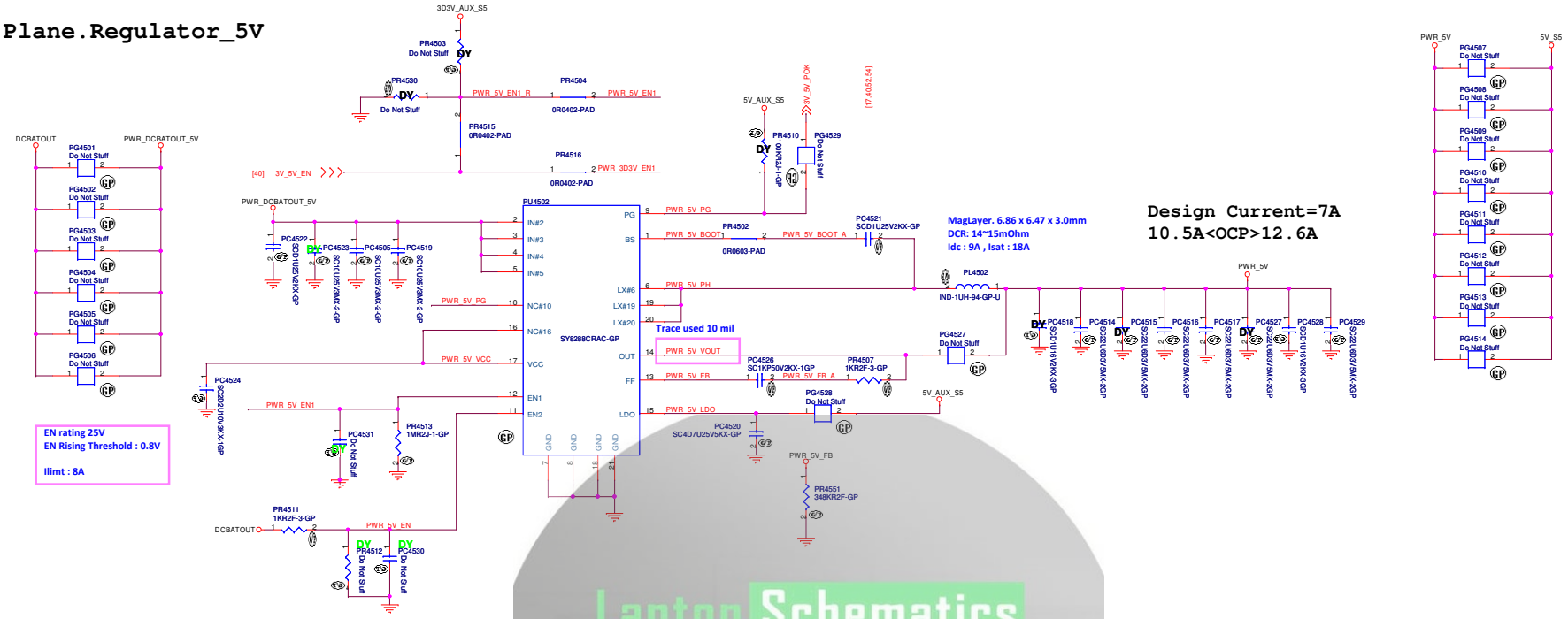
Title: DCIN
Size: A2 | Document Number: Starload SKL-U | Rev: A00
Date: Thursday, February 25, 2016 | Sheet 43 of 106

Main Func = Charger

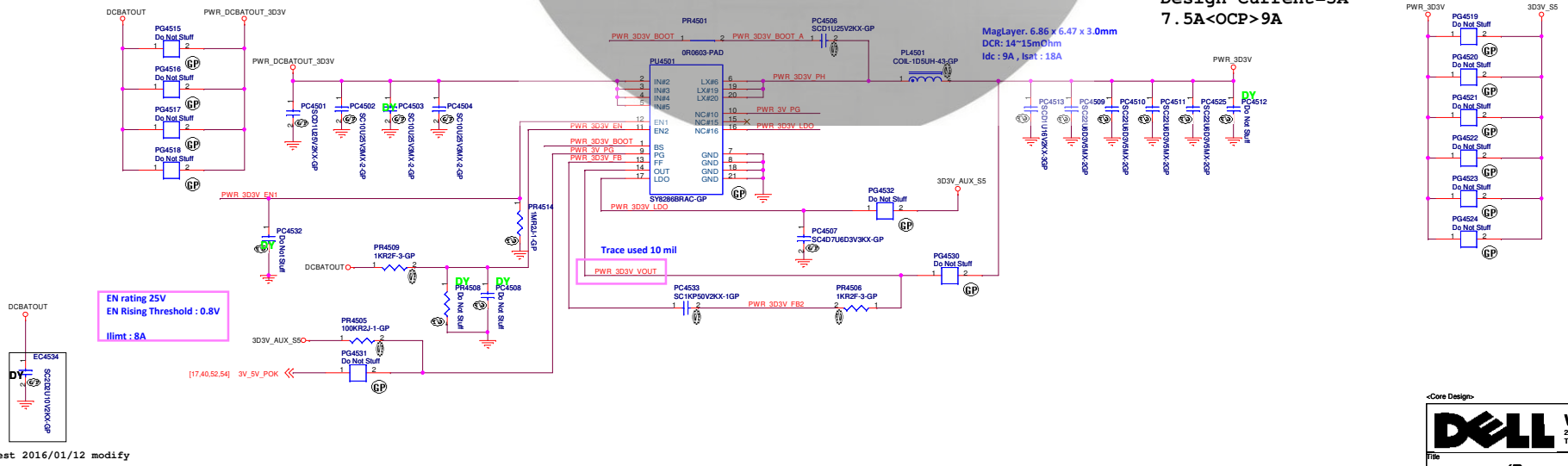


PR4433	2 cell	3 cell	4 cell
NVDC	100k	66.5k	82.5k
HYBRID	165k	182k	147k

SSID = PWR.Plane.Regulator_5V



SSID = PWR.Plane.Regulator_3D3V



RF request 2016/01/12 modify

<Core Design>

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Title: (Reserved)

Size	Document Number	Rev
A2	Starload SKL-U	A00

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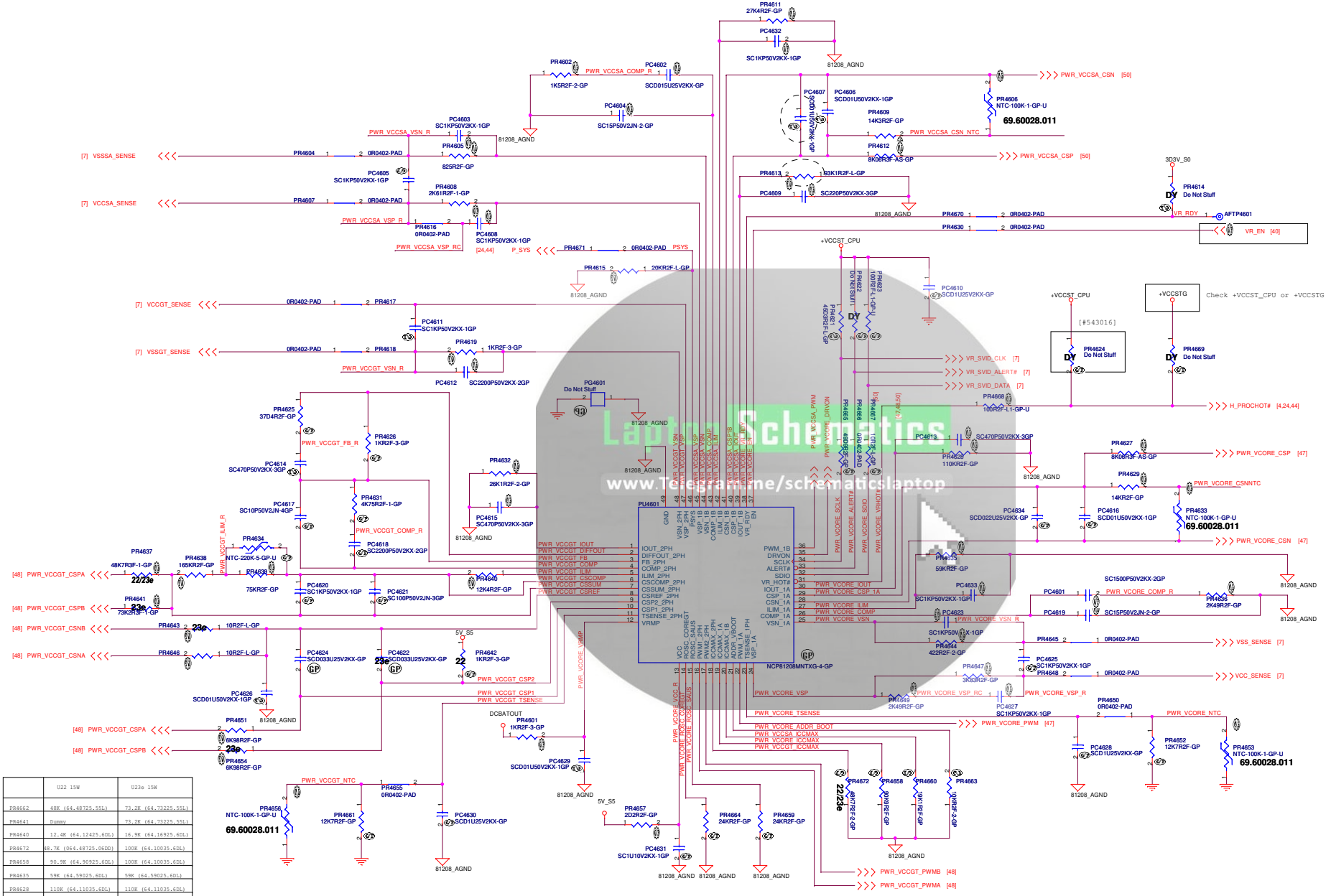
Main Func = CPU_CORE



	U22 15W	U23e 15W
PR4662	48K (64.48725.55L)	73.2K (64.73225.55L)
PR4641	Dummy	73.2K (64.73225.55L)
PR4640	12.4K (64.12425.6DL)	16.9K (64.16925.6DL)
PR4672	48.7K (064.48725.06DD)	100K (64.10035.6DL)
PR4658	90.9K (64.90925.6DL)	100K (64.10035.6DL)
PR4635	59K (64.59025.6DL)	59K (64.59025.6DL)
PR4628	110K (64.11035.6DL)	110K (64.11035.6DL)
PR4643	Dummy	10R (64.10R05.6DL)
PR4654	Dummy	6.98K (64.69815.6DL)
PC4624	Dummy	D33U (78.33322.2FL)
PR4642	1K (64.10015.6DL)	Dummy
PR4602	1.5K (64.15015.6DL)	1.5K (64.15015.6DL)
PC4602	15n (78.15322.2FL)	15n (78.15322.2FL)

<Core Design>

Wistron Corporation
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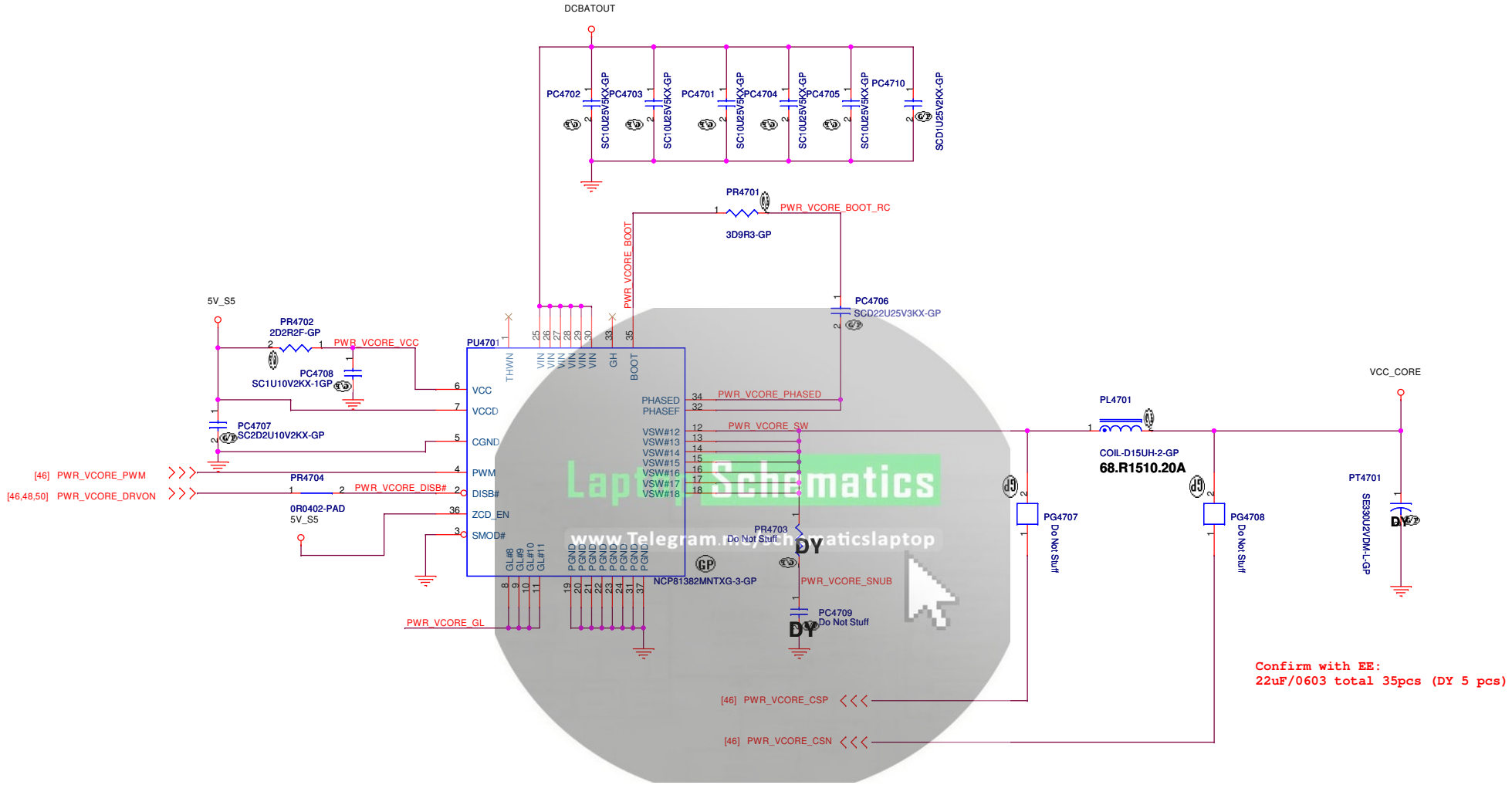
Taipei Hsien 221, Taiwan, R.O.C.

Title: NCP81208MN_CPU_VCORE(1/3)

Size: A2 | Document Number: Starload SKL-U | Rev: A00

Date: Thursday, February 25, 2016 | Sheet 46 of 106

Main Func = CPU_CORE



<Core Design>

Wistron Corporation
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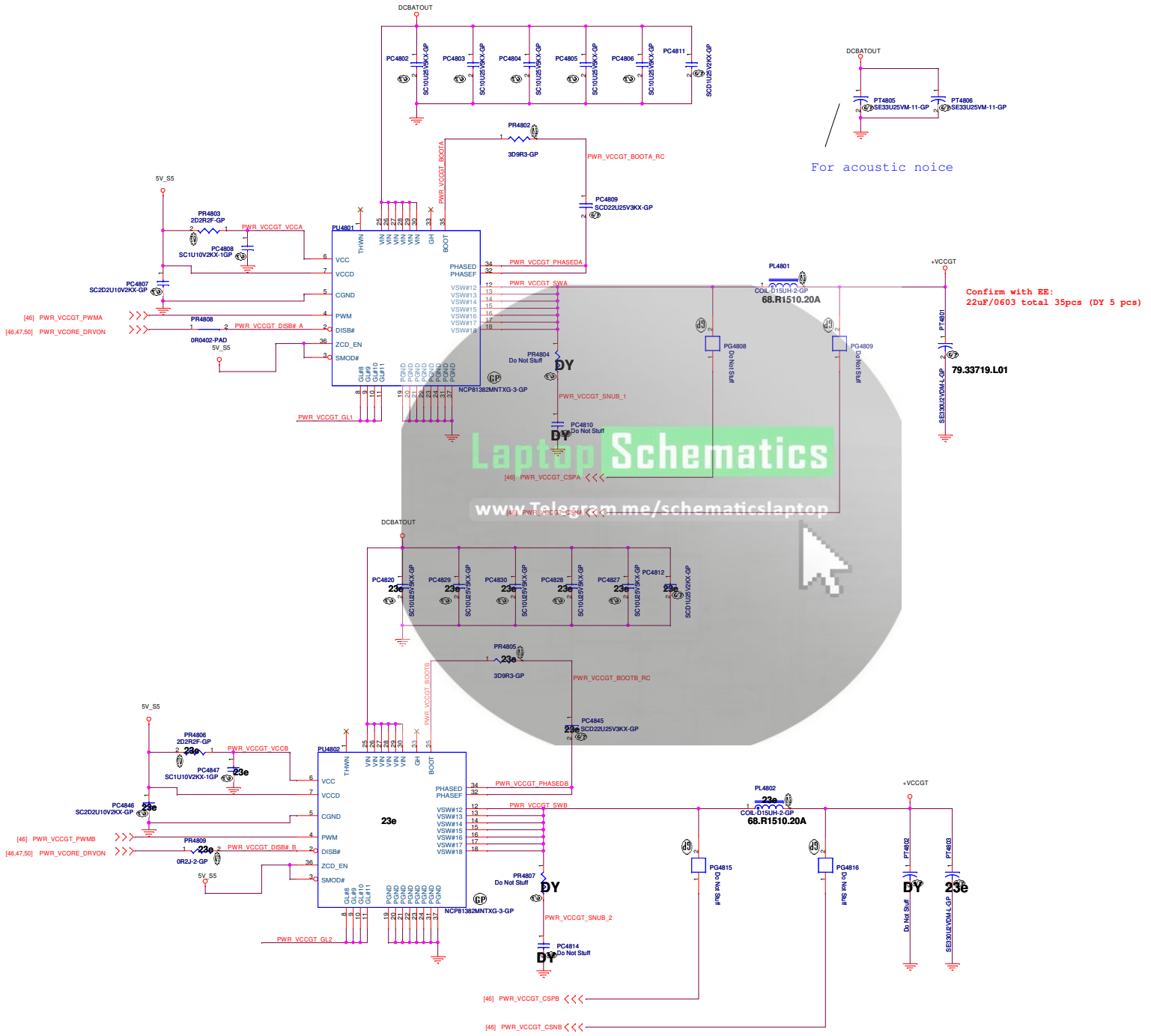
Taipei Hsien 221, Taiwan, R.O.C.

Title: NCP81382MN_CPU_VCORE(2/3)

Size: A3 | Document Number: Starload SKL-U | Rev: A00

Date: Thursday, February 25, 2016 | Sheet 47 of 106

Main Func = CPU_CORE



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: NCP81382MN_CPU_VCCGT(3/3)

Size: A2 | Document Number: Starload SKL-U | Rev: A00

Date: Thursday, February 25, 2016 | Sheet 48 of 106

<Core Design>

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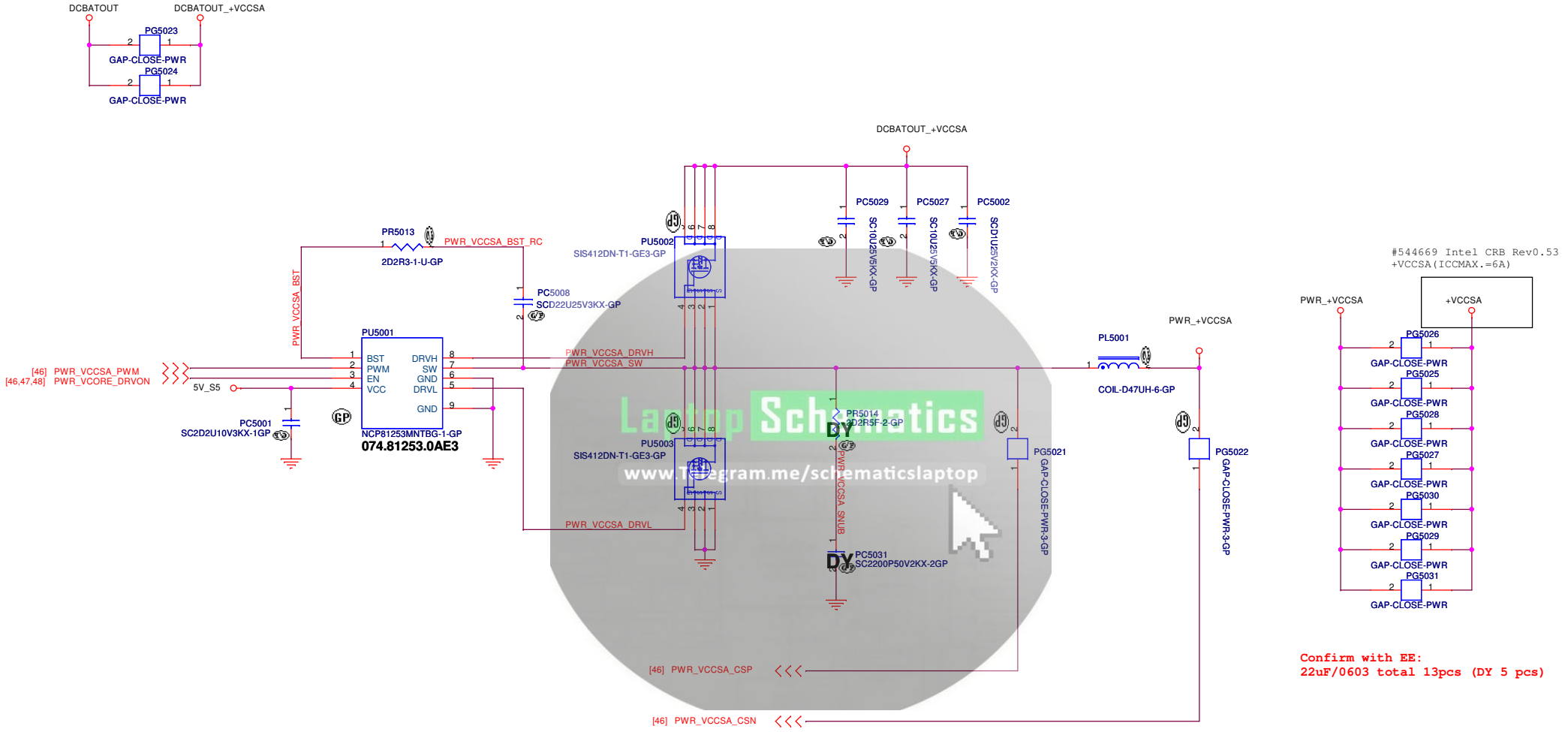
Title: NCP81210MN_CPU_VCCGTUS

Size: A2 | Document Number: Starload SKL-U | Rev: A00

Date: Thursday, February 18, 2016 | Sheet 49 of 106

Main Func = CPU_CORE



#544669 Intel CRB Rev0.53
+VCCSA(ICCMAX.=6A)

Confirm with EE:
22uF/0603 total 13pcs (DY 5 pcs)

<Core Design>

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Title	VCCSA	
Size A3	Document Number Starload SKL-U	Rev A00
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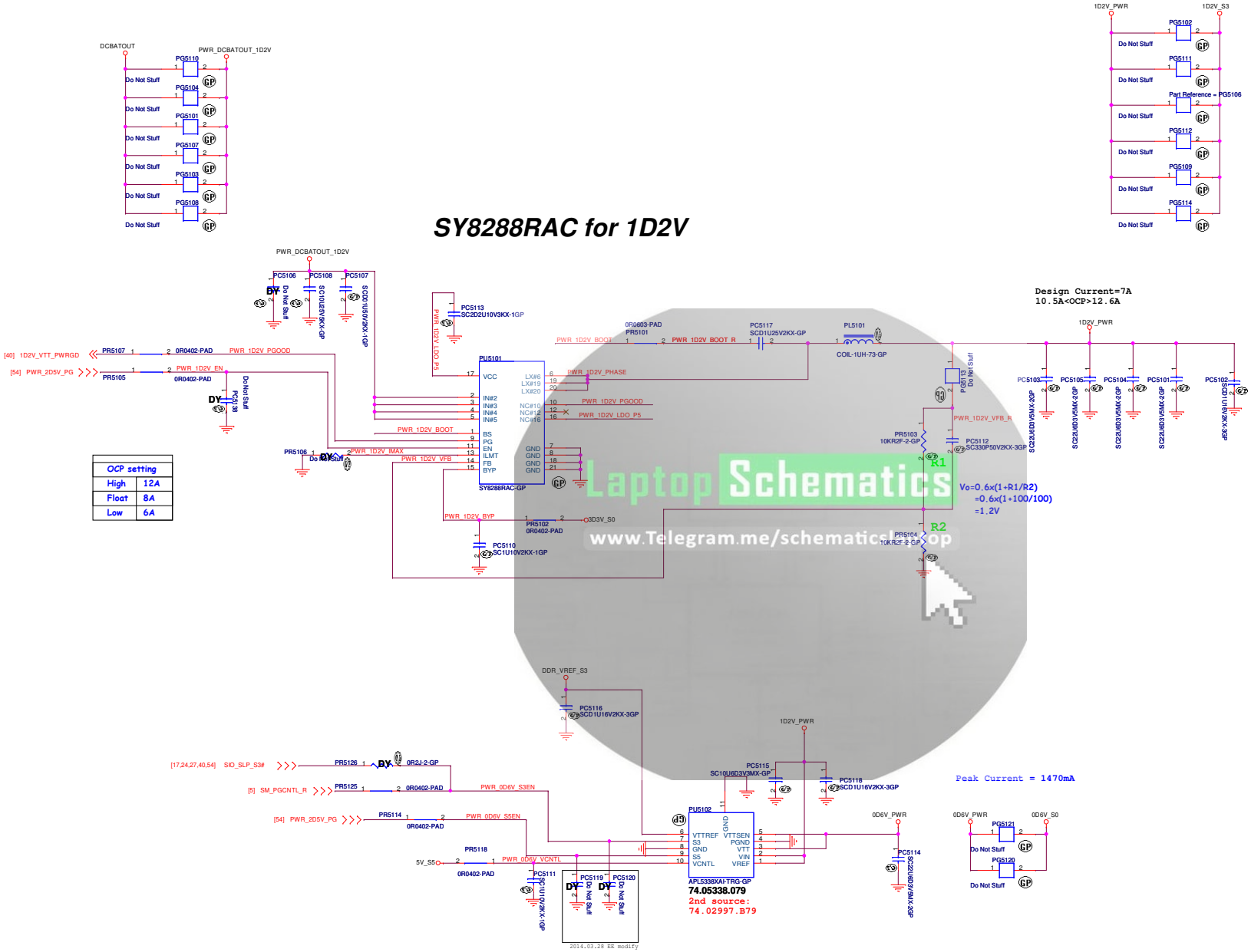
SSID = PWR.Plane.Regulator_1p2v

SY8288RAC for 1D2V



<Core Design>

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Title: (Reserved)

Size	Document Number	Rev
A2	Starload SKL-U	A00

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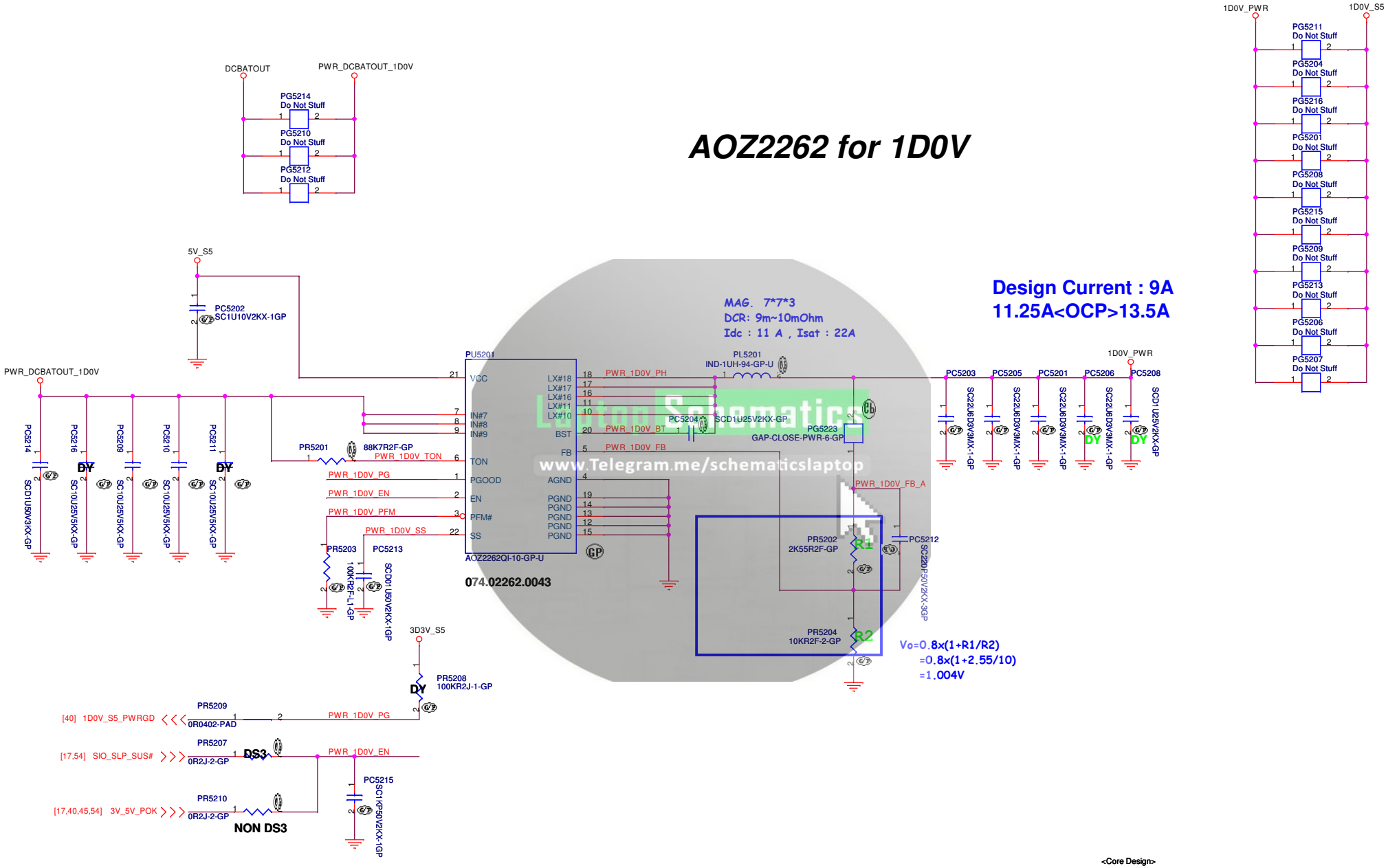
SSID = PWR.Plane.Regulator_1D0V

AOZ2262 for 1D0V



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserved)

Size: A3 | Document Number: Starload SKL-U | Rev: A00

Date: Thursday, February 25, 2016 | Sheet 52 of 106

<Core Design>

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Title

(Reserved)

Size	Document Number	Rev
A3	*Starload SKL-U*	*A00*

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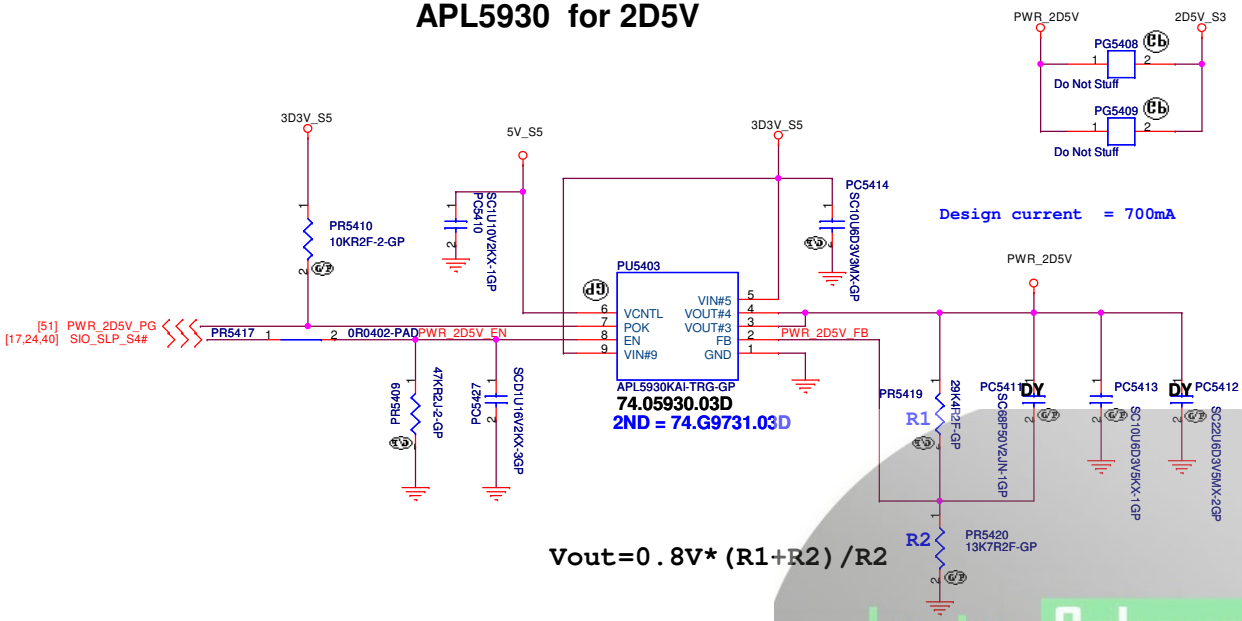
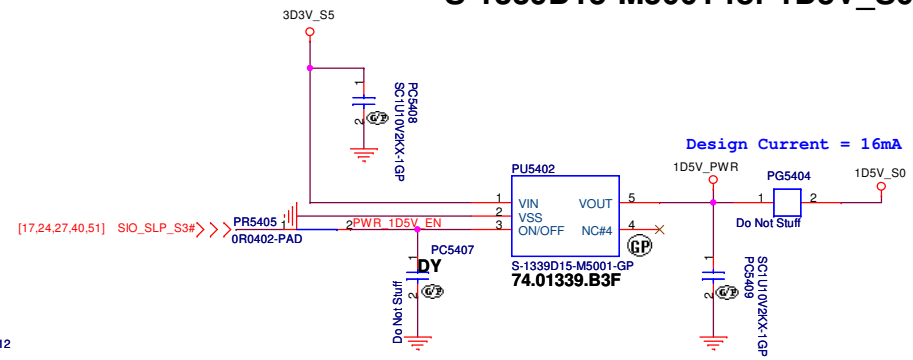
Main Func = 1D5V

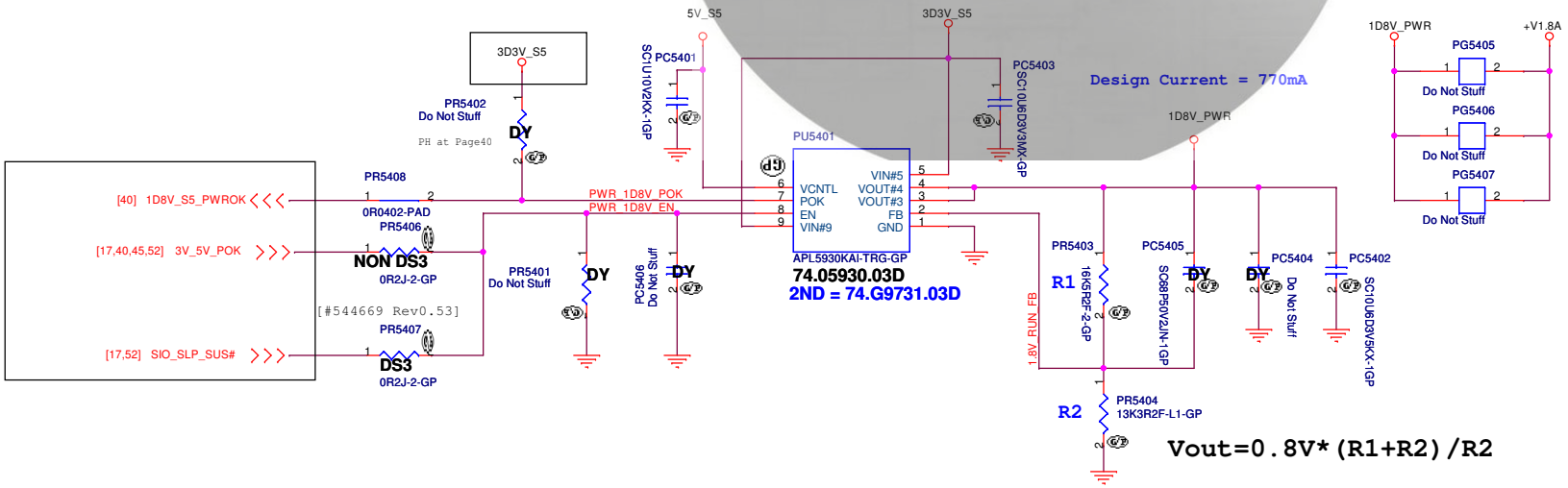
APL5930 for 2D5V



S-1339D15-M5001 for 1D5V_S0



APL5930 for 1D8V_S5



<Core Design>

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Title: (Reserved)

Size	Document Number	Rev
A3	Starload SKL-U	A00

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Main Func = LCD

Panel Conn.

Backup , 20141114

LCD1 — 20.F1407.040 (IPEX-CON40-3-GP)

DCBATOUT_LCD, LCDVDD

EDP_AUX / EDP_AUX# — C5510 / C5511 — SCD1U16V2KX-3GP — EDP_AUX_DP / EDP_AUX_DN [8]

EDP_TX3# / EDP_TX3 — C5532 / C5531 — EDP_TX3_DN / EDP_TX3_DP [8]

EDP_TX2# / EDP_TX2 — C5533 / C5519 — EDP_TX2_DN / EDP_TX2_DP [8]

EDP_TX1# / EDP_TX1 — C5501 / C5504 — EDP_TX1_DN / EDP_TX1_DP [8]

EDP_TX0# / EDP_TX0 — C5506 / C5509 — EDP_TX0_DN / EDP_TX0_DP [8]

EDP_HPD_CONN

LCD_TST_C

LCD_BRIGHTNESS

BLON_OUT_C

DBC_EN_R — R5503 — 0R0402-PAD — DBC_PANEL_EN [20]

X02 0414

R5501 — 0R0402-PAD — MIC_GND

Power Pin Count : 7

GND Pin Count : 9

HSYNC

Remove HSYNC schematic
201511276

IR CAMERA Power

DCBATOUT_CAMERA — R5520 0R3J-0-U-GP — DCBATOUT

C5542 SCD1U50V3KX-GP

C5534 SC1KP50V2KX-1GP

TCBD1

JAE-CON32-2-GP-U — 20.K0801.032

DCBATOUT_CAMERA, 3D3V_SEN_S0, 3D3V_CAMERA_S0

SENSOR_I2C_SDA [20,69,70]

SENSOR_I2C_SCL [20,69,70]

GSEN_INT1 [20,69]

GSEN_INT2 [20,69]

GYRO_INT [70]

GYRO_DRDY [20,69]

USB_CAMERA_P, USB_CAMERA_N

DMIC_CLK_C, DMIC_DATA_C

MIC_GND

IR_CAMERA_DET# — R5540 — 0R0402-PAD — IR_CAMERA_DET# [20]

TPAN_VDD

USB_PP5_TPNL, USB_PN5_TPNL

TOUCH_PANEL_INTR# [4,24]

Hi:2.0V
Lo:0.8V
LCDVDD Layout 80 mil

[8] EDP_VDD_EN — D5501 BAT54C-7-F-3-GP — 75.00054.E7D

[24] LCD_TST_EN

LVDS_VDD_EN_R

LCDVDD

U5501 RT9724GB-GP — 74.09724.09F — 2ND = 74.03514.07F

3D3V_S0

C5507 SCD1U16V2KX-3GP, C5508 SC1U10V2KX-1GP, C5505 SC4D7U6D3V3KX-GP

Add 0ohm , 20141118

C5502 SC4D7U6D3V3KX-GP

R5502 0R2J-2-GP DY

D5502 BAT54C-7-F-3-GP — 75.00054.E7D

BKLT_CTRL — L_BKLT_CTRL [8]

LCD_TST

R5504,R5505 merge to RN5503
2015/10/06 modify

RN5503 SRN33J-5-GP-U

DMIC_CLK_C — DMIC_CLK [27]

DMIC_DATA_C — DMIC_DATA [27]

EC5503, EC5504 SC22P50V2JN-4GP — EMI DVT1 0210

RN5501 SRN100J-4-GP

LCD_TST_C, BLON_OUT_C, LCD_BRIGHTNESS, BKLT_CTRL

LCD_TST [24], PANEL_BKEN_EC [24]

EDP_HPD_CONN — R5506 100R2J-2-GP — EDP_HPD [8]

RN5502 SRN100KJ-5-GP

LVDS_VDD_EN_R, EDP_HPD, BLON_OUT_C, BKLT_CTRL

LCD_BRIGHTNESS — EC5501 DY SC6D8P50V2DN-GP

USB_CAMERA_N — USB_CPU_PN4 [16]

DLP11SN900HL2L-GP — TR5501

USB_CAMERA_P — USB_CPU_PP4 [16]

USB_PN6_TPNL — R5510 — 0R0603-PAD — USB_CPU_PN6 [16]

USB_PP6_TPNL — R5511 — 0R0603-PAD — USB_CPU_PP6 [16]

CAMERA POWER

3D3V_S0 — Add 0603 0ohm , 20141118 — R5513 DY 0R3J-0-U-GP — 3D3V_CAMERA_S0

F5502 POLYSW-D5A6V1-GP — 69.50007.921

EC5502 SCD1U25V2KX-GP, C5503 SC4D7U6D3V3KX-GP

INVERTER POWER

Add 1206 0ohm , 20141118

DCBATOUT — R5514 DY 0R6J-L-GP — DCBATOUT_LCD

F5503 POLYSW-1D1A24V-GP-U — 69.50007.A31 — 2nd = 69.50007.D31

C5512 SCD1U16V3KX-GP, C5513 SC1KP50V2KX-1GP, C5514 SC22U10V6KX-GP, C5518 SC22U10V6KX-GP

Starload height limite change to 0603 package
2015/09/24 modify

SENSOR POWER

3D3V_S0 — R5516 DY 0R3J-0-U-GP — 3D3V_SEN_S0

Add 0603 0ohm , 20141118

F5504 POLYSW-1D1A6V-9-GP-U — 69.48001.081

EC5505 SC33P50V2JN-3GP DY, C5515 SC4D7U6D3V3KX-GP

TOUCH PANEL POWER

5V_S0 — TPAN_VDD

69.50007.A31
2nd = 69.50007.D31
3rd = 69.50007.A41

F5501 POLYSW-1D1A24V-GP-U

R5507 0R3J-0-U-GP DY

C5516 SCD1U16V3KX-GP, C5517 SC4D7U6D3V3KX-GP

Starload height limite change to 0603 package
2015/09/30 modify

DVT2 03/24

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD&CAM&DMC&Touch

Size: A2 | Document Number: Starload SKL-U | Rev: A00

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT

Size	Document Number	Rev
A2	Starload SKL-U	A00

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Main Func = HDMI

260mA

Exchange 0603 0ohm , 20141118

change to 180 for HDMI signal quality 2016/01/05

Change symbol part number, because origin symbol is DELL OBS part

20150116 2037

75.00056.07D

X01 0227

For DIODE in case of leakage from HDMI1

69.48001.081

2nd = 69.50011.081

Vendor suggest, Dummy for floating 20141117

071.08407.0003

HDMI CONN

22.10296.961

X01 0214

4th = 84.2N702.W31

3rd = 84.07002.I31

2ND = 84.2N702.031

84.2N702.J31

Remove DUMMY-HDMI , 20141118

Remove DUMMY-HDMI , 20141118

Remove DUMMY-HDMI , 20141118

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI

Size: A3 | Document Number: Starload SKL-U | Rev: A00

Date: Thursday, February 25, 2016 | Sheet 57 of 106

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title
(Reserved)

Size	Document Number	Rev
A3	*Starload SKL-U*	*A00*

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<Core Design>

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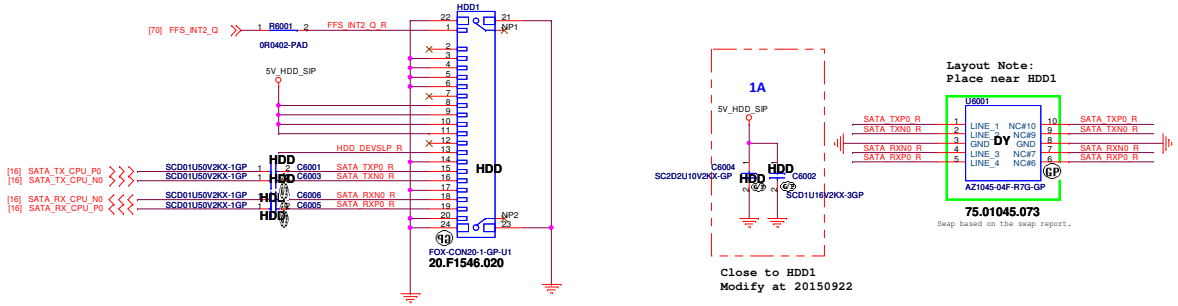
Title
(Reserved)

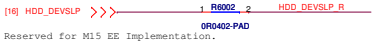
Size	Document Number	Rev
A3	*Starload SKL-U*	*A00*

Date: Thursday, February 18, 2016 Sheet 59 of 106

Main Func = HDD

SATA HDD Connector

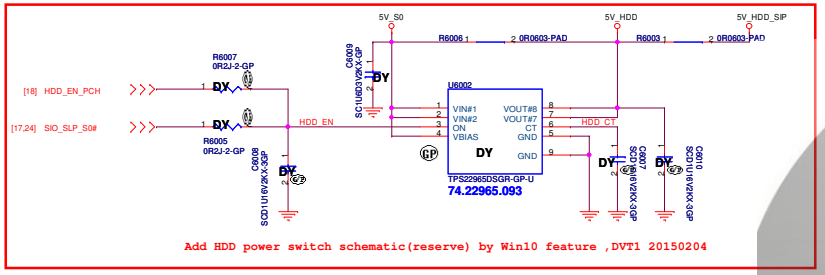




Reserved for M15 EE Implementation.

Close to HDD1
Modify at 20150922

Layout Note:
Place near HDD1



Add HDD power switch schematic(reserve) by Win10 feature ,DVT1 20150204

Main Func = ODD

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SATA IF HDD/ODD

Size: A2 | Document Number: Starload SKL-U | Rev: A00

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Main Func = WLAN

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NGFF WLAN CONN

Size: A3 | Document Number: Starload SKL-U | Rev: A00

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<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	***Starload SKL-U***	***A00***

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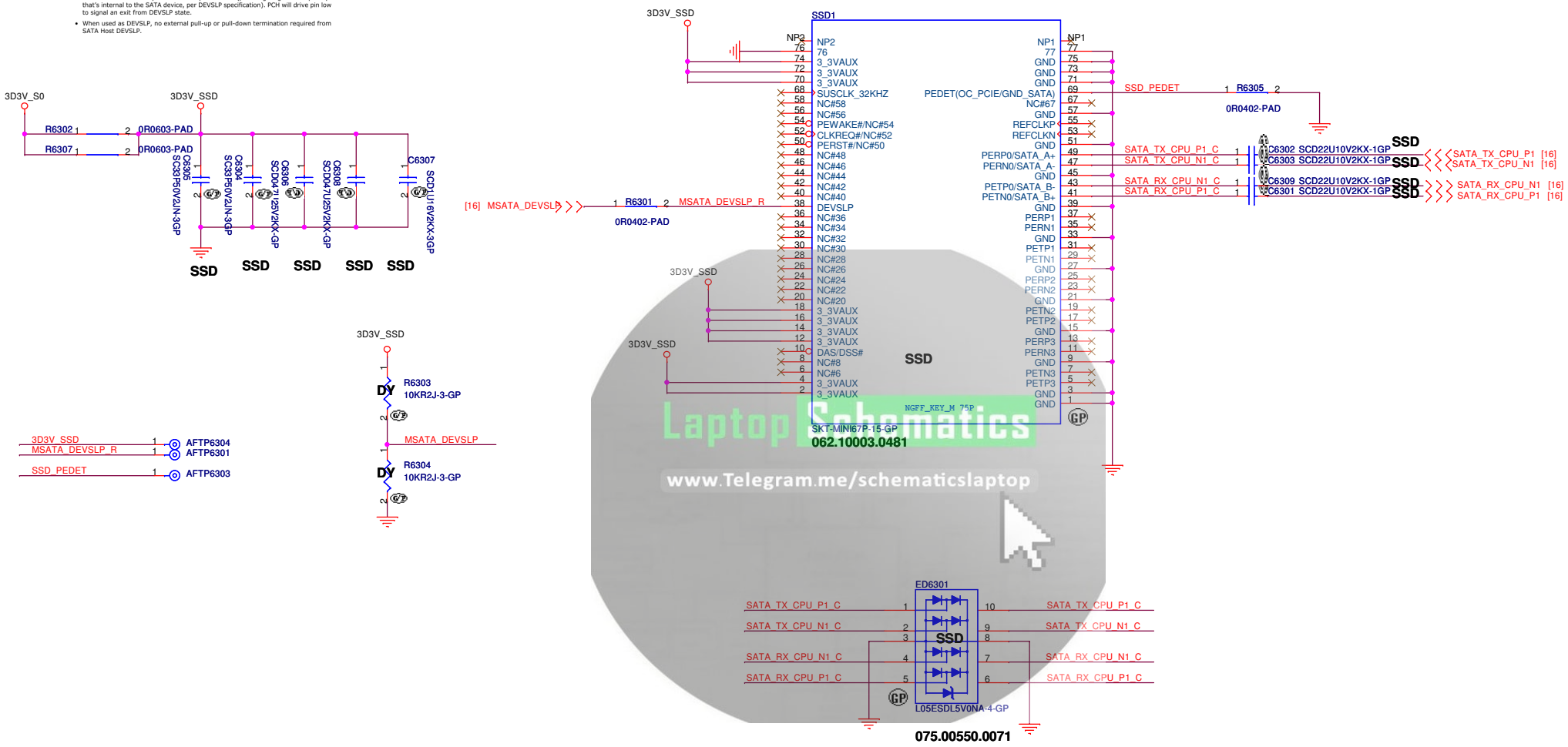
SSD M.2

Important! SATA Host DEVSLP signals shall not be terminated since device shall terminate the signal.

- This is an open-drain pin on the PCH side. PCH will tri-state this pin to signal to the SATA device that it may enter a lower power state (pin will go high due to pull-up that's internal to the SATA device, per DEVSLP specification). PCH will drive pin low to signal an exit from DEVSLP state.
- When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.

SSD M.2 CONN



<Core Design>

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Title: *(Reserved)*

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A3	*Starload SKL-U*	*A00*

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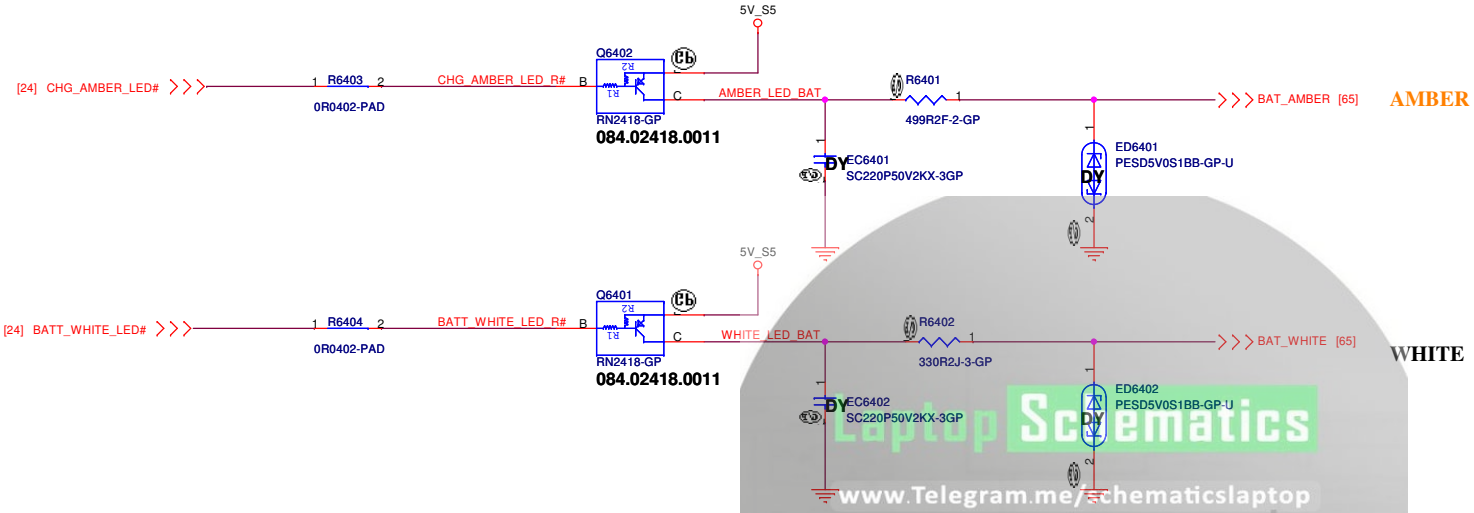
Main Func = Power BTN

Battery LED1 (AMBER_LED)

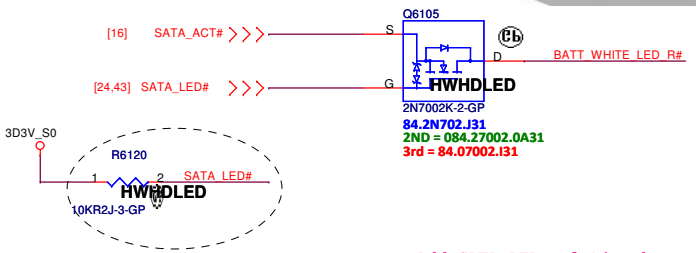
Low actived from KBC GPIO



Battery LED2 (WHITE_LED)

Low actived from KBC GPIO

SATA LED



Add SATA LED solution by customer request 2016/02/03

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Board&Power Button

Size: A3 | Document Number: Starload SKL-U | Rev: A00

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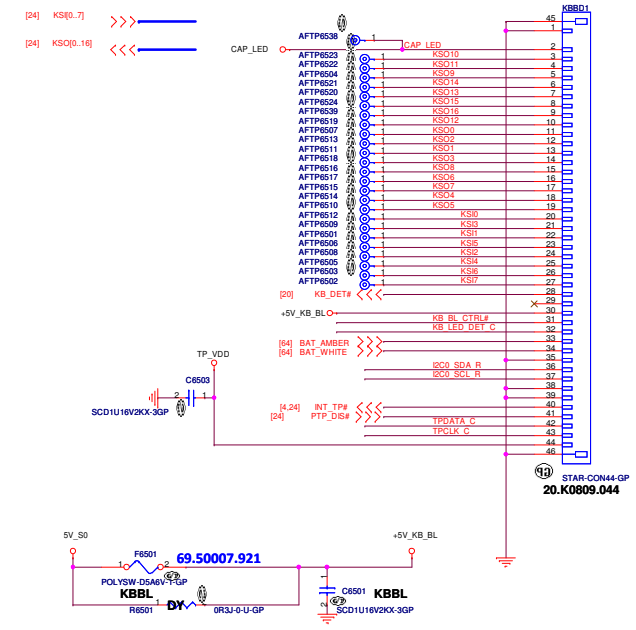
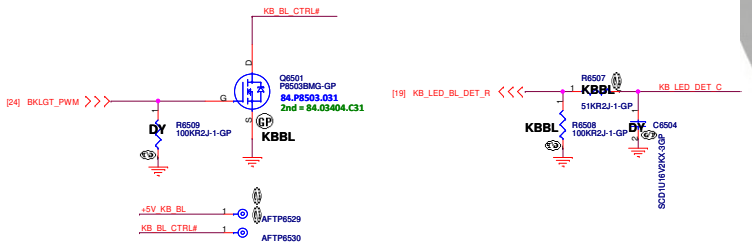
Main Func = KB

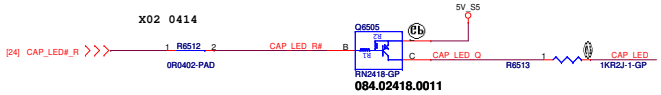
Keyboard



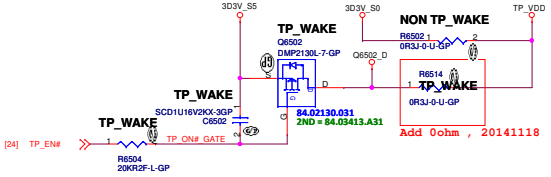
KB Backlight Power Consumption: 285mA max.



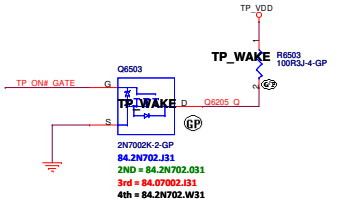
CAP LED Control
LOW actived from KBC GPIO



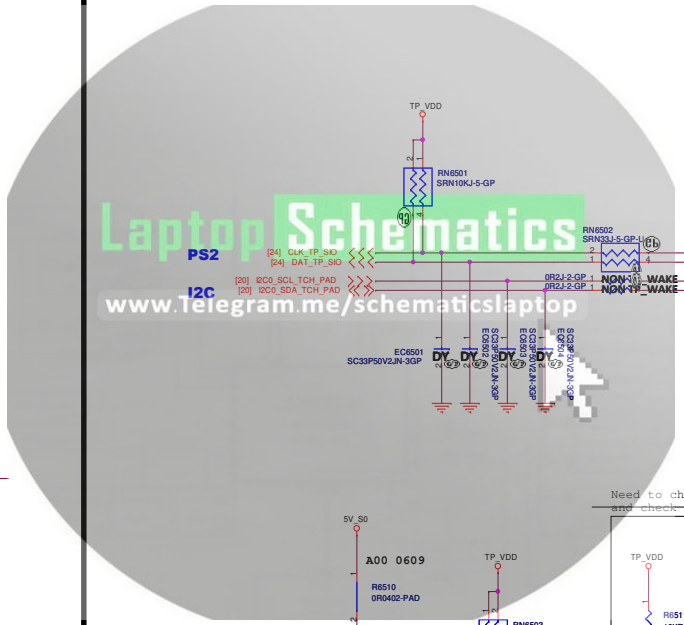
Main Func = TPAD



TP_VDD Discharge Circuit

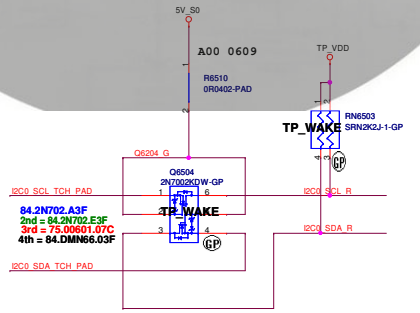


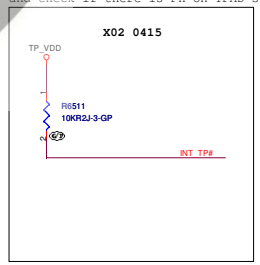
GPIO_TPAD: TBD
(Touch pad wake# for S3 wake up @ PCH GPIO??)



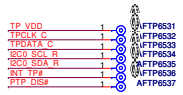
Change pindefine DVT1 0210 1330

Need to check if it is Active High or Active Low and check if there is PH on TPAD side.





Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: Key Board&Touch Pad
Size: A2 | Document Number: Starload SKL-U | Rev: A00
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Main Func = IO Connector

IOBD1

Cutomer remove IO board USB3.0

PCIE_RX_CPU_P5 [16]
PCIE_RX_CPU_N5 [16]
PCIE_TX_WLAN_N5 [16]
PCIE_TX_WLAN_P5 [16]
WLAN
PEG_CLK1_CPU# [18]
PEG_CLK1_CPU [18]
USB_CPU_PN5_C
USB_CPU_PP5_C
USB_CPU_PN2_C
USB_CPU_PP2_C
USB3.0 port3
USB_CPU_PN7_C
USB_CPU_PP7_C
Card Reader
5V_S5
+RTC_VCC
3D3V_S0
VOL_UP# [24]
VOL_DOWN# [24]
PLT_RST# [17,24,68]
CLKREQ_PCIE#1 [18]
KBC_PWRBTN# [24]
WIFI_RF_EN [15]
BLUETOOTH_EN [20]
USB_OC1# [16]
USB_EN# [24,35]

IPEX-CON50-1-GP
020.F0574.0050

Change choke Height just for Starload
2015/09/23 modify

COIL-90OHM-100MHZ-5-GP
USB_CPU_PP2_C → USB_CPU_PP2 [16]
USB_CPU_PN2_C → USB_CPU_PN2 [16]
TR6601

68.00396.001
2nd: = 68.01012.20B

COIL-90OHM-100MHZ-5-GP
USB_CPU_PP7_C → USB_CPU_PP7 [16]
USB_CPU_PN7_C → USB_CPU_PN7 [16]
TR6602

R6605 0R0603-PAD
USB_CPU_PN5_C → USB_CPU_PN5 [16]
R6606 0R0603-PAD
USB_CPU_PP5_C → USB_CPU_PP5 [16]

EMI Reserve , 20141118

KBC_PWRBTN# — DY — EC6601 SC33P50V2JN-3GP
PLT_RST# — DY — EC6602 SC33P50V2JN-3GP
WIFI_RF_EN — DY — EC6603 SC33P50V2JN-3GP

GPU1

[18] CLKREQ_PEG#0
[16] dGPU_RXP_C_CPU_TXP0
[16] dGPU_RXN_C_CPU_TXN0
[16] dGPU_RXP_C_CPU_TXP1
[16] dGPU_RXN_C_CPU_TXN1
[20] GC6_FB_EN
[24] OVER_CURRENT_P8#
[20] DGPU_PWR_EN
[16] CPU_RXP_C_dGPU_TXP0
[16] CPU_RXN_C_dGPU_TXN0
[16] CPU_RXP_C_dGPU_TXP1
[16] CPU_RXN_C_dGPU_TXN1
[18,24,26] SML1_SMBCLK
[18,24,26] SML1_SMBDATA

dGPU_RXP_C_CPU_TXP2 [16]
dGPU_RXN_C_CPU_TXN2 [16]
dGPU_RXP_C_CPU_TXP3 [16]
dGPU_RXN_C_CPU_TXN3 [16]
CLK_PCIE_VGA [18]
CLK_PCIE_VGA# [18]
PLT_RST# [17,24,68]
DGPU_PWROK [24]
DGPU_HOLD_RST# [20]
3D3V_AUX_S5
CPU_RXP_C_dGPU_TXP2 [16]
CPU_RXN_C_dGPU_TXN2 [16]
CPU_RXP_C_dGPU_TXP3 [16]
CPU_RXN_C_dGPU_TXN3 [16]
GPU_EVENT# [20]

OPS
UNI-CONN48-6R-GP-U1
020.F0581.0048

GPU2

DCBATOUT
3D3V_S0
5V_S0

OPS
UNI-CONN28-6R-GP-U
020.F0588.0028

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector
Size: A3
Document Number: Starload SKL-U
Rev: A00
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Starload SKL-U*	*A00*

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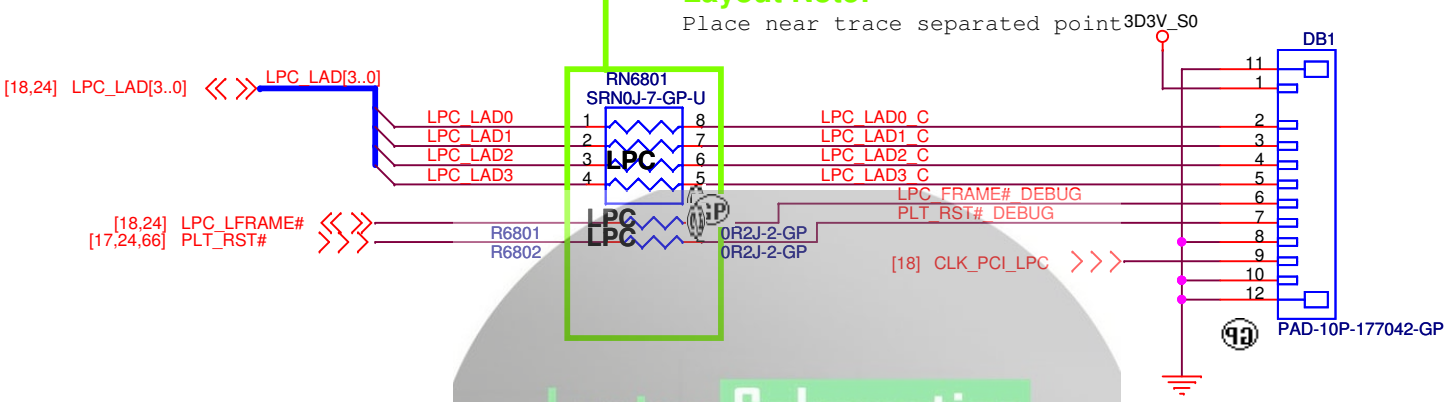
Main Func = Debug

Debug Connector

Layout Note:
Place near trace separated point



20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41
DB1 Optional: New one smaller LPC connector is 20.F1180.010.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Dubug connector

Size	Document Number	Rev
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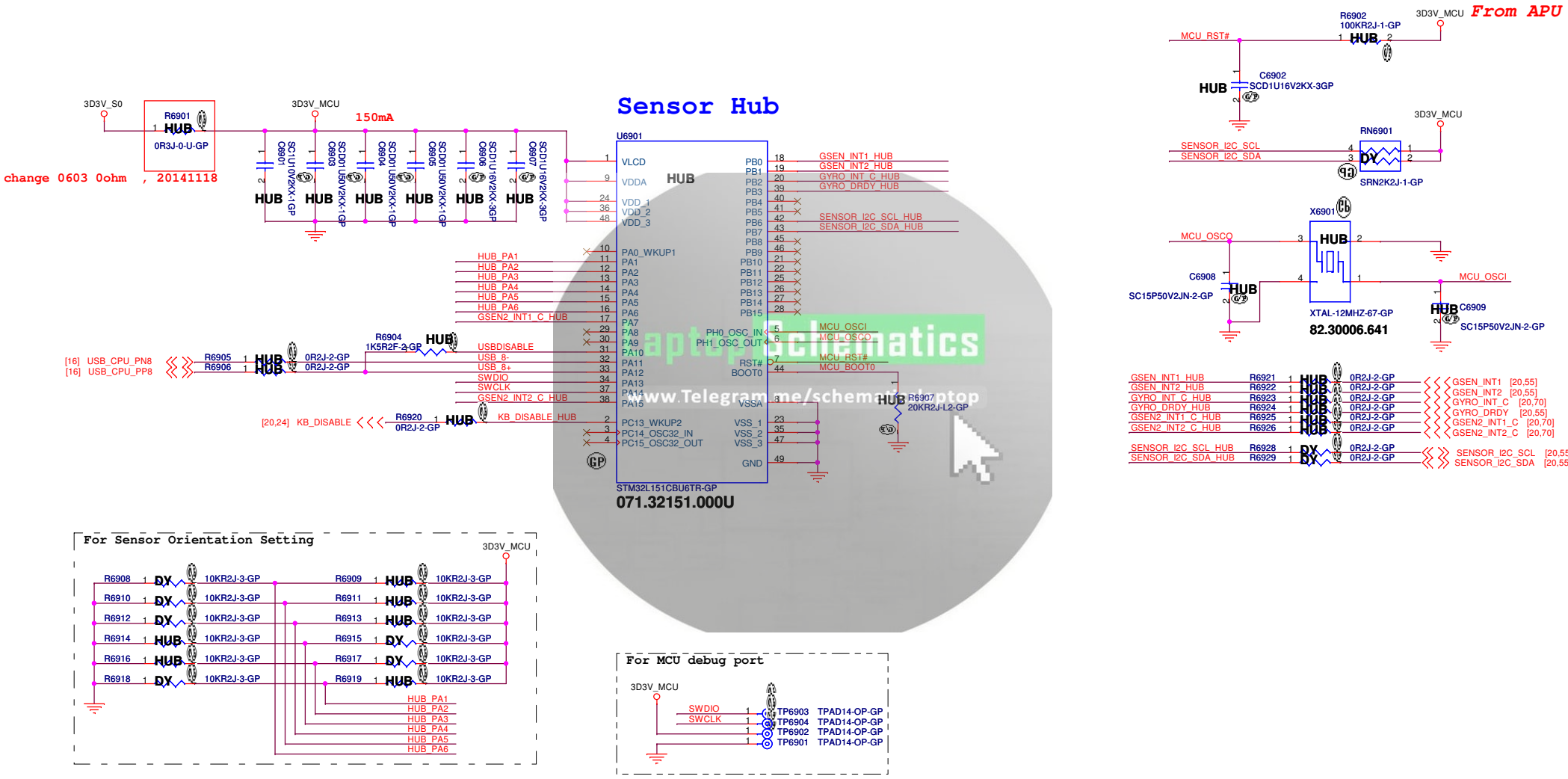
Sensor Hub



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size	Document Number	Rev
A3	Starload SKL-U	A00

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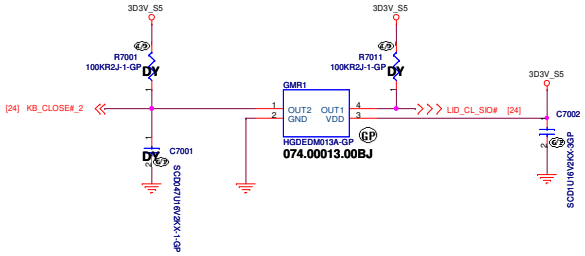
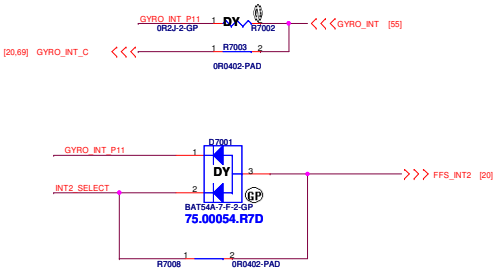
Main Func = Hall Sensor

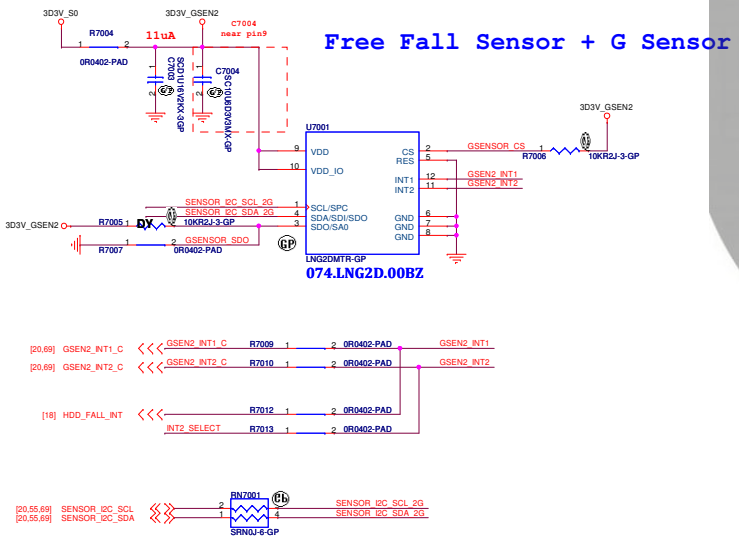
LID sensoe



combine G



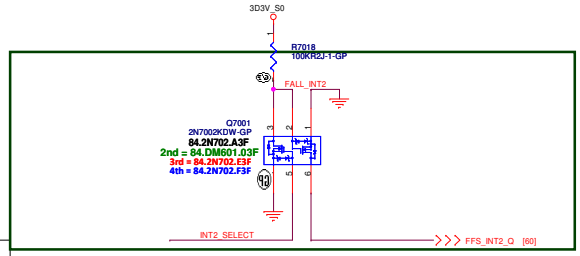
Free Fall Sensor + G Sensor



Note:
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

Note:
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Please help to close with U6602



<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
(Reserved)
Size A2
Document Number
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RESERVED

Size: A3 | Document Number: Starload SKL-U | Rev: A00

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

USB3.0 PORT

Size	Document Number	Rev
A3	Starload SKL-U	A00

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Starload SKL-U | Rev: A00

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(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: Reserved

Size: A3 | Document Number: Starload SKL-U | Rev: A00

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(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Starload SKL-U | Rev: A00

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Main Func = dGPU

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU(1/5)PEG

Size	Document Number	Rev
A2	Starload SKL-U	A00

Date: Thursday, February 18, 2016 Sheet 76 of 106

Main Func = dGPU

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU(2/5)DIGITALOUT

Size: A2 | Document Number: Starload SKL-U | Rev: A00

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Main Func = dGPU

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU(3/5)VRAM/F

Size	Document Number	Rev
A3	Starload SKL-U	A00

Date: Thursday, February 18, 2016 Sheet 79 of 156

Main Func = dGPU

<Core Design>

Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU(4/5)GPIO/STRAP

Size	Document Number	Rev
Custom	Starload SKL-U	A00

Date: Thursday, February 16, 2016 Sheet 79 of 105

Main Func = dGPU

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU(5/5)PWR/GND

Size: Custom | Document Number: Starload SKL-U | Rev: A00

Date: Thursday, February 18, 2016 | Sheet 80 of 106

Main Func = dGPU

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM1,2 (1/4)

Size	Document Number	Rev
A3	Starload SKL-U	A00

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Main Func = dGPU

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM3,4 (2/4)

Size: A3 | Document Number: Starload SKL-U | Rev: A00

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Main Func = dGPU

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU-VRAM5,6 (3/4)*

Size	Document Number	Rev
A3	Starload SKL-U	A00

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Main Func = dGPU

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM7,8 (4/4)

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Main Func = dGFX_CORE

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU CORE

Size	Document Number	Rev
A2	Starload SKL-U	A00

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Main Func = dGPU

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU Discrete Power

Size: A2 | Document Number: Starload SKL-U | Rev: A00

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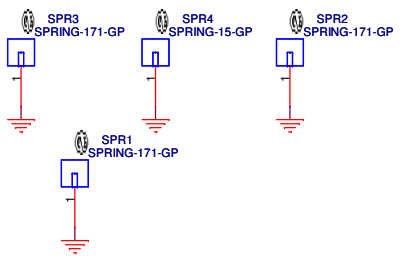
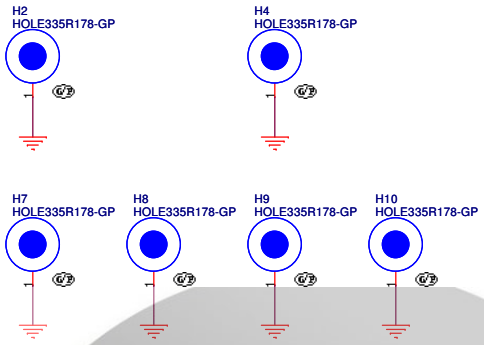
Main Func = UnusedParts

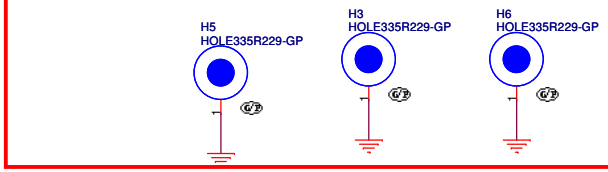
34.4YW18.001

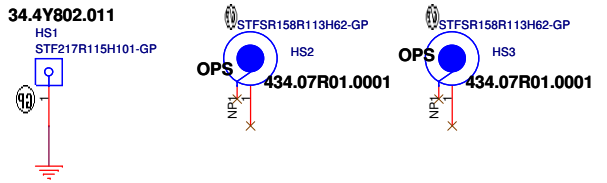


ZZ.00PAD.7F1



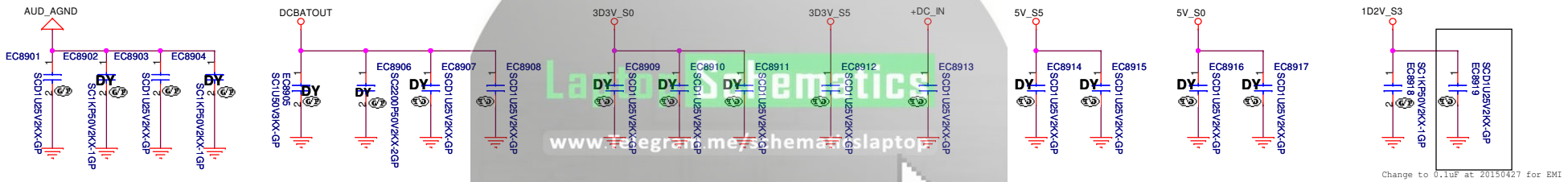
ZZ.00PAD.7G1



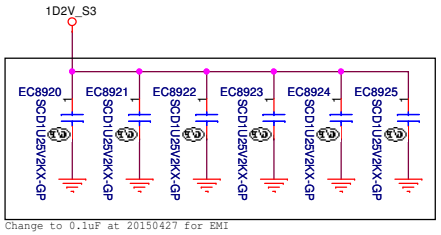


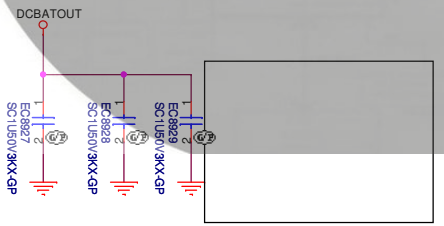
SSID = EMI

Mind the voltage rating of the caps.

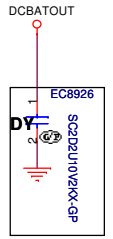


SSID = RF

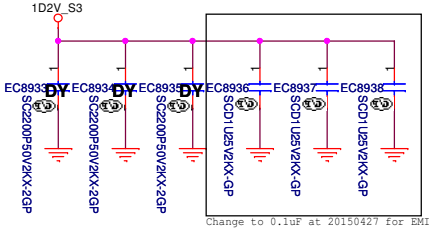




Remove EC8931,EC8932,EC8926,EC8930for placement



RF request 2016/01/12 modify



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SSID = TPM

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Title: *CRT_Switch*

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Main Func = Debug

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Title: CPU_XDP;PCH_XDP

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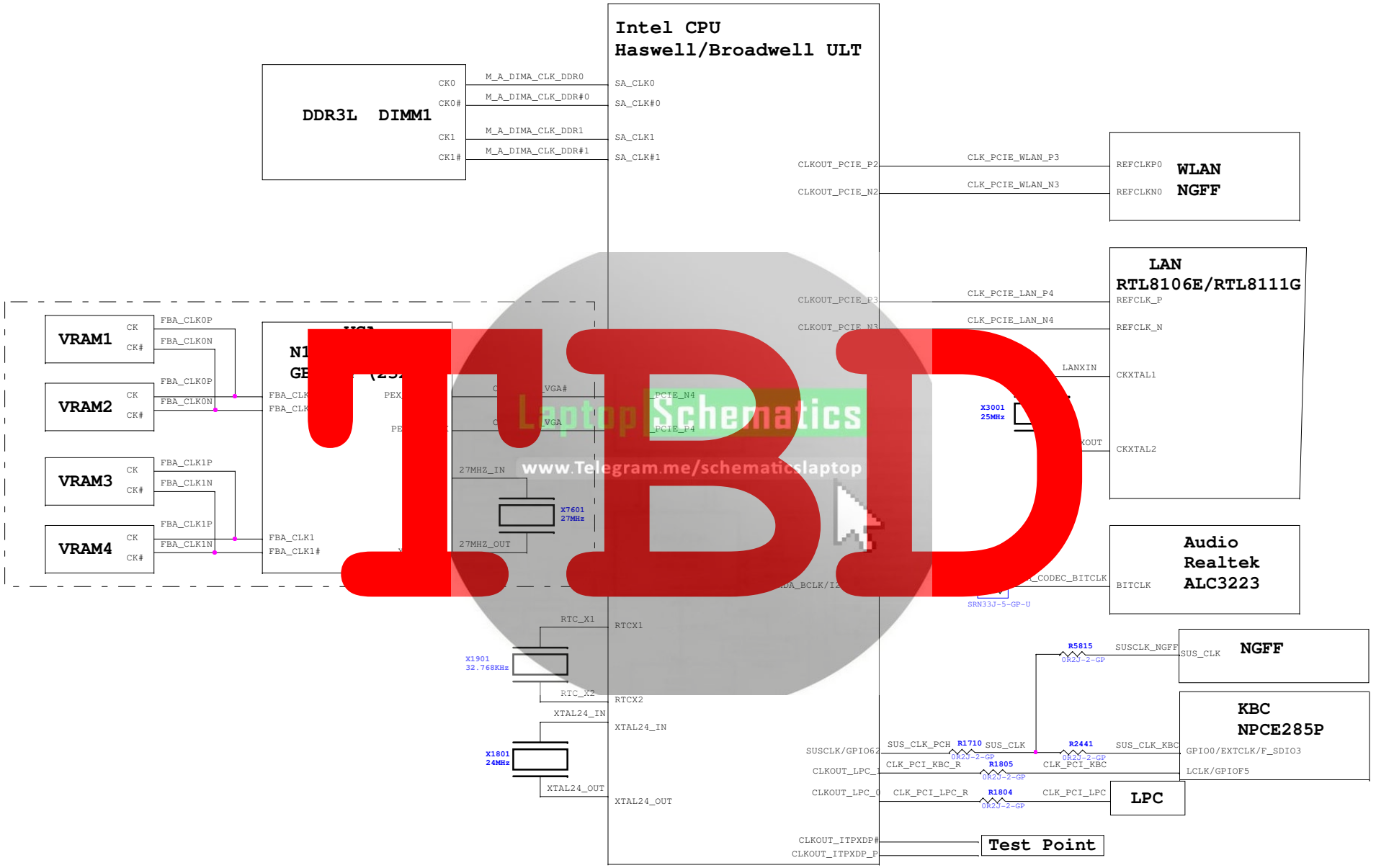
CLK Block Diagram



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Title: CLK Block Diagram

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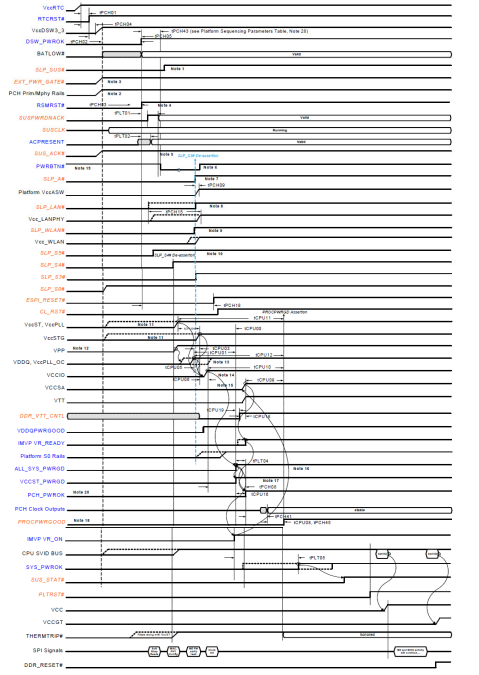
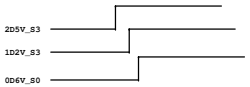
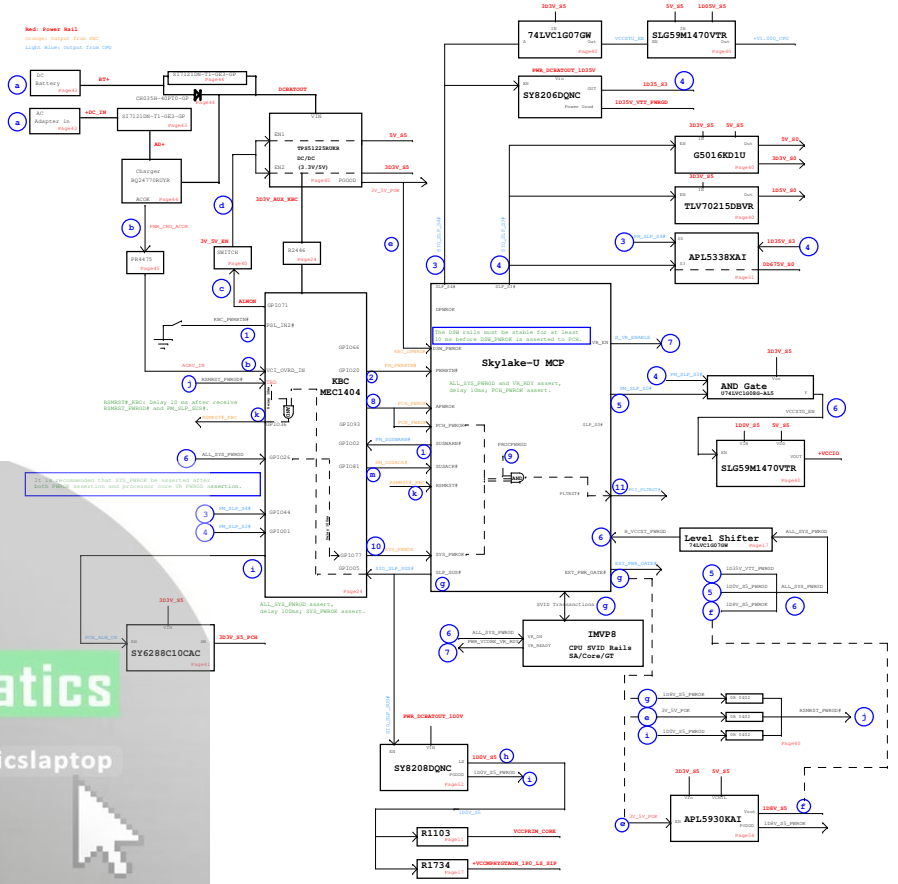
SKL-U/Y Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]



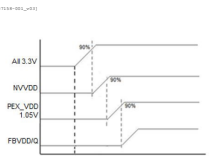
For DDR4 power sequence



Tulip Skylake POWER UP SEQUENCE DIAGRAM (Deep Sx Platform)



[dGPU] N16x Power-Up/Down Sequence



Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

Note:
- The ramp time for any rail must be more than 40 us and is recommended to be less than 2ms.
- The ramp up overshoot should not exceed the silicon reliability limit voltage.
- The previous power rail must ramp up to 90% before the next power rail can start ramping up.
- No signal should be applied to the GPU before the power rails are fully ramped
- Refer to the JEDEC Memory Specification for memory related power sequencing.
- The order of NVVDD and PEX_VDD ramp-up can be reversed during GC6 exit when there is a back-to-back GC6 entry/exit and/or when PEX_VDD takes longer to ramp down during GC6 entry.

3.10.2.2 Power-Down Sequence

There is no specific power down sequence. However, residual voltage from power down must not violate the power-up sequence when back to back GPU power-down and power-up events take place.

18.3.2.3 GC6 2.0 Entry/Exit Timing

The following timing diagram in Figure 18-12 and Table 18-3 describes the GC6 2.0 entry and exit sequence and timing requirements.

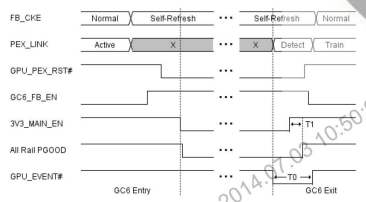


Figure 18-12. GC6 2.0 Entry/Exit Sequence Timing Diagram

Table 18-2. GC6 2.0 Entry/Exit Sequence Timing Parameters

Symbol	Description	Min	Max	Unit
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	3V3_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

Note:
- ALL Rail PGOOD=1 represents all GPU power rails are ramped up and in regulation. If any GPU power rail cannot be guaranteed in regulation this state should equal to 0.
- During GC6 exit, the order of power rail ramp-up must follow the power-up sequence described in Chapter 3 with the exception that FBVDD/Q stays on.
- All delays should be minimized to increase time spent in GC6 for maximum power saving.
- The entire entry/exit sequence must complete within 200 ms.

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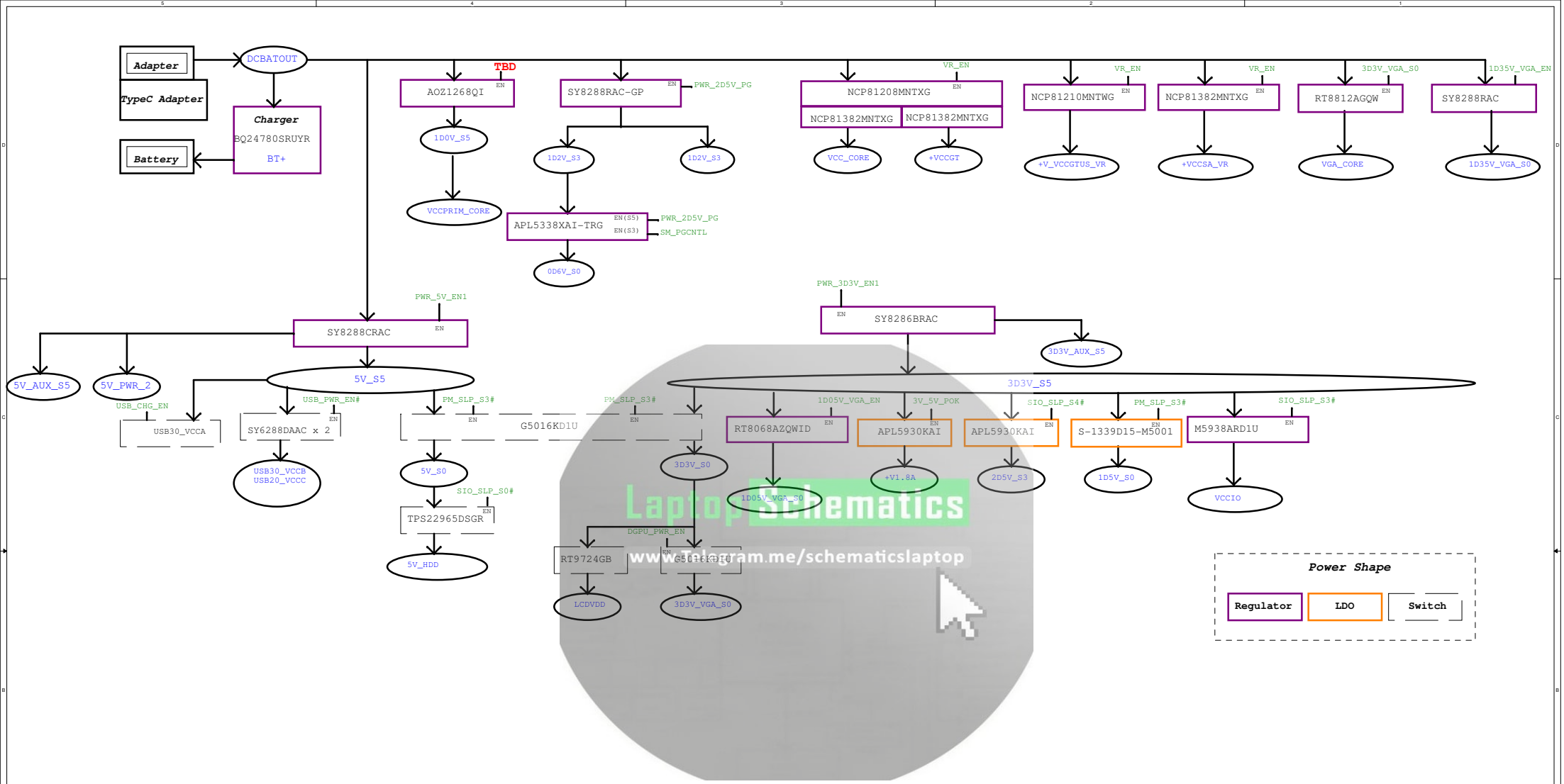
Power Sequence
Starbad SKL-U



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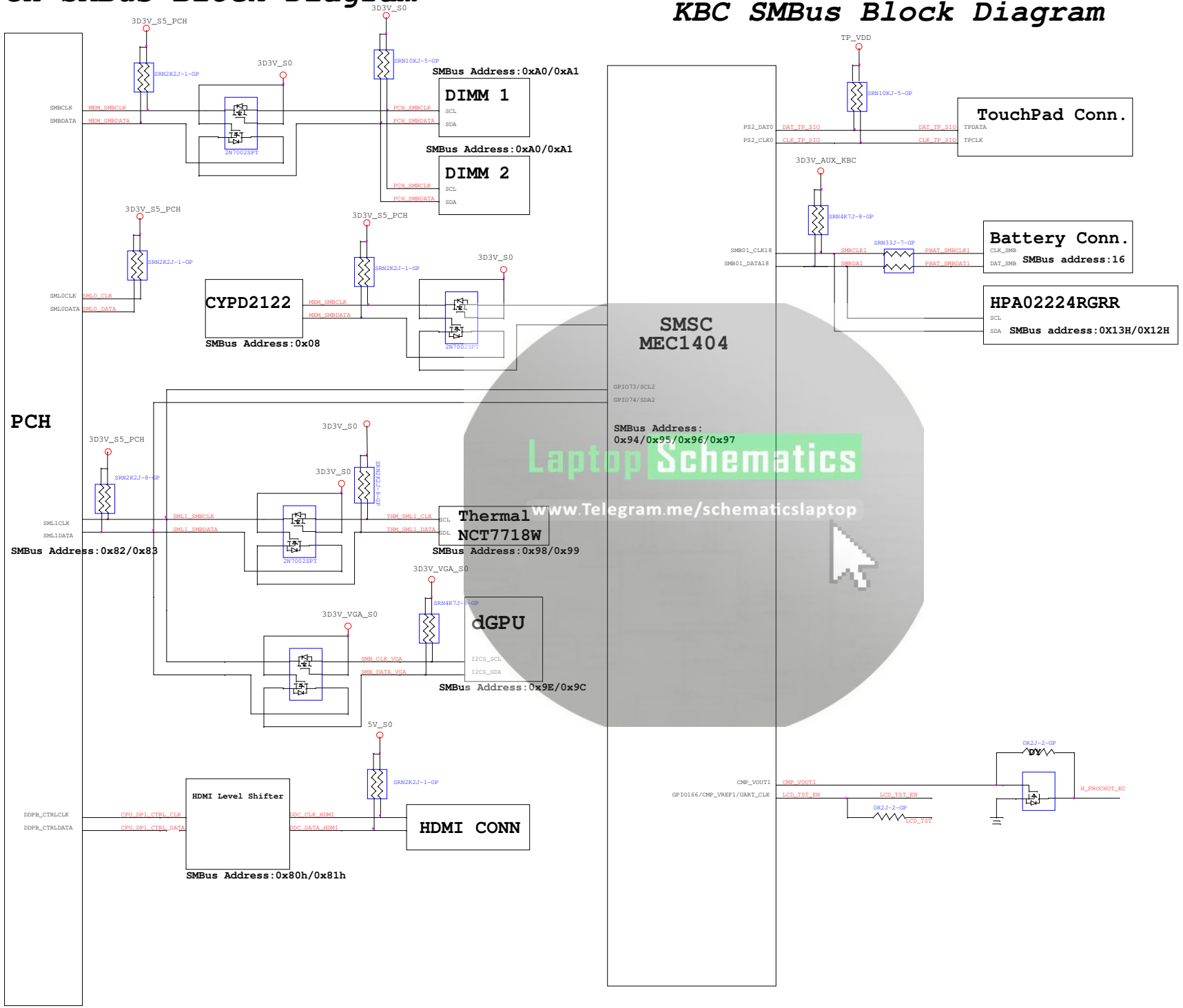
PCH SMBus Block Diagram



KBC SMBus Block Diagram

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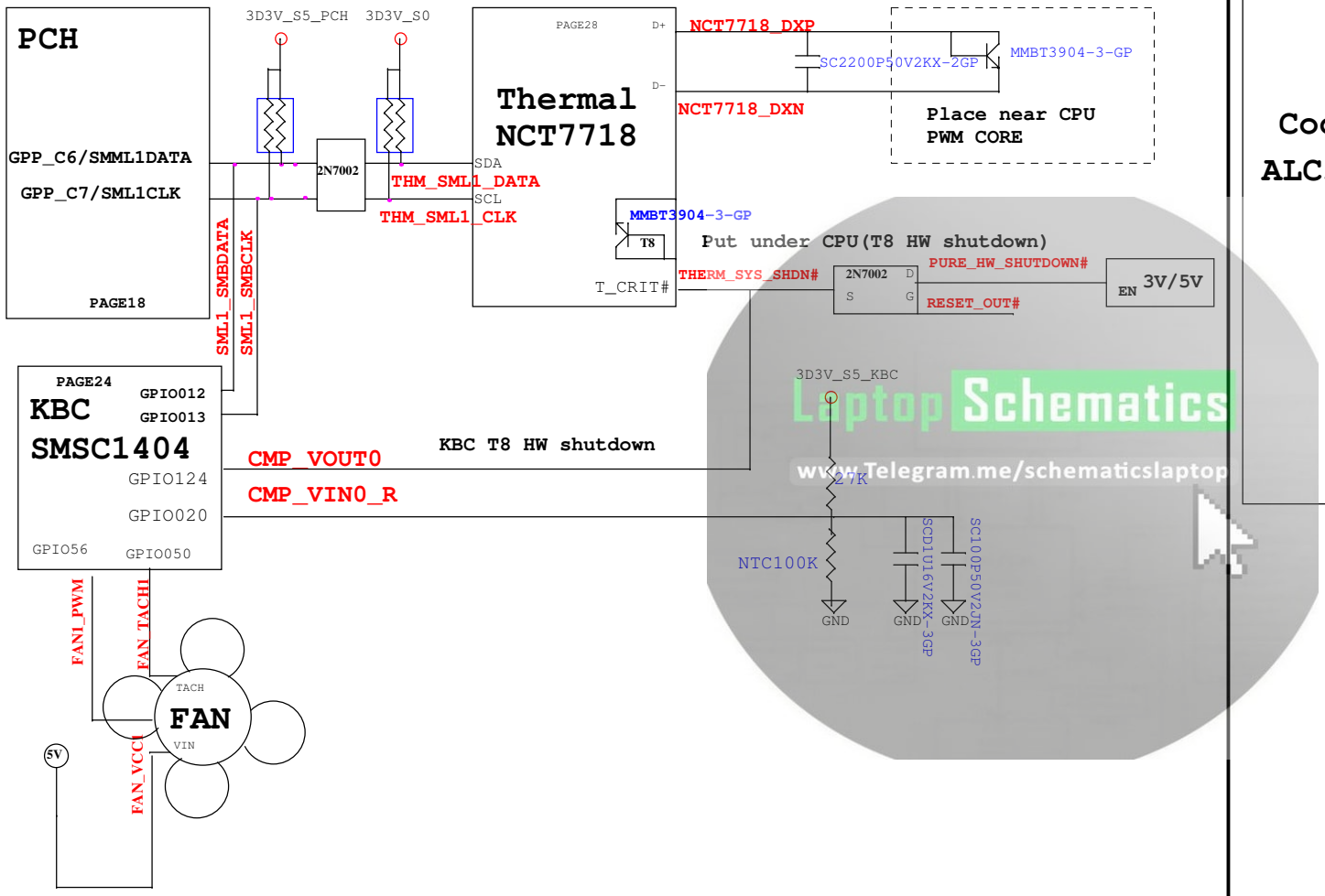
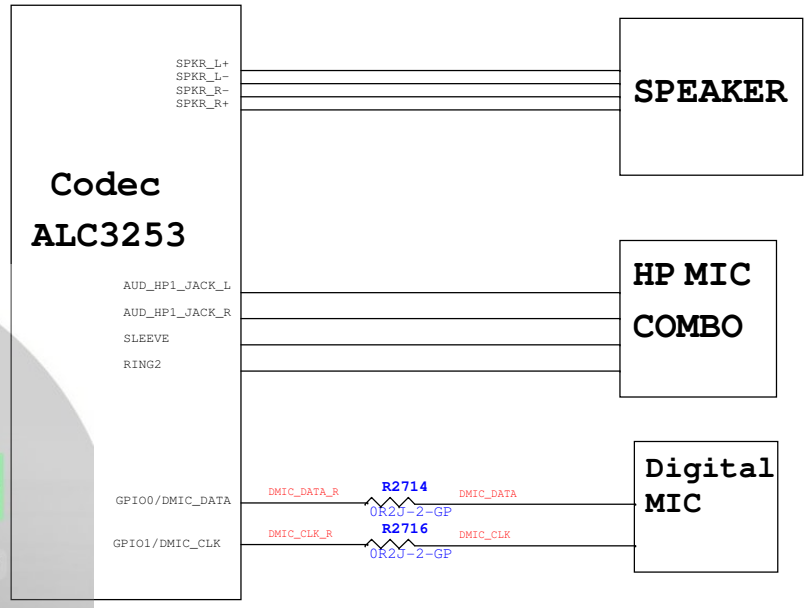
Thermal Block Diagram



Audio Block Diagram



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SIP connector

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