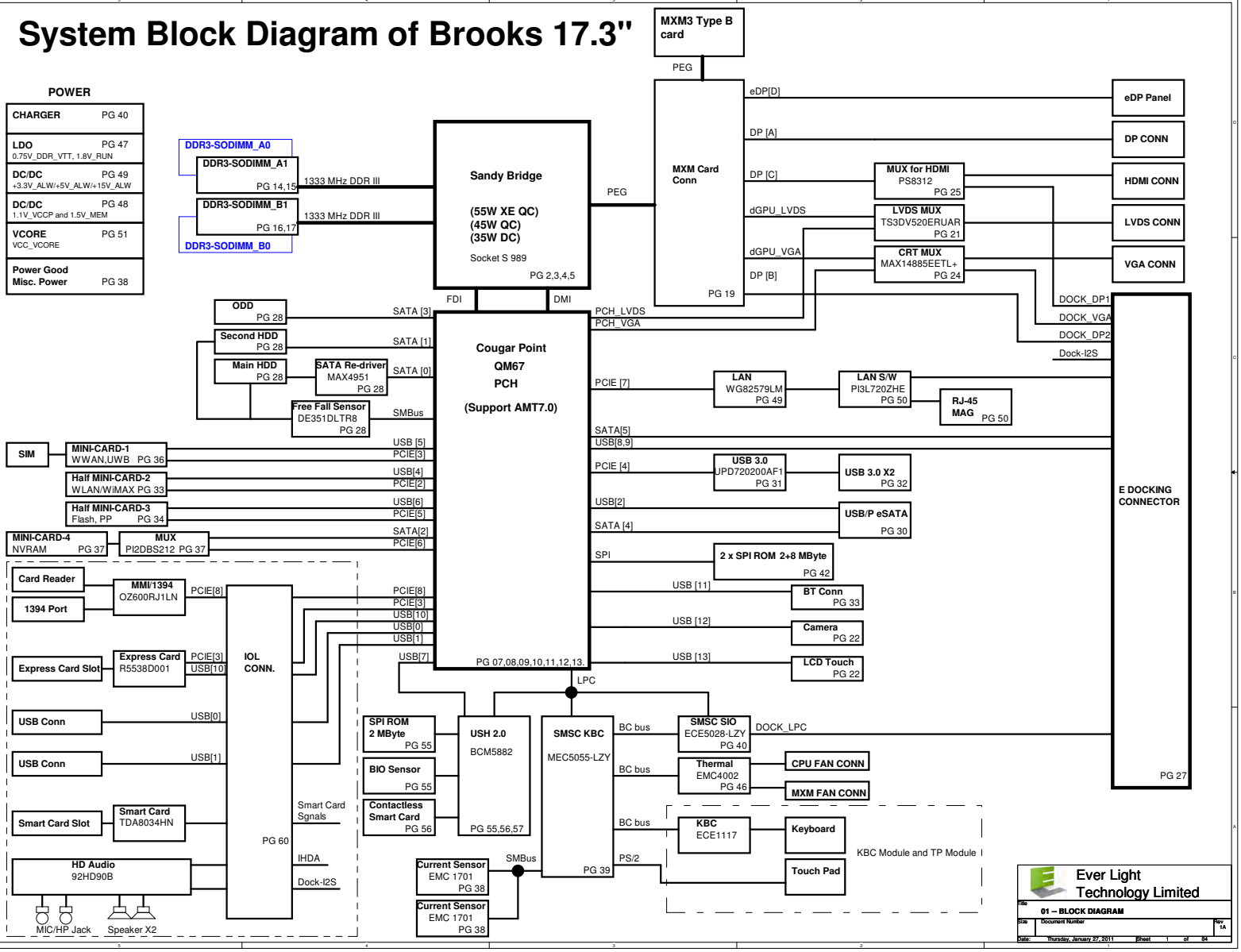
System Block Diagram of Brooks 17.3"



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File: 01 -- BLOCK DIAGRAM

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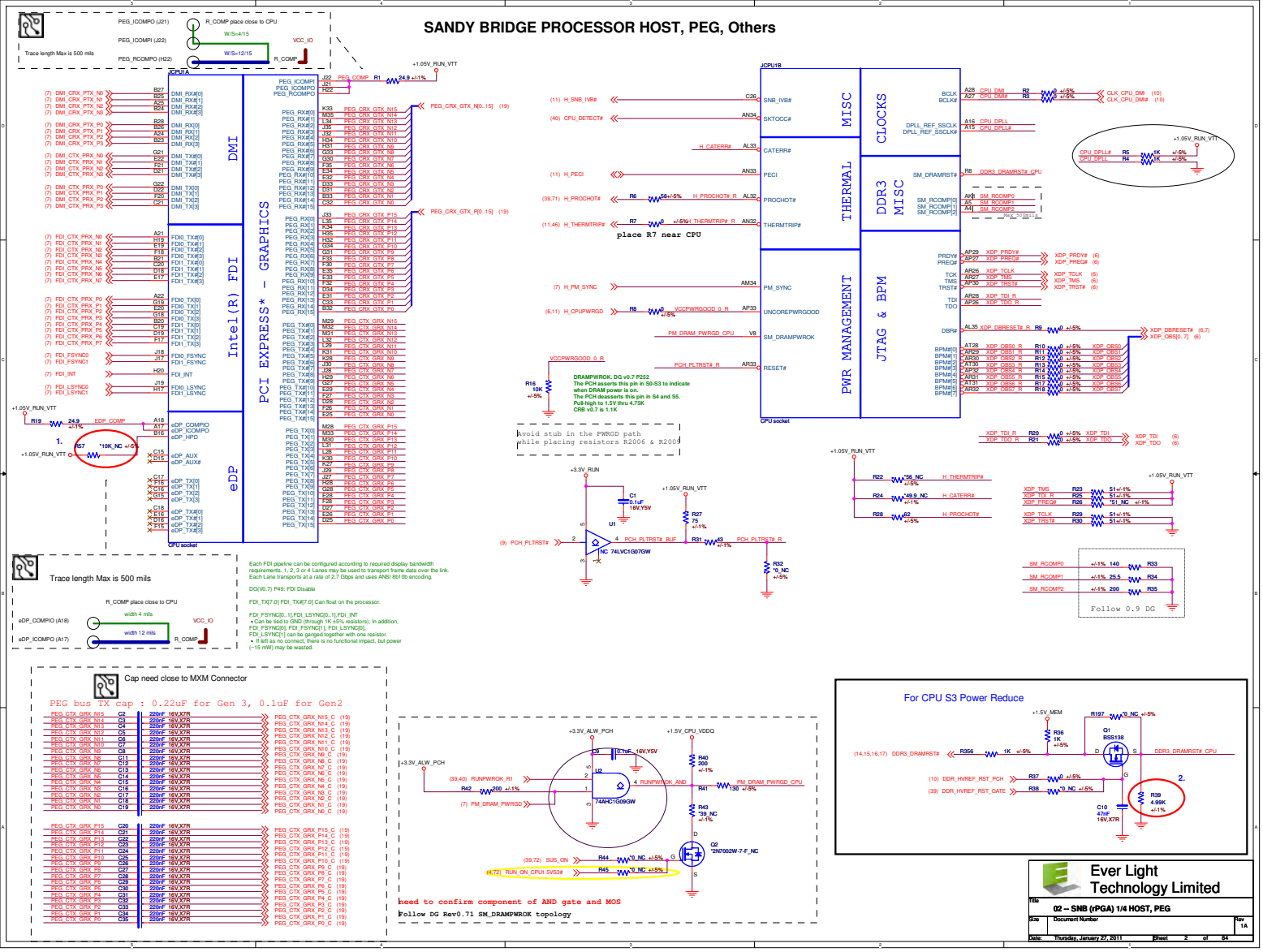
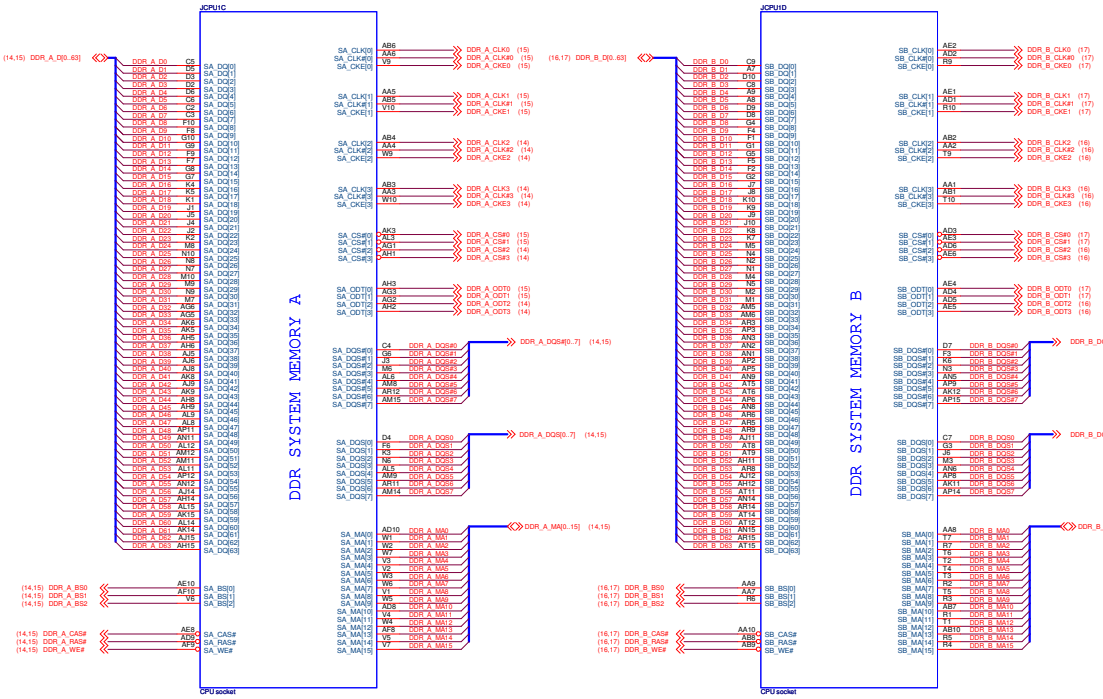
SANDY BRIDGE PROCESSOR HOST, PEG, Others



SANDY BRIDGE PROCESSOR (DDR3)



Ever Light Technology Limited	
Title	03 -- SNB (rPGA) 2/4 DDR
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SANDY BRIDGE PROCESSOR (POWER)

SANDY BRIDGE PROCESSOR (GRAPHICS POWER)

POWER

CPU socket

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

SENSE LINES

VREF

DDR3 -1.5V RAILS

SA RAIL

MISC

1.8V RAIL

GRAPHICS

22uF x 16
470uF x 2 on VR side

+V_SM_VREF should have 10 mil trace width.

10uF x 6
330uF x 1

10uF x 2, NC x 2

For CPU S3 Power Reduce

Power page :
22uF x 3
EE page :
330uF x 1, NC x 1
22uF x 12, NC x 7

Intel DG :
330uF x 2 near CPU
22uF x 5, NC x 5 Bottom Socket Cavity
22uF x 7, NC x 2 Top Socket Cavity
for 2012 capable designs
330 µF x3

CPU Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	0.65~1.3	53
VCCIO	1.05	8.5
VAXG	0.0~1.1	26
VCCPLL	1.8	3
VDDQ	1.5	5
VCCSA	0.65~0.9	6
+1.5V_MEM	1.5	12~16 *

* Description
5A to Mem controller(+1.5V_CPU_VDDQ)
5~6A to 2 DIMMs/channel
2~5A to +1.5V_RUN & +0.75V_DDR_VTT

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Title	04 – SNB (rPGA) 3/4 POWER		
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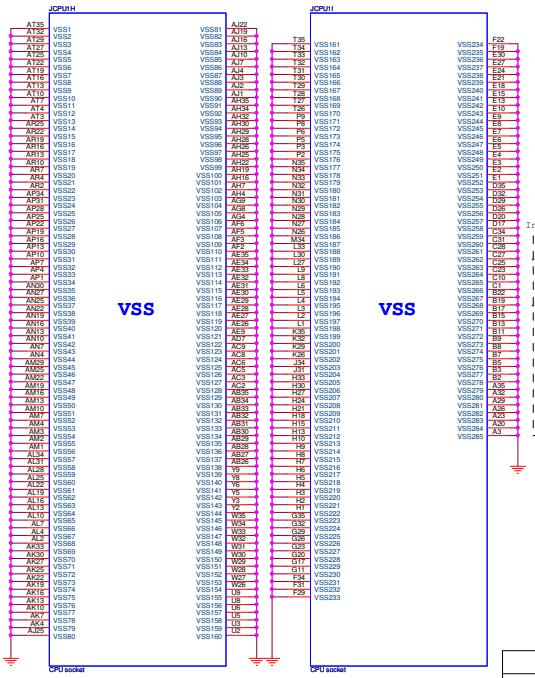
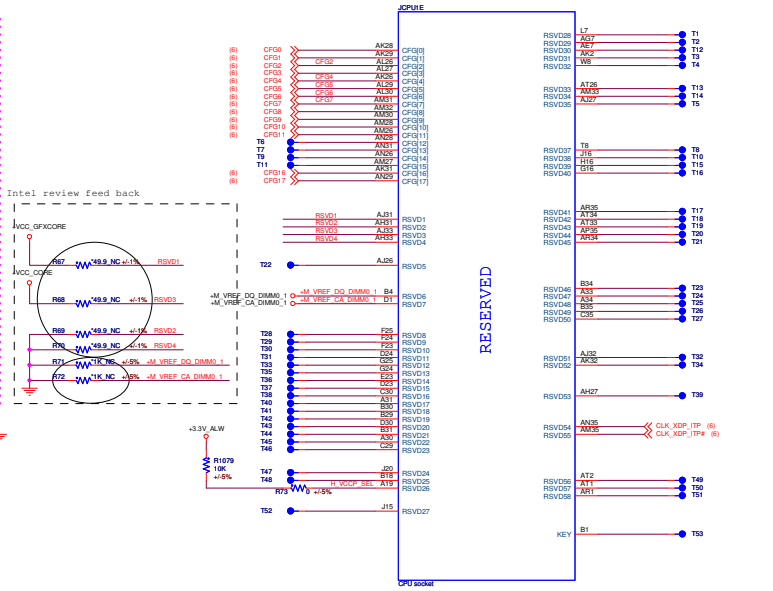
SANDY BRIDGE PROCESSOR (GND)



SANDY BRIDGE PROCESSOR(RESERVED, CFG)



	1	0
CFG2 (PEG Static Lane Reversal)	Lan# definition matches socket pin map definition (Default Value)	Lan Reversed
CFG4 (Display Port Presence strap)	Disabled; No Physical Display Port attached to Embedded Display Port (Default Value)	Enabled; An external Display port device is connected to the Embedded Display port
CFG[6:5]		
CFG7 (PEG Defer Training)	PEG Train immediately following xxRESETB de assertion (Default Value)	PEG Wait for BIOS for training

CFG[6:5] (PCIe Port Bifurcation Straps)	11	x16 - Device 1 functions 1 and 2 disable (Default Value)
	10	x8, x8 - Device 1 function 1 enable; function 2 disable
	01	Reserved - (Device 1 function 1 disable; function 2 enable)
	00	x8, x8, x4 - Device 1 function 1 and 2 enable

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Title	05 -- SNB (rPGA) 4/4(GND)	
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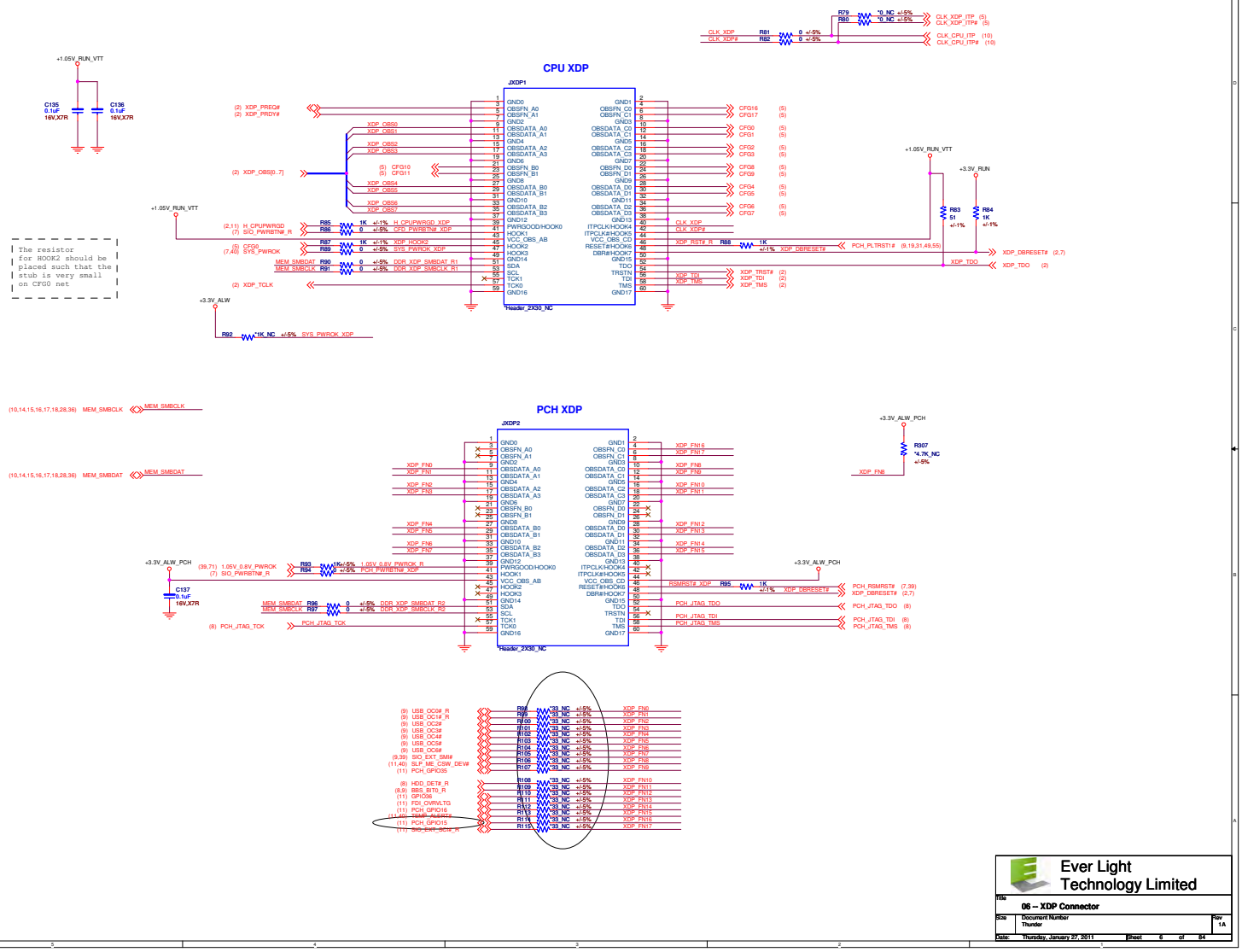

Ever Light Technology Limited	
Title	06 -- XDP Connector
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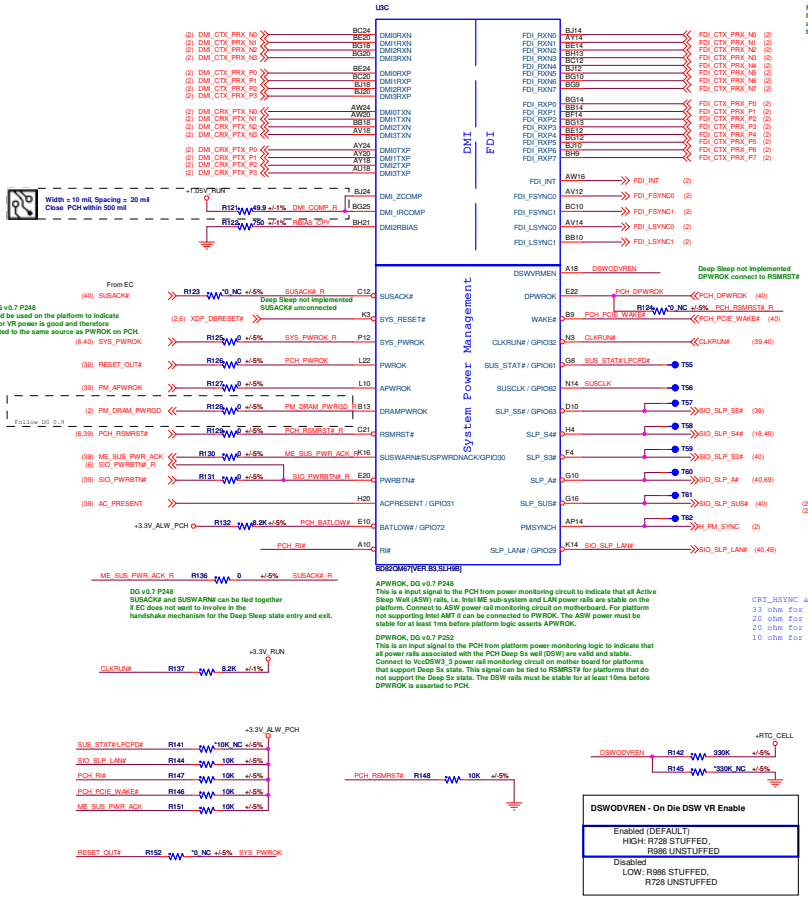
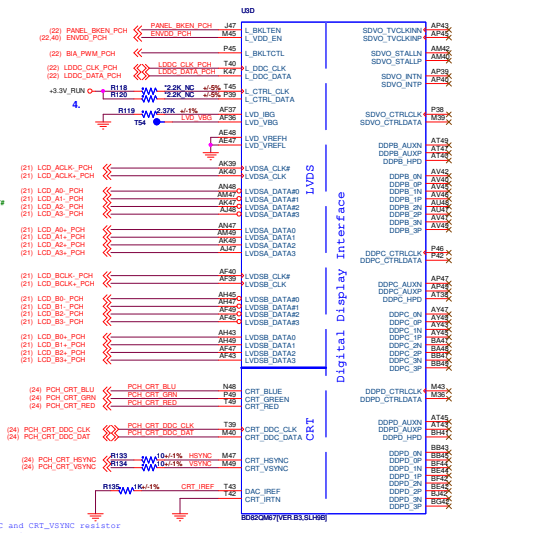
COUGAR POINT (DMI,FDI,GPIO)



COUGAR POINT (LVDS,DDI)



PDG v0.7 P166
If the LVDS interface is not implemented, all signals associated with the interface can be left as No Connects

CRT_HSYNC and CRT_VSYNC resistor
33 ohm for Direct Connect
20 ohm for Dock Support
20 ohm for Switchable Graphics Device Down Topology
10 ohm for Switchable Graphics Dock Support

SYS_PWROK, DG v0.7 P248
This signal should be used on the platform to indicate that the processor VR power is good and therefore it can be connected to the same source as PWROK on PCH.

Deep Sleep not implemented
DPWROK connect to RSMRST#

APWROK, DG v0.7 P248
This is a input signal to the PCH from power monitoring circuit to indicate that all Active Sleep Well (ASW) rails, i.e. Intel ME sub-system and LAN power rails are stable on the platform. Connect to ASW power rail monitoring circuit on motherboard. For platform not supporting Intel AMT it can be connected to PWROK. The ASW power must be stable for at least 1ms before platform logic asserts APWROK.

DPWROK, DG v0.7 P252
This is an input signal to the PCH from platform power monitoring logic to indicate that all power rails associated with the PCH Deep Sx well (DSW) are valid and stable. Connect to VccDSW3_3 power rail monitoring circuit on mother board for platforms that support Deep Sx state. This signal can be tied to RSMRST# for platforms that do not support the Deep Sx state. The DSW rails must be stable for at least 10ms before DPWROK is asserted to PCH.

DG v0.7 P248
SUSACK# and SUSWARN# can be tied together
If EC does not want to involve in the handshake mechanism for the Deep Sleep state entry and exit.

DSWODVREN - On Die DSW VR Enable

Enabled (DEFAULT)
HIGH: R728 STUFFED,
R986 UNSTUFFED

Disabled
LOW: R986 STUFFED,
R728 UNSTUFFED

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Title	07 -- CBT 1/6 (DMI&VIDEO)
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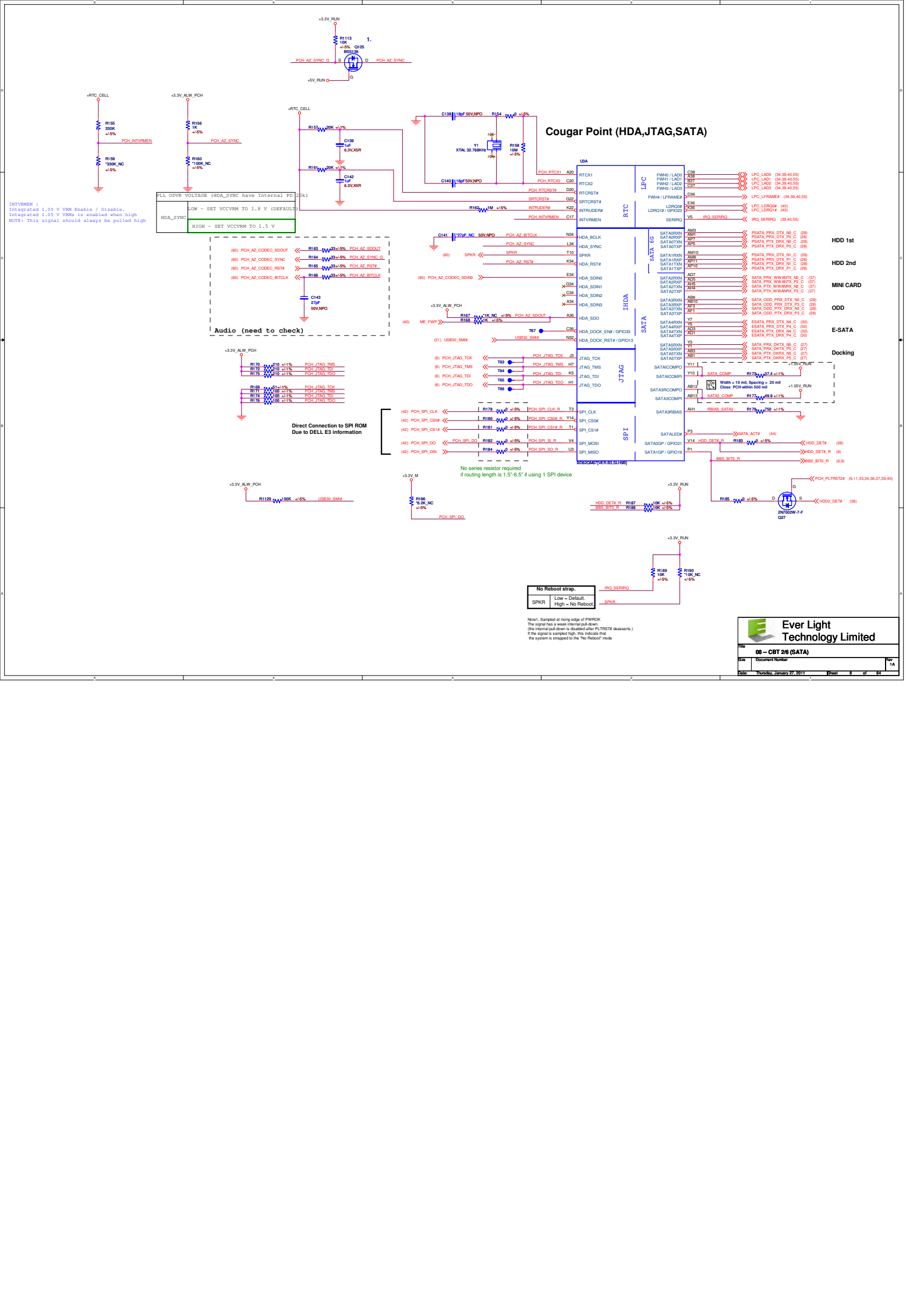
Cougar Point (HDA,JTAG,SATA)
INTVRMEN :
Integrated 1.05 V VRM Enable / Disable.
Integrated 1.05 V VRMs is enabled when high
NOTE: This signal should always be pulled high
PLL ODVR VOLTAGE (HDA_SYNC have Internal PD 20k)
HDA_SYNC
LOW - SET VCCVRM TO 1.8 V (DEFAULT)
HIGH - SET VCCVRM TO 1.5 V
Audio (need to check)
Direct Connection to SPI ROM
Due to DELL E3 information
No series resistor required
if routing length is 1.5"-6.5" if using 1 SPI device
No Reboot strap.
SPKR
Low = Default.
High = No Reboot.
Note1, Sampled at rising edge of PWROK
The signal has a weak internal pull-down.
(the internal pull-down is disabled after PLTRST# deasserts.)
If the signal is sampled high, this indicate that
the system is strapped to the "No Reboot" mode
HDD 1st
HDD 2nd
MINI CARD
ODD
E-SATA
Docking
Ever Light
Technology Limited
08 -- CBT 2/6 (SATA)
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Cougar Point (PCI,USB,NVRAM)

R191 *1K_NC +/-5% BBS_BIT0_R (6,8)
R192 *1K_NC +/-5% BBS_BIT7

Boot BIOS Strap

BBS_BIT[1]	BBS_BIT[0]	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

U2E

RSVD

PCI

USB

GNT2# : Strap for ESI mode
This signal has a weak internal pull-up.
Note : The internal pull-up is disable after PLTRST# deasserts.
Tying this strap low configures DMI for ESI compatible opeartion.
Note : ESI compatible mode is for server platform only.
This signal should not be pulled low for desktop and mobile.

REQ# functionality is not available on Mobile

GNT# functionality is not available on Mobile

PIRQ[H:E]# functionality is not available on Mobile

- Right Side pair top
- Right Side pair bottom
- Back Side
- AUX module (Removed)
- 2nd Mini Card (WLAN/WIMAX)
- 1st Mini Card (WWAN)
- 3rd Mini Card
- USH
- DOCK
- DOCK
- Express Card
- BlueTooth
- Camera
- LCD Touch or Nvidia 3D IR

EMI request

C778 *10pF_NC 50V,NPO
C779 *10pF_NC 50V,NPO
C790 *10pF_NC 50V,NPO
C811 *10pF_NC 50V,NPO

Net USB_BIAS route impedacnes should be 50-ohm and length less than 500-mil spacing is 15-mil.

Add Buffers as needed for Loading and fanout concerns.

PLTRST1# for USH, OZ600, EXP, XDP, LAN, USB3.0, MXM.

PLTRST2# for 5055,5028,WLAN,PP,WWAN,NVRAM.

A16 swap override Strap/Top-Block Swap Override jumper

GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

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Title	09 -- CBT 3/6 (USB, PCI, NVRAM)	
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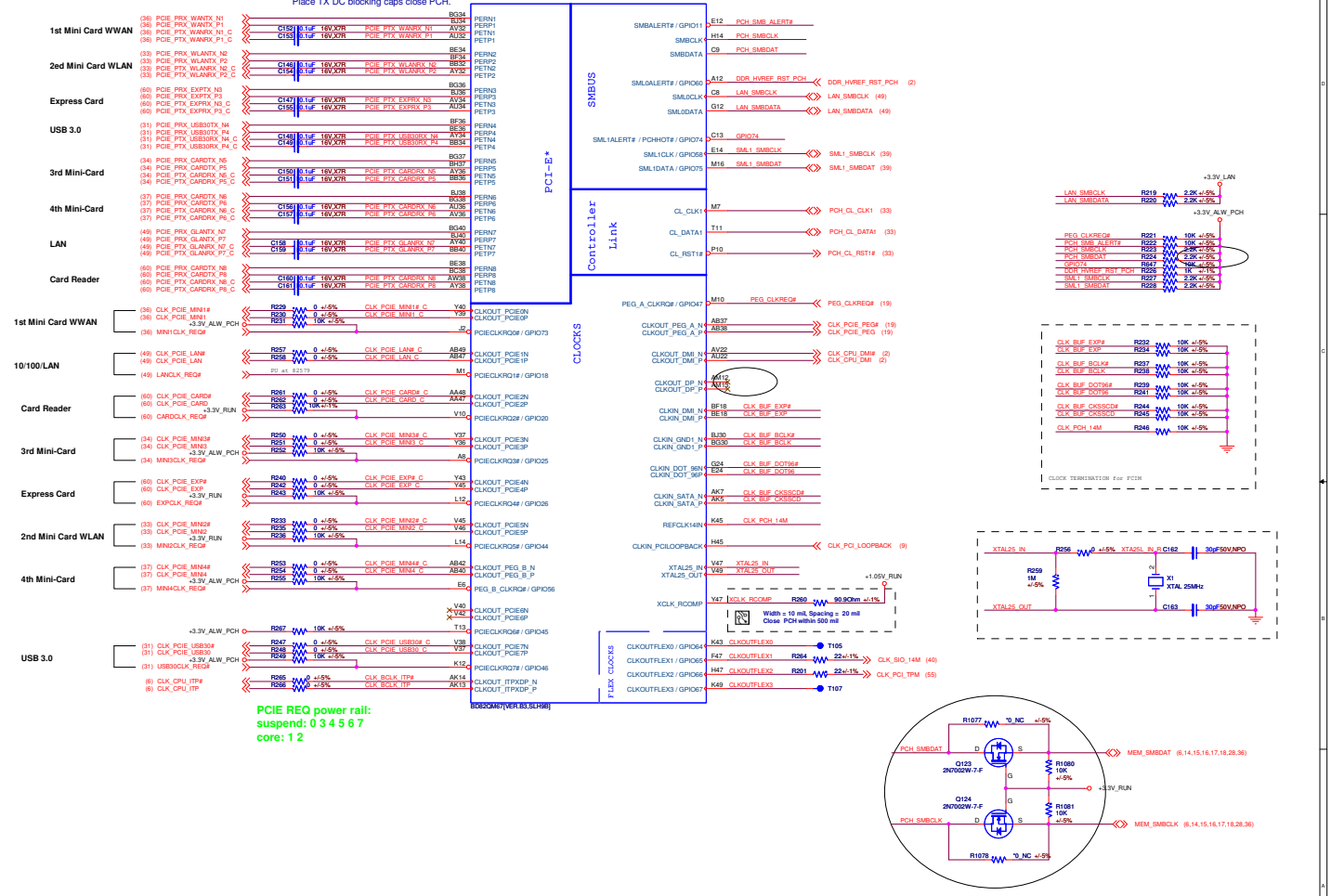
Cougar Point (PCI-E,SMBUS,CLK)

Place TX DC blocking caps close PCH.



PCIE REQ power rail:
suspend: 0 3 4 5 6 7
core: 1 2

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Title	10 – CBT 4/7 (PCIE, CLK)
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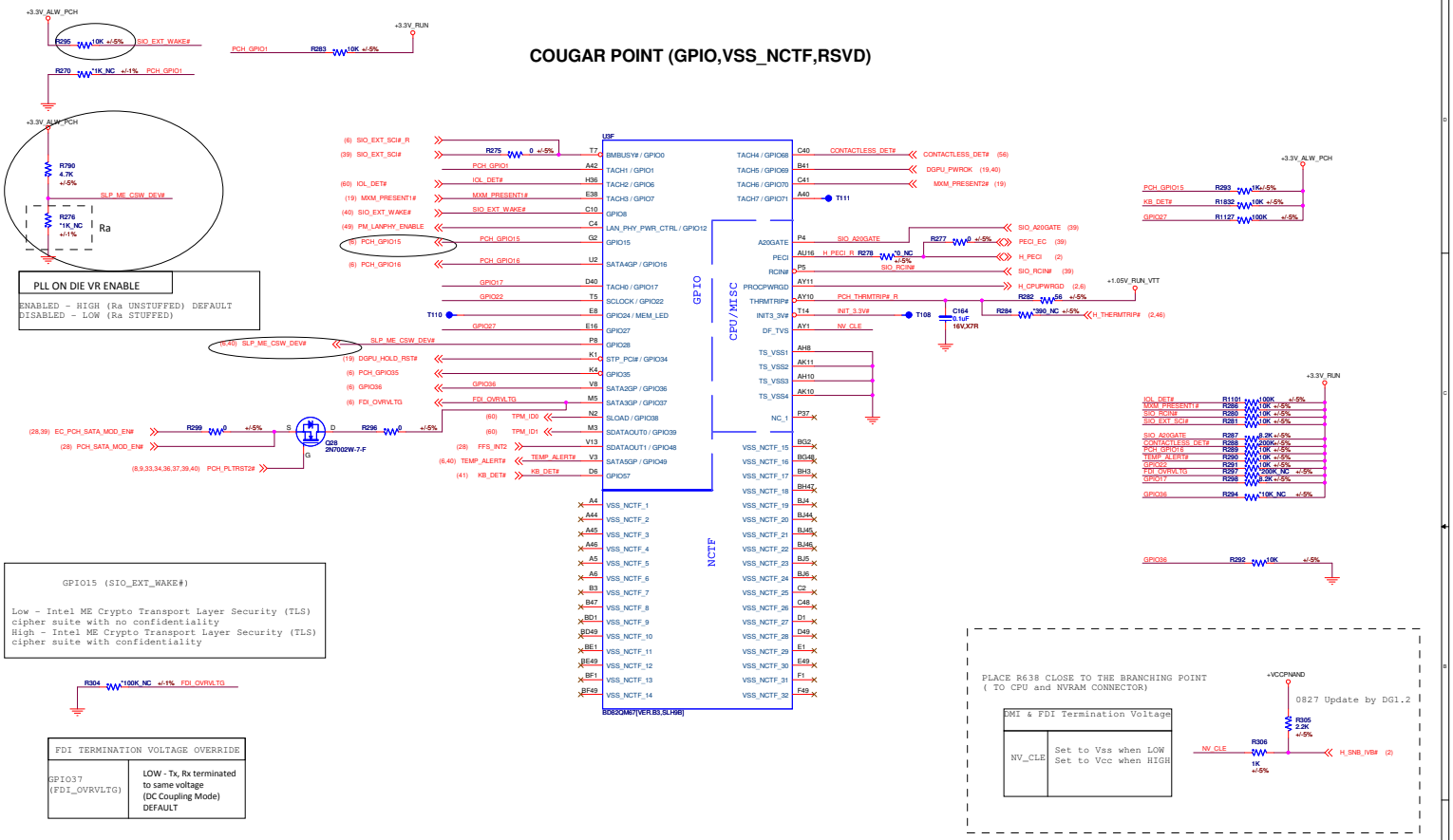
COUGAR POINT (GPIO,VSS_NCTF,RSVD)



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Title	11 -- CBT 5/7 (GPIO)	
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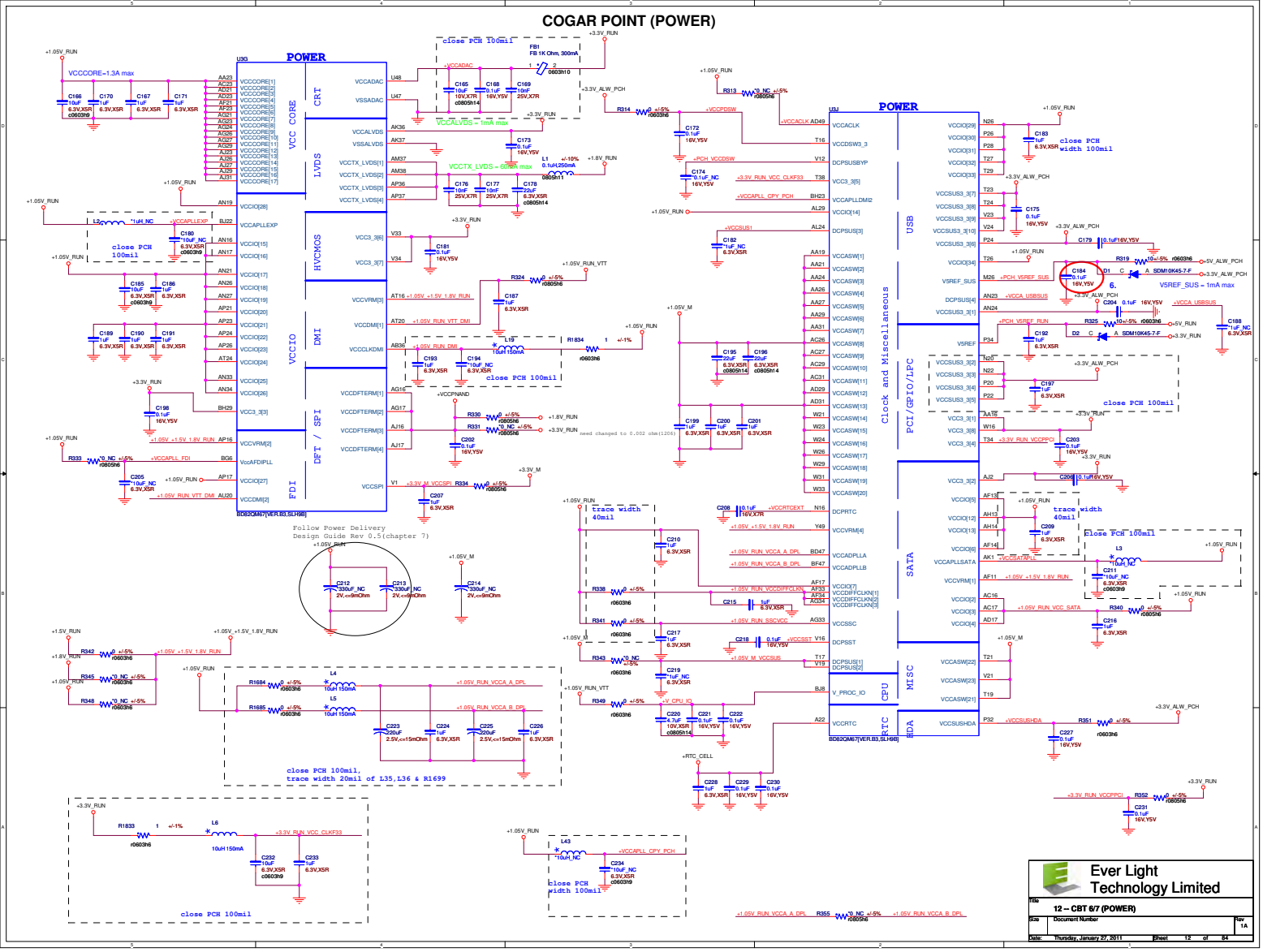
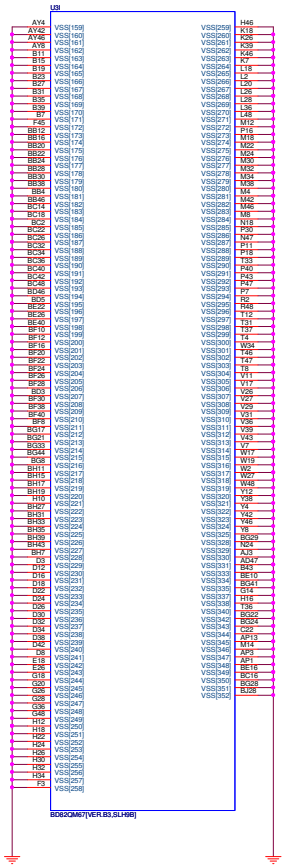
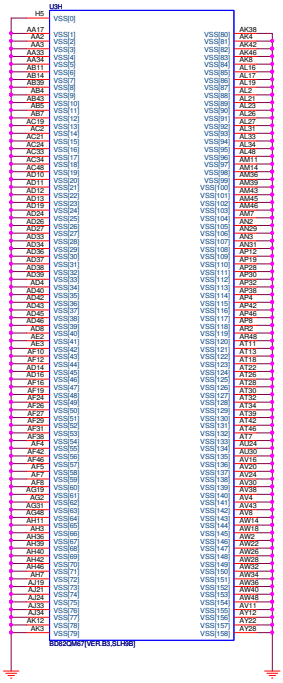
COGAR POINT (POWER)



Cougar Point (GND)





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Title	13 – CBT 7/7 (GND)	
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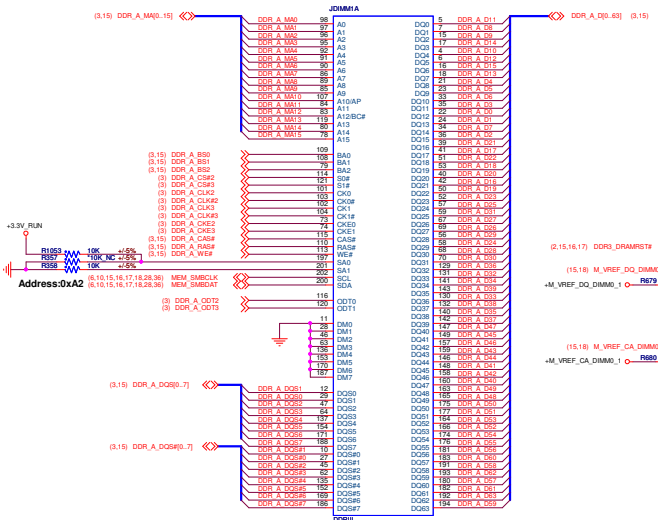
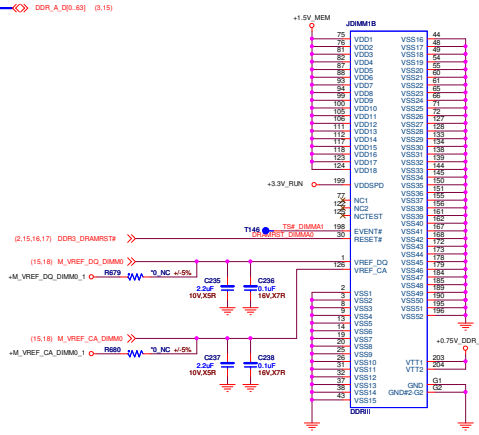
DDR3 Length Matching Formulas		
Signal Group	Min Length	Max Length
Control-to-Clock	Clock - 0.5"	Clock - 0.0"
Command-to-Clock	Clock - 0.5"	Clock - 0.5"
Strobe-to-Clock	Clock - 0.5"	Clock - 1.0"
Data-to-Strobe (per byte lane)	Strobe - 20 mils	Strobe + 20 mils

CHA_DIMM1_TOP_SIDE

JDIMM1 is RVS type.(H=100)



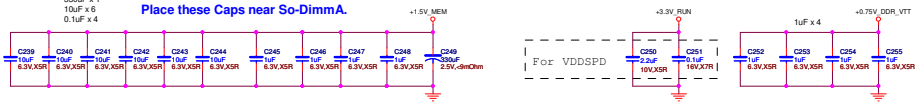


	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

+1.5V_SUS decoupling caps be located at the VDD pins of each SO-DIMM connector in the vicinity of the CMD, Clock and Control signals
Those capacitors should be placed on the same side of the motherboard as the SO-DIMM connector

330uF x 1
10uF x 6
0.1uF x 4

Place these Caps near So-DimmA.



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Title: 15 -- SODIMM-204P-A1

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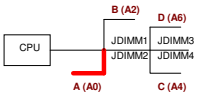
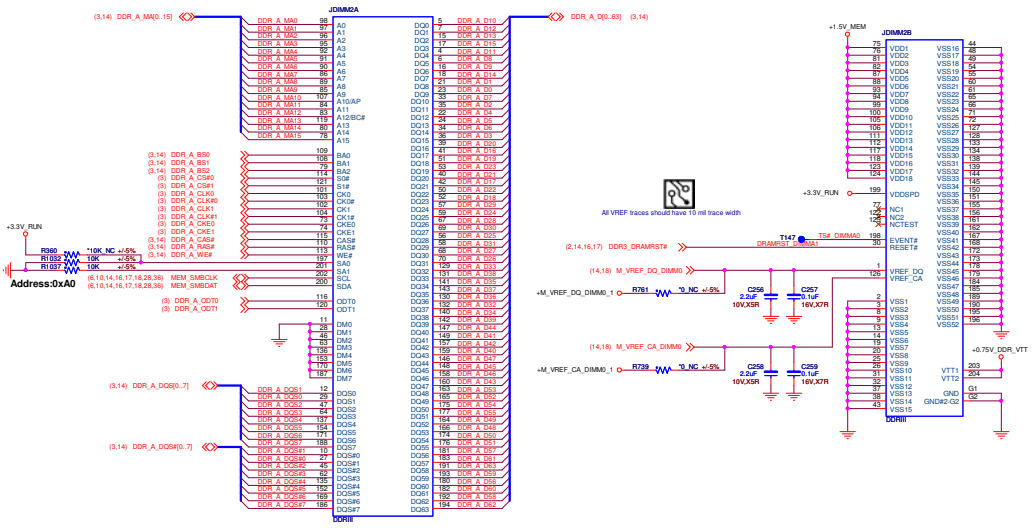


CHA_DIMM0_BOT_SIDE

JDIMM2 is RVS type.

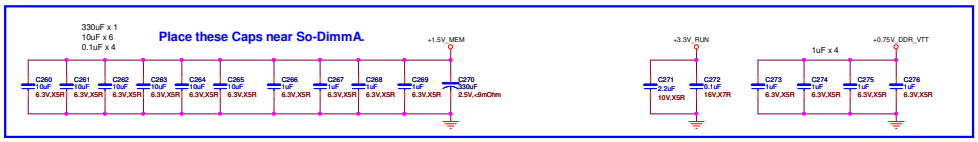
0510GC: CIS OK

DDR3 Length Matching Formulas		
Signal Group	Min Length	Max Length
Control-to-Clock	Clock - 0.5"	Clock - 0.0"
Command-to-Clock	Clock - 0.5"	Clock - 0.5"
Strobe-to-Clock	Clock - 0.5"	Clock - 1.0"
Data-to-Strobe (per byte lane)	Strobe - 20 mils	Strobe + 20 mils



	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

+1.5V_SUS decoupling caps be located at the VDD pins of each SO-DIMM connector in the vicinity of the CMD, Clock and Control signals
Those capacitors should be placed on the same side of the motherboard as the SO-DIMM connector



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Title	14 -- SODIMM-204P-A0	
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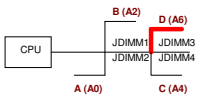
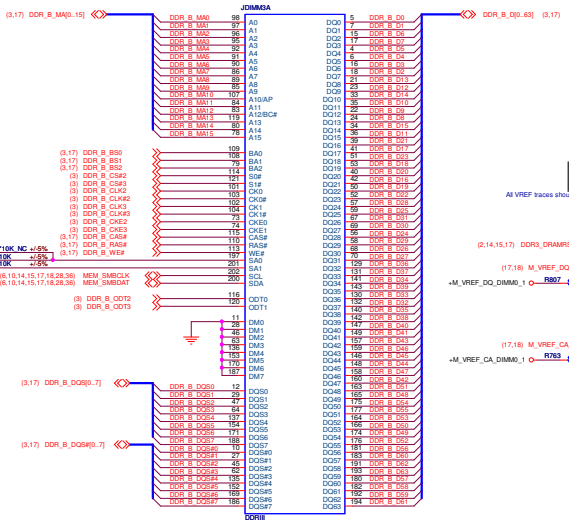


CHB_DIMM1_TOP_SIDE

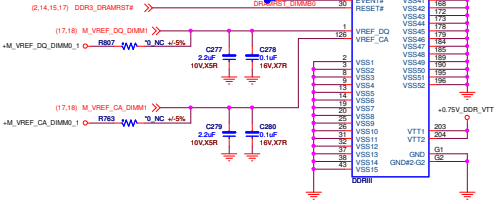
DDR3 Length Matching Formulas		
Signal Group	Min Length	Max Length
Control-to-Clock	Clock - 0.5"	Clock - 0.0"
Command-to-Clock	Clock - 0.5"	Clock - 0.5"
Strobe-to-Clock	Clock - 0.5"	Clock - 1.0"
Data-to-Strobe (per byte lane)	Strobe - 20 mils	Strobe + 20 mils

JDIMM3 is RVS type.

0526GC: change to RVS type

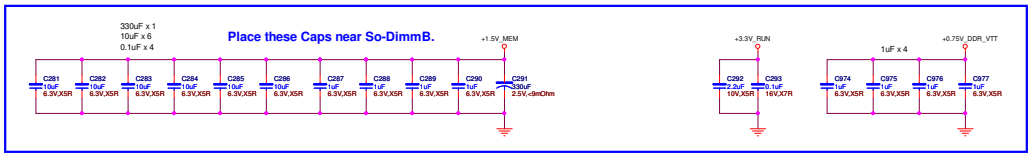


All VREF traces should have TO mil trace width



	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

+1.5V_SUS decoupling caps be located at the VDD pins of each SO-DIMM connector in the vicinity of the CMD, Clock and Control signals
Those capacitors should be placed on the same side of the motherboard as the SO-DIMM connector



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Title	17 -- SODIMM-204P-B0	
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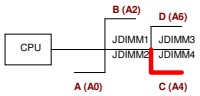
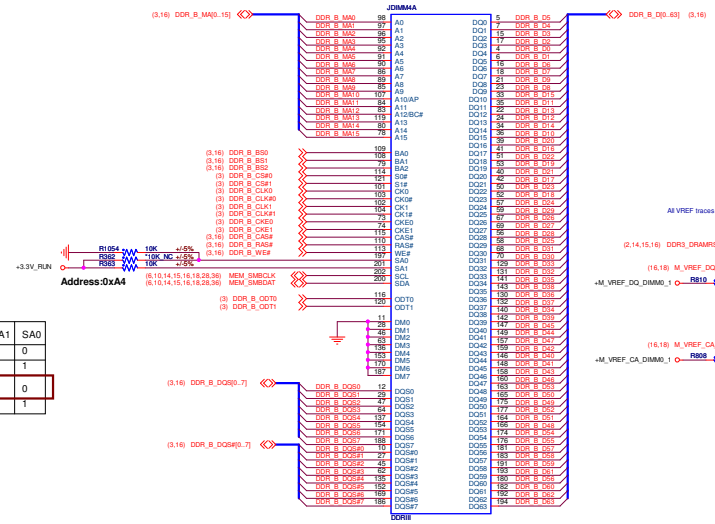


CHB_DIMM0_BOT_SIDE

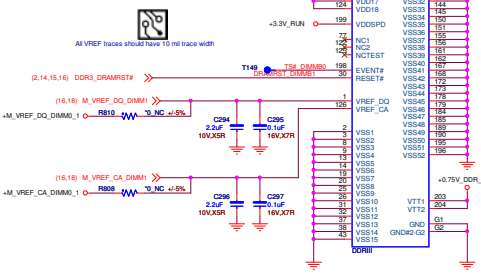
DDR3 Length Matching Formulas		
Signal Group	Min Length	Max Length
Control-to-Clock	Clock - 0.5"	Clock - 0.0"
Command-to-Clock	Clock - 0.5"	Clock - 0.5"
Strobe-to-Clock	Clock - 0.5"	Clock - 1.0"
Data-to-Strobe (per byte lane)	Strobe - 20 mils	Strobe + 20 mils

JDIMM4 is STD type.

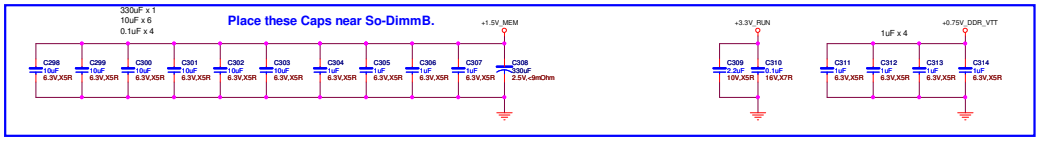
0510GC: CIS OK



	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1



+1.5V_SUS decoupling caps be located at the VDD pins of each SO-DIMM connector in the vicinity of the CMD, Clock and Control signals
Those capacitors should be placed on the same side of the motherboard as the SO-DIMM connector



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Title	16 -- SODIMM-204P-B0	
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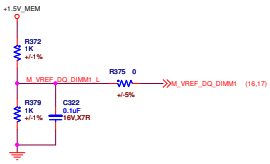
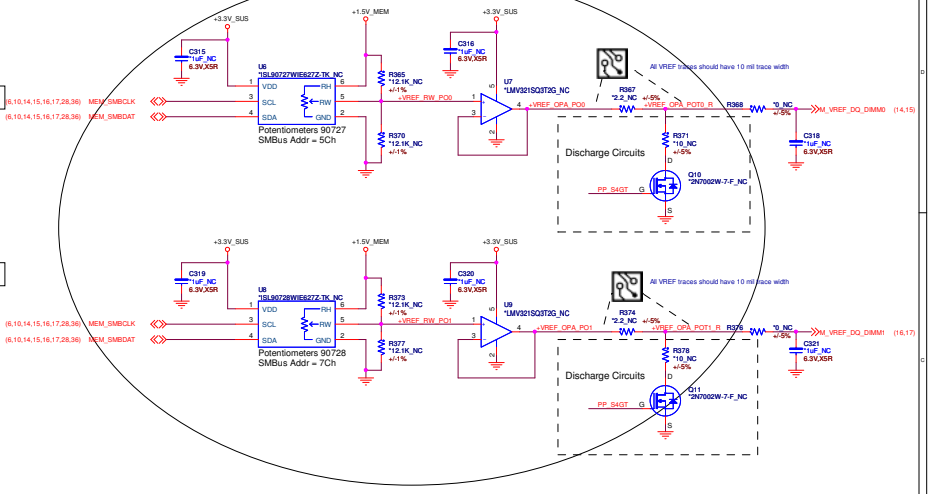
M1: Fixed SO-DIMM VREF_DQ (Default)

For CH A SO-DIMM VREF_DQ

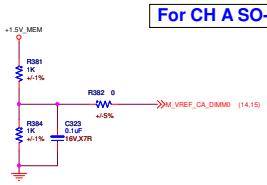


For CH B SO-DIMM VREF_DQ

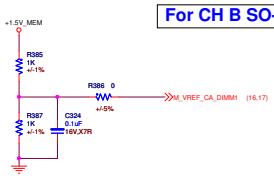
M2: Programmable SODIMM VREFDQ

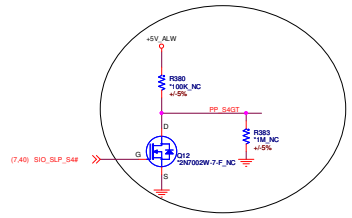


For CH A SO-DIMM VREF_CA



For CH B SO-DIMM VREF_CA





Ever Light Technology Limited		
Title	18 -- DDR3 VREF	
Size	Document Number: Thunder	Rev: 1A
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MXM 3.0 CONNECTOR

MXM SPEC:
7~20V, Up to 10A

0524GC: CIS OK

2.5 A

PEX swing slect
0: High swing
NC: Lowing swing

CEC MXM Internal PU

GPU internal PU.

To GPIO module side is GND

DOCK DP1
MB HDMI

eDP Panel

DOCK DP2

MB DP Port

PU at PCH.

DPA and DPC output on MXM3.0 is must
DPB and DPD output is optional.

Mechanical Key

CONN-PCI-X

1.Whole TX & RX AC decoupling Cap(64 pcs) need to place within 0.5" of MXM Conn
2.TX cap at CPU Side

MXM PEG SPEC
Length Low swing: 7 inches High swing: 10 inches

Thermal Trip

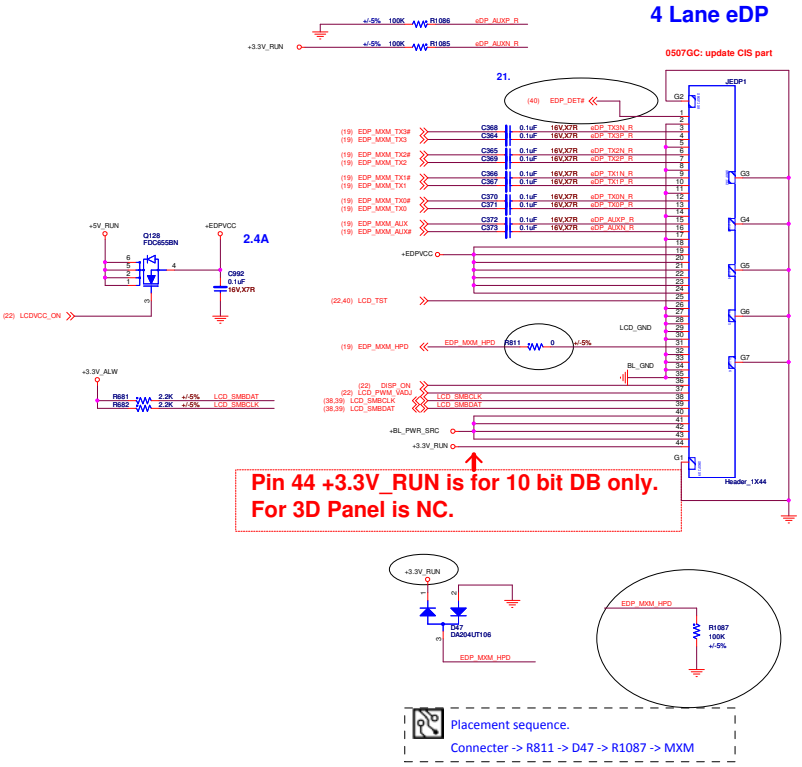
Thermal Alert

GPU internal PU.

From 5048

Ever Light Technology Limited

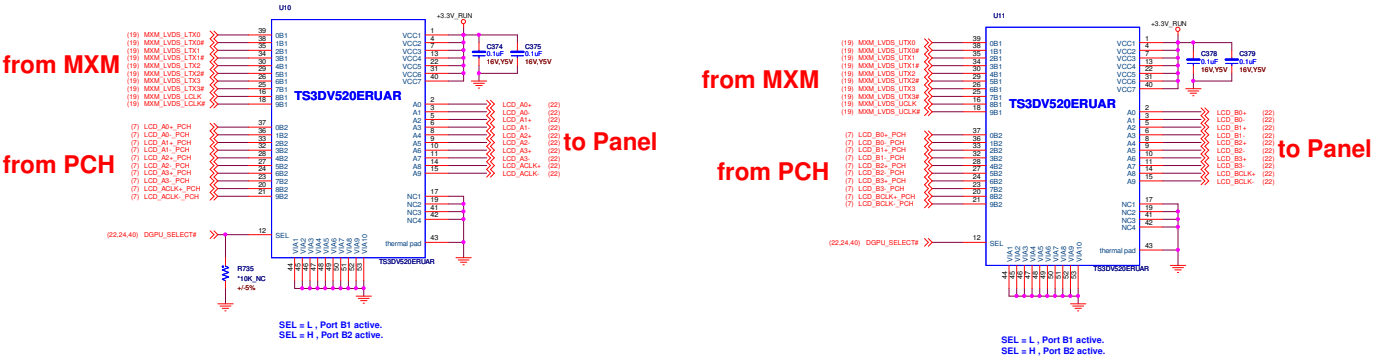
Title: 19 – MXM3.0 Connector
Size: | Document Number: | Rev: 1A
Date: Thursday, January 27, 2011 | Sheet 19 of 84



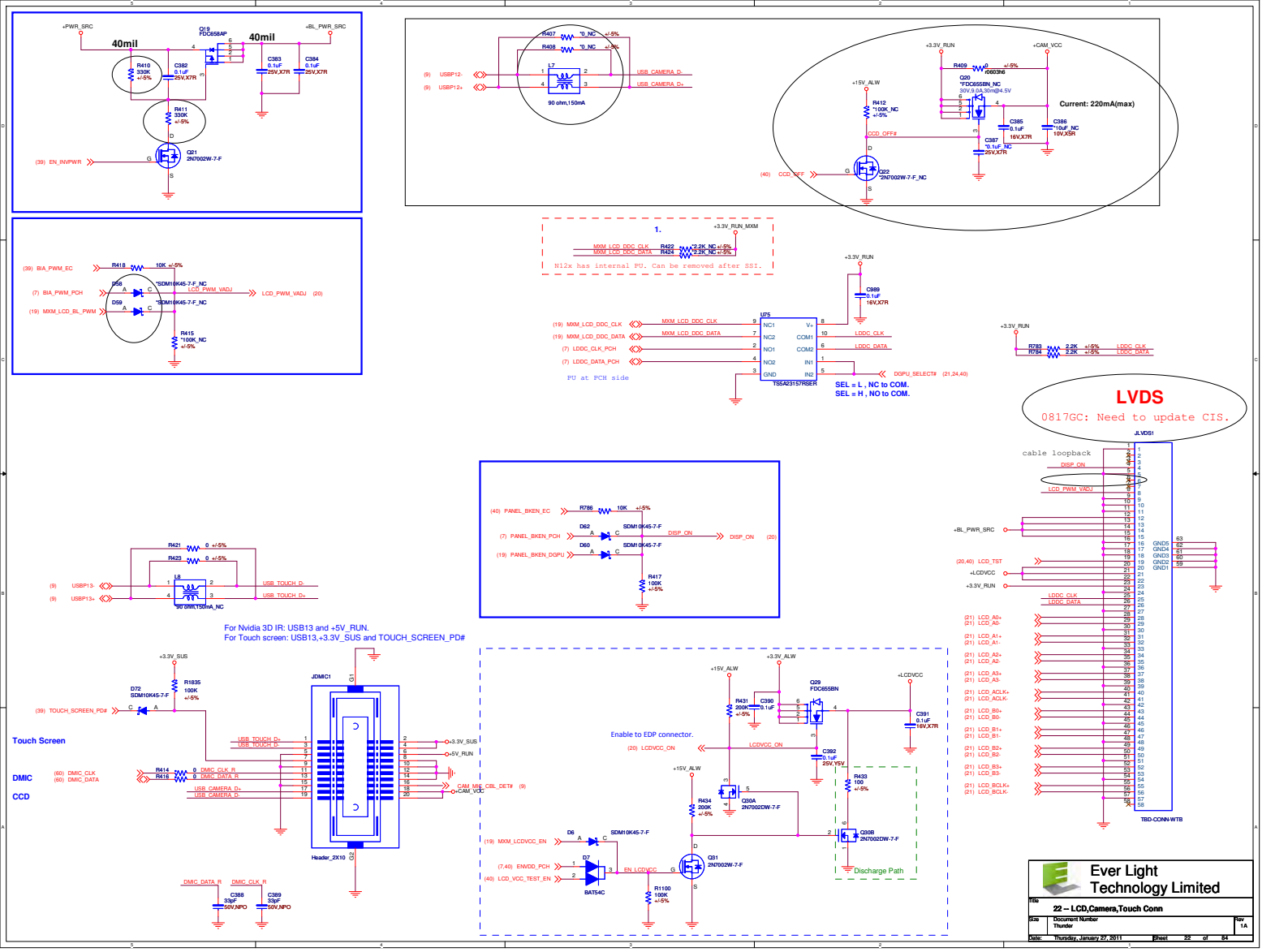
Ever Light Technology Limited

Title	20 – 17" eDP for PANEL	
Size	Document Number: Thunder	Rev: 1A
Date: Thursday, January 27, 2011	Sheet 20 of 84	

LVDS MUX for Panel



Ever Light Technology Limited	
Title	21 -- LVDS MUX for PANEL
Size	Document Number: Thunder — Rev: 1A
Date: Thursday, January 27, 2011	Sheet 21 of 84


+PWR_SRC
40mil
Q19
FDC658AP
40mil
+BL_PWR_SRC
R416
330K
+/-5%
C382
0.1uF
25V,X7R
C383
0.1uF
25V,X7R
C384
0.1uF
25V,X7R
R411
330K
+/-5%
Q21
2N7002W-7-F
(39) EN_INVPWR
(39) BIA_PWM_EC
R418
10K +/-5%
D58
*SDM10K45-7-F_NC
(7) BIA_PWM_PCH
LCD_PWM_VADJ
LCD_PWM_VADJ (20)
D59
*SDM10K45-7-F_NC
(19) MXM_LCD_BL_PWM
R415
*100K_NC
+/-5%
(9) USBP12-
(9) USBP12+
R407
*0_NC +/-5%
R408
*0_NC +/-5%
L7
90 ohm,150mA
USB_CAMERA_D-
USB_CAMERA_D+
+3.3V_RUN
+CAM_VCC
R409
0
+/-5%
r0603n6
Q20
*FDC655BN_NC
30V,9.6A,30m@4.5V
Current: 220mA(max)
+15V_ALW
R412
*100K_NC
+/-5%
C385
0.1uF
16V,X7R
C386
*10uF_NC
10V,X5R
CCD_OFF#
C387
*0.1uF_NC
25V,X7R
(40) CCD_OFF
Q22
*2N7002W-7-F_NC
1.
+3.3V_RUN_MXM
MXM_LCD_DDC_CLK
MXM_LCD_DDC_DATA
R422
*2.2K_NC +/-5%
R424
*2.2K_NC +/-5%
N12x has internal PU. Can be removed after SSI.
+3.3V_RUN
C989
0.1uF
16V,X7R
(19) MXM_LCD_DDC_CLK
(19) MXM_LCD_DDC_DATA
(7) LDDC_CLK_PCH
(7) LDDC_DATA_PCH
PU at PCH side
U75
NC1
NC2
NO1
NO2
GND
V+
COM1
COM2
IN1
IN2
TS5A23157RSER
LDDC_CLK
LDDC_DATA
DGPU_SELECT# (21,24,40)
SEL = L , NC to COM.
SEL = H , NO to COM.
+3.3V_RUN
R783
R784
2.2K
2.2K
+/-5%
+/-5%
LDDC_CLK
LDDC_DATA
LVDS
0817GC: Need to update CIS.
JLVDS1
cable loopback
DISP_ON
LCD_PWM_VADJ
+BL_PWR_SRC
(20,40) LCD_TST
+LCDVCC
+3.3V_RUN
LDDC_CLK
LDDC_DATA
(21) LCD_A0+
(21) LCD_A0-
(21) LCD_A1+
(21) LCD_A1-
(21) LCD_A2+
(21) LCD_A2-
(21) LCD_A3+
(21) LCD_A3-
(21) LCD_ACLK+
(21) LCD_ACLK-
(21) LCD_B0+
(21) LCD_B0-
(21) LCD_B1+
(21) LCD_B1-
(21) LCD_B2+
(21) LCD_B2-
(21) LCD_B3+
(21) LCD_B3-
(21) LCD_BCLK+
(21) LCD_BCLK-
GND5
GND4
GND3
GND2
GND1
TBD-CONN-WTB
(40) PANEL_BKEN_EC
R786
10K +/-5%
D62
SDM10K45-7-F
(7) PANEL_BKEN_PCH
DISP_ON
DISP_ON (20)
D60
SDM10K45-7-F
(19) PANEL_BKEN_DGPU
R417
100K
+/-5%
R421
0 +/-5%
R423
0 +/-5%
(9) USBP13-
(9) USBP13+
L8
90 ohm,150mA_NC
USB_TOUCH_D-
USB_TOUCH_D+
For Nvidia 3D IR: USB13 and +5V_RUN.
For Touch screen: USB13,+3.3V_SUS and TOUCH_SCREEN_PD#
+3.3V_SUS
R1935
100K
+/-5%
D72
SDM10K45-7-F
(39) TOUCH_SCREEN_PD#
JDMIC1
Header_2X10
Touch Screen
DMIC
CCD
(60) DMIC_CLK
(60) DMIC_DATA
R414
R416
0
0
DMIC_CLK_R
DMIC_DATA_R
USB_CAMERA_D+
USB_CAMERA_D-
USB_TOUCH_D+
USB_TOUCH_D-
+3.3V_SUS
+5V_RUN
CAM_MIC_CBL_DET# (9)
+CAM_VCC
DMIC_DATA_R
DMIC_CLK_R
C388
33pF
50V,NPO
C389
33pF
50V,NPO
Enable to EDP connector.
(20) LCDVCC_ON
LCDVCC_ON
+15V_ALW
+3.3V_ALW
R431
200K
+/-5%
C390
0.1uF
Q29
FDC655BN
+LCDVCC
C391
0.1uF
16V,X7R
C392
0.1uF
25V,Y5V
R434
200K
+/-5%
Q30A
2N7002DW-7-F
R433
100
+/-5%
Q30B
2N7002DW-7-F
Discharge Path
(19) MXM_LCDVCC_EN
(7,40) ENVDD_PCH
(40) LCD_VCC_TEST_EN
D6
SDM10K45-7-F
D7
BAT54C
EN_LCDVCC
Q31
2N7002W-7-F
R1100
100K
+/-5%
Ever Light
Technology Limited
Title
22 -- LCD,Camera,Touch Conn
Size
Document Number
Thunder
Rev
1A
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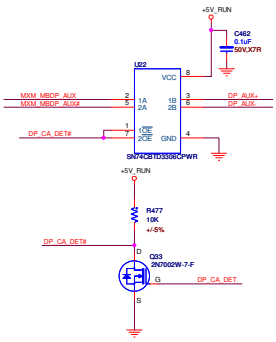
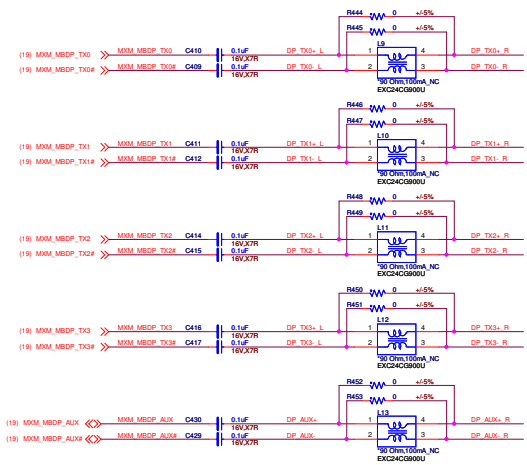
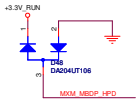
22
of
84

FOR Dongle

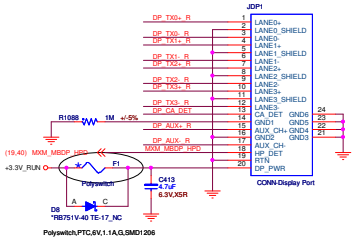


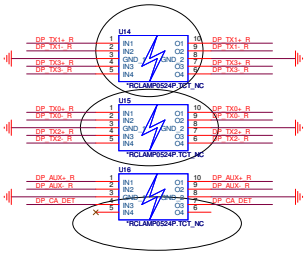
Display Port



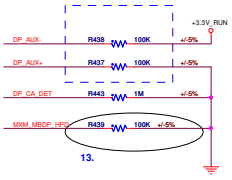


0524GC: CIS OK





Put close to connecter.



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Title	22 -- Display Port & Re-Driver	
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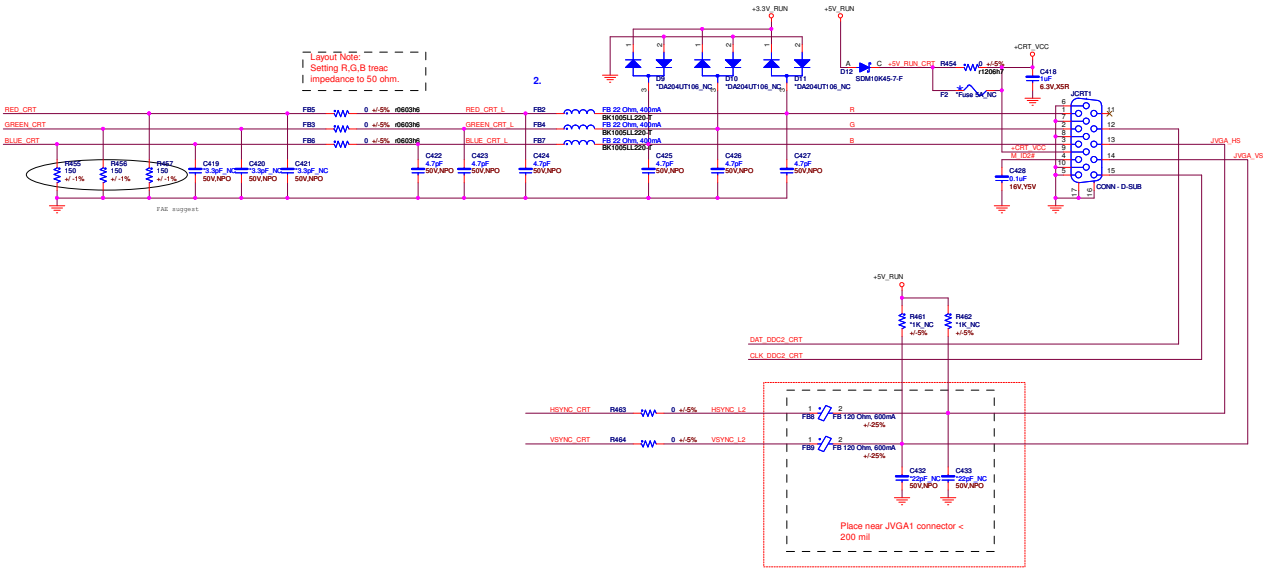
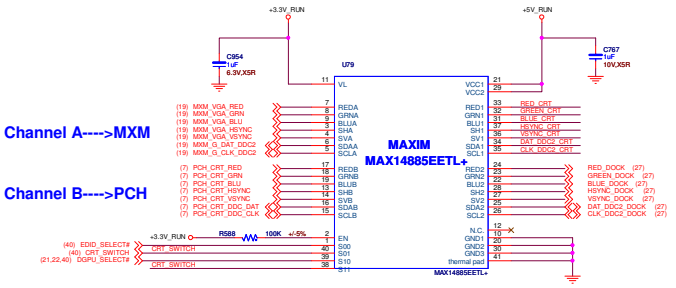
CRT





Truth table

	A-->Port 1	B-->Port 1	A-->Port 2	B-->Port 2
S01/S11 (CRT_SWITCH)	0	0	1	1
S10 (DGPU_SELECT#)	0	1	0	1
S00 (EDID_SELECT#)	0	1	0	1

Ever Light Technology Limited

Title	23 -- CRT & MUX	
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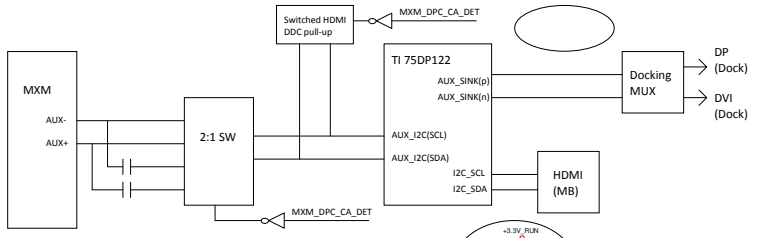
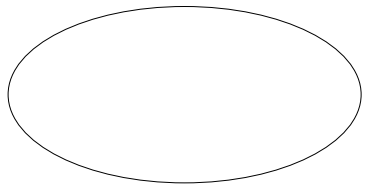
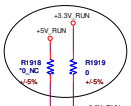
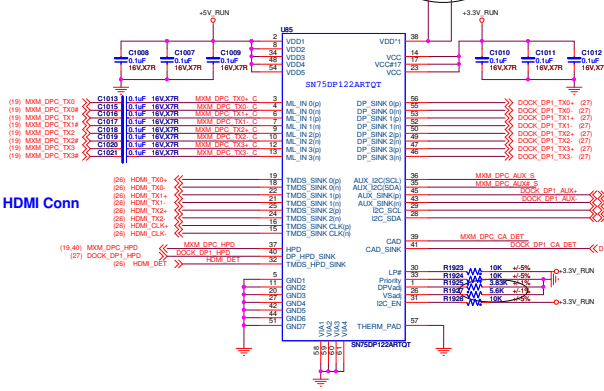




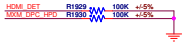


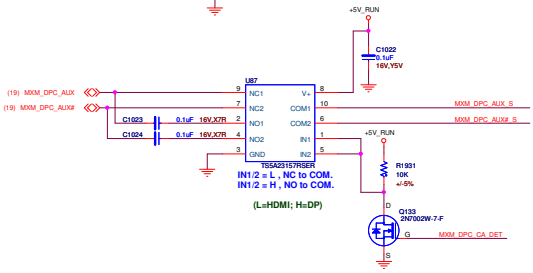
From dGPU

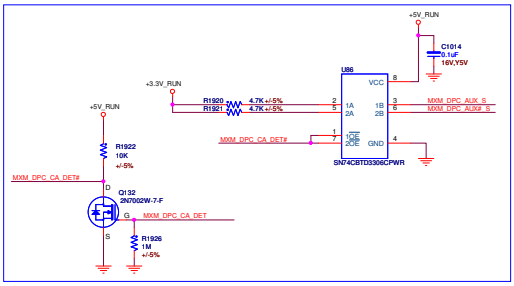


To Docking DP1 Port

TO MB HDMI Conn







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Title	24 -- MUX for HDMI	
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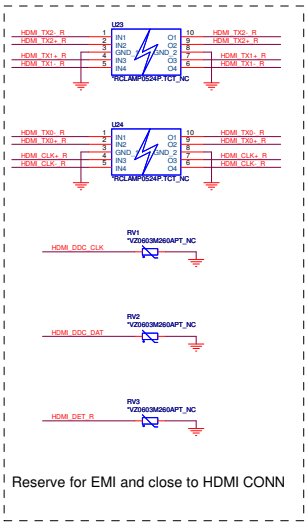
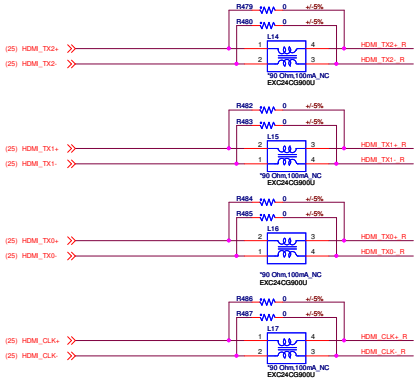
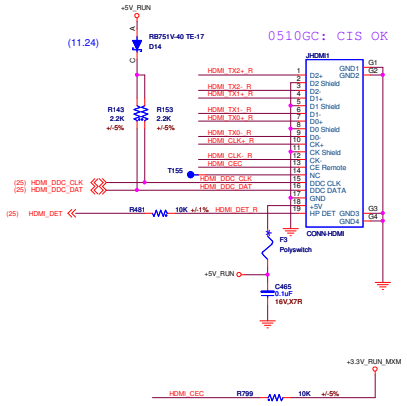
HDMI CONN







Ever Light Technology Limited			
Title	25 -- HDMI		
Size	Document Number Thunder		Rev 1A
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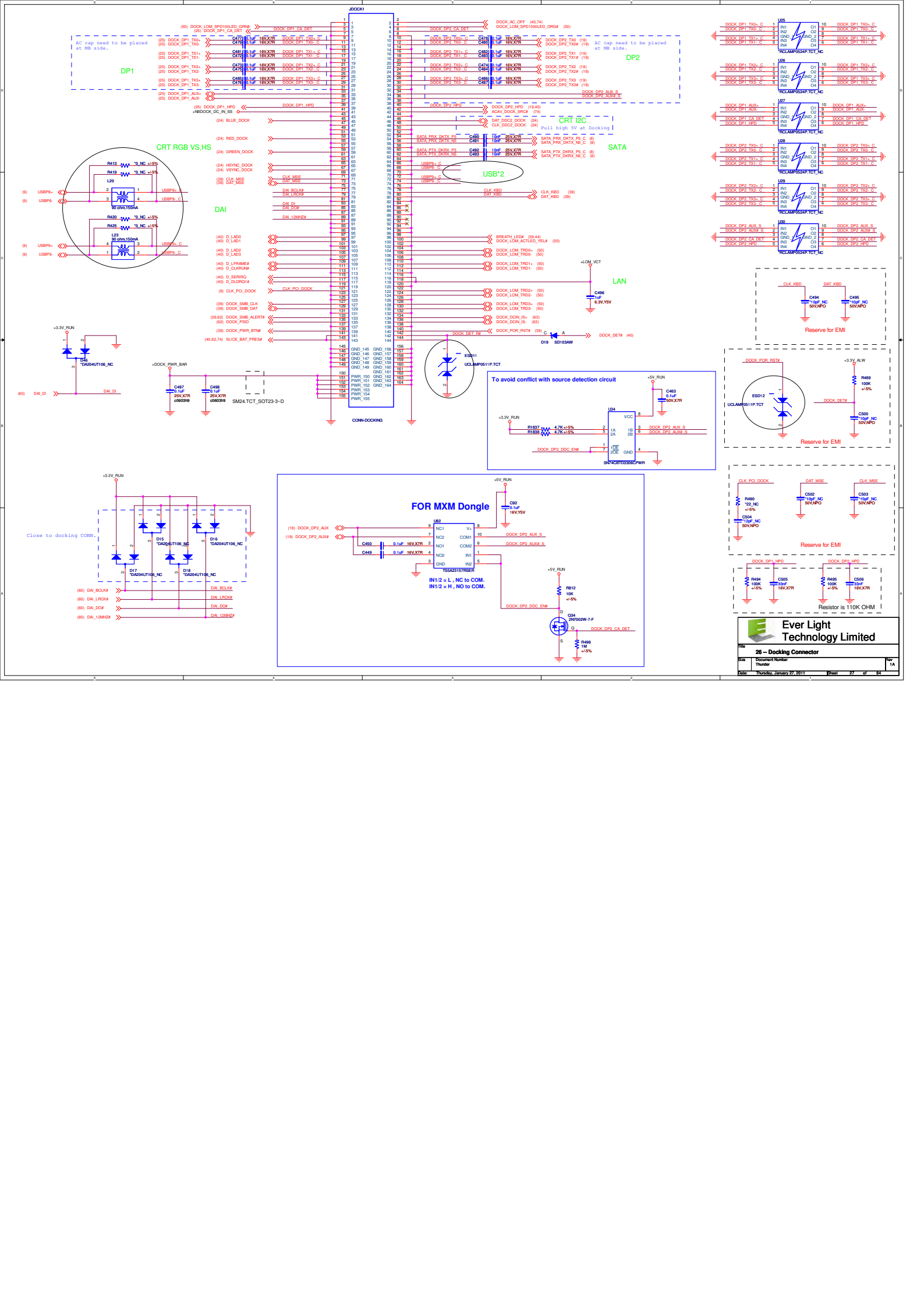
JDOCK1
CONN-DOCKING
DP1
DP2
CRT RGB VS,HS
DAI
CRT I2C
Pull high 5V at Docking
SATA
USB*2
LAN
AC cap need to be placed at MB side.
AC cap need to be placed at MB side.
To avoid conflict with source detection circuit
FOR MXM Dongle
IN1/2 = L , NC to COM.
IN1/2 = H , NO to COM.
Close to docking CONN.
Reserve for EMI
Reserve for EMI
Reserve for EMI
Resistor is 110K OHM
Ever Light Technology Limited
26 -- Docking Connector
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Second HDD

HDD Connector

6.

JHDD1

SATA Port 1

CONN-SATA
LD2122J-S0PL6H

HDD POWER

3-axis Fall Sensor (HDD data protector)

U52

DE3510LTR8

I2C Address Setting

SDO = H (3A) Internal PU	SDO = L (38)
Addr = 0011101	Addr = 0011100

Main HDD

HDD Connector

6.

JHDD2

SATA Port 0

CONN-SATA
LD2122J-S0PL6H

SATA3 Re-Driver For main HDD

Current: 92mA(max)

U53

MAX49519ECTP+

ODD Connector

JODD1

SATA port 3

CONN-SATA

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Title	28 -- 17" HDD, ODD, G-SENSOR
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Title	29 -- 15" HDD, ODD, G-SENSOR	
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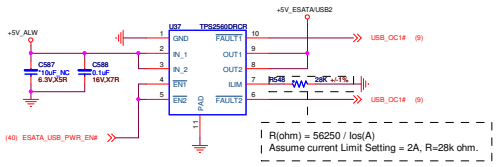
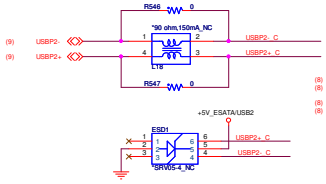
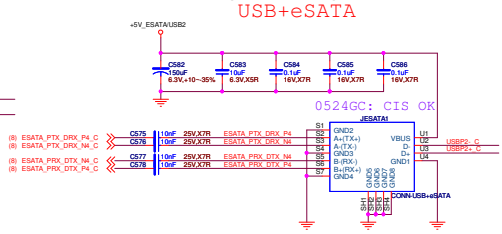
USB Power





USB(Back Side)

USB+eSATA



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Title	29 -- eSATA/USB, USB x 2	
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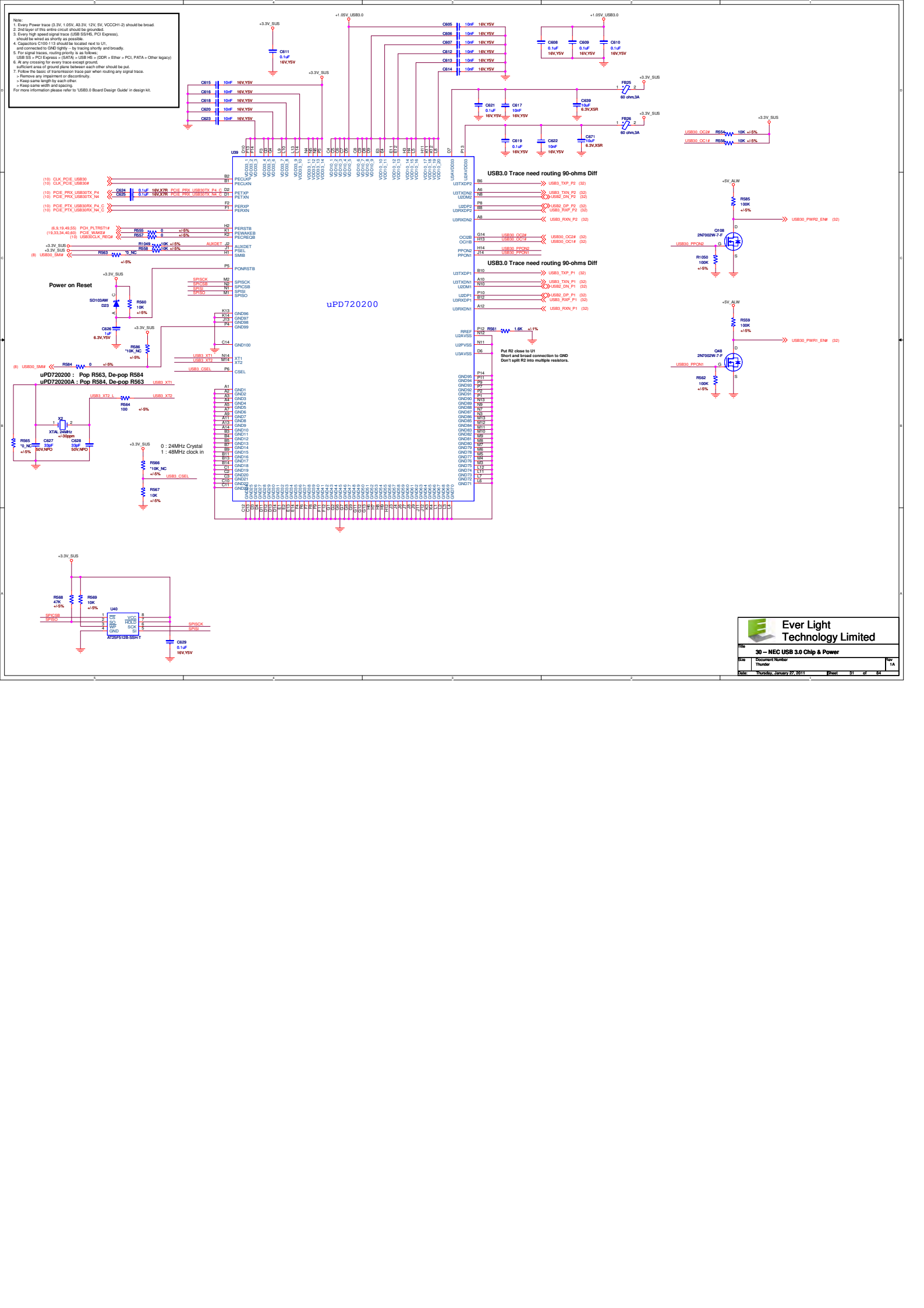
Note:
1. Every Power trace (3.3V, 1.05V, A0,3V, 12V, 5V, VCCCH1-2) should be broad.
2. 2nd layer of this entire circuit should be grounded.
3. Every high speed signal trace (USB SS/HS, PCI Express), should be wired as shortly as possible.
4. Capacitors C100-113 should be located next to U1, and connected to GND tightly - by tracing shortly and broadly.
5. For signal traces, routing priority is as follows; USB SS > PCI Express > (SATA) > USB HS > (DDR > Ether > PCI, PATA > Other legacy)
6. At any crossing for every trace except ground, sufficient area of ground plane between each other should be put.
7. Follow the basic of transmission trace pair when routing any signal trace.
> Remove any impairment or discontinuity.
> Keep same length by each other.
> Keep same width and spacing.
For more information please refer to 'USB3.0 Board Design Guide' in design kit.
uPD720200
USB3.0 Trace need routing 90-ohms Diff
USB3.0 Trace need routing 90-ohms Diff
Power on Reset
uPD720200 : Pop R563, De-pop R584
uPD720200A : Pop R584, De-pop R563
0 : 24MHz Crystal
1 : 48MHz clock in
Put R2 close to U1
Short and broad connection to GND
Don't split R2 into multiple resistors.
Ever Light Technology Limited
30 -- NEC USB 3.0 Chip & Power
Thunder
Thursday, January 27, 2011
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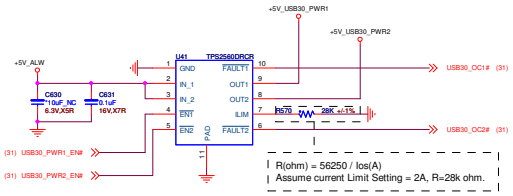

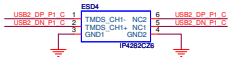

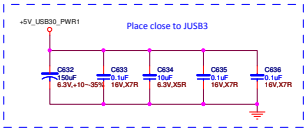

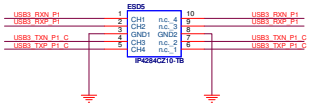

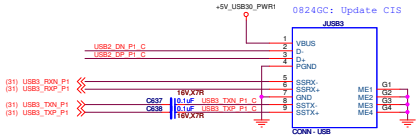

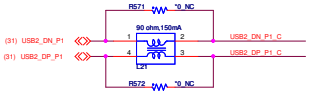

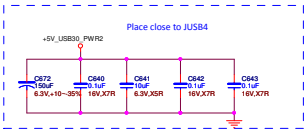

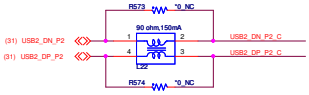

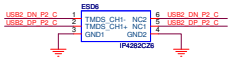

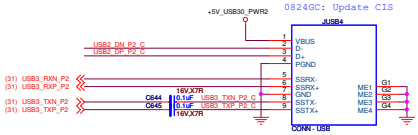

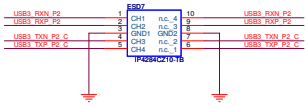

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Title	31 -- USB 3.0 Connector x 2	
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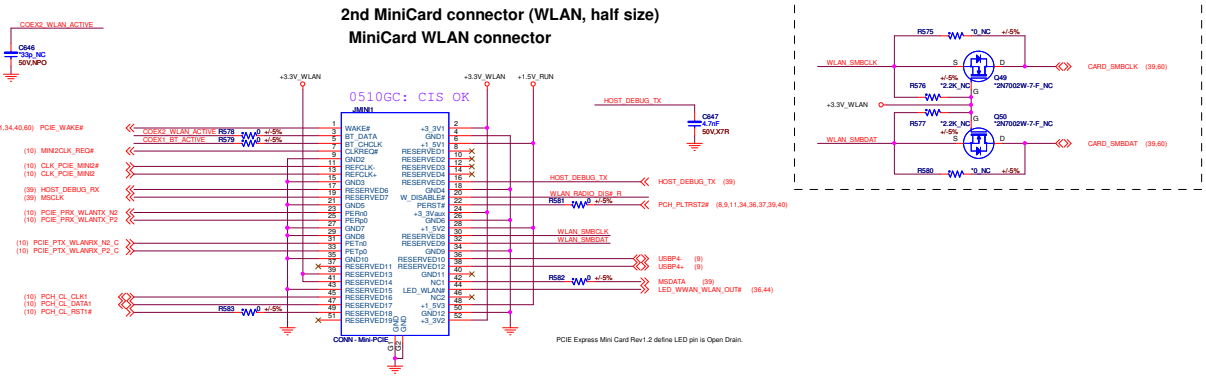
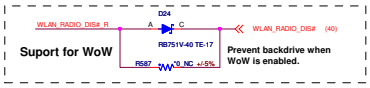
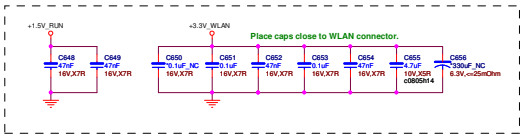
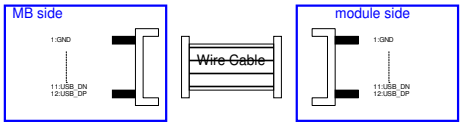
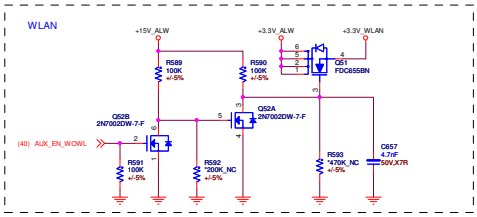
2nd MiniCard connector (WLAN, half size)
MiniCard WLAN connector

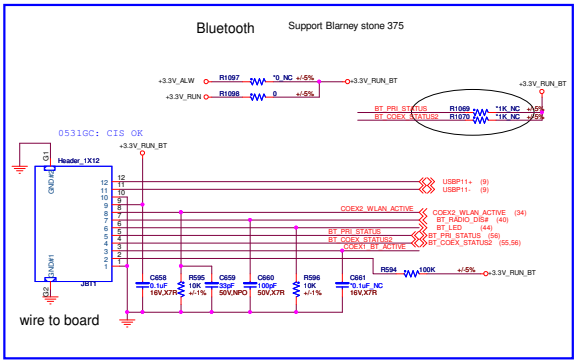












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Title	33 -- WLAN(1/2 Mini cad), BT
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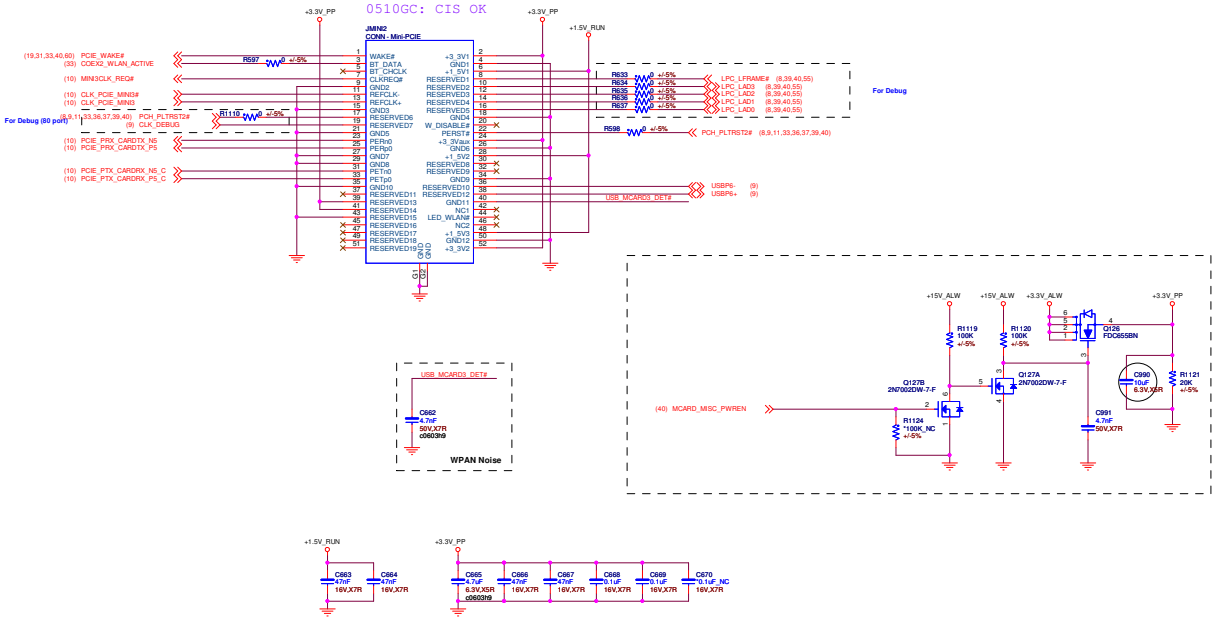
3rd MiniCard connector (Flash, half size)
MiniCard connector



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Title	34 -- Flash /PP(1/2Mini cad)		
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Title	3S -- 15" WWAN+ SIM+MUX	
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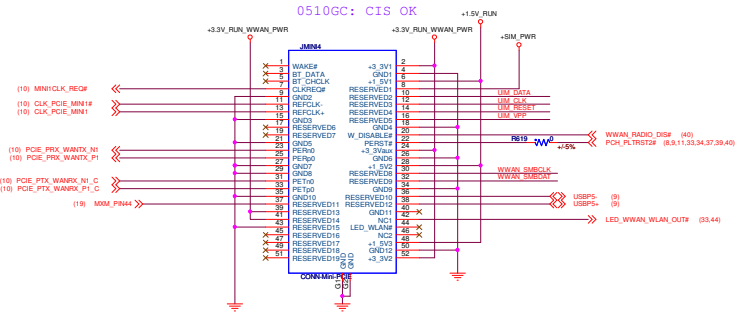
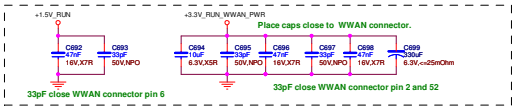
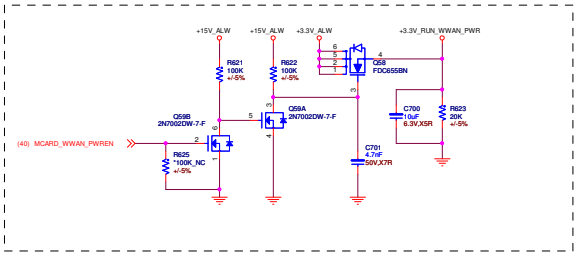
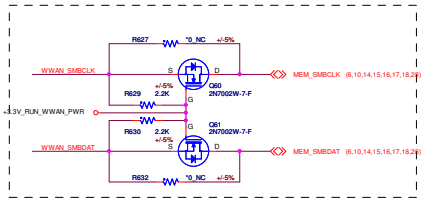
MiniCard WWAN connector

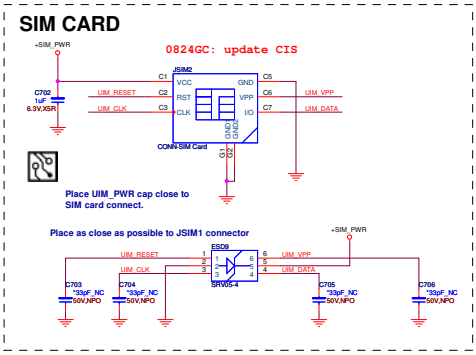








SIM CARD



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Title	36 -- 17" WWAN+ SIM	
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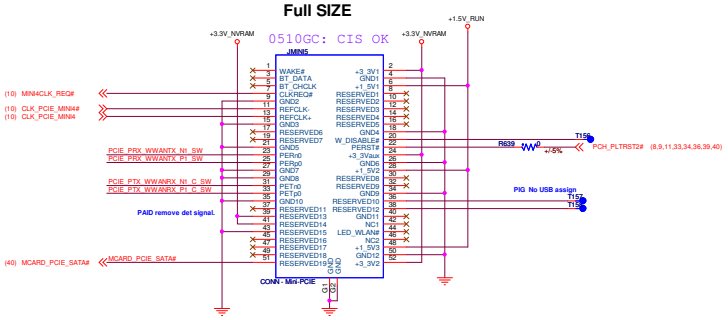
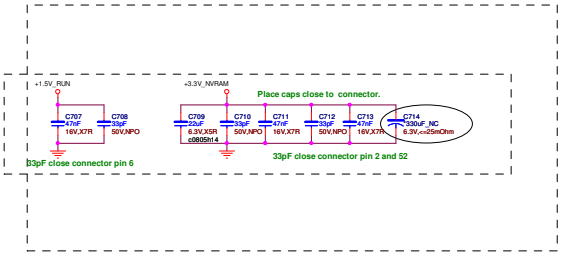
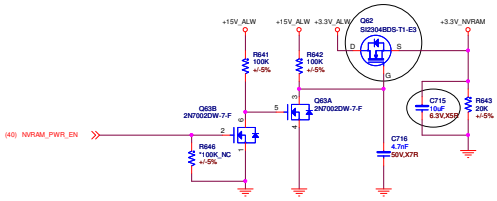
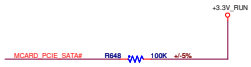
4th MiniCard connector (NVRAM, full size)

NVRAM connector
Full SIZE

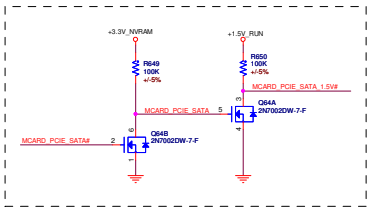






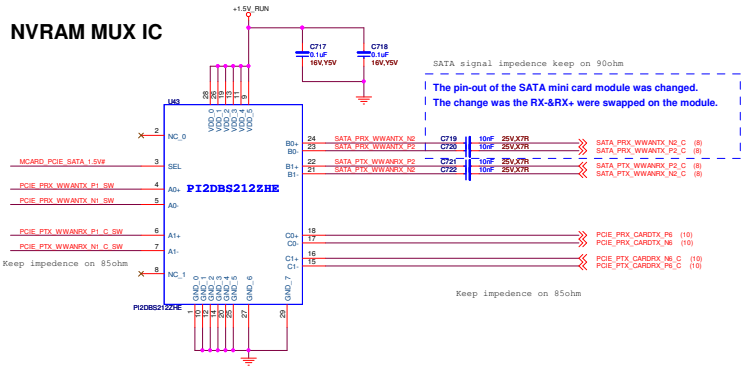


PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+-9%	1000	750	
	+-9%	330	250	250 (wake enable) 5 (Not wake enable)
+1.5V	+-5%	500	375	NA



Function	SEL
Port A to Port B	0
Port A to Port C	1

NVRAM MUX IC



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Title	37 – 17" NVRAM+MUX	
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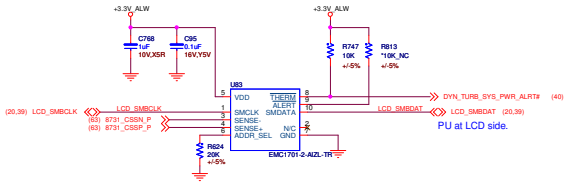
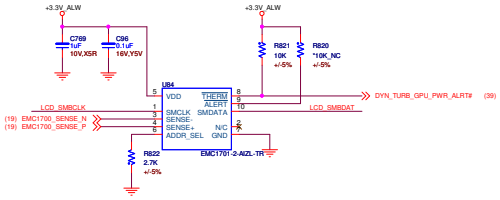
Monitor Charger current



RESISTOR (5%)	SMBUS ADDRESS	RESISTOR (5%)	SMBUS ADDRESS	
0	1001_100(r/w)	1600	0101_000(r/w)	
100	1001_101(r/w)	2000	0101_001(r/w)	
180	1001_110(r/w)	2700	0101_010(r/w)	U84
300	1001_111(r/w)	3600	0101_011(r/w)	
430	1001_000(r/w)	5600	0101_100(r/w)	
560	1001_001(r/w)	9100	0101_100(r/w)	
750	1001_010(r/w)	20000	0101_101(r/w)	U83
1270	1001_011(r/w)	Open	0111_000(r/w)	

Monitor PWR_SRC_MXM



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Title	38 -- Express Card & Power	
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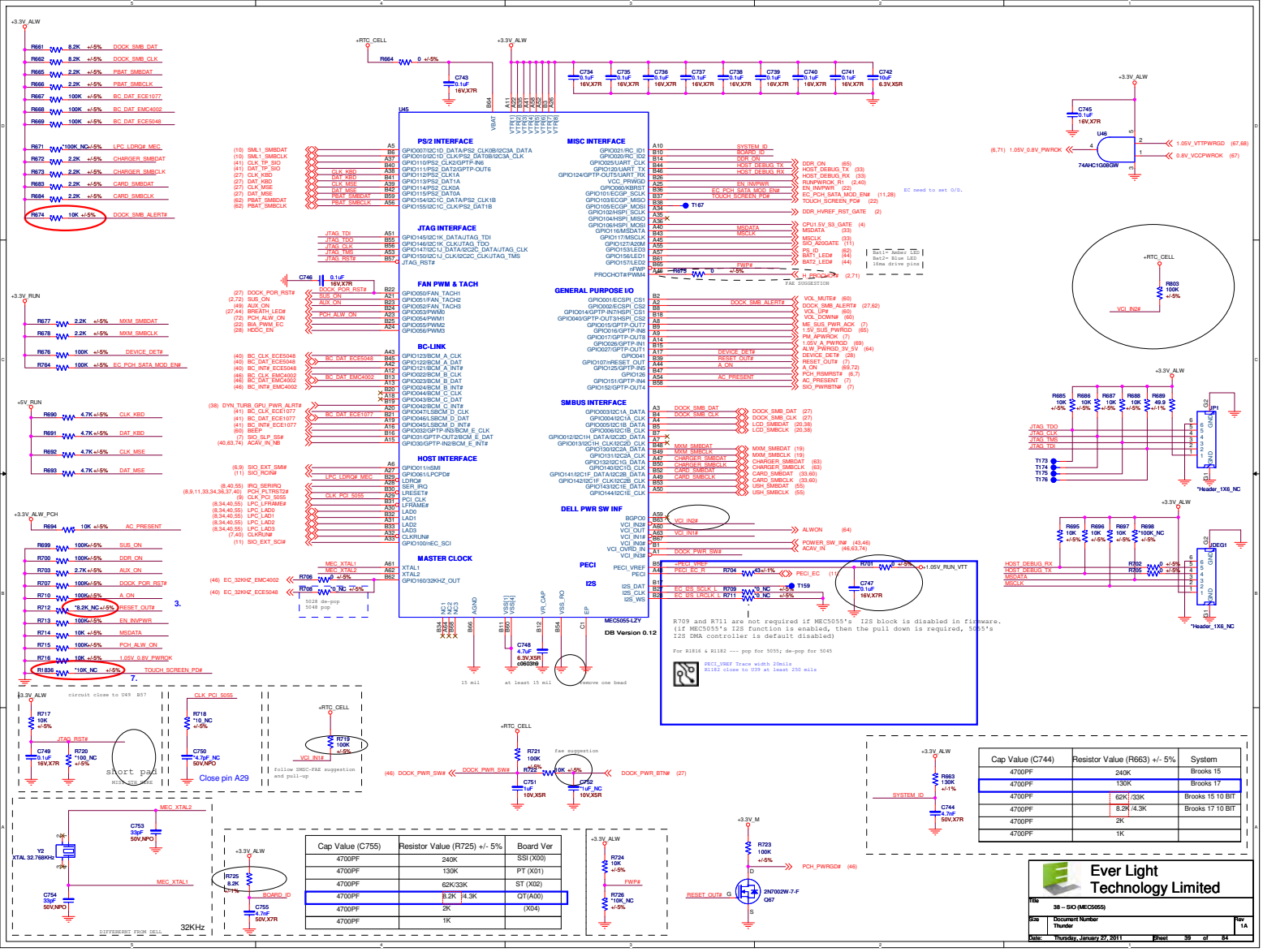

Cap Value (C744)	Resistor Value (R663) +/- 5%	System
4700PF	240K	Brooks 15
4700PF	130K	Brooks 17
4700PF	62K /33K	Brooks 15 10 BIT
4700PF	8.2K /4.3K	Brooks 17 10 BIT
4700PF	2K	
4700PF	1K	

Cap Value (C755)	Resistor Value (R725) +/- 5%	Board Ver
4700PF	240K	SSI (X00)
4700PF	130K	PT (X01)
4700PF	62K/33K	ST (X02)
4700PF	8.2K /4.3K	QT(A00)
4700PF	2K	(X04)
4700PF	1K	

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Title	38 – SIO (MEC5055)	
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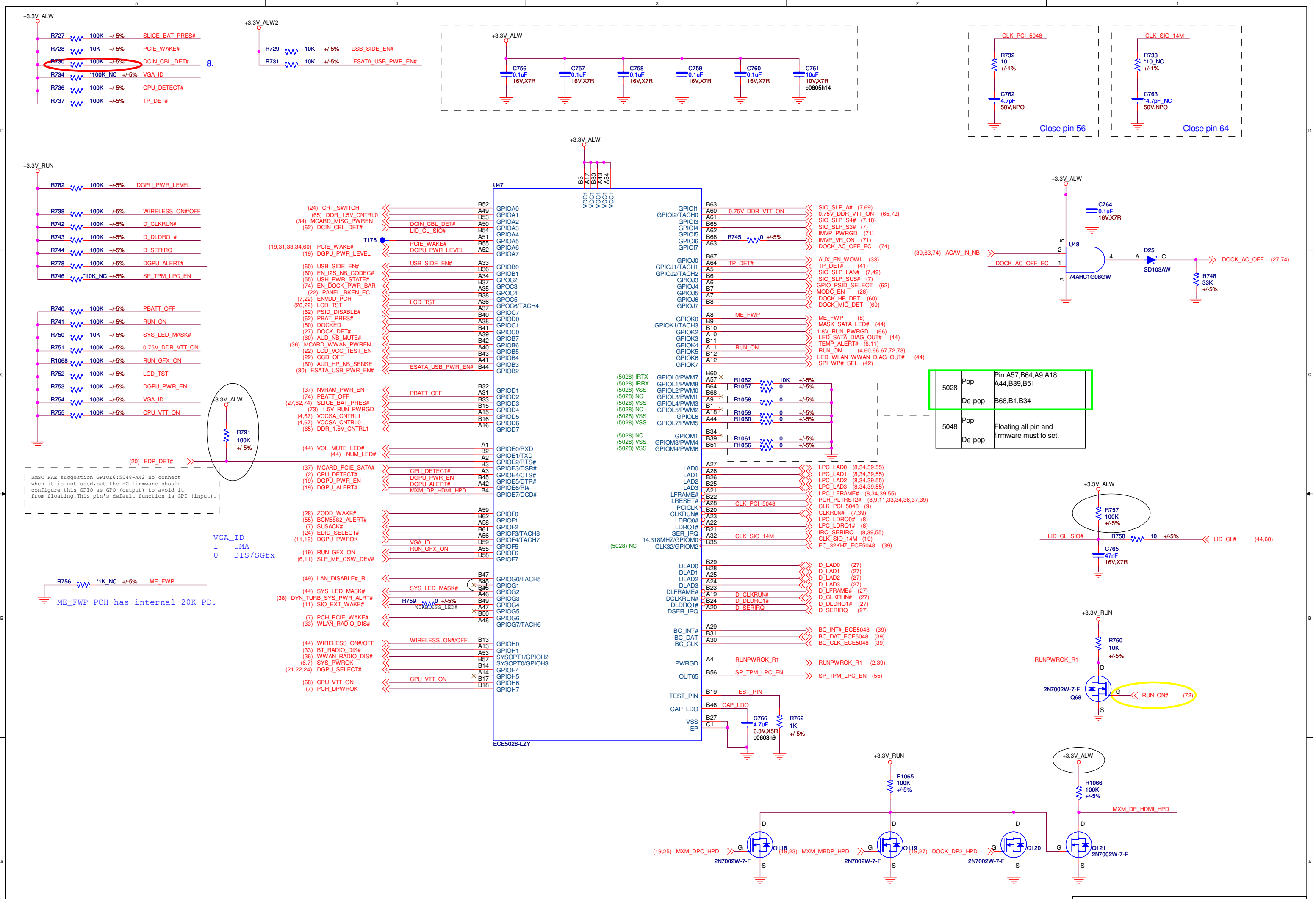

5028	Pop	Pin A57,B64,A9,A18 A44,B39,B51
	De-pop	B68,B1,B34
5048	Pop	Floating all pin and firmware must to set.
	De-pop	

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Title: 39 -- SIO (ECE5048)

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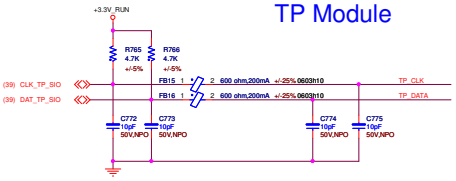
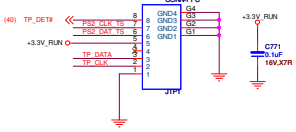
TP Module

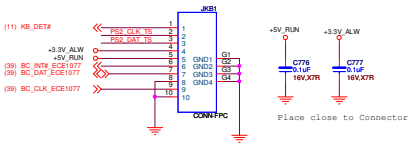


0524GC: CIS OK



Keyboard Module

1116 update to CIS



Place close to Connector

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Title	40 -- ECE1099+KB+TP	
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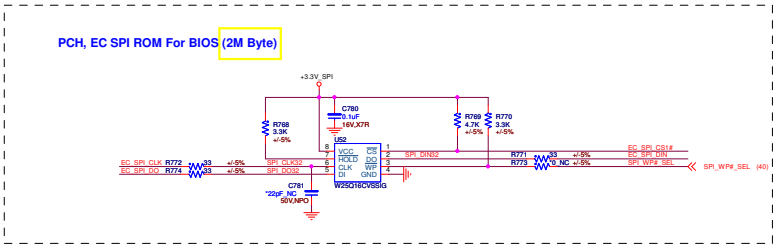

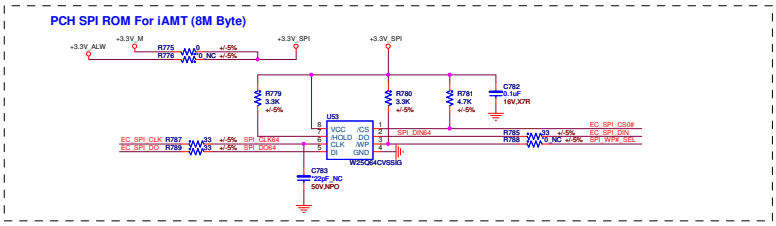

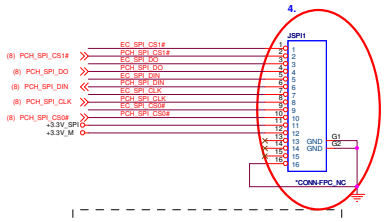

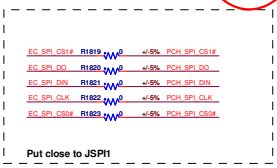

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Title	41 -- BIOS ROM(4M+8M)	
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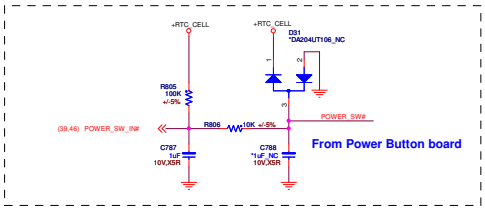
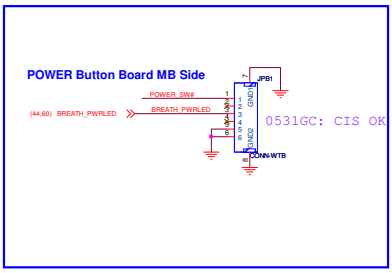
For AUX Module Conn

Remove AUX Module

7.





Ever Light Technology Limited		
Title	43 -- DB Connector x 7	
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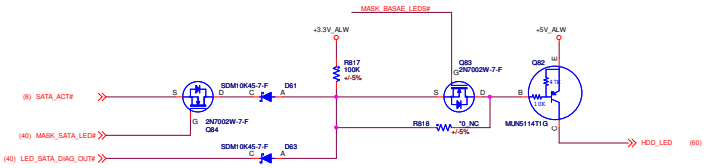
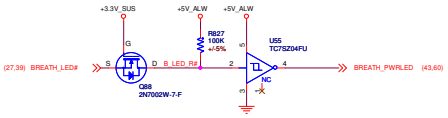
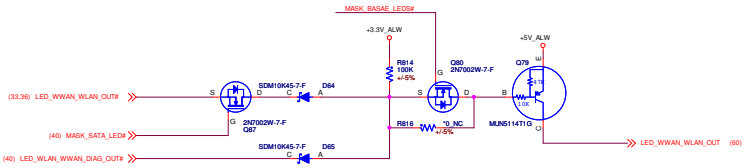
HDD

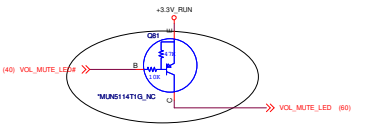


BREATH PWRLED

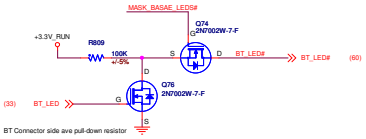


WWAN/WLAN

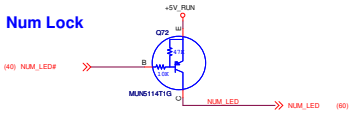




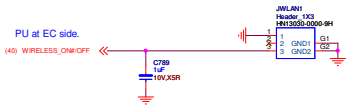
BT



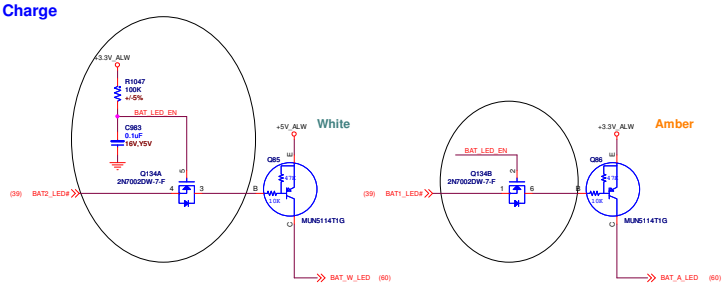
Num Lock

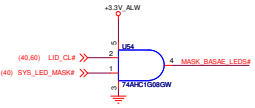


Wireless ON/OFF switch



Charge





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Title	44 -- LED+Control, Wirele	
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DS_0412: should be on touch Pad module.

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Title	45 -- Hall sensor	
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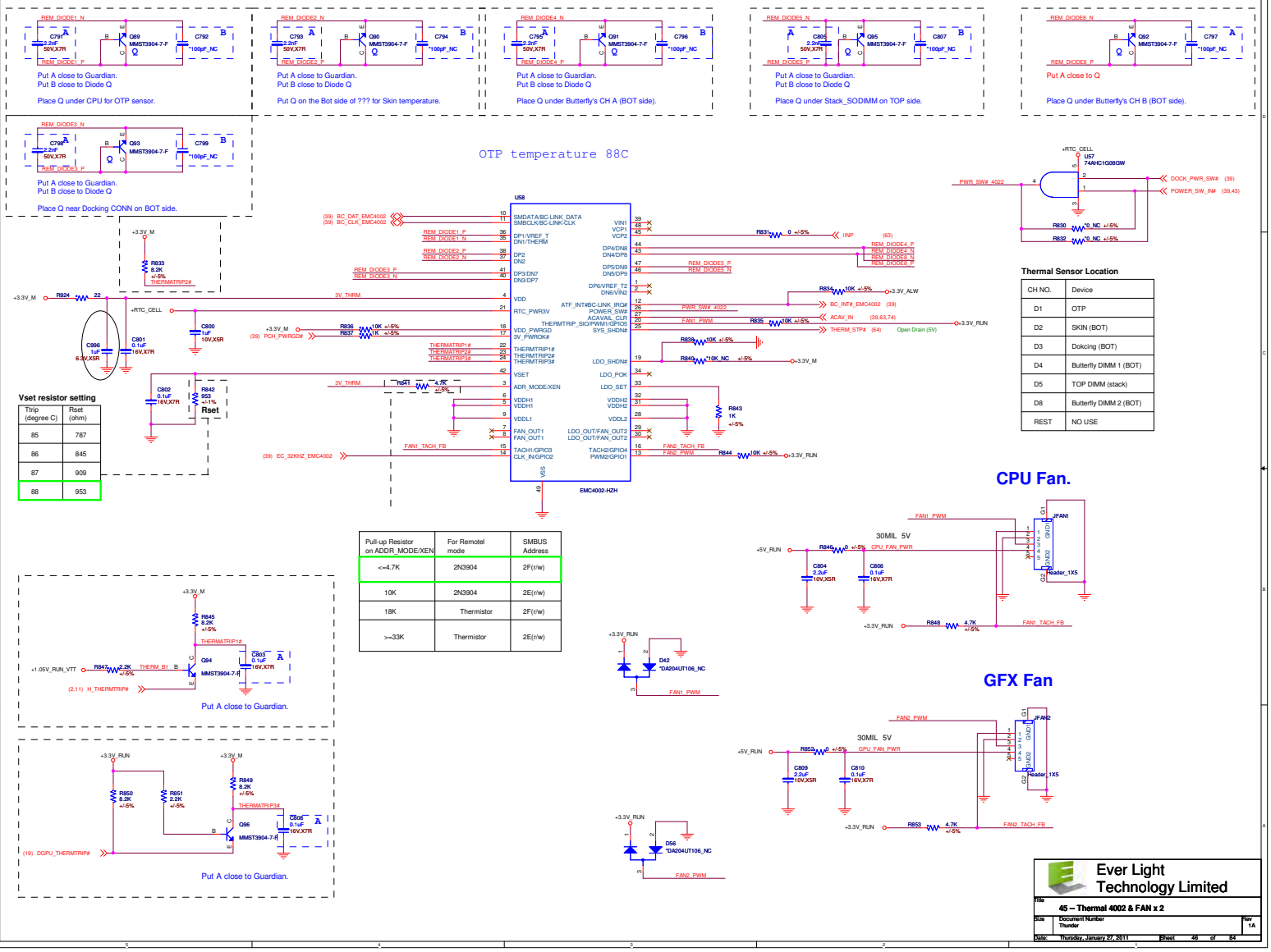
REM_DIODE1_N
C791 2.2nF 50V,X7R
Q89 MMST3904-7-F
C792 *100pF_NC
REM_DIODE1_P
Put A close to Guardian.
Put B close to Diode Q
Place Q under CPU for OTP sensor.
REM_DIODE2_N
C793 2.2nF 50V,X7R
Q90 MMST3904-7-F
C794 *100pF_NC
REM_DIODE2_P
Put A close to Guardian.
Put B close to Diode Q
Put Q on the Bot side of ??? for Skin temperature.
REM_DIODE4_N
C795 2.2nF 50V,X7R
Q91 MMST3904-7-F
C796 *100pF_NC
REM_DIODE4_P
Put A close to Guardian.
Put B close to Diode Q
Place Q under Butterfly's CH A (BOT side).
REM_DIODES_N
C805 2.2nF 50V,X7R
Q95 MMST3904-7-F
C807 *100pF_NC
REM_DIODES_P
Put A close to Guardian.
Put B close to Diode Q
Place Q under Stack_SODIMM on TOP side.
REM_DIODE8_N
C797
Q92 MMST3904-7-F
*100pF_NC
REM_DIODE8_P
Put A close to Q
Place Q under Butterfly's CH B (BOT side).
REM_DIODE3_N
C798 2.2nF 50V,X7R
Q93 MMST3904-7-F
C799 *100pF_NC
REM_DIODE3_P
Put A close to Guardian.
Put B close to Diode Q
Place Q near Docking CONN on BOT side.
OTP temperature 88C
U58
EMC4002-HZH
SMDATA/BC-LINK_DATA
SMBCLK/BC-LINK_CLK
DP1/VREF_T
DN1/THERM
DP2
DN2
DP3/DN7
DN3/DP7
VDD
RTC_PWR3V
VDD_PWRGD
3V_PWROK#
VSET
ADR_MODE/XEN
VDDH1
VDDL1
FAN_OUT1
FAN_OUT2
TACH1/GPIO3
CLK_IN/GPIO2
VIN1
VCP1
VCP2
DP4/DN8
DN4/DP8
DP5/DN9
DN5/DP9
DP6/VREF_T2
DN6/VIN2
ATF_INT#/BC-LINK_IRQ#
POWER_SW#
ACAVAIL_CLK
THERMTRIP_SIO/PWM1/GPIO5
SYS_SHDN#
LDO_SHDN#
LDO_POK
LDO_SET
VDDH2
VDDL2
LDO_OUT/FAN_OUT2
LDO_OUT/FAN_OUT3
TACH2/GPIO4
PWM2/GPIO1
VSS
(39) BC_DAT_EMC4002
(39) BC_CLK_EMC4002
REM_DIODE1_P
REM_DIODE1_N
REM_DIODE2_P
REM_DIODE2_N
REM_DIODE3_P
REM_DIODE3_N
REM_DIODE4_P
REM_DIODE4_N
REM_DIODE8_P
REM_DIODE8_N
REM_DIODES_P
REM_DIODES_N
3V_THRM
+RTC_CELL
+3.3V_M
(39) PCH_PWRGD#
(39) EC_32KHZ_EMC4002
FAN1_TACH_FB
FAN2_TACH_FB
FAN1_PWM
FAN2_PWM
THERMTRIP1#
THERMTRIP2#
THERMTRIP3#
R831 0 +/-5%
R832 *0_NC +/-5%
R833 8.2K +/-5%
R834 10K +/-5%
R835 10K +/-5%
R836 10K +/-5%
R837 1K +/-5%
R838 10K +/-5%
R839 10K +/-5%
R840 *10K_NC +/-5%
R841 4.7K +/-5%
R842 953 +/-1%
R843 1K +/-5%
R844 10K +/-5%
R924 22
C800 1uF 10V,X5R
C801 0.1uF 16V,X7R
C802 0.1uF 16V,X7R
C996 1uF 6.3V,X5R
U57 74AHC1G08GW
PWR_SW# 4022
DOCK_PWR_SW# (39)
POWER_SW_IN# (39,43)
R830 *0_NC +/-5%
R832 *0_NC +/-5%
Thermal Sensor Location
CH NO. | Device
D1 | OTP
D2 | SKIN (BOT)
D3 | Dokcing (BOT)
D4 | Butterfly DIMM 1 (BOT)
D5 | TOP DIMM (stack)
D8 | Butterfly DIMM 2 (BOT)
REST | NO USE
Vset resistor setting
Trip (degree C) | Rset (ohm)
85 | 787
86 | 845
87 | 909
88 | 953
Rset
Pull-up Resistor on ADDR_MODE/XEN | For Remotel mode | SMBUS Address
<=4.7K | 2N3904 | 2F(r/w)
10K | 2N3904 | 2E(r/w)
18K | Thermistor | 2F(r/w)
>=33K | Thermistor | 2E(r/w)
CPU Fan.
JFAN1
FAN1_PWM
30MIL 5V
+5V_RUN
R846 0 +/-5%
CPU_FAN_PWR
C804 2.2uF 10V,X5R
C806 0.1uF 16V,X7R
Header_1X5
R848 4.7K +/-5%
FAN1_TACH_FB
D42 *DA204UT106_NC
GFX Fan
JFAN2
FAN2_PWM
R852 0 +/-5%
GPU_FAN_PWR
C809 2.2uF 10V,X5R
C810 0.1uF 16V,X7R
R853 4.7K +/-5%
FAN2_TACH_FB
D56 *DA204UT106_NC
R845 8.2K +/-5%
THERMATRIP1#
+1.05V_RUN_VTT
R847 2.2K +/-5%
THERM_B1
Q94 MMST3904-7-F
C803 0.1uF 16V,X7R
(2,11) H_THERMTRIP#
Put A close to Guardian.
R849 8.2K +/-5%
THERMATRIP3#
R850 8.2K +/-5%
R851 2.2K +/-5%
Q96 MMST3904-7-F
C804 0.1uF 16V,X7R
(19) DGPU_THERMTRIP#
Put A close to Guardian.
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Title: 45 -- Thermal 4002 & FAN x 2
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Title	47 -- AUDIO(92HD90B)+SPK+JACK	
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Title	48 -- AUDIO for Docking+Crystal		
Size	Document Number Thunder		Rev 1A
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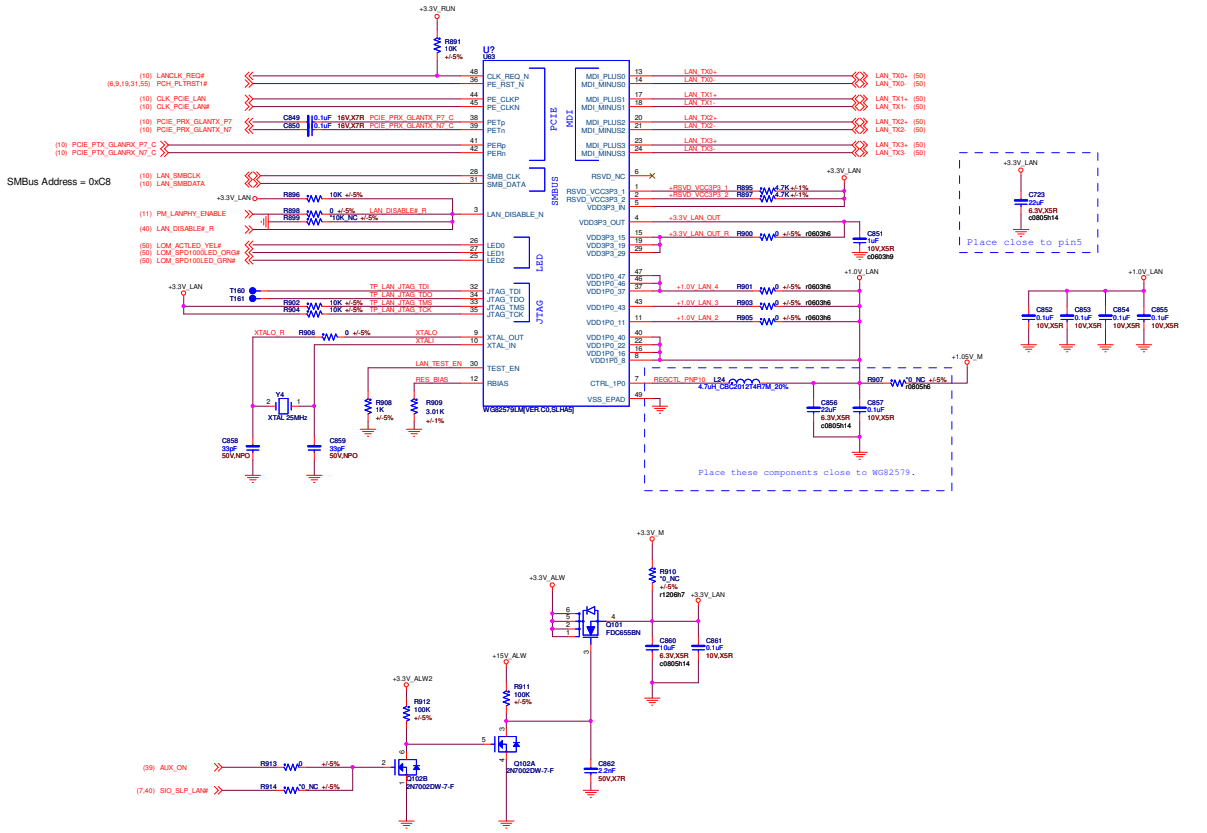

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Title	48 -- LOM 82579	
Size	Document Number: Thunder	Rev: 1A
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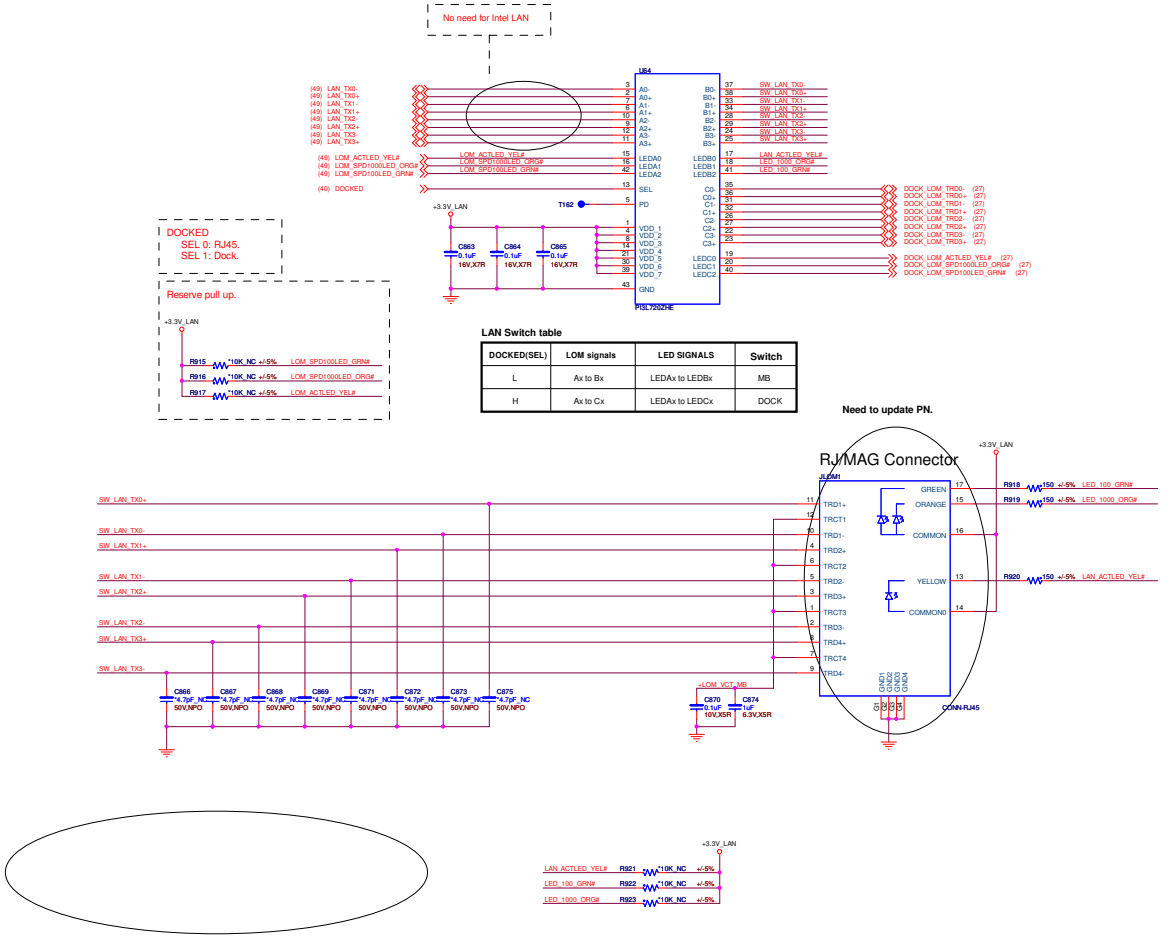

LAN Switch table

DOCKED(SEL)	LOM signals	LED SIGNALS	Switch
L	Ax to Bx	LEDAx to LEDBx	MB
H	Ax to Cx	LEDAx to LEDCx	DOCK

Need to update PN.

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Title	49 -- RJ45+MID, MUX Switch	
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Title	50 – TPM for China	
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Title	51 -- Card Reader & Conn	
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Title	52 – 15" 1394 Conn	
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Title	53 – 17" 1394 Conn+ Power	
Size	Document Number Thunder	Rev 1A
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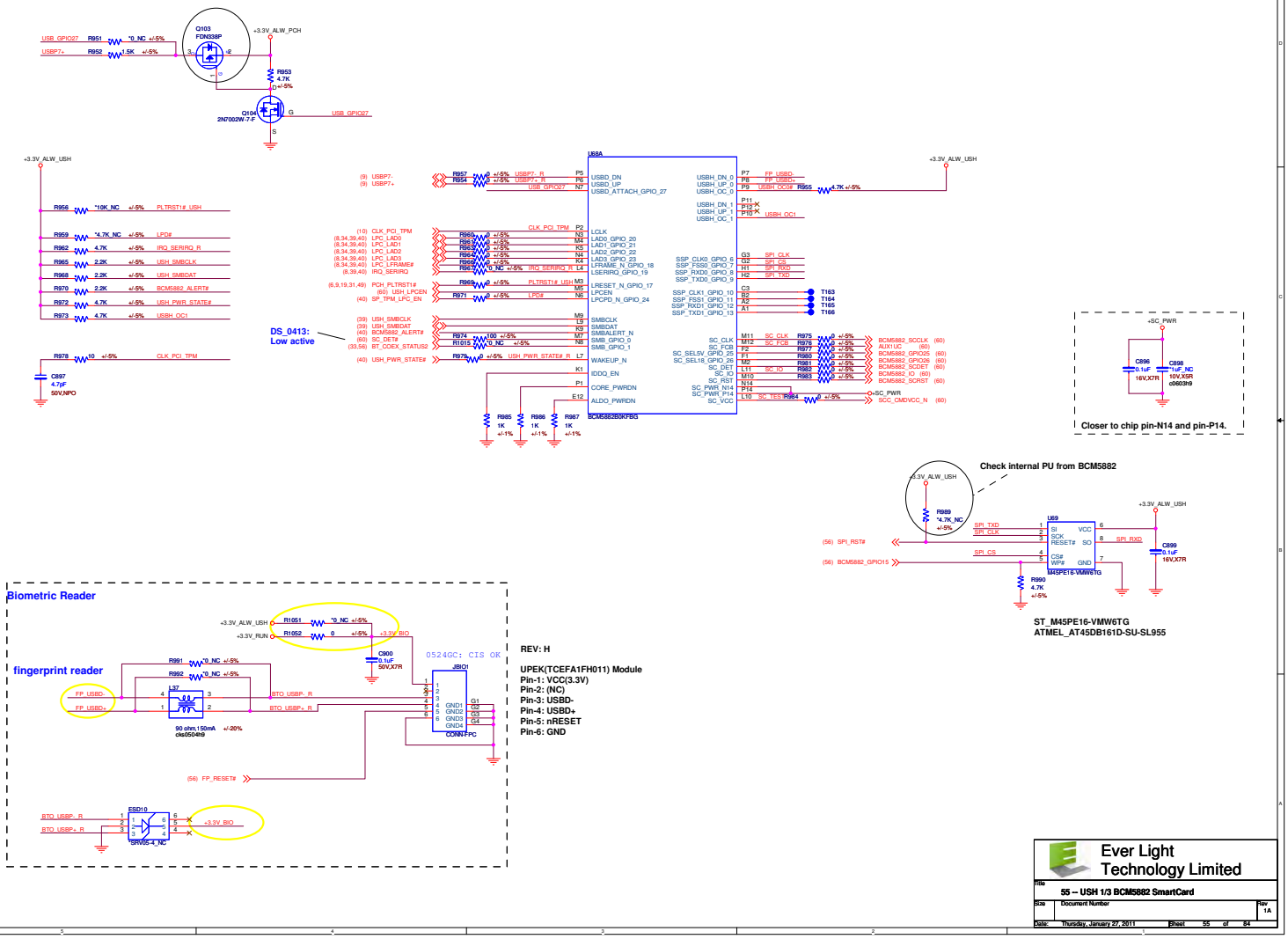
Q103
FDN338P
+3.3V_ALW_PCH
USB_GPIO27
R951 *0_NC +/-5%
USBP7+
R952 1.5K +/-5%
R953 4.7K +/-5%
Q104
2N7002W-7-F
USB_GPIO27
+3.3V_ALW_USH
R956 *10K_NC +/-5% PLTRST1#_USH
R959 *4.7K_NC +/-5% LPD#
R962 4.7K +/-5% IRQ_SERIRQ_R
R965 2.2K +/-5% USH_SMBCLK
R968 2.2K +/-5% USH_SMBDAT
R970 2.2K +/-5% BCM5882_ALERT#
R972 4.7K +/-5% USH_PWR_STATE#
R973 4.7K +/-5% USBH_OC1
R978 *10 +/-5% CLK_PCI_TPM
C897 4.7pF 50V,NPO
DS_0413:
Low active
U68A
BCM5882B0KFBG
USBD_DN
USBD_UP
USBD_ATTACH_GPIO_27
LCLK
LAD0_GPIO_20
LAD1_GPIO_21
LAD2_GPIO_22
LAD3_GPIO_23
LFRAME_N_GPIO_18
LSERIRQ_GPIO_19
LRESET_N_GPIO_17
LPCPD_N_GPIO_24
SMBCLK
SMBDAT
SMBALERT_N
SMB_GPIO_0
SMB_GPIO_1
WAKEUP_N
IDDQ_EN
CORE_PWRDN
ALDO_PWRDN
SSP_CLK0_GPIO_6
SSP_FSS0_GPIO_7
SSP_RXD0_GPIO_8
SSP_TXD0_GPIO_9
SSP_CLK1_GPIO_10
SSP_FSS1_GPIO_11
SSP_RXD1_GPIO_12
SSP_TXD1_GPIO_13
SC_CLK
SC_FCB
SC_SEL5V_GPIO_25
SC_SEL18_GPIO_26
SC_DET
SC_IO
SC_RST
SC_PWR_N14
SC_PWR_P14
SC_VCC
SC_TES
R985 1K +/-1%
R986 1K +/-1%
R987 1K +/-1%
R957 0 +/-5%
R954 0 +/-5%
R960 0 +/-5%
R961 0 +/-5%
R963 0 +/-5%
R964 0 +/-5%
R966 0 +/-5%
R967 *0_NC +/-5%
R969 0 +/-5%
R971 0 +/-5%
R974 100 +/-5%
R1015 *0_NC +/-5%
R975 0 +/-5%
R976 0 +/-5%
R977 0 +/-5%
R980 0 +/-5%
R981 0 +/-5%
R982 0 +/-5%
R983 0 +/-5%
R984 0 +/-5%
R955 4.7K +/-5%
+SC_PWR
SCC_CMDVCC_N
Closer to chip pin-N14 and pin-P14.
C896 0.1uF 16V,X7R
C898 1uF_NC 10V,X5R
Check internal PU from BCM5882
R989 *4.7K_NC +/-5%
U69
M45PE16-VMW6TG
R990 4.7K +/-5%
C899 0.1uF 16V,X7R
ST_M45PE16-VMW6TG
ATMEL_AT45DB161D-SU-SL955
Biometric Reader
fingerprint reader
R1051 *0_NC +/-5%
R1052 0 +/-5%
C900 0.1uF 50V,X7R
0524GC: CIS OK
R991 *0_NC +/-5%
R992 *0_NC +/-5%
L37
90 ohm,150mA +/-20%
JBIO1
CONN-FPC
ESD10
SRV05-4_NC
REV: H
UPEK(TCEFA1FH011) Module
Pin-1: VCC(3.3V)
Pin-2: (NC)
Pin-3: USBD-
Pin-4: USBD+
Pin-5: nRESET
Pin-6: GND
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JTAG_TDI_USH R994 *0_NC +/-5% JTAG_CLK_USH

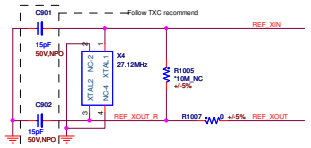
JTAG_TMS_USH R995 *0_NC +/-5% JTAG_TDO_USH

JTCE_USH R996 *0_NC +/-5% JTAG_RST#_USH

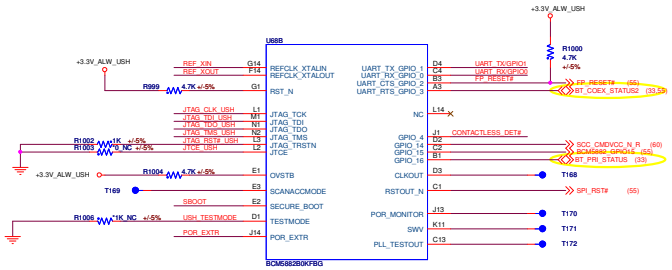
HF_RX_TEST1 R997 *0_NC +/-5% HF_RX_TEST0

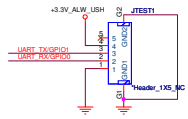
HF_RX_TEST3 R998 *0_NC +/-5% HF_RX_TEST2

27.12Mhz regardless support RFID or not.



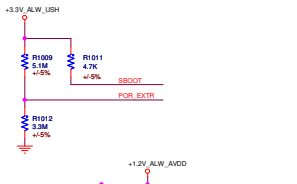
* XTAL CIRCUIT (COMPONENTS + WIRING) SHOULD BE ON TOP LAYER ONLY, TO CONTROL INTERFERENCE

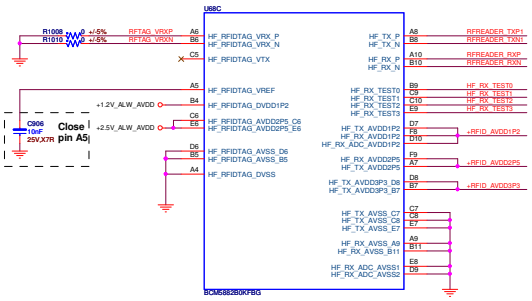


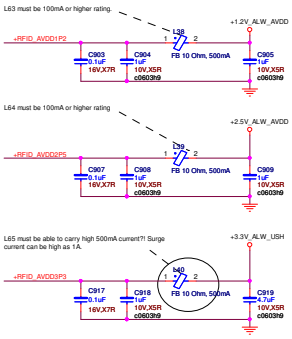


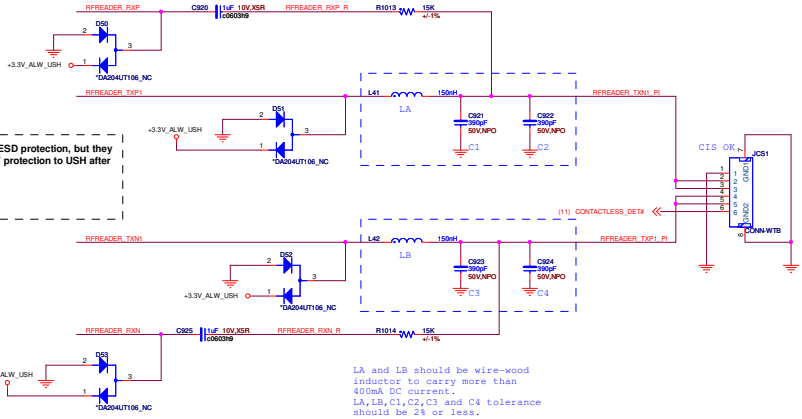
UART_TX/GPIO1, UART_RX_GPIO0, 3.3V_ALW_USH and GND to a connector. This is required for BIOS/FW debugging and EVMCo certification test.

Connector should be placed in place to be easy access by opening cover. Connector can be depop for production.









BRCM : D87, D88, D89, D90 are required for ESD protection, but they could be removed if ODM can guarantee 8kV protection to USH after contacted ESD test.

Note: USH only protect upto 2kV at I/O pins.

LA and LB should be wire-wood inductor to carry more than 400mA DC current.
LA,LB,C1,C2,C3 and C4 tolerance should be 2% or less.

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Title	56 -- USH 2/3 BCM5882 RFID	
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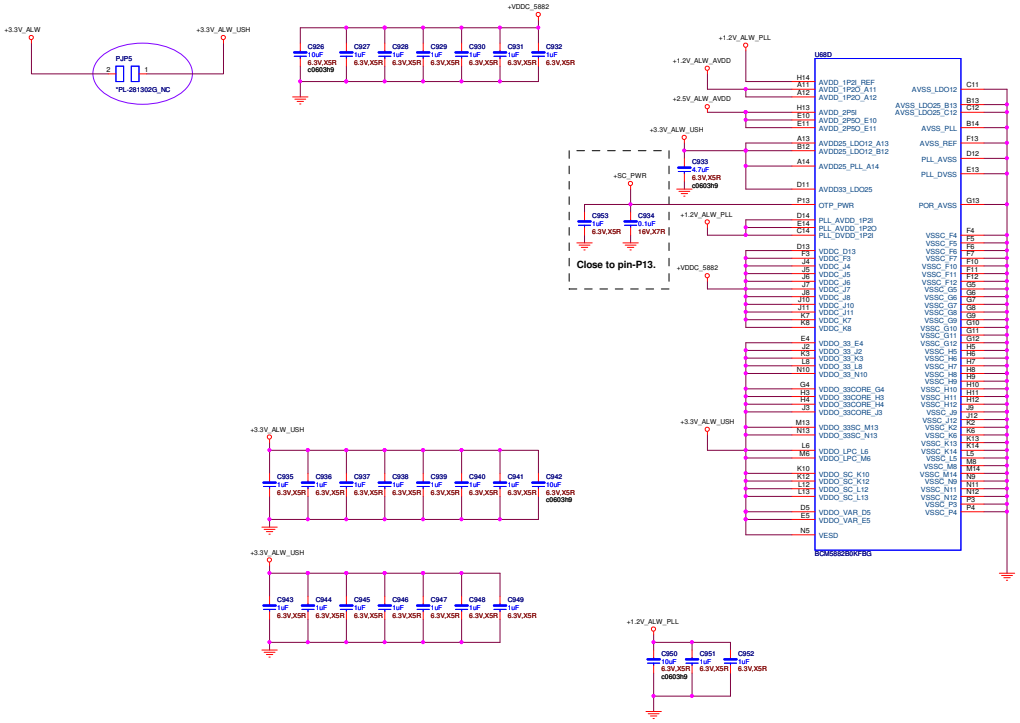

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Title	57 -- USH 3/3 BCM5882 Power	
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Title: 58 -- Smart Card IC & Conn

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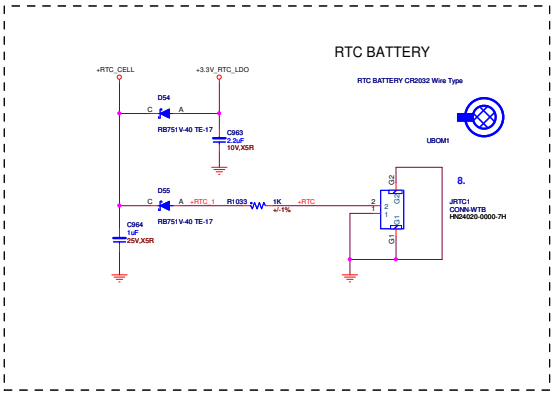

Ever Light Technology Limited

Title	58 -- System Reset, RTC	
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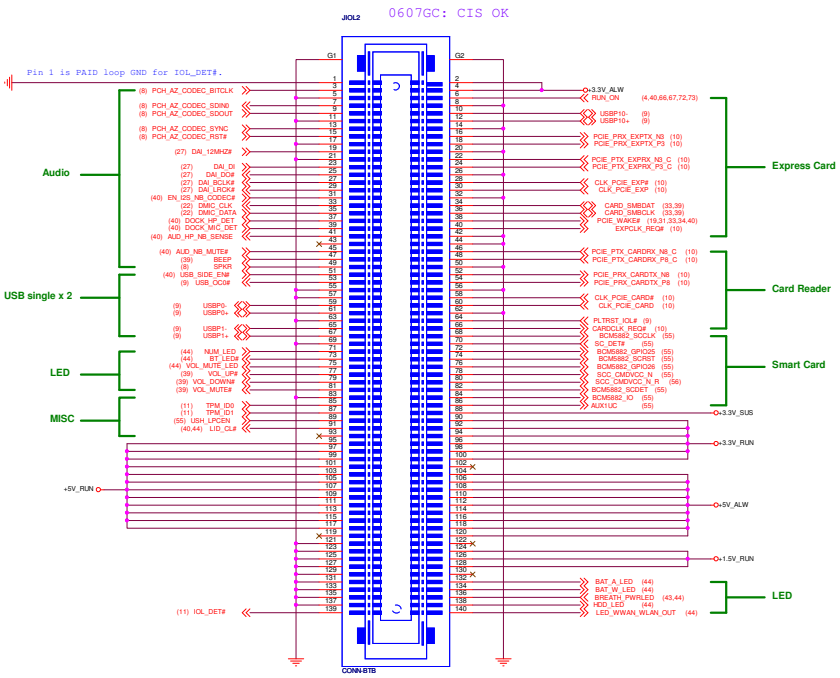

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Title	76 -- Blank Page	
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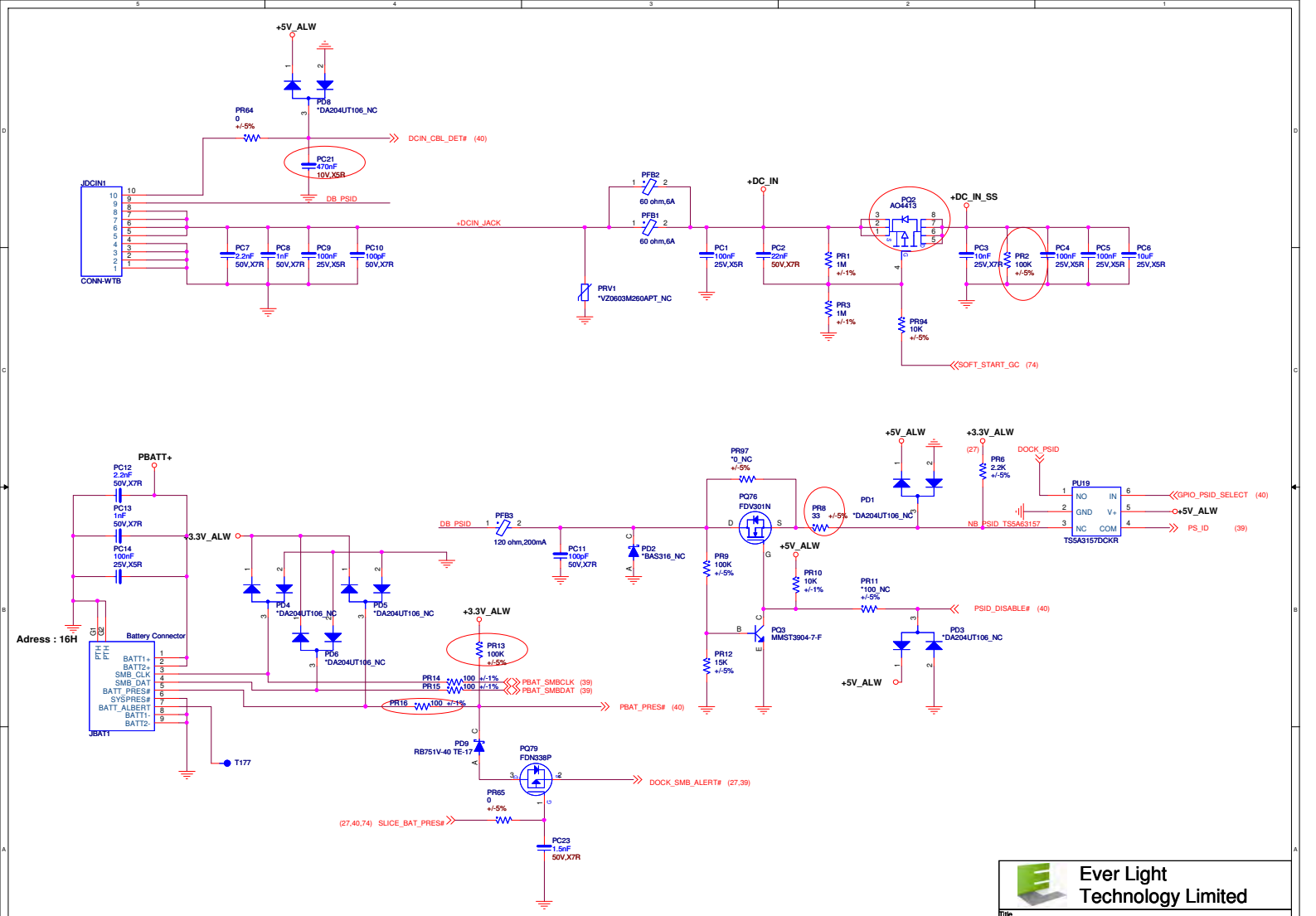

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Title	PW_DCin & Batt	
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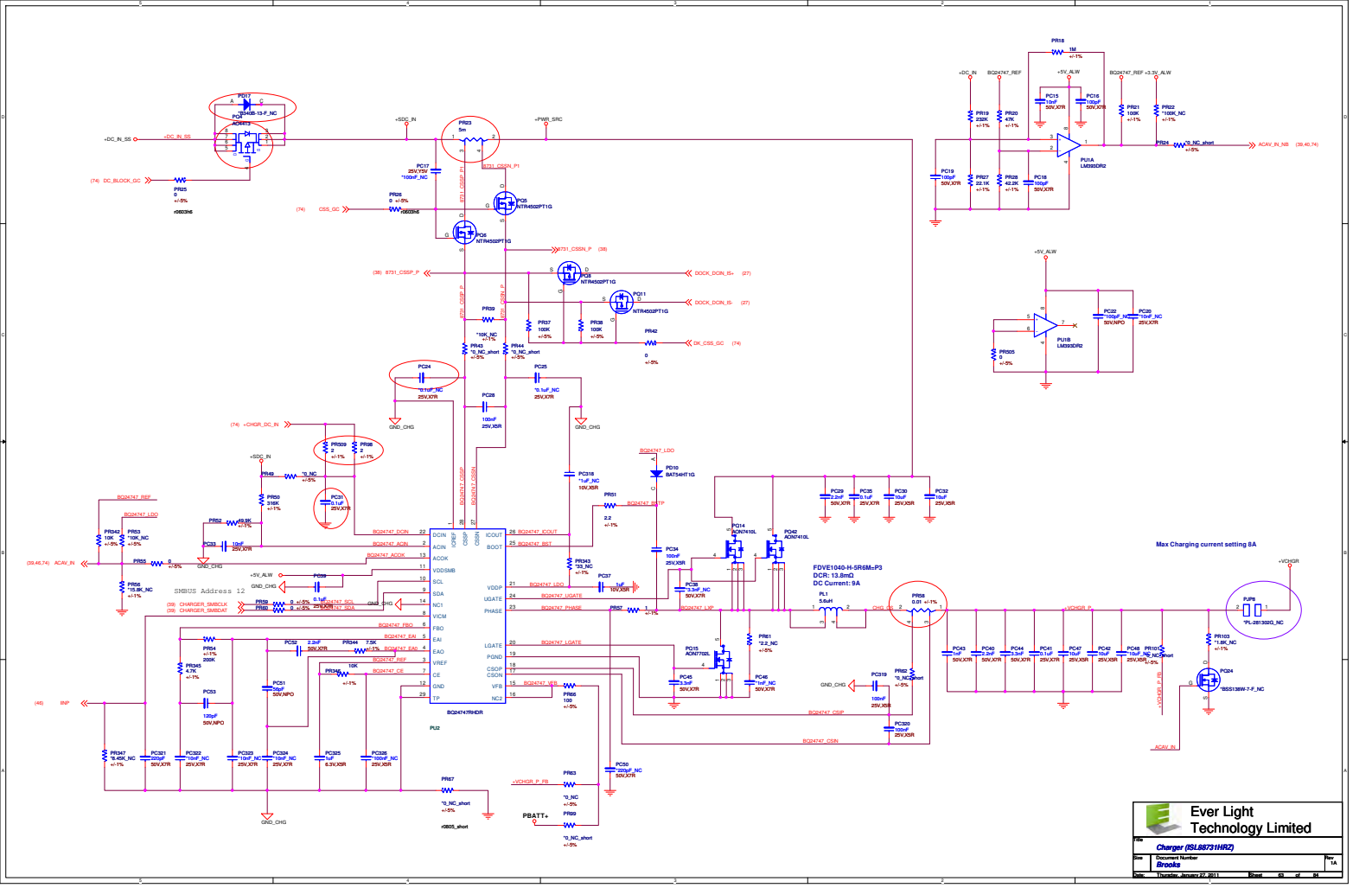
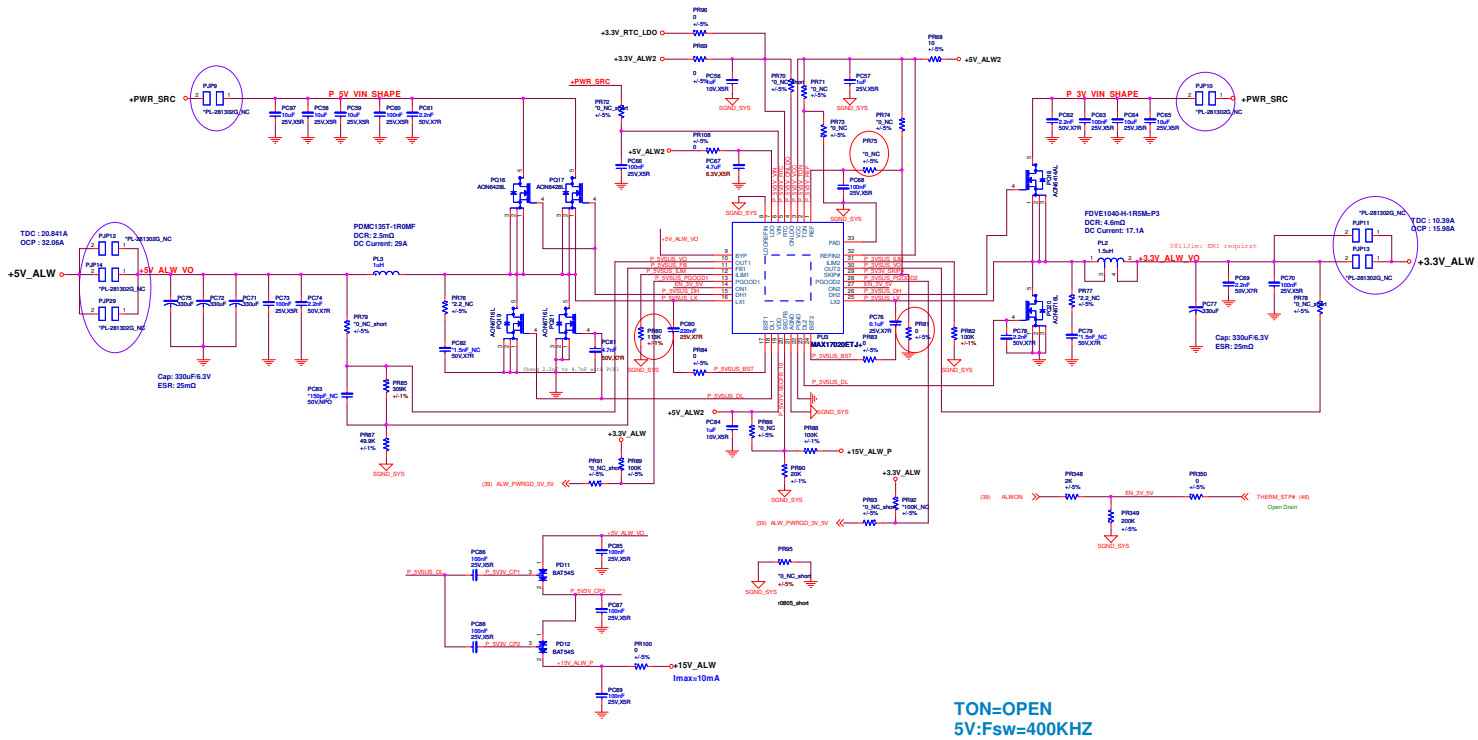

Max Charging current setting 8A
FDVE1040-H-5R6M=P3
DCR: 13.8mΩ
DC Current: 9A
SMBUS Address 12
BQ24747RHDR
Ever Light Technology Limited
Charger (ISL88731HRZ)
Brooks
Thursday, January 27, 2011

+5V_ALW / +3.3V_ALW POWER SUPPLY



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File	PW_SYSTEM(MAX17020)
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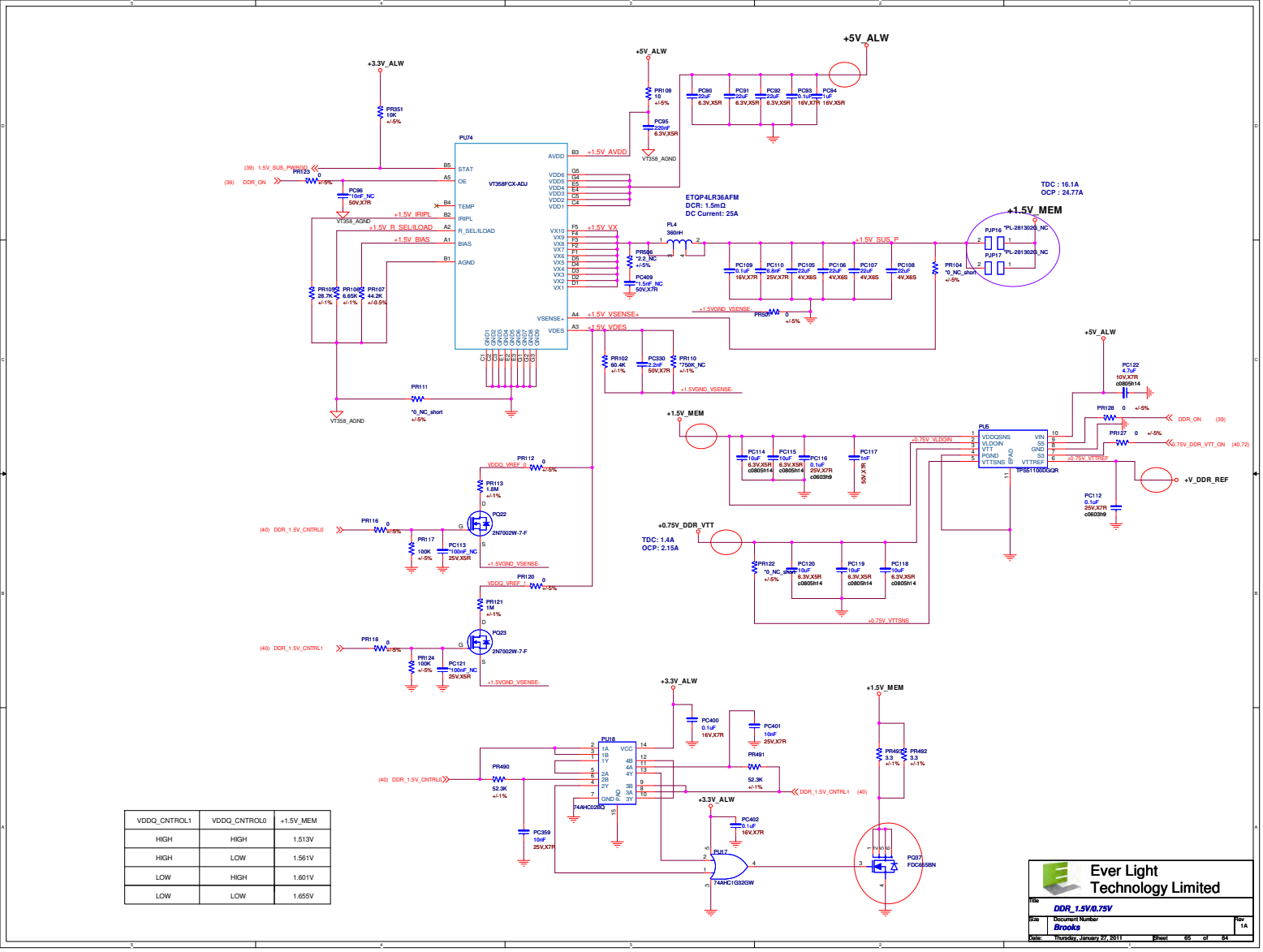

VDDQ_CNTROL1	VDDQ_CNTROL0	+1.5V_MEM
HIGH	HIGH	1.513V
HIGH	LOW	1.561V
LOW	HIGH	1.601V
LOW	LOW	1.655V

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Title	DDR_1.5V/0.75V	
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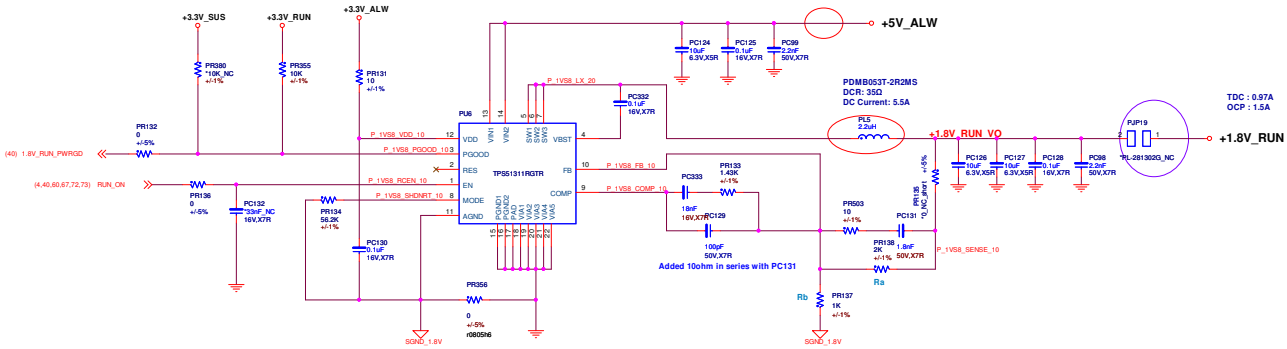
+1.8V_RUN POWER SUPPLY



<Variant Name>

Ever Light Technology Limited

Title	PW_SW_+1.8V(TPS51311)	
Size	Document Number: Brooks	Rev: 1A
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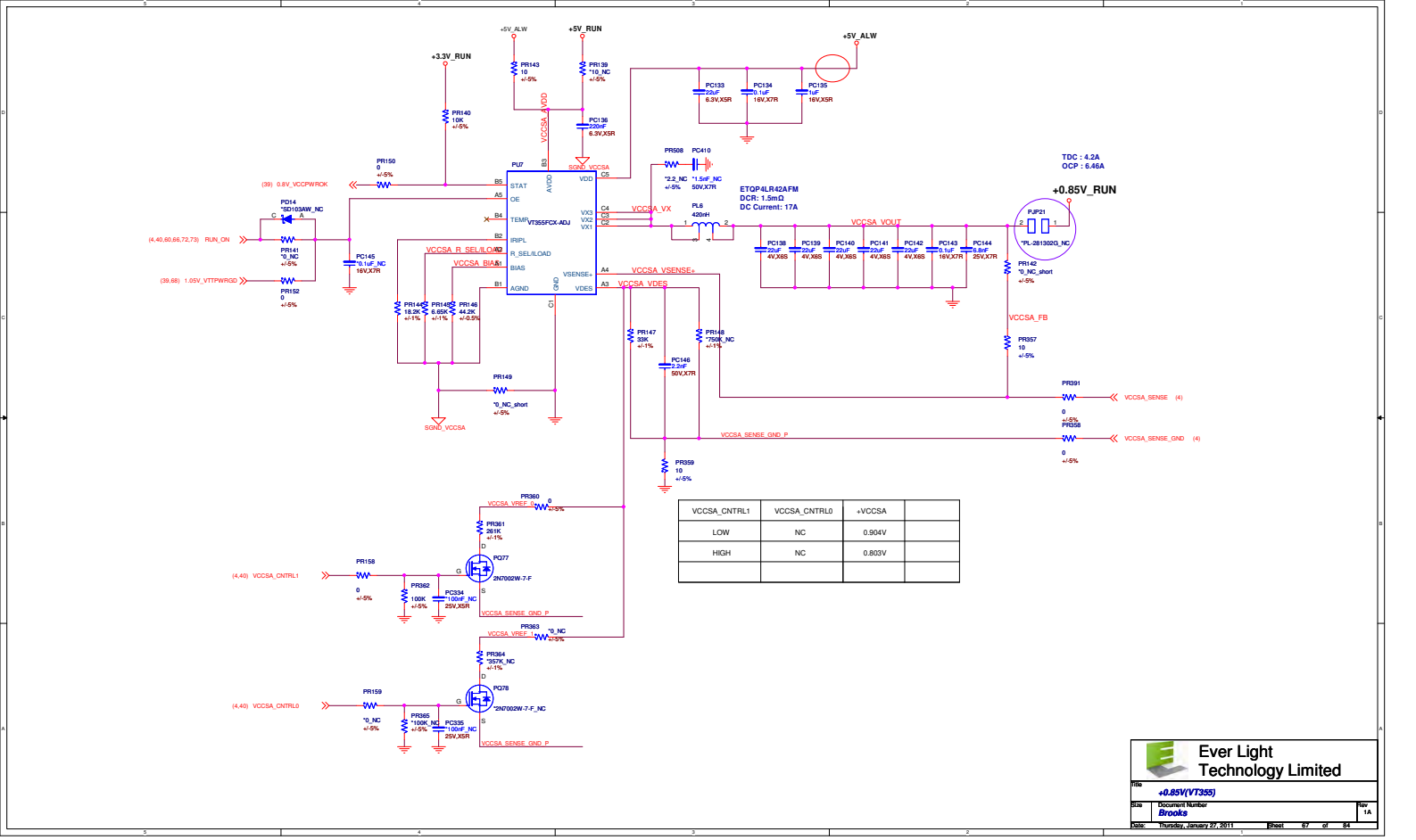

VCCSA_CNTRL1	VCCSA_CNTRL0	+VCCSA	
LOW	NC	0.904V	
HIGH	NC	0.803V	

Ever Light Technology Limited

Title	+0.85V(VT355)	
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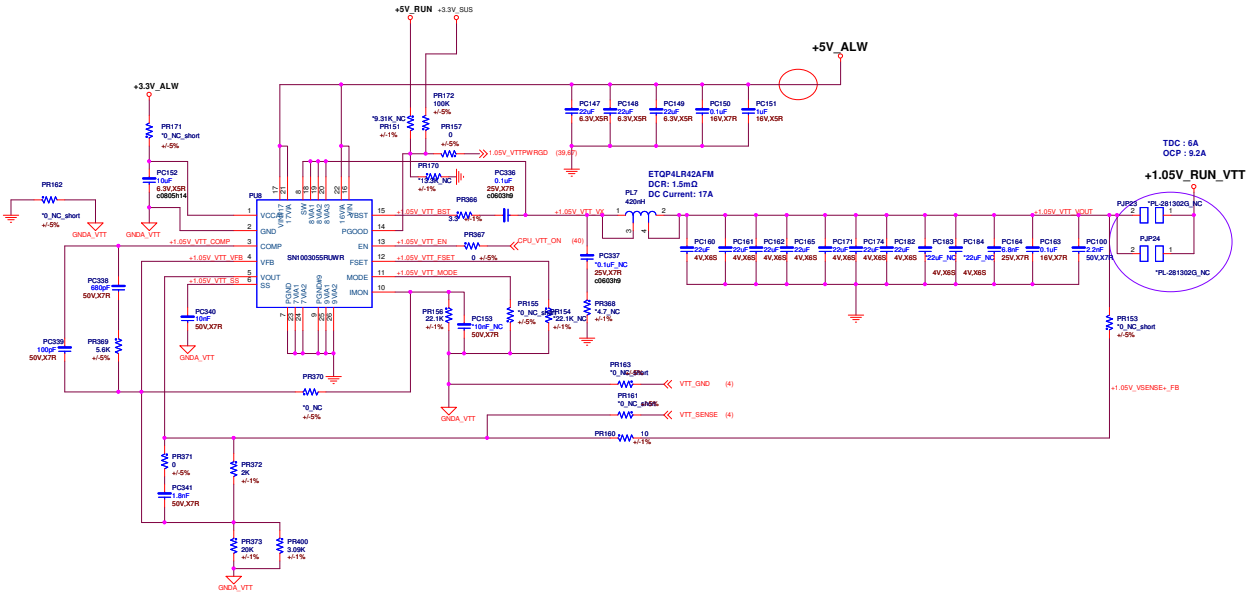

Ever Light Technology Limited

Title	PW_+1.05V_VTT(SN1003055RUWR)	
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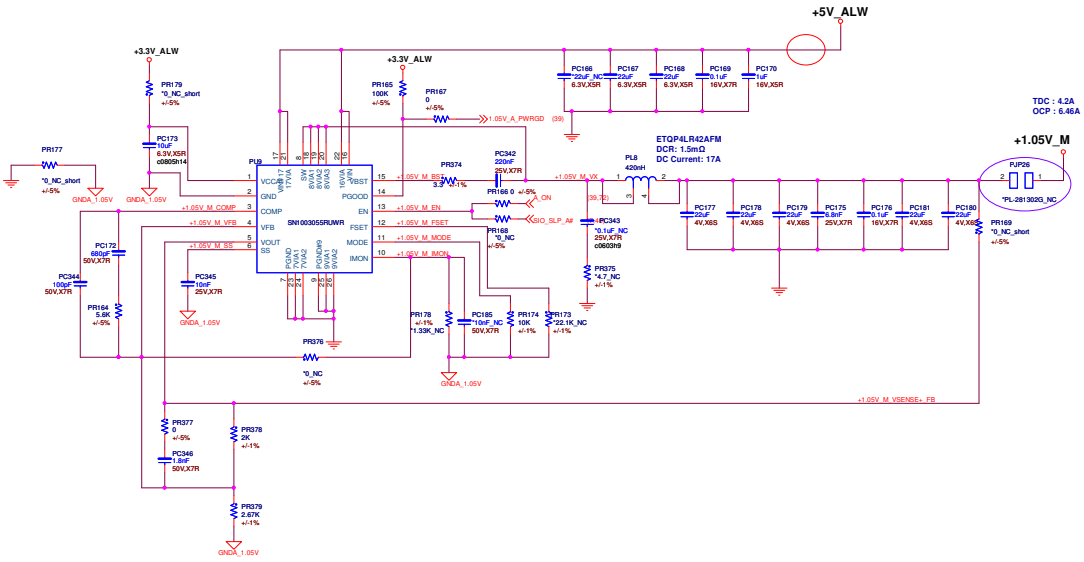

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Title	PW_+1.05VM(VT355)	
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Title	<Title>
Size: A	Document Number: <Doc>
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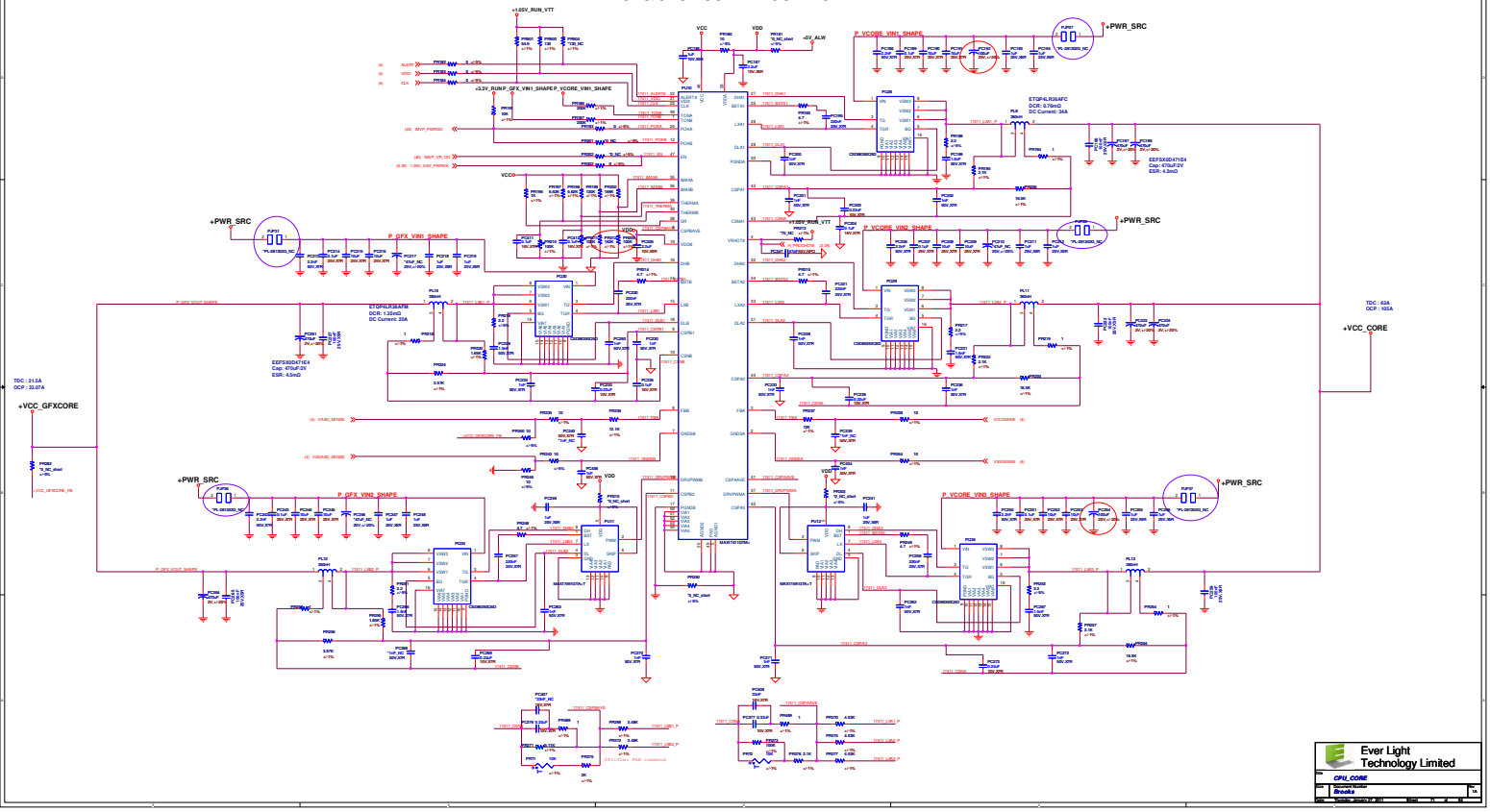
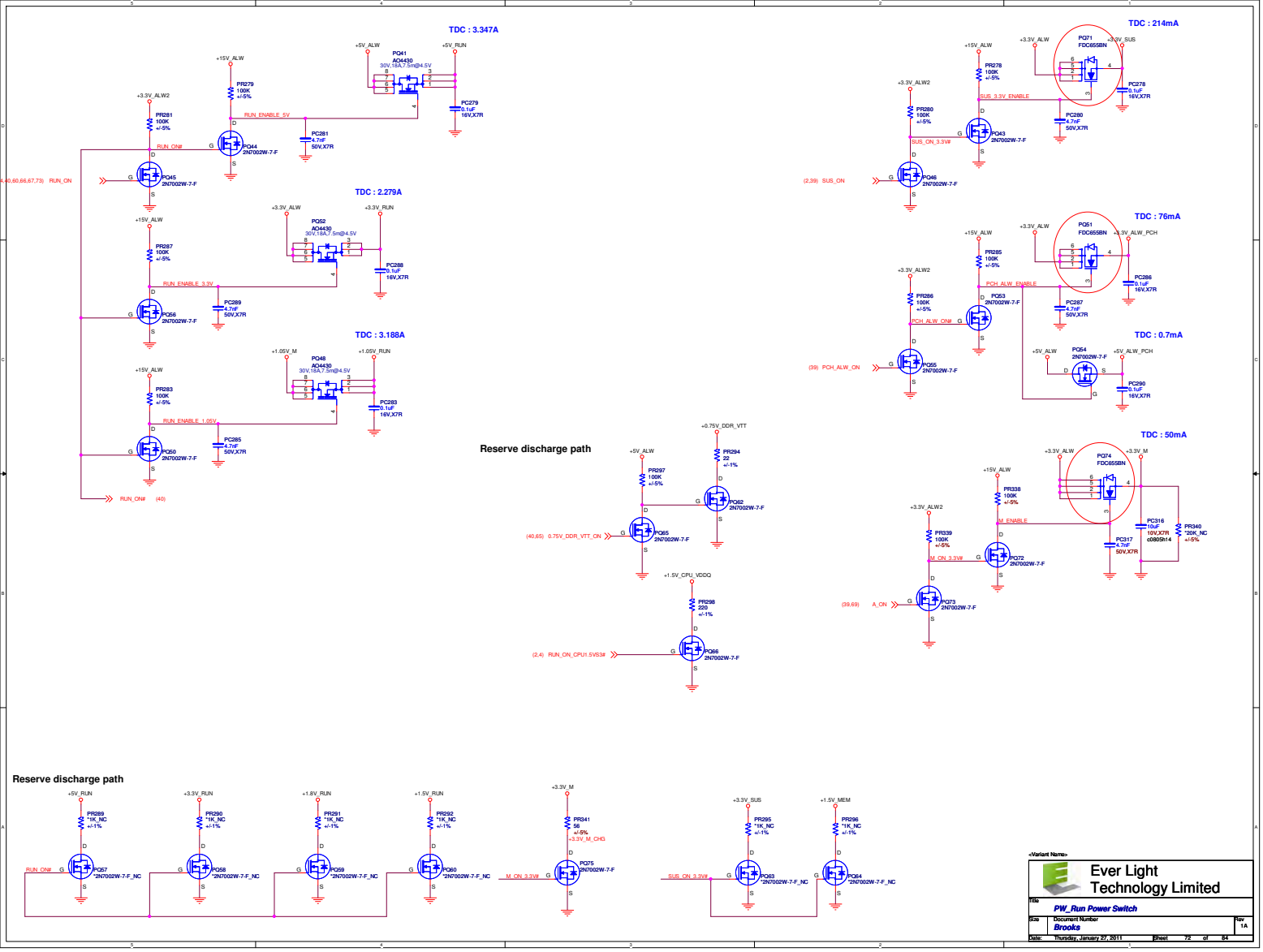
IMVP7 CPU/GPU VCORE REGULATOR




TDC : 3.347A
TDC : 214mA
TDC : 2.279A
TDC : 76mA
TDC : 3.188A
TDC : 0.7mA
TDC : 50mA
Reserve discharge path
Reserve discharge path
PQ41 AO4430 30V,18A,7.5m@4.5V
PQ51 FDC655BN
PQ52 AO4430 30V,18A,7.5m@4.5V
PQ54 2N7002W-7-F
PQ48 AO4430 30V,18A,7.5m@4.5V
PQ74 FDC655BN
PQ43 2N7002W-7-F
PQ44 2N7002W-7-F
PQ45 2N7002W-7-F
PQ46 2N7002W-7-F
PQ53 2N7002W-7-F
PQ55 2N7002W-7-F
PQ56 2N7002W-7-F
PQ50 2N7002W-7-F
PQ62 2N7002W-7-F
PQ65 2N7002W-7-F
PQ66 2N7002W-7-F
PQ72 2N7002W-7-F
PQ73 2N7002W-7-F
PQ57 *2N7002W-7-F_NC
PQ58 *2N7002W-7-F_NC
PQ59 *2N7002W-7-F_NC
PQ60 *2N7002W-7-F_NC
PQ75 2N7002W-7-F
PQ63 *2N7002W-7-F_NC
PQ64 2N7002W-7-F_NC
RUN_ENABLE_5V
RUN_ON#
RUN_ENABLE_3.3V
RUN_ENABLE_1.05V
SUS_3.3V_ENABLE
PCH_ALW_ON#
M_ENABLE
SUS_ON_3.3V#
M_ON_3.3V#
+3.3V_M_CHG
RUN_ON# (40)
(40,60,66,67,73) RUN_ON
(2,39) SUS_ON
(39) PCH_ALW_ON
(40,65) 0.75V_DDR_VTT_ON
(2,4) RUN_ON_CPU1.5VS3#
(39,69) A_ON

<Variant Name>
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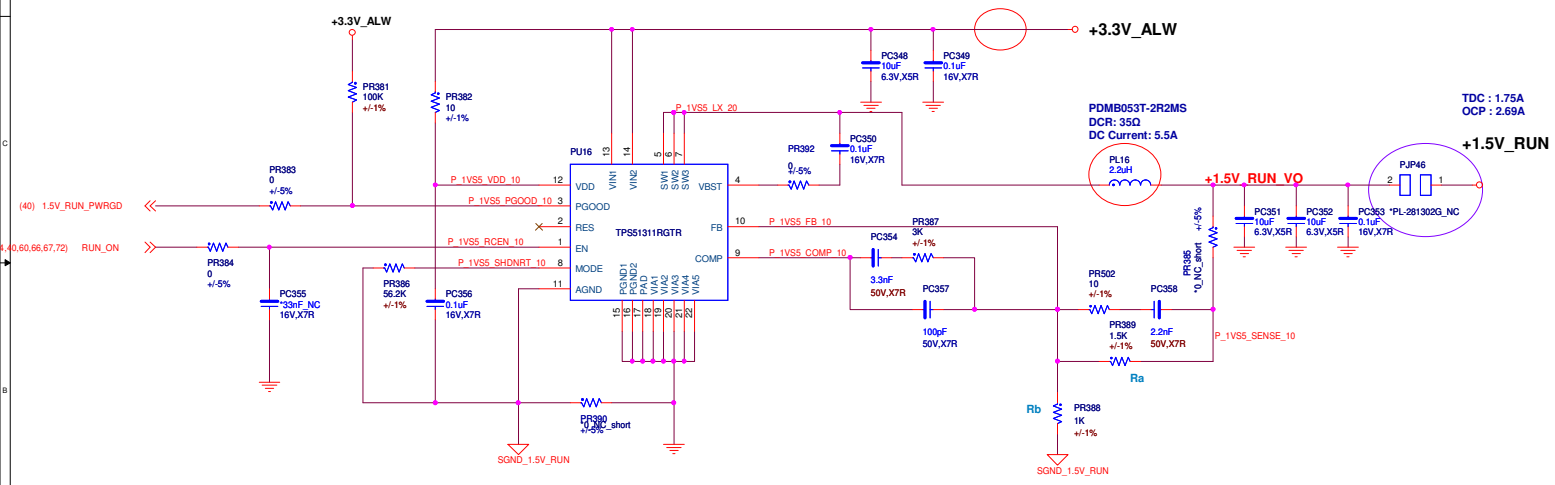
+1.5V_RUN POWER SUPPLY



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Title	PW_SW_+1.8V(TPS51311)	
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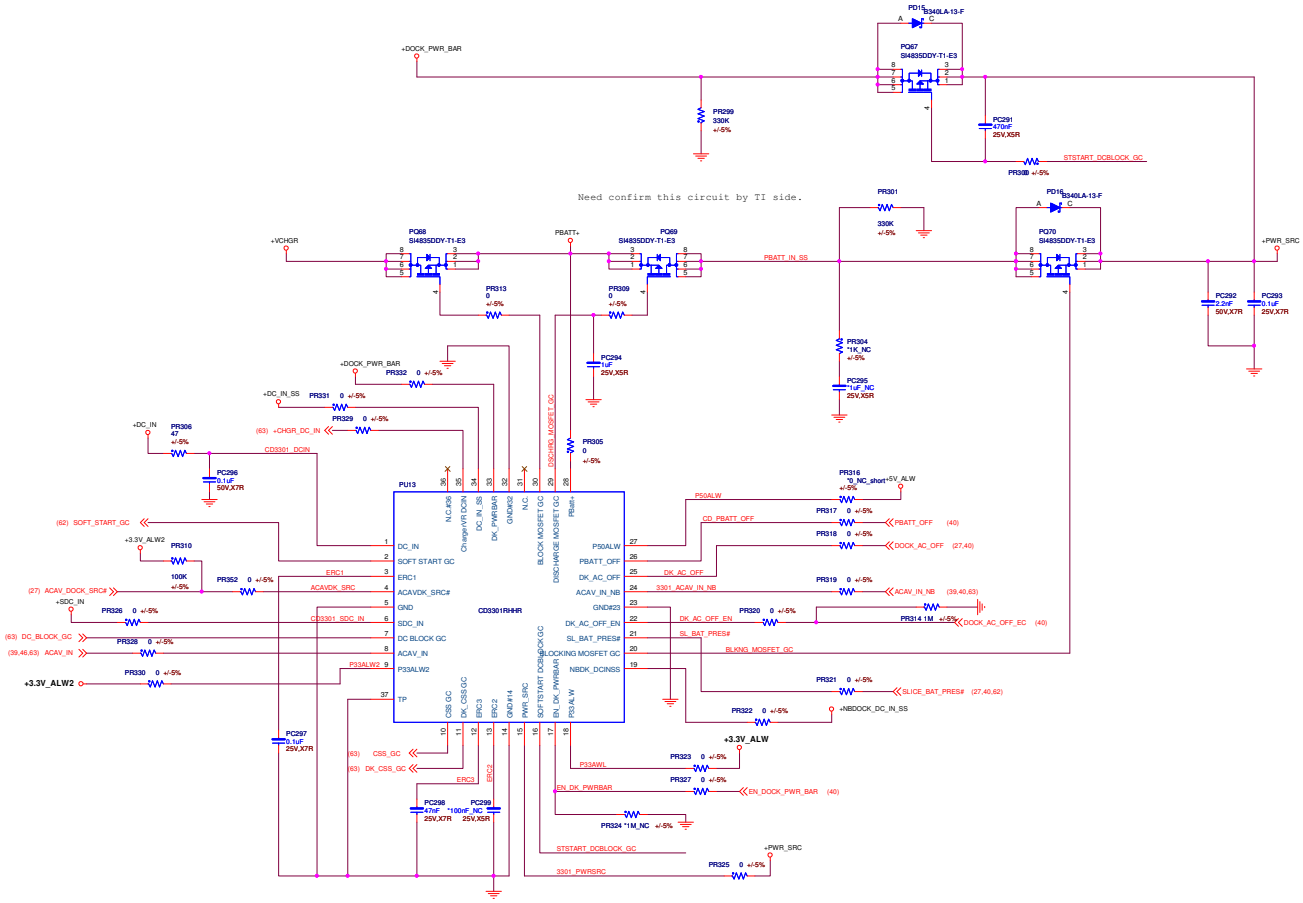

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Title	Docking Selector(CD3301)	
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Title
+12V_1394(MAX688)

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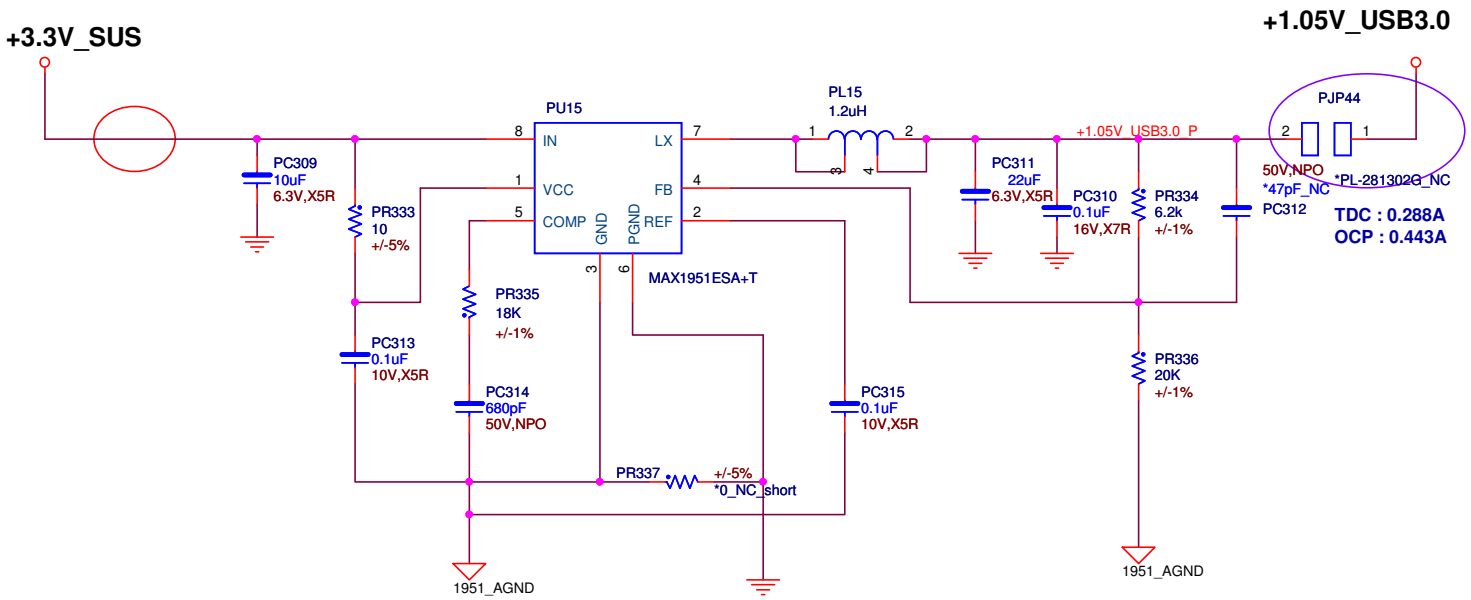

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Title	*+1.05V_USB3.0*	
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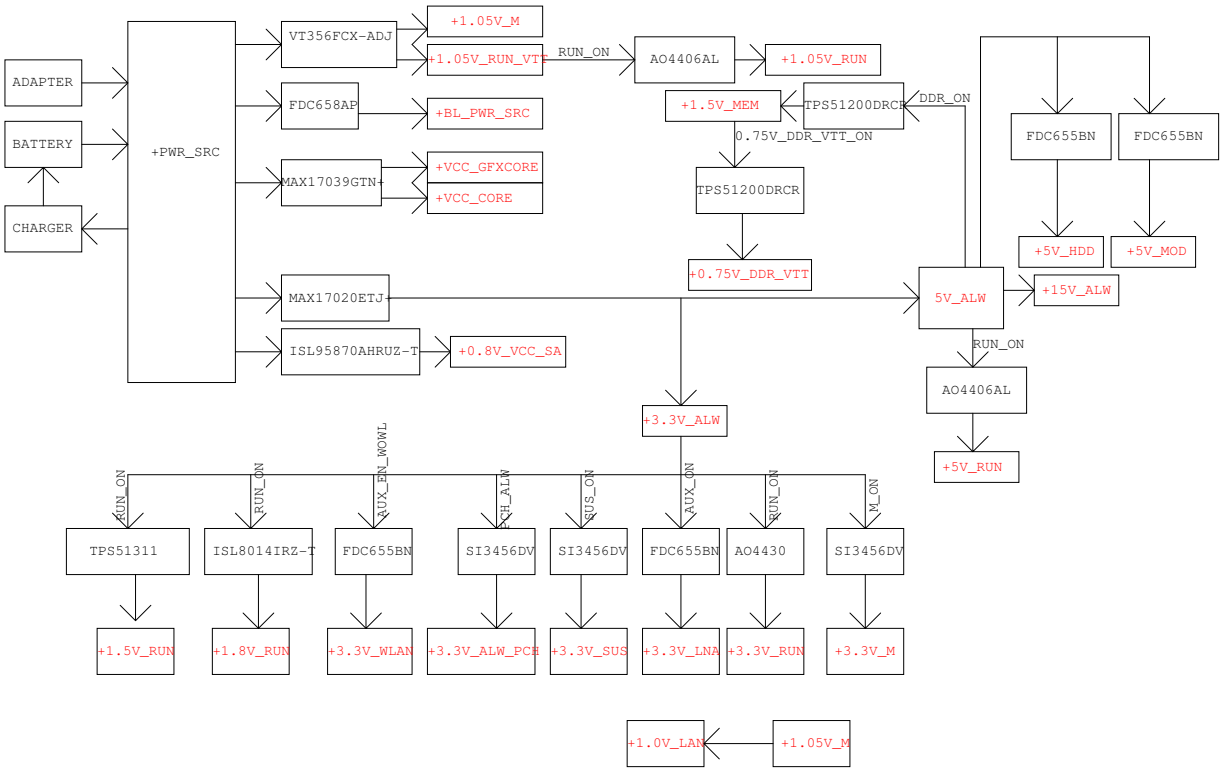

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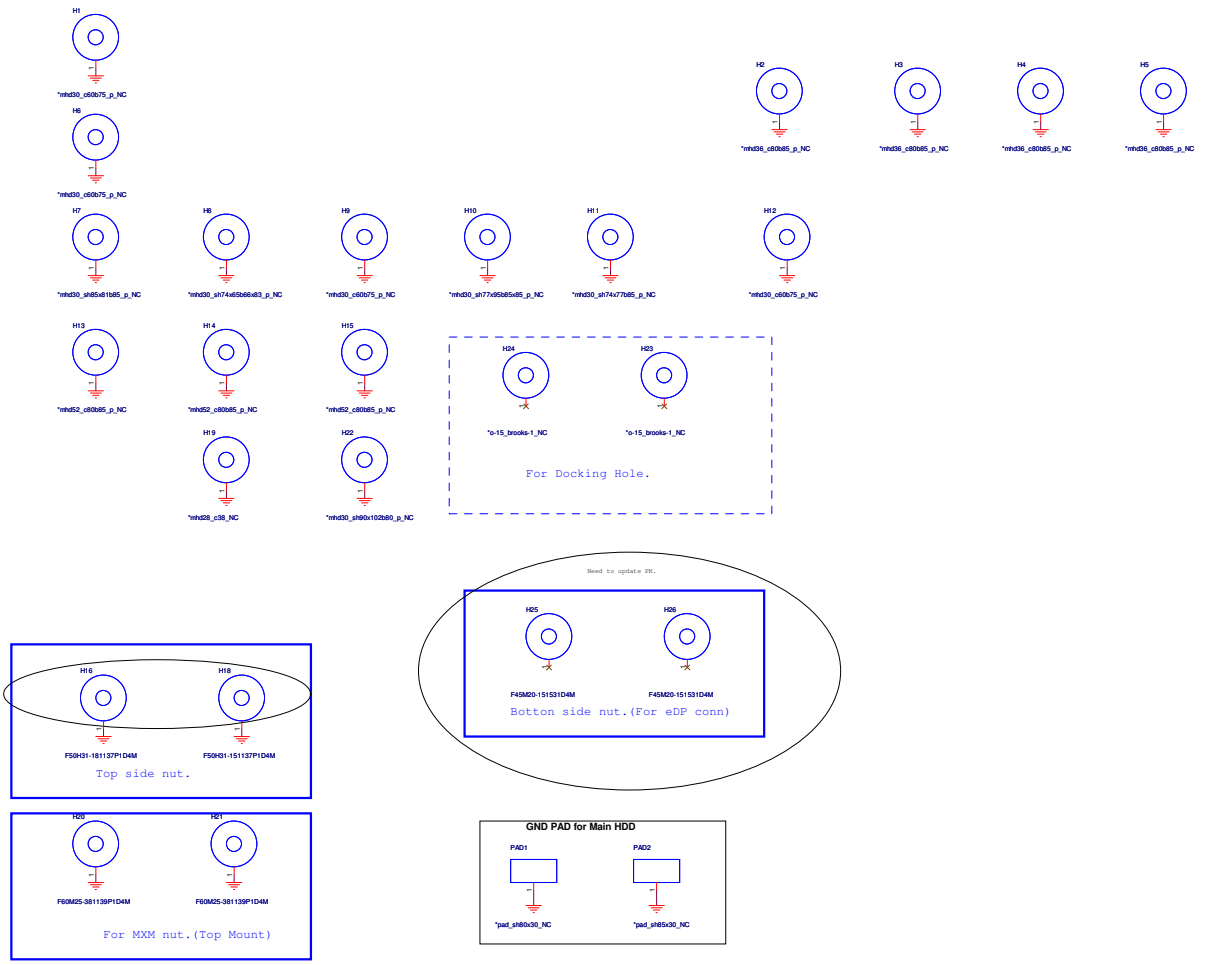

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Title	71 -- PAD,SCREW & Stiching CAPs	
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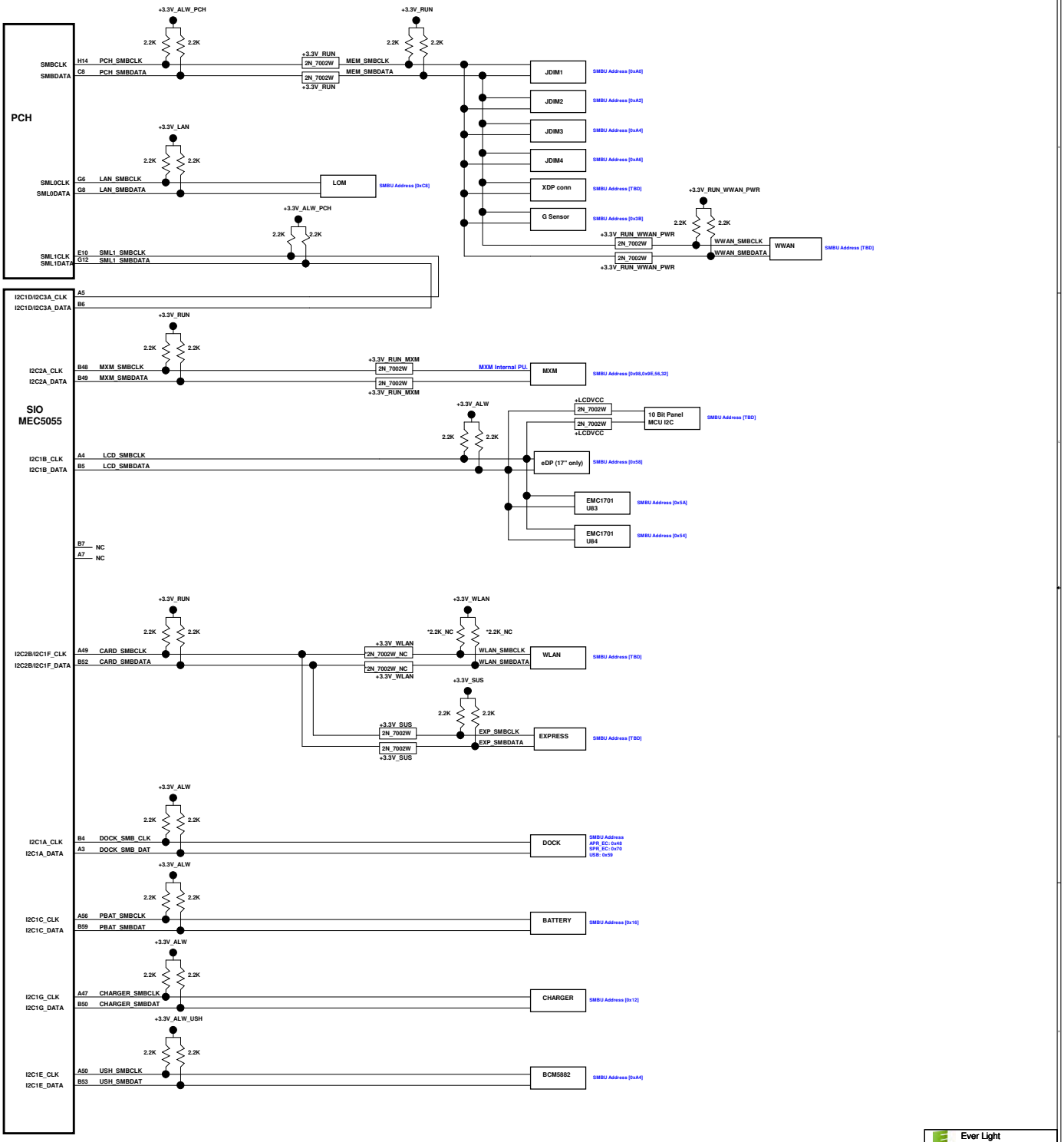

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72 – SMBus Block Diagram

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POWER SATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0(Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3(Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to HDD) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	OFF
S5 (Soft off) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3(Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	ON	ON	OFF	OFF
S4 (Suspend to HDD) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (Soft off) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ Power Plane	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF	OFF	OFF

	USB PORT#	DESTINATION
PCH	0	Right Side top
	1	Right Side bot
	2	Back Side
	3	NC
	4	2nd Mini Card (WLAN/WIMAX)
	5	1st Mini Card (WWAN)
	6	3rd Mini Card
	7	USH
	8	DOCKING
	9	DOCKING
	10	Express Card
	11	BlueTooth
	12	Camera
	13	LCD Touch or Nvidia 3D IR

USH	0	BIO
	1	NC

	PCI EXPRESS	DESTINATION
PCH	Lane 1	1st Mini Card WWAN
	Lane 2	2nd Mini Card WLAN
	Lane 3	Express Card
	Lane 4	USB 3.0
	Lane 5	3rd Mini-Card
	Lane 6	4th Mini-Card
	Lane 7	LAN
	Lane 8	Card Reader

	SATA	DESTINATION
PCH	SATA 0	HDD 1st
	SATA 1	HDD 2nd
	SATA 2	MINI CARD
	SATA 3	ODD
	SATA 4	E-SATA
	SATA 5	Docking

	MXM PORT	CONNECTION
MXM Graphics Module	PORT A	MB DP Port
	PORT B	DOCK DP2
	PORT C	DOCK DP1 and MB HDMI
	PORT D	eDP Panel

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Title	99 -- Media Control	
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