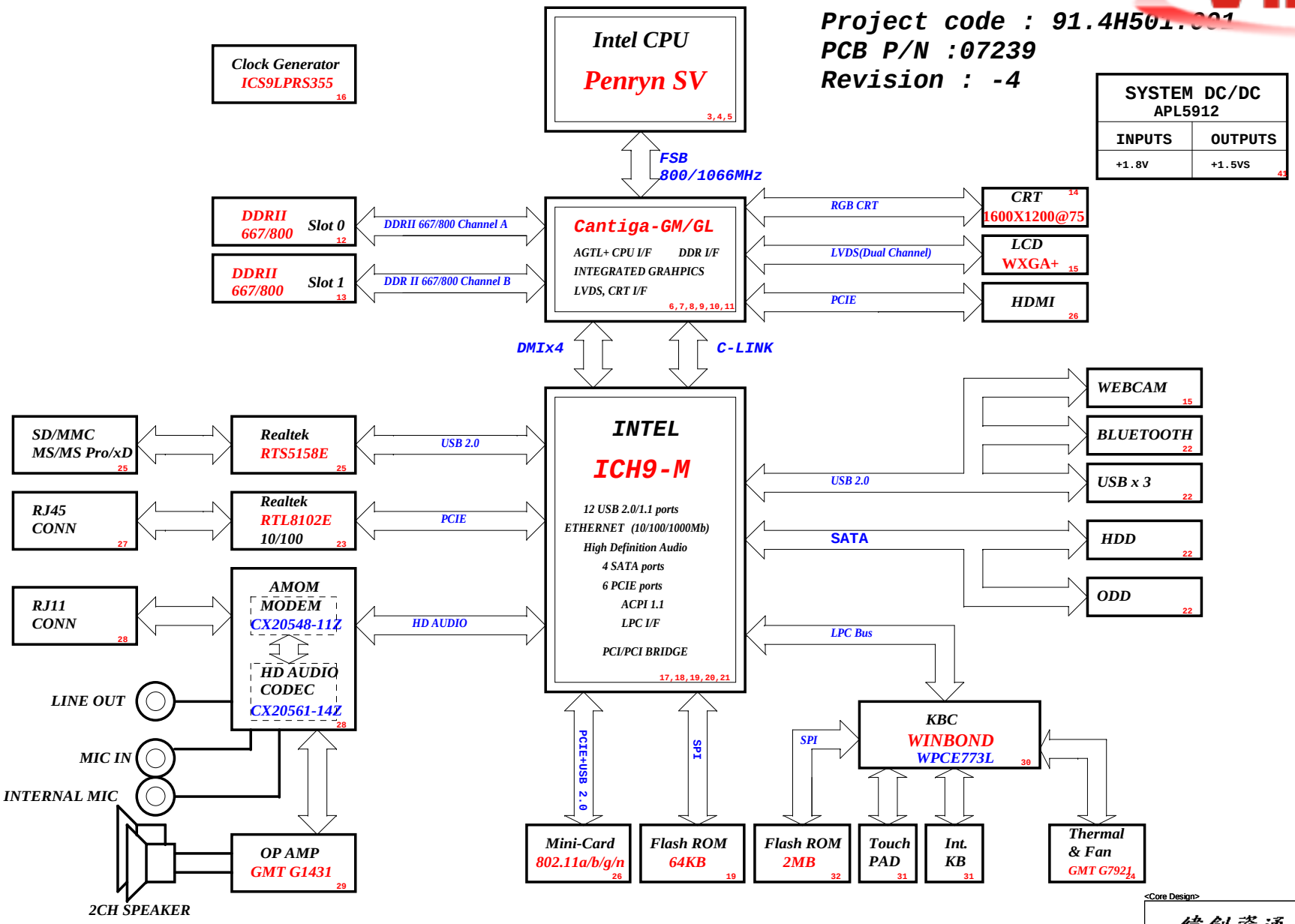
Warrior Intel UMA Block Diagram

Project code : 91.4H501.001
PCB P/N :07239
Revision : -4



SYSTEM DC/DC
APL5912

INPUTS	OUTPUTS
+1.8V	+1.5VS 43

SYSTEM DC/DC
TPS51116

INPUTS	OUTPUTS
DCBATOUT	+0.9VS +1.8V 39

SYSTEM DC/DC
SC412A

INPUTS	OUTPUTS
+5VALW	+1.05V 40

MAXIM CHARGER
MAX8731

INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA 34

CPU DC/DC
ISL6269CCRZ

INPUTS	OUTPUTS
DCBATOUT	+VCC_CORE 0.844~1.3V 22A 36,37

PCB LAYER

L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 4
L5: VCC
L6: Signal 4

<Core Design>

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Title: Block Diagram
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ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK.	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC (Cofig Registers: offset 224h). This signal has weak internal pull-down.
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of PRC.PC (Config Registers: Offset 224h).
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of PRC.PC2 (Config Registers: Offset 224h).
GPIO20	Reserved.	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK.	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/ GPIO55	Top-Block Swap override. Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK.	Sample low: the Integrated TPM will be disable. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of CLPWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0:Offset D8).
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap. Rising Edge of PWROK.	Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9 Integrated pull-up and pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller.
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO20	PULL-DOWN 20K
GPIO49	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4 (Default)**
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2) **1 = The iTPM Host Interface is disabled (default)**
CFG7	Intel Management engine crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality(Default)**
CFG9	PCIE Graphics Lane	0 = Reserved Lanes, 15->0, 14->1 ect.. **1 = Normal operation (Default): Lane Numbered in Order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1 = Disable (Default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enable (Note 3) **11 = Disabled (Default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation (Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode [MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH->ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 = Digital display Port and PCIe are operating simulataneously via the PEG port
SDVO _CTRLDATA	SDVO Present	**0 = No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1 = LFP Card Present; PCIE disabled

NOTE:

1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

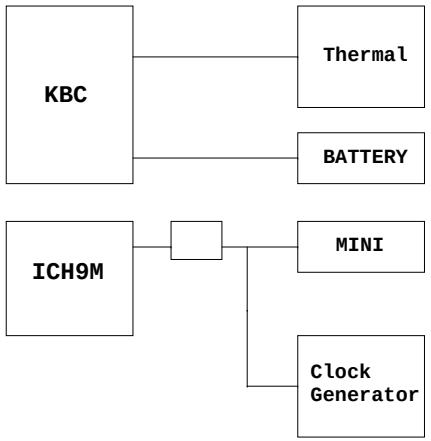
PCIE Routing page 19

LANE1	LAN
LANE2	MiniCard WLAN

USB Table page 19

USB	
Pair	Device
0	USB3
1	FREE
2	External USB3
3	FREE
4	External USB2
5	FREE
6	WLAN
7	BLUETOOTH
8	CARD_READER
9	FREE
10	CAMERA
11	FREE

SMBus



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Title: Table of Content

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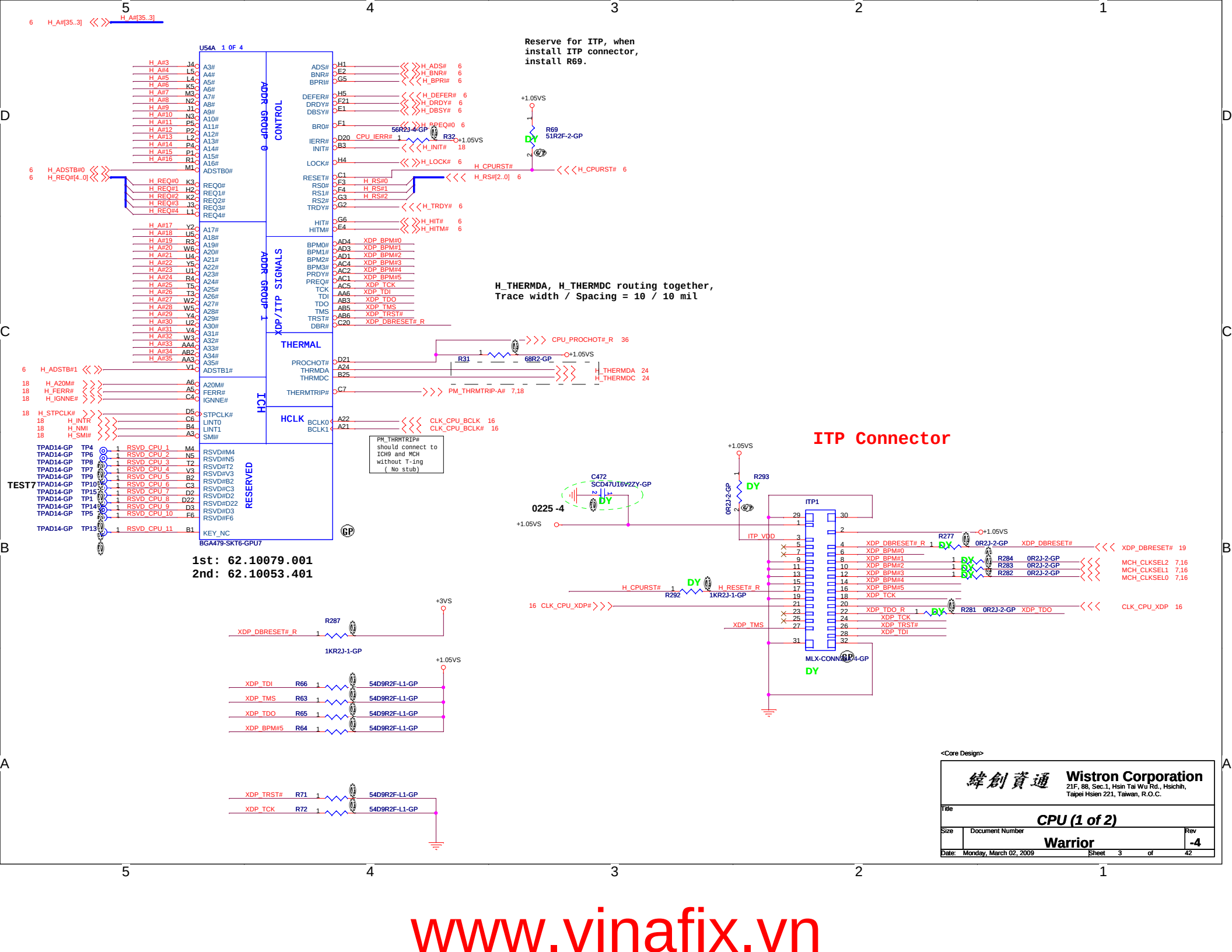

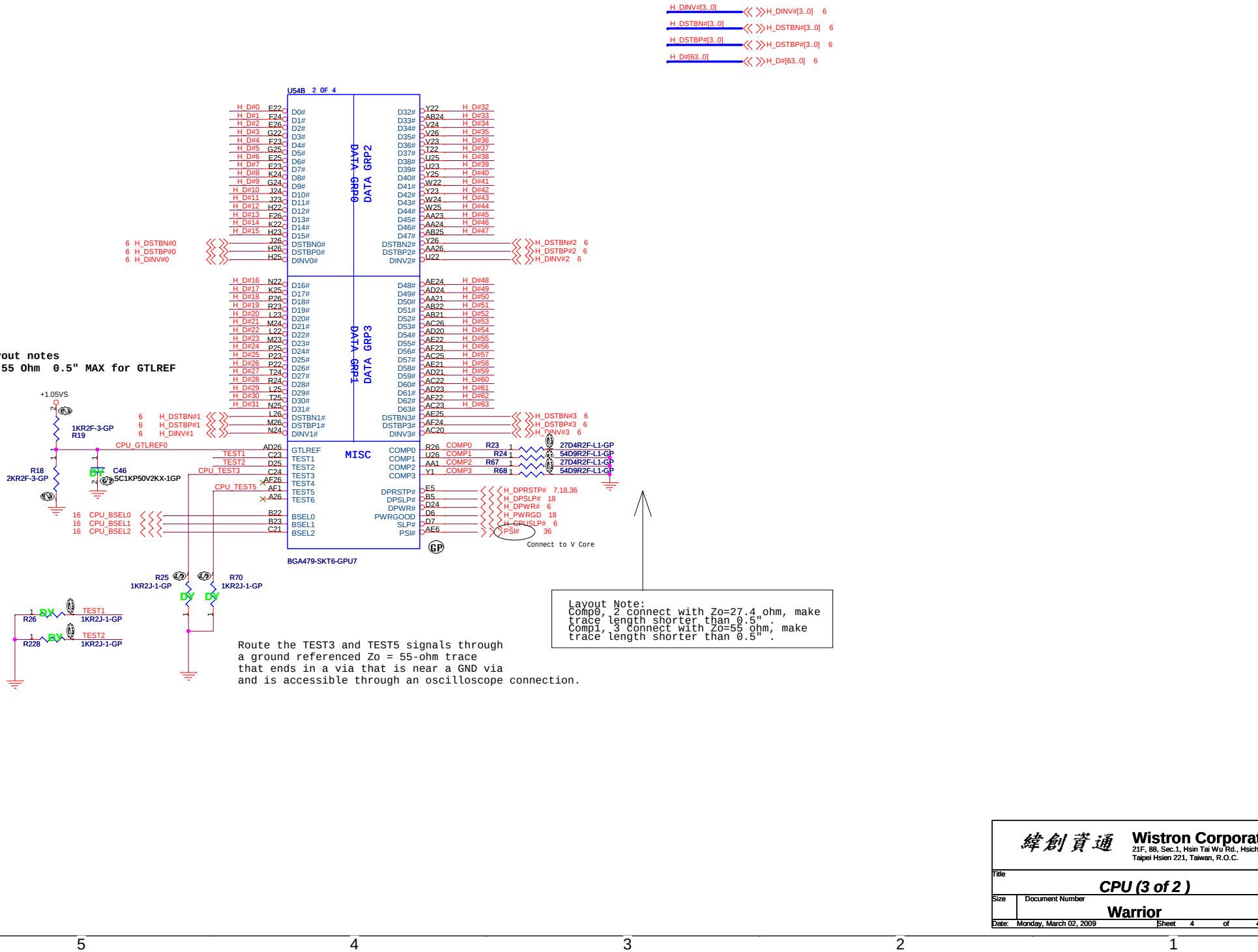

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Please these inside socket cavity on L8(North side Secondary)

Please these inside socket cavity on L8(South side Secondary)

Please these inside socket cavity on L8(North side Primary)

Please these outside socket cavity on L8(North side Secondary)

Please these outside socket cavity on L8(South side Secondary)

Please these inside socket cavity on L8(South side Primary)

Please these inside socket cavity on L8(North side Secondary)

layout note: "1D5V_VCCA_S0" as short as possible

Layout Note:
Place as close as possible to the CPU VCCA pin.

Connect to V Core

Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

0225 -4

U54C 3 0F 4

BGA479-SKT6-GPU7

U54D 4 0F 4

BGA479-SKT6-GPU7

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Title	CPU (3 of 3)
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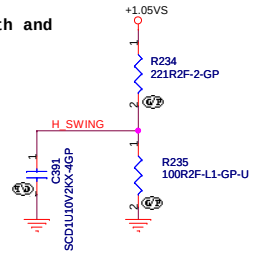
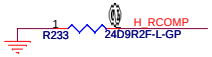
H_SWING routing Trace width and Spacing use 10 / 20 mil

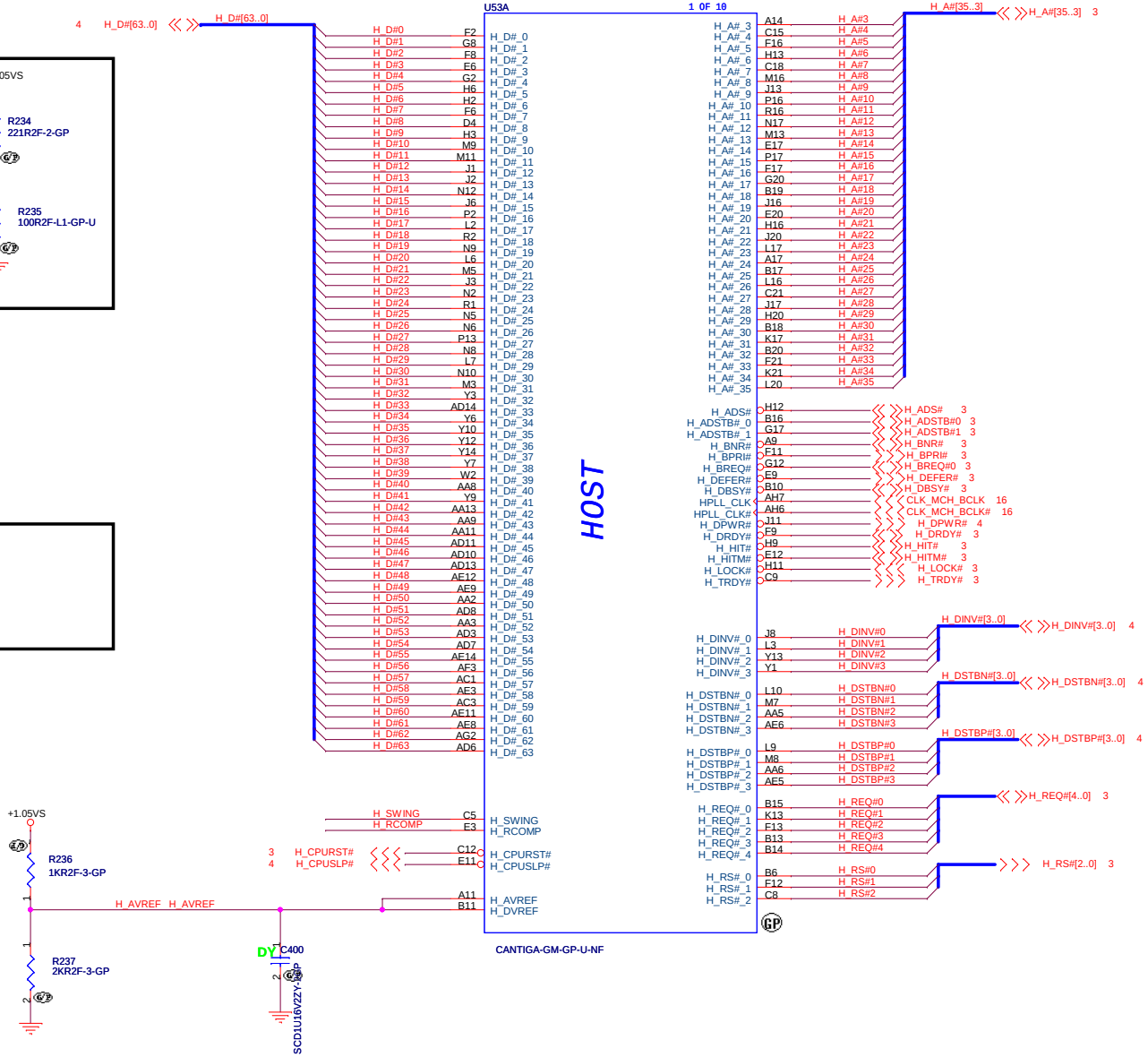
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



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Title: **Cantiga (1 of 6)**

Size	Document Number	Rev
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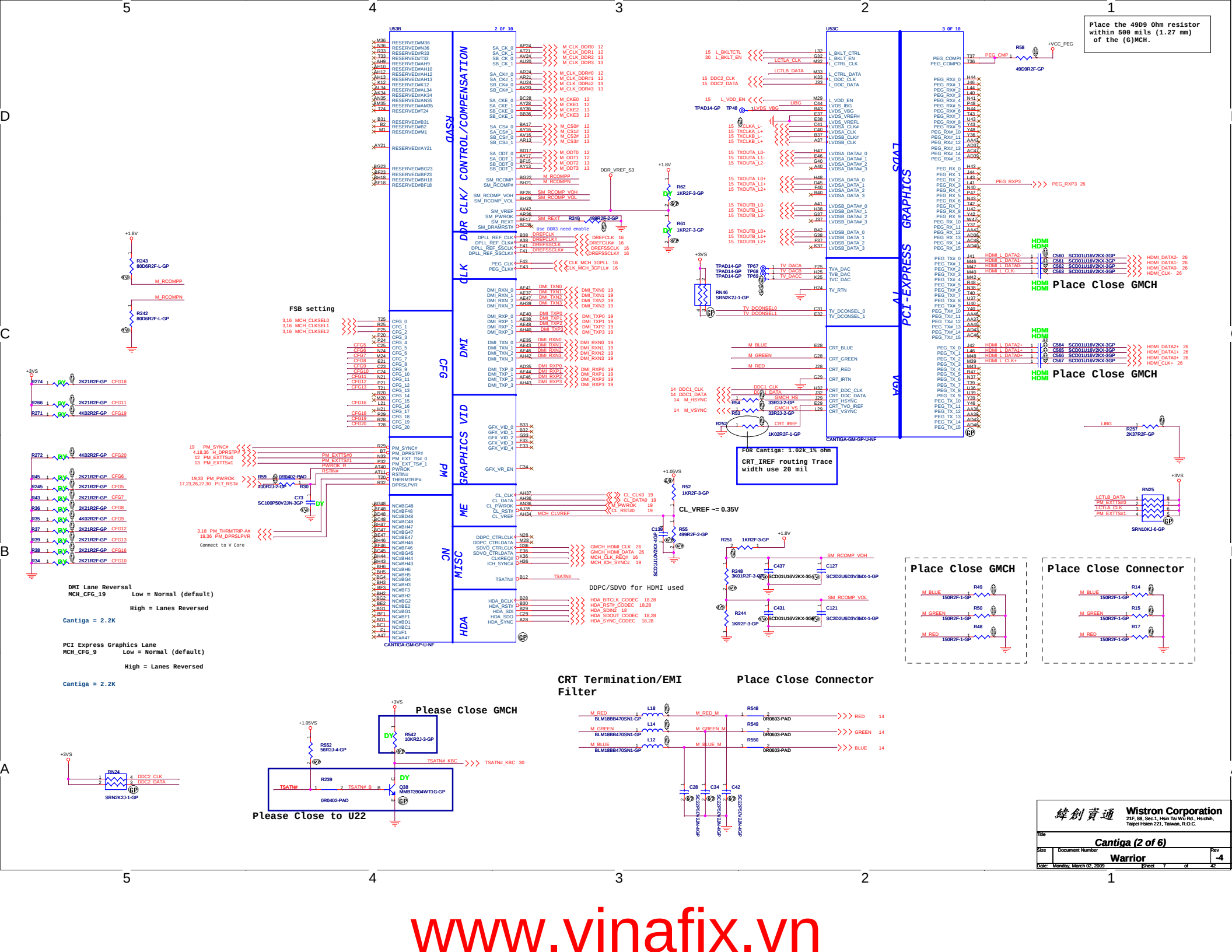
Date: Monday, March 02, 2009 Sheet 6 of 42


Place the 49D9 Ohm resistor within 500 mils (1.27 mm) of the (G)MCH.
FSB setting
DMI Lane Reversal
MCH_CFG_19 Low = Normal (default)
High = Lanes Reversed
Cantiga = 2.2K
PCI Express Graphics Lane
MCH_CFG_9 Low = Normal (default)
High = Lanes Reversed
Cantiga = 2.2K
FOR Cantiga: 1.02k_1% ohm
CRT_IREF routing Trace width use 20 mil
CL_VREF ~= 0.35V
DDPC/SDVO for HDMI used
CRT Termination/EMI Filter
Place Close GMCH
Place Close Connector
Please Close GMCH
Please Close to U22
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Cantiga (2 of 6)
Warrior
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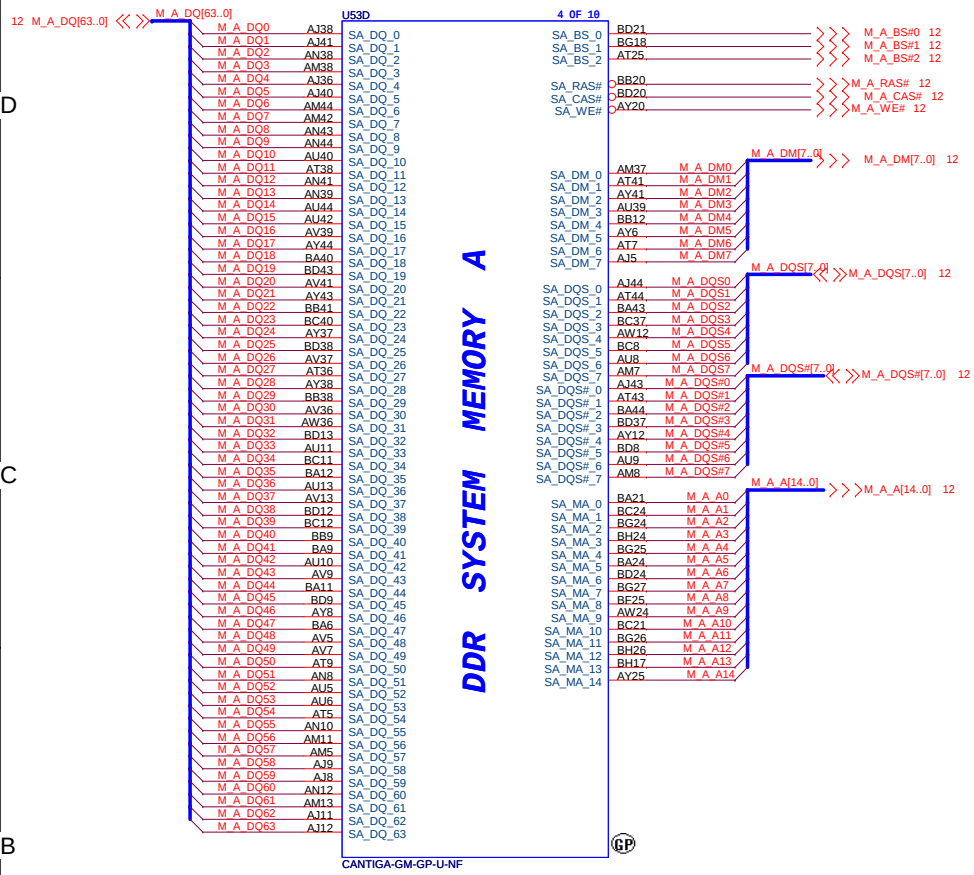

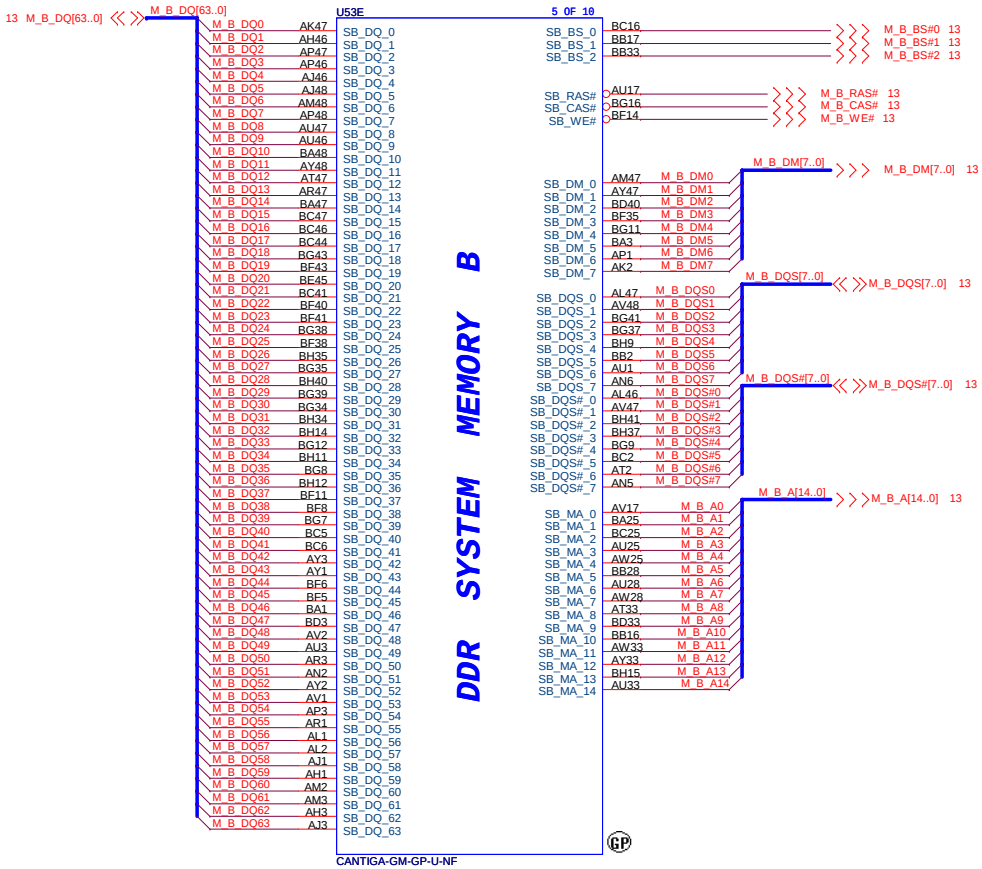

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Title	***Cantiga (3 of 6)***
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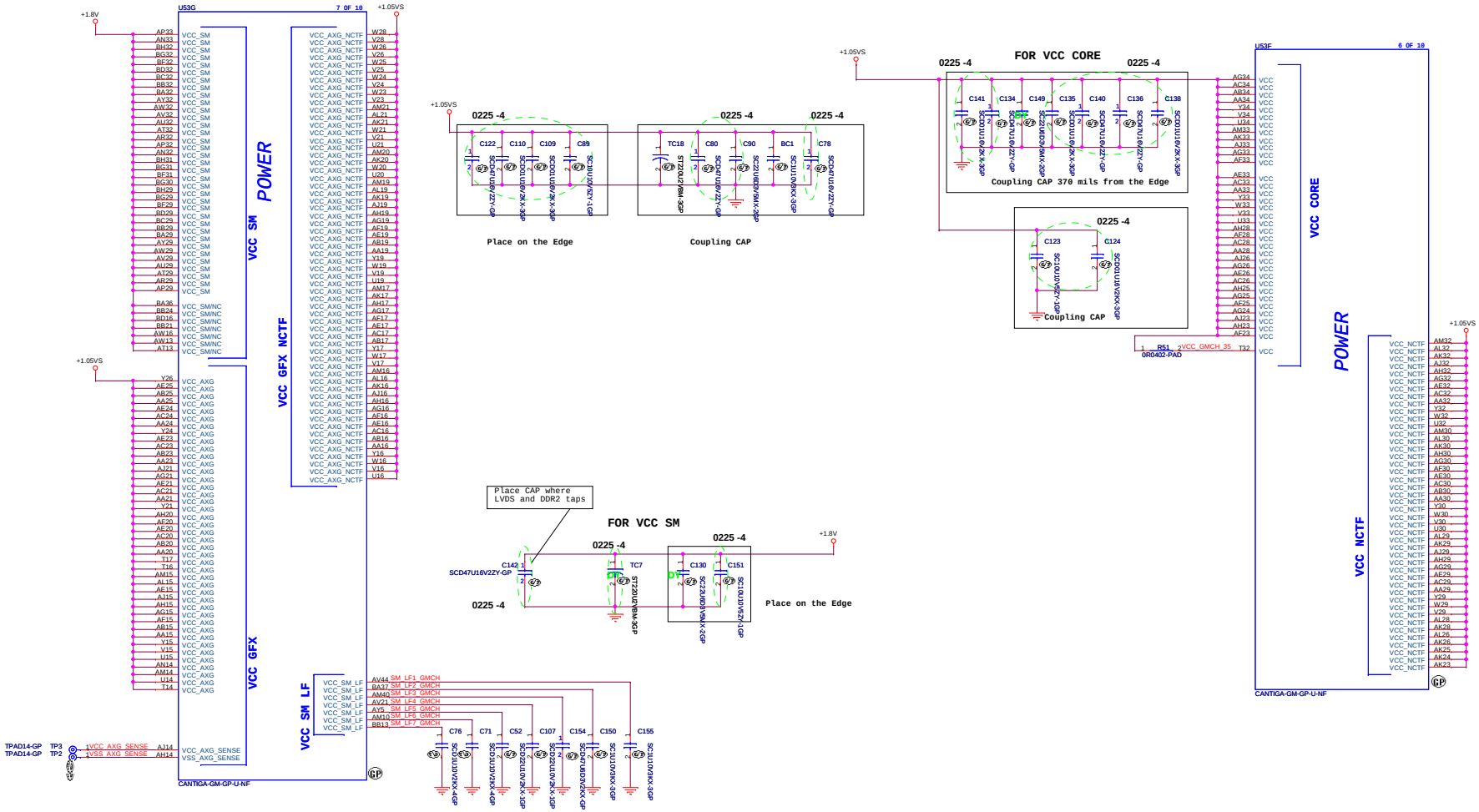
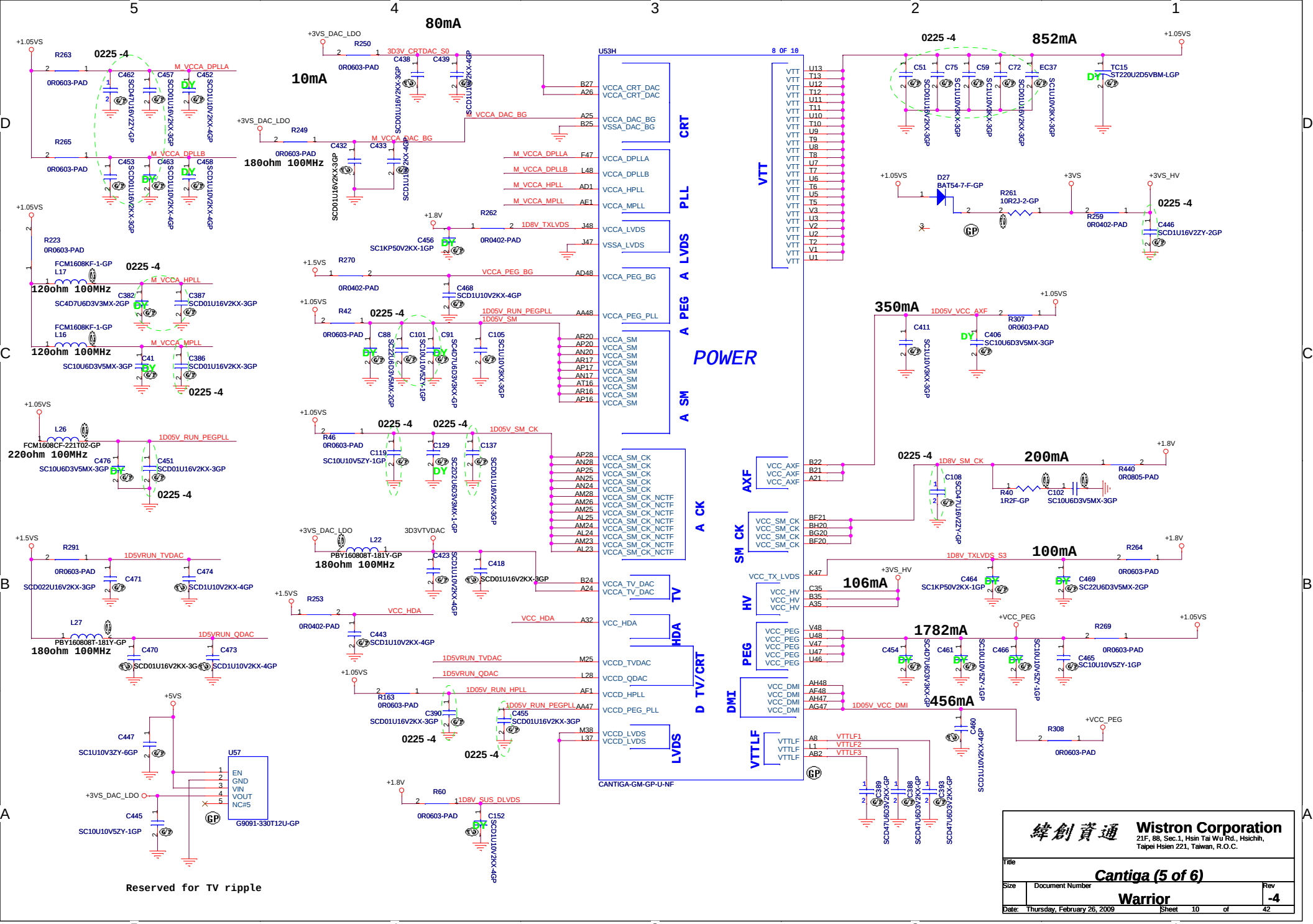
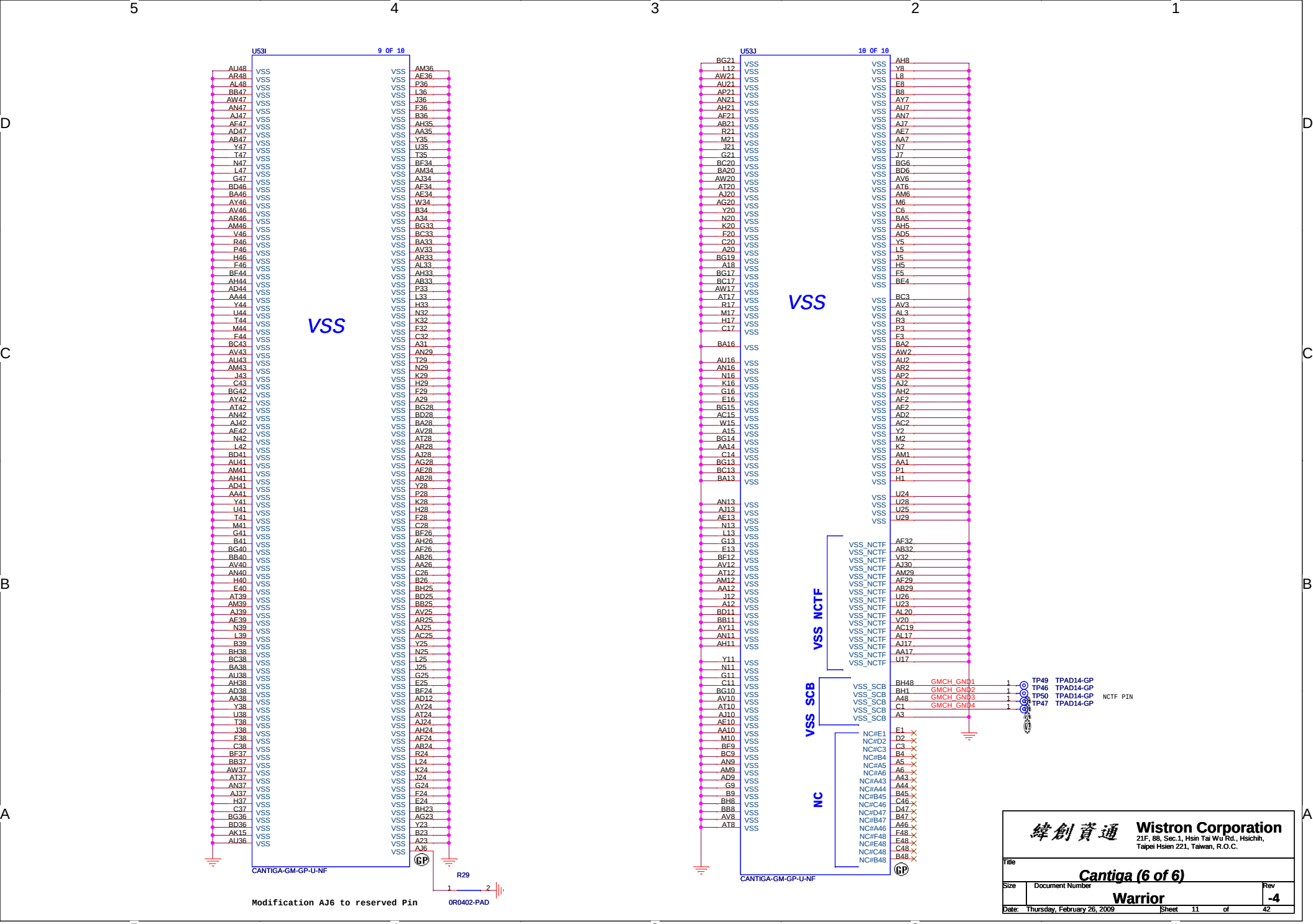
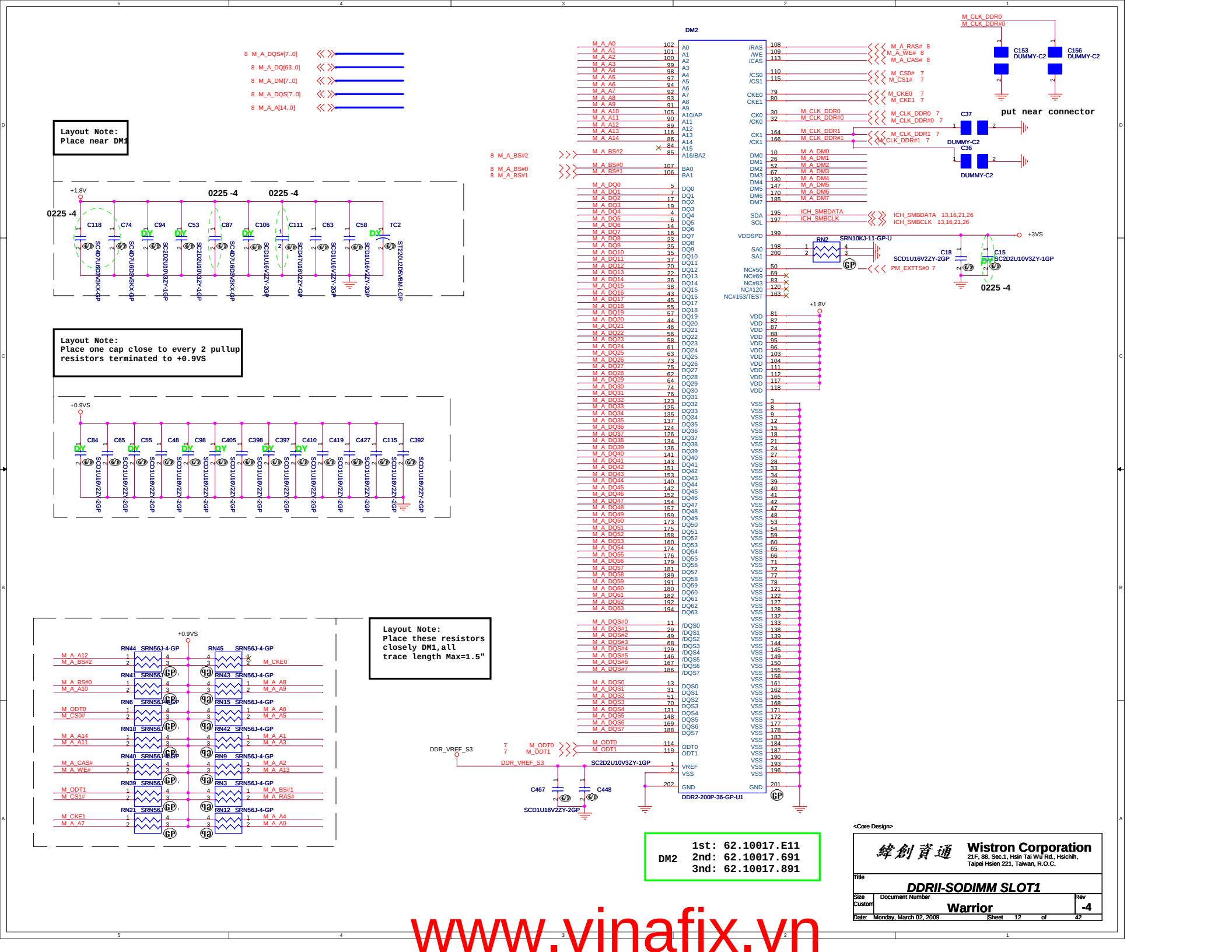
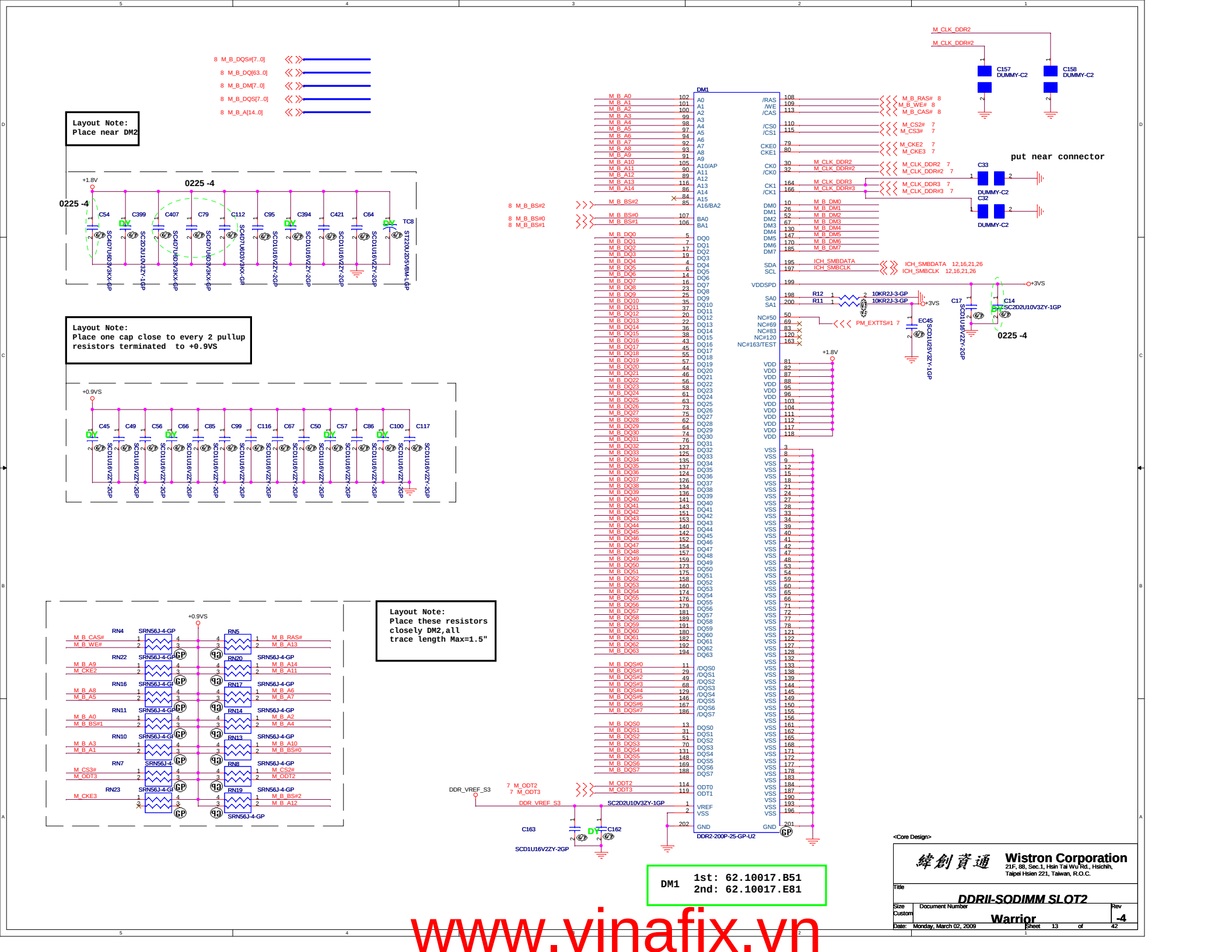


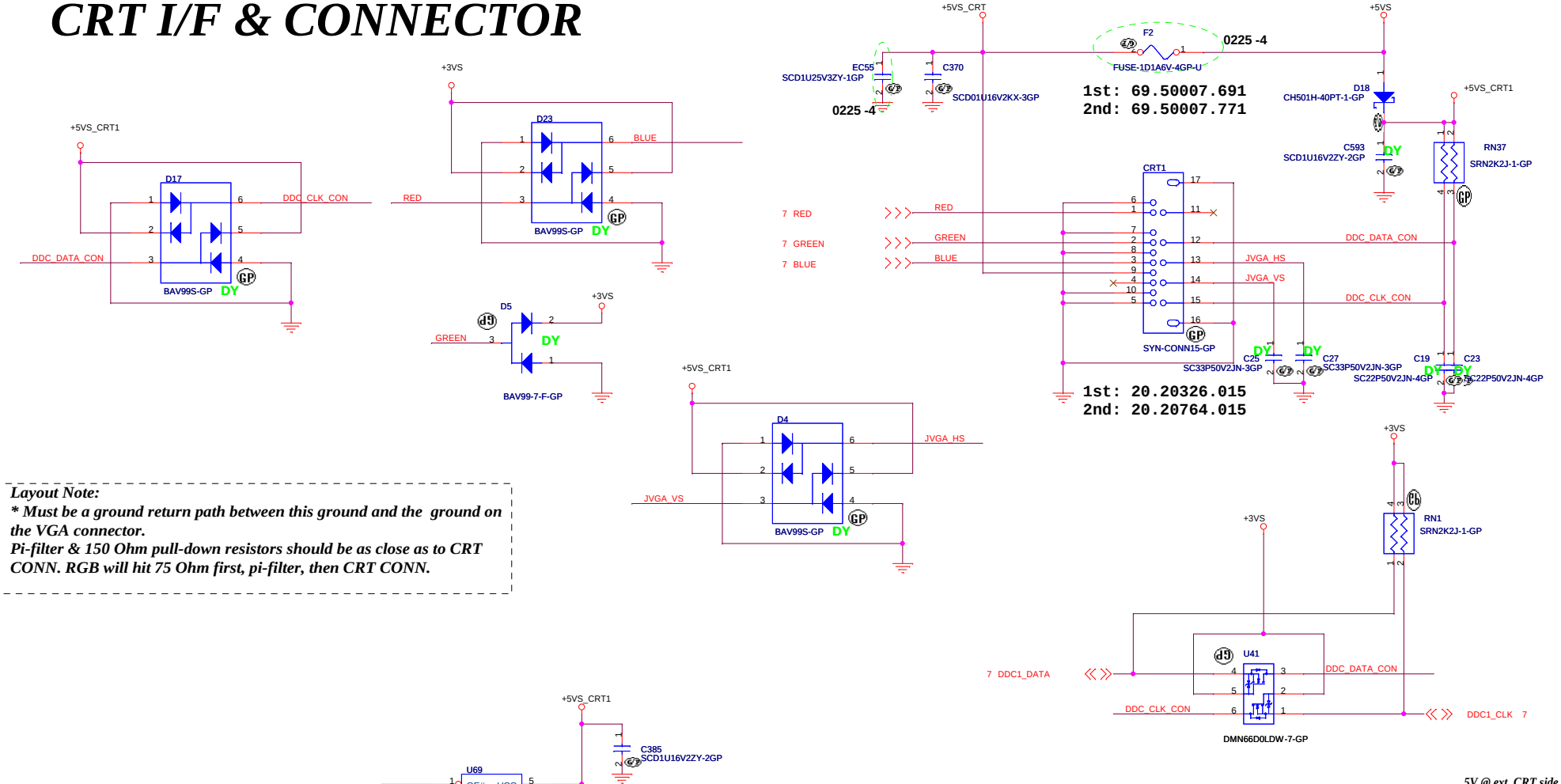








CRT I/F & CONNECTOR



Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

5V @ ext. CRT side

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Title: **CRT Connector**

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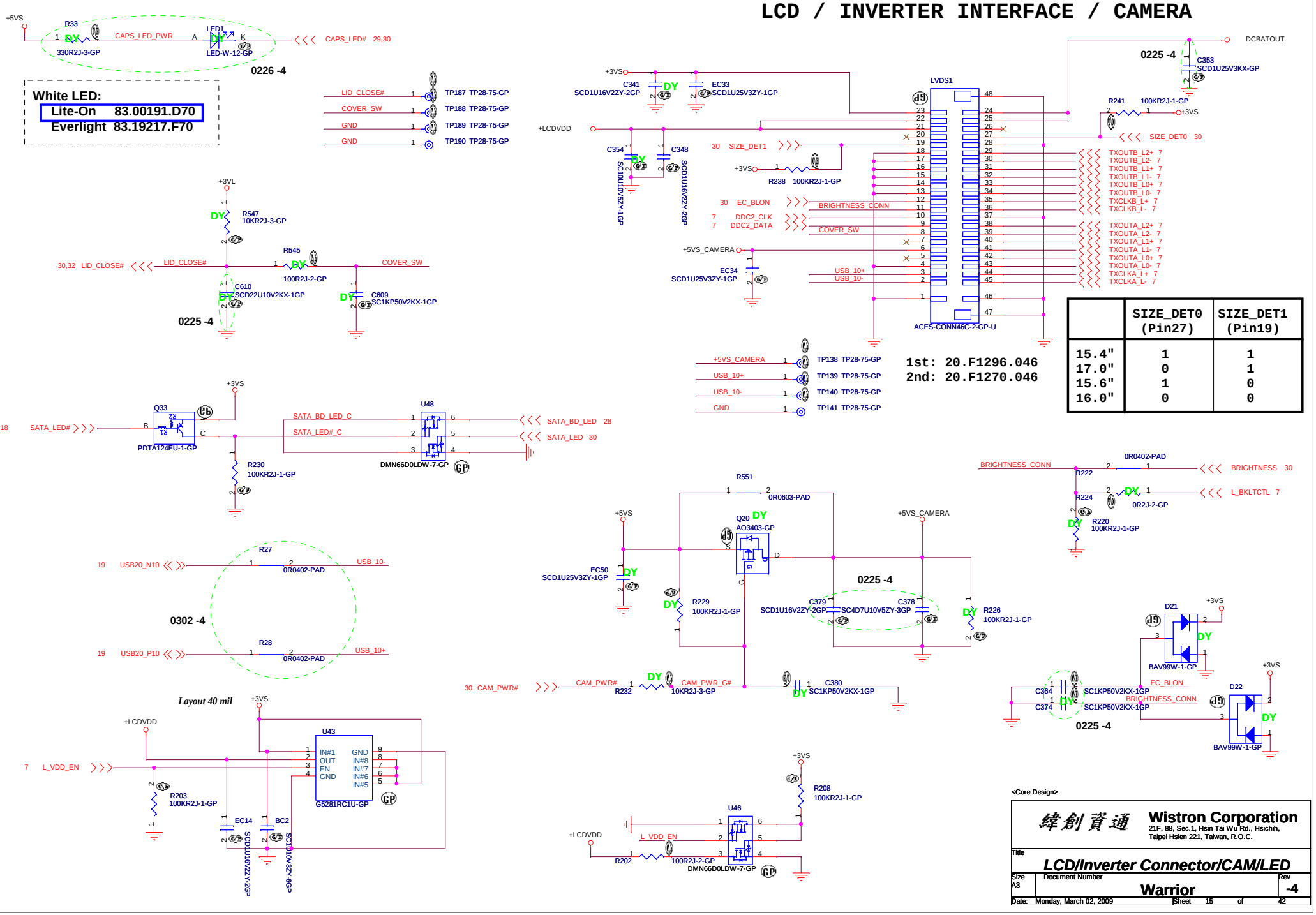
LCD / INVERTER INTERFACE / CAMERA



	SIZE_DET0 (Pin27)	SIZE_DET1 (Pin19)
15.4"	1	1
17.0"	0	1
15.6"	1	0
16.0"	0	0

<Core Design>

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Title: **LCD/Inverter Connector/CAM/LED**

Size: A3 | Document Number: Warrior | Rev: -4

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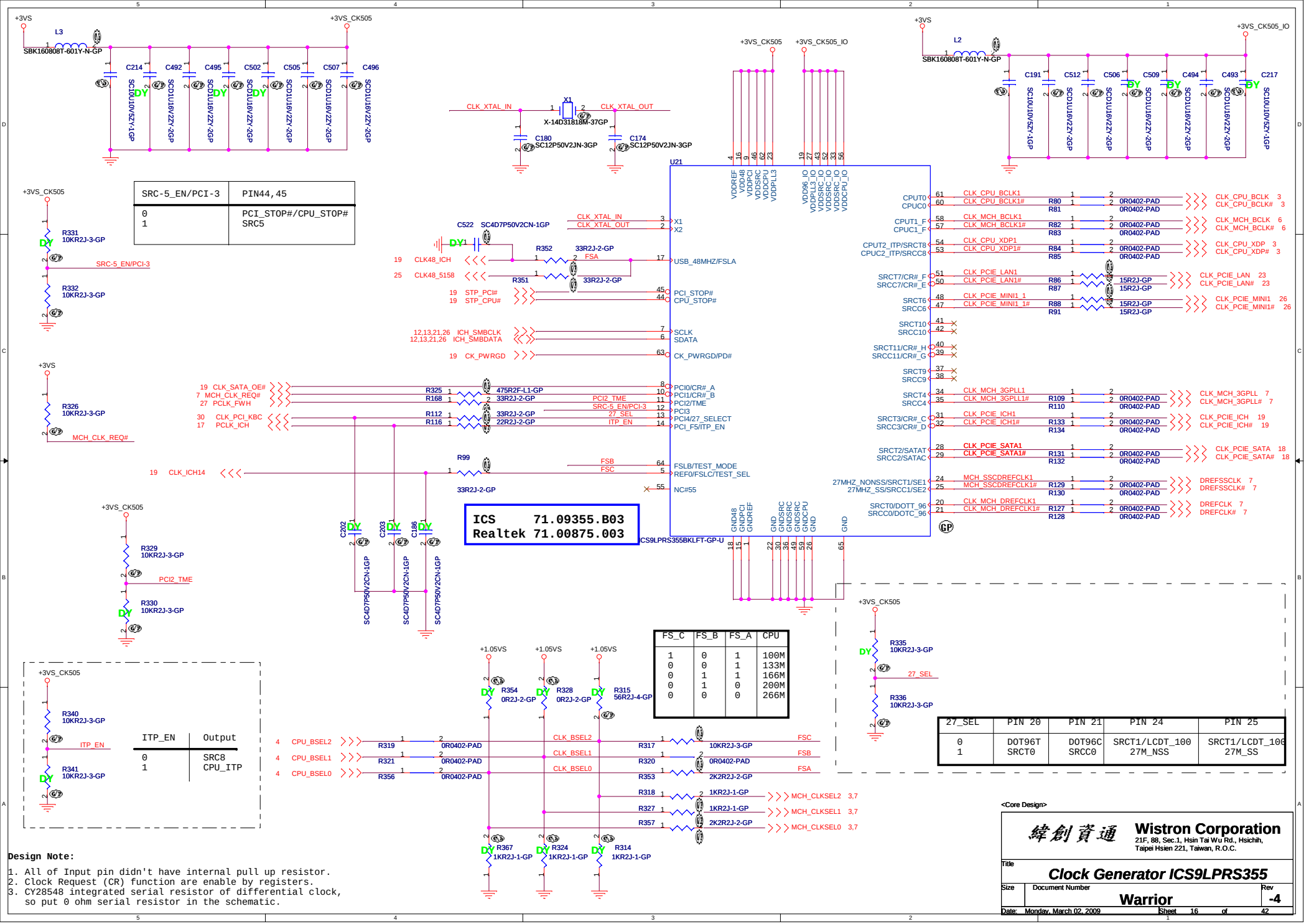

SRC-5_EN/PCI-3	PIN44,45
0	PCI_STOP#/CPU_STOP#
1	SRC5

ITP_EN	Output
0	SRC8
1	CPU_ITP

FS_C	FS_B	FS_A	CPU
1	0	1	100M
0	0	1	133M
0	1	1	166M
0	1	0	200M
0	0	0	266M

27_SEL	PIN 20	PIN 21	PIN 24	PIN 25
0	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1	SRCT0	SRCC0	27M_NSS	27M_SS

ICS 71.09355.B03
Realtek 71.00875.003

Design Note:

1. All of Input pin didn't have internal pull up resistor.
2. Clock Request (CR) function are enable by registers.
3. CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.

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Title: **Clock Generator ICS9LPRS355**

Size | Document Number: **Warrior** | Rev: **-4**

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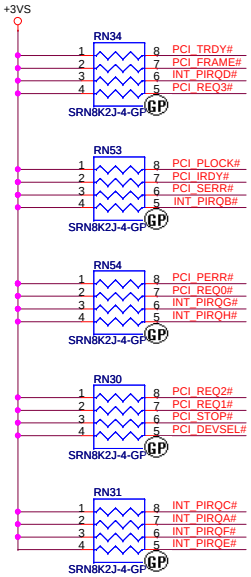
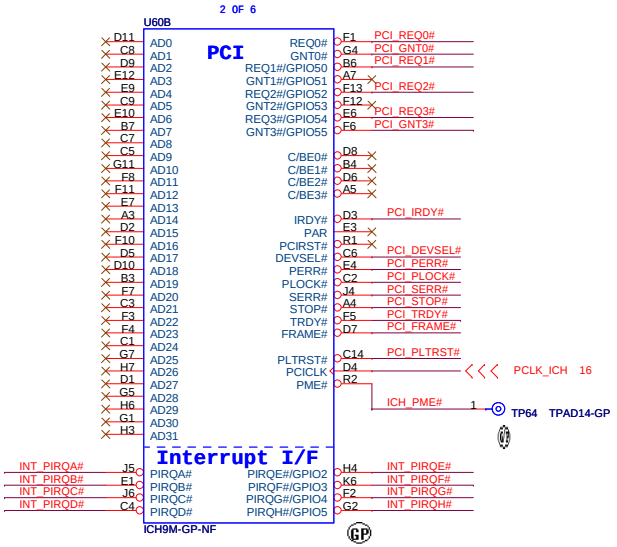
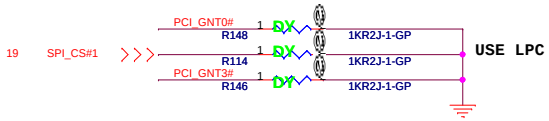
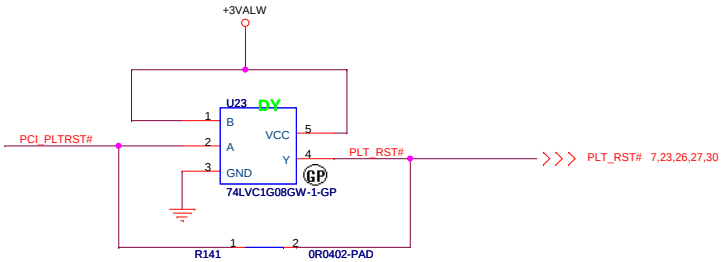






BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

A16 swap override strap	
PCI_GNT#3	low = A16 swap override enable high = default



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Title: ICH9-M (1 of 5)

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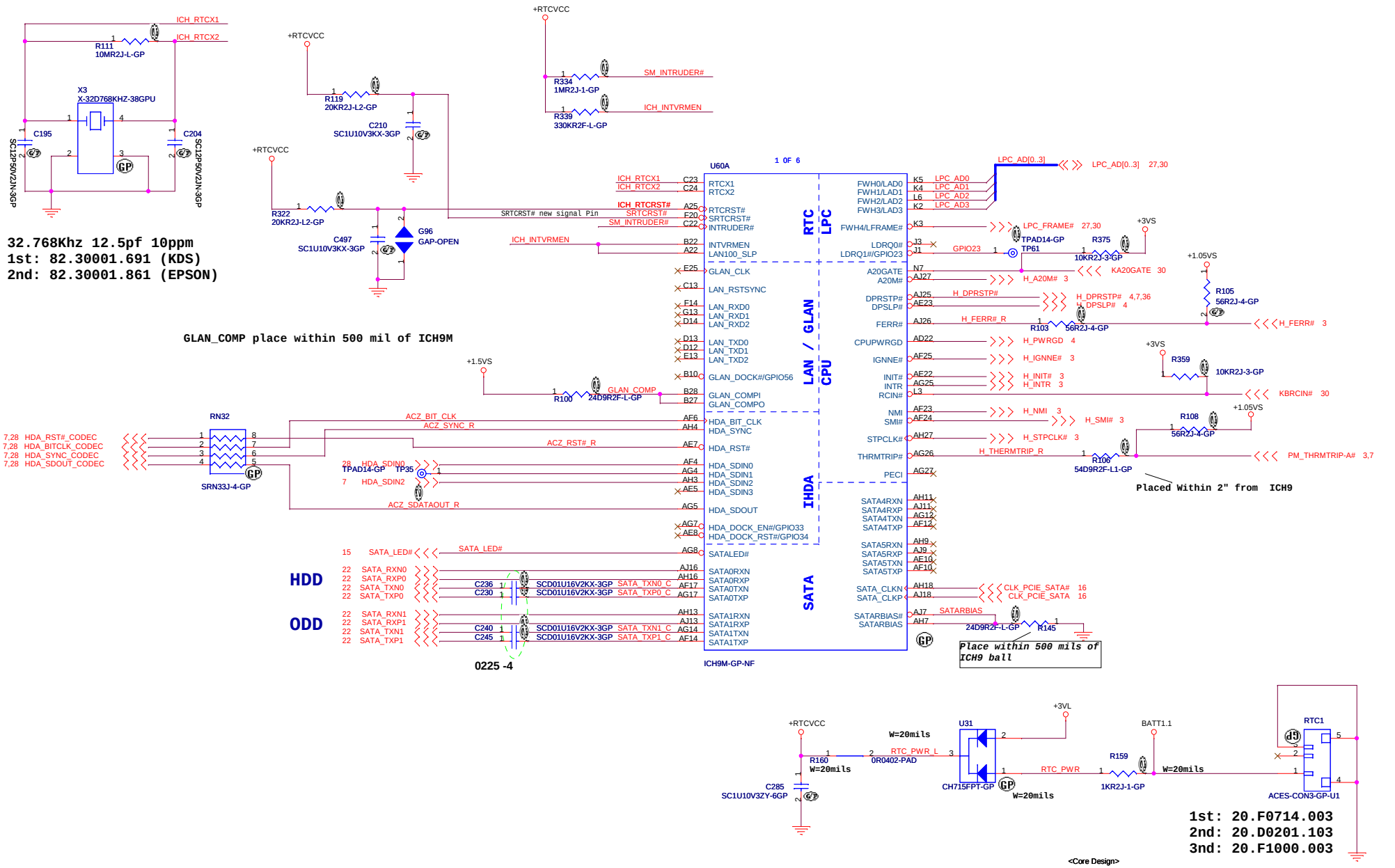

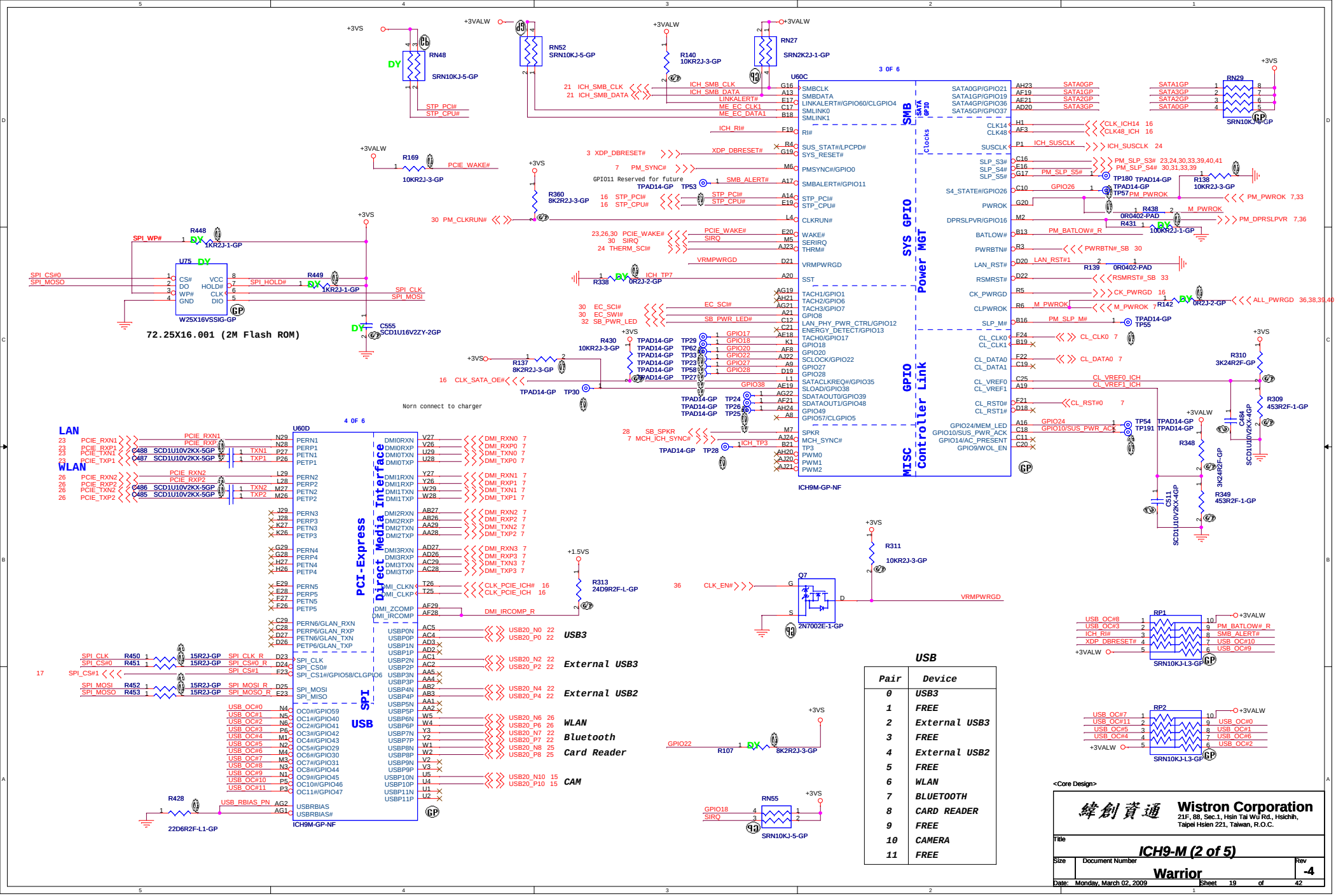

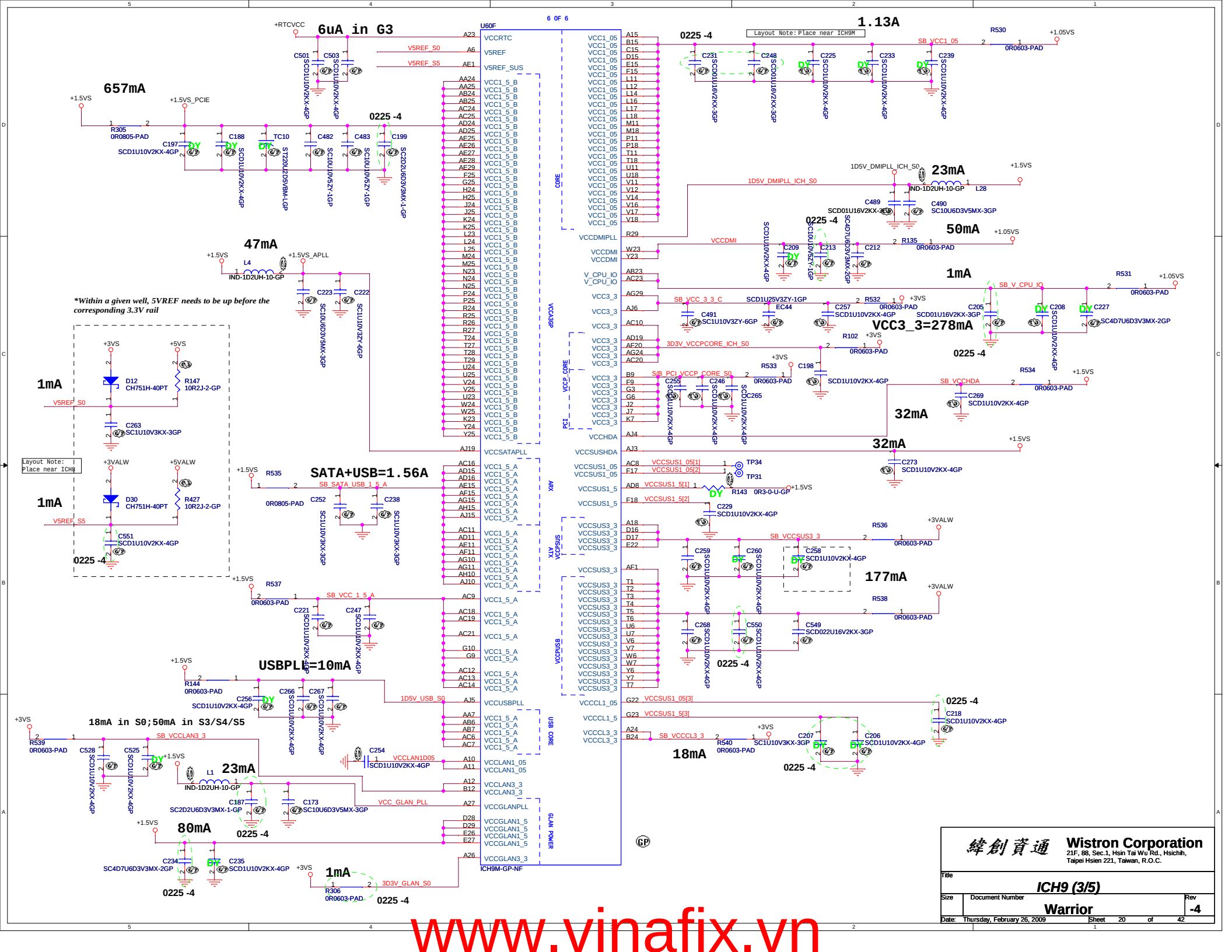
6 OF 6
U60F
ICH9M-GP-NF
6uA in G3
657mA
47mA
1mA
1mA
1mA
SATA+USB=1.56A
USBPLL=10mA
18mA in S0;50mA in S3/S4/S5
23mA
80mA
1mA
1.13A
23mA
50mA
1mA
VCC3_3=278mA
32mA
32mA
177mA
18mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note: Place near ICH9M
Layout Note: Place near ICH9
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Title
ICH9 (3/5)
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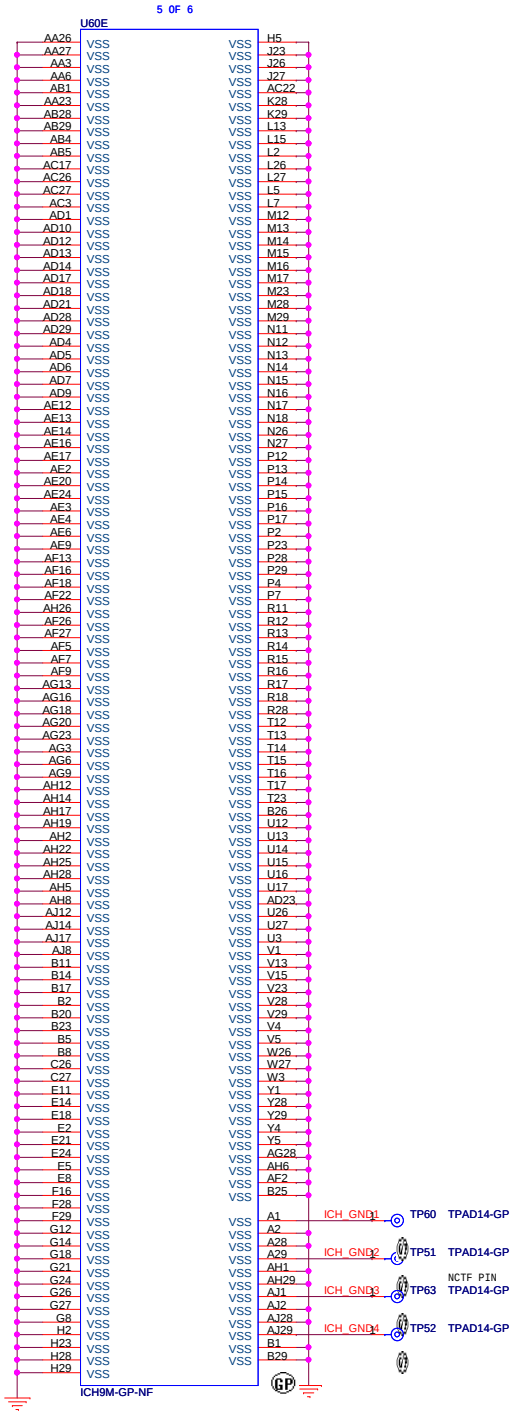
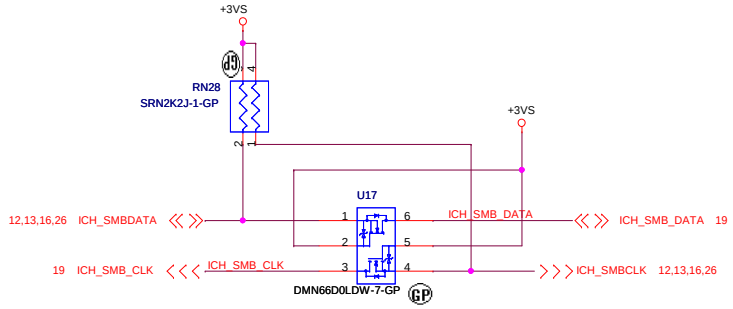
www.vinafix.vn



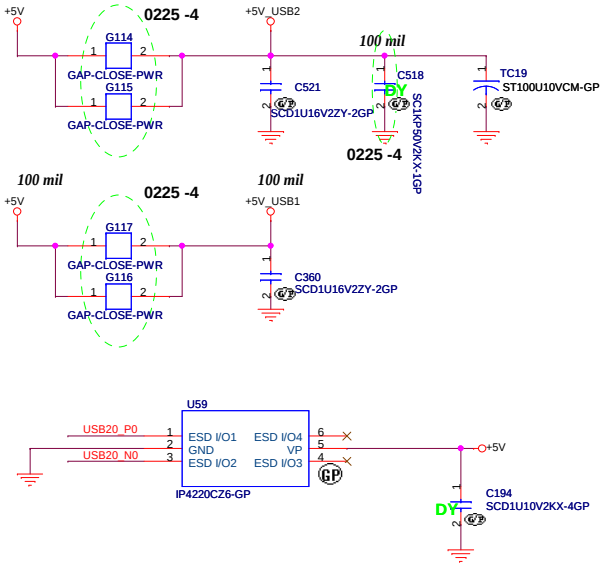


SMBUS

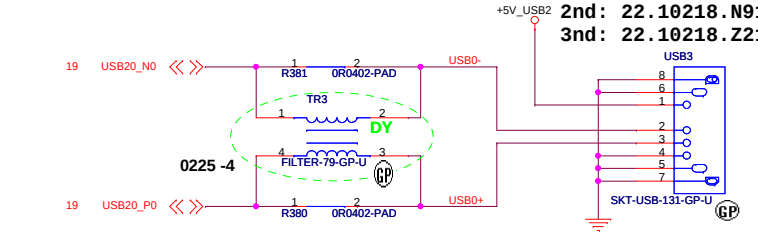
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***ICH9-M (4 of 4)***	
Size	Document Number: **Warrior**	Rev: **-4**
Date: Monday, March 02, 2009	Sheet 21 of 42	

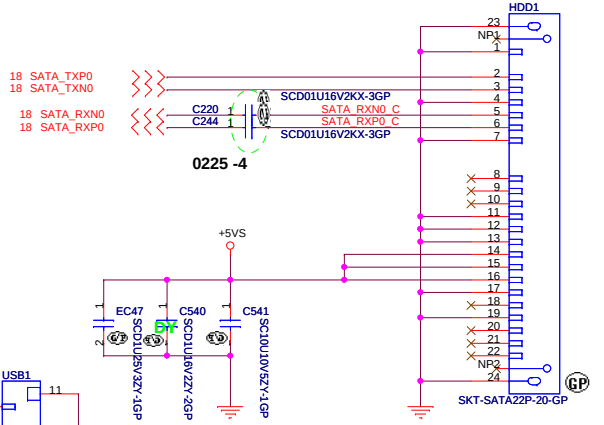
USB PORT



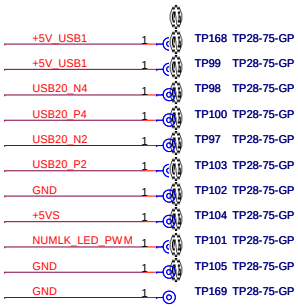
1st: 22.10218.N21
2nd: 22.10218.N91
3nd: 22.10218.Z21

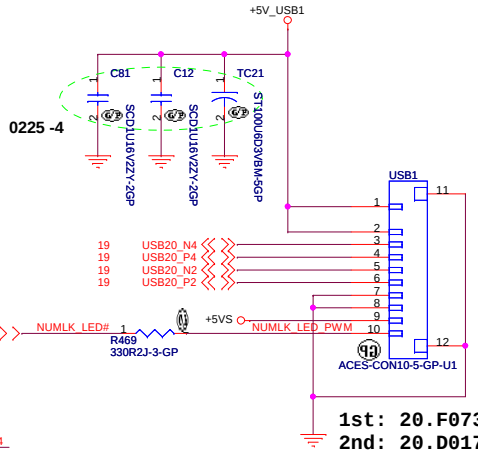


SATA HDD Connector

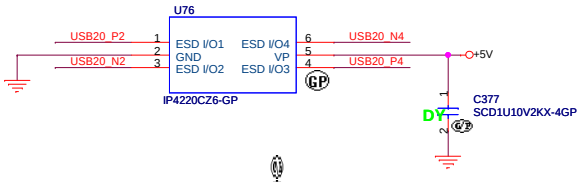


1st: 62.10065.261
2nd: 62.10065.511

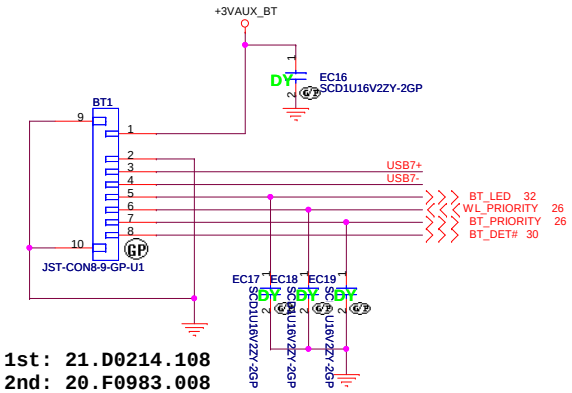




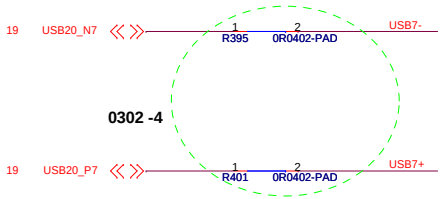
1st: 20.F0735.010
2nd: 20.D0174.110
3nd: 20.F0984.010

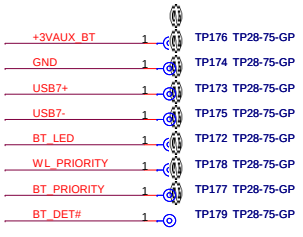


BLUETOOTH

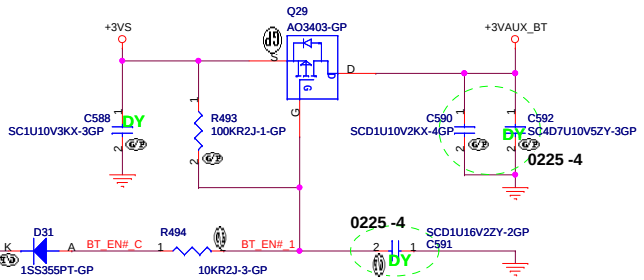


1st: 21.D0214.108
2nd: 20.F0983.008

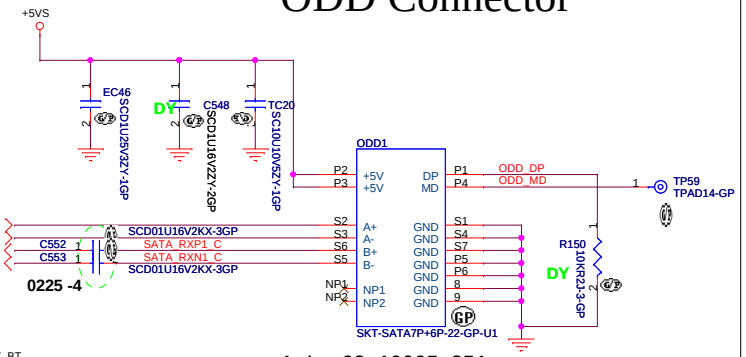




MAX 150mA



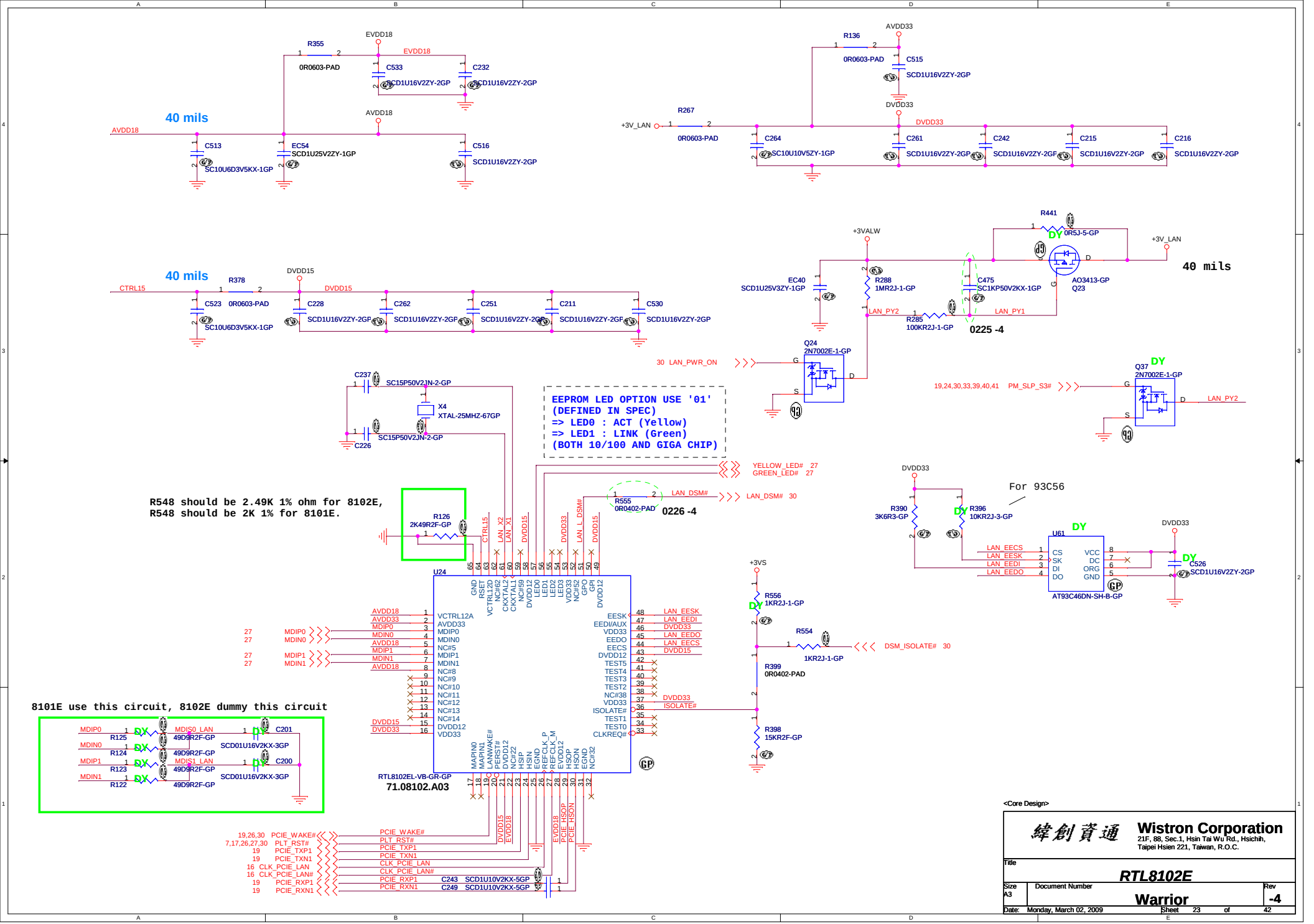
ODD Connector

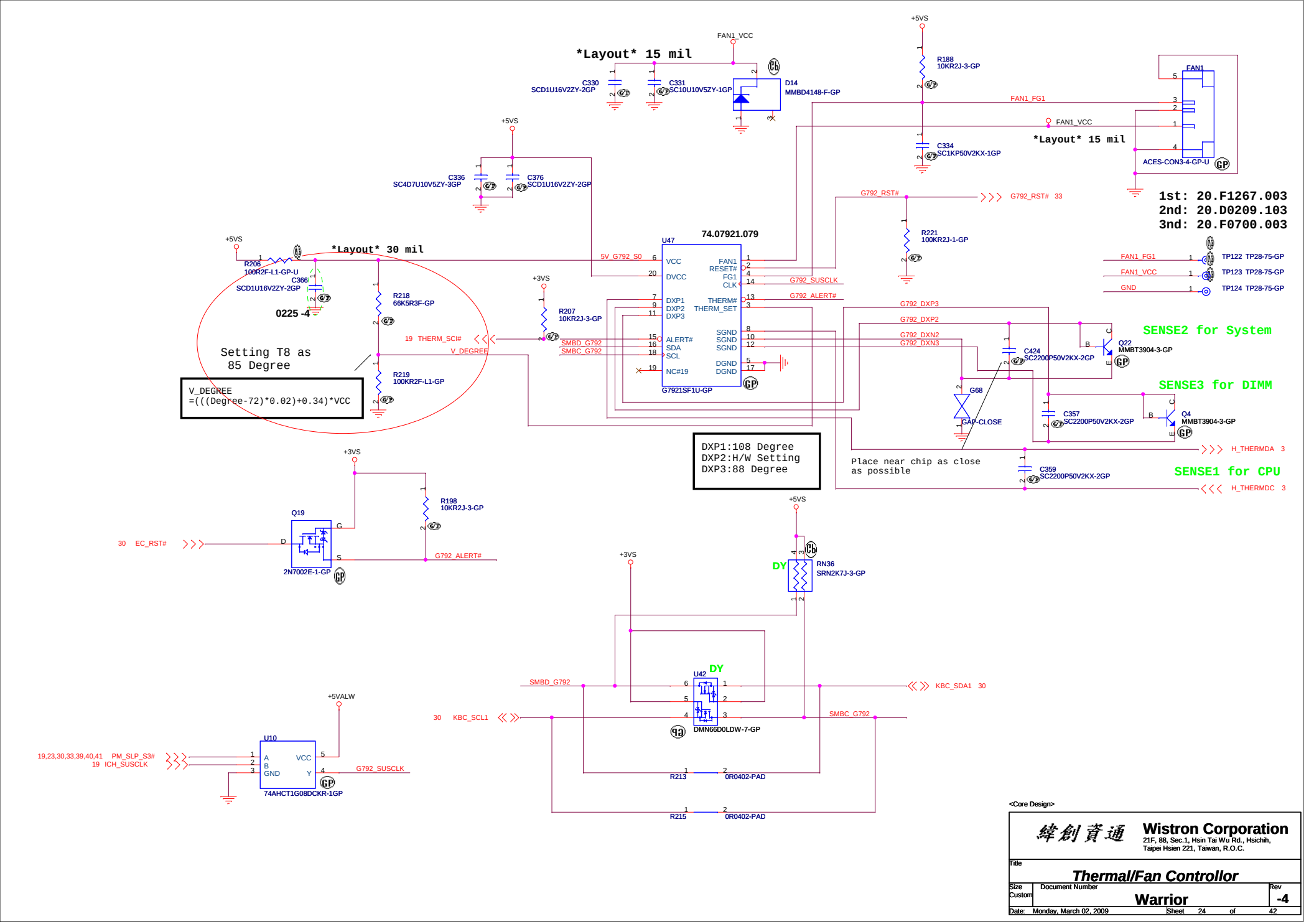


1st: 62.10065.351
2nd: 62.10065.421
3nd: 62.10065.521

<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	HDD/CDROM/USB/BT	
Size A3	Document Number: Warrior	Rev: -4
Date: Monday, March 02, 2009	Sheet 22 of 42	





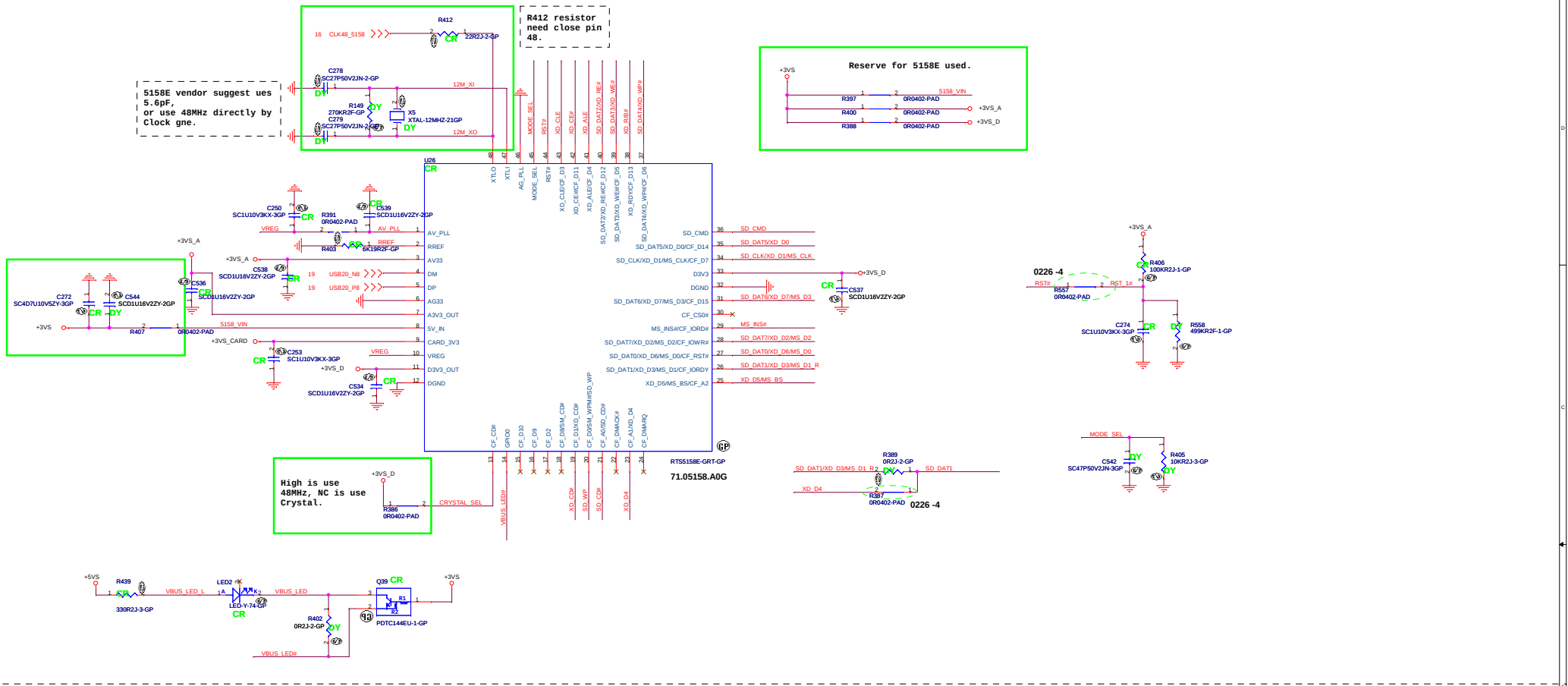
<Core Design>

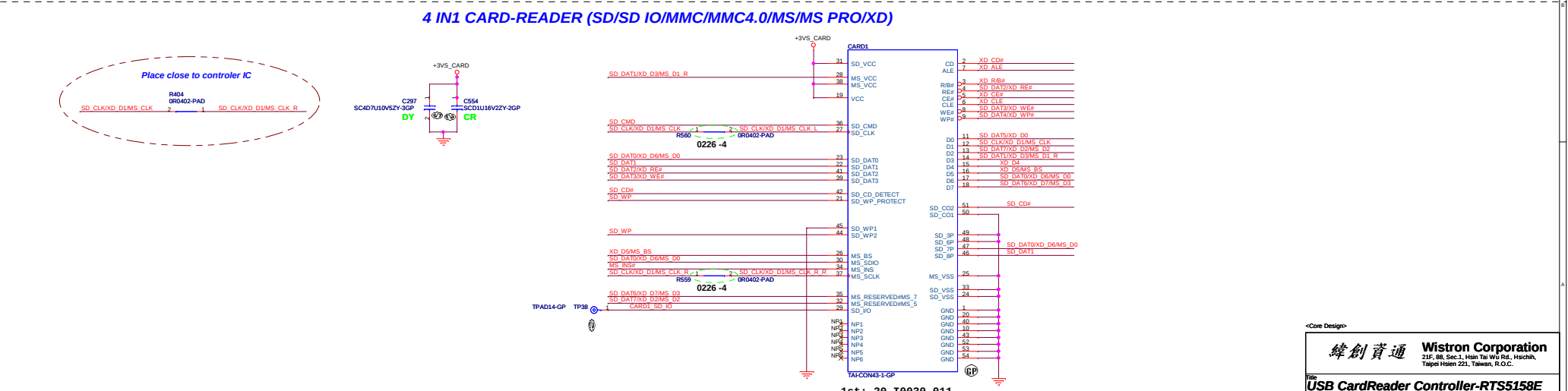
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor

Size	Document Number	Rev
Custom	Warrior	-4

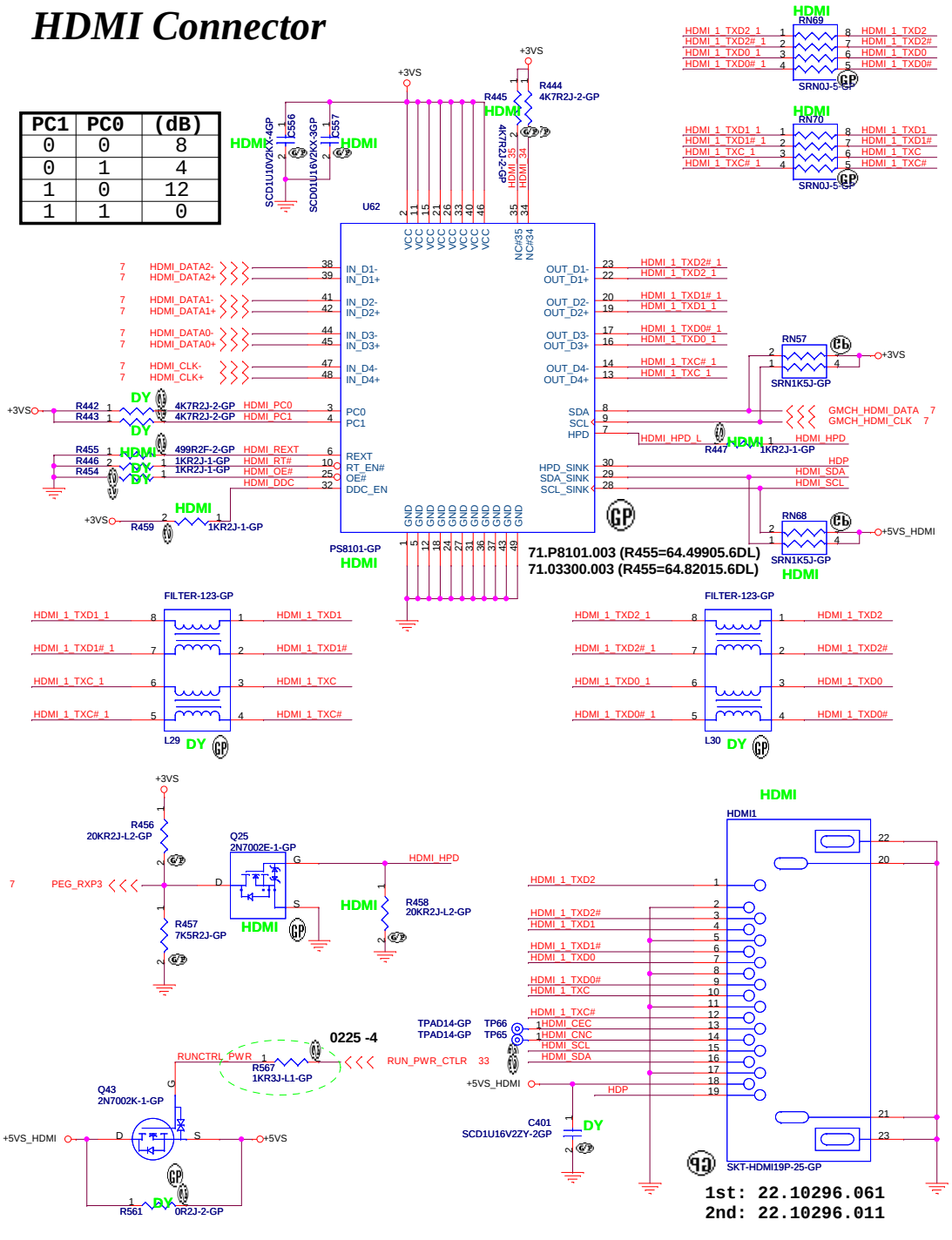
Date: Monday, March 02, 2009 Sheet 24 of 42



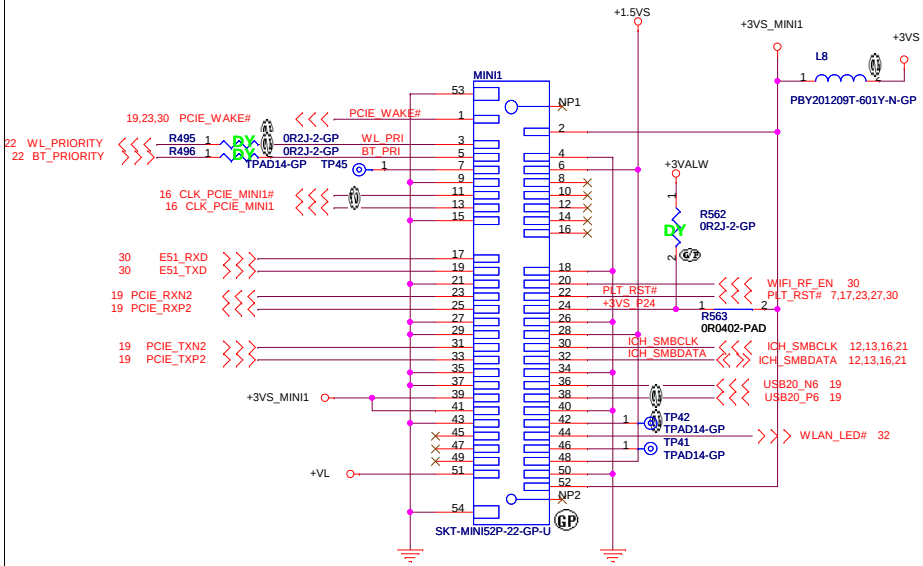


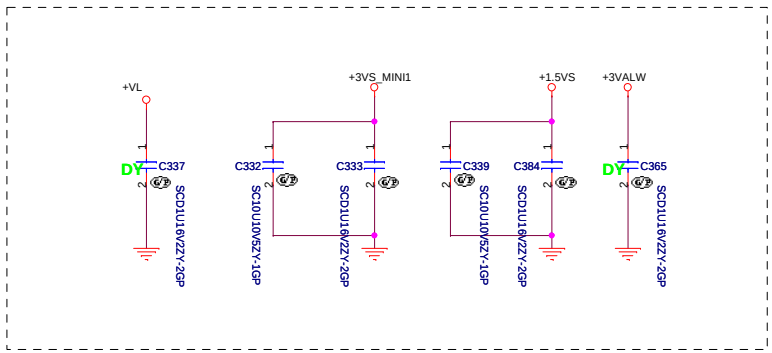
HDMI Connector

PC1	PC0	(dB)
0	0	8
0	1	4
1	0	12
1	1	0



Mini Card Connector1(802.11a/b/g)





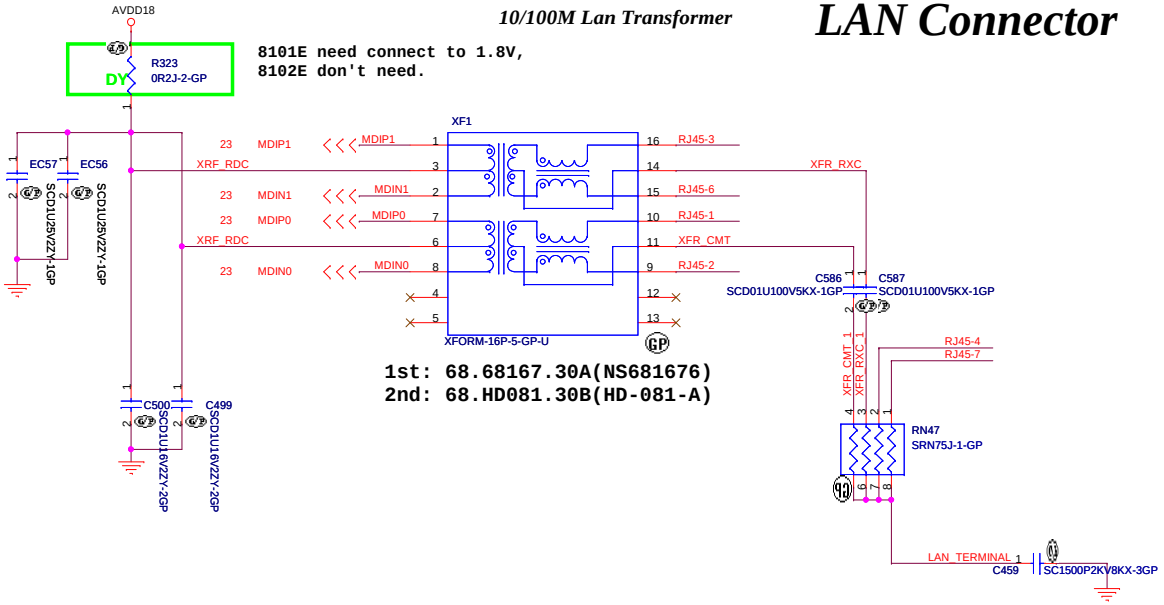
<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***MINI CARD/HDMI CONN .***
Size A3 / Document Number	**Warrior** / Rev **-4**
Date: Monday, March 02, 2009	Sheet 26 of 42

LAN Connector

10/100M Lan Transformer

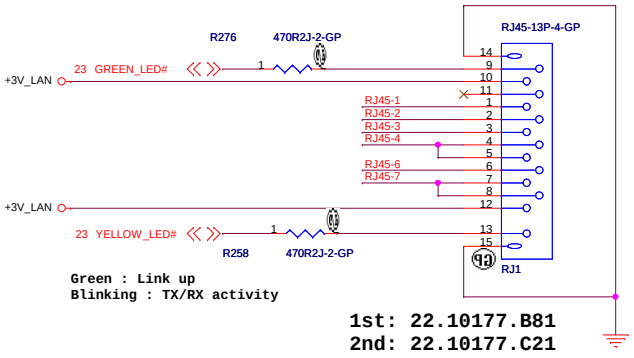
8101E need connect to 1.8V,
8102E don't need.



1st: 68.68167.30A(NS681676)
2nd: 68.HD081.30B(HD-081-A)

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

PIN A1 : GREEN
PIN A3 : ORANGE
PIN B2 : YELLOW



Green : Link up
Blinking : TX/RX activity

1st: 22.10177.B81
2nd: 22.10177.C21

Remark:
Add trace width to 20mils
for RJ1 pin4, 5 and pin 7, 8.

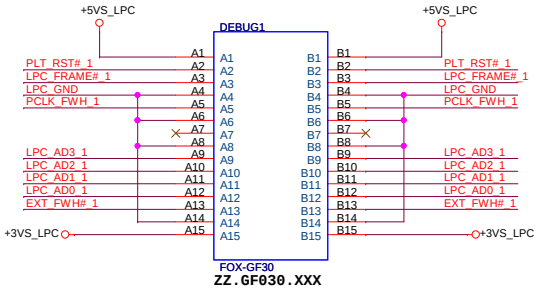
Golden Finger for Debug Board

TOP VIEW (A)

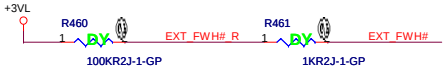
A15 (B1)
A14 (B2)
A2 (B14)
A1 (B15)

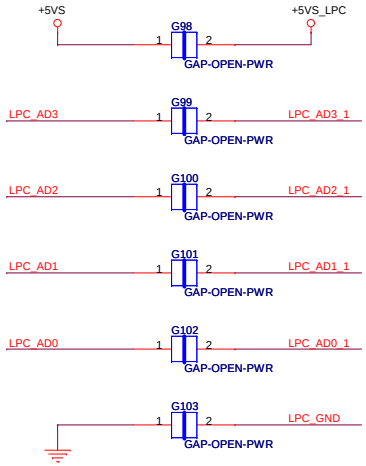
BOTTOM VIEW (B)

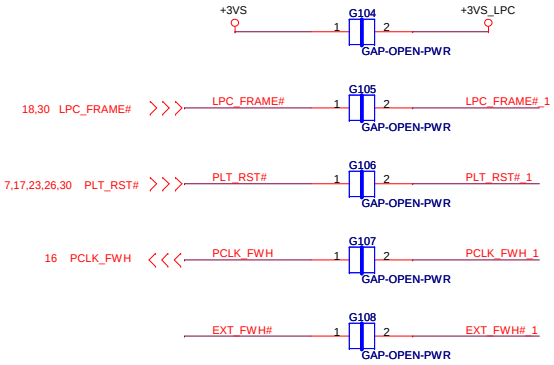
Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46



Please put near board edge.



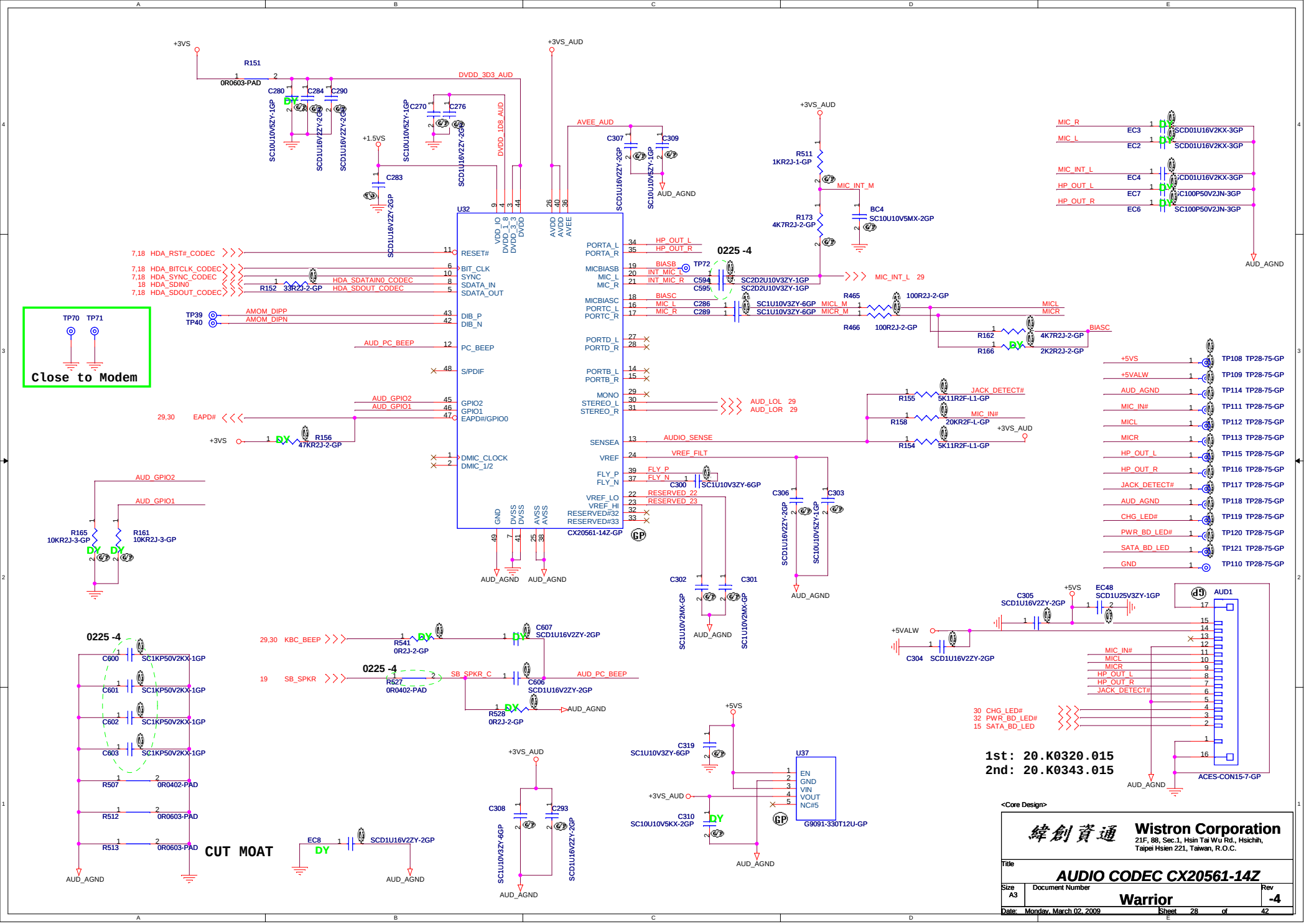


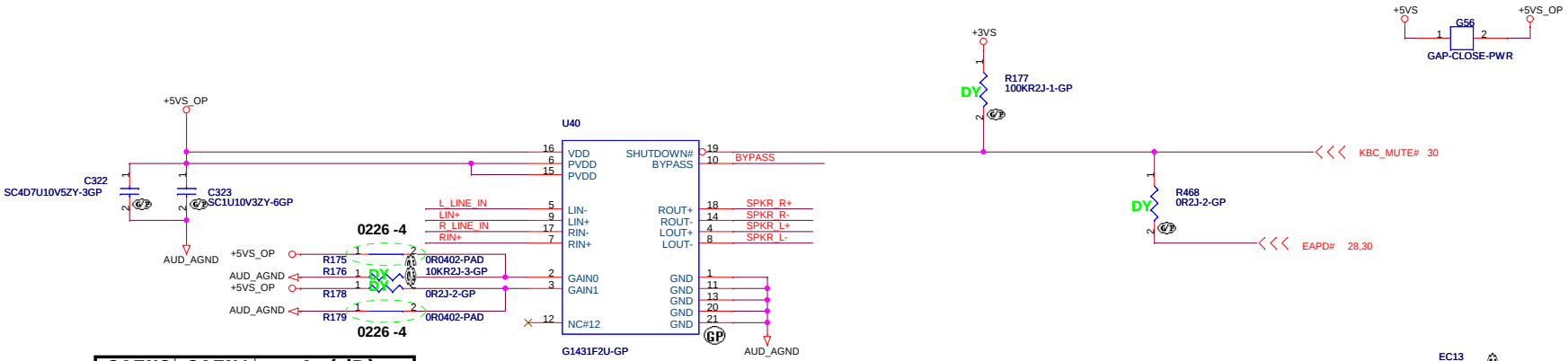


<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***LAN CONN/Debug***
Size A3 / Document Number	**Warrior** / Rev **-4**
Date: Monday, March 02, 2009	Sheet 27 of 42

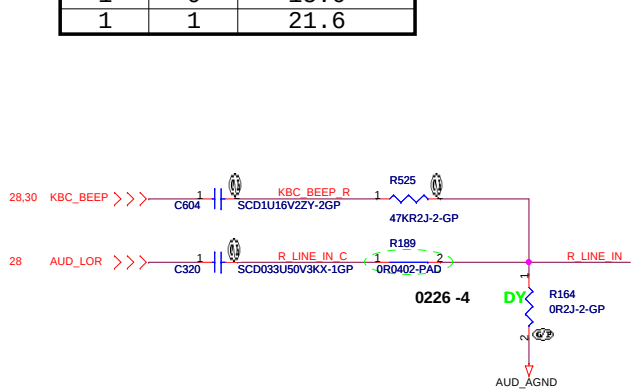
CLOSE TO TRANSFORMER

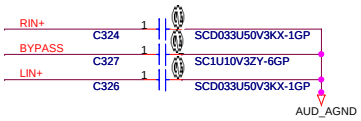


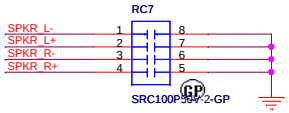


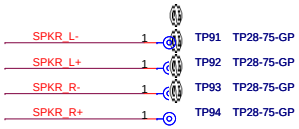
GAIN0	GAIN1	Av(dB)
0	0	6
0	1	10
1	0	15.6
1	1	21.6

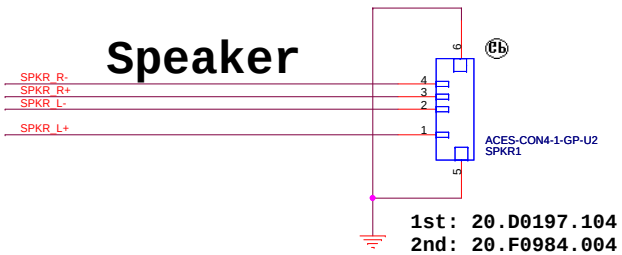
1st: 74.01431.A1G(GMT)
2nd: 74.06017.A1G(TI)



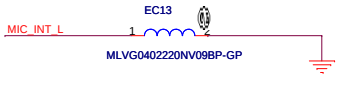


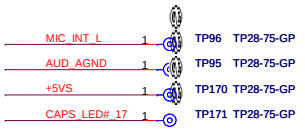


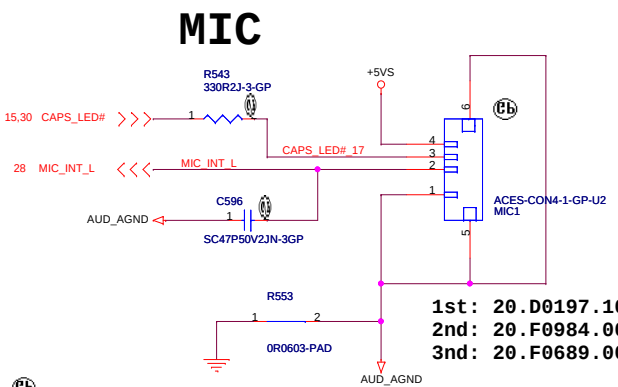




1st: 20.D0209.104
2nd: 20.F0984.004
3nd: 20.D0197.104







1st: 20.D0197.104
2nd: 20.F0984.004
3nd: 20.F0689.004

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO AMP/SPEAKER

Size	Document Number	Rev
A3	Warrior	-4

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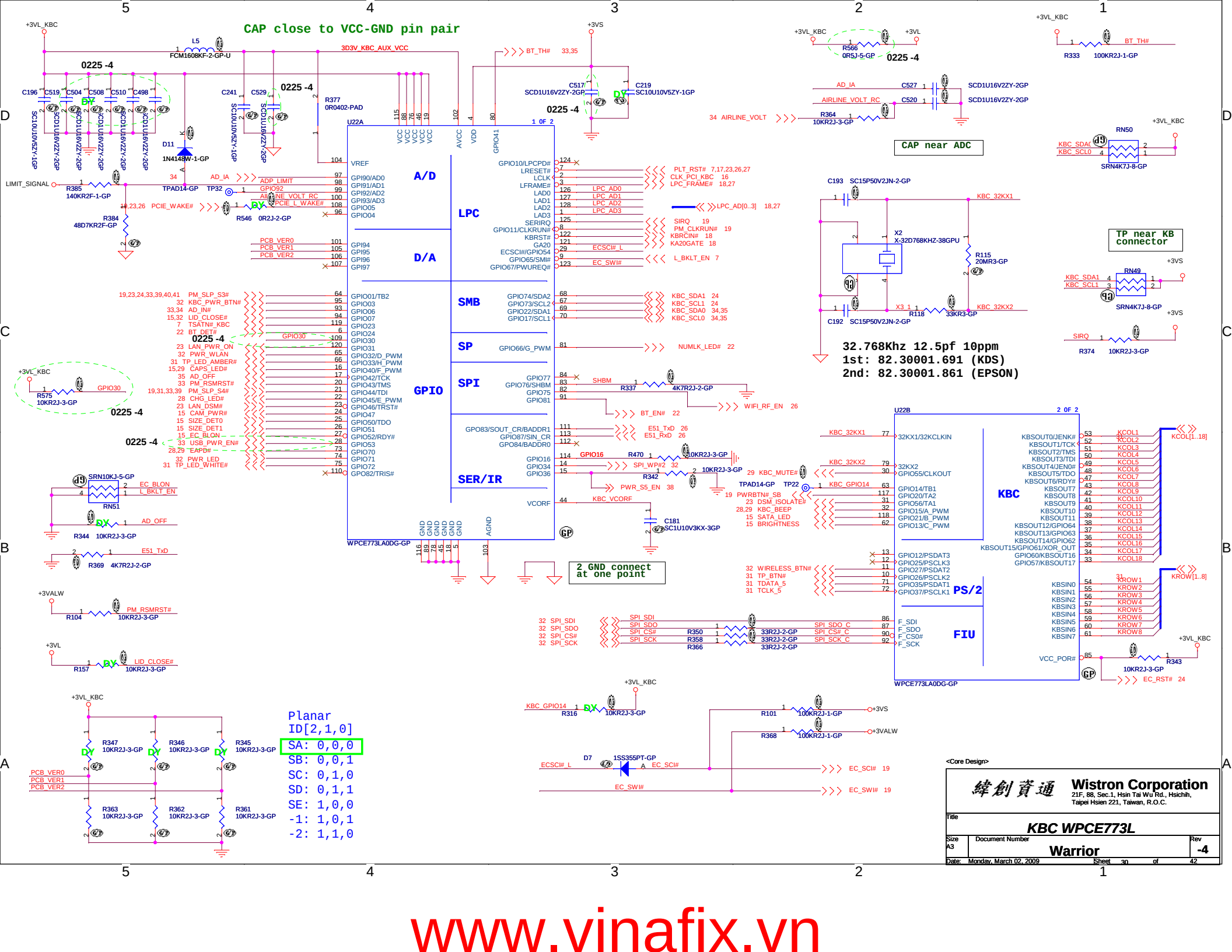
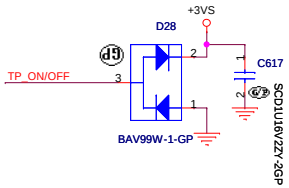
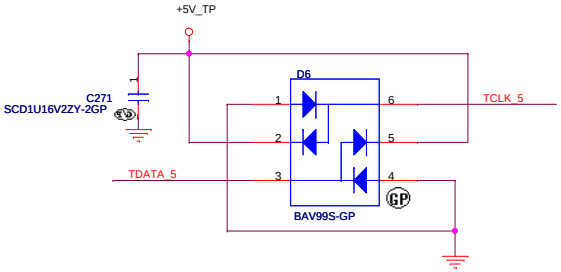


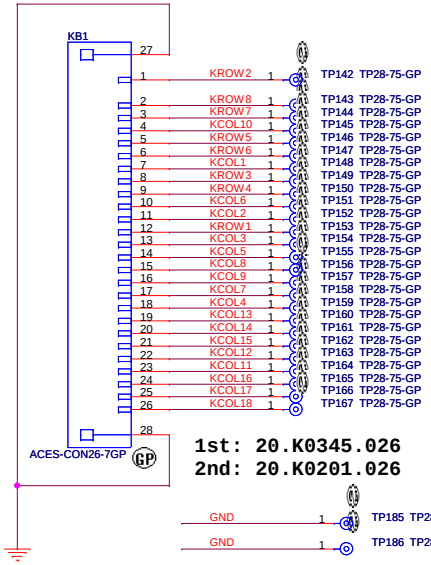
Internal KeyBoard Connector

Keyboard matrix (from vendor)

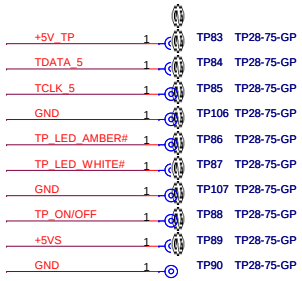
	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1



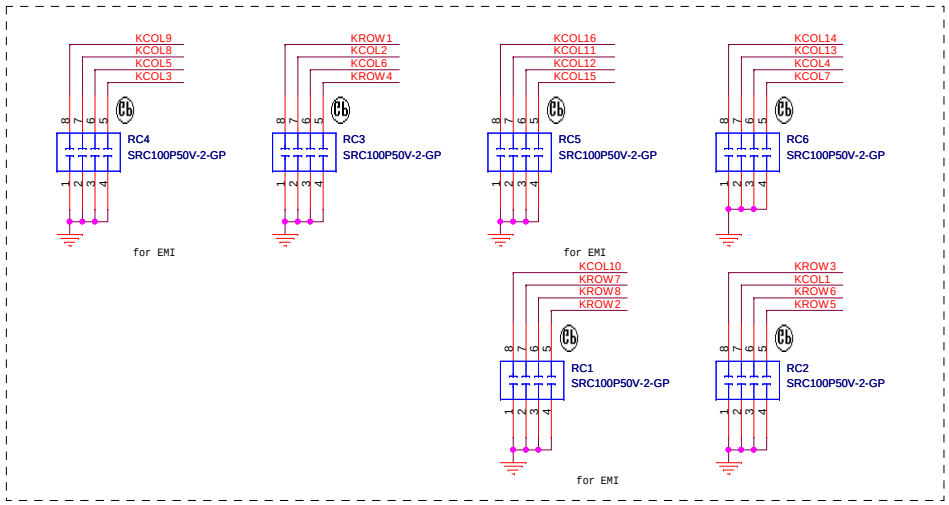




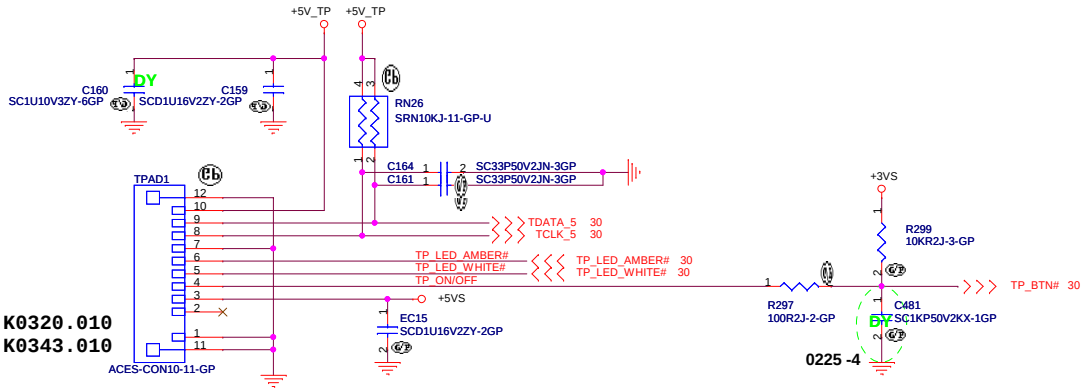
1st: 20.K0345.026
2nd: 20.K0201.026



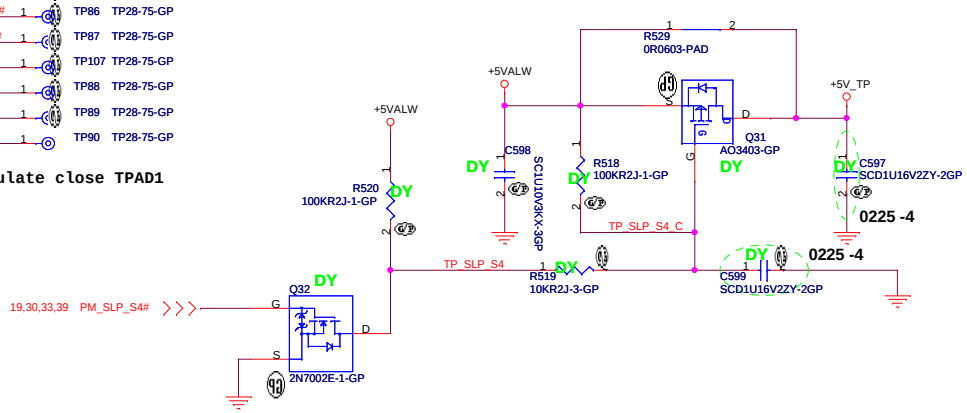
Please populate close TPAD1



TouchPad Connector



1st: 20.K0320.010
2nd: 20.K0343.010



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KeyBoard-CONN

Size: A3 | Document Number: Warrior | Rev: -4

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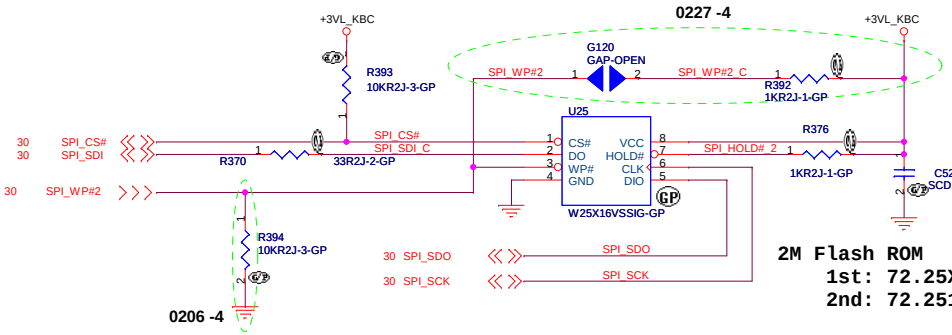
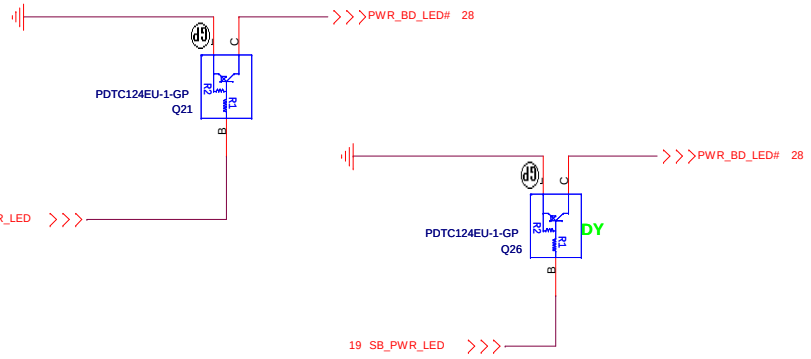
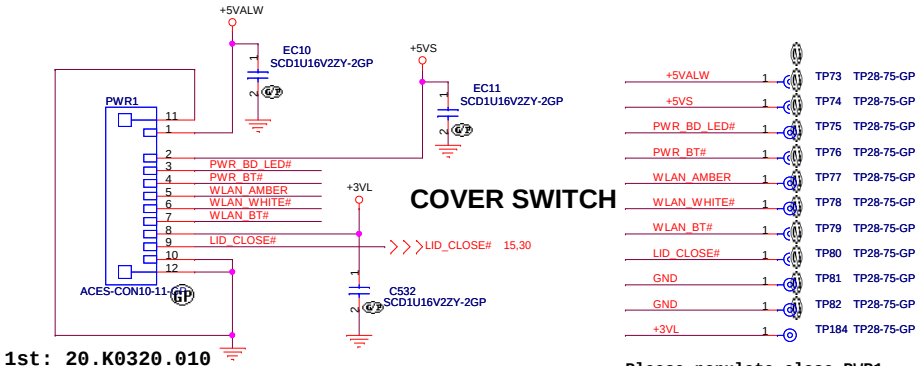


2M Flash ROM
1st: 72.25X16.A01
2nd: 72.25165.A01

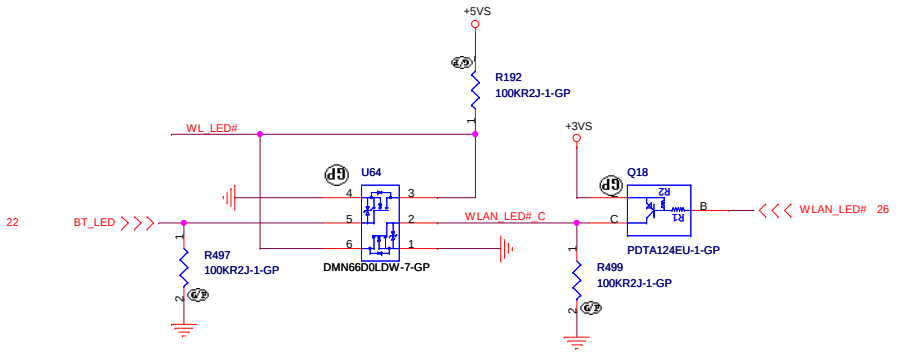




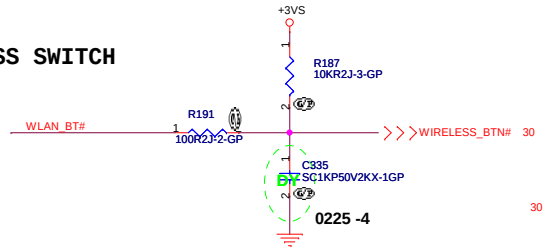
COVER SWITCH

1st: 20.K0320.010
2nd: 20.K0343.010

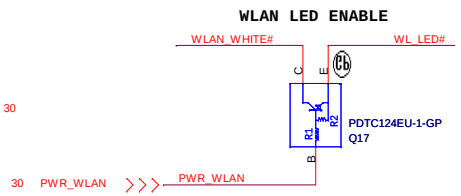
Please populate close PWR1



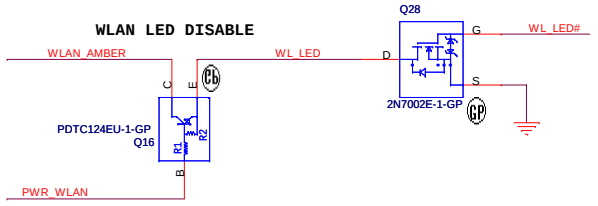
WIRELESS SWITCH

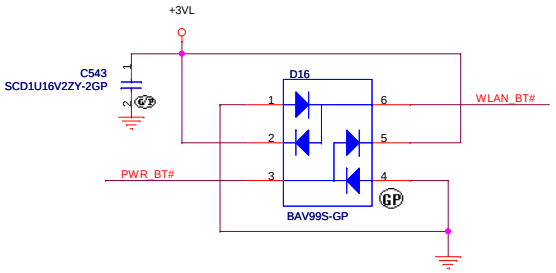


WLAN LED ENABLE

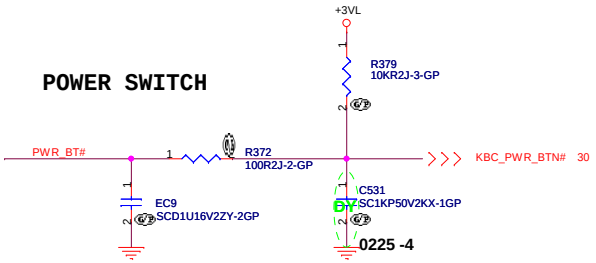


WLAN LED DISABLE





POWER SWITCH



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: FWH and CONN.

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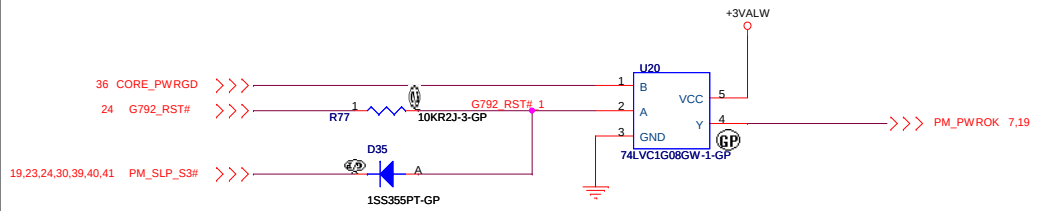
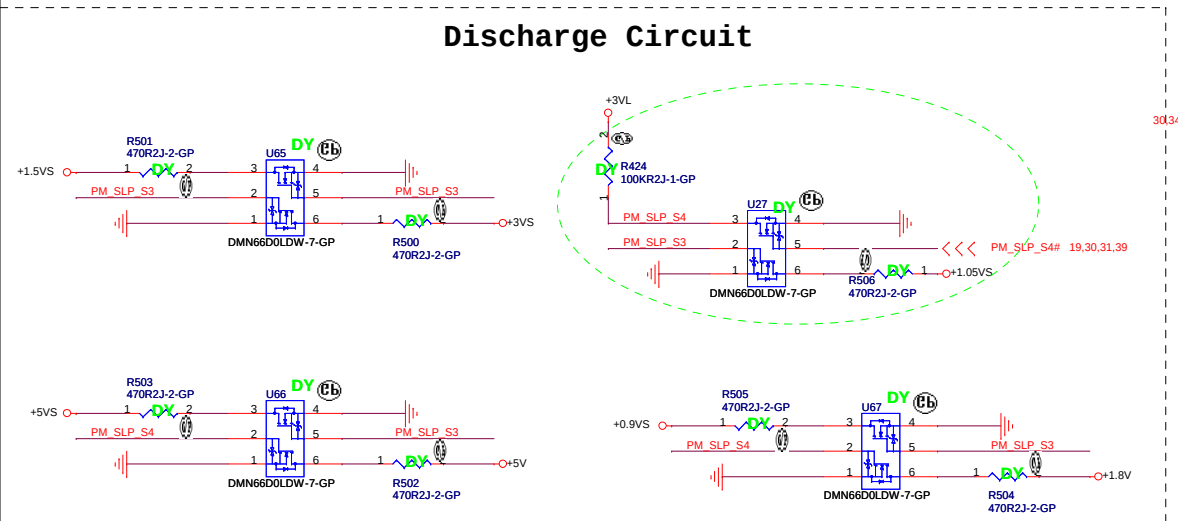
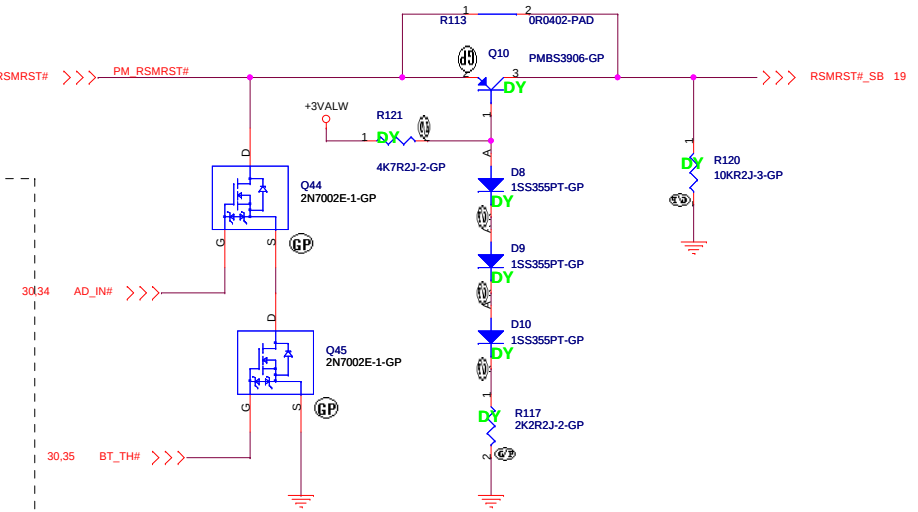


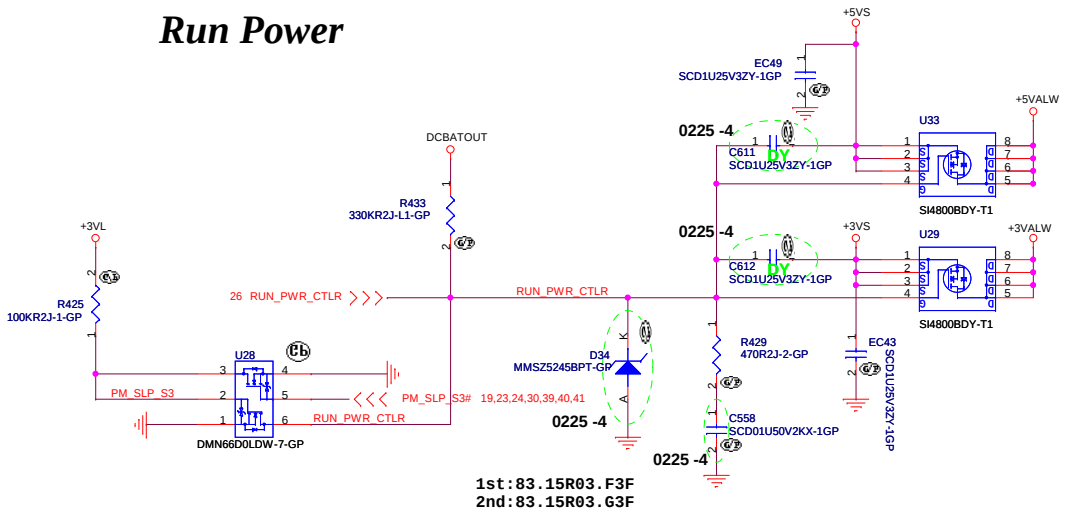




0523 SF

+5VALW to +5VS Transfer
+3VALW to +3VS Transfer

Run Power



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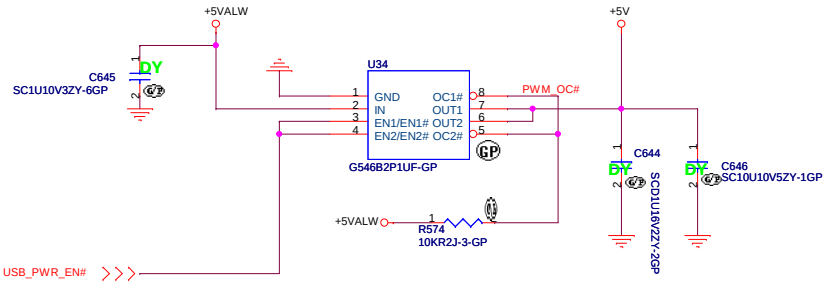
+5VALW to +5V Transfer

G546B2P1 Low active, 1.5A per channel



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Title	***PWRPLANE***
Size A3 / Document Number	**Warrior** / Rev **-4**
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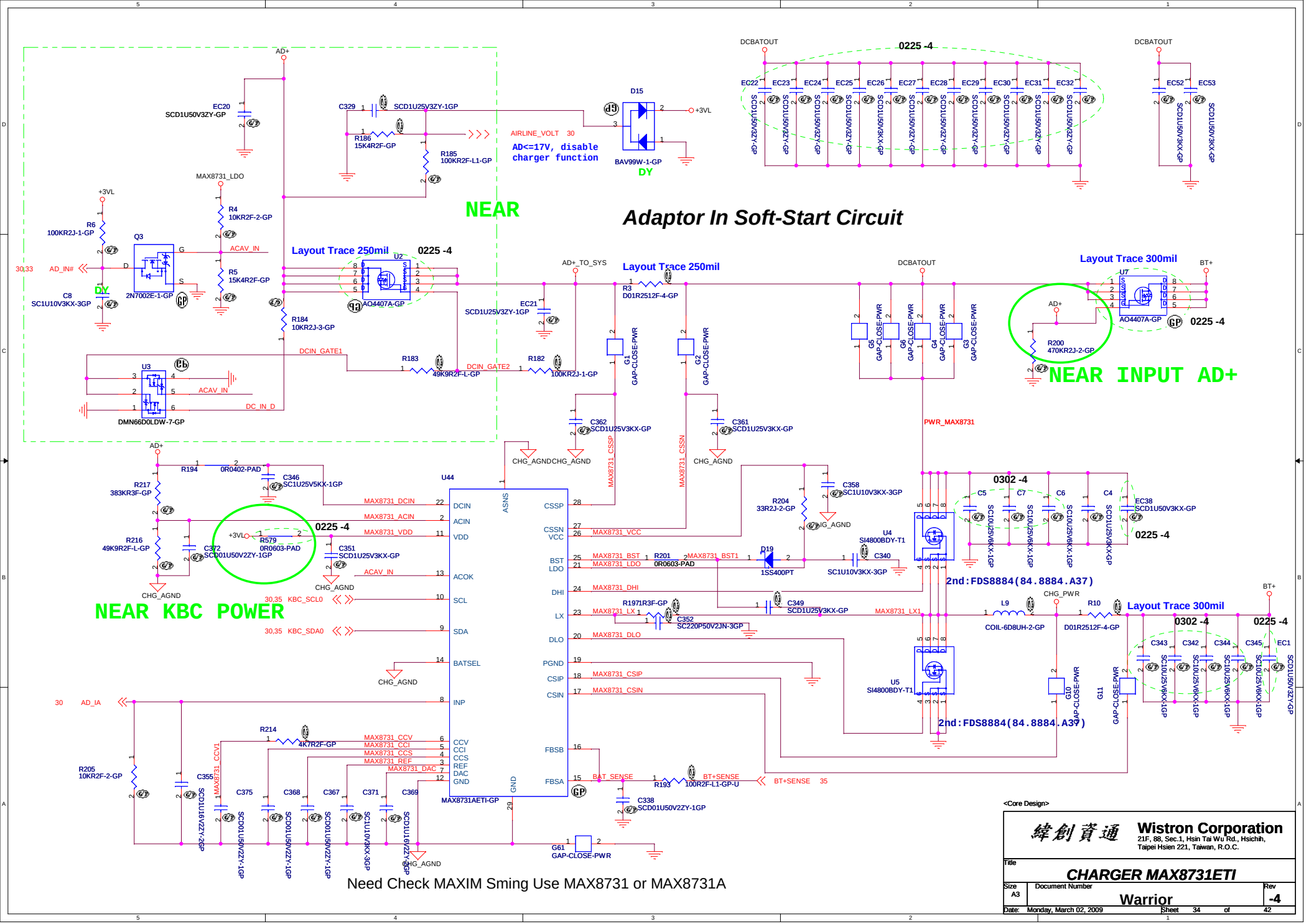
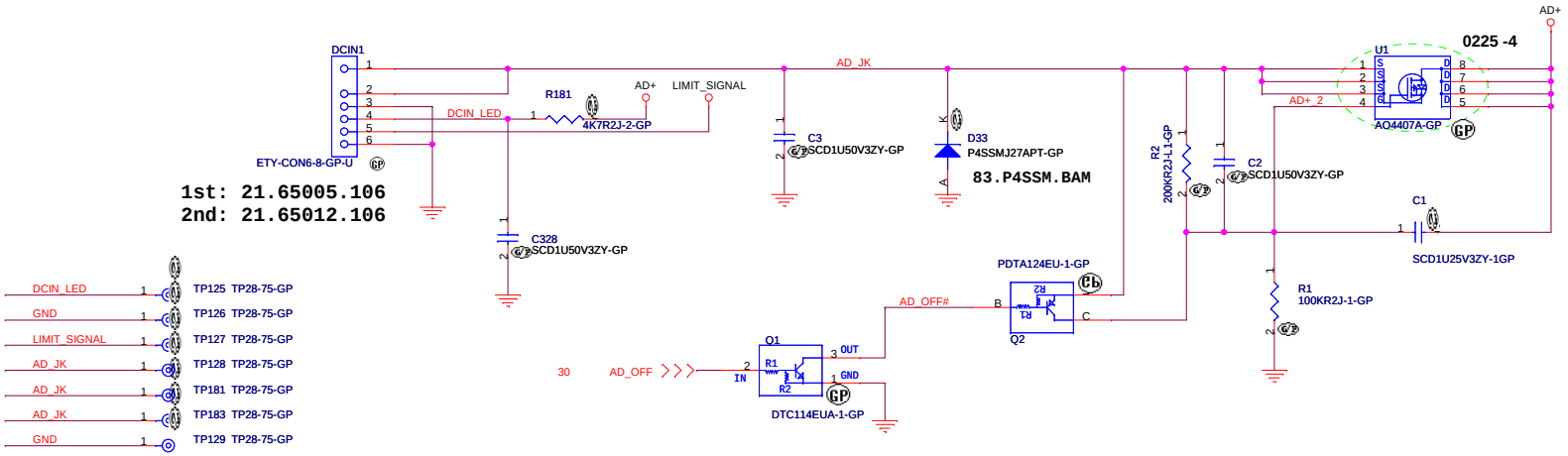
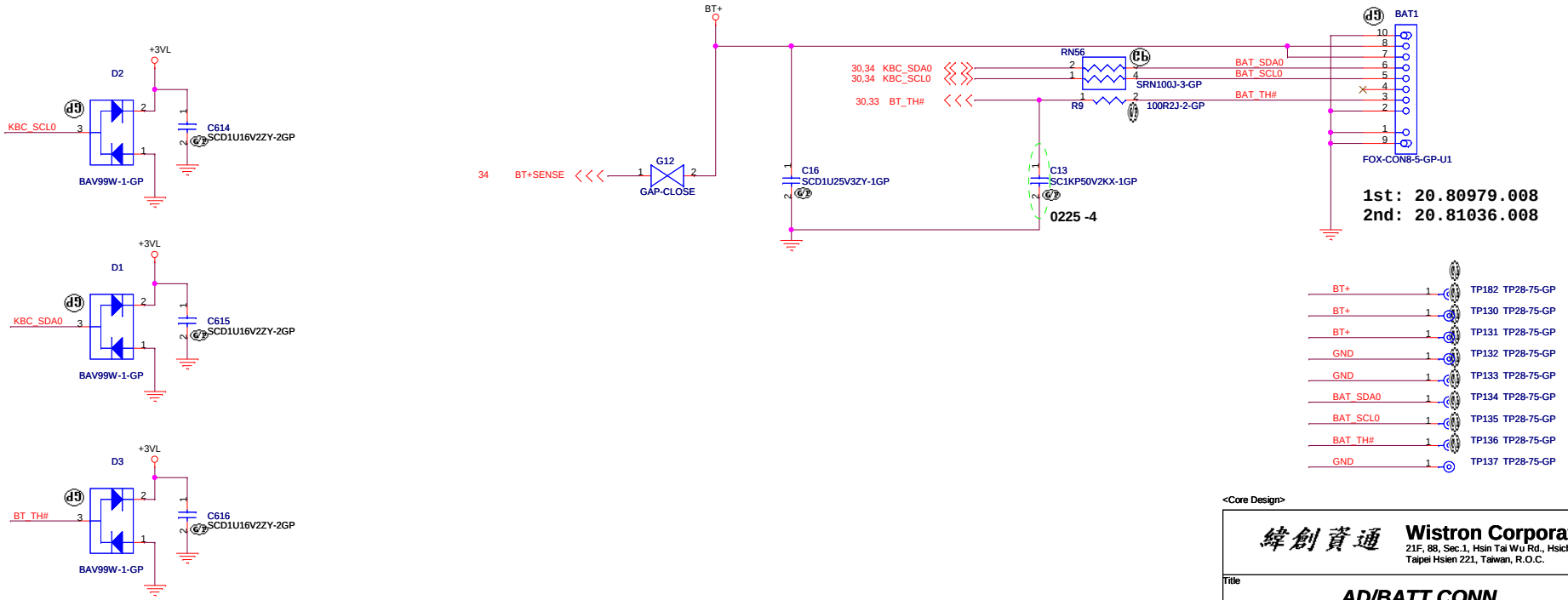


Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AD/BATT CONN***

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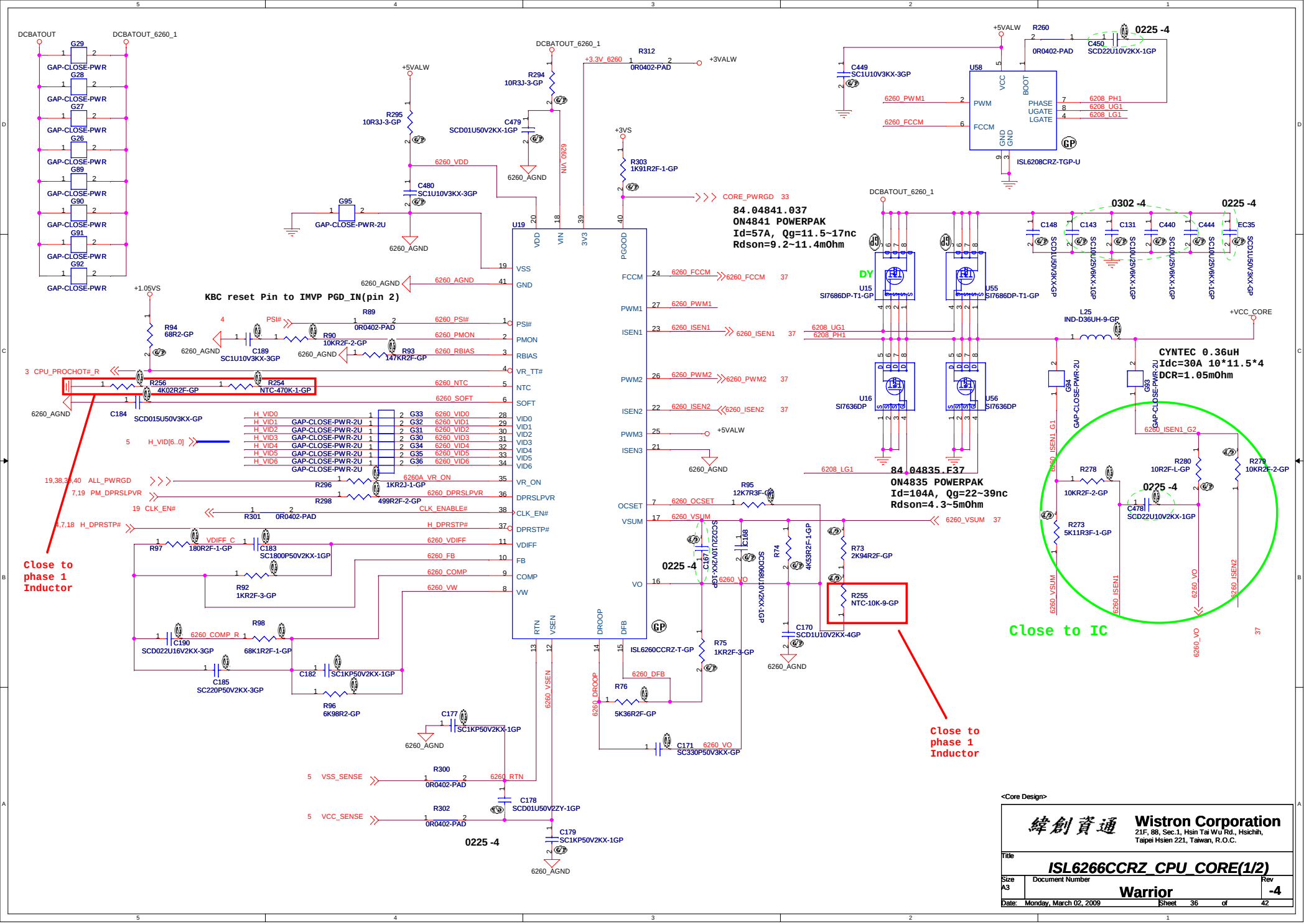

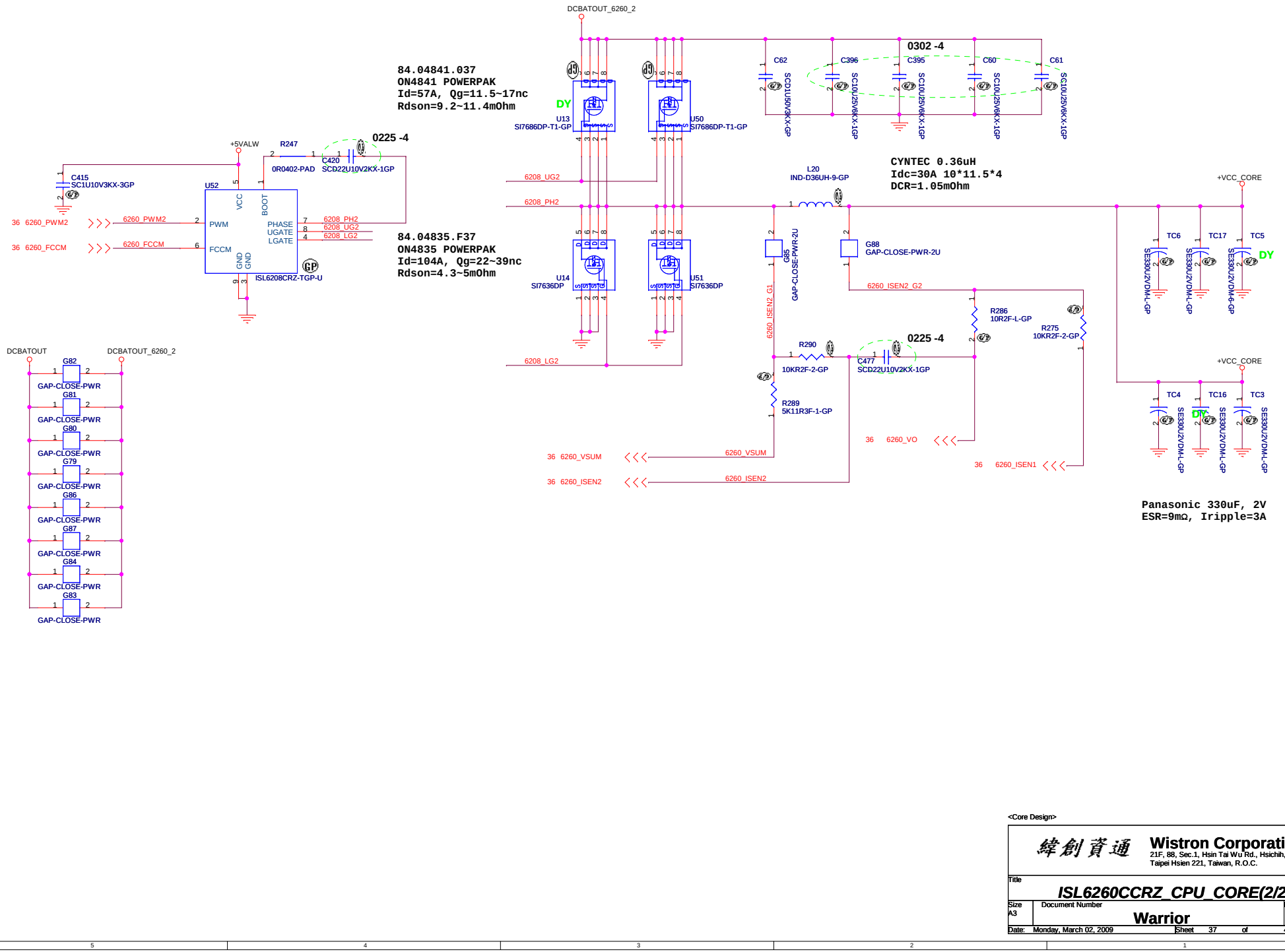

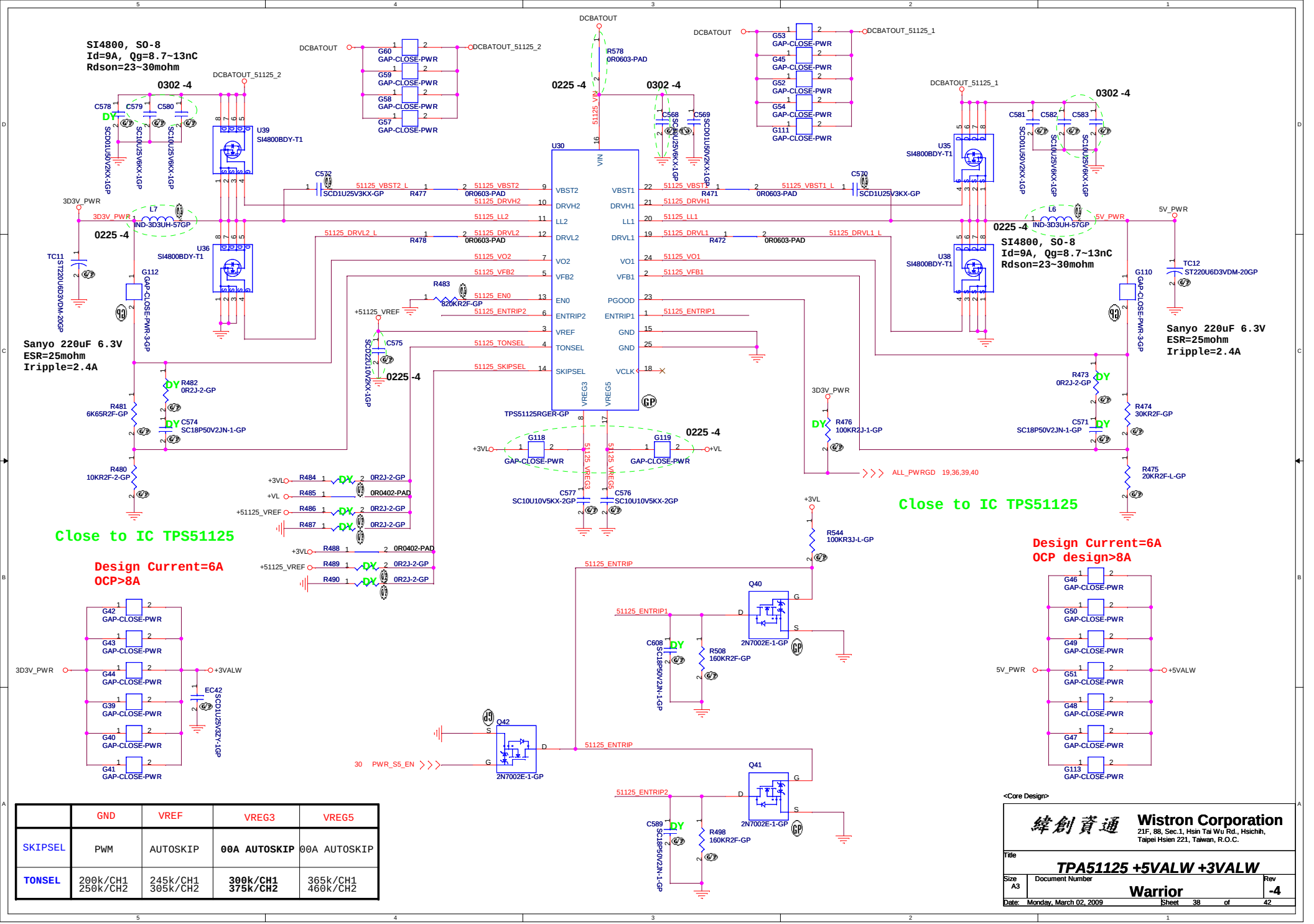

	GND	VREF	VREG3	VREG5
SKIPSEL	PWM	AUTOSKIP	**00A AUTOSKIP**	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	**300k/CH1** **375k/CH2**	365k/CH1 460k/CH2

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Title: **TPA51125 +5VALW +3VALW**

Size: A3 | Document Number: **Warrior** | Rev: **-4**

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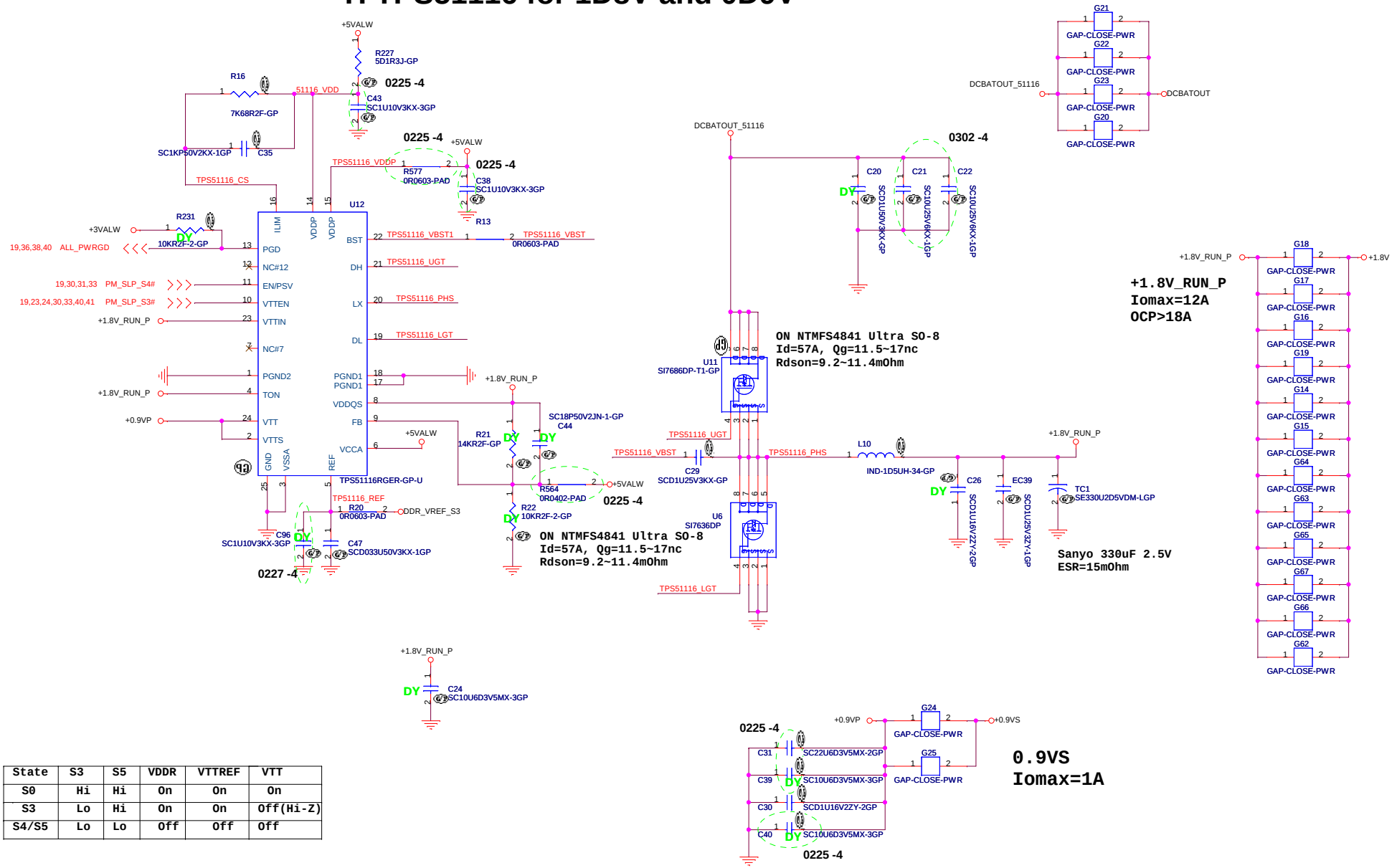
TI TPS51116 for 1D8V and 0D9V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

<Core Design>

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Title: ***TPS51116 1D8V/0D9V***

Size: A3 | Document Number: **Warrior** | Rev: **-4**

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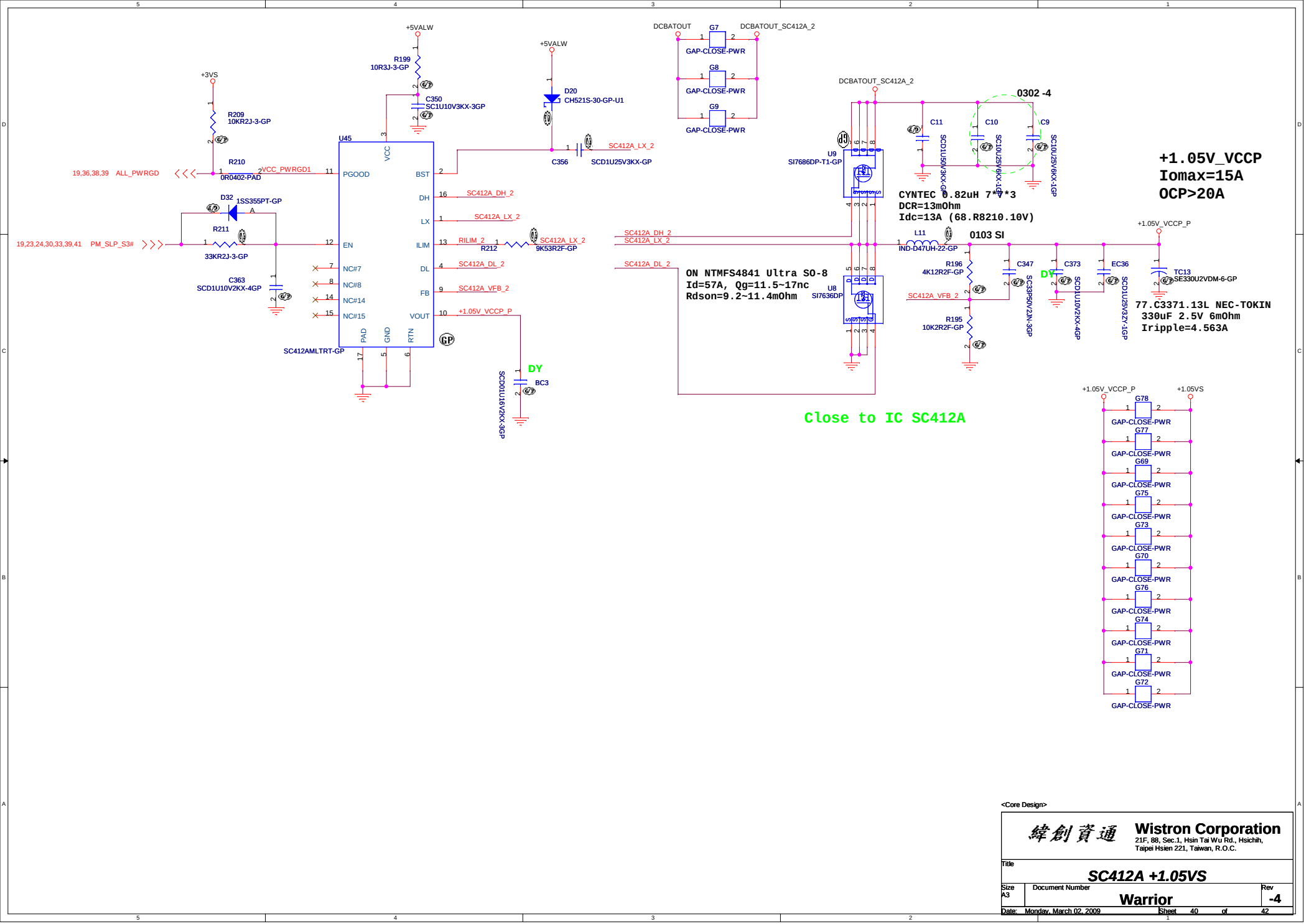

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Title: **SC412A +1.05VS**

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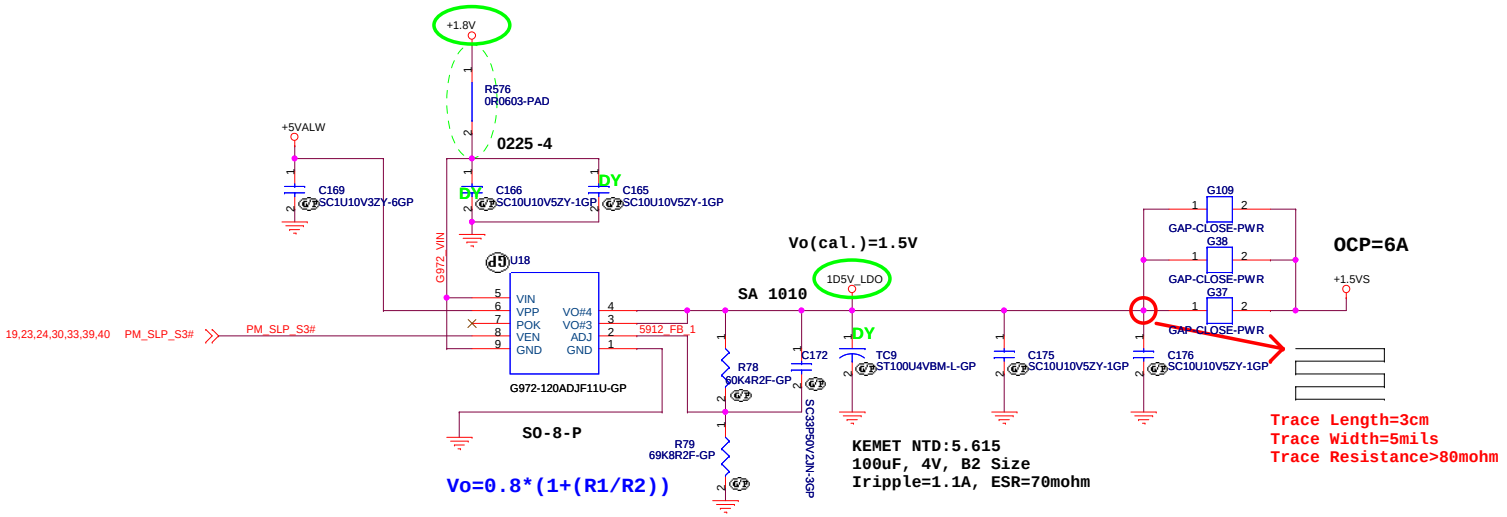

1st: 74.00972.031(GMT)
2nd: 74.05912.A71(Anpac)

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Taipei Hsien 221, Taiwan, R.O.C.

Title	GMT_1D5V_LDO	
Size A3	Document Number Warrior	Rev -4
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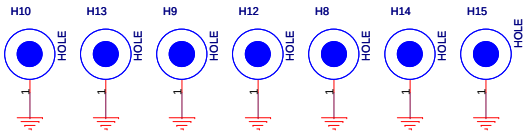

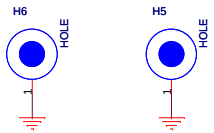

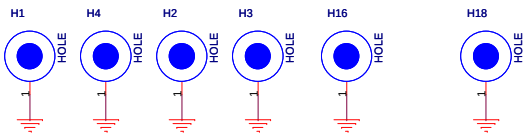

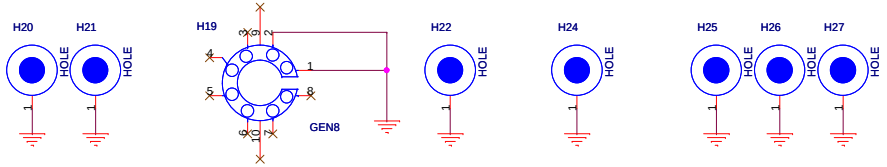

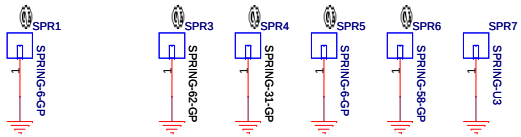

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SPR5: 34.13B01.001,
SPR6: 34.4B312.002, 34.4B312.101
SPR7: 34.40U07.001, 34.40U07.101

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Title: ***MISC***

Size	Document Number	Rev
A3	**Warrior**	**-4**

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