

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : SGND1
LAYER 3 : IN1
LAYER 4 : SVCC
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : SGND2
LAYER 8 : BOT

PCI DEVICES IRQ ROUTING

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
R5C832	AD17	REQ0# / GNT0#	INT A/B#

CPU CORE MAX8736
PAG 40

SYSTEM POWER MAX8734
PAG 41

DDR II SMDR_VTERM
1.8V/1.8VSUS(TPS51116)
PAG 42

VCCP +1.5V AND GMCH
1.05V(TPS51124)
PAG 43

VGACORE(1.025V)MAX1993
PAG 44

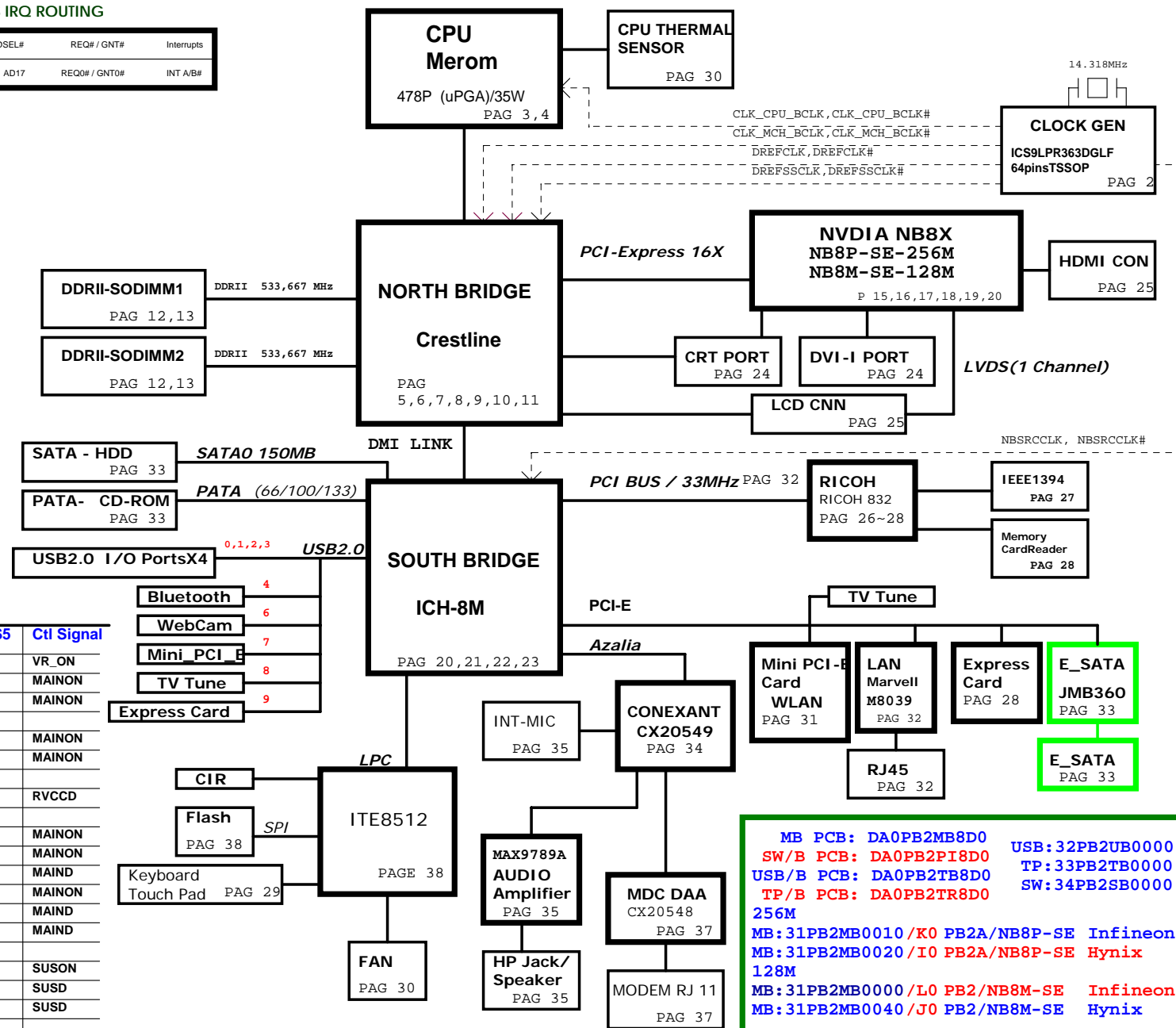
SYSTEM CHARGER(MAX8672)
PAG 45,46

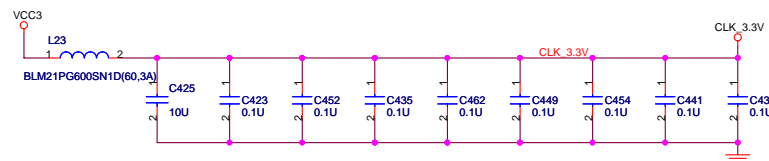
Voltage Rails

Voltage Rails	ON S0-S2	ON S3	ON S4	ON S5	Ctl Signal
VCC_CORE	X				VR_ON
VCCP	X				MAINON
SMDR_VTERM	X				MAINON
VGACORE	X				MAINON
VGA1.2	X				MAINON
RVCC3	X	X	X		RVCCD
VCC1.25	X				MAINON
VCC1.5	X				MAINON
VCC1.8	X				MAIND
VCC2.5	X				MAINON
VCC3	X				MAIND
VCC5	X				MAIND
1.8VSUS	X	X			SUSON
3VSUS	X	X			SUSD
5VSUS	X	X			SUSD
3VPCU	X	X	X	X	8734LDO5
5VPCU	X	X	X	X	8734LDO5
15VPCU	X	X	X	X	5VPCU

PB2/PB2A BLOCK DIAGRAM

01

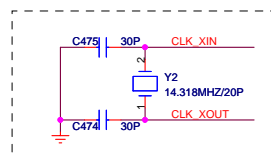




14.318MHz

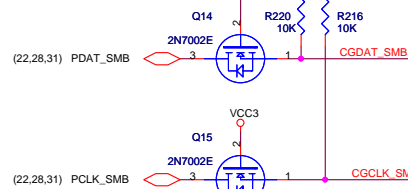
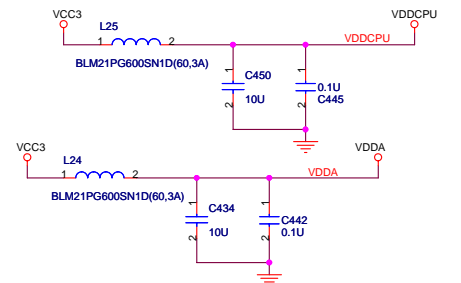
BG614318Q33

XTL-5_3X3_2-3_8-1_2H

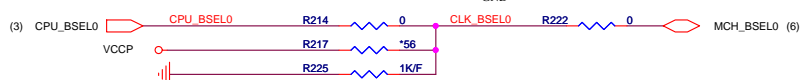


FCE P/N:BG614318F84

P/N:BG614318Q33



CPU Clock select



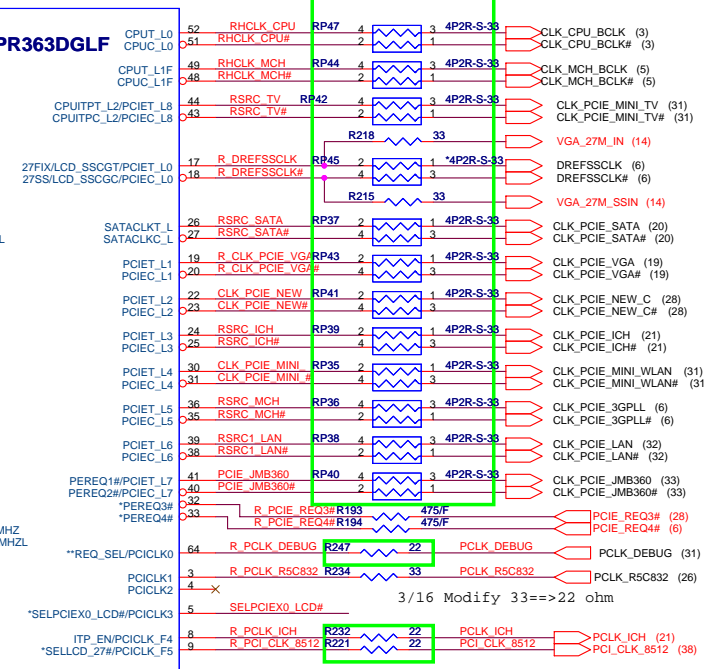
* Internal pull up to VDD
** Internal pull down to GND

FSC BSEL2	FSB BSEL1	FSA BSEL0	CPU	SRC	PCI	REF	USB	DOT	Spread %
0	0	0	266.66	100	33.33	14.318	48	96	0.5 Down
0	0	1	133.33	100	33.33	14.318	48	96	0.5 Down
* 0	1	0	200.00	100	33.33	14.318	48	96	0.5 Down
0	1	1	166.66	100	33.33	14.318	48	96	0.5 Down
1	0	0	333.33	100	33.33	14.318	48	96	0.5 Down
1	0	1	100.00	100	33.33	14.318	48	96	0.5 Down
1	1	0	400.00	100	33.33	14.318	48	96	0.5 Down
1	1	1	200.00	100	33.33	14.318	48	96	0.5 Down

R_PCLK_DEBUG
H: PEREQ
L: PCI_E

ITP_EN(PIN8)			
LOW : PIN43/44 SRC			
HIGH : PIN43,44 CPUITP			
PCIE_REQ1#	PCIE_L0	PCIE_L6	
PCIE_REQ2#	PCIE_L1	PCIE_L8	
PCIE_REQ3#	PCIE_L2	PCIE_L4	
PCIE_REQ4#	PCIE_L3	PCIE_L5	PCIE_L7

ICS9PR363DGLF

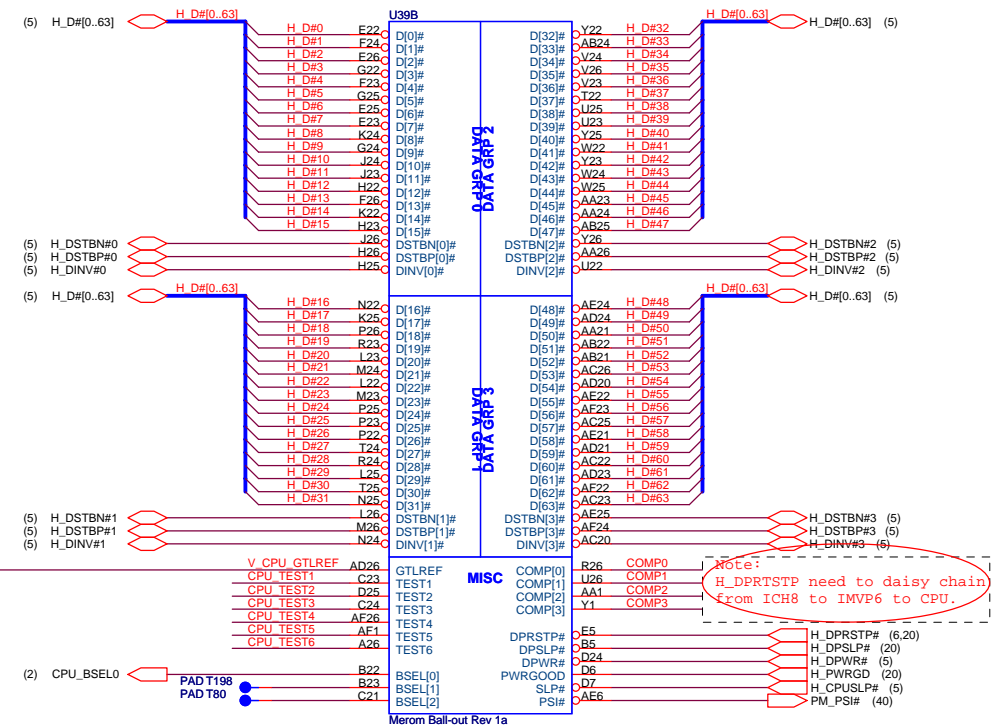
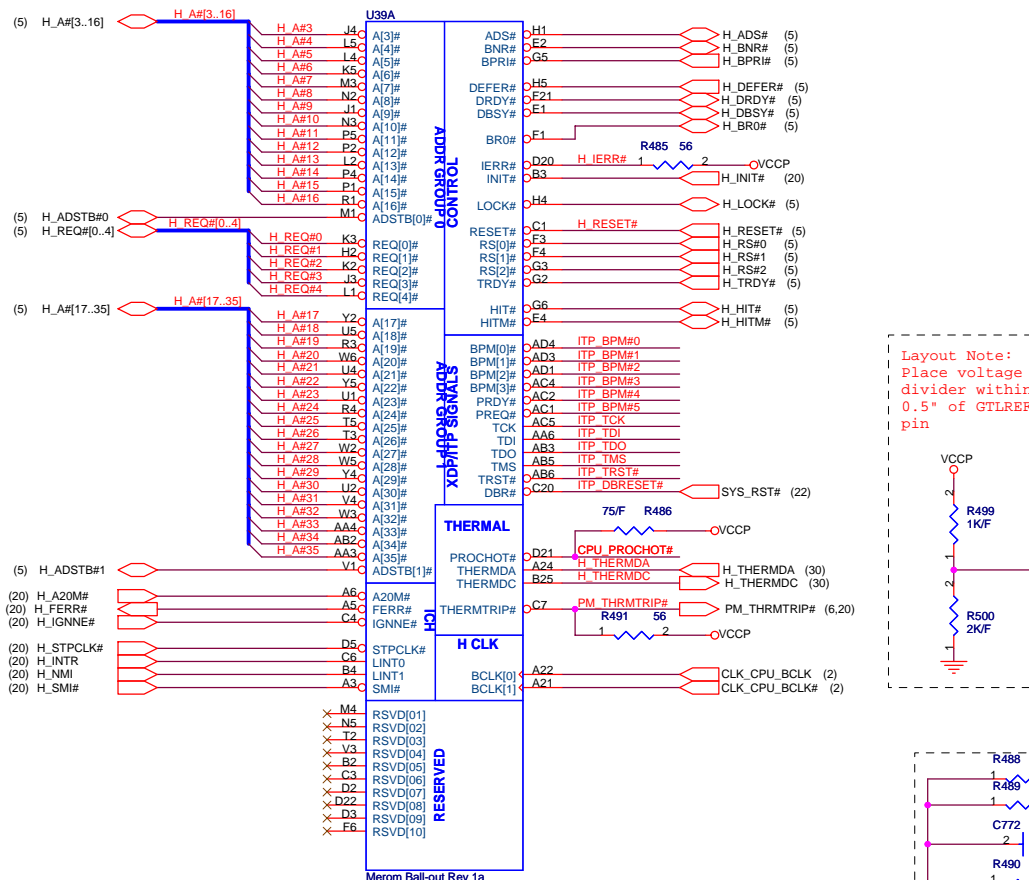


ALLPR363K00 P/N:ALLPR363K00 VER:D

10/24 modify

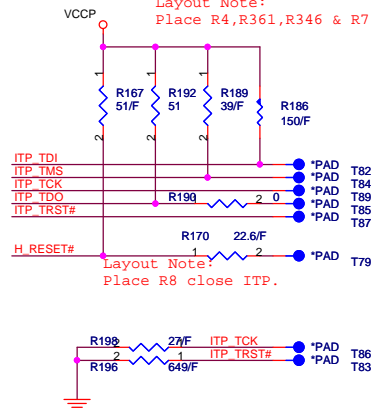
PIN 5	PIN 9	Pin14/15	Pin17/18/7
LO (10K)	LO (10K)	PCIE9	27M
HI (NC)	HI (NC)	DOT96	LCD
HI (NC)	LO (10K)	PCIE9	PCIE0
	HI (NC)	DOT96	PCIE0

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

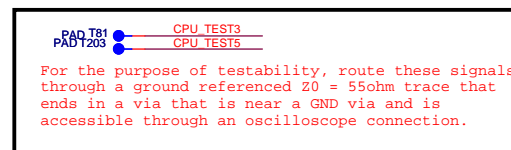
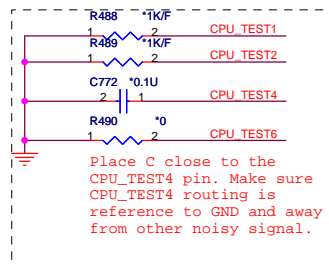
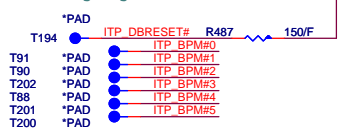


Populate ITP700Flex for bringup

Layout Note:
Place R4,R361,R346 & R7 close to CPU.



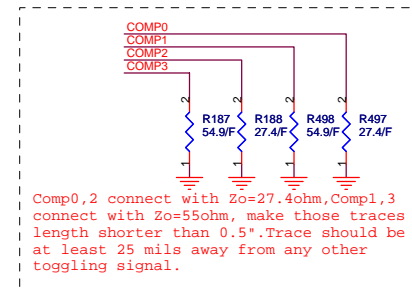
ITP debug signals

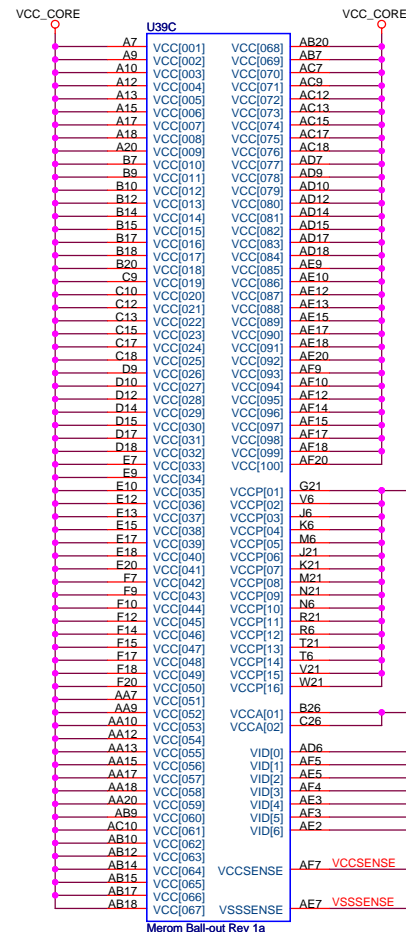
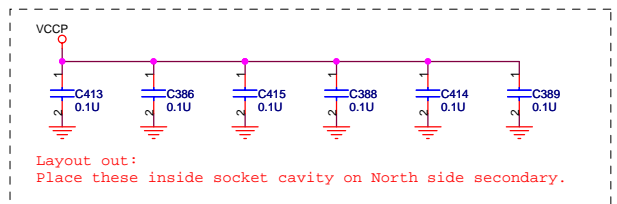
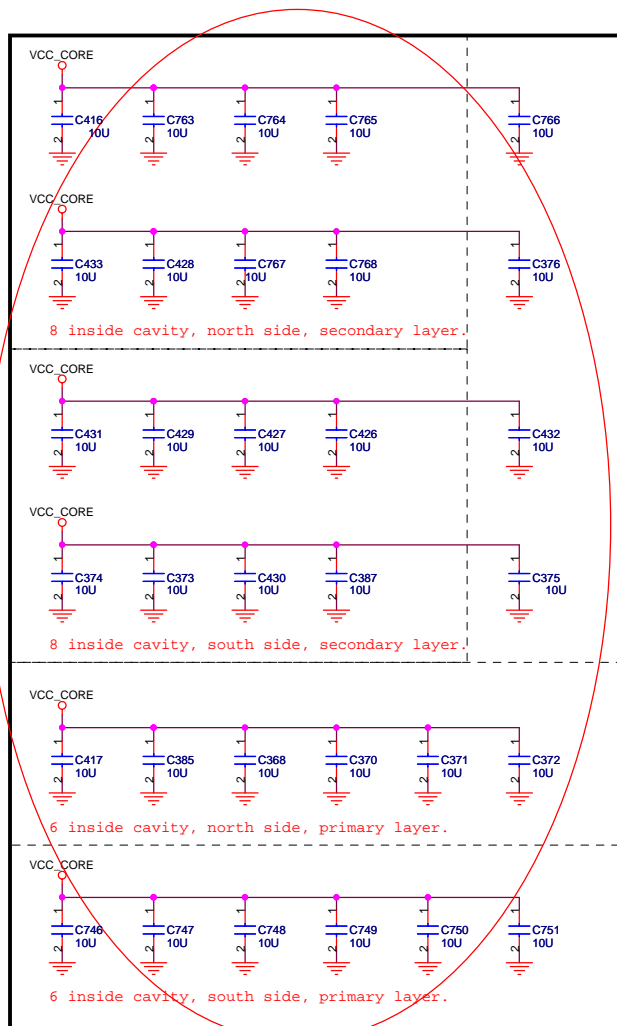


FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

ITP disable guidelines			
Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 1%	VTT	Within 2.0" of the ITP
TRST#	500-680ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 1%	GND	Within 2.0" of the ITP
TDO	150 ohm +/- 5%	VTT	Within 2.0" of the ITP

Note: Populate R5, R8, C372 & R430 when ITP connector is populated.

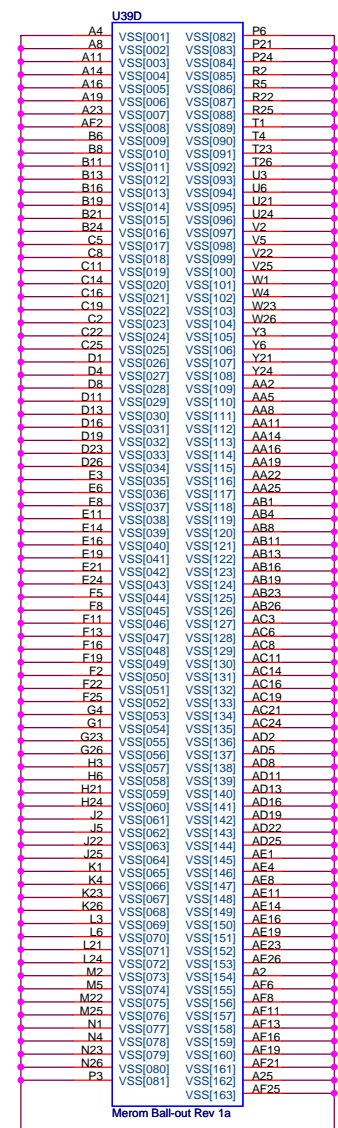
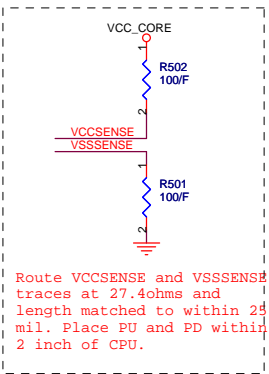
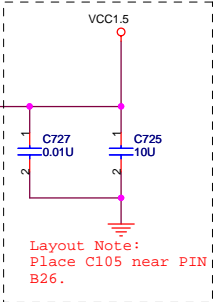


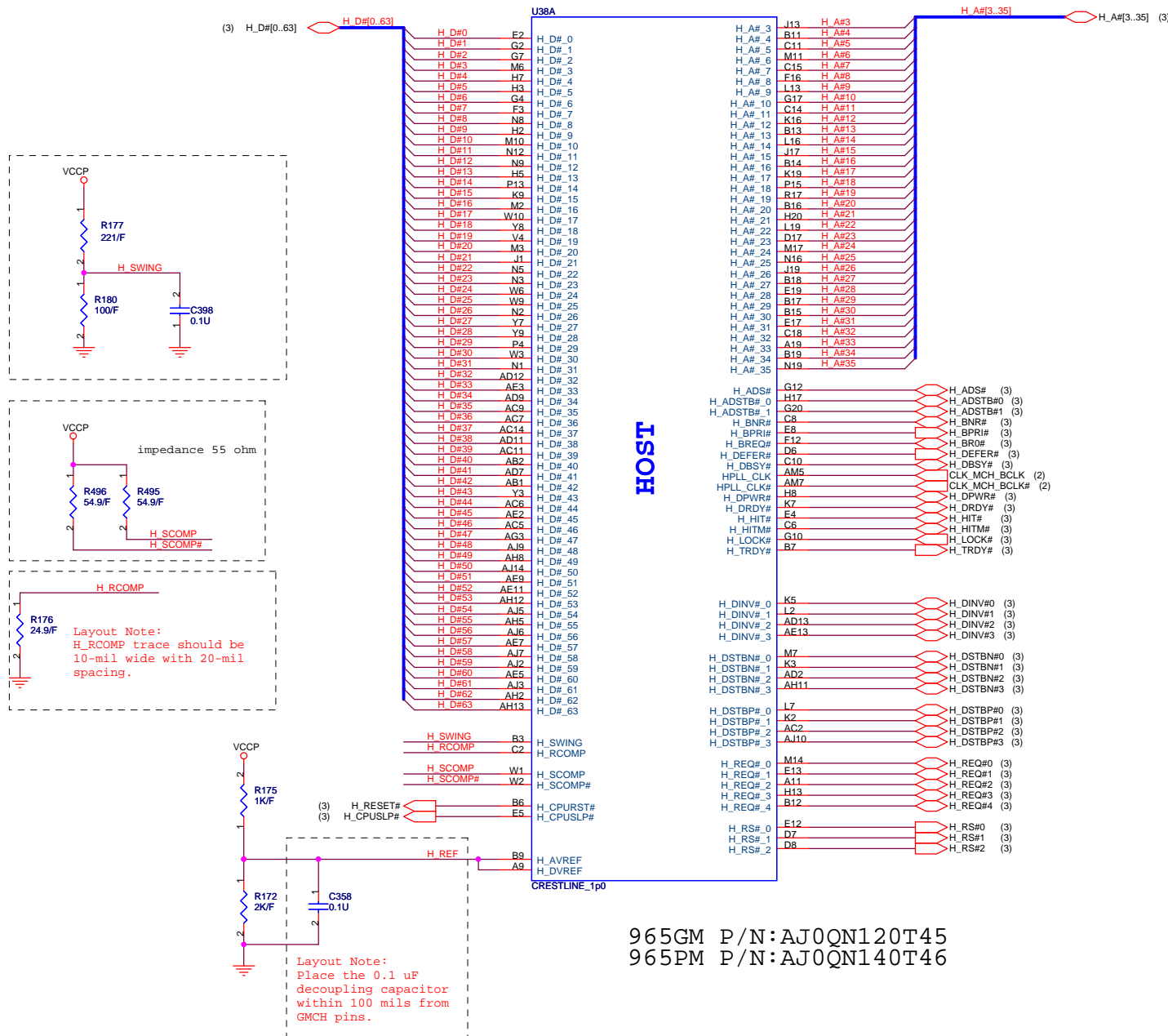


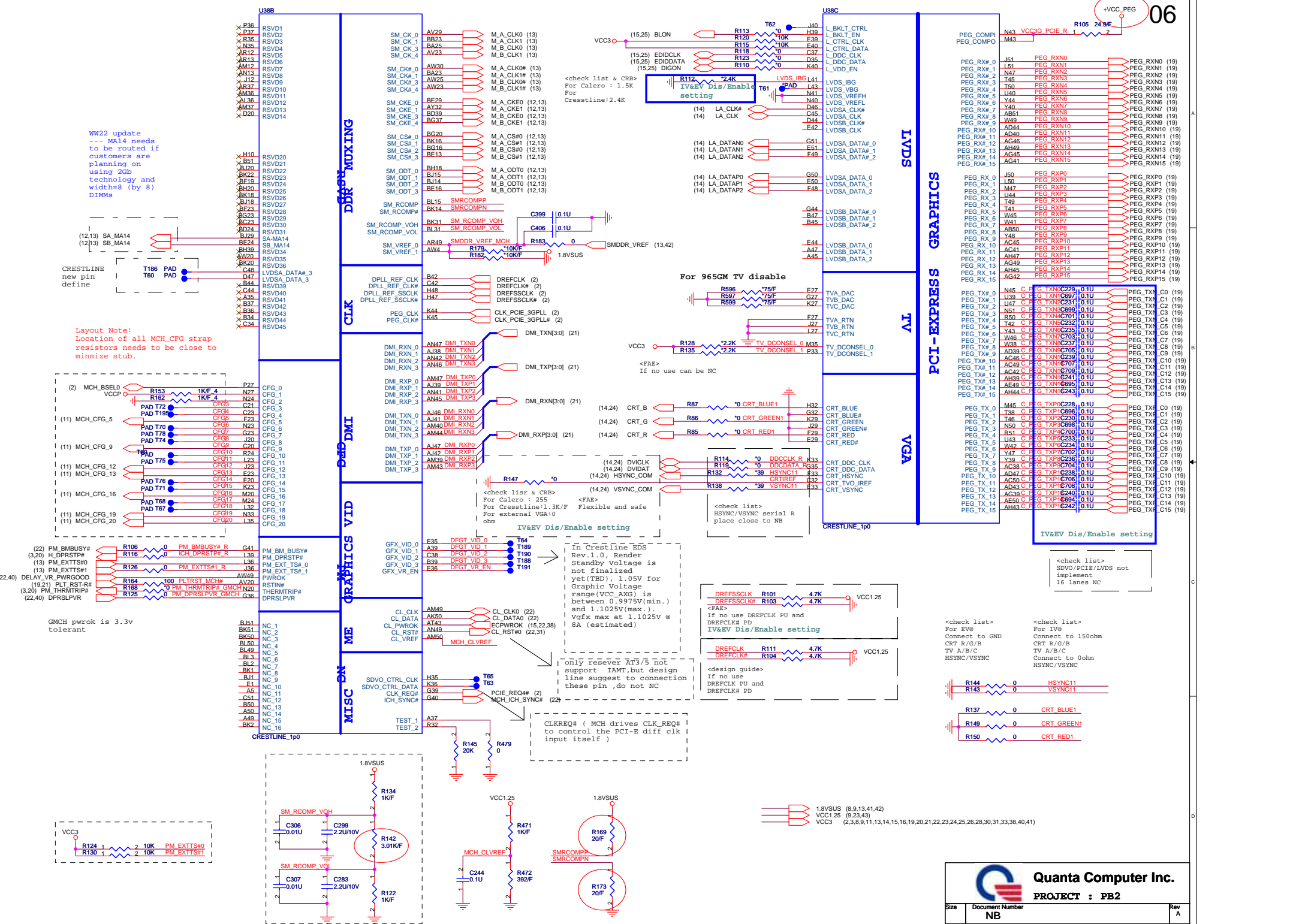
ICCODE:
for Merom processors
recommended design
target is 44A

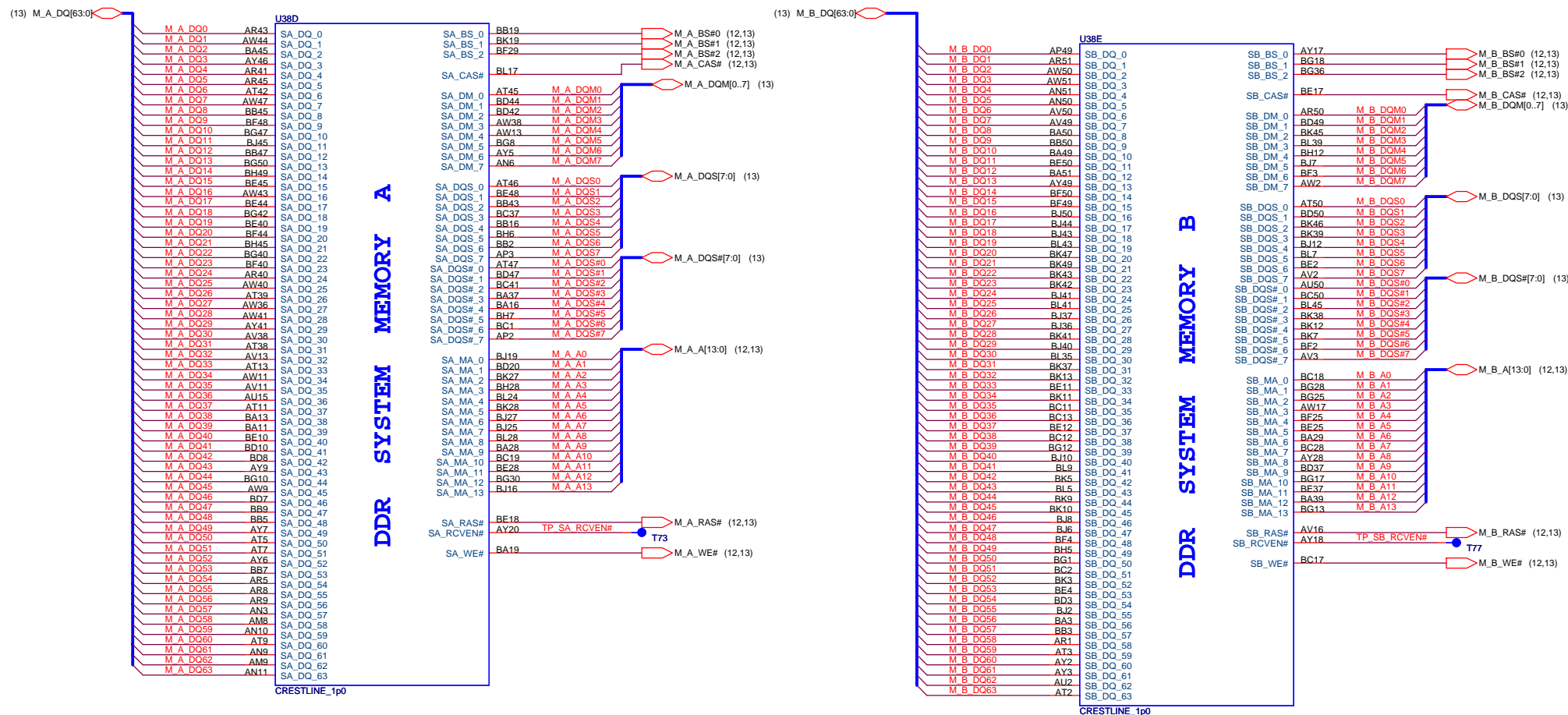
ICCP:
1.before vccore stable
peak current is 4.5A
2.after vccore stable
continue current is
2.5A

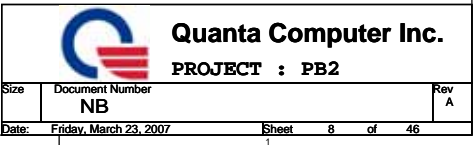
ICCA 130mA

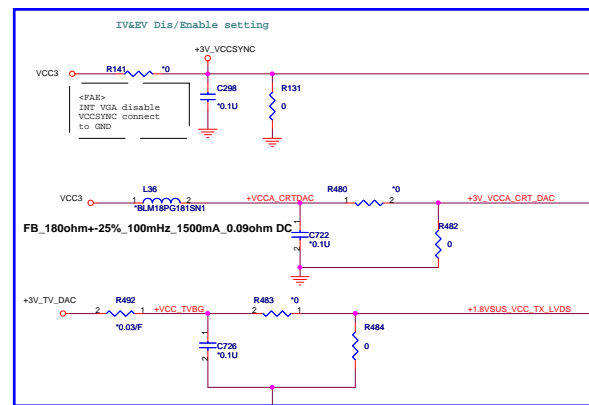












CRT/TV Disable/Enable guideline

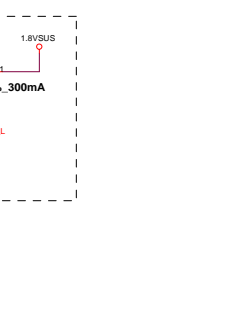
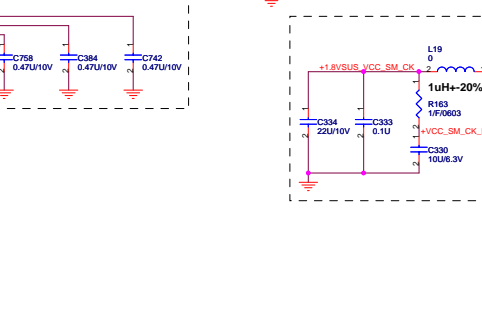
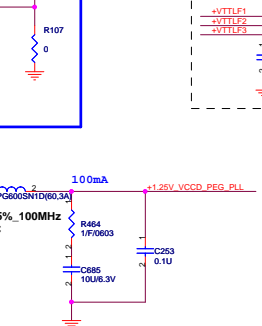
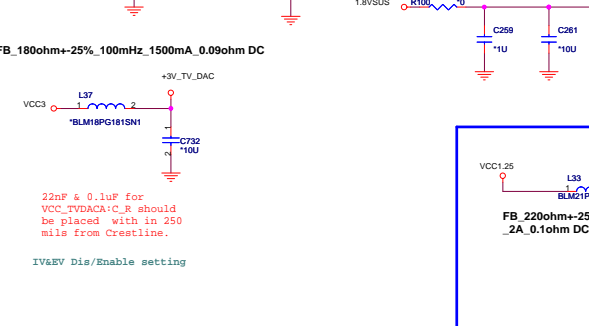
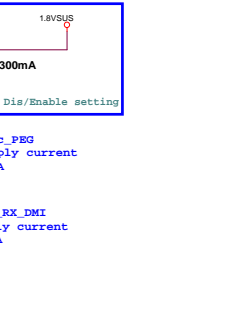
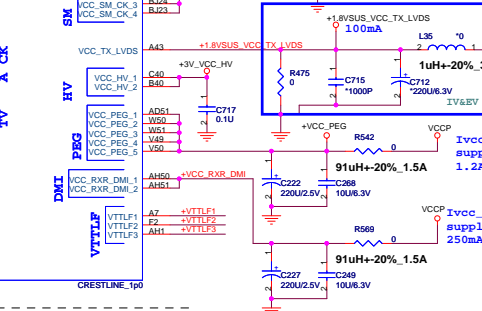
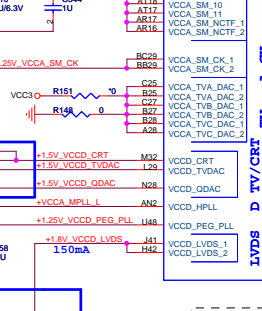
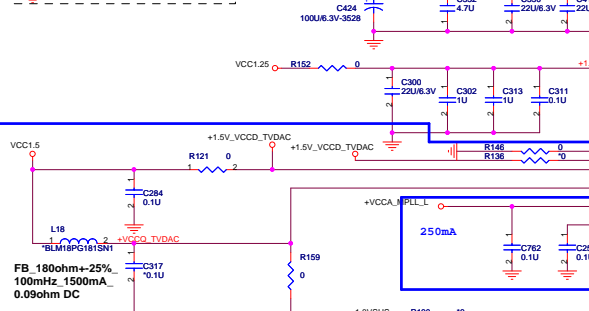
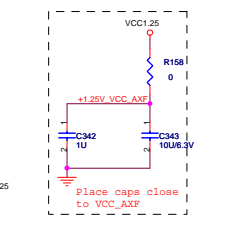
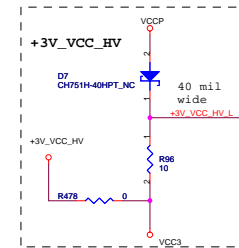
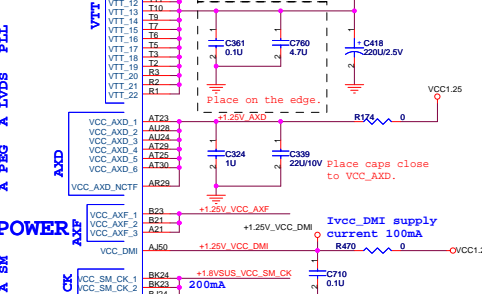
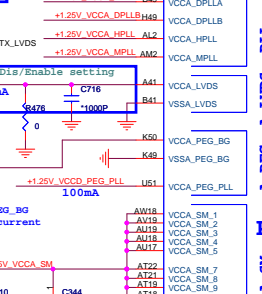
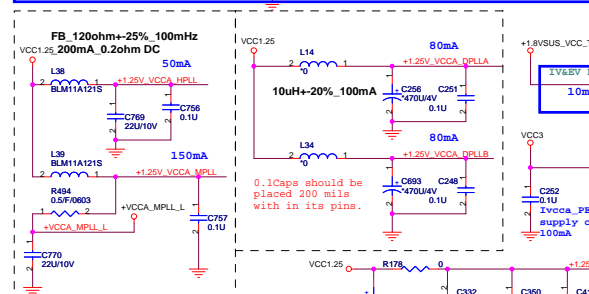
External VGA with EV@part, Internal VGA with IV@ part

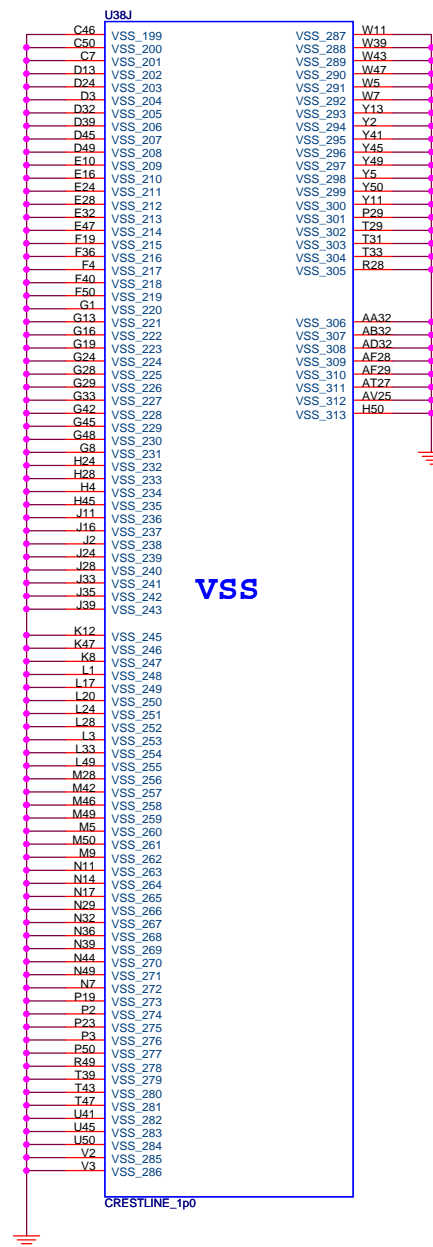
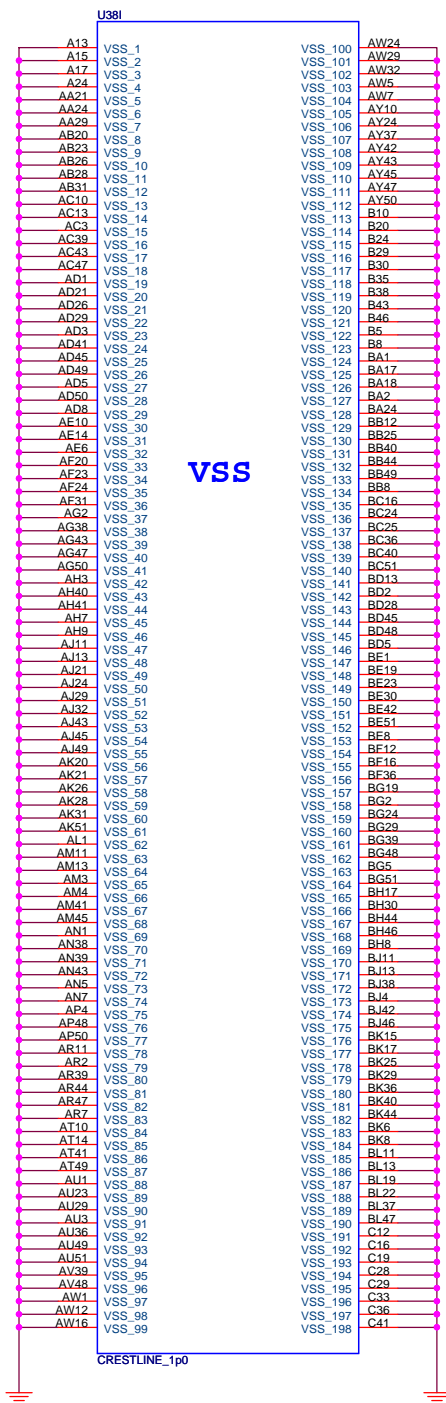
Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT_DAC	3.3V	GND	VCCA_TVC_DAC	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TVDBAC	1.5V	1.5V
VCCD_QDAC	1.5V	GND	VCCA_DAC_BG	3.3V	GND
VCCA_TVA_DAC	3.3V	GND	VSS_DAC_BG	GND	GND
VCCA_TVB_DAC	3.3V	GND	VCCSYNC	3.3V	GND

LVDS Disable/Enable guideline

External VGA with EV@part, Internal VGA with IV@ part

Signal	If SDVO Disable LVDS Disable	If LV enable
VCCD_LVDS	GND	1.8V
VCCA_LVDS	GND	1.8V
VCC_TX_LVDS	GND	1.6V





All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal
CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIx4(Default)
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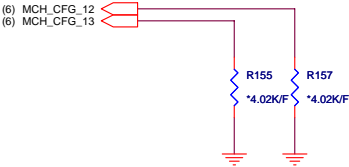
DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane
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XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)



PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)
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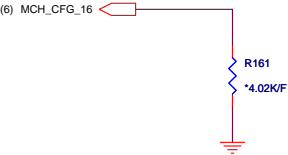


SDVO Present

Strap define at External DVI control page

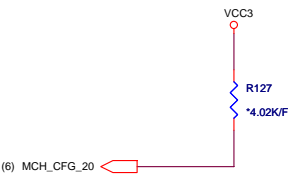
FSB Dynamic ODT

MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)
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SDVO/PCIE Concurrent operation

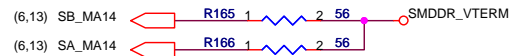
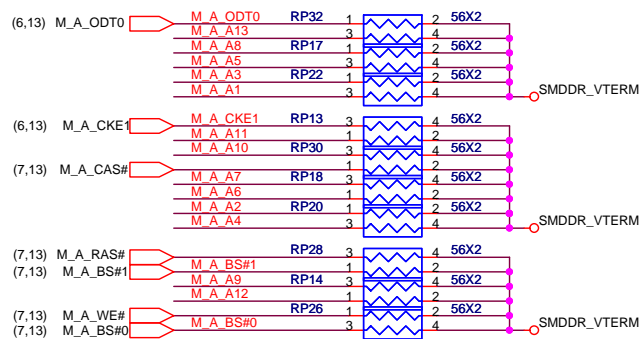
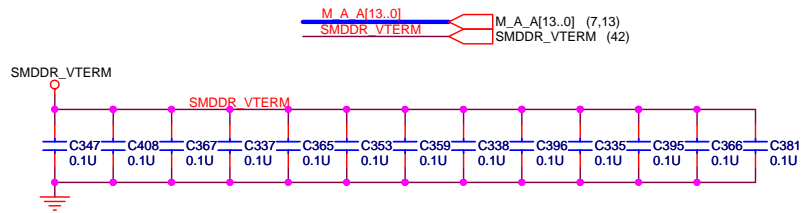
MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO andPCIE X1 are operating simultaneously via the PEG port
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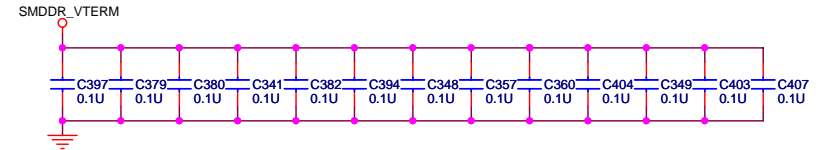
DDRII DUAL CHANNEL A,B.

12

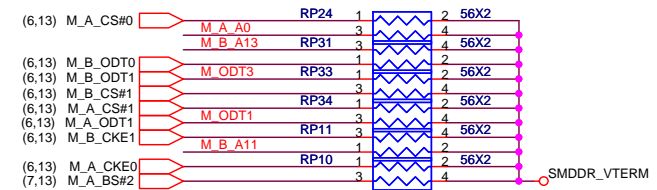
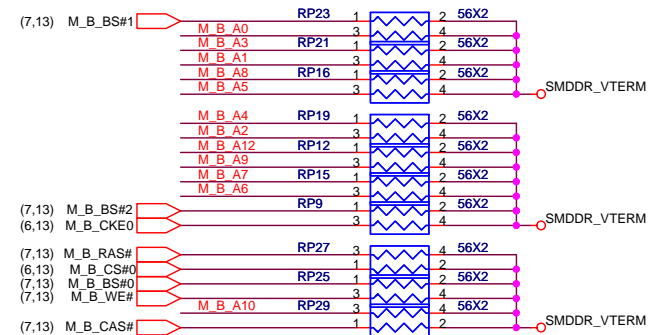
DDRII A CHANNEL



DDRII B CHANNEL



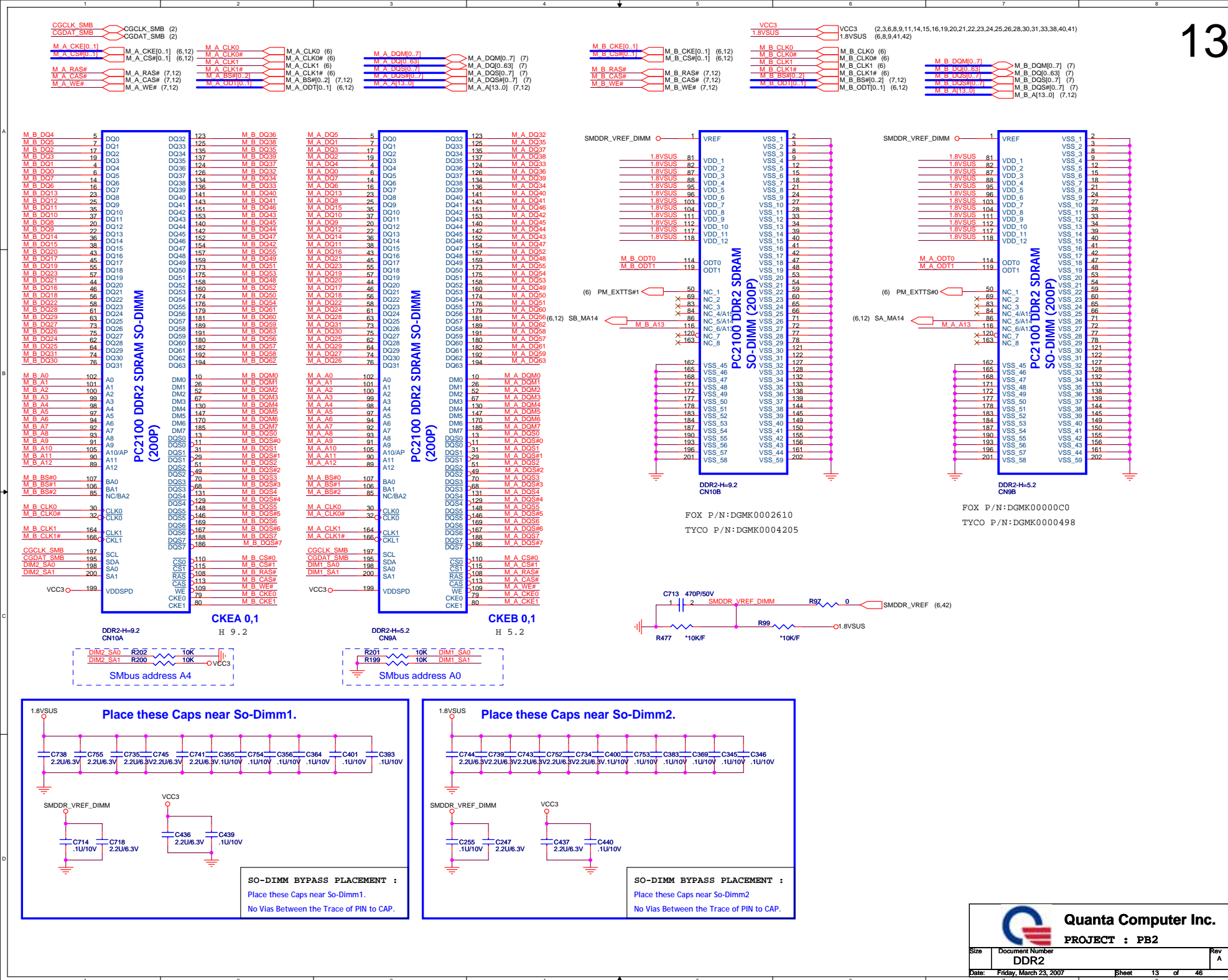
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDRR_VTERM

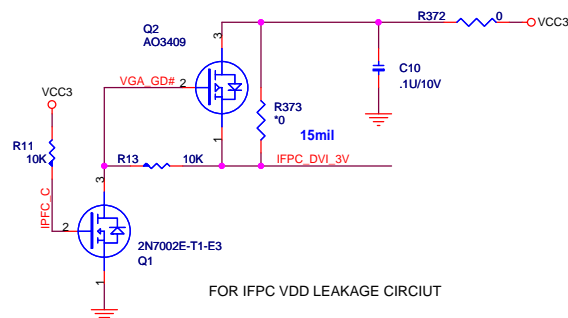
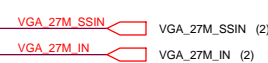
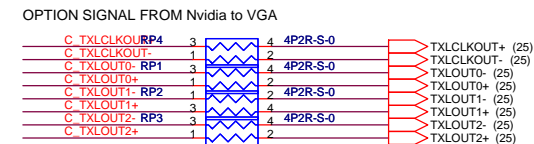
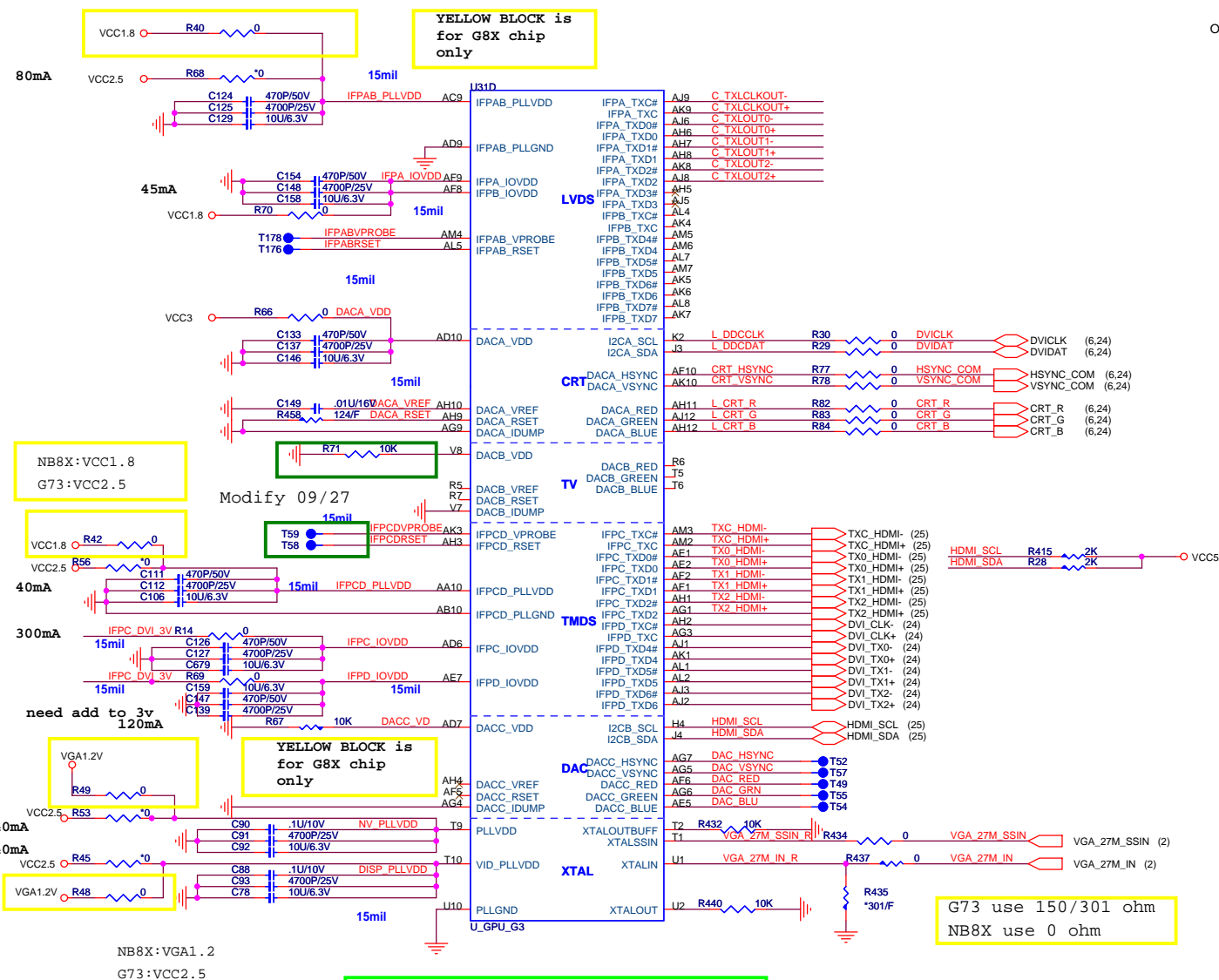


Quanta Computer Inc.

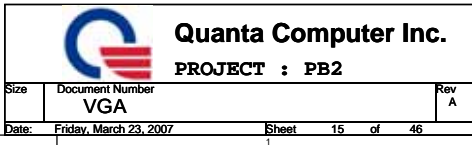
PROJECT : PB2

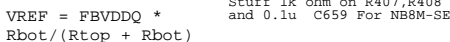
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Date:	Friday, March 23, 2007	Sheet 12 of 46



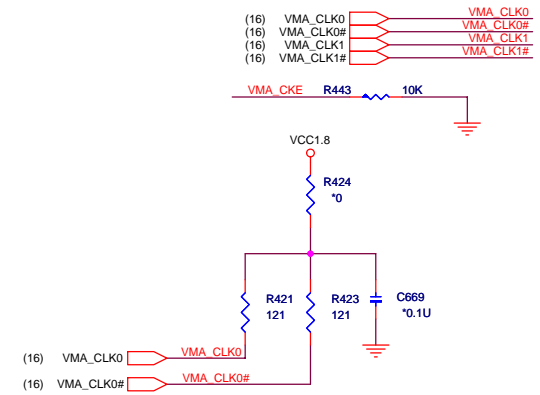
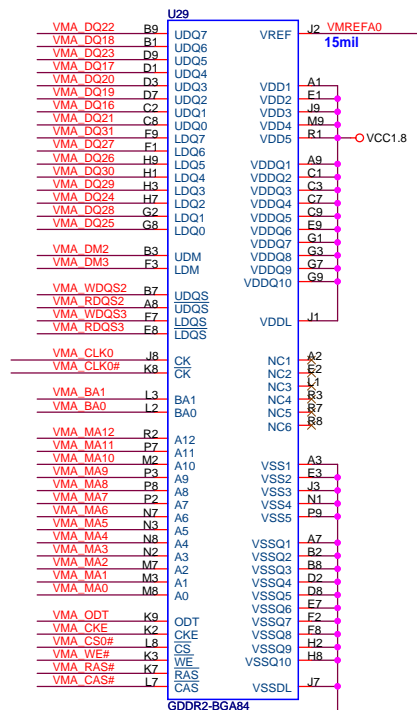
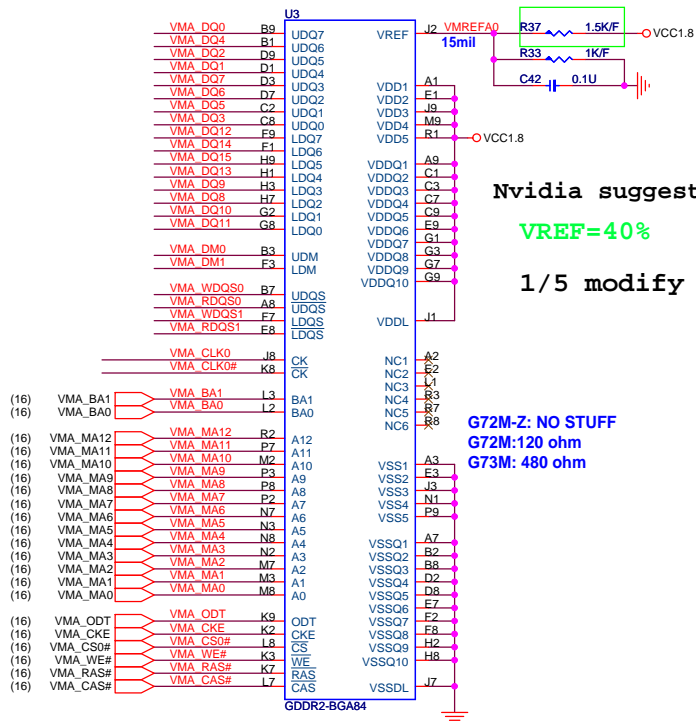


FOR IFPC VDD LEAKAGE CIRCUIT

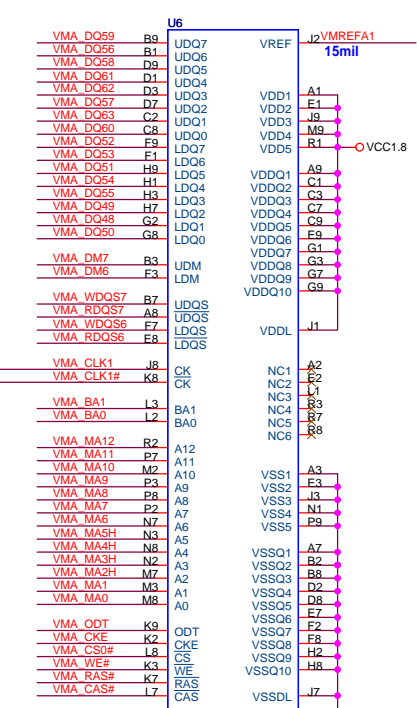
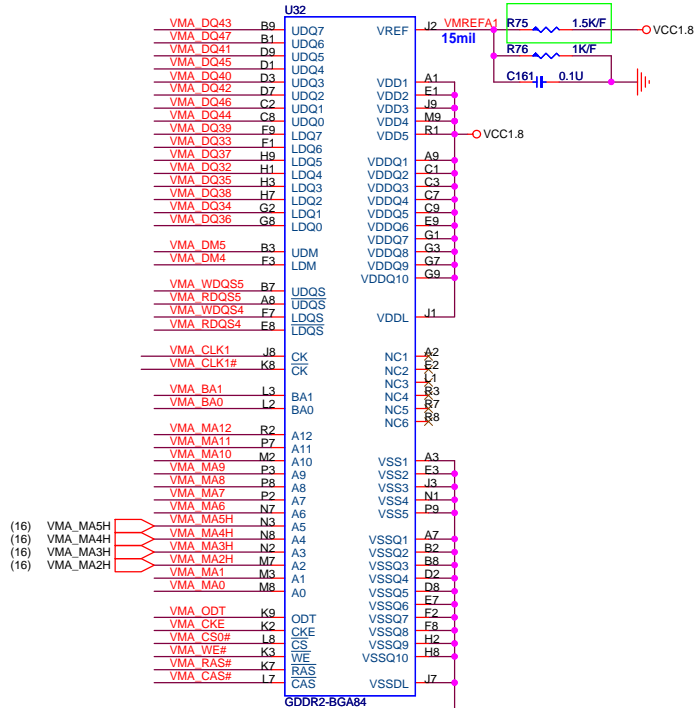
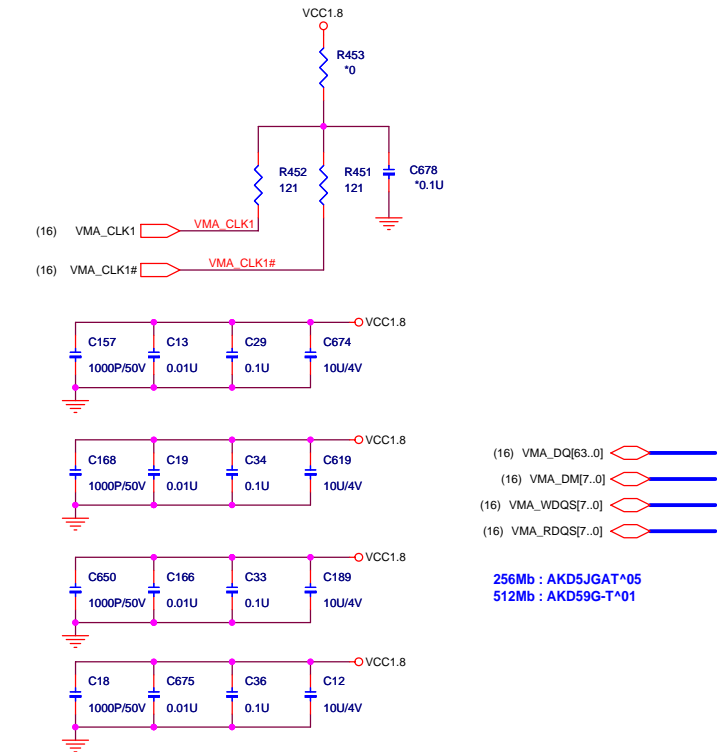


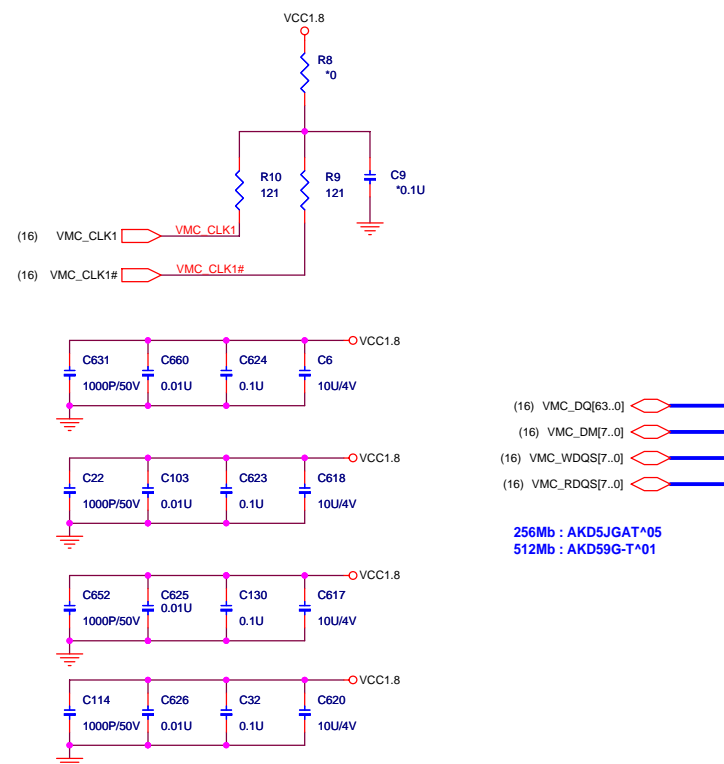
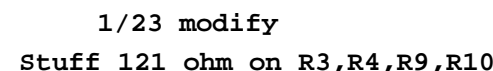
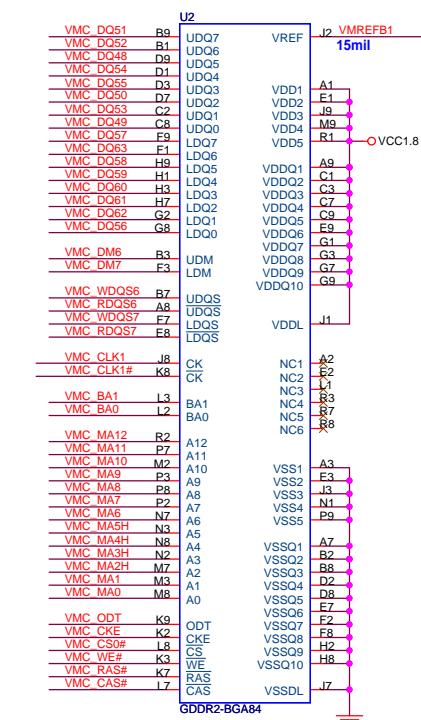
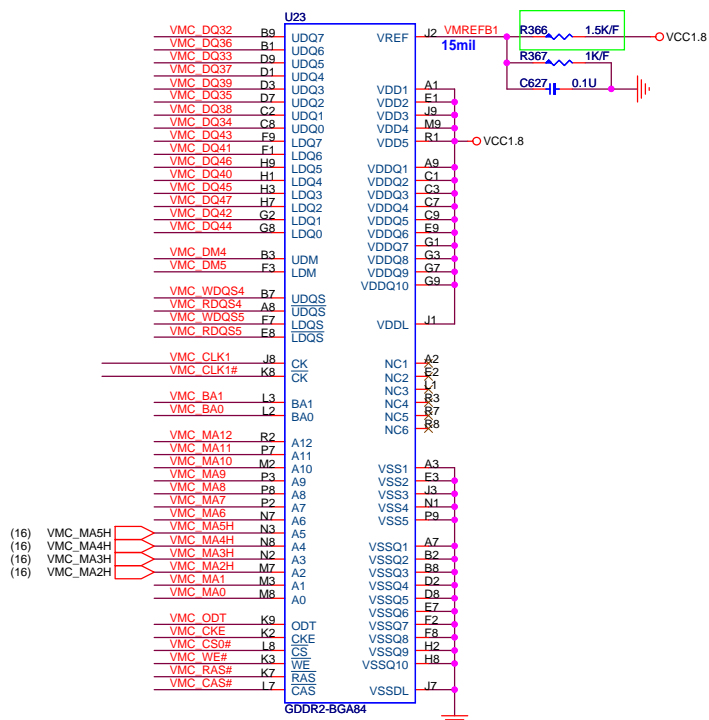


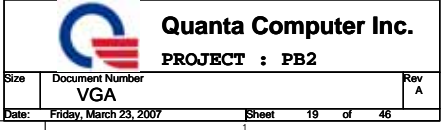
F_VREF2 filter can be
remove from nvidia
HANK recommend
G70,G71: Stuff these parts
G72M,G73M : NC

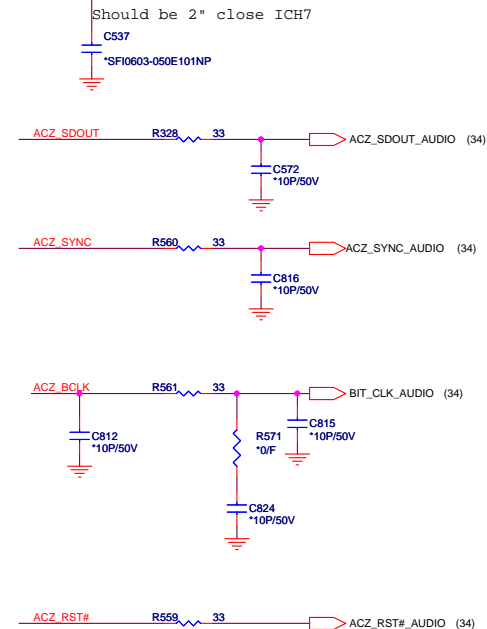


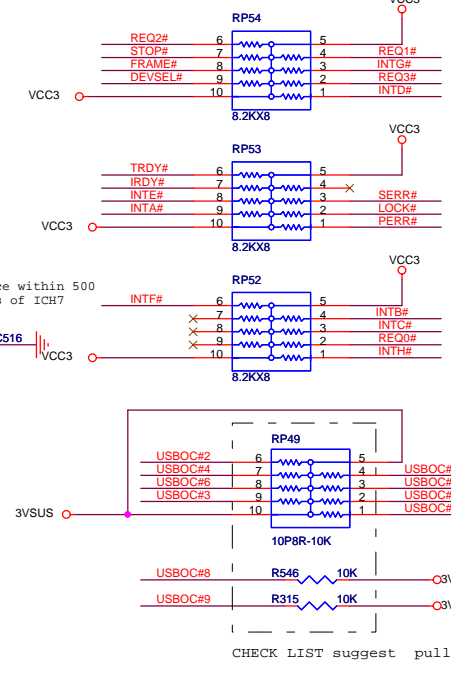
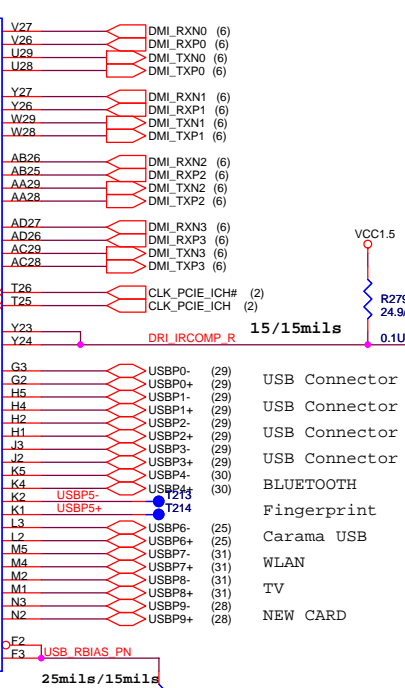
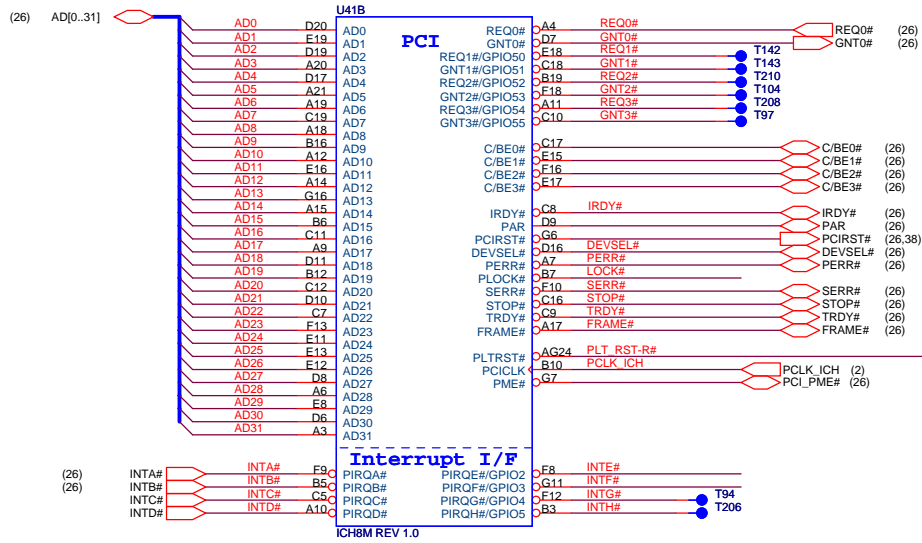
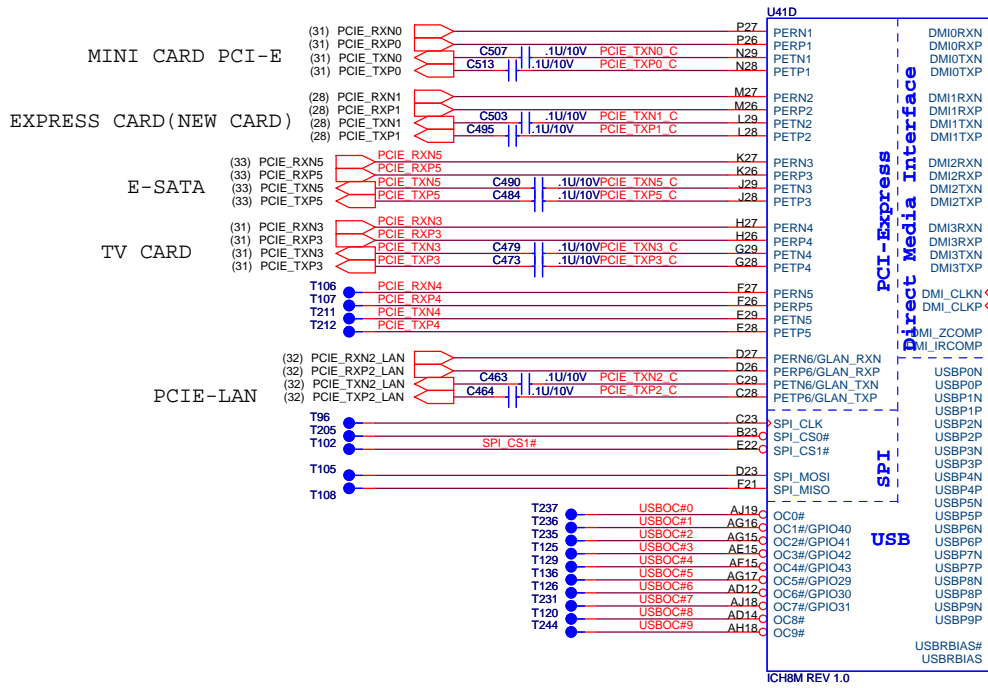
NB8M/8P: Stuff 121 ohm on R421,R423,R452,R451





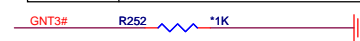






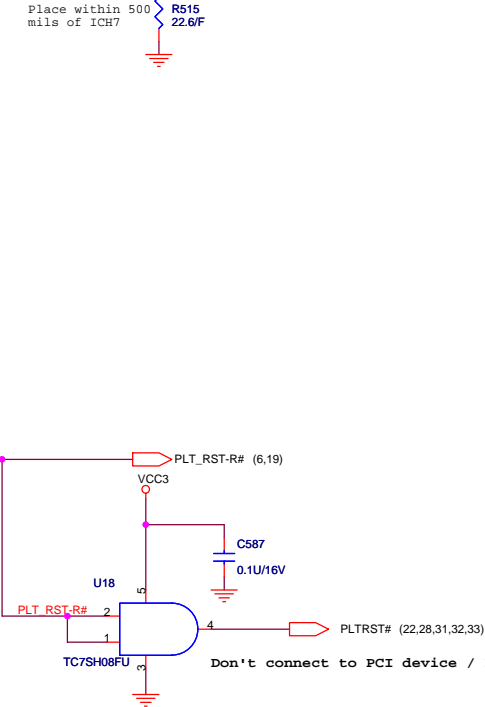
A16 SWAP Override strap

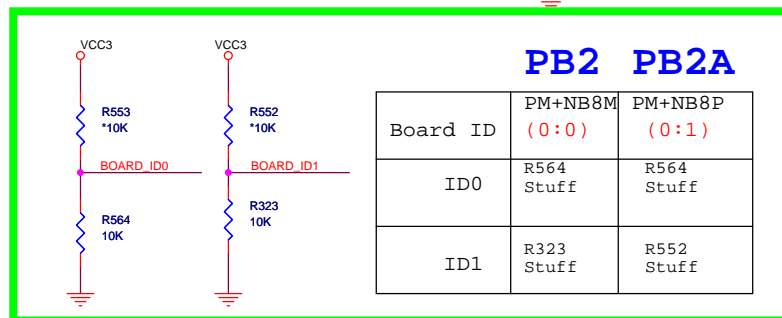
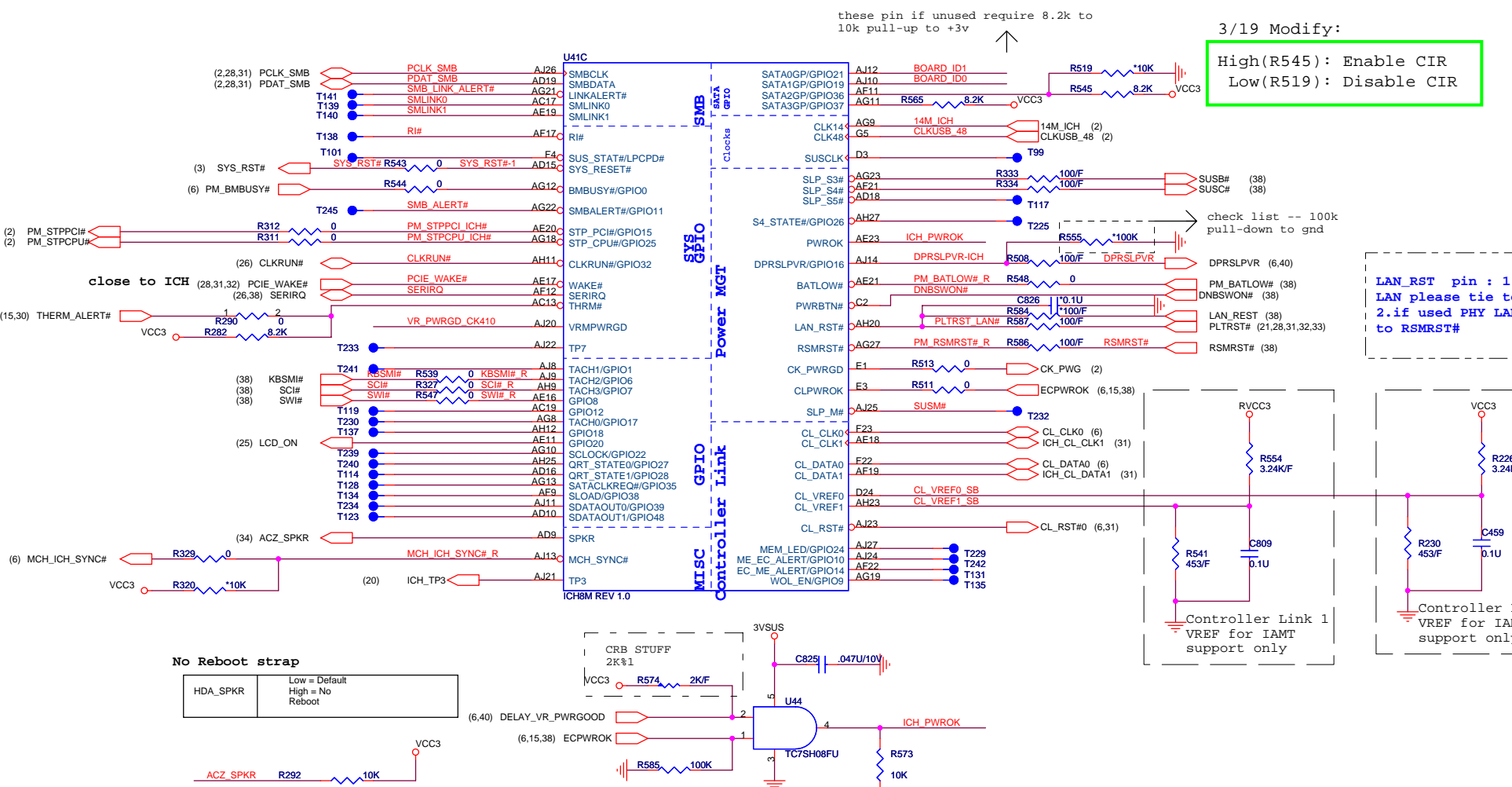
PCL_GNT#3	Low = A16 swap override enabled High = Default
-----------	---

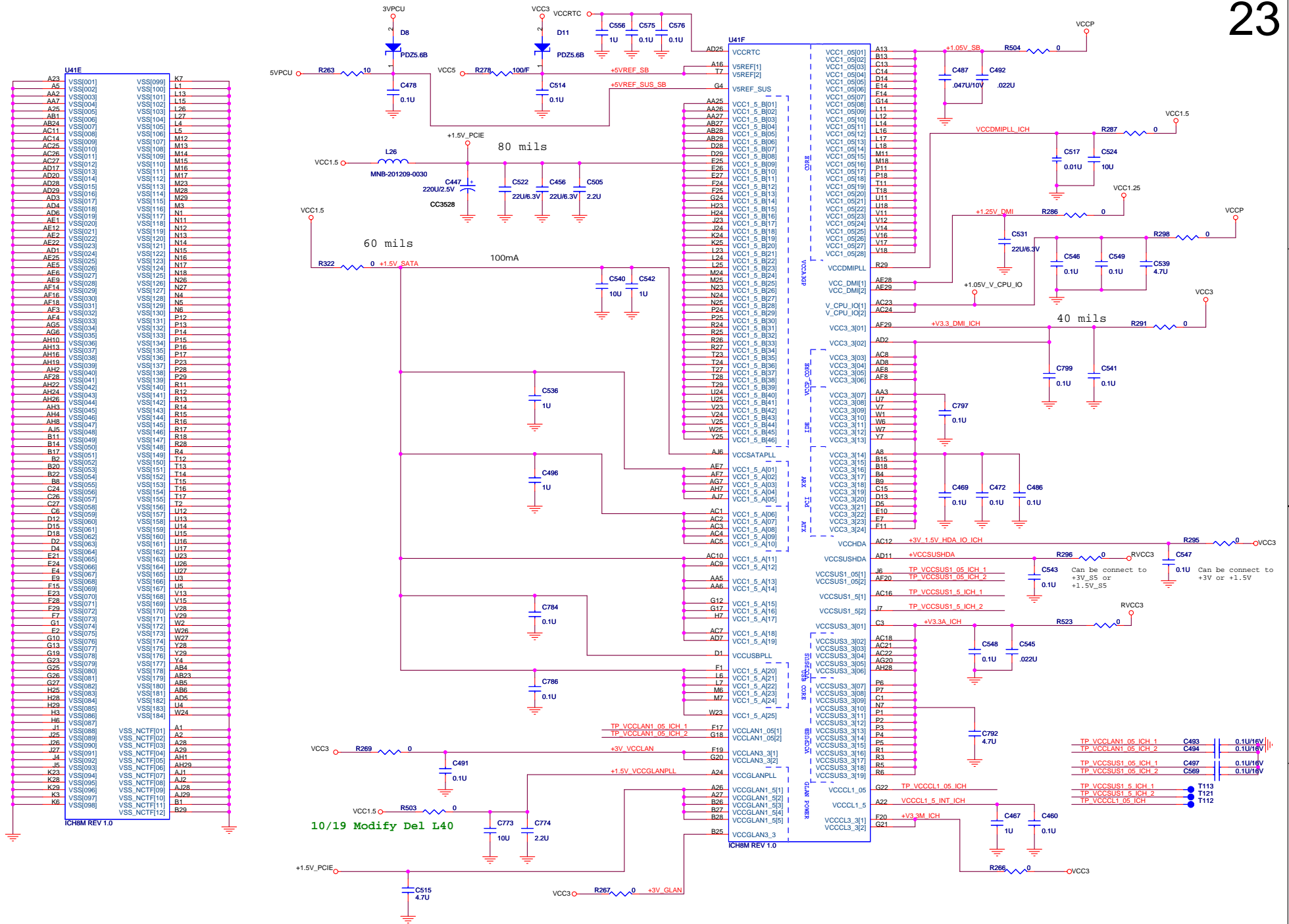


ICH8 Boot BIOS select

PCL_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

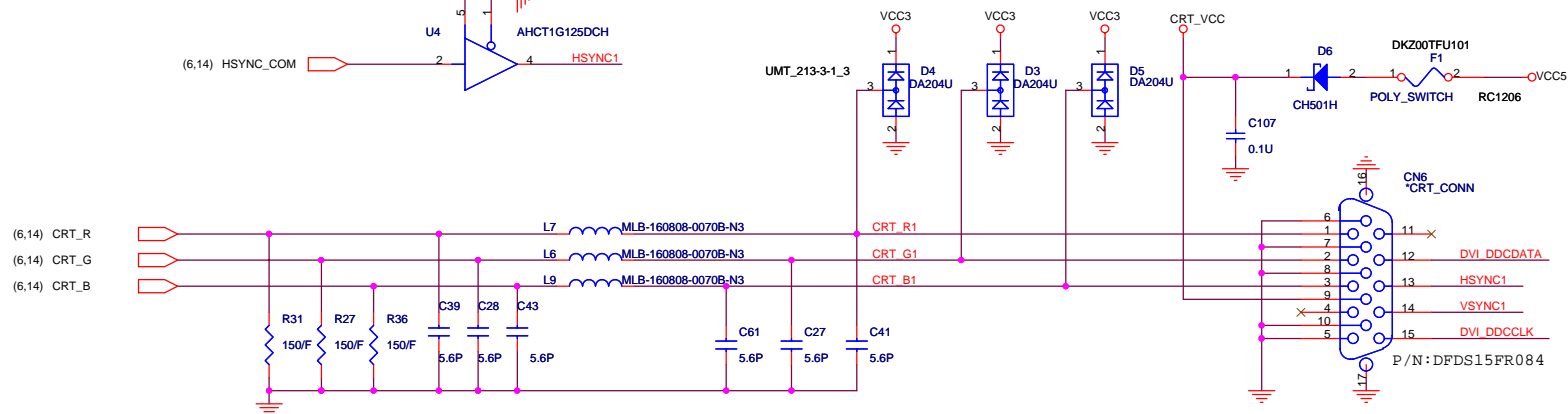
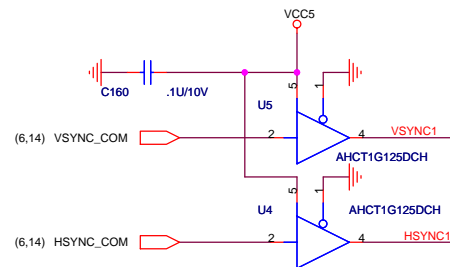
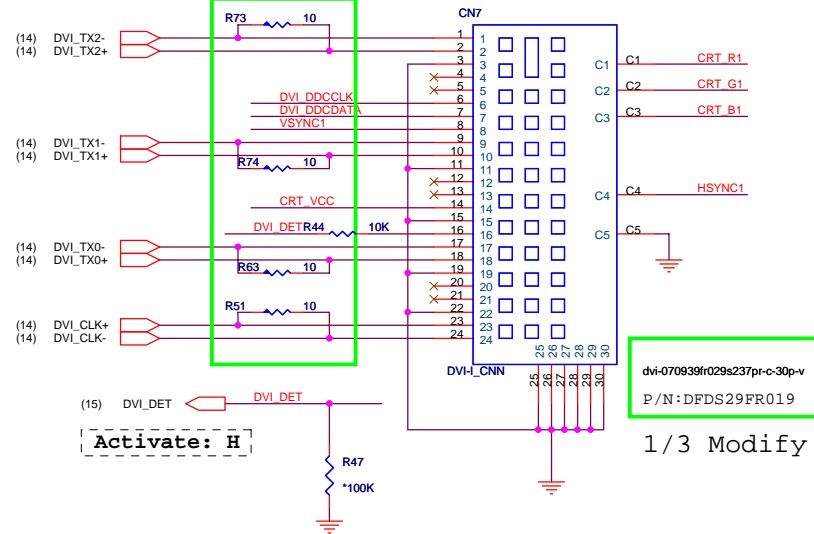
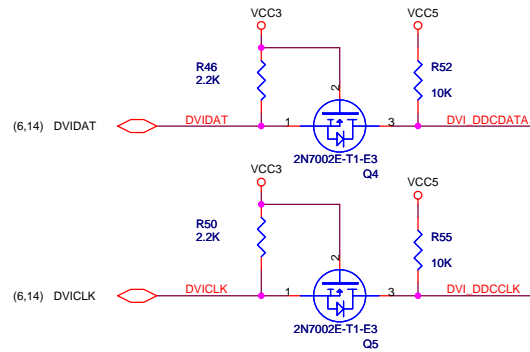




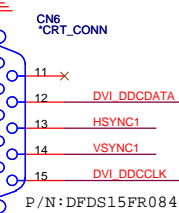


DVI-I

For EMI
Modify 11/28

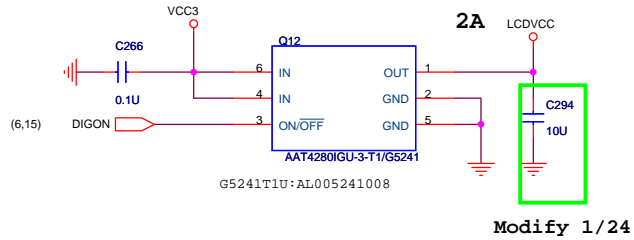


PTC:DK100TPU028

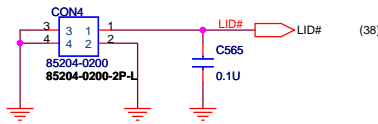


Quanta Computer Inc.
PROJECT : PB2

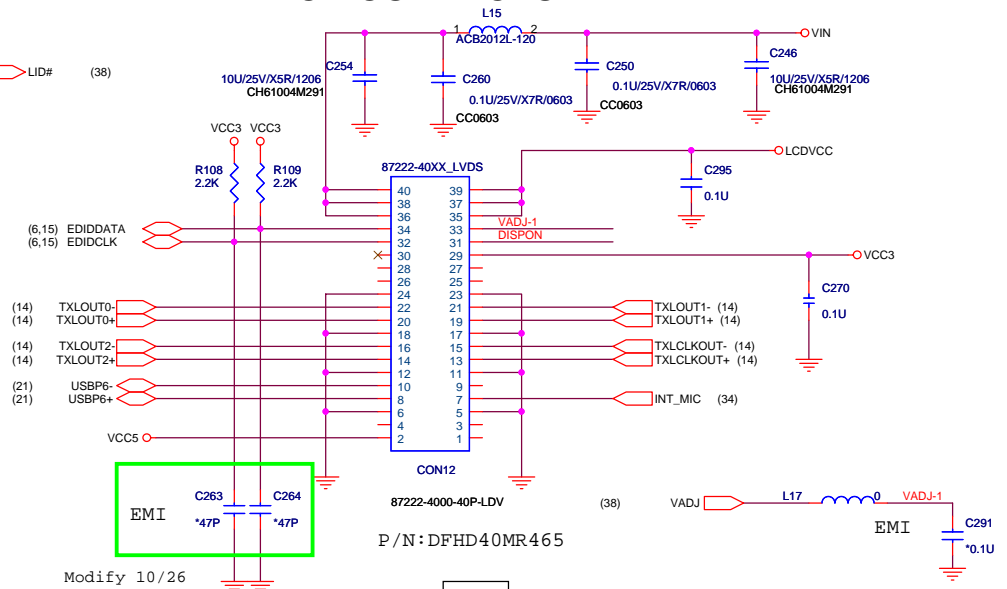
PANEL VCC CONTROL



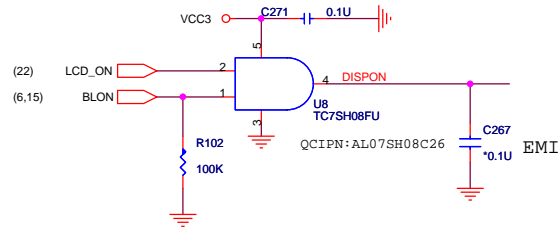
LID



LCD CONNECTOR

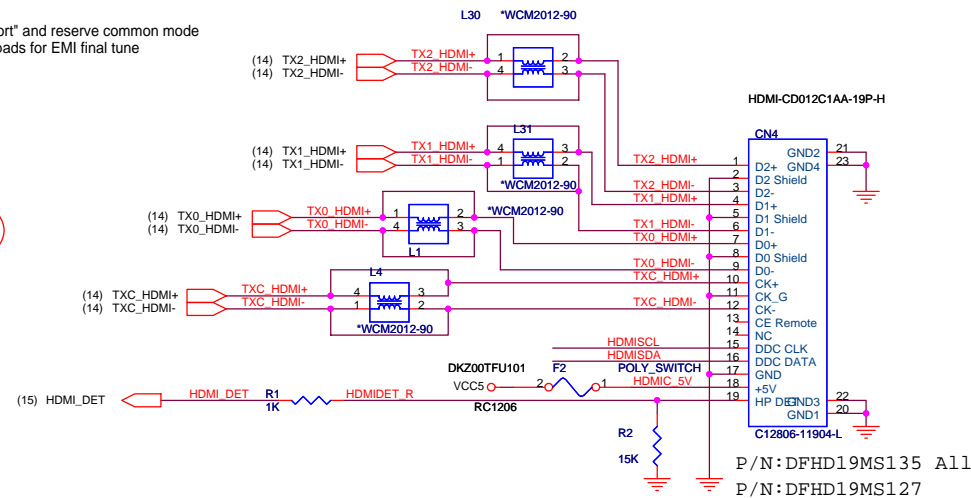
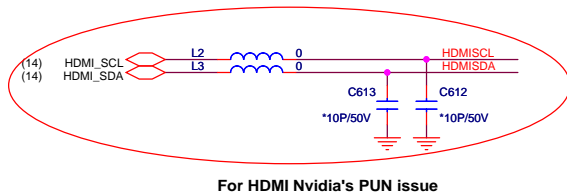


BACKLIGHT CONTROL

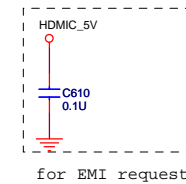


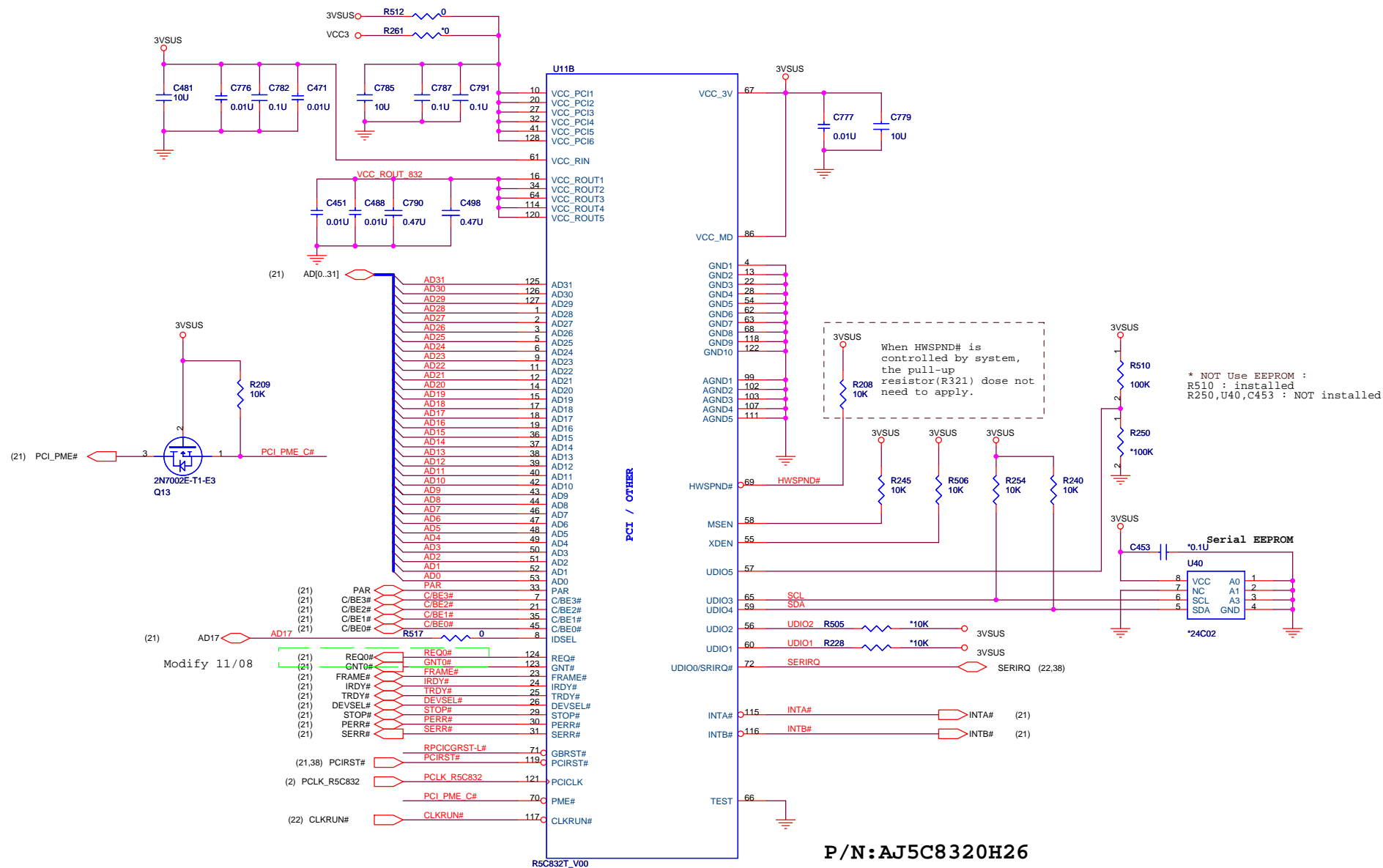
1. VCC5
2. D-
3. D+
4. MIC
5. GND

DB "short" and reserve common mode choke pads for EMI final tune



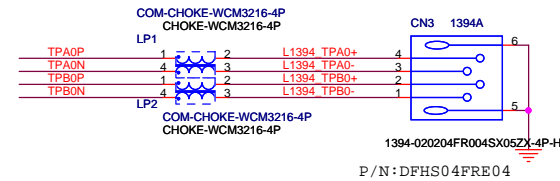
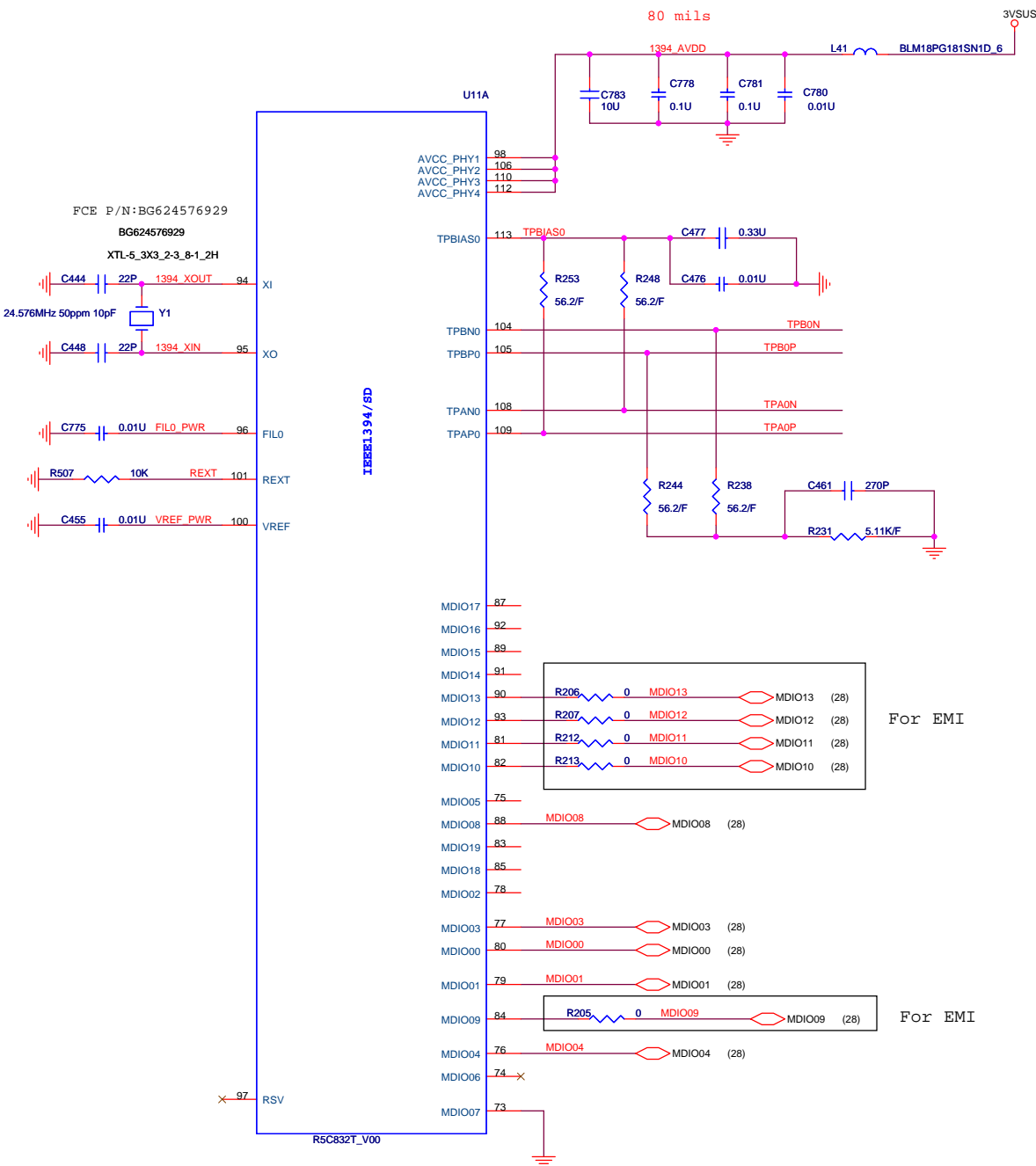
HDMI PORT



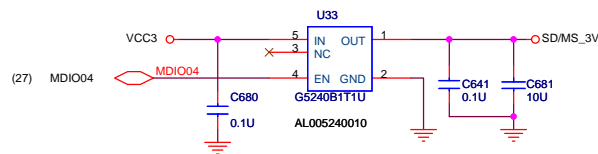


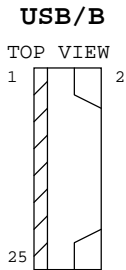
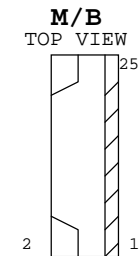
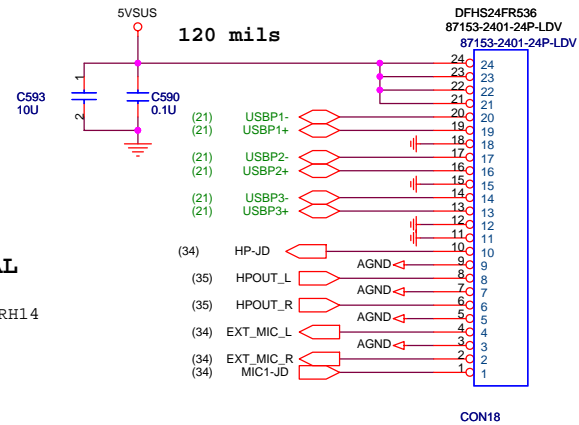
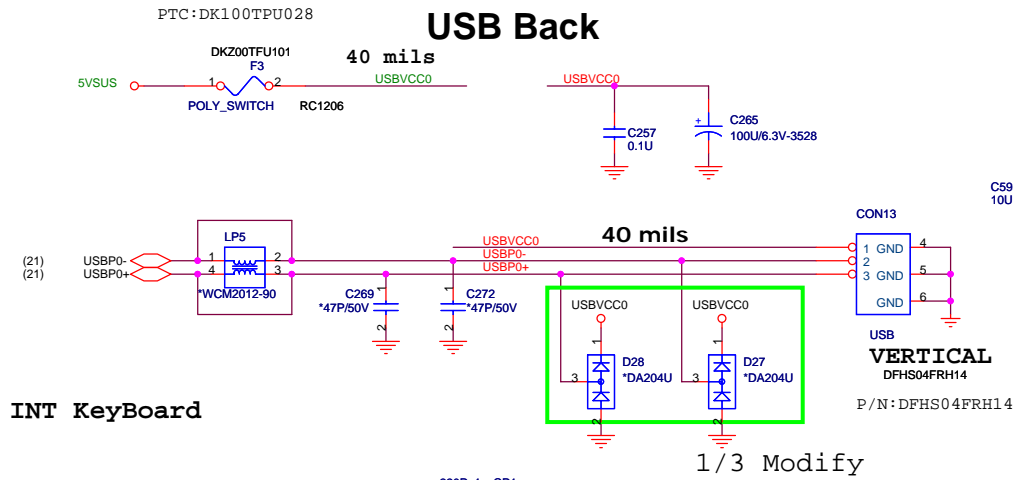
P/N: AJ5C8320H26

Modify 12/26

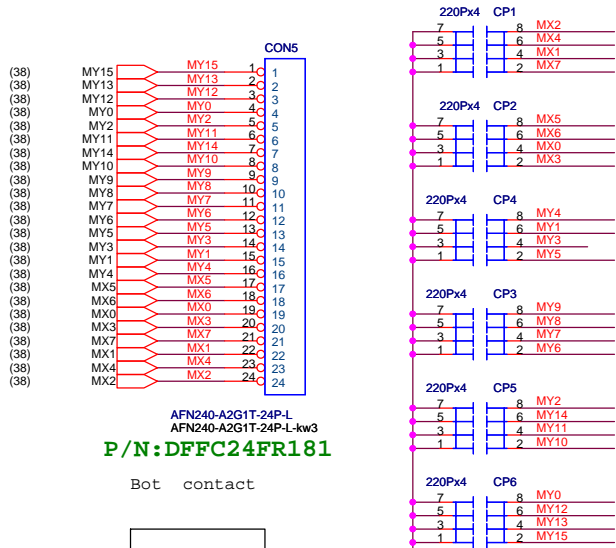


	Vendor ID	Device ID
1394	1180	0832
SD	1180	0822
MMC	1180	0843
MS	1180	0592
xD	1180	0852

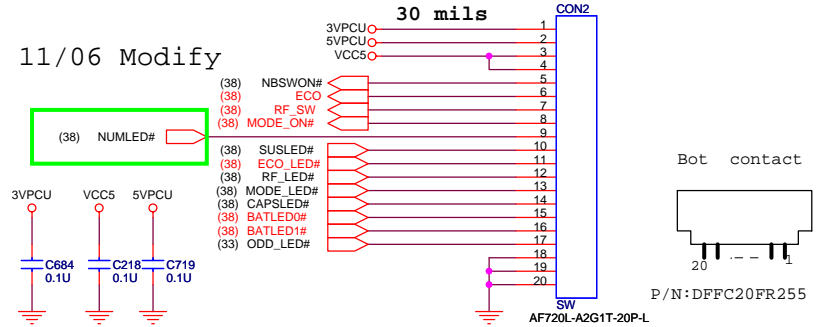




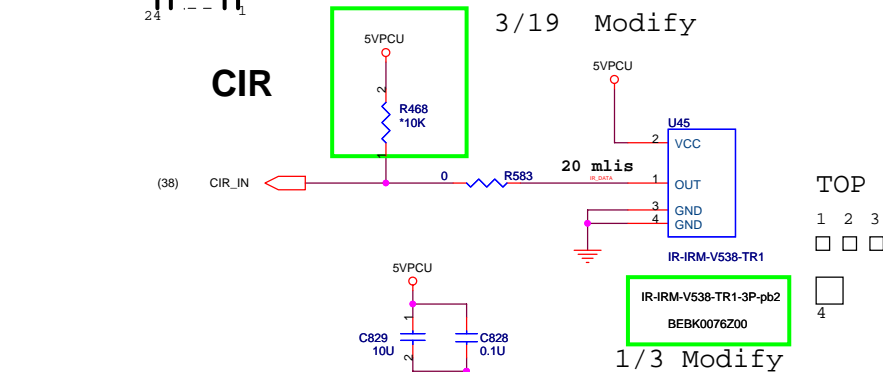
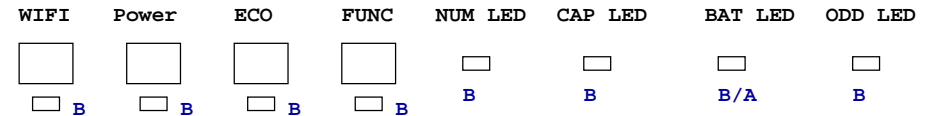
INT Keyboard



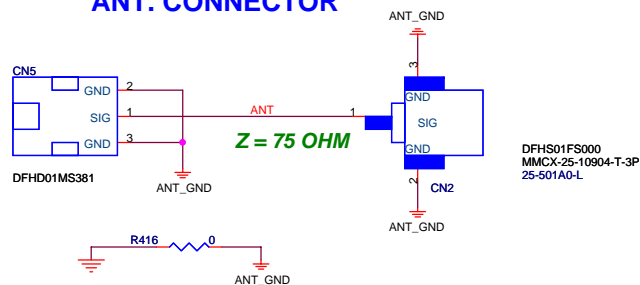
SWITCH BOARD



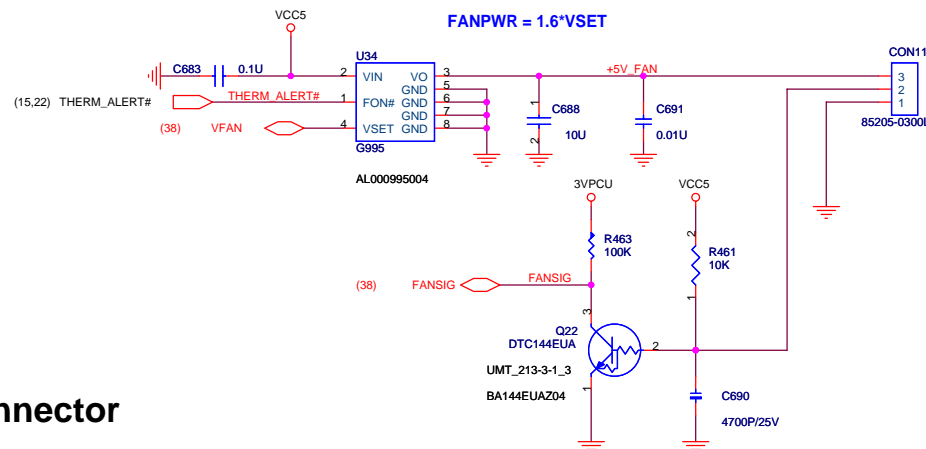
SW/B Blue: B Amber: A



ANT. CONNECTOR

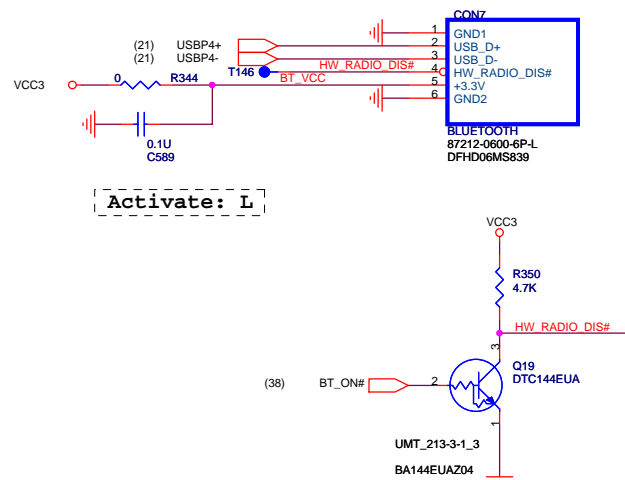
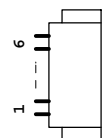


FAN CONN

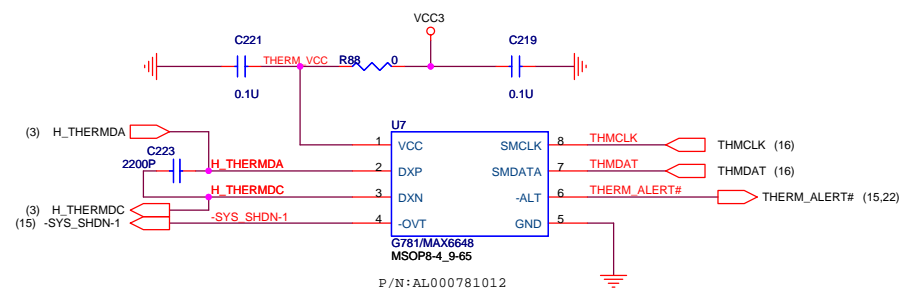


BT Connector

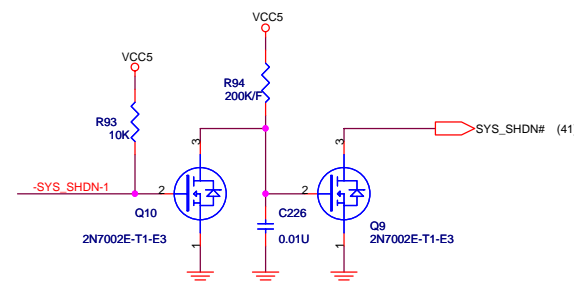
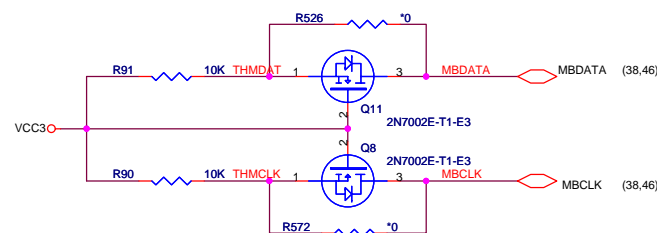
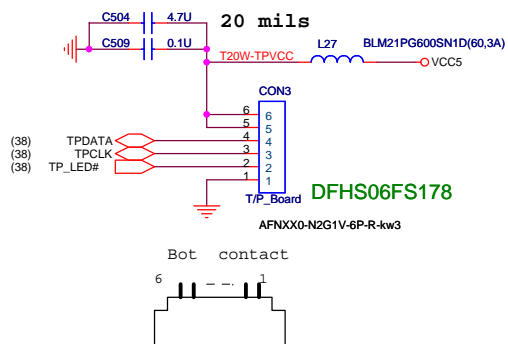
TOP Side



Thermal Sensor

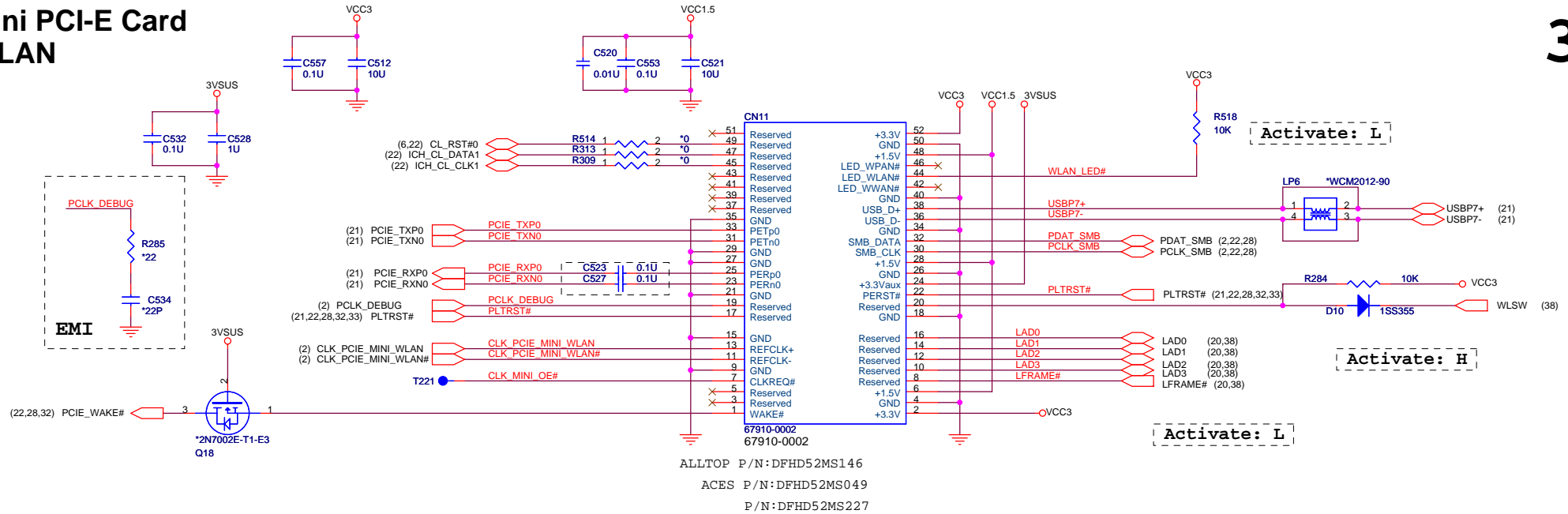


TOUCH PAD

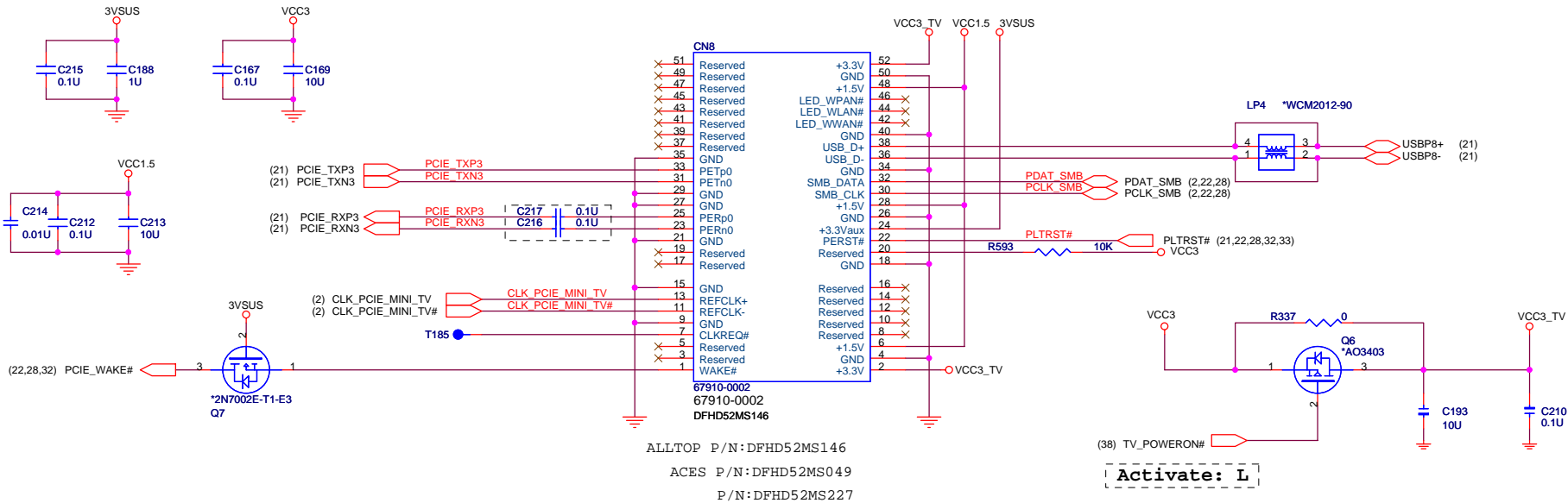


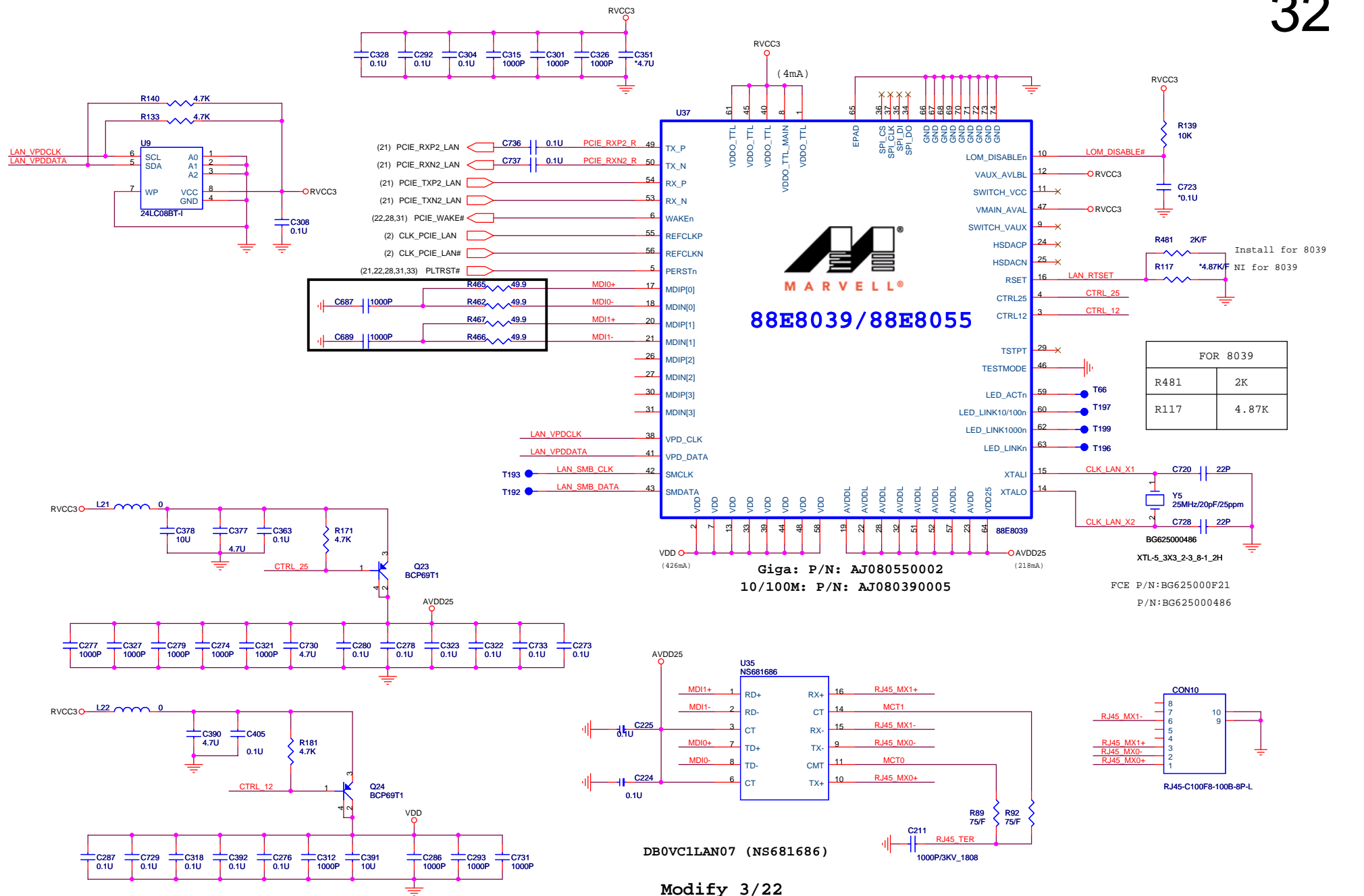
Mini PCI-E Card WLAN

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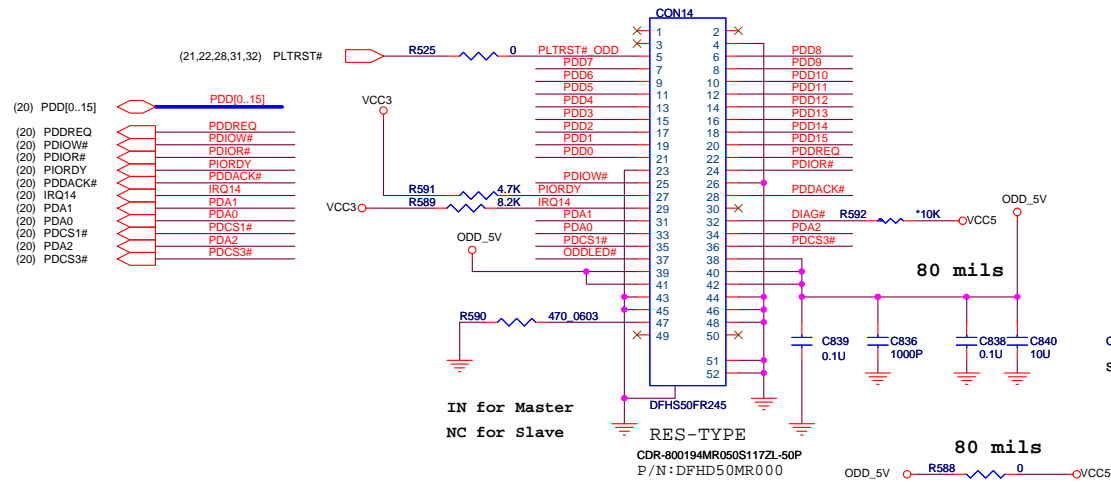


Mini PCI-E Card TV





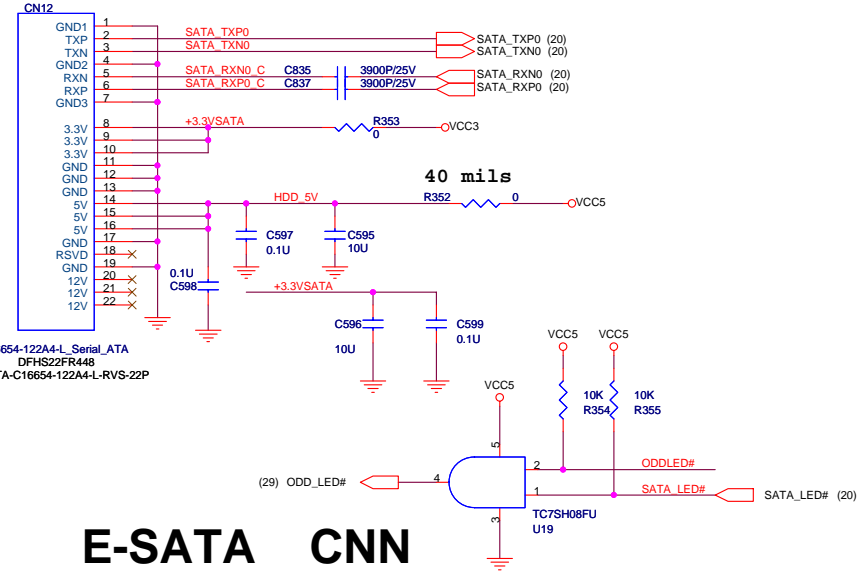
CD-ROM CONNECTOR SMT TYPE CNN



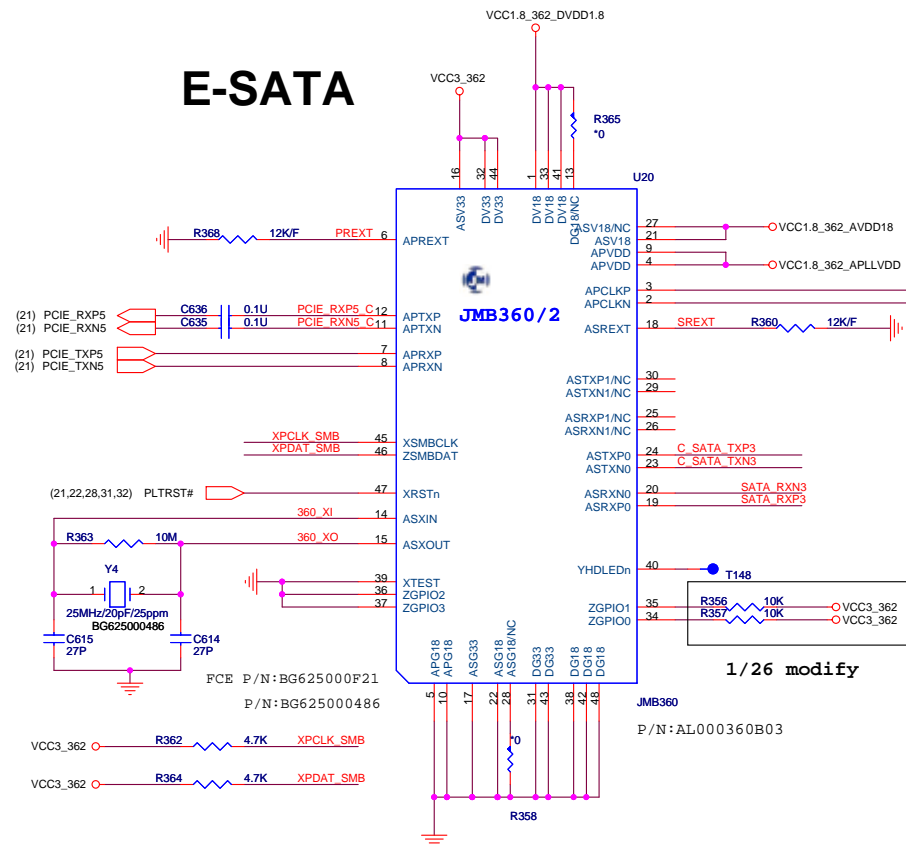
SATA HDD

10/19 Modify H=4.5mm

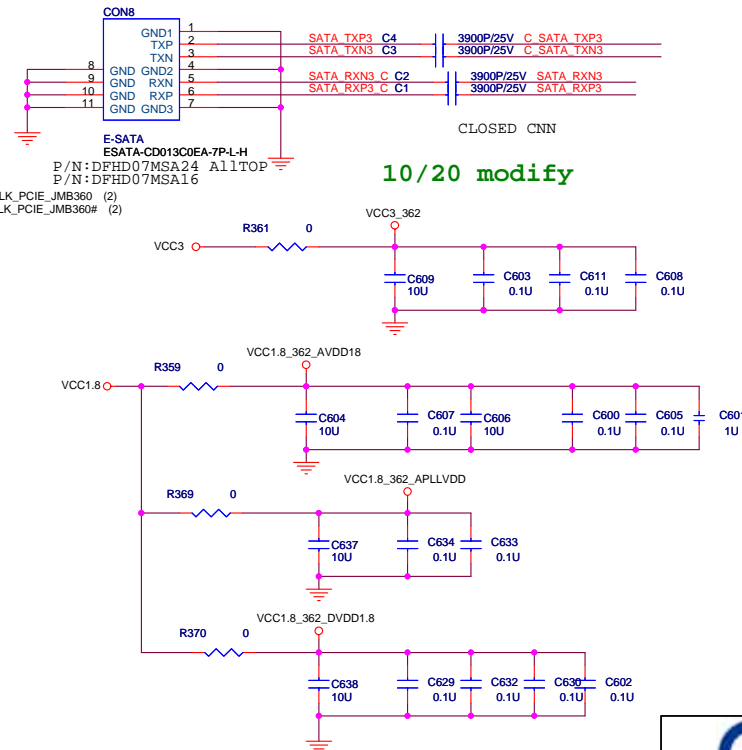
P/N:DFHS22FR448 REF: ZC3



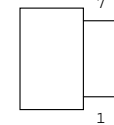
E-SATA

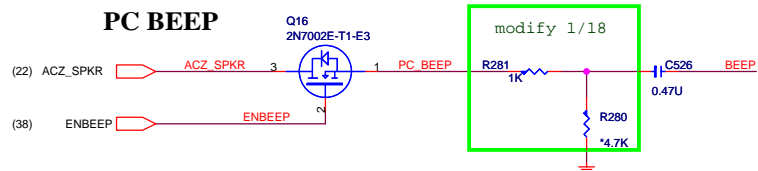
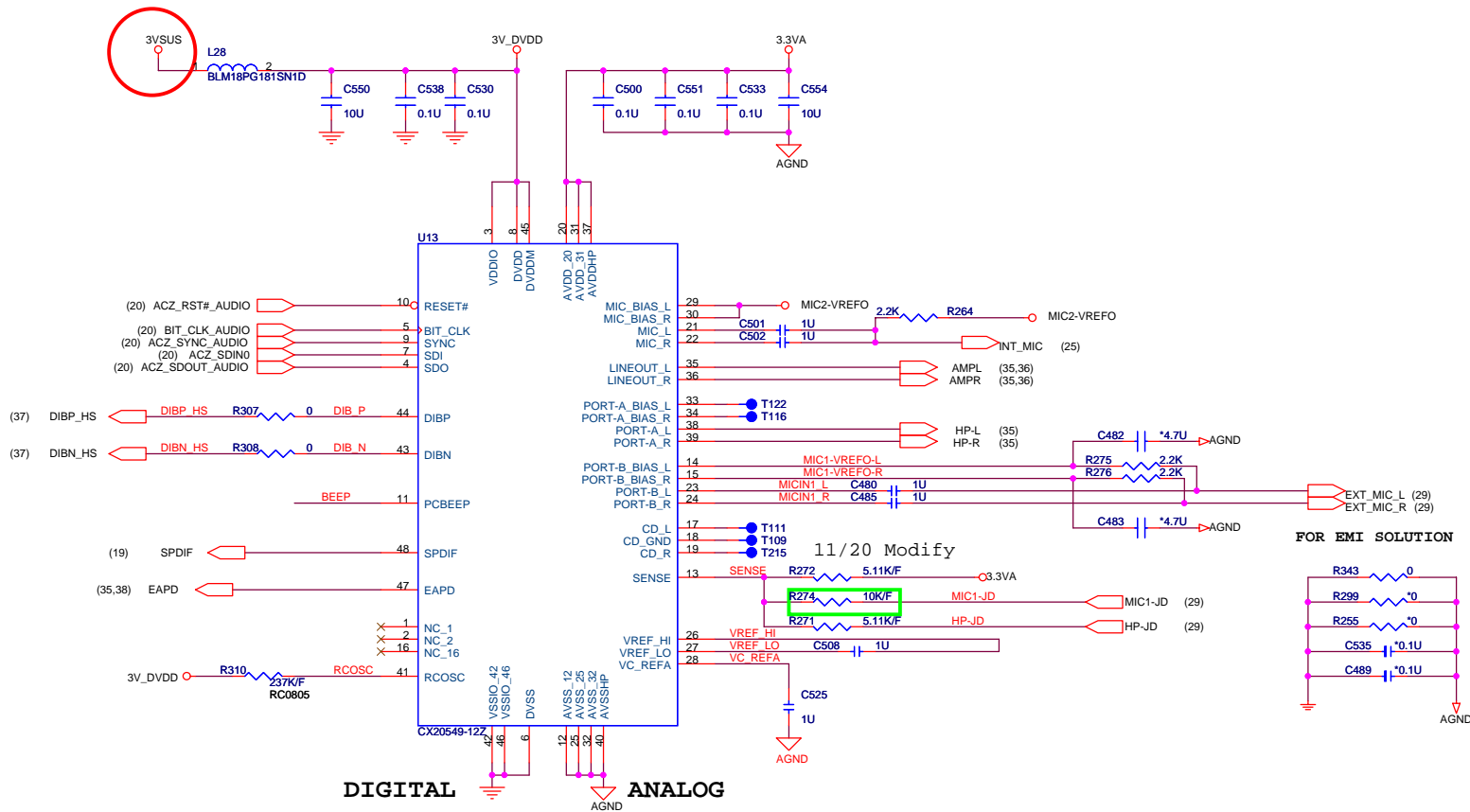


E-SATA CNN



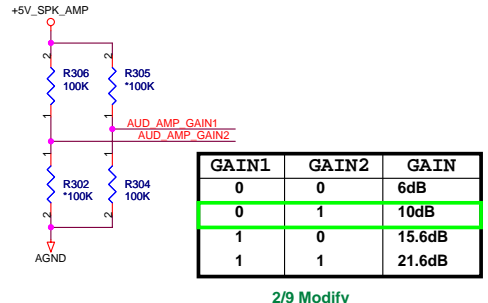
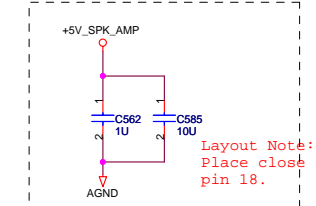
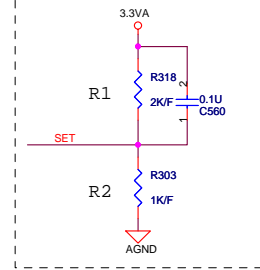
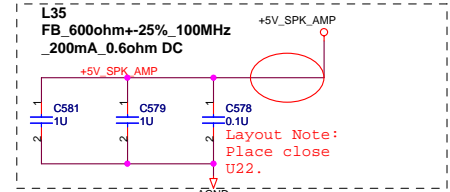
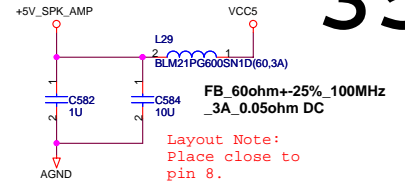
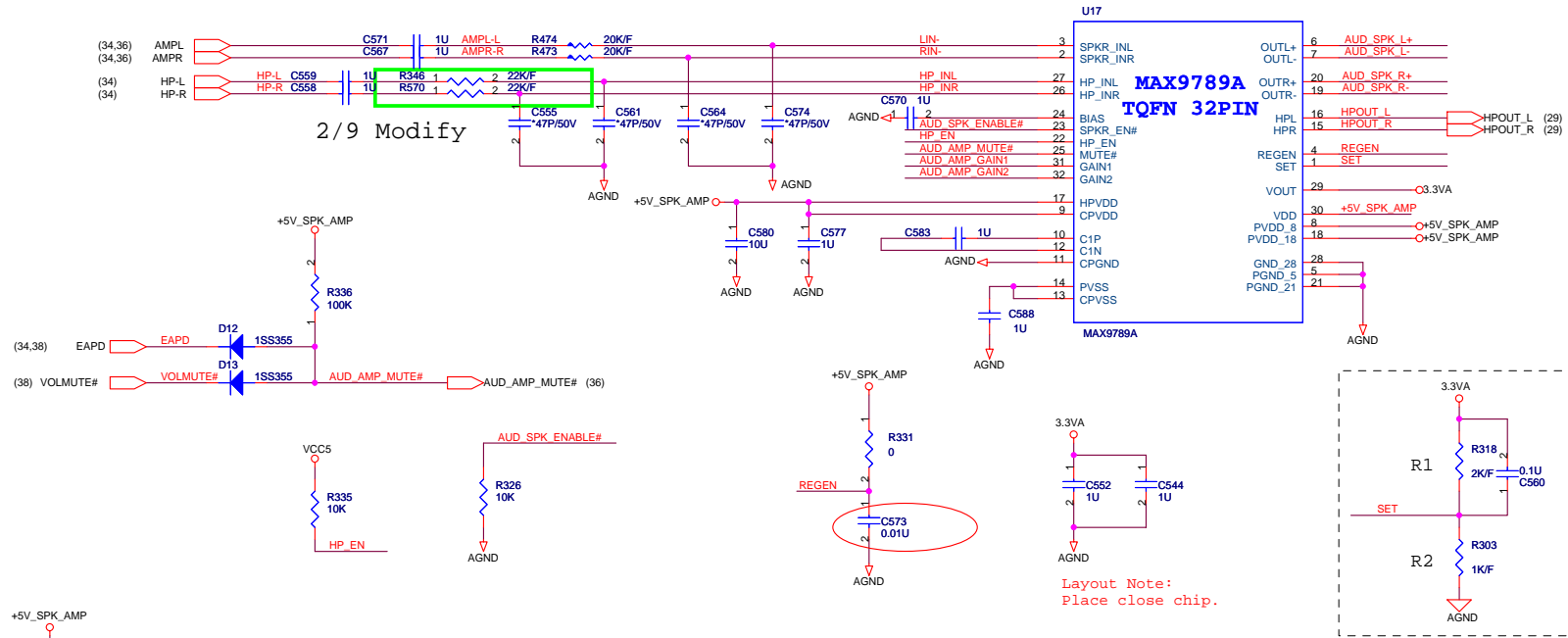
Bottom Side





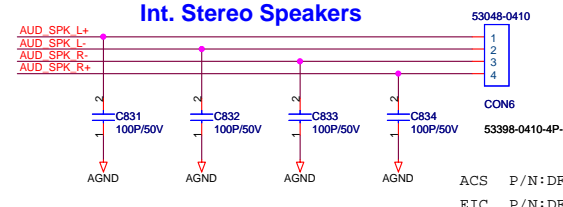
AUDIO AMPLIFIER

35



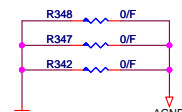
GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

Int. Stereo Speakers



ACS P/N: DFHD04MR779
EIC P/N: DFWF04MS427

FOR EMI SOLUTION



$$V_{LDO_OUT} = V_{set} (1 + R1/R2)$$

$$V_{set} = 1.21V$$



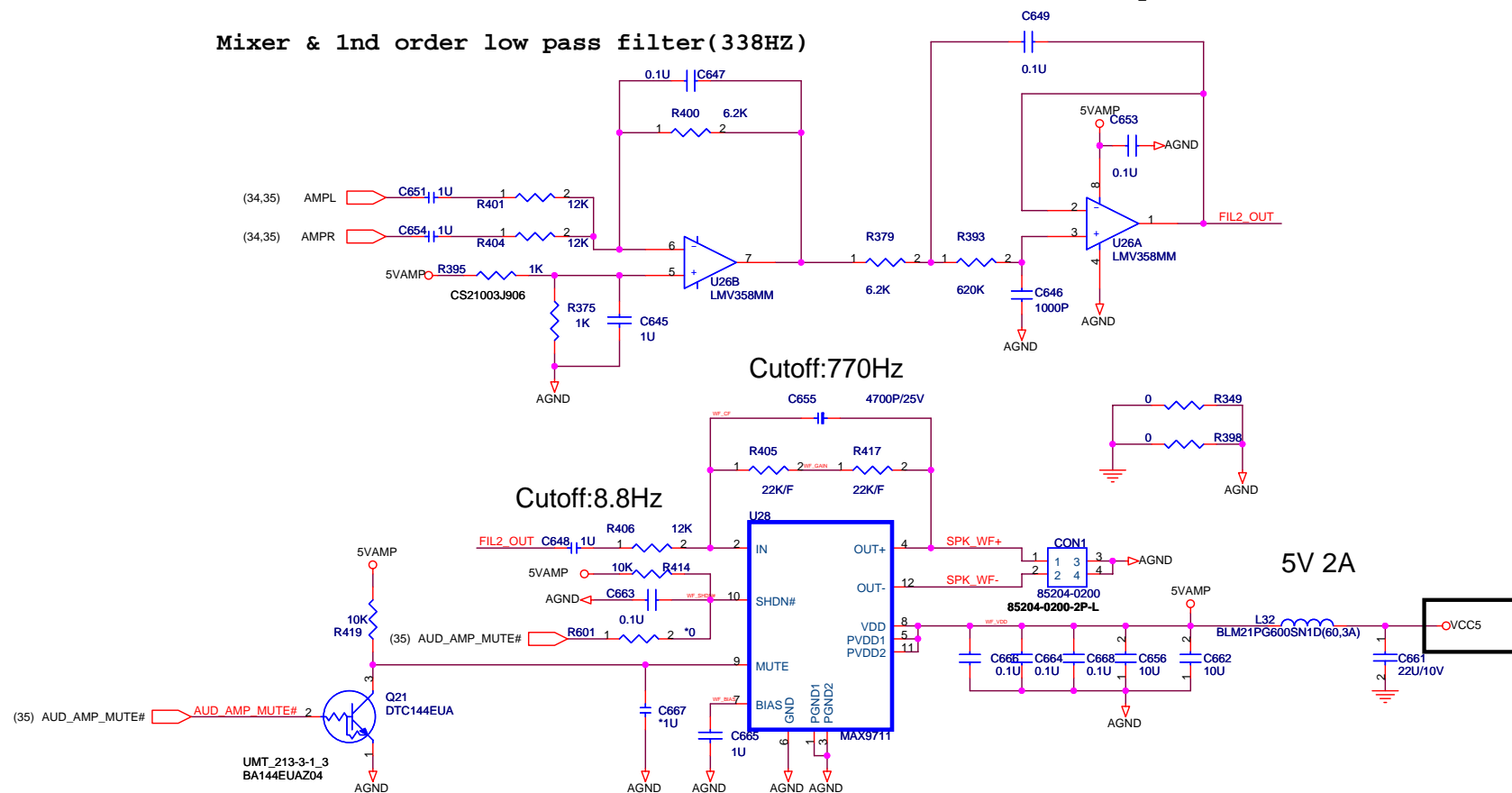
Quanta Computer Inc.
PROJECT : PB2

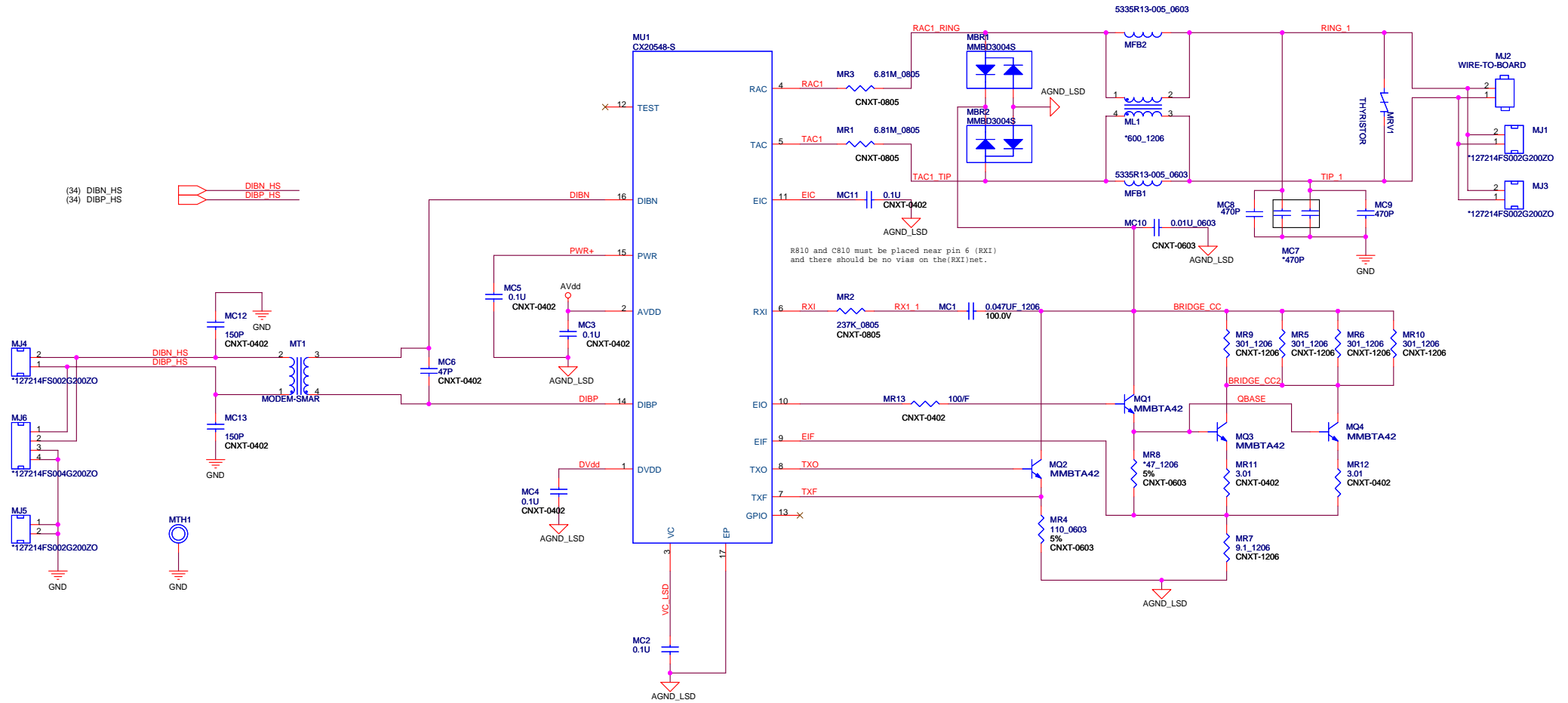
Size	Document Number	Rev
	AUDIO	A

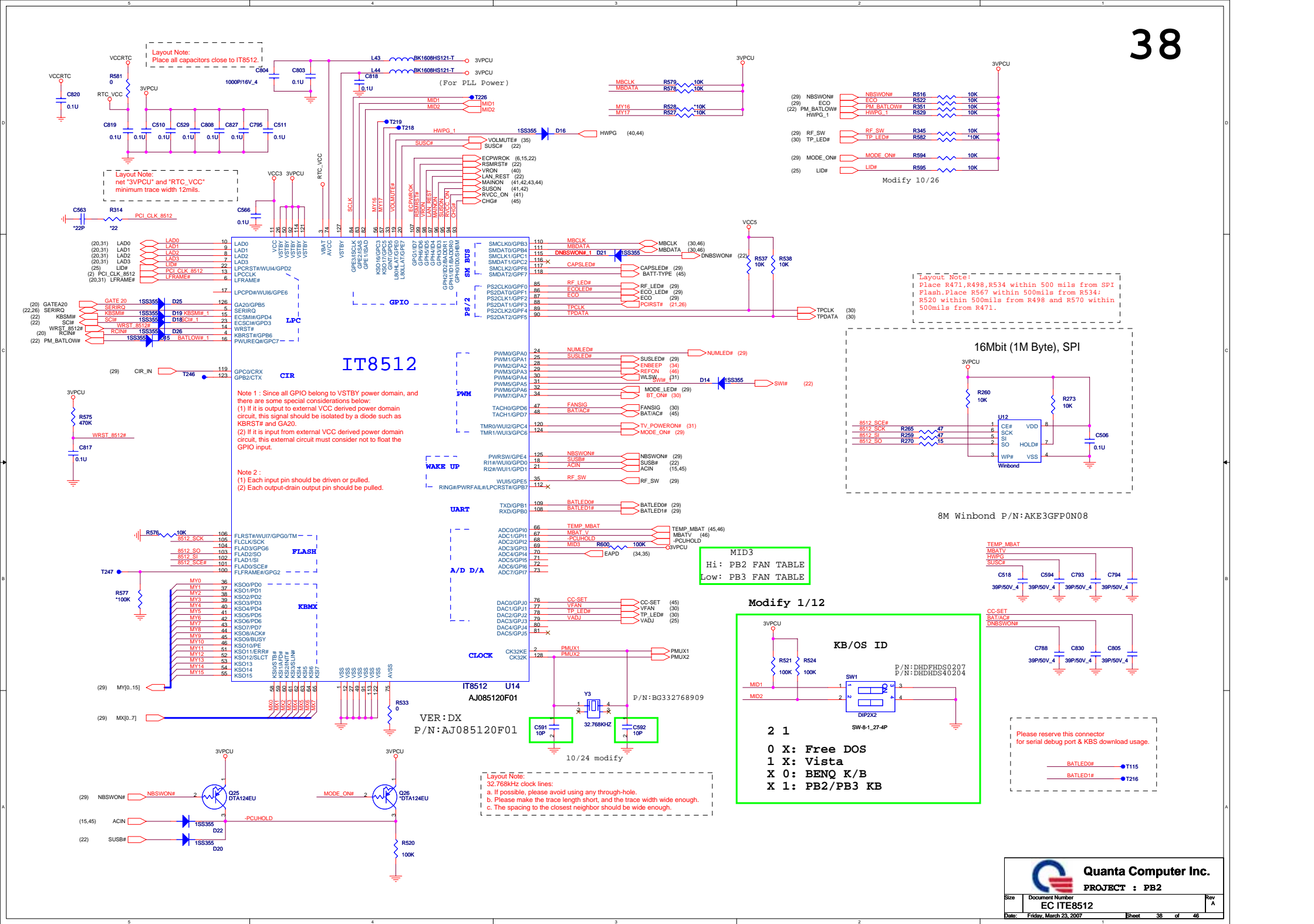
Date: Friday, March 23, 2007 Sheet 35 of 46

Mixer & 1st order low pass filter(338HZ)

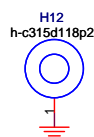
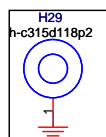
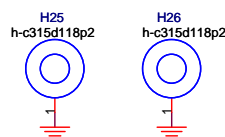
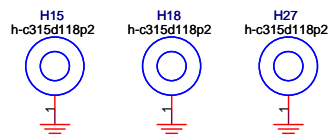
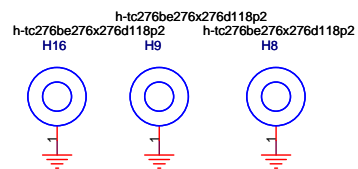
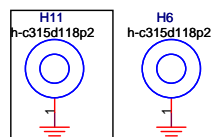
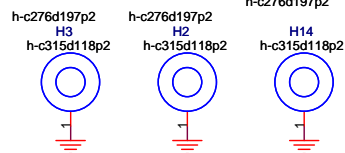
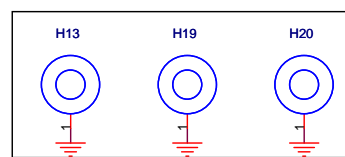
2nd order low pass filter(338HZ)



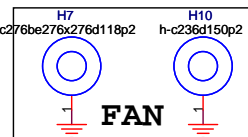
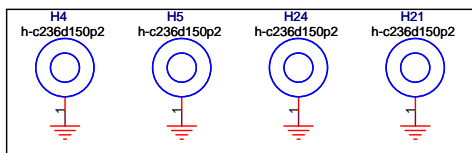




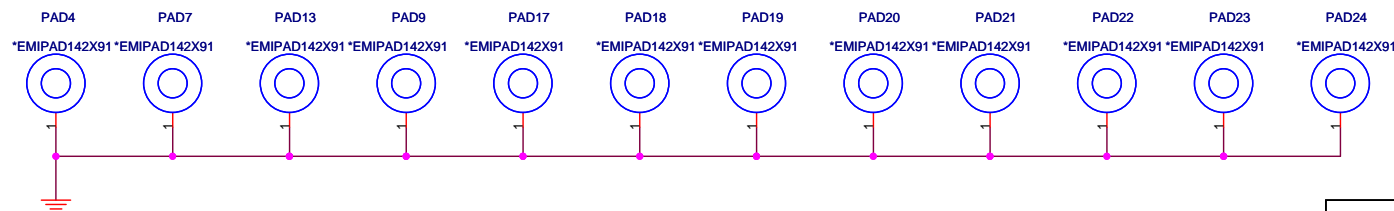
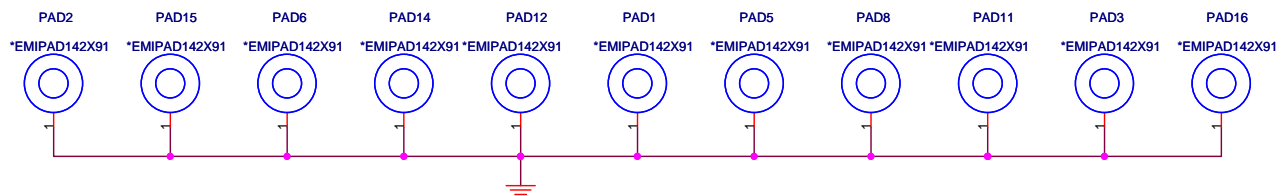
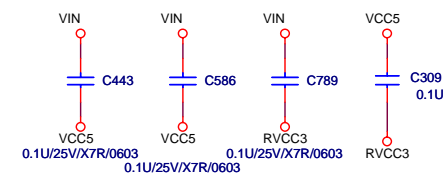
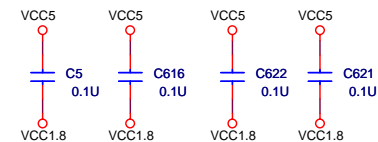
CPU



PCI_E



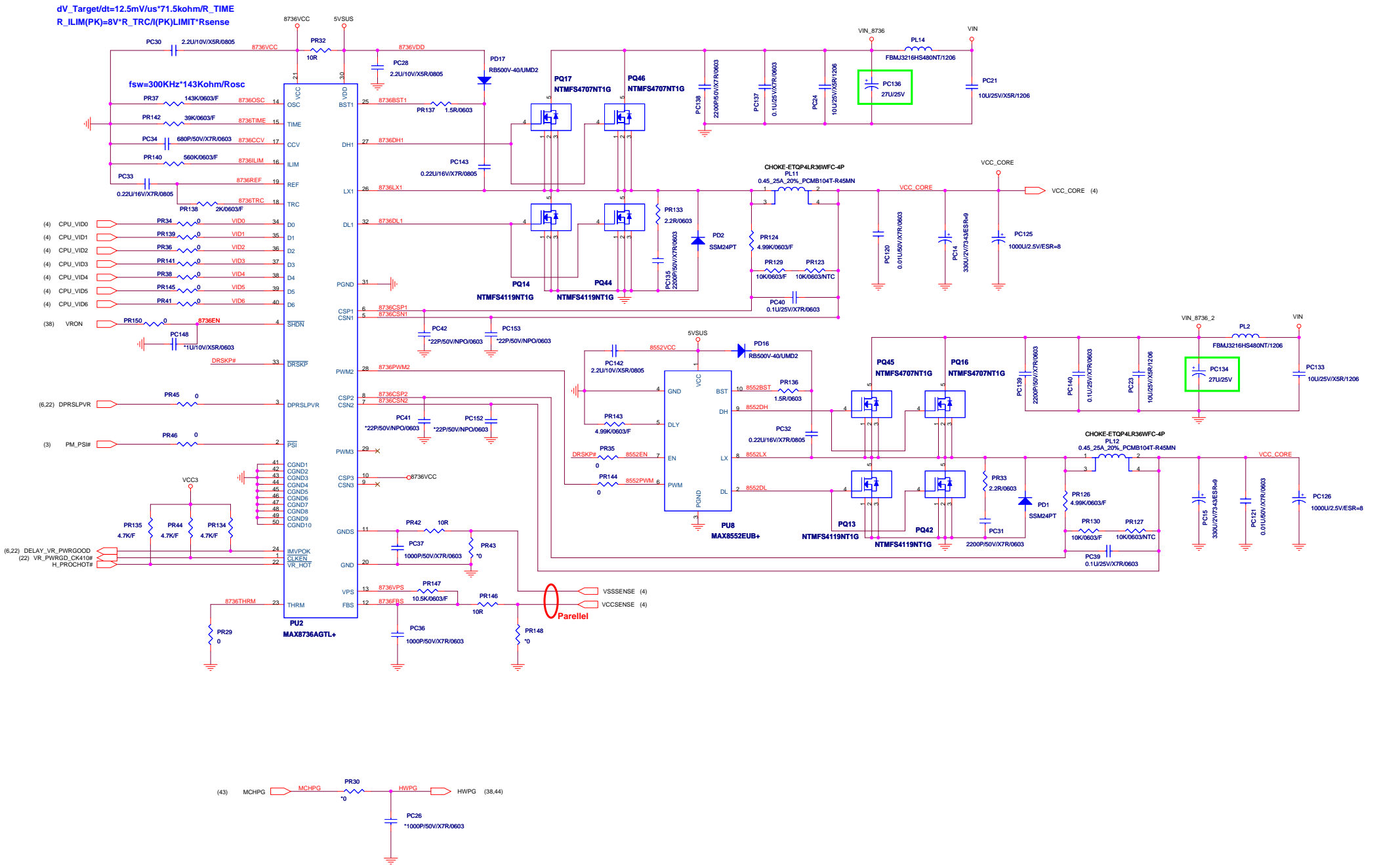
For EMI

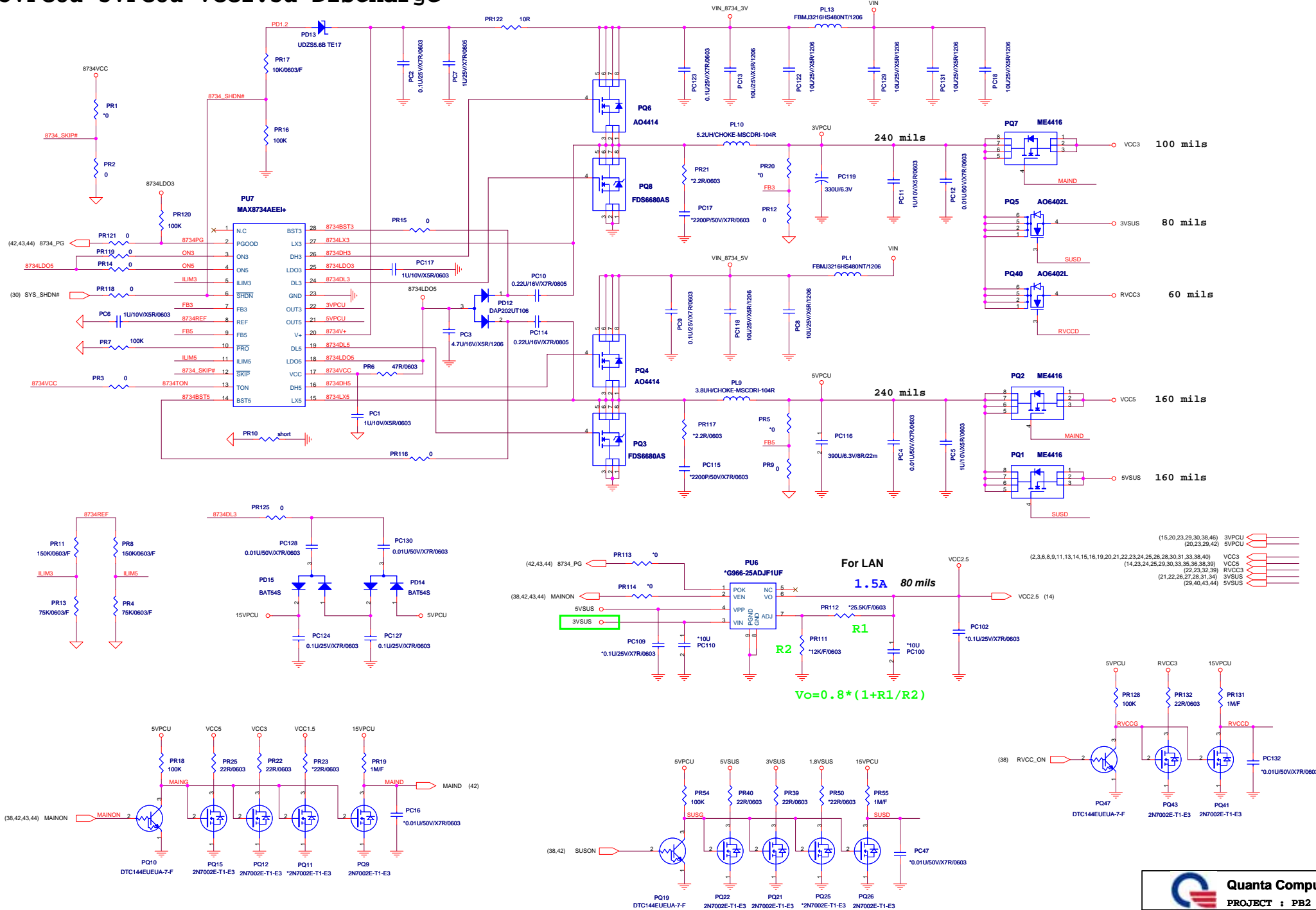


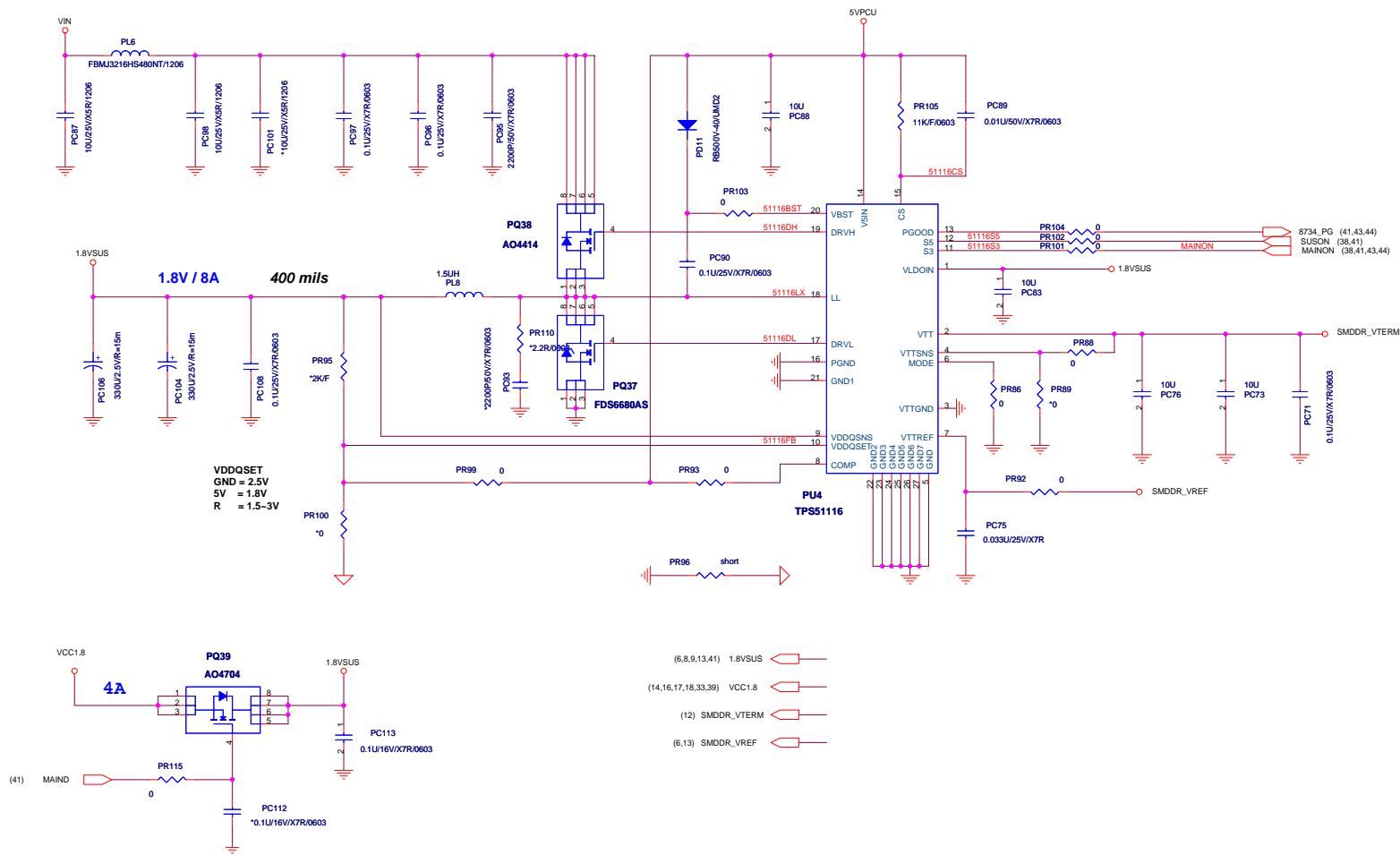
Quanta Computer Inc.

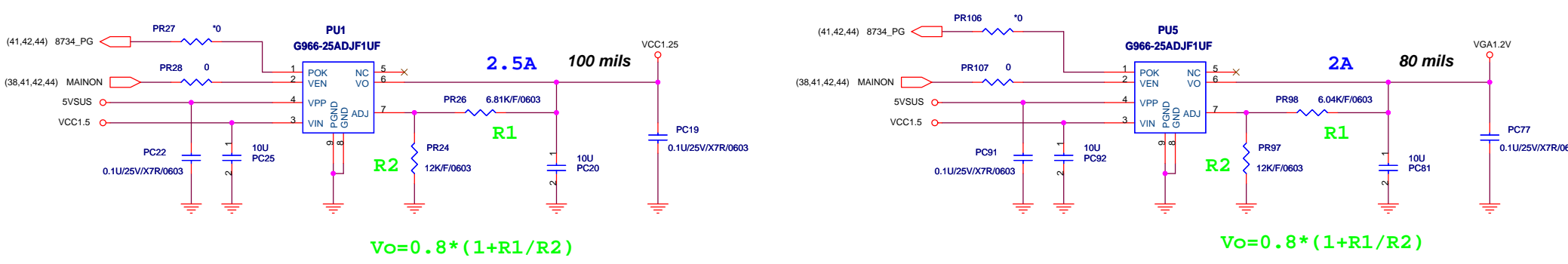
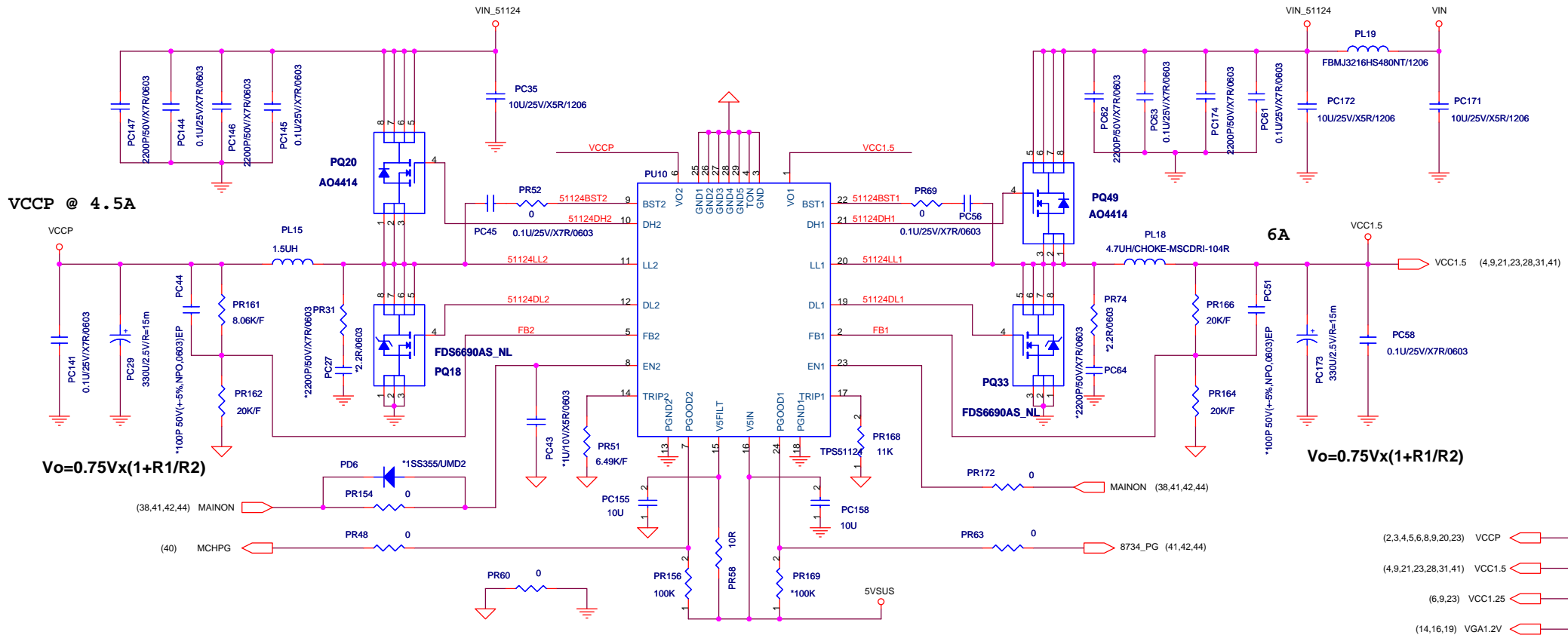
PROJECT : PB2

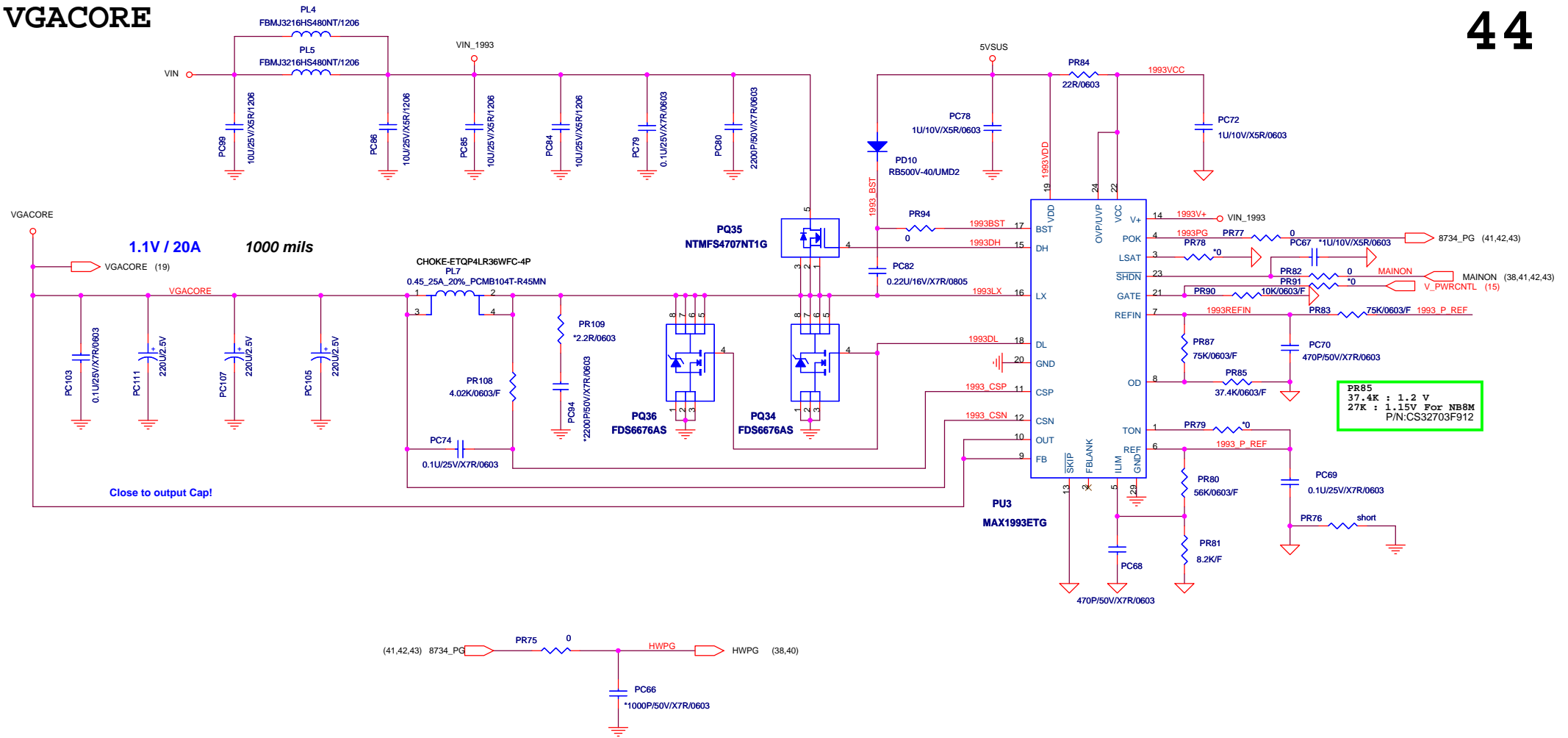
Size	Document Number	Rev
	EMI/SCREW	A
Date:	Friday, March 23, 2007	Sheet 39 of 46

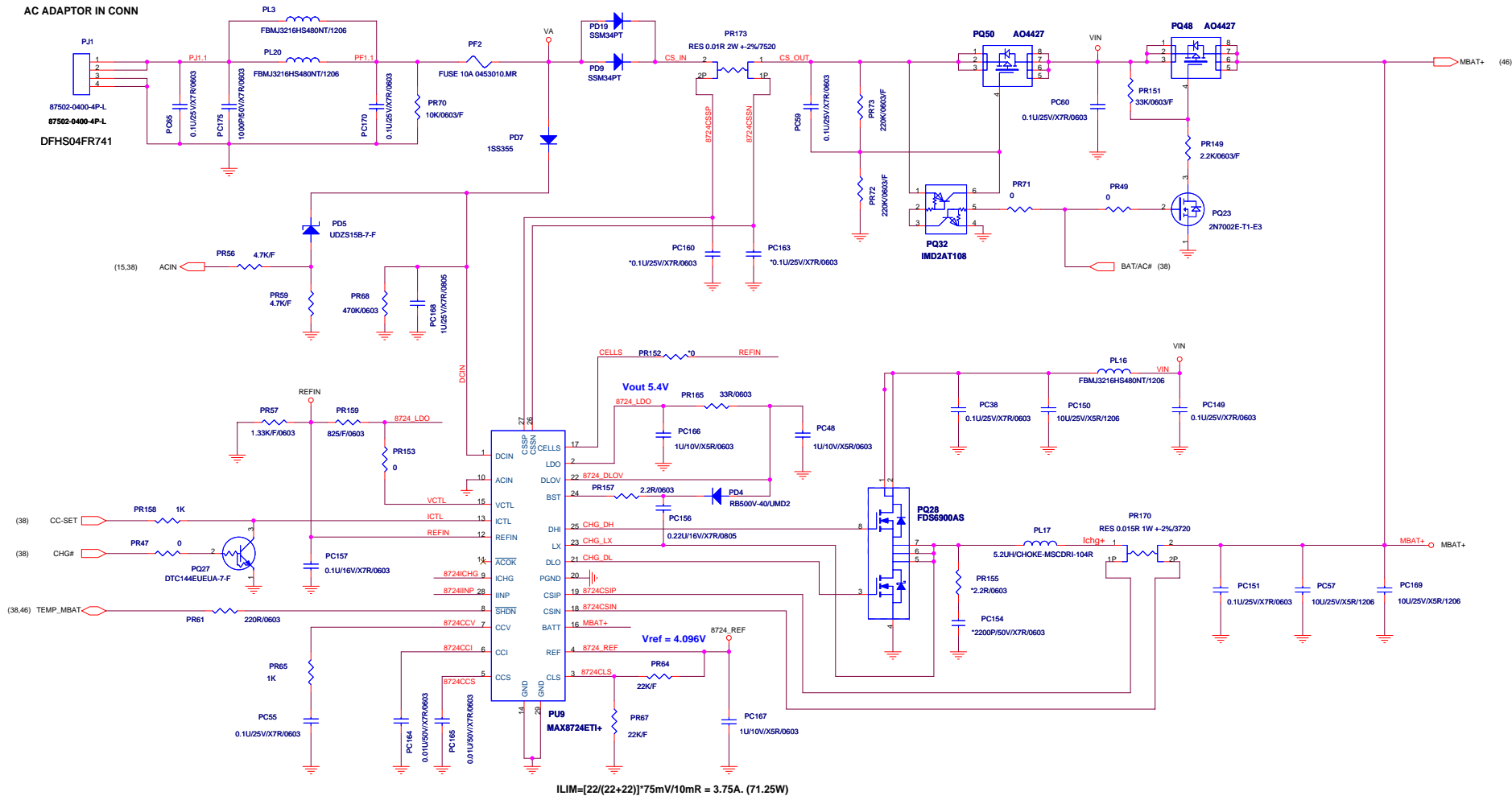




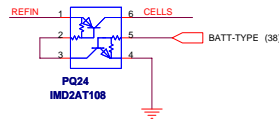
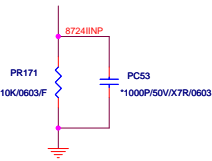
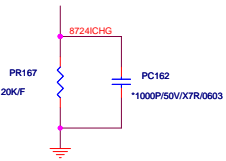








$$ILIM = \frac{22 \times (22 + 22)}{75mV/10mR} = 3.75A. (71.25W)$$



BATT-TYPE	
High	Low
Li-Ion 4S2P	Li-Ion 3S2P
Li-Ion 4S1P	Li-Ion 3S1P
Ni-MH 8S1P	

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