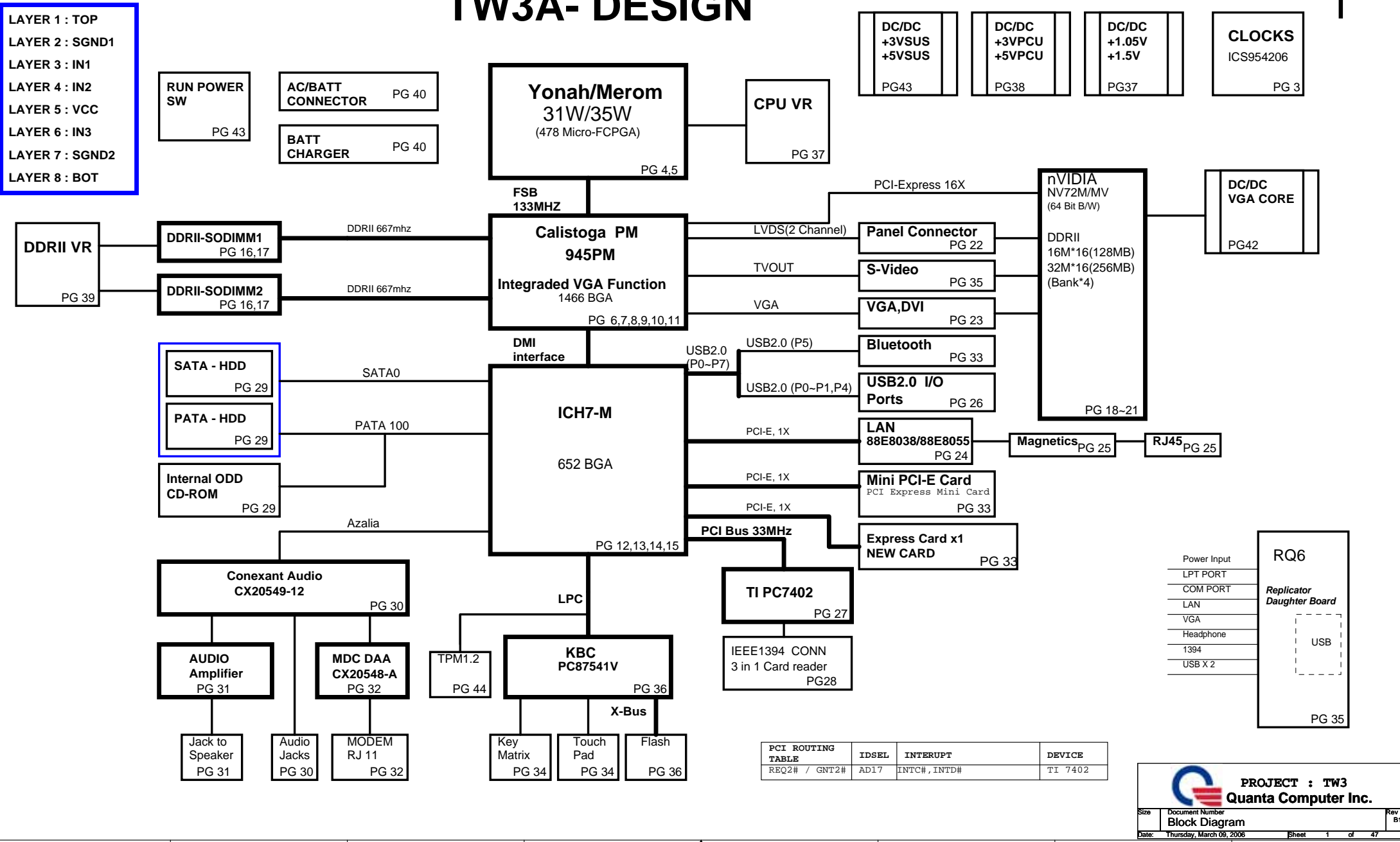


## 1

LAYER 1 : TOP  
LAYER 2 : SGND1  
LAYER 3 : IN1  
LAYER 4 : IN2  
LAYER 5 : VCC  
LAYER 6 : IN3  
LAYER 7 : SGND2  
LAYER 8 : BOT



PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ2# / GNT2#	AD17	INTC#,INTD#	TI 7402

Power Input

LPT PORT

COM PORT

LAN

VGA

Headphone

1394

USB X 2

RQ6

Replicator  
Daughter Board

USB

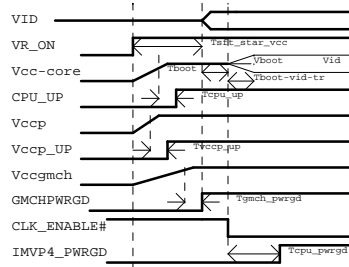
PG 35

## Board Stack up Description

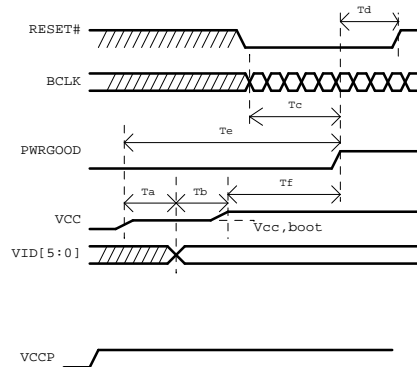
## PCB Layers

Layer 1		TOP (Component, Other)
Layer 2		Ground Plane
Layer 3		IN1
Layer 4		IN2
Layer 5		Power Plane
Layer 6		IN3
Layer 7		Ground Plane
Layer 8		BOTTOM

Power On Sequencing Timing Diagram



Dothan Power-up Timing Specifications

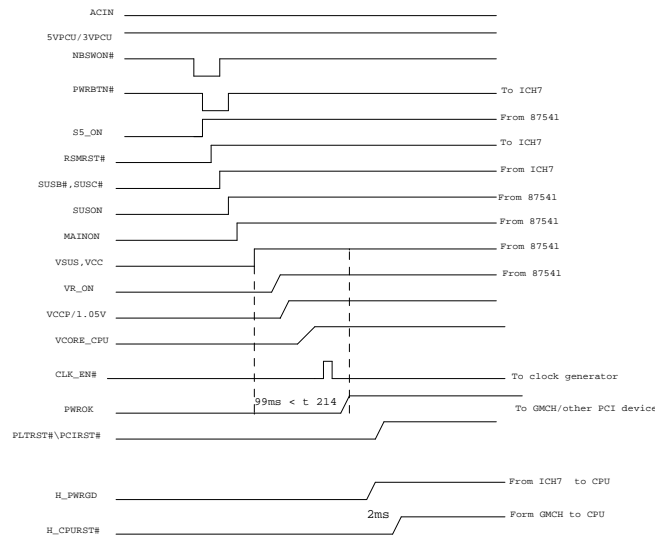


Ta=VCC and VCCP assertion to VID[5:0] valid  
Tb=VID[5:0] stable to VCC valid  
Tc=BCLK stable to PWRGOOD assertion  
Td=PWRGOOD to RESET# de-assertion time  
Te=Vcc.boot valid to PWRGOOD assertion time

## Voltage Rails

Voltage Rails	ON S0-S2	ON S3	ON S4	ON S5	Control signal
VCC CORE Core voltage for Processor	X				VR_ON 0.726V~0.94V
VCCP Core voltage for CPU / NB	X				VR_ON
SMDRR_VTERM0.9V for DDR2 Termination voltage	X				MAINON
RVCC1.5	X	X	X		RVCC_ON
RVCC3	X	X	X		RVCCD
VCC1.5	X				MAIND
VCC2.5	X				MAINON
VCC3	X				MAIND
VCC5	X				MAIND
1.8VSUS	X	X			SUSON
3VSUS	X	X			SUSD
5VSUS	X	X			SUSD
3VPCU	X	X	X	X	VL
5VPCU	X	X	X	X	VL
9VPCU	X	X	X	X	5VPCU

ACIN POWER ON TIMING

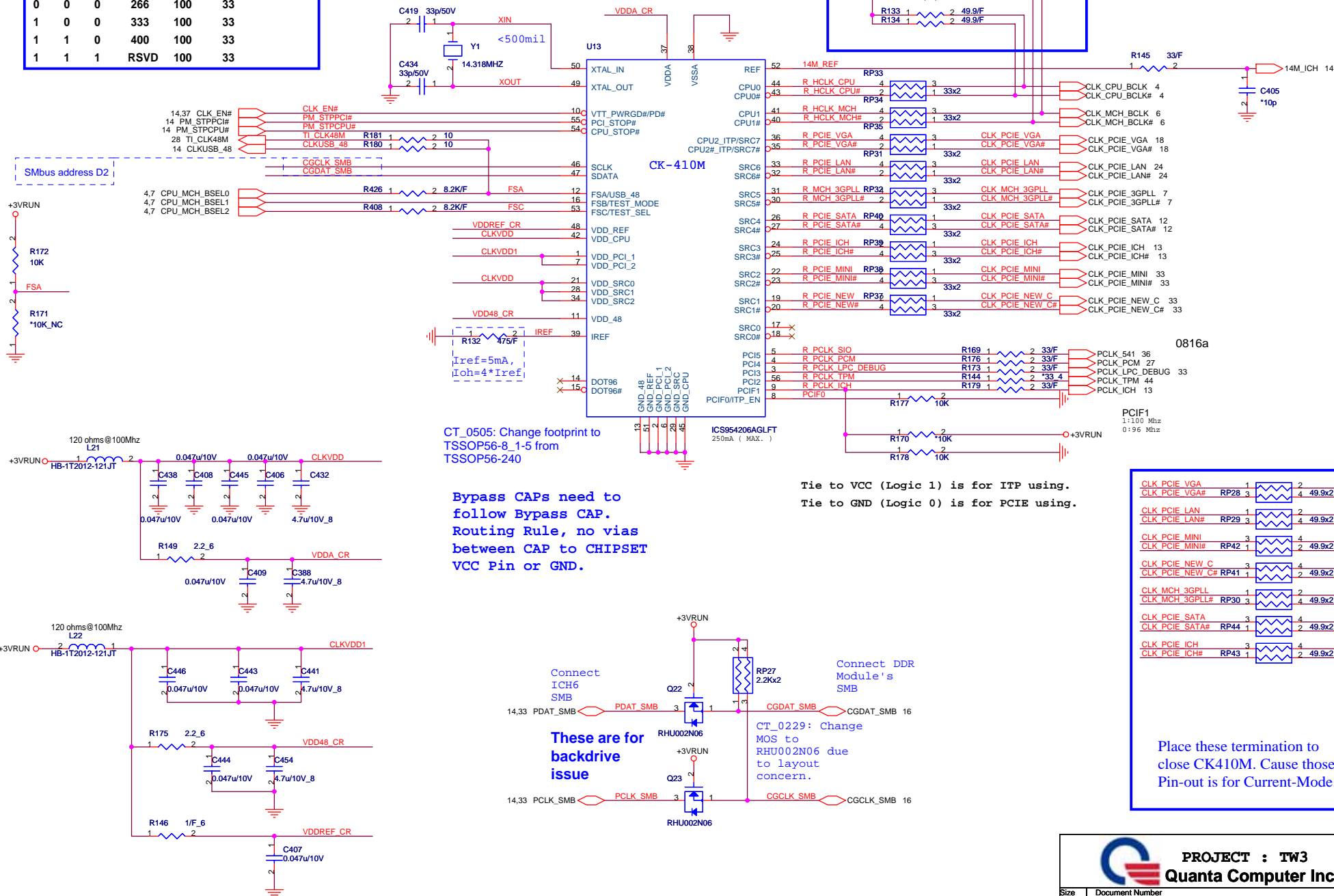
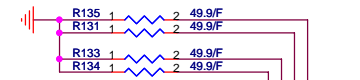


Voltage Rails	ON S0-S1	ON S3	ON S4	ON S5	Control signal
VCC CORE Core voltage for Processor	X				VRON
GMCH VTT Core voltage for GMCH 1.05V	X				MAINON
SMDRR_VTERM 0.9V for DDR II Termination voltage	X				MAINON
SMDRR_VREF 0.9V for DDR II Reference Voltage	X				MAINON
GMCH 1.5V	X				MAINON
1.8VSUS 1.8V for DDR II voltage	X	X			SUSON
2.5V	X				MAINON
3VPCU	X	X	X	X	VL
5VSUS	X	X			SUSON
3V	X				MAINON
4VPCU	X	X	X	X	VL
5VSUS	X	X			SUSON
5V	X				MAINON
VR	X	X	X	X	

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
PCI#402	AD17	REQ2# / GNT2#	PIRQ CD

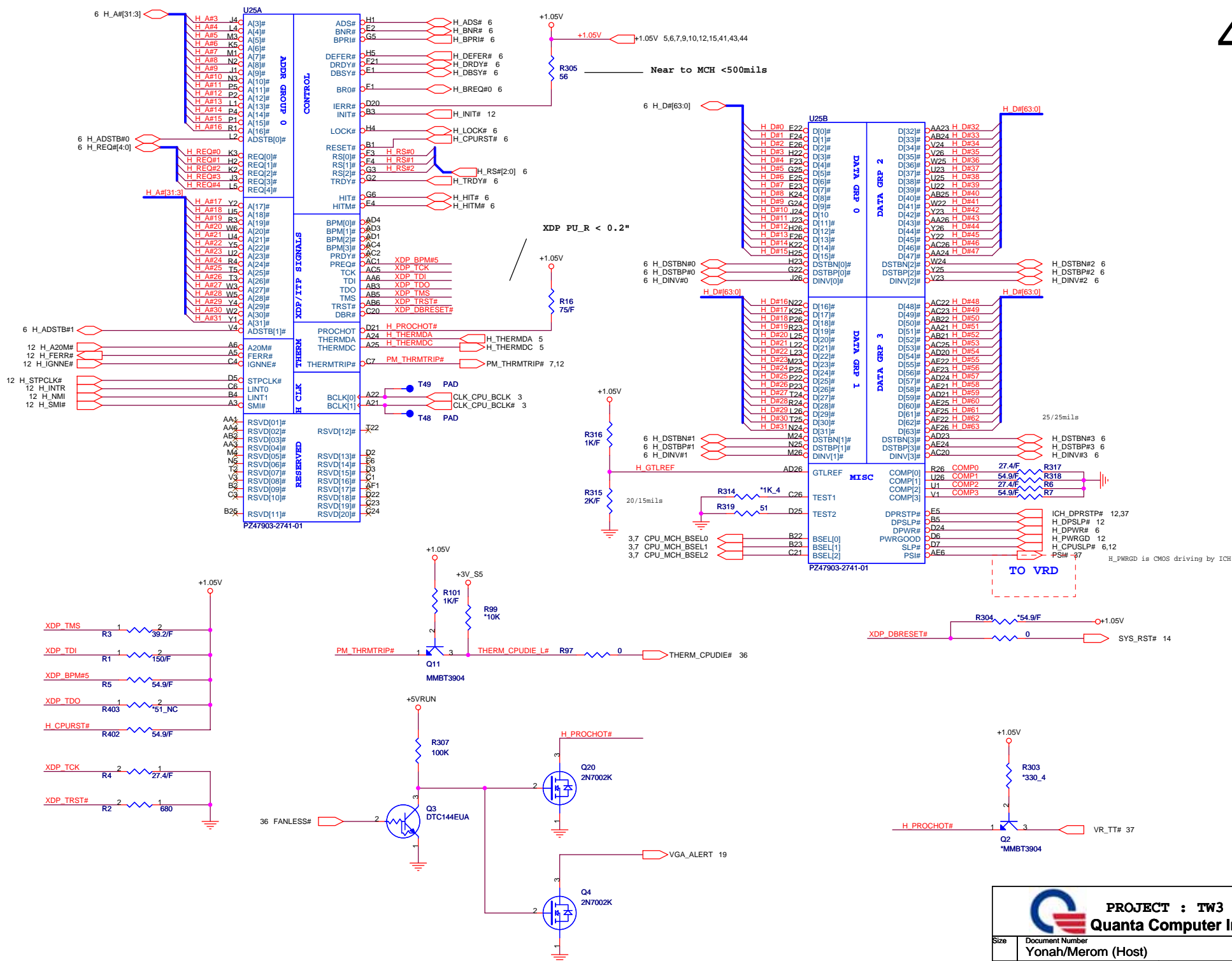
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

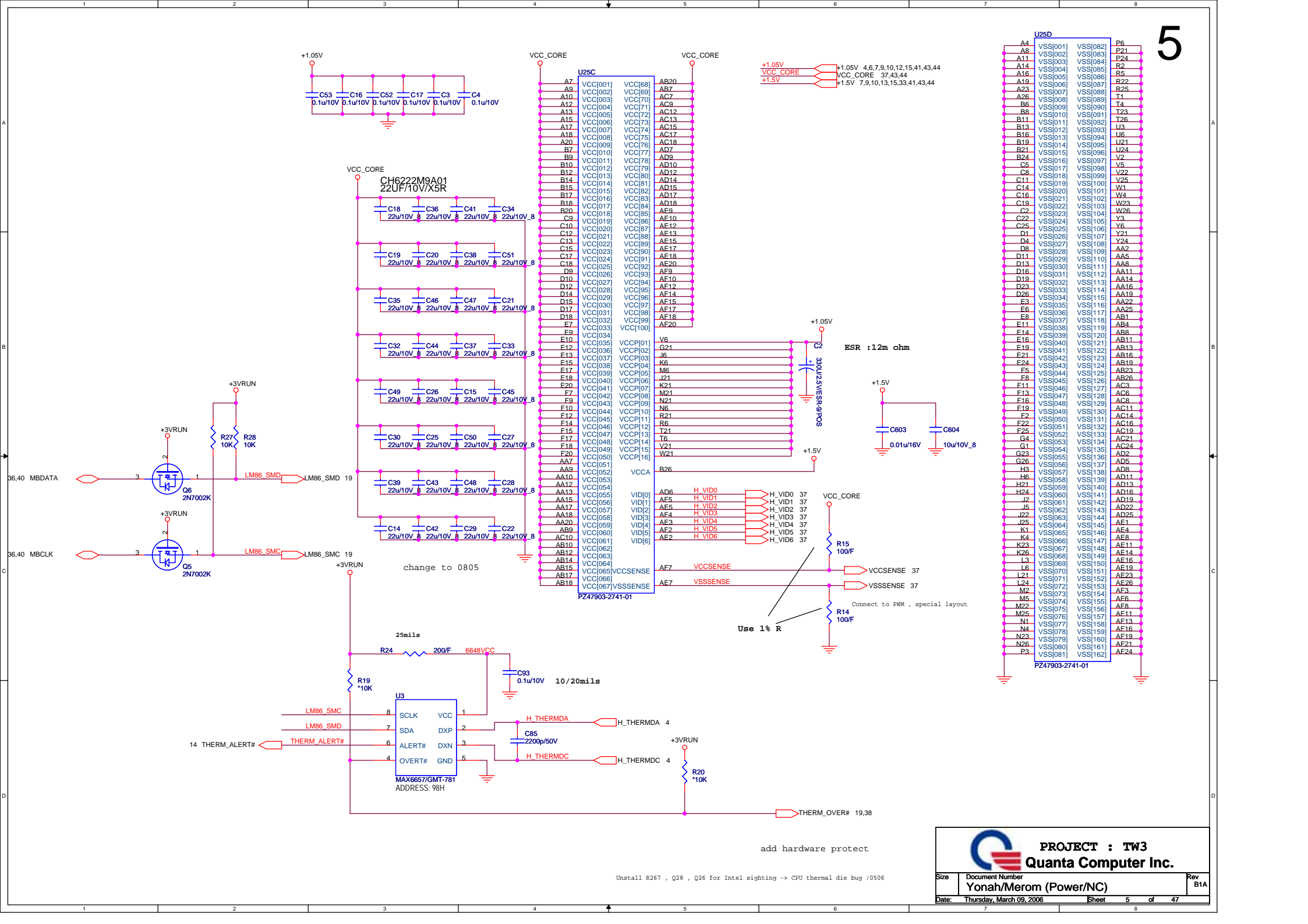
Place these termination to close CK410M. Cause those Pin-out is for Current-Mode.




Tie to VCC (Logic 1) is for ITP using.  
Tie to GND (Logic 0) is for PCIE using.

Place these termination to close CK410M. Cause those Pin-out is for Current-Mode.





5



**PROJECT : TW3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	Yonah/Merom (Power/NC)	B1A
Date:	Thursday, March 09, 2006	Sheet 5 of 47

Uninstall R267 , Q28 , Q26 for Intel sighting -> CPU thermal die bug /0506

add hardware protect

Connect to PWM , special layout

Use 1% R

change to 0805

ESR :12m ohm

P247903-2741-01

P247903-2741-01

MAX6657/GMT-781

ADDRESS: 98H

14 THERM\_ALERT#

THERM\_ALERT#

14 THERM\_ALERT#

THERM\_ALERT#

14 THERM\_ALERT#

THERM\_ALERT#

14 THERM\_ALERT#

THERM\_ALERT#

14 THERM\_ALERT#

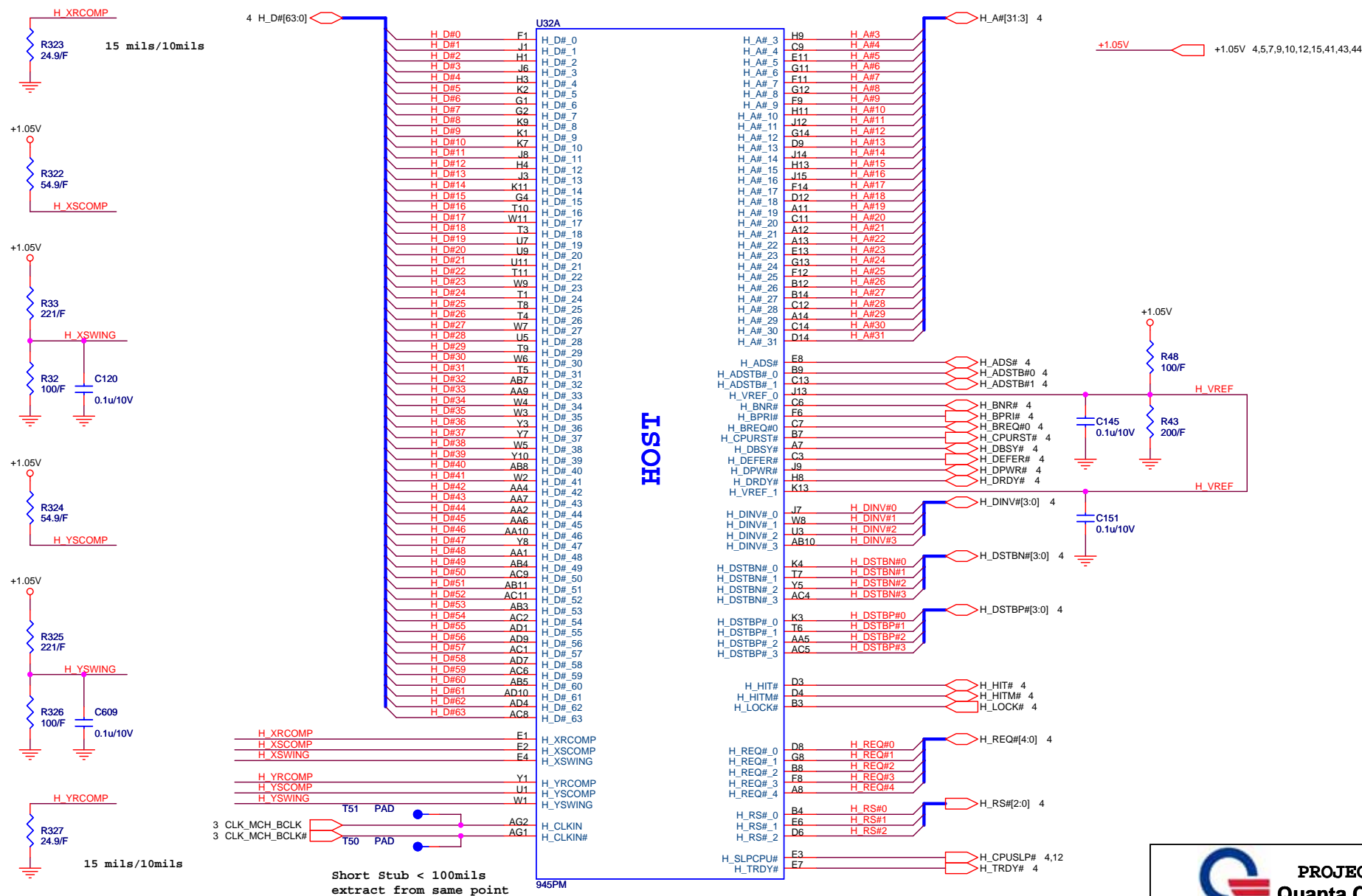
THERM\_ALERT#

14 THERM\_ALERT#

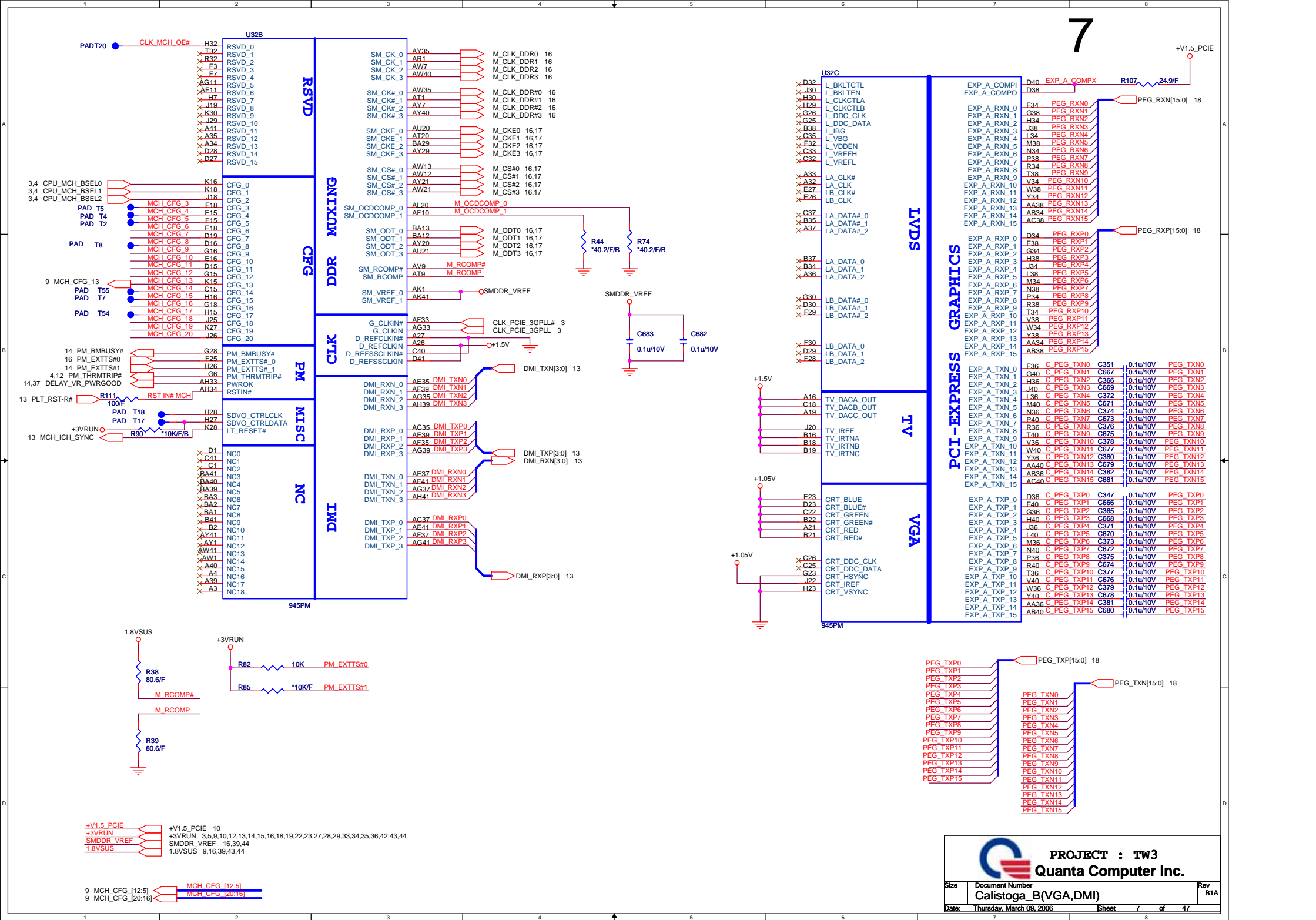
THERM\_ALERT#

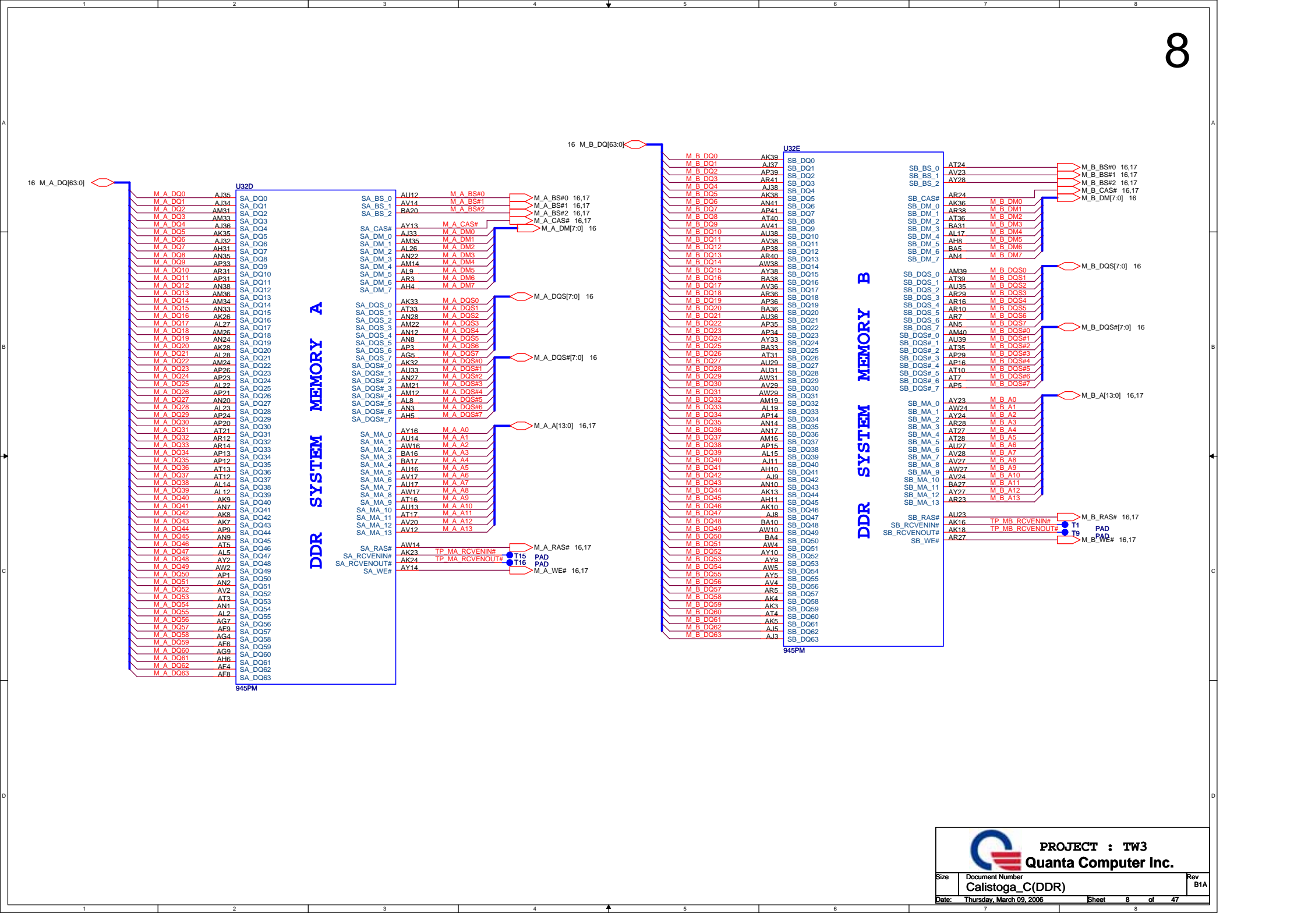
14 THERM\_ALERT#

THERM\_ALERT#

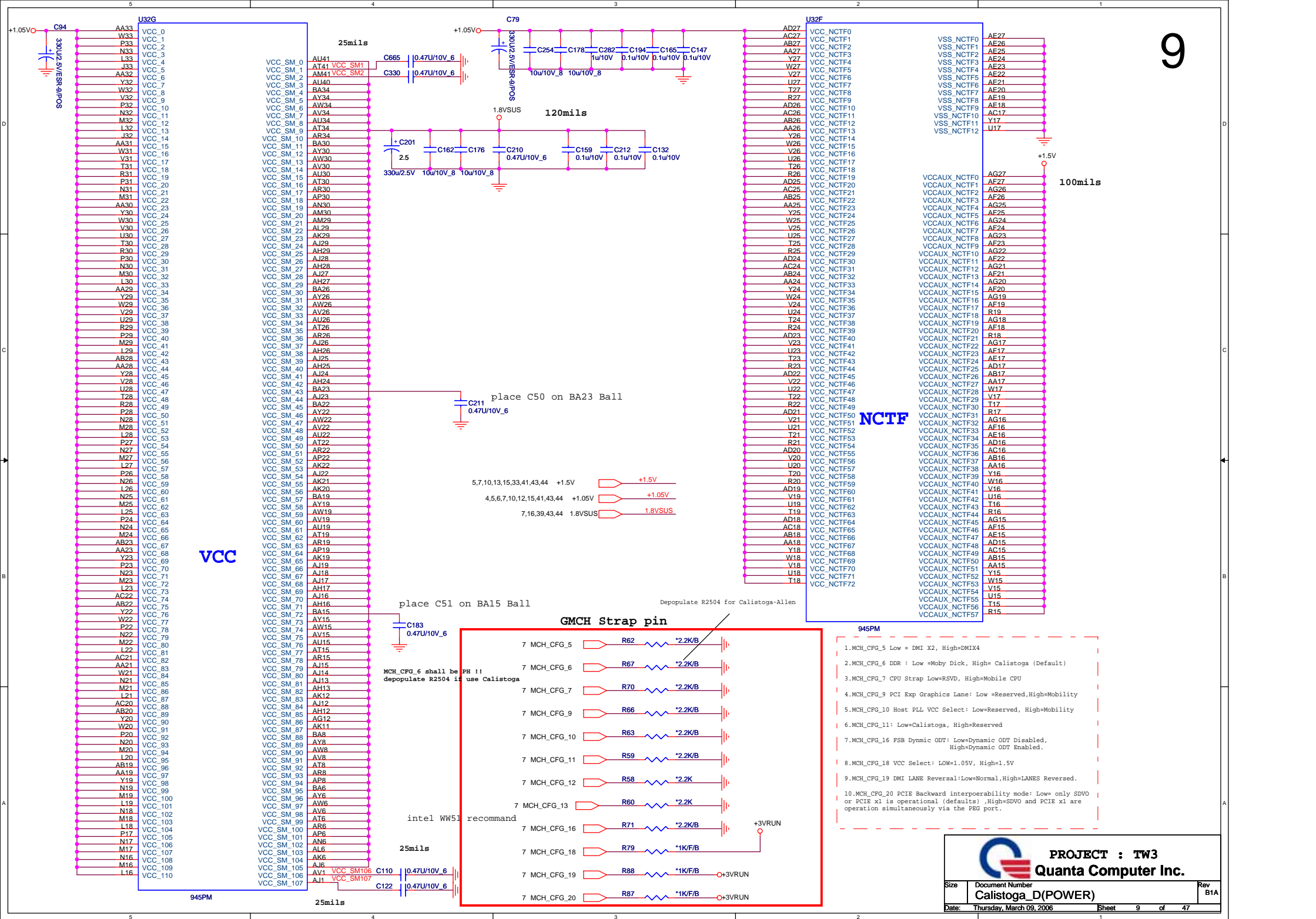


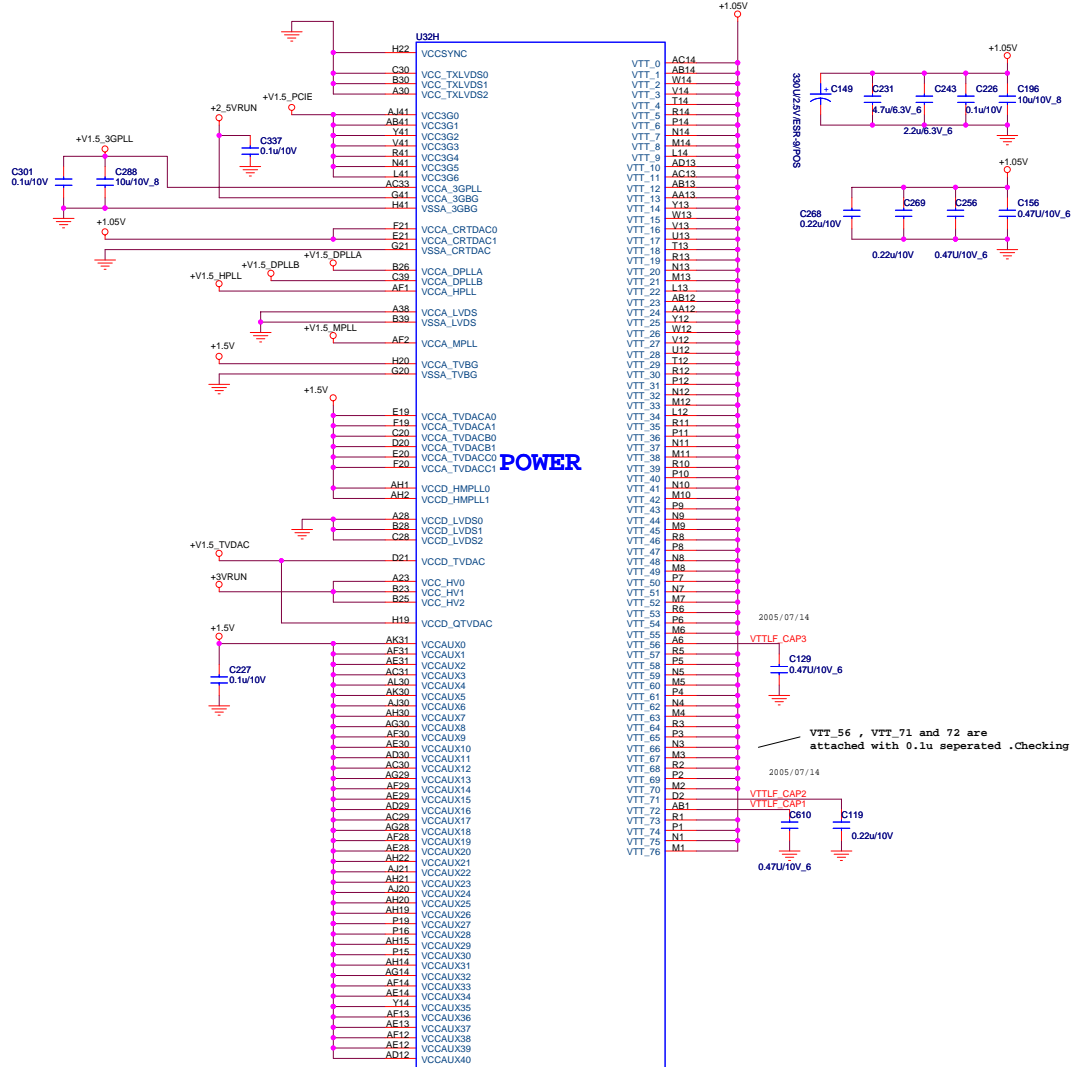
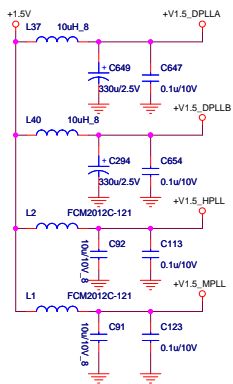
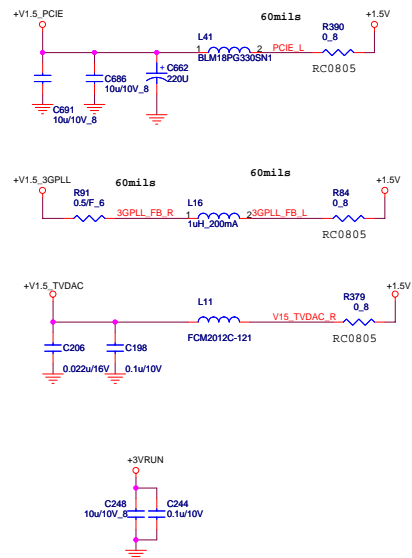




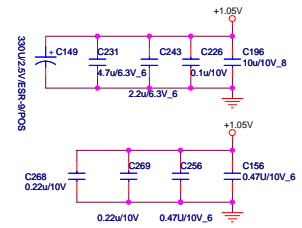








+1.05V → +1.05V 4,5,6,7,9,12,15,41,43,44  
 +1.5V → +1.5V 5,7,9,13,15,33,41,43,44  
 +V1.5\_PCIE → +V1.5\_PCIE 7  
 +2.5VRUN → +2.5VRUN 19,43,44  
 +3VRUN → +3VRUN 3,5,7,9,12,13,14,15,16,18,19,22,23,27,28,29,33,34,35,36,42,43,44



2005/07/14

VTTLE\_CAP3

C129

0.47uF/10V\_6

VTT\_56, VTT\_71 and 72 are

attached with 0.1u separated .Checking

2005/07/14

VTTLE\_CAP2

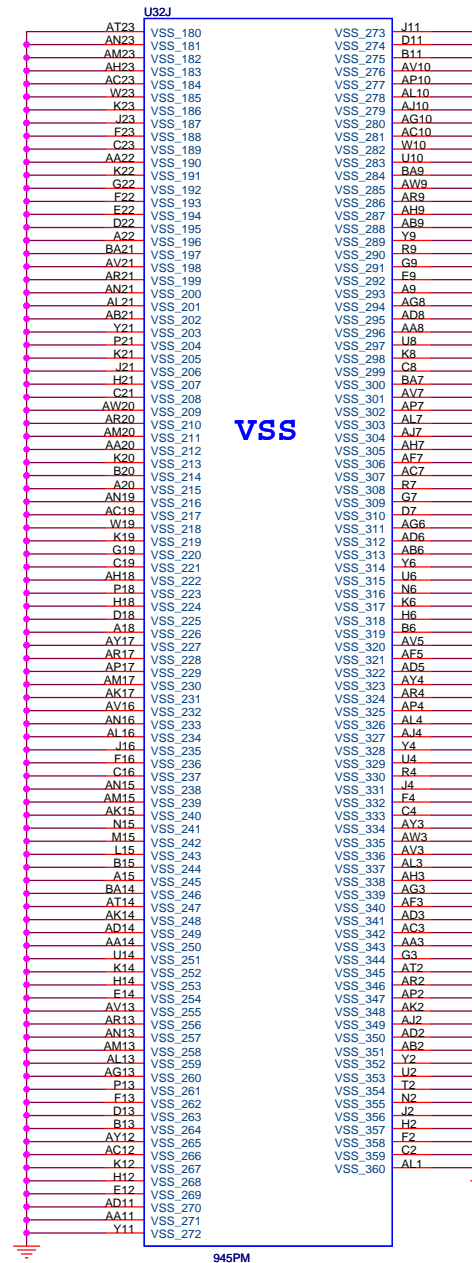
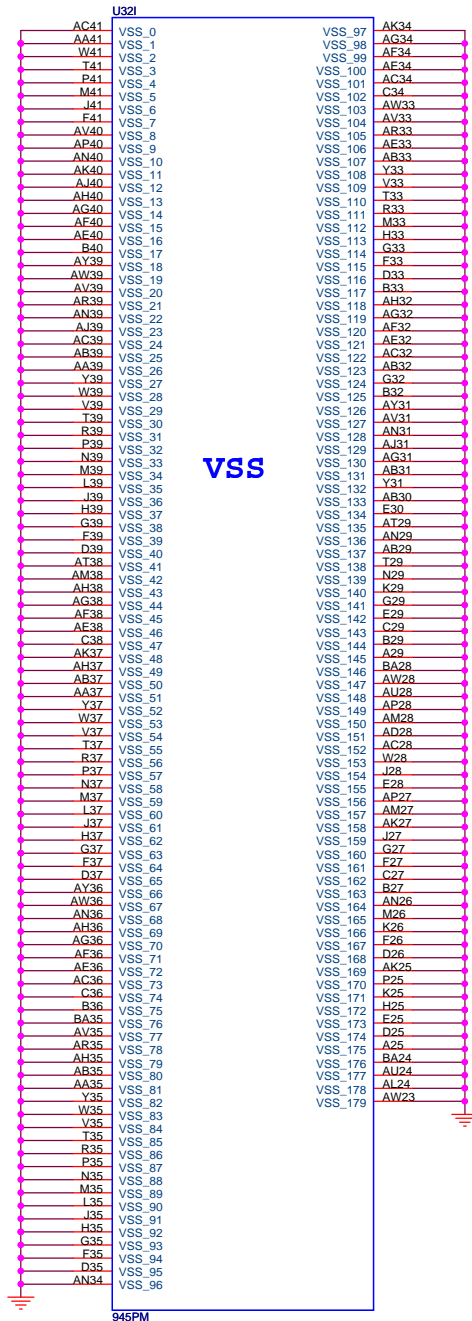
VTTLE\_CAP1

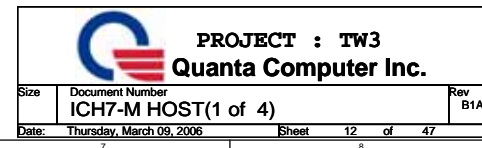
C119

0.22uF/10V

C110

0.47uF/10V\_6

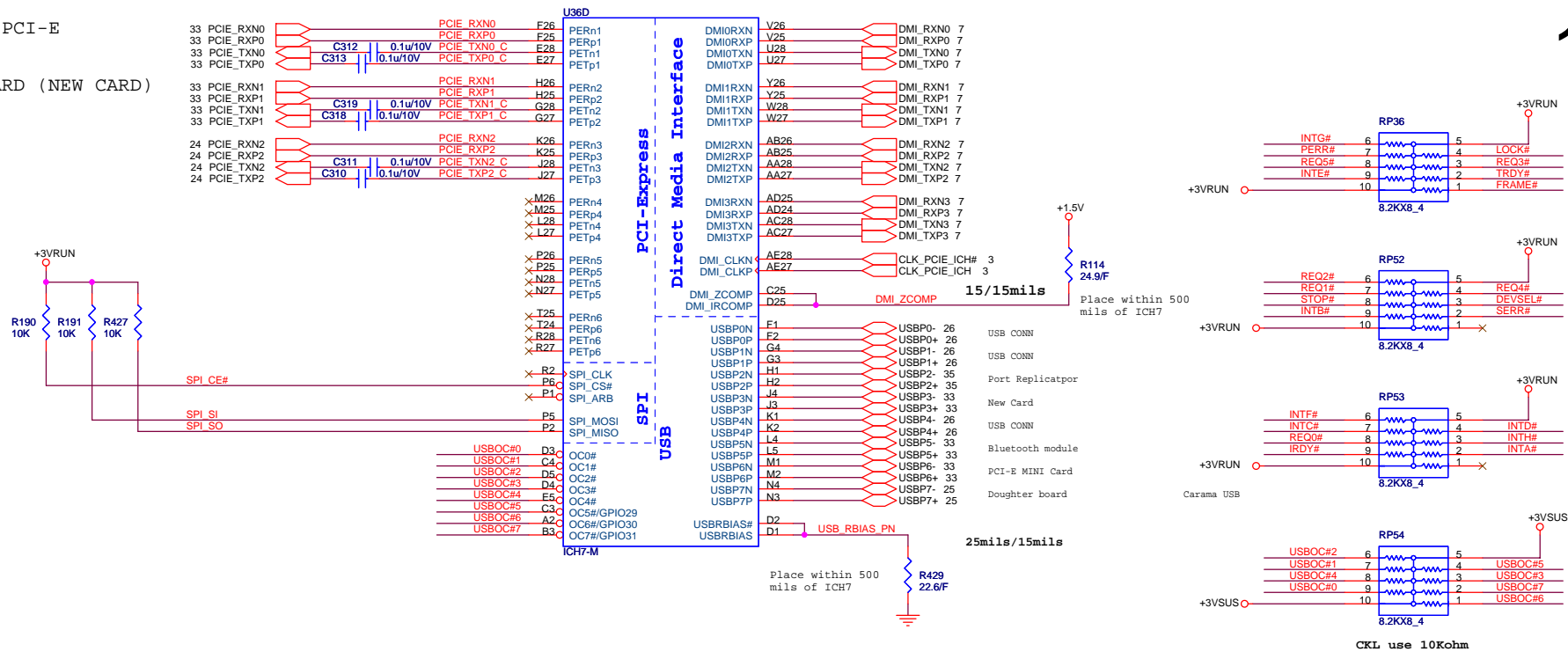




MINI CARD PCI-E

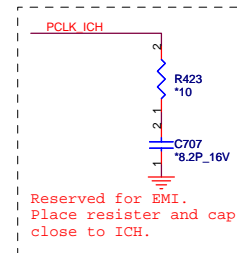
EXPRESS CARD (NEW CARD)

13



ICH7 Boot BIOS select

	STRAP	GNT5# R1	GNT4# R2
LPC (default)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF



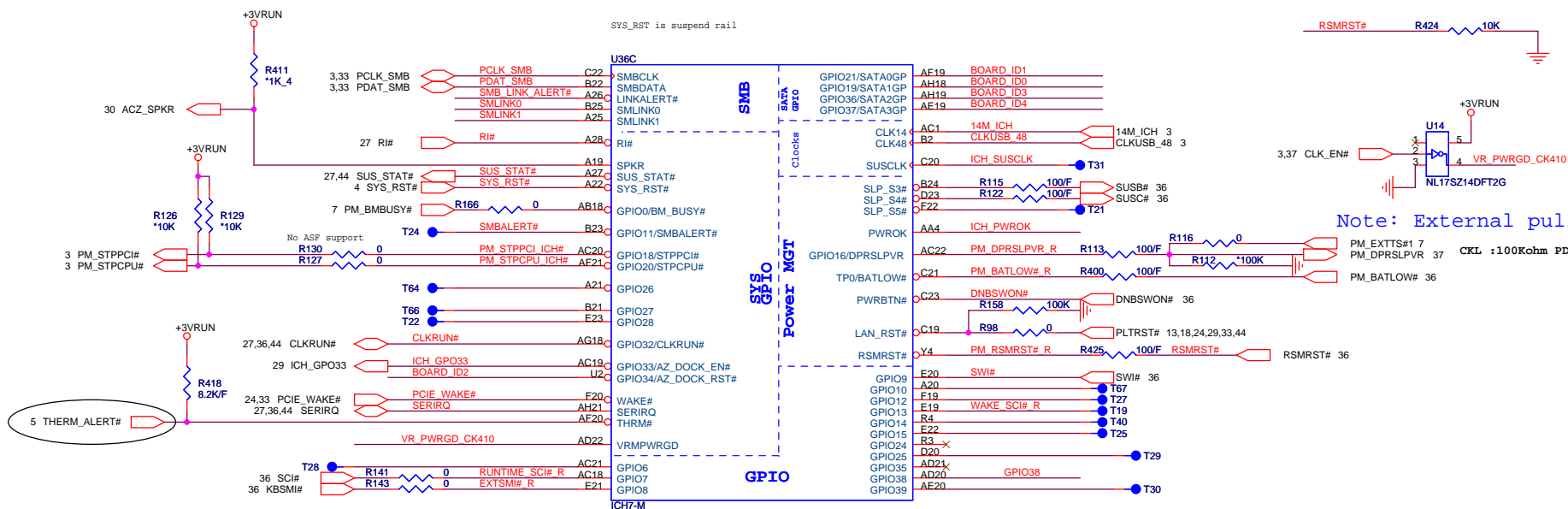
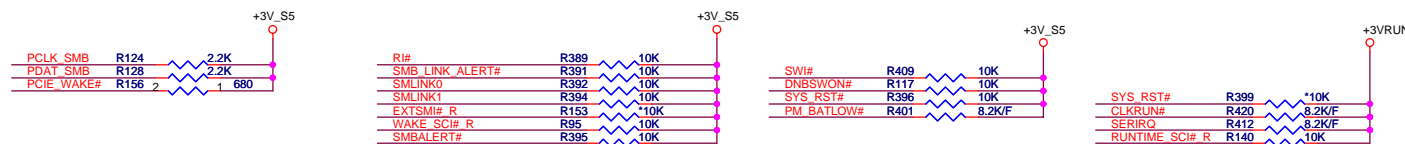
**PROJECT : TW3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	ICH7-M PCI E(2 of 4)	B1A
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Don't connect to PCI device / Express card

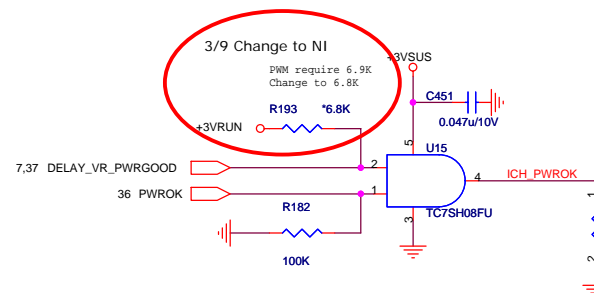
R376

No stuff-->boot  
Stuff-->No boot



Note: External pull-up 3V

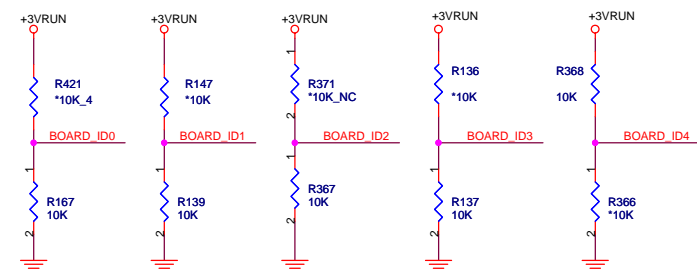
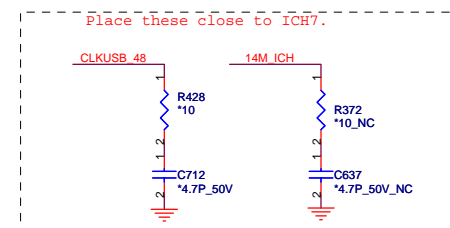
GPIO25 /Suspend rail is a HW strap , don't pull down .



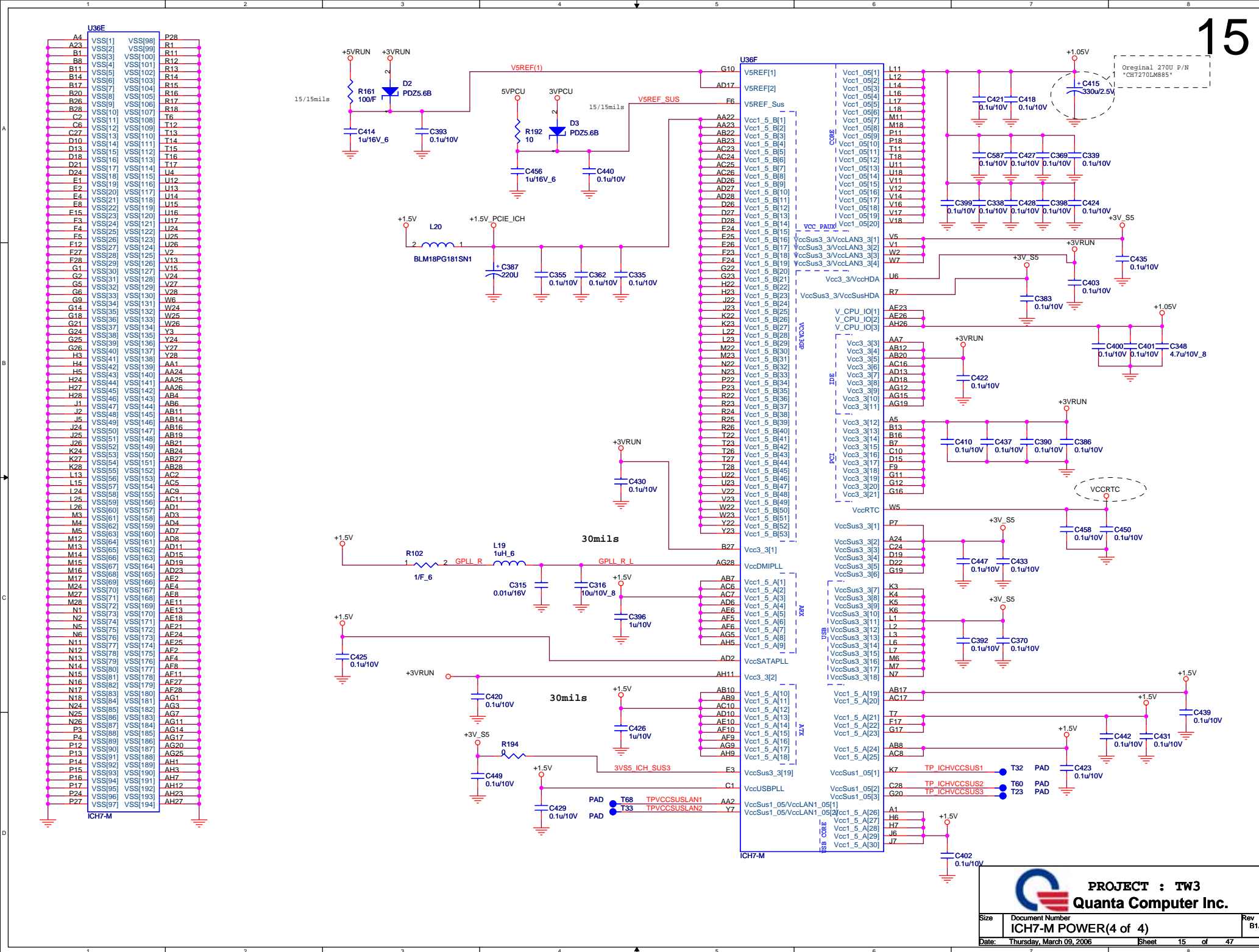
Level is incorrect !!

GPIO38	Function
High	CRT
Low	DVI

Board ID	Function
ID [1:0]	00: TW3 01: DW1
ID2	0: SATA HDD 1: PATA HDD
ID3	Reserve
ID4	0: No docking. 1: w/ docking





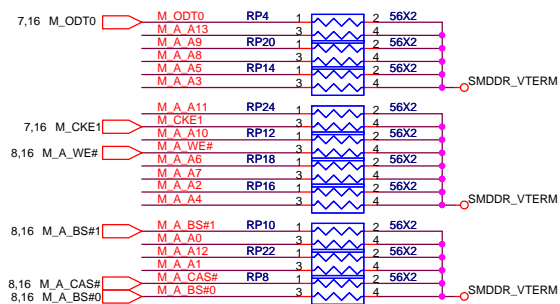
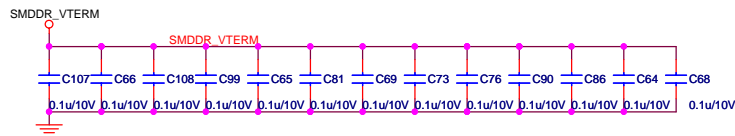




# DDRII DUAL CHANNEL A,B.

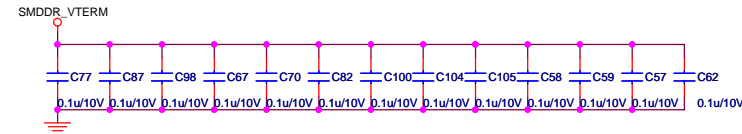
## DDRII A CHANNEL

M\_A\_A[13..0] M\_A\_A[13..0] 8,16  
SMDRR\_VTERM SMDRR\_VTERM 39,43,44

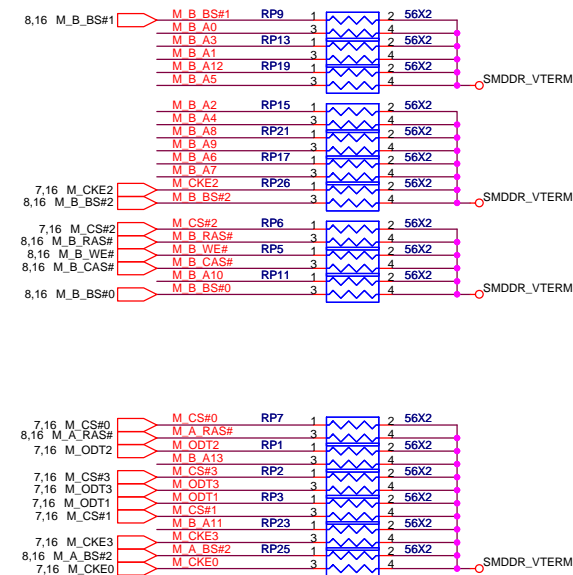


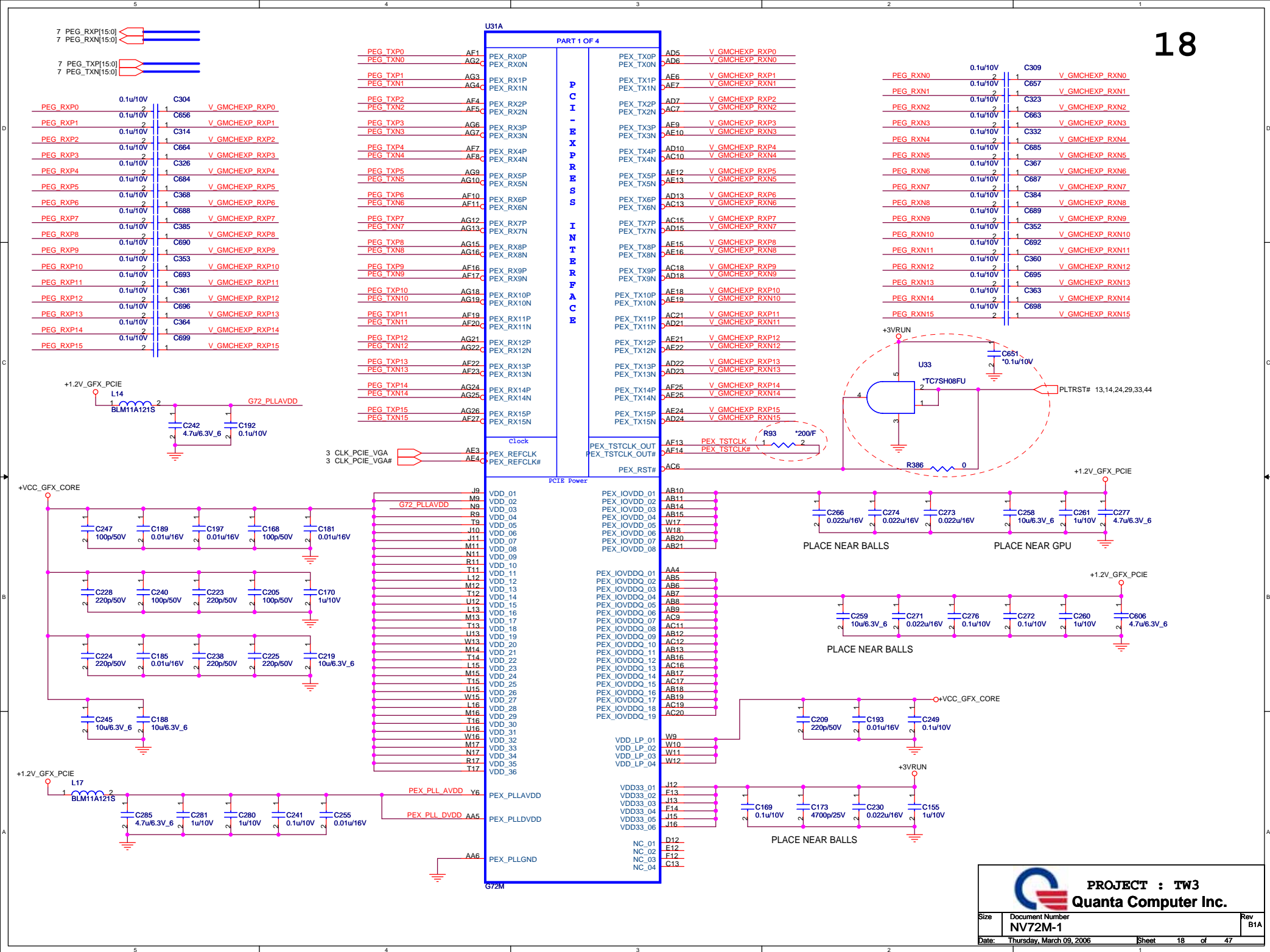
## DDRII B CHANNEL

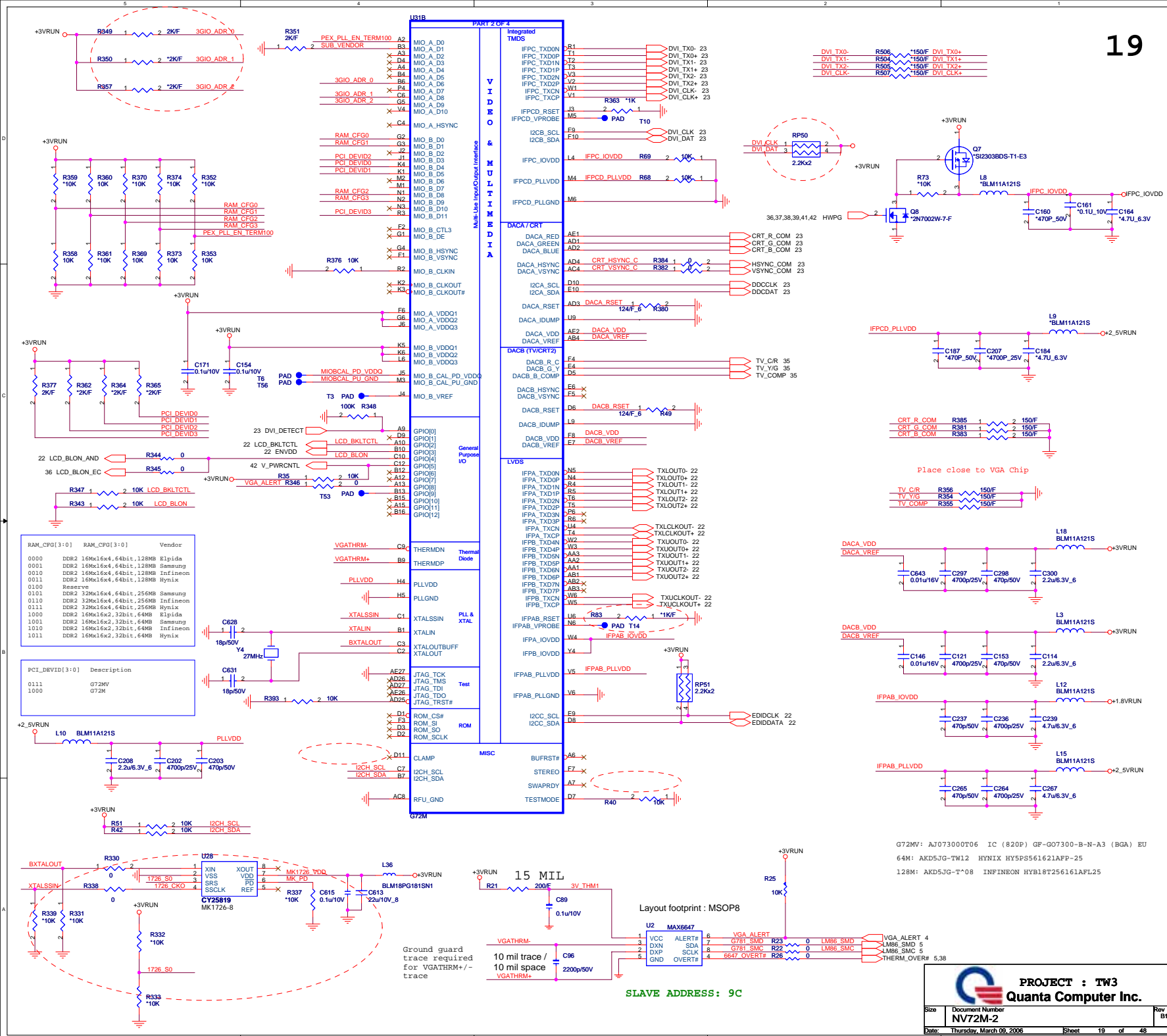
M\_B\_A[13..0] M\_B\_A[13..0] 8,16  
1.8VSUS 1.8VSUS 7,9,16,39,43,44  
+3VRUN +3VRUN 3,5,7,9,10,12,13,14,15,16,18,19,22,23,27,28,29,33,34,35,36,42,43,44



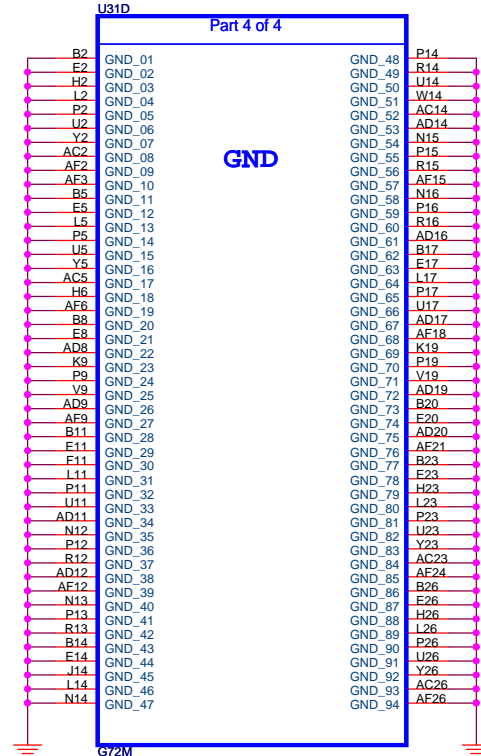
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDRR\_VTERM



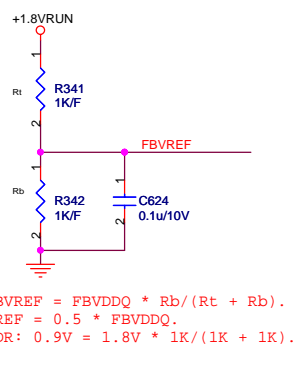
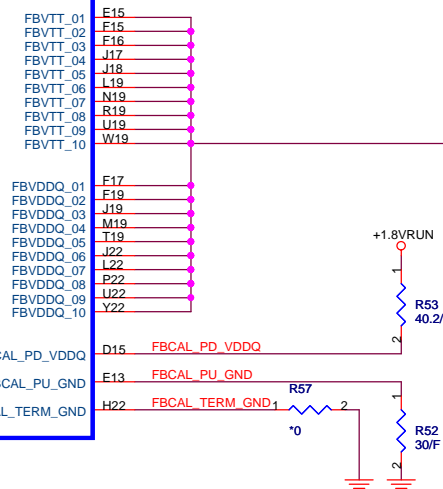
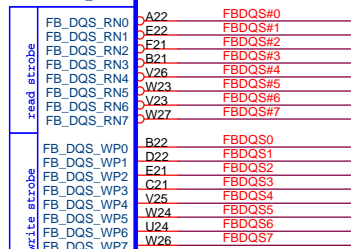
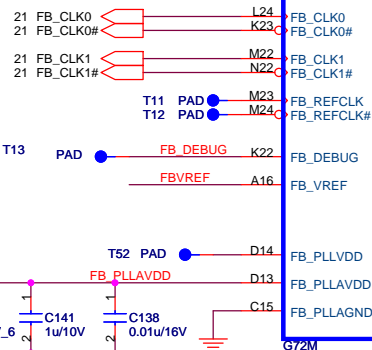




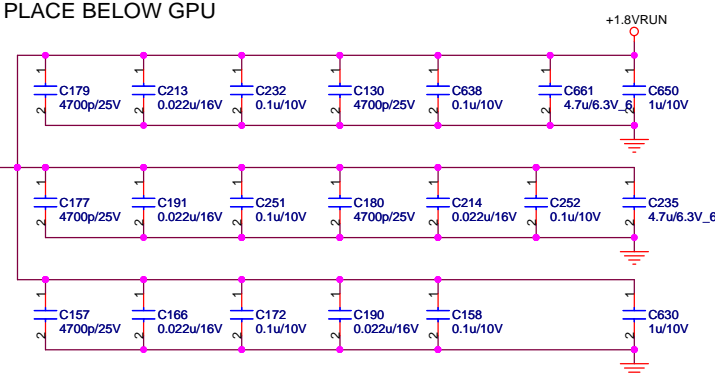




20


$$\begin{aligned}\text{FBVREF} &= \text{FBVDDQ} * \text{Rb} / (\text{Rt} + \text{Rb}). \\ \text{VREF} &= 0.5 * \text{FBVDDQ}. \\ \text{DDR: } 0.9\text{V} &= 1.8\text{V} * 1\text{K} / (1\text{K} + 1\text{K}).\end{aligned}$$


PLACE BELOW GPU

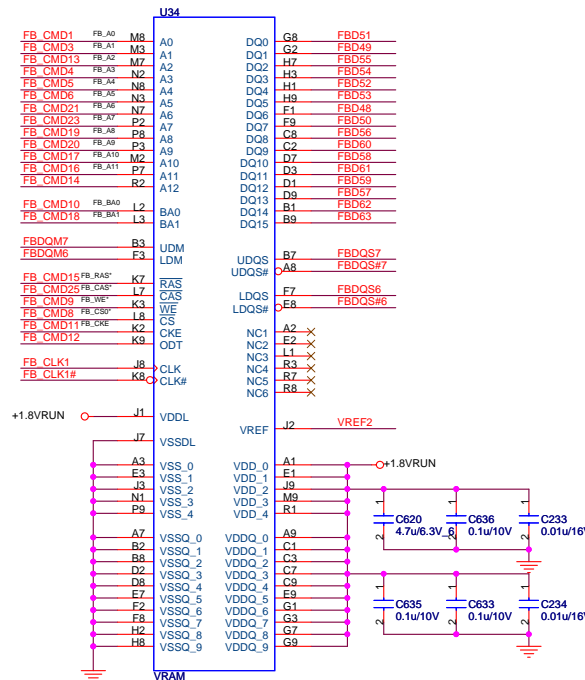
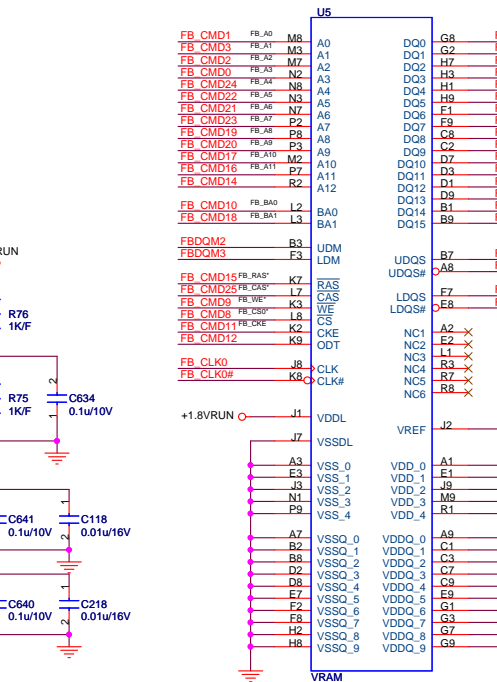
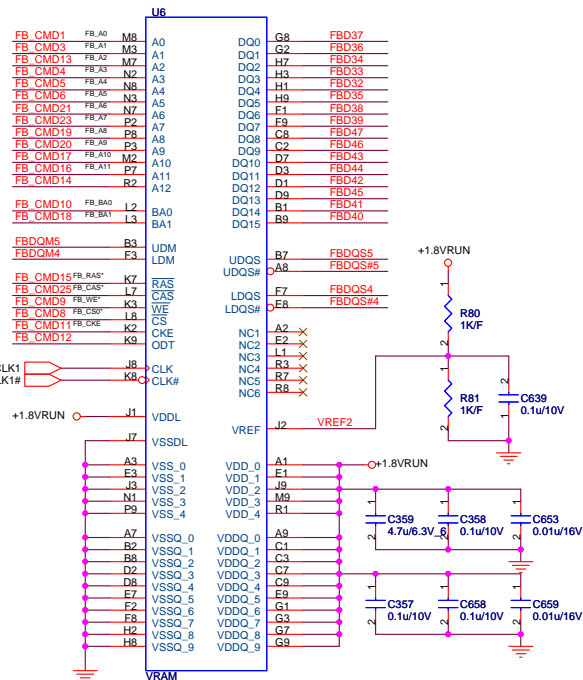
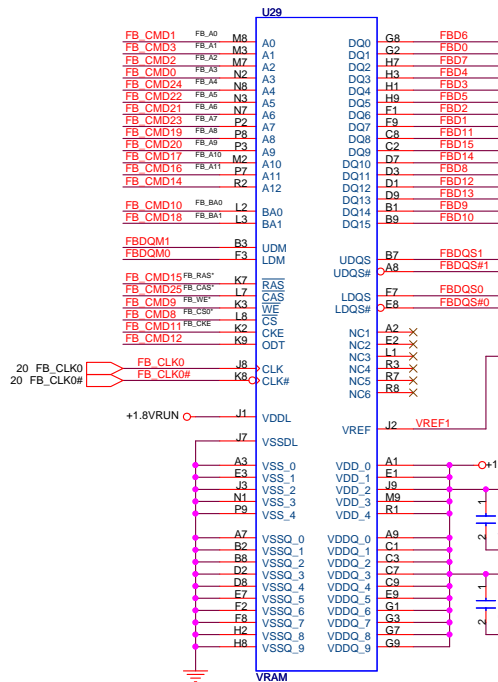
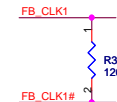
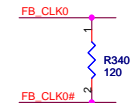
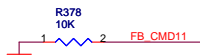
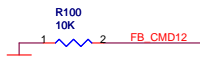


**PROJECT : TW3**  
**Quanta Computer Inc.**

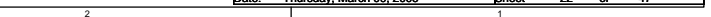
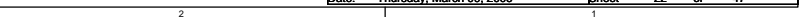
Size	Document Number <b>NV72M-3</b>	Rev B1A
Date:	Thursday, March 09, 2006	Sheet 20 of 47

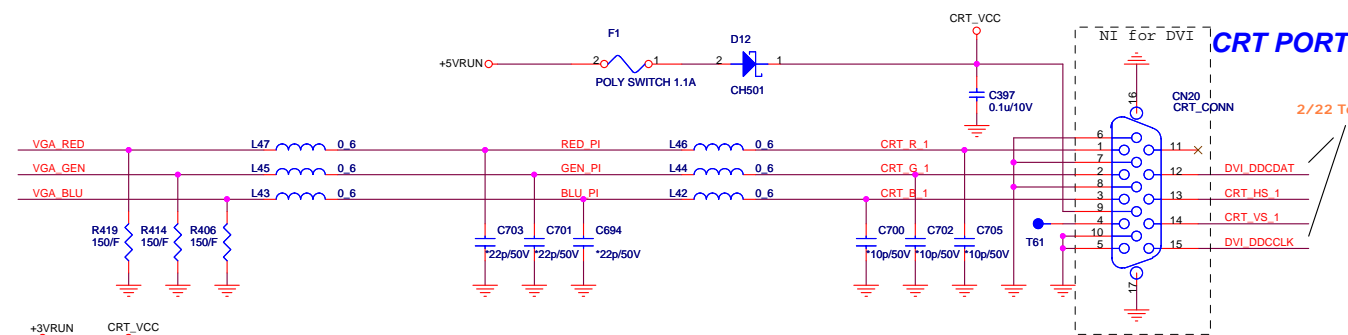


FB\_CMD[0..26] 20  
FBD[0..63] 20  
FBDQM[0..7] 20  
FBDQS[0..7] 20

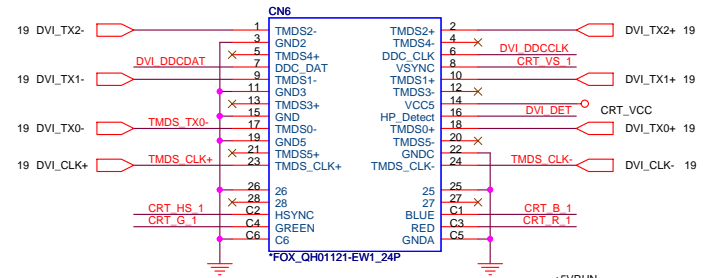


PROJECT : TW3  
Quanta Computer Inc.

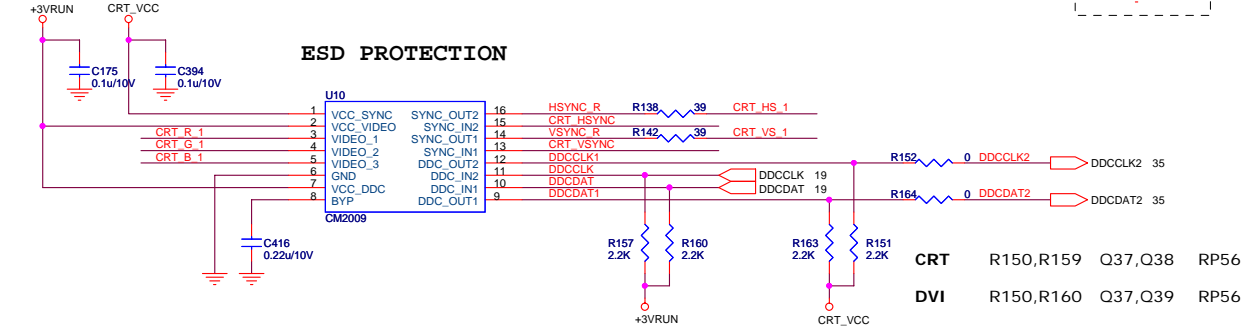




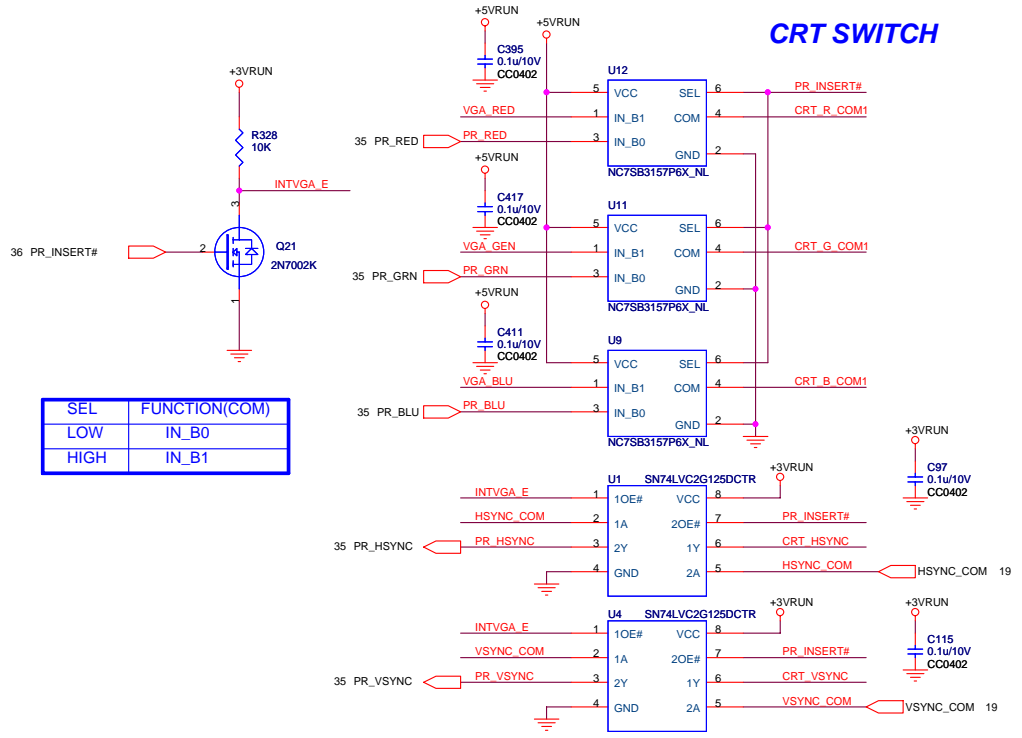
2/22 Tony Huang



### ESD PROTECTION

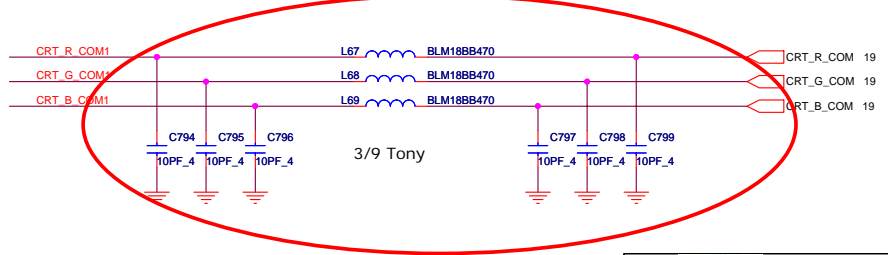
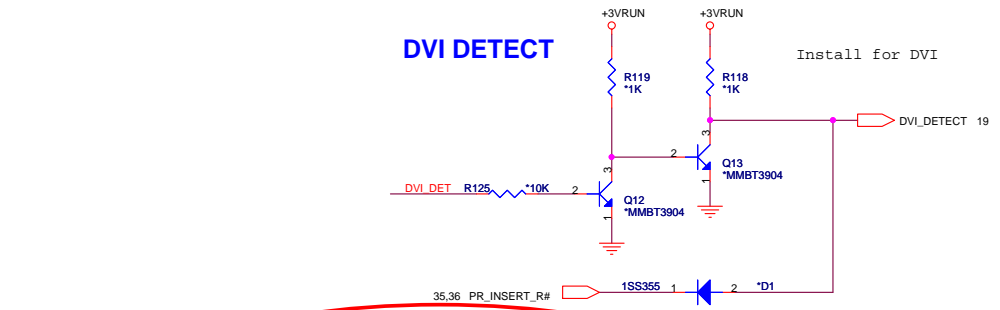


### CRT SWITCH



SEL	FUNCTION(COM)
LOW	IN_B0
HIGH	IN_B1

### DVI DETECT



3/9 Tony

C: 88E8053 LF PN: AJ080530010 (20050414)

1Mbps

C: Add 9 X GND Pad for LAN controller.  
(20050411)

C: Add these GND pin for via hole to GND Plane.

C: Add RC (R37 change to 200K, Add C101) delay to  
control LOM\_DISABLE#. (20050411)C: Reserve R36. Change  
LANRST# to PCIRST# source  
from MB option  
modify. (2005/04/11)

DELAY PIN10 AT LEAST 150ms

**CLOSE CHIP**

13 PCIE_RXP2	PCIE_RXP2	C350	0.1u/10V	PCIE_RXP2_R	49
13 PCIE_RXN2	PCIE_RXN2	C349	0.1u/10V	PCIE_RXN2_R	50
13 PCIE_TXP2	PCIE_TXP2			PCIE_TXP2	54
13 PCIE_TXN2	PCIE_TXN2			PCIE_TXN2	53
14,33 PCIE_WAKE#	PCIE_WAKE			PCIE_WAKE	6
3 CLK_PCIE_LAN	CLK_PCIE_LAN			CLK_PCIE_LAN	55
3 CLK_PCIE_LAN#	CLK_PCIE_LAN#			CLK_PCIE_LAN#	56
13,14,18,29,33,44	PLTRST#			PLTRST#	5
25 TX0P	TX0P			TX0P	17
25 TX0N	TX0N			TX0N	18
25 TX1P	TX1P			TX1P	20
25 TX1N	TX1N			TX1N	21
25 TX2P	TX2P			TX2P	26
25 TX2N	TX2N			TX2N	27
25 TX3P	TX3P			TX3P	30
25 TX3N	TX3N			TX3N	31

88E8038/88E8055

T58 PAD LAN\_SMB\_CLK  
T59 PAD LAN\_SMB\_DATA

LANVCC L38 HI0805R800R-10  
120 ohms@100Mhz

C253 22u/10V\_8 C646 4.7u/10V\_8 C221 0.1u/10V R77 4.7K

C: Widen to 20 mils. AVDD25 to  
20 mils. (20050411)

Q9 2SA1797T100Q AVDD25  
C642 4.7u/10V\_8 C215 0.1u/10V

PLACEMENT CLOSE TO EACH OTHER

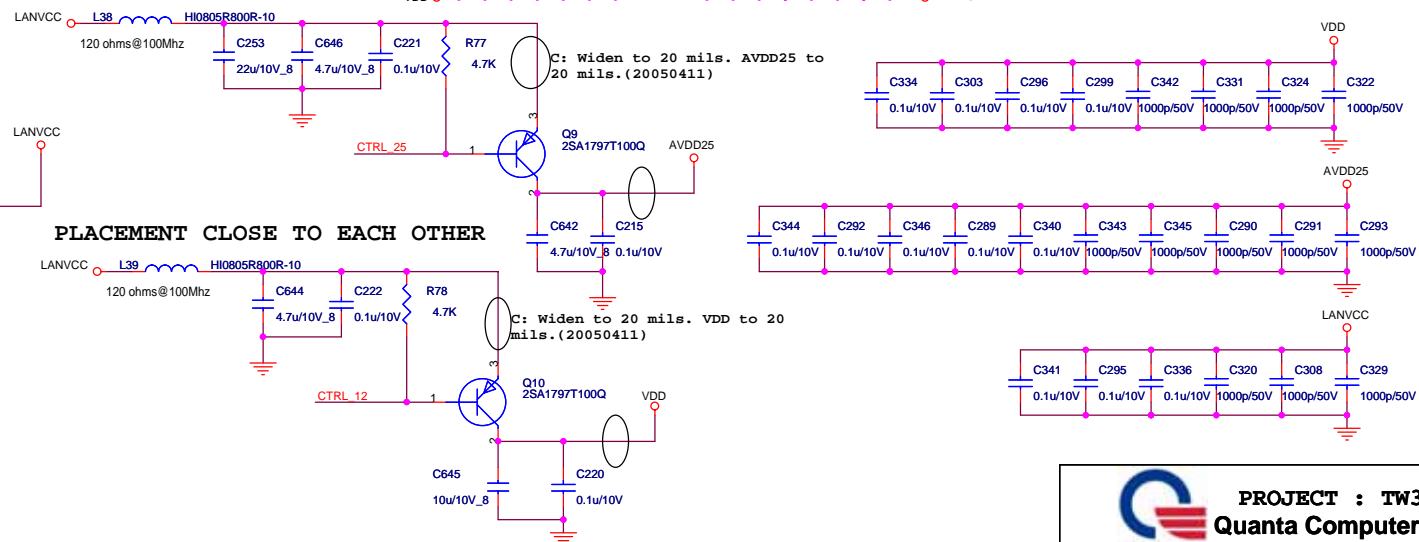
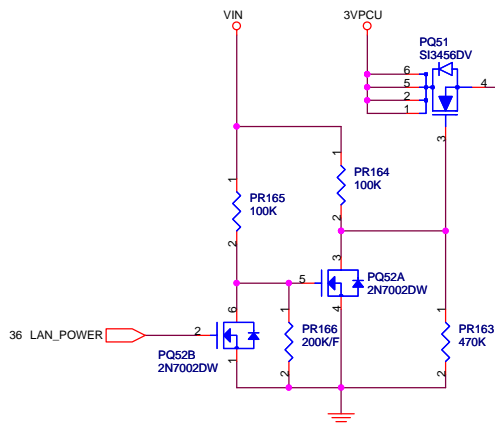
LANVCC L39 HI0805R800R-10  
120 ohms@100Mhz

C644 4.7u/10V\_8 C222 0.1u/10V R78 4.7K

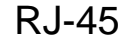
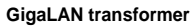
C: Widen to 20 mils. VDD to 20  
mils. (20050411)

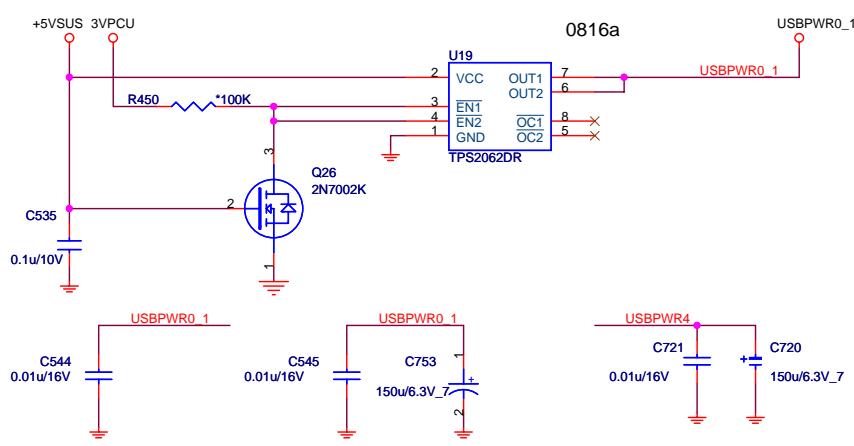
Q10 2SA1797T100Q VDD  
C645 10u/10V\_8 C220 0.1u/10V

LANVCC

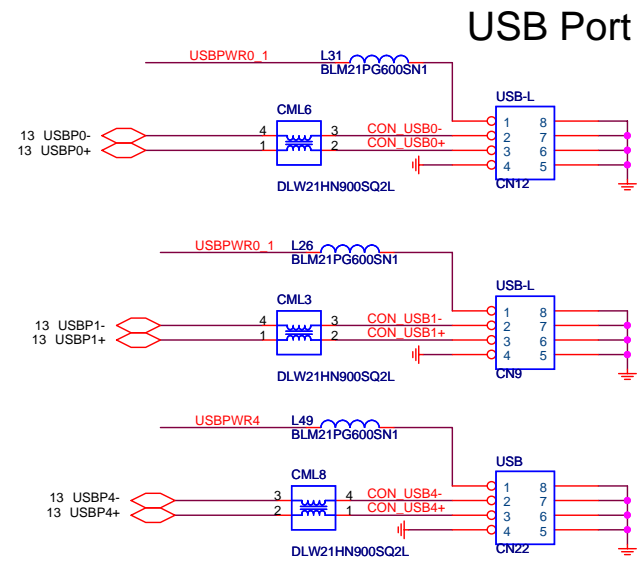
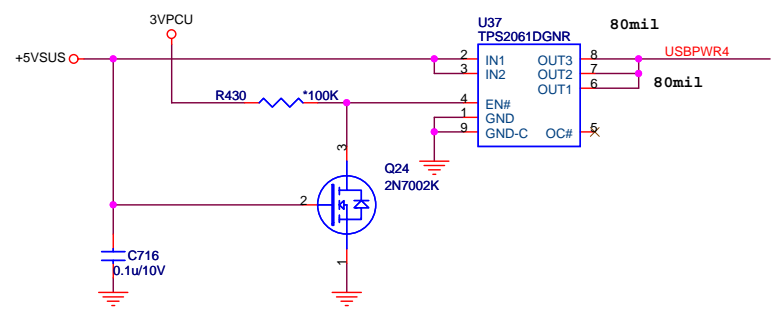


0804 REDUCING THE LANVCC NOISE





C:Change U1 from G528 to TPS2061

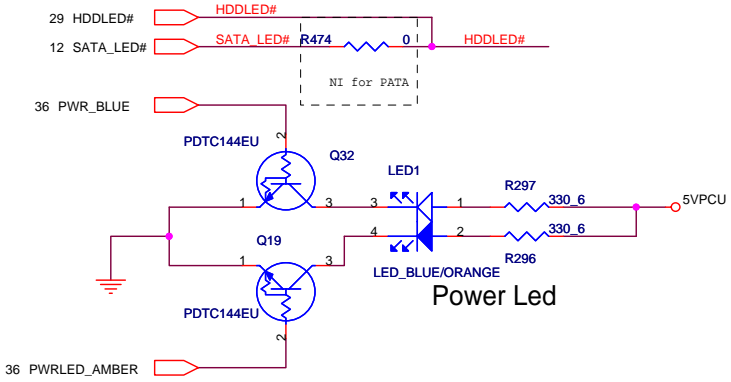


Left

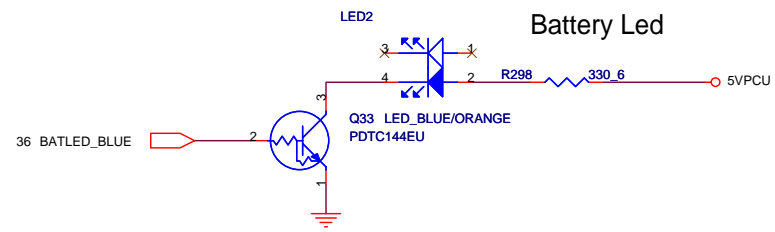
Right

For Bottom Board

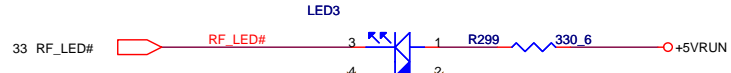
## HDD,SATA Led



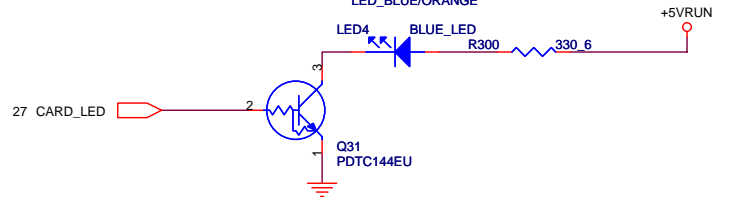
## Battery Led



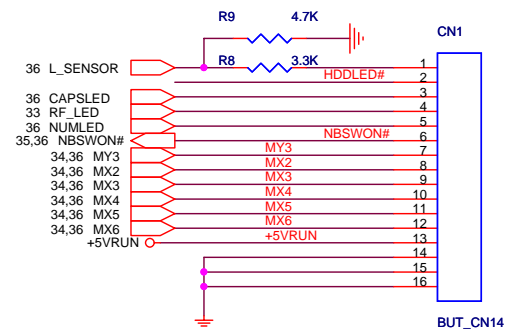
## Wireless Led



## Card reader Led



## Power Led

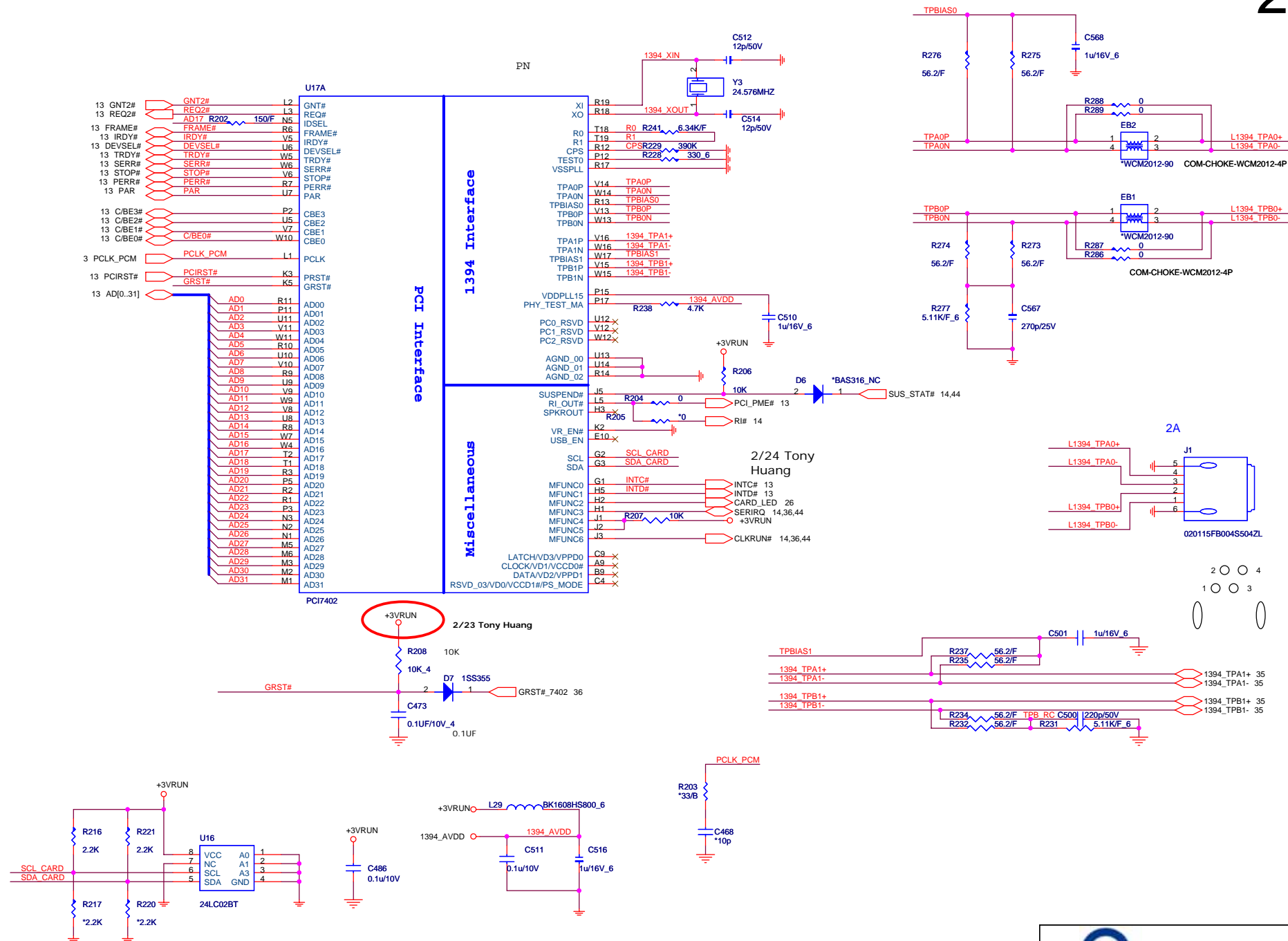


**PROJECT : TW3**

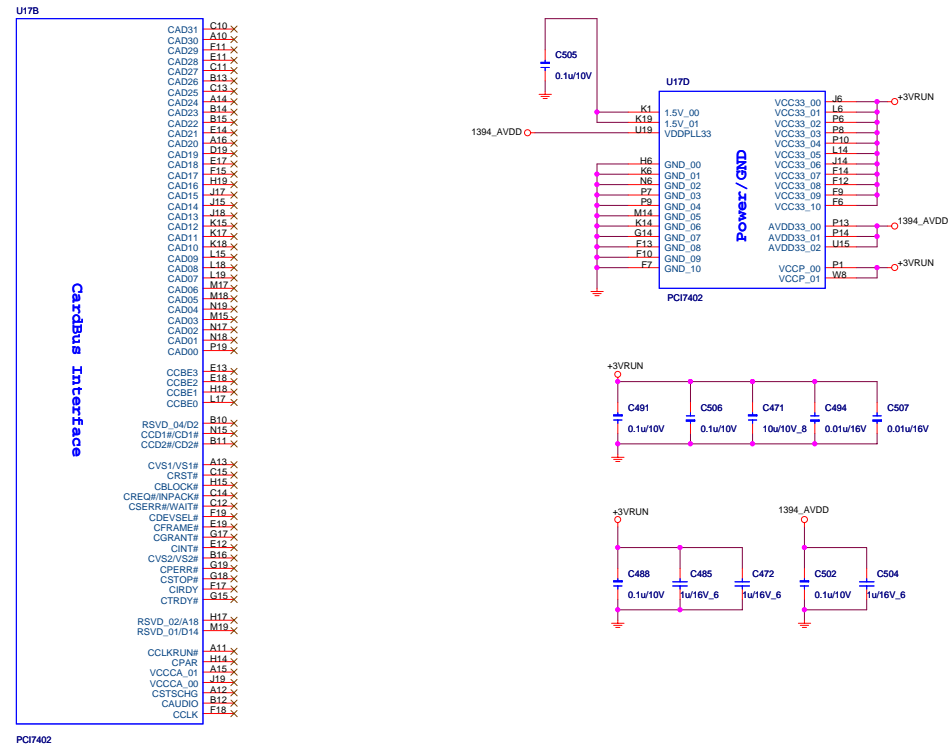
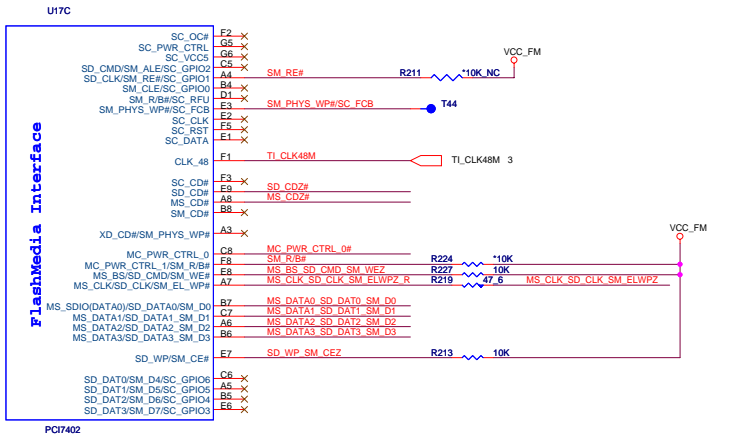
**Quanta Computer Inc.**

Size	Document Number	Rev
	USB,LED,Bottom/B	B1A
Date:	Thursday, March 09, 2006	Sheet 26 of 47

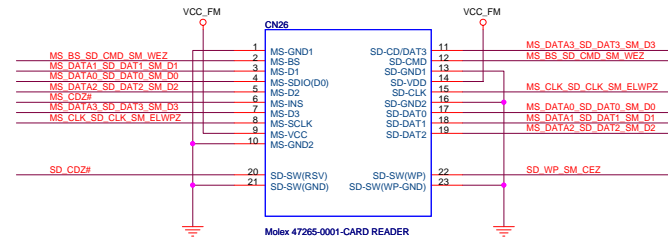
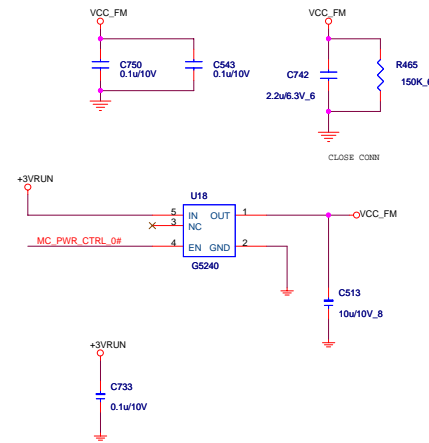




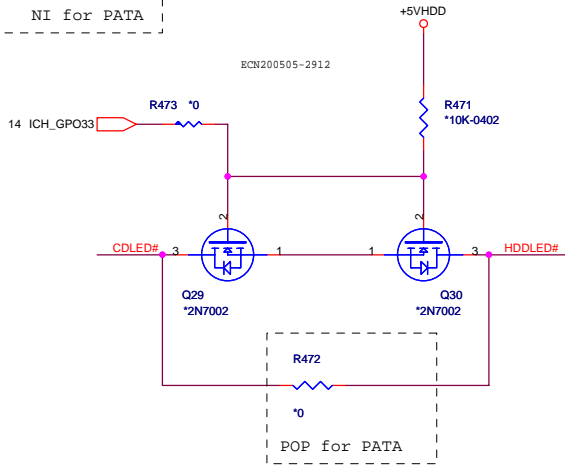
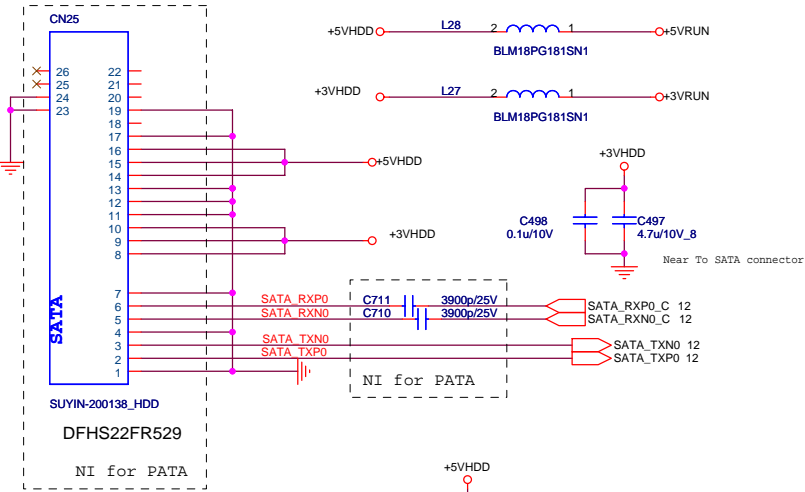
DO NOT INSERT SD/MMC, MEMORYSTICK AND XD SIMULTANEOUSLY.



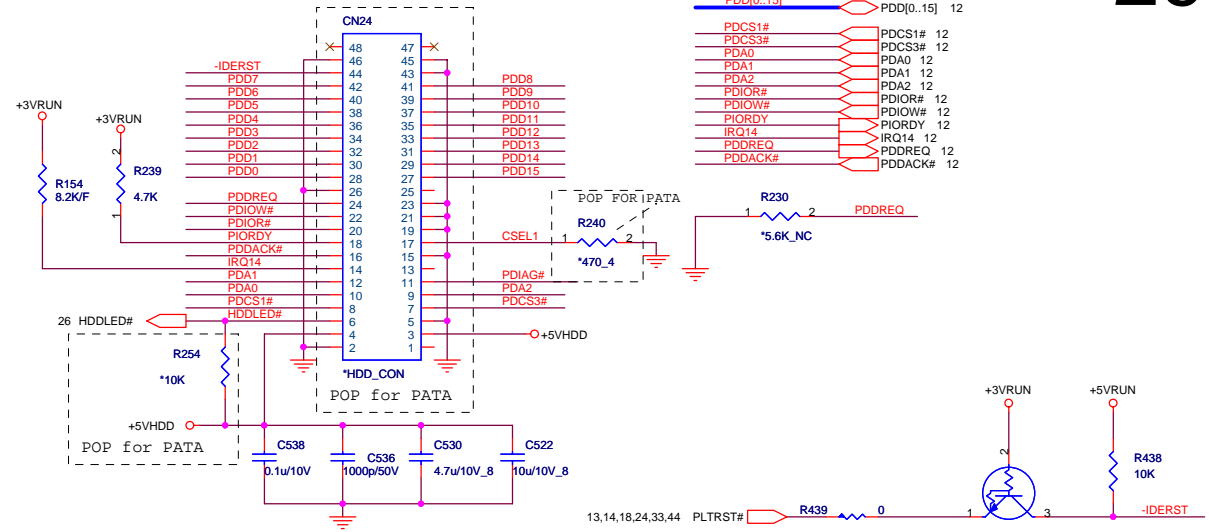
## 3 IN1 CARD READER (push-push)

Supporting MMC/SD/MS Cards  
Molex P/N:DPHD23MS0B6

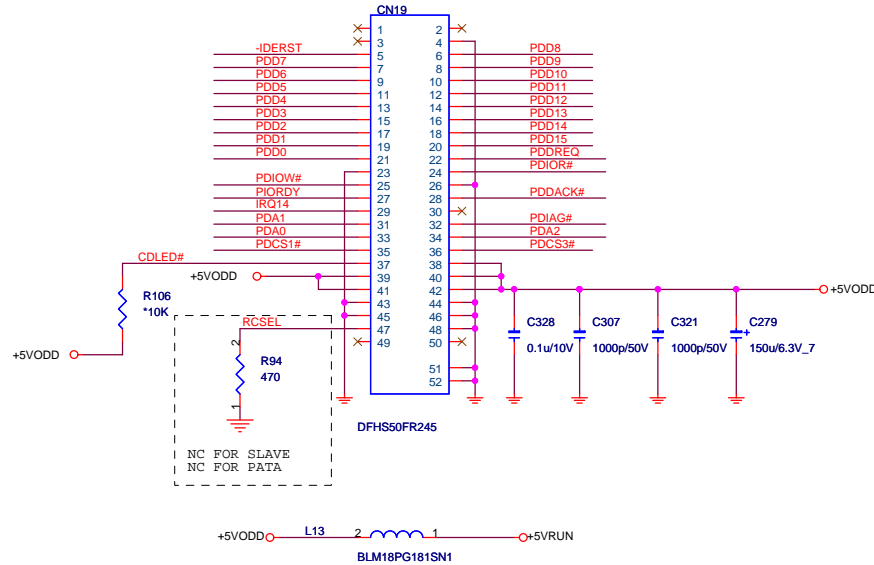
# SATA HDD



# PATA HDD

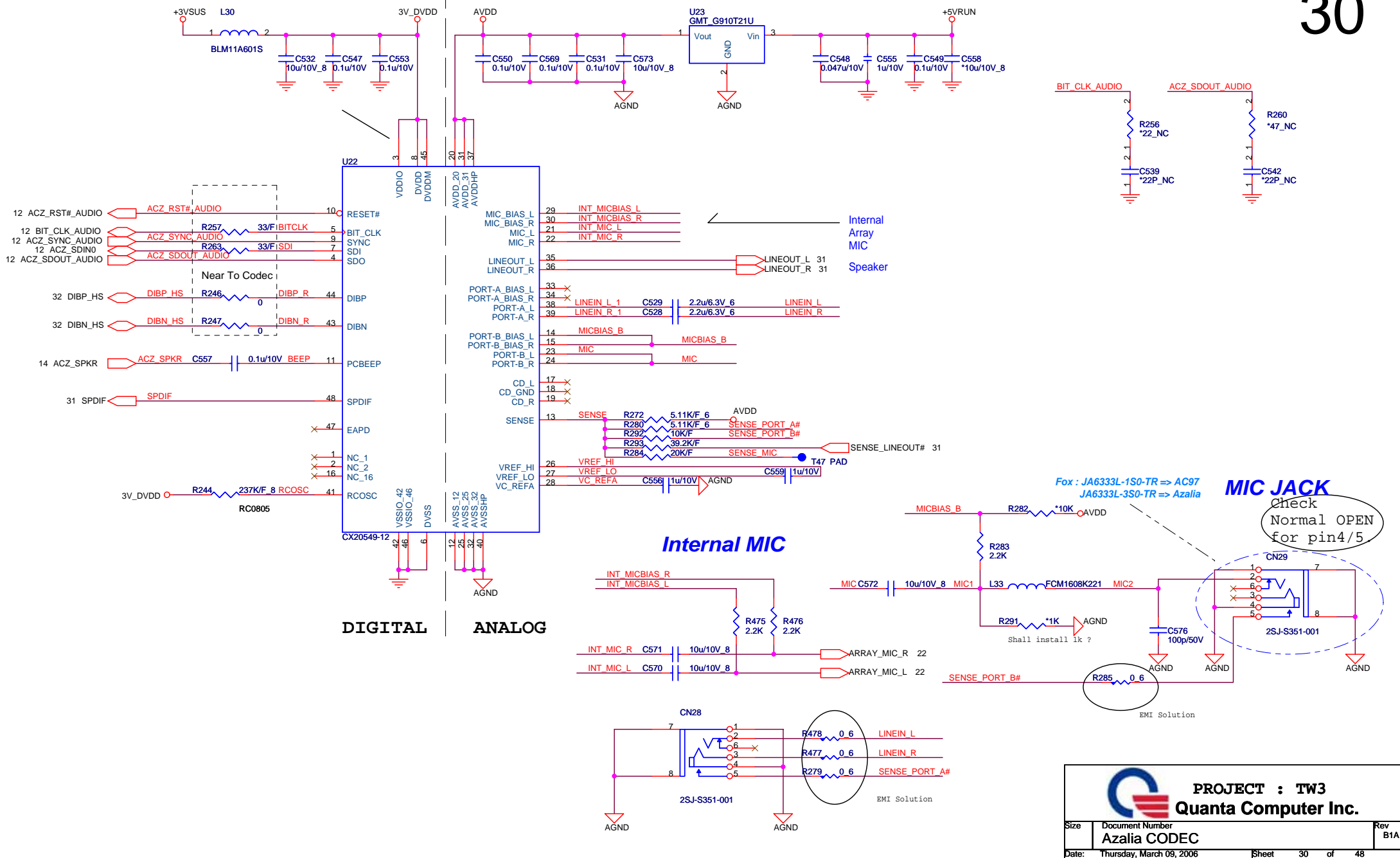


# ODD

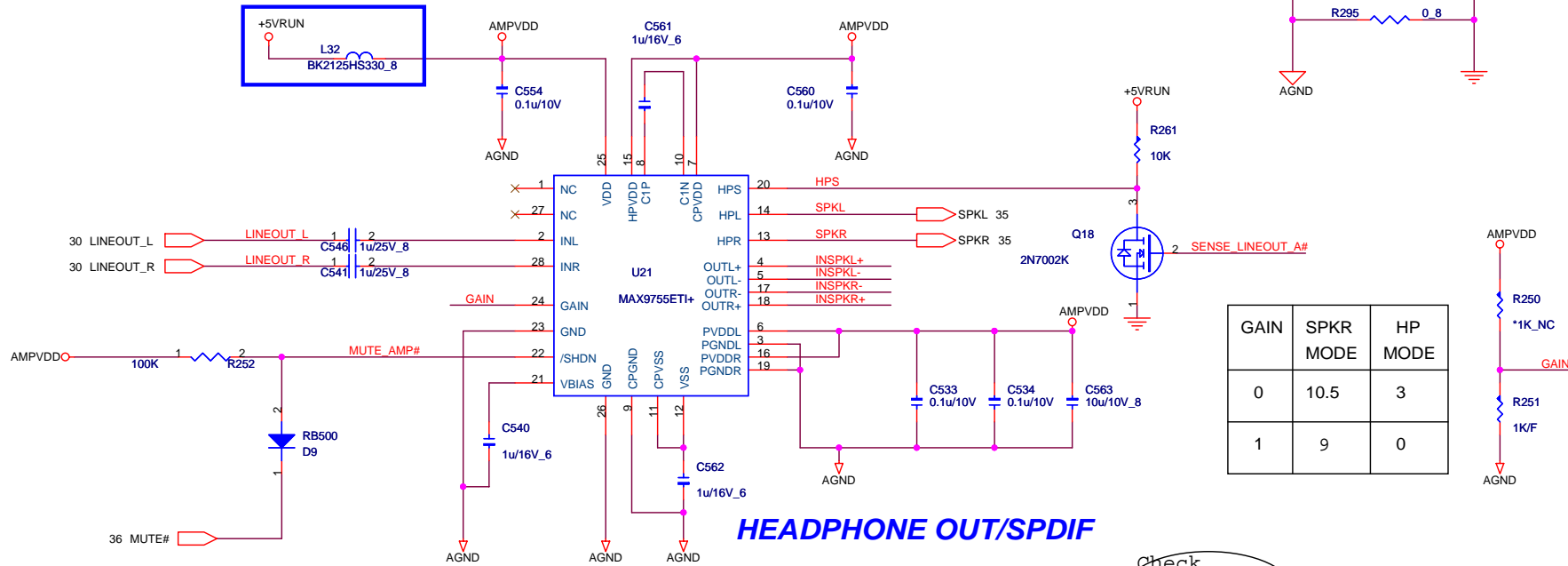
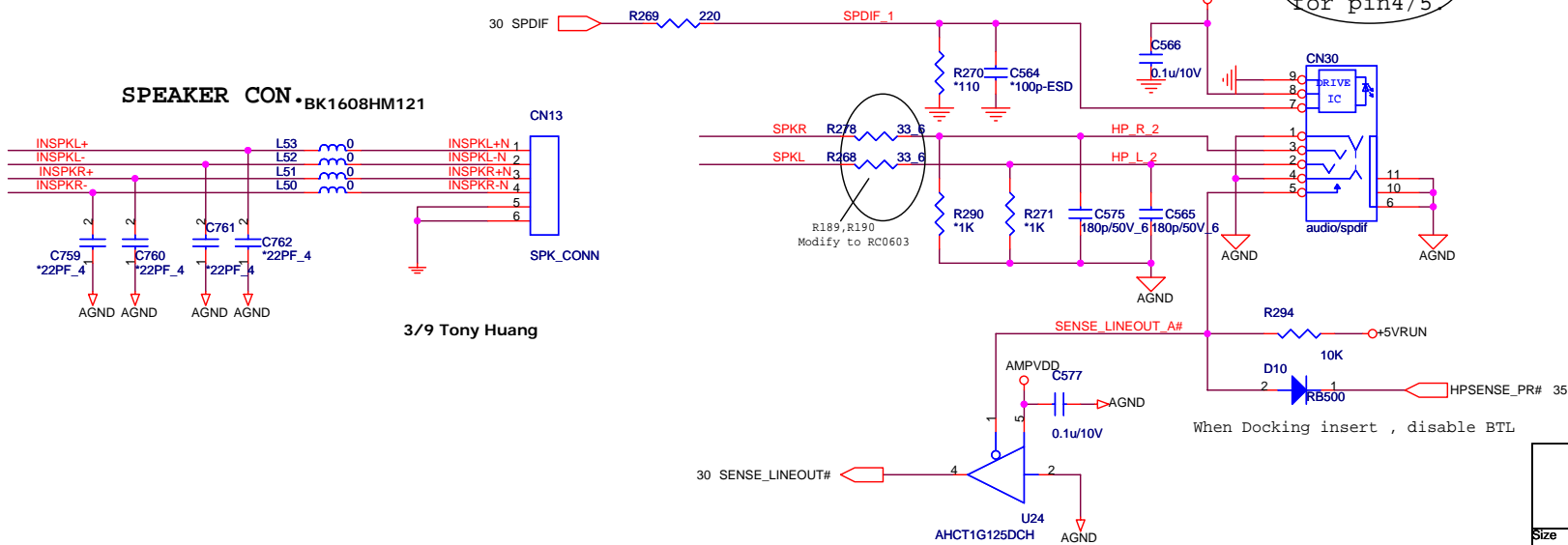


FOR PATA HDD

CN19	NI
C730	NI
C729	NI
CN18	HDD CON
R517	NI
Q25	2N7002
Q26	2N7002
R513	10K
R512	0
R168	470



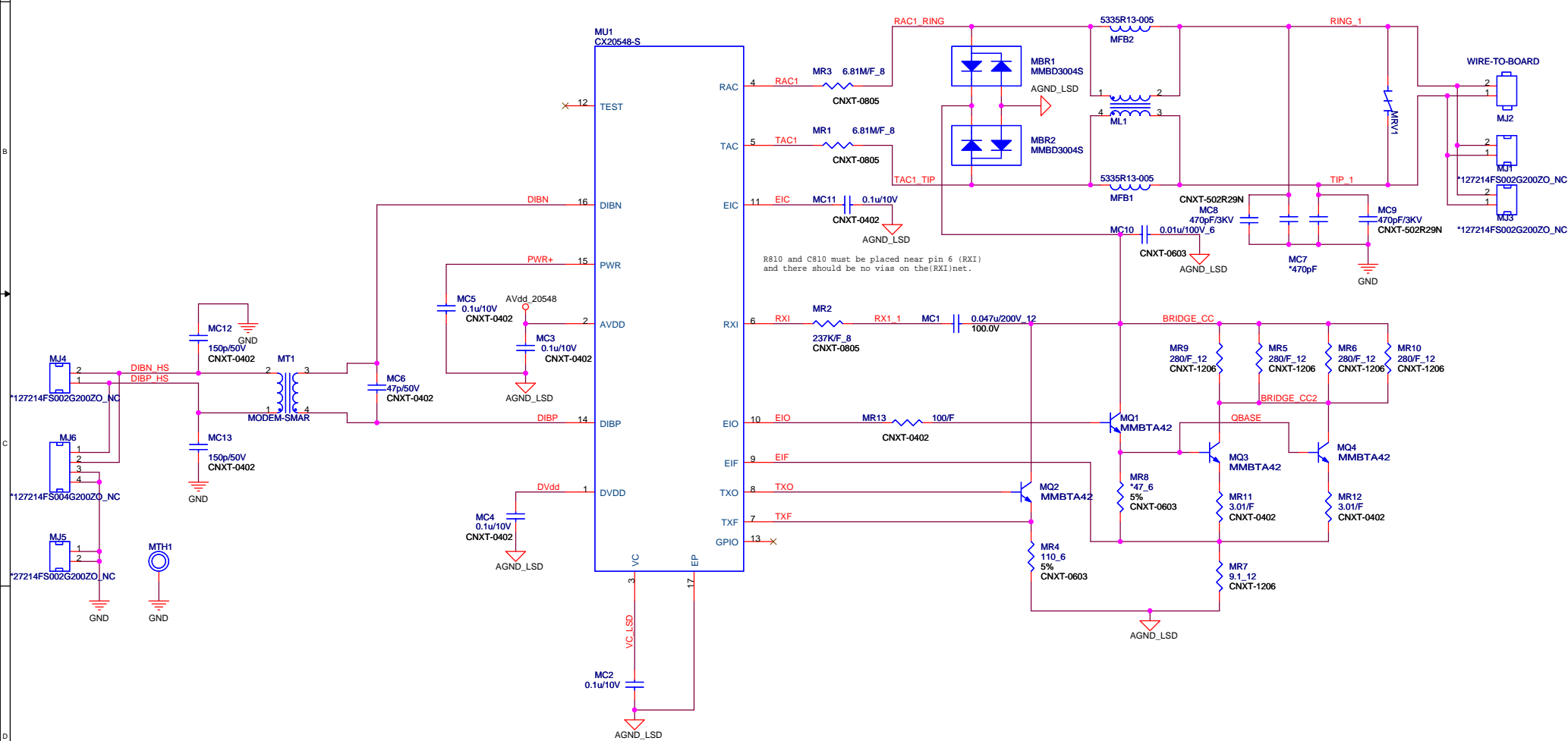
0816a

**HEADPHONE OUT/SPDIF**

Revision History		
REV	Description	Date
0	Initial Release	April 26, 2005

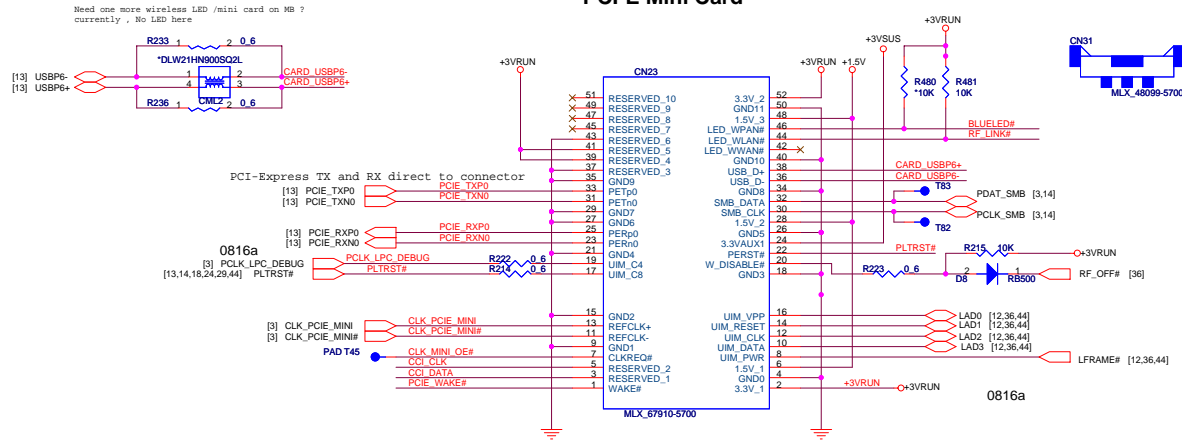
30 DIBN\_HS  
30 DIBP\_HS

DIBN\_HS  
DIBP\_HS

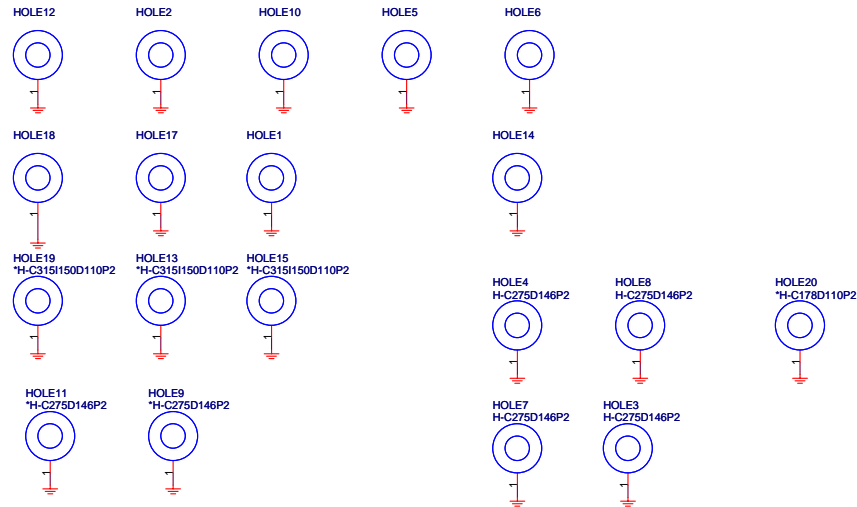
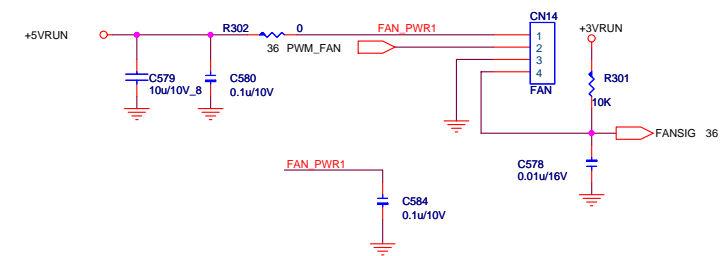
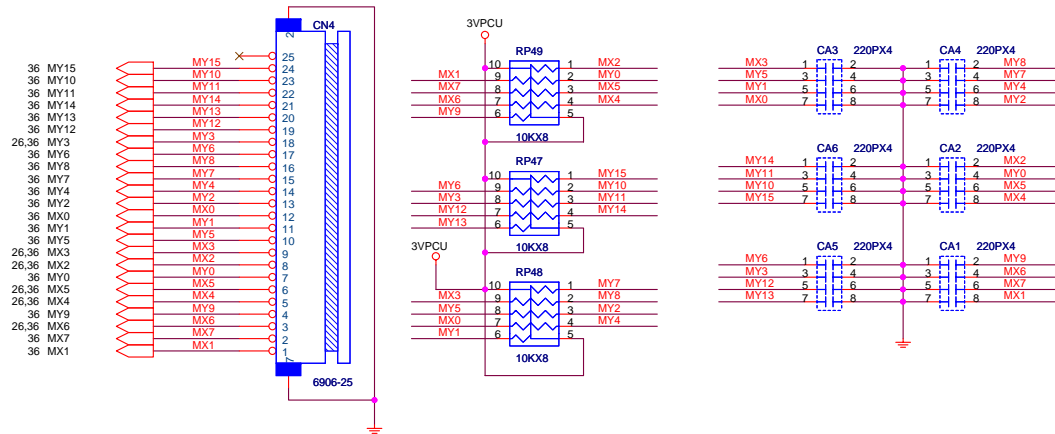




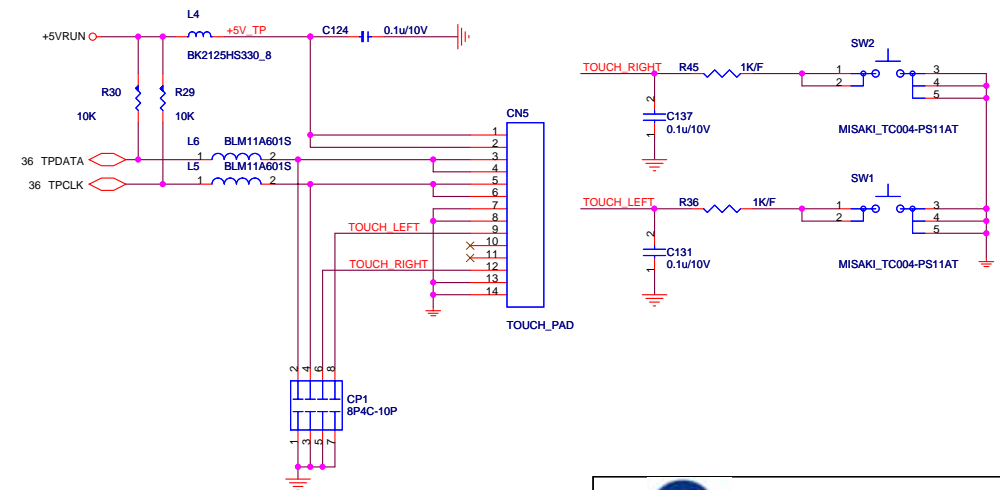
## PCI-E Mini Card



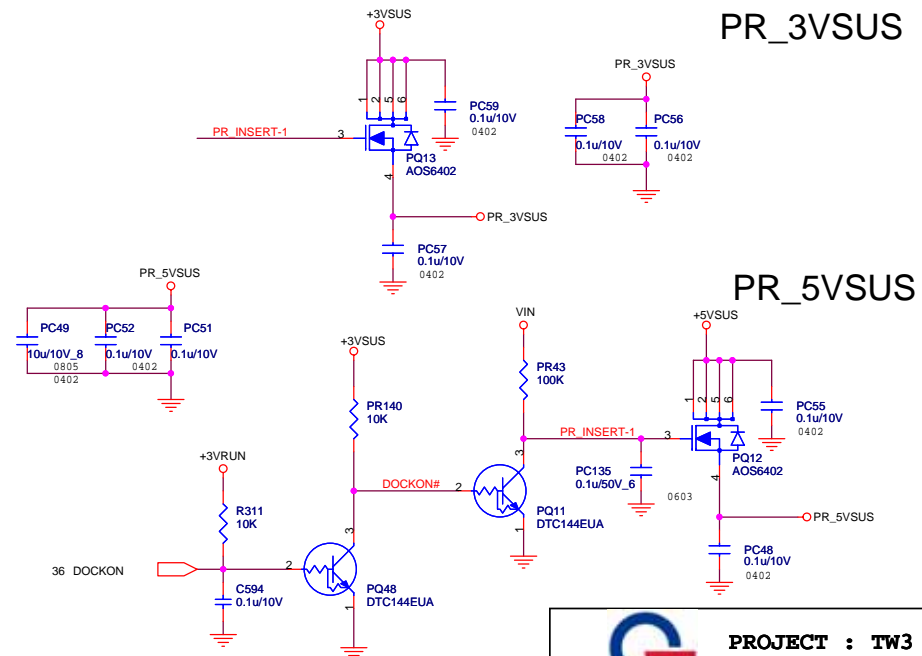
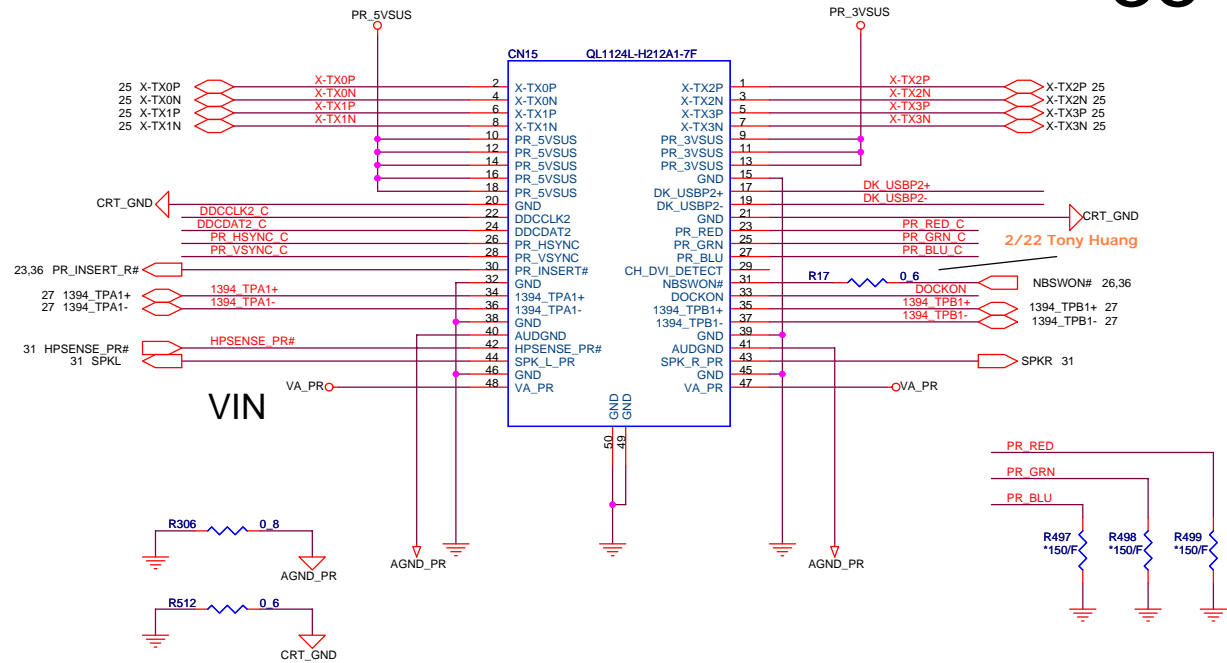
## KeyBoard Interface




## TOUCH PAD

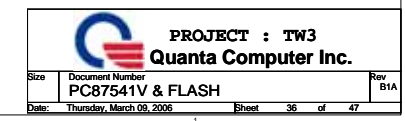


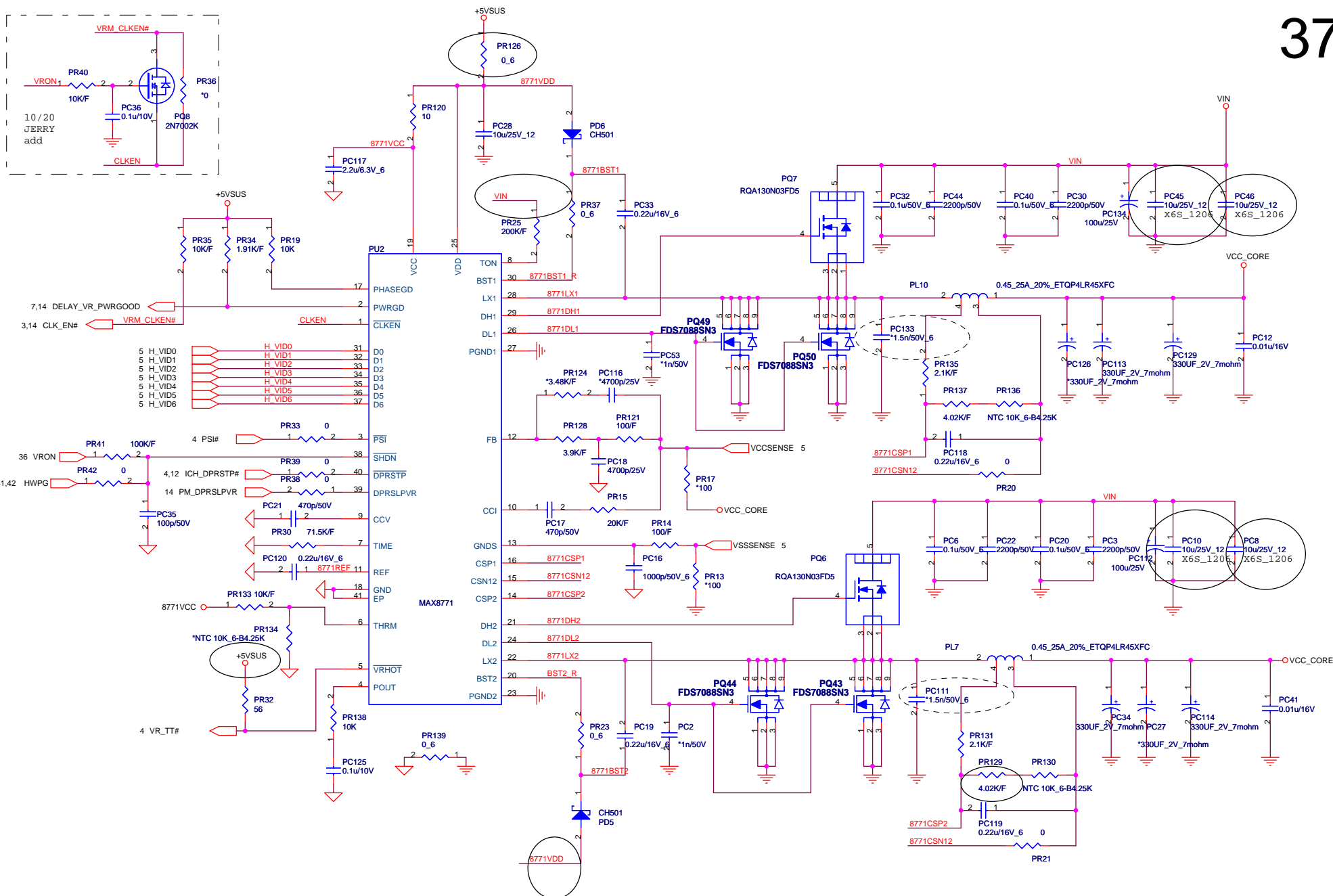
## 35

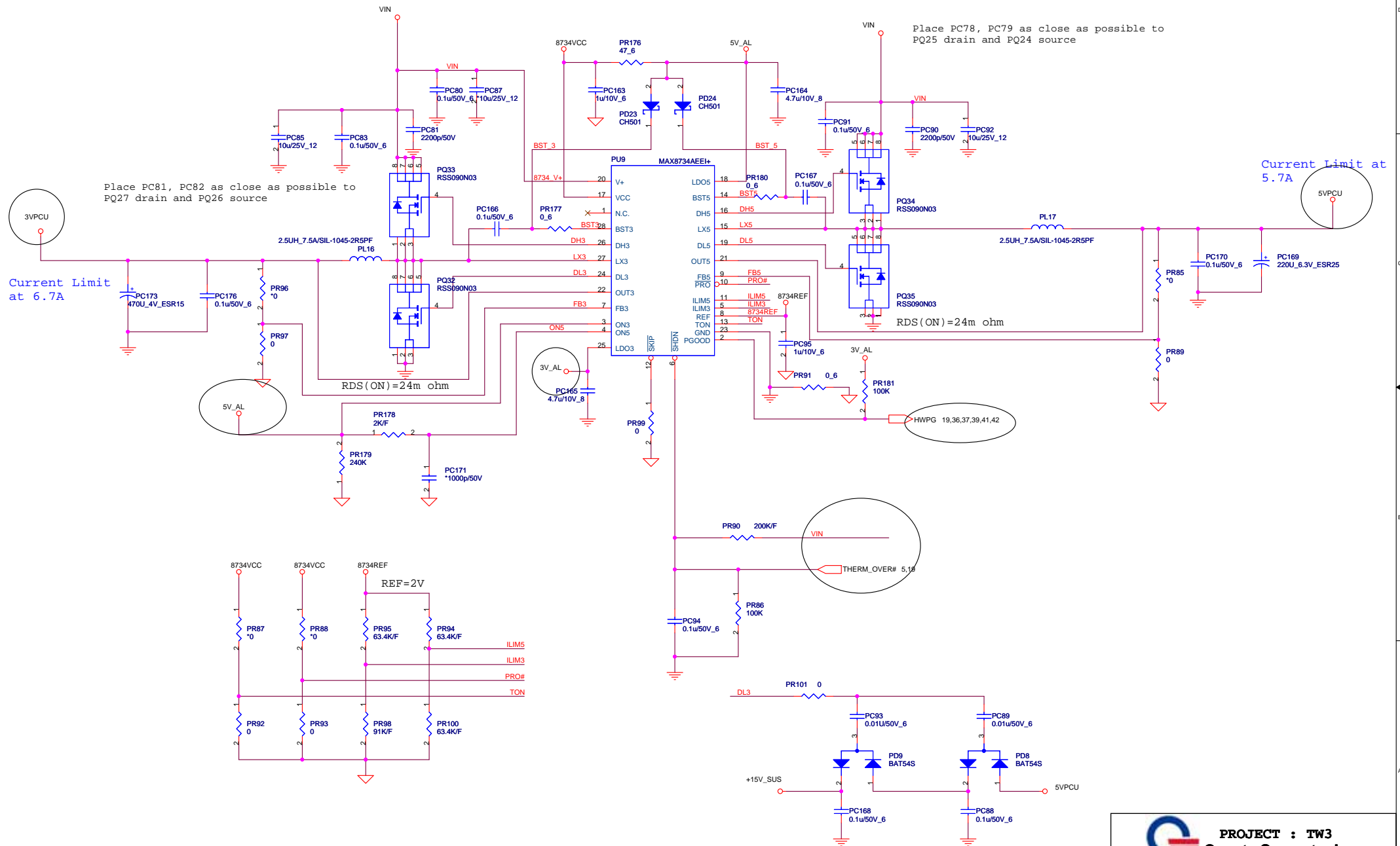


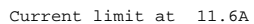
PR\_5VSUS

 <div style="display: inline-block; vertical-align: middle; margin-left: 10px;"> <b>PROJECT : TW3</b>  <b>Quanta Computer Inc.</b> </div>		
Size	Document Number <b>PORT REPLICATOR</b>	Rev <b>B1A</b>
Date: <b>Thursday, March 09, 2006</b>	Sheet <b>35</b> of <b>47</b>	



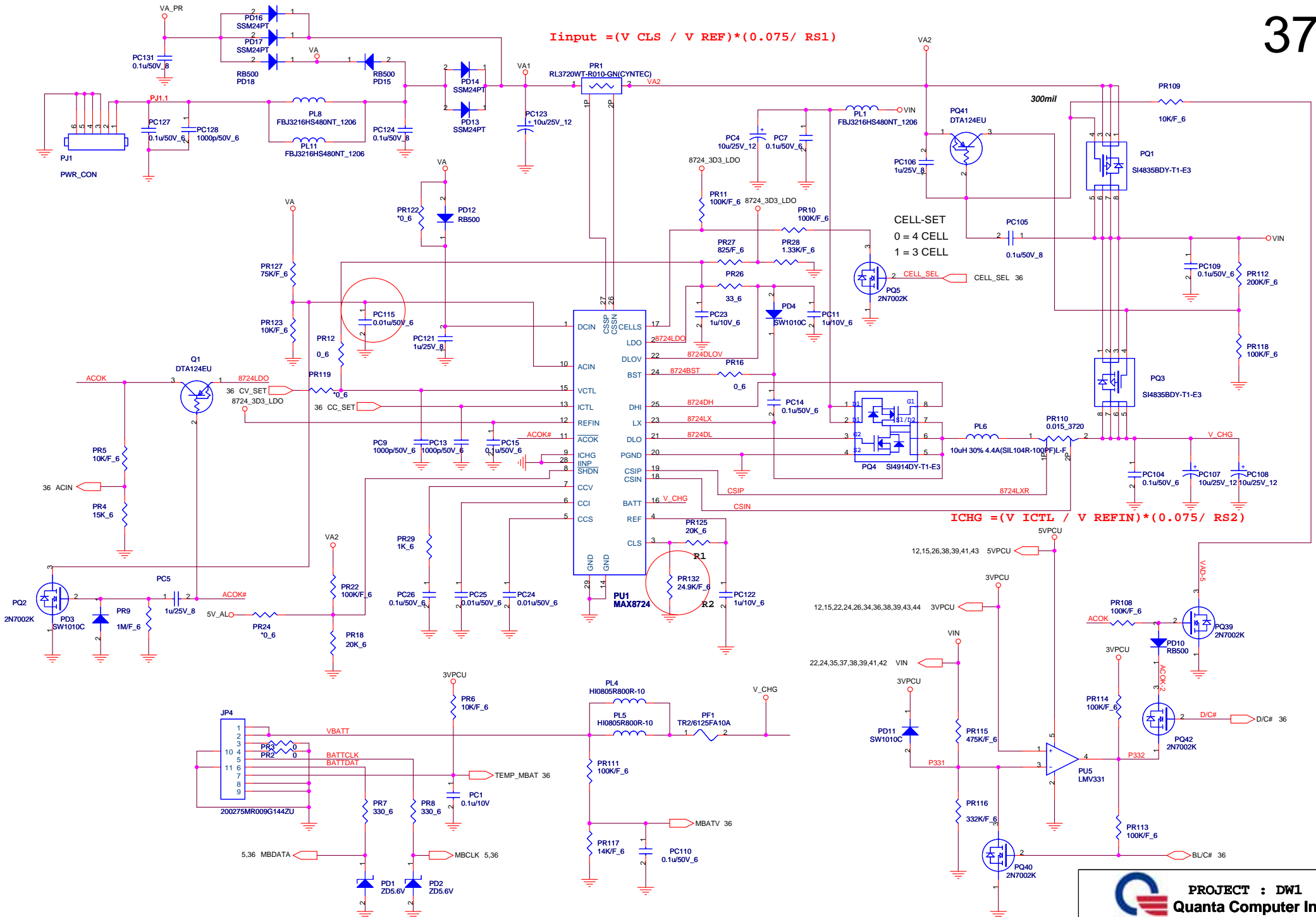




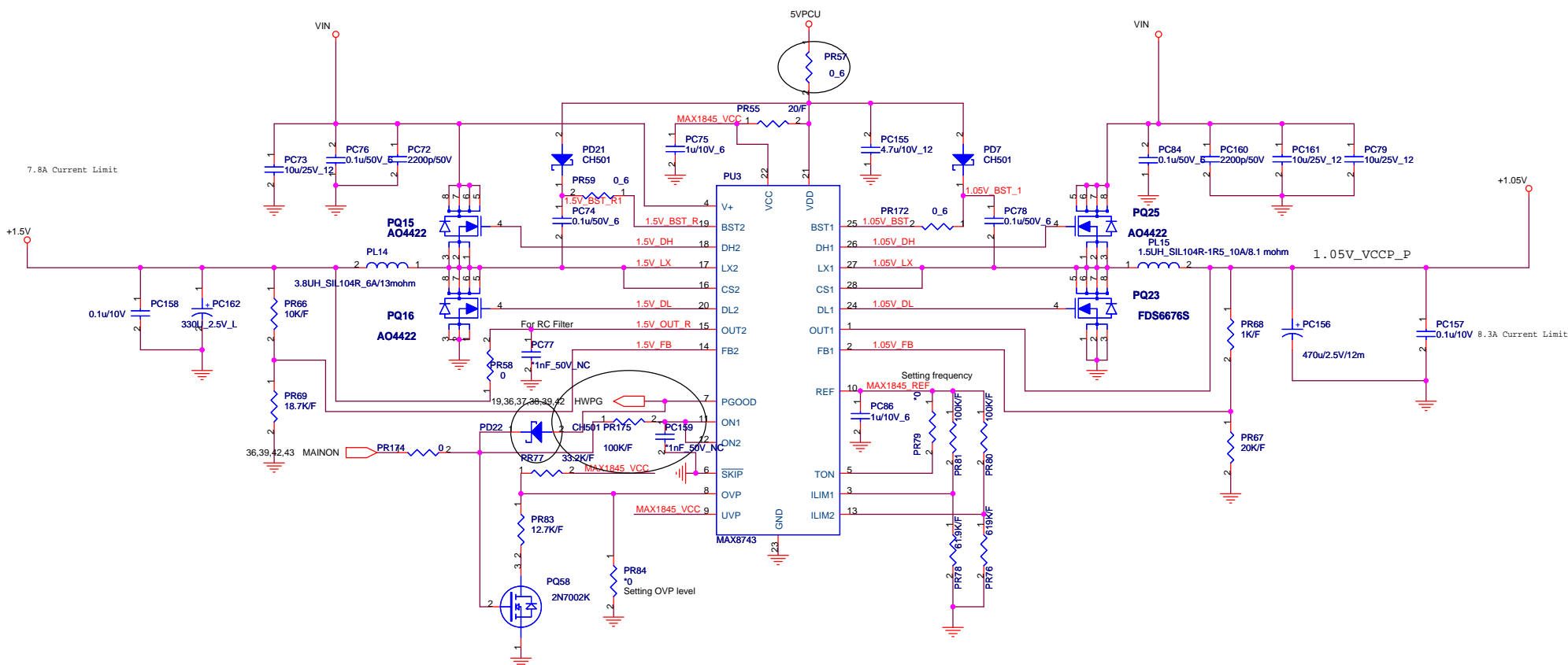


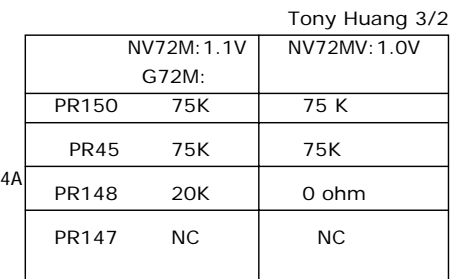
0.9 Volt +/-5%  
Design current 1.05A  
Peak current 1.5A



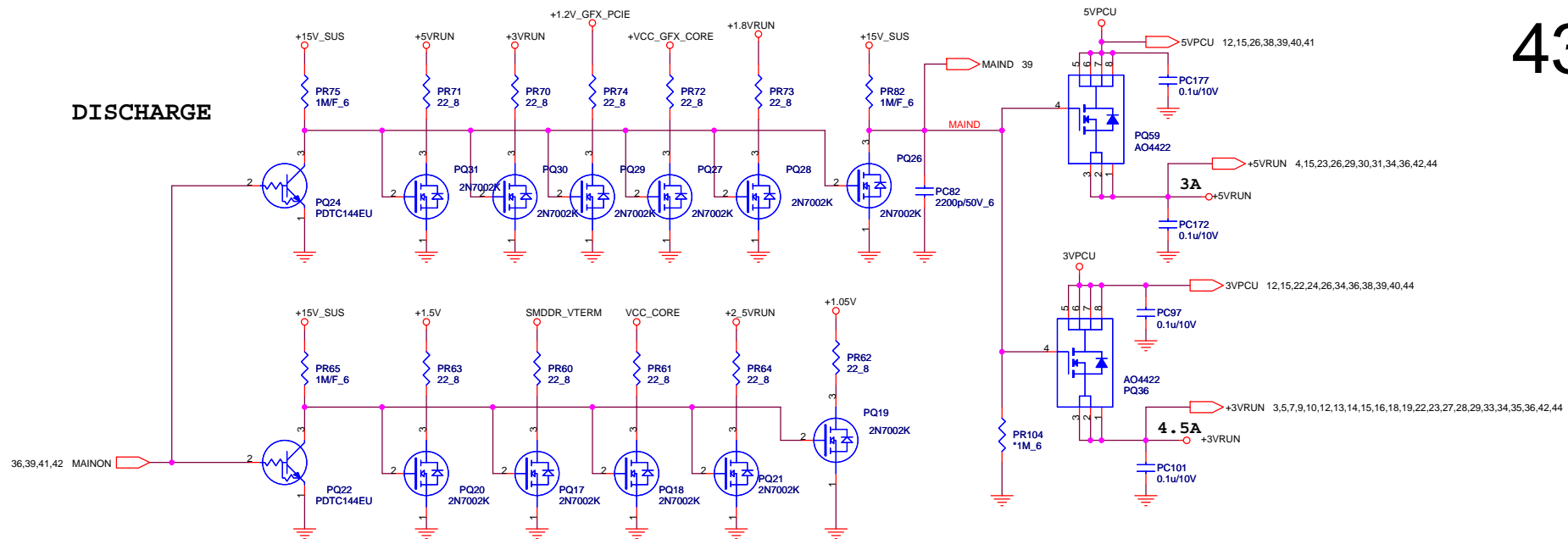


AO4422: Id= 11A, Rdson= 24m ohm, Qg= 19.8nC  
FDS6676S: Id= 14.5A, Rdson= 7.25m ohm, Qg= 43 nC





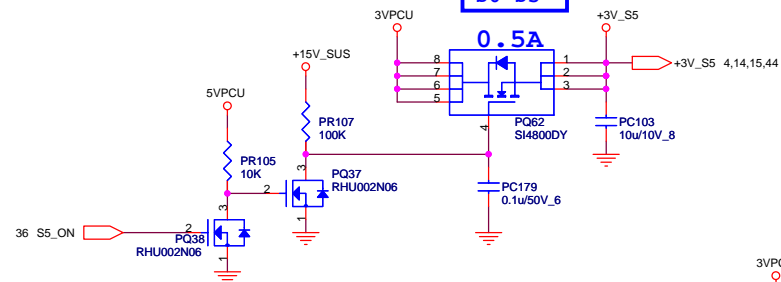
## DISCHARGE



200mils

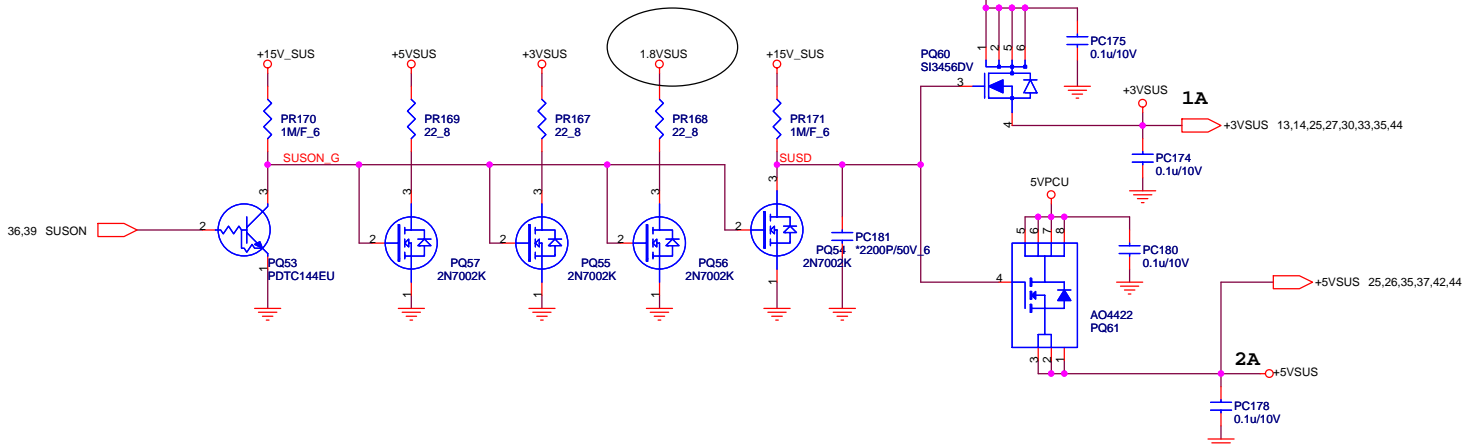
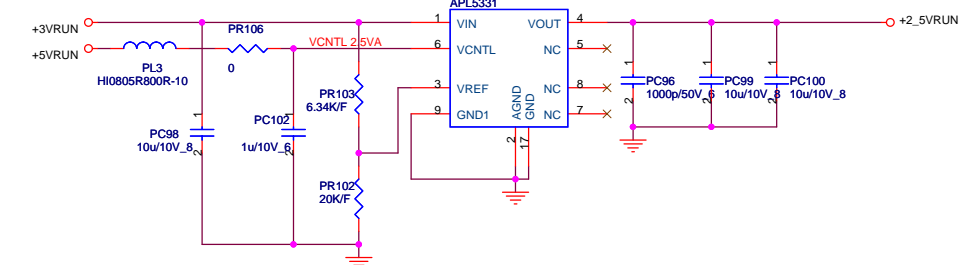
S0-S5

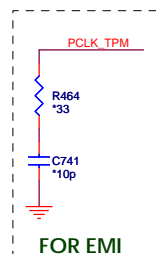
0.5A



+2\_5VRUN

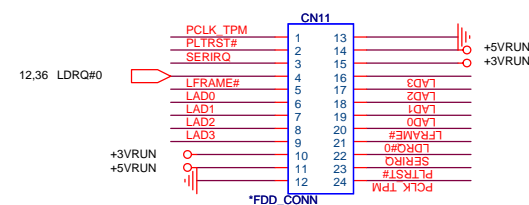
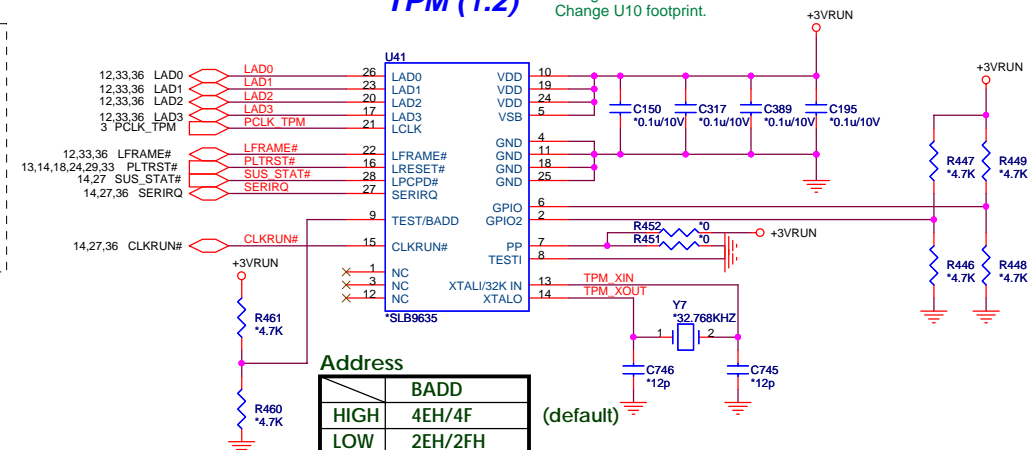
2.5V/ 1A






## TPM (1.2)

B stage:  
Change U10 footprint.



MODEL	REV	CHANGE LIST		Model	TW3 M/B	
				Page	From	To
TW3A	B to 1223  					

MODEL	REV	CHANGE LIST		Model	TW3 M/B	
				Page	From	To
TW3A	1230 to 0102	Page 38	PC173 change to 470uF.	1	1A	
		Page 39	PC66 change to install.	2	1A	
		Page 42	PR153 change to 20K.	3	1A	
		Page 41	PD7,PD21,PD22 change to CH501.	4	1A	
		Page 37	PD6,PD5 change to CH501.	5	1A	
		Page 42	PQ47 change to RQW180N03.	6	1A	
		Page 26	CN12,CN9 USB connector change to DIP type.	7	1A	
		Page 29	CN25 pin25,26 and CN24 pin47,48 disconnect to GND.	8	1A	
		Page 23	CN6 pin27,28 disconnect to GND.	9	1A	
		Page 34	SW1,SW2 P/N change to DHP00FC1G16.	10	1A	
		Page 36	Change R454 to 100K,R508,R509 to 10K.	11	1A	
	0102 to 0103	Page 4	R101,R97,Q11 change to install.	12	1A	
		Page 6,7,8,9,10,11	Change U32 P/N to AJSL8Z40T26.(945PM)	13	1A	
		Page 12,13,14,15	Change U36 P/N to AJSL8YB0T12.(ICH7M)	14	1A	
		Page 37	PR128 change to 3.9K.	15	1A	
				16	1A	
				17	1A	
	0103 to 0105	Page 45,46	Update change list.	18	1A	
		Page 27	Change J1 P/N to DFHS04FRE47.	19	1A	
		Page 35	Change CN15 to install and P/N to DFHS48FR001	20	1A	
		Page 44	Change B1,B2,B4 P/N to FDTW3002018.	21	1A	
		Page 36	U38 P/N change to AKE35ZAKK17.	22	1A	
		Page 42	PR45,PR150 P/N change to CS37502FB12.	23	1A	
	0105 to 0111	Page 30	Change C528,C529 to 2.2uF/6.3V for audio precision.	24	1A	
				25	1A	
				26	1A	
				27	1A	
				28	1A	
				29	1A	
C1 TO C2	0111 to 0119	Page 19	Change R26 to 0 ohm and change connection to THERM_OVER#.	30	1A	
		Page 23	Q21 mirror vertical.	31	1A	
		Page 23	Add C794~C799, L67~L69 for EMI.	32	1A	
		Page 23	L46,L44,L42 change to 0 ohm. C700,C702,C705 change to NI for EMI.	33	1A	
		Page 32	Change MR5,MR6,MR,MR10 to 280ohm. Add MR11,MR12,MR13. Change MR8 to NI.	34	1A	
		Page 35	R17 change to install.	35	1A	
		Page 35	CN15.21,22 change to CRT_GND. Add R512 for EMI.	36	1A	
		Page 35	Change D1 to page23 and its connection and to NI.	37	1A	
		Page 41	PL14 P/N change to DC-38600001.	38	1A	
		Page 43	PQ59,PQ61,PQ36 P/N change to BAM44220002.	39	1A	
		Page 36	RN2 P/N change to CJ247084N25.	40	1A	
		Page 26	LED4 P/N change to BEBL0002Z62. LED1~3 P/N change to BEAB0013ZA1.	41	1A	
		Page 33	CN10 P/N change to DFHS26FR489.	42	1A	
	0119 to 0120	Page 14	Change R368 to install,R366 to NI to set w/ docking.	43	1A	
		Page 27	Change D7 to install to solve 7402 does not work.	44	1A	
		Page 19	Delete R410,R413,R417 for EMI layout.	45	1A	
		Page 23	Correct CN6 C1~C4 pin define.			
		Page 23	Reserve Q37,Q38,RP56,R513,R514 for DVI disable when docking attach.			
		Page 29	CN25 footprint change to "SATA-C16647-122A4-B-22P-R-V" for SMT issue.			
C2 TO C3	0120 to 0209A	Page 25	LAN active/link LED change to +3VSUS.			



PROJECT : TW3  
Quanta Computer Inc.

Size	Document Number	Rev
Change List (B2A)		B1A
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PROJECT: TW3	PCBA NO.	REV: 2B	DOC. NO :
APPROVED BY : Johnson Hsu	CHECK BY : Titan Chiang	DRAWING BY : Tony Huang	DATE :05/05/2005
		SHEET 1	



A. G72M to G72MV

1. change P/N to G72MV (AJ073000T14)
2. Set VGA core to 1.0V fix.
3. Change PCI\_DEVID.

B. VRAM 128MB to 64MB

- 1.follow config table to set RAM\_CFG.
- 2.Change VRAM P/N to HYNIX.
- 3.VRAMx2

C. LAN GIGA to 10/100.


- 1.Change LAN chip to 8038(AJ080380000).
- 2.Change Rset resistor.
- 3.Change transformer.


D. SATA to PATA

- 1.Set ODD to slave.
- 2.Set HDD to master.
3. Remove SATA conn.
4. Add PATA conn.
5. Change board ID to PATA.
6. Install resistor to connect ODD and HDD LED.
7. NI resistor of SATA LED.

E. docking to no docking.

- 1.Set board ID4 to low.

MODEL	REV	CHANGE LIST		Model	TW3 M/B	
				Page	From	To
TW3A  C2 to C3	0209 to 0222A	Page 23  Page 27  Page 31  Page 34  Page 42	(1)CN20 pin 12,15 change connect to DVI_DDCDAT,DVI_DDCCLK (In C1 was connect to DDCCLK2,DDCDAT2) (2)R150,R159,Q37,Q38,RP56 Change to install for DVI,CRT I2C,D1 change to NI (3) Change L67,L68,L69 P/N from CX8BB121002 to CX8BB470007 (4)Change C794,C795,C796 P/N from CH01806JB07 to CH01006JB08 (1)Change R208 pin1 contact to +3VRUN Change R208 P/N to CS31002JB28,C473 change to CH4102K1B03 ,D7 change to NI. (1)Change L50,L51,L52,L53 P/N from CS00003J951 to CX0HM121008 (2)Add C759,C760,C761,C762 to install (CH02206GB02) (1)RP47,RP48,RP49 change to CJ3100A8N21(meet Rohs) (1)Change PR147 to NI	1	1A	
				2	1A	
				3	1A	
				4	1A	
				5	1A	
				6	1A	
				7	1A	
				8	1A	
				9	1A	
				10	1A	
				11	1A	
				12	1A	
				13	1A	
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				39	1A	
				40	1A	
				41	1A	
				42	1A	
				43	1A	
				44	1A	
				45	1A	
				<div><div></div><div>PROJECT : TW3 Quanta Computer Inc.</div></div> <div><div>Size</div><div>Document Number</div><div>Rev</div></div> <div><div>Change List (B2A)</div><div>B1A</div></div> <div><div>Date: Thursday, March 09, 2006</div><div>Sheet 47 of 48</div></div>		
PROJECT: TW3		PCBA NO.	REV: 2B	DOC. NO :		
APPROVED BY : Johnson Hsu		CHECK BY : Titan Chiang	DRAWING BY : Tony Huang	DATE :05/05/2005		SHEET 1



PROJECT : TW3  
Quanta Computer Inc.

Size

Document Number

Rev

Change List (B2A)

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