Model Name:MRHM7AP-LF

Revision 1.0

SHEET	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	PWRGD&RESET MAP
05	POWER DELIVERY CHART
06	CPU_1-PCIE_DMI_FDI_eDP
07	CPU_2-MEM Controller
08	DDRIII CHANNEL A,B
09	CPU_3-PWR
10	CPU_4-GND
11	HDMI,mDP
12	NM70_FDI, DMI,USB,PCI
13	NM70_DISPLAY,GPIO
14	NM70_HOST,SATA,HDA,SPI
15	NM70_CLK BUFFER,PCIE
16	NM70_PWR
17	NM70_GND
18	SIO ITE8773 , FAN,FP
19	AUDIO CODEC ALC887
20	AUDIO JACK
21	RTL8111E-CG/RTL8105E-H
22	LINNER POWER-1
23	DISCRETE POWER
24	AD19V & VCC5 & VCC3
25	VCORE & VCPU_VAXG NCP6131
26	
27	

SHEET	TITLE
28	
29	
30	
31	
32	
33	

GIGABYTE TECHNOLOGIES , INC.

Title	Cover Sheet	
Size: Custom	Document Number: MRHM7AP-LF	Rev: 1.0
Date: Tuesday, March 26, 2013	Sheet 1 of 25	

Model Name: MRHM7AP-LF

Revision 0.1

Component value change history

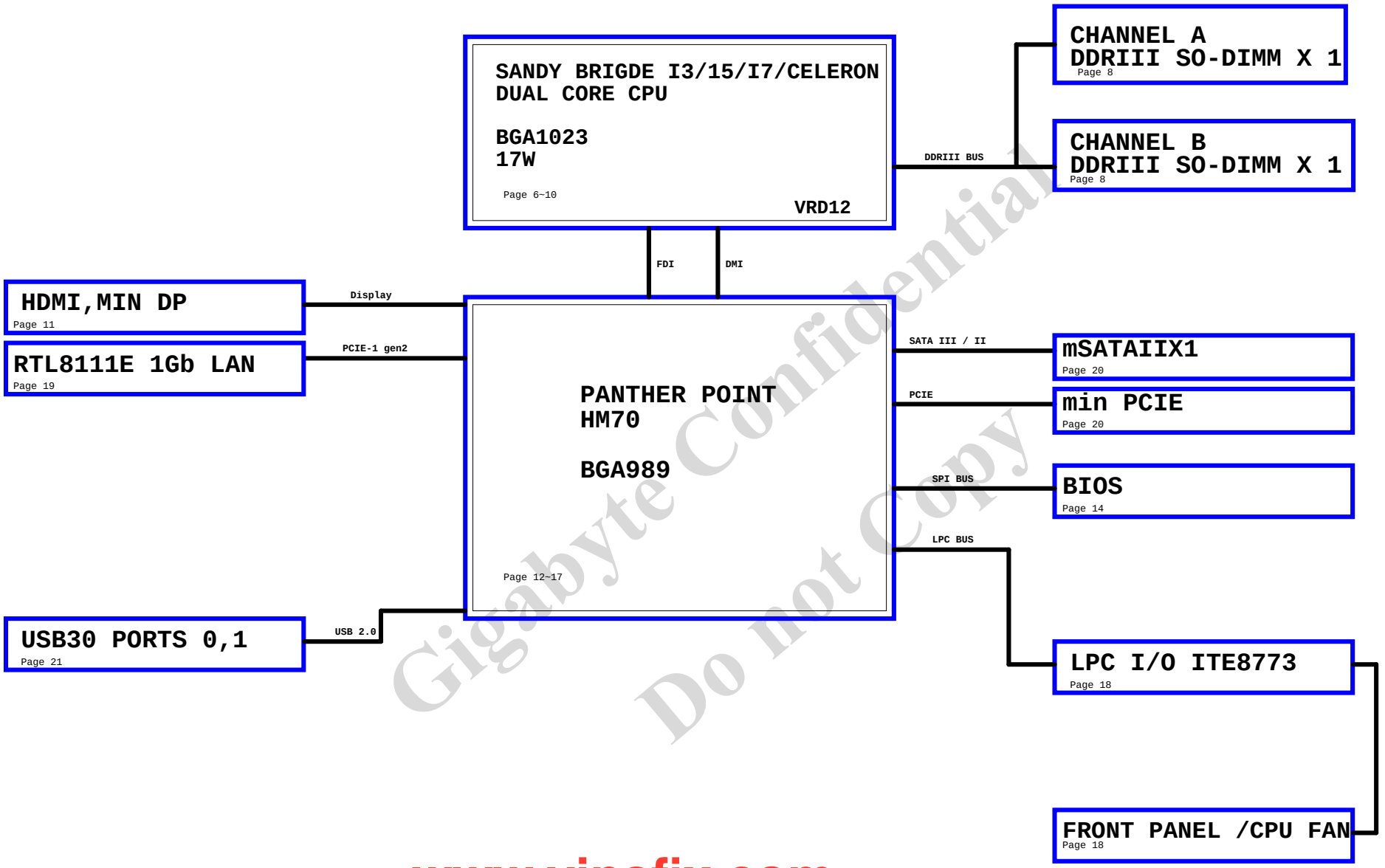
2012/07/31

Data	Change Item	Reason

Circuit or PCB layout change

DATE	Change Item	Reason

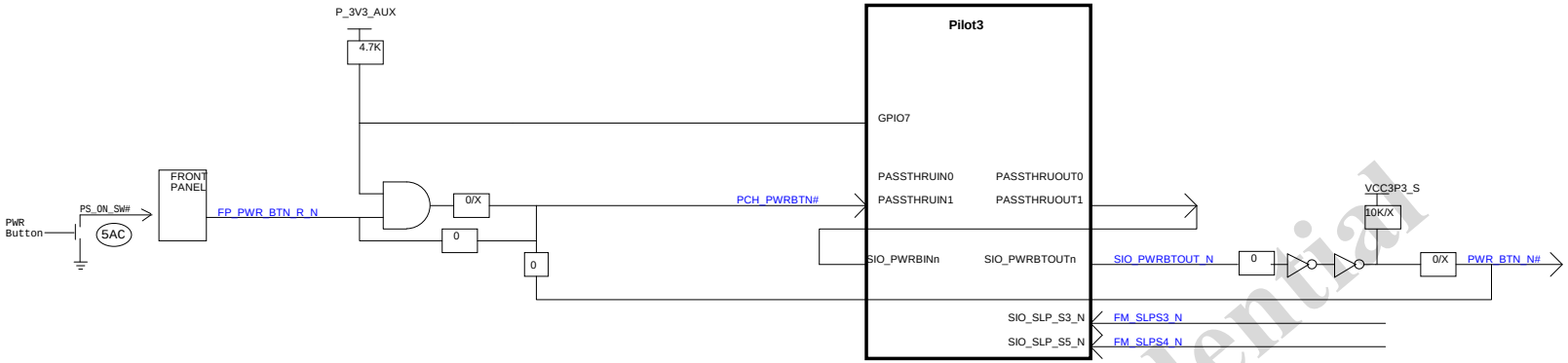
BLOCK DIAGRAM

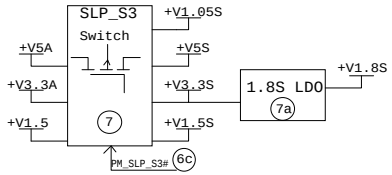


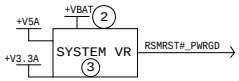
GIGABYTE TECHNOLOGIES , INC.

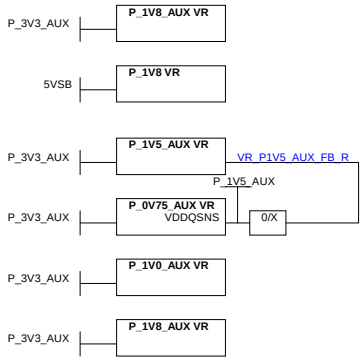
Title	BLOCK DIAGRAM	
Size C	Document Number MRHM7AP-LF	Rev 1.0
Date: Tuesday, March 26, 2013	Sheet 3 of 25	

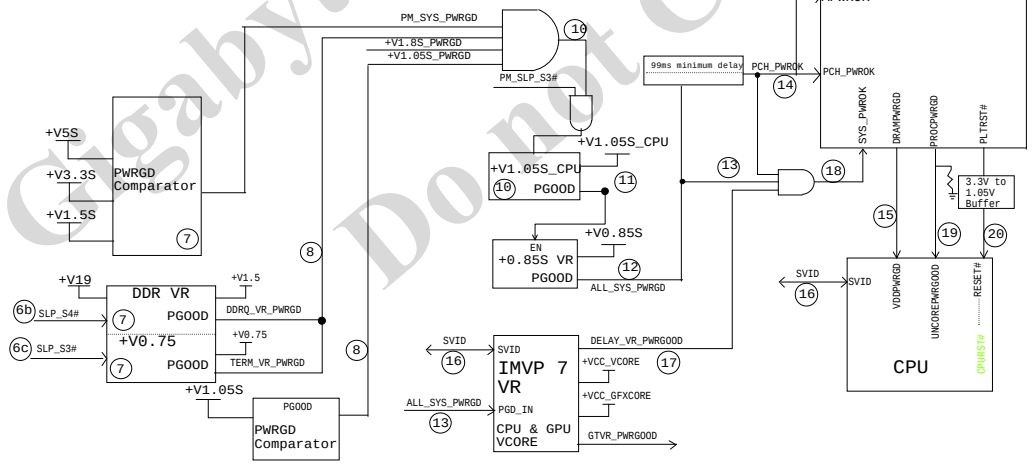
Huron River Power Up Sequence Diagram



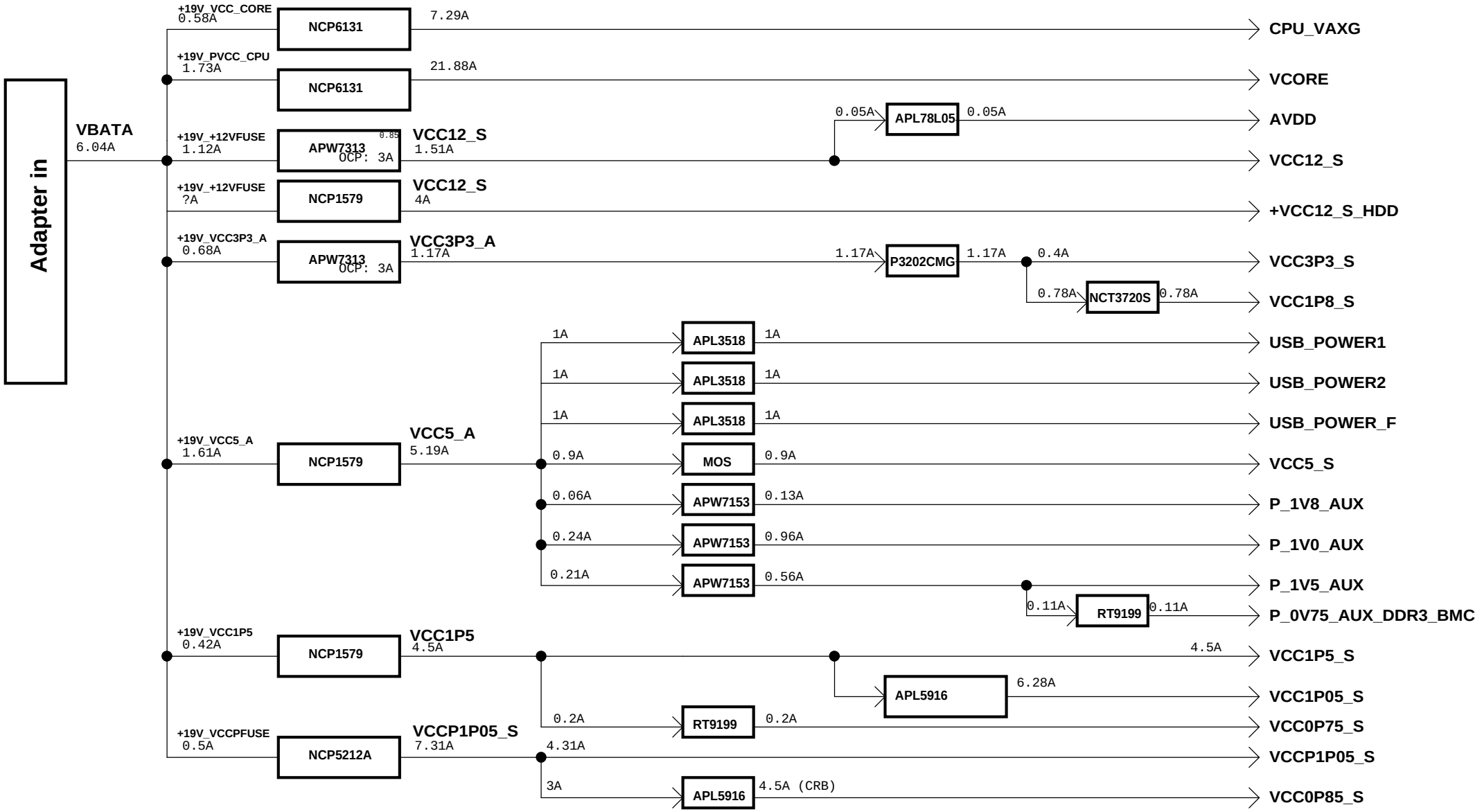








Title	PWRGD&RESET MAP	
Size: Custom	Document Number: MRHM7AP-LF	Rev: 1.0
Date: Tuesday, March 26, 2013	Sheet 4 of 25	



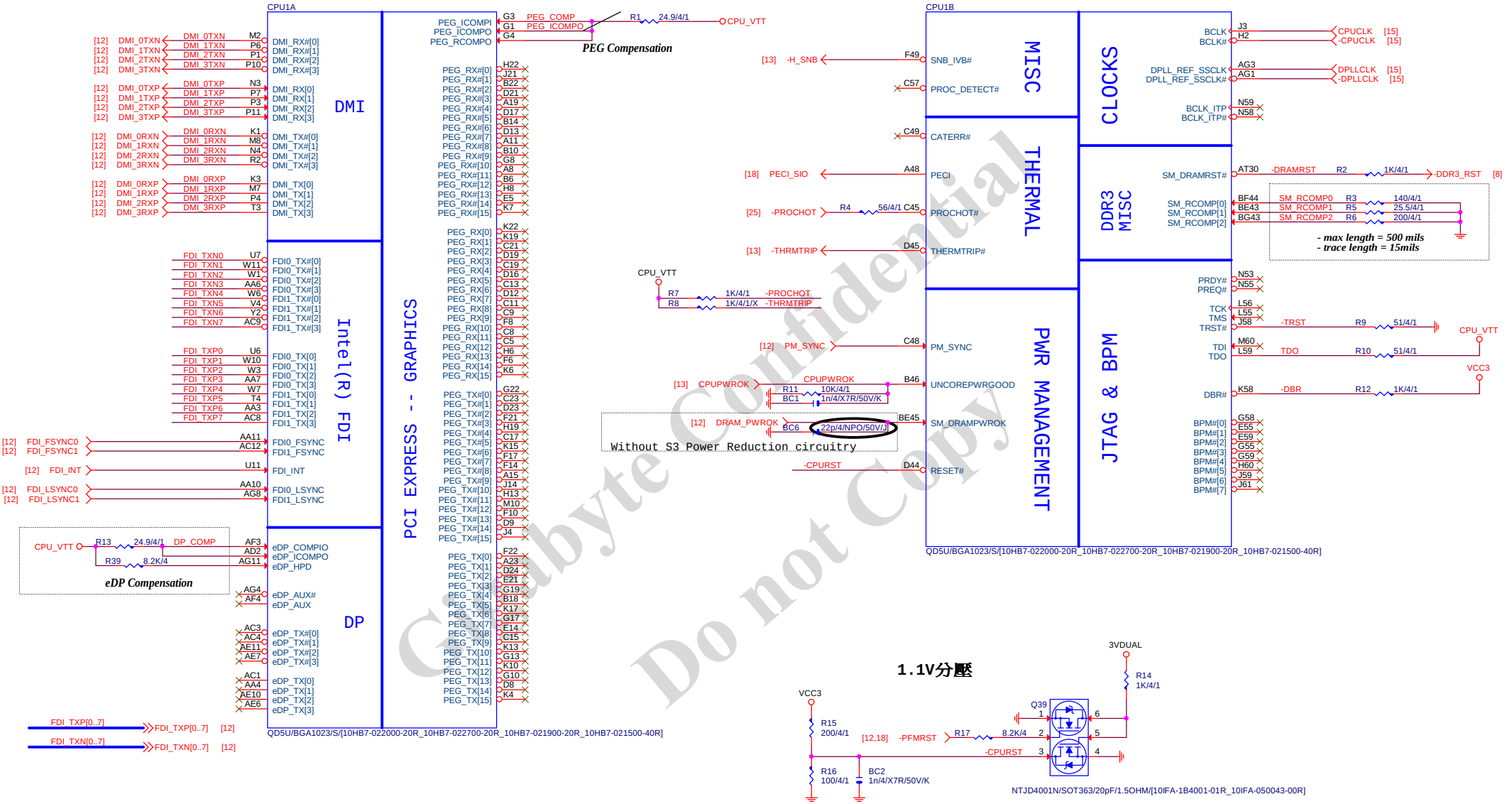
Title	POWER DELIVERY CHART	
Size B	Document Number MRHM7AP-LF	Rev 1.0
Date: Tuesday, March 26, 2013	Sheet 5 of 25	

Sandy Bridge 2C BGA Processor (DMI,DP,PEG,FDI)

Sandy Bridge 2C BGA Processor (CLK,MISC,JTAG)

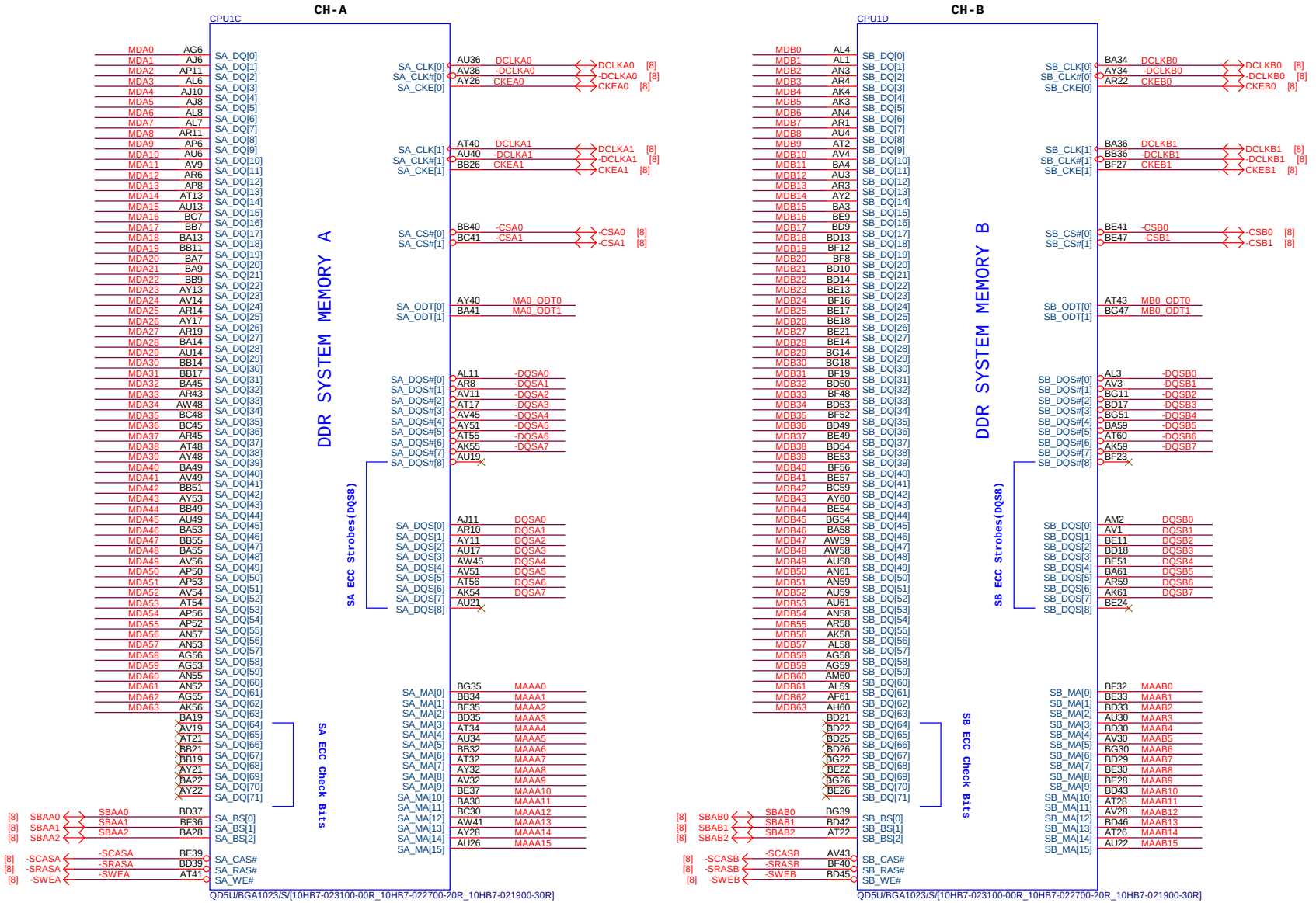
Please don't reversal DMI and FDI lane.

PEG_ICOMPO 12 mils



GIGABYTE TECHNOLOGIES , INC.			
Title	Sandy Bridge--DMI, FDI, eDP, PEG		
Size	Document Number MRHM7AP-LF		Rev 1.0
Date: Tuesday, March 26, 2013	Sheet 6 of 25		

Sandy Bridge 2C BGA Processor (DDR3)



GIGABYTE TECHNOLOGIES , INC.		
Title	Sandy Bridge--Memory	
Size	Document Number: MRHM7AP-LF	Rev: 1.0
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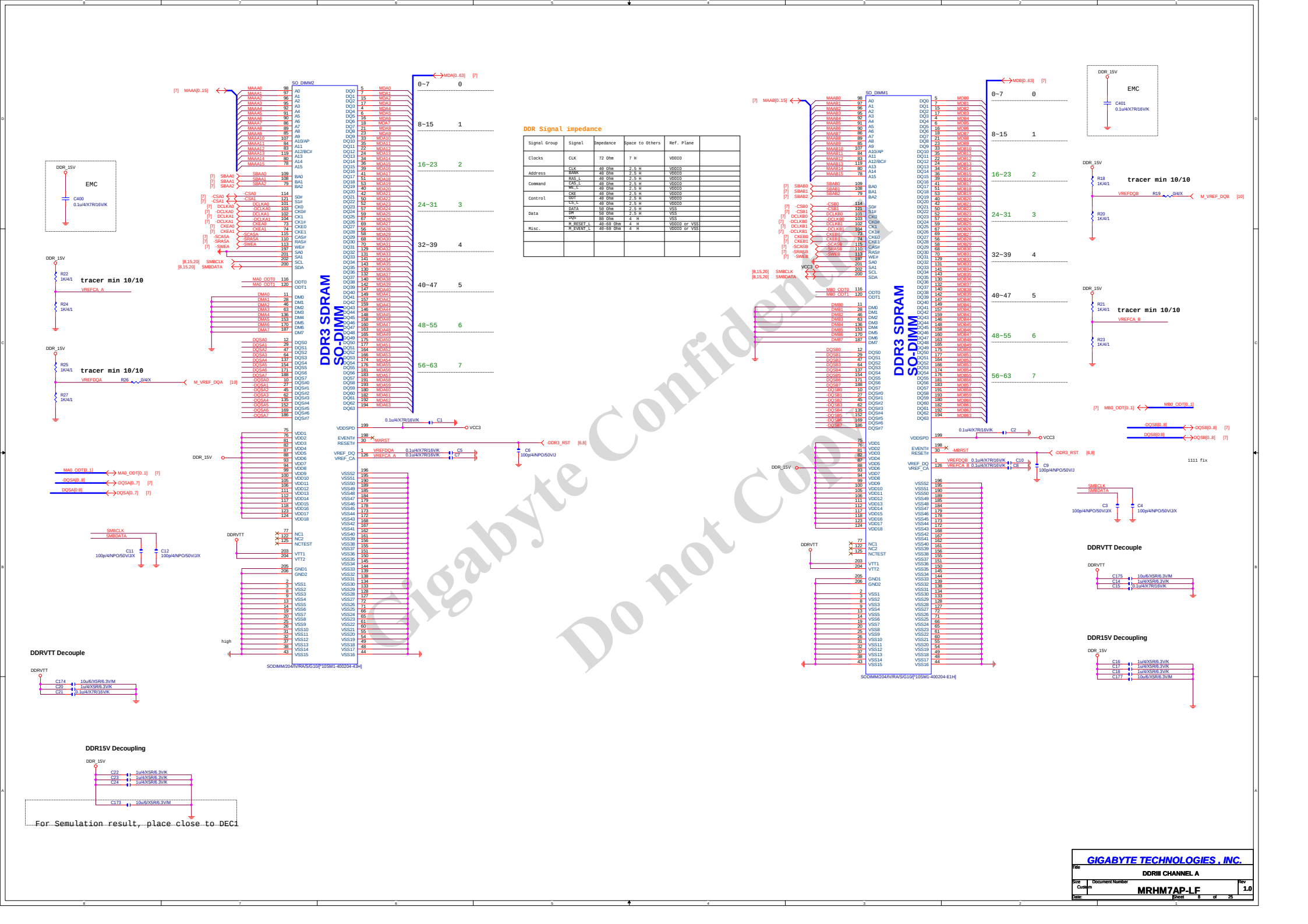
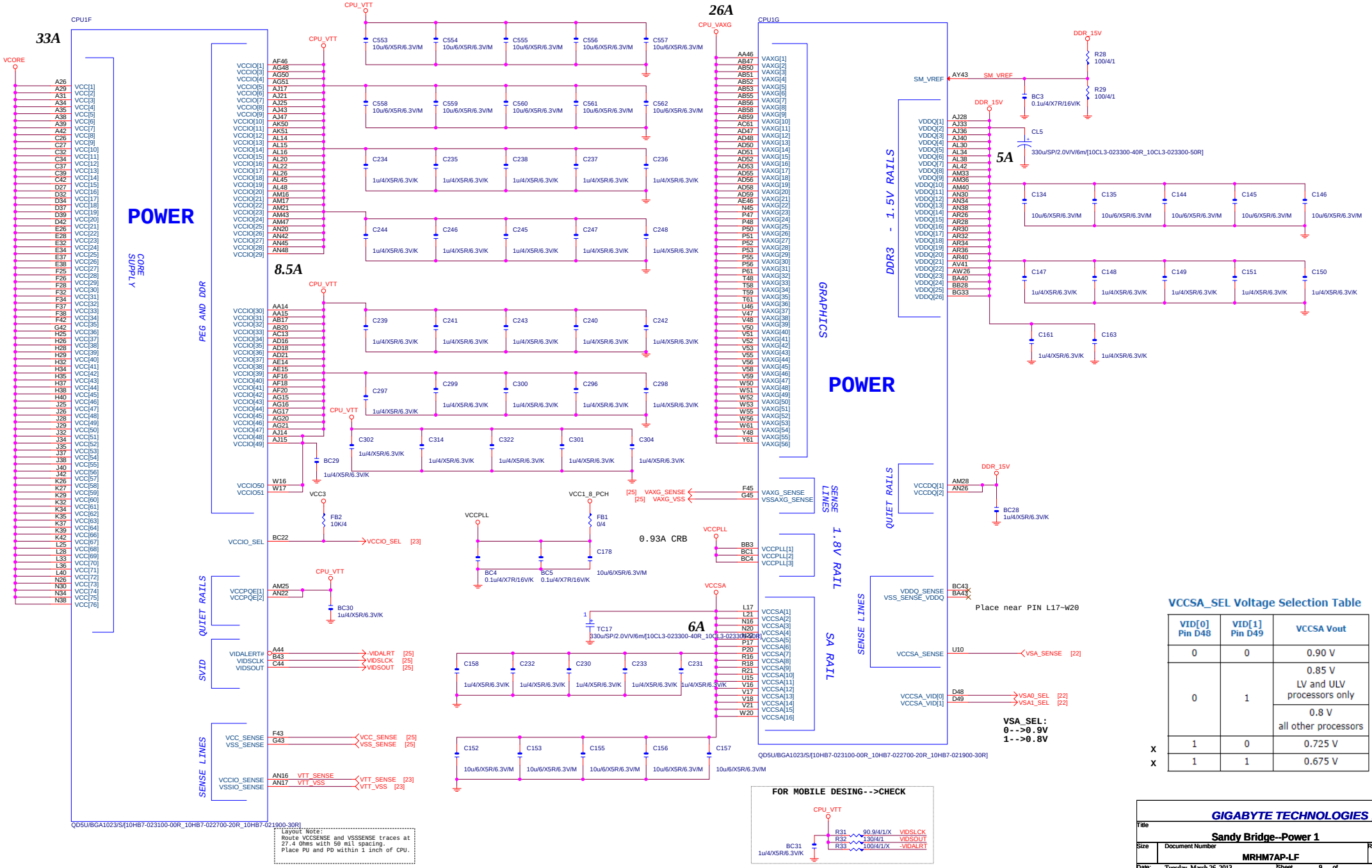

SO_DIMM2
DDR3 SDRAM
SO-DIMM
SO_DIMM1
DDR3 SDRAM
SO-DIMM
DDR Signal impedance
Signal Group | Signal | Impedance | Space to Others | Ref. Plane
Clocks | CLK | 72 Ohm | 7 H | VDDIO
Address | BANK | 48 Ohm | 2.5 H | VDDIO
Command | RAS_L | 48 Ohm | 2.5 H | VDDIO
Control | CAS_L | 48 Ohm | 2.5 H | VDDIO
Data | DQ | 48 Ohm | 2.5 H | VDDIO
Misc. | M_RESET_L | 48-60 Ohm | 4 H | VDDIO or VSS
Misc. | M_EVENT_L | 48-60 Ohm | 4 H | VDDIO or VSS
EMC
tracer min 10/10
DDRVTT Decouple
DDR15V Decoupling
For Semulation result, place close to DEC1
GIGABYTE TECHNOLOGIES , INC.
DDRIII CHANNEL A
MRHM7AP-LF
1.0
Gigabyte Confidential
Do not Copy

Sandy Bridge 2C BGA Processor (Power)



VCCSA_SEL Voltage Selection Table

VID[0] Pin D48	VID[1] Pin D49	VCCSA Vout
0	0	0.90 V
0	1	0.85 V LV and ULV processors only
		0.8 V all other processors
1	0	0.725 V
1	1	0.675 V

X
X

GIGABYTE TECHNOLOGIES , INC.

Title	Sandy Bridge--Power 1	
Size	Document Number	Rev
	MRHM7AP-LF	1.0
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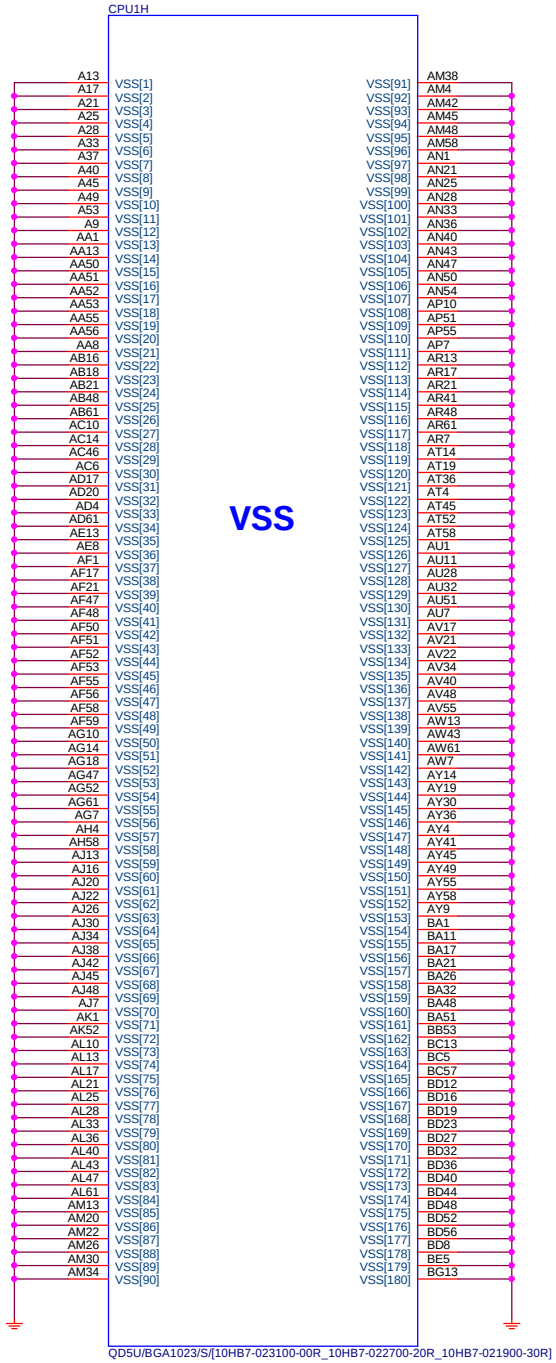
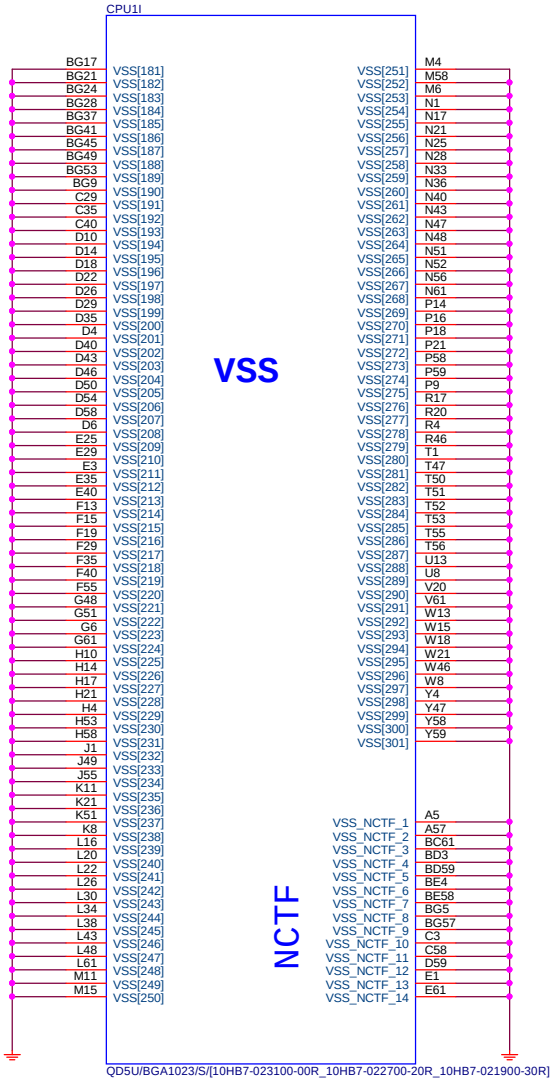
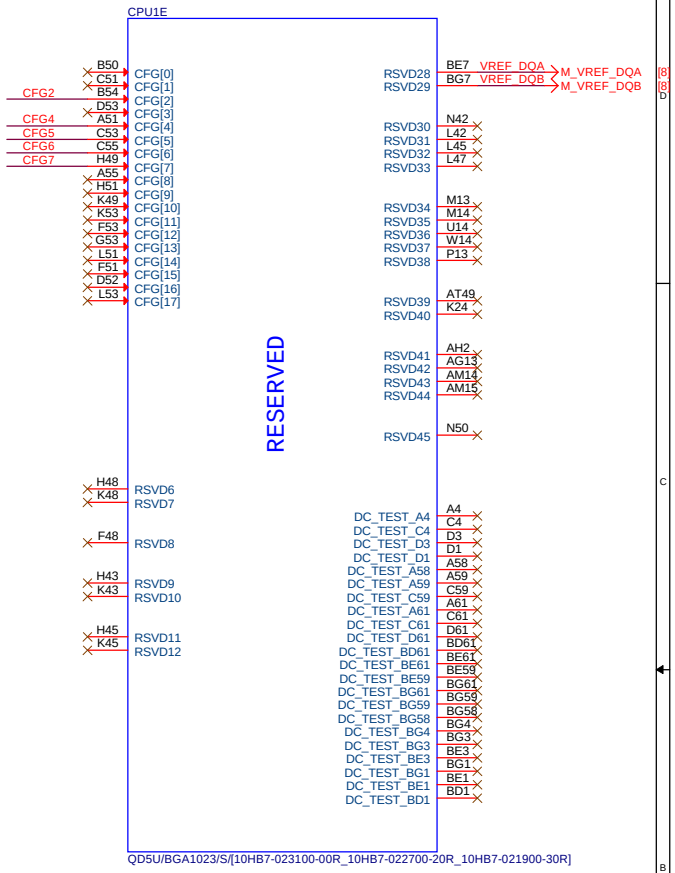
Sandy Bridge 2C BGA Processor (GND)





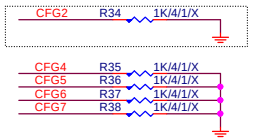
Sandy Bridge 2C BGA Processor (Reserved)



CFG	H	L	NOTE
0	RSVD	RSVD	RSVD
1	RSVD	RSVD	RSVD
2	**NORM**	**Reverse**	LANE REVERSAL[0],x16
3	RSVD	RSVD	RSVD
4	**DISABLE**	**ENABLE**	eDP ENABLE
7	RSVD	RSVD	RSVD
8	RSVD	RSVD	RSVD
9	RSVD	RSVD	RSVD
10	RSVD	RSVD	RSVD
11	RSVD	RSVD	RSVD
12	RSVD	RSVD	RSVD
13	RSVD	RSVD	RSVD
14	RSVD	RSVD	RSVD
15	RSVD	RSVD	RSVD
16	RSVD	RSVD	RSVD
17	RSVD	RSVD	RSVD

CFG6	CFG5	PCIE CONFIG
1	1	1X16 , Default
1	0	2X8
0	1	RSVD
0	0	X8,X4,X4

CFG 0-17 all internal PULL-UP



GIGABYTE TECHNOLOGIES , INC.

Title	Sandy Bridge --GND	
Size	Document Number: MRHM7AP-LF	Rev: 1.0
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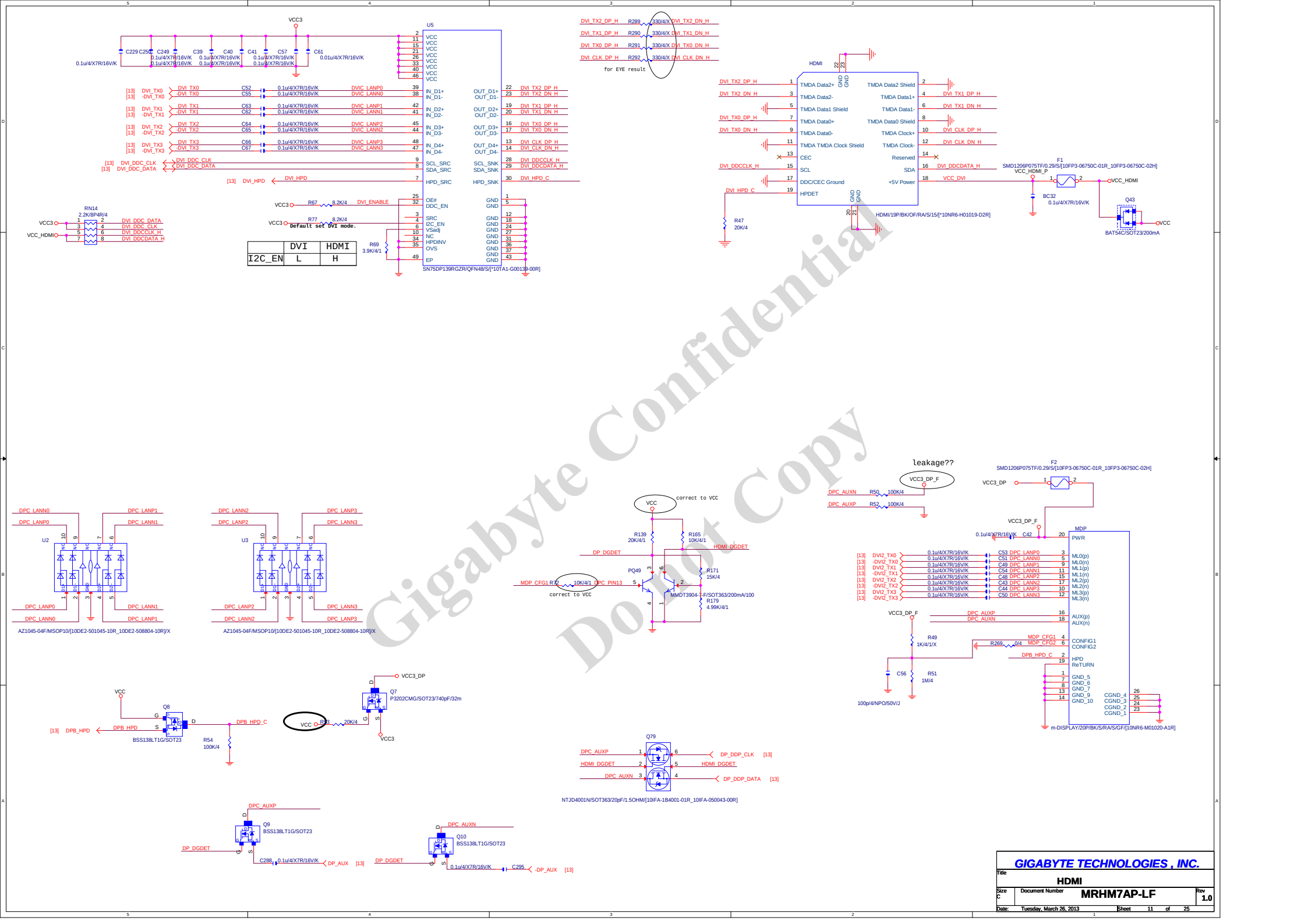

Title	HDMI
Size	C
Document Number	MRHM7AP-LF
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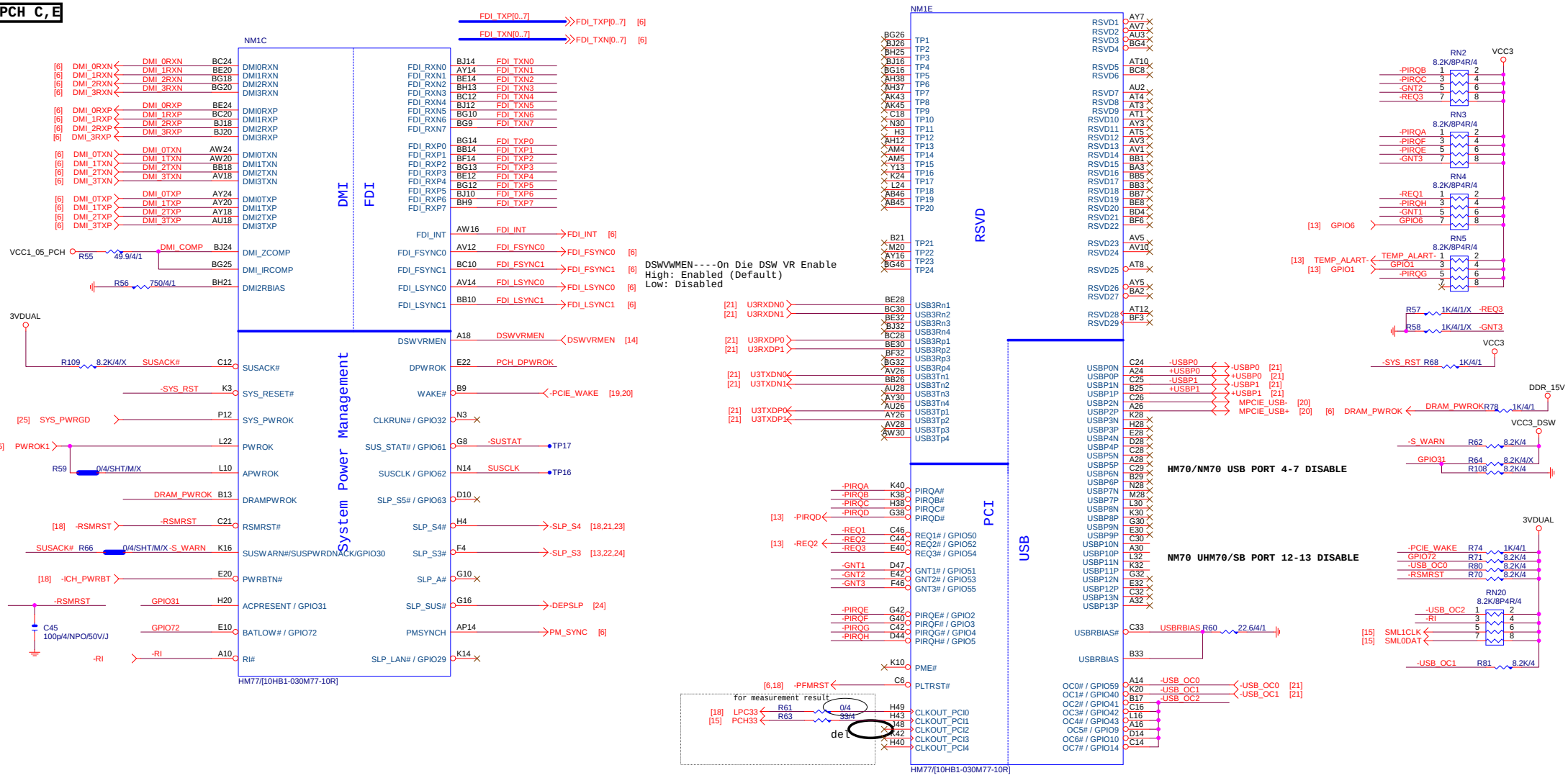
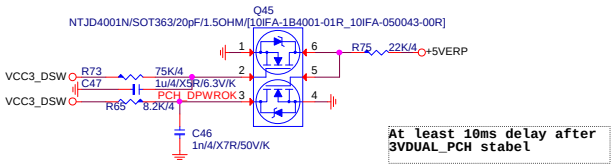
GIGABYTE TECHNOLOGIES , INC.

PCH C,E





At least 10ms delay after 3VDUAL_PCH stabel

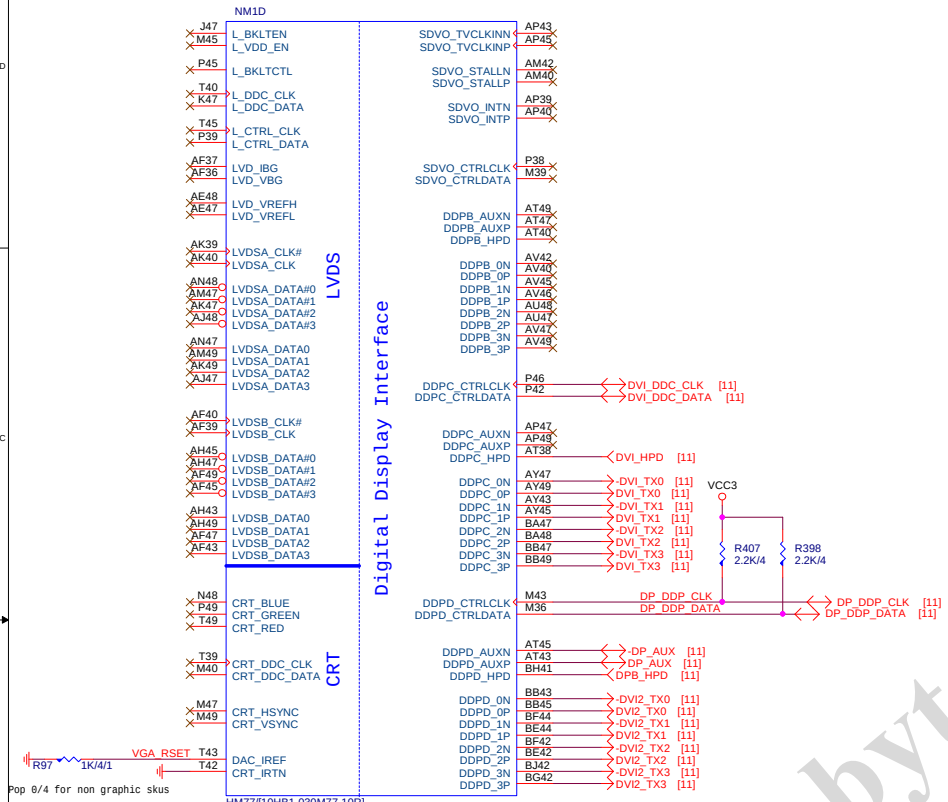
FOR FUSE SHORT GPIO

USB OC# Configure	
OC0#	USB0,1(USB2_1)
OC1#	USB2,3(USB2_2)
OC2#	USB4,5(NM70:N/A)
OC3#	USB6,7(NM70:N/A)
OC4#	USB8,9(F_USB2_1)
OC5#	USB10~11(TP/TV_USB)
OC6#	USB12~13(N/A)
OC7#	GPIO14

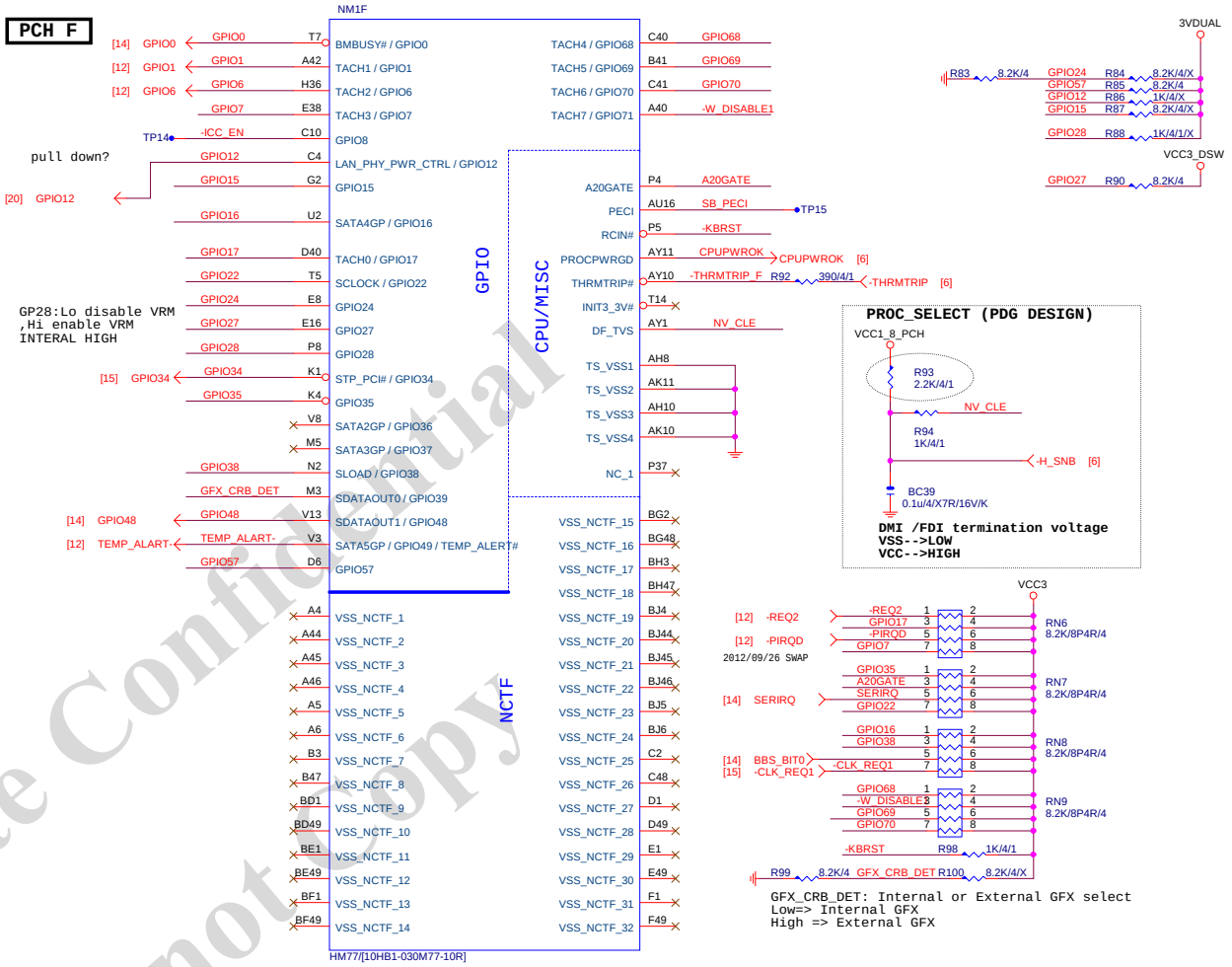
GIGABYTE TECHNOLOGIES , INC.

Title	PCH FDI,DMI,USB ,PCIE,NVRAM		
Size: Custom	Document Number: MRHM7AP-LF		Rev: 1.0
Date: Tuesday, March 26, 2013	Sheet 12 of 25		

PCH D DISPLAY



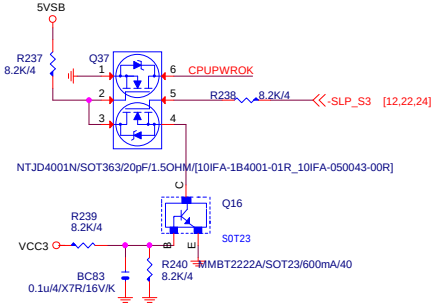
PCH F



VGA ESD

VGA SIGNAL

CPUPWROK



GIGABYTE TECHNOLOGIES , INC.		
Title: PCH DISPLAY ,CLK BUFFER		
Size: Custom	Document Number: MRHM7AP-LF	Rev: 1.0
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PCH A

[18] LAD[0..3] → LAD[0..3]

Y1 A20 RTCX1
Y2 C20 RTCX2
-RTCRST D20 RTCRST#
-SRTCRST G22 SRTCRST#
[14,16] RTCVDD — R111 1M/4 — K22 INTRUDER#
INTVRMEN C17 INTVRMEN

N34 HDA_BCLK
A_SYC L34 HDA_SYNC
T10 SPKR
K34 HDA_RST#
E34 HDA_SDIN0
G34 HDA_SDIN1
C34 HDA_SDIN2
A34 HDA_SDIN3
A_SO A36 HDA_SDO
C36 HDA_DOCK_EN# / GPIO33
GPIO13 N32 HDA_DOCK_RST# / GPIO13

PCH_TCK J3 JTAG_TCK
PCH_TMS H7 JTAG_TMS
PCH_TDI K5 JTAG_TDI
PCH_TDO H1 JTAG_TDO

SPI_CLK_R R134 33/4/1 SPI_CLK T3 SPI_CLK
SPI_CS0#_R R136 0/4 SPI_CS0# Y14 SPI_CS0#
T1 SPI_CS1#
SPI_SI_R R138 33/4/1 SPI_SI V4 SPI_MOSI
SPI_SO U3 SPI_MISO

FWH0 / LAD0 C38 LAD0 → LAD0 [18]
FWH1 / LAD1 A38 LAD1 → LAD1 [18]
FWH2 / LAD2 B37 LAD2 → LAD2 [18]
FWH3 / LAD3 C37 LAD3 → LAD3 [18]
FWH4 / LFRAME# D36 -LFRAME → -LFRAME [18]
LDRQ0# E36
LDRQ1# / GPIO23 K36
SERIRQ V5 SERIRQ → SERIRQ [13]

SATA0RXN AM3 MSATA_RX0N → MSATA_RX0N [20]
SATA0RXP AM1 MSATA_RX0P → MSATA_RX0P [20]
SATA0TXN AP7 SATA0TXN — C59 0.01u/4/X7R/16V/K → MSATA_TX0N [20]
SATA0TXP AP5 SATA0TXP — C60 0.01u/4/X7R/16V/K → MSATA_TX0P [20]
SATA1RXN AM10
SATA1RXP AM8
SATA1TXN AP11
SATA1TXP AP10
SATA2RXN AD7
SATA2RXP AD5
SATA2TXN AH5
SATA2TXP AH4
SATA3RXN AB8
SATA3RXP AB10
SATA3TXN AF3
SATA3TXP AF1
SATA4RXN Y7
SATA4RXP Y5
SATA4TXN AD3
SATA4TXP AD1
SATA5RXN Y3
SATA5RXP Y1
SATA5TXN AB3
SATA5TXP AB1
SATAICOMPO Y11
SATAICOMPI Y10 — SATA1COMP R130 37.4/4/1 → VCC1_05_PCH
SATA3RCOMPO AB12
SATA3COMPI AB13 — SATA3COMP R131 49.9/4/1 → VCC1_05_PCH
SATA3RBIAS AH1 — SATA3BIAS R135 750/4/1
SATALED# P3
SATA0GP / GPIO21 V14 GPIO21
SATA1GP / GPIO19 P1 BBS_BIT0 → BBS_BIT0 [13]

HM70/NM70 SATA3.0 ONLY PORT0
FOR 4PORT SKU PORT 1,3 DISABLE

BBS_BIT0: BIOS Boot Strap Bit 0

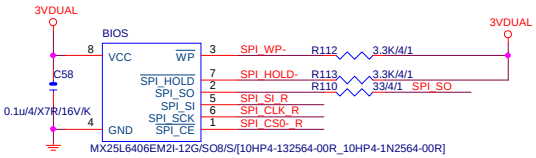
PCH HS

Boot BIOS Strap

PCI_GNT#1	BBS_BIT0	Boot BIOS Location
1	1	SPI (Default)
0	1	Reserved (NAND)
0	0	LPC

1 means floating
0 means PD 1K

BIOS



VCC3
[15] -CLK_REQ2 — -CLK_REQ2 R116 8.2K/4
[13] GPIO48 — GPIO48 R118 8.2K/4

3VDUAL
PCH_TDI R119 210/4/1
PCH_TDO R120 210/4/1
PCH_TMS R121 210/4/1
GPIO13 R123 8.2K/4
A_SO R124 1K/4/1/X
A_SYC R125 8.2K/4

HDA_SDOUT: Flash Descriptor Security Overide
Low (Default) ==> Disabled
High ==> Enabled

A_SYC: PLL ODVR Voltage
Low (Default) ==> 1.8V
High ==> 1.5V

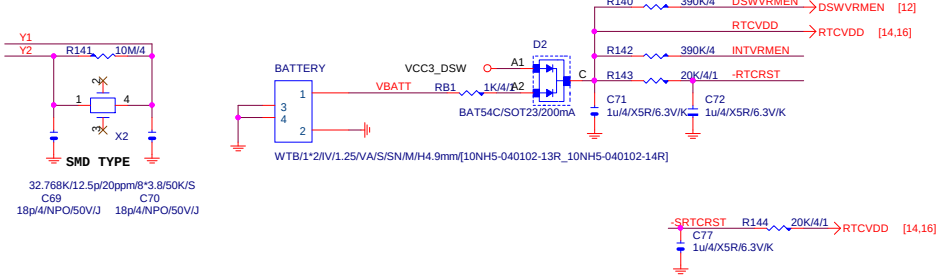
PCH_TDI R126 100/4/1
PCH_TDO R127 100/4/1
PCH_TMS R128 100/4/1
PCH_TCK R129 4.7K/4

ICH_INTVRMEN: Integrated SUS 1.05V VRM Enable
High ==> Enabled internal VRs
Low ==> Enabled external VRs

VCC3
[13] GPIO0 — GPIO0 R132 8.2K/4
GPIO21 R133 8.2K/4

CR2032 BATTERY
CR2032/[11BL5-032032-31R_11BL5-032032-32R]

RB 必須放在BAT外



GIGABYTE TECHNOLOGIES , INC.

Title	PCH HOST , SATA, PCI	
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PCH B

NM1B

LAN

[19] LAN_GPPRXN
[19] LAN_GPPRXP
[19] LAN_GPPTXN
[19] LAN_GPPTXP
0.1u/4/X7R/16V/K C78 PET_N1
0.1u/4/X7R/16V/K C79 PET_P1

[20] PCIEMIN1_RXN
[20] PCIEMIN1_RXP
[20] PCIEMIN1_TXN
[20] PCIEMIN1_TXP
0.1u/4/X7R/16V/K C82 PET_N3
0.1u/4/X7R/16V/K C83 PET_P3

PCI-E*

HM/NM70 5~8 PORT DISABLE

LAN

[19] PCIE_LAN_CLKN
[19] PCIE_LAN_CLKP

Mini_PCIE

[20] mPCIE1_CLK
[20] -mPCIE1_CLK

SMBUS

SMBALERT# / GPIO11
SMBCLK
SMBDATA
SML0ALERT# / GPIO60
SML0CLK
SML0DATA
SML1ALERT# / PCHHOT# / GPIO74
SML1CLK / GPIO58
SML1DATA / GPIO75

Controller Link

CL_CLK1
CL_DATA1
CL_RST1#

CLOCKS

PEG_A_CLKRQ# / GPIO47
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_DMI_N
CLKOUT_DMI_P
CLKOUT_DP_N
CLKOUT_DP_P
CLKIN_DMI_N
CLKIN_DMI_P
CLKIN_GND1_N
CLKIN_GND1_P
CLKIN_DOT_96N
CLKIN_DOT_96P
CLKIN_SATA_N
CLKIN_SATA_P
REFCLK14IN
CLKIN_PCILOOPBACK
XTAL25_IN
XTAL25_OUT
XCLK_RCOMP

FLEX CLOCKS

CLKOUTFLEX0 / GPIO64
CLKOUTFLEX1 / GPIO65
CLKOUTFLEX2 / GPIO66
CLKOUTFLEX3 / GPIO67

native 48Mhz

all the CLKRQ# signals are Mobile Only.

HM77/[10HB1-030M77-10R]

Flex0,2 : 33MHZ
Flex1,3 : 27/14/24/48/25MHZ

Company	GIGABYTE TECHNOLOGIES , INC.
Title	PCH GPIO , CTRL , AUDIO
Size	Custom
Document Number	MRHM7AP-LF
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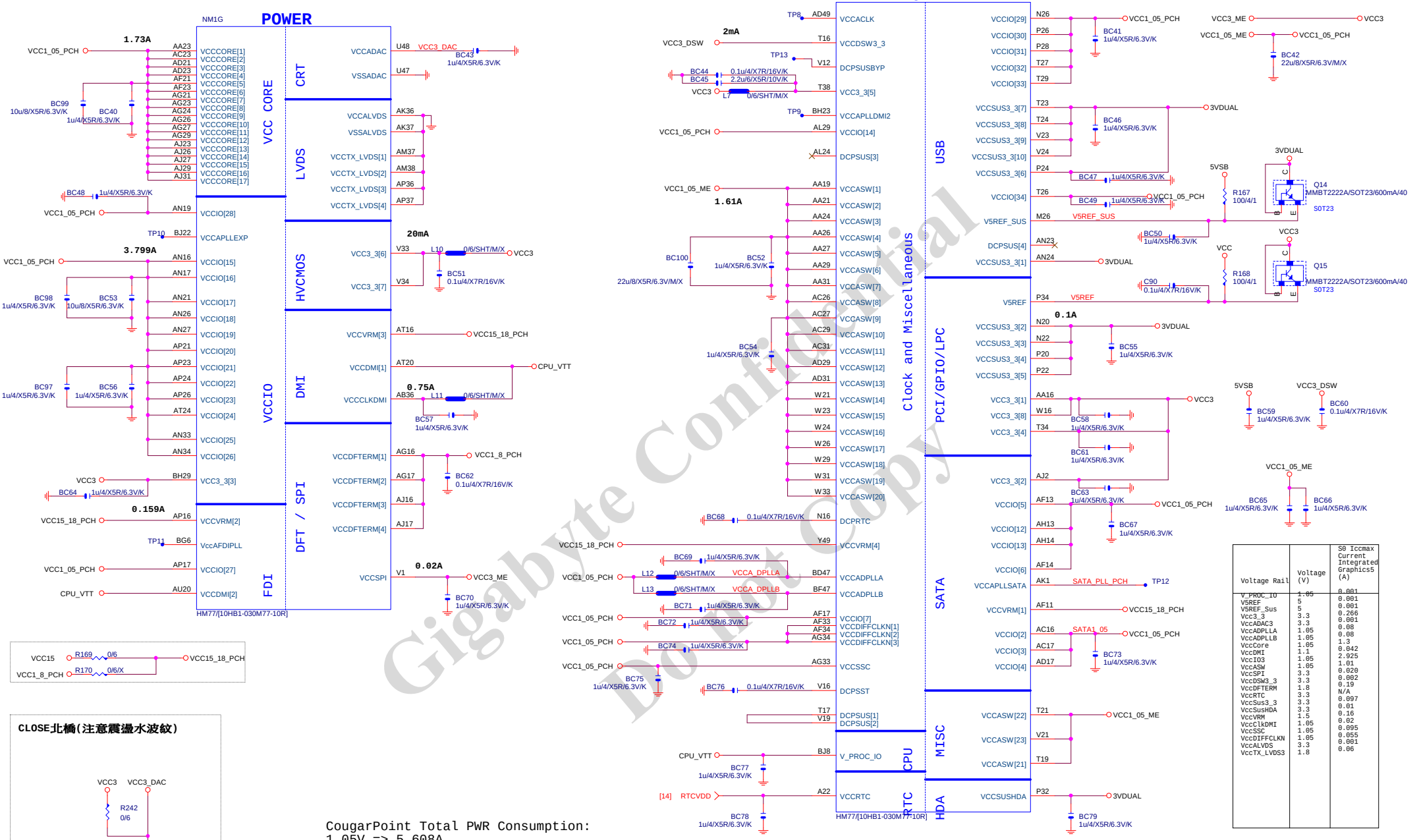
PCH G,J POWER



Voltage Rail	Voltage (V)	S0 Iccmax Current Integrated Graphics5 (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.1	0.042
VccIO3	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.020
VccDSW3_3	3.3	0.002
VccDFTERM	1.8	0.19
VccRTC	3.3	N/A
VccSus3_3	3.3	0.097
VccSusHDA	3.3	0.01
VccVRM	1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS3	1.8	0.06

CougarPoint Total PWR Consumption:
1.05V => 5.608A
5V => 0.002A
3.3V => 0.399A
1.8V => 0.25A
1.5V => 0.16A

CLOSE北橋(注意震盪水波紋)

GIGABYTE TECHNOLOGIES , INC.

Title	PCH PWR ,GND		
Size: Custom	Document Number: MRHM7AP-LF		Rev: 1.0
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PCH H,I GND

GIGABYTE TECHNOLOGIES , INC.		
Title: PCH ,GND		
Size: Custom	Document Number: MRHM7AP-LF	Rev: 1.0
Date: Tuesday, March 26, 2013	Sheet 17 of 25	

Power On Strapping Options

Symbol		value	Description
JP4	K8PWR_EN	1	K8 power sequence function is disabled
Pin 126		0	K8 power sequence function is enabled
JP3 & JP5	FAN_CTL_SEL	11	The default value of EC Index 15h/16h/17h is 80h
		10	The default value of EC Index 15h/16h/17h is FFh(Fan off)
Pin 124 & 46		01	The default value of EC Index 15h/16h/17h is 00h(Fan full speed)
		00	The default value of EC Index 15h/16h/17h is 40h
JP2	WDT_EN	1	Disable WDT to rest PWROK
Pin122		0	Enable WDT to rest PWROK

If without use these pins, Please pull-up. Don't let it floating
1.Pin 6:ATXPG
2.Pin 29:SUSB#
3.Pin 21/ Pin 57/ Pin 59/ Pin61
4.Pin37-40 KCLK/KDAT/MCLK/MDAT

5.Pin 63 pull high to 3VSB

Note:use EUP function:Pin29/Pin30/Pin31/Pin34/Pin42 pull high to SYS_3VSB.
Pin 5,Pin 32, pull high to 3.3VSB.Pin33 pull high to VCCH.

TEMP H/W MONITOR

Please close to SIO

80H

Company	GIGABYTE TECHNOLOGIES , INC.
Title	ITE8773,FAN,FP
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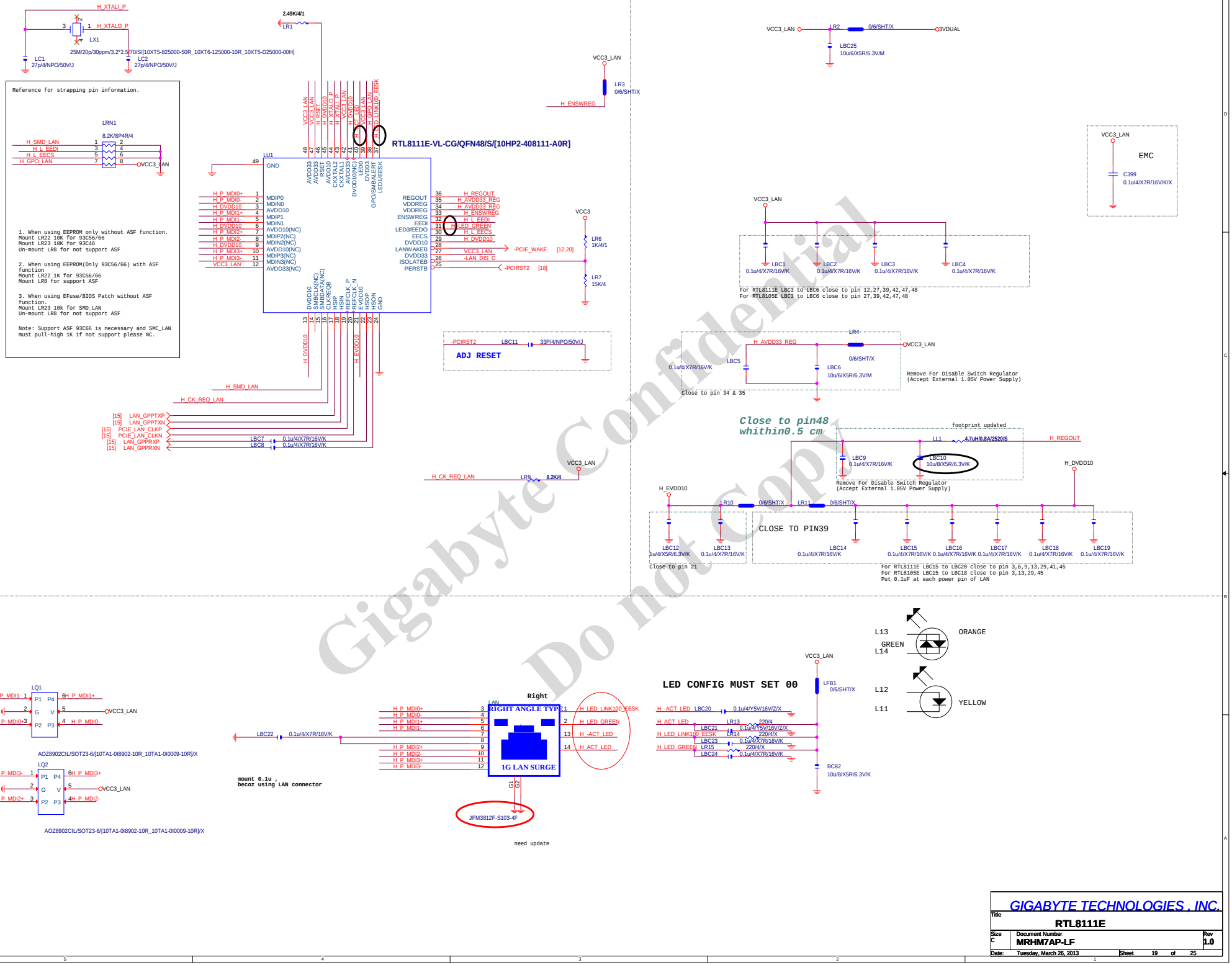

GIGABYTE TECHNOLOGIES , INC.		
Title: RTL8111E		
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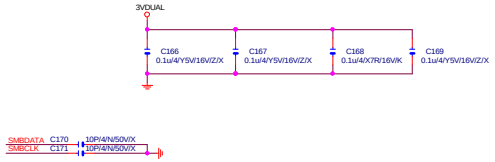
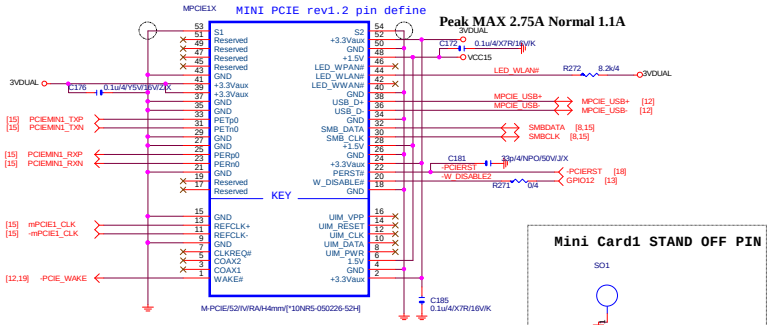
MINI_PCIE

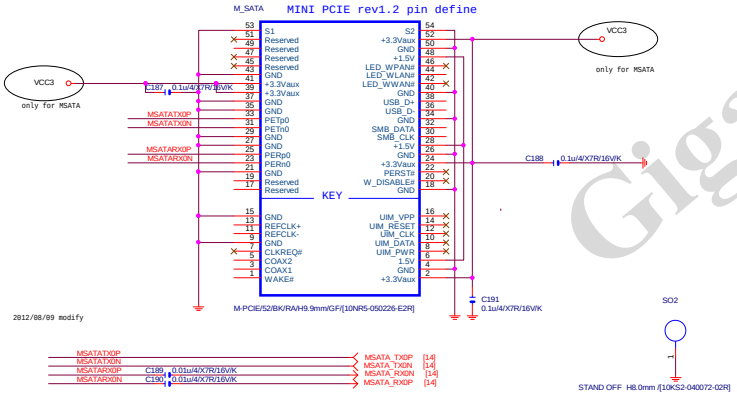


For WLAN slot



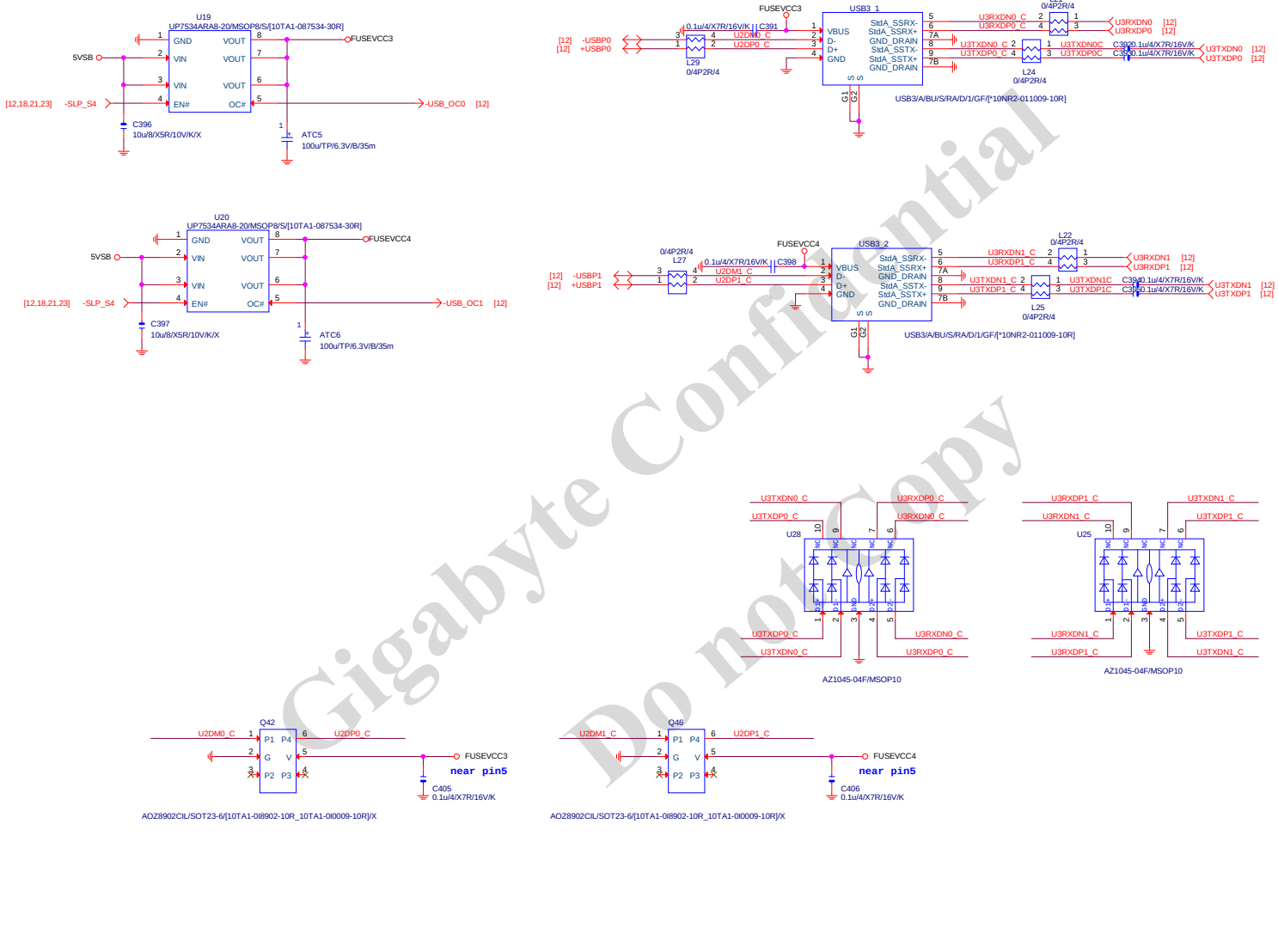
MSATA

For mSATA slot



EXT_CON PWR CIRCUIT

GIGABYTE TECHNOLOGIES , INC.		
Title: MINI-PCIE & PCIE& EXT_CON		
Size: Custom	Document Number: MRHM7AP-LF	Rev: 1.0
Date: Tuesday, March 26, 2013	Sheet 20 of 25	



GIGABYTE TECHNOLOGIES , INC.		
Title: FRONT & REAR USB		
Size: Custom	Document Number: MRHM7AP-LF	Rev: 1.0
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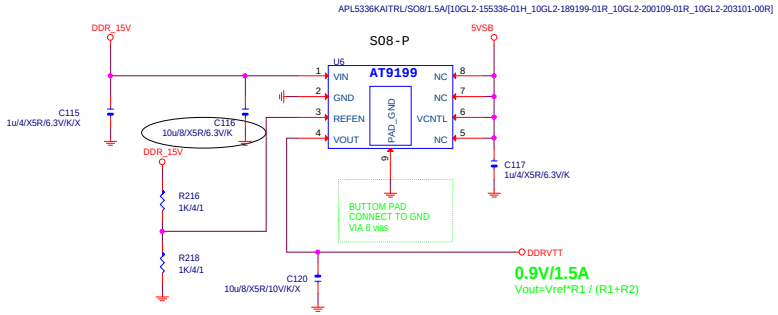
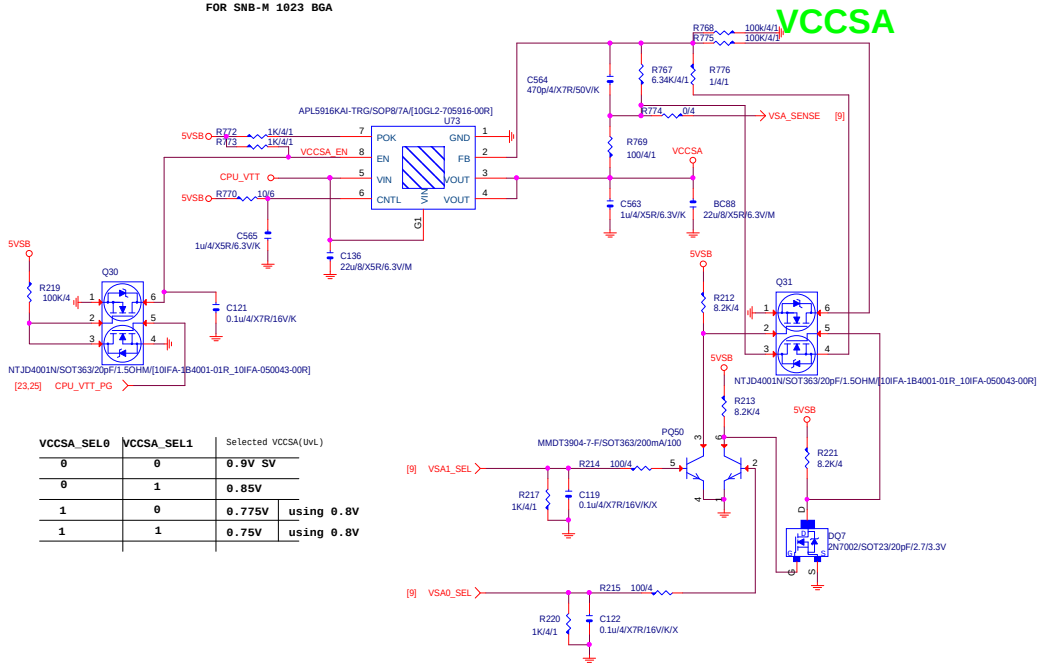
DDRVTT

DDR3 0.75V/0.83A



FOR SNB-M 1023 BGA

VCCSA

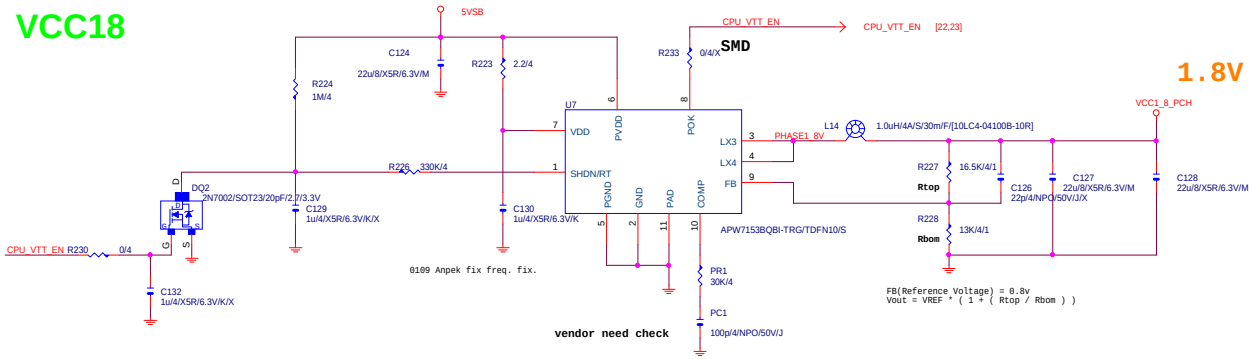


VCCSA_SEL0	VCCSA_SEL1	Selected VCCSA(UvL)	
0	0	0.9V 5V	
0	1	0.85V	
1	0	0.775V	using 0.8V
1	1	0.75V	using 0.8V

5VDUAL

VCC18

1.8V

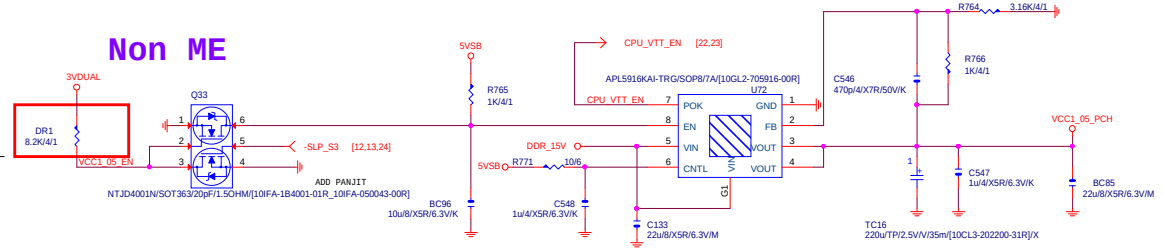


VCC1_05

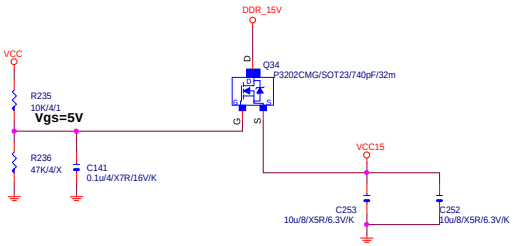
Note.

Non AMT model:
R225 remove.
DQ2.R230.C132.DR1 use.

Non ME



VCC15&VCC12



GIGABYTE TECHNOLOGIES , INC.		
Title: LINNER-POWER-1		
Size	Document Number: MRHM7AP-LF	Rev: 1.0
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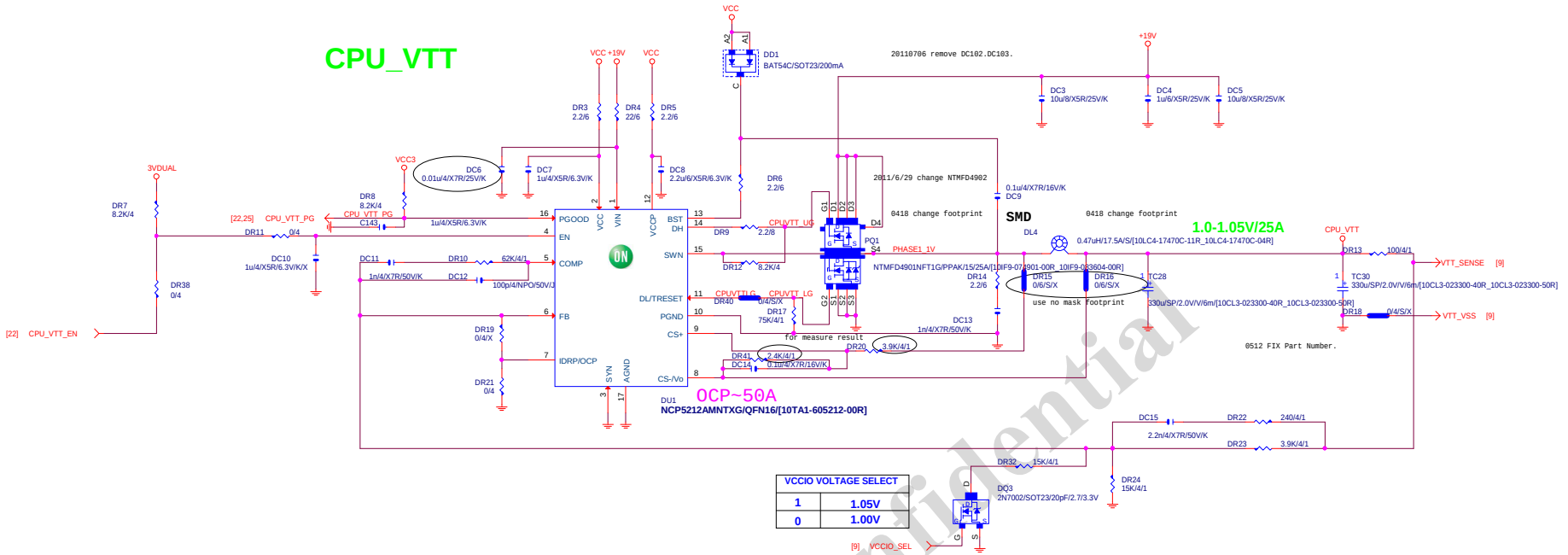
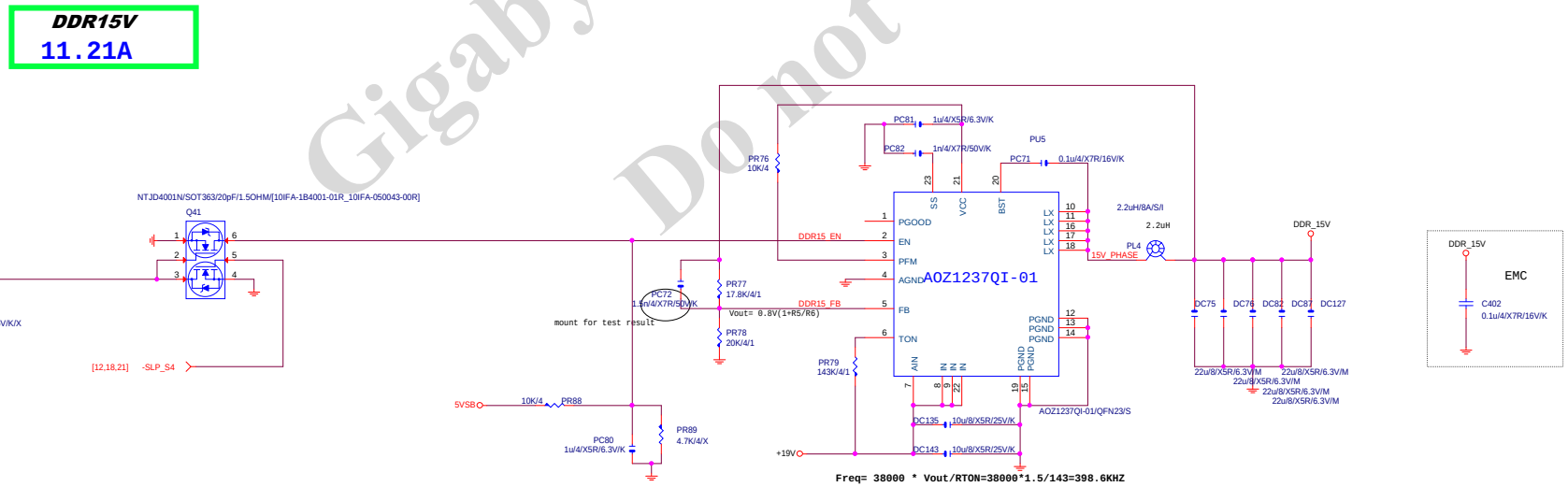
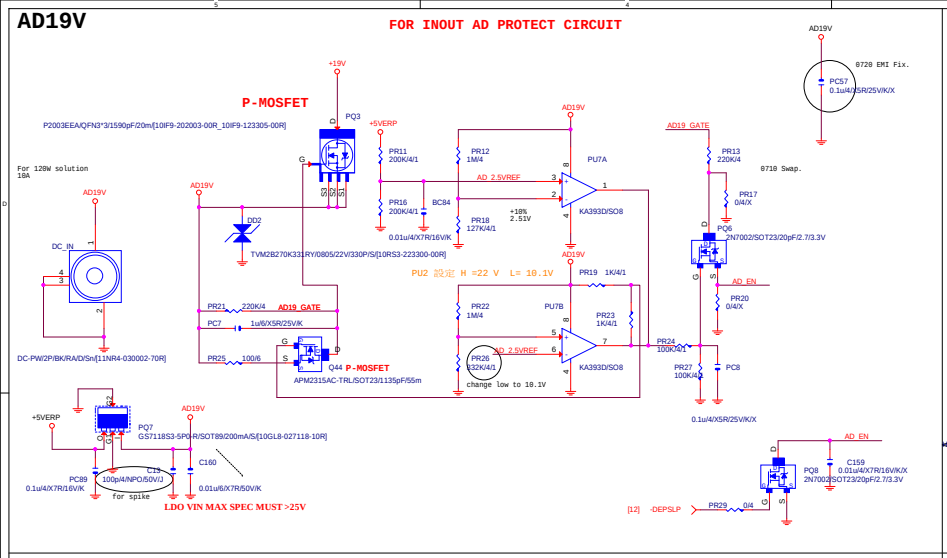
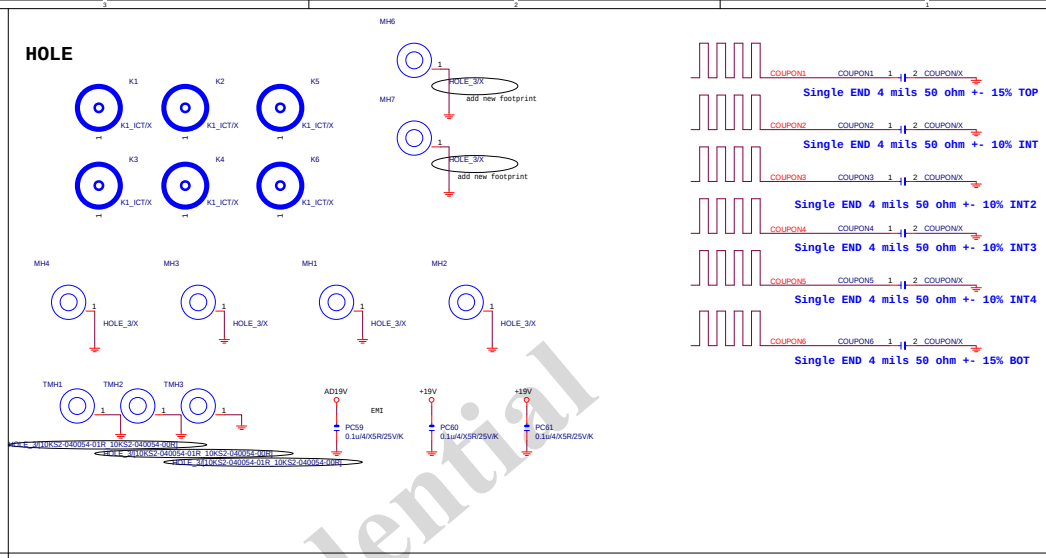


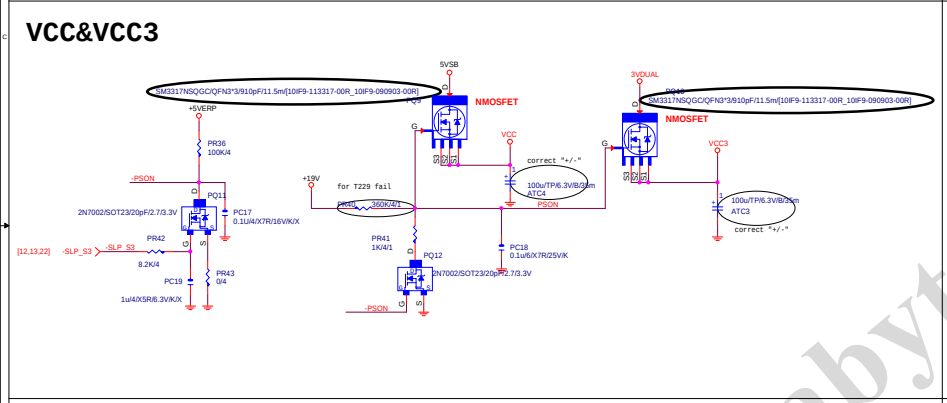
VCCIO VOLTAGE SELECT	
1	1.05V
0	1.00V

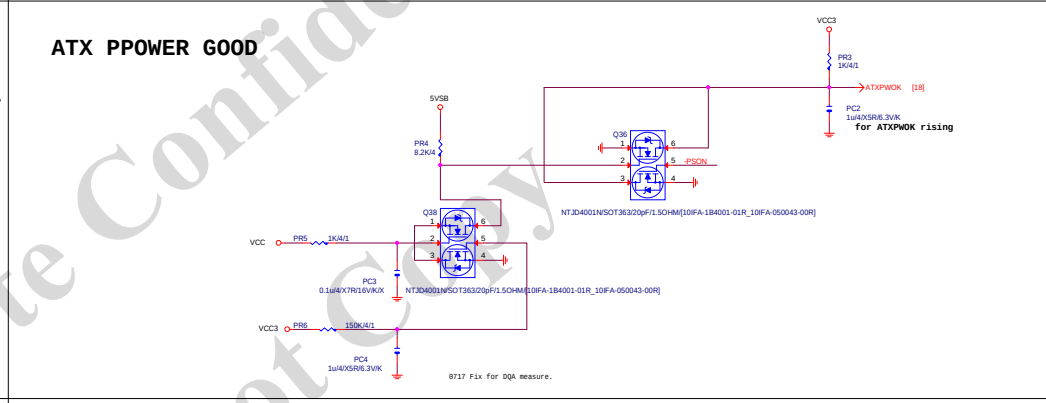


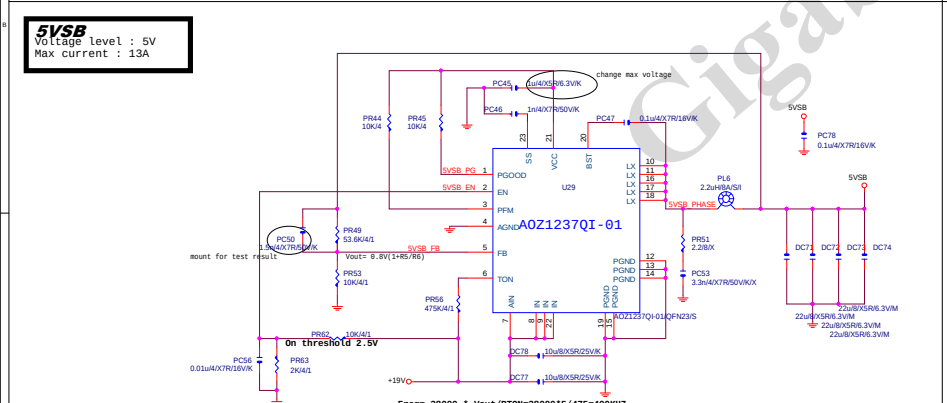
GIGABYTE TECHNOLOGIES , INC.	
Title	DISCRETE POWER
Size C	Document Number MRHM7AP-LF Rev 1.0
Date: Tuesday, March 26, 2013	Sheet 23 of 25

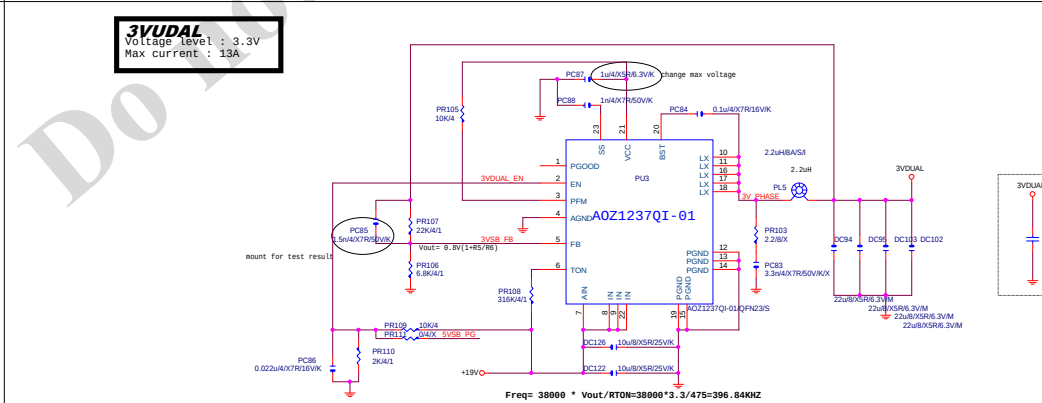












GIGABYTE TECHNOLOGIES , INC.			
Title: AD19V & VCC & VCC3			
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Vcore loadline=5.9 m ohm
Vaxg loadline=4.1 m ohm

NCP6131 VR12 POWER CKT - 1+1 PHASE

PWM ADDRESS		
RESISTOR VALUE	SVID ADDRESS FOR VCORE RAIL	SVID ADDRESS FOR V_GT RAIL
10K	0000	0001
25K	0010	0011
45K	0100	0101
70K	0110	0111
95K	1000	1001
125K	1010	1011
165K	1100	1101

BOOT VOLTAGE	
RESISTOR VALUE	BOOT VOLTAGE
10K	0V
25K	0.9V
45K	1V
70K	1.1V
95K	1.2V
125K	1.35V
165K	1.5V
VCC	SHUTDOWN

VCORE VBOOT SET AT 0 V

V_GT IMAX SET AT 18A

PWM ADDRESS

VCORE IMAX SET AT 33A

Refer Intel design guide

VCORE PORTION

V_GT PORTION

OC

BOTTOM PAD CONNECT TO GND Through 4 VIAs

PUT COLSE TO V_GT HOT SPOT

please close MOS

PUT COLSE TO VCORE HOT SPOT

Work F= 380Khz

Placement close to U2

17W CPU power spec :
Vcore: Iccmax = 33A ;TDC = 21.5A
Loadline = 2.9m ohm
Vboot = 0 A OCP = 50A

VGFX : Iccmax = 18A ;TDC = 12A
Loadline = 4.6m ohm
Vboot = 0 A; OCP = 29A

Please close to CPU

GIGABYTE TECHNOLOGIES , INC.

Title: VCORE&VGFX NCP6131

Size: Custom | Document Number: MRHM7AP-LF | Rev: 1.0

Date: Tuesday, March 26, 2013 | Sheet 25 of 25