

DV14 CP UMA+DIS Schematics Document

Arrandale

Intel IbeX Peak-M

2011-03-18

REV : X01

DY : Nopop Component

UMA: POP for UMA option

DIS: POP for DIS option

65 BOM : Nopop for 65 BOM option

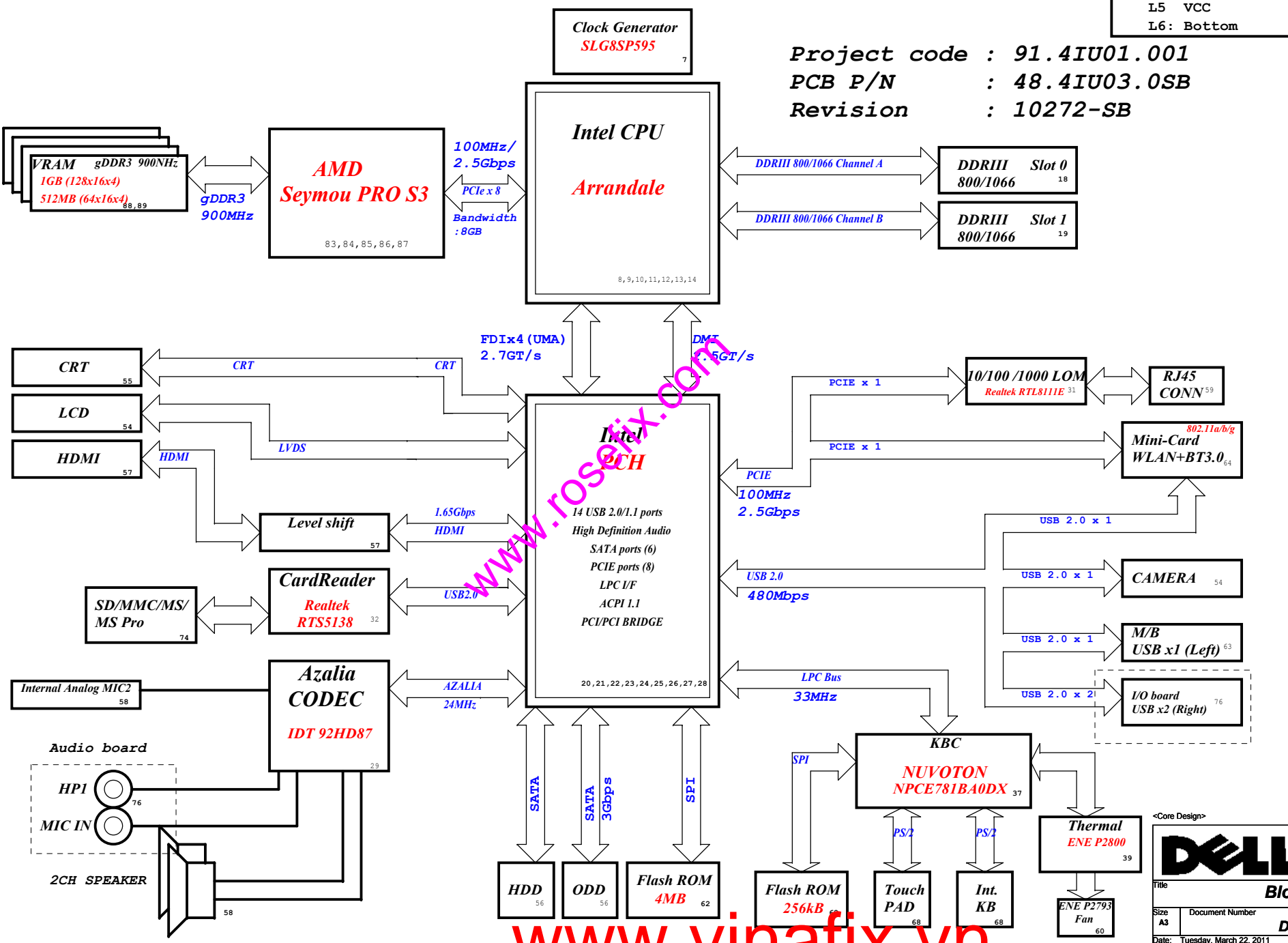
<Core Design>

DV14 CP Block Diagram (UMA/DIS Co-layout)

PCB LAYER	
L1:	Top
L2:	GND
L3:	Signal
L4:	Signal
L5:	VCC
L6:	Bottom

CPU DC/DC	
ISL62882 47,48	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE
SYSTEM DC/DC	
RT8237AGQW 49	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VTT
SYSTEM DC/DC	
TPS51123RGER 46	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW +15V_ALW
SYSTEM DC/DC	
RT8207LGQW 50	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_REF
SYSTEM DC/DC	
G9731F11U 93	
INPUTS	OUTPUTS
+1.5V_SUS	+1V_GPU_PCIE
VGA	
RT8208BGQW 92	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_GFX_CORE
MAXIM CHARGER	
BQ24707RGRG4 45	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC
SYSTEM DC/DC	
RT9025-25PSP 51	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN
SYSTEM DC/DC	
RT9025-25PSP 93	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN_GPU
SYSTEM DC/DC	
Switches 42	
INPUTS	OUTPUTS
+1.5V_SUS +5V_ALW +3.3V_ALW	+1.5V_RUN +5V_RUN +3.3V_RUN

Project code : 91.4IU01.001
PCB P/N : 48.4IU03.0SB
Revision : 10272-SB



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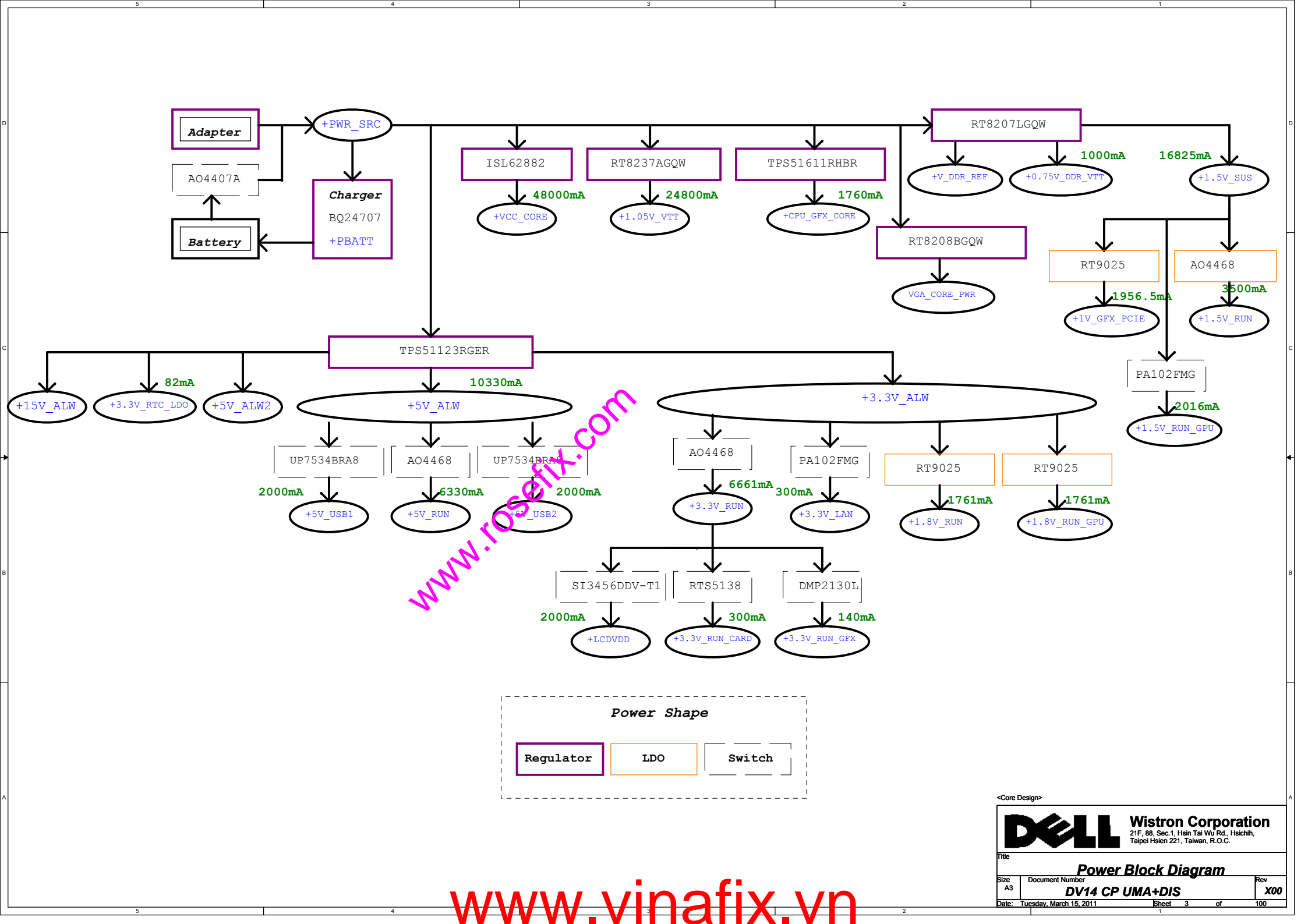
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Title: **Block Diagram**

Size: A3 Document Number: **DV14 CP UMA+DIS** Rev: **X00**

Date: Tuesday, March 22, 2011 Sheet 2 of 100

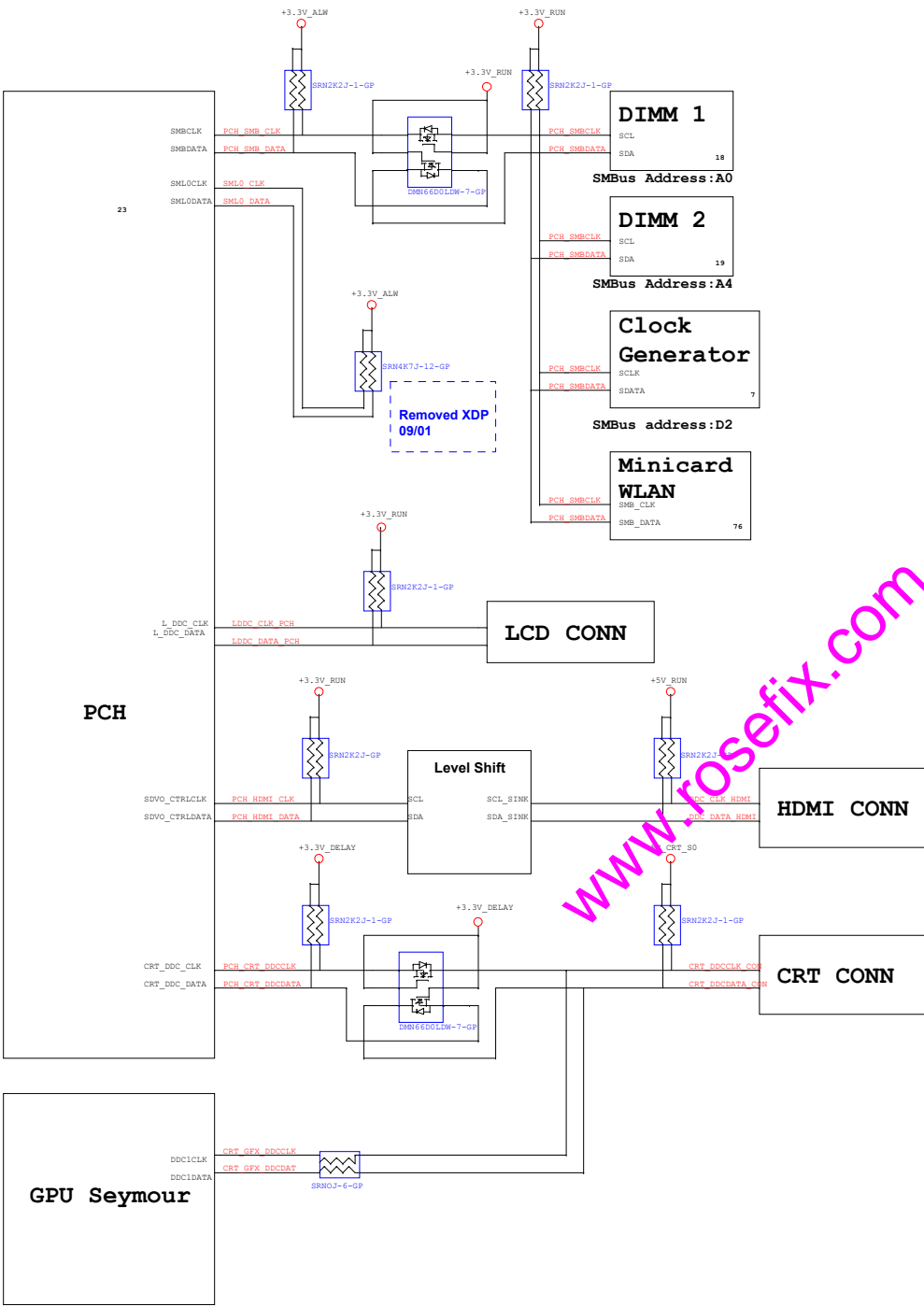


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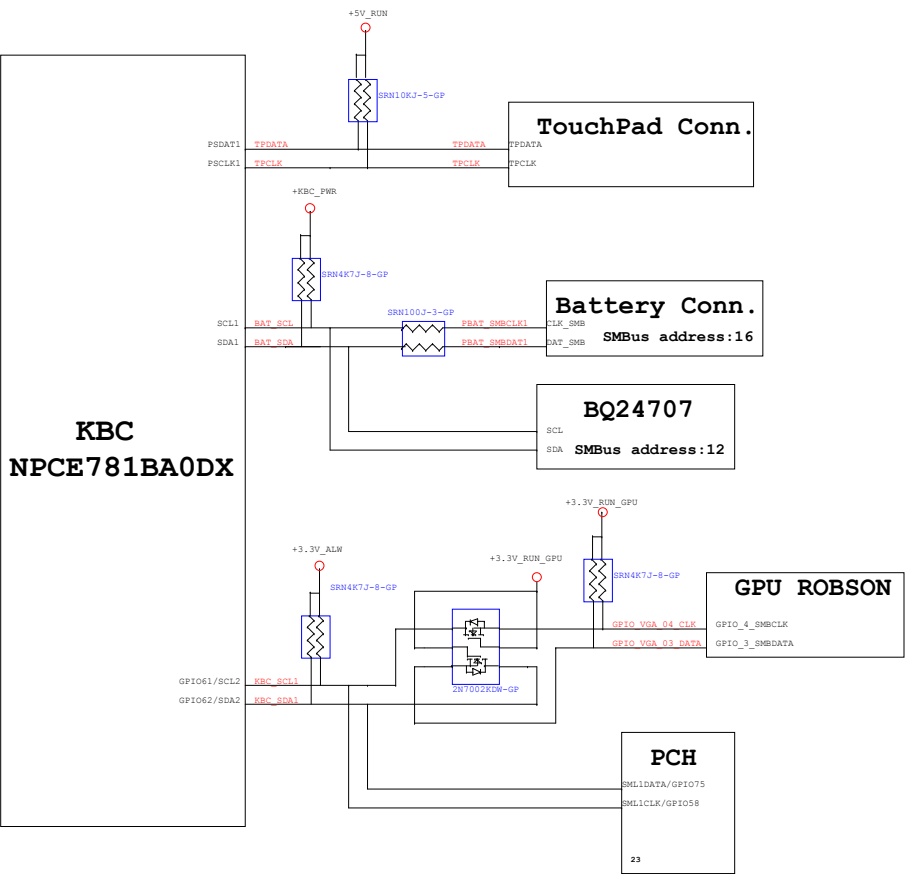
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DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Power Block Diagram			
Size A3	Document Number DV14 CP UMA+DIS	Rev X00	
Date: Tuesday, March 15, 2011		Sheet 3 of 100	

PCH SMBus Block Diagram



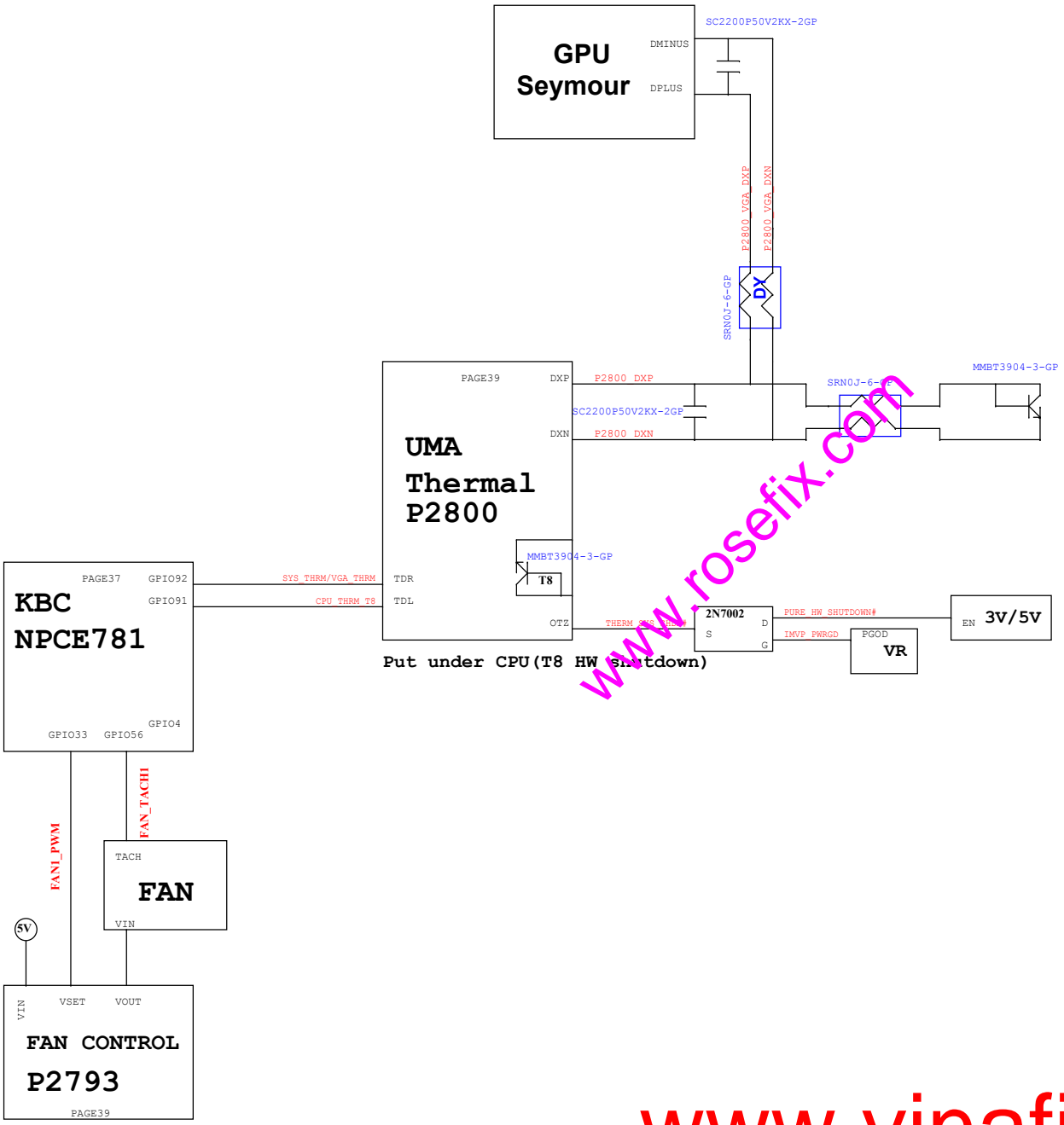
KBC SMBus Block Diagram



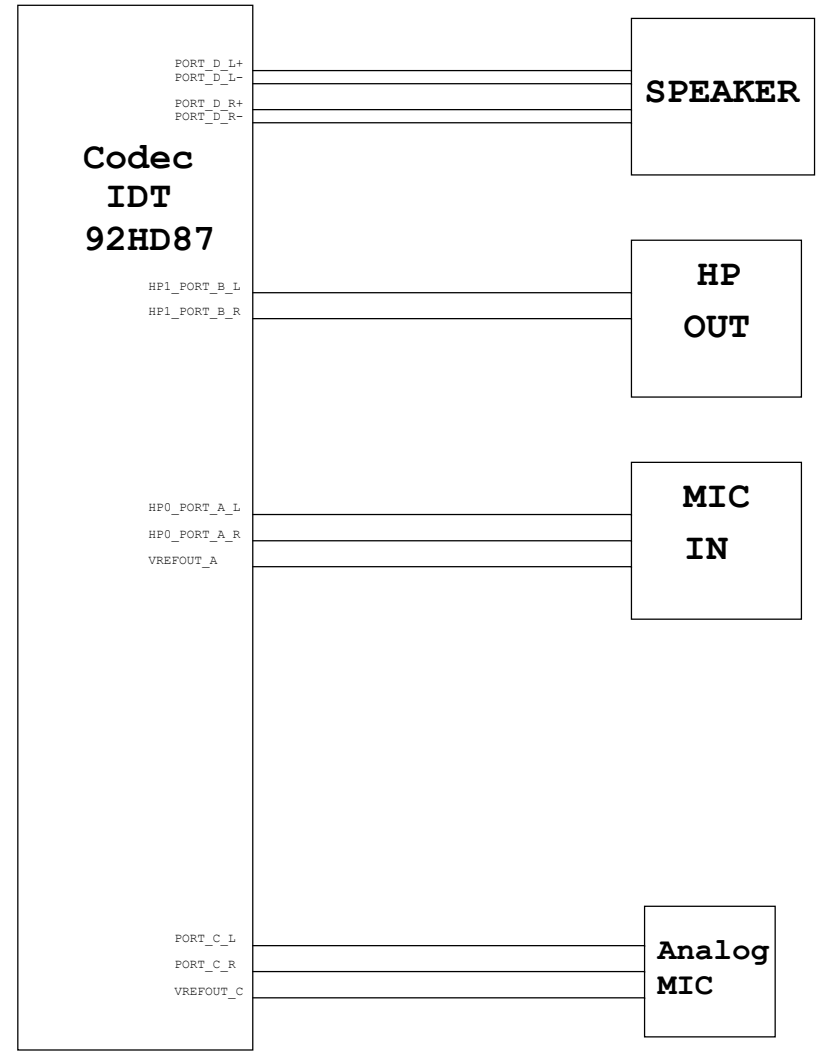
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Thermal Block Diagram



Audio Block Diagram



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PCH Strapping

Calpella Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-k weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-k weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#/GPIO51	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-k pull-down resistor. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-k pull-down resistor.
GNT2#/GPIO53	Default = Internal pull-up. Low (0) = Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-k pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-k weak pull-up resistor. Disable iTPM: Connect to GND with 8.2-k pull-down resistor.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-k pull-up resistor. Disable Danbury: Connect to ground with 4.7-k weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN#/GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1): Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIE Routing

LANE2	MiniCard WLAN
LANE3	LAN

USB Table


USB	
Pair	Device
0	X
1	USB1
2	USB2
3	USB3
4	X
5	X
6	X
7	X
8	X
9	WLAN for BLUETOOTH
10	CARD READER
11	CAMERA
12	X
13	X

Processor Strapping

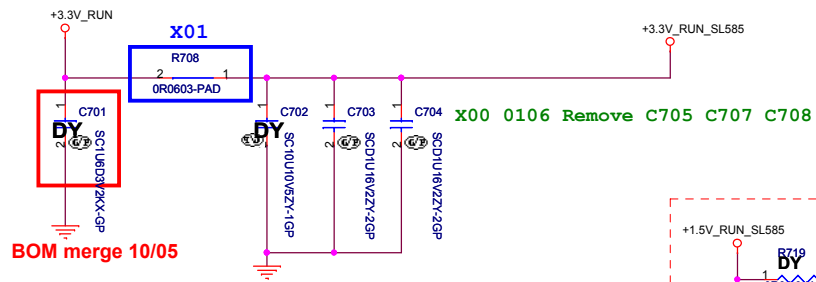
Calpella Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksville samples.	Clarksville (only for early samples pre-ES1) - Connect to GND with 3.01k Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

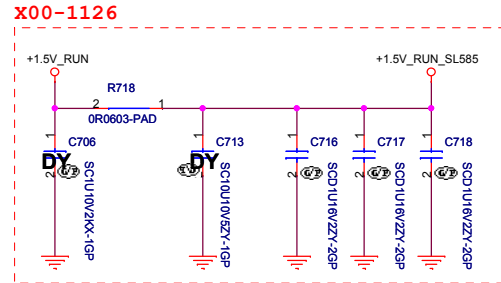
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Size A3	Document Number DV14 CP UMA+DIS	Rev X00	
Date: Friday, January 14, 2011	Sheet 6	of	100

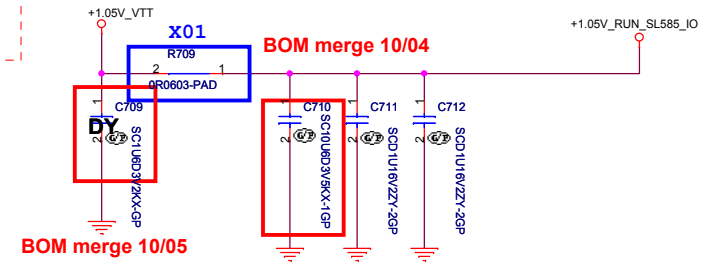
SSID = CLOCK



BOM merge 10/05



Note: 595 stuff R718, 585 stuff R719

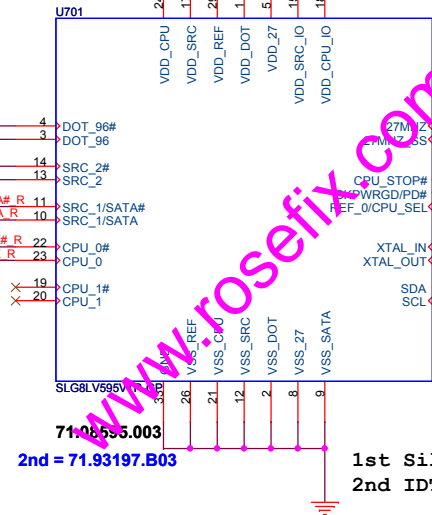
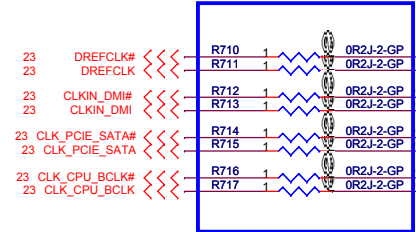


BOM merge 10/05

BOM merge 10/04

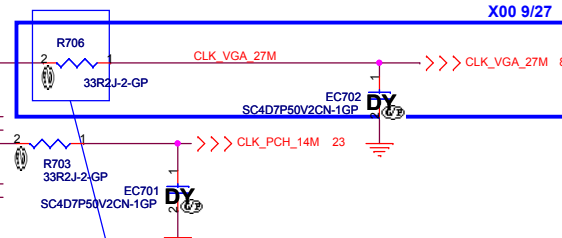


X00 09/23



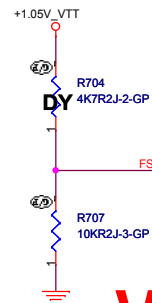
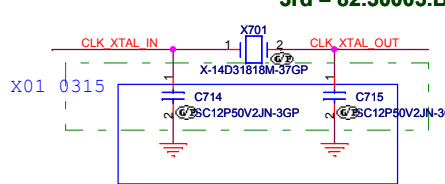
1st Silego : 71.08595.003
2nd = 71.93197.B03

1st Silego : 71.08595.003
2nd IDT : 71.93197.B03

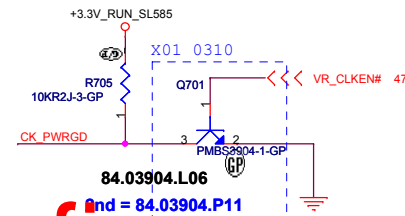


X01 0316
if U701 is 71.08595.003, R706 install 33ohm (63.33034.1DL);
if U701 is 2nd=71.93197.B03, R706 install 22ohm(63.22034.1DL).

82.30005.901
2nd = 82.30005.A51
3rd = 82.30005.B81



FSC	0	1
SPEED	133MHz (Default)	100MHz



84.03904.L06
2nd = 84.03904.P11

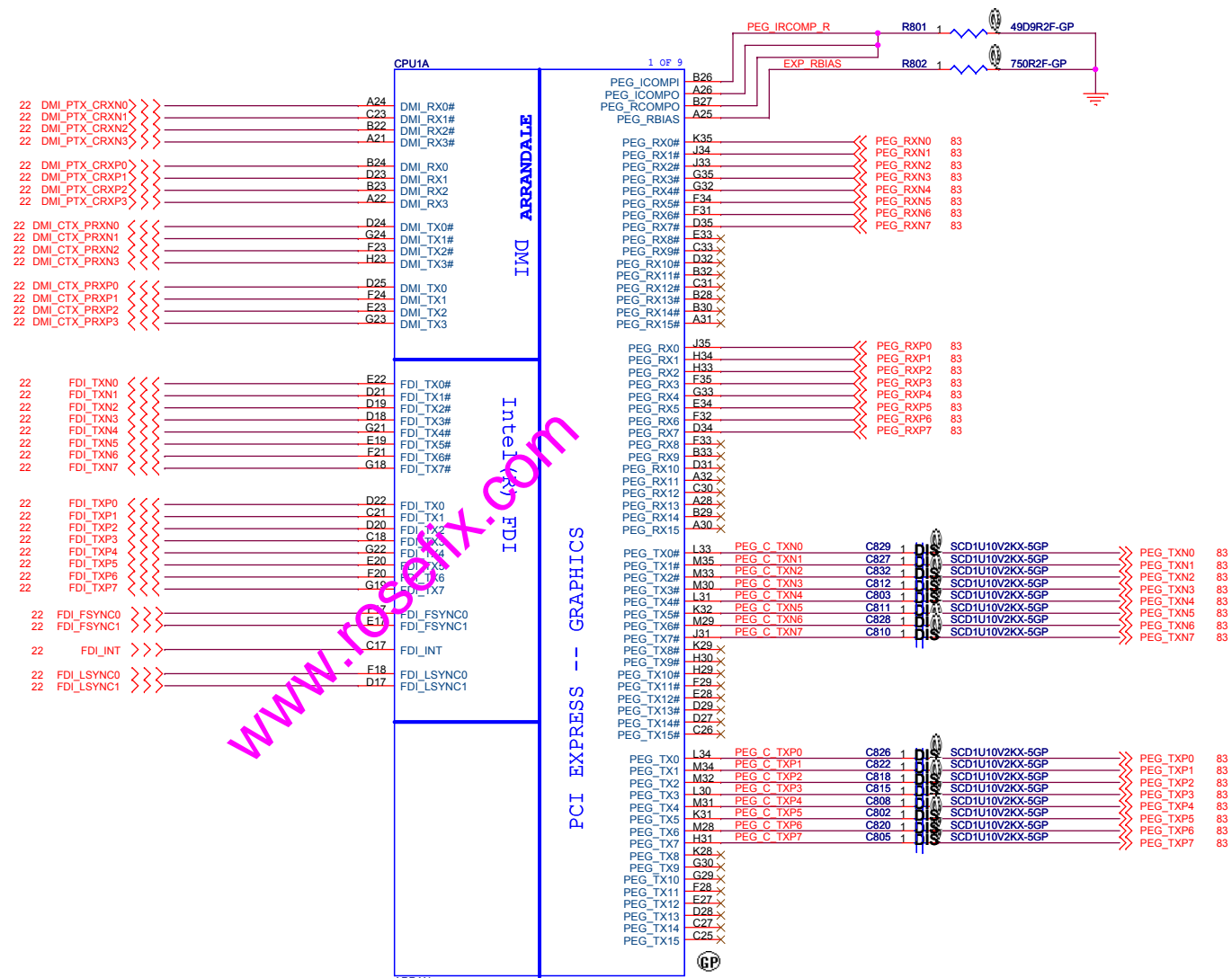
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Title: **Clock Generator SLG8SP585**

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SSID = CPU



62.10055.321

2nd = 62.10040.821

3rd = 62.10055.551

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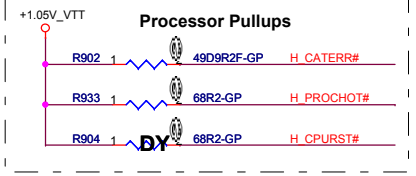
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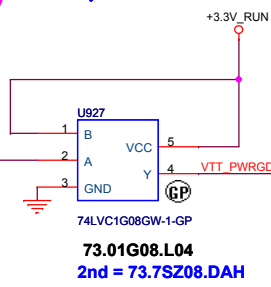
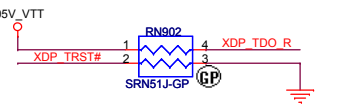
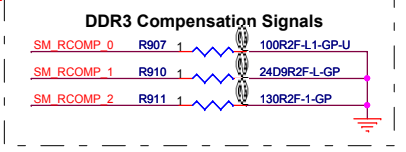
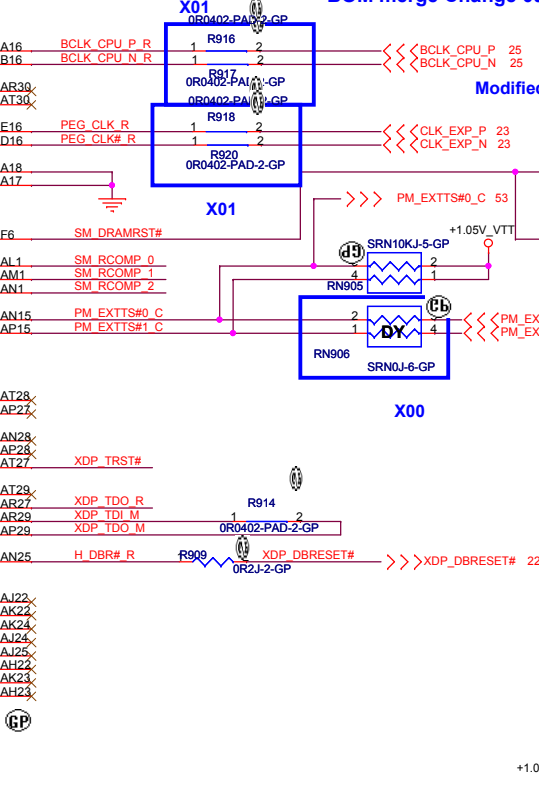
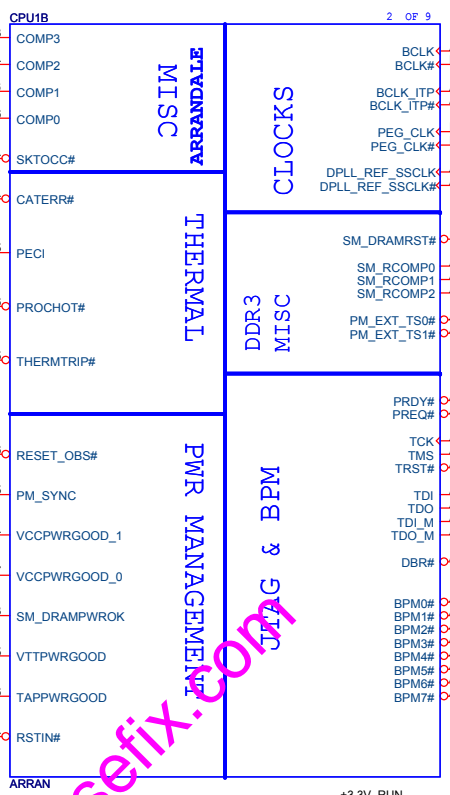
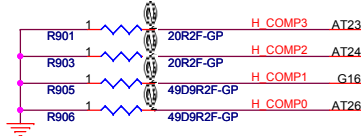
Title: **CPU (PCIE/DMI/FDI)**

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SSID = CPU



Processor Compensation Signals



	R919	R937	R977
S3 circuit	DY	0.75k	1.6k
Normal	1.27k	3k	DY

Remove XDP 8/22

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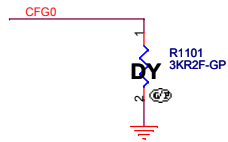
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Title: **CPU (THERMAL/CLOCK/PM)**

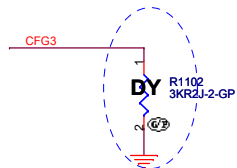
Size A3 Document Number: **DV14 CP UMA+DIS** Rev: **X00**

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SSID = CPU

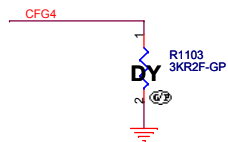


PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

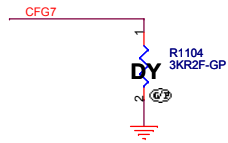


CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

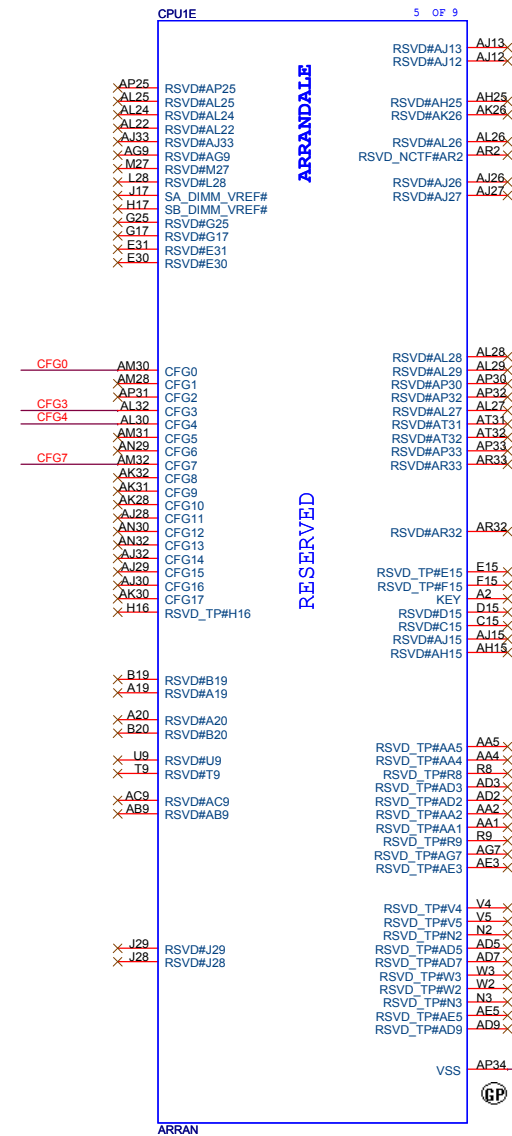
Change to Normal operation
20100202



CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port



CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.



VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

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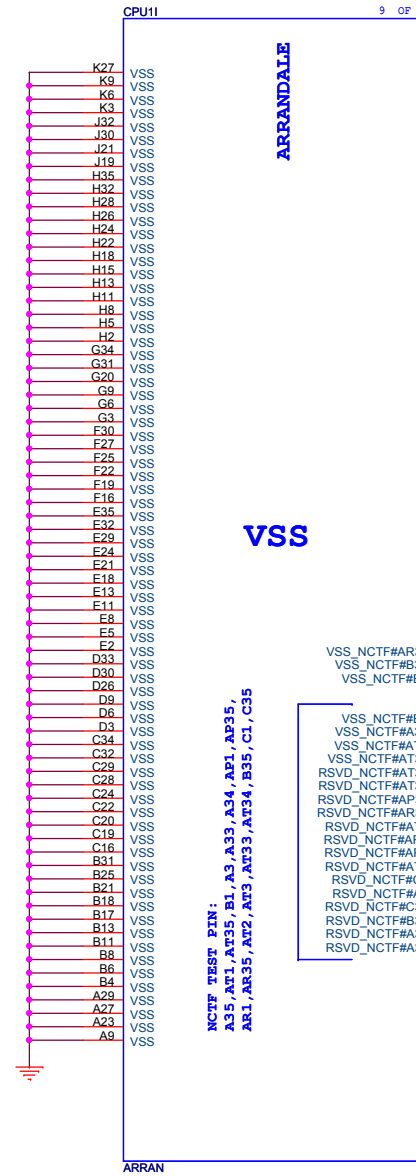
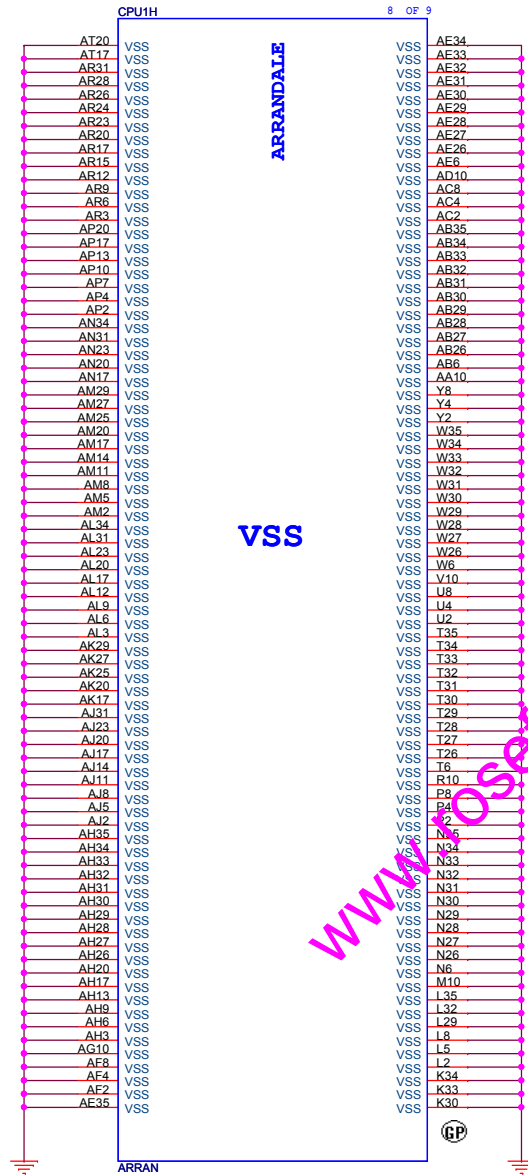
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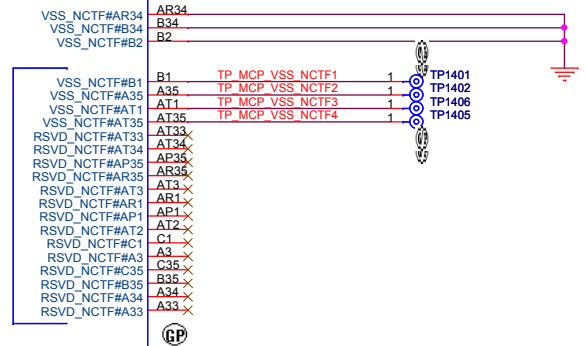
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SSID = CPU



NCTF TEST PIN:
 A35, AT1, AT35, B1, A3, A33, A34, AP1, AP35,
 AR1, AR35, AT2, AT3, AT33, AT34, B35, C1, C35



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Title: **CPU (VSS)**

Size: A3	Document Number: DV14 CP UMA+DIS	Rev: X00
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Title		
Reserved		
Size A3	Document Number DV14 CP UMA+DIS	Rev X00
Date: Thursday, January 06, 2011	Sheet 15	of 100

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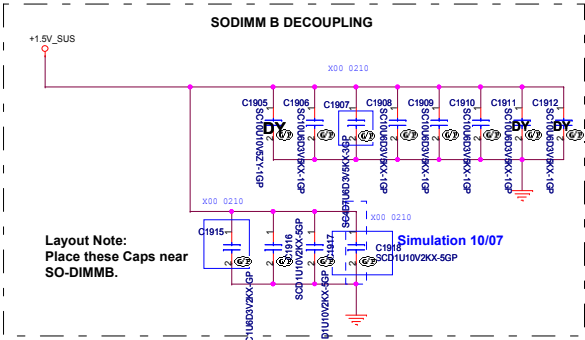
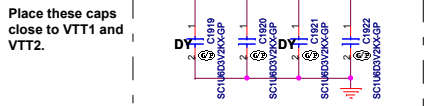
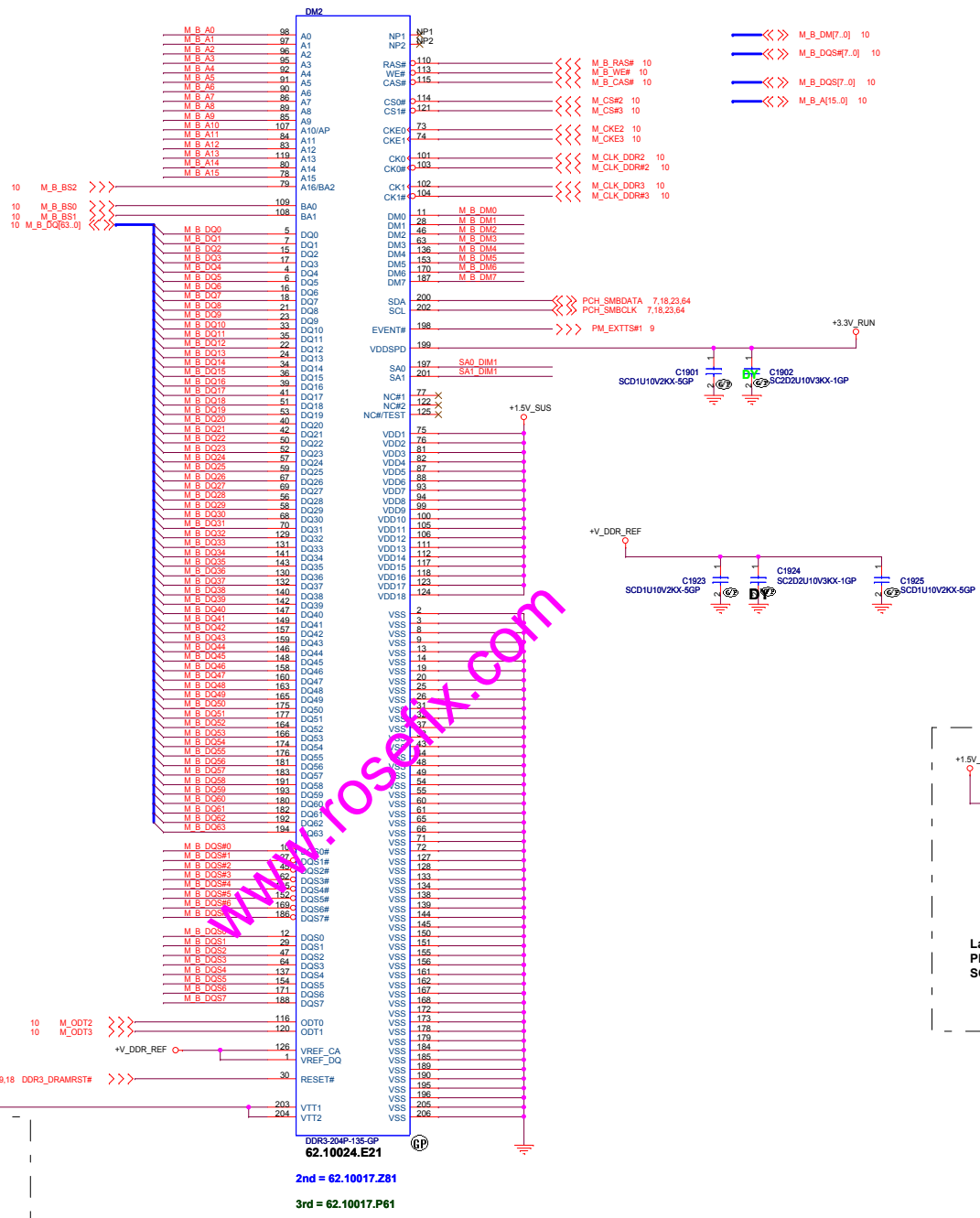
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Reserved		
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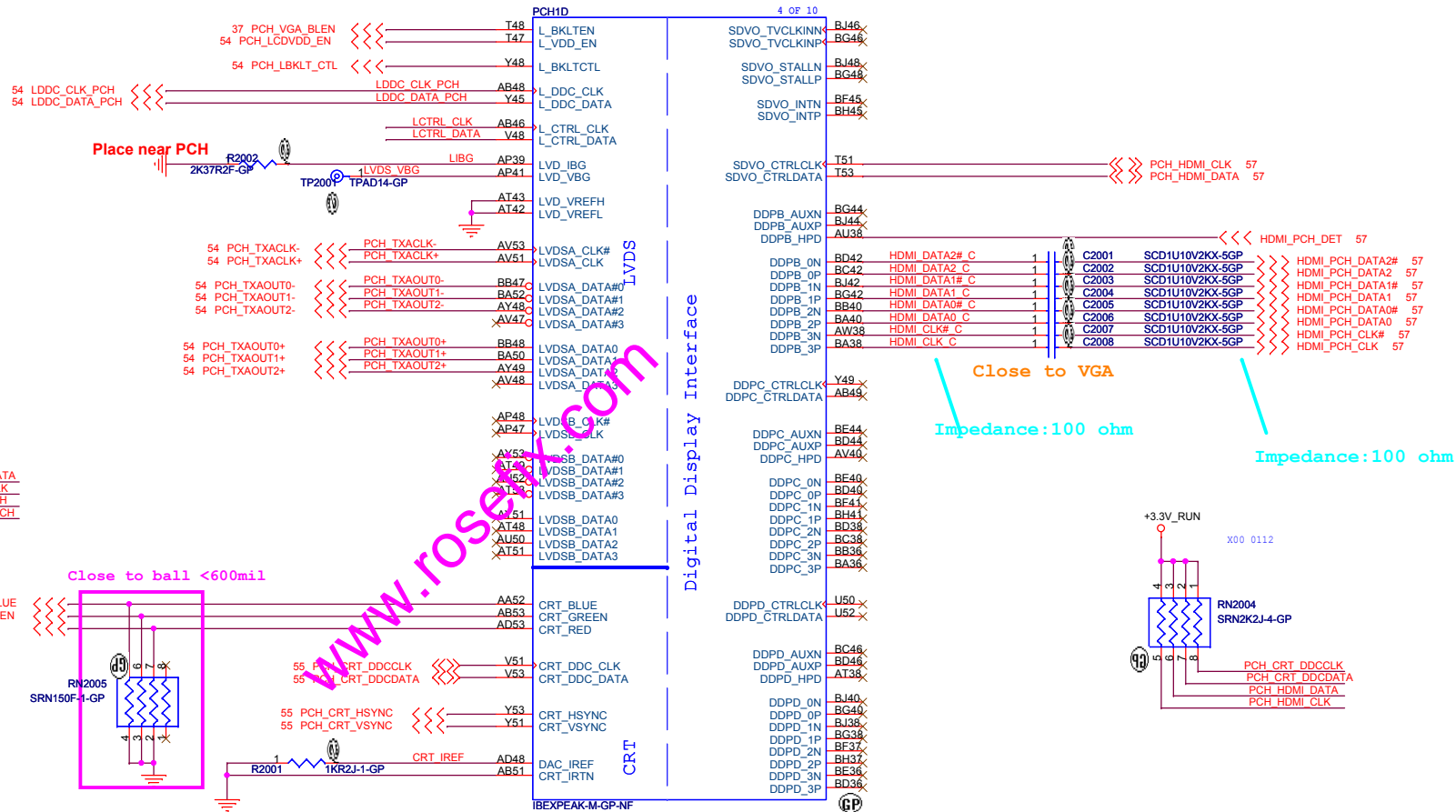
SSID = MEMORY



Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

SSID = PCH



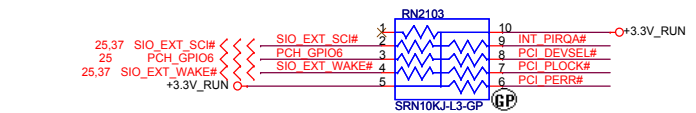
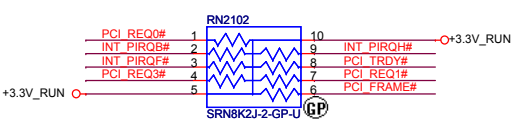
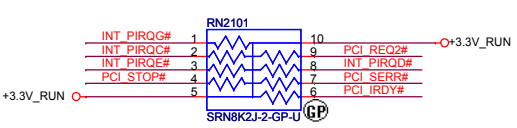
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Title PCH (LVDS/CRT/DDI)		
Size A3	Document Number DV14 CP UMA+DIS	Rev X00
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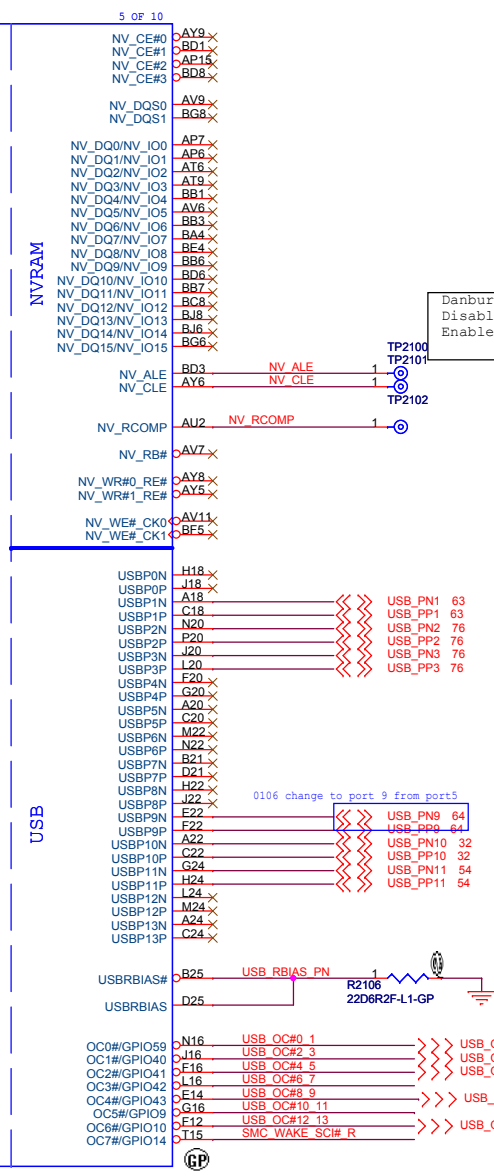
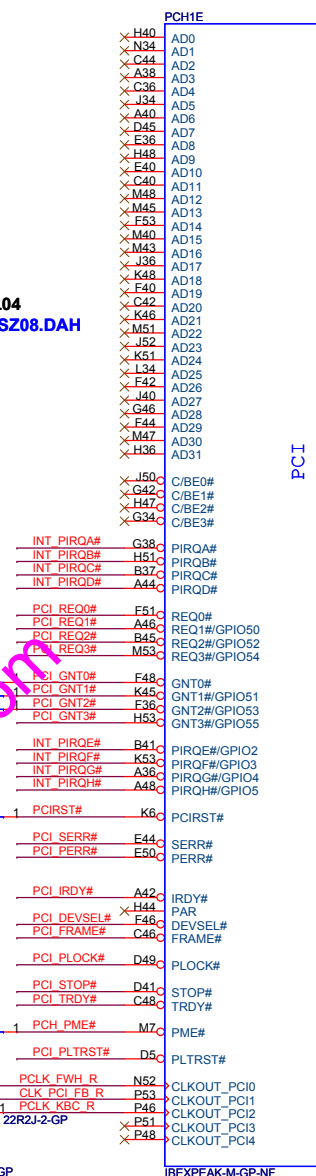
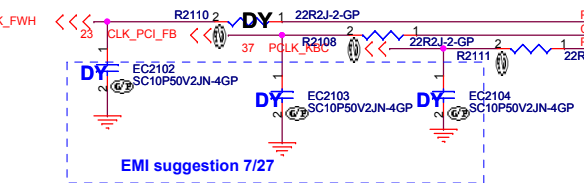
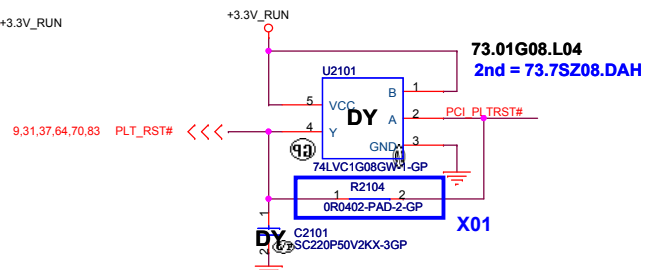
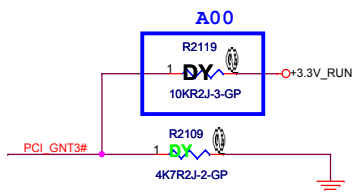
SSID = PCH



BOOT BIOS Strap		
PCI_GNT#1	PCI_GNT#0	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI (Default)

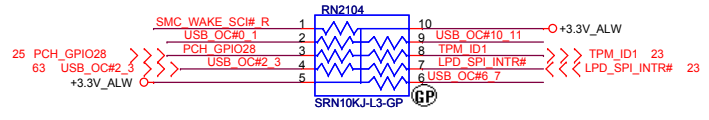
A16 swap override Strap/Top-Block Swap Override jumper

PCI_GNT#3 Low = A16 swap override/Top-Block Swap Override enabled High = Default



Danbury Technology:
Disabled when Low.
Enable when High.

USB	
Pair	Device
0	X
1	USB1
2	USB2
3	USB3
4	X
5	X
6	X
7	X
8	X
9	WLAN for BLUETOOTH
10	CARD READER
11	CAMERA
12	X
13	X



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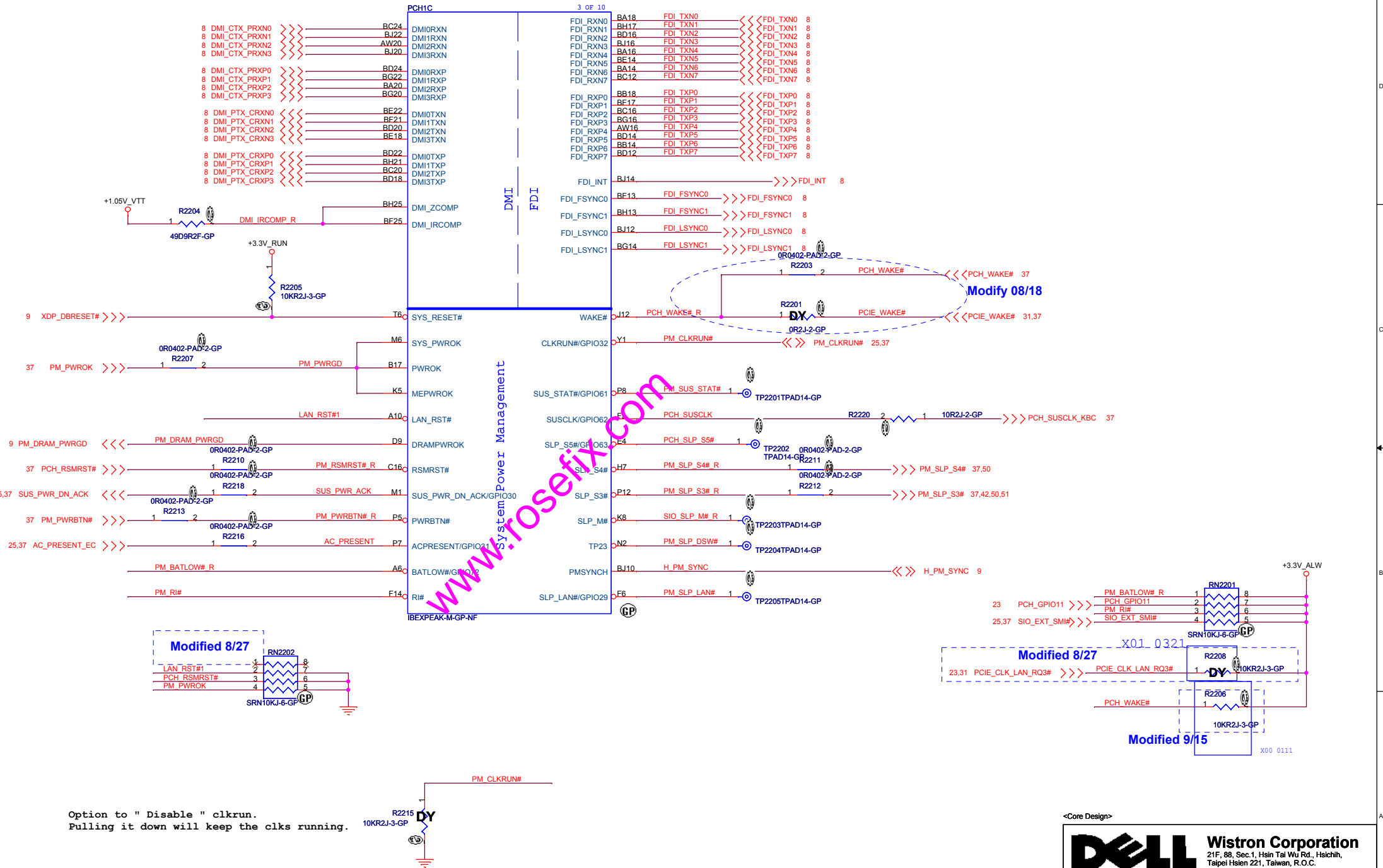
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Title: **PCH (PCI/USB/NVRAM)**

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SSID = PCH



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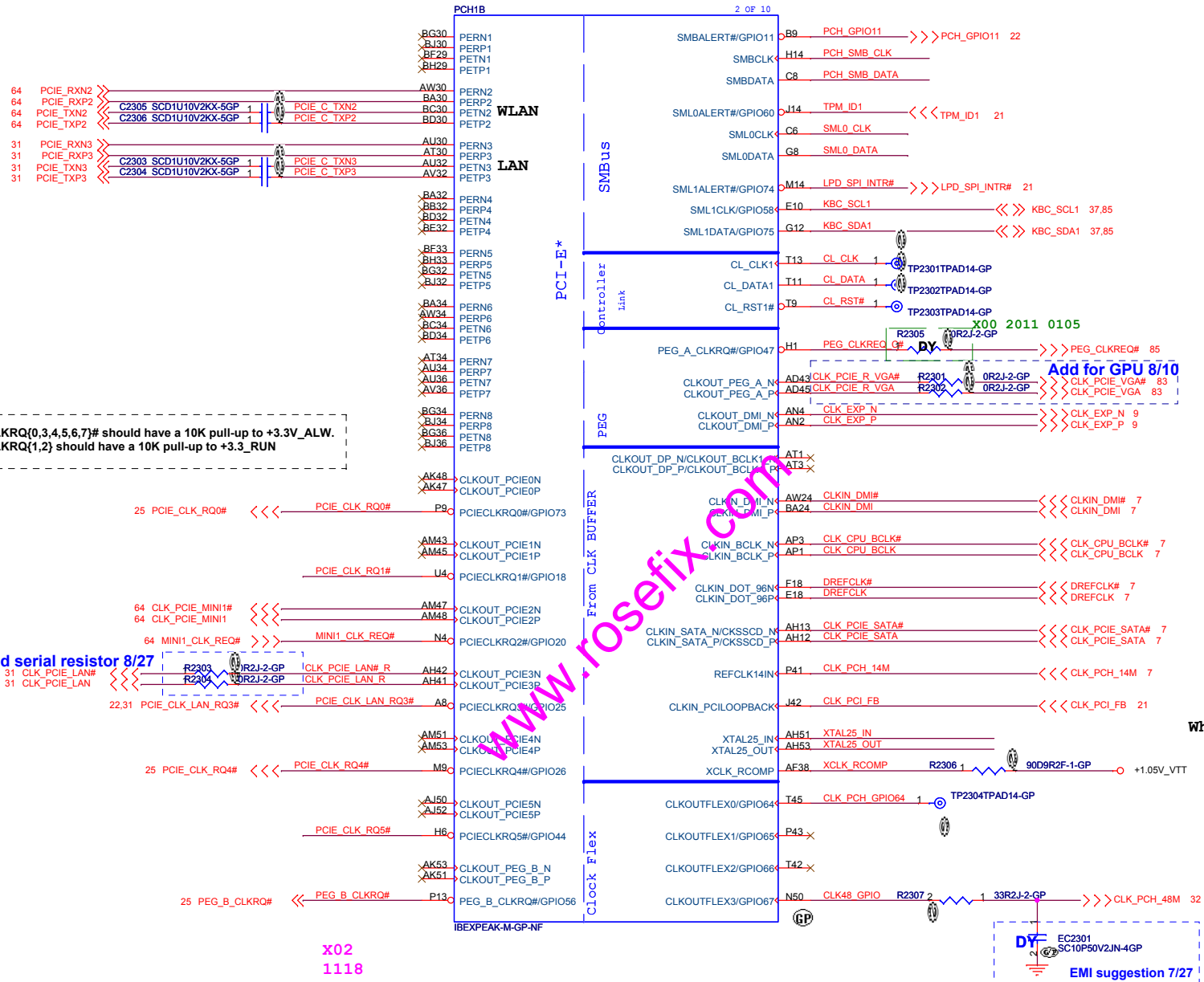
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (DM I/FDI/PM)**

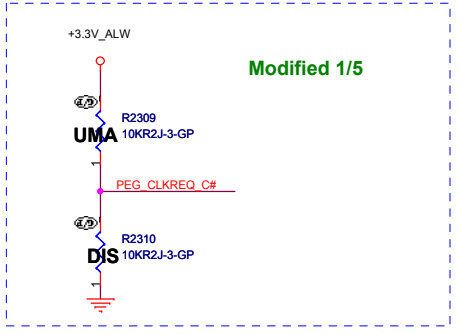
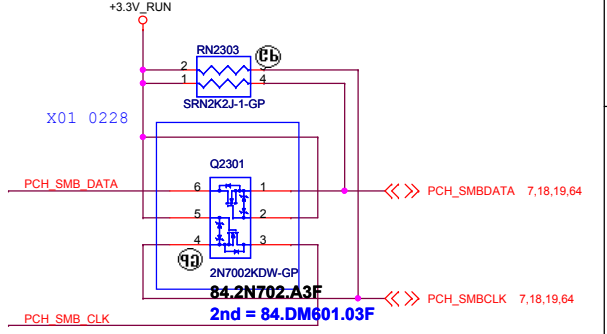
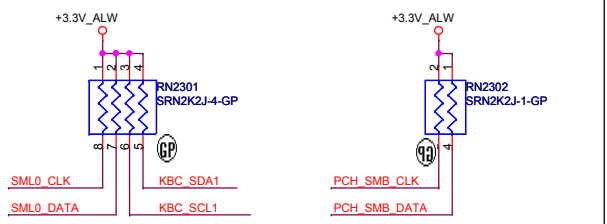
Size A3	Document Number DV14 CP UMA+DIS	Rev X00
Date: Wednesday, March 23, 2011		Sheet 22 of 100

SSID = PCH

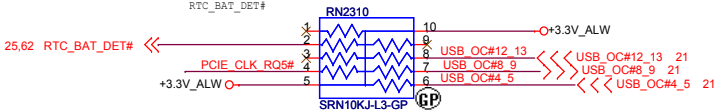
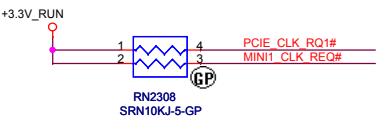
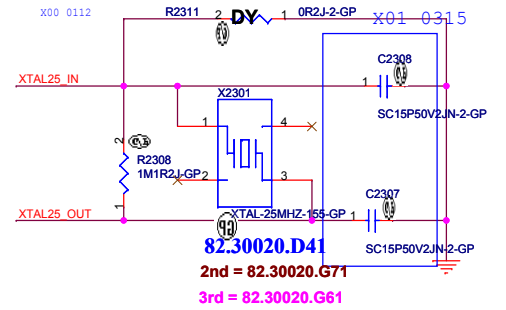


PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3.3V_ALW.
 PCIECLKRQ{1,2} should have a 10K pull-up to +3.3_RUN

Add serial resistor 8/27



When HDMI parts stuffed, the R2311 need DY.



Core Design

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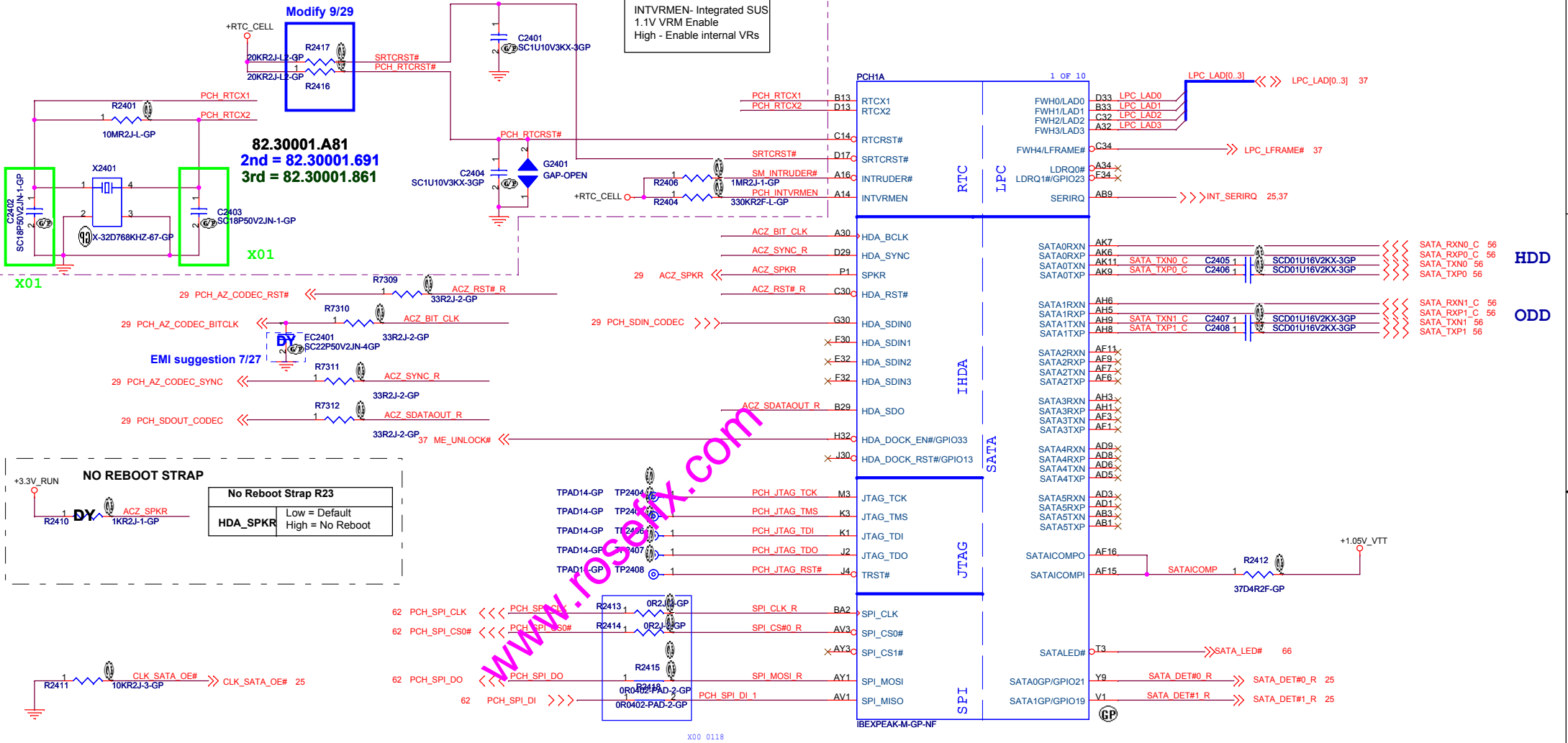
Title: **PCH (PCI-E/SMBUS/CLOCK/CL)**

Size: A3, Document Number: **DV14 CP UMA+DIS**, Rev: **X00**

Date: Wednesday, March 23, 2011, Sheet 23 of 100

SSID = RTC

SSID = PCH



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<Core Design>

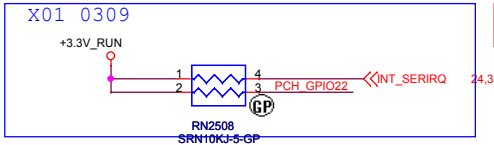
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (SPI/RTC/LPC/SATA/IHDA)**

Size: A3 Document Number: **DV14 CP UMA+DIS** Rev: **X00**

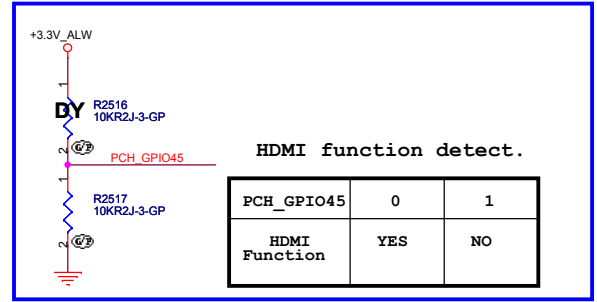
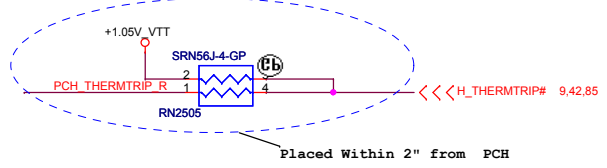
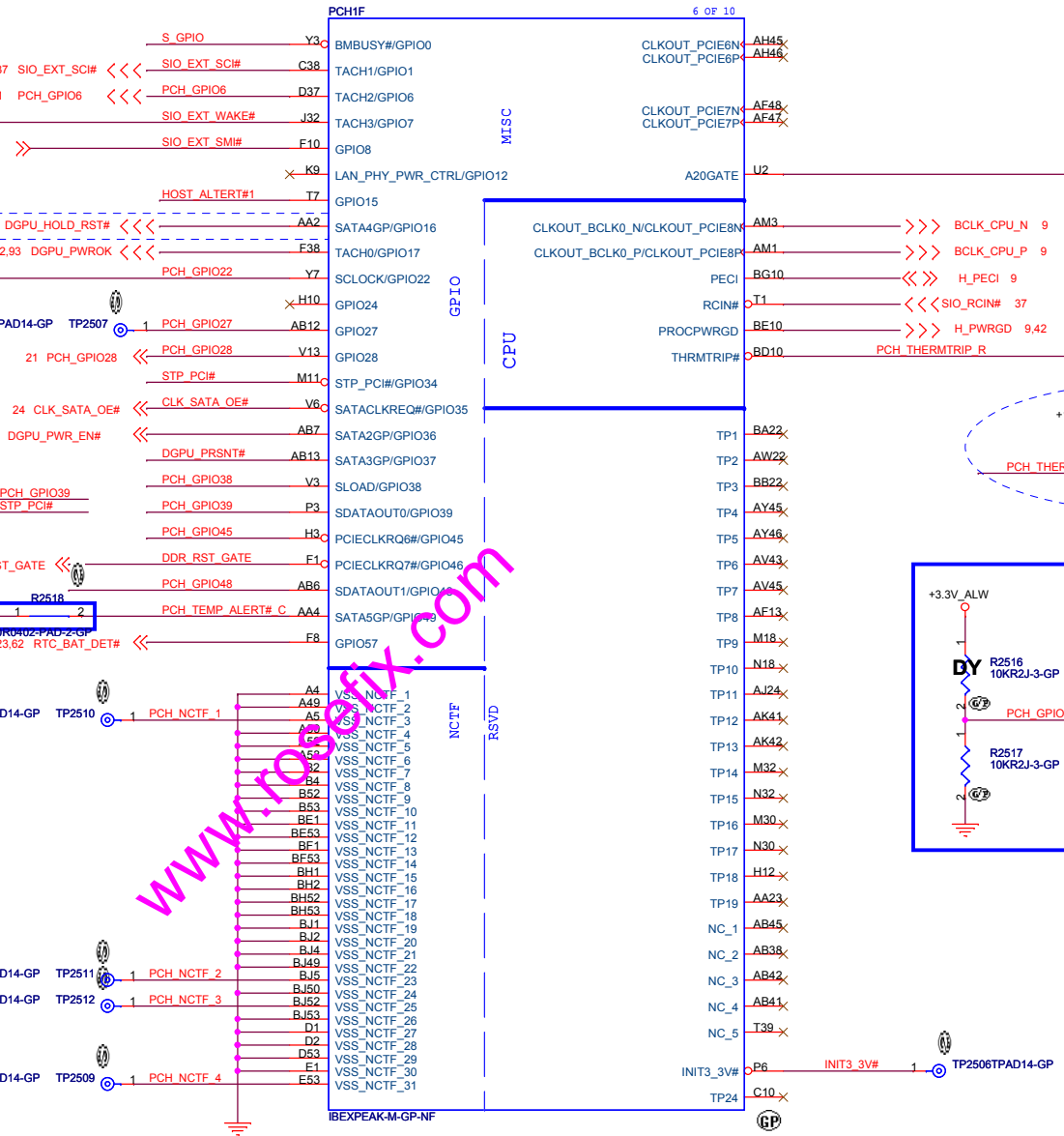
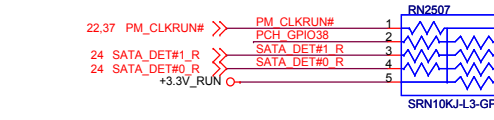
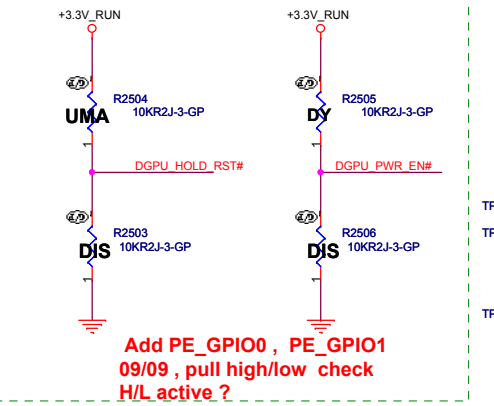
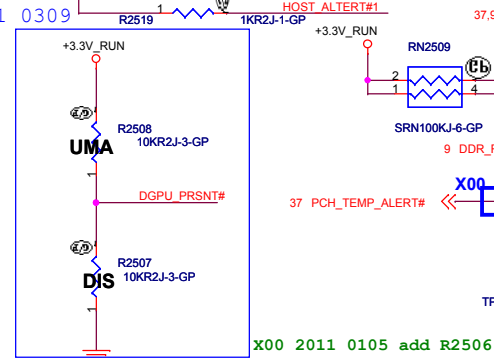
Date: Wednesday, March 23, 2011 Sheet 24 of 100

SSID = PCH

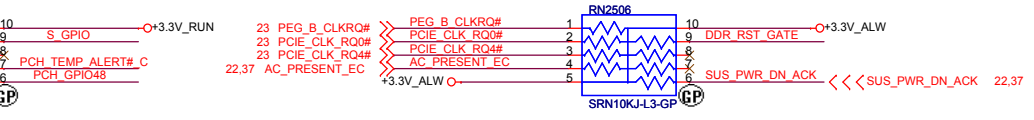


Change NET DGPU_HOLD_RST# to PE_GPIO0 to reset GPU ,09/23

Remove GPIO12,GPIO24 Pull high 09/10



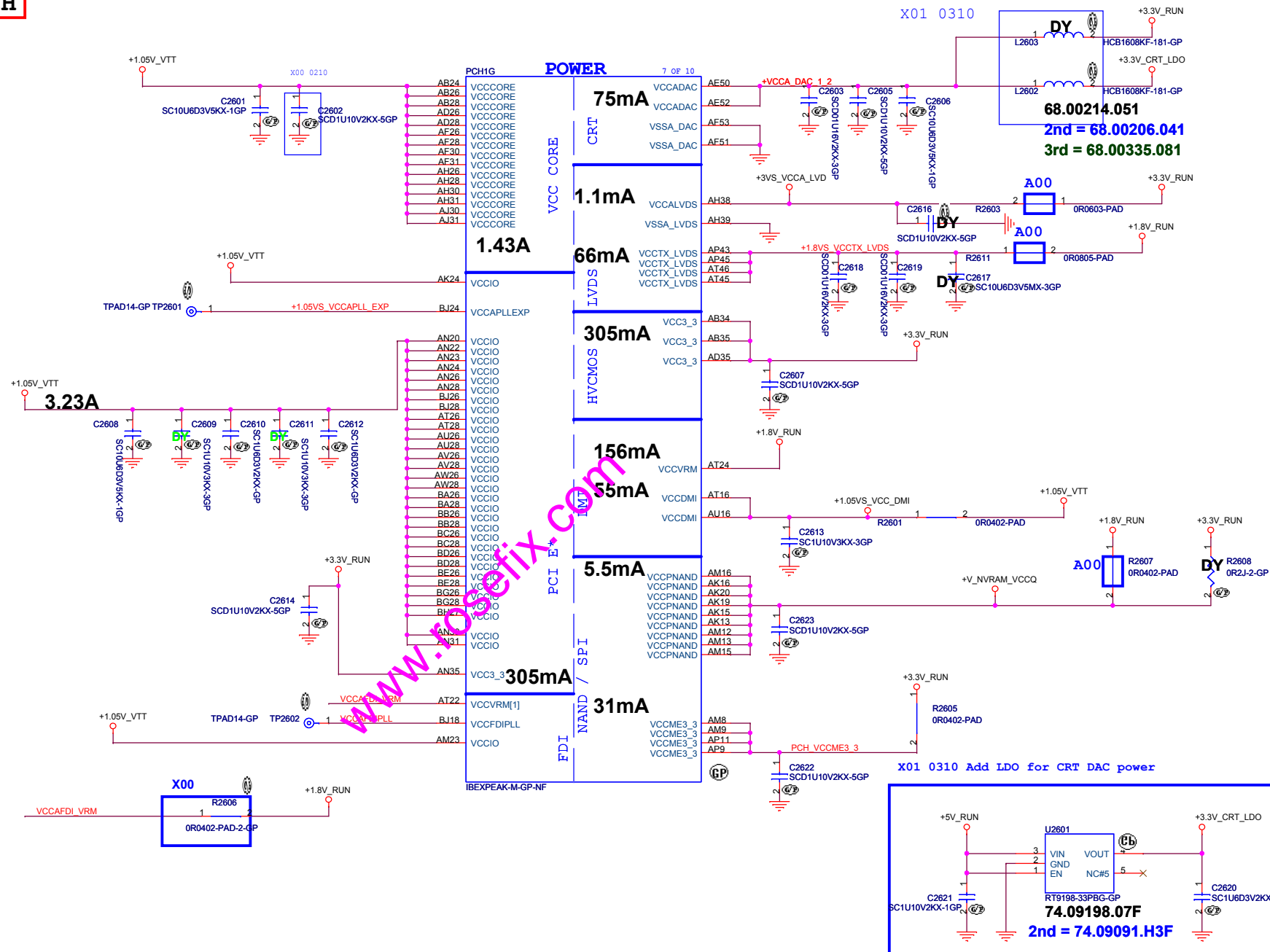
HDMI function detect table with columns for PCH_GPIO45 (0, 1) and rows for HDMI Function (YES, NO).



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Dell Wistron Corporation logo and document information including Title (PCH (GPIO/CPU)), Size (A3), and Date (Wednesday, March 23, 2011).

SSID = PCH



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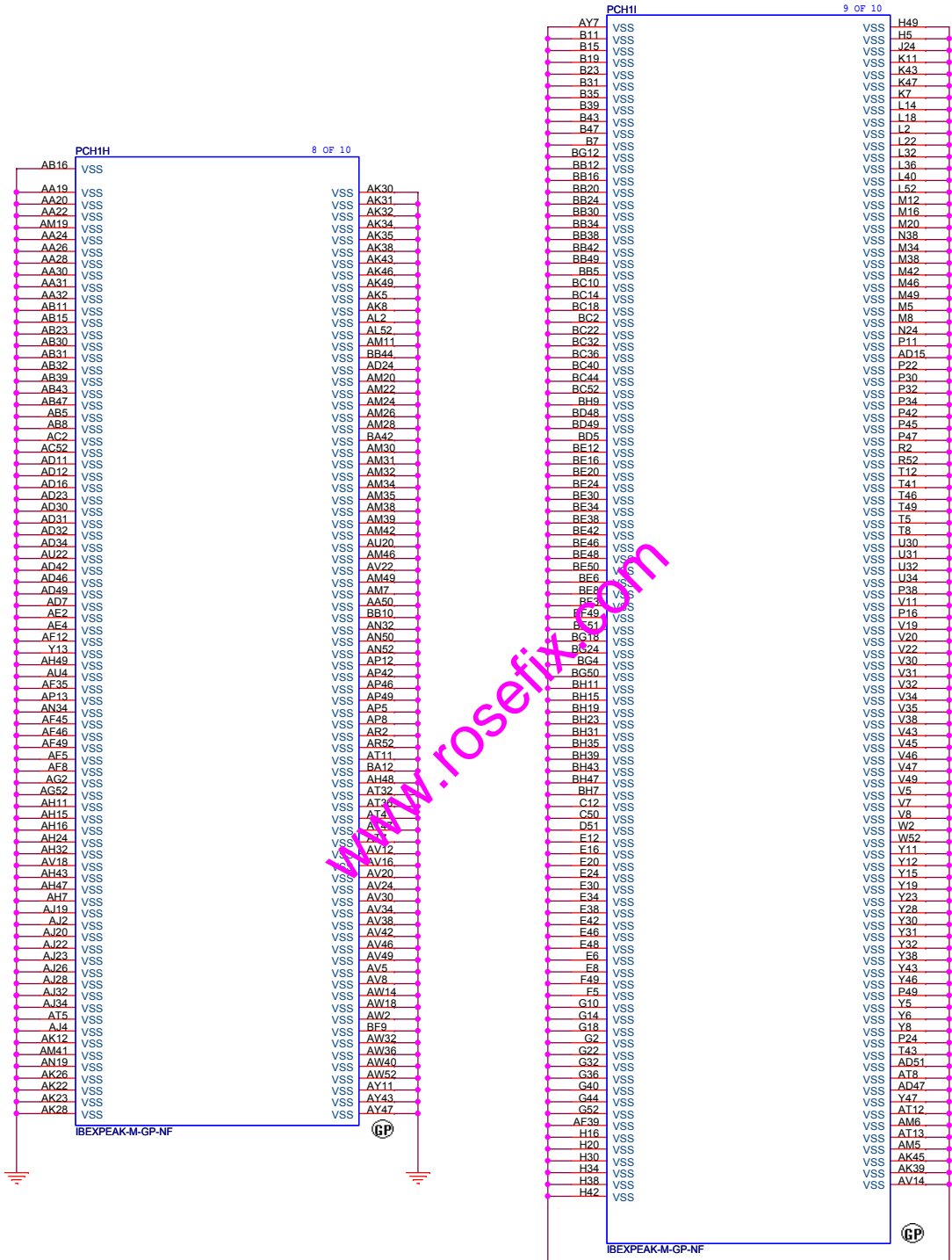
<Core Design>

Wistron Corporation
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Title: **PCH (POWER1)**

Size: A3	Document Number: DV14 CP UMA+DIS	Rev: X00
Date: Tuesday, March 22, 2011	Sheet: 26 of 100	

SSID = PCH



<Core Design>

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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (VSS)**


Size: A3	Document Number: DV14 CP UMA+DIS	Rev: X00
Date: Tuesday, January 25, 2011	Sheet: 28	of 100

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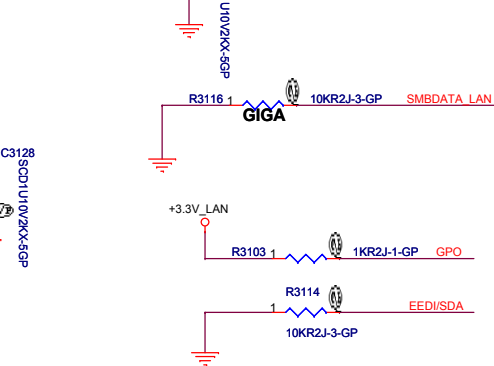
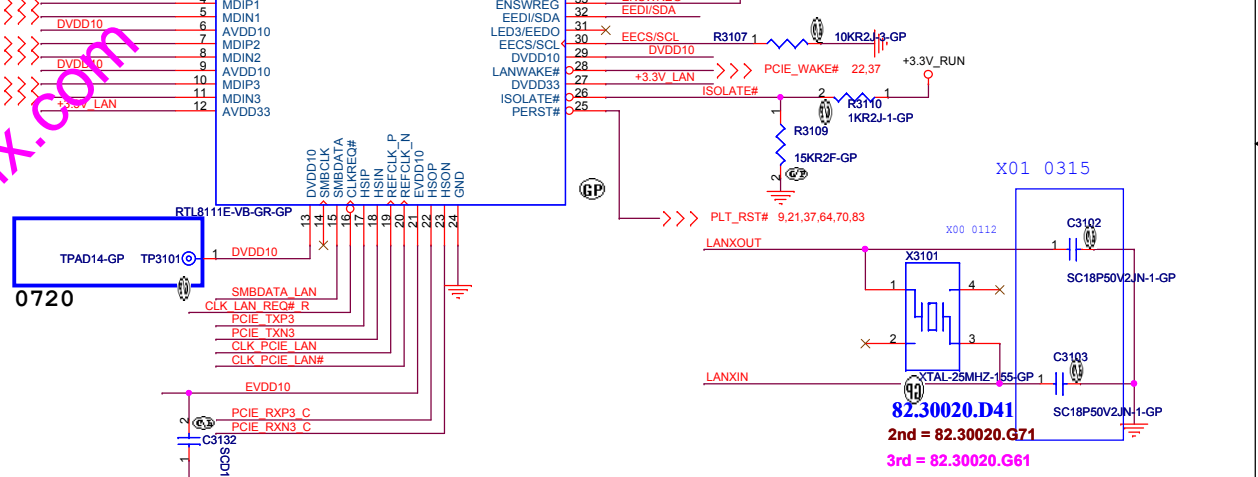
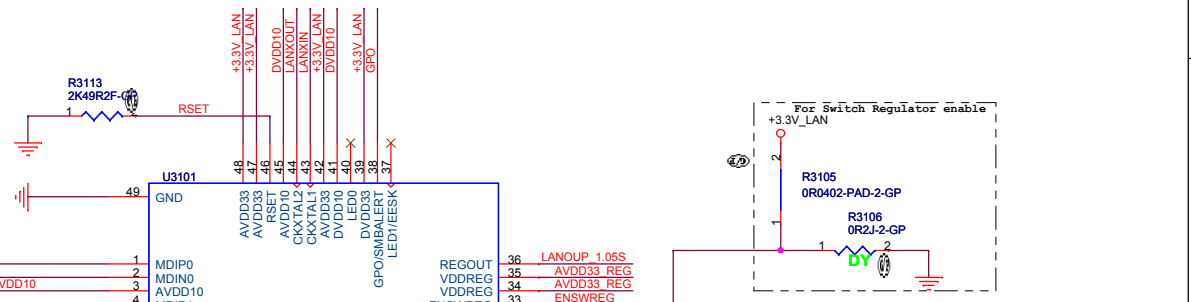
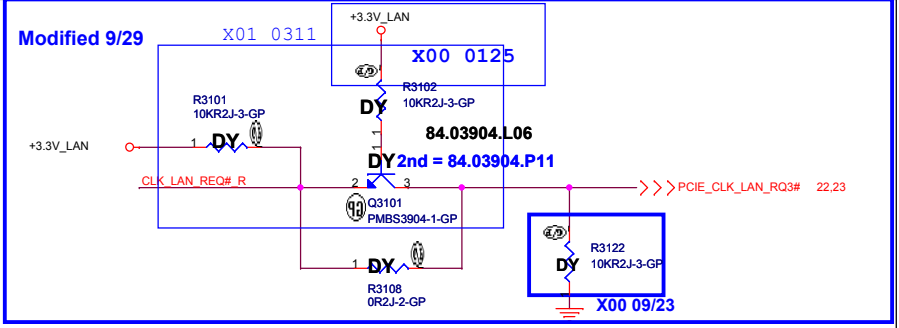
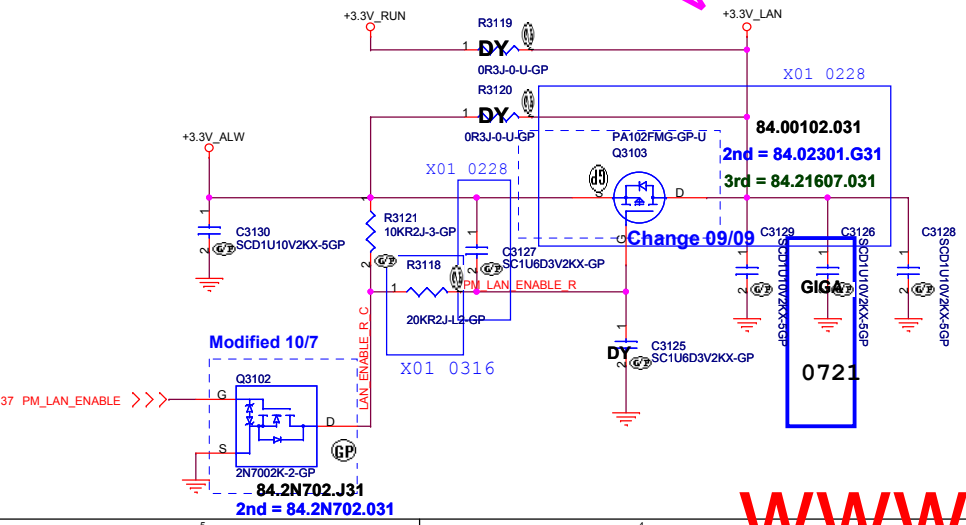
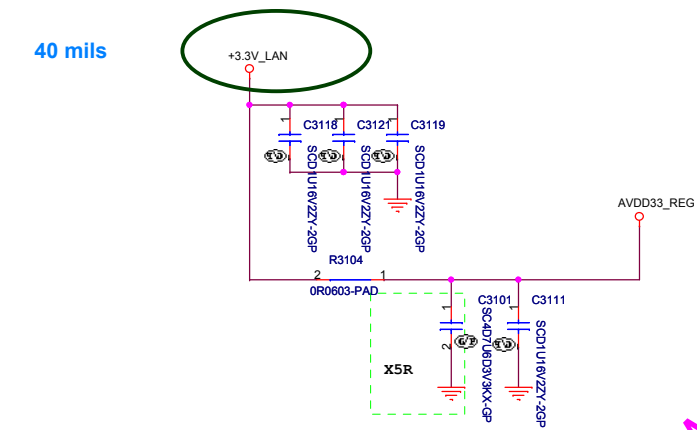
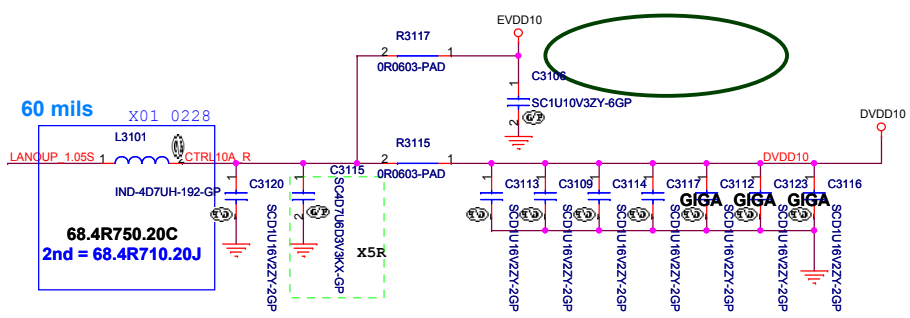
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<Core Design>

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Title		Reserved
Size A3	Document Number DV14 CP UMA+DIS	Rev X00
Date: Thursday, January 06, 2011	Sheet 30 of 100	

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SSID = LOM LAN CHIP



<Core Design>

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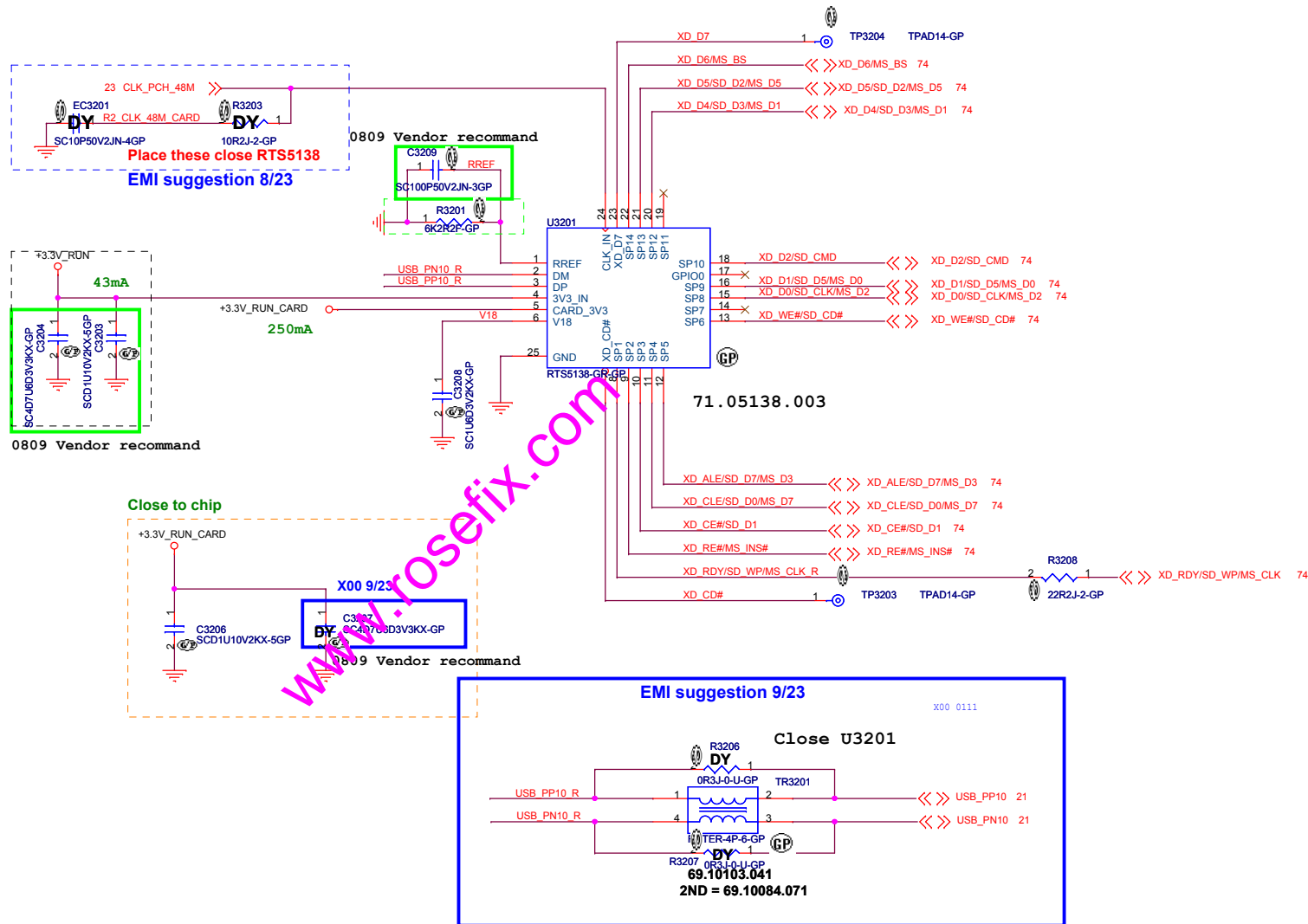
Title: **LAN-RTL8111E**

Size A3	Document Number DV14 CP UMA+DIS	Rev X00
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SSID = SDIO



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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.


Title: **Card Reader-RTS5138**

Size: A3	Document Number: DV14 CP UMA+DIS	Rev: X00
Date: Wednesday, March 23, 2011	Sheet: 32 of 100	

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Size A3	Document Number DV14 CP UMA+DIS	Rev X00	
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Size A3	Document Number DV14 CP UMA+DIS	Rev X00	
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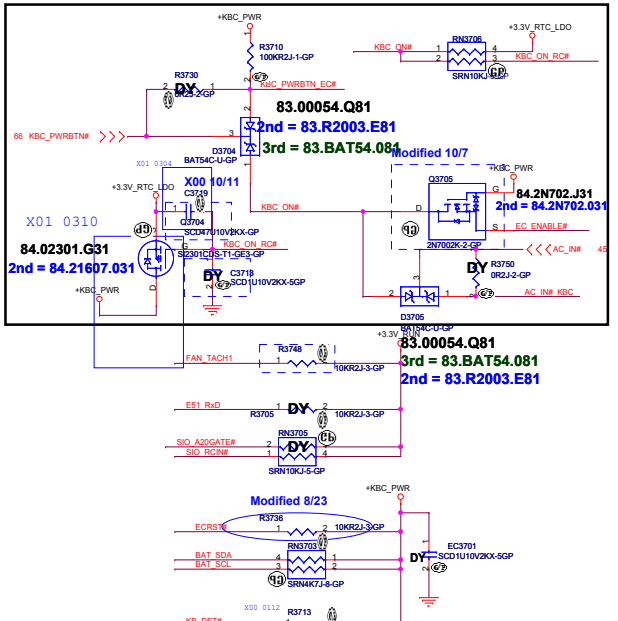
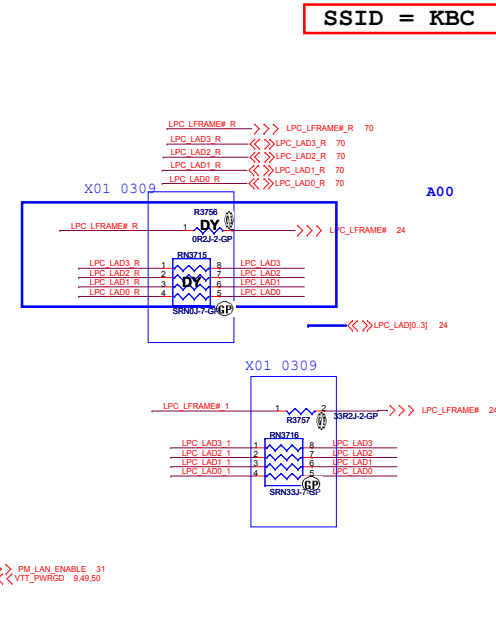
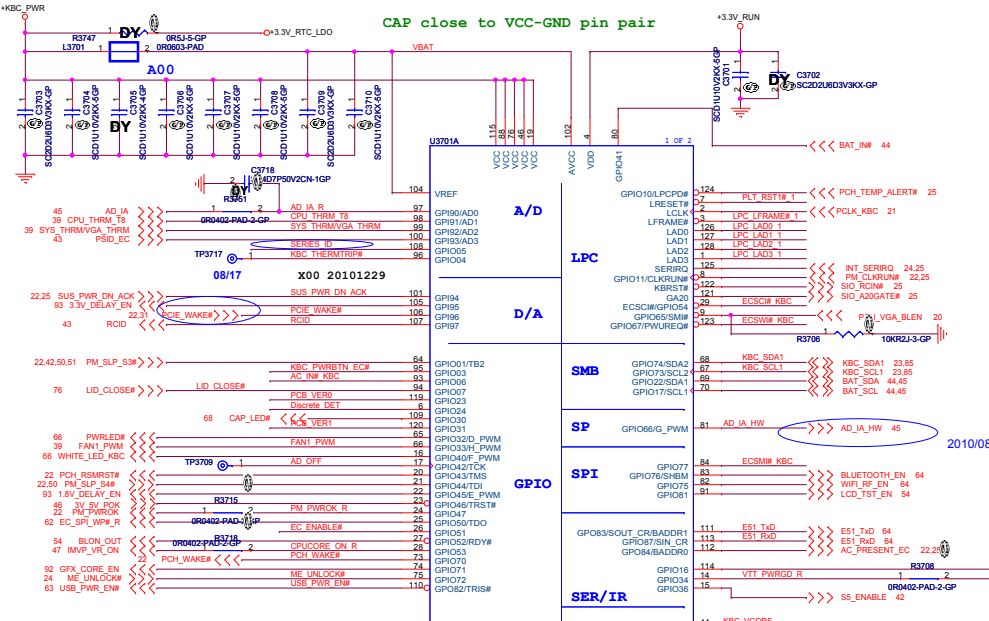
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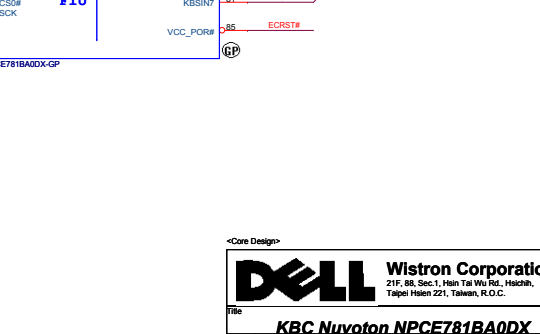
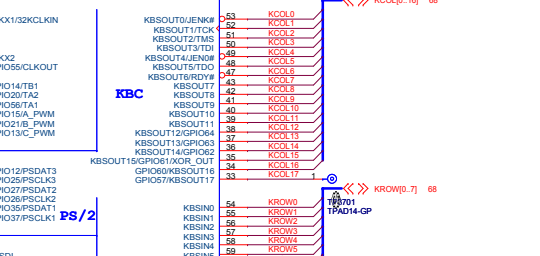
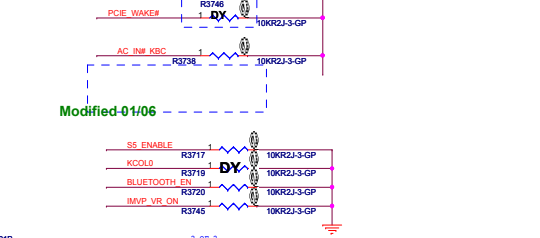
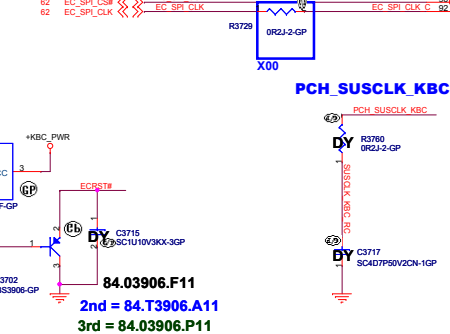
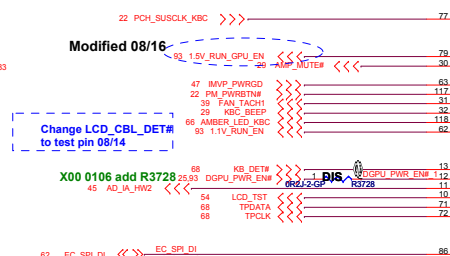
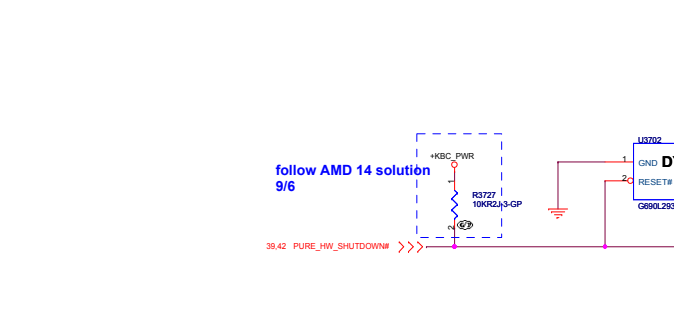
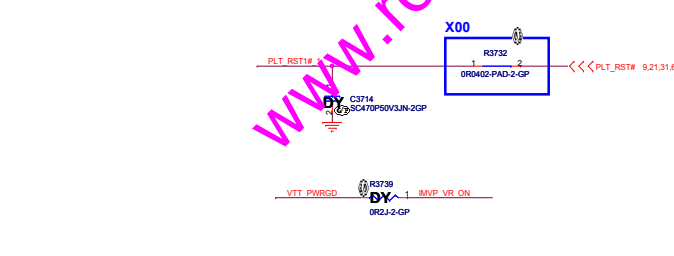
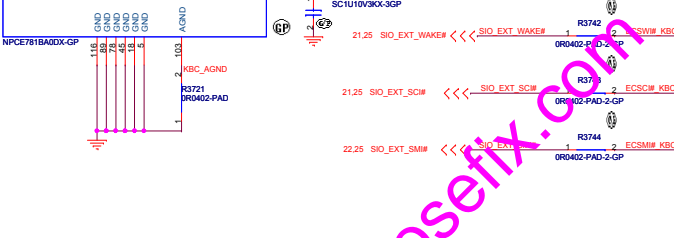
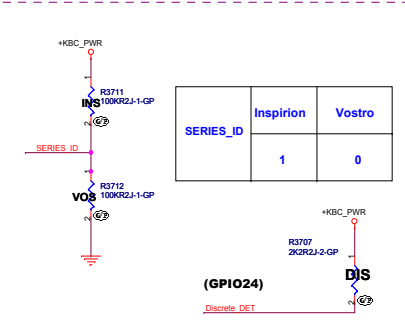
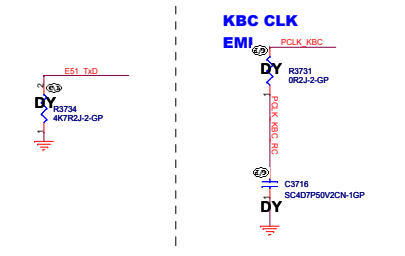
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Size A3	Document Number DV14 CP UMA+DIS	Rev X00	
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MB VERSION


ID	VER1	VER0
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X01	0	1
X02	1	0
A00	1	1



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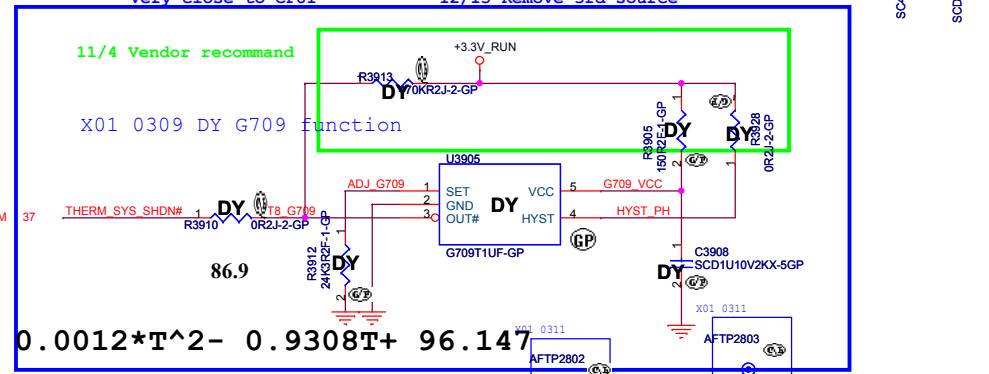
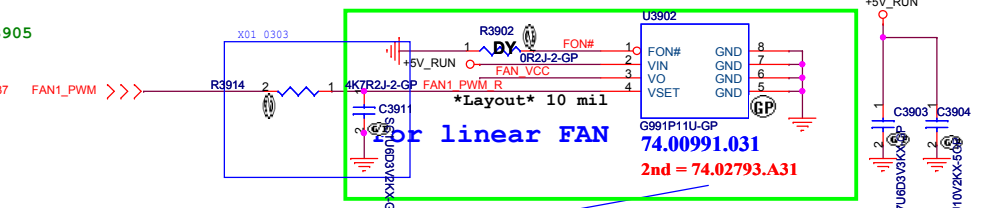
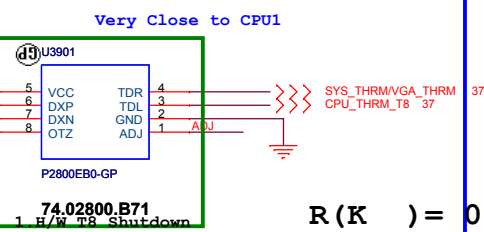
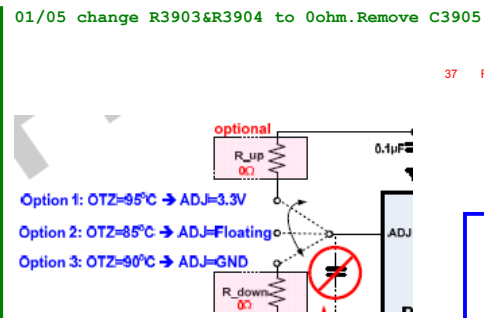
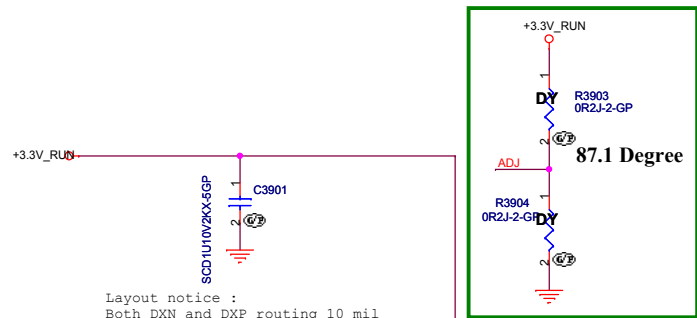
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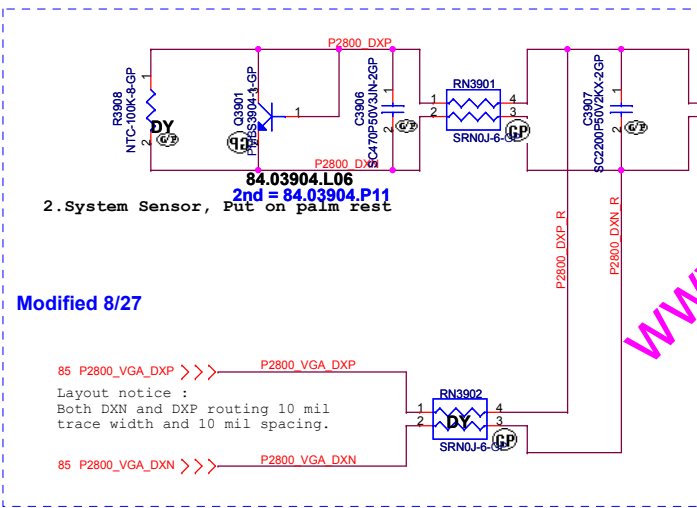
SSID = Thermal

Thermal sensor P2800

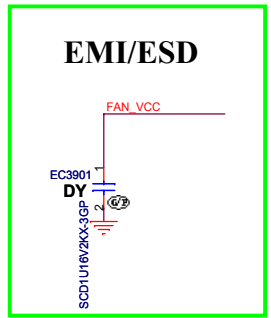
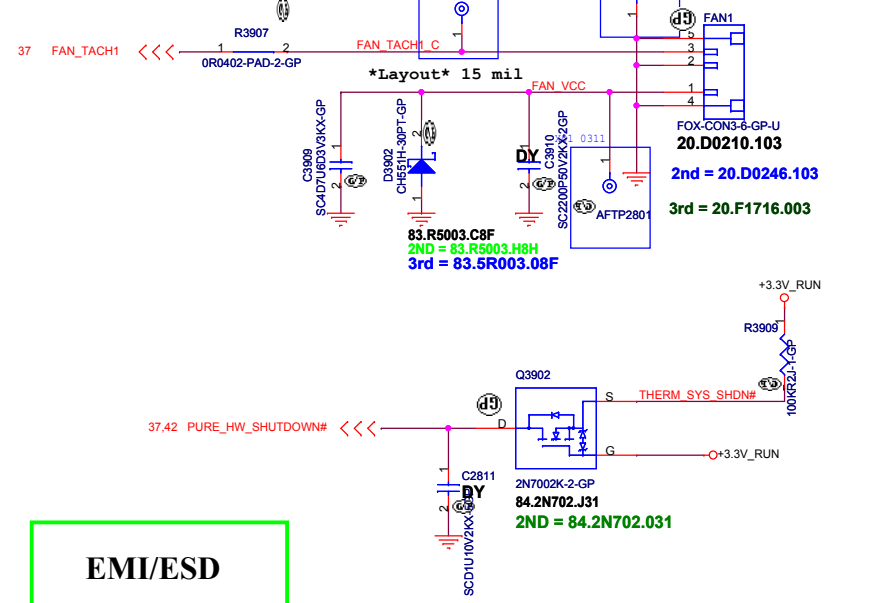
Fan controller P2793



$$R(K) = 0.0012 * T^2 - 0.9308T + 96.147$$



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<Core Design>

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Title: **Thermal P2800/Fan Controller P2793**


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Size A3	Document Number DV14 CP UMA+DIS	Rev X00
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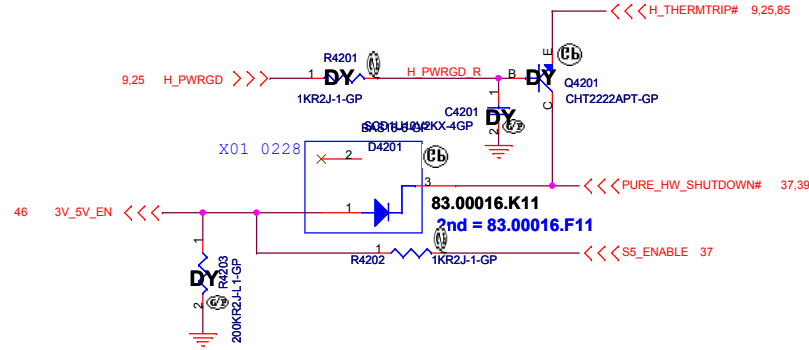
www.rosefix.com

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Size A3	Document Number DV14 CP UMA+DIS	Rev X00	
Date: Thursday, January 06, 2011	Sheet 41	of 100	

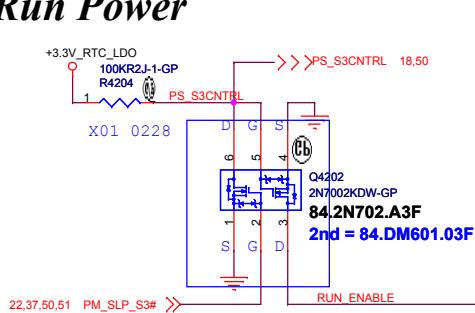
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SSID = Reset.Suspend



Peak current: 6370mA (HD:1100 ODD:2500)
 Design current: 4459 mA
 11.6A
 Rds=14m ohm ==> 0.09V

Run Power



Peak current: 3861mA
 Design current: 2702mA
 11.6A
 Rds=14m ohm ==> 0.054

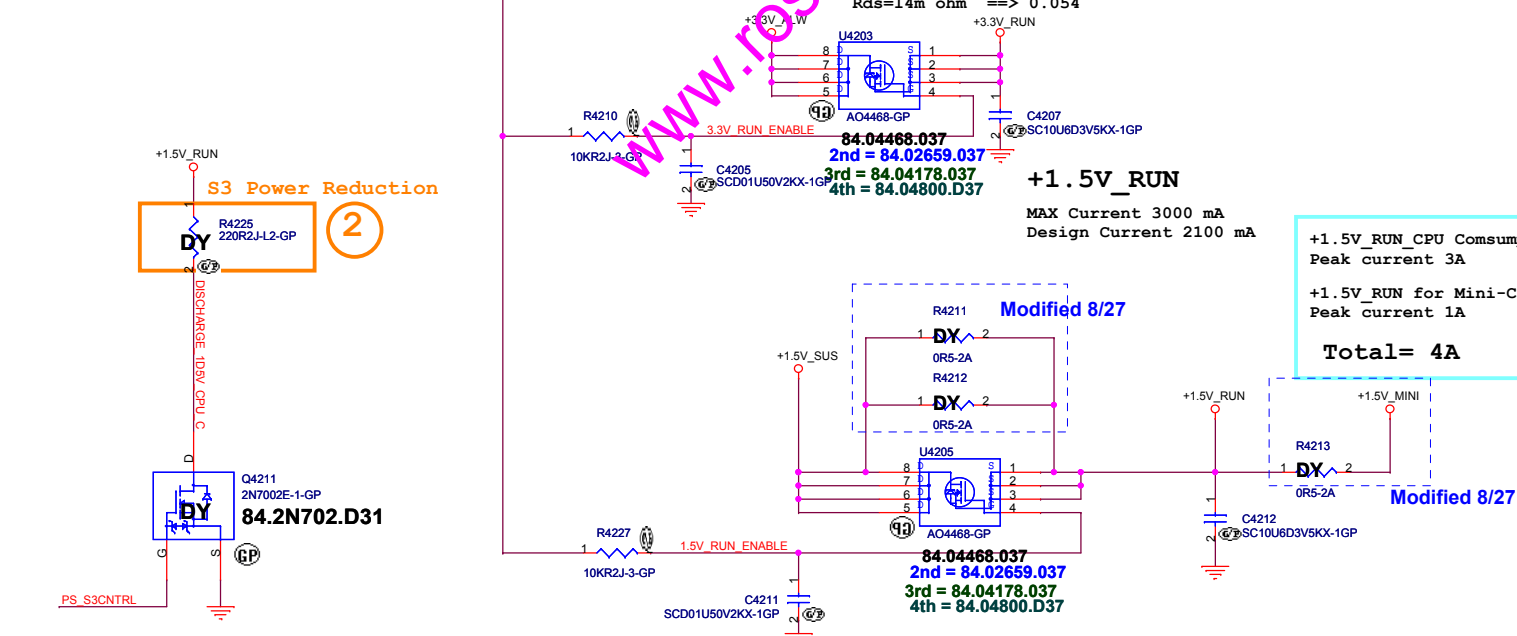


+1.5V_RUN
 MAX Current 3000 mA
 Design Current 2100 mA

+1.5V_RUN_CPU Consumption
 Peak current 3A
 +1.5V_RUN for Mini-Card Consumption
 Peak current 1A
Total= 4A

Modified 8/27

Modified 8/27



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<Core Design>

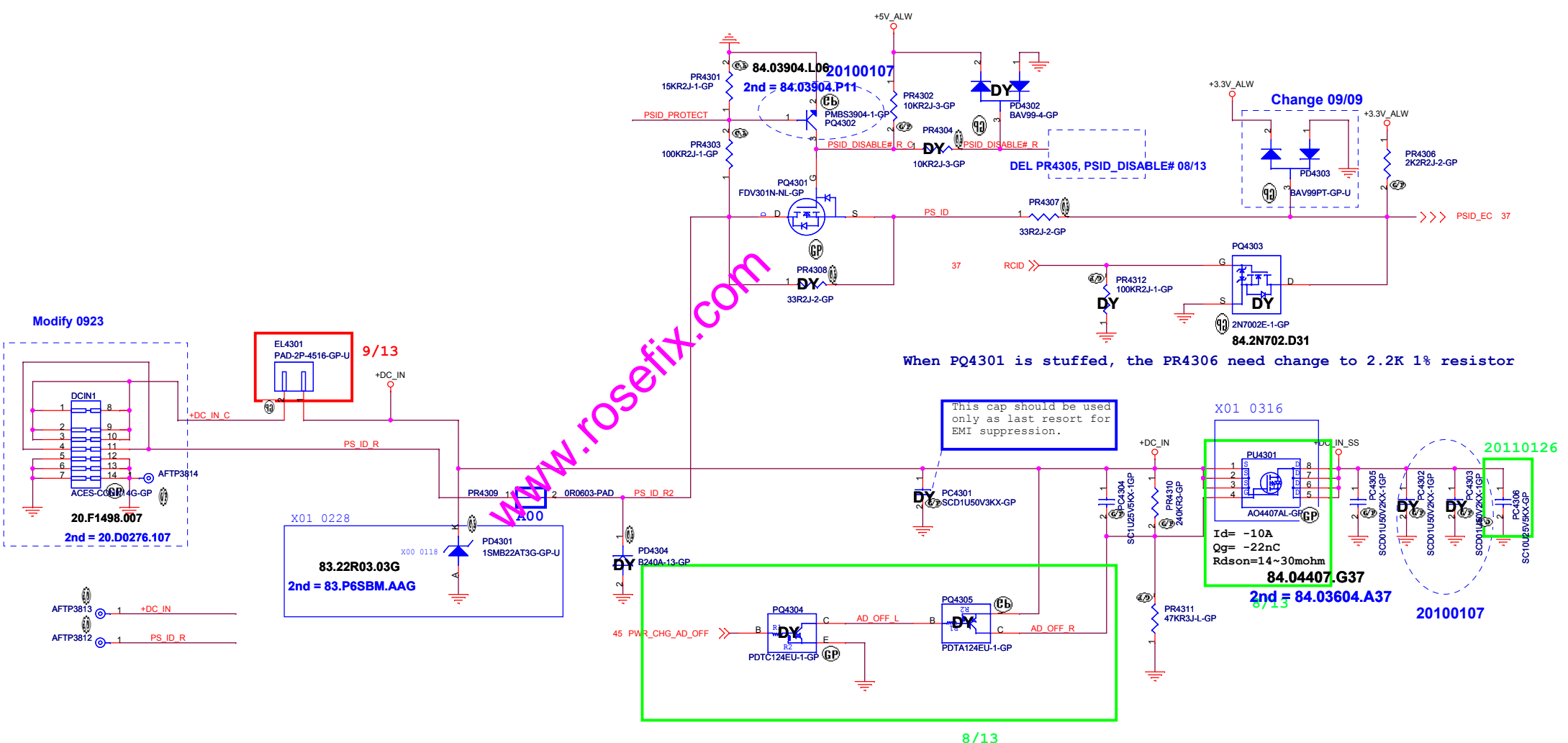
DELL Wistron Corporation
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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Plane Enable**

Size A3	Document Number DV14 CP UMA+DIS	Rev X00
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SSID = PWR.Support

DCin CONN



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<Core Design>

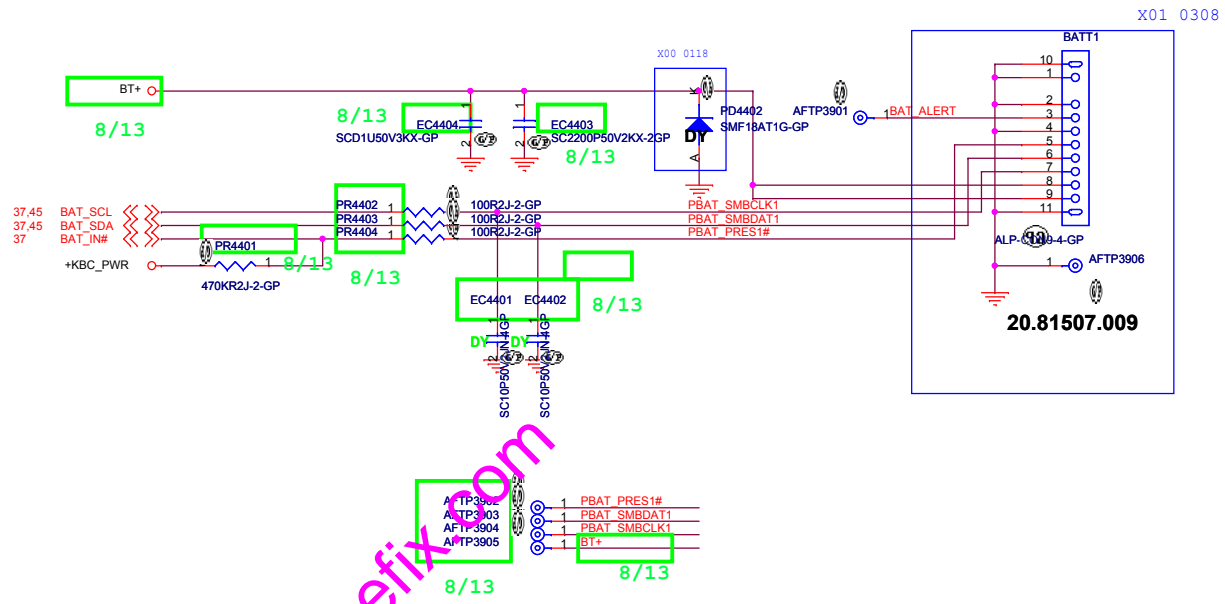
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DCIN Jack**

Size A3	Document Number DV14 CP UMA+DIS	Rev X00
Date: Wednesday, March 23, 2011	Sheet 43 of 100	

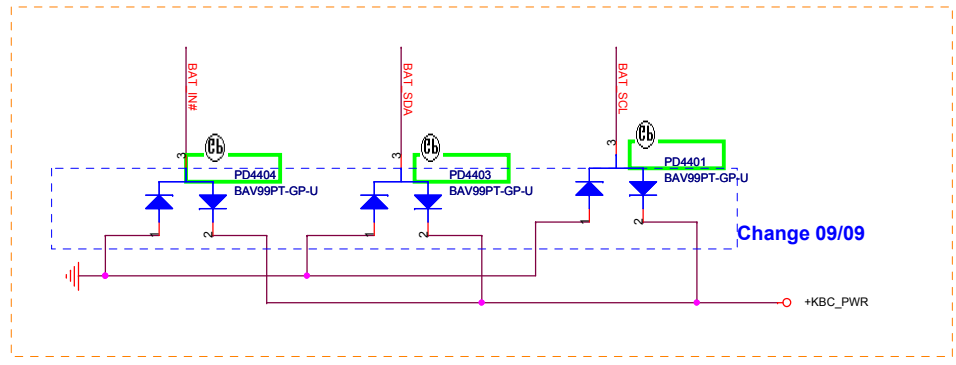
SSID = PWR.Support

Batt Connector



For actual location, need to be swap all pin

Close to Batt Connector



Change 09/09

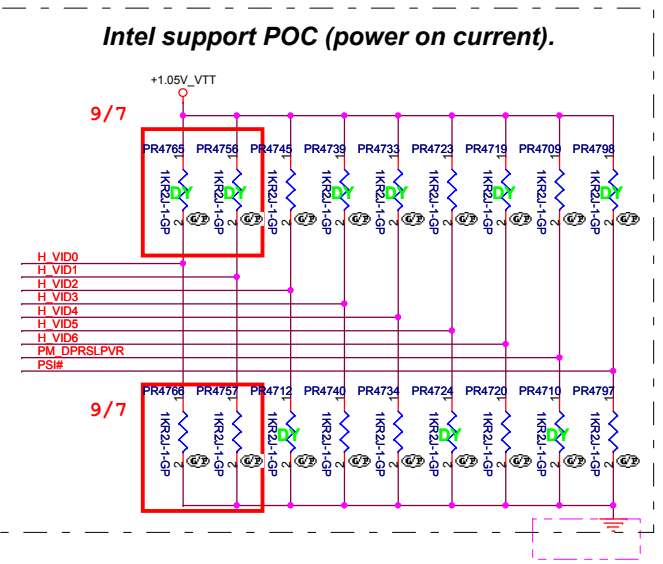
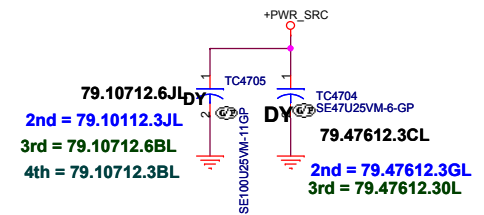
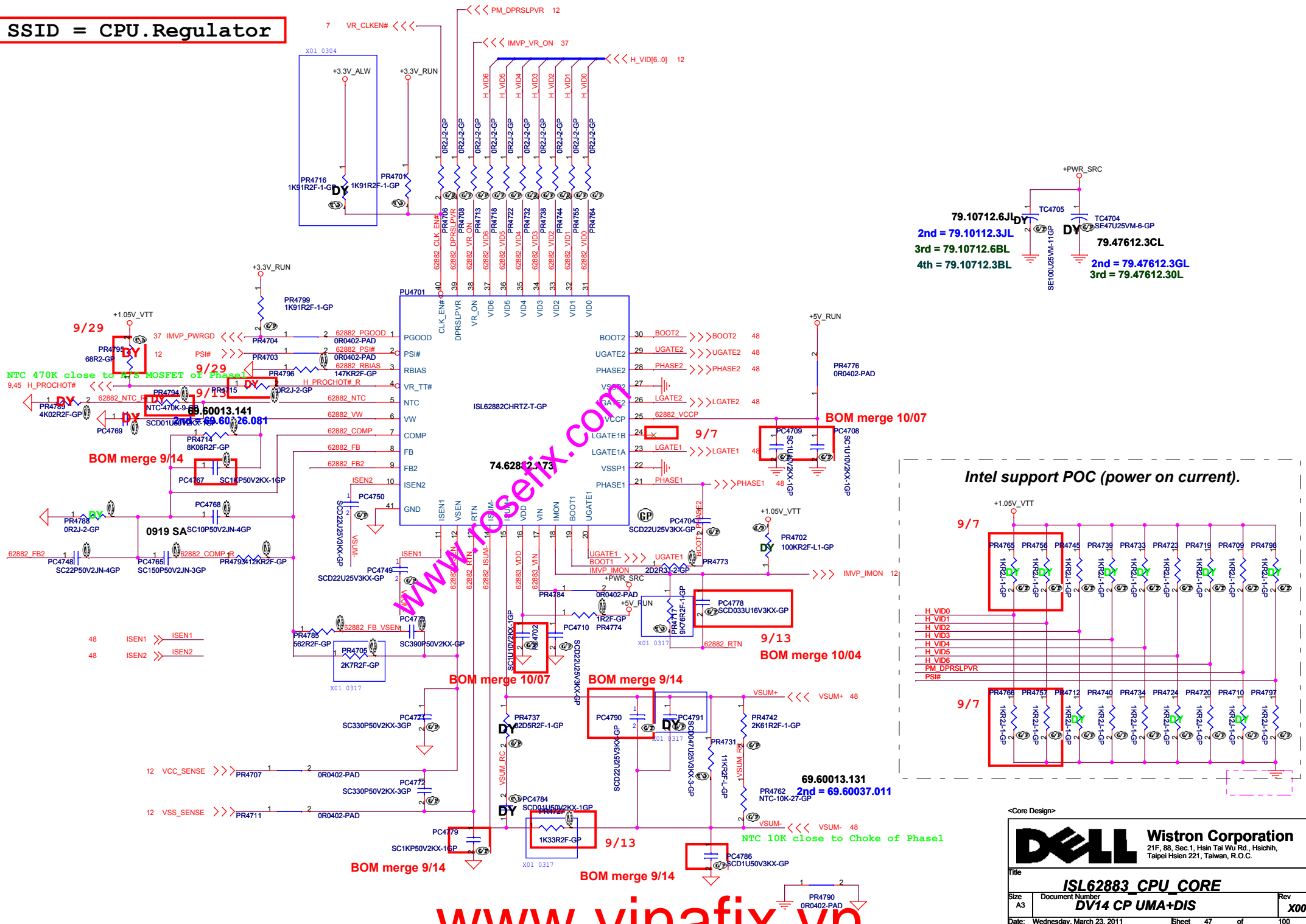
<Core Design>

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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **BATT CONN**

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SSID = CPU.Regulator



<Core Design>

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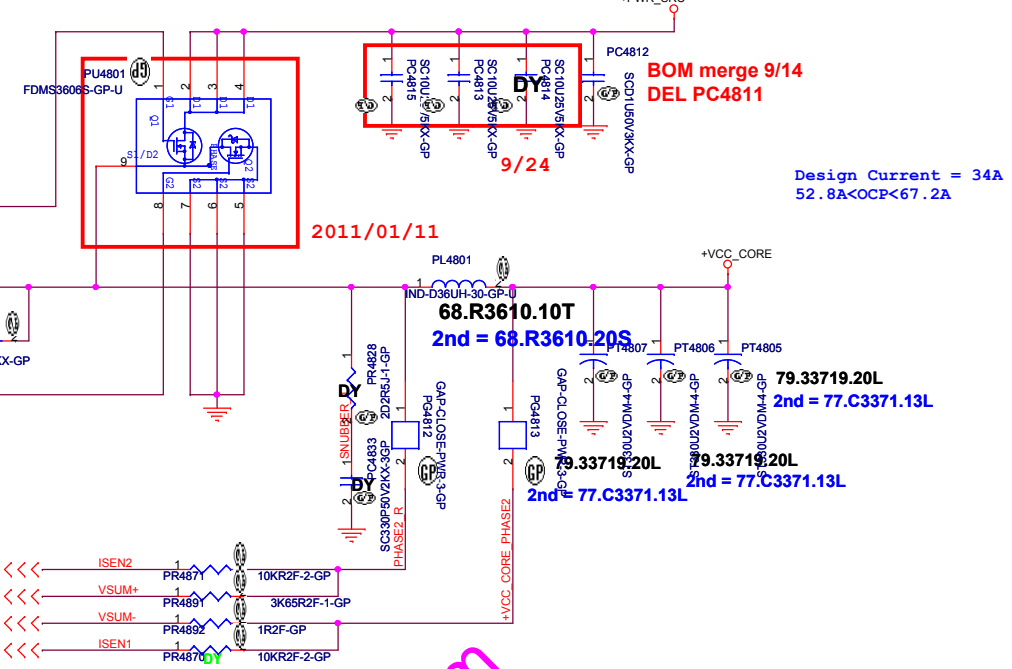
File: **ISL62883 CPU CORE**

Size: A3	Document Number: DV14 CP UMA+DIS	Rev: X00
Date: Wednesday, March 23, 2011	Sheet: 47	of 100

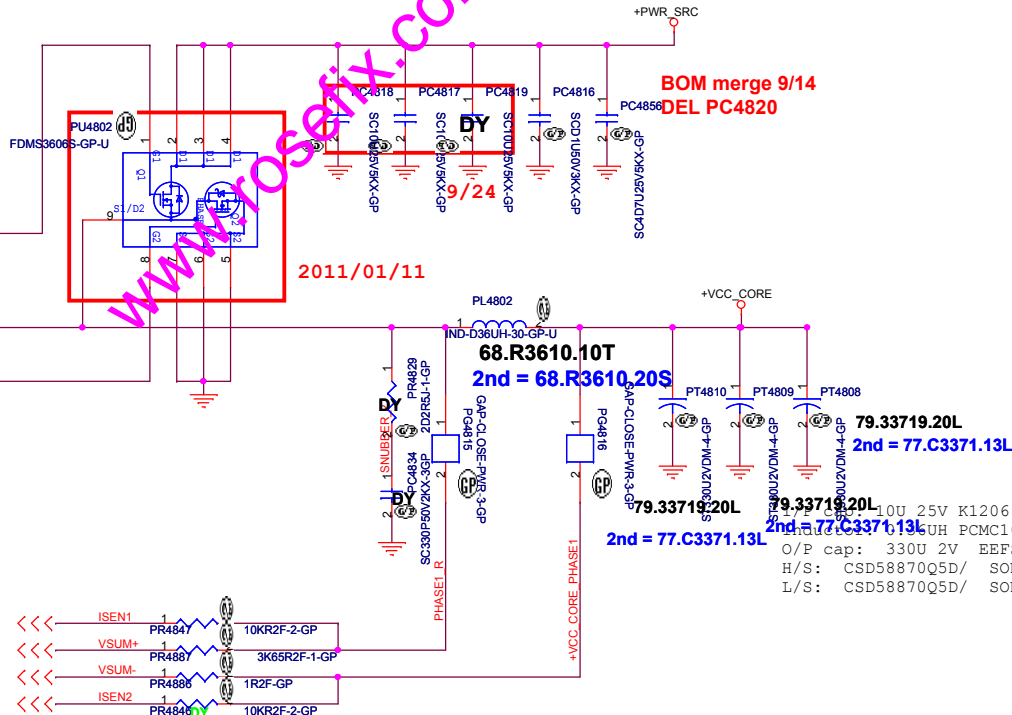
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SSID = CPU.Regulator

47 UGATE2 >>> UGATE2
 47 PHASE2 >>> PHASE2
 47 BOOT2 >>> BOOT2
 47 LGATE2 >>> LGATE2



47 UGATE1 >>> UGATE1
 47 PHASE1 >>> PHASE1
 47 LGATE1 >>> LGATE1



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L10U 25V K1206 X5R/ 78.10622.52L
 L10UH PCMC104T-R36MN1R05J Cyntec 1.05mohm/ 68.R3610.20C
 O/P cap: 330U 2V EEF5X0D331XE 6mOhm 3.4Arms Panasonic/79.33719.20L
 H/S: CSD58870Q5D/ SON 8P/5.0mOhm/6.6mOhm@4.5Vgs/ 84.58870.037
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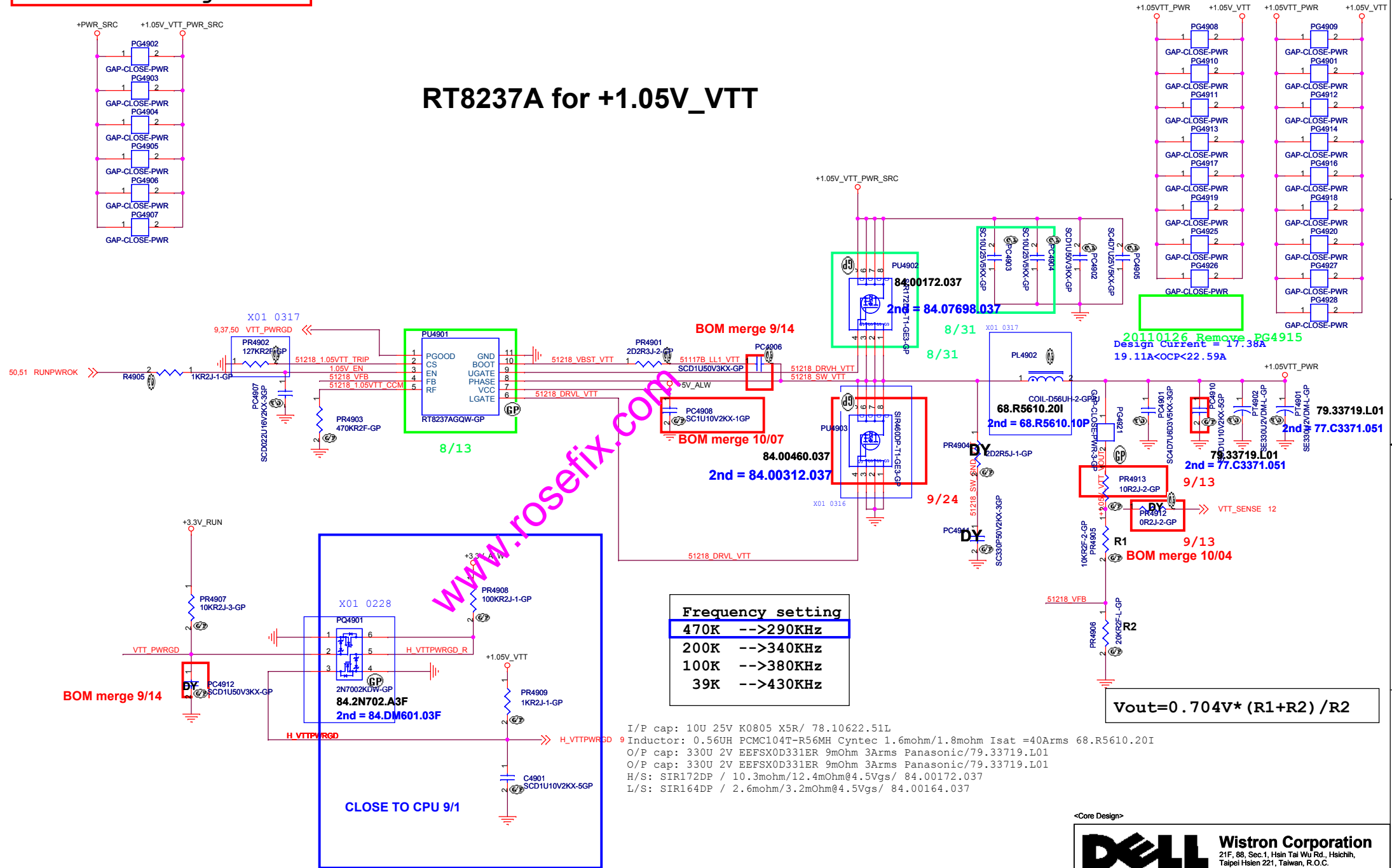
Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **ISL62883 CPU_CORE**

Size: A3	Document Number: DV14 CP UMA+DIS	Rev: X00
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SSID = CPU.Regulator

RT8237A for +1.05V_VTT



Frequency setting

470K	-->290KHz
200K	-->340KHz
100K	-->380KHz
39K	-->430KHz

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: 0.56UH PCMC104T-R56MH Cyntec 1.6mohm/1.8mohm Isat =40Arms 68.R5610.201
 O/P cap: 330U 2V EEF5X0D331ER 9mOhm 3Arms Panasonic/79.33719.L01
 O/P cap: 330U 2V EEF5X0D331ER 9mOhm 3Arms Panasonic/79.33719.L01
 H/S: SIR172DP / 10.3mohm/12.4mOhm@4.5Vgs/ 84.00172.037
 L/S: SIR164DP / 2.6mohm/3.2mOhm@4.5Vgs/ 84.00164.037

$$V_{out} = 0.704V * (R1 + R2) / R2$$

<Core Design>

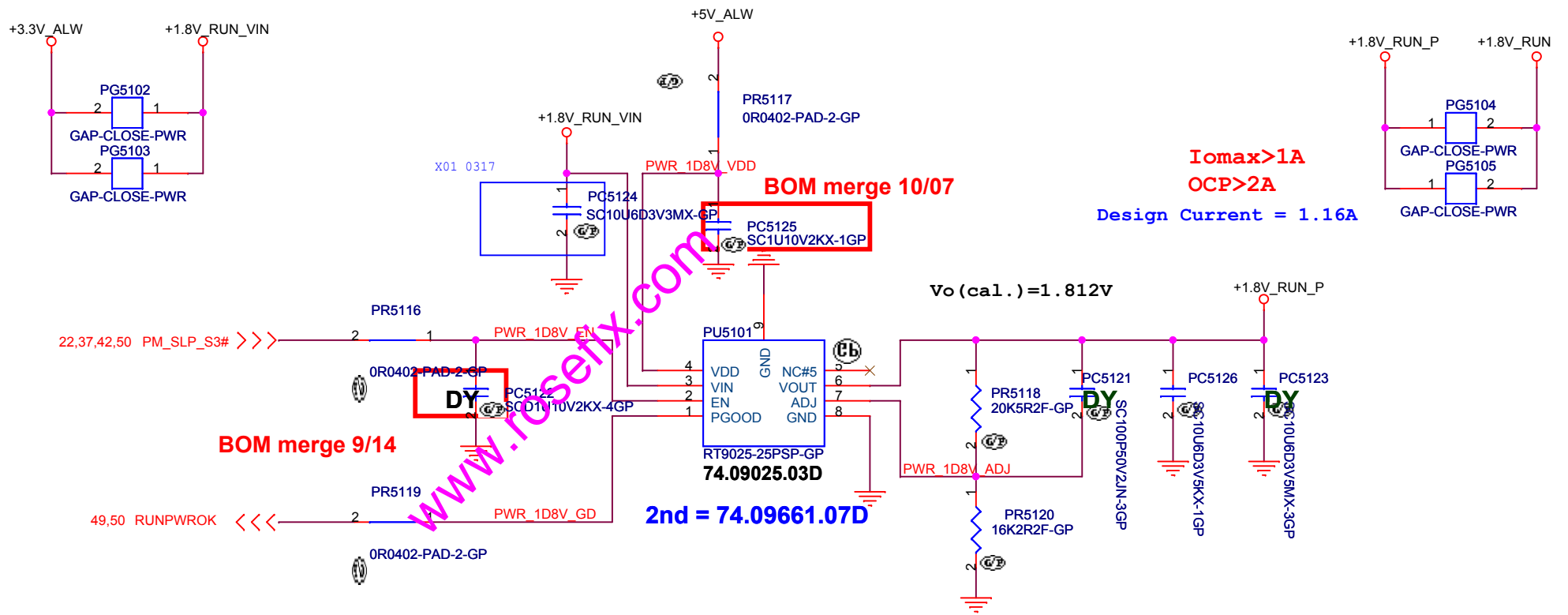
Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51218 +1.05V_VTT**


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SSID = PWR.Plane.Regulator_1p8v

RT9025 for +1.8V_RUN



<Core Design>


		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title RT9025 +1.8V_RUN		
Size A4	Document Number DV14 CP UMA+DIS	Rev X00
Date: Wednesday, March 23, 2011	Sheet 51	of 100

www.vinafix.vn

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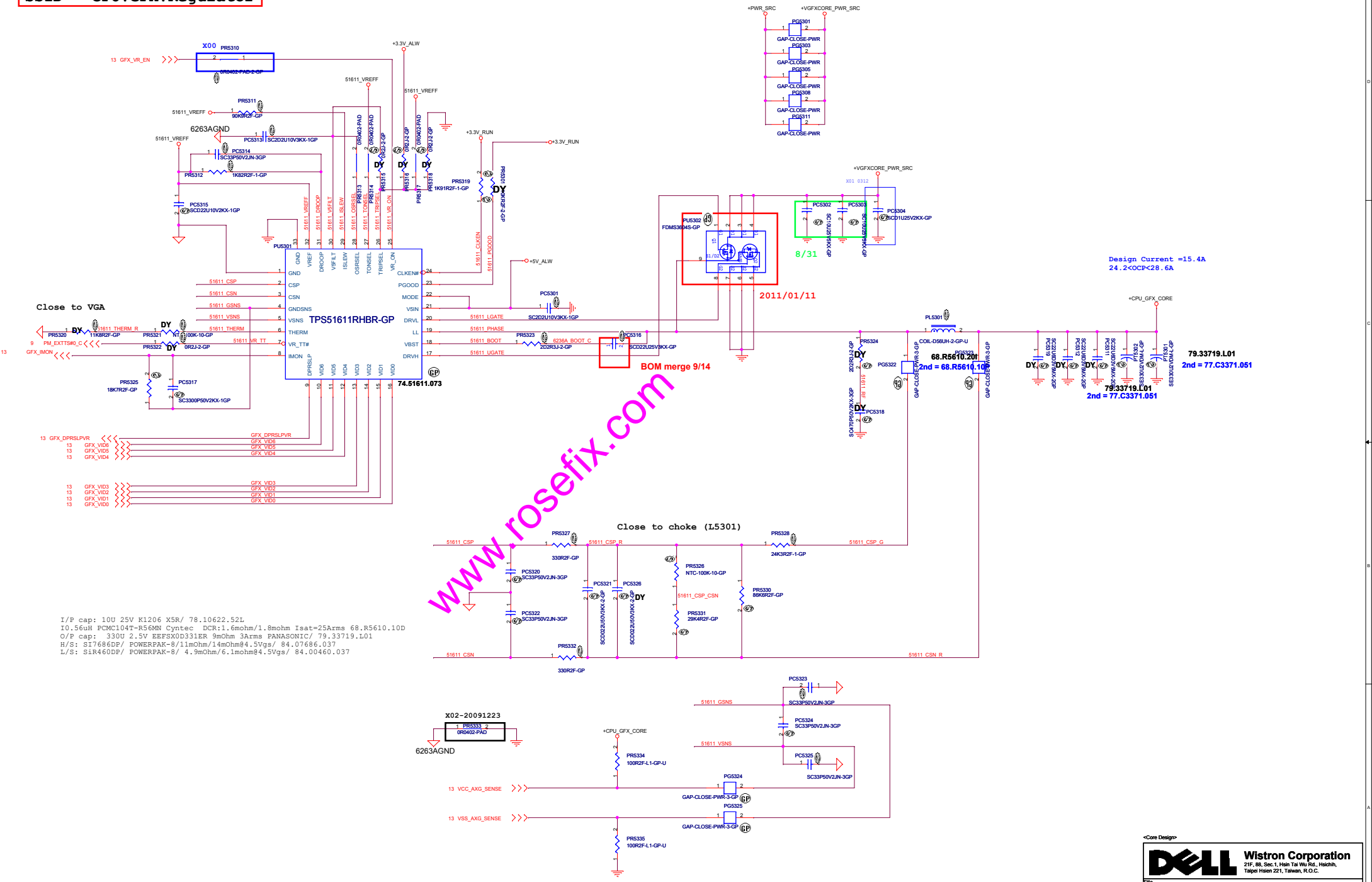
www.rosefix.com

<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number	Rev	
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SSID = CPU.GFX.Regulator



Design Current =15.4A
24.2<OCP<28.6A

2011/01/11

BOM merge 9/14

79.33719.L01
2nd = 77.C3371.051

79.33719.L01
2nd = 77.C3371.051

Close to choke (L5301)

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 I/O.56uH PCMC104T-R56MN Cynotec DCR:1.6mohm/1.8mohm Isat=25Arms 68.R5610.10D
 O/P cap: 330U 2.5V BEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L01
 H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
 L/S: SI1460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

www.rosefix.com

www.vinafix.vn

<Core Design>

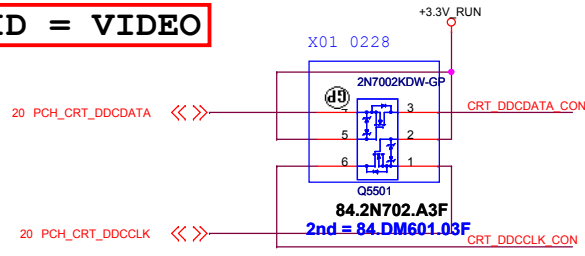
DELL Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchi,
 Taipei Hsein 221, Taiwan, R.O.C.

Title: **TPS51611 +GFX CORE**

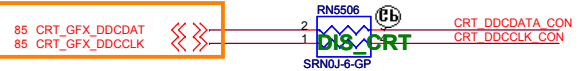
Size: Document Number **DV14 CP UMA+DIS** Rev **X00**

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SSID = VIDEO

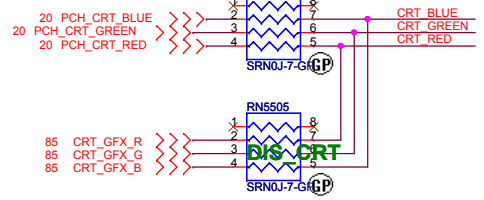


5V Tolerance

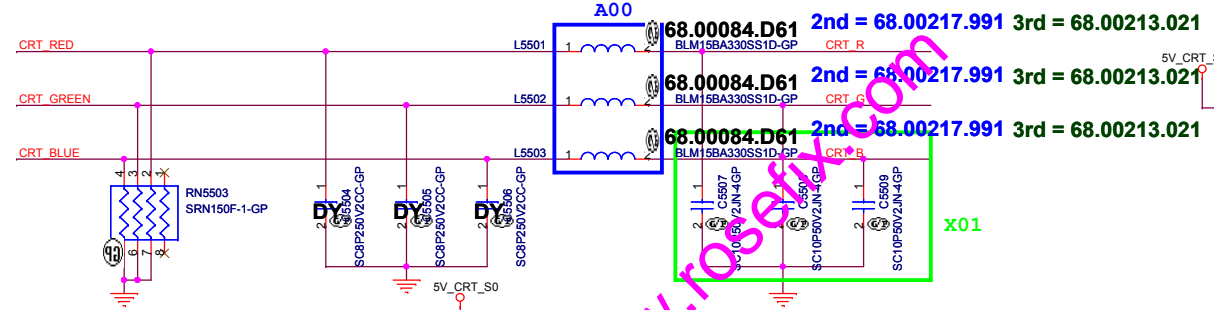
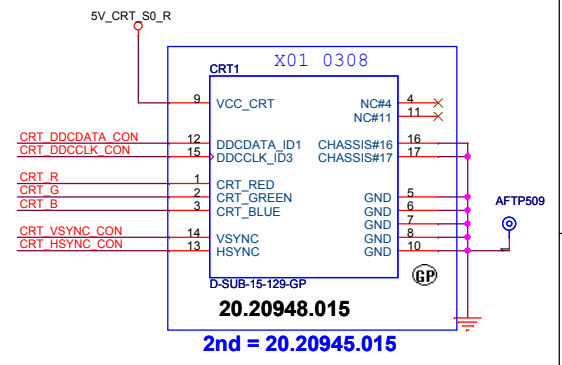


Layout Note:

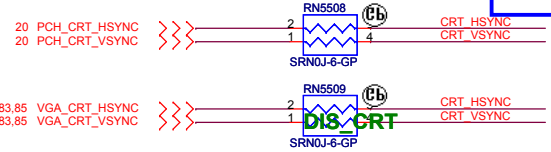
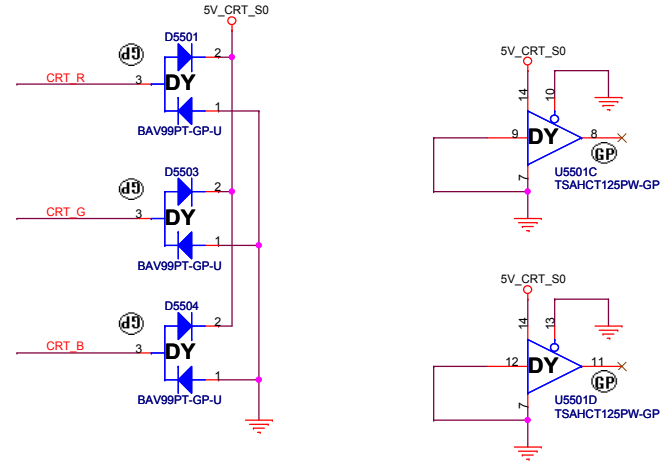
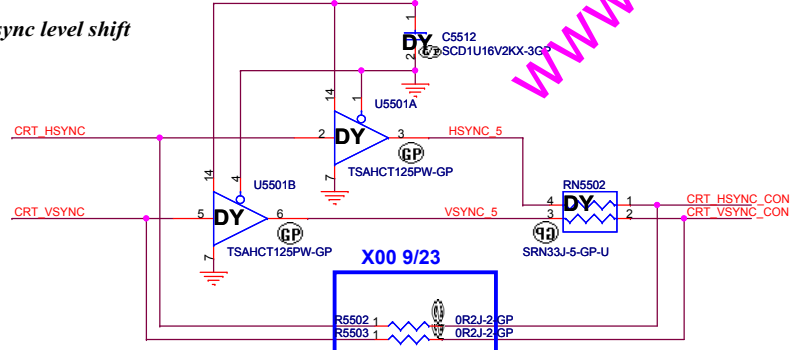
- *Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
- * RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.



- AFTP501 1 5V CRT_S0
- AFTP502 1 CRT_DDCDATA_CON
- AFTP503 1 CRT_DDCCLK_CON
- AFTP504 1 CRT_R
- AFTP505 1 CRT_G
- AFTP506 1 CRT_B
- AFTP507 1 CRT_HSYNC_CON
- AFTP508 1 CRT_VSYNC_CON



Hsync & Vsync level shift



CLOSE TO TRANSFORMER

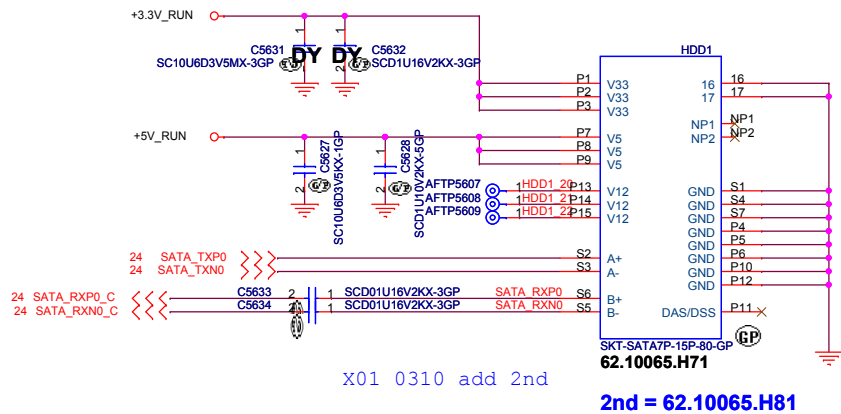
Dell Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

CRT Connector

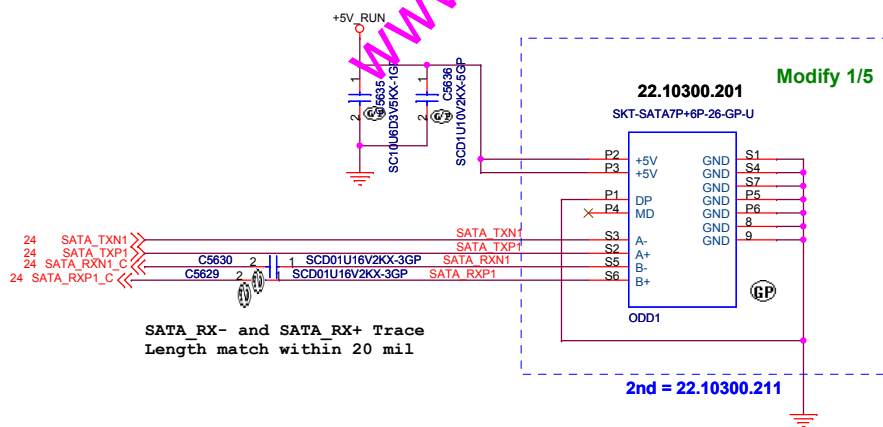
Size A3	Document Number DV14 CP UMA+DIS	Rev X00
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SSID = SATA

SATA HDD Connector



SATA ODD Connector



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<Core Design>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

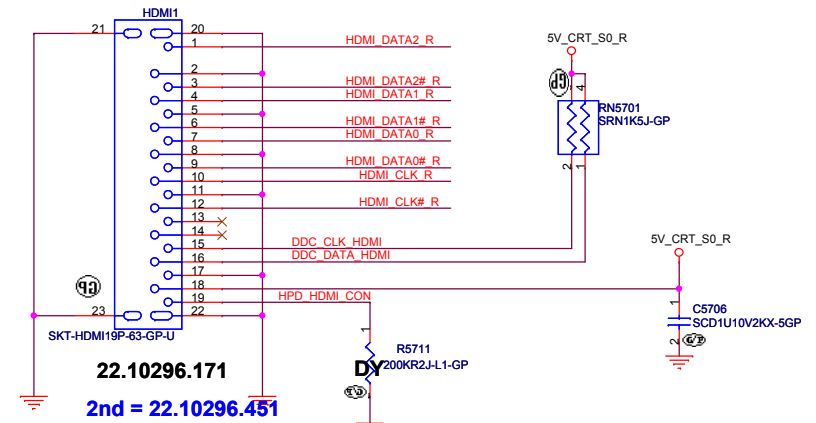
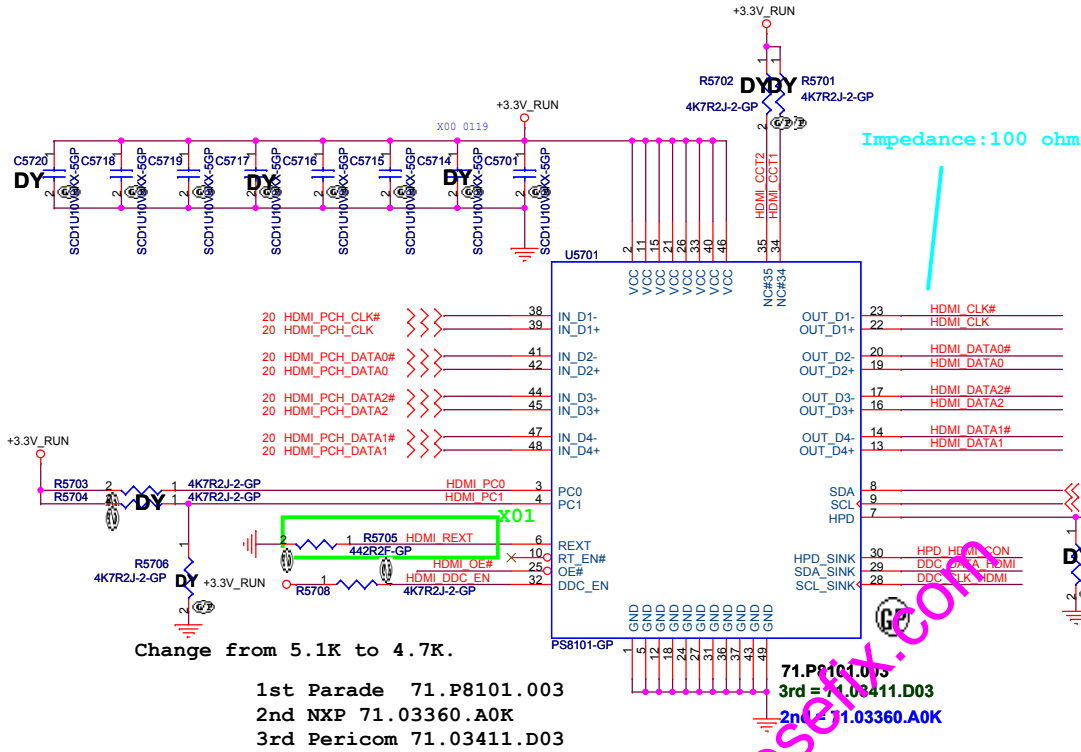
Title: **HDD/ODD**

Size: A3	Document Number: DV14 CP UMA+DIS	Rev: X00
Date: Wednesday, March 23, 2011		
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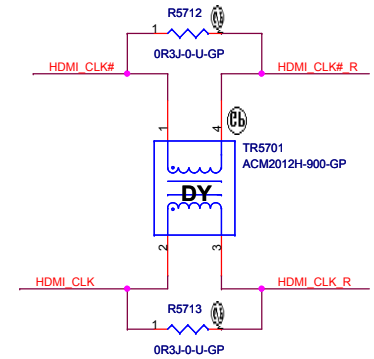
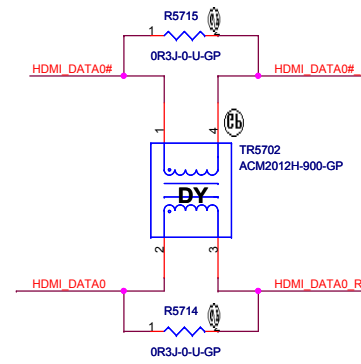
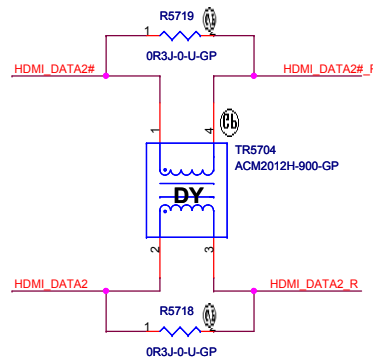
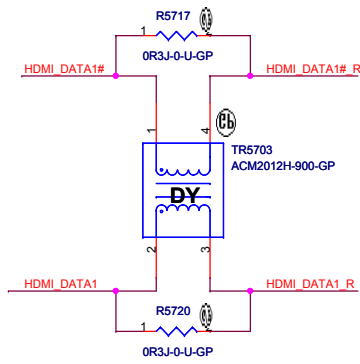
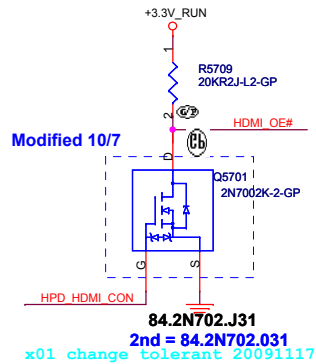
SSID = VIDEO

HDMI Level Shifter & CONNECTOR

HDMI CONN



HDMI level shift circuit



<Core Design>

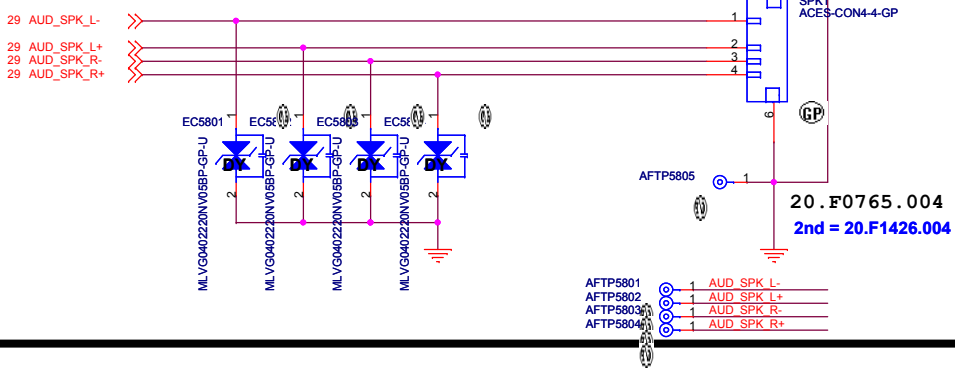
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDMI Level Shift/ Connector**

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SSID = AUDIO

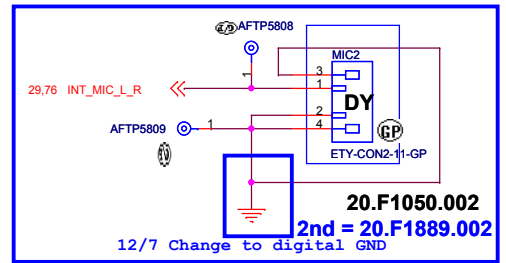
Speaker Connector



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11/26 reserve MIC2
12/7 change MIC2 to 20.F1050.002 X01 0309

X01 0309
20.F1889.002 20.F1050.002



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<Core Design>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio Jack**

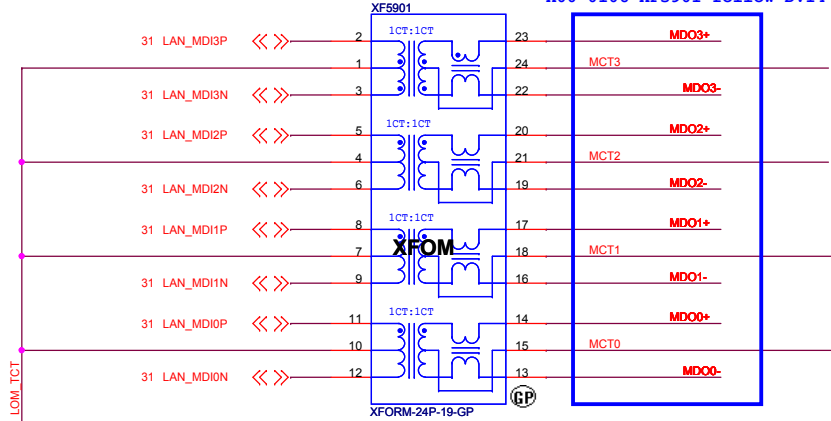
Size: A3	Document Number: DV14 CP UMA+DIS	Rev: X00
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SSID = LOM

LAN TransFormer

X01-0312
Add EMI solution for Surge

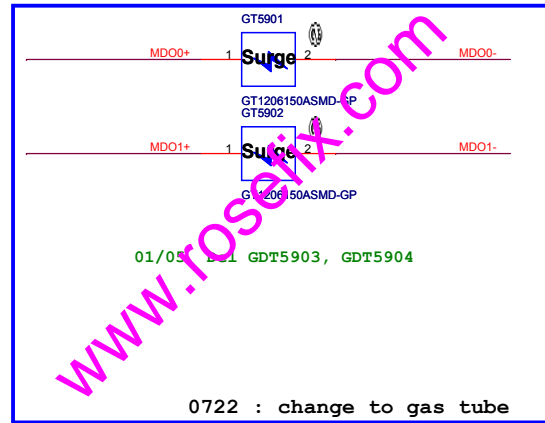
X00 0106 XF5901 follow DV14 HR



X00 0210
For GIGA LAN, use Transformer
68.IH601.301
For 10/100 LAN, use Transformer
68.HH035.301

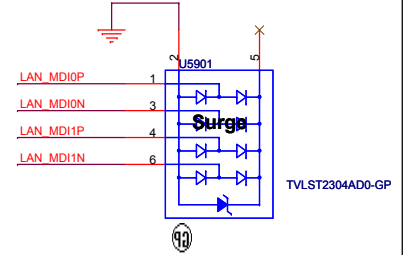
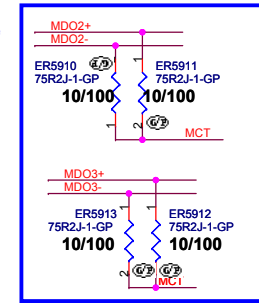
C5902
SCD1U10V2KX-5GP

68.IH601.301
2nd = 68.05009.30A

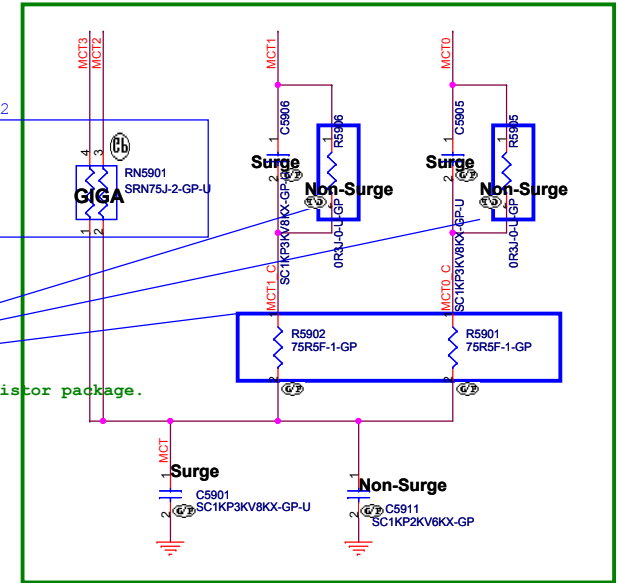


01/05 Add GDT5903, GDT5904

0722 : change to gas tube



X00 20110105

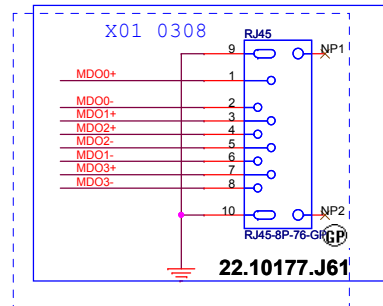


X01 0312

1/5 follow HR change resistor package.

11/25 modify to CRC circuit and divided resistor as EMI suggest
11/29 Change C5911 to 78.1022S.22L

RJ45



MDO0+	1	AFTP5907
MDO0-	1	AFTP5908
MDO1+	1	AFTP5901
MDO1-	1	AFTP5902
MDO2+	1	AFTP5903
MDO2-	1	AFTP5904
MDO3+	1	AFTP5905
MDO3-	1	AFTP5906

<Core Design>

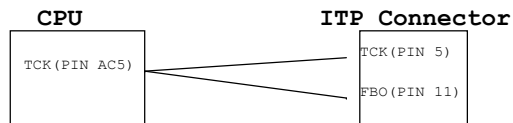
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien T21, Taiwan, R.O.C.

Title		
LAN CONN		
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SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



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<Core Design>


DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
ITP/Fan Connector		
Size	Document Number	Rev
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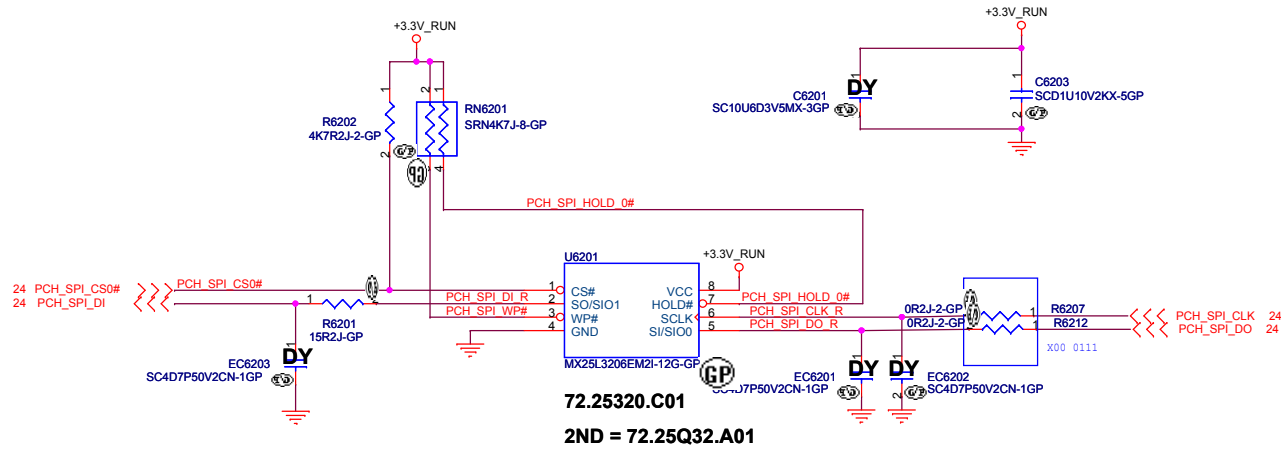
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Title			
Reseved			
Size	Document Number	Rev	
A3	DV14 CP UMA+DIS	X00	
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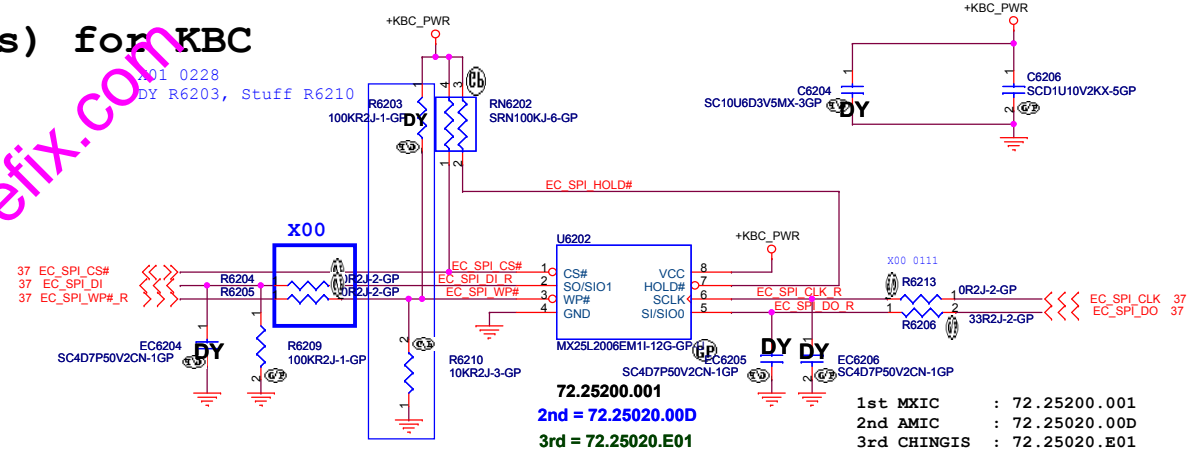
www.vinafix.vn

SSID = Flash.ROM

SPI FLASH ROM (32M bits) for PCH

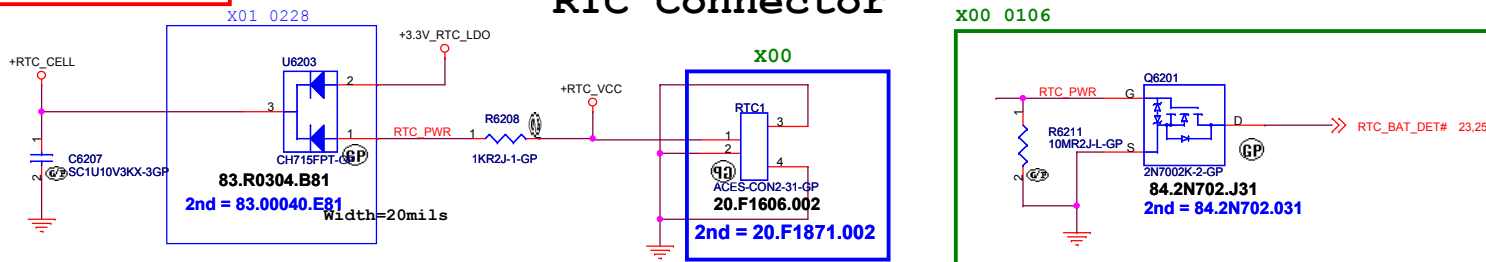


SPI FLASH ROM (2M bits) for KBC



SSID = RBATT

RTC Connector



<Core Design>

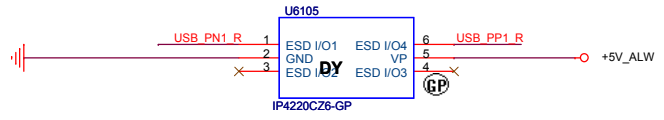
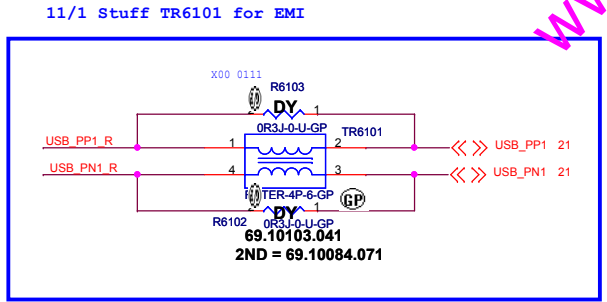
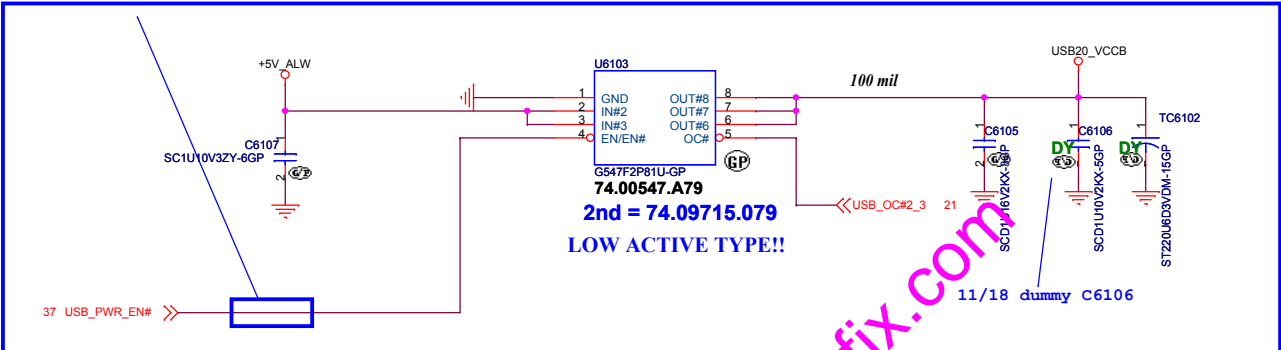
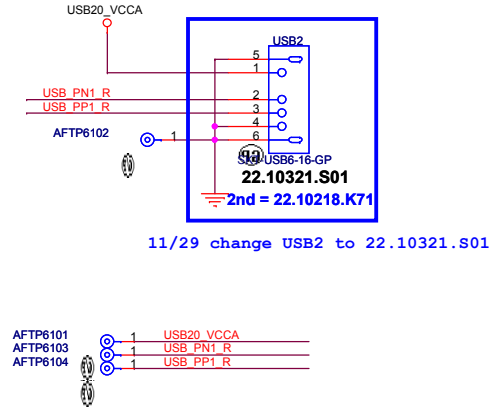
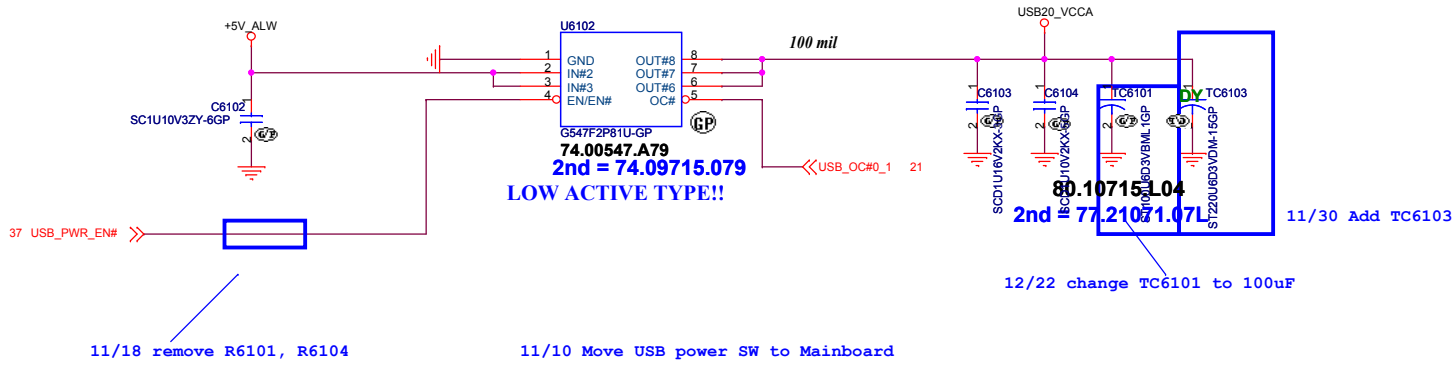
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Flash/RTC**

Size: A3	Document Number: DV14 CP UMA+DIS	Rev: X00
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SSID = USB



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<Core Design>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.


Title: **USB**

Size A3	Document Number DV14 CP UMA+DIS	Rev X00
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www.rosefix.com

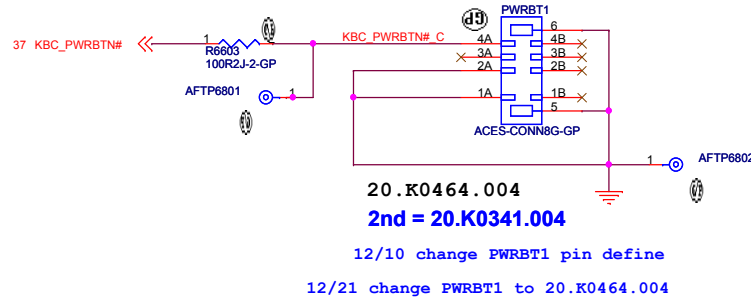
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
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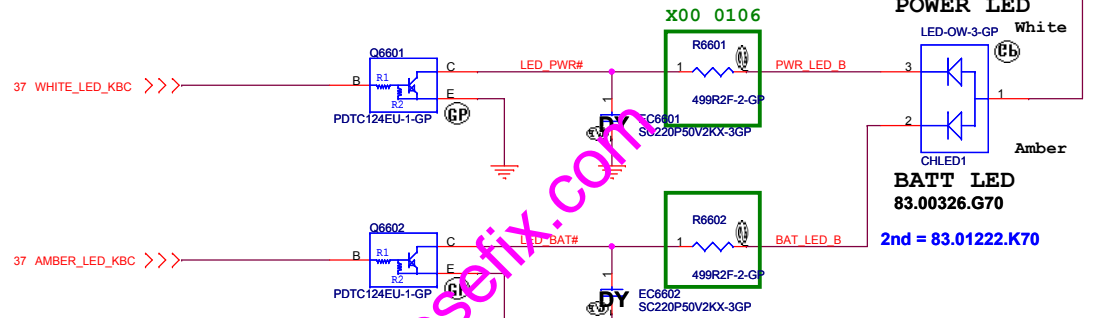
SSID = User.Interface

Power BTN Connector

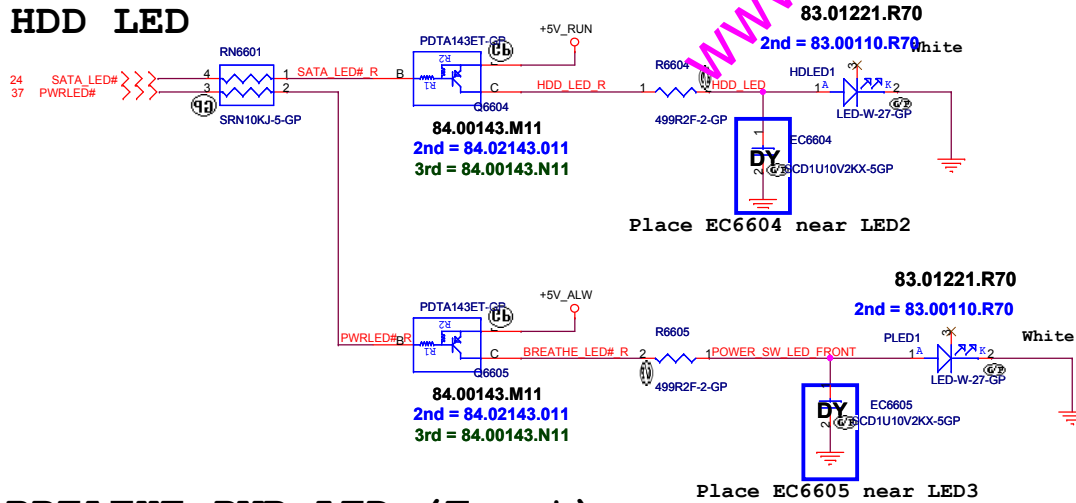


Modify 09/02

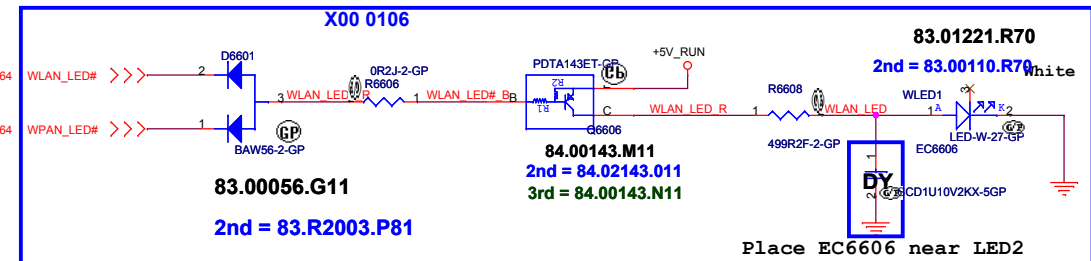
Battery LED



HDD LED



WLAN LED



<Core Design>




Title			PWR_BTN/LED		
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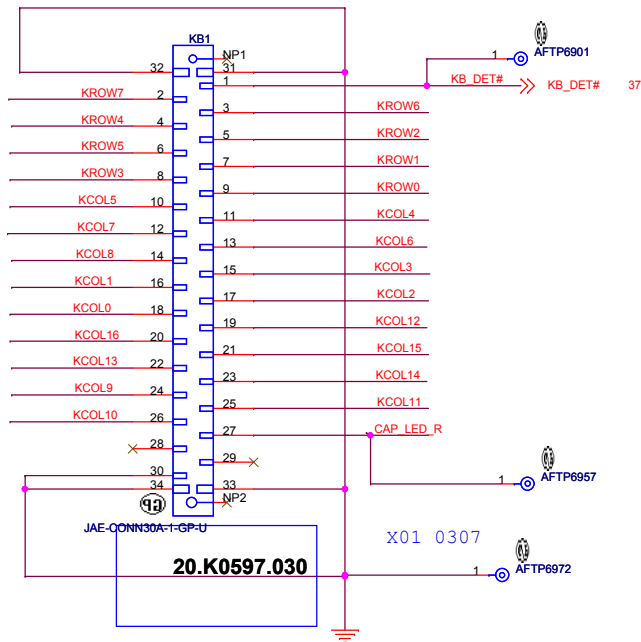
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
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www.vinafix.vn

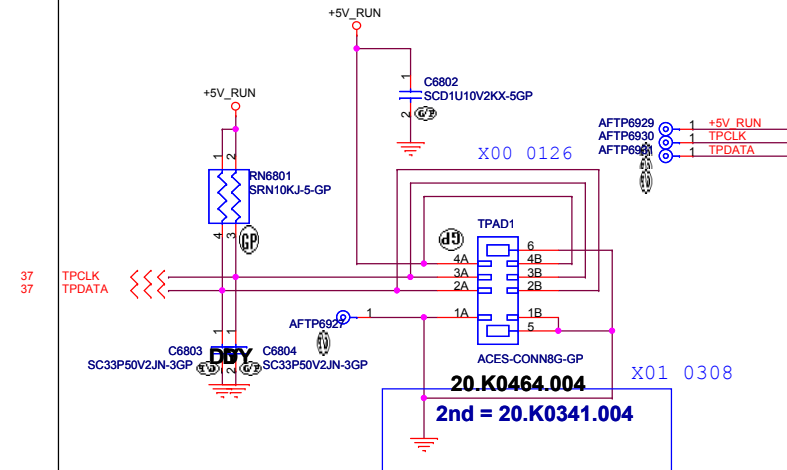
SSID = KBC

Internal KeyBoard Connector



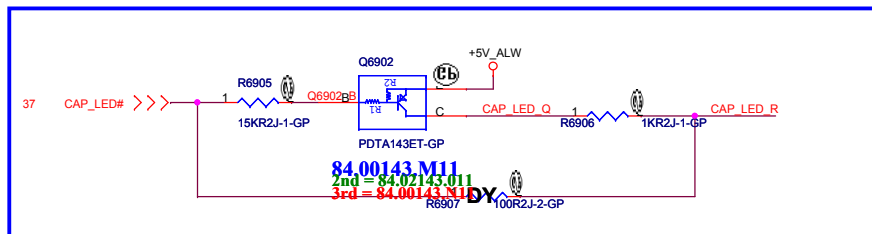
SSID = Touch . Pad

TouchPad Connector



12/8 Add Cap LED control circuit

CAP LED CONTROL



11/23 change TPAD1 to 20.K0320.004

KROW7	1	AFTP6902	KCOL5	1	TP6910	KCOL0	1	AFTP6918
KROW6	1	TP6903	KCOL4	1	TP6911	KCOL12	1	AFTP6919
KROW4	1	TP6904	KCOL7	1	TP6912	KCOL16	1	AFTP6920
KROW2	1	TP6905	KCOL6	1	TP6913	KCOL15	1	TP6921
KROW5	1	TP6906	KCOL8	1	TP6914	KCOL13	1	TP6922
KROW1	1	TP6907	KCOL3	1	TP6915	KCOL14	1	AFTP6923
KROW3	1	AFTP6908	KCOL1	1	AFTP6916	KCOL9	1	AFTP6924
KROW0	1	AFTP6909	KCOL2	1	AFTP6917	KCOL11	1	TP6925
						KCOL10	1	AFTP6926

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Key Board/Touch Pad**

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SSID = User.Interface

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<Core Design>

	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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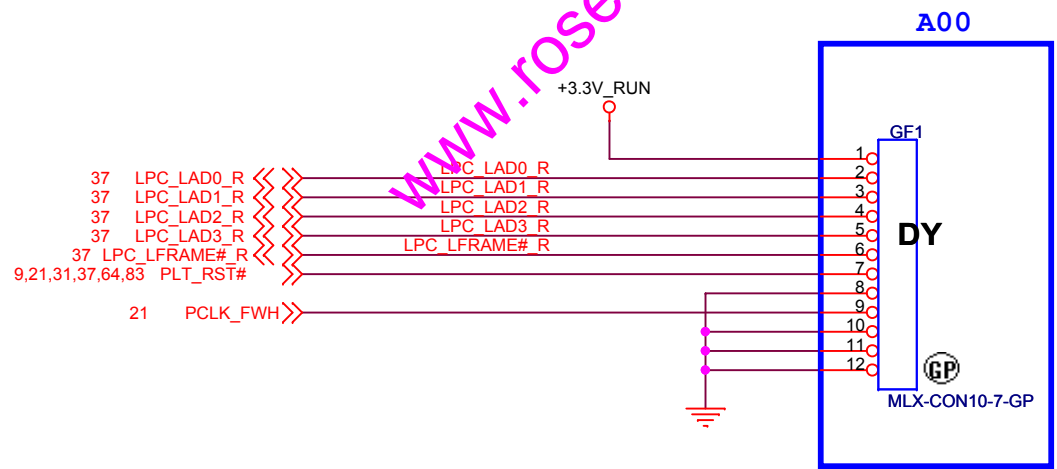
Title **Hall Sensor**

Size A4	Document Number DV14 CP UMA+DIS	Rev X00
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SSID = User.Interface



<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A4

Document Number

DV14 CP UMA+DIS

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X00

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<Core Design>


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Title			
Reserved			
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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		RESERVED
Size A3	Document Number DV14 CP UMA+DIS	Rev X00
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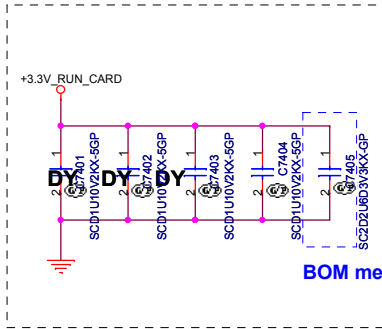
www.vinafix.vn

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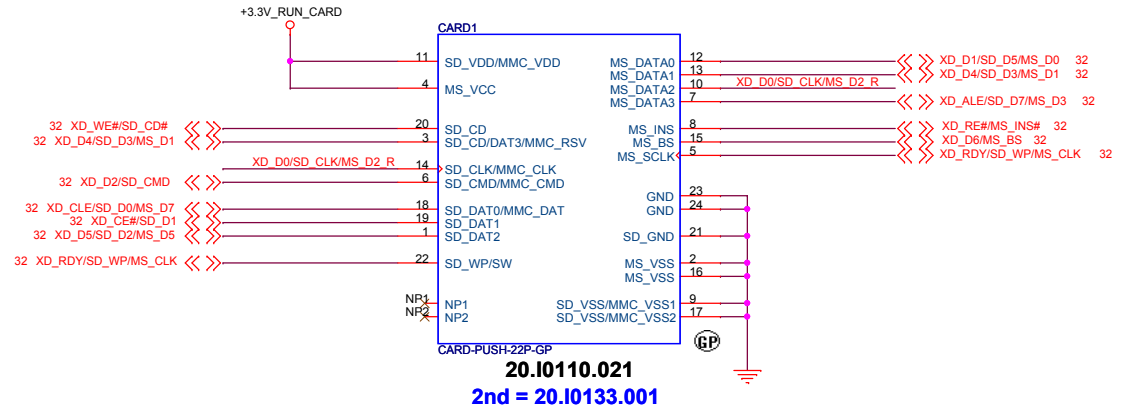
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size	Document Number	Rev
A3	DV14 CP UMA+DIS	X00
Date:	Thursday, January 06, 2011	Sheet 73 of 100

SSID = SDIO

SD/XD/MS Card Reader

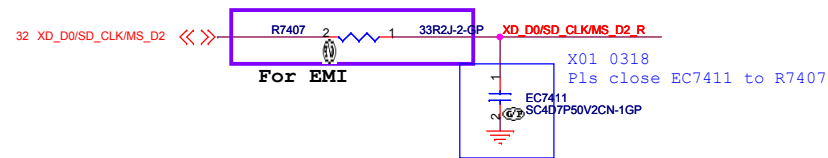
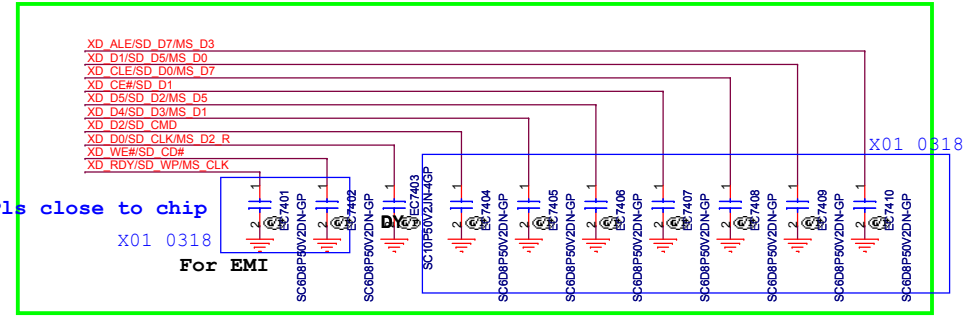


BOM merge Change 09/09



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0810 Vendor Recommend



<Core Design>




Title		
Reserved		
Size	Document Number	Rev
A3	DV14 CP UMA+DIS	X00
Date:	Wednesday, March 23, 2011	Sheet 74 of 100

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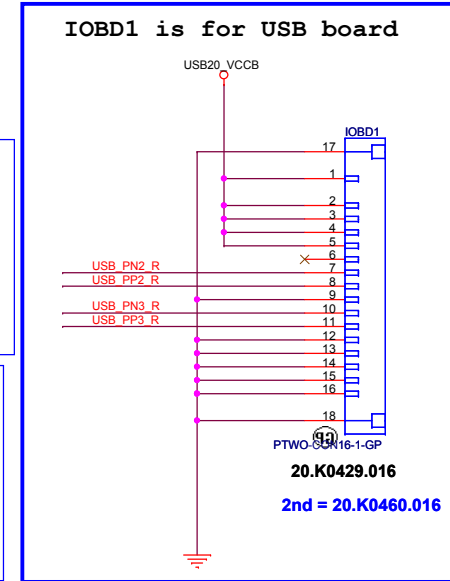
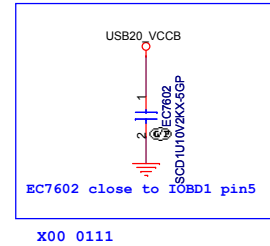
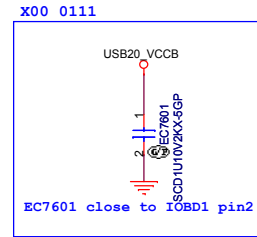
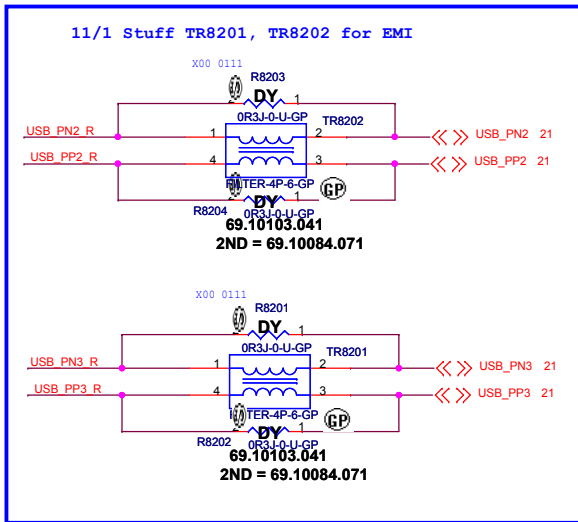
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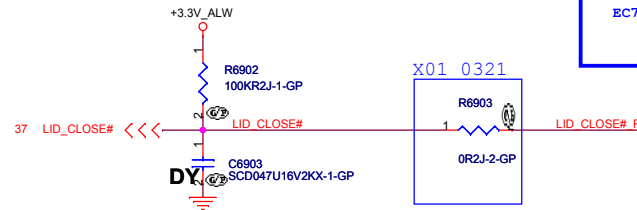
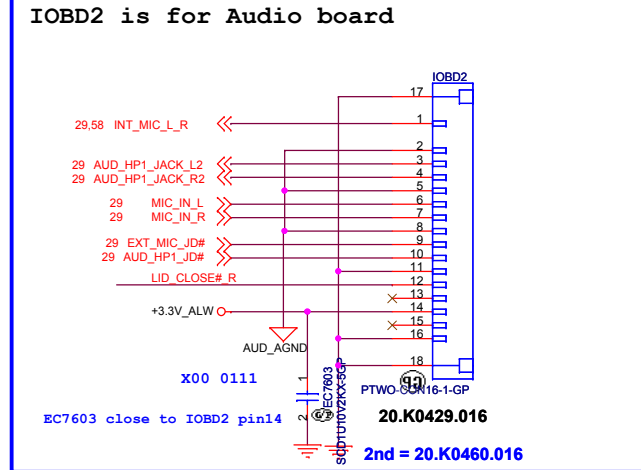
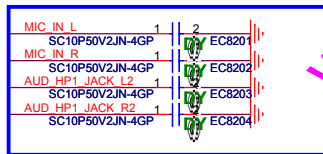
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Title			
Reserved			
Size	Document Number	Rev	
A3	DV14 CP UMA+DIS	X00	
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SSID = User.Interface



11/1 Add EC2901~EC2904 for EMI request



<Core Design>




Title		
IO Board		
Size A3	Document Number DV14 CP UMA+DIS	Rev X00
Date: Wednesday, March 23, 2011	Sheet 76	of 100

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Title			
Reserved			
Size	Document Number	Rev	
A3	DV14 CP UMA+DIS	X00	
Date:	Thursday, January 06, 2011	Sheet	77 of 100

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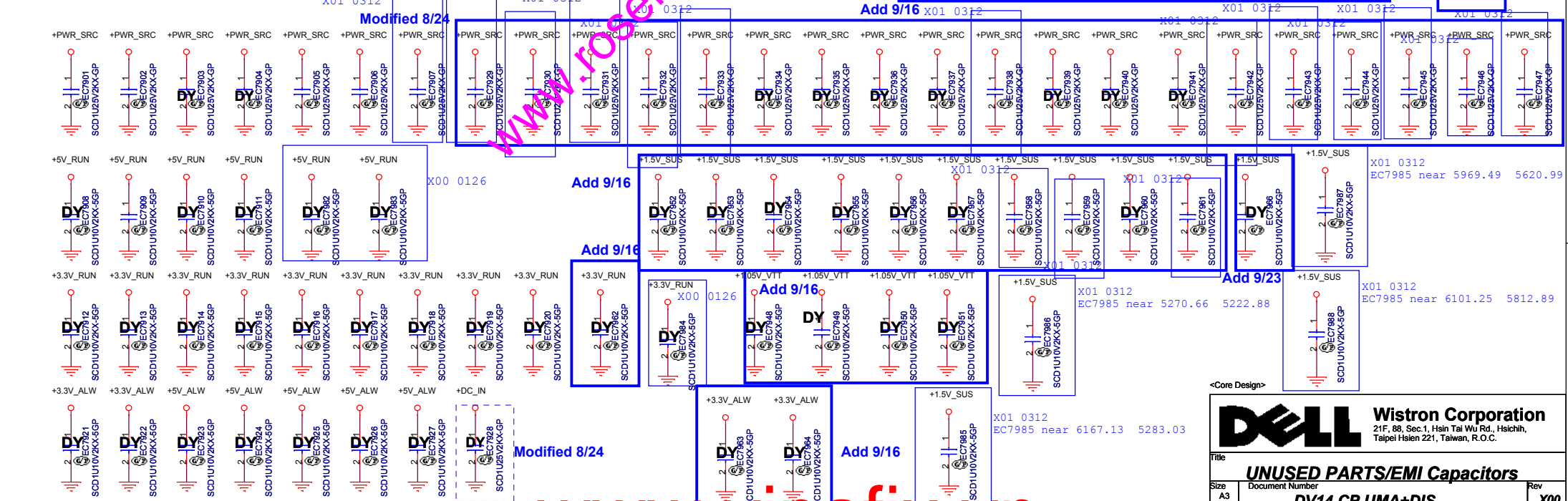
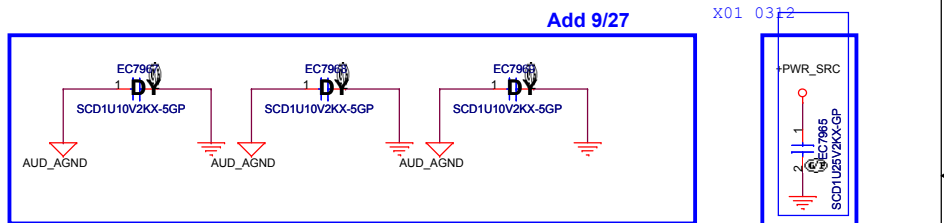
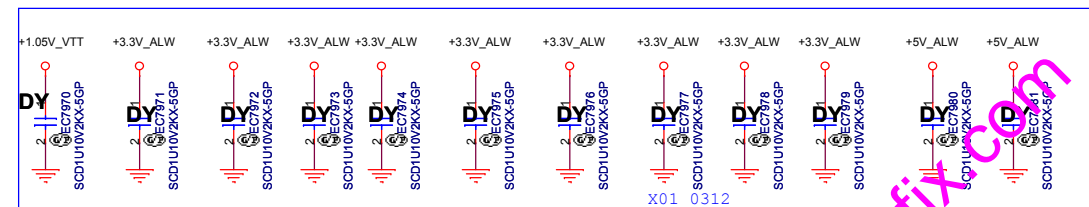
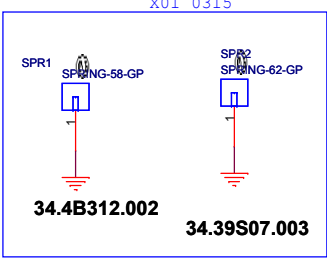
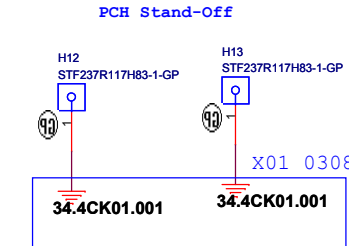
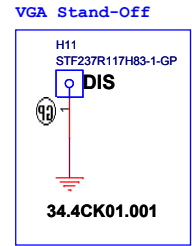
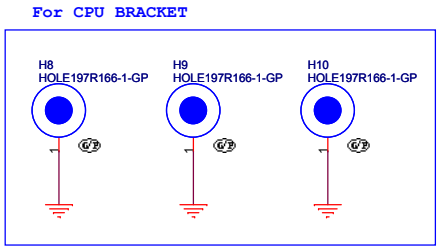
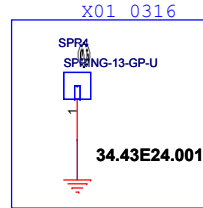
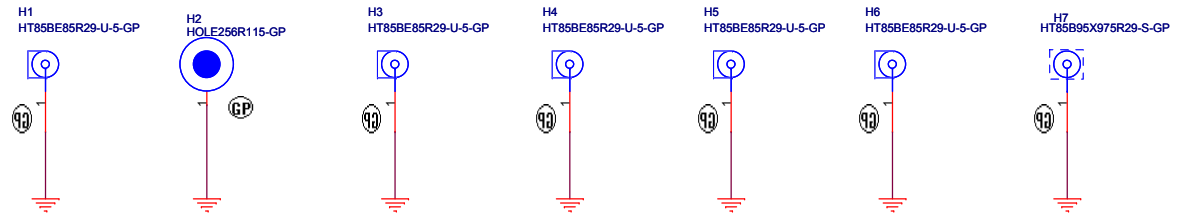
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Title			
Reserved			
Size A3	Document Number DV14 CP UMA+DIS	Rev X00	
Date: Thursday, January 06, 2011	Sheet 78	of 100	

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Title: **UNUSED PARTS/EMI Capacitors**

Size: A3	Document Number: DV14 CP UMA+DIS	Rev: X00
Date: Tuesday, March 22, 2011	Sheet: 79 of 100	

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<Core Design>

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Title		
Reserved		
Size	Document Number	Rev
A3	DV14 CP UMA+DIS	X00
Date:	Thursday, January 06, 2011	Sheet 80 of 100

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DELL **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.


Title		
Reserved		
Size	Document Number	Rev
A3	DV14 CP UMA+DIS	X00
Date:	Thursday, January 06, 2011	Sheet 81 of 100

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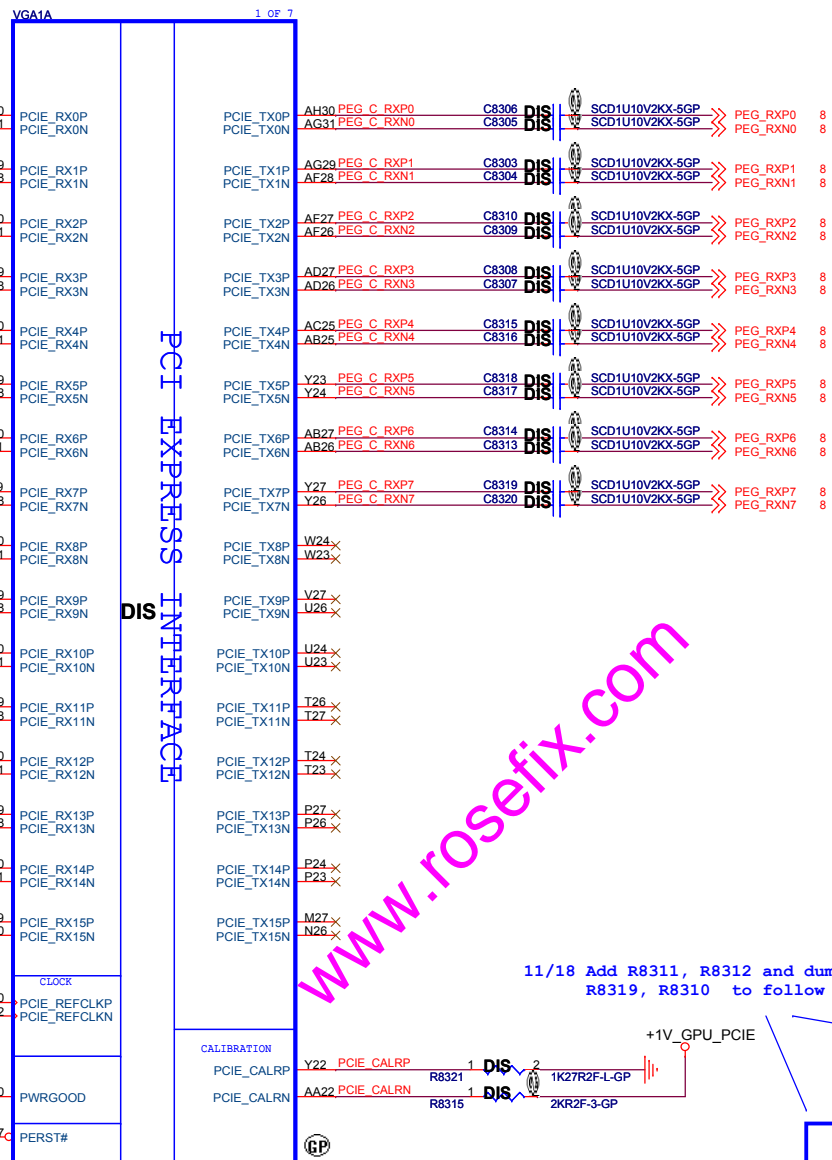
www.rosefix.com

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Title Reserved		
Size A3	Document Number DV14 CP UMA+DIS	Rev X00
Date: Thursday, January 06, 2011		Sheet 82 of 100

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SSID = VIDEO

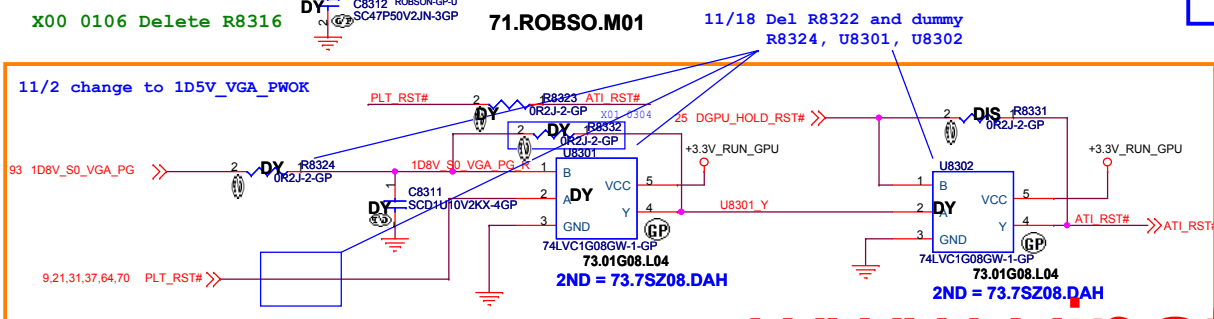
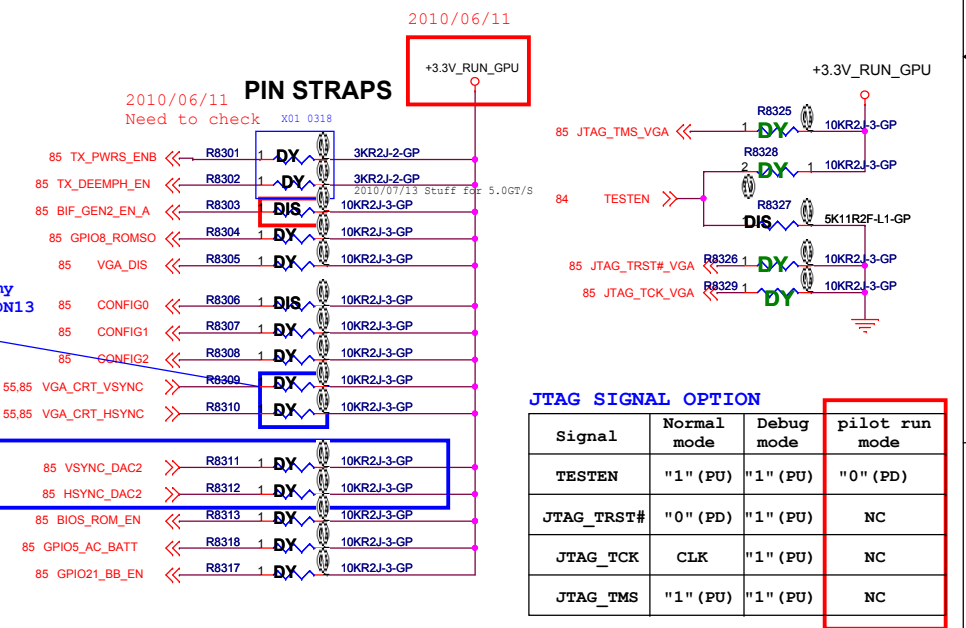


CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1= INSTALL 3K RESISTOR
X= DESIGN DEPENDANT
NA= NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	0
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.	?	0
GPIO8_ROMSO	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (2.5 6MB)
GPIO21_BB_EN	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSXNC		X	1



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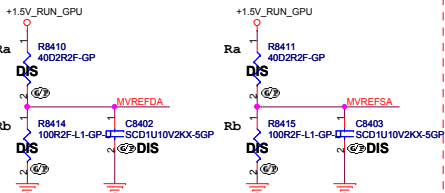
Title: **GPU PCIE/STRAPPING(1/5)**

Size A3 Document Number: **Enrico Caruso 14** Rev: **X00**

Date: Wednesday, March 23, 2011 Sheet 83 of 100

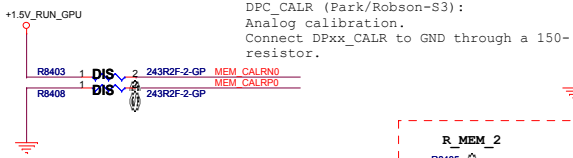
	PE_GPIO0
dGPU mode	H
IGPU	L
IGPU with BACC	H

PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC



DDR3/GDDR3 Memory Stuff Option (ROBSON-S3/SEYMOUR-XT-S3)

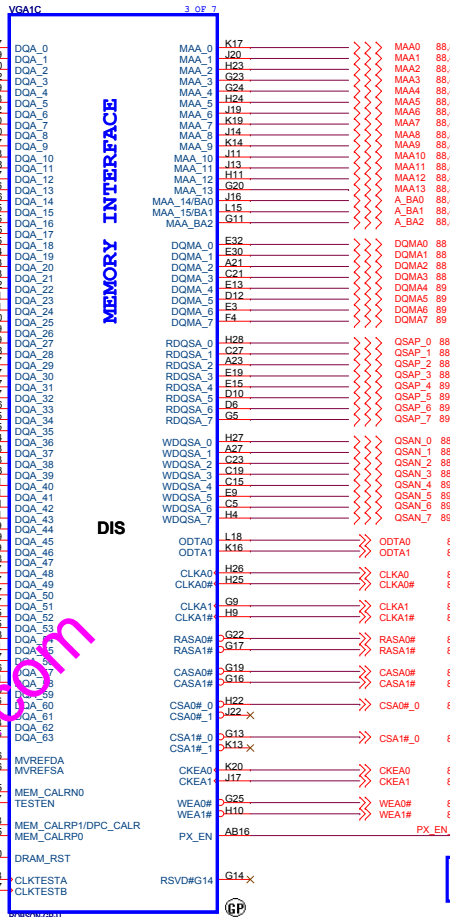
	DDR5	DDR3
MVDDQ	1.5V	1.5V/1.8V
Ra	40.2R	40.2R
Rb	100R	100R



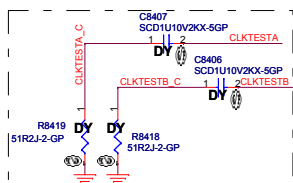
★ This basic topology should be used for DRAM RST for DDR3/GDDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory, DRAM Load and board to pass Reset Signal Spec.

Designator	For SEYMOUR	For Robson
R_MEM_1	10R	10R
R_MEM_2	50R	50R
R_MEM_3	5K	5K
C_MEM	120pF	120pF

Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except R_MEM_2



71.ROBSO.M01



For normal GPU operation, these signals can be left floating (do not populate the capacitors and resistors).

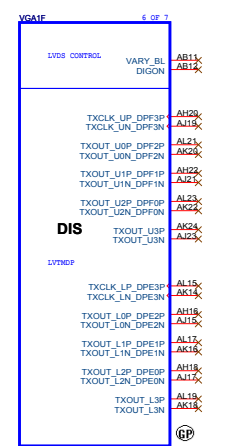
2010/07/06
Schematics check list:
A pull-down resistor is required.

R8441
10KR2J-3-GP
11/16 change part reference to R8441 and stuff
11/18 move R8441 before R8440

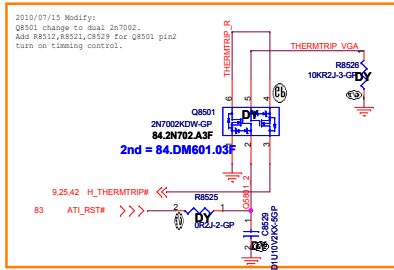
MEMORY ID Table	
DVPDATA [3:0]	Description
0000	DDR3 SAMSUNG-K4W1G1646G-BC11 (900MHz) 64M*16
0001	DDR3 Hynix-H5TQ1G63DFR-11C (900MHz) 64M*16
0010	DDR3 SAMSUNG K4W2G1646C-HC11 (900MHz) 128M*16
0011	DDR3 Hynix-H5TQ2G63BFR-11C (900MHz) 128M*16

SSID = VIDEO

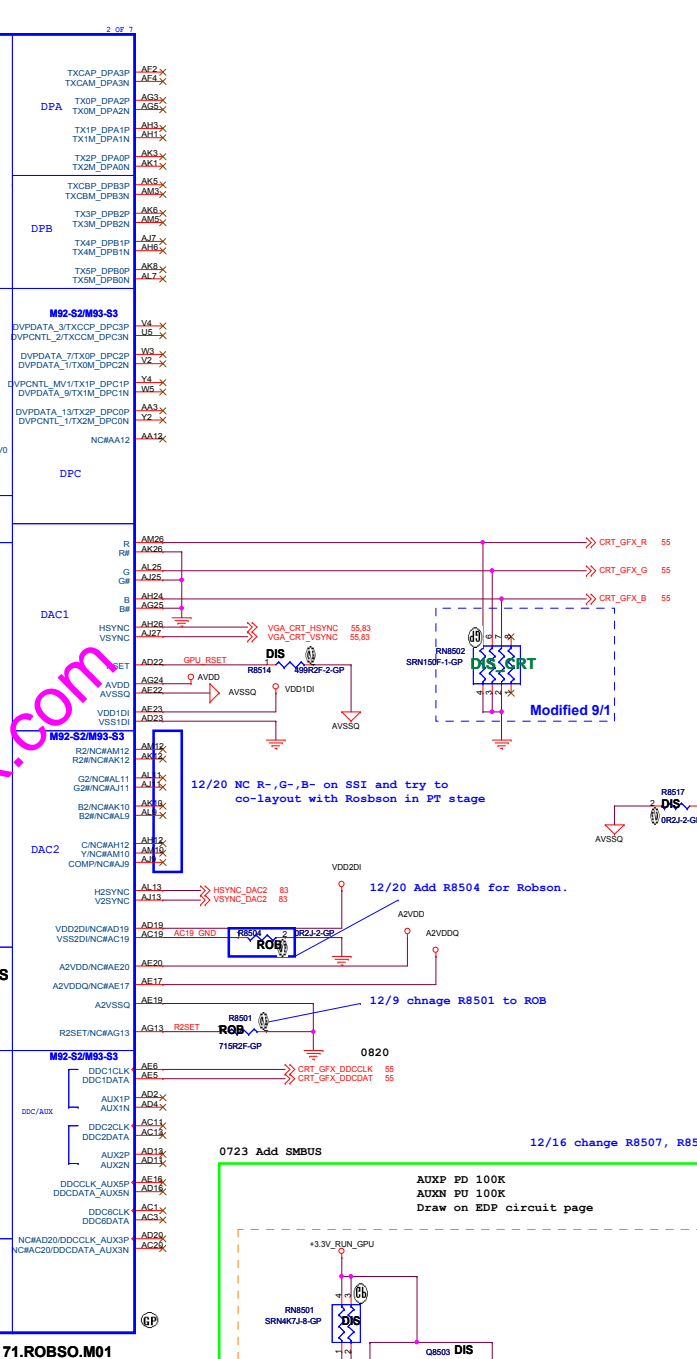
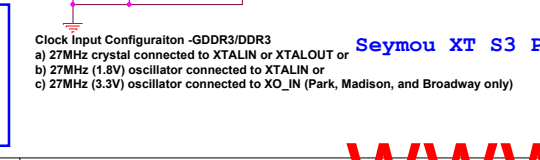
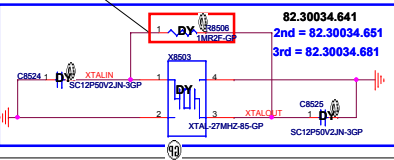
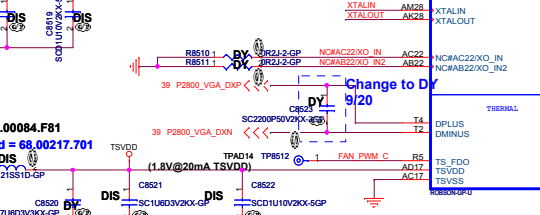
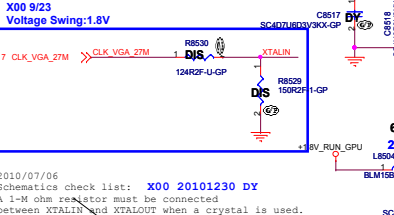
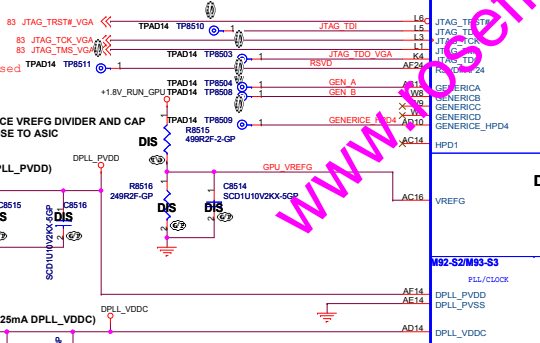
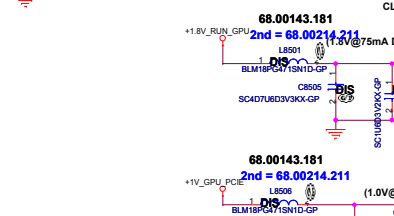
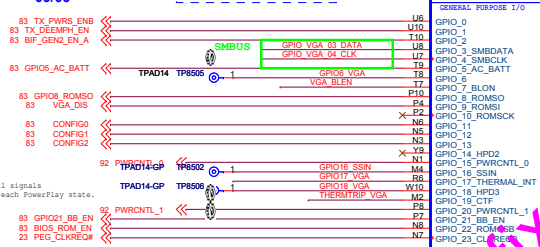
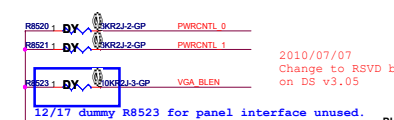
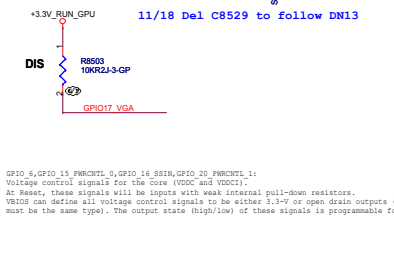
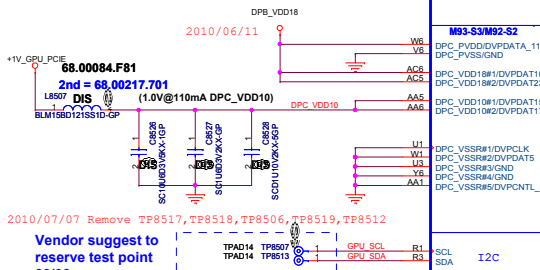
LVDS Interface



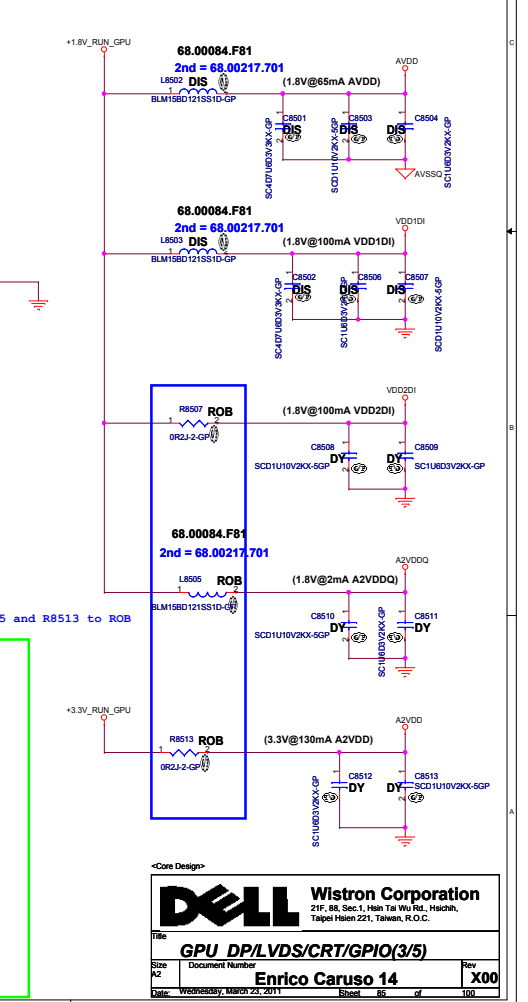
For Seymour,
 DPC_VDD18 is DPC_VDD18 2010/06/11
 DPC_VSS8 and all DPC_VSSR are DP_VSSR



MEM_ID Control

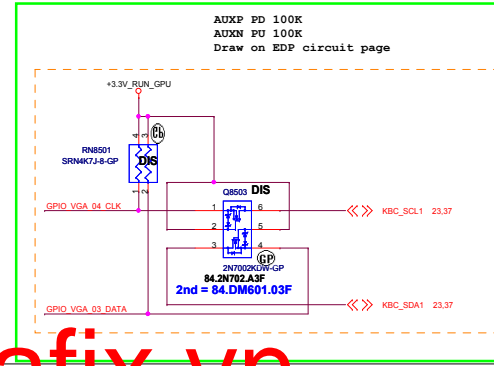


71.ROBSO.M01



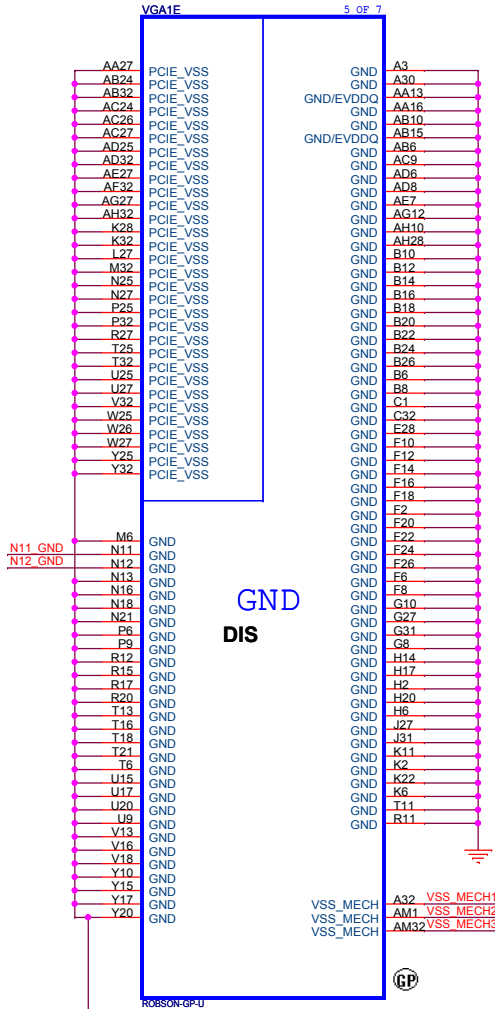
Schematics check list: X00 20101230 DY
 A 1-ohm resistor must be connected between XTALIN and XTALOUT when a crystal is used.

Clock input Configuration -GDDR3/DDR3
 a) 27MHz crystal connected to XTALIN or XTALOUT or
 b) 27MHz (1.8V) oscillator connected to XTALIN or
 c) 27MHz (3.3V) oscillator connected to XO_IN (Park, Madison, and Broadway only)



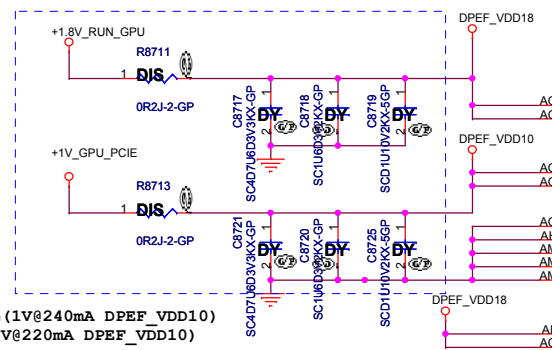
<Core Design>
DELL Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 221, Taiwan, R.O.C.
 Document Number: **GPU DP/LVDS/CRT/GPIO(3/5)**
 Rev: **Enrico Caruso 14**
 Date: Wednesday, March 24, 2010 Sheet: 62 of 100

SSID = VIDEO



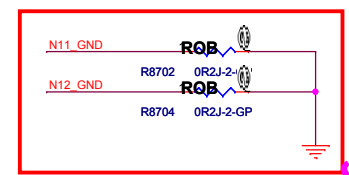
71.ROBSO.M01

Vendor suggest 09/23
LVDS mode (1.8V@440mA DPEF_VDD18)
DP mode (1.8V@300mA DPEF_VDD18)

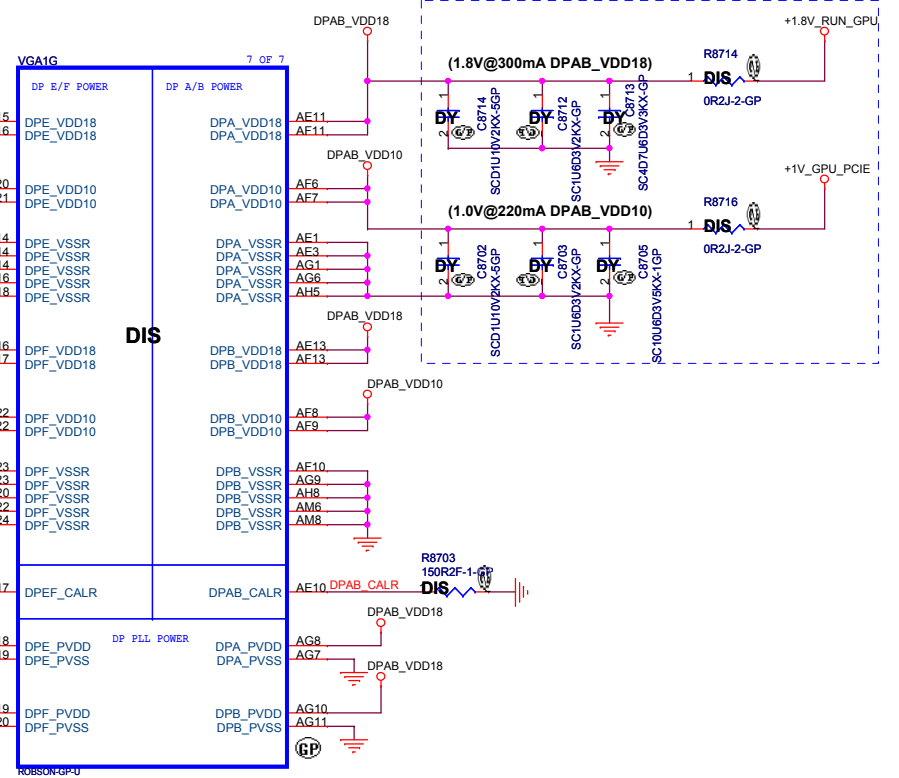


LVDS mode (1V@240mA DPEF_VDD10)
DP mode (1V@220mA DPEF_VDD10)

2010/07/09 N11 and N12: in Seymour is NC

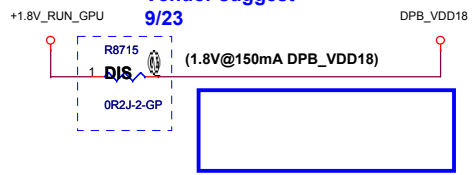


Vendor suggest 09/23



71.ROBSO.M01

Vendor suggest 9/23



11/18 Del R8709, C8710, C8711

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Title: **GPU DPPWR/GND(5/5)**

Size A3 Document Number: **Enrico Caruso 14** Rev: **X00**

Date: Tuesday, March 22, 2011 Sheet 87 of 100

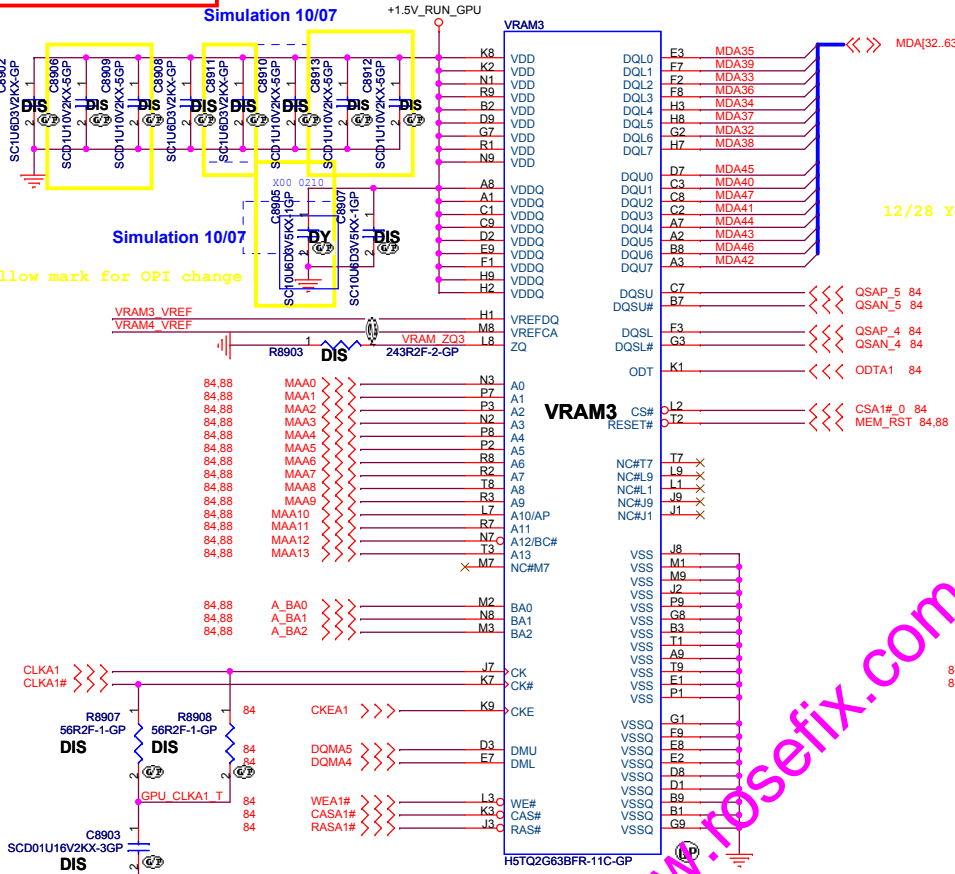
SSID = VIDEO

Simulation 10/07

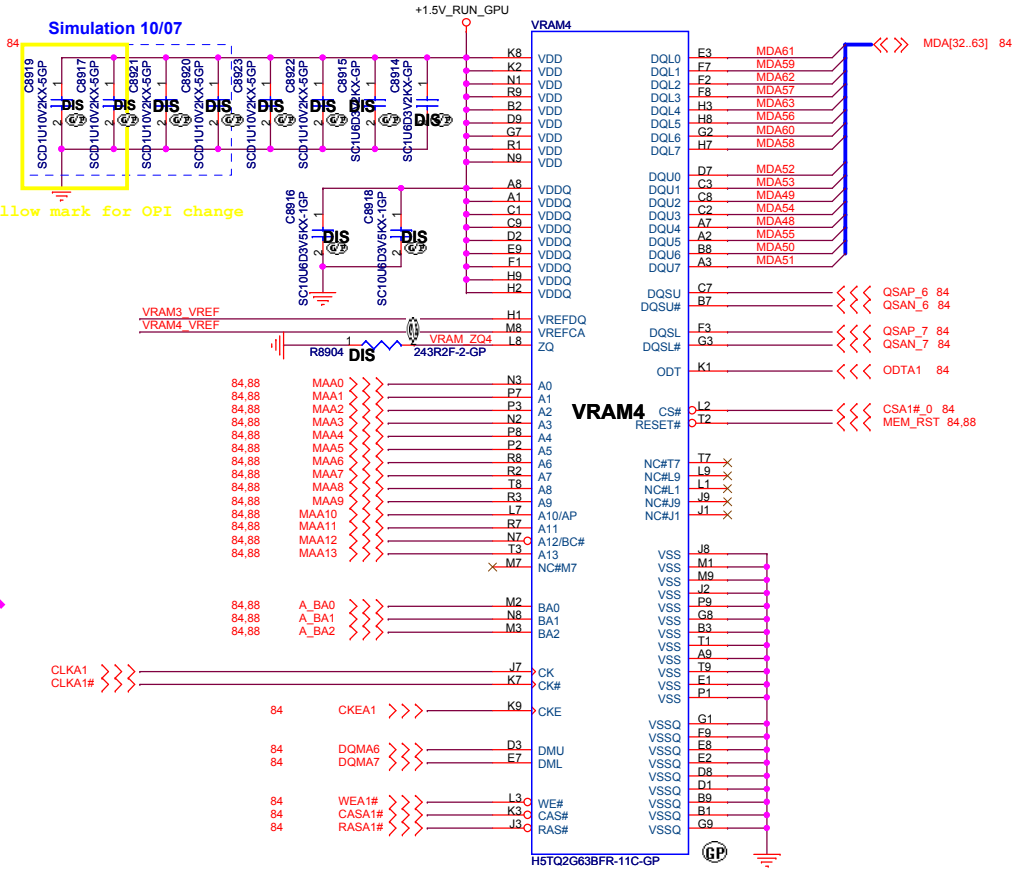
Simulation 10/07

12/28 Yellow mark for OPI change

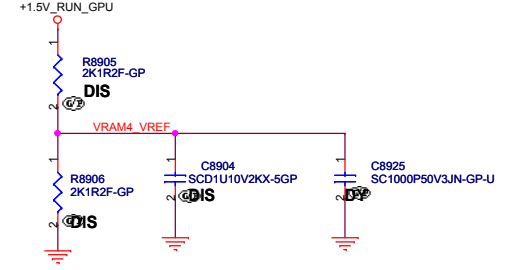
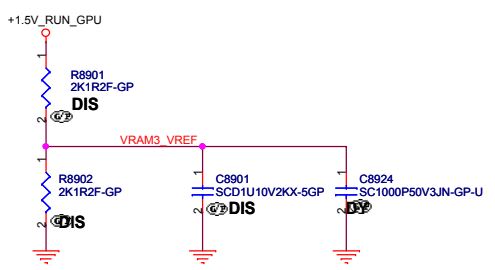
12/28 Yellow mark for OPI change



72.52G63.A0N



72.52G63.A0U



<Core Design>

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Title: **GPU-VRAM3,4 (2/4)**


Size: Custom Document Number: **Enrico Caruso 14** Rev: **X00**

Date: Wednesday, March 23, 2011 Sheet: 89 of 100

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<Core Design>

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Title		GPU-VRAM5,6 (3/4)	
Size A3	Document Number	Rev X00	
Date: Thursday, January 06, 2011	Sheet 90	of	100

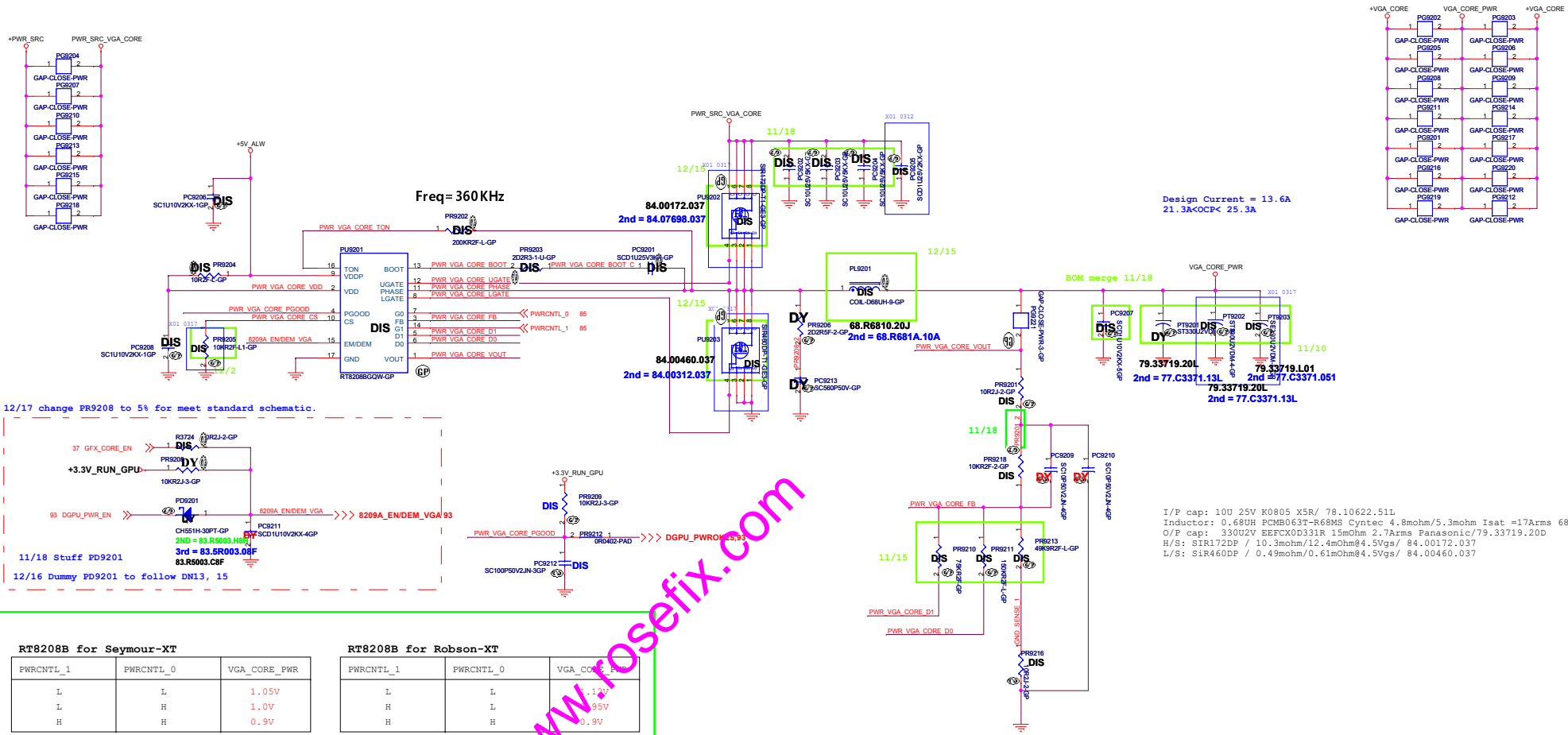
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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		GPU-VRAM7,8 (4/4)	
Size A3	Document Number	Rev X00	
Date: Thursday, January 06, 2011	Sheet 91	of	100

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12/17 change PR9208 to 5% for meet standard schematic.

37 GFX_CORE_EN >>> R3724 10KR2J-2-GP
 +3.3V_RUN_GPU >>> PR9202 10KR2J-3-GP
 93 DGPU_PWR_EN >>> PD9201
 8209A ENDEM_VGA >>> 8209A ENDEM_VGA 93
 CH551H-30PT-1-GP
 2ND = 83.R5003.04F
 3rd = 83.ER003.04F
 83.R5003.C8F

11/18 Stuff PD9201
 12/16 Dummy PD9201 to follow DM13, 15

Design Current = 13.6A
 21.3A < OCP < 25.3A

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: 0.680UH PCMB063T-R68MS Cynotec 4.8mohm/5.3mohm Isat =17Arms 68.R6810.20J
 O/P cap: 330U2V EEFCX0D331R 15mOhm 2.7Arms Panasonic/79.33719.20D
 H/S: SIR172DF / 10.3mohm/12.4mOhm@4.5Vgs/ 84.00172.037
 L/S: SIR460DF / 0.49mohm/0.61mOhm@4.5Vgs/ 84.00460.037

RT8208B for Seymour-XT

PWRCNTL_1	PWRCNTL_0	VGA_CORE_PWR
L	L	1.05V
L	H	1.0V
H	H	0.9V

RT8208B for Robson-XT

PWRCNTL_1	PWRCNTL_0	VGA_CORE_PWR
L	L	1.12V
L	H	0.95V
H	H	0.9V

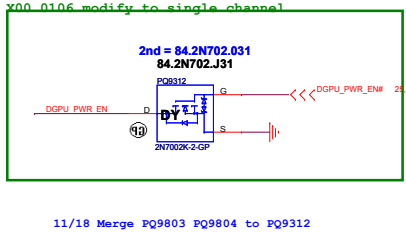
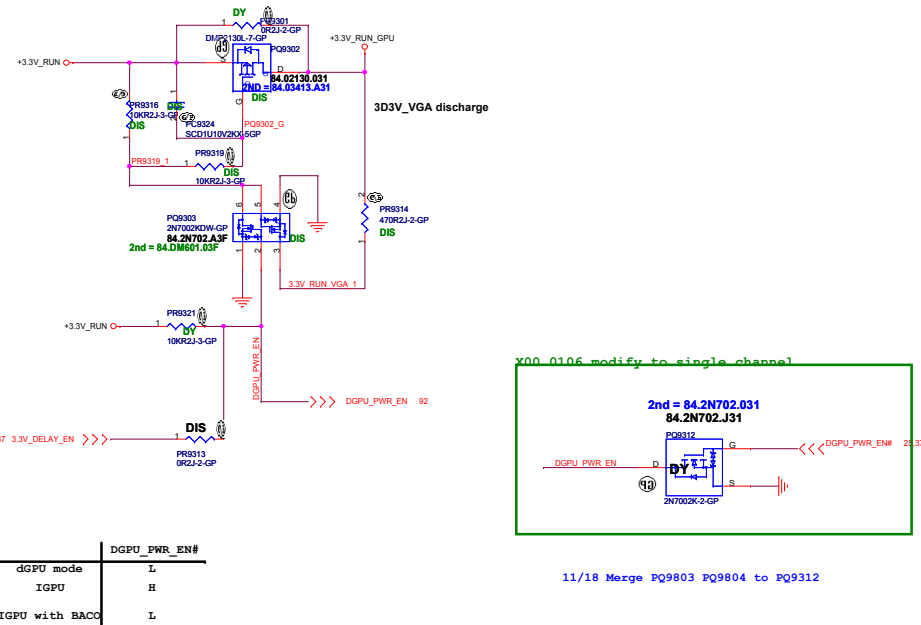
For Robson:
 PR9218=10K
 PR9213=49.9K
 PR9211=150K
 PR9210=44.2K

$$V_{out} = 0.75V * (R1 + R2) / R2$$

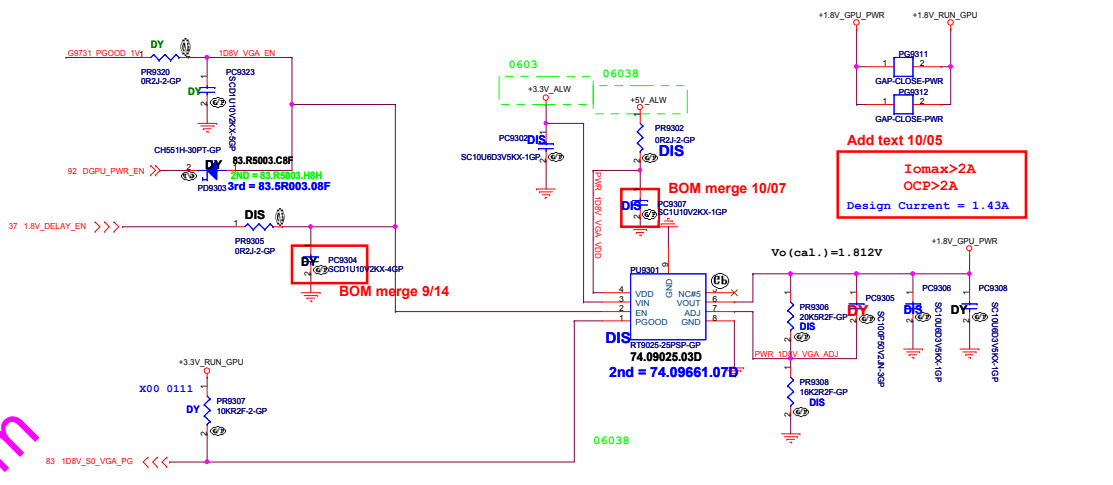
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3D3V_S0 to 3D3V_VGA_S0 Transfer

Change DUMMY Reference Name to PX_BACO

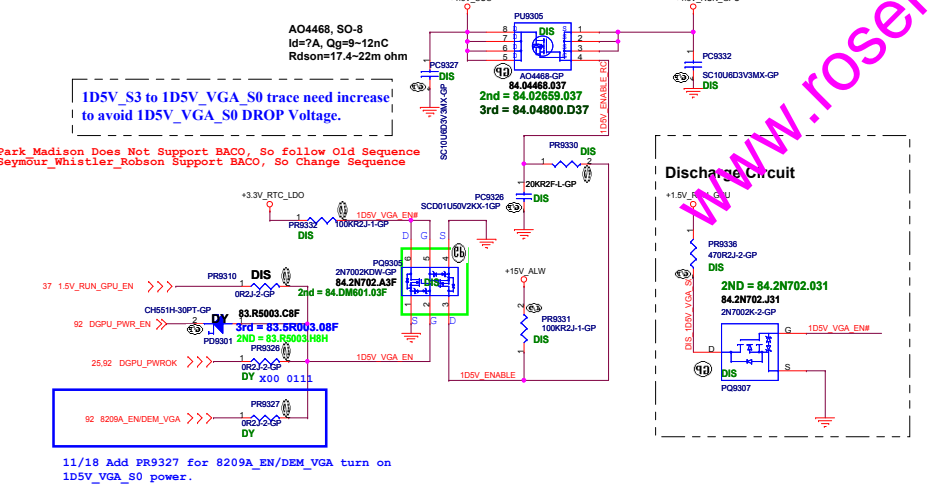


+1.8V_RUN_GPU

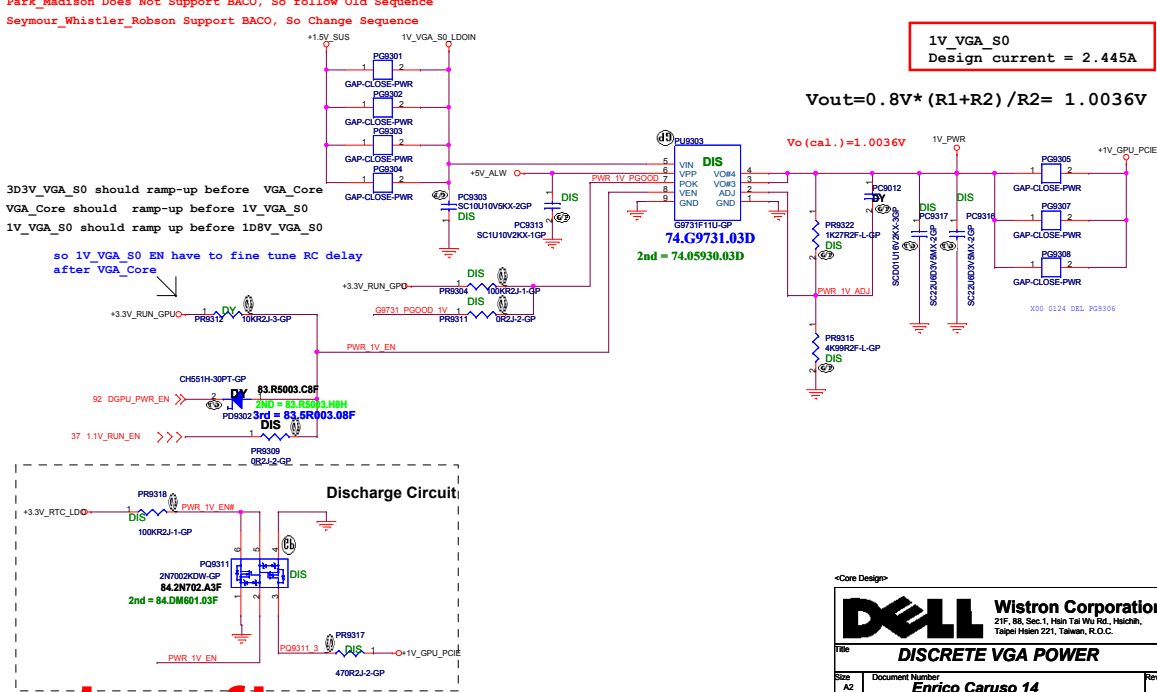


I_{omax} > 2A
OC_P > 2A
Design Current = 1.43A

1D5V_VGA_S0



G9731 for 1V_VGA_S0



1V_VGA_S0
Design current = 2.445A

$$V_{out} = 0.8V * (R1+R2) / R2 = 1.0036V$$

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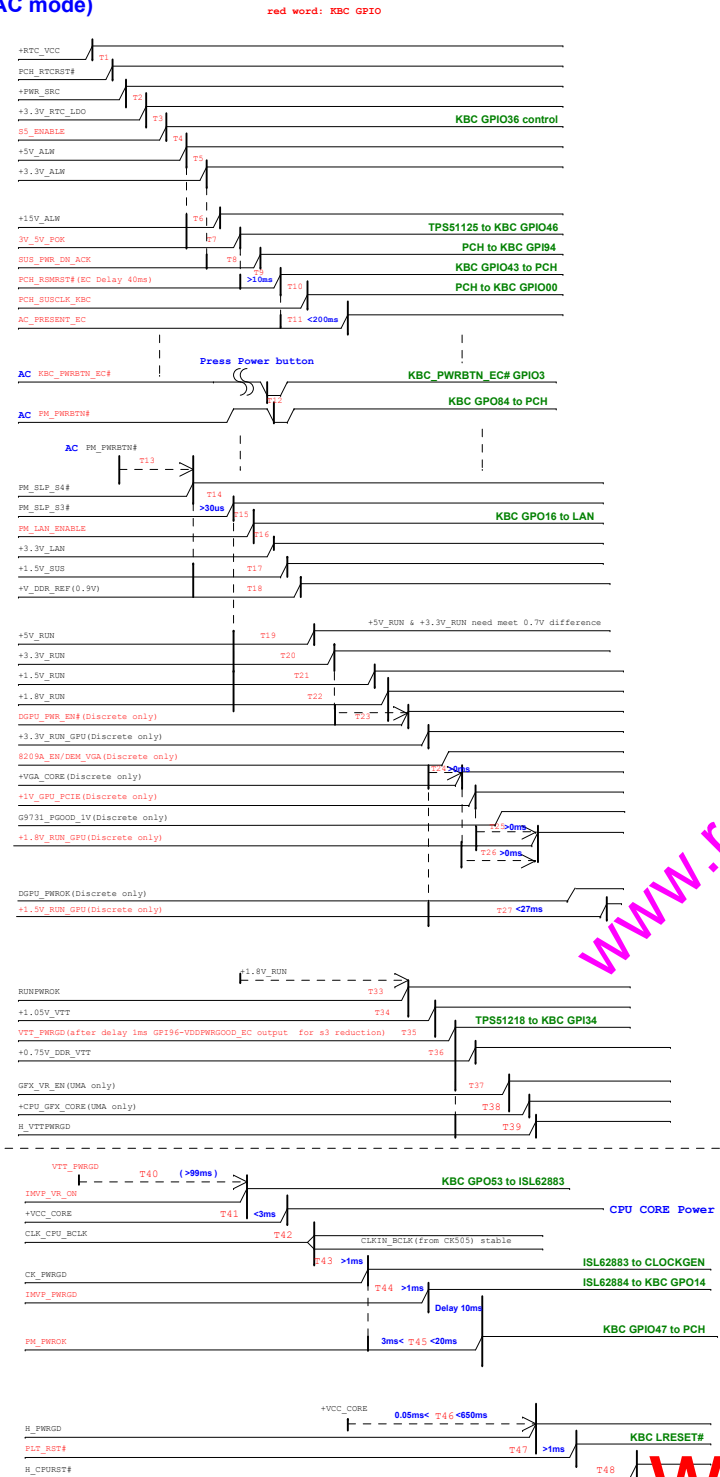
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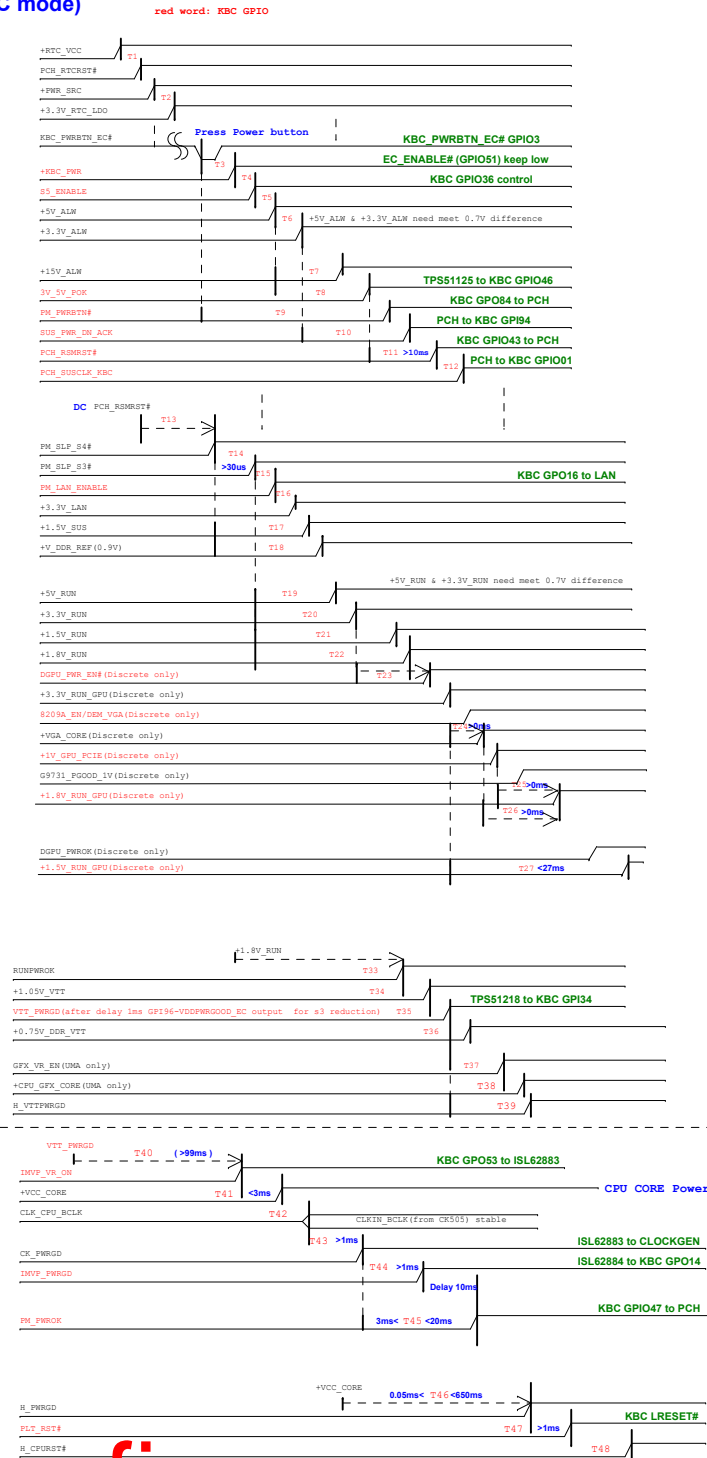
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DV14 Calpella UMA&DIS Power Up Sequence

(AC mode)



(DC mode)



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