1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM,MLB_BAFFIN2

LAST CHANGE: 2016-10-30 PROTO1A : PRELIMINARY TEST

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
10	000689**8975**	ENGINEERING RELEASED	2016-10-30

DRAWING

TITLE=MLB_BAFFIN2
ABBREV=ABBREV

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-00**789**	1	SCHEM,MLB-BAFFIN2	SCH	CRITICAL	
820-00**928**	1	PCBF,MLB-BAFFIN2	PCB	CRITICAL	

DRAWING TITLE: SCHEM,MLB-BAFFIN2

Apple Inc.

DRAWING NUMBER: 051-00789 SIZE: D
REVISION: PROTO1A
BRANCH: dvt-fab10
PAGE: 1 OF 145
SHEET: 1 OF 121

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00123	COMMON PARTS,MLB-BAFFIN2	BAFFIN2_COMMON
985-00137	DEV,MLB-BAFFIN2	BAFFIN2_DEVEL:PROTO1A
985-00264	DEV,MLB-BAFFIN2, PROTO1A	BAFFIN2_DEVEL:PROTO1A

GPU Options

BOM GROUP	BOM OPTIONS
2GB_MC_BAFFIN	FB_2GB_MICRON,VRAM:GRP1
2GB_HY_BAFFIN	FB_2GB_HYNIX,VRAM:GRP1
2GB_SM_BAFFIN	FB_2GB_SAMSUNG,VRAM:GRP2
4GB_SM_BAFFIN	FB_4GB_SAMSUNG,VRAM:GRP1
4GB_MC_BAFFIN	FB_4GB_MICRON,VRAM:GRP1

FB VDRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S00044	4	IC,GDDR5,4Gb,7Gbps,1.5V,25NM,A,170 BGA	UA400,UA450,UA500,UA550	CRITICAL	FB_2GB_MICRON
333S00043	4	IC,GDDR5,4Gb,7Gbps,1.5V,25NM,A,170 BGA	UA400,UA450,UA500,UA550	CRITICAL	FB_2GB_HYNIX
333S00078	4	IC,GDDR5,8Gb,7Gbps,1.5V,25NM,B,170 BGA	UA400,UA450,UA500,UA550	CRITICAL	FB_2GB_SAMSUNG
333S00074	4	IC,GDDR5,8Gb,7Gbps,1.5V,25NM,B,170 BGA	UA400,UA450,UA500,UA550	CRITICAL	FB_4GB_SAMSUNG
333S00075	4	IC,GDDR5,8Gb,7Gbps,1.5V,25NM,A,170 BGA	UA400,UA450,UA500,UA550	CRITICAL	FB_4GB_MICRON

Sub-BOM DIPLEXER

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00085	DIPLEXERS,MURATA,X363G	DIPLEXER:MURATA

Main DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S00050	4	IC,SDRAM,LPDDR3-2133,32GBIT,20NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	16G_SAMSUNG_2133
333S00070	4	IC,SDRAM,LPDDR3-2133,32GBIT,20NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	16G_MICRON_2133

Main DRAM SPD Straps

BOM GROUP	BOM OPTIONS
RAM_16G_SAMSUNG_2133	16G_SAMSUNG_2133,RAMCFG4:L,RAMCFG3:L,RAMCFG0:L
RAM_16G_MICRON_2133	16G_MICRON_2133,RAMCFG4:L,RAMCFG3:L,RAMCFG1:L

BAFFIN2 BOM Groups

BOM GROUP	BOM OPTIONS
BAFFIN2_COMMON	ALTERNATE,COMMON,BAFFIN2_COMMON1,BAFFIN2_COMMON2,BAFFIN2_COMMON3,BAFFIN2_COMMON4,BAFFIN2_PROGPARTS
BAFFIN2_COMMON1	SOC:HYNIX,SE:PROD,SKIP_5V3V3:AUDIBLE,DIPLEXER:MURATA,T208_PROG:REV5,BOARD_ID:17,VCCHDA:S0
BAFFIN2_COMMON2	XDP:YES,SAMCONN,SOC_BOOT:SPI,DPMUX_XTAL:NO,GPUCLK:OSC,BAFFIN,AP_TEMP,VCCPLLOC:S3,WIFI_SAK:NO
BAFFIN2_COMMON3	CPUTHRM:ALRT,TBTTHRM:ALRT,LOADRC:NO,OTHERRC:YES,DDRRC:YES,TBTRC:YES,TPADRC:YES,LID_FEATURE_ON
BAFFIN2_COMMON4	EDP:YES,CPUPEG:X8X4X4,TBTTHRM_SNS,GPUTHRM_SNS,S3_STATE:YES,GPU_ROM:YES,SVID_PU:CORE
BAFFIN2_PROGPARTS	BOOTROM_PROG:DVT,BT_PROG:DVT,WIFI_PROG:DVT,UPCROM_PROG:DVT,SMC_PROG:PVT,DPMUXMCU:PROG,PCC:NO
BAFFIN2_DEVEL:ENG	ALTERNATE,ENGISNS,DBGLED,XDP_CONN,USBC_DBG,DBG_BTN,DBG_FAN,DBG_XTAL,DPMUX_DEBUG,WIFI_DBG,SSD_DEBUG,GPUROM:BLANK,PCC:YES
BAFFIN2_DEVEL:DVT	ALTERNATE,ENGISNS,DBGLED,XDP_CONN,USBC_DBG,DBG_BTN,DBG_FAN,DBG_XTAL,DPMUX_DEBUG,WIFI_DBG,SSD_DEBUG
BAFFIN2_DEVEL:PVT	ALTERNATE,XDP_CONN,USBC_DBG
ENGISNS	TBTISNS,LOADISNS,TPADISNS,DDRISNS,OTHERISNS

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00248	1	CPU,KBL,SR32Q,R1,PRQ,4/2,2.8,BGA1440	U0500	CRITICAL	CPU_KBL:2.8
337S00249	1	CPU,KBL,SR32N,R1,PRQ,4/2,2.9,BGA1440	U0500	CRITICAL	CPU_KBL:2.9
337S00250	1	CPU,KBL,SR32L,R1,PRQ,4/2,3.1,BGA1440	U0500	CRITICAL	CPU_KBL:3.1
998-04701	1	INTERPOSER,INTEL,BGA1440,MM040989	U0500	CRITICAL	CPU_KBL:SOCKET
337S00258	1	IC,SKL PCH-H,SFF,SR2NH,PRQ,D1,BGA939	U1100	CRITICAL	
353S00961	4	IC,CD3215,ACE,C0,USB PWR SW,BLNK,BGA96	U3100,U3200,UB300,UB400	CRITICAL	
338S00254	2	IC,TBT,ALPINE RIDGE DP,QT5S,QS,C1,BGA337	U2800,UB000	CRITICAL	
353S01016	1	IC,ISL9239HIZ,PMU,TUBA,WCSP40,2.1X3.3MM	U7000	CRITICAL	
338S00221	1	IC,PMU,P650839,7X7MM.BGA168	U7800	CRITICAL	
338S00142	1	IC,CODEC,CLIFDEN,CS42L83A,B0,WLCSP49	U6300	CRITICAL	
337S00330	1	IC,GPU,BAFFIN,ULA,A1,PS,BGA769	UA000	CRITICAL	BAFFIN_ULA
337S00331	1	IC,GPU,BAFFIN,PROA,A1,PS,BGA769	UA000	CRITICAL	BAFFIN_PROA
337S00332	1	IC,GPU,BAFFIN,LEA,A1,PS,BGA769	UA000	CRITICAL	BAFFIN_LEA
998-04866	1	INTERPOSER,AMD,C989,BGA769,VDDCI/MVDD	UA000	CRITICAL	STARDUST:VDDCI_MVDD
998-04867	1	INTERPOSER,AMD,C988,BGA769,VDDC	UA000	CRITICAL	STARDUST:VDDC
677-04532	2	SUBASSY (T&R) PCBA, AMR, INTERPOSER, BAF2	J5250,J5260	CRITICAL	

Development/Base BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-00076	1	COMMON PARTS,MLB-BAF2	BASE	CRITICAL	BASE_BOM
985-00126	1	DEV,MLB-BAF2	DEVEL	CRITICAL	DEVEL_BOM

WIFI/BT Diplexers

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
155S0979	3	FLTR,DIPLEXER,2.45/5.54GHZ,0805	U3810,U3820,U3830	CRITICAL	DIPLEXER:MURATA

Strategic Silicon

PART#	STRATEGIC VALUE	COMMENT
337S00227	08	CPU
337S00228	08	CPU
337S00229	08	CPU
333S00050	07	MAIN MEMORY
333S00070	07	MAIN MEMORY
335S00149	02	SSD NAND
335S00204	02	SSD NAND
335S00205	02	SSD NAND
335S00219	02	SSD NAND
339S00154	02	SSD CONTROLLER
339S00155	02	SSD CONTROLLER
338S00166	02	SSD PMIC
337S00225	08	GPU
337S00285	08	GPU
337S00286	08	GPU
333S00044	07	VIDEO MEMORY
333S00043	07	VIDEO MEMORY
333S00078	07	VIDEO MEMORY
333S00074	07	VIDEO MEMORY
333S00075	07	VIDEO MEMORY
343S00135	10	T208
343S00136	10	T208
343S00137	10	T208
338S00138	10	T208
338S00193	09	BERKELIUM
353S3978	02	MOJAVE
338S00097	02	SECURE ELEMENT
338S00254	08	ALPINE RIDGE
353S00961	09	ACE
338S00142	09	CLIFDEN
353S00604	07	AUDIO AMP
353S4316	08	BAYSIDE
338S00221	08	BANJO
353S00853	09	TUBA
339S00056	05	ICEBOCK
359S00006	08	GREEN CLOCK
353S00795	09	DEBUG MUX

SYNC_MASTER=J80_MLB SYNC_DATE=07/07/2015

PAGE TITLE

BOM Configuration

Apple Inc.

DRAWING NUMBER 051-00789 SIZE D

REVISION PROTO1A

BRANCH dvt-fab10

PAGE 2 OF 145

SHEET 2 OF 121

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
338S1231	1	IC,SMC12,40MHZ/50DMIPS MCU,7X7,168BGA	U5000	CRITICAL	SMC_PROG:BLANK	Blank
341S00701	1	IC,SMC-B1,EXT (v2.37F7) PROTO1A,BAFFIN2	U5000	CRITICAL	SMC_PROG:PVT	TI
335S00013	1	IC,SPI SERIAL FLASH,64M BITS,3V,8P SOIC,QE=1	U6100	CRITICAL	BOOTROM_PROG:BLANK	Blank
341S00699	1	IC,EFI ROM (V0193), PROTO1A,BAFFIN2	U6100	CRITICAL	BOOTROM_PROG:DVT	Macronix/Winbond
353S00926	2	IC,CD3215,ACE,B03,BLNK,BGA96	U2890,UB090	CRITICAL	UPCROM_PROG:BLANK	Blank
341S00707	1	T29,AR1 (V10.5) PROTO1A,BAFFIN2	U2890	CRITICAL	UPCROM_PROG:DVT	Winbond
341S00708	1	T29,AR2 (V10.5) PROTO1A,BAFFIN2	UB090	CRITICAL	UPCROM_PROG:DVT	Winbond
335S00024	1	IC,SERIAL-FLASH,2MBIT,4V,8-USON,2x3x,6MM	U3750	CRITICAL	BT_PROG:BLANK	Blank
341S00695	1	IC,BT ROM (V28), PROTO1A, BAFFIN/BAFFIN2	U3750	CRITICAL	BT_PROG:DVT	Macronix/Winbond
341S00709	1	WIFI ROM (P107) DVT,NEW,WW1,BAFFIN/BAFFIN2	U3710	CRITICAL	WIFI_PROG:DVT	Rohm/On Semi
341S3565	1	IC, EDP MUX-95C, (RENESAS) V3.2.8,DVB,D2	U9800	CRITICAL	DPMUXMCU:PROG	
335S0724	1	IC,1Mbit SERIAL FLASH 2X3X0.6MM UFDFPN8 PKG	UA701	CRITICAL	GPUROM:BLANK	Blank

SYNC_MASTER=J20_MLB_BRYCE_2.2.0A SYNC_DATE=11/30/2020

PAGE TITLE

BOM Configuration

Apple Inc.

DRAWING NUMBER 051-00789 | SIZE D

REVISION PROTO1A

BRANCH dvt-fab10

PAGE 3 OF 145

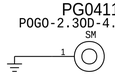
SHEET 3 OF 121

Pogo Pins

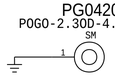
APN 870-01771

PG0410
POGO-2.30D-4.63H-SM

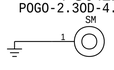
PG0411
POGO-2.30D-4.63H-SM



PG0420
POGO-2.30D-4.63H-SM



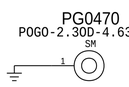
PG0421
POGO-2.30D-4.63H-SM



PG0430
POGO-2.30D-4.63H-SM

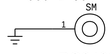
PG0471
POGO-2.30D-4.63H-SM

PG0470
POGO-2.30D-4.63H-SM

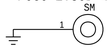


APN 870-01772

PG0400
POGO-2.30D-4.06H-SM



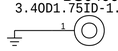
PG0401
POGO-2.30D-4.06H-SM



SMT Bosses

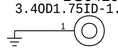
APN 860-00392

BS0400
3.40D1.75ID-1.12H-SM



USB-C Left
BOT side - North

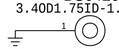
BS0410
3.40D1.75ID-1.12H-SM



USB-C Right
BOT side - North

APN 806-06520

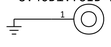
BS0420
3.40D1.75ID-1.45H-SM



DFR Touch
BOT side

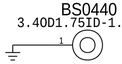
APN 806-06521

BS0430
3.40D1.75ID-1.9H-SM



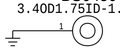
DFR Display
BOT side - Left

BS0440
3.40D1.75ID-1.9H-SM



Keyboard
BOT side - Left

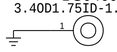
BS0450
3.40D1.75ID-1.9H-SM



Trackpad
BOT side - Left

APN 860-00413

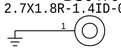
BS0460
3.40D1.75ID-1.57H-SM



Lifeboat
BOT side - North

APN 860-00469

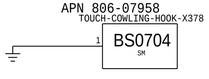
BS0470
2.7X1.8R-1.4ID-0.91H-SM



eDP
TOP side - Left

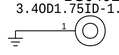
APN 806-07958
TOUCH-COWLING-HOOK-X378

BS0704
SM



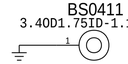
DFR Touch - TOP side

BS0401
3.40D1.75ID-1.12H-SM



USB-C Left
BOT side - South

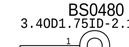
BS0411
3.40D1.75ID-1.12H-SM



USB-C Right
BOT side - South

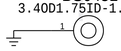
APN 806-06600

BS0480
3.40D1.75ID-2.12H-SM



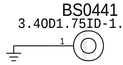
USB-C Right
BOT side - Left

BS0431
3.40D1.75ID-1.9H-SM



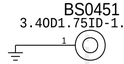
DFR Display
BOT side - Right

BS0441
3.40D1.75ID-1.9H-SM



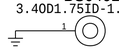
Keyboard
BOT side - Right

BS0451
3.40D1.75ID-1.9H-SM



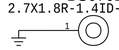
Trackpad
BOT side - Right

BS0461
3.40D1.75ID-1.57H-SM



Lifeboat
BOT side - South

BS0701
2.7X1.8R-1.4ID-0.91H-SM

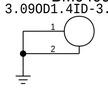


eDP
TOP side - Right

Rubber Mount Standoffs

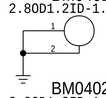
APN 860-00452

BM0400
3.09OD1.4ID-3.25H-SM

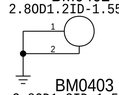


APN 860-00435

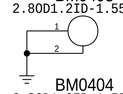
BM0401
2.8OD1.2ID-1.55H-SM



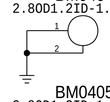
BM0402
2.8OD1.2ID-1.55H-SM



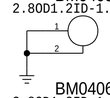
BM0403
2.8OD1.2ID-1.55H-SM



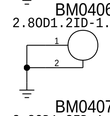
BM0404
2.8OD1.2ID-1.55H-SM



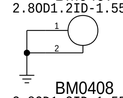
BM0405
2.8OD1.2ID-1.55H-SM



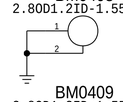
BM0406
2.8OD1.2ID-1.55H-SM



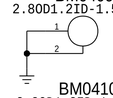
BM0407
2.8OD1.2ID-1.55H-SM



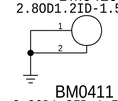
BM0408
2.8OD1.2ID-1.55H-SM



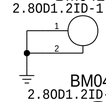
BM0409
2.8OD1.2ID-1.55H-SM



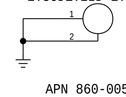
BM0410
2.8OD1.2ID-1.55H-SM



BM0411
2.8OD1.2ID-1.55H-SM

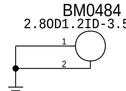


BM0483
2.8OD1.2ID-1.55H-SM



APN 860-00500

BM0484
2.8OD1.2ID-3.5H-SM



APN 860-00500

BM0485
2.8OD1.2ID-3.5H-SM

BM0486
2.8OD1.2ID-3.5H-SM

BM0487
2.8OD1.2ID-3.5H-SM

Shield Can TH

APN 998-2691

TH0400
TH-NSP

System Memory - BOT side - Left

TH0401
TH-NSP

System Memory - BOT side - Right

TH0410
TH-NSP

TBT Left - BOT side - North

TH0411
TH-NSP

TBT Left - BOT side - South

TH0420
TH-NSP

TBT Right - BOT side - North

TH0421
TH-NSP

TBT Right - BOT side - South

T208 - TOP side - North

T208 through holes are non-plated... for now

T208 - TOP side - South

TH0440
TH-NSP

SSD - BOT side - North

TH0441
TH-NSP

SSD - BOT side - South

TH0450
TH-NSP

SSD - TOP side - North

TH0451
TH-NSP

SSD - TOP side - South

TH0460
TH-NSP

Frame Buffer Memory - BOT side - Left

TH0461
TH-NSP

Frame Buffer Memory - BOT side - Right

Shield Can Fence

SH0400
SM

SHLD-FENCE-MLB-M8-X379

OMIT_TABLE
DRAM - BOT side
APN 806-06590

SH0410
SM

SHLD-FENCE-MLB-M8-X379

OMIT_TABLE
AR Right - BOT side
APN 806-06586

SH0420
SM

SHLD-FENCE-MLB-M8-X379

OMIT_TABLE
AR Left - BOT side
APN 806-06588

SH0430
SM

SHLD-FENCE-M8-X379

T208 - TOP side
APN 806-07814

SH0440
SM

SHLD-FENCE-MLB-M8-X379

OMIT_TABLE
SSD - TOP side
APN 806-06584

SH0450
SM

SHLD-FENCE-MLB-M8-X379

OMIT_TABLE
SSD - BOT side
APN 806-06585

SH0460
SM

SHLD-FENCE-MLB-M8-X379

OMIT_TABLE
Diplexer - BOT side
APN 806-06591

SH0470
SM

SHLD-FENCE-MLB-M8-X379

OMIT_TABLE
VRAM - BOT side
APN 806-08026

Shield Can Omit Table

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-08023	1	SHIELD,FENCE,DRAM,X378	SH0400	CRITICAL	
806-08019	1	SHIELD,FENCE,ALPINE RIDGE,RIGHT,X378	SH0410	CRITICAL	
806-08021	1	SHIELD,FENCE,ALPINE RIDGE,LEFT,X378	SH0420	CRITICAL	
806-07918	1	SHIELD,NAND,TOP,ALT,X363	SH0440	CRITICAL	
806-07917	1	SHIELD,NAND,BOTTOM,ALT,X363	SH0450	CRITICAL	
806-08024	1	SHIELD,DIPLEX,EG,X378	SH0460	CRITICAL	
806-08026	1	FENCE,VRAM,EG,X378	SH0470	CRITICAL	

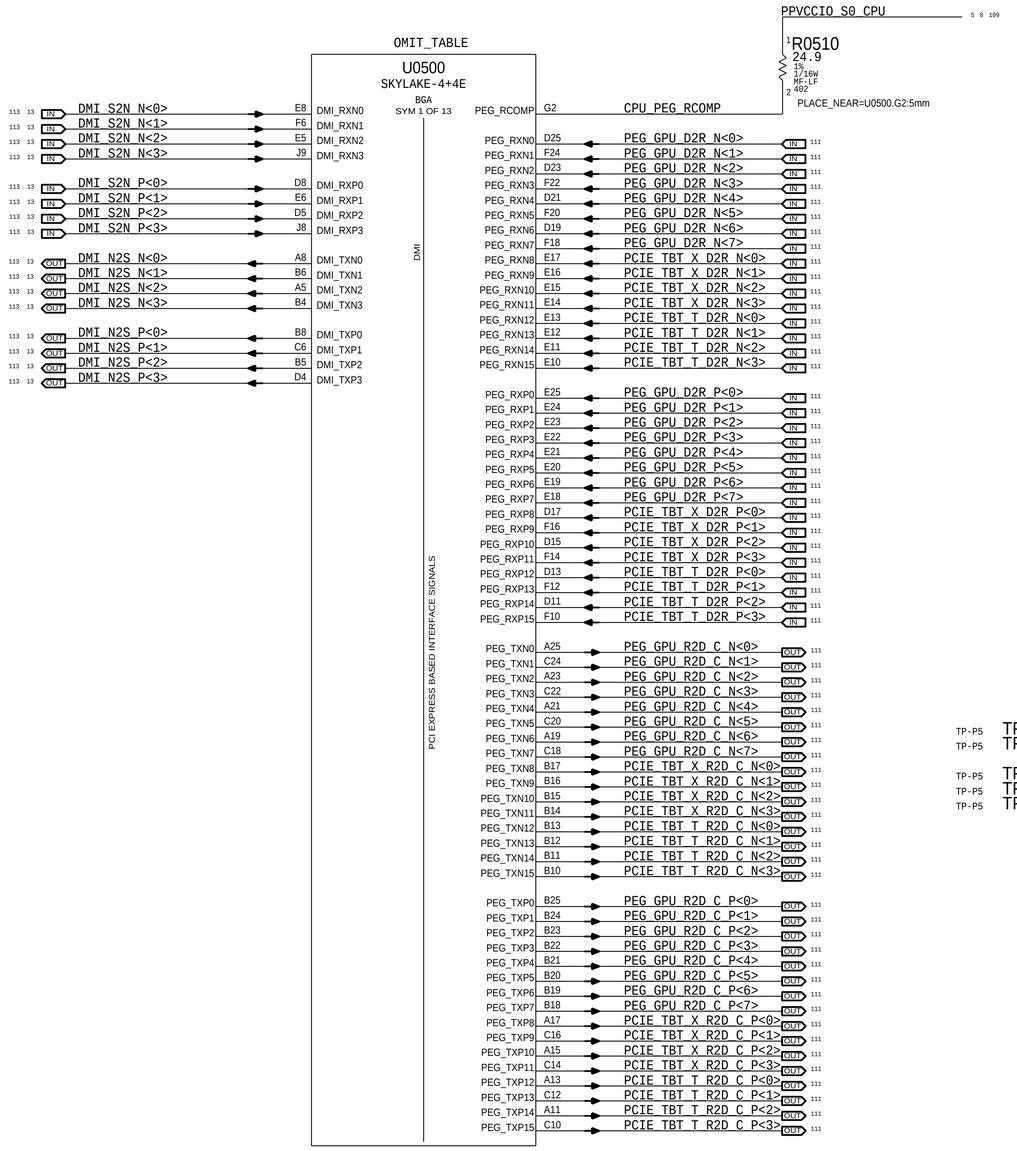
BOM_COST_GROUP=MECHANICALS

SYNC_MASTER=J80_MLB
SYNC_DATE=11/16/2015

PAGE TITLE
PD Parts

Apple Inc.

DRAWING NUMBER 051-00789
SIZE D
REVISION PROTO1A
BRANCH dvt-fab10
PAGE 4 OF 145
SHEET 4 OF 121



PAGE TITLE

CPU DMI/PEG/FDI/RSVD

Apple Inc.

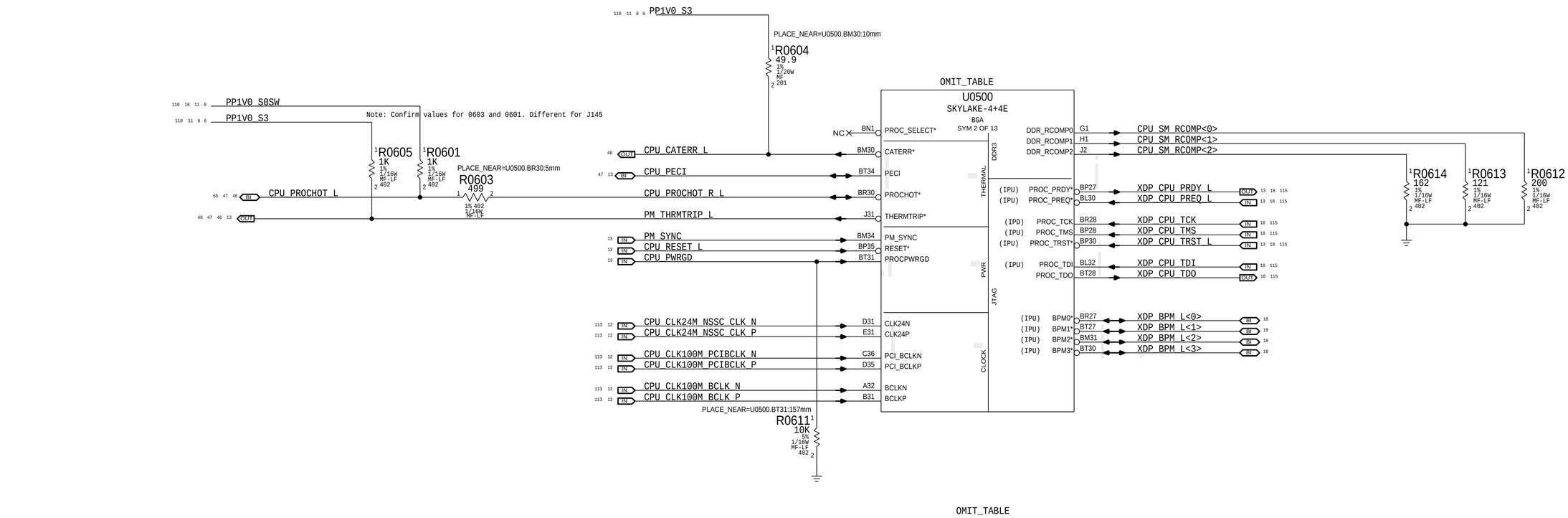
DRAWING NUMBER 051-00789 | SIZE D

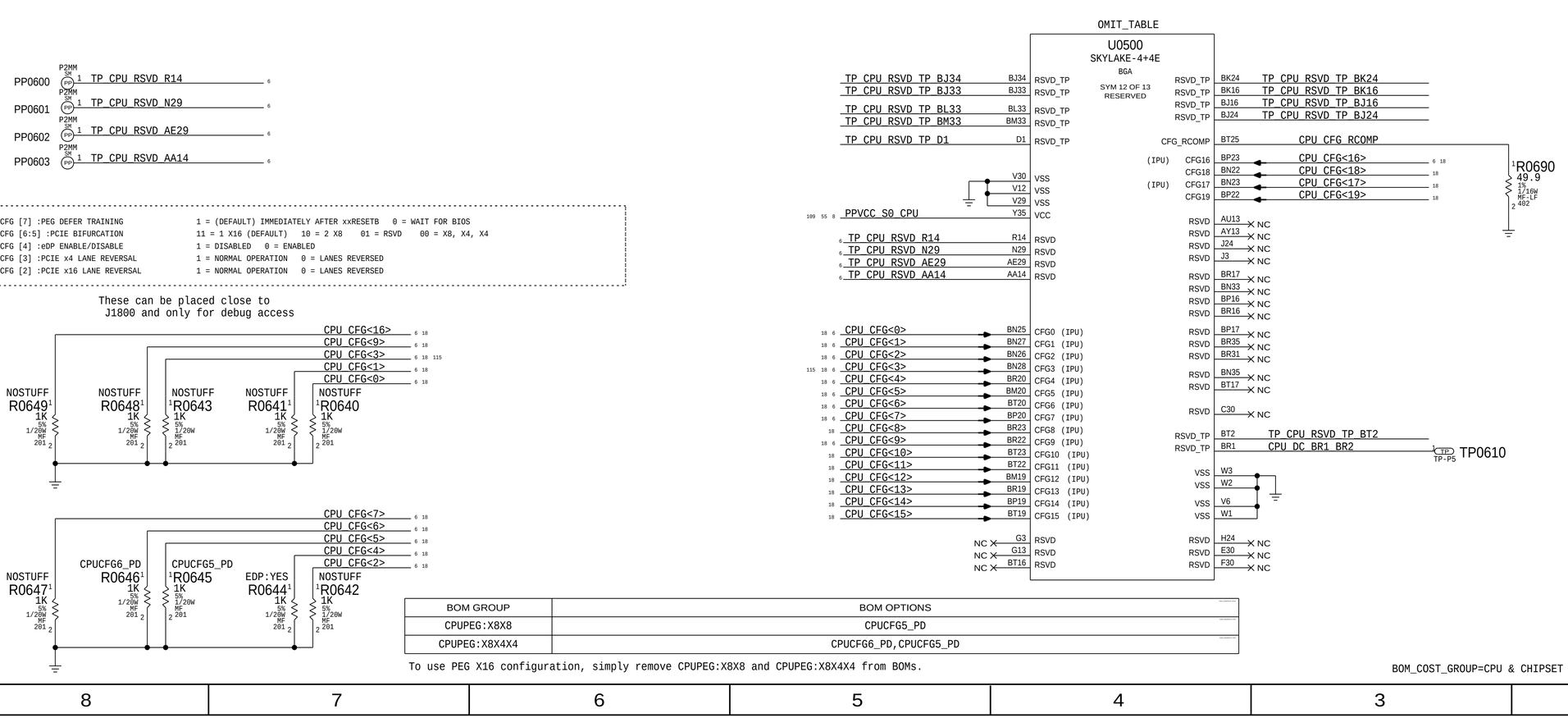
REVISION PROTO1A

BRANCH dvt-fab10

PAGE 5 OF 145

SHEET 5 OF 121






```
CFG [7] :PEG DEFER TRAINING              1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB   0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION              11 = 1 X16 (DEFAULT)   10 = 2 X8    01 = RSVD    00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE              1 = DISABLED   0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL           1 = NORMAL OPERATION   0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL          1 = NORMAL OPERATION   0 = LANES REVERSED
```

These can be placed close to
J1800 and only for debug access

BOM GROUP	BOM OPTIONS
CPUPEG:X8X8	CPUCFG5_PD
CPUPEG:X8X4X4	CPUCFG6_PD,CPUCFG5_PD

To use PEG X16 configuration, simply remove CPUPEG:X8X8 and CPUPEG:X8X4X4 from BOMs.

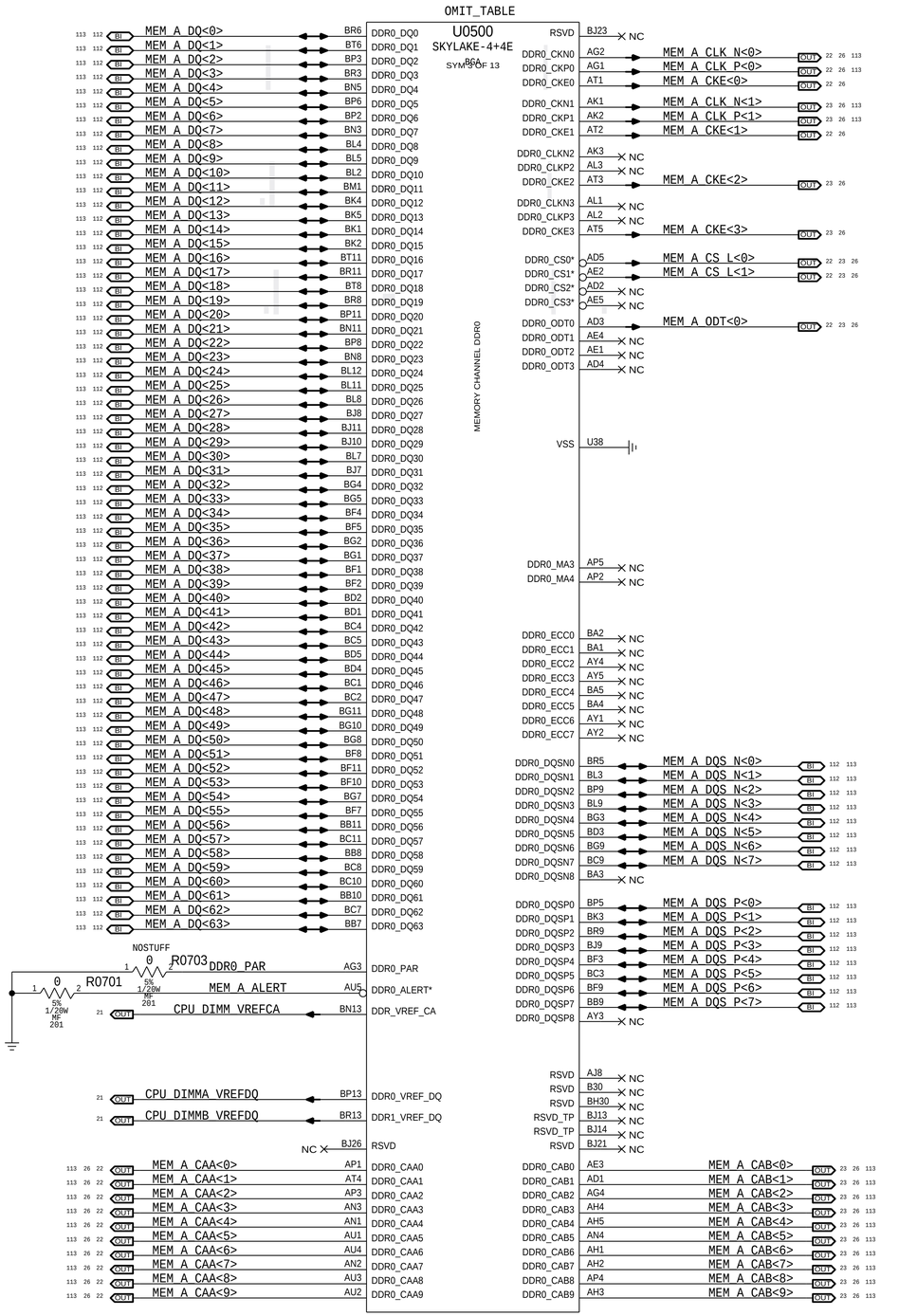
BOM_COST_GROUP=CPU & CHIPSET

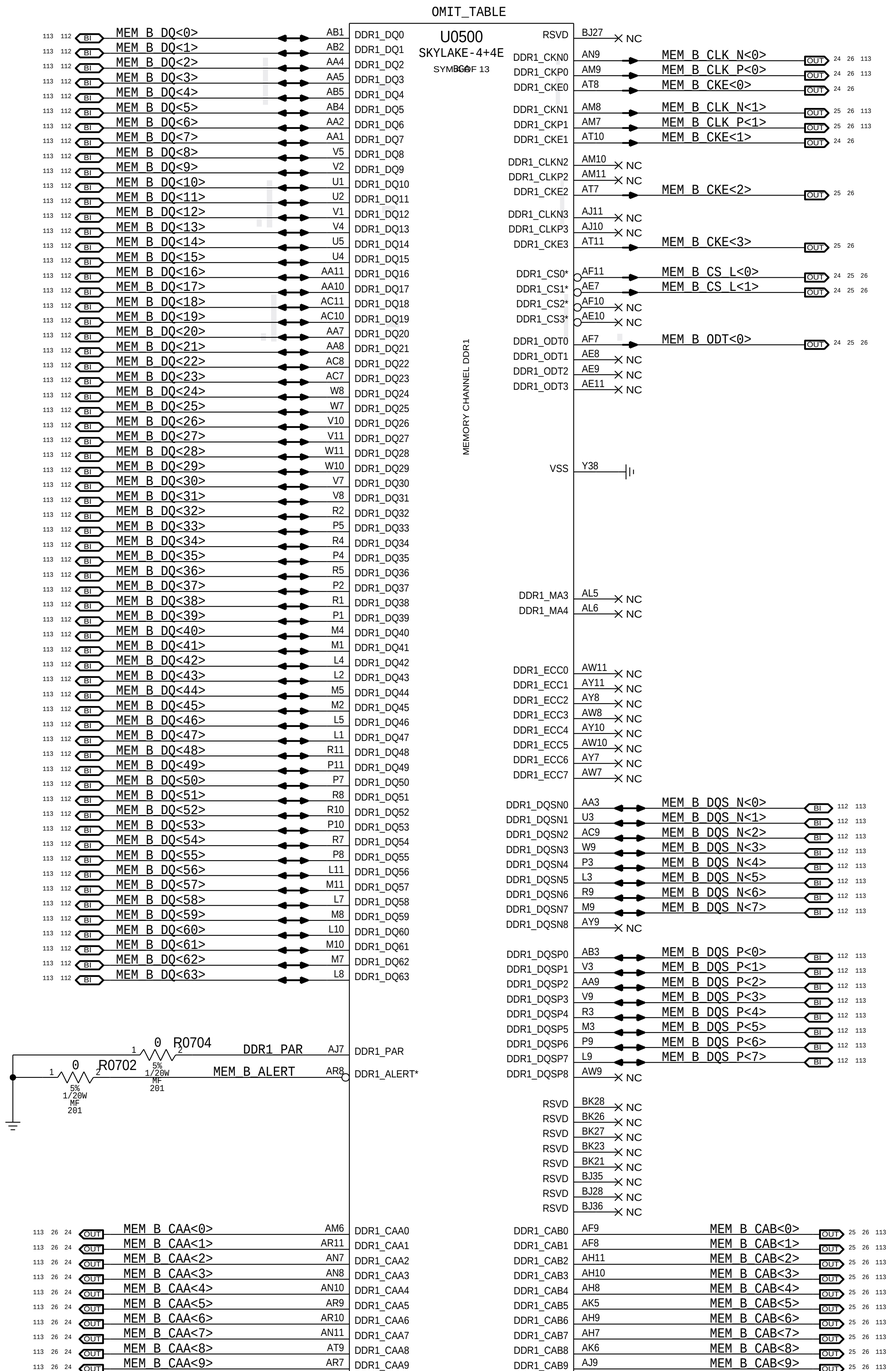
SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2016

PAGE TITLE
CPU Clock/Misc/JTAG/CFG

Apple Inc.

DRAWING NUMBER 051-00789 SIZE D
REVISION PROTO1A
BRANCH dvt-fab10
PAGE 6 OF 145
SHEET 6 OF 121





BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE

CPU DDR3 Interfaces

Apple Inc.

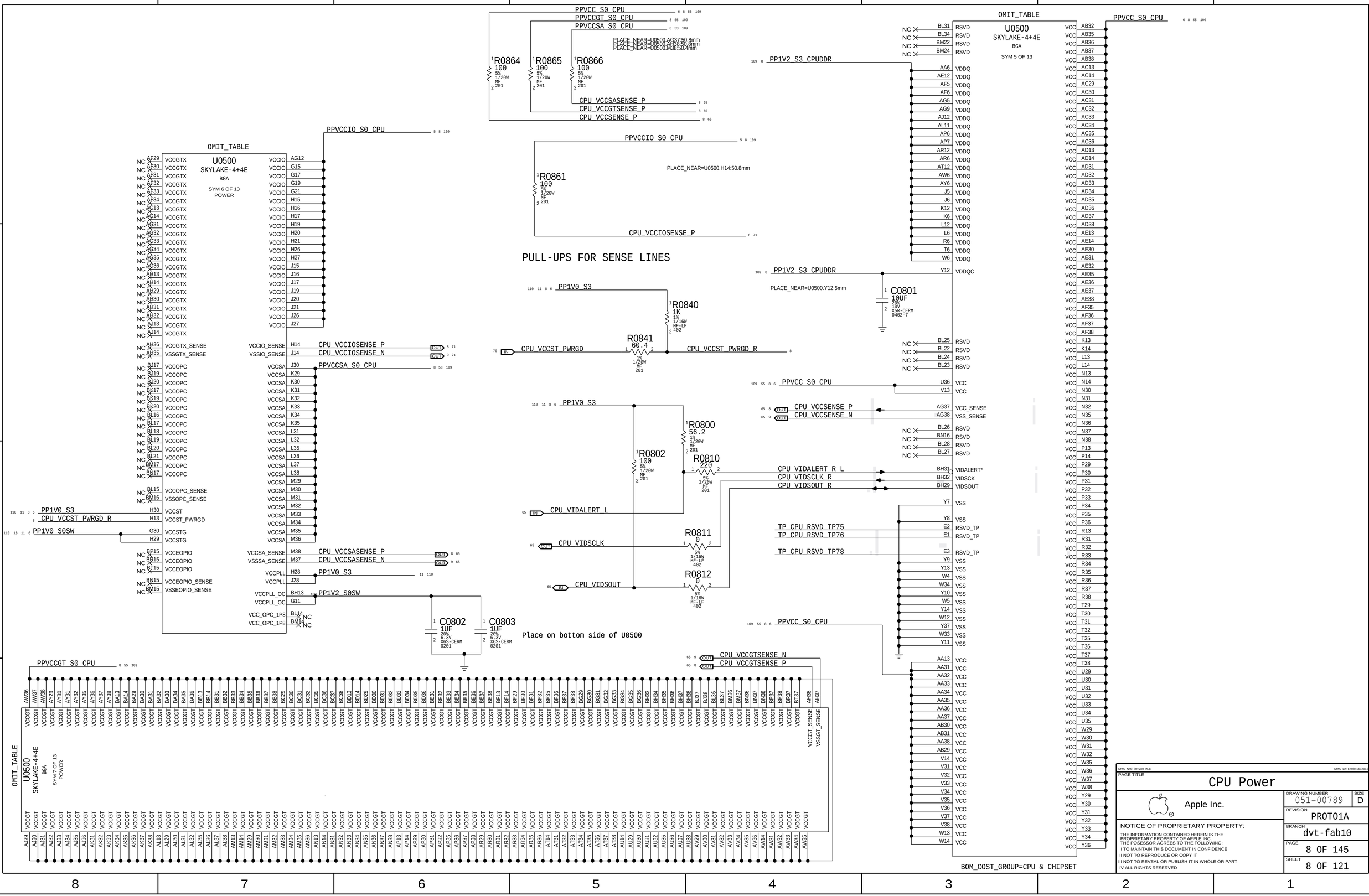
DRAWING NUMBER 051-00789 SIZE D

REVISION PR0T01A

BRANCH dvt-fab10

PAGE 7 OF 145

SHEET 7 OF 121



SYNC_MASTER=J80_MLB SYNC_DATE=08/16/2016

PAGE TITLE

CPU Power

Apple Inc.

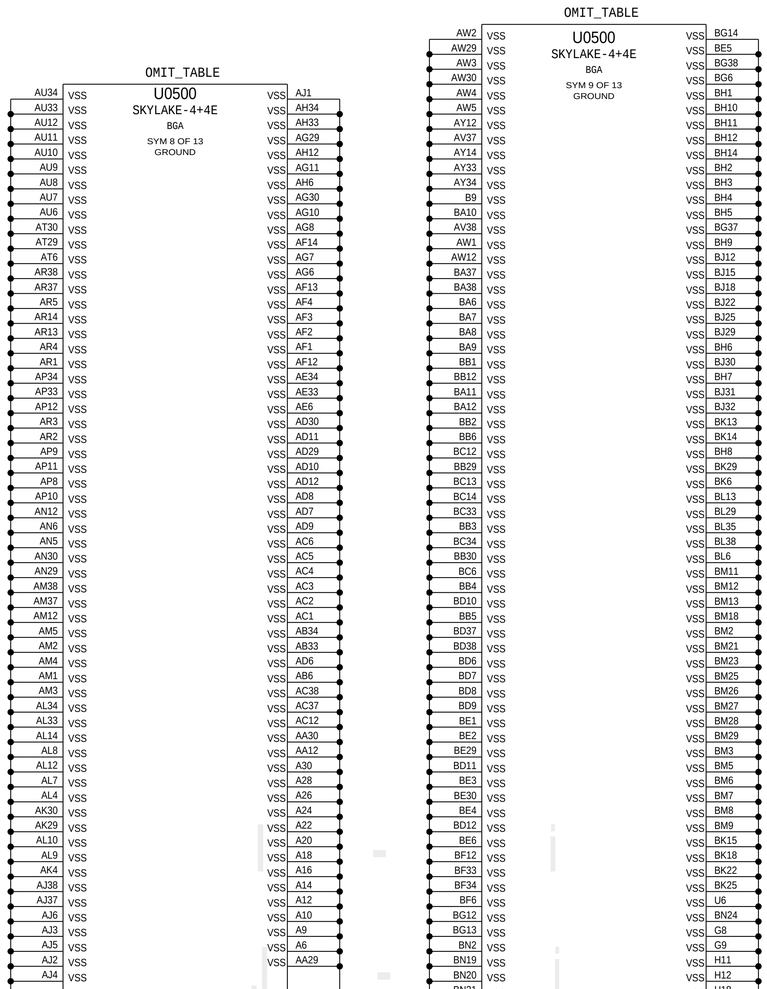
DRAWING NUMBER 051-00789 SIZE D

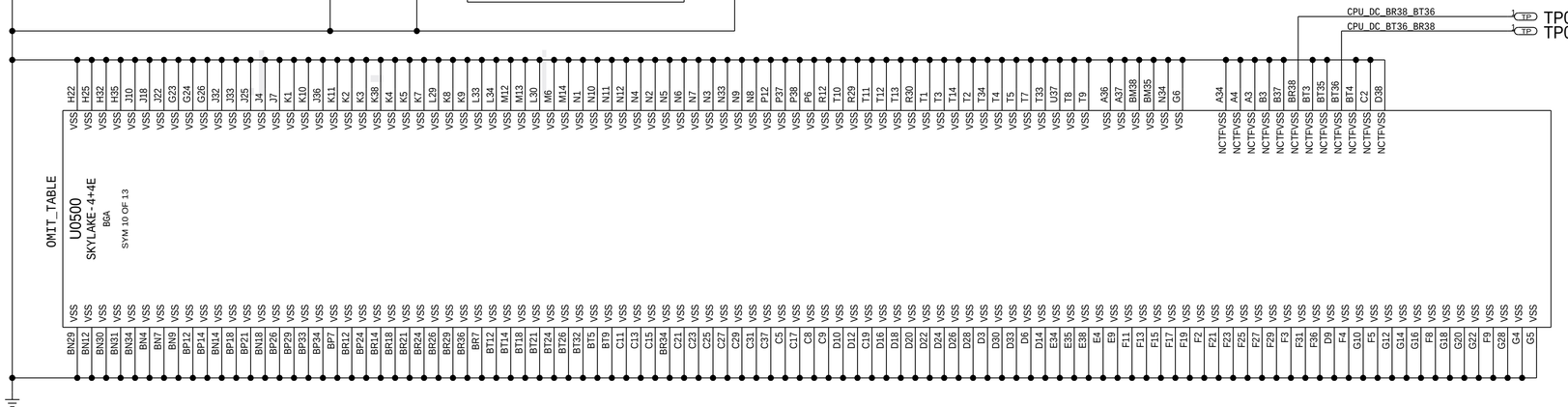
REVISION PROTO1A

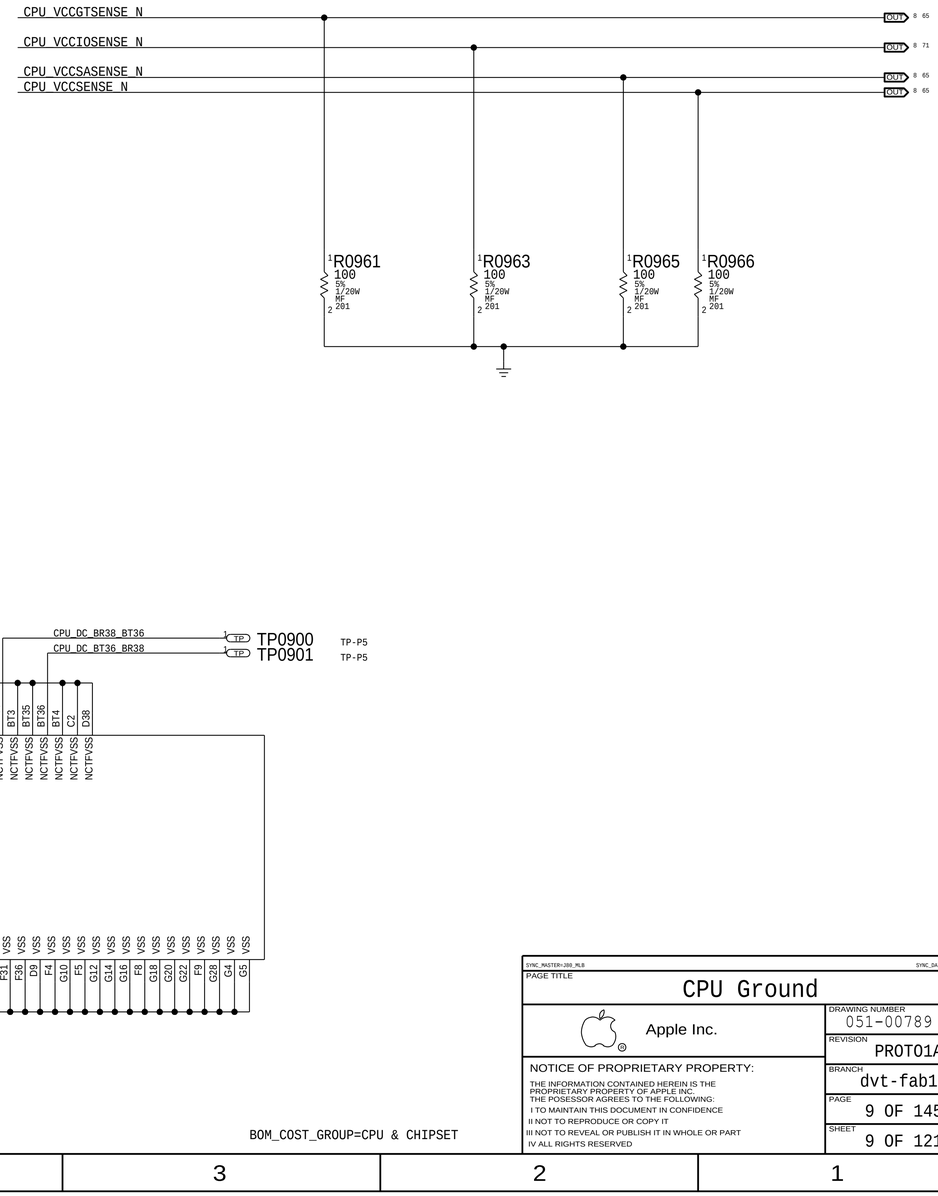
BRANCH dvt-fab10

PAGE 8 OF 145

SHEET 8 OF 121







BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J80_MLB SYNC_DATE=08/17/2015

PAGE TITLE

CPU Ground

Apple Inc.

DRAWING NUMBER 051-00789 SIZE D

REVISION PROTO1A

BRANCH dvt-fab10

PAGE 9 OF 145

SHEET 9 OF 121

Vcc CPU Core Decoupling from 20140905 BOM

CPU VCORE Decoupling

Intel recommendation: 5x 220uF ESR 5m ohms ESL 1.9nH each,4x 47uF 0805 8x22uF 0603, 28x 10uF 0402, 3x 10uF 0402, 69x 1uF 0201 Board Edge: 2x 220uF, 4x 47uF rest on the back side
Apple Implementation:

109 PPVCC_S0_CPU

Place on bottom side of U0500

C1000 1UF 20% 4V CERM-X6S 0201
C1001 1UF 20% 4V CERM-X6S 0201
C1002 1UF 20% 4V CERM-X6S 0201
C1003 1UF 20% 4V CERM-X6S 0201
C1004 1UF 20% 4V CERM-X6S 0201
C1005 1UF 20% 4V CERM-X6S 0201
C1006 1UF 20% 4V CERM-X6S 0201
C1007 1UF 20% 4V CERM-X6S 0201
C1008 1UF 20% 4V CERM-X6S 0201
C1009 1UF 20% 4V CERM-X6S 0201
C1010 1UF 20% 4V CERM-X6S 0201
C1011 1UF 20% 4V CERM-X6S 0201
C1012 1UF 20% 4V CERM-X6S 0201
C1013 1UF 20% 4V CERM-X6S 0201
C1014 1UF 20% 4V CERM-X6S 0201
C1015 1UF 20% 4V CERM-X6S 0201
C1016 1UF 20% 4V CERM-X6S 0201
C1017 1UF 20% 4V CERM-X6S 0201
C1018 1UF 20% 4V CERM-X6S 0201
C1019 1UF 20% 4V CERM-X6S 0201
C1020 1UF 20% 4V CERM-X6S 0201
C1021 1UF 20% 4V CERM-X6S 0201
C1022 1UF 20% 4V CERM-X6S 0201

Place on bottom side of U0500

C1023 1UF 20% 4V CERM-X6S 0201
C1024 1UF 20% 4V CERM-X6S 0201
C1025 1UF 20% 4V CERM-X6S 0201
C1026 1UF 20% 4V CERM-X6S 0201
C1027 1UF 20% 4V CERM-X6S 0201
C1028 1UF 20% 4V CERM-X6S 0201
C1029 1UF 20% 4V CERM-X6S 0201
C1030 1UF 20% 4V CERM-X6S 0201
C1031 1UF 20% 4V CERM-X6S 0201
C1032 1UF 20% 4V CERM-X6S 0201
C1033 1UF 20% 4V CERM-X6S 0201
C1034 1UF 20% 4V CERM-X6S 0201
C1035 1UF 20% 4V CERM-X6S 0201
C1036 1UF 20% 4V CERM-X6S 0201
C1037 1UF 20% 4V CERM-X6S 0201
C1038 1UF 20% 4V CERM-X6S 0201
C1039 1UF 20% 4V CERM-X6S 0201
C1040 1UF 20% 4V CERM-X6S 0201
C1041 1UF 20% 4V CERM-X6S 0201
C1042 1UF 20% 4V CERM-X6S 0201
C1043 1UF 20% 4V CERM-X6S 0201
C1044 1UF 20% 4V CERM-X6S 0201
C1045 1UF 20% 4V CERM-X6S 0201

Place on bottom side of U0500

C1046 1UF 20% 4V CERM-X6S 0201
C1047 1UF 20% 4V CERM-X6S 0201
C1048 1UF 20% 4V CERM-X6S 0201
C1049 1UF 20% 4V CERM-X6S 0201
C1050 1UF 20% 4V CERM-X6S 0201
C1051 1UF 20% 4V CERM-X6S 0201
C1052 1UF 20% 4V CERM-X6S 0201
C1053 1UF 20% 4V CERM-X6S 0201
C1054 1UF 20% 4V CERM-X6S 0201
C1055 1UF 20% 4V CERM-X6S 0201
C1056 1UF 20% 4V CERM-X6S 0201
C1057 1UF 20% 4V CERM-X6S 0201
C1058 1UF 20% 4V CERM-X6S 0201
C1059 1UF 20% 4V CERM-X6S 0201
C1060 1UF 20% 4V CERM-X6S 0201
C1061 1UF 20% 4V CERM-X6S 0201
C1062 1UF 20% 4V CERM-X6S 0201

NOSTUFF
C10A0 20UF 20% 2.5V X6S-CERM 0402-1
C10A1 20UF 20% 2.5V X6S-CERM 0402-1
C10A2 20UF 20% 2.5V X6S-CERM 0402-1
C10A3 20UF 20% 2.5V X6S-CERM 0402-1
C10A4 20UF 20% 2.5V X6S-CERM 0402-1
C10A5 20UF 20% 2.5V X6S-CERM 0402-1
C10A6 20UF 20% 2.5V X6S-CERM 0402-1
C10A7 20UF 20% 2.5V X6S-CERM 0402-1
C10A8 20UF 20% 2.5V X6S-CERM 0402-1
C10A9 20UF 20% 2.5V X6S-CERM 0402-1
C10B0 20UF 20% 2.5V X6S-CERM 0402-1
C10B1 20UF 20% 2.5V X6S-CERM 0402-1
C10B2 20UF 20% 2.5V X6S-CERM 0402-1
C10B3 20UF 20% 2.5V X6S-CERM 0402-1
C10B4 20UF 20% 2.5V X6S-CERM 0402-1
C10B5 20UF 20% 2.5V X6S-CERM 0402-1
C10B6 20UF 20% 2.5V X6S-CERM 0402-1
C10B7 20UF 20% 2.5V X6S-CERM 0402-1
C10B8 20UF 20% 2.5V X6S-CERM 0402-1
C10B9 20UF 20% 2.5V X6S-CERM 0402-1
C10C0 20UF 20% 2.5V X6S-CERM 0402-1
C10C1 20UF 20% 2.5V X6S-CERM 0402-1
C10C3 20UF 20% 2.5V X6S-CERM 0402-1
C10C4 20UF 20% 2.5V X6S-CERM 0402-1
C10C5 20UF 20% 2.5V X6S-CERM 0402-1
C10C6 20UF 20% 2.5V X6S-CERM 0402-1
C10C7 20UF 20% 2.5V X6S-CERM 0402-1

Noise Floor caps

NOSTUFF
C10D0 20UF 20% 2.5V X6S-CERM 0402-1
C10D1 20UF 20% 2.5V X6S-CERM 0402-1
C10D2 20UF 20% 2.5V X6S-CERM 0402-1
C10D3 20UF 20% 2.5V X6S-CERM 0402-1
C10D4 20UF 20% 2.5V X6S-CERM 0402-1
C10D5 20UF 20% 2.5V X6S-CERM 0402-1
C10D6 20UF 20% 2.5V X6S-CERM 0402-1
C10D7 20UF 20% 2.5V X6S-CERM 0402-1
C10E0 20UF 20% 2.5V X6S-CERM 0402-1
C10E1 20UF 20% 2.5V X6S-CERM 0402-1
C10E2 20UF 20% 2.5V X6S-CERM 0402-1
C10E3 20UF 20% 2.5V X6S-CERM 0402-1

C10N1 12PF 5% 25V NP0-C0G 0201
C10N2 12PF 5% 25V NP0-C0G 0201
C10N3 12PF 5% 25V NP0-C0G 0201
C10N4 12PF 5% 25V NP0-C0G 0201
C10N5 12PF 5% 25V NP0-C0G 0201
C10N6 12PF 5% 25V NP0-C0G 0201
C10N7 12PF 5% 25V NP0-C0G 0201

Place near inductors on bottom side.

NOSTUFF
C10Z1 20UF 20% 2.5V X6S-CERM 0402-1
C10Z2 20UF 20% 2.5V X6S-CERM 0402-1
C10Z3 20UF 20% 2.5V X6S-CERM 0402-1
C10Z4 20UF 20% 2.5V X6S-CERM 0402-1
C10Z5 20UF 20% 2.5V X6S-CERM 0402-1
C10Z6 20UF 20% 2.5V X6S-CERM 0402-1
C10Z7 20UF 20% 2.5V X6S-CERM 0402-1
C10Z8 20UF 20% 2.5V X6S-CERM 0402-1
C10Z9 20UF 20% 2.5V X6S-CERM 0402-1
C10ZA 20UF 20% 2.5V X6S-CERM 0402-1
C10ZB 20UF 20% 2.5V X6S-CERM 0402-1
C10ZC 20UF 20% 2.5V X6S-CERM 0402-1

C1068 220UF 20% 2V ELEC SM-COMBO
C1069 220UF 20% 2V ELEC SM-COMBO
C1070 220UF 20% 2V ELEC SM-COMBO
C1071 220UF 20% 2V ELEC SM-COMBO
C1072 220UF 20% 2V ELEC SM-COMBO
C1073 220UF 20% 2V ELEC SM-COMBO

116 109 PP1V2_S3_CPUDDR

Place on bottom side of U0500.

C1080 20UF 20% 2.5V X6S-CERM 0402-1
C1081 20UF 20% 2.5V X6S-CERM 0402-1
C1082 20UF 20% 2.5V X6S-CERM 0402-1
C1083 20UF 20% 2.5V X6S-CERM 0402-1
C1084 20UF 20% 2.5V X6S-CERM 0402-1
C1085 20UF 20% 2.5V X6S-CERM 0402-1

Place on bottom side of U0500

C1090 20UF 20% 2.5V X6S-CERM 0402-1
C1091 20UF 20% 2.5V X6S-CERM 0402-1
C1092 20UF 20% 2.5V X6S-CERM 0402-1
C1093 20UF 20% 2.5V X6S-CERM 0402-1
C1094 20UF 20% 2.5V X6S-CERM 0402-1
C1095 20UF 20% 2.5V X6S-CERM 0402-1

CPU VDDQ Decoupling

Intel recommendation: 10x 10uF 0402, 4x 22uF 0602
Apple Implementation:

CPU VCCIO Decoupling

Intel recommendation: 3x 10uF 0402 (opposite CPU)
Apple Implementation:

Place near U0500 on bottom side. U0500 on bottom side

109 PPVCCIO_S0_CPU

C1086 20UF 20% 2.5V X6S-CERM 0402-1
C1087 20UF 20% 2.5V X6S-CERM 0402-1
C1088 20UF 20% 2.5V X6S-CERM 0402-1
C1089 20UF 20% 2.5V X6S-CERM 0402-1
C108A 20UF 20% 2.5V X6S-CERM 0402-1

NOTE: Intel decoupling recommendations from CBR schematics for Skylake H doc#557227 and PDG section 48.1 (document# 546884)

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J30_DT&DMA_RLS_BAFF39 SYNC_DATE=11/22/2013

PAGE TITLE: CPU Decoupling 1 [10]

Apple Inc.

DRAWING NUMBER: 051-00789 SIZE: D
REVISION: PROTO1A
BRANCH: dvt-fab10
PAGE: 10 OF 145
SHEET: 10 OF 121

Vcc GT Slice Core Decoupling from 20140905 BOM

CPU VGTSlice Decoupling

Intel recommendation: 7x 220uF, 6x 47uF 0805, 6x 22uF 0603, 35x 10uF 0402, 68 1uF 0201
Apple Implementation:

Board Edge: 4x220uF, 7x 47uF rest on back side

116 109 PPVCCGT_S0_CPU

Place on bottom side of U0500

C1100 1UF 20% 4V CERM-X6S 0201
C1101 1UF 20% 4V CERM-X6S 0201
C1102 1UF 20% 4V CERM-X6S 0201
C1103 1UF 20% 4V CERM-X6S 0201
C1104 1UF 20% 4V CERM-X6S 0201
C1105 1UF 20% 4V CERM-X6S 0201
C1106 1UF 20% 4V CERM-X6S 0201
C1107 1UF 20% 4V CERM-X6S 0201
C1108 1UF 20% 4V CERM-X6S 0201
C1109 1UF 20% 4V CERM-X6S 0201
C1110 1UF 20% 4V CERM-X6S 0201
C1111 1UF 20% 4V CERM-X6S 0201
C1112 1UF 20% 4V CERM-X6S 0201
C1113 1UF 20% 4V CERM-X6S 0201
C1114 1UF 20% 4V CERM-X6S 0201
C1115 1UF 20% 4V CERM-X6S 0201
C1116 1UF 20% 4V CERM-X6S 0201
C1117 1UF 20% 4V CERM-X6S 0201
C1118 1UF 20% 4V CERM-X6S 0201
C1119 1UF 20% 4V CERM-X6S 0201
C1120 1UF 20% 4V CERM-X6S 0201
C1121 1UF 20% 4V CERM-X6S 0201
C1122 1UF 20% 4V CERM-X6S 0201
C1123 1UF 20% 4V CERM-X6S 0201

Place on bottom side of U0500

C1124 1UF 20% 4V CERM-X6S 0201
C1125 1UF 20% 4V CERM-X6S 0201
C1126 1UF 20% 4V CERM-X6S 0201
C1127 1UF 20% 4V CERM-X6S 0201
C1128 1UF 20% 4V CERM-X6S 0201
C1129 1UF 20% 4V CERM-X6S 0201
C1130 1UF 20% 4V CERM-X6S 0201
C1131 1UF 20% 4V CERM-X6S 0201
C1132 1UF 20% 4V CERM-X6S 0201
C1133 1UF 20% 4V CERM-X6S 0201
C1134 1UF 20% 4V CERM-X6S 0201
C1135 1UF 20% 4V CERM-X6S 0201
C1136 1UF 20% 4V CERM-X6S 0201
C1137 1UF 20% 4V CERM-X6S 0201
C1138 1UF 20% 4V CERM-X6S 0201
C1139 1UF 20% 4V CERM-X6S 0201
C1140 1UF 20% 4V CERM-X6S 0201
C1141 1UF 20% 4V CERM-X6S 0201
C1142 1UF 20% 4V CERM-X6S 0201
C1143 1UF 20% 4V CERM-X6S 0201
C1144 1UF 20% 4V CERM-X6S 0201
C1145 1UF 20% 4V CERM-X6S 0201
C1146 1UF 20% 4V CERM-X6S 0201
C1147 1UF 20% 4V CERM-X6S 0201

Place on bottom side of U0500

C1148 1UF 20% 4V CERM-X6S 0201
C1149 1UF 20% 4V CERM-X6S 0201
C1150 1UF 20% 4V CERM-X6S 0201
C1151 1UF 20% 4V CERM-X6S 0201
C1152 1UF 20% 4V CERM-X6S 0201
C1153 1UF 20% 4V CERM-X6S 0201
C1154 1UF 20% 4V CERM-X6S 0201
C1155 1UF 20% 4V CERM-X6S 0201
C1156 1UF 20% 4V CERM-X6S 0201
C1157 1UF 20% 4V CERM-X6S 0201
C1158 1UF 20% 4V CERM-X6S 0201
C1159 1UF 20% 4V CERM-X6S 0201
C1160 1UF 20% 4V CERM-X6S 0201
C1161 1UF 20% 4V CERM-X6S 0201
C1162 1UF 20% 4V CERM-X6S 0201
C1163 1UF 20% 4V CERM-X6S 0201
C1164 1UF 20% 4V CERM-X6S 0201
C1165 1UF 20% 4V CERM-X6S 0201
C1166 1UF 20% 4V CERM-X6S 0201
C1167 1UF 20% 4V CERM-X6S 0201

NOSTUFF
C11A0 20UF 20% 2.5V X6S-CERM 0402-1
C11A1 20UF 20% 2.5V X6S-CERM 0402-1
C11A2 20UF 20% 2.5V X6S-CERM 0402-1
C11A3 20UF 20% 2.5V X6S-CERM 0402-1
C11A4 20UF 20% 2.5V X6S-CERM 0402-1
C11A5 20UF 20% 2.5V X6S-CERM 0402-1
C11A6 20UF 20% 2.5V X6S-CERM 0402-1
C11A7 20UF 20% 2.5V X6S-CERM 0402-1
C11A8 20UF 20% 2.5V X6S-CERM 0402-1
C11A9 20UF 20% 2.5V X6S-CERM 0402-1
C11B0 20UF 20% 2.5V X6S-CERM 0402-1
C11B1 20UF 20% 2.5V X6S-CERM 0402-1
C11B2 20UF 20% 2.5V X6S-CERM 0402-1
C11B3 20UF 20% 2.5V X6S-CERM 0402-1
C11B4 20UF 20% 2.5V X6S-CERM 0402-1
C11B5 20UF 20% 2.5V X6S-CERM 0402-1
C11B6 20UF 20% 2.5V X6S-CERM 0402-1
C11B7 20UF 20% 2.5V X6S-CERM 0402-1
C11B8 20UF 20% 2.5V X6S-CERM 0402-1
C11B9 20UF 20% 2.5V X6S-CERM 0402-1
C11C0 20UF 20% 2.5V X6S-CERM 0402-1
C11C1 20UF 20% 2.5V X6S-CERM 0402-1
C11C2 20UF 20% 2.5V X6S-CERM 0402-1
C11C3 20UF 20% 2.5V X6S-CERM 0402-1
C11C4 20UF 20% 2.5V X6S-CERM 0402-1
C11C5 20UF 20% 2.5V X6S-CERM 0402-1
C11C6 20UF 20% 2.5V X6S-CERM 0402-1
C11C7 20UF 20% 2.5V X6S-CERM 0402-1
C11C8 20UF 20% 2.5V X6S-CERM 0402-1
C11C9 20UF 20% 2.5V X6S-CERM 0402-1
C11D0 20UF 20% 2.5V X6S-CERM 0402-1

NOSTUFF
C11F0 20UF 20% 2.5V X6S-CERM 0402-1
C11F1 20UF 20% 2.5V X6S-CERM 0402-1
C11F2 20UF 20% 2.5V X6S-CERM 0402-1
C11F3 20UF 20% 2.5V X6S-CERM 0402-1
C11F4 20UF 20% 2.5V X6S-CERM 0402-1
C11F5 20UF 20% 2.5V X6S-CERM 0402-1
C11F6 20UF 20% 2.5V X6S-CERM 0402-1
C11F7 20UF 20% 2.5V X6S-CERM 0402-1
C11E0 20UF 20% 2.5V X6S-CERM 0402-1
C11E1 20UF 20% 2.5V X6S-CERM 0402-1
C11E2 20UF 20% 2.5V X6S-CERM 0402-1
C11E3 20UF 20% 2.5V X6S-CERM 0402-1
C11E4 20UF 20% 2.5V X6S-CERM 0402-1
C11E5 20UF 20% 2.5V X6S-CERM 0402-1

NOSTUFF
C11D4 20UF 20% 2.5V X6S-CERM 0402-1
C11D3 20UF 20% 2.5V X6S-CERM 0402-1
C11D2 20UF 20% 2.5V X6S-CERM 0402-1
C11D1 20UF 20% 2.5V X6S-CERM 0402-1

C1168 220UF 20% 2V ELEC SM-COMBO
C1169 220UF 20% 2V ELEC SM-COMBO
C1170 220UF 20% 2V ELEC SM-COMBO
C1171 220UF 20% 2V ELEC SM-COMBO
C1172 220UF 20% 2V ELEC SM-COMBO

CPU VCCSTG Decoupling

110 18 8 6 PP1V0_S0SW

Place near U0500 on bottom side

C11L1 1UF 20% 4V CERM-X6S 0201
C11L2 1UF 20% 4V CERM-X6S 0201

CPU VCCPLL and VCCST Decoupling

110 8 PP1V0_S3
110 8 6 PP1V0_S3

C11M1 1UF 20% 4V CERM-X6S 0201
C11M2 1UF 20% 4V CERM-X6S 0201

Place near U0500 on bottom side

109 PPVCCSA_S0_CPU

Place on bottom side of U0500

C11H0 1UF 20% 4V CERM-X6S 0201
C11H1 1UF 20% 4V CERM-X6S 0201
C11H2 1UF 20% 4V CERM-X6S 0201

NOSTUFF
C11I0 20UF 20% 2.5V X6S-CERM 0402-1
C11I1 20UF 20% 2.5V X6S-CERM 0402-1
C11I2 20UF 20% 2.5V X6S-CERM 0402-1
C11I3 20UF 20% 2.5V X6S-CERM 0402-1
C11I4 20UF 20% 2.5V X6S-CERM 0402-1
C11I5 20UF 20% 2.5V X6S-CERM 0402-1
C11I6 20UF 20% 2.5V X6S-CERM 0402-1
C11I7 20UF 20% 2.5V X6S-CERM 0402-1

NOSTUFF
C11J0 47UF 20% 6.3V POLY-TANT 0805
C11J1 47UF 20% 6.3V POLY-TANT 0805

C11K9 220UF 20% 2V ELEC SM-COMBO

NOTE: Intel decoupling recommendations from CBR schematics for Skylake H doc#557227 and PDG section 48.1 (document# 546884)

CPU VCCSA Decoupling

Intel recommendation: 2x 220uF, 1x 47uF 0805. 1x 22uF. 7x 10uF 0402, 3x 1uF 0201_
2x 220uF, 1x 22uF on board edge, everything else on back side
Apple Implementation:

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE: CPU Decoupling 2 [11]

Apple Inc.

DRAWING NUMBER: 051-00789
SIZE: D
REVISION: PROTO1A
BRANCH: dvt-fab10
PAGE: 11 OF 145
SHEET: 11 OF 121

OMIT_TABLE

U1100
SKL-PCH-SFF
H65946
FCBGA
SYM 4 OF 12

SYSTEM POWER MANAGEMENT

48 IN	SMC_PCH_SUSACK_L	AL15	GPP_A15/SUSACK* (IPU)	DRAM_RESET*	AM11	NC_PCH_DRAM_RESET_L 20
115 46 18 12 IN	PM_SYSRST_L	AJ4	SYS_RESET*	(OD) DSW_PWROK	AF8	PM_DSW_PWRGD — IN 46
114 73 46 IN	PM_PCH_SYS_PWROK	AK3	SYS_PWROK	(IPD-DeepSx) WAKE*	AG12	PCIE_WAKE_L — IN 12 19
115 70 IN	PM_PCH_PWROK	AJ11	PCH_PWROK	GPP_A8/CLKRUN*	AK14	LPC_CLKRUN_L — BI 12 46
				GPP_A14/SUS_STAT*/ESPI_RESET*	AM15	LPC_PWRDWN_L — OUT 46
114 35 20 OUT	PLT_RST_L	AG23	GPP_B13/PLTRST*	(IPU-RSMRST#) GPD8/SUSCLK	AH12	PM_CLK32K_SUSCLK_R — OUT 47
115 73 46 18 IN	PM_RSMRST_L	AF12	RSMRST*	GPD10/SLP_S5*	AG10	PM_SLP_S5_L — OUT 12 20 46 73
48 OUT	SMC_PCH_SUSWARN_L	AJ16	GPP_A13/SUSWARN* /SUSPWRDNACK	GPD5/SLP_S4*	AK10	PM_SLP_S4_L — OUT 12 20 43 46 70 73
48 12 IN	PM_PWRBTN_L	AM10	GPD3/PWRBTN*	GPD4/SLP_S3*	AK9	PM_SLP_S3_L — OUT 12 20 27 46 70 73 76 89 101 114
12	SSD_SR_EN_L	AL12	GPD1/ACPRESENT	GPD6/SLP_A*	AG11	NC_PCH_SLP_A_L 20
103 46 29 12 IN	PM_BATLOW_L (IPU)	AM12	GPD0/BATLOW*	SLP_SUS*	AH13	PM_SLP_SUS_L — OUT 12 70 73
70 46 20 12 OUT	PM_SLP_S0_L	AM22	GPP_B12/SLP_S0*	SLP_LAN*	AK11	NC_PCH_SLP_LAN_L 20
111	NC_PCH_SLP_WLAN_L	AH10	GPD9/SLP_WLAN*	GPD2/LAN_WAKE*	AL9	SMC_WAKE_SCI_L — IN 12 46
20	NC_PCH_PME_L	AG16	GPP_A11/PME*	GPD11/LANPHYPC	AJ13	NC_PCH_LANPHYPC 20
59 12	AUD_PWR_EN	AG18	GPP_A12/BMBUSY*/ISH_GP6 /SX_EXIT_HOLDOFF*	GPP_B2/VRALERT*	AH20	BT_LOW_PWR_L — OUT 12 35

NOSTUFF R1204 0 5% 1/20W MF 0201

R1205 100K 5% 1/20W MF 201

RTC

20 IN	SYSCLK_CLK32K_PCH	AL8	RTCX1	GPP_A0/RCIN*/ESPI_ALERT1*	AM13	PCH_RCIN_L_PU 12
20 OUT	NC_PCH_CLK32K_RTCX2	AM8	RTCX2	GPP_A1/LAD0/ESPI_IO0	AK12	LPC_AD_R<0> — R1440 33 — LPC_AD<0> BI 46 89
12	PCH_INTRUDER_L	AJ10	INTRUDER*	GPP_A2/LAD1/ESPI_IO1	AK13	LPC_AD_R<1> — R1441 33 — LPC_AD<1> BI 46 89
12	PCH_SRTCRST_L	AJ8	SRTCRST*	GPP_A3/LAD2/ESPI_IO2	AG20	LPC_AD_R<2> — R1442 33 — LPC_AD<2> BI 46 89
12	RTC_RESET_L	AH8	RTCRST*	GPP_A4/LAD3/ESPI_IO3	AM14	LPC_AD_R<3> — R1443 33 — LPC_AD<3> BI 46 89
				GPP_A5/LFRAME*/ESPI_CS0*	AL14	LPC_FRAME_R_L — R1444 33 — LPC_FRAME_L OUT 46 89
				GPP_A6/SERIRQ/ESPI_CS1*	AH14	LPC_SERIRQ — BI 12 46
				GPP_A7/PIRQA*/ESPI_ALERT0*	AJ18	SMC_RUNTIME_SCI_L — IN 12 46
				GPD7/RSVD	AL11	NC_PCH_GPD7 20

PLACE_NEAR=U1100.AL14:1.25mm

PP3V0_G3H 16 17 109

R1201 1M 5% 1/20W MF 201
R1202 20K 5% 1/20W MF 201
R1203 20K 5% 1/20W MF 201

PCH_SRTCRST_L 12
PCH_INTRUDER_L 12
RTC_RESET_L 12

C1202 1UF 10% 10V X5R 402-1
C1203 1UF 10% 10V X5R 402-1

OMIT_TABLE

U1100
SKL-PCH-SFF
H65946
FCBGA
SYM 2 OF 12

CLOCK SIGNALS

PCI EXPRESS CLOCKS & CONTROL

113 35 OUT	PCIE_CLK100M_AP_N	J5	CLKOUT_PCIE_N0	XTAL24_IN	B4	SYSCLK_CLK24M_PCH — IN 20
113 35 OUT	PCIE_CLK100M_AP_P	J6	CLKOUT_PCIE_P0	XTAL24_OUT	B3	NC_PCH_CLK24M_XTALOUT — OUT 20 113
111 OUT	NC_CLKOUT_PCIE_1_N	F2	CLKOUT_PCIE_N1			
111 OUT	NC_CLKOUT_PCIE_1_P	F1	CLKOUT_PCIE_P1			
111 OUT	NC_CLKOUT_PCIE_2_N	K6	CLKOUT_PCIE_N2			
111 OUT	NC_CLKOUT_PCIE_2_P	K5	CLKOUT_PCIE_P2			
27 OUT	PCIE_CLK100M_TBT_X_N	F3	CLKOUT_PCIE_N3			
27 OUT	PCIE_CLK100M_TBT_X_P	F4	CLKOUT_PCIE_P3			
101 OUT	PCIE_CLK100M_TBT_T_N	G2	CLKOUT_PCIE_N4			
101 OUT	PCIE_CLK100M_TBT_T_P	G3	CLKOUT_PCIE_P4			
113 87 OUT	PCIE_CLK100M_SSD_N	E2	CLKOUT_PCIE_N5			
113 87 OUT	PCIE_CLK100M_SSD_P	E1	CLKOUT_PCIE_P5			
111 OUT	NC_CLKOUT_PCIE_6_N	K2	CLKOUT_PCIE_N6			
111 OUT	NC_CLKOUT_PCIE_6_P	K3	CLKOUT_PCIE_P6			
111 OUT	EG_PEG_CLK100M_N	L1	CLKOUT_PCIE_N7			
111 OUT	EG_PEG_CLK100M_P	L2	CLKOUT_PCIE_P7			
111 OUT	NC_CLKOUT_PCIE_8_N	M3	CLKOUT_PCIE_N8			
111 OUT	NC_CLKOUT_PCIE_8_P	M4	CLKOUT_PCIE_P8			
111 OUT	NC_CLKOUT_PCIE_9_N	M2	CLKOUT_PCIE_N9			
111 OUT	NC_CLKOUT_PCIE_9_P	M1	CLKOUT_PCIE_P9			
111 OUT	NC_CLKOUT_PCIE_10_N	R6	CLKOUT_PCIE_N10			
111 OUT	NC_CLKOUT_PCIE_10_P	R7	CLKOUT_PCIE_P10			
111 OUT	NC_CLKOUT_PCIE_11_N	T6	CLKOUT_PCIE_N11			
111 OUT	NC_CLKOUT_PCIE_11_P	T5	CLKOUT_PCIE_P11			
111 OUT	NC_CLKOUT_PCIE_12_N	N3	CLKOUT_PCIE_N12			
111 OUT	NC_CLKOUT_PCIE_12_P	N2	CLKOUT_PCIE_P12			
20 OUT	NC_CLKOUT_PCIE_13_N	P5	CLKOUT_PCIE_N13			
20 OUT	NC_CLKOUT_PCIE_13_P	P6	CLKOUT_PCIE_P13			
111 OUT	NC_CLKOUT_PCIE_14_N	N5	CLKOUT_PCIE_N14			
111 OUT	NC_CLKOUT_PCIE_14_P	N6	CLKOUT_PCIE_P14			
111 OUT	NC_CLKOUT_PCIE_15_N	M6	CLKOUT_PCIE_N15			
111 OUT	NC_CLKOUT_PCIE_15_P	M7	CLKOUT_PCIE_P15			

XCLK_BIASREF E4 — PCH_DIFFCLK_BIASREF — R1234 2.7K 1% 1/20W MF 201 — PP1V0_SUS 110
PLACE_NEAR=U1100.E4:1.25mm

GPP_A9/CLKOUT_LPC0 /ESPI_CLK	AJ14	LPC_CLK24M_SMC_R — R1235 22 1% 1/20W MF 201 — LPC_CLK24M_SMC	BI 46			
GPP_A10/CLKOUT_LPC1	AH15	LPC_CLK24M_DPMUX_UC_R	20			
GPP_A16/CLKOUT_48	AL16	CAMERA_PWR_EN	12			
CLKOUT_ITPXDP_N	L6	NC_ITPXDP_CLK100MN	OUT 18 113 115			
CLKOUT_ITPXDP_P	L5	NC_ITPXDP_CLK100MP	OUT 18 113 115			
CLKOUT_CPUBCLK_N	J3	CPU_CLK100M_BCLK_N	OUT 6 113			
CLKOUT_CPUBCLK_P	J4	CPU_CLK100M_BCLK_P	OUT 6 113			
CLKOUT_CPUNSSC_N	H1	CPU_CLK24M_NSSC_CLK_N	OUT 6 113			
CLKOUT_CPUNSSC_P	H2	CPU_CLK24M_NSSC_CLK_P	OUT 6 113			
CLKOUT_CPUPCIBCLK_N	J1	CPU_CLK100M_PCIBCLK_N	OUT 6 113			
CLKOUT_CPUPCIBCLK_P	J2	CPU_CLK100M_PCIBCLK_P	OUT 6 113			

R1238 47K, R1239 47K, R1240 47K, R1241 100K, R1242 100K, R1243 100K, R1244 100K, R1245 100K, R1246 100K — 5% 1/20W MF 201

PP3V3_S0 14 20 73 110

GPP_B5/SRCCLKREQ0*	AL20	AP_CLKREQ_L_R	BI 20
GPP_B6/SRCCLKREQ1*	AM19	ENETSD_CLKREQ_L	IN 20
GPP_B7/SRCCLKREQ2*	AK20	CAMERA_CLKREQ_L	IN 20
GPP_B8/SRCCLKREQ3*	AL19	TBT_X_CLKREQ_L_R	IN 20
GPP_B9/SRCCLKREQ4*	AH22	TBT_T_CLKREQ_L_R	IN 20
GPP_B10/SRCCLKREQ5*	AK22	SSD_CLKREQ_L_R	BI 20
GPP_H0/SRCCLKREQ6*	AM25	TBT_W_CLKREQ_L	IN 20
GPP_H1/SRCCLKREQ7*	AH26	EG_CLKREQ_OUT_L	111
GPP_H2/SRCCLKREQ8*	AL25	AP_S0IX_WAKE_SEL	OUT 12 19
GPP_H3/SRCCLKREQ9*	AF26	AP_S0IX_WAKE_L	IN 12 19
GPP_H4/SRCCLKREQ10*	AK26	TBT_X_CIO_PWR_EN	OUT 29
GPP_H5/SRCCLKREQ11*	AL26	TBT_T_CIO_PWR_EN	OUT 103
GPP_H6/SRCCLKREQ12*	AJ27	TBT_W_CIO_PWR_EN	OUT 20
GPP_H7/SRCCLKREQ13*	AH27	TBT_X_USB_PWR_EN	OUT 29
GPP_H8/SRCCLKREQ14*	AM26	TBT_T_USB_PWR_EN	OUT 103
GPP_H9/SRCCLKREQ15*	AK27	TBT_W_USB_PWR_EN	OUT 20

BOM_COST_GROUP=CPU & CHIPSET

PP3V3_S4 110
SSD_SR_EN_L 12 — R1211 100K 5% 1/20W MF 201

PP3V3_SUS 110 17 16 14
PM_SYSRST_L 115 46 18 12 — R1247 3.0K 5% 1/20W MF 201

PP3V3_SUS 110 17 16 15

PP3V3_S5 110 17 16

PCIE_WAKE_L 19 12	R1248	100K
SMC_WAKE_SCI_L 46 12	R1209	100K
PM_PWRBTN_L 48 12	R1210	1K
PM_BATLOW_L 103 46 29 12	R1212	10K
SMC_RUNTIME_SCI_L 46 12	R1207	100K
LPC_CLKRUN_L 46 12	R1208	10K
PCH_RCIN_L_PU 12	R1251	100K

5% 1/20W MF 201

PP3V3_S0 110 15 13 12

LPC_SERIRQ 46 12	R1206	10K
AUD_PWR_EN 59 12	R1214	100K
CAMERA_PWR_EN 12	R1215	100K
AP_S0IX_WAKE_L 19 12	R1216	100K
PM_SLP_S5_L 73 46 20 12	R1230	100K
PM_SLP_S4_L 73 70 46 43 20 12	R1231	100K
PM_SLP_S3_L 114 101 89 76 73 70 46 27 20 12	R1232	100K
PM_SLP_S0_L 70 46 20 12	R1233	100K
AP_S0IX_WAKE_SEL 19 12	R1236	100K
PM_SLP_SUS_L 73 70 12	R1237	100K

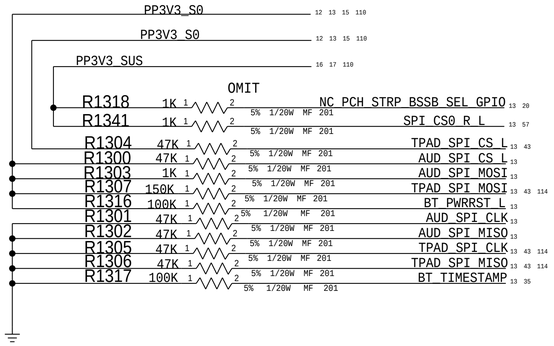
5% 1/20W MF 201

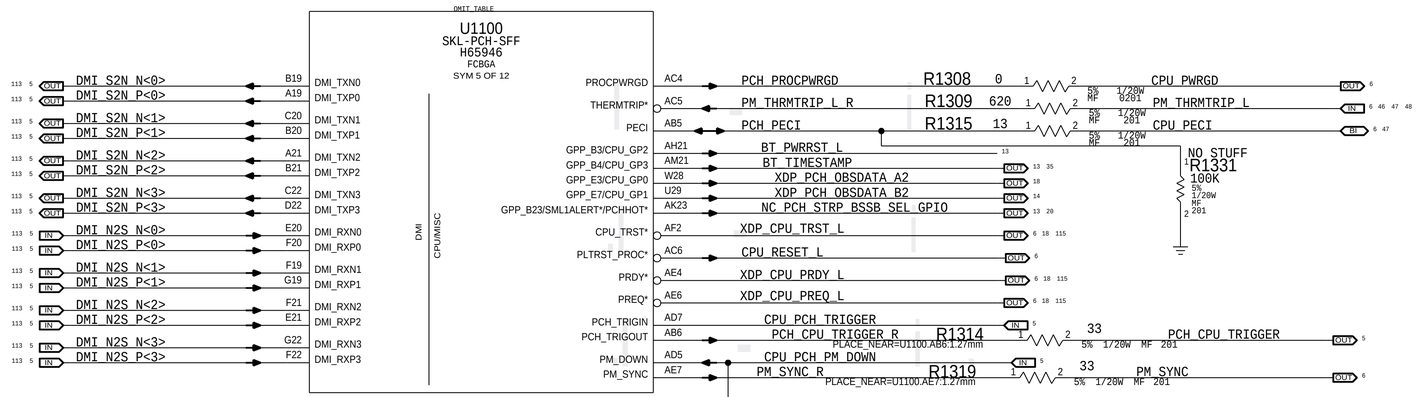
PP3V3_S0 110 15 13 12
BT_LOW_PWR_L 35 12 — R1213 10K 5% 1/20W MF 201

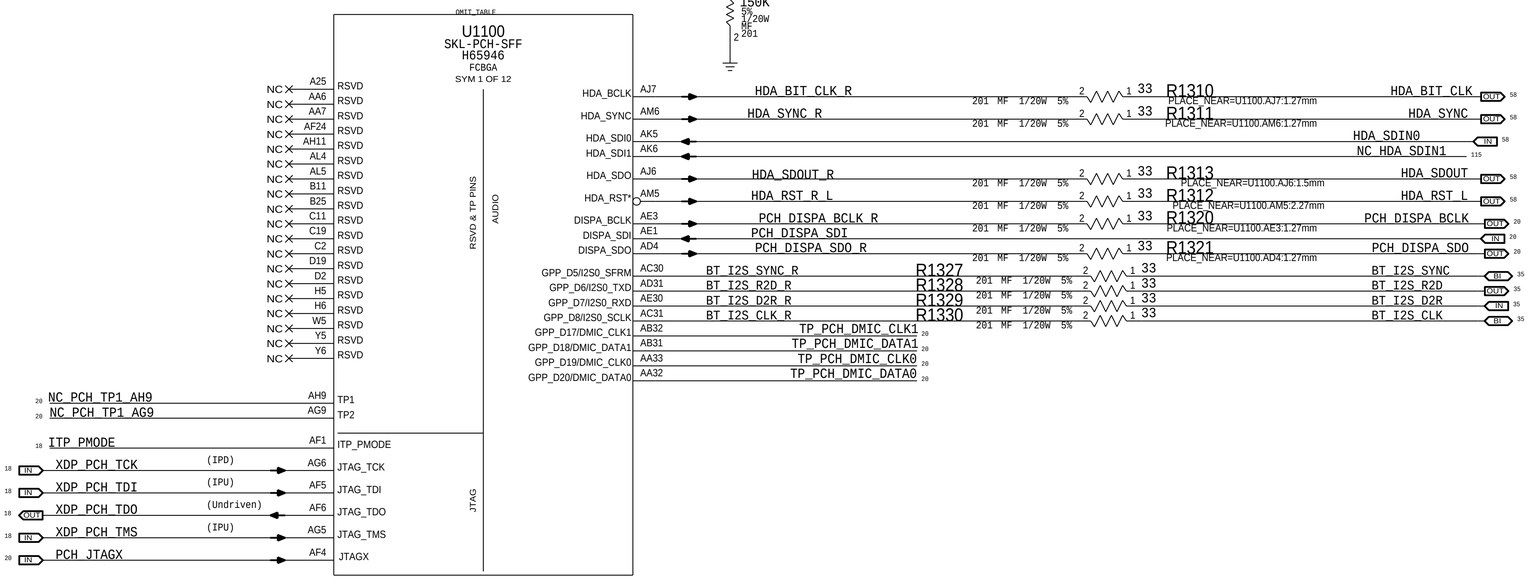
PAGE TITLE: PCH RTC/HDA/JTAG/SATA/CLK

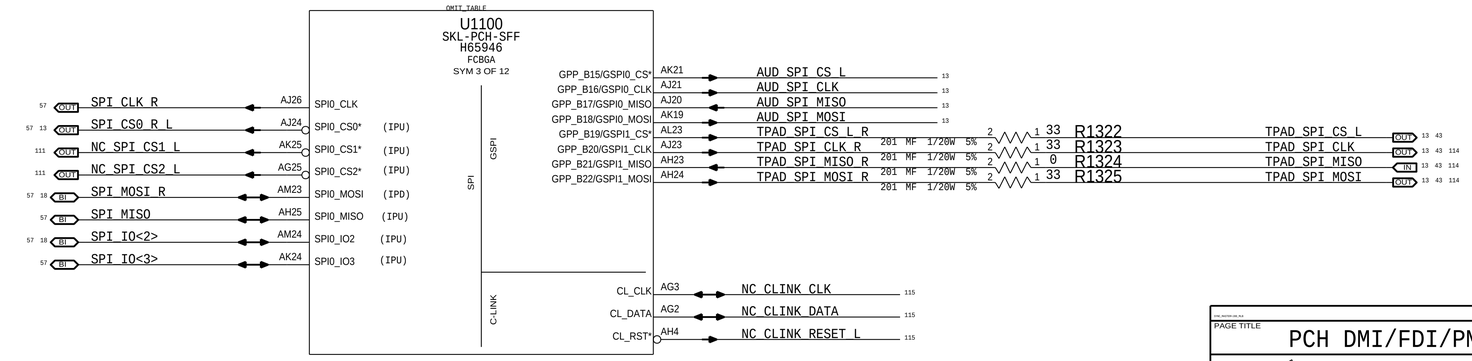
Apple Inc.

DRAWING NUMBER: 051-00789
SIZE: D
REVISION: PROTO1A
BRANCH: dvt-fab10
PAGE: 12 OF 145
SHEET: 12 OF 121







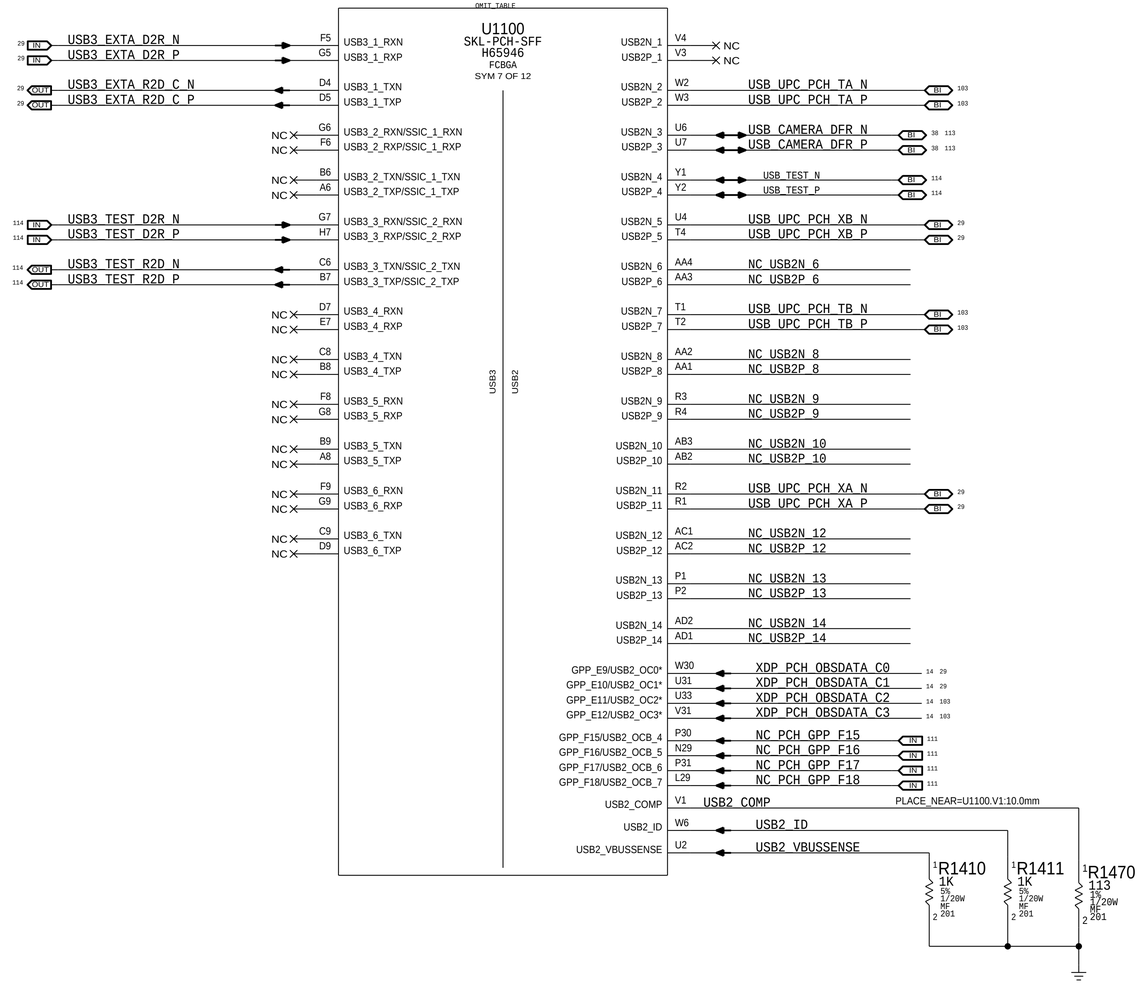


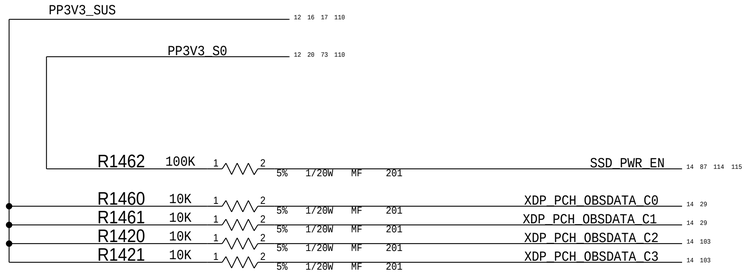
BOM_COST_GROUP=CPU & CHIPSET

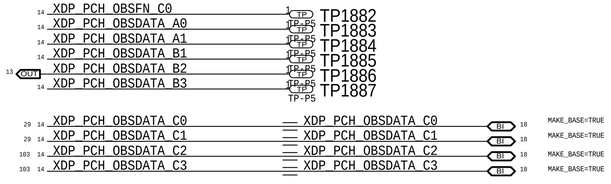
PAGE TITLE
PCH DMI/FDI/PM/GFX/PCI

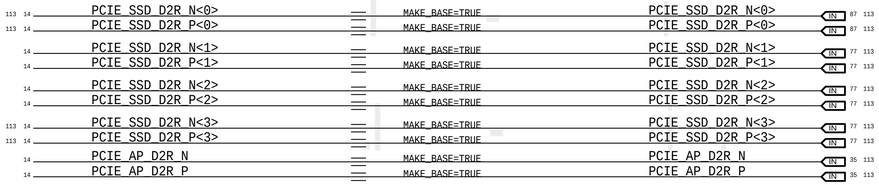
Apple Inc.

DRAWING NUMBER 051-00789 | SIZE D
REVISION PROTO1A
BRANCH dvt-fab10
PAGE 13 OF 145
SHEET 13 OF 121







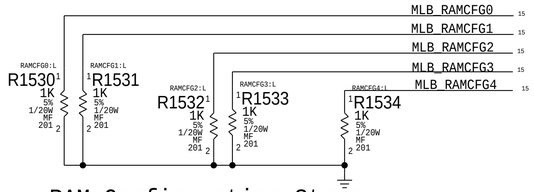


BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
PCH PCI-E/USB

Apple Inc.

DRAWING NUMBER	051-00789
SIZE	D
REVISION	PROTO1A
BRANCH	dvt-fab10
PAGE	14 OF 145
SHEET	14 OF 121

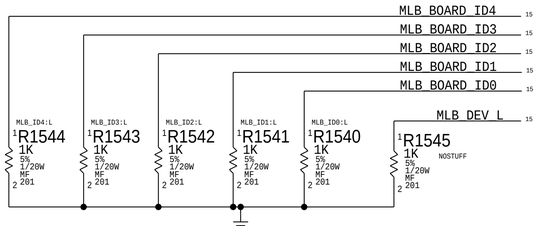


RAM Configuration Straps

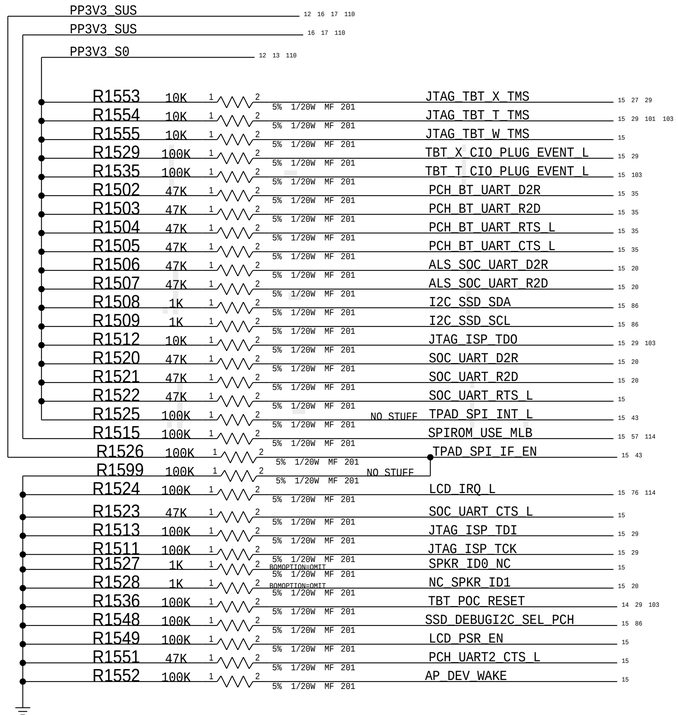
BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG4:L,RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L

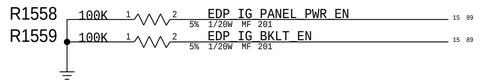
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
117S0006	0	RES,MF,1/20W,1KOHM,5%,0201,SMD		BOARD_ID:1F
117S0006	1	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1540	BOARD_ID:1E
117S0006	1	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1541	BOARD_ID:1D
117S0006	2	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1541,R1540	BOARD_ID:1C
117S0006	1	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1542	BOARD_ID:1B
117S0006	2	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1542,R1540	BOARD_ID:1A
117S0006	2	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1542,R1541	BOARD_ID:19
117S0006	3	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1542,R1541,R1540	BOARD_ID:18
117S0006	1	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1543	BOARD_ID:17
117S0006	2	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1543,R1540	BOARD_ID:16
117S0006	2	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1543,R1541	BOARD_ID:15
117S0006	3	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1543,R1541,R1540	BOARD_ID:14

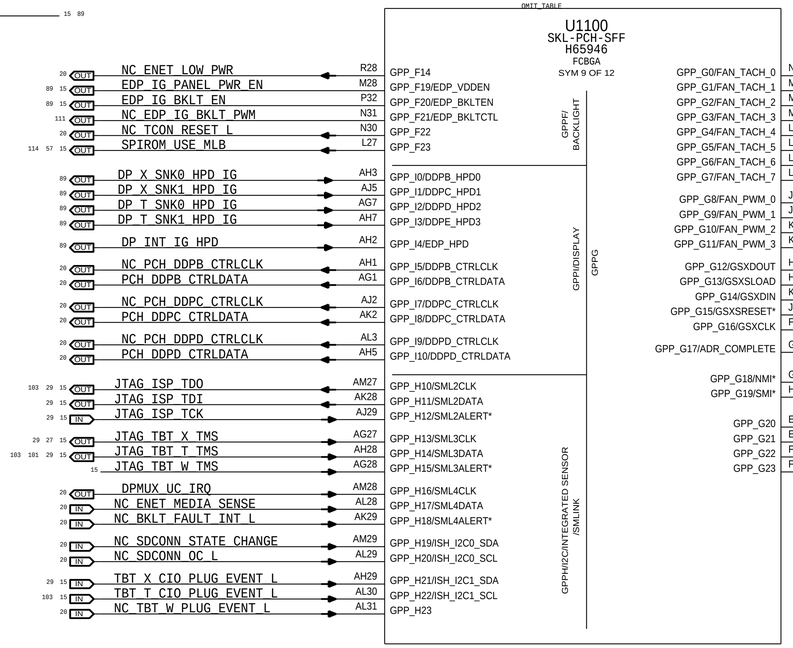
```
PROTO 0 = 0x1F = 1 1 1 1 1 (-01 PCB)
PROTO 0B = 0x1E = 1 1 1 1 0 (-02 PCB)
PROTO 1 = 0x1D = 1 1 1 0 1 (-03 PCB)
PROTO 2 = 0x1C = 1 1 1 0 0 (-04 & -05 PCB)
EVT1 = 0x1B = 1 1 0 1 1 (-06 PCB)
EVT2 = 0x1A = 1 1 0 1 0 (-07 PCB)
DVT = 0x19 = 1 1 0 0 1 (-08 PCB)
DVT1-1 = 0x18 = 1 1 0 0 0 (-09 PCB)
PVT = 0x17 = 1 0 1 1 1 (-10 PCB)
0x16 = 1 0 1 1 0
0x15 = 1 0 1 0 1
0x14 = 1 0 1 0 0
```

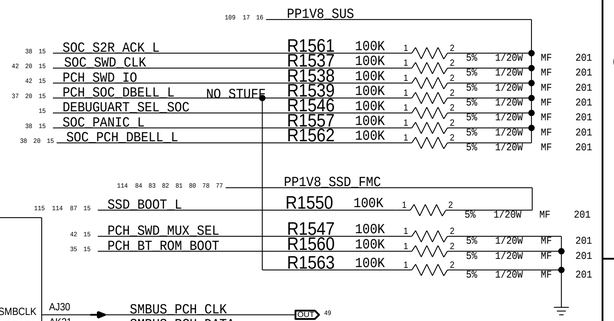


MLB BOARD ID Configuration Straps









BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE

PCH GPIO/MISC/NCTF

Apple Inc.

DRAWING NUMBER 051-00789 | SIZE D

REVISION PROTO1A

BRANCH dvt-fab10

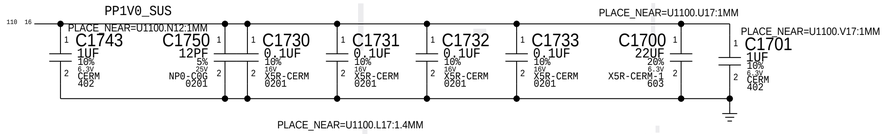
PAGE 15 OF 145

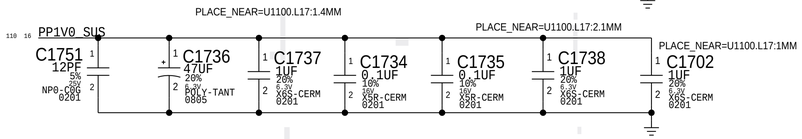
SHEET 15 OF 121

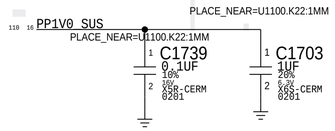
PAGE TITLE	PCH Power
DRAWING NUMBER	051-00789
SIZE	D
REVISION	PROTO1A
BRANCH	dvt-fab10
PAGE	16 OF 145
SHEET	16 OF 121

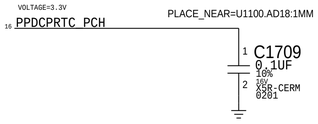
Apple Inc.

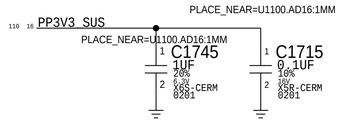
1000PF CAPS ARE INTEL PLACEHOLDERS & ALL PLACENEAR NEED TO BE UPDATED

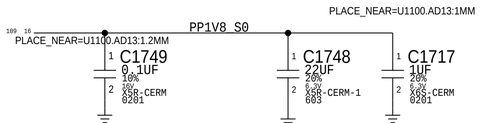


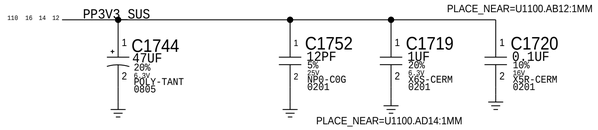


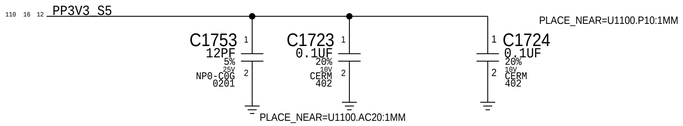


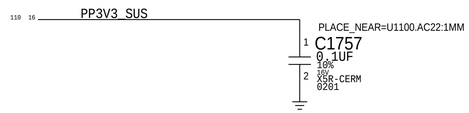


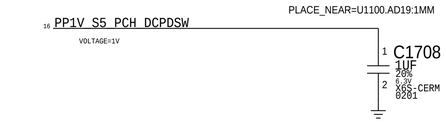


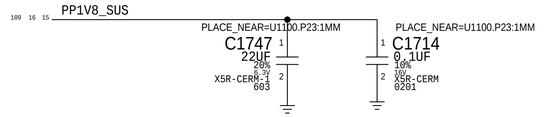


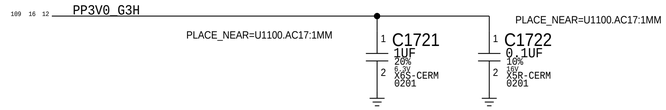






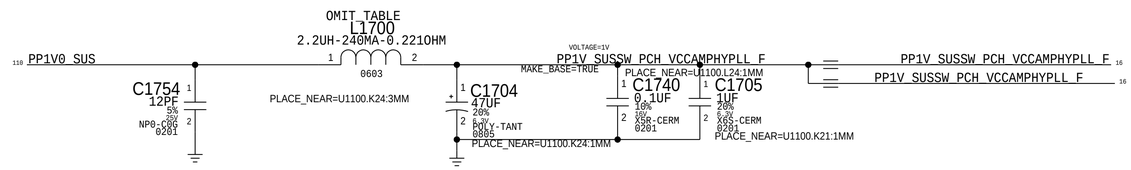


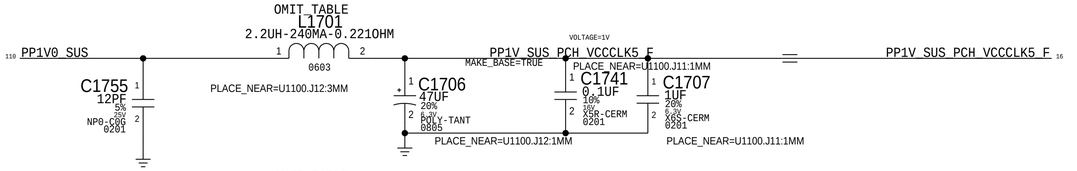


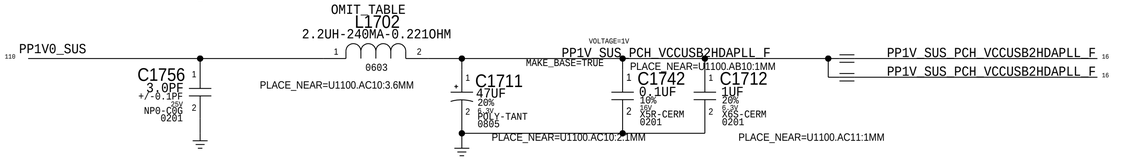


RAIL SIDE

PCH SIDE







PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0022	3	RES,MF,1A MAX,00HM,5%,0603	L1700,L1701,L1702		

Current data from LPT EDS (doc #486708, Rev 1.0).

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE

PCH DECOUPLING

Apple Inc.

DRAWING NUMBER 051-00789 SIZE D

REVISION PROTO1A

BRANCH dvt-fab10

PAGE 17 OF 145

SHEET 17 OF 121

Primary / Merged (CPU/PCH) Micro2-XDP

Extra BPM Testpoints

XDP_BPM_L<0> → TP1800
XDP_BPM_L<1> → TP1801
XDP_BPM_L<2> → TP1802
XDP_BPM_L<3> → TP1803

(TP-P6)

PCH XDP Signals

These signals do not connect to the Primary (Merged) XDP connector in this architecture.
The PDG puts them on a secondary XDP connector that is only needed in some PCH debugging situation.
They are listed here to show their secondary XDP functions and to provide test points for signals that are not used elsewhere.

PCH/XDP Signals	Non-XDP Signals
XDP_PCH_OBSDATA_A2	TP1870
XDP_PCH_OBSDATA_A3	TP1871
XDP_PCH_OBSDATA_B0	TP1872
XDP_PCH_OBSDATA_C0	TP1873
XDP_PCH_OBSDATA_C1	TP1874
XDP_PCH_OBSDATA_C2	TP1875
XDP_PCH_OBSDATA_C3	TP1876
XDP_PCH_OBSDATA_D0	TP1877
XDP_PCH_OBSDATA_D1	TP1878
XDP_PCH_OBSDATA_D2	TP1879
XDP_PCH_OBSDATA_D3	TP1880
XDP_PCH_OBSFN_C1	TP1881

Unused GPIOs have TPs.

USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.

JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.

PP1V0_SUS

PULL CFG<3> LOW WHEN XDP PRESENT
PLACE_NEAR=U0500.BN28:2.54MM
XDP:YES R1801 1K 5% 1/20W MF 201 — NO_XNET_CONNECTION

XDP_CONN J1800
DF40RC-60DP-0.4V
M-ST-SM1

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

J1800 pin	Net	J1800 pin	Net
62		61	
2	XDP_PRESENT_CPU	1	
4	XDP_CPU_PREQ_L	3	CPU_CFG<17>
6	XDP_CPU_PRDY_L	5	CPU_CFG<16>
8		7	
10	CPU_CFG<0>	9	CPU_CFG<8>
12	CPU_CFG<1>	11	CPU_CFG<9>
14		13	
16	CPU_CFG<2>	15	CPU_CFG<10>
18	CPU_CFG<3>	17	CPU_CFG<11>
20		19	
22	NC	21	CPU_CFG<19>
24	NC	23	CPU_CFG<18>
26		25	
28	CPU_CFG<4>	27	CPU_CFG<12>
30	CPU_CFG<5>	29	CPU_CFG<13>
32		31	
34	CPU_CFG<6>	33	CPU_CFG<14>
36	CPU_CFG<7>	35	CPU_CFG<15>
38		37	
40	XDP_PM_RSMRST_L	39	ITPCLK/HOOK4 — NC_ITPXDP_CLK100MP
42	XDP_CPU_PWRBTN_L	41	ITPCLK#/HOOK5 — NC_ITPXDP_CLK100MN
44	VCC_OBS_AB	43	VCC_OBS_CD
46	NC	45	RESET#/HOOK6 — ITP_PMODE
48	SPI_MOSI_R_CONN	47	DBR#/HOOK7 — XDP_DBRESET_L
50		49	
52	NC SDA	51	TDO
54	NC SCL	53	TRSTn
56	TCK1	55	TDI
58	TCK0	57	TMS
60		59	XDP_PRESENT#
64		63	

518S0847

OBSFN_A0, OBSFN_A1, OBSDATA_A0, OBSDATA_A1, OBSDATA_A2, OBSDATA_A3, OBSFN_B0, OBSFN_B1, OBSDATA_B0, OBSDATA_B1, OBSDATA_B2, OBSDATA_B3, HOOK0, HOOK1, HOOK2, HOOK3, SCL, SDA

PP3V3_SUS — PLACE_NEAR=J1800.48:2.54MM
XDP:YES R1804 1K 5% 1/20W MF 201

PM_RSMRST_L → R1800 1K XDP:YES — PLACE_NEAR=U1100.AF12:3.8MM
PM_PWRBTN_L → R1802 10 XDP:YES — PLACE_NEAR=U1100.AM10:3MM
SPI_MOSI_R → R1803 1K XDP:YES — PLACE_NEAR=U1100.AM23:2.54MM
XDP_CPU_TCK → PCH_JTAGX R1835 0 XDP:YES — PLACE_NEAR=J1800.58:28MM
XDP_PCH_TCK

C1804 0.1UF 10% 6.3V CERM-X5R 0201 — PLACE_NEAR=J1800.42:28MM
C1800 0.1UF 10% 6.3V CERM-X5R 0201 — PLACE_NEAR=J1800.44:28MM
C1801 0.1UF 10% 6.3V CERM-X5R 0201 — PLACE_NEAR=J1800.43:28MM
C1806 0.1UF 10% 6.3V CERM-X5R 0201 — PLACE_NEAR=J1800.47:28MM

PP1V0_S0SW

XDP_PCH_TDO	R1890 51	PLACE_NEAR=U1100.AF6:28MM	XDP:YES
XDP_PCH_TDI	R1891 51	PLACE_NEAR=U1100.AF5:28MM	XDP:YES
XDP_PCH_TMS	R1892 51	PLACE_NEAR=U1100.AG5:28MM	XDP:YES
XDP_CPU_TDO	R1810 51	PLACE_NEAR=U0500.BT28:28MM	XDP:YES
XDP_CPU_TCK	R1813 51	PLACE_NEAR=U0500.BR28:28MM	XDP:YES
XDP_PCH_TCK	R1897 51	PLACE_NEAR=U1100.AG6:28MM	NOSTUFF
XDP_PCH_TRST_L	R1898 51	PROPER WAY TO TERMINATE?	NOSTUFF

R1830 1K 5% 1/20W MF 201 — PLACE_NEAR=U0500.EB:2.54MM

XDP:YES R1806 0 5% 1/20W MF 0201 — PM_SYSRST_L

ROUTE IN STAR TOPOLOGY FROM XDP CONNECTOR.

XDP_CPU_TDO	R1821 0	PLACE_NEAR=J1800.51:2.54MM	XDP:YES
XDP_CPU_TRST_L	R1822 0	PLACE_NEAR=J1800.53:2.54MM	XDP:YES
XDP_CPU_TDI	R1823 0	PLACE_NEAR=J1800.55:2.54MM	XDP:YES
XDP_CPU_TMS	R1824 0	PLACE_NEAR=J1800.57:2.54MM	XDP:YES

XDP_PCH_TDO
XDP_PCH_TRST_L
XDP_PCH_TDI
XDP_PCH_TMS

PP3V3_SUS
XDP:YES C1830 0.1UF 10% 10V X5R-CERM 0201
XDP:YES U1830 74AUP1G07GF SOT891 (VCC, A, Y, (OD), GND, NC)
PLACE_NEAR=U1830.4:7.54MM R1831 1.5K MF XDP:YES — SPI_IO2_STRAP_L → SPI_IO<2> (STRAP TO PCH) — NO_XNET_CONNECTION
PLACE_NEAR=U1830.4:2.54MM R1832 49.9 MF NOSTUFF 1% 1/20W 201 — NO_XNET_CONNECTION
XDP_PRESENT_L

PP3V3_SUS → XDP:YES R1850 100K 5% 1/20W MF 201

NEED TO CONNECT TO VCCST, *STG POWER LOGIC

BOM_COST_GROUP=DEBUG : 21:05:19

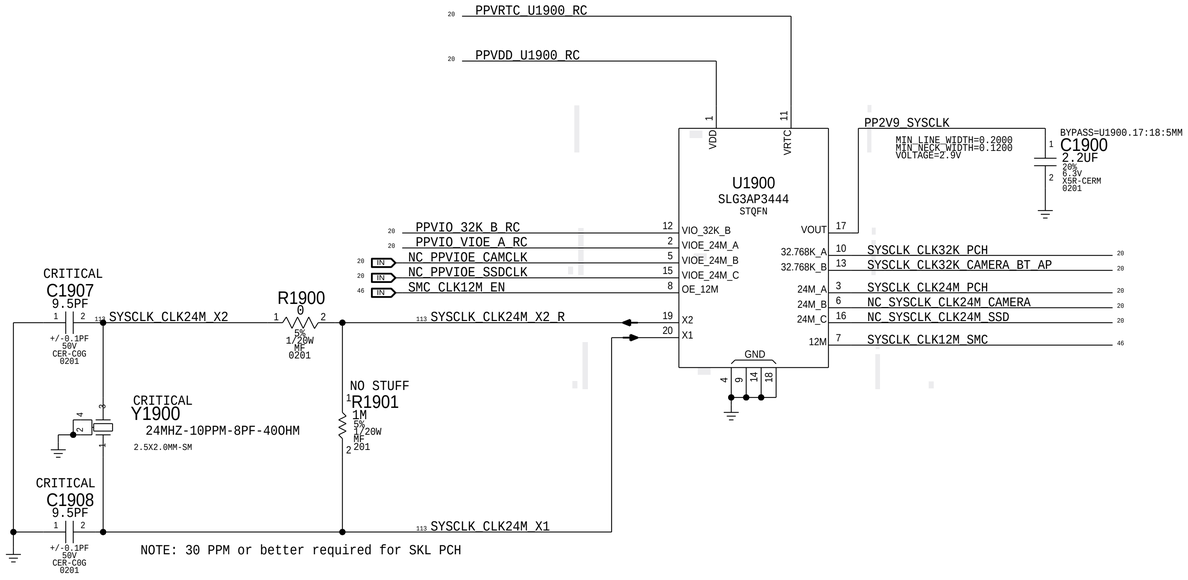
DESIGN: X502/MLB
LAST CHANGE: Mon Jun 15 22:04:28 2015

PAGE TITLE: CPU/PCH Merged XDP

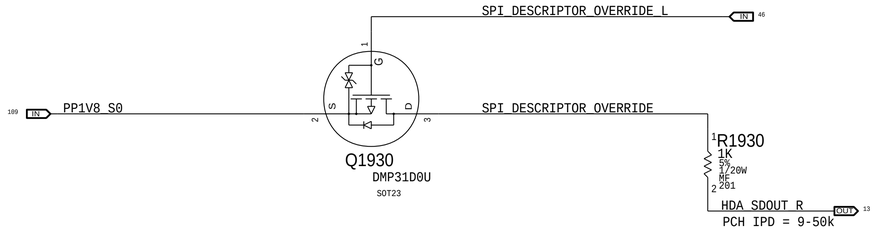
Apple Inc.

DRAWING NUMBER: 051-00789
SIZE: D
REVISION: PROTO1A
BRANCH: dvt-fab10
PAGE: 18 OF 145
SHEET: 18 OF 121

System 32kHz / 12MHz / 24MHz Clock Generator

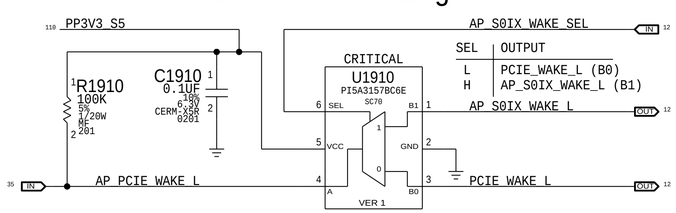


PCH ME Disable Strap



PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
***** Circuit does not support HDA voltage >3.3V.

PCIe Wake Muxing

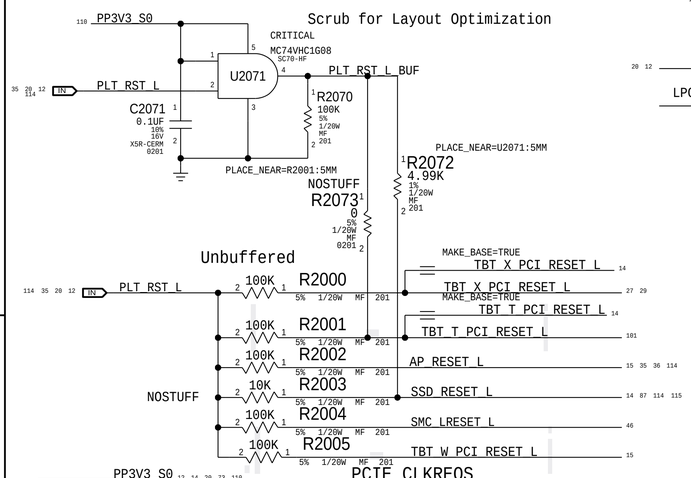


BOM_COST_GROUP=CPU & CHIPSET 9102.05_04

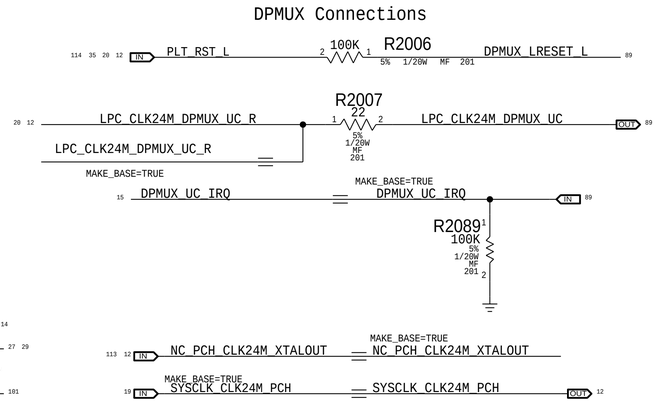
PAGE TITLE	Chipset Support 1
	Apple Inc.
DRAWING NUMBER	051-00789
SIZE	D
REVISION	PROTO1A
BRANCH	dvt-fab10
PAGE	19 OF 145
SHEET	19 OF 121

Platform Reset Connections

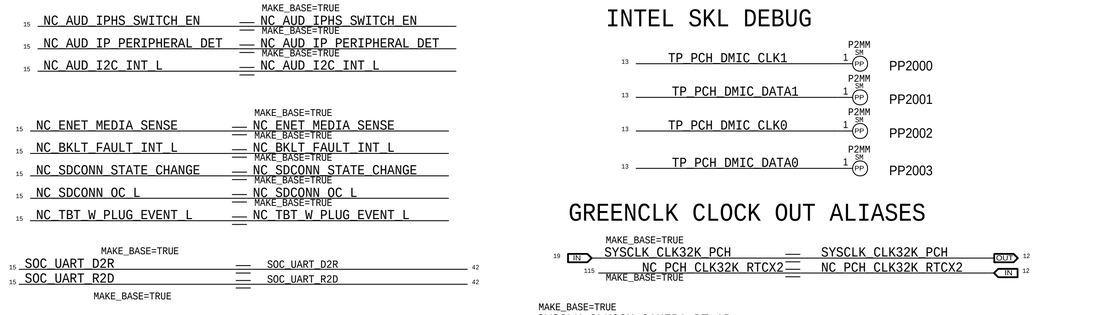
Buffered



DPMUX Connections

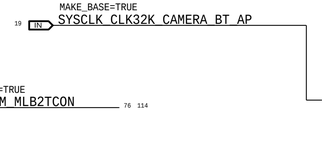


NC ALIASES 3

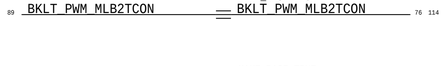


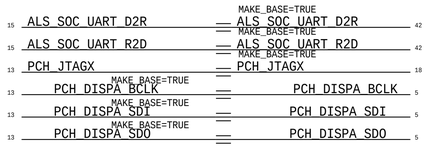
INTEL SKL DEBUG

GREENCLK CLOCK OUT ALIASES

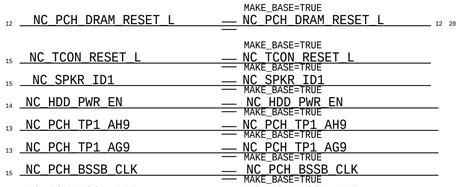


SIGNAL ALIASES

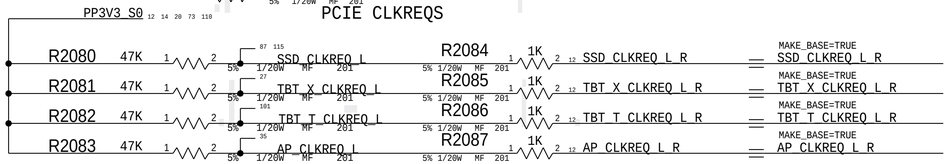




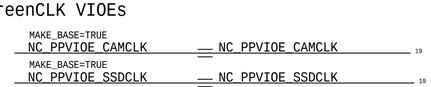
NC ALIASES



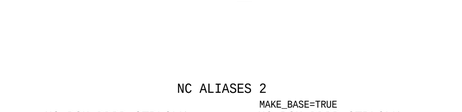
PCIE CLKREQS

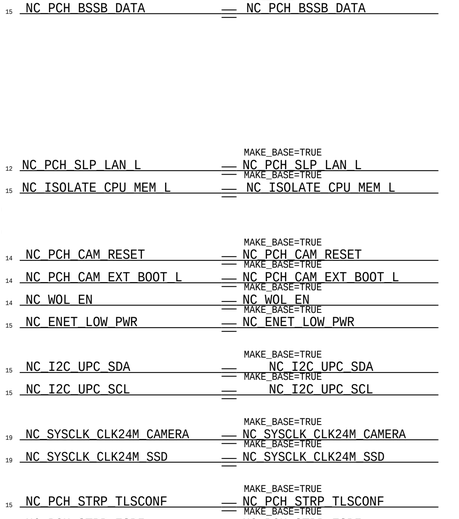


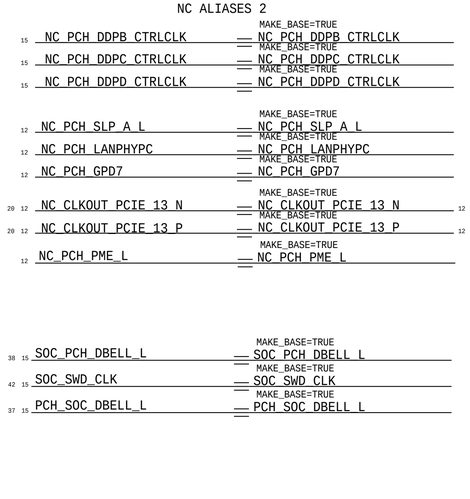
GreenCLK VIOEs

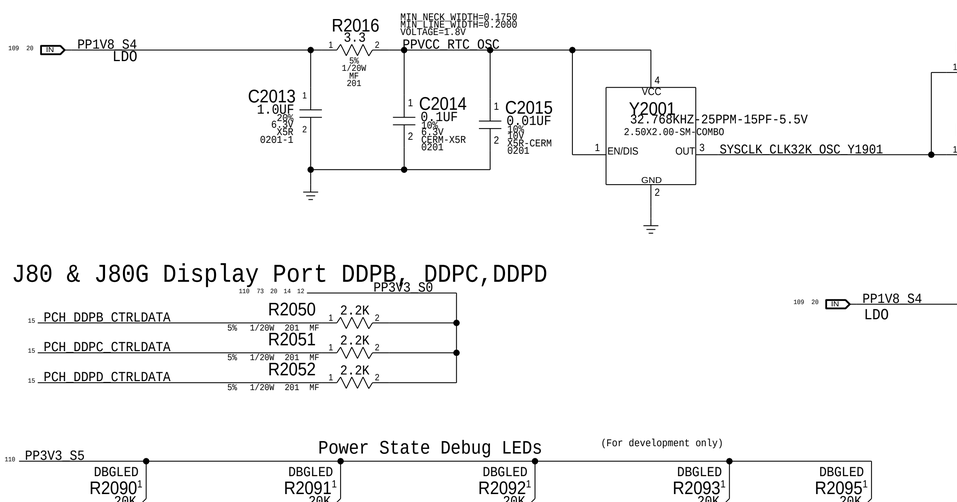


NC ALIASES 2

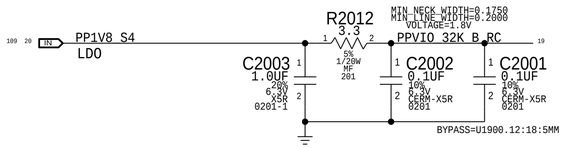






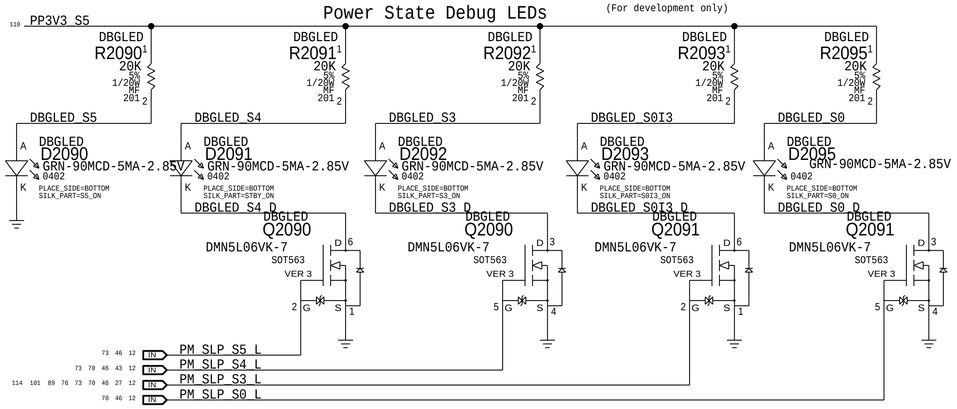


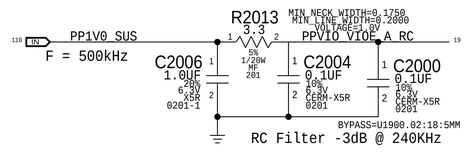
J80 & J80G Display Port DDPB, DDPC,DDPD

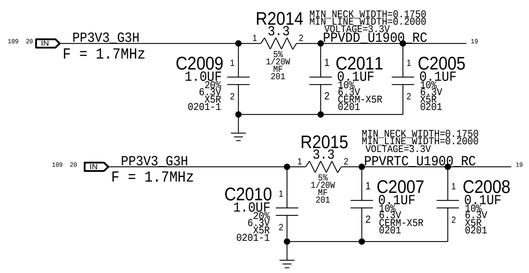


Power State Debug LEDs

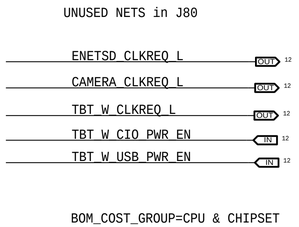
(For development only)







UNUSED NETS in J80



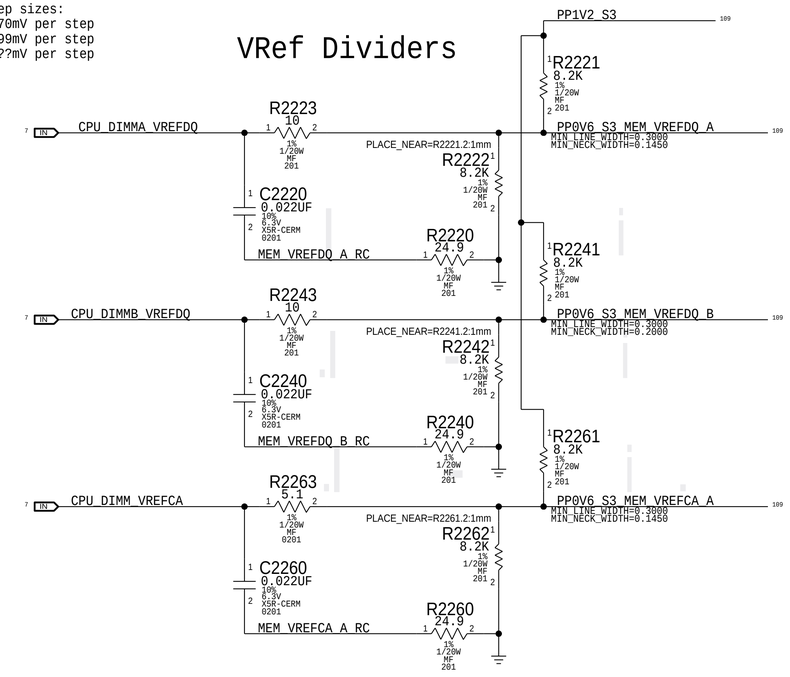
BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE	Chipset Support 2
	Apple Inc.
DRAWING NUMBER	051-00789
SIZE	D
REVISION	PROTO1A
BRANCH	dvt-fab10
PAGE	20 OF 145
SHEET	20 OF 121

CPU-Based Margining

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step
LPDDR3 (1.2V) ?.??mV per step

VRef Dividers



BOM_COST_GROUP=DRAM

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE: LPDDR3 VREF MARGINING

Apple Inc.

DRAWING NUMBER: 051-00789 SIZE: D

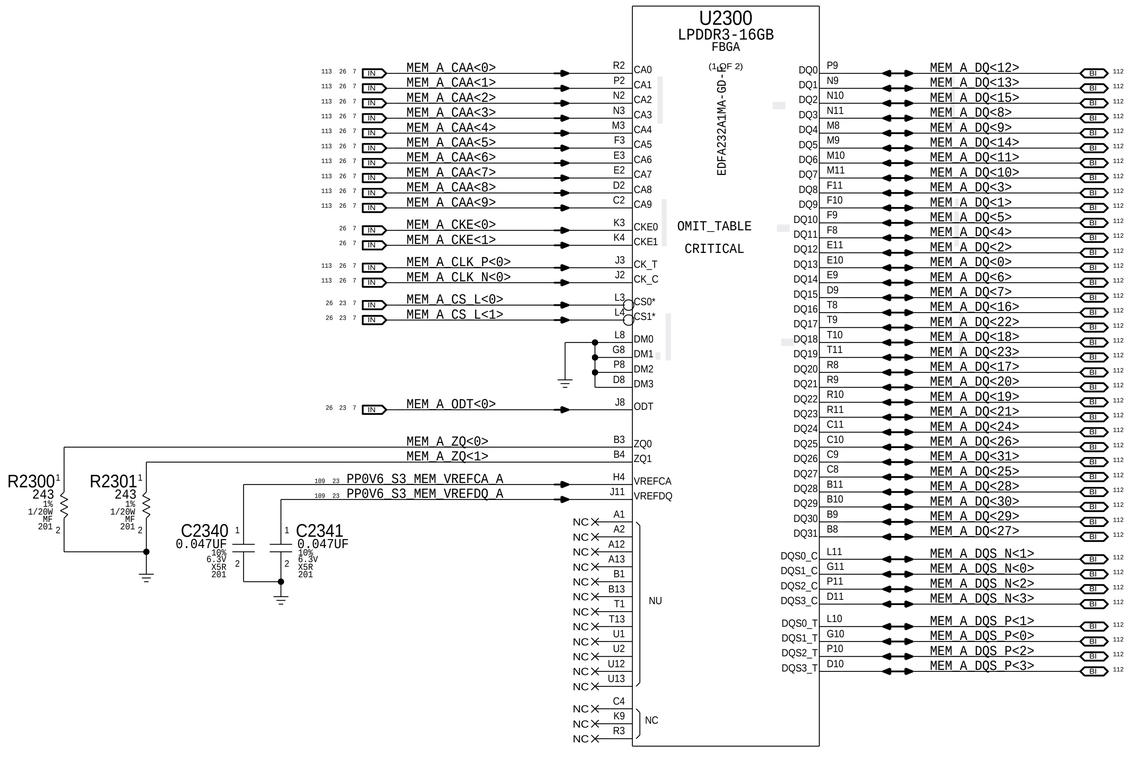
REVISION: PROTO1A

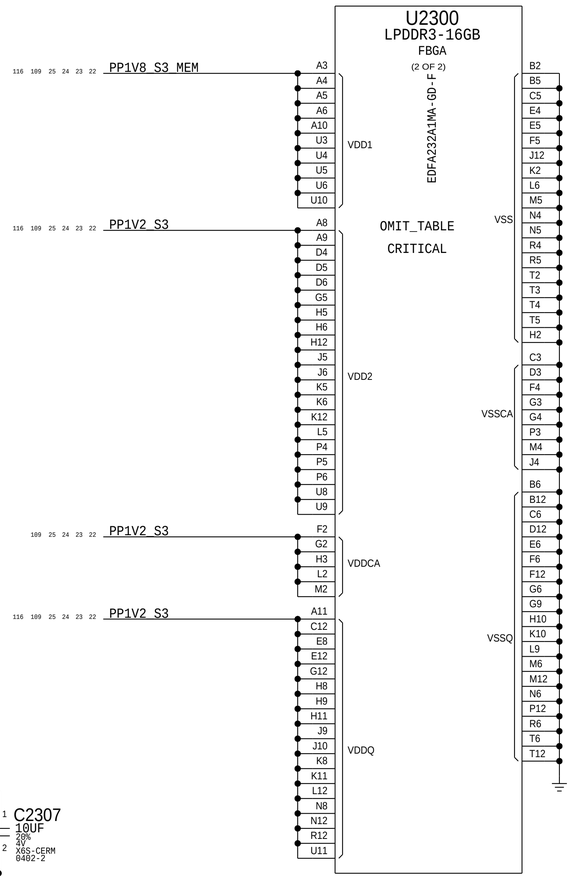
BRANCH: dvt-fab10

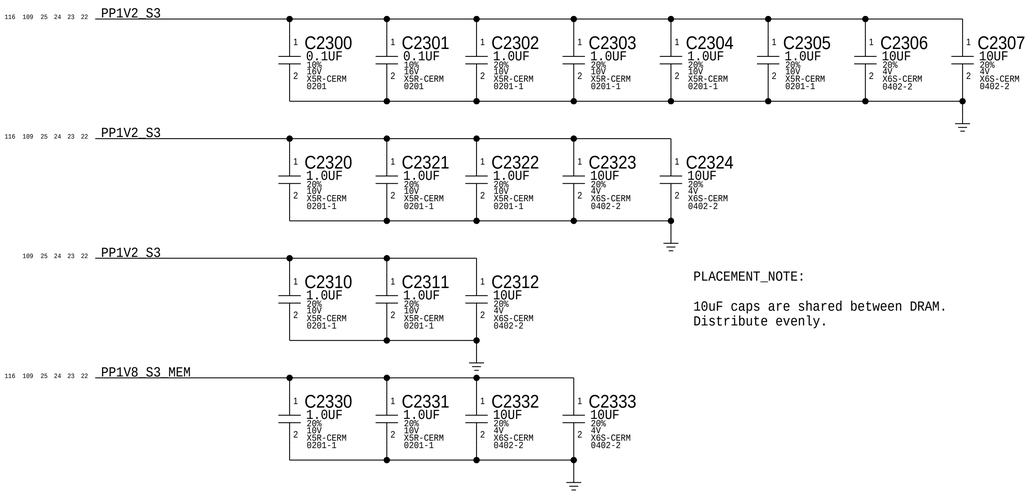
PAGE: 22 OF 145

SHEET: 21 OF 121

LPDDR3 CHANNEL A (0-31)







PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

BOM_COST_GROUP=DRAM

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE: LPDDR3 DRAM Channel A (0-31)

Apple Inc.

DRAWING NUMBER: 051-00789 SIZE: D

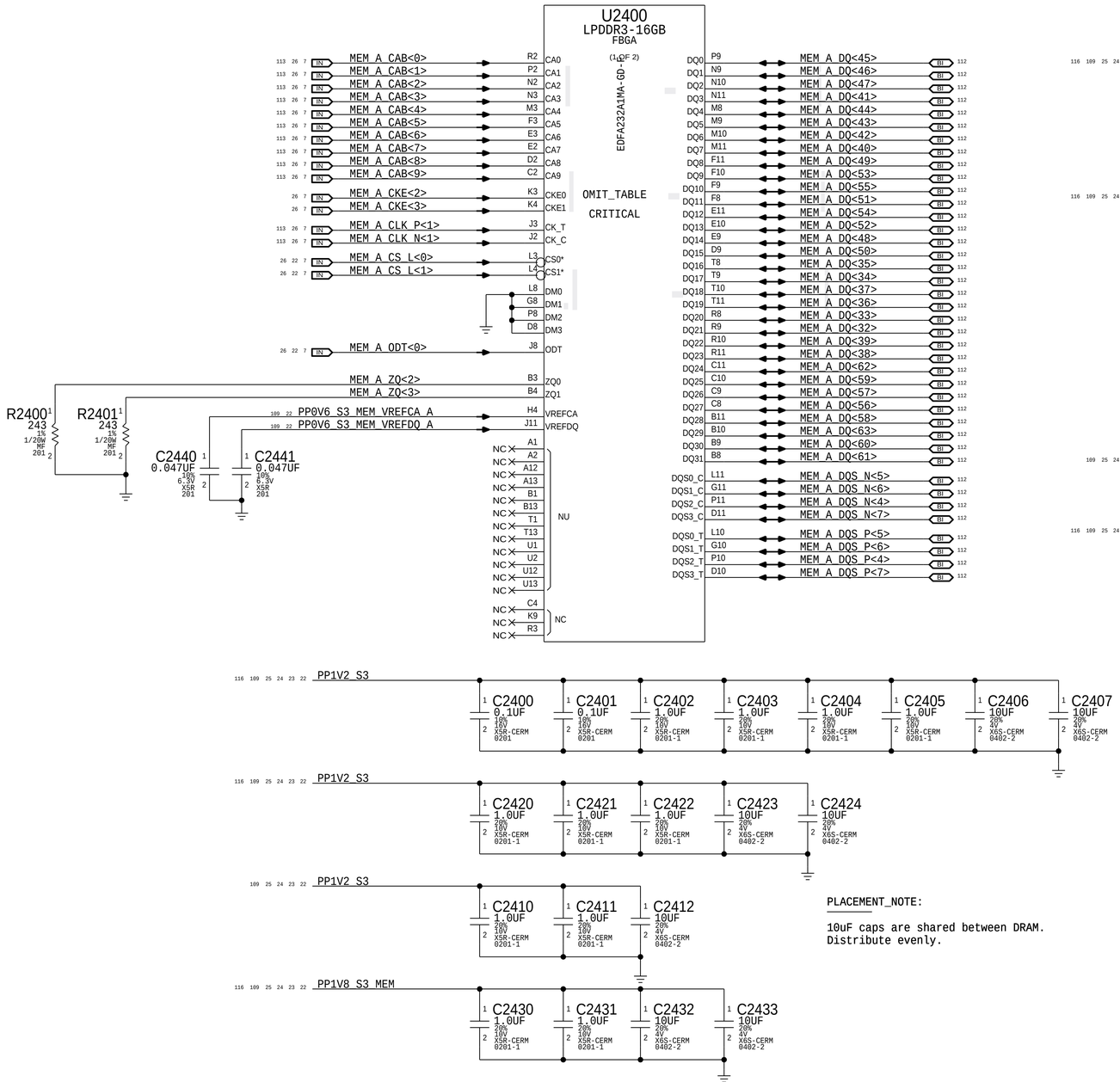
REVISION: PROTO1A

BRANCH: dvt-fab10

PAGE: 23 OF 145

SHEET: 22 OF 121

LPDDR3 CHANNEL A (32-63)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

BOM_COST_GROUP=DRAM

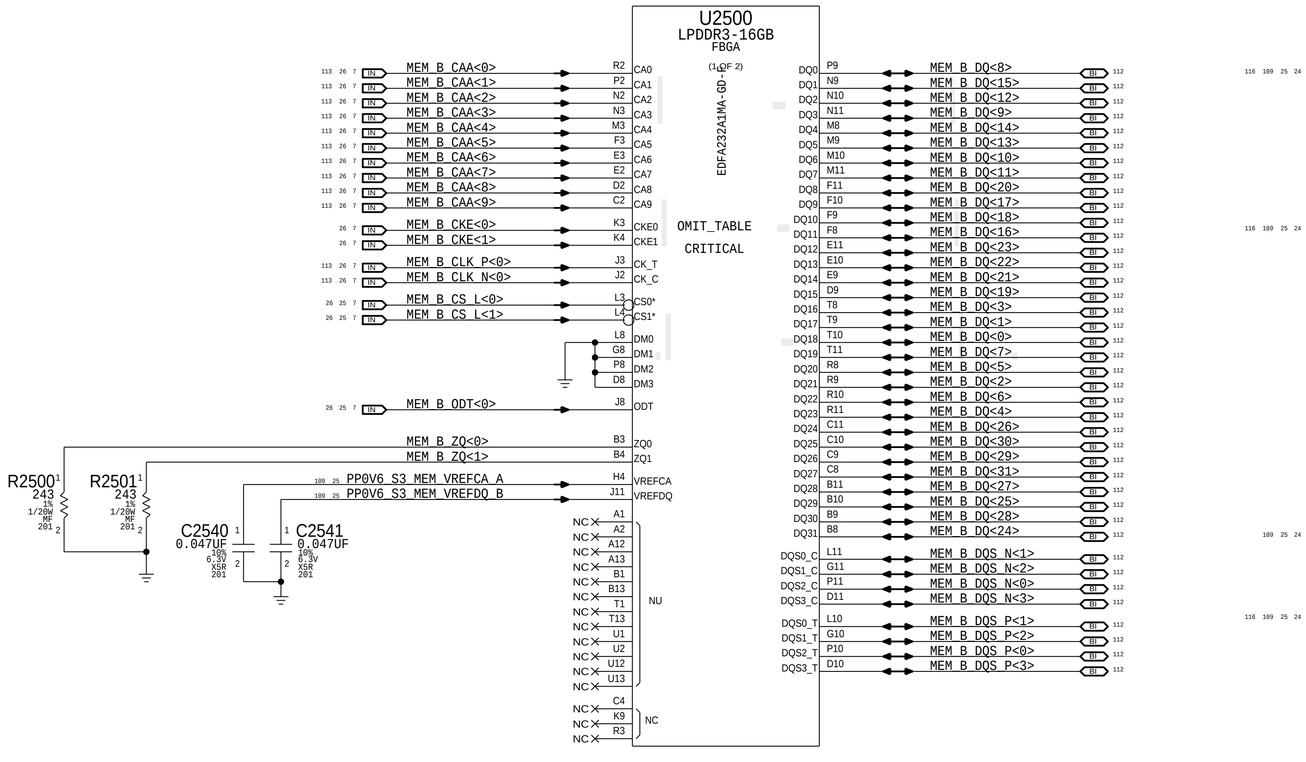
SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

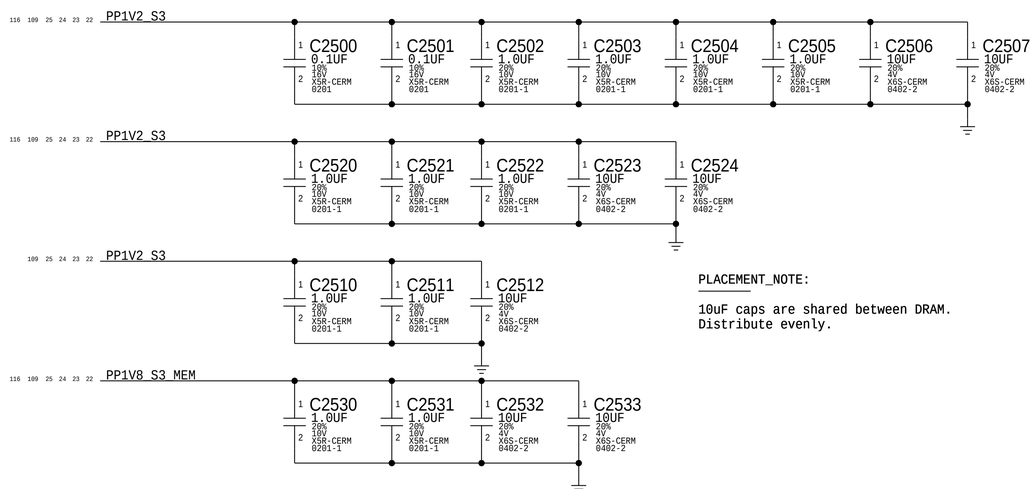
PAGE TITLE: LPDDR3 DRAM Channel A (32-63)

Apple Inc.

DRAWING NUMBER: 051-00789 SIZE: D
REVISION: PROTO1A
BRANCH: dvt-fab10
PAGE: 24 OF 145
SHEET: 23 OF 121

LPDDR3 CHANNEL B (0-31)





PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

BOM_COST_GROUP=DRAM

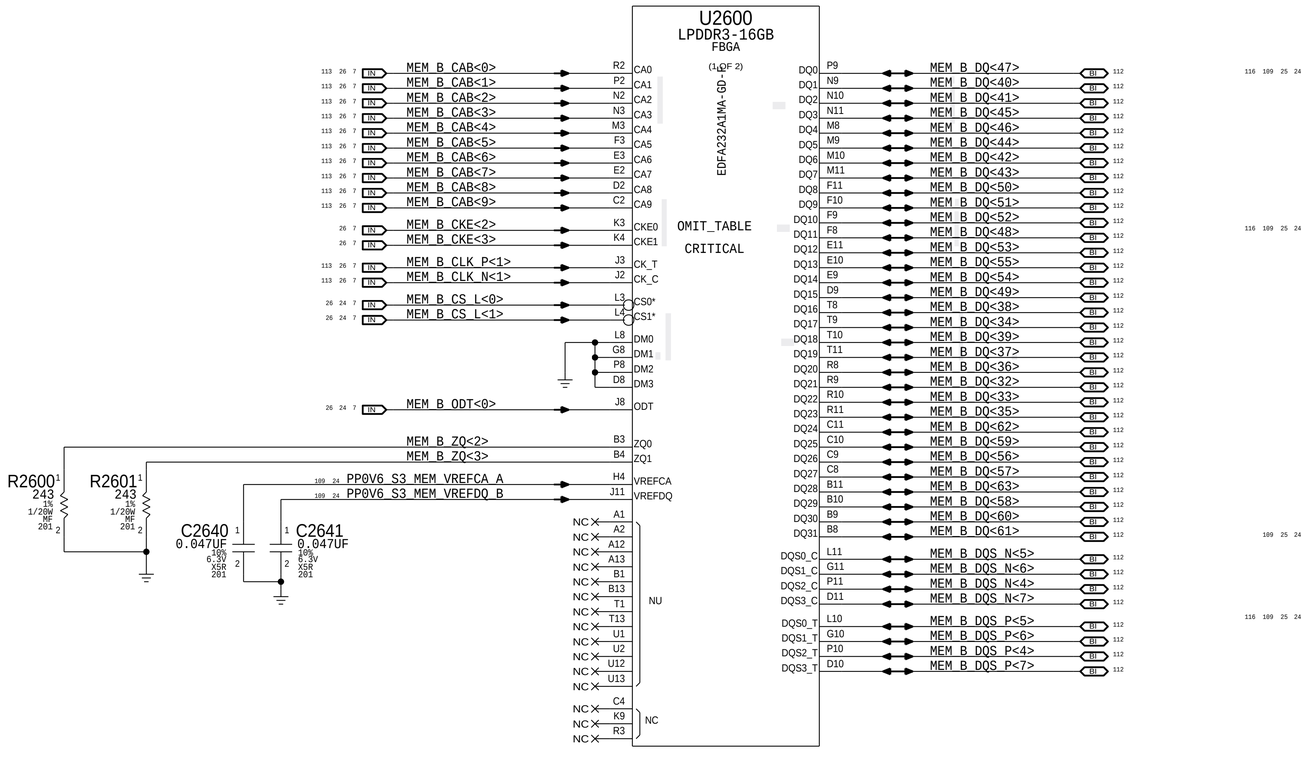
SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

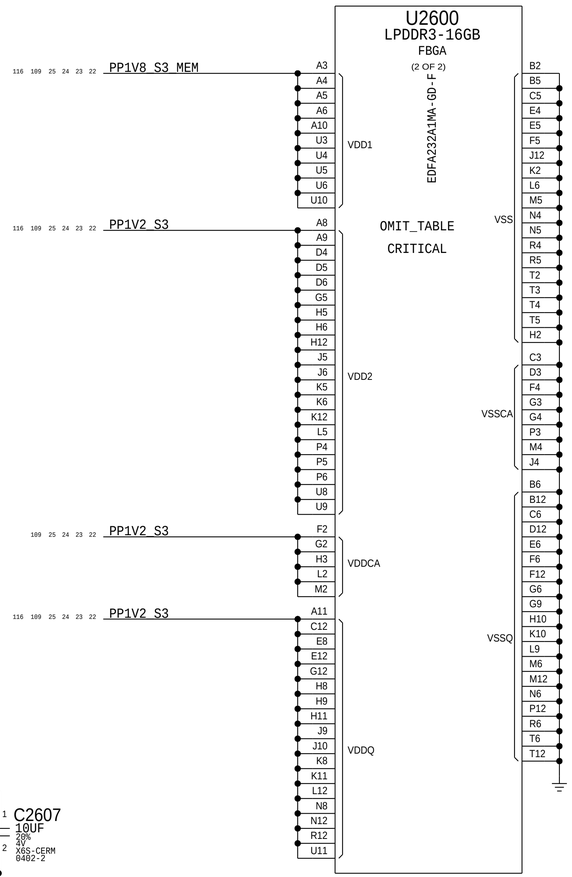
PAGE TITLE: LPDDR3 DRAM Channel B (0-31)

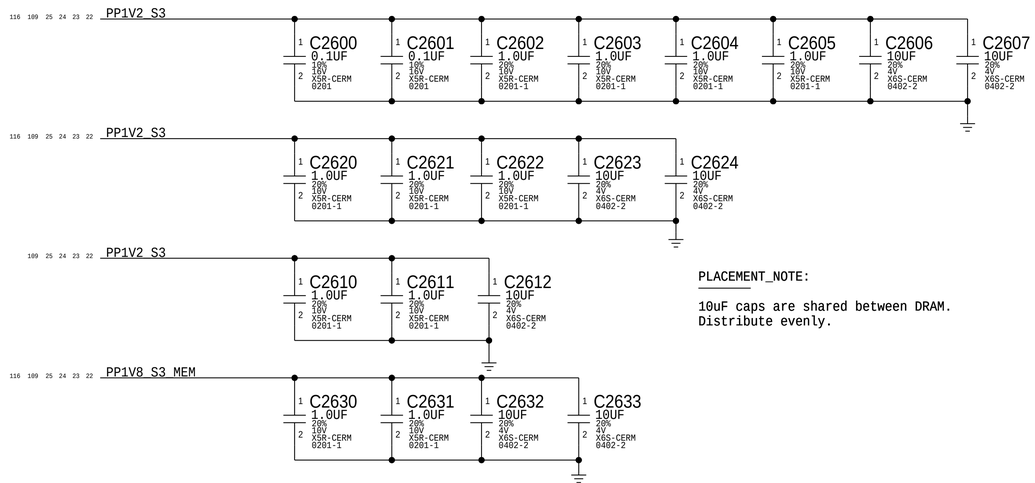
Apple Inc.

DRAWING NUMBER: 051-00789 SIZE: D
REVISION: PROTO1A
BRANCH: dvt-fab10
PAGE: 25 OF 145
SHEET: 24 OF 121

LPDDR3 CHANNEL B (32-63)







PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

BOM_COST_GROUP=DRAM

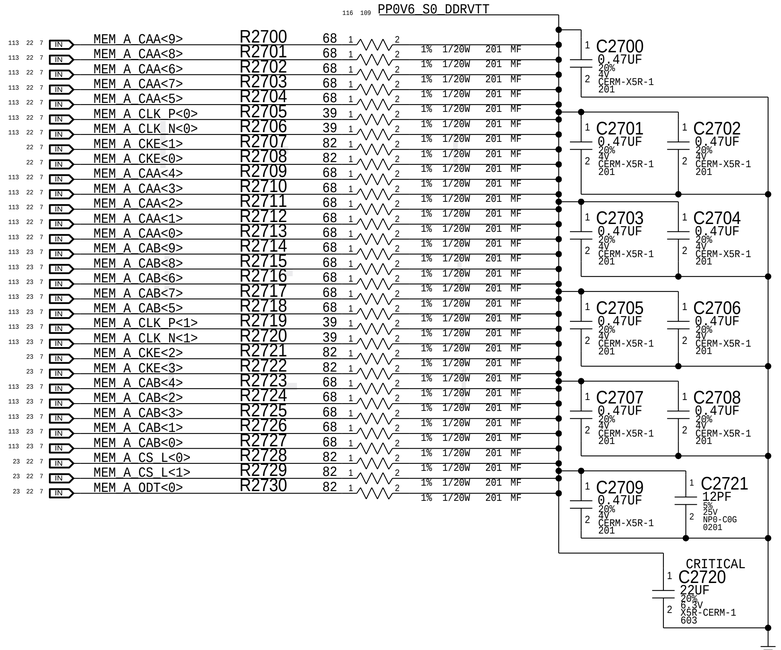
SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

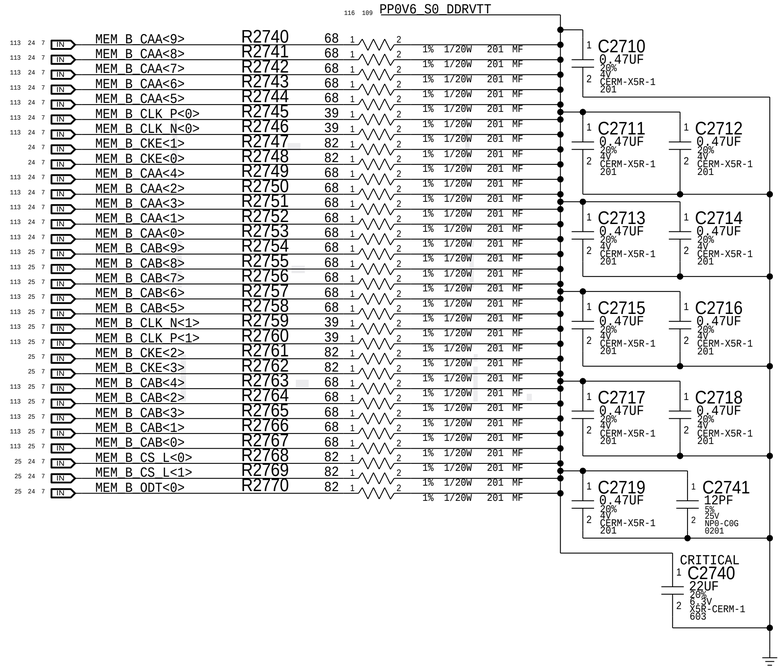
PAGE TITLE: LPDDR3 DRAM Channel B (32-63)

Apple Inc.

DRAWING NUMBER: 051-00789 SIZE: D
REVISION: PROTO1A
BRANCH: dvt-fab10
PAGE: 26 OF 145
SHEET: 25 OF 121

Intel recommends 68 Ohm for CMD/ADDR, 80 Ohm for CTRL/CKE, 38 Ohm for CLK





BOM_COST_GROUP=DRAM

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE

LPDDR3 DRAM Termination

Apple Inc.

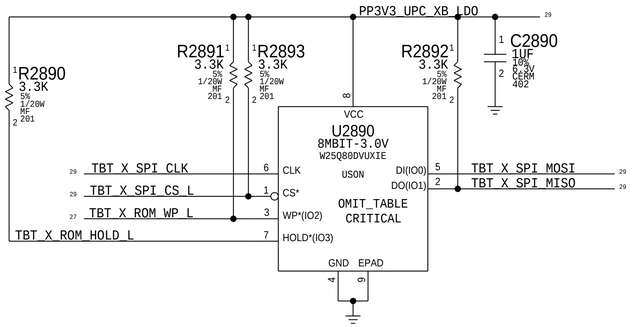
DRAWING NUMBER 051-00789 SIZE D

REVISION PROTO1A

BRANCH dvt-fab10

PAGE 27 OF 145

SHEET 26 OF 121



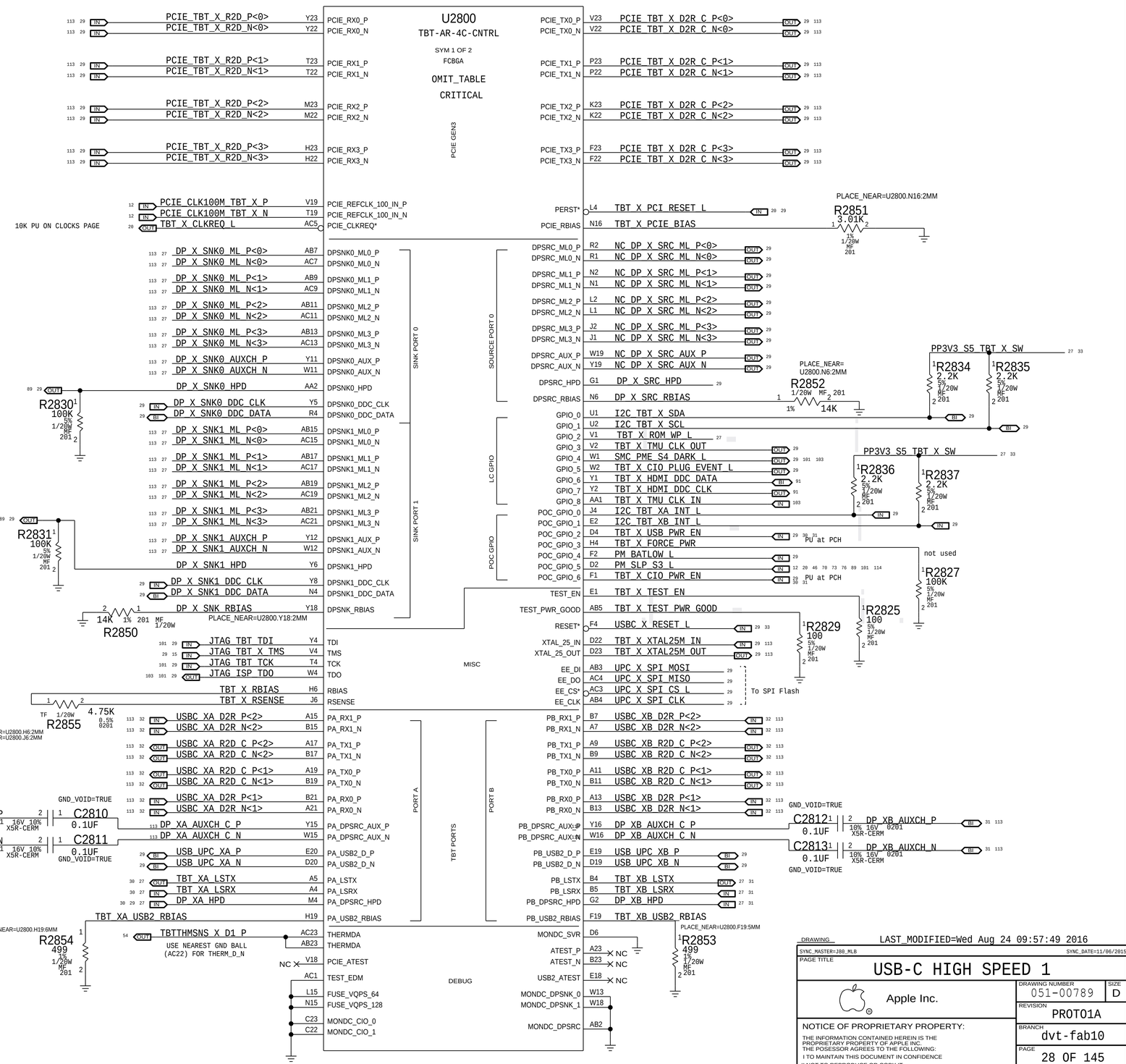
SNK0 AC Coupling

DP_X_SNK0_ML_C_P<0>	C2820	0.1UF	DP_X_SNK0_ML_P<0>	GND_VOID=TRUE
DP_X_SNK0_ML_C_N<0>	C2821	0.1UF	DP_X_SNK0_ML_N<0>	GND_VOID=TRUE
DP_X_SNK0_ML_C_P<1>	C2822	0.1UF	DP_X_SNK0_ML_P<1>	GND_VOID=TRUE
DP_X_SNK0_ML_C_N<1>	C2823	0.1UF	DP_X_SNK0_ML_N<1>	GND_VOID=TRUE
DP_X_SNK0_ML_C_P<2>	C2824	0.1UF	DP_X_SNK0_ML_P<2>	GND_VOID=TRUE
DP_X_SNK0_ML_C_N<2>	C2825	0.1UF	DP_X_SNK0_ML_N<2>	GND_VOID=TRUE
DP_X_SNK0_ML_C_P<3>	C2826	0.1UF	DP_X_SNK0_ML_P<3>	GND_VOID=TRUE
DP_X_SNK0_ML_C_N<3>	C2827	0.1UF	DP_X_SNK0_ML_N<3>	GND_VOID=TRUE
DP_X_SNK0_AUXCH_C_P	C2828	0.1UF	DP_X_SNK0_AUXCH_P	GND_VOID=TRUE
DP_X_SNK0_AUXCH_C_N	C2829	0.1UF	DP_X_SNK0_AUXCH_N	

SNK1 AC Coupling

DP_X_SNK1_ML_C_P<0>	C2830	0.1UF	DP_X_SNK1_ML_P<0>	GND_VOID=TRUE
DP_X_SNK1_ML_C_N<0>	C2831	0.1UF	DP_X_SNK1_ML_N<0>	GND_VOID=TRUE
DP_X_SNK1_ML_C_P<1>	C2832	0.1UF	DP_X_SNK1_ML_P<1>	GND_VOID=TRUE
DP_X_SNK1_ML_C_N<1>	C2833	0.1UF	DP_X_SNK1_ML_N<1>	GND_VOID=TRUE
DP_X_SNK1_ML_C_P<2>	C2834	0.1UF	DP_X_SNK1_ML_P<2>	GND_VOID=TRUE
DP_X_SNK1_ML_C_N<2>	C2835	0.1UF	DP_X_SNK1_ML_N<2>	GND_VOID=TRUE
DP_X_SNK1_ML_C_P<3>	C2836	0.1UF	DP_X_SNK1_ML_P<3>	GND_VOID=TRUE
DP_X_SNK1_ML_C_N<3>	C2837	0.1UF	DP_X_SNK1_ML_N<3>	GND_VOID=TRUE
DP_X_SNK1_AUXCH_C_P	C2838	0.1UF	DP_X_SNK1_AUXCH_P	GND_VOID=TRUE
DP_X_SNK1_AUXCH_C_N	C2839	0.1UF	DP_X_SNK1_AUXCH_N	

100K	R2862	DP_XA_HPD
100K	R2872	DP_XB_HPD
1M	R2860	TBT_XA_LSTX
1M	R2861	TBT_XA_LSRX
1M	R2870	TBT_XB_LSTX
1M	R2871	TBT_XB_LSRX



DRAWING LAST_MODIFIED=Wed Aug 24 09:57:49 2016

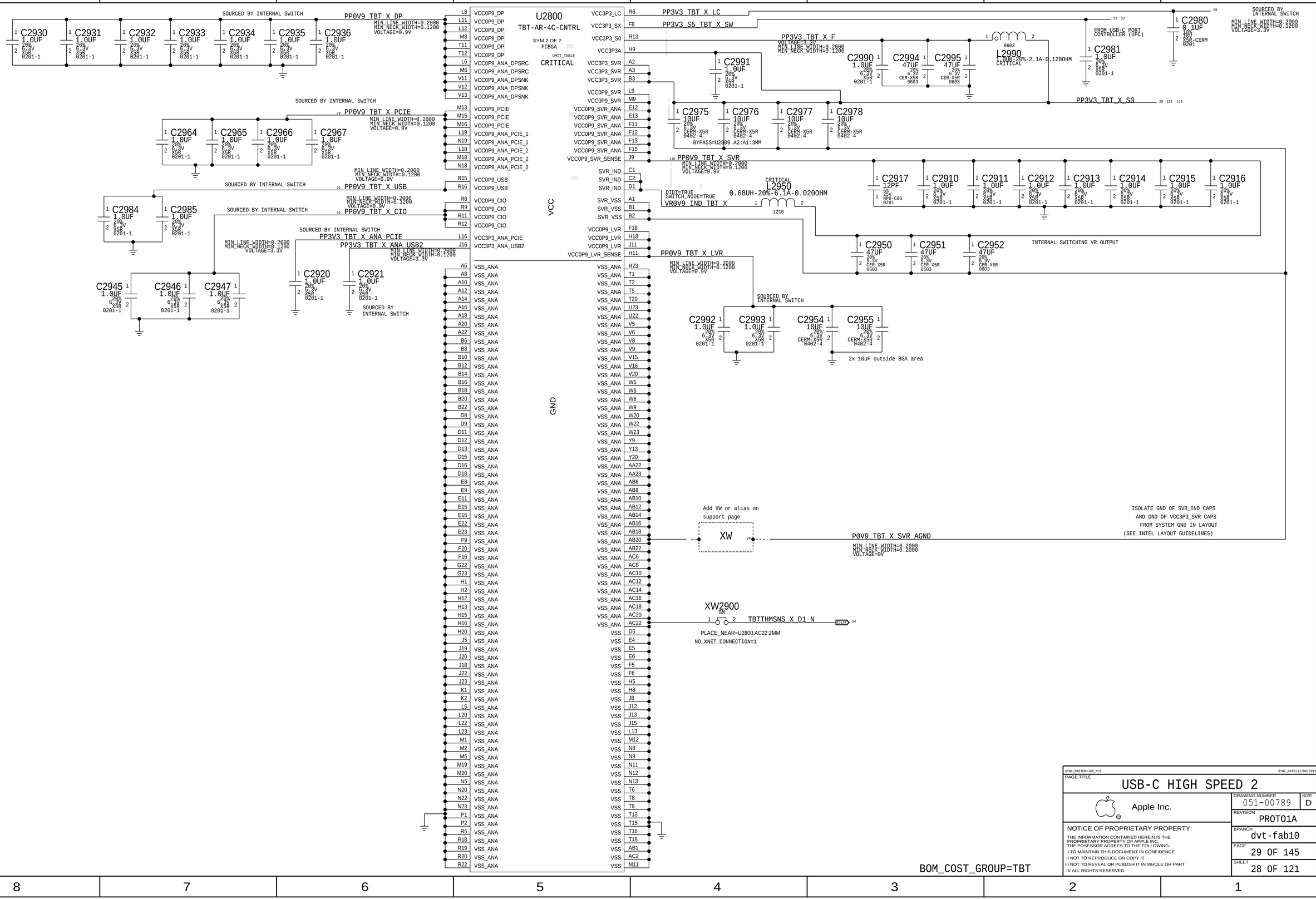
SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE

USB-C HIGH SPEED 1

Apple Inc.

DRAWING NUMBER	051-00789
SIZE	D
REVISION	PROTO1A
BRANCH	dvt-fab10
PAGE	28 OF 145
SHEET	27 OF 121



SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE: USB-C HIGH SPEED 2

Apple Inc.

DRAWING NUMBER: 051-00789 SIZE: D

REVISION: PROTO1A

BRANCH: dvt-fab10

PAGE: 29 OF 145

SHEET: 28 OF 121

TMU CLKs

TBT_X_TMU_CLK_OUT → R3025 15 5% 1/20W MF 201 (PLACE_NEAR=U2800.V2:5mm) → TBT_T_TMU_CLK_IN (MAKE_BASE=TRUE)
TBT_X_TMU_CLK_OUT (MAKE_BASE=TRUE)
R3026 100K 5% 1/20W MF 201

USBC 5V EN PD

UPC_X_5V_EN → R3032 100K 5% 1/20W MF 201

ACE/SMC I2C PU

PP3V3_G3H
R3038 10K 5% 1/20W MF 201 → SMC_USBC_INT_L

DP SRC OPTIONS

IF DP SRC NOT USED

DP_X_SRC_HPD → R3040 1M 5% 1/20W MF 201

NC_DP_X_SRC_ML_P<3..0> — NC_DP_X_SRC_ML_P<3..0> (MAKE_BASE=TRUE, NO_TEST=1)
NC_DP_X_SRC_ML_N<3..0> — NC_DP_X_SRC_ML_N<3..0> (MAKE_BASE=TRUE, NO_TEST=1)
NC_DP_X_SRC_AUX_P — NC_DP_X_SRC_AUX_P (MAKE_BASE=TRUE)
NC_DP_X_SRC_AUX_N — NC_DP_X_SRC_AUX_N (MAKE_BASE=TRUE)

FUSES FOR UPC

PLACE_NEAR=Q3100:5MM
F3000 CRITICAL 0603 6AMP-32V-0.00950HM
PP20V_USBC_XA_VBUS → PP20V_USBC_XA_VBUS_F
PLACE_NEAR=Q3200:5MM
F3001 CRITICAL 0603 740S0135 6AMP-32V-0.00950HM
PP20V_USBC_XB_VBUS → PP20V_USBC_XB_VBUS_F

25MHz xtal

TBT_X_XTAL25M_OUT → R3007 0 5% 1/20W MF 201 → TBT_X_XTAL25M_OUT_R
NOSTUFF R3006 1M 5% 1/20W MF 201
CRITICAL Y3000 25MHZ-25PPM-20PF-500HM 2.00X1.60-SM
C3002 20PF 5% 25V C0G 0201
C3003 20PF 5% 25V C0G 0201
TBT_X_XTAL25M_IN
to/from Ridge

AR/ACE SPI BUS SERIES R'S

ROM: TBT_X_SPI_CLK, TBT_X_SPI_CS_L, TBT_X_SPI_MOSI, TBT_X_SPI_MISO
R3094 100 TBT_X_SPI_CLK_DBG
R3095 15 UPC_XB_SPI_CLK
R3096 15 UPC_XB_SPI_CS_L
R3097 15 UPC_XB_SPI_MOSI
R3098 15 UPC_XB_SPI_MISO
R3090 15 UPC_X_SPI_CLK
R3091 15 UPC_X_SPI_CS_L
R3092 15 UPC_X_SPI_MOSI
R3093 15 UPC_X_SPI_MISO
Ace / AR

USBC DEBUG CONN

TBT_X_SPI_CLK_DBG
I2C_TBT_XB_INT_L
I2C_TBT_XA_INT_L
I2C_TBT_X_SCL2
I2C_TBT_X_SDA
I2C_UPC_X_SDA2
I2C_TBT_X_SCL
SMC_USBC_INT_L
I2C_UPC_XA_DBG_CTL_SDA
TBT_X_SPI_CLK_DBG
I2C_UPC_XA_DBG_CTL_SCL
UPC_XA_UART_TX
UPC_XA_UART_RX

RIDGE JTAG ISOLATION

PLACE_NEAR=U1100.AJ29:10mm
JTAG_TBT_TCK → R3043 0 → JTAG_ISP_TCK
JTAG_TBT_TDI → R3044 0 → JTAG_ISP_TDI
PLACE_NEAR=U1100.AK28:10mm

TP_UPC_XA_SWD_DATA → TP3001
TP_UPC_XA_SWD_CLK → TP3002
TP_UPC_XB_SWD_DATA → TP3003
TP_UPC_XB_SWD_CLK → TP3004
(TP-P5)

POWER ALIASES

PP3V3_UPC_XB_LDO	PP3V3_UPC_XB_LDO	MAKE_BASE=TRUE
PP3V3_UPC_XB_LDO		
PP3V3_UPC_XA_LDO	PP3V3_UPC_XA_LDO	MAKE_BASE=TRUE
PP3V3_UPC_XA_LDO		
PP20V_USBC_XA_VBUS	PP20V_USBC_XA_VBUS	MAKE_BASE=TRUE
PP20V_USBC_XB_VBUS	PP20V_USBC_XB_VBUS	MAKE_BASE=TRUE
PPDCIN_G3H	PPDCIN_G3H	MAKE_BASE=TRUE (MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=20V)
PP5V_S4_X_USBC	PP5V_S4_X_USBC	MAKE_BASE=TRUE (MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=5V)
PP5V_S4_X_USBC		
PP5V_S4_X_USBC		
PP3V3_TBT_X_S0	PP3V3_TBT_X_S0	MAKE_BASE=TRUE (MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=3.3V)

OMIT

R3089 ACE Debug Support

NOSTUFF R3089 UPC_XA_DBG_UART_TX
UPC_XA_DBG_UART_RX
NOSTUFF R3088 OMIT TP_UPC_XB_DBG_UART_TX
TP_UPC_XB_DBG_UART_RX

Ridge PDs

DP_X_SNK0_DDC_CLK → R3067 100K → DP_X_SNK0_DDC_CLK (MAKE_BASE=TRUE)
DP_X_SNK0_DDC_DATA → R3068 100K → DP_X_SNK0_DDC_DATA (MAKE_BASE=TRUE)
DP_X_SNK1_DDC_CLK → R3069 100K → DP_X_SNK1_DDC_CLK (MAKE_BASE=TRUE)
DP_X_SNK1_DDC_DATA → R3070 100K → DP_X_SNK1_DDC_DATA (MAKE_BASE=TRUE)
5% 1/20W MF 201

ACE DEBUG CONN

Place on bottom
USBC_DBG J3000 505070-1220 M-ST-SM

I2C_TBT_XB_INT_L	1	2	I2C_TBT_XA_INT_L
I2C_TBT_X_SCL2	3	4	I2C_TBT_X_SDA
I2C_UPC_X_SDA2	5	6	I2C_TBT_X_SCL
SMC_USBC_INT_L	7	8	I2C_UPC_XA_DBG_CTL_SDA
TBT_X_SPI_CLK_DBG	9	10	I2C_UPC_XA_DBG_CTL_SCL
UPC_XA_UART_TX	11	12	UPC_XA_UART_RX
	15	16	

ACE A RPD STRAPPING

USBC_XA_CC1 — USBC_XA_CC1 (MAKE_BASE=TRUE)
USBC_XA_CC2 — USBC_XA_CC2 (MAKE_BASE=TRUE)

NC ALIASES / NO TEST

NC_UPC_XB_I2C_ADDR

GND ALIASES

GND (MAKE_BASE=TRUE)

RIDGE DEBUG CONN

Place on bottom
USBC_DBG J3001 505070-1220 M-ST-SM

TBT_X_CIO_PLUG_EVENT_L	1	2	TBT_X_PCI_RESET_L
DP_X_SNK0_HPD	3	4	USBC_X_RESET_L
DP_X_SNK1_HPD	5	6	PP3V3_S5_TBT_X_SW
DP_XA_HPD	7	8	PP0V9_TBT_X_PCIE
TBT_POC_RESET	9	10	PP0V9_TBT_X_USB
PP3V3_TBT_X_LC	11	12	PP0V9_TBT_X_CIO
	15	16	

ACE B RPD STRAPPING

USBC_XB_CC1 — USBC_XB_CC1 (MAKE_BASE=TRUE)
USBC_XB_CC2 — USBC_XB_CC2 (MAKE_BASE=TRUE)

ACE PDs

UPC_XA_HPD_RX → R3033 100K (NO STUFF)
UPC_XB_HPD_RX → R3034 100K
UPC_XA_HPD_RX → R3035 0 → SMC_RESET_L
UPC_XB_HPD_RX → R3036 0 → SMC_RESET_L
5% 1/20W MF 201

USB_UPC_XA_P → R3081 0 (NOSTUFF) → R3084 0 → USB_UPC_XB_P (NOSTUFF)
USB_UPC_XA_N → R3082 0 (NOSTUFF) → R3085 0 → USB_UPC_XB_N (NOSTUFF)
5% 1/20W MF 0201

SIGNAL ALIASES

UPC_X_5V_EN	UPC_X_5V_EN	MAKE_BASE=TRUE
UPC_X_5V_EN		
USB2_UPC_XB_P	USB_UPC_PCH_XB_P	MAKE_BASE=TRUE (R3086 0)
USB2_UPC_XB_N	USB_UPC_PCH_XB_N	MAKE_BASE=TRUE (R3087 0)
TBT_X_CIO_PWR_EN	TBT_X_CIO_PWR_EN	MAKE_BASE=TRUE
TBT_X_USB_PWR_EN	TBT_X_USB_PWR_EN	MAKE_BASE=TRUE
PM_BATLOW_L	PM_BATLOW_L	MAKE_BASE=TRUE
SMC_PME_S4_DARK_L	SMC_PME_S4_DARK_L	MAKE_BASE=TRUE
SMC_PME_S4_DARK_L		

UPC_X_SPI_CLK	UPC_X_SPI_CLK	MAKE_BASE=TRUE
UPC_X_SPI_CS_L	UPC_X_SPI_CS_L	MAKE_BASE=TRUE
UPC_X_SPI_MOSI	UPC_X_SPI_MOSI	MAKE_BASE=TRUE
UPC_X_SPI_MISO	UPC_X_SPI_MISO	MAKE_BASE=TRUE
UPC_T_SPI_CLK	UPC_T_SPI_CLK	MAKE_BASE=TRUE
UPC_T_SPI_CS_L	UPC_T_SPI_CS_L	MAKE_BASE=TRUE
UPC_T_SPI_MOSI	UPC_T_SPI_MOSI	MAKE_BASE=TRUE
UPC_T_SPI_MISO	UPC_T_SPI_MISO	MAKE_BASE=TRUE
JTAG_ISP_TDO	JTAG_ISP_TDO	MAKE_BASE=TRUE
SMC_USBC_INT_L	SMC_USBC_INT_L	MAKE_BASE=TRUE
SMC_USBC_INT_L		
TBT_POC_RESET	TBT_POC_RESET	MAKE_BASE=TRUE
TBT_X_CIO_PLUG_EVENT_L	TBT_X_CIO_PLUG_EVENT_L	

UPC_XA_FAULT_L → R3078 0 → XDP_PCH_OBSDATA_C0
UPC_XB_FAULT_L → R3079 0 → XDP_PCH_OBSDATA_C1
5% 1/20W MF 0201

JTAG_TBT_X_TMS	JTAG_TBT_X_TMS	MAKE_BASE=TRUE
JTAG_TBT_T_TMS	JTAG_TBT_T_TMS	MAKE_BASE=TRUE
PP3V3_S4	PP3V3_S4	MAKE_BASE=TRUE
PP3V3_S4		

SMC MOJO

SMC_DEBUGPRT_TX_L — SMC_DEBUGPRT_TX_L (MAKE_BASE=TRUE)
SMC_DEBUGPRT_RX_L — SMC_DEBUGPRT_RX_L (MAKE_BASE=TRUE)

TP_USBC_XA_RESET_L — TP_USBC_XA_RESET_L (MAKE_BASE=TRUE)

DCI PCH USB3

USB3_EXTA_D2R_P	USB3_EXTA_D2R_P	MAKE_BASE=TRUE
USB3_EXTA_D2R_N	USB3_EXTA_D2R_N	MAKE_BASE=TRUE

USB3_EXTA_R2D_C_P → C3020 0.1UF 10% 16V X5R-CERM 0201 → USB3_EXTA_R2D_P (MAKE_BASE=TRUE)
USB3_EXTA_R2D_C_N → C3021 0.1UF 10% 16V X5R-CERM 0201 → USB3_EXTA_R2D_N (MAKE_BASE=TRUE)

USB2_UPC_XA_P → R3076 0 → USB_UPC_PCH_XA_P (MAKE_BASE=TRUE)
USB2_UPC_XA_N → R3077 0 → USB_UPC_PCH_XA_N (MAKE_BASE=TRUE)
5% 1/20W MF 0201

BOM_COST_GROUP=TBT

I2C SERIES R'S

PLACE_NEAR=U5000:5mm
I2C_UPC_X_SDA2 → R3041 33 → SMBUS_SMC_4_G3H_SDA
I2C_UPC_X_SCL2 → R3042 33 → SMBUS_SMC_4_G3H_SCL
5% 1/20W MF 201

RIDGE 0.9V SVR XW

P0V9_TBT_X_SVR_AGND → XW3000 SM
NO_XNET_CONNECTION=1

TBT to ACE

TBT
Alpine Ridge U2800
(MASTER)

I2C_TBT_X_SCL	I2C_TBT_X_SCL
I2C_TBT_X_SDA	I2C_TBT_X_SDA
I2C_TBT_XA_INT_L	I2C_TBT_XA_INT_L
I2C_TBT_XB_INT_L	I2C_TBT_XB_INT_L

Pri ACE
U3100
(Write: 0x70 Read: 0x71)

Sec ACE
U3200
(Write: 0x7E Read: 0x7F)

Ridge PCIE Caps

PCIE_TBT_X_R2D_C_P<0>	C3040 0.22UF	PCIE_TBT_X_R2D_P<0>
PCIE_TBT_X_R2D_C_N<0>	C3041 0.22UF	PCIE_TBT_X_R2D_N<0>
PCIE_TBT_X_R2D_C_P<1>	C3042 0.22UF	PCIE_TBT_X_R2D_P<1>
PCIE_TBT_X_R2D_C_N<1>	C3043 0.22UF	PCIE_TBT_X_R2D_N<1>
PCIE_TBT_X_R2D_C_P<2>	C3044 0.22UF	PCIE_TBT_X_R2D_P<2>
PCIE_TBT_X_R2D_C_N<2>	C3045 0.22UF	PCIE_TBT_X_R2D_N<2>
PCIE_TBT_X_R2D_C_P<3>	C3046 0.22UF	PCIE_TBT_X_R2D_P<3>
PCIE_TBT_X_R2D_C_N<3>	C3047 0.22UF	PCIE_TBT_X_R2D_N<3>
PCIE_TBT_X_D2R_C_P<0>	C3050 0.22UF	PCIE_TBT_X_D2R_P<0>
PCIE_TBT_X_D2R_C_N<0>	C3051 0.22UF	PCIE_TBT_X_D2R_N<0>
PCIE_TBT_X_D2R_C_P<1>	C3052 0.22UF	PCIE_TBT_X_D2R_P<1>
PCIE_TBT_X_D2R_C_N<1>	C3053 0.22UF	PCIE_TBT_X_D2R_N<1>
PCIE_TBT_X_D2R_C_P<2>	C3054 0.22UF	PCIE_TBT_X_D2R_P<2>
PCIE_TBT_X_D2R_C_N<2>	C3055 0.22UF	PCIE_TBT_X_D2R_N<2>
PCIE_TBT_X_D2R_C_P<3>	C3056 0.22UF	PCIE_TBT_X_D2R_P<3>
PCIE_TBT_X_D2R_C_N<3>	C3057 0.22UF	PCIE_TBT_X_D2R_N<3>

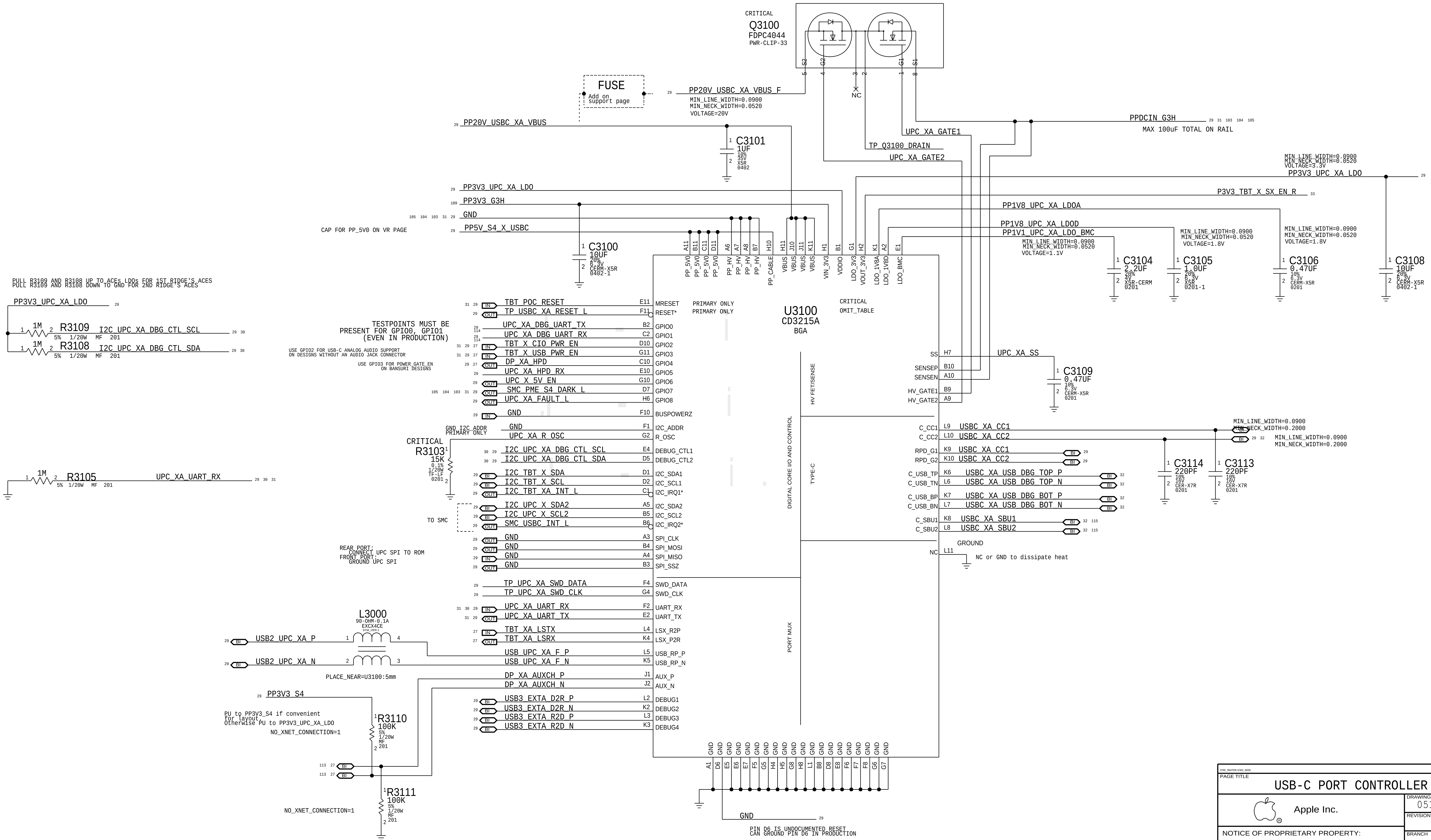
0201 X5R 6.3V 20%
GND_VOID=TRUE

PAGE TITLE: USB-C Support

Apple Inc.

DRAWING NUMBER: 051-00789
SIZE: D
REVISION: PROTO1A
BRANCH: dvt-fab10
PAGE: 30 OF 145
SHEET: 29 OF 121

PRIMARY ACE USB-C PORT CONTROLLER (UPC)



CRITICAL
Q3100
FDPC4044
PWR-CLIP-33
NC
FUSE
Add on support page
PP20V_USBC_XA_VBUS_F
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=20V
PP20V_USBC_XA_VBUS
PPDCIN_G3H
MAX 100uF TOTAL ON RAIL
UPC_XA_GATE1
TP_Q3100_DRAIN
UPC_XA_GATE2
C3101
1UF
10%
35V
X5R
0402
PP3V3_UPC_XA_LDO
PP3V3_G3H
GND
PP5V_S4_X_USBC
CAP FOR PP_5V0 ON VR PAGE
C3100
10UF
20%
6.3V
CERM-X5R
0402-1
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.3V
P3V3_TBT_X_SX_EN_R
PP1V8_UPC_XA_LDOA
PP1V8_UPC_XA_LDOD
PP1V1_UPC_XA_LDO_BMC
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=1.8V
VOLTAGE=1.1V
C3104
2.2UF
20%
4V
X5R-CERM
0201
C3105
1.0UF
20%
6.3V
X5R
0201-1
C3106
0.47UF
10%
6.3V
CERM-X5R
0201
C3108
10UF
20%
6.3V
CERM-X5R
0402-1
PULL R3109 AND R3108 UP TO ACEs LDOs FOR 1ST RIDGE'S ACES
PULL R3109 AND R3108 DOWN TO GND FOR 2ND RIDGE'S ACES
PP3V3_UPC_XA_LDO
R3109
1M
5% 1/20W MF 201
I2C_UPC_XA_DBG_CTL_SCL
R3108
1M
5% 1/20W MF 201
I2C_UPC_XA_DBG_CTL_SDA
TESTPOINTS MUST BE PRESENT FOR GPIO0, GPIO1 (EVEN IN PRODUCTION)
USE GPIO2 FOR USB-C ANALOG AUDIO SUPPORT ON DESIGNS WITHOUT AN AUDIO JACK CONNECTOR
USE GPIO3 FOR POWER_GATE_EN ON BANSURI DESIGNS
U3100
CD3215A
BGA
PRIMARY ONLY
PRIMARY ONLY
CRITICAL
OMIT_TABLE
TBT_POC_RESET
TP_USBC_XA_RESET_L
UPC_XA_DBG_UART_TX
UPC_XA_DBG_UART_RX
TBT_X_CIO_PWR_EN
TBT_X_USB_PWR_EN
DP_XA_HPD
UPC_XA_HPD_RX
UPC_X_5V_EN
SMC_PME_S4_DARK_L
UPC_XA_FAULT_L
GND
GND I2C_ADDR
PRIMARY ONLY
GND
UPC_XA_R_OSC
CRITICAL
R3103
15K
0.1%
1/20W
TF-LF
0201
I2C_UPC_XA_DBG_CTL_SCL
I2C_UPC_XA_DBG_CTL_SDA
I2C_TBT_X_SDA
I2C_TBT_X_SCL
I2C_TBT_XA_INT_L
I2C_UPC_X_SDA2
I2C_UPC_X_SCL2
SMC_USBC_INT_L
TO SMC
REAR PORT: CONNECT UPC SPI TO ROM
FRONT PORT: GROUND UPC SPI
TP_UPC_XA_SWD_DATA
TP_UPC_XA_SWD_CLK
UPC_XA_UART_RX
UPC_XA_UART_TX
TBT_XA_LSTX
TBT_XA_LSRX
USB_UPC_XA_F_P
USB_UPC_XA_F_N
DP_XA_AUXCH_P
DP_XA_AUXCH_N
USB3_EXTA_D2R_P
USB3_EXTA_D2R_N
USB3_EXTA_R2D_P
USB3_EXTA_R2D_N
R3105
1M
5% 1/20W MF 201
UPC_XA_UART_RX
L3000
90-OHM-0.1A
EXCX4CE
USB2_UPC_XA_P
USB2_UPC_XA_N
PLACE_NEAR=U3100:5mm
PP3V3_S4
PU to PP3V3_S4 if convenient for layout. Otherwise PU to PP3V3_UPC_XA_LDO
NO_XNET_CONNECTION=1
R3110
100K
5%
1/20W
MF
201
R3111
100K
5%
1/20W
MF
201
NO_XNET_CONNECTION=1
MRESET
RESET*
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
BUSPOWERZ
I2C_ADDR
R_OSC
DEBUG_CTL1
DEBUG_CTL2
I2C_SDA1
I2C_SCL1
I2C_IRQ1*
I2C_SDA2
I2C_SCL2
I2C_IRQ2*
SPI_CLK
SPI_MOSI
SPI_MISO
SPI_SSZ
SWD_DATA
SWD_CLK
UART_RX
UART_TX
LSX_R2P
LSX_P2R
USB_RP_P
USB_RP_N
AUX_P
AUX_N
DEBUG1
DEBUG2
DEBUG3
DEBUG4
HV FET/SENSE
DIGITAL CORE I/O AND CONTROL
TYPE-C
PORT MUX
PP_5V0
PP_HV
PP_CABLE
VBUS
VIN_3V3
VDDIO
LDO_3V3
VOUT_3V3
LDO_1V8A
LDO_1V8D
LDO_BMC
SS
SENSEP
SENSEN
HV_GATE1
HV_GATE2
C_CC1
C_CC2
RPD_G1
RPD_G2
C_USB_TP
C_USB_TN
C_USB_BP
C_USB_BN
C_SBU1
C_SBU2
NC
UPC_XA_SS
C3109
0.47UF
10%
6.3V
CERM-X5R
0201
USBC_XA_CC1
USBC_XA_CC2
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.2000
USBC_XA_CC1
USBC_XA_CC2
USBC_XA_USB_DBG_TOP_P
USBC_XA_USB_DBG_TOP_N
USBC_XA_USB_DBG_BOT_P
USBC_XA_USB_DBG_BOT_N
USBC_XA_SBU1
USBC_XA_SBU2
C3114
220PF
10%
16V
CER-X7R
0201
C3113
220PF
10%
16V
CER-X7R
0201
GROUND
NC or GND to dissipate heat
GND
PIN D6 IS UNDOCUMENTED RESET
CAN GROUND PIN D6 IN PRODUCTION

BOM_COST_GROUP=USB-C

PAGE TITLE

USB-C PORT CONTROLLER A

Apple Inc.

DRAWING NUMBER 051-00789 SIZE D

REVISION PROTO1A

BRANCH dvt-fab10

SECONDARY ACE USB-C PORT CONTROLLER (UPC)

CRITICAL
Q3200
FDPC4044
PWR-CLIP-33
FUSE
Add on support page
PP20V_USBC_XB_VBUS_F
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=20V
PP20V_USBC_XB_VBUS
C3201
1UF
PPDCIN_G3H
MAX 100uF TOTAL ON RAIL
UPC_XB_GATE1
TP_Q3200_DRAIN
UPC_XB_GATE2
PP3V3_UPC_XB_LDO
P3V3_TBT_X_SX_EN_R
PP1V8_UPC_XB_LDOA
PP1V8_UPC_XB_LDOD
PP1V1_UPC_XB_LDO_BMC
VOUT_3V3 FOR RIDGE, OR FLOAT IF UNUSED
PP3V3_G3H
GND
PP5V_S4_X_USBC
CAP FOR PP_5V0 ON VR PAGE
C3200
10UF
C3205
1.0UF
C3208
10UF
C3204
2.2UF
C3206
0.47UF
U3200
CD3215A
BGA
CRITICAL
OMIT_TABLE
TESTPOINTS MUST BE PRESENT FOR GPIO0, GPIO1 (EVEN IN PRODUCTION)
TBT_POC_RESET
USBC_X_RESET_L_R
TP_UPC_XB_DBG_UART_TX
TP_UPC_XB_DBG_UART_RX
TBT_X_CIO_PWR_EN
TBT_X_USB_PWR_EN
DP_XB_HPD
UPC_XB_HPD_RX
UPC_X_5V_EN
SMC_PME_S4_DARK_L
UPC_XB_FAULT_L
NC_UPC_XB_I2C_ADDR
UPC_XB_R_OSC
I2C_UPC_XB_DBG_CTL_SCL
I2C_UPC_XB_DBG_CTL_SDA
I2C_TBT_X_SDA
I2C_TBT_X_SCL
I2C_TBT_XB_INT_L
I2C_UPC_X_SDA2
I2C_UPC_X_SCL2
SMC_USBC_INT_L
TO SMC
UPC_XB_SPI_CLK
UPC_XB_SPI_MOSI
UPC_XB_SPI_MISO
UPC_XB_SPI_CS_L
REAR PORT: CONNECT UPC SPI TO ROM
FRONT PORT: GROUND UPC SPI
TP_UPC_XB_SWD_DATA
TP_UPC_XB_SWD_CLK
UPC_XA_UART_TX
UPC_XA_UART_RX
TBT_XB_LSTX
TBT_XB_LSRX
USB_UPC_XB_F_P
USB_UPC_XB_F_N
DP_XB_AUXCH_P
DP_XB_AUXCH_N
SOC_SWCLK_DBG
SOC_SWDIO_DBG
SMC_DEBUGPRT_TX_L
SMC_DEBUGPRT_RX_L
PULL R3209 AND R3208 UP TO ACEs LDOs FOR 1ST RIDGE'S ACES
PULL R3209 AND R3208 DOWN TO GND FOR 2ND RIDGE'S ACES
PP3V3_UPC_XB_LDO
R3209
R3208
1M
I2C_UPC_XB_DBG_CTL_SCL
I2C_UPC_XB_DBG_CTL_SDA
CRITICAL
R3203
15K
NEED 0.1%
R3205
UPC_XA_UART_TX
L3200
90-OHM-0.1A
EXCX4CE
USB2_UPC_XB_P
USB2_UPC_XB_N
PLACE_NEAR=U3200.L5:5mm
PLACE_NEAR=U3200.K5:5mm
PP3V3_S4
PU to PP3V3_S4 if convenient for layout.
Otherwise PU to PP3V3_UPC_XA_LDO
NO_XNET_CONNECTION=1
R3210
100K
R3211
100K
UPC_XB_SS
C3209
0.47UF
USBC_XB_CC1
USBC_XB_CC2
C3214
220PF
C3213
220PF
USBC_XB_USB_TOP_P
USBC_XB_USB_TOP_N
USBC_XB_USB_BOT_P
USBC_XB_USB_BOT_N
USBC_XB_SBU1
USBC_XB_SBU2
GROUND
NC or GND to dissipate heat
HV FET/SENSE
DIGITAL CORE I/O AND CONTROL
TYPE-C
PORT MUX
GND
PIN D6 IS UNDOCUMENTED RESET
CAN GROUND PIN D6 IN PRODUCTION

BOM_COST_GROUP=USB-C

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE

USB-C PORT CONTROLLER B

Apple Inc.

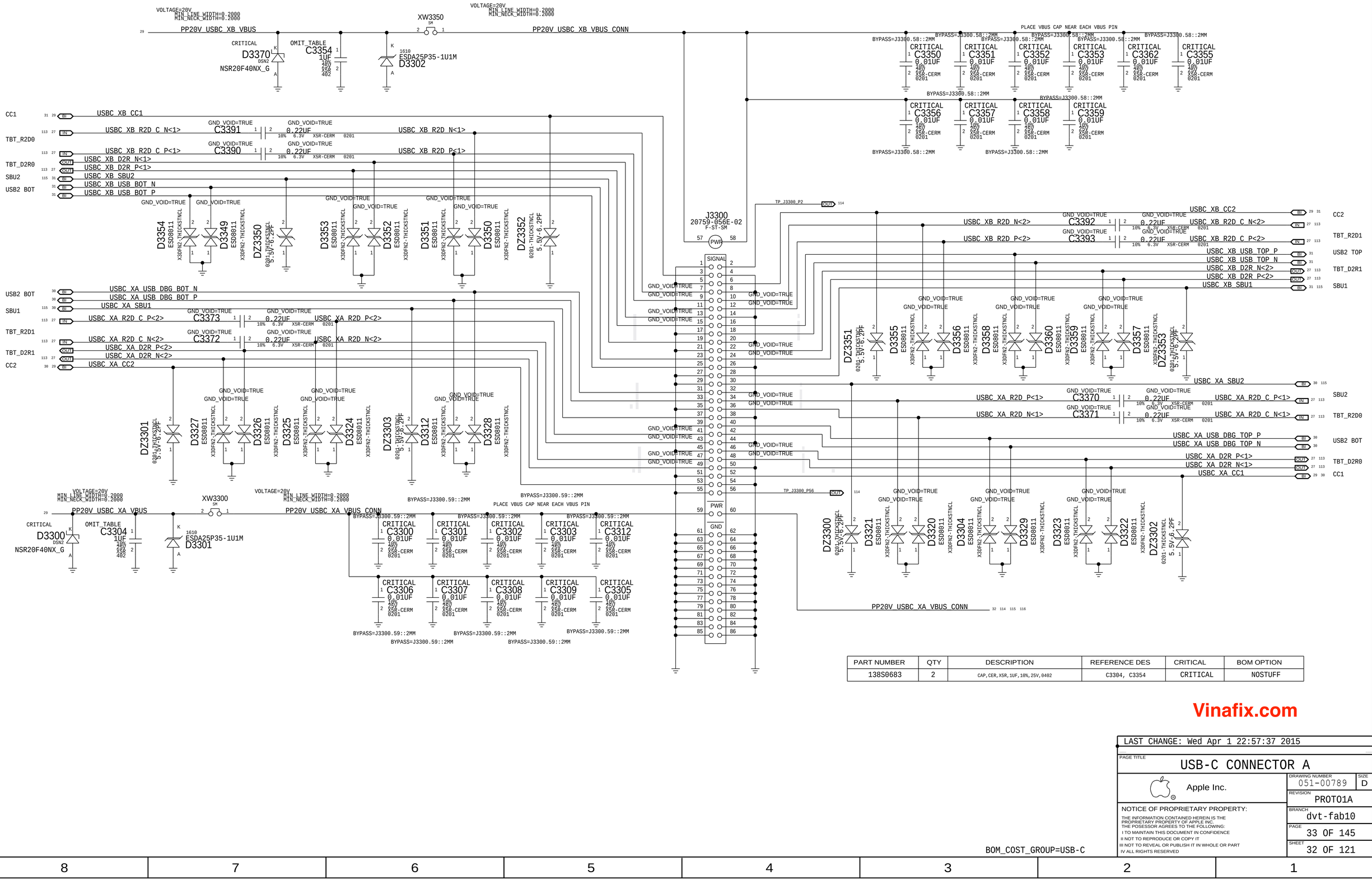
DRAWING NUMBER 051-00789 SIZE D

REVISION PROTO1A

BRANCH dvt-fab10

PAGE 32 OF 145

SHEET 31 OF 121



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0683	2	CAP,CER,X5R,1UF,10%,25V,0402	C3304, C3354	CRITICAL	NOSTUFF

BOM_COST_GROUP=USB-C

LAST CHANGE: Wed Apr 1 22:57:37 2015

PAGE TITLE: USB-C CONNECTOR A

Apple Inc.

DRAWING NUMBER: 051-00789 SIZE: D

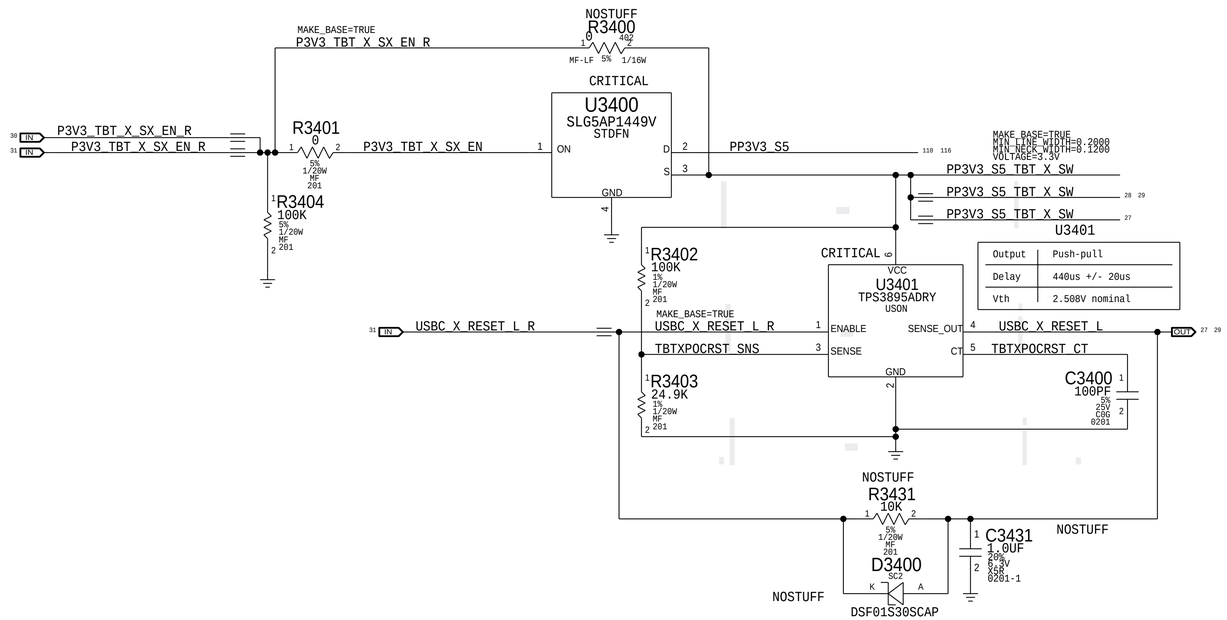
REVISION: PROTO1A

BRANCH: dvt-fab10

PAGE: 33 OF 145

SHEET: 32 OF 121

TBT X "POC" Power-up Reset



BOM_COST_GROUP=USB-C

DESIGN: X502/DEV_MLB_U

LAST CHANGE: Wed Feb 18 17:12:24 2015

SYNC_MASTER=X502_MLB SYNC_DATE=03/29/2016

PAGE TITLE

USB-C CONNECTOR B

Apple Inc.

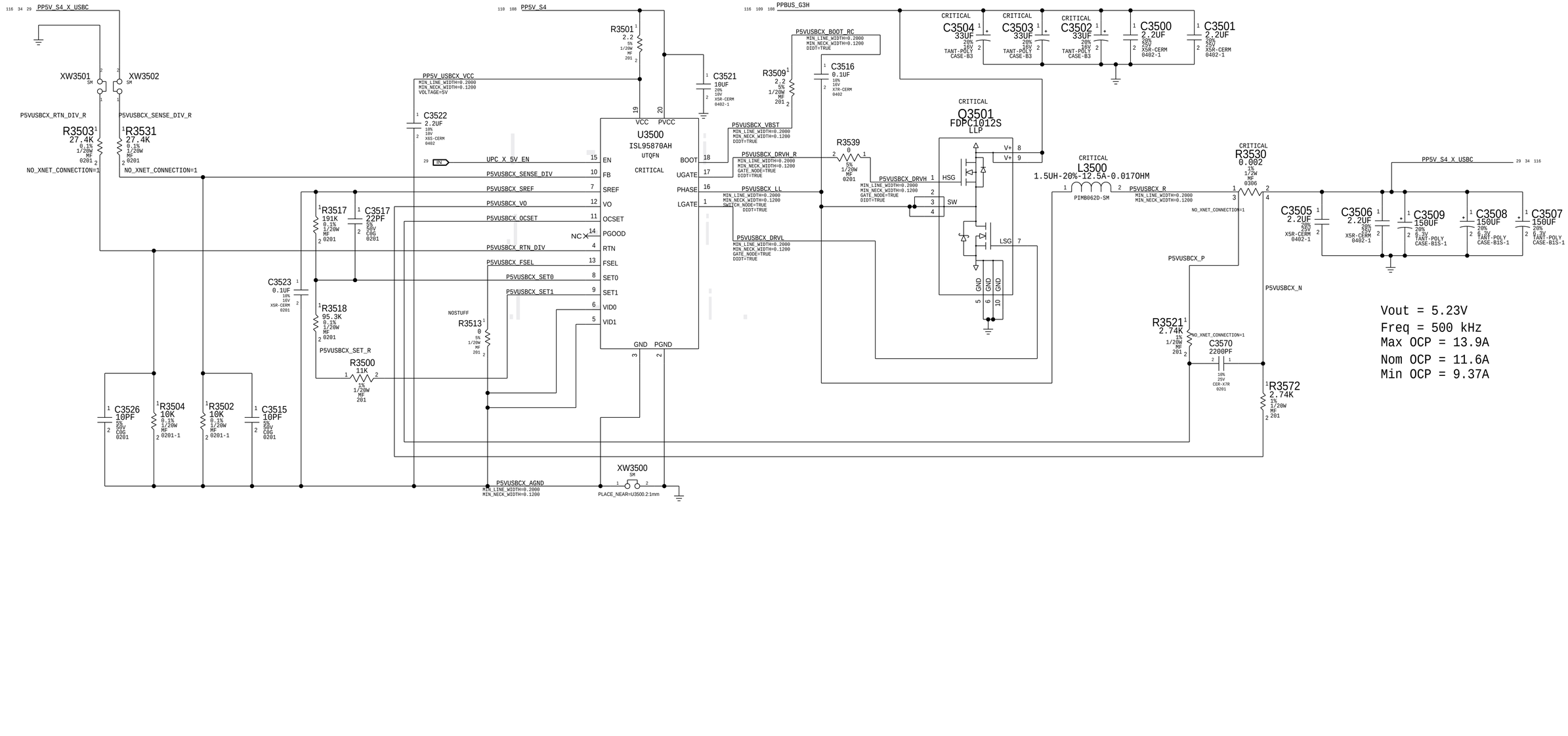
DRAWING NUMBER 051-00789 SIZE D

REVISION PROTO1A

BRANCH dvt-fab10

PAGE 34 OF 145

SHEET 33 OF 121



BOM_COST_GROUP=USB-C

SYNC_MASTER=J80_ZIFENGSHEN_MLB_BAFFIN SYNC_DATE=12/04/2015

PAGE TITLE: TBT 5V REGULATOR

Apple Inc.

DRAWING NUMBER: 051-00789 SIZE: D

REVISION: PROTO1A

BRANCH: dvt-fab10

PAGE: 35 OF 145

SHEET: 34 OF 121


U3730
LBEE5UQ1HG-844
LGA
SYM 2 OF 2
THRM_PAD
PP3V3_S4_BT
PP3V3_S4_WLAN_SW
MAKE_BASE=TRUE
VOLTAGE=3.3V
FOR JTAG MODE REMOVE R3735
NO_XNET_CONNECTION=1
R3735
WLAN_1P2V_EN
C3761
C3740
C3736
C3762
C3763
C3742
C3741
C3737
C3738
FEM SUPPLY SHUNT CAPACITORS
PLACE ON THE TOP SIDE CLOSE TO U3730
C3758
C3757
C3704
C3705
C3702
C3703
C3739
C3701
C3759
C3760
SROM_STRAPS
R3731
R3734
WLAN_STRAP_0
WLAN_STRAP_1
STRAP_0 HI:SROM (Default)
STRAP_1 LO:16kb SROM
U3730
LBEE5UQ1HG-844
LGA
SYM 1 OF 2
R3701
R3759
Q3701
DMN32D2LFB4
PCH_BT_ROM_BOOT
BT_ROM_BOOT_L
BT_TIMESTAMP
R3766
R3767
R3762
R3776
R3777
Q3702
DMN32D2LFB4
SYSCLK_CLK32K_WIFIBT
BT UART TX & RTS ISOLATION CIRCUIT
R3764
C3764
U3760
74LVC2G126
R3765
BT UART RX & CTS ISOLATION CIRCUIT
R3774
C3774
U3770
74LVC2G126
R3775
BLUETOOTH SERIAL FLASH
R3751
R3752
R3753
R3754
U3750
2MBIT
USON
MX25L2006EZUI-12G
C3756
WLAN SERIAL EEPROM
U3710
CAS93C86B
UDFN8
C3711
R3712
DEBUG CONNECTOR
J3701
AA25D-S038VA1
F-ST-SM
BOM_COST_GROUP=WIRELESS

PAGE TITLE

WIFI/BT: MODULE 1

DRAWING NUMBER 051-00789 SIZE D

Apple Inc.

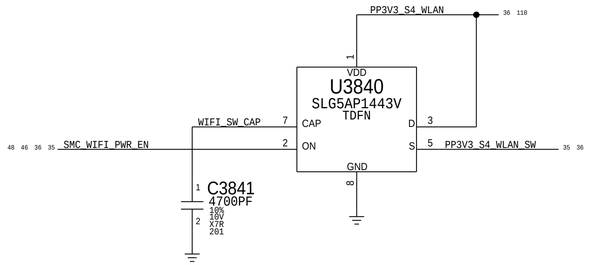
REVISION PROTO1A

BRANCH dvt-fab10

PAGE 37 OF 145

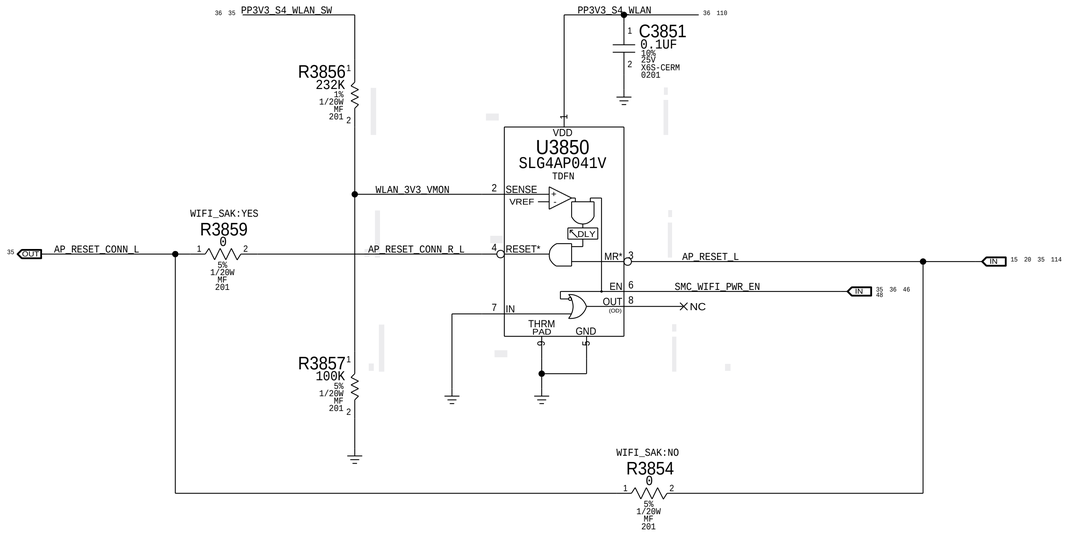
SHEET 35 OF 121

WLAN Power Switch

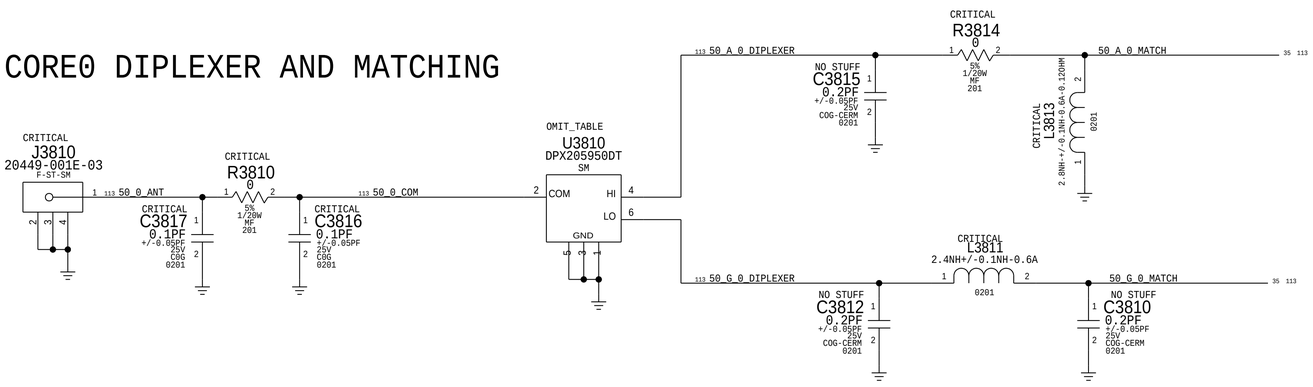


Supervisor & CLKREQ# Isolation

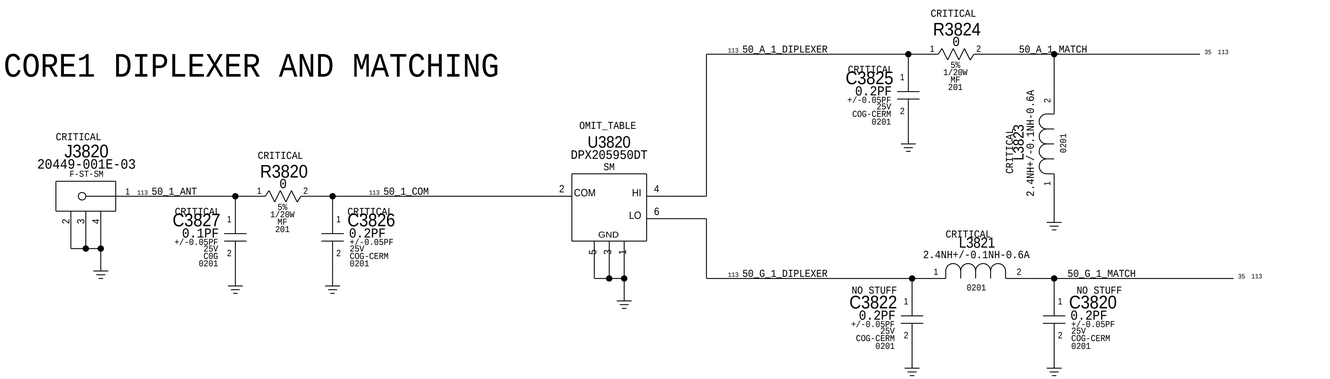
Delay = 130ms +/- 20%



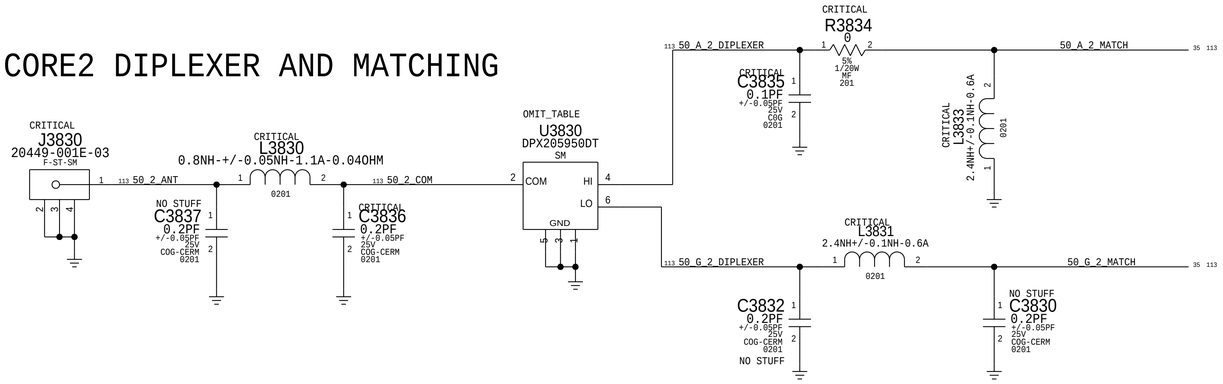
CORE0 DIPLEXER AND MATCHING



CORE1 DIPLEXER AND MATCHING



CORE2 DIPLEXER AND MATCHING



BOM_COST_GROUP=WIRELESS

SYNC_MASTER=J80_MLB	SYNC_DATE=11/06/2015
PAGE TITLE	WIFI/BT: MODULE 2
Apple Inc.	DRAWING NUMBER 051-00789 SIZE D
	REVISION PROTO1A
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	BRANCH dvt-fab10
	PAGE 38 OF 145
	SHEET 36 OF 121

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S00136	1	IC,M8+512MB 20NM DDR,A12,S,SCK,BGA700	U3900	CRITICAL	SOC:HYNIX

T208

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S00147	1	IC,RTM2,DEV,PN549A1,P61D0	U3905	CRITICAL	SE:DEV
338S00097	1	IC,RTM2,MP,PN549A1,P61D0	U3905	CRITICAL	SE:PROD

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00203	1	IC,FLASH,SERIAL,SPI,4MX8,4X3MM,DFN8	U3906		

PAGE TITLE
Camera/DFR 1

Apple Inc.

DRAWING NUMBER 051-00789 SIZE D

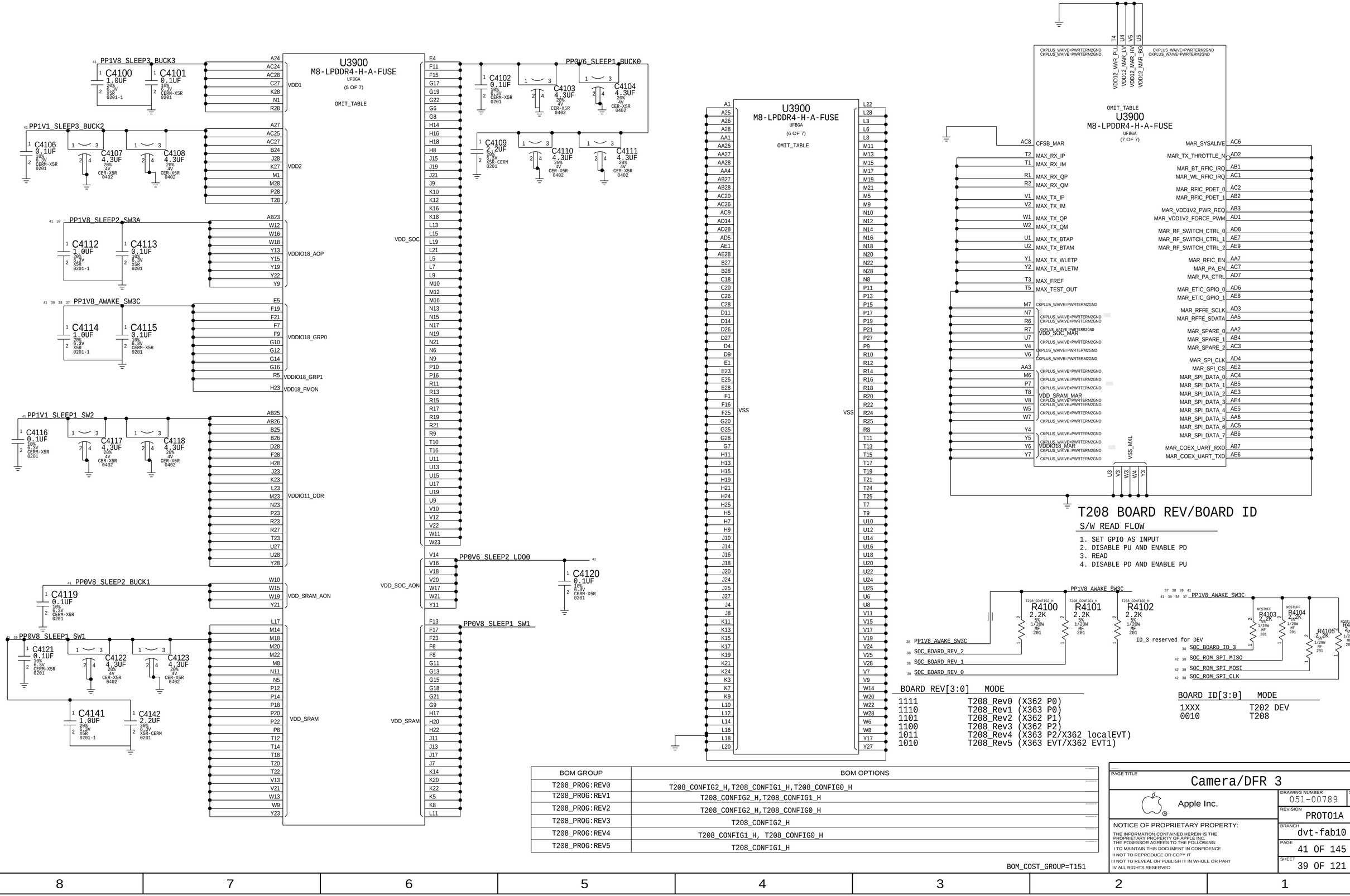
REVISION PROTO1A

BRANCH dvt-fab10

PAGE 39 OF 145

SHEET 37 OF 121

U3900
M8-LPDDR4-H-A-FUSE
UFBGA
(3 OF 7)
OMIT_TABLE
U3900
M8-LPDDR4-H-A-FUSE
UFBGA
(4 OF 7)
OMIT_TABLE
PP1V8_AWAKE_SW3C
PP3V0_AWAKE_LDO7
PP1V1_SLEEP1_SW2
PP0V8_SLEEP1_SW1
PP1V8_S4
PP3V3_S4_SOC_PMU
C4002 0.1UF
C4001 0.1UF
C4000 0.1UF
C4004 0.1UF
C4005 0.1UF
C4003 0.1UF
C4006 1.0UF
C4007 0.1UF
C4008 0.1UF
C4050 0.22UF
L4010 120-OHM-0.2A-0.5-OHM
R4035 47K
R4023 100K
R4017 2.2K
R4022 10K
R4042 10K NOSTUFF
R4001 200
R4003 4.02K
R4004 4.02K
R4036 10K
R4037 10K
R4024 100K
SOC_BOOT:DFU
SOC_BOOT:SPI
SOC_FORCE_DFU
DFU_STATUS
SOC_REQUEST_DFU1
SOC_REQUEST_DFU2
PMU_TO_SOC_VDD_OK
PMU_TO_SOC_AWAKE_PWRGD
TP_SOC_TST_CKOUT
DFR_CLKIN_RESET_L
SOC_BOOT_CONFIG_0
SOC_BOARD_ID_3
SOC_BOARD_REV_0
SOC_BOARD_REV_1
SOC_BOARD_REV_2
DFR_DISP_RST_L
DFR_TOUCH_INT_L
MESA_SNSR_INT
SOC_TO_STOCKHOLM_EN
DFR_DISP_INT
SOC_PMU_I2C_SCL
SOC_PMU_I2C_SDA
DFR_TOUCH_ROM_I2C_SCL
DFR_TOUCH_ROM_I2C_SDA
DFRDRV_I2C_SCL
DFRDRV_I2C_SDA
SOC_ROM_SPI_MISO
SOC_ROM_SPI_MOSI
SOC_ROM_SPI_CLK
SOC_ROM_SPI_CS_L
MESA_SPI_MISO
MESA_SPI_MOSI
MESA_SPI_CLK
SOC_XTAL_24M_I
SOC_XTAL_24M_O
USB_CAMERA_DFR_P
USB_CAMERA_DFR_N
SOC_USB_VBUS
SOC_USB_REXT
PLACE_NEAR=U3900.H4:2mm
To/From PCH for logging/debug
PCH_TO_SOC_UART_TXD
SOC_TO_PCH_UART_TXD
To/From PCH for ALS
PCH_ALS_TO_SOC_UART_TXD
SOC_TO_PCH_ALS_UART_TXD
UART_SOC_TO_STOCKHOLM_RTS_L
UART_STOCKHOLM_TO_SOC_RTS_L
UART_STOCKHOLM_TO_SOC_TXD
UART_SOC_TO_STOCKHOLM_TXD
PLACE_NEAR=U3900.K1:2mm
MIPIC_DATA_P
MIPIC_DATA_N
MIPIC_CLK_P
MIPIC_CLK_N
SOC_MIPI1C_REXT
I2C_CAM_SDA
I2C_CAM_SCL
MIPID_DATA_P
MIPID_DATA_N
MIPID_CLK_P
MIPID_CLK_N
SOC_MIPI0D_REXT
PLACE_NEAR=U3900.K2:3mm
DFR_DISP_VSYNC
DFR_DISP_TE
SOC_NAND_CEN_0
DFR_TOUCH_PANEL_DETECT
DFR_TOUCH_GPIO2
DFR_TOUCH_ROM_WC
SOC_PANIC_L
S2R_ACK_L
SOC_PCH_DBELL_L
SEP_I2C_SCL
SEP_I2C_SDA
MIPIC FILTERING
L4002 3.25-OHM-0.1A-2.4GHZ TAM0605-4SM
L4003 3.25-OHM-0.1A-2.4GHZ TAM0605-4SM
PLACE_NEAR=J8500:2.54mm
GND_VOID=TRUE
MIPI_DATA_CONN_P
MIPI_DATA_CONN_N
MIPI_CLK_CONN_P
MIPI_CLK_CONN_N
L4004 FERR-120-OHM-1.5A
PP5V_S0
PP5V_S0_ALSCAM_F
C4062 0.1UF
R4010 499K
R4020 0.00
Y4000 24.000MHZ-30PPM-9.5PF-60OHM
SOC_XTAL_24M_O_R
C4041 12PF
C4040 12PF
T208 SOC_S2R_ACK_L bi-directional Isolation
PP3V3_S0_LEFT
R4082 10K
R4080 200K NOSTUFF
Q4000 DMN32D2LFB4 DFN1006H4-3
SOC_S2R_ACK_L
Q4000 to act as bi-directional islation for SOC_S2R_ACK_L
When in system S0 and M8 AWAKE, FET will be on & line will be pulled high
Below S0, SOC_S2R_ACK_L will be low and FET will be open (isolated from M8 power rails)
When M8 enters S2R, FET will be on, PP1V8_AWAKE_SW3C will turn off and SOC_S2R_ACK_L will be low
T208 SOC_S2R_ACK_L Isolation (NOSTUFF)
PP1V8_S0
C4080 0.1UF NOSTUFF
U4080 74LVC1G08FW5 DFN1010 NOSTUFF
T208 FORCE_DFU Isolation
SOC_FORCE_DFU should be pulled up to S4
In the SOC_BOOT:DFU option
U4070 prevents it from leaking into PCH
R4070 47K
C4070 0.1UF
U4070 74LVC1G08FW5 DFN1010
PCH_SOC_FORCE_DFU
R4071 0
BOM_COST_GROUP=T151
PAGE TITLE
Camera/DFR 2
DRAWING NUMBER 051-00789
SIZE D
Apple Inc.
REVISION PROTO1A
BRANCH dvt-fab10
PAGE 40 OF 145
SHEET 38 OF 121
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



BOM GROUP	BOM OPTIONS
T208_PROG:REV0	T208_CONFIG2_H,T208_CONFIG1_H,T208_CONFIG0_H
T208_PROG:REV1	T208_CONFIG2_H,T208_CONFIG1_H
T208_PROG:REV2	T208_CONFIG2_H,T208_CONFIG0_H
T208_PROG:REV3	T208_CONFIG2_H
T208_PROG:REV4	T208_CONFIG1_H, T208_CONFIG0_H
T208_PROG:REV5	T208_CONFIG1_H

BOM_COST_GROUP=T151

PAGE TITLE
Camera/DFR 3

Apple Inc.

DRAWING NUMBER 051-00789
SIZE D
REVISION PROTO1A
BRANCH dvt-fab10
PAGE 41 OF 145
SHEET 39 OF 121

Berkelium

FB for Bucks

R4200 0 5% 1/16W MF-LF 402 — SOC_PMU_BUCK0_FB → PP0V6_SLEEP1_BUCK0
R4201 0 5% 1/16W MF-LF 402 — SOC_PMU_BUCK1_FB → PP0V8_SLEEP1_SW1
R4202 0 5% 1/16W MF-LF 402 — SOC_PMU_BUCK2_FB → PP1V1_SLEEP3_BUCK2
R4203 0 5% 1/16W MF-LF 402 — SOC_PMU_BUCK3_FB → PP1V8_SLEEP3_BUCK3

Q4201 CSD58892Q2 SON2X2
SW1_EXT_ON → Q4201.G
Q4201.S → PP0V8_SLEEP1_SW1
Q4201.D → PP0V8_SLEEP2_BUCK1

U4200 D2346A1-OTP-CE WLCSP SYM 1 OF 2

Pin	Net
A7	VDD_MAIN_BUCK0
A8	VDD_MAIN_BUCK1
A2	VDD_MAIN_BUCK2
F12	VDD_MAIN_BUCK3
G12	VDD_MAIN_BUCK4
D1	VDD_MAIN_BB
K11	VDD_MAIN_CHG
L11	VDD_MAIN_CHG
M11	VDD_MAIN_CHG
J1	VDD_MAIN_BBCORE
K3	ACT_DIODE
L2	VDD_MAIN_SW4
K12	VBAT
L12	VBAT
M12	VBAT
K10	VBAT_SENSE
C6	SW0_EXT
D7	SW1_EXT
E1	BB_LX1
G1	BB_LX2
J3	BB_FB
H1	BB_OUT
M4	VDD_HVLDO_237
N2	VDD_HVLDO_45
L8	VDD_HVLDO_RTC
L3	VDD_HVLDO_SW6
M5	LDO2_OUT
N4	LDO3_OUT
M1	LDO4_OUT
N3	LDO5_OUT
N5	LDO7_OUT
M2	SW4_OUT
M10	VDD_MAIN_LDO_16
M6	VDD_MAIN_LDO_8
M9	VDD_MAIN_LDO_9
N7	VDD_MAIN_LDO_AUX
N10	LDO1_OUT
N9	LDO6_OUT
N6	LDO8_OUT
M8	LDO9_OUT
N8	AUX_PWR_OUT
B10	SW1_IN
A11	SW1_OUT
C10	LDO0_OUT
B1	SW2_IN
C1	SW2_OUT
B12	SW3_IN
B11	SW3A_OUT
C11	SW3B_OUT
C12	SW3C_OUT
K1	SW5_IN
L1	SW5_OUT
K2	SW6_OUT
F1	VSS_BB
A5	VSS_BUCK0
A10	VSS_BUCK1
A4	VSS_BUCK2
D12	VSS_BUCK3
J12	VSS_BUCK4
B2, B9, C4, C5, E5, E6, H5, H6, F5, F6, G5, G6, M3, M7, G8, H7, H8, E7, F7, F8, G7, A1, A12, N1, N12	VSS1–VSS9

PP3V3_S4_SOC_PMU
- CRITICAL C4203 15UF 20% 6.3V CERM 0402 — PLACE_NEAR=U4200.K11:2mm
- CRITICAL C4202 15UF 20% 6.3V CERM 0402 — PLACE_NEAR=U4200.D1:2mm
- CRITICAL C4204 15UF 20% 6.3V CERM 0402 — PLACE_NEAR=U4200.A7:2mm
- CRITICAL C4205 15UF 20% 6.3V CERM 0402 — PLACE_NEAR=U4200.A2:2mm
- CRITICAL C4206 15UF 20% 6.3V CERM 0402 — PLACE_NEAR=U4200.F12:2mm
- CRITICAL C4207 15UF 20% 6.3V CERM 0402 — PLACE_NEAR=U4200.E1:3mm
- C4219 2.2UF 20% 6.3V X5R-CERM 0201 — PLACE_NEAR=U4200.M4:2mm
- C4218 2.2UF 20% 6.3V X5R-CERM 0201 — PLACE_NEAR=U4200.L8:2mm

C4220 2.2UF 20% 6.3V X5R-CERM 0201 — PP3V0_AWAKE_LDO7

VOLTAGE=1.8V
- PP1V8_ALWAYS_LDO9
- C4227 0.22UF 20% 10V CERM-X5R 0201
- C4226 0.022UF 10% 6.3V X5R-CERM 0201

VOLTAGE=0.6V
- PP0V6_SLEEP2_LDO0
- C4228 2.2UF 20% 6.3V X5R-CERM 0201

VDD_SOC — 501MA MAX

BUCK0_LX ← L4202 1.0UH-1.82A-0.203OHM MCFK2012-SM ← SOC_PMU_BUCK0_LX
BUCK0_FB ← SOC_PMU_BUCK0_FB
MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.1200 DIDT=TRUE SWITCH_NODE=TRUE
- CRITICAL C4208 15UF 20% 6.3V CERM 0402
- CRITICAL C4209 15UF 20% 6.3V CERM 0402
- C4210 2.2UF 20% 6.3V X5R-CERM 0201
- C4230 2.2UF 20% 6.3V X5R-CERM 0201

PP0V6_SLEEP1_BUCK0
Mirror Capacitors in Layout

VDD_SRAM_AON VDD_SRAM VDD_SOC_AON — VDD_FIXED_MIPI VDD_FIXED_USB — 300MA MAX

BUCK1_LX ← L4203 1.0UH-1.3A-0.326OHM MCFK1608T1R0M NA ← SOC_PMU_BUCK1_LX
BUCK1_FB ← SOC_PMU_BUCK1_FB
MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.1200 DIDT=TRUE SWITCH_NODE=TRUE
- CRITICAL C4211 4.2UF 10% 10V X5R-CERM 0402-1
- CRITICAL C4231 4.2UF 10% 10V X5R-CERM 0402-1
- CRITICAL C4233 4.7UF 20% 6.3V CER-X5R 0402
- CRITICAL C4232 4.7UF 20% 6.3V CER-X5R 0402

PP0V8_SLEEP2_BUCK1
Mirror Capacitors in Layout

VDD2 VDDQ VDD11_XTAL — 460MA MAX

BUCK2_LX ← L4204 1.0UH-1.3A-0.326OHM MCFK1608T1R0M NA ← SOC_PMU_BUCK2_LX
BUCK2_FB ← SOC_PMU_BUCK2_FB
MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.1200 DIDT=TRUE SWITCH_NODE=TRUE
- CRITICAL C4238 10UF 20% 6.3V CERM-X5R 0402
- CRITICAL C4239 10UF 20% 6.3V CERM-X5R 0402
- CRITICAL C4240 4.7UF 20% 6.3V CER-X5R 0402
- CRITICAL C4241 4.7UF 20% 6.3V CER-X5R 0402

PP1V1_SLEEP3_BUCK2
Mirror Capacitors in Layout

VDD1 VDD18_USB VDDIO18_GRP0 — 100MA MAX

BUCK3_LX ← L4205 1.0UH-1.3A-0.326OHM MCFK1608T1R0M NA ← SOC_PMU_BUCK3_LX
BUCK3_FB ← SOC_PMU_BUCK3_FB
MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.1200 DIDT=TRUE SWITCH_NODE=TRUE
- CRITICAL C4234 4.7UF 20% 6.3V CER-X5R 0402
- CRITICAL C4235 4.7UF 20% 6.3V CER-X5R 0402
- CRITICAL C4236 4.7UF 20% 6.3V CER-X5R 0402
- CRITICAL C4237 4.7UF 20% 6.3V CER-X5R 0402

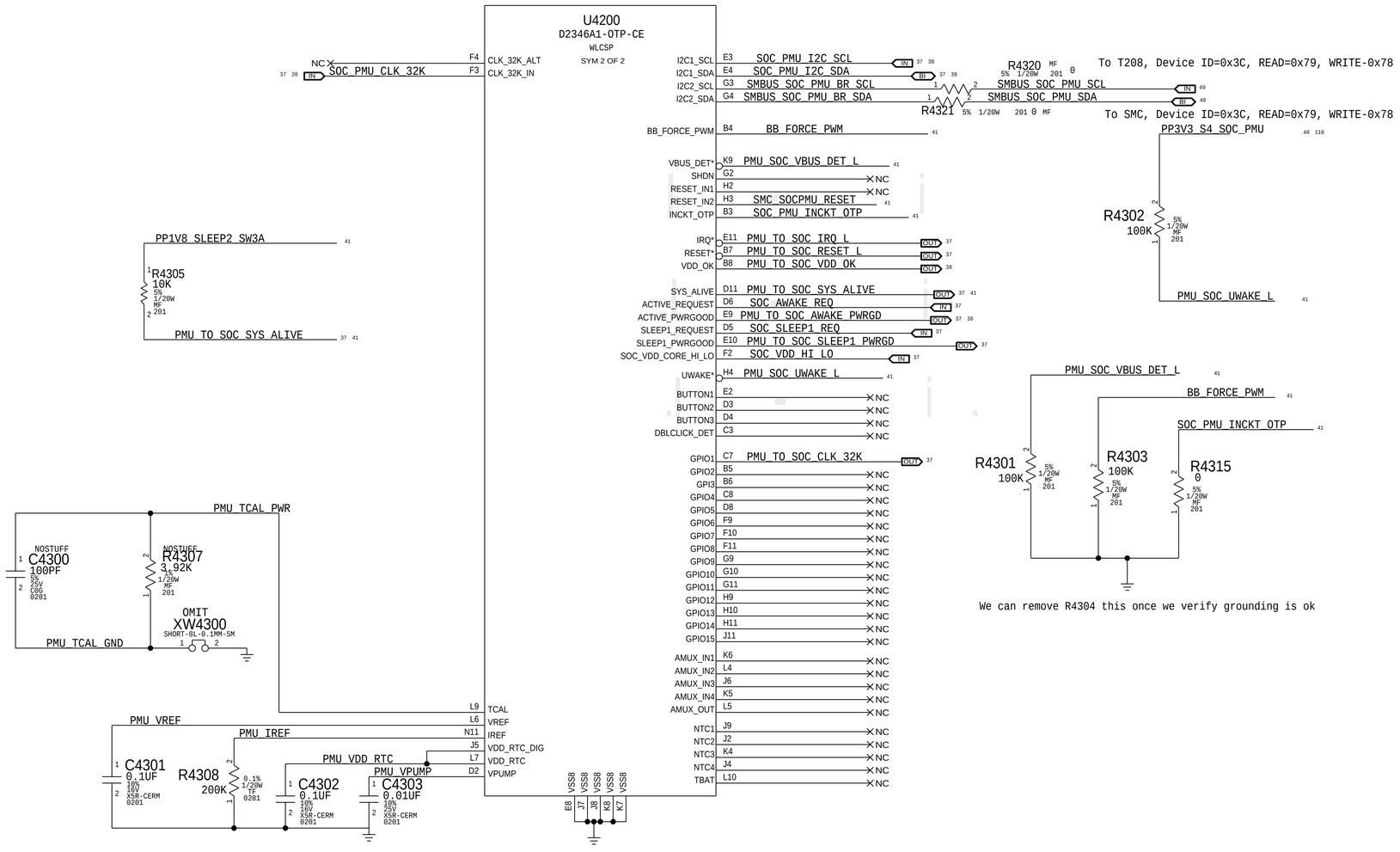
PP1V8_SLEEP3_BUCK3
Mirror Capacitors in Layout

BUCK4_LX ← Not using Buck4 → NC
BUCK4_FB → NC

BOM_COST_GROUP=T151

PAGE TITLE	Berkelium - 1
	Apple Inc.
DRAWING NUMBER	051-00789
SIZE	D
REVISION	PROTO1A
BRANCH	dvt-fab10
PAGE	42 OF 145
SHEET	40 OF 121

Berkelium - 2

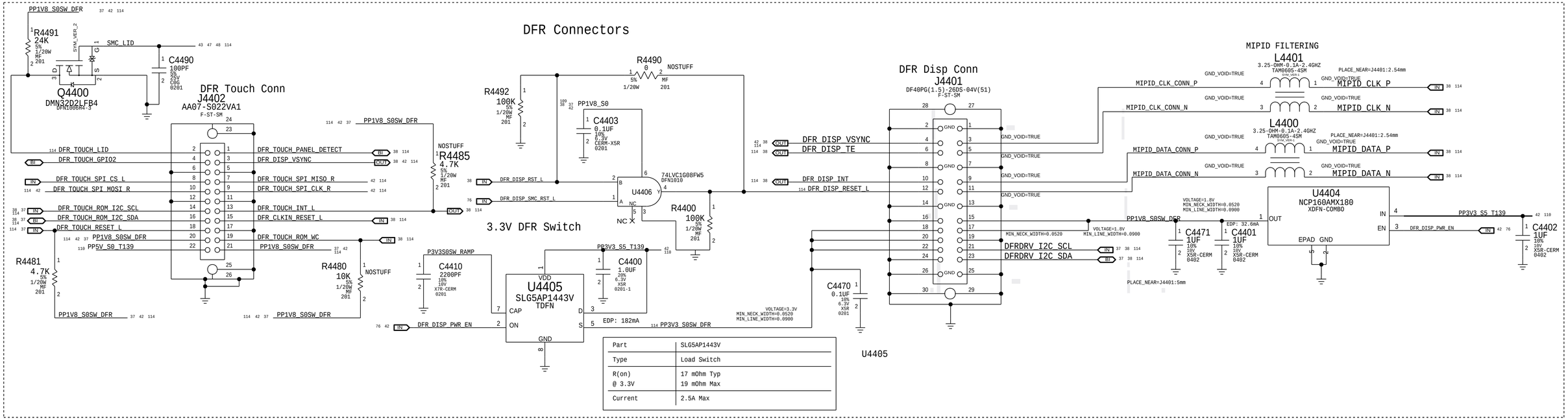


BOM_COST_GROUP=T151

PAGE TITLE	Berkelium - 2
	Apple Inc.
DRAWING NUMBER	051-00789
SIZE	D
REVISION	PROTO1A
BRANCH	dvt-fab10
PAGE	43 OF 145
SHEET	41 OF 121

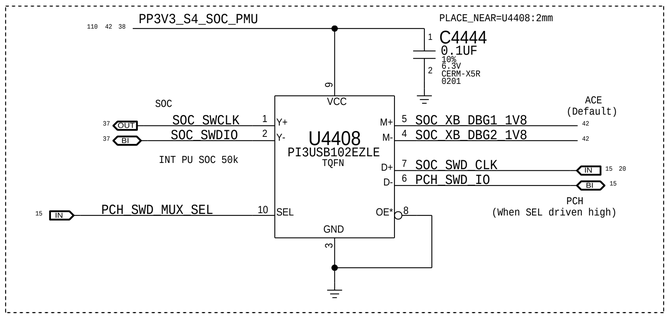
T208 Support

DFR Connectors



Part	SLG5AP1443V
Type	Load Switch
R(on) @ 3.3V	17 mOhm Typ 19 mOhm Max
Current	2.5A Max

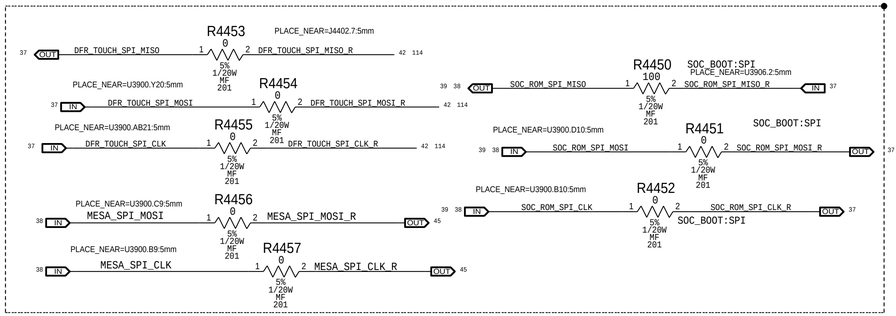
SWD DEBUG MUX



T208 I2C Mapping

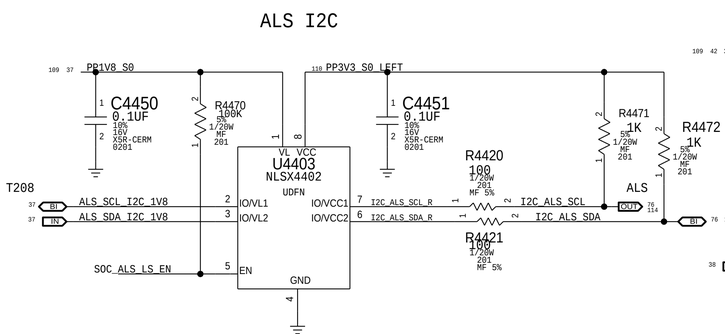
Bus	Device	7-bit Address	8-bit Address Read	8-bit Address Write
AP0	PMU	0011110 (0x3C)	0x79	0x78
AP1	Touch EEPROM	1010000 (0x50)	0xA1	0xA0
AP2_0	Tesla	1010100 (0x4C)	0x99	0x98
AOP0	Mesa EEPROM	101000x (0x50/0x51)	0xA1/A3	0xA0/A2
AOP1	ALS	0111001 (0x39)	0x73	0x72
SEP	M34128 EEPROM	1010001 (0x51)	0xA3	0xA2

SPI TERM

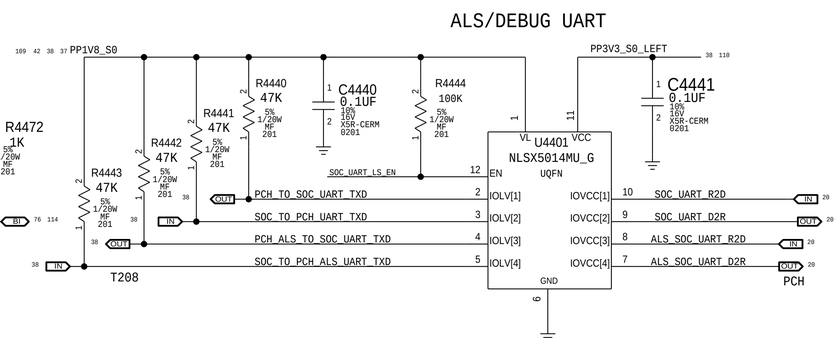


T208 LEVEL SHIFTING

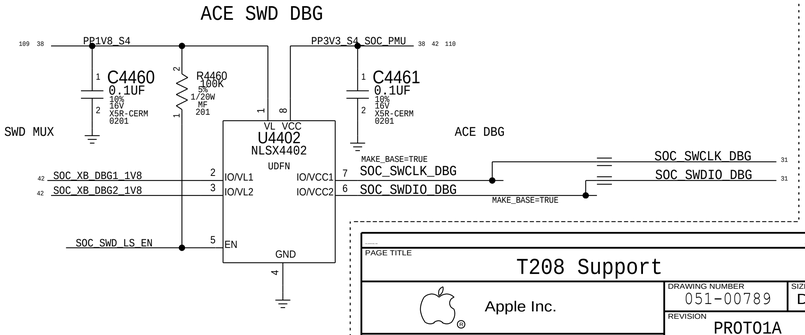
ALS I2C



ALS/DEBUG UART



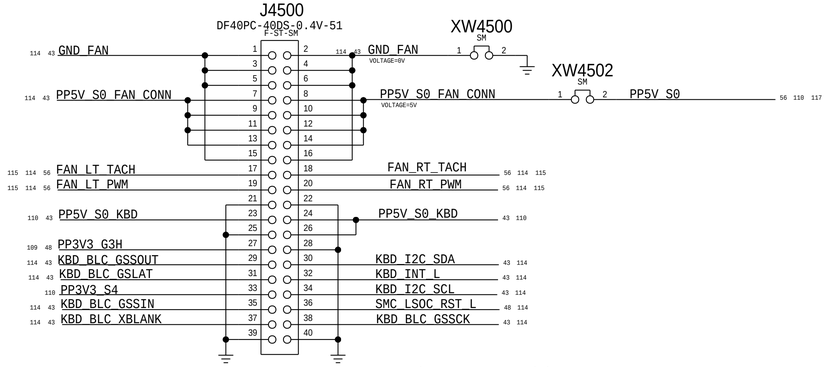
ACE SWD DBG



BOM_COST_GROUP=T151

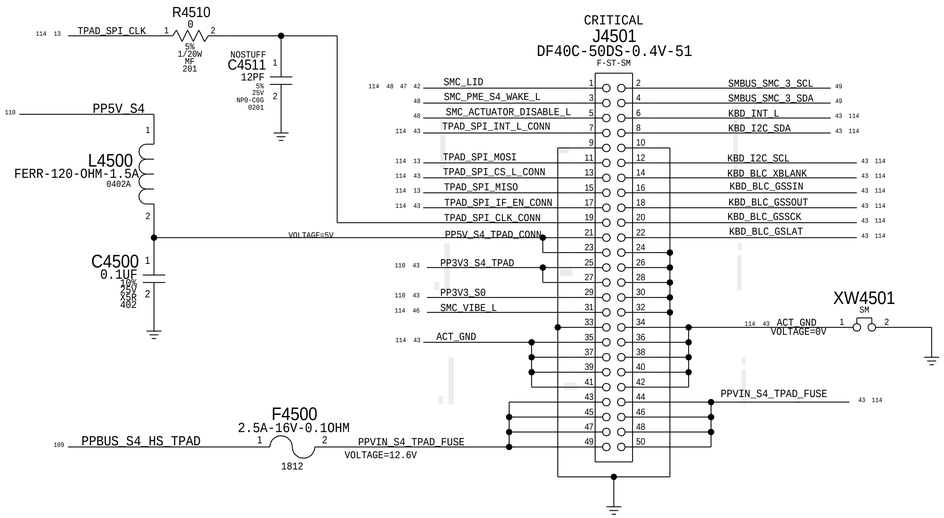
PAGE TITLE	T208 Support
Apple Inc.	
DRAWING NUMBER	051-00789
SIZE	D
REVISION	PROTO1A
BRANCH	dvt-fab10
PAGE	44 OF 145
SHEET	42 OF 121

KBD CONNECTOR



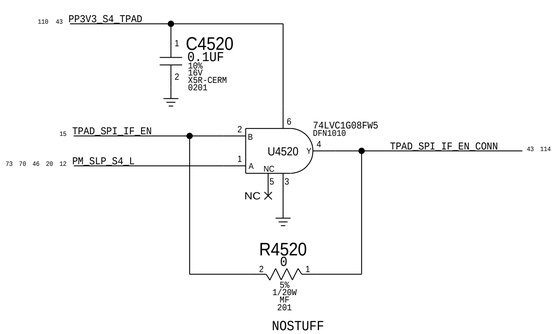
518S00177 (RCPT, 0.3A per pin)
MATE WITH PLUG 516S00054

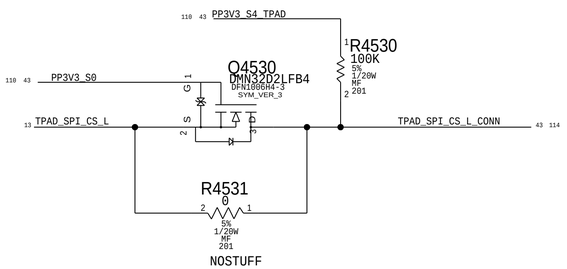
TPAD CONNECTOR

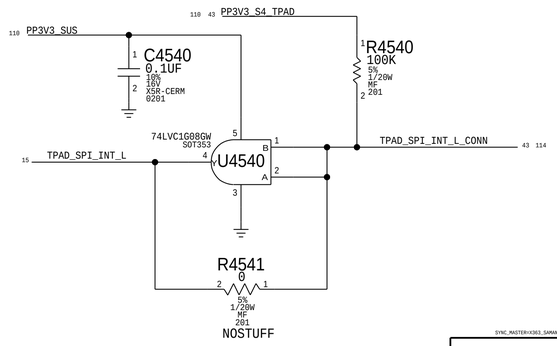


516S00187, MATE WITH 516S00188

TRACKPAD ISOLATION GATES/FET







BOM_COST_GROUP=KEYBOARD

SYNC_MASTER=X383_SAMANTHA SYNC_DATE=01/08/2018

PAGE TITLE
Connectors&ESD

Apple Inc.

DRAWING NUMBER 051-00789
SIZE D
REVISION PROTO1A
BRANCH dvt-fab10
PAGE 45 OF 145
SHEET 43 OF 121

BOM_COST_GROUP=DEBUG

SYNC_MASTER=288_MLB SYNC_DATE=08/26/2015

PAGE TITLE

External A USB3 Connector

Apple Inc.

DRAWING NUMBER 051-00789

SIZE D

REVISION PROTO1A

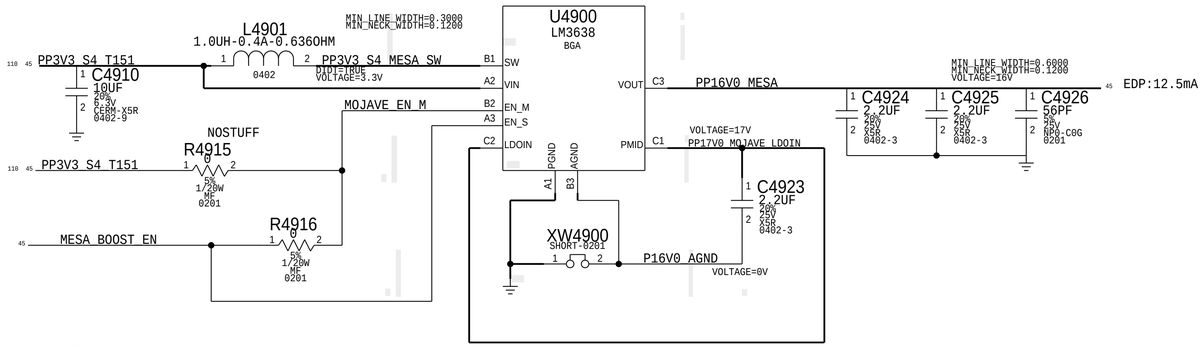
BRANCH dvt-fab10

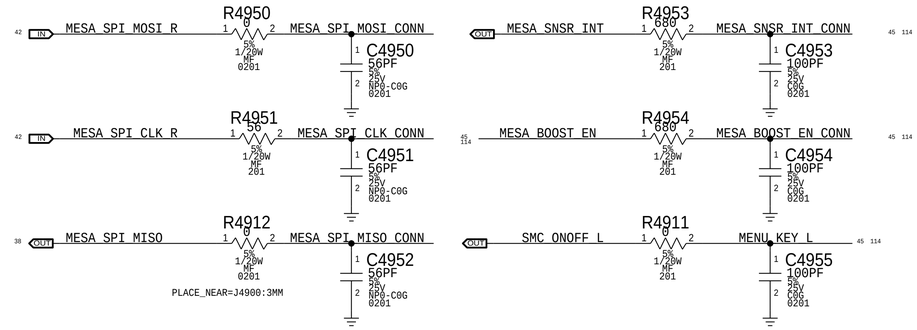
PAGE 47 OF 145

SHEET 44 OF 121

ISOLATE FROM OTHER COMPONENTS/NETS AS MUCH AS POSSIBLE

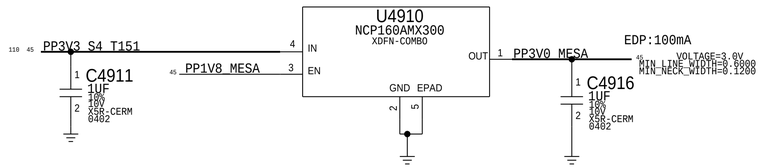
MOJAVE 16V BOOST

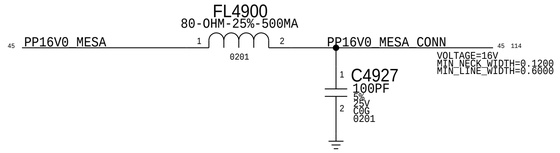


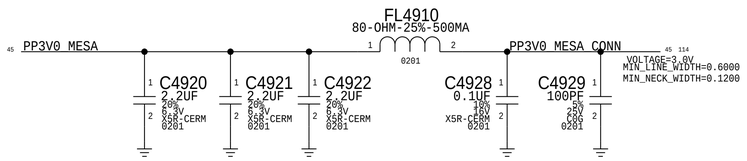


3.0V MESA

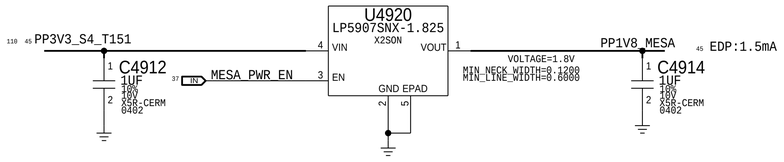
Option to feed LDO from 5V in case of dropout issue

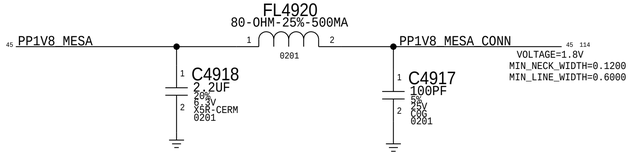






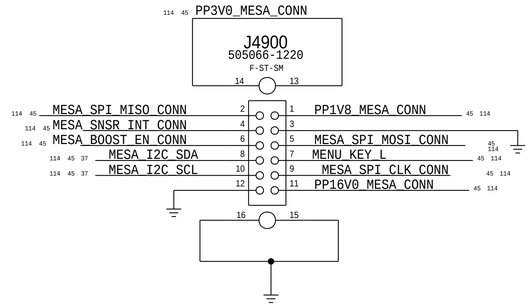
1.8V MESA





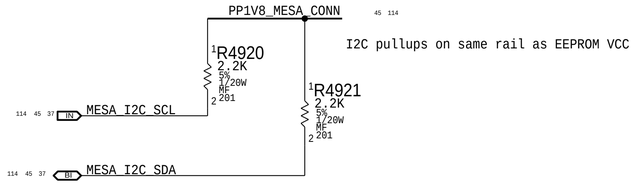
MESA FLEX CONNECTOR

Proto1 Connector for X434/X435 Support
PLUG (516S00115) - X434/ X435 Jumper
Recptacle (516S00203) - X362/X363 MLB



Mesa Power Sequencing Requirements

Power On: 1V8 -> 3V3 -> 16V0

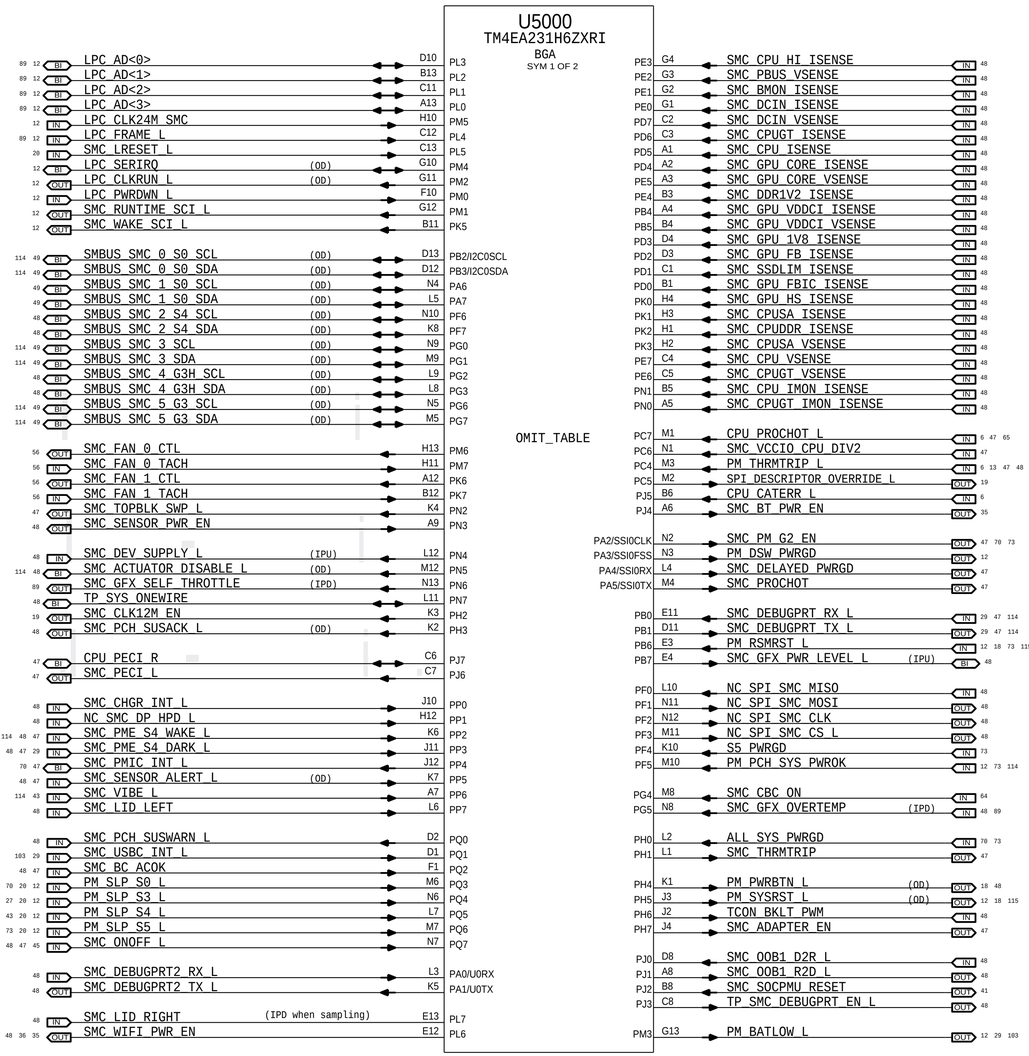


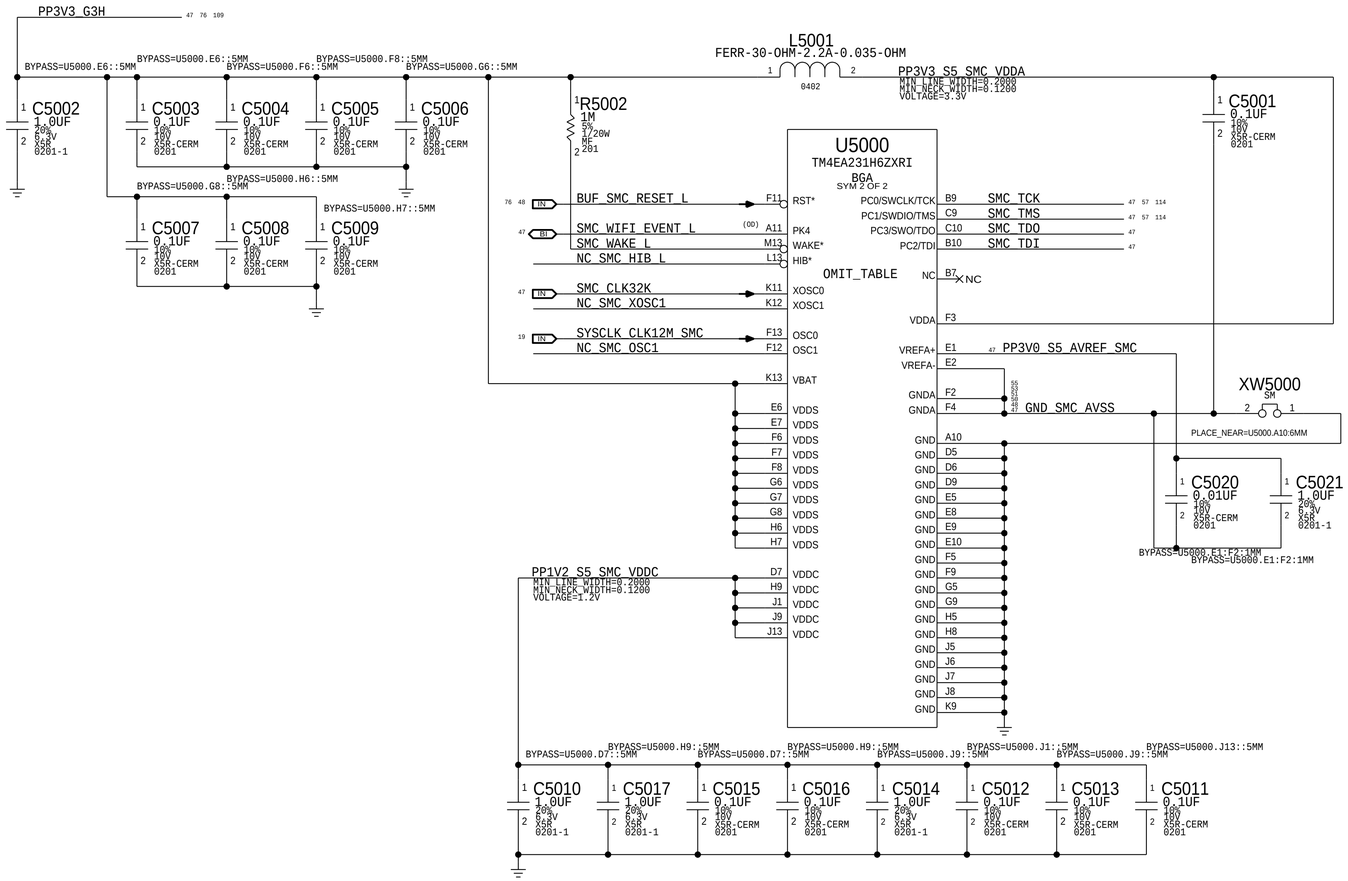
BOM_COST_GROUP=T151

PAGE TITLE: MESA

Apple Inc.

DRAWING NUMBER: 051-00789
SIZE: D
REVISION: PROTO1A
BRANCH: dvt-fab10
PAGE: 49 OF 145
SHEET: 45 OF 121





NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.

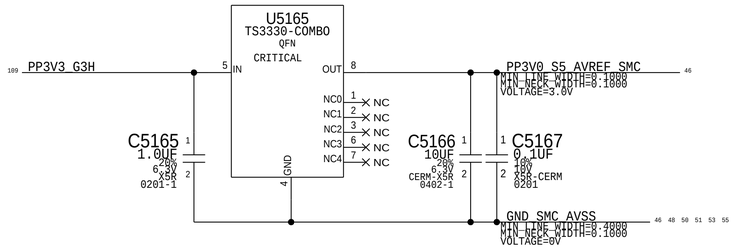
BOM_COST_GROUP=SMC

PAGE TITLE
SMC

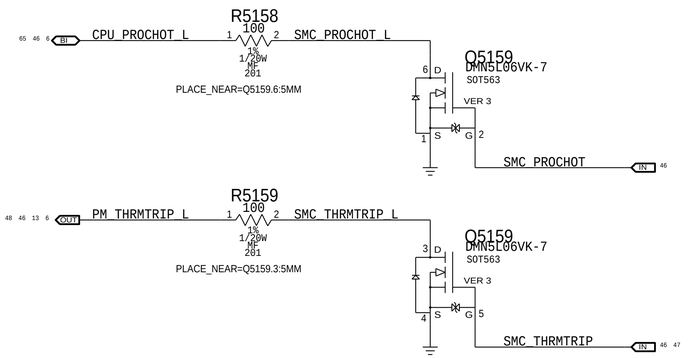
Apple Inc.

DRAWING NUMBER 051-00789
SIZE D
REVISION PR0T01A
BRANCH dvt-fab10
PAGE 50 OF 145
SHEET 46 OF 121

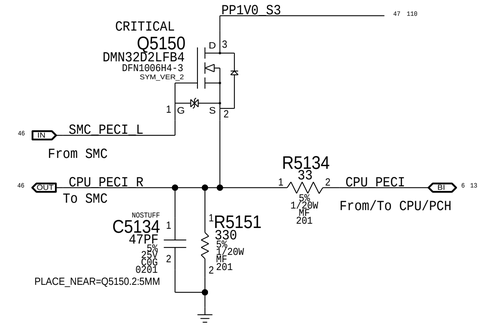
SMC AVREF Supply



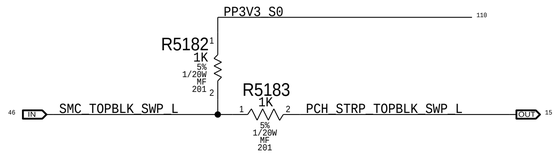
PROCHOT/THRMTRIP Support

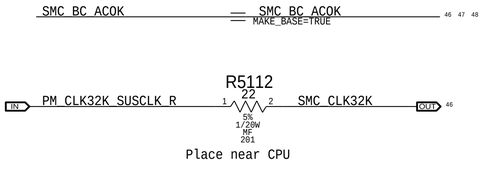


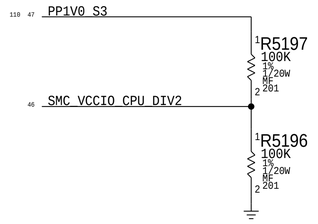
PECI Support

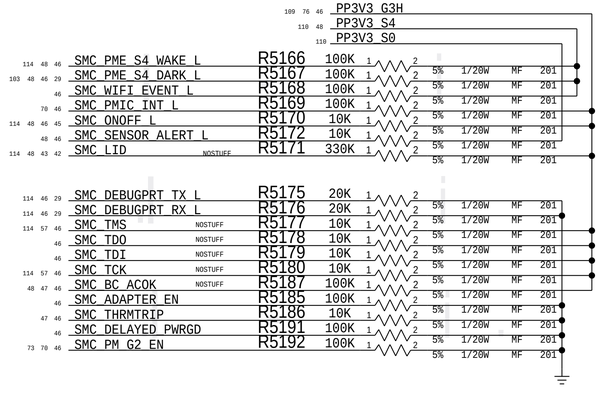


Top-Block Swap









BOM_COST_GROUP=SMC

SYNC_MASTER=J80_ZIFENGSHEN_MLB_BAFFIN SYNC_DATE=11/19/2015

PAGE TITLE: SMC Shared Support

Apple Inc.

DRAWING NUMBER: 051-00789
SIZE: D
REVISION: PROTO1A
BRANCH: dvt-fab10
PAGE: 51 OF 145
SHEET: 47 OF 121

SMC12 ADC Assignments

SMC_CPU_HI_ISENSE	SMC_CPU_HI_ISENSE	MAKE_BASE=TRUE	
SMC_PBUS_VSENSE	SMC_PBUS_VSENSE	MAKE_BASE=TRUE	
SMC_BMON_ISENSE	SMC_BMON_ISENSE	MAKE_BASE=TRUE	
SMC_DCIN_ISENSE	SMC_DCIN_ISENSE	MAKE_BASE=TRUE	
SMC_DCIN_VSENSE	SMC_DCIN_VSENSE	MAKE_BASE=TRUE	
SMC_CPUGT_ISENSE	SMC_CPUGT_ISENSE	MAKE_BASE=TRUE	
SMC_CPU_ISENSE	SMC_CPU_ISENSE	MAKE_BASE=TRUE	
SMC_GPU_CORE_ISENSE	SMC_GPU_CORE_ISENSE	MAKE_BASE=TRUE	
SMC_GPU_CORE_VSENSE	SMC_GPU_CORE_VSENSE	MAKE_BASE=TRUE	
SMC_DDR1V2_ISENSE	SMC_DDR1V2_ISENSE	MAKE_BASE=TRUE	
SMC_GPU_VDDCI_ISENSE	SMC_GPU_VDDCI_ISENSE	MAKE_BASE=TRUE	
SMC_GPU_VDDCI_VSENSE	SMC_GPU_VDDCI_VSENSE	MAKE_BASE=TRUE	
SMC_GPU_1V8_ISENSE	SMC_GPU_1V8_ISENSE	MAKE_BASE=TRUE	
SMC_GPU_FB_ISENSE	SMC_GPU_FB_ISENSE	MAKE_BASE=TRUE	
SMC_SSDLIM_ISENSE	SMC_SSDLIM_ISENSE	MAKE_BASE=TRUE	
SMC_GPU_FBIC_ISENSE	SMC_GPU_FBIC_ISENSE	MAKE_BASE=TRUE	
SMC_GPU_HS_ISENSE	SMC_GPU_HS_ISENSE	MAKE_BASE=TRUE	
SMC_CPUSA_ISENSE	SMC_CPUSA_ISENSE	MAKE_BASE=TRUE	
SMC_CPUDDR_ISENSE	SMC_CPUDDR_ISENSE	MAKE_BASE=TRUE	
SMC_CPUSA_VSENSE	SMC_CPUSA_VSENSE	MAKE_BASE=TRUE	
SMC_CPU_VSENSE	SMC_CPU_VSENSE	MAKE_BASE=TRUE	
SMC_CPUGT_VSENSE	SMC_CPUGT_VSENSE	MAKE_BASE=TRUE	
SMC_CPU_IMON_ISENSE	SMC_CPU_IMON_ISENSE	MAKE_BASE=TRUE	
SMC_CPUGT_IMON_ISENSE	SMC_CPUGT_IMON_ISENSE	MAKE_BASE=TRUE	

SMC12 Pin Assignments

SMC_GFX_PWR_LEVEL_L	SMC_GFX_PWR_LEVEL_L	MAKE_BASE=TRUE
TP_SYS_ONEWIRE	TP_SYS_ONEWIRE	MAKE_BASE=TRUE
TP_SMC_DEBUGPRT_EN_L	TP_SMC_DEBUGPRT_EN_L	MAKE_BASE=TRUE
NC_SMC_DP_HPD_L	NC_SMC_DP_HPD_L	MAKE_BASE=TRUE

PM_THRMTRIP_L

CRITICAL
O5290
DMN32D2LFB4
DFN1006H4-3
SYM_VER_2

SMC_GFX_OVERTEMP

NC_SPI_SMC_MISO	NC_SPI_SMC_MISO	TRUE
NC_SPI_SMC_MOSI	NC_SPI_SMC_MOSI	TRUE
NC_SPI_SMC_CLK	NC_SPI_SMC_CLK	TRUE
NC_SPI_SMC_CS_L	NC_SPI_SMC_CS_L	TRUE

SMC_PCH_SUSWARN_L	SMC_PCH_SUSWARN_L	MAKE_BASE=TRUE
SMC_PCH_SUSACK_L	SMC_PCH_SUSACK_L	MAKE_BASE=TRUE
SMC_SENSOR_PWR_EN	SMC_SENSOR_PWR_EN	MAKE_BASE=TRUE
PM_PWRBTN_L	PM_PWRBTN_L	MAKE_BASE=TRUE
SMC_BC_ACOK	SMC_BC_ACOK	
SMC_BC_ACOK	SMC_BC_ACOK	MAKE_BASE=TRUE
SMBUS_SMC_4_G3H_SCL	SMBUS_SMC_4_G3H_SCL	MAKE_BASE=TRUE
SMBUS_SMC_4_G3H_SDA	SMBUS_SMC_4_G3H_SDA	MAKE_BASE=TRUE
SMBUS_SMC_2_S4_SCL	SMBUS_SMC_2_S4_SCL	MAKE_BASE=TRUE
SMBUS_SMC_2_S4_SDA	SMBUS_SMC_2_S4_SDA	MAKE_BASE=TRUE
SMC_OOB1_D2R_L	SMC_OOB1_D2R_L	MAKE_BASE=TRUE
SMC_OOB1_R2D_L	SMC_OOB1_R2D_L	MAKE_BASE=TRUE
SMC_ACTUATOR_DISABLE_L	SMC_ACTUATOR_DISABLE_L	MAKE_BASE=TRUE
SMC_CHGR_INT_L	SMC_CHGR_INT_L	MAKE_BASE=TRUE

Debug Power "Buttons"

PLACE_SIDE=TOP
SILK_PART=PWR_BTN
R5226
RES
0603-NSP
BOMOPTION=OMIT

SMC_ONOFF_L

SW5200
EVQPUA02K

BOMOPTION=DBG_BTN
SILK_PART=PWR_BTN
PLACE_SIDE=BOTTOM

Debug RESET "Buttons"

BOMOPTION=DBG_BTN
PLACE_SIDE=BOTTOM
SILK_PART=RESET_BTN
CRITICAL
SW5227
SOX-152HNT
SM

SMC_RESET_L

Thermal Alerts

SMC_CPUHI_COMP_ALERT_L	R5217 100		
CPUTHMSNS_THM_L	R5216 100	CPUTHRM_THRM:SMC	
CPUTHMSNS_ALERT_L	R5214 100	CPUTHRM_ALRT:SMC	
TBTTHMSNS_X_THM_L	R5220 100	TBTTHRM_THRM:SMC	
TBTTHMSNS_T_THM_L	R5221 100	TBTTHRM_THRM:SMC	
TBTTHMSNS_X_ALERT_L	R5210 100	TBTTHRM_ALRT:SMC	
TBTTHMSNS_T_ALERT_L	R5211 100	TBTTHRM_ALRT:SMC SMC_SENSOR_ALERT_L	

NOSTUFF
5% 1/20W MF 201

BYPASS=U5256.5::5MM
PP3V3_G3H
R5256 100K 5% 1/20W MF 201
C5256 0.1UF 10% 10V X5R-CERM 0201

SMC_LSOC_RST_L
SMC_ONOFF_L
SN74LVC1G02 SOT553-5
U5256
CRITICAL
SMC_4FINGERS_RST

S4 SMC Wake Sources

SMC_PME_S4_WAKE_L	SMC_PME_S4_WAKE_L	MAKE_BASE=TRUE
SMC_PME_S4_DARK_L	SMC_PME_S4_DARK_L	MAKE_BASE=TRUE

R5258 0 5% 1/20W MF 201
PP3V3_G3H
BYPASS=U5255.6::5MM
C5255 0.1UF 10% 10V X5R-CERM 0201
LID_FEATURE_ON
SMC_LID_LEFT
R5257 0 5% 1/20W MF 201
LID_FEATURE_OFF

U5255
74LVC1G32
SOT891
SMC_LID_LEFT_R
SMC_LID_RIGHT
SMC_LID_R
CRITICAL
R5255 10K 5% 1/20W MF 201
SMC_LID

R5259 0 5% 1/20W MF 201
SMC_DEV_SUPPLY_L
SMC_DEV_SUPPLY_R_L

R5260 10 5% 1/20W MF 201
TCON_BKLT_PWM
BKLT_PWM_TCON2MLB
C5257 3300PF 10% 16V X7R-CERM 0201
NOSTUFF

Hall Effect Pads - Left

J5250
AMR-MLB-X502
SM
OMIT_TABLE
HALL_SENSOR_LEFT
PP3V3_G3H
C5250 1000PF 10% 16V X7R-1 0201
NOSTUFF
R5252 10K 5% 1/20W MF 201
SMC_LID_LEFT_R

Hall Effect Pads - Right

J5260
AMR-MLB-X502
SM
OMIT_TABLE
HALL_SENSOR_RIGHT
PP3V3_G3H
C5260 1000PF 10% 16V X7R-1 0201
NOSTUFF
R5253 10K 5% 1/20W MF 201
SMC_LID_RIGHT

Specify one of these BOM GROUPS.

BOM GROUP	BOM OPTIONS
CPUTHRM:BOTH	CPUTHRM_THRM:SMC,CPUTHRM_ALRT:SMC
CPUTHRM:THRM	CPUTHRM_THRM:SMC
CPUTHRM:ALRT	CPUTHRM_ALRT:SMC

Specify one of these BOM GROUPS.

BOM GROUP	BOM OPTIONS
TBTTHRM:BOTH	TBTTHRM_THRM:SMC,TBTTHRM_ALRT:SMC
TBTTHRM:THRM	TBTTHRM_THRM:SMC,TBTTHRM_ALRT:PU
TBTTHRM:ALRT	TBTTHRM_THRM:PU,TBTTHRM_ALRT:SMC
TBTTHRM:NONE	TBTTHRM_THRM:PU,TBTTHRM_ALRT:PU

PP3V3_S4
R5274 100K 5% 1/20W MF 201
R5273 10K 5% 1/20W MF 201
PLACE_SIDE=BOTTOM
NOSTUFF
R5275 0 5% 1/20W MF 0201
SMC_DEBUGPRT2_TX_L
WLAN_UART_RX
PLACE_SIDE=BOTTOM
NOSTUFF
R5276 0 5% 1/20W MF 0201
SMC_DEBUGPRT2_RX_L
WLAN_UART_TX
PP3V3_G3H
R5280 100K 5% 1/20W MF 201
R5281 10K 5% 1/20W MF 201
PLACE_SIDE=BOTTOM
R5277 0 5% 1/20W MF 0201
SMC_DEBUGPRT2_R_TX
TP5200
R5278 0 5% 1/20W MF 0201
SMC_DEBUGPRT2_R_RX
TP5201
PLACE_SIDE=BOTTOM

SMC_WIFI_PWR_EN
R5295 10K 5% 1/20W MF 201
NOSTUFF
SMC_SENSOR_PWR_EN
R5294 10K 5% 1/20W MF 201
NOSTUFF

BUF_SMC_RESET_L
NOSTUFF
C5270 1000PF 10% 16V X7R-CERM 0201
GND_SMC_AVSS

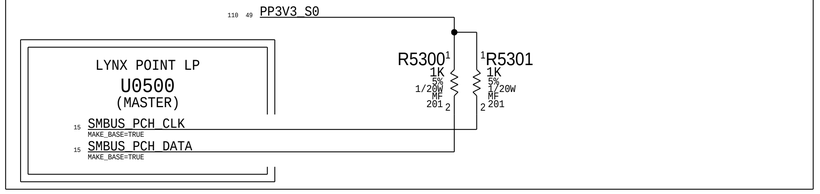
BOM_COST_GROUP=SMC

PAGE TITLE
SMC Project Support

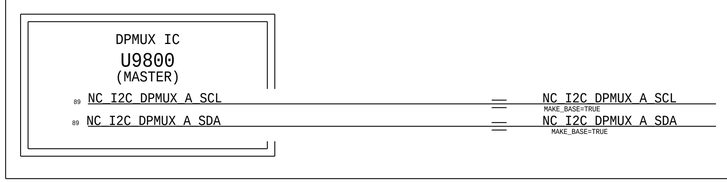
Apple Inc.

DRAWING NUMBER 051-00789
SIZE D
REVISION PROTO1A
BRANCH dvt-fab10
PAGE 52 OF 145
SHEET 48 OF 121

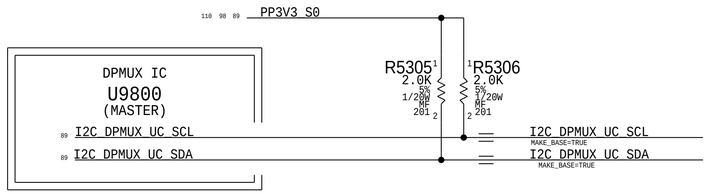
LYNX POINT LP S0 "SMBus 0" Connections



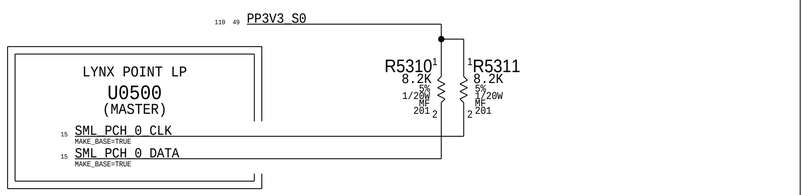
DPMUX Connections



DPMUX Connections



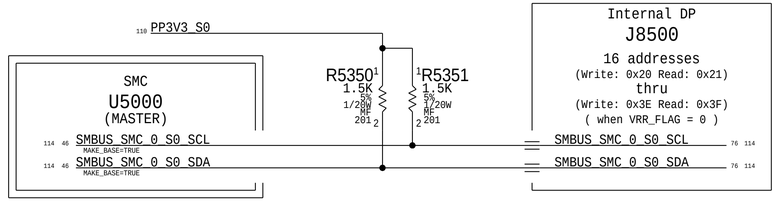
LYNX POINT LP S0 "SMLink 0" Connections



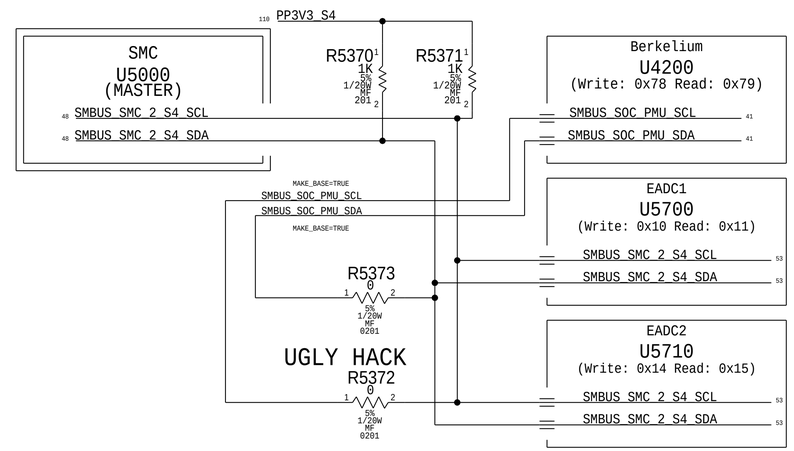
LYNX POINT LP S0 "SMLink 1" Connections

SMLink 1 is slave port to
access PCH.

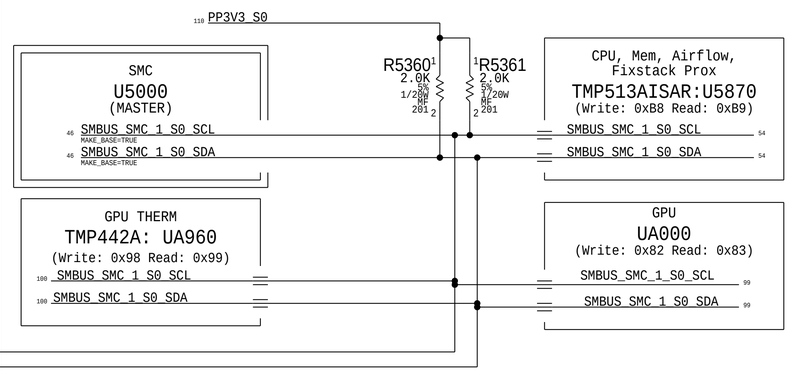
SMC SMBus "0" S0 Connections



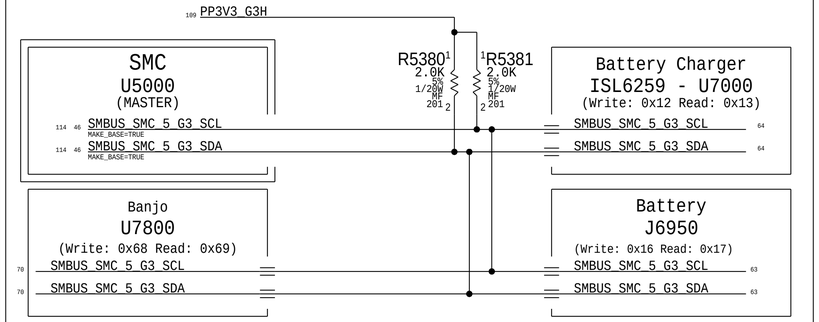
SMC SMBus "2" S4 Connections



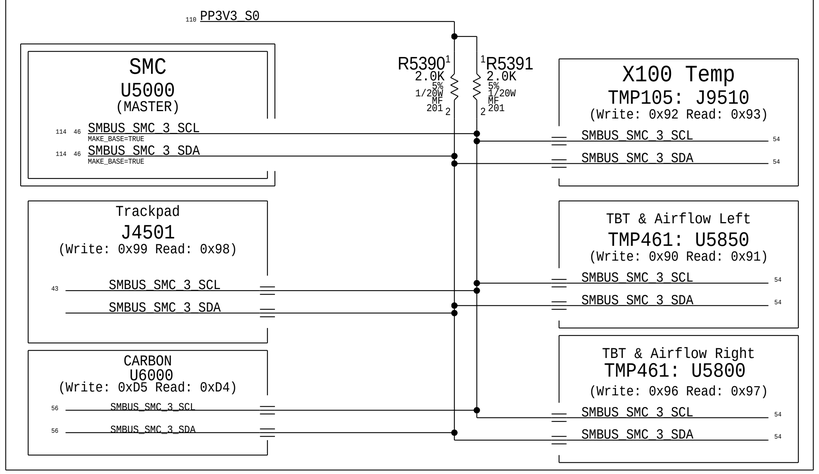
SMC SMBus "1" S0 Connections



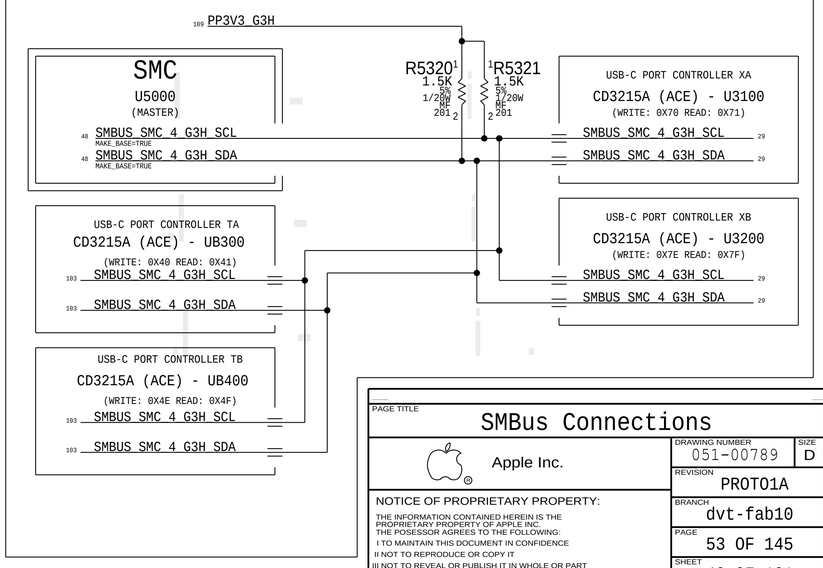
SMC SMBus "5" G3H Connections



SMC SMBus "3" S0 Connections



SMC SMBUS "4" G3H CONNECTIONS



BOM_COST_GROUP=SMC

PAGE TITLE

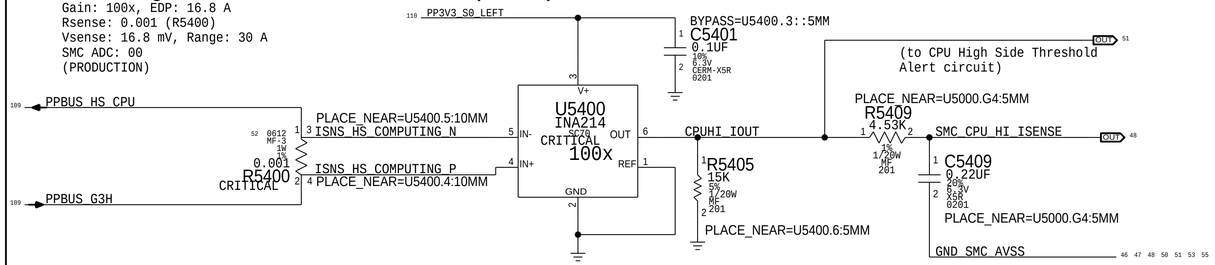
SMBus Connections

Apple Inc.

DRAWING NUMBER 051-00789 | SIZE D
REVISION PROTO1A
BRANCH dvt-fab10
PAGE 53 OF 145
SHEET 49 OF 121

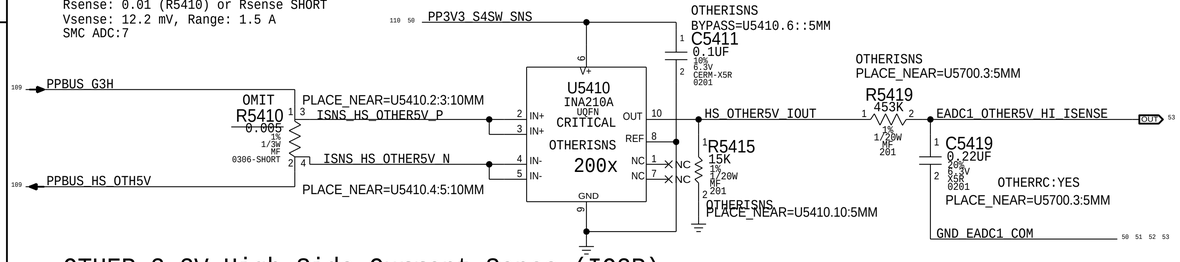
CPU High Side Current Sense (IC0R)

Gain: 100x, EDP: 16.8 A
Rsense: 0.001 (R5400)
Vsense: 16.8 mV, Range: 30 A
SMC ADC: 00
(PRODUCTION)



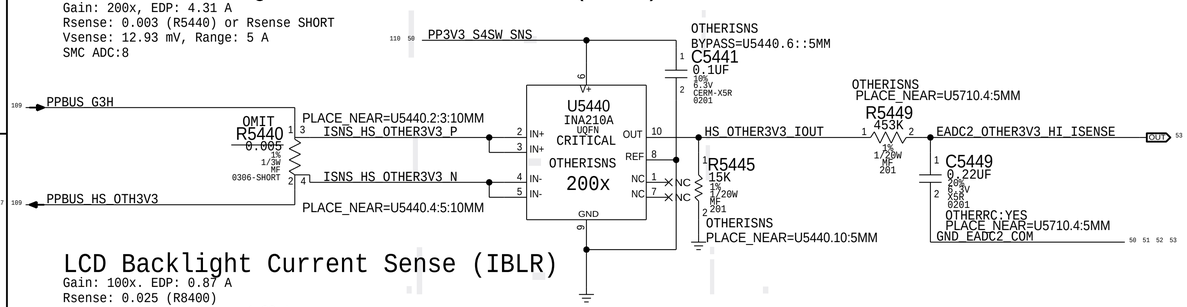
OTHER 5V High Side Current Sense (IO5R)

Gain: 200x, EDP: 1.22 A
Rsense: 0.01 (R5410) or Rsense SHORT
Vsense: 12.2 mV, Range: 1.5 A
SMC ADC:7



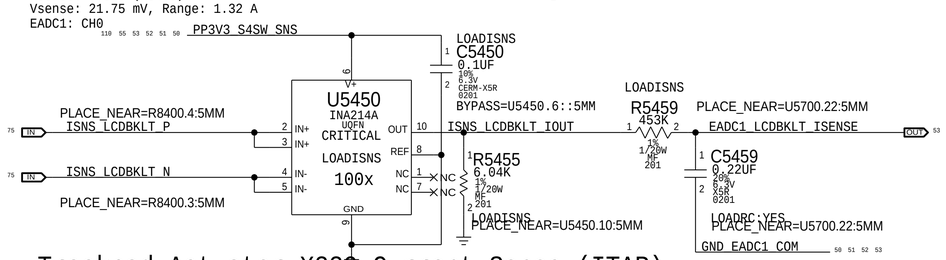
OTHER 3.3V High Side Current Sense (IO3R)

Gain: 200x, EDP: 4.31 A
Rsense: 0.003 (R5440) or Rsense SHORT
Vsense: 12.93 mV, Range: 5 A
SMC ADC:8



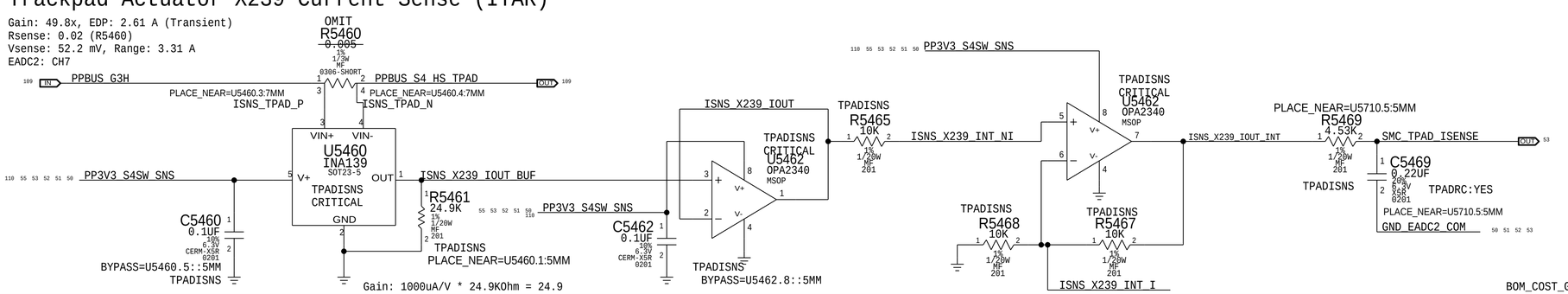
LCD Backlight Current Sense (IBLR)

Gain: 100x. EDP: 0.87 A
Rsense: 0.025 (R8400)
Vsense: 21.75 mV, Range: 1.32 A
EADC1: CH0



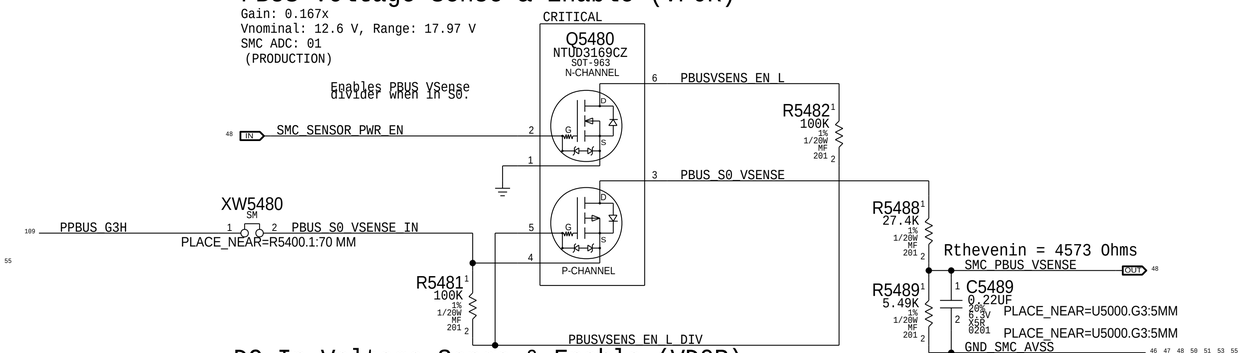
Trackpad Actuator X239 Current Sense (ITAR)

Gain: 49.8x, EDP: 2.61 A (Transient)
Rsense: 0.02 (R5460)
Vsense: 52.2 mV, Range: 3.31 A
EADC2: CH7



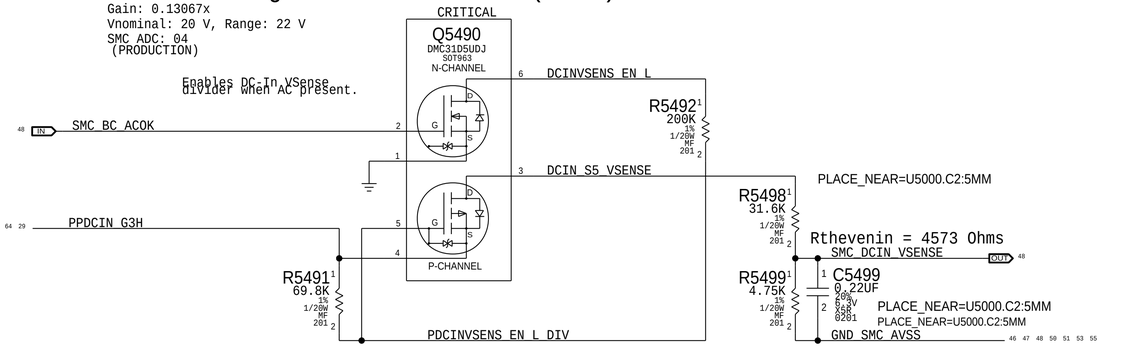
PBUS Voltage Sense & Enable (VP0R)

Gain: 0.167x
Vnominal: 12.6 V, Range: 17.97 V
SMC ADC: 01
(PRODUCTION)



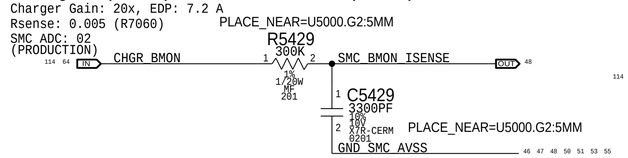
DC In Voltage Sense & Enable (VD0R)

Gain: 0.13067x
Vnominal: 20 V, Range: 22 V
SMC ADC: 04
(PRODUCTION)



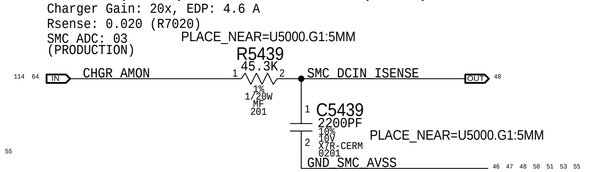
Charger (BMON) Current Sense (IPBR)

Charger Gain: 20x, EDP: 7.2 A
Rsense: 0.005 (R7060)
SMC ADC: 02
(PRODUCTION)



DC-IN (AMON) Current Sense (ID0R)

Charger Gain: 20x, EDP: 4.6 A
Rsense: 0.020 (R7020)
SMC ADC: 03
(PRODUCTION)



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5419,C5449		OTHERRC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5459		LOADRC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5469		TPADRC:NO

BOM_COST_GROUP=SENSORS

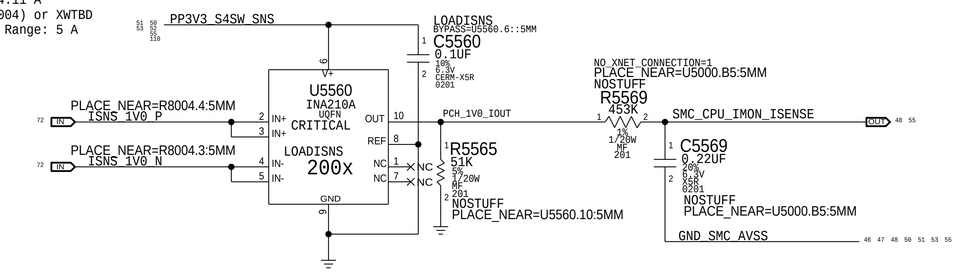
PAGE TITLE: Power Sensors: High Side

Apple Inc.

DRAWING NUMBER: 051-00789
SIZE: D
REVISION: PROT01A
BRANCH: dvt-fab10
PAGE: 54 OF 145
SHEET: 50 OF 121

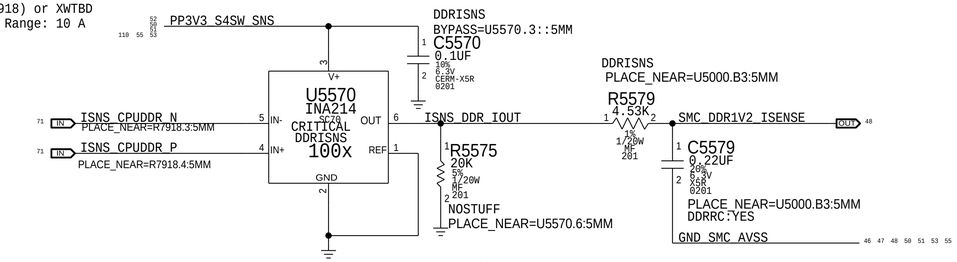
PCH 1.0V Current Sense (ISCC)

Gain: 200x, EDP: 4.11 A
Rsense: 0.003 (R8004) or XWTBD
Vsense: 11.33 mV, Range: 5 A
SMC ADC: 22



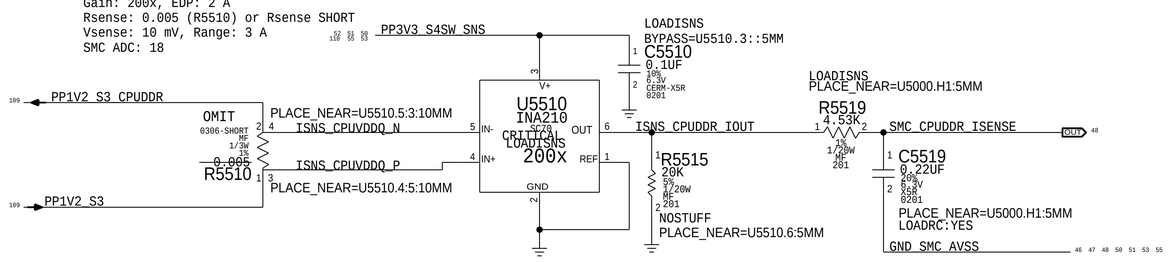
DDR 1.2V S3 (CPU & Memory) Current Sense (IM0C)

Gain: 100x, EDP: 9.01 A
Rsense: 0.003 (R7918) or XWTBD
Vsense: 27.03 mV, Range: 10 A
SMC ADC: 09



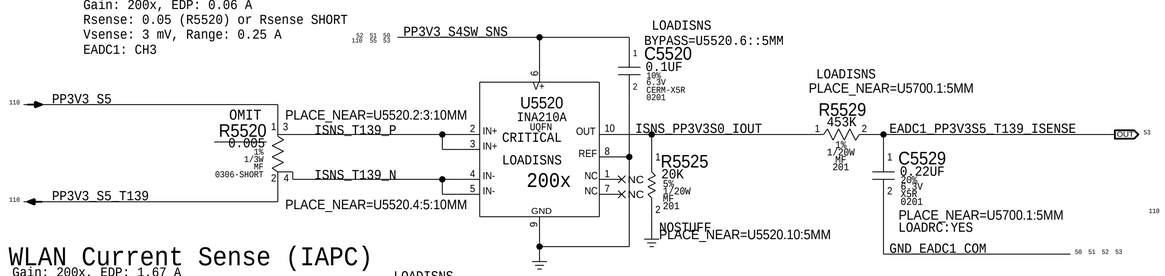
CPU DDR 1.2V S3 (CPU Only) Current Sense (IMCC)

Gain: 200x, EDP: 2 A
Rsense: 0.005 (R5510) or Rsense SHORT
Vsense: 10 mV, Range: 3 A
SMC ADC: 18



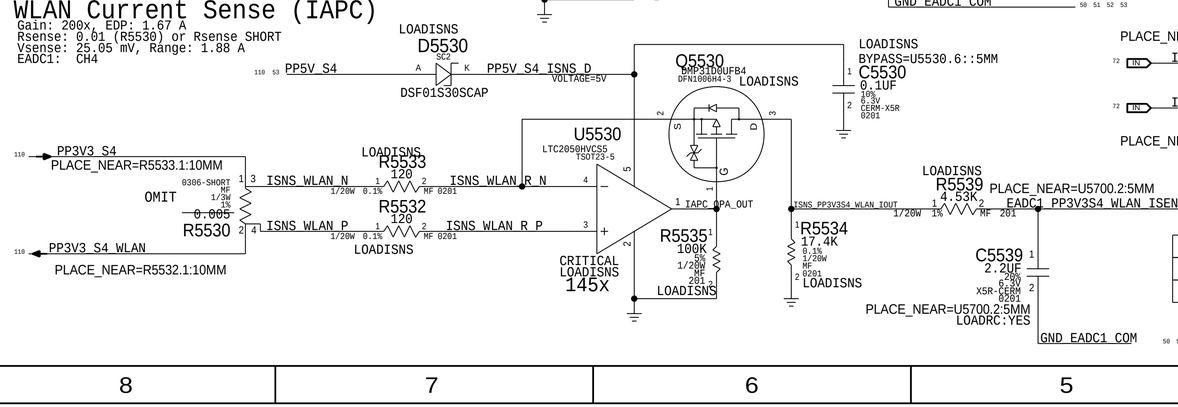
T139 Current Sense (IF3C)

Gain: 200x, EDP: 0.06 A
Rsense: 0.05 (R5520) or Rsense SHORT
Vsense: 3 mV, Range: 0.25 A
EADC1: CH3



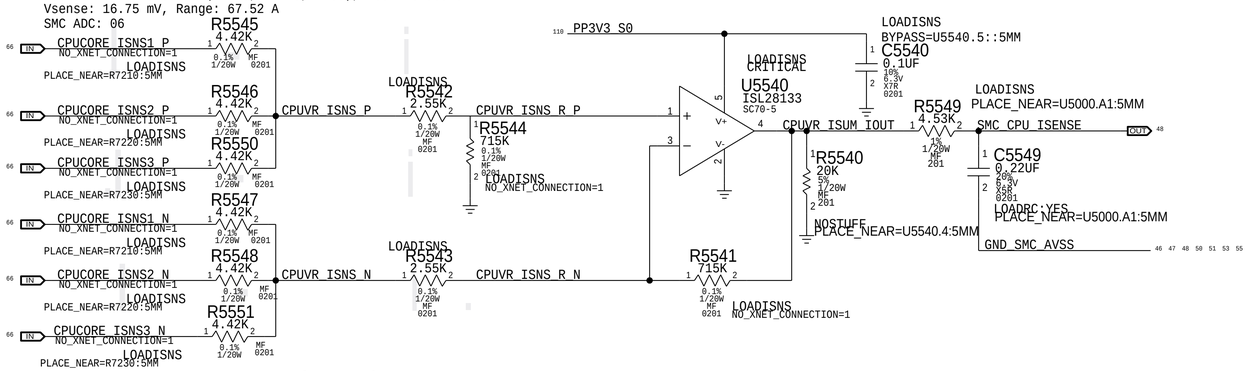
WLAN Current Sense (IAPC)

Gain: 200x, EDP: 1.67 A
Rsense: 0.01 (R5530) or Rsense SHORT
Vsense: 25.05 mV, Range: 1.88 A
EADC1: CH4



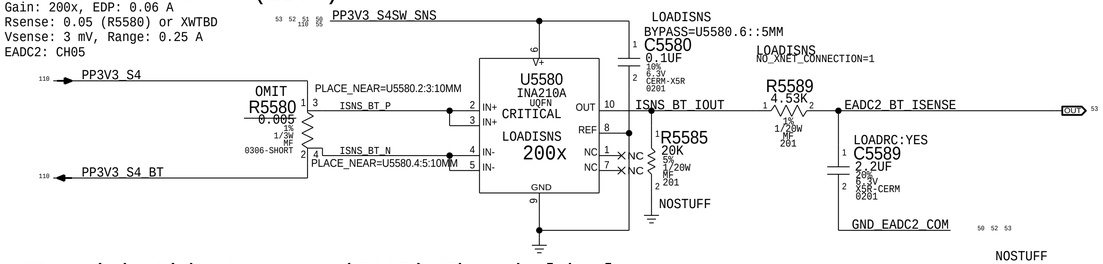
CPU Fixed Current Sense (ICAC)

Gain: 177.71x, EDP: 67 A
Rsense: 3x of 0.00075 (R7210, R7220,R7230), Rsum: 0.00025
Vsense: 16.75 mV, Range: 67.52 A
SMC ADC: 06



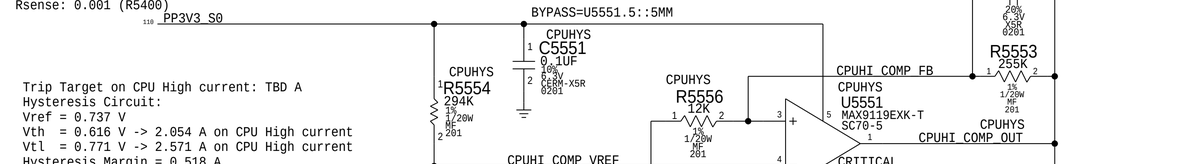
BT Current Sense (IBTC)

Gain: 200x, EDP: 0.06 A
Rsense: 0.05 (R5580) or XWTBD
Vsense: 3 mV, Range: 0.25 A
EADC2: CH05

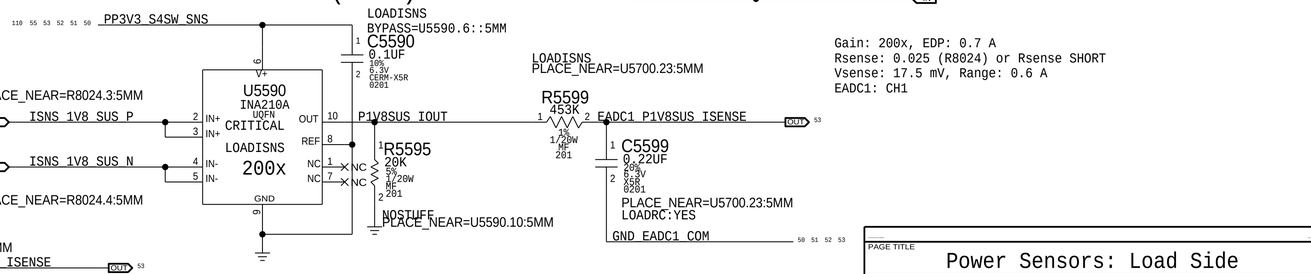


CPU High Side Current (IC0R) Threshold Alert

Gain: 100x
Rsense: 0.001 (R5400)



1.8V Current Sense (I18C)



Gain: 200x, EDP: 0.7 A
Rsense: 0.025 (R8024) or Rsense SHORT
Vsense: 17.5 mV, Range: 0.6 A
EADC1: CH1

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	6	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5519,C5529,C5539,C5549,C5589,C5599		LOADRC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5579		DDRRC:NO

BOM_COST_GROUP=SENSORS

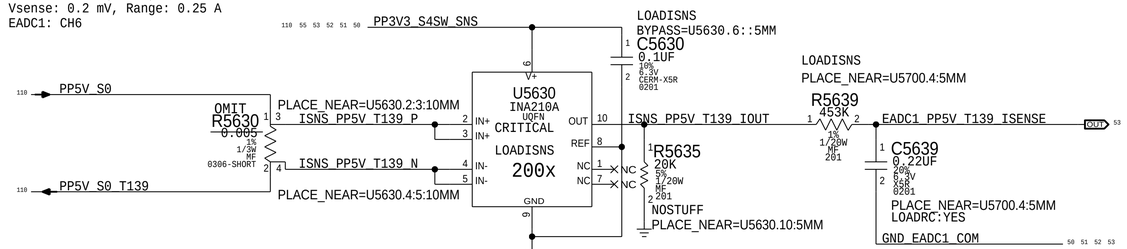
PAGE TITLE: Power Sensors: Load Side

Apple Inc.

DRAWING NUMBER: 051-00789
SIZE: D
REVISION: PROTO1A
BRANCH: dvt-fab10
PAGE: 55 OF 145
SHEET: 51 OF 121

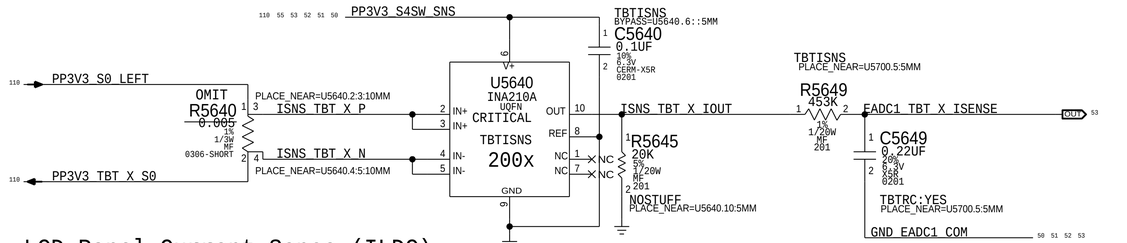
T139 5V Current Sense (IF5C)

Gain: 200x, EDP: 0.004 A
Rsense: 0.05 (R5630) or Rsense SHORT
Vsense: 0.2 mV, Range: 0.25 A
EADC1: CH6



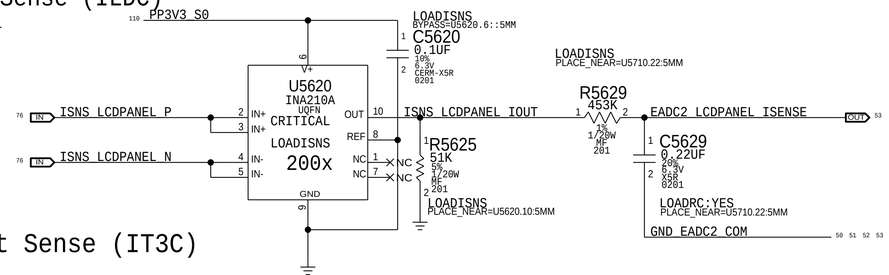
Thunderbolt TBT LEFT Current Sense (IULC)

Gain: 200x. EDP: 0.5 A
Rsense: 0.025 (R5640) or Rsense SHORT
Vsense: 12.5 mV, Range: 0.5 A
EADC1: CH7



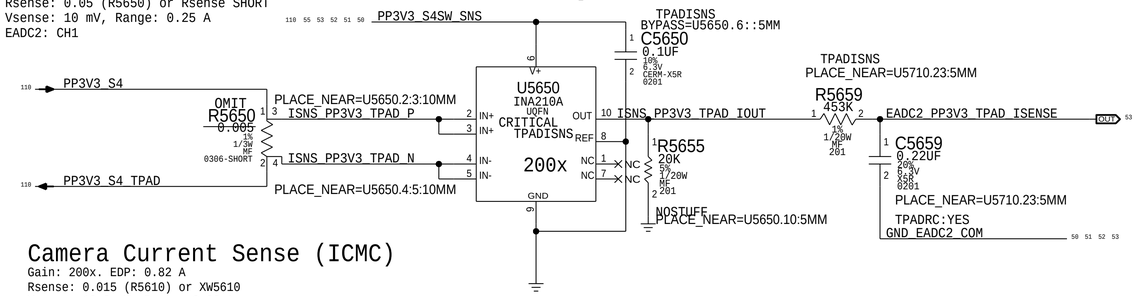
LCD Panel Current Sense (ILDC)

Gain: 200x. EDP: 1 A
RSENSE: 0.01 (R8520) or Rsense SHORT
Vsense: 5 mV, Range: 1.25 A
EADC2: CH0



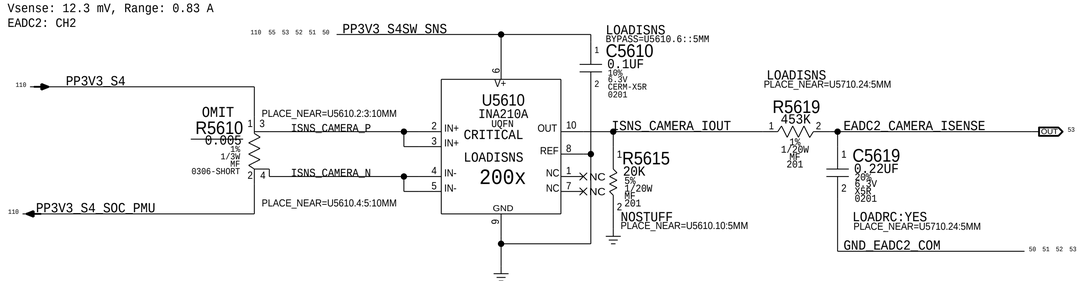
Trackpad 3V Current Sense (IT3C)

Gain: 200x, EDP: 0.2 A
Rsense: 0.05 (R5650) or Rsense SHORT
Vsense: 10 mV, Range: 0.25 A
EADC2: CH1

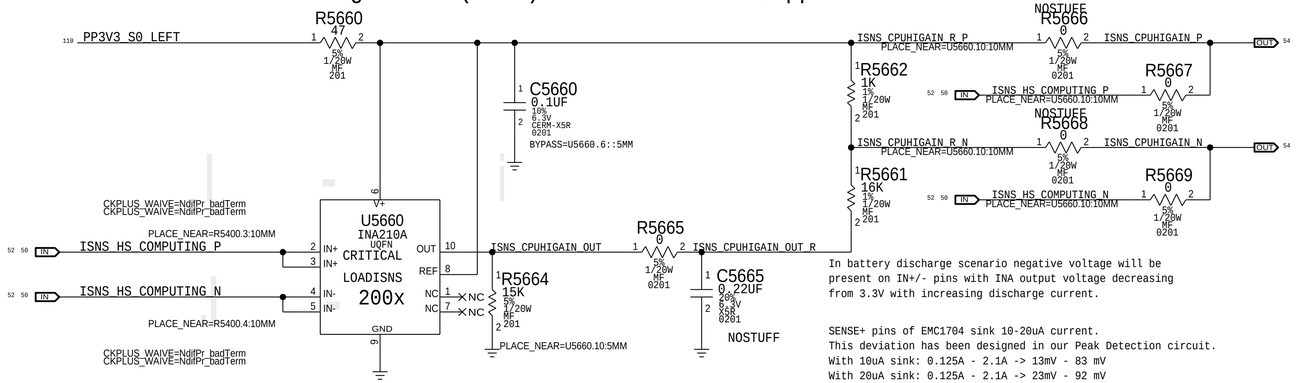


Camera Current Sense (ICMC)

Gain: 200x. EDP: 0.82 A
Rsense: 0.015 (R5610) or XW5610
Vsense: 12.3 mV, Range: 0.83 A
EADC2: CH2



CPU High Side (IC0R) Peak Detection Support

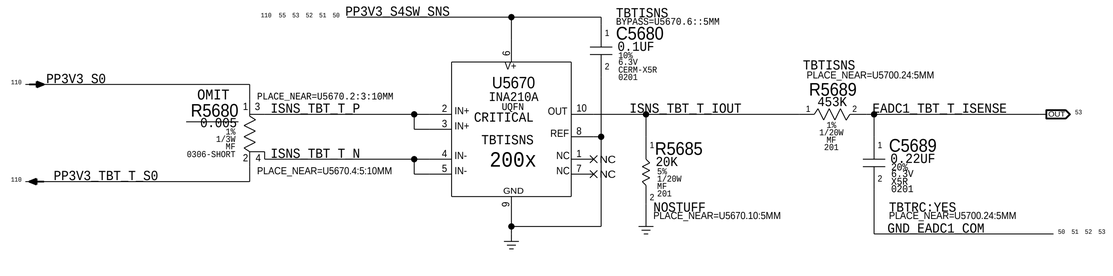


In battery discharge scenario negative voltage will be present on IN+/- pins with INA output voltage decreasing from 3.3V with increasing discharge current.

SENSE+ pins of EMC1704 sink 10-20uA current.
This deviation has been designed in our Peak Detection circuit.
With 10uA sink: 0.125A - 2.1A -> 13mV - 83 mV
With 20uA sink: 0.125A - 2.1A -> 23mV - 92 mV

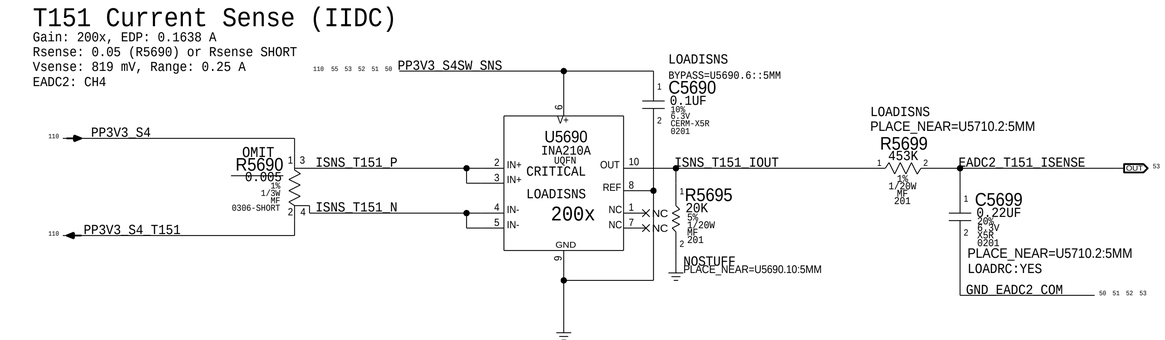
Thunderbolt TBT RIGHT Current Sense (IURC)

Gain: 200x. EDP: 0.5 A
Rsense: 0.025 (R5680) or Rsense SHORT
Vsense: 12.5 mV, Range: 0.5 A
EADC1: CH2



T151 Current Sense (IIDC)

Gain: 200x, EDP: 0.1638 A
Rsense: 0.05 (R5690) or Rsense SHORT
Vsense: 819 mV, Range: 0.25 A
EADC2: CH4



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	4	RES,MTL FILM,100K,1/16W,0201,SMD,LF	C5619,C5629,C5639,C5699		LOADRC:NO
117S0008	2	RES,MTL FILM,100K,1/16W,0201,SMD,LF	C5649,C5689		TBTRC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5659		TPADRC:NO

BOM_COST_GROUP=SENSORS

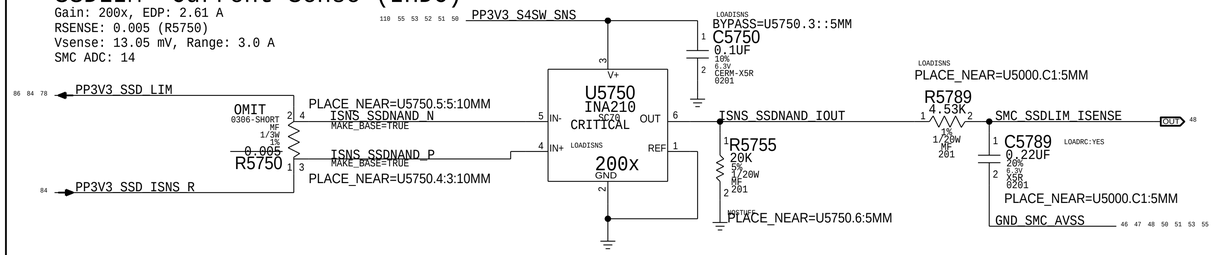
PAGE TITLE: Power Sensors: Extended

Apple Inc.

DRAWING NUMBER: 051-00789
SIZE: D
REVISION: PROTO1A
BRANCH: dvt-fab10
PAGE: 56 OF 145
SHEET: 52 OF 121

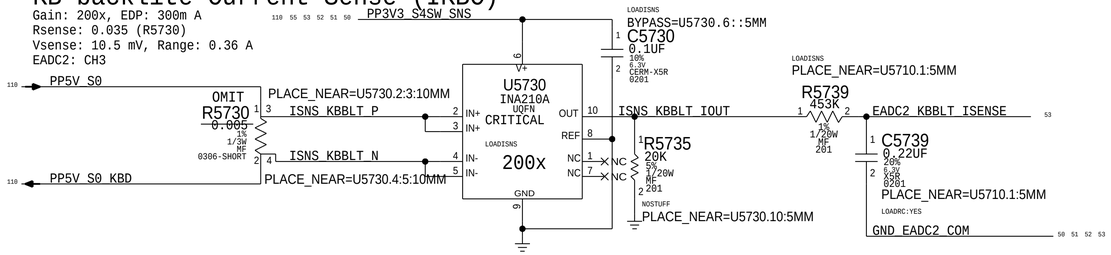
SSDLIM Current Sense (IHDC)

Gain: 200x, EDP: 2.61 A
RSENSE: 0.005 (R5750)
Vsense: 13.05 mV, Range: 3.0 A
SMC ADC: 14



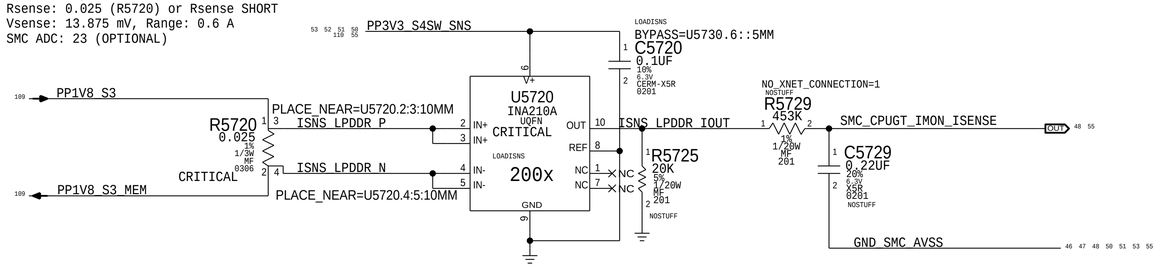
KB backlite Current Sense (IKBC)

Gain: 200x, EDP: 300m A
Rsense: 0.035 (R5730)
Vsense: 10.5 mV, Range: 0.36 A
EADC2: CH3



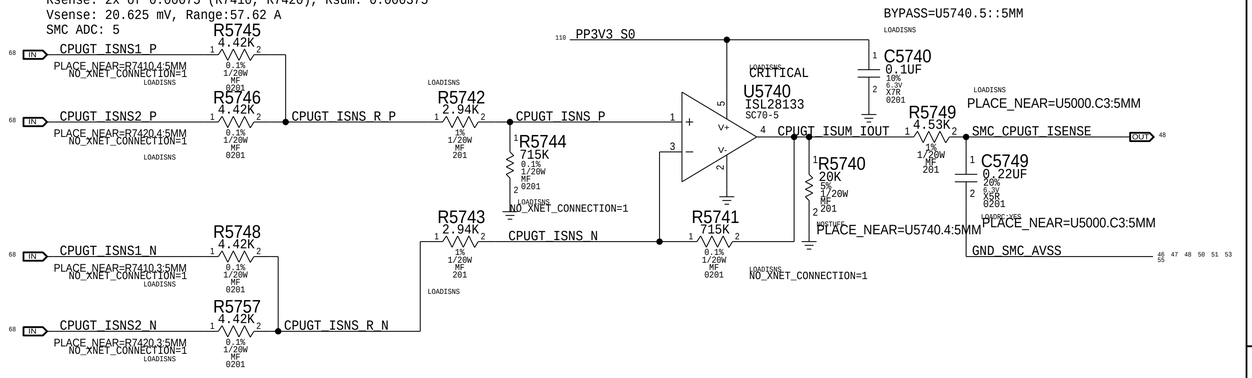
LPDDR 1.8V Current Sense (IM1C)

Gain: 200x, EDP: 0.555 A
Rsense: 0.025 (R5720) or Rsense SHORT
Vsense: 13.875 mV, Range: 0.6 A
SMC ADC: 23 (OPTIONAL)



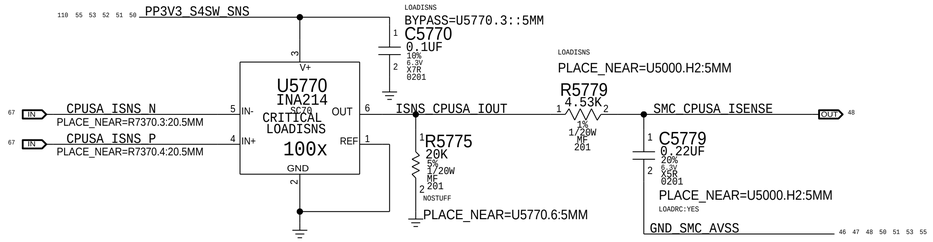
CPU GT Current Sense (ICTC)

Gain: 202.93x, EDP: 55 A
Rsense: 2x of 0.00075 (R7410, R7420), Rsum: 0.000375
Vsense: 20.625 mV, Range:57.62 A
SMC ADC: 5



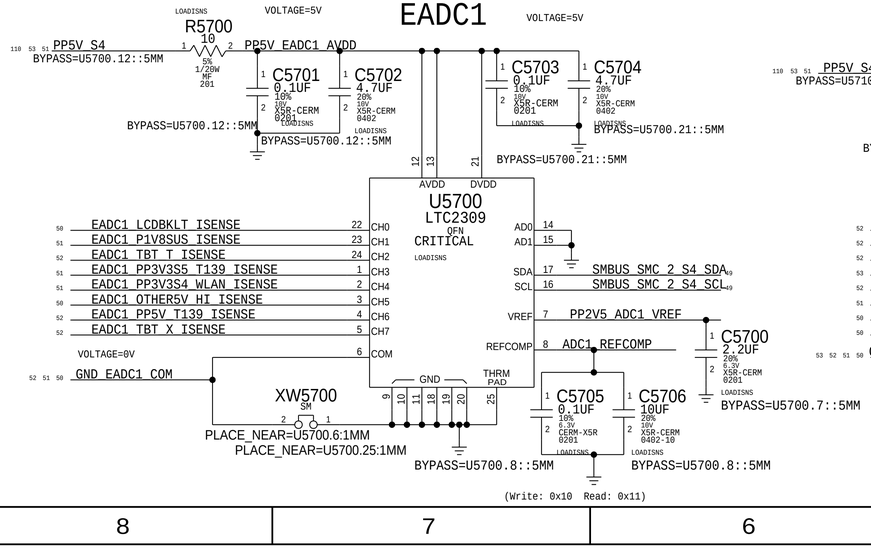
CPU SA Current Sense (ICSC)

Gain: 200x, EDP: 8 A
Rsense: 0.002 (R7570)
Vsense: 16 mV, Range: 7.5 A
SMC ADC: 17



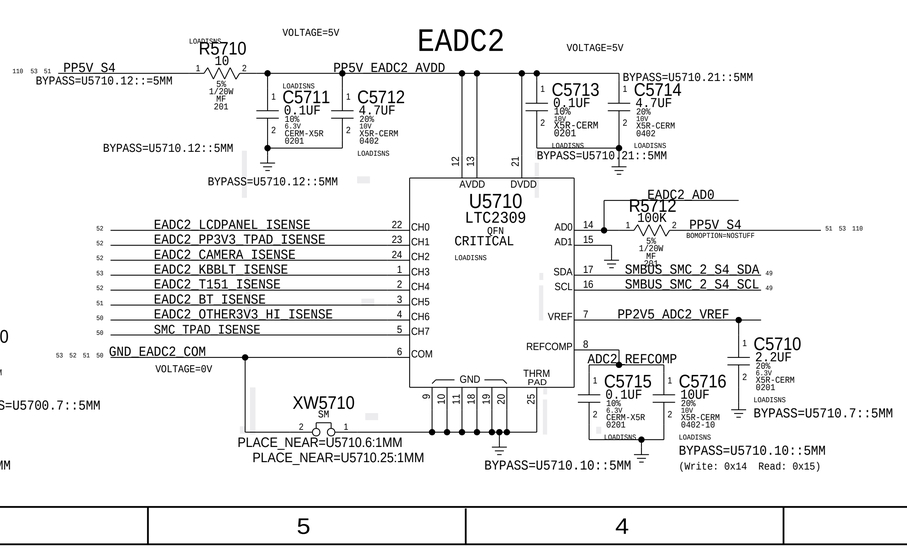
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	4	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5739,C5749,C5779,C5789		LOADRC:NO

EADC1



(Write: 0x10 Read: 0x11)

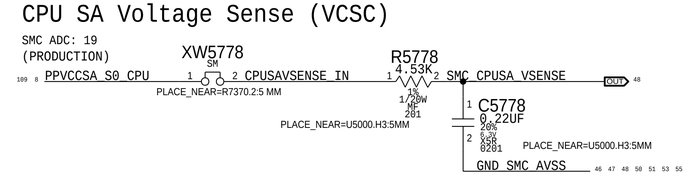
EADC2



(Write: 0x14 Read: 0x15)

CPU SA Voltage Sense (VCSC)

SMC ADC: 19
(PRODUCTION)



BOM_COST_GROUP=SENSORS

PAGE TITLE: Power Sensors: Extended 2

Apple Inc.

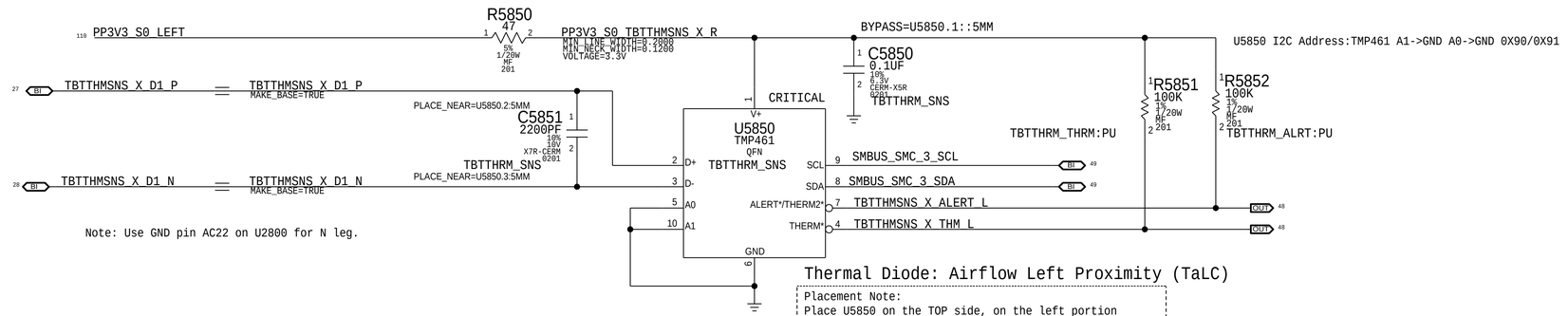
DRAWING NUMBER: 051-00789
SIZE: D
REVISION: PROTO1A
BRANCH: dvt-fab10
PAGE: 57 OF 145
SHEET: 53 OF 121

Thermal Sensor A:
Thunderbolt Die, Airflow Left

I2C Write: 0xD8, I2C Read: 0xD9

Thermal Diode: TBT Die (TTLD)

Placement Note:
The P leg connects to THERMDA pin of the TBT chip, the N leg connect to pin AC22.



Thermal Diode: Airflow Left Proximity (TaLC)

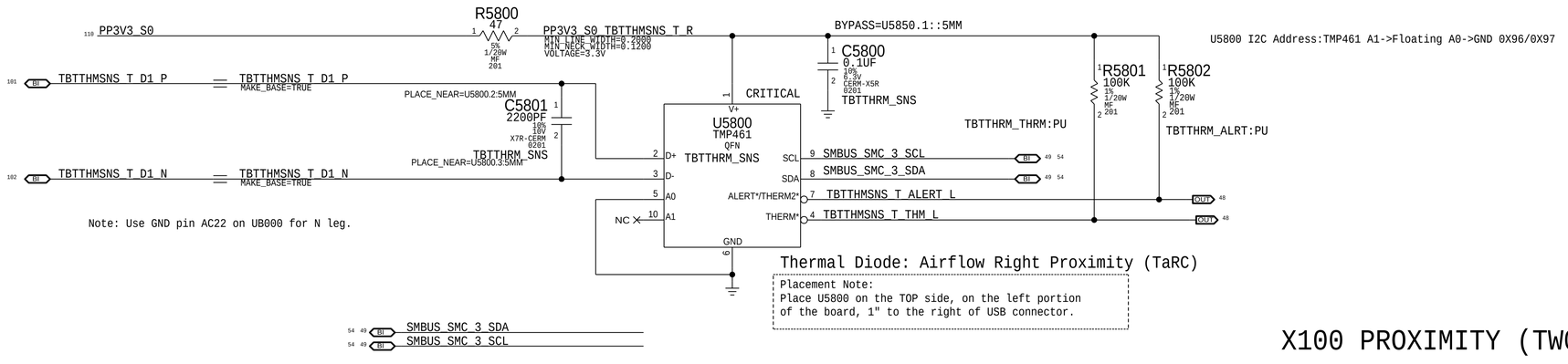
Placement Note:
Place U5850 on the TOP side, on the left portion of the board, 1" to the right of USB connector.

Thermal Sensor C:
Thunderbolt Die, Air Flow Right

I2C Write: 0x98, I2C Read: 0x99

Thermal Diode: TBT Die (TTRD)

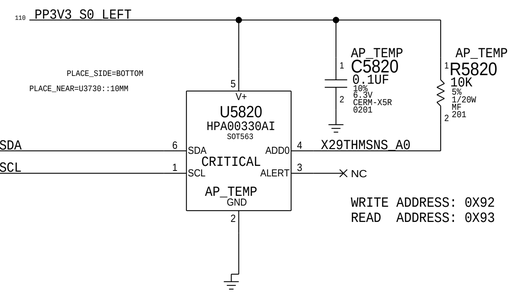
Placement Note:
The P leg connects to THERMDA pin of the TBT chip, the N leg connect to pin AC22.



Thermal Diode: Airflow Right Proximity (TaRC)

Placement Note:
Place U5800 on the TOP side, on the left portion of the board, 1" to the right of USB connector.

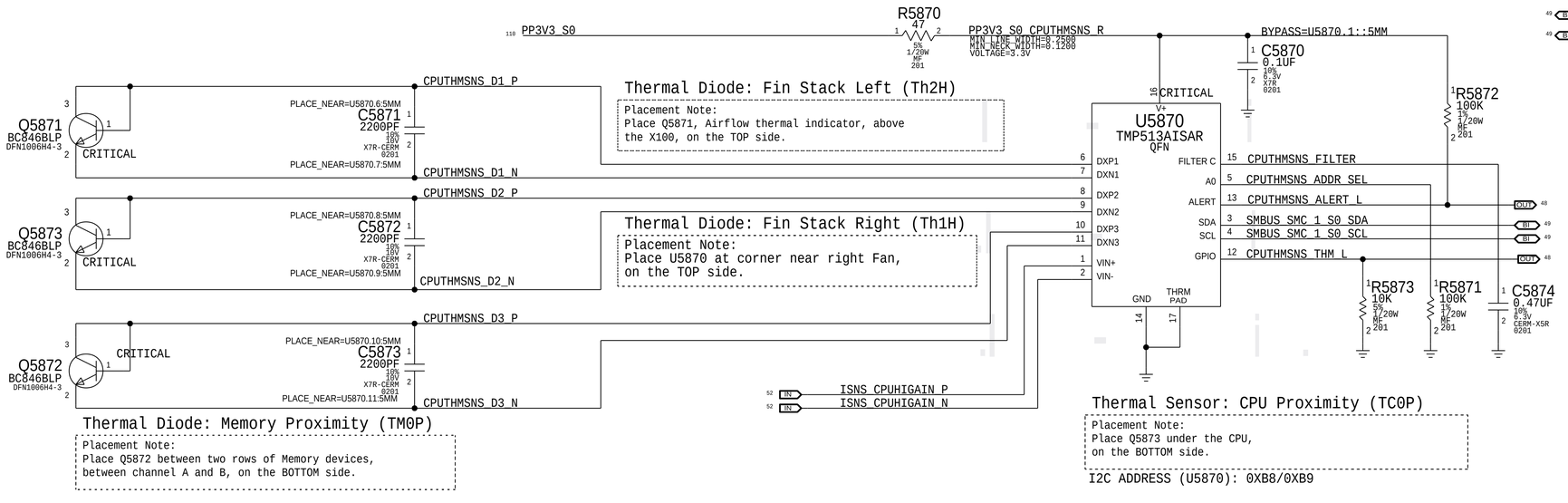
X100 PROXIMITY (TW0P)



Placement note:
PLACE U5820 ON BOTTOM NEAR X100

Thermal Sensor B & CPU High Peak Detection:
CPU Proximity, Memory Proximity, Fin Stack Left, Fin Stack Right

I2C Write: 0x98, I2C Read: 0x99



BOM_COST_GROUP=SENSORS

PAGE TITLE: Thermal Sensors

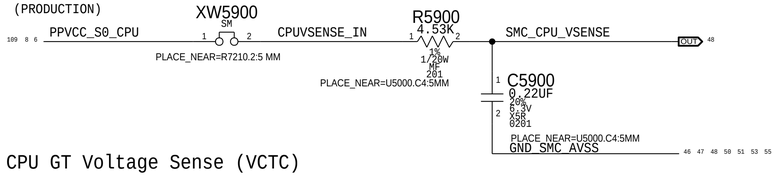
Apple Inc.

DRAWING NUMBER	051-00789
SIZE	D
REVISION	PROTO1A
BRANCH	dvt-fab10
PAGE	58 OF 145
SHEET	54 OF 121

SENSORS: EXTENDER 3

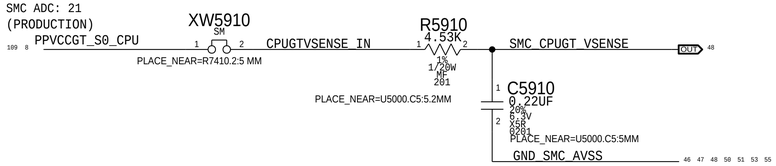
CPU Core Voltage Sense (VCAC)

SMC ADC: 20
(PRODUCTION)



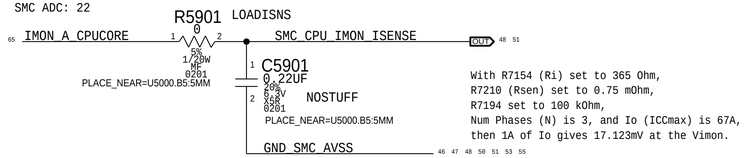
CPU GT Voltage Sense (VCTC)

SMC ADC: 21
(PRODUCTION)



CPU Core IMON Current Sense (ICAM)

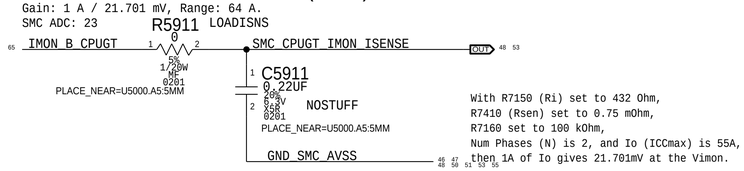
Gain: 1 A / 17.123 mV, Range: 67 A.
SMC ADC: 22



With R7154 (Ri) set to 365 Ohm,
R7210 (Rsen) set to 0.75 mOhm,
R7194 set to 100 kOhm,
Num Phases (N) is 3, and Io (ICCmax) is 67A,
then 1A of Io gives 17.123mV at the Vimon.

CPU GT IMON Current Sense (ICTM)

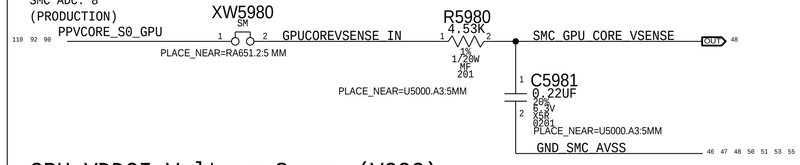
Gain: 1 A / 21.701 mV, Range: 64 A.
SMC ADC: 23



With R7150 (Ri) set to 432 Ohm,
R7410 (Rsen) set to 0.75 mOhm,
R7160 set to 100 kOhm,
Num Phases (N) is 2, and Io (ICCmax) is 55A,
then 1A of Io gives 21.701mV at the Vimon.

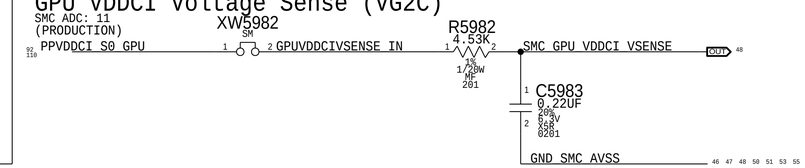
GPU CORE Voltage Sense (VG0C)

SMC ADC: 8
(PRODUCTION)



GPU VDDCI Voltage Sense (VG2C)

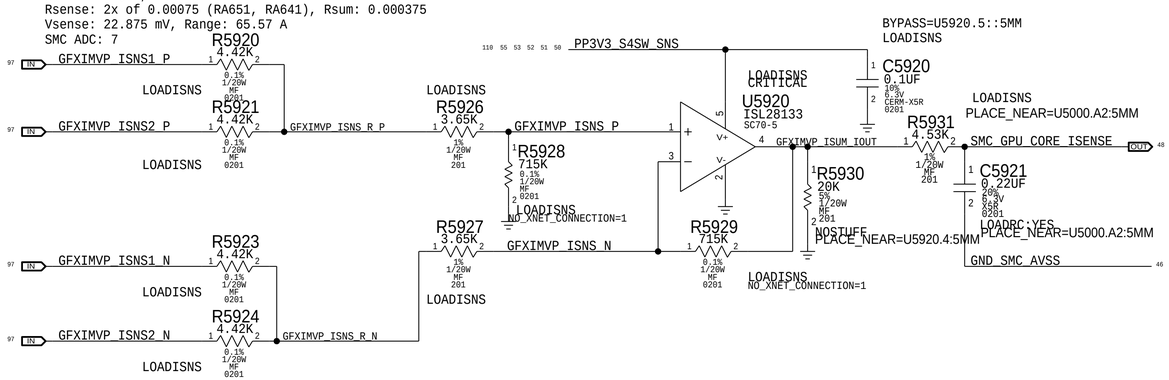
SMC ADC: 11
(PRODUCTION)



GPU SENSORS

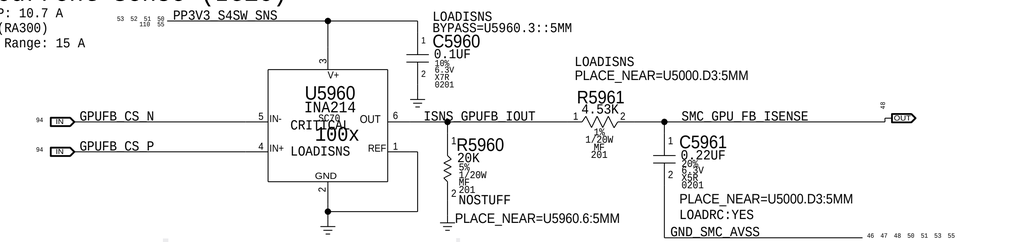
GPU CORE Current Sense (IG0C)

Gain: 122.01x, EDP: 64.2 A
Rsense: 2x of 0.00075 (RA651, RA641), Rsum: 0.000375
Vsense: 22.875 mV, Range: 65.57 A
SMC ADC: 7



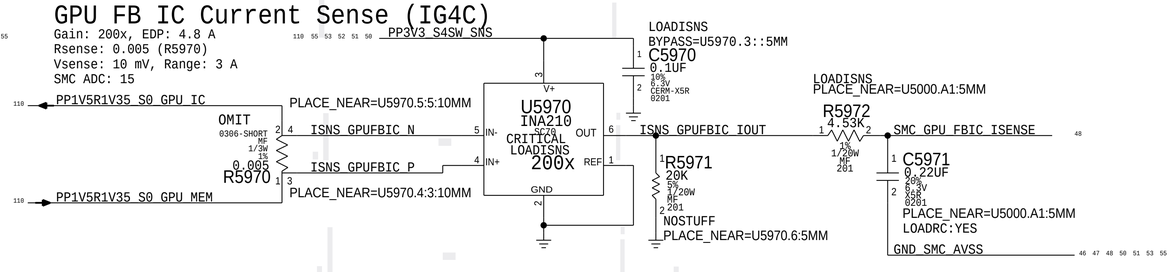
GPU FB Current Sense (IG1C)

Gain: 100x, EDP: 10.7 A
Rsense: 0.002 (RA300)
Vsense: 16 mV, Range: 15 A
SMC ADC: 13



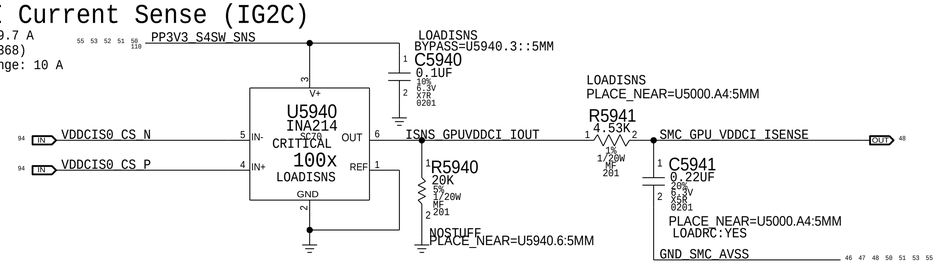
GPU FB IC Current Sense (IG4C)

Gain: 200x, EDP: 4.8 A
Rsense: 0.005 (R5970)
Vsense: 10 mV, Range: 3 A
SMC ADC: 15



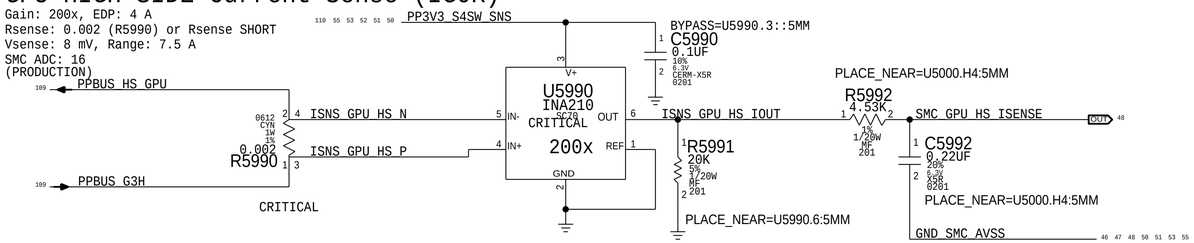
GPU VDDCI Current Sense (IG2C)

Gain: 100x, EDP: 9.7 A
Rsense: 0.003 (RA368)
Vsense: 24 mV, Range: 10 A
SMC ADC: 10



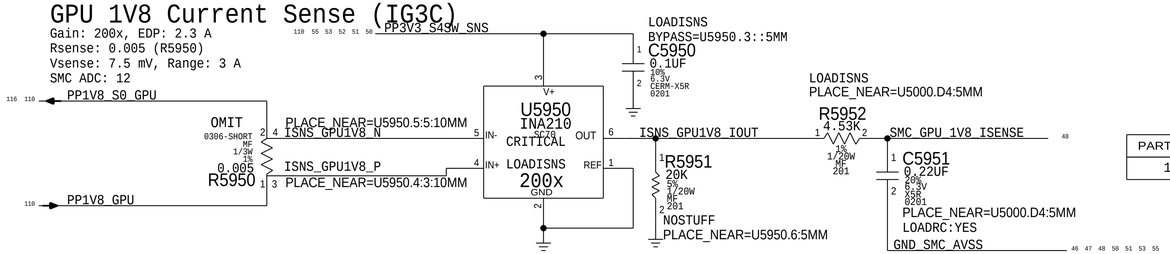
GPU HIGH SIDE Current Sense (IG0R)

Gain: 200x, EDP: 4 A
Rsense: 0.002 (R5990) or Rsense SHORT
Vsense: 8 mV, Range: 7.5 A
SMC ADC: 16
(PRODUCTION)



GPU 1V8 Current Sense (IG3C)

Gain: 200x, EDP: 2.3 A
Rsense: 0.005 (R5950)
Vsense: 7.5 mV, Range: 3 A
SMC ADC: 12



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	5	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5921,C5941,C5951,C5961,C5971		LOADRC:NO

BOM_COST_GROUP=SENSORS

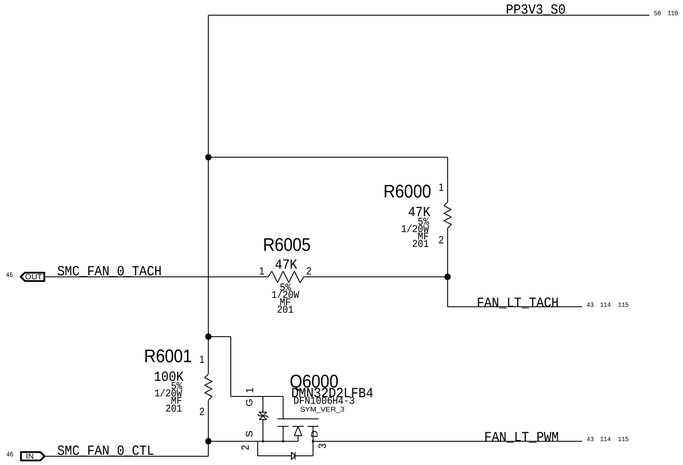
PAGE TITLE
Sensor Extended 3

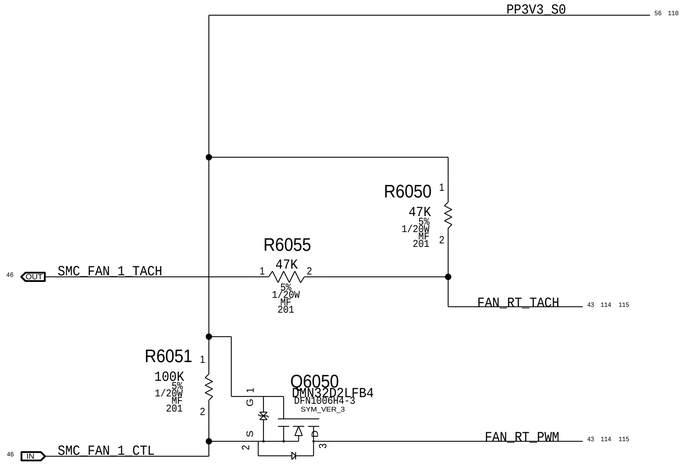
Apple Inc.

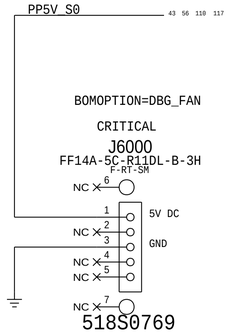
DRAWING NUMBER 051-00789
SIZE D
REVISION PROTO1A
BRANCH dvt-fab10
PAGE 59 OF 145
SHEET 55 OF 121

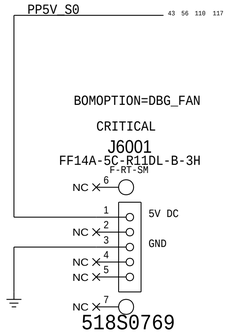
FAN CONNECTOR

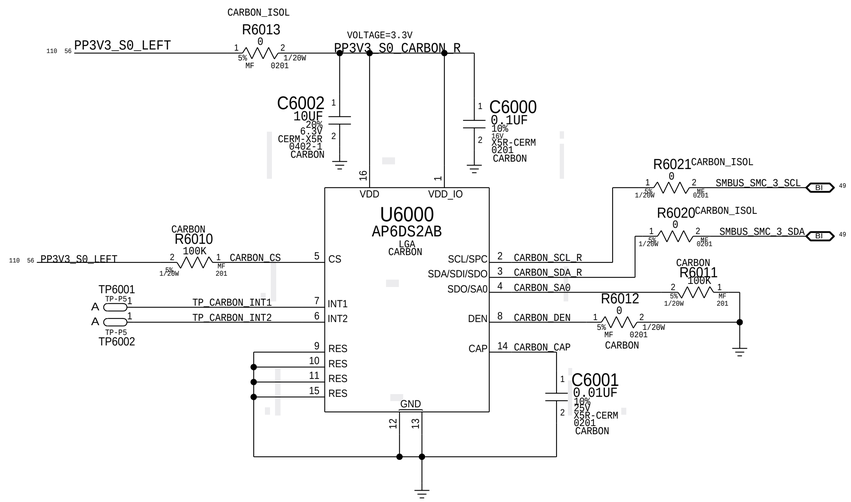
KEEP THE 5 PIN CONNECTOR FROM D1







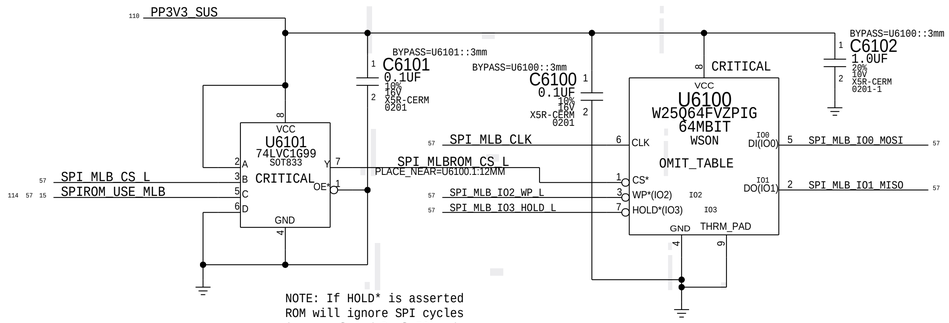




BOM_COST_GROUP=FAN

SPI ROM

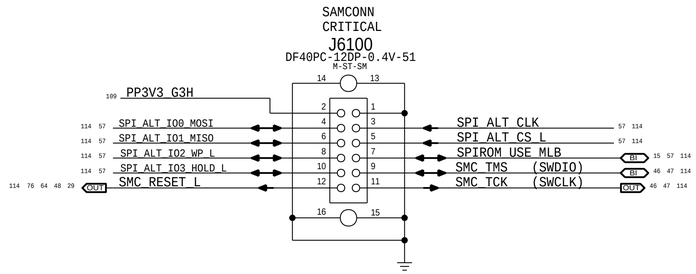
Quad-IO Mode (Mode 0 & 3) supported.
SPI Frequency: 50MHz for CPU, 20MHz for SMC.



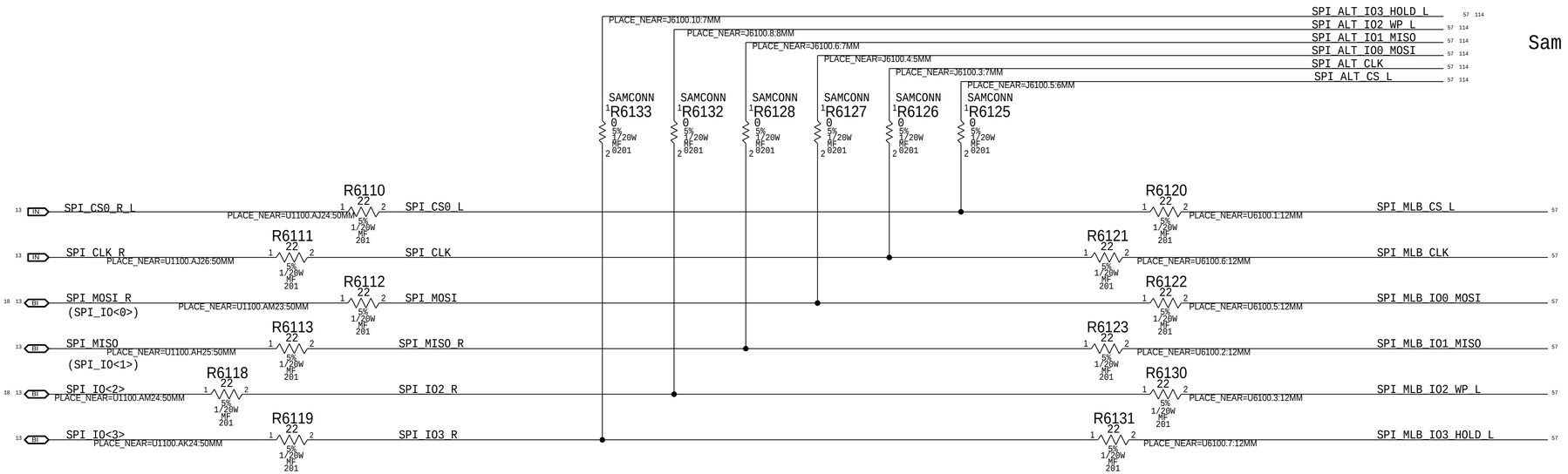
NOTE: If HOLD* is asserted
ROM will ignore SPI cycles
in normal and Dual-IO modes.

Quad SPI and QPI instructions require the non-volatile Quad Enable bit (QE)
in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and /HOLD pin becomes IO3.

SPI+SWD SAM Connector



SPI Bus Series Termination (Modified per PDG)



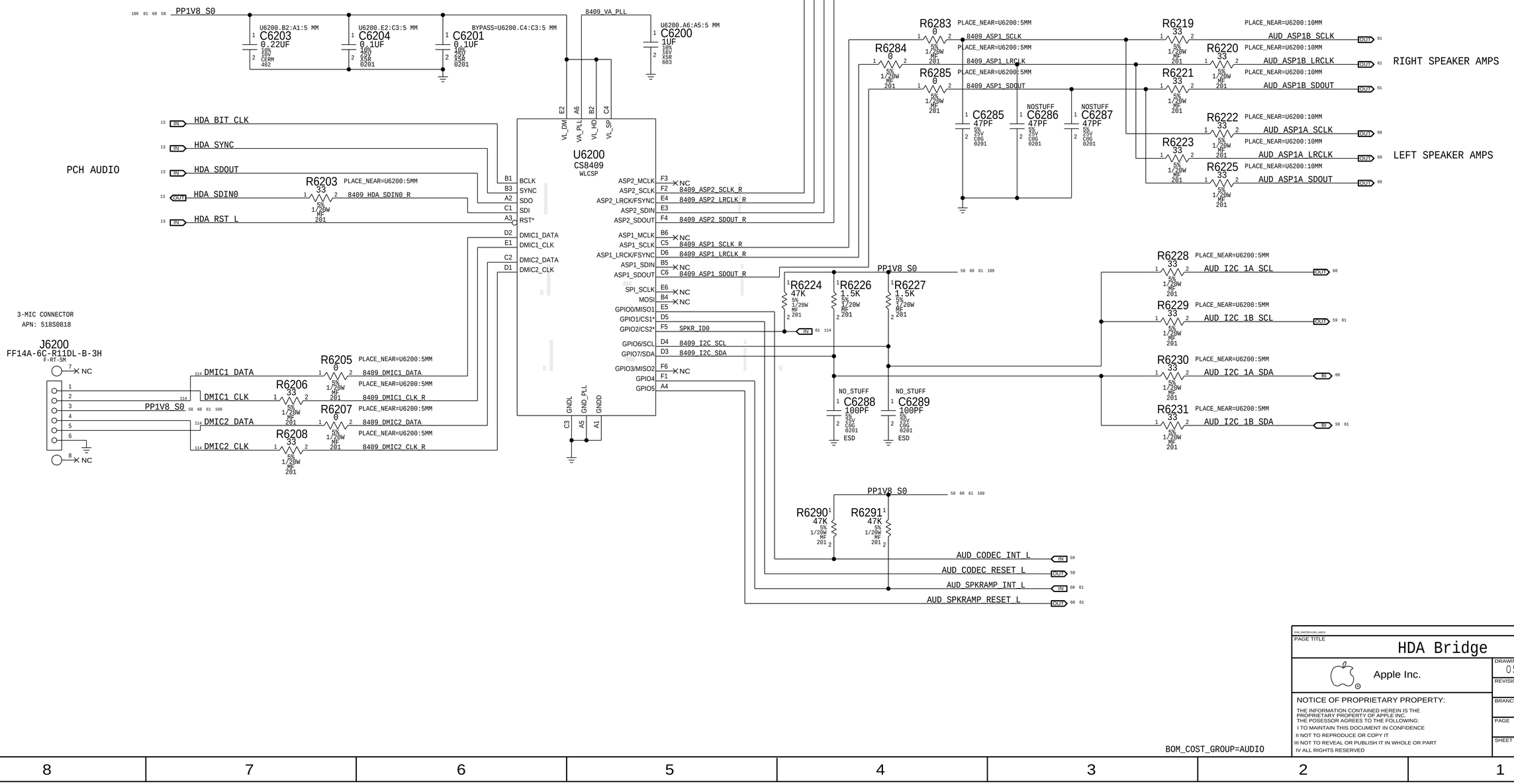
BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE: SPI Debug Connector

Apple Inc.

DRAWING NUMBER: 051-00789 SIZE: D
REVISION: PROTO1A
BRANCH: dvt-fab10
PAGE: 61 OF 145
SHEET: 57 OF 121



PAGE TITLE	HDA Bridge
Apple Inc.	DRAWING NUMBER 051-00789 SIZE D
	REVISION PROTO1A
	BRANCH dvt-fab10
	PAGE 62 OF 145
	SHEET 58 OF 121

AUDIO JACK CODEC I2C ADDRESS

AD1	AD0	ADDRESS
GND	GND	0x48 <--
GND	1.8V	0x49
1.8V	GND	0x4A
1.8V	1.8V	0x4B

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0719	2	CAP,CER,4.7UF,20%,10V,X5R,0402,MURATA	C6305,C6306	CRITICAL	

BOM_COST_GROUP=AUDIO

PAGE TITLE

AUDIO JACK CODEC

Apple Inc.

DRAWING NUMBER 051-00789 SIZE D

REVISION PROTO1A

BRANCH dvt-fab10

2X MONO SPEAKER AMPLIFIER
APN: 353S00604
0dBFS = 9VPK

VREF_AMP_WL
BYPASS=U6400.E4:C4:5 MM
C6400 1.0UF 20% 10V X5R-CERM 0201-1
BYPASS=U6400.A2:C2:10 MM
BYPASS=U6400.E2:C2:10 MM
BYPASS=U6400.A3:B3:5 MM
BYPASS=U6400.E3:D3:5 MM
PPBUS_G3H 60 61 109
C6401 0.1UF 10% 16V X7R-CERM 0402
C6402 0.1UF 10% 16V X7R-CERM 0402
C6403 10UF 20% 35V X5R-CERM 0603
C6404 10UF 20% 35V X5R-CERM 0603
C6480 100UF 20% 20V POLY SM-1
C6481 100UF 20% 20V POLY SM-1
PP1V8_S0 109 61 60 58
BYPASS=U6400.A4:B4:5 MM
C6405 1.0UF 20% 10V X5R-CERM 0201-1

U6400 MAX98706 WLP CRITICAL
DVDD A4
VREFC E4
PVDD A2 E2 A3 E3
IRQ* D5
SCL A6
SDA B6
RESET* E5
BCLK E6
LRCLK C6
DIN D6
DOUT C5
NC
AGND C4 D4
DGND B4 B3
PGND C1 C2 C3 D3
OUTPSNS E1
OUTP D1 D2
OUTN B1 B2
OUTNSNS A1
ADDR0 B5
ADDR1 A5

AUD_SPKRAMP_INT_L 61 58 OUT
AUD_SPKRAMP_RESET_L 61 58 IN
R6401 100K 5% 1/20W MF 201
AUD_I2C_1A_SCL 60 58 IN
AUD_I2C_1A_SDA 60 58 BI
PP1V8_S0 58 60 61 109
I2C ADDRESS = 0x31

PLACE_NEAR=U6400:5MM
AUD_ASP1A_SCLK 58 60 IN
R6402 0 5% 1/20W MF 201
SPKRAMP_WL_SCLK
PLACE_NEAR=U6400:5MM
AUD_ASP1A_LRCLK 58 60 IN
R6403 0 5% 1/20W MF 201
SPKRAMP_WL_LRCLK
PLACE_NEAR=U6400:5MM
AUD_ASP1A_SDOUT 58 60 IN
R6405 0 5% 1/20W MF 201
SPKRAMP_WL_SDIN

SPKRAMP_WL_OUT_POS
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
L6400 180OHM-3.4A 0806
SPKRCONN_WL_OUT_POS 114
SPKRAMP_WL_OUT_NEG
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
L6401 180OHM-3.4A 0806
SPKRCONN_WL_OUT_NEG 114
C6406 220PF 5% 25V C0G-CERM 0402
C6407 220PF 5% 25V C0G-CERM 0402

APN: 518S00521
J6410 78171-0004 M-RT-SM
LEFT SPEAKER CONNECTOR

VREF_AMP_TL
BYPASS=U6450.E4:C4:5 MM
C6450 1.0UF 20% 10V X5R-CERM 0201-1
BYPASS=U6450.A2:C2:10 MM
BYPASS=U6450.E2:C2:10 MM
BYPASS=U6450.A3:B3:5 MM
BYPASS=U6450.E3:D3:5 MM
PPBUS_G3H 60 61 109
C6451 0.1UF 10% 16V X7R-CERM 0402
C6452 0.1UF 10% 16V X7R-CERM 0402
C6453 10UF 20% 35V X5R-CERM 0603
C6454 10UF 20% 35V X5R-CERM 0603
PP1V8_S0 109 61 60 58
BYPASS=U6450.A4:B4:5 MM
C6455 1.0UF 20% 10V X5R-CERM 0201-1

U6450 MAX98706 WLP CRITICAL
DVDD A4
VREFC E4
PVDD A2 E2 A3 E3
IRQ* D5
SCL A6
SDA B6
RESET* E5
BCLK E6
LRCLK C6
DIN D6
DOUT C5
NC
AGND C4 D4
DGND B4 B3
PGND C1 C2 C3 D3
OUTPSNS E1
OUTP D1 D2
OUTN B1 B2
OUTNSNS A1
ADDR0 B5
ADDR1 A5

AUD_I2C_1A_SCL 60 58 IN
AUD_I2C_1A_SDA 60 58 BI
I2C ADDRESS = 0x32

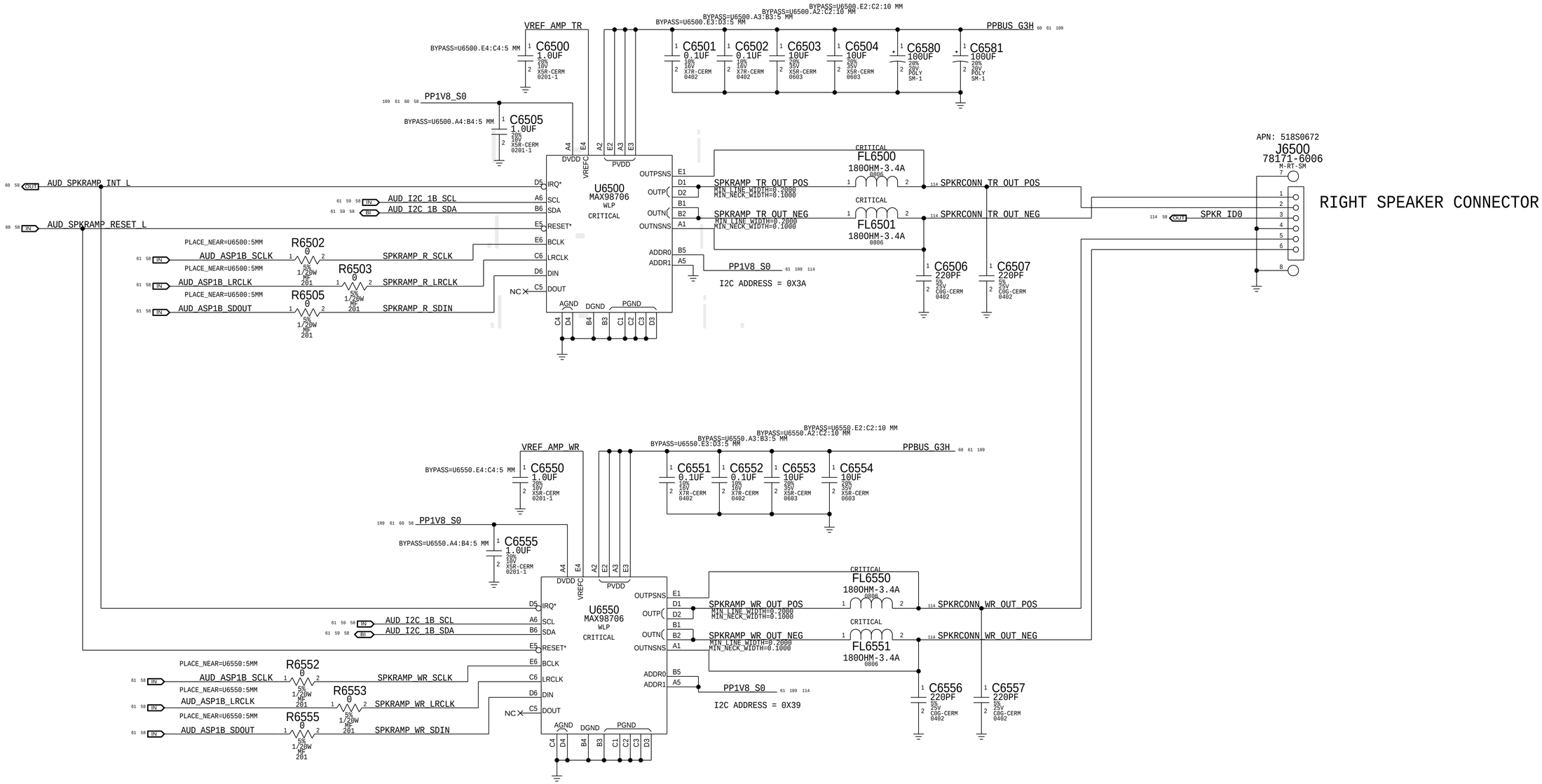
PLACE_NEAR=U6450:5MM
AUD_ASP1A_SCLK 58 60 IN
R6452 0 5% 1/20W MF 201
SPKRAMP_TL_SCLK
PLACE_NEAR=U6450:5MM
AUD_ASP1A_LRCLK 58 60 IN
R6453 0 5% 1/20W MF 201
SPKRAMP_TL_LRCLK
PLACE_NEAR=U6450:5MM
AUD_ASP1A_SDOUT 58 60 IN
R6455 0 5% 1/20W MF 201
SPKRAMP_TL_SDIN

SPKRAMP_TL_OUT_POS
L6450 180OHM-3.4A 0806
SPKRCONN_TL_OUT_POS 114
SPKRAMP_TL_OUT_NEG
L6451 180OHM-3.4A 0806
SPKRCONN_TL_OUT_NEG 114
C6456 220PF 5% 25V C0G-CERM 0402
C6457 220PF 5% 25V C0G-CERM 0402

BOM_COST_GROUP=AUDIO

PAGE TITLE
AUDIO Speaker Amps & Conn
Apple Inc.
DRAWING NUMBER 051-00789
SIZE D
REVISION PROTO1A
BRANCH dvt-fab10
PAGE 64 OF 145
SHEET 60 OF 121

2X MONO SPEAKER AMPLIFIER
APN: 353S00604
0dBFS = 9VPK

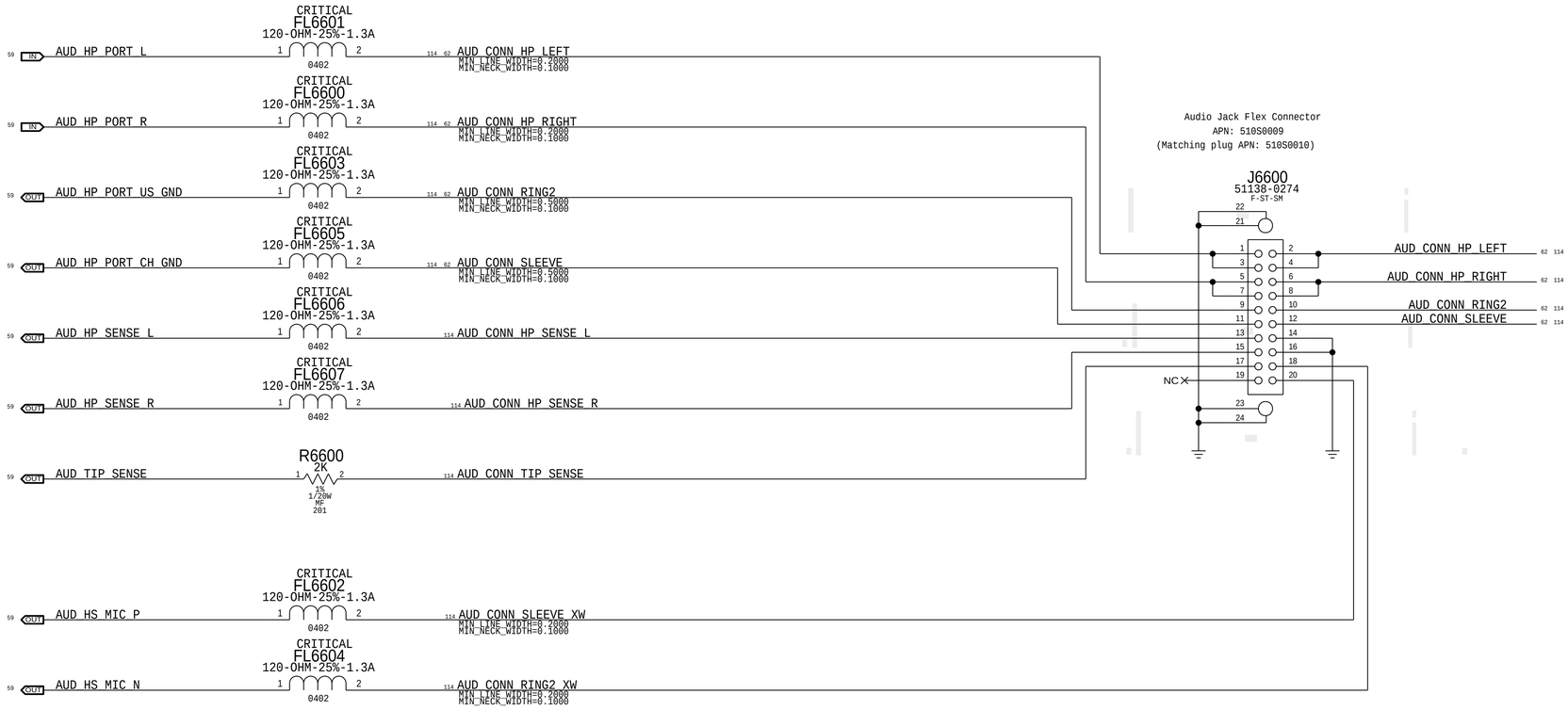


BOM_COST_GROUP=AUDIO

PAGE TITLE: AUDIO Speaker Amps & Conn

Apple Inc.

DRAWING NUMBER: 051-00789
SIZE: D
REVISION: PROTO1A
BRANCH: dvt-fab10
PAGE: 65 OF 145
SHEET: 61 OF 121



BOM_COST_GROUP=AUDIO

PAGE TITLE

AUDIO JACK CONNECTOR

Apple Inc.

DRAWING NUMBER 051-00789

SIZE D

REVISION PROTO1A

BRANCH dvt-fab10

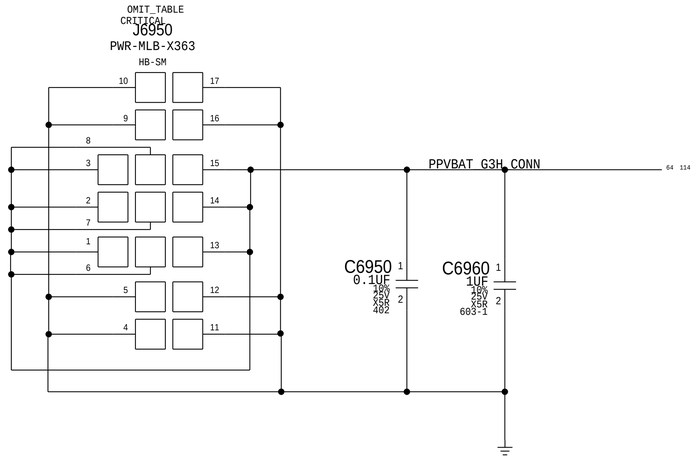
PAGE 66 OF 145

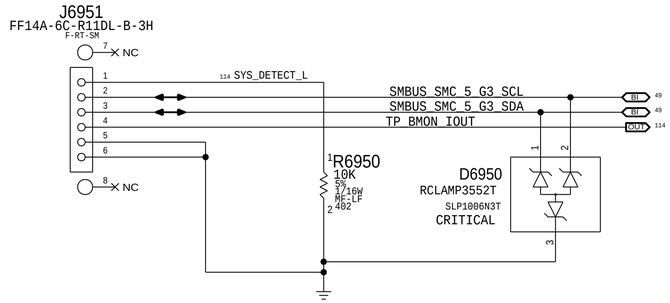
SHEET 62 OF 121

J80 Battery Hotbar Flex Pads 998-03902

Flex Pad TO MLB 998-03780.

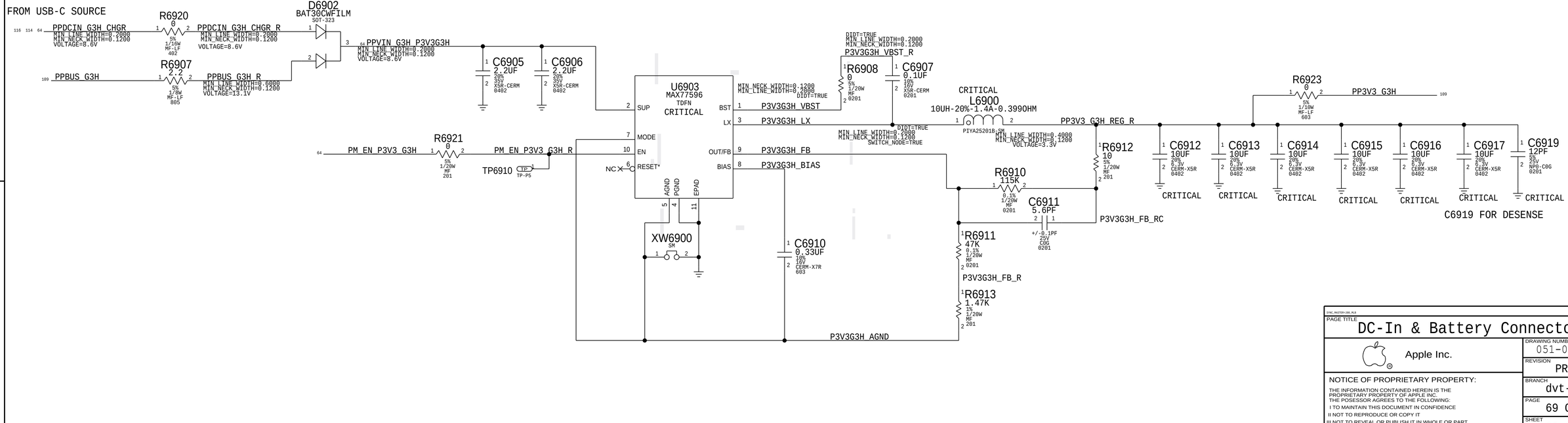
APN:518S0818





BMU POWER FLEX HOTBAR'd TO THE MLB:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
632-00862	1	PCBA,FLEX,BMU PWR,X363	J6950	CRITICAL	



PAGE TITLE

DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER 051-00789

SIZE D

REVISION PROTO1A

BRANCH dvt-fab10

PAGE 69 OF 145

SHEET 63 OF 121

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S00199	1	IND,MLD,2.7UH,16A,14.8MO,10.0x10.0x3.00	L7030	CRITICAL	

BOM_COST_GROUP=PLATFORM POWER

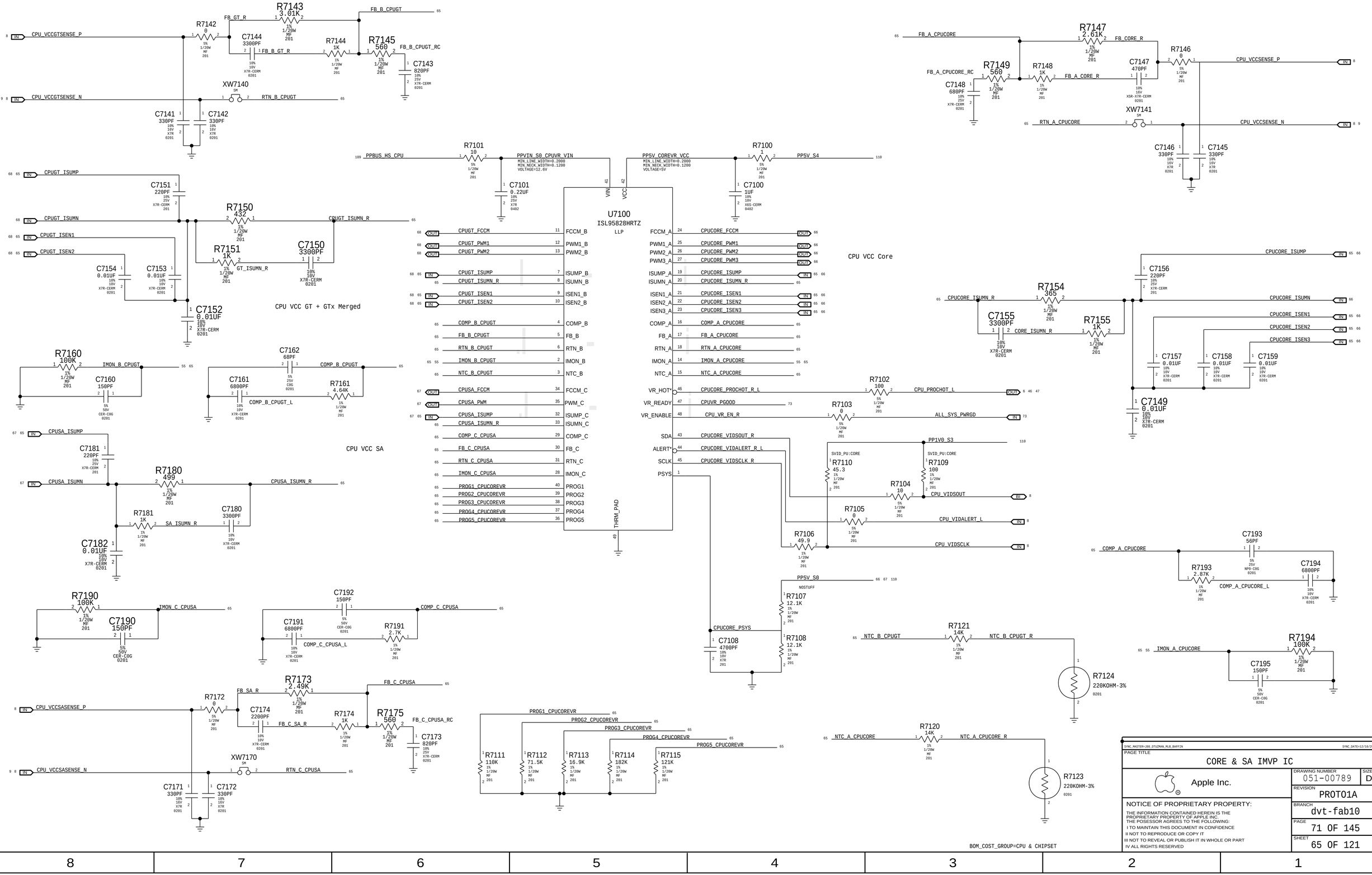
PAGE TITLE
PBUS Supply & Battery Charger

Apple Inc.

DRAWING NUMBER 051-00789 SIZE D

REVISION PROTO1A

BRANCH dvt-fab10


CPU_VCCGTSENSE_P
CPU_VCCGTSENSE_N
R7142 0
R7143 3.01K
R7144 1K
R7145 560
C7144 3300PF
C7143 820PF
XW7140
RTN_B_CPUGT
FB_GT_R
FB_B_CPUGT
FB_B_CPUGT_RC
C7141 330PF
C7142 330PF
CPUGT_ISUMP
CPUGT_ISUMN
CPUGT_ISEN1
CPUGT_ISEN2
C7151 220PF
R7150 432
R7151 1K
C7150 3300PF
C7154 0.01UF
C7153 0.01UF
C7152 0.01UF
CPUGT_ISUMN_R
GT_ISUMN_R
CPU VCC GT + GTx Merged
R7160 100K
C7160 150PF
IMON_B_CPUGT
C7162 68PF
C7161 6800PF
R7161 4.64K
COMP_B_CPUGT
COMP_B_CPUGT_L
CPUSA_ISUMP
CPUSA_ISUMN
C7181 220PF
R7180 499
R7181 1K
C7180 3300PF
C7182 0.01UF
SA_ISUMN_R
CPUSA_ISUMN_R
CPU VCC SA
R7190 100K
C7190 150PF
IMON_C_CPUSA
C7192 150PF
C7191 6800PF
R7191 2.7K
COMP_C_CPUSA
COMP_C_CPUSA_L
CPU_VCCSASENSE_P
CPU_VCCSASENSE_N
R7172 0
R7173 2.49K
R7174 1K
R7175 560
C7174 2200PF
C7173 820PF
XW7170
RTN_C_CPUSA
FB_SA_R
FB_C_CPUSA
FB_C_CPUSA_RC
FB_C_SA_R
C7171 330PF
C7172 330PF
PPBUS_HS_CPU
R7101 10
C7101 0.22UF
PPVIN_S0_CPUVR_VIN
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=12.6V
PP5V_COREVR_VCC
R7100 1
C7100 1UF
PP5V_S4
U7100
ISL95828HRTZ
LLP
VIN
VCC
THRM_PAD
FCCM_B
PWM1_B
PWM2_B
ISUMP_B
ISUMN_B
ISEN1_B
ISEN2_B
COMP_B
FB_B
RTN_B
IMON_B
NTC_B
FCCM_C
PWM_C
ISUMP_C
ISUMN_C
COMP_C
FB_C
RTN_C
IMON_C
PROG1
PROG2
PROG3
PROG4
PROG5
FCCM_A
PWM1_A
PWM2_A
PWM3_A
ISUMP_A
ISUMN_A
ISEN1_A
ISEN2_A
ISEN3_A
COMP_A
FB_A
RTN_A
IMON_A
NTC_A
VR_HOT*
VR_READY
VR_ENABLE
SDA
ALERT*
SCLK
PSYS
CPUCORE_FCCM
CPUCORE_PWM1
CPUCORE_PWM2
CPUCORE_PWM3
CPUCORE_ISUMP
CPUCORE_ISUMN_R
CPUCORE_ISEN1
CPUCORE_ISEN2
CPUCORE_ISEN3
COMP_A_CPUCORE
FB_A_CPUCORE
RTN_A_CPUCORE
IMON_A_CPUCORE
NTC_A_CPUCORE
CPUCORE_PROCHOT_R_L
CPU_VR_EN_R
CPUCORE_VIDSOUT_R
CPUCORE_VIDALERT_R_L
CPUCORE_VIDSCLK_R
CPU VCC Core
R7102 100
R7103 0
CPU_PROCHOT_L
ALL_SYS_PWRGD
PP1V0_S3
R7110 45.3
R7109 100
R7104 10
R7105 0
R7106 49.9
CPU_VIDSOUT
CPU_VIDALERT_L
CPU_VIDSCLK
SVID_PU:CORE
PP5V_S0
NOSTUFF
R7107 12.1K
R7108 12.1K
C7108 4700PF
CPUCORE_PSYS
R7111 110K
R7112 71.5K
R7113 16.9K
R7114 182K
R7115 121K
PROG1_CPUCOREVR
PROG2_CPUCOREVR
PROG3_CPUCOREVR
PROG4_CPUCOREVR
PROG5_CPUCOREVR
R7120 14K
R7123 220KOHM-3%
NTC_A_CPUCORE_R
R7121 14K
R7124 220KOHM-3%
NTC_B_CPUGT
NTC_B_CPUGT_R
FB_A_CPUCORE
R7147 2.61K
R7149 560
R7148 1K
C7147 470PF
C7148 680PF
R7146 0
FB_A_CPUCORE_RC
FB_A_CORE_R
FB_CORE_R
CPU_VCCSENSE_P
CPU_VCCSENSE_N
XW7141
RTN_A_CPUCORE
C7146 330PF
C7145 330PF
CPUCORE_ISUMP
CPUCORE_ISUMN_R
R7154 365
R7155 1K
C7155 3300PF
CORE_ISUMN_R
C7156 220PF
C7157 0.01UF
C7158 0.01UF
C7159 0.01UF
C7149 0.01UF
CPUCORE_ISUMN
CPUCORE_ISEN1
CPUCORE_ISEN2
CPUCORE_ISEN3
C7193 56PF
R7193 2.87K
C7194 6800PF
COMP_A_CPUCORE_L
R7194 100K
C7195 150PF
BOM_COST_GROUP=CPU & CHIPSET
SYNC_MASTER=J80_DTU2MAR_MLB_BAFFIN
SYNC_DATE=12/10/2015
PAGE TITLE
CORE & SA IMVP IC
Apple Inc.
DRAWING NUMBER 051-00789
SIZE D
REVISION PR0T01A
BRANCH dvt-fab10
PAGE 71 OF 145
SHEET 65 OF 121
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

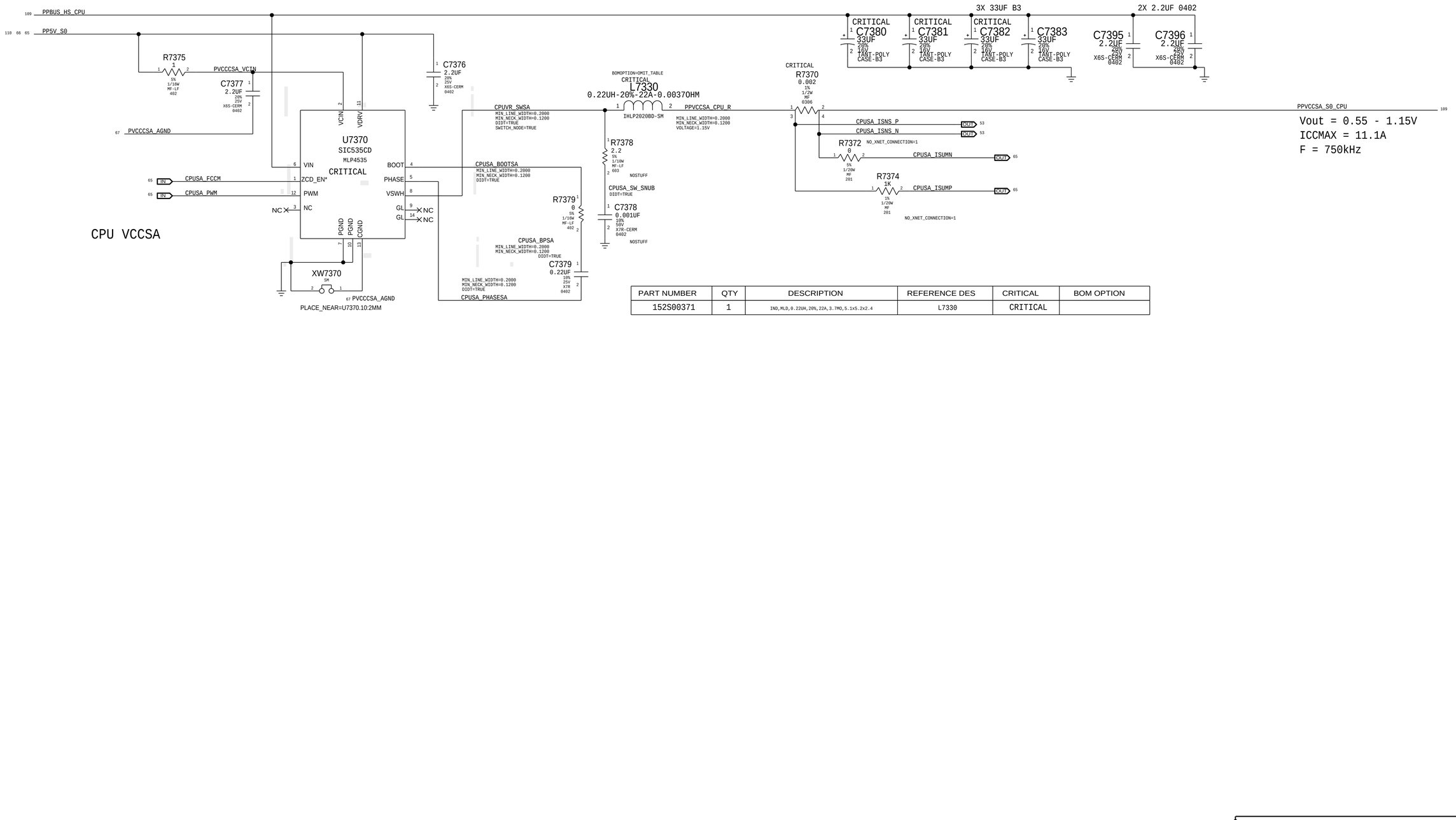
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00497	3	IC,SIC635,DRMOS,IMVP-8,40A,PQFN31,5X5	U7210,U7220,U7230	CRITICAL	

SYNC_MASTER=J80_DTUZMAN_MLB_BAFFIN
SYNC_DATE=09/03/2015

PAGE TITLE
CORE IMVP POWER BLOCK

Apple Inc.

DRAWING NUMBER 051-00789
SIZE D
REVISION PROTO1A
BRANCH dvt-fab10
PAGE 72 OF 145
SHEET 66 OF 121



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S00371	1	IND,MLD,0.22UH,20%,22A,3.7MO,5.1x5.2x2.4	L7330	CRITICAL	

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J80_DTUZMAN_MLB_BAFFIN SYNC_DATE=11/18/2015

PAGE TITLE

SA IMVP IC

Apple Inc.

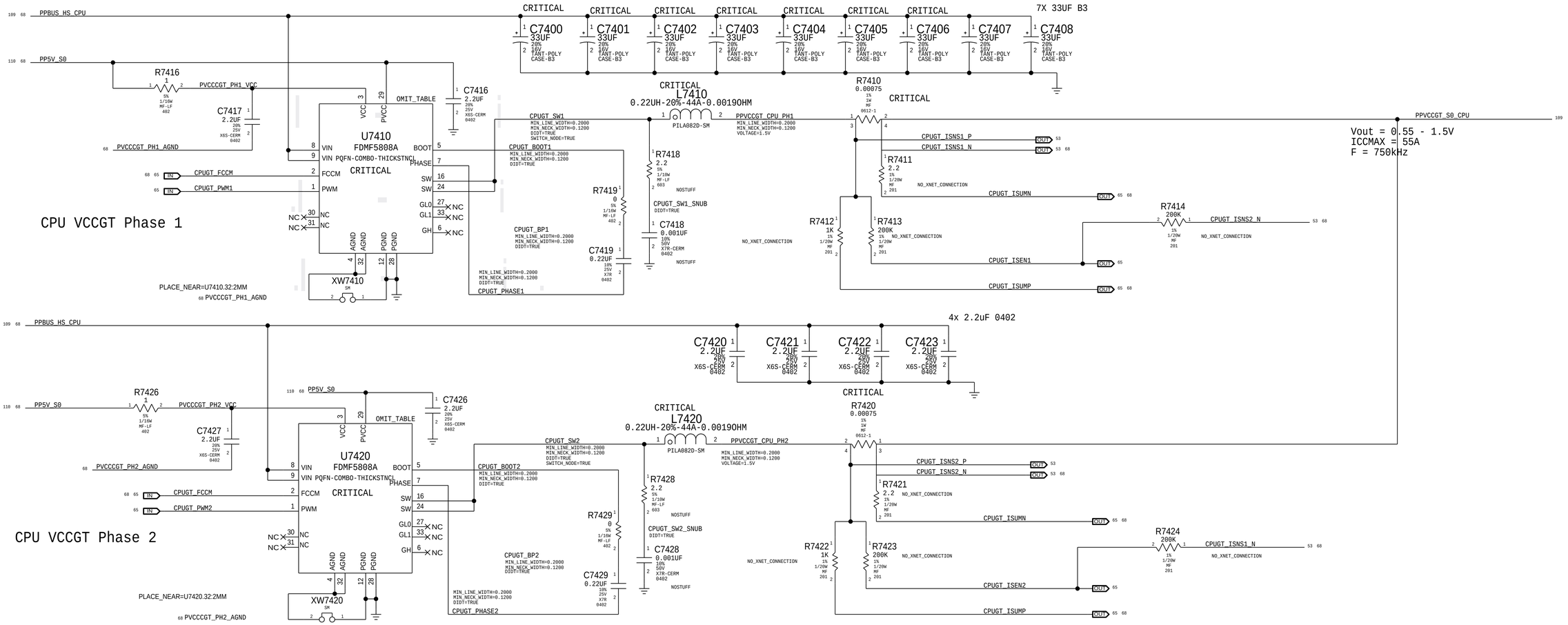
DRAWING NUMBER 051-00789 SIZE D

REVISION PROTO1A

BRANCH dvt-fab10

PAGE 73 OF 145

SHEET 67 OF 121



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00497	2	IC,SIC635,DRMOS,IMVP-8,40A,PQFN31,5X5	U7410,U7420	CRITICAL	

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J80_DTU2MAN_MLB_BAFFIN SYNC_DATE=09/03/2015

PAGE TITLE

GT & GTX IMVP POWER BLOCK

Apple Inc.

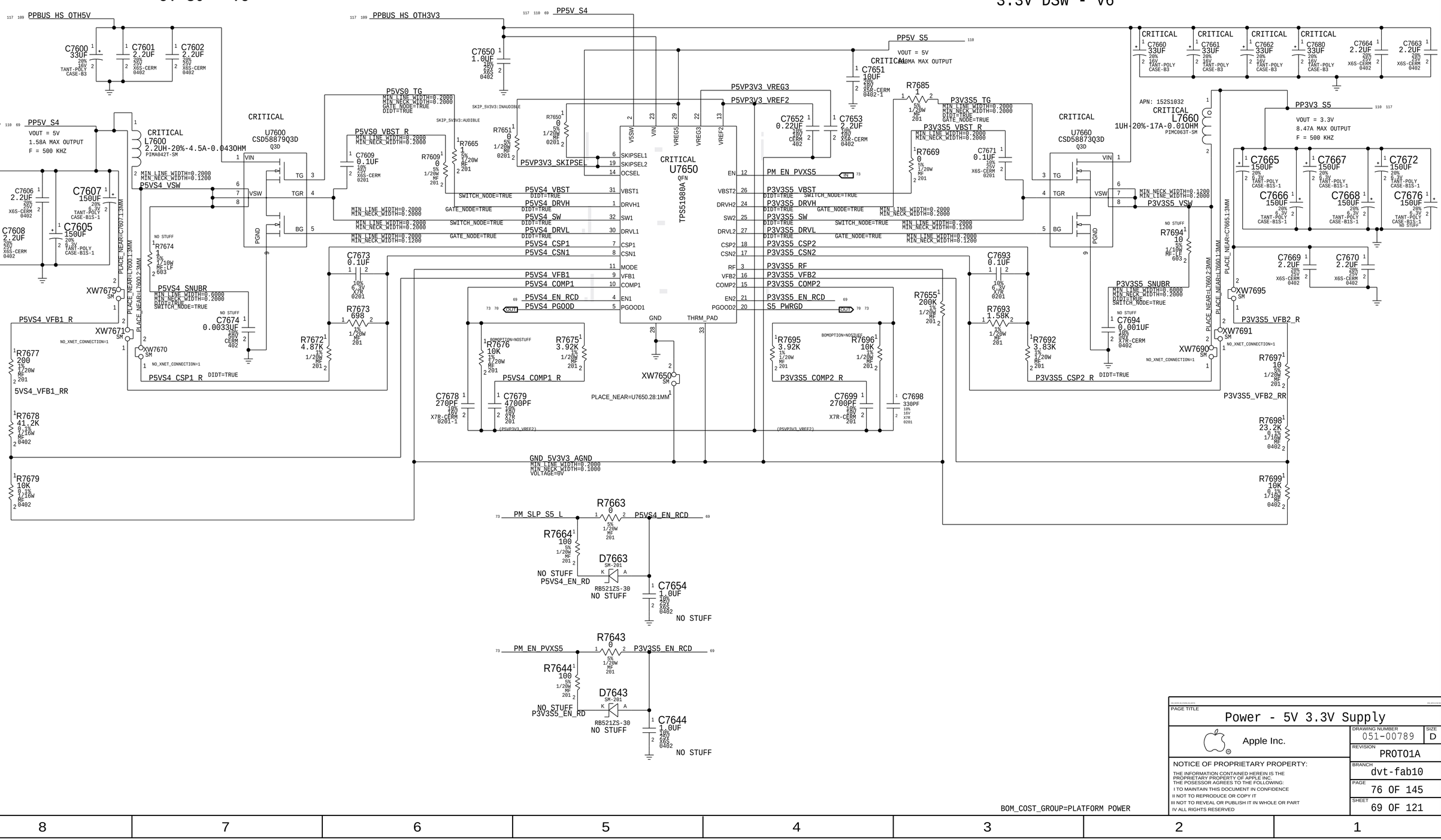
DRAWING NUMBER 051-00789 SIZE D

REVISION PROTO1A

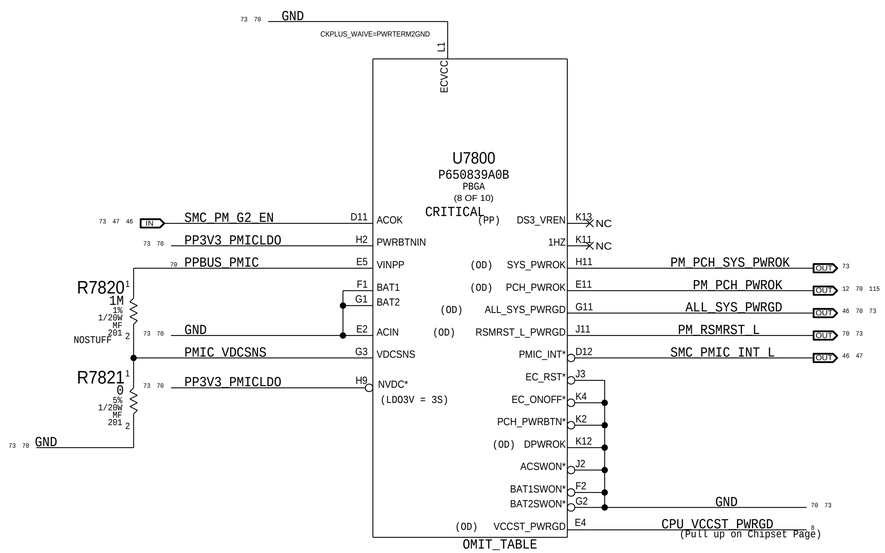
BRANCH dvt-fab10

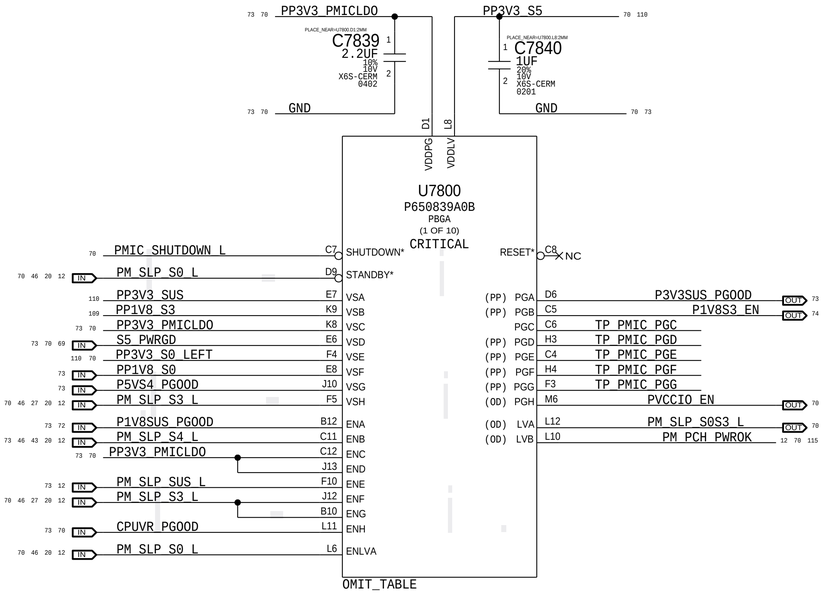
PAGE 74 OF 145

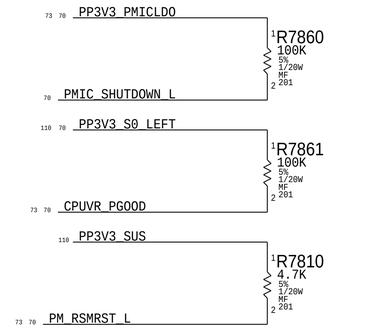
SHEET 68 OF 121

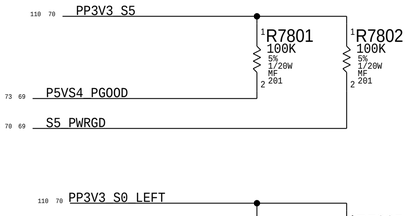

5V S0 - V5
3.3V DSW - V6
PPBUS_HS_OTH5V
PPBUS_HS_OTH3V3
PP5V_S4
PP5V_S5
VOUT = 5V
1.58A MAX OUTPUT
F = 500 KHZ
8.47A MAX OUTPUT
PP3V3_S5
VOUT = 3.3V
F = 500 KHZ
U7600
CSD58879Q3D
U7650
TPS51980A
L7600
2.2UH-20%-4.5A-0.0430HM
L7660
1UH-20%-17A-0.01OHM
P5VS0_TG
P5VS0_VBST_R
P5VS4_VBST
P5VS4_DRVH
P5VS4_SW
P5VS4_DRVL
P5VS4_CSP1
P5VS4_CSN1
P5VS4_VFB1
P5VS4_COMP1
P5VS4_EN_RCD
P5VS4_PGOOD
P5VP3V3_VREG3
P5VP3V3_VREF2
P5VP3V3_SKIPSEL
PM_EN_PVXS5
P3V3S5_VBST
P3V3S5_DRVH
P3V3S5_SW
P3V3S5_DRVL
P3V3S5_CSP2
P3V3S5_CSN2
P3V3S5_RF
P3V3S5_VFB2
P3V3S5_COMP2
P3V3S5_EN_RCD
S5_PWRGD
P3V3S5_TG
P3V3S5_VSW
P3V3S5_SNUBR
P3V3S5_VFB2_R
P3V3S5_CSP2_R
P3V3S5_COMP2_R
P3V3S5_VFB2_RR
5VS4_VFB1_RR
P5VS4_VFB1_R
P5VS4_CSP1_R
P5VS4_COMP1_R
PM_SLP_S5_L
P5VS4_EN_RCD
PM_EN_PVXS5
P3V3S5_EN_RCD
P5VS4_EN_RD
P3V3S5_EN_RD
GND_5V3V3_AGND
PLACE_NEAR=U7650.28:1MM
PLACE_NEAR=L7600.2:3MM
PLACE_NEAR=C7607.1:3MM
PLACE_NEAR=L7660.1:3MM
PLACE_NEAR=C7665.1:3MM
BOM_COST_GROUP=PLATFORM POWER
PAGE TITLE
Power - 5V 3.3V Supply
Apple Inc.
DRAWING NUMBER
051-00789
SIZE
D
REVISION
PROTO1A
BRANCH
dvt-fab10
PAGE
76 OF 145
SHEET
69 OF 121
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

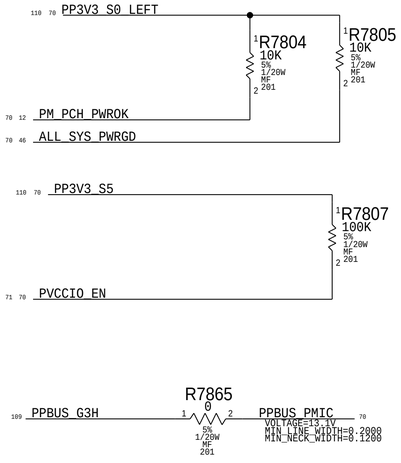
BANJO - PMIC Control

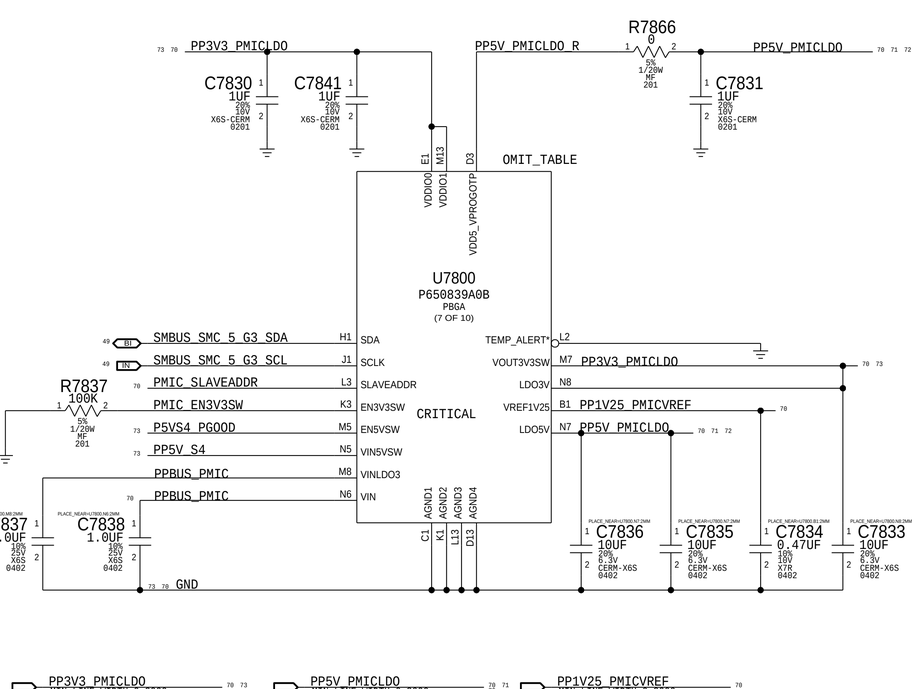


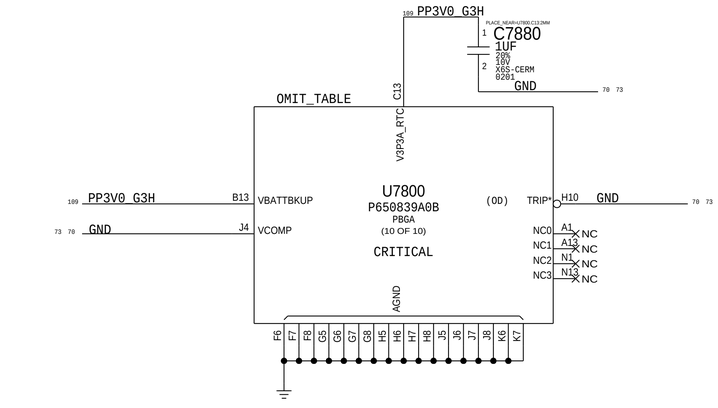


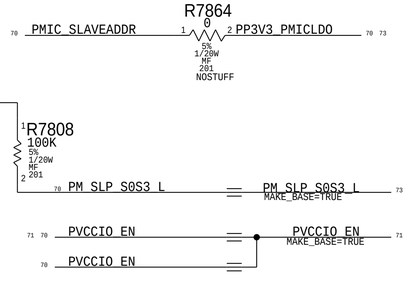


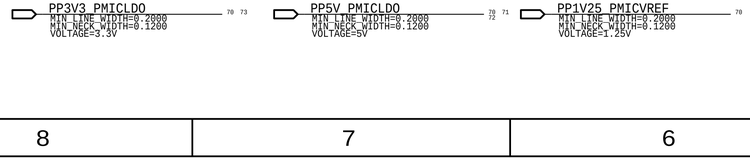












BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=J08_MLB SYNC_DATE=12/08/2010

PAGE TITLE

PMIC-1 & Power Control

Apple Inc.

DRAWING NUMBER 051-00789 SIZE D

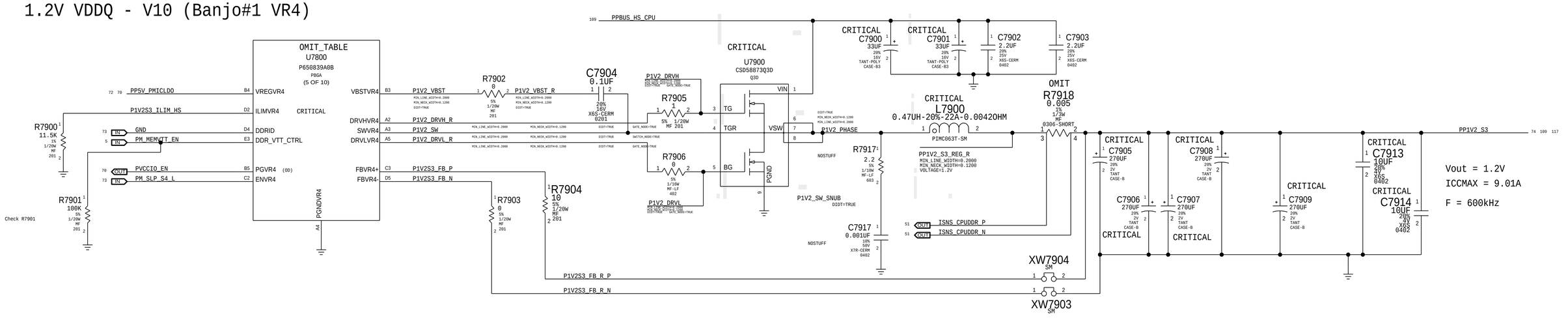
REVISION PROTO1A

BRANCH dvt-fab10

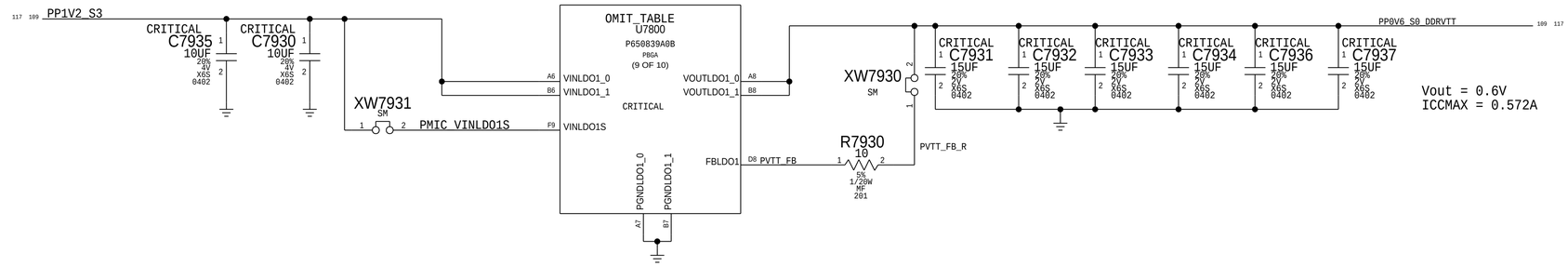
PAGE 78 OF 145

SHEET 70 OF 121

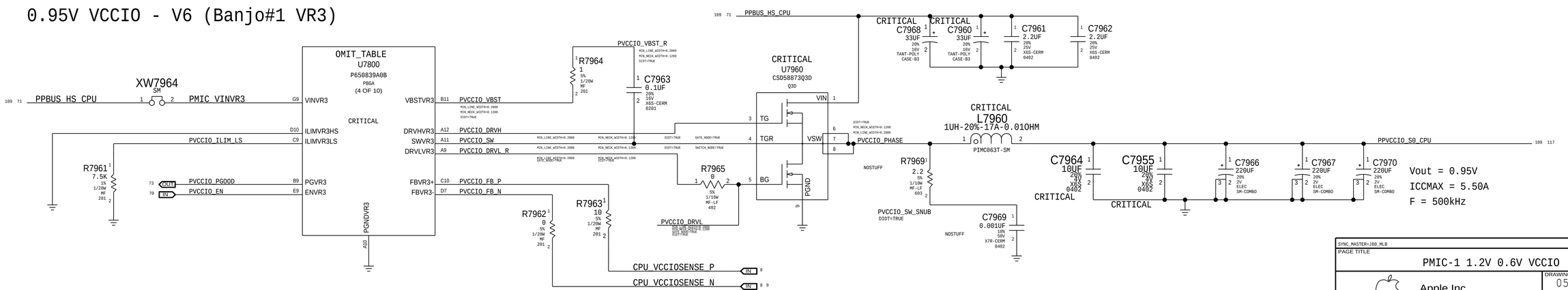
1.2V VDDQ - V10 (Banjo#1 VR4)



0.6V VTT - V13 (Banjo#1 LDO1)



0.95V VCCIO - V6 (Banjo#1 VR3)



BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE

PMIC-1 1.2V 0.6V VCCIO

Apple Inc.

DRAWING NUMBER 051-00789 SIZE D

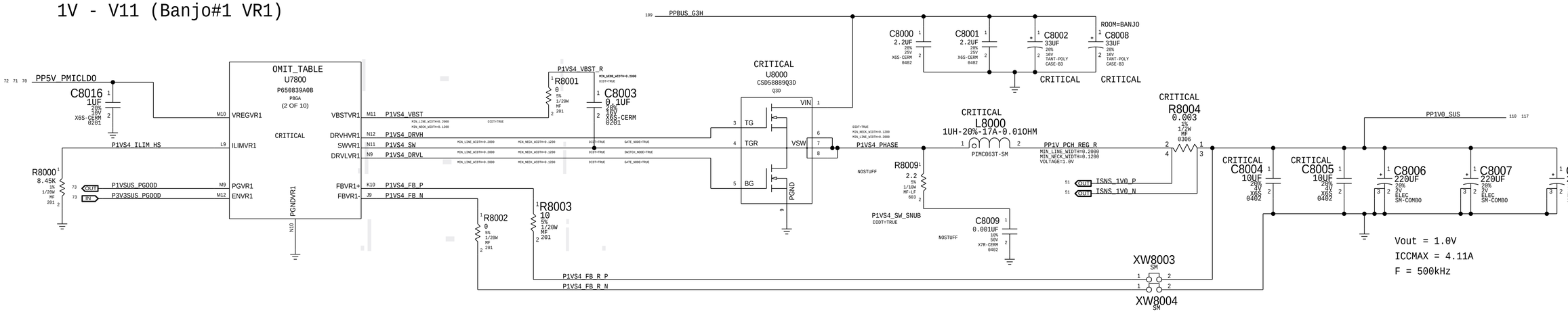
REVISION PROTO1A

BRANCH dvt-fab10

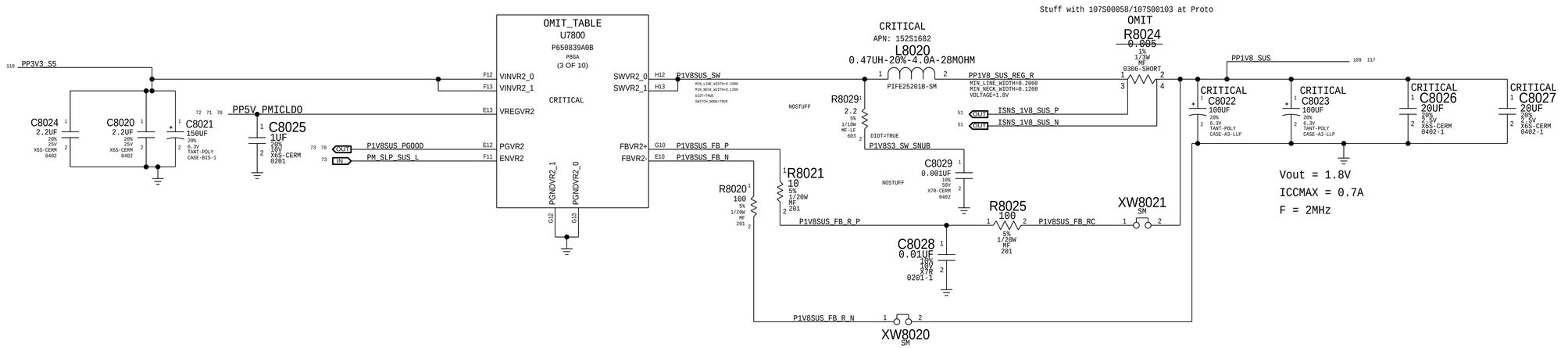
PAGE 79 OF 145

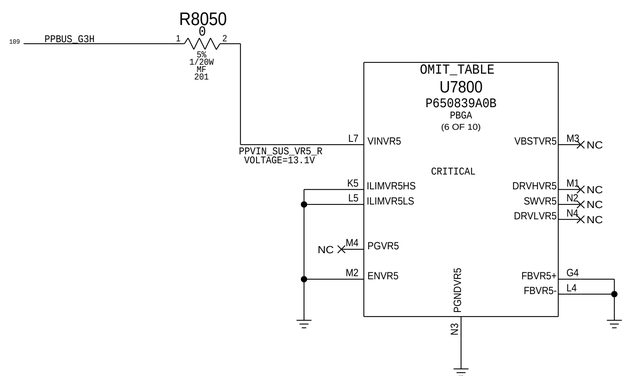
SHEET 71 OF 121

1V - V11 (Banjo#1 VR1)



1.8V - V8 (Banjo#1 VR2)





BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE: PMIC-1 1V 1.8V VCCPCH

Apple Inc.

DRAWING NUMBER: 051-00789 SIZE: D

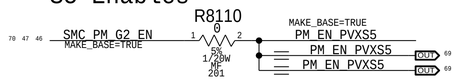
REVISION: PROTO1A

BRANCH: dvt-fab10

PAGE: 80 OF 145

SHEET: 72 OF 121

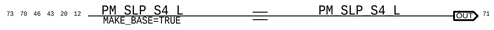
S5 Enables



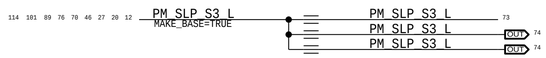
SUS Enables

S4 Enables

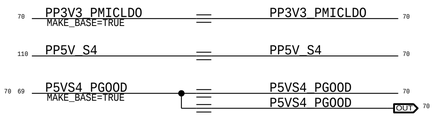
S3 Enables

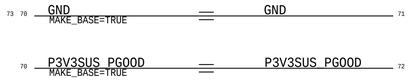


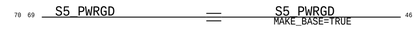
S0 Enables

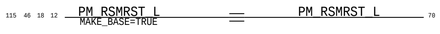


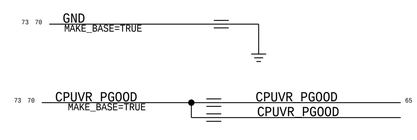
S0i Enables

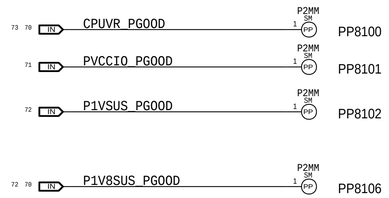




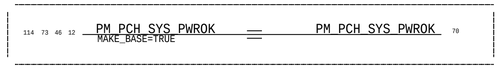


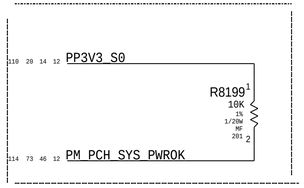




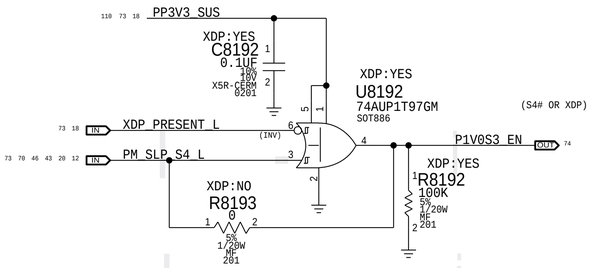


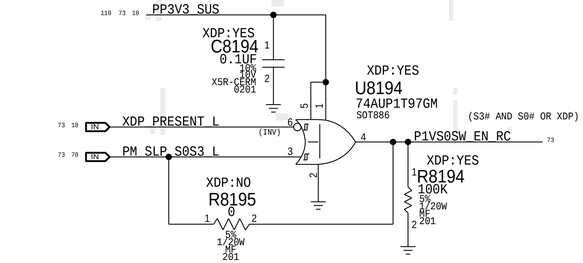
J80G specific

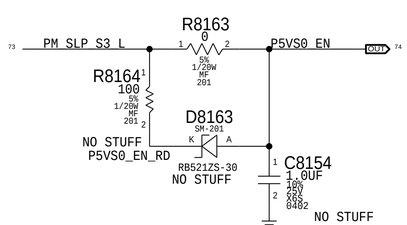




KEEP THESE RAILS ON WHEN USING XDP







BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE

PMIC-1 Aliases & TPs

Apple Inc.

DRAWING NUMBER 051-00789 SIZE D

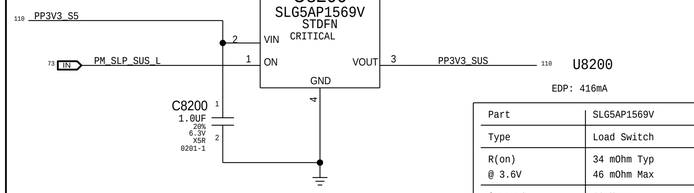
REVISION PROTO1A

BRANCH dvt-fab10

PAGE 81 OF 145

SHEET 73 OF 121

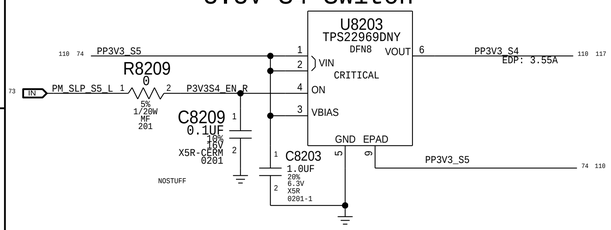
3.3V SUS Switch



U8200
EDP: 416mA

Part	SLG5AP1569V
Type	Load Switch
R(on) @ 3.6V	34 mOhm Typ 46 mOhm Max
Current	1A Max

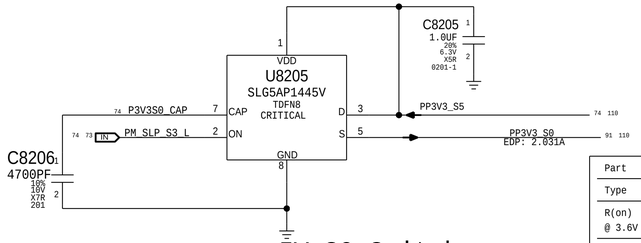
3.3V S4 Switch



U8203

Part	TPS22969
Type	Load Switch
R(on) @ 3.6V	4.4 MOHM TYP 6.6 MOHM MAX
Current	6A MAX

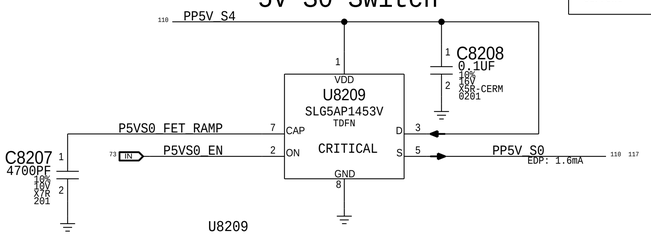
3.3V S0 Switch



U8205

Part	SLG5AP1445V
Type	Load Switch
R(on) @ 3.6V	7.8 MOHM TYP 8.5 MOHM MAX
Current	4A MAX

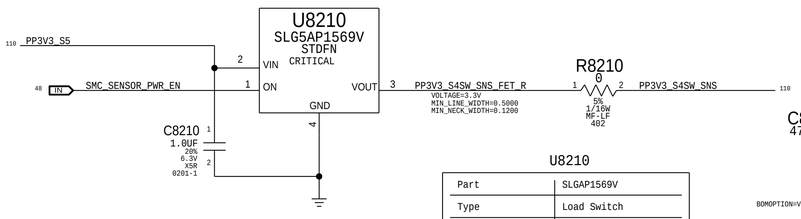
5V S0 Switch



U8209

Part	SLG5AP1453V
Type	Load Switch
R(on)	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A

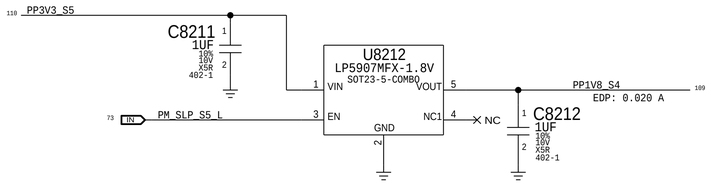
3.3V Sensor Switch



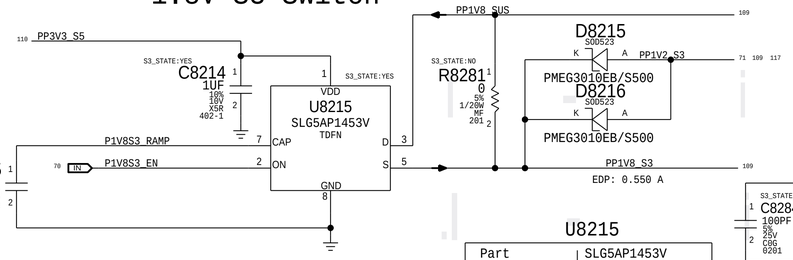
U8210

Part	SLGAP1569V
Type	Load Switch
R(on) @ 3.6V	34 mOhm Typ 46 mOhm Max
Current	1A Max

1.8V S4 LDO



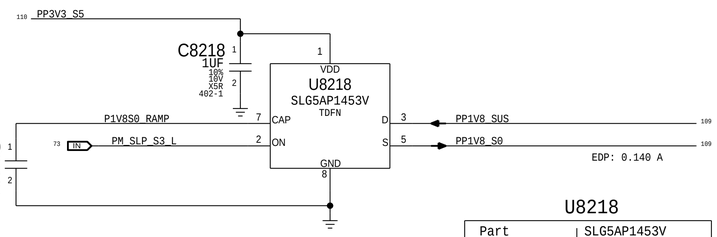
1.8V S3 Switch



U8215

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 5.3A	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A Max

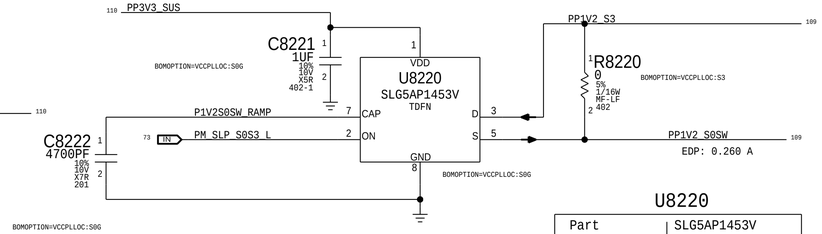
1.8V S0 Switch



U8218

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 5.3A	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A Max

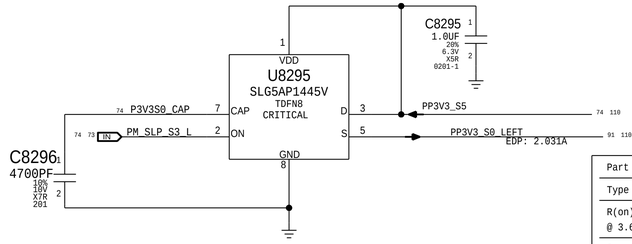
1.2V S0 SW Switch



U8220

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 5.3A	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A Max

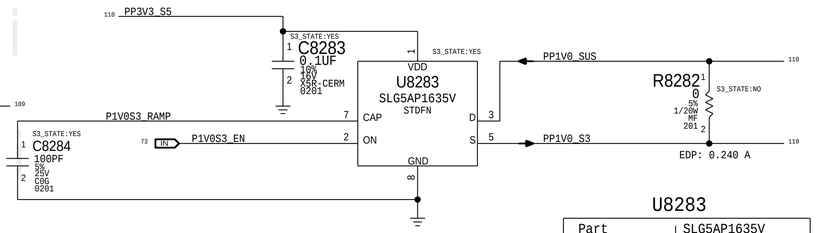
3.3V S0 Switch LEFT



U8295

Part	SLG5AP1445V
Type	Load Switch
R(on) @ 3.6V	7.8 MOHM TYP 8.5 MOHM MAX
Current	4A MAX

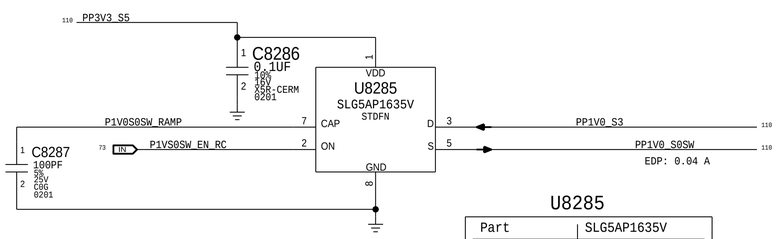
1.0V S3 Switch



U8283

Part	SLG5AP1635V
Type	Load Switch
R(on) @ 25C	20 mOhm Typ 28 mOhm Max
Current	2.5A Max
Ton Total	39us max @ 1V

1.0V S0 SW Switch



U8285

Part	SLG5AP1635V
Type	Load Switch
R(on) @ 25C	20 mOhm Typ 28 mOhm Max
Current	2.5A Max
Ton Total	39us max @ 1V

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE

Power FETs

Apple Inc.

DRAWING NUMBER	051-00789
SIZE	D
REVISION	PROTO1A
BRANCH	dvt-fab10
PAGE	82 OF 145
SHEET	74 OF 121

Page Notes

Power aliases required by this page:

- +PPVIN_S0SW_LCDBKLTFET (9-12.6V LCD BACKLIGHT INPUT)
- +PP5V_S0_BKLT (5V BACKLIGHT DRIVER INPUT)

PLATFORM_RESET NO LONGER GATES THE BKLT_EN AS BOTH COME FROM PCH NOW

I2C ID DEDICATED.ONLY CONNECTS TO JERRY

VOUT = 52V TYP, 59V MAX
IOUT = 0.135A TYP, 0.15A MAX
FS = 625KHZ TYP (+/- 7%)

PBUS LINE WIDTHS

LCD BKLT LINE WIDTHS

BOM_COST_GROUP=DISPLAY

PAGE TITLE	LCD Backlight Driver
	Apple Inc.
DRAWING NUMBER	051-00789
SIZE	D
REVISION	PROTO1A
BRANCH	dvt-fab10
PAGE	84 OF 145
SHEET	75 OF 121

LCD PANEL INTERFACE (eDP) + Camera (MIPI)

PP5V_S0 — CRITICAL — U8500 SLG5AP1443V TDFN (VDD, CAP, ON, GND, D, S)
R8515 150K 5% 1/20W MF 201 — LCD_PWR_SLEW — PANEL_P5V_EN
R8517 330 5% 1/20W MF 201 — PANEL_P5V_EN_D — D8517 SC2 DSF01S30SCAP
C8515 0.1UF 10% 16V X5R-CERM 0201
C8509 2200PF 10% 10V X7R-CERM 0201
C8511 0.1UF 10% 16V X5R-CERM 0201
C8512 10UF 20% 6.3V X5R-CERM 0402-7
VOLTAGE=5V — PP5V_S0SW_LCD — 76 114

PP3V3_S5 — CRITICAL — U8501 SLG5AP1443V TDFN (VDD, CAP, ON, GND, D, S)
R8516 200K 1% 1/20W MF 201 — PANEL_P3V3_EN — LCD_PWR_SLEW_3V3
R8518 330 5% 1/20W MF 201 — PANEL_P3V3_EN_D — D8518 SC2 DSF01S30SCAP
C8516 0.47UF 10% 6.3V CERM-X5R 0201
C8513 2200PF 10% 10V X7R-CERM 0201
C8510 1.0UF 20% 6.3V X5R 0201-1
VOLTAGE=3.3V — PP3V3_S0SW_LCD_R

Stuff with 107S0276/107S0020 at Proto
0MIT
R8520 0.005 1% 1/2W MF 0306-SHORT — NO_XNET_CONNECTION=1
PP3V3_S0SW_LCD — MIN_NECK_WIDTH=0.2000 MIN_LINE_WIDTH=0.2000 VOLTAGE=3.3V — 76 114
ISNS_LCDPANEL_P — 52
ISNS_LCDPANEL_N — 52

PPVOUT_S0_LCDBKLT — 75 76 114 116
C8500 1000PF 10% 100V X7R-CERM 0603

76 PANEL_FET_EN_DLY
109 47 46 PP3V3_G3H
CRITICAL — U8510 SLG4AP4998 STQFN (VDD, EDP_PANEL_PWR_EN, PM_SLP_S3_L, SMC_RESET_INPUT_L, PANEL_FET_EN_DLY, PANEL_PWR_EN_CONN, SMC_RESET_OUTPUT_L, X604_DISP_PWR_EN, X604_DISP_SMC_RST_L, NC0, NC1, GND)
89 76 IN EDP_PANEL_PWR_EN
114 101 89 73 70 46 27 20 12 IN PM_SLP_S3_L
114 76 64 57 48 29 IN SMC_RESET_L
BUF_SMC_RESET_L — OUT 46 48 76
DFR_DISP_PWR_EN — OUT 42
DFR_DISP_SMC_RST_L — OUT 42
BUF_EDP_PANEL_PWR_EN — 76 114
NC_U8510_5
NC_U8510_11

NO_XNET_CONNECTION=1
J8500 20759-042E-02 F-ST-SM (PWR, SIGNAL)
116 114 76 75 PPVOUT_S0_LCDBKLT — PP3V3_S0SW_LCD — 76 114
114 76 EDP_AUXCH_C_N
114 76 EDP_AUXCH_C_P
BUF_EDP_PANEL_PWR_EN — 76 114
76 EDP_INT_ML_N<0>
76 EDP_INT_ML_P<0>
DP_INT_HPD_R — 76
LCD_FSS — 76 89 114
LCD_IRQ_L — OUT 15 114
76 EDP_INT_ML_N<1>
76 EDP_INT_ML_P<1>
BKLT_PWM_TCON2MLB — OUT 48 114
BKLT_PWM_MLB2TCON — IN 20 114
76 EDP_INT_ML_N<2>
76 EDP_INT_ML_P<2>
I2C_BKLT_SDA — BI 111 114
I2C_BKLT_SCL — IN 111 114
76 EDP_INT_ML_N<3>
76 EDP_INT_ML_P<3>
SMBUS_SMC_0_S0_SDA — BI 49 114
SMBUS_SMC_0_S0_SCL — IN 49 114
38 MIPI_DATA_CONN_N — BI
38 MIPI_DATA_CONN_P — BI
I2C_ALS_SDA — BI 42 114
I2C_ALS_SCL — IN 42 114
38 MIPI_CLK_CONN_N — IN
38 MIPI_CLK_CONN_P — IN
I2C_CAM_SCL — IN 37 38 114
I2C_CAM_SDA — BI 37 38 114
114 76 PP5V_S0SW_LCD
PP5V_S0_ALSCAM_F — 38 114

U8510 BYPASS

NO_STUFF R8590 0 5% 1/20W MF 0201 — 89 76 EDP_PANEL_PWR_EN — PANEL_FET_EN_DLY — 76
NO_STUFF R8591 0 5% 1/20W MF 0201 — BUF_EDP_PANEL_PWR_EN — 76 114
NO_STUFF R8592 0 5% 1/20W MF 0201 — 76 64 57 48 29 114 IN SMC_RESET_L — BUF_SMC_RESET_L — OUT 46 48 76

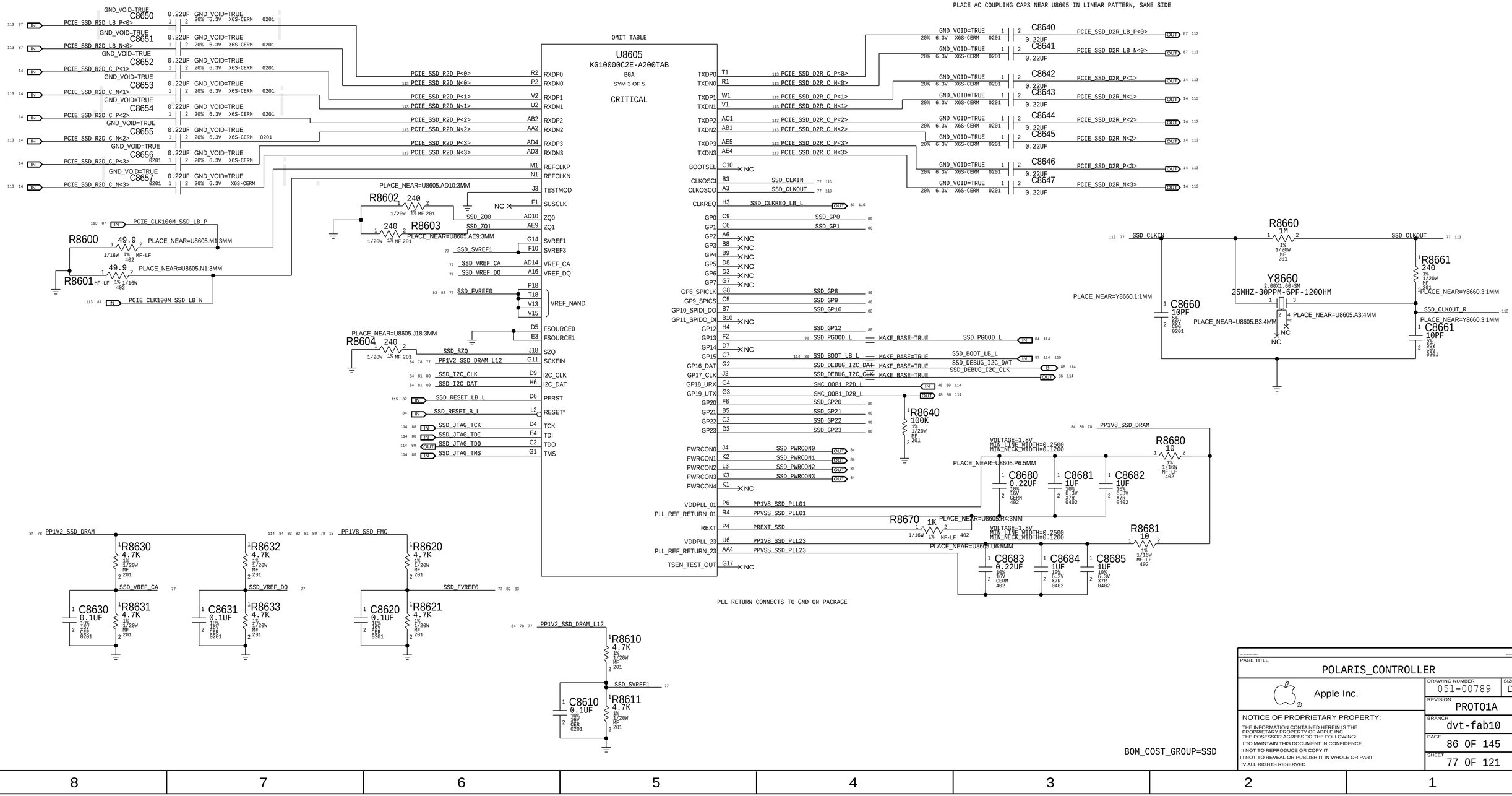
LCD Panel HPD, FSS & AUX strapping

116 PP3V3_S0
NO_XNET_CONNECTION=1
NO_STUFF R8503 1M 5% 1/20W MF 201
114 89 OUT DP_INT_HPD — R8505 0 5% 1/20W MF 0201 — DP_INT_HPD_R — 76
114 76 EDP_AUXCH_C_N
114 76 EDP_AUXCH_C_P
114 76 89 LCD_FSS
R8504 100K 5% 1/20W MF 201
R8501 100K 5% 1/20W MF 201
NO_XNET_CONNECTION=1
NO_STUFF R8502 1M 5% 1/20W MF 201

114 111 IN EDP_INT_ML_P<0> = EDP_INT_ML_P<0> MAKE_BASE=TRUE — 76
114 111 IN EDP_INT_ML_N<0> = EDP_INT_ML_N<0> MAKE_BASE=TRUE — 76
114 111 IN EDP_INT_ML_P<1> = EDP_INT_ML_P<1> MAKE_BASE=TRUE — 76
114 111 IN EDP_INT_ML_N<1> = EDP_INT_ML_N<1> MAKE_BASE=TRUE — 76
114 111 IN EDP_INT_ML_P<2> = EDP_INT_ML_P<2> MAKE_BASE=TRUE — 76
114 111 IN EDP_INT_ML_N<2> = EDP_INT_ML_N<2> MAKE_BASE=TRUE — 76
114 111 IN EDP_INT_ML_P<3> = EDP_INT_ML_P<3> MAKE_BASE=TRUE — 76
114 111 IN EDP_INT_ML_N<3> = EDP_INT_ML_N<3> MAKE_BASE=TRUE — 76
113 111 BI EDP_AUXCH_C_P = EDP_AUXCH_C_P MAKE_BASE=TRUE — 76 114
113 111 BI EDP_AUXCH_C_N = EDP_AUXCH_C_N MAKE_BASE=TRUE — 76 114

BOM_COST_GROUP=DISPLAY

PAGE TITLE: eDP Display Connector
Apple Inc.
DRAWING NUMBER: 051-00789 — SIZE: D
REVISION: PROTO1A
BRANCH: dvt-fab10
PAGE: 85 OF 145
SHEET: 76 OF 121


PLACE AC COUPLING CAPS NEAR U8605 IN LINEAR PATTERN, SAME SIDE
OMIT_TABLE
U8605
KG10000C2E-A200TAB
BGA
SYM 3 OF 5
CRITICAL
C8650 0.22UF
C8651 0.22UF
C8652 0.22UF
C8653 0.22UF
C8654 0.22UF
C8655 0.22UF
C8656 0.22UF
C8657 0.22UF
PCIE_SSD_R2D_LB_P<0>
PCIE_SSD_R2D_LB_N<0>
PCIE_SSD_R2D_C_P<1>
PCIE_SSD_R2D_C_N<1>
PCIE_SSD_R2D_C_P<2>
PCIE_SSD_R2D_C_N<2>
PCIE_SSD_R2D_C_P<3>
PCIE_SSD_R2D_C_N<3>
PCIE_SSD_R2D_P<0>
PCIE_SSD_R2D_N<0>
PCIE_SSD_R2D_P<1>
PCIE_SSD_R2D_N<1>
PCIE_SSD_R2D_P<2>
PCIE_SSD_R2D_N<2>
PCIE_SSD_R2D_P<3>
PCIE_SSD_R2D_N<3>
RXDP0
RXDN0
RXDP1
RXDN1
RXDP2
RXDN2
RXDP3
RXDN3
REFCLKP
REFCLKN
TESTMOD
SUSCLK
ZQ0
ZQ1
SVREF1
SVREF3
VREF_CA
VREF_DQ
VREF_NAND
FSOURCE0
FSOURCE1
SZQ
SCKEIN
I2C_CLK
I2C_DAT
PERST
RESET*
TCK
TDI
TDO
TMS
PCIE_SSD_D2R_C_P<0>
PCIE_SSD_D2R_C_N<0>
PCIE_SSD_D2R_C_P<1>
PCIE_SSD_D2R_C_N<1>
PCIE_SSD_D2R_C_P<2>
PCIE_SSD_D2R_C_N<2>
PCIE_SSD_D2R_C_P<3>
PCIE_SSD_D2R_C_N<3>
TXDP0
TXDN0
TXDP1
TXDN1
TXDP2
TXDN2
TXDP3
TXDN3
BOOTSEL
CLKOSCI
CLKOSCO
CLKREQ
SSD_CLKIN
SSD_CLKOUT
SSD_CLKREQ_LB_L
GP0
GP1
GP2
GP3
GP4
GP5
GP6
GP7
GP8_SPICLK
GP9_SPICS
GP10_SPIDI_DO
GP11_SPIDO_DI
GP12
GP13
GP14
GP15
GP16_DAT
GP17_CLK
GP18_URX
GP19_UTX
GP20
GP21
GP22
GP23
SSD_GP0
SSD_GP1
SSD_GP8
SSD_GP9
SSD_GP10
SSD_GP12
SSD_PGOOD_L
SSD_BOOT_LB_L
SSD_DEBUG_I2C_DAT
SSD_DEBUG_I2C_CLK
SMC_OOB1_R2D_L
SMC_OOB1_D2R_L
SSD_GP20
SSD_GP21
SSD_GP22
SSD_GP23
MAKE_BASE=TRUE
PWRCON0
PWRCON1
PWRCON2
PWRCON3
PWRCON4
SSD_PWRCON0
SSD_PWRCON1
SSD_PWRCON2
SSD_PWRCON3
VDDPLL_01
PLL_REF_RETURN_01
REXT
VDDPLL_23
PLL_REF_RETURN_23
TSEN_TEST_OUT
PP1V8_SSD_PLL01
PPVSS_SSD_PLL01
PREXT_SSD
PP1V8_SSD_PLL23
PPVSS_SSD_PLL23
PLL RETURN CONNECTS TO GND ON PACKAGE
PCIE CLK100M SSD_LB_P
PCIE CLK100M SSD_LB_N
R8600 49.9
R8601 49.9
PLACE_NEAR=U8605.M13MM
PLACE_NEAR=U8605.N1:3MM
R8602 240
R8603 240
PLACE_NEAR=U8605.AD10:3MM
PLACE_NEAR=U8605.AE9:3MM
R8604 240
PLACE_NEAR=U8605.J18:3MM
R8640 100K
R8660 1M
Y8660 25MHZ-30PPM-6PF-120OHM
R8661 240
C8660 10PF
C8661 10PF
PLACE_NEAR=Y8660.1:1MM
PLACE_NEAR=U8605.B3:4MM
PLACE_NEAR=U8605.A3:4MM
PLACE_NEAR=Y8660.3:1MM
SSD_CLKOUT_R
R8670 1K
PLACE_NEAR=U8605.R4:3MM
PLACE_NEAR=U8605.U6:5MM
R8680 10
R8681 10
C8680 0.22UF
C8681 1UF
C8682 1UF
C8683 0.22UF
C8684 1UF
C8685 1UF
PP1V8_SSD_DRAM
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.2500
MIN_NECK_WIDTH=0.1200
PP1V2_SSD_DRAM
PP1V8_SSD_FMC
PP1V2_SSD_DRAM_L12
R8630 4.7K
R8631 4.7K
R8632 4.7K
R8633 4.7K
R8620 4.7K
R8621 4.7K
R8610 4.7K
R8611 4.7K
C8630 0.1UF
C8631 0.1UF
C8620 0.1UF
C8610 0.1UF
SSD_VREF_CA
SSD_VREF_DQ
SSD_FVREF0
SSD_SVREF1
BOM_COST_GROUP=SSD
PAGE TITLE
POLARIS_CONTROLLER
Apple Inc.
DRAWING NUMBER
051-00789
SIZE
D
REVISION
PROT01A
BRANCH
dvt-fab10
PAGE
86 OF 145
SHEET
77 OF 121
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

OMIT_TABLE

U8605
KG10000C2E-A200TAB
BGA
SYM 4 OF 5
CRITICAL

VDD1: B4, B23, AD8, AD21 ← PP1V8_SSD_DRAM (84 80 78 77)
VDD2: A4, A8, A15, A23, C1, J1, AE8, AE14, AE18, AE21 ← PP1V2_SSD_DRAM (84 78 77)
VDD33_ALV33: E2 ← PP3V3_SSD_LIM (86 84 53)
VDD33_UART: E1
VDD10_ALV: M9, N10, P9, R10, T9
VDD10_SRAM: U10 ← PP1V0_SSD_CORE (114 84)
VDD10_LOG: H17, K9, K11, K13, K15, K17, M11, M15, M17, P11, P15, P17, T11, T13, T15, T17 ← PP1V0_SSD_CORE_L12 (84 78)
VDD10_PLL: K8 ← PP1V0_SSD_PLL
VDD11_LVDS: R7 ← PP1V1_SSD_LVDS (78)
VDD12_CKE: F11 ← PP1V2_SSD_DRAM (84 78 77)
VDD12_DDR: G9, G13, H7, H8, H9, H10, H11, H12, H13, H14, H15, H16 ← PP1V2_SSD_DRAM_L12 (84 78 77)

VDD18_ALV18: K4, L4, M4 → PP1V8_SSD_DRAM (77 78 80 84)
VDD18_GPIO: F6, G6 → PP1V8_SSD_DRAM_L12 (78 84)
VDD18_LVDS: T7 → PP1V8_SSD_LVDS (78)
VDD18_NAND: F17, F20, J20, K18, L18, N18, N20, R18, U18, V10, V12, V14, V16, V18, Y12, Y18, Y20 → PP1V8_SSD_FMC (15 77 78 80 81 82 83 84 114)
VDD18_OSC: F4 → PP1V8_SSD_OSC (78)
VDD18_PLL0: M6 → PP1V8_SSD_PLL0 (78)
VDD18_PLL1: M7 → PP1V8_SSD_PLL1 (78)
VDD18_PLL2: K6 → PP1V8_SSD_PLL2 (78)
VDD18_PLL3: K7 → PP1V8_SSD_PLL3 (78)
VDD18_TS: G16 → PP1V8_SSD_FMC (15 77 78 80 81 82 83 84 114)
VDDCA: AE10, AE13, AE15, AE19 → PP1V2_SSD_DRAM (77 78 84)
VDDIO_01: P8, R8
VDDIO_23_0: U8
VDDIO_23_1: V8 → PP1V1_SSD_PCIE (78 84)
VDDIO_SENSE_01: T4 → NC
VDDIO_SENSE_23: AB4 → NC
VDDQ: A5, A7, A9, A11, A14, A17, A19, A22, C25, D1, D25, H1, H25 → PP1V2_SSD_DRAM (77 78 84)

L8700 FERR-30-OHM-2.2A-0.035-OHM 0402 — PP1V1_SSD_PCIE (84 78) — PP1V1_SSD_LVDS (78)
C8700 1UF 10% 6.3V X7R 0402
C8701 0.1UF 10% 16V CER 0201
VOLTAGE=1.1V MIN_NECK_WIDTH=0.1200 MIN_LINE_WIDTH=0.2000

L8710 FERR-30-OHM-2.2A-0.035-OHM 0402 — PP1V8_SSD_DRAM (84 80 78 77) — PP1V8_SSD_LVDS (78)
C8710 1UF 10% 6.3V X7R 0402
C8711 0.1UF 10% 16V CER 0201
VOLTAGE=1.8V MIN_NECK_WIDTH=0.1200 MIN_LINE_WIDTH=0.2000

L8715 FERR-30-OHM-2.2A-0.035-OHM 0402 — PP1V8_SSD_OSC (78)
C8716 1UF 10% 6.3V X7R 0402
C8715 0.1UF 10% 16V CER 0201
VOLTAGE=1.8V MIN_NECK_WIDTH=0.1200 MIN_LINE_WIDTH=0.2000

C870C 12PF 5% 25V NP0-C0G 0201
C870D 3.0PF +/-0.1PF 25V NP0-C0G 0201
PP1V8_SSD_DRAM_L12 (84 78)

L8720 FERR-30-OHM-2.2A-0.035-OHM 0402 — PP1V8_SSD_PLL0 (78)
C8721 1UF 10% 6.3V X7R 0402
C8720 0.1UF 10% 16V CER 0201
VOLTAGE=1.8V MIN_NECK_WIDTH=0.1200 MIN_LINE_WIDTH=0.2000

L8725 FERR-30-OHM-2.2A-0.035-OHM 0402 — PP1V8_SSD_PLL1 (78)
C8726 1UF 10% 6.3V X7R 0402
C8725 0.1UF 10% 16V CER 0201
VOLTAGE=1.8V MIN_NECK_WIDTH=0.1200 MIN_LINE_WIDTH=0.2000

L8730 FERR-30-OHM-2.2A-0.035-OHM 0402 — PP1V8_SSD_PLL2 (78)
C8731 1UF 10% 6.3V X7R 0402
C8730 0.1UF 10% 16V CER 0201
VOLTAGE=1.8V MIN_NECK_WIDTH=0.1200 MIN_LINE_WIDTH=0.2000

L8735 FERR-30-OHM-2.2A-0.035-OHM 0402 — PP1V8_SSD_PLL3 (78)
C8736 1UF 10% 6.3V X7R 0402
C8735 0.1UF 10% 16V CER 0201
VOLTAGE=1.8V MIN_NECK_WIDTH=0.1200 MIN_LINE_WIDTH=0.2000

C8702 0.1UF 10% 16V CER 0201
C8703 0.1UF 10% 16V CER 0201
C8704 1UF 10% 6.3V X7R 0402
C8705 1UF 10% 6.3V X7R 0402

C8796 12PF 5% 25V NP0-C0G 0201
C8797 3.0PF +/-0.1PF 25V NP0-C0G 0201
C8795 0.22UF 20% 6.3V X5R 0201

C8746 12PF 5% 25V NP0-C0G 0201
C8745 3.0PF +/-0.1PF 25V NP0-C0G 0201
C8744 1UF 10% 6.3V X7R 0402
C8743 1UF 10% 6.3V X7R 0402
C8742 0.1UF 10% 16V CER 0201
C8741 0.1UF 10% 16V CER 0201
C8740 0.1UF 10% 16V CER 0201

C8758 12PF 5% 25V NP0-C0G 0201
C8757 3.0PF +/-0.1PF 25V NP0-C0G 0201
C8756 1UF 10% 6.3V X7R 0402
C8755 1UF 10% 6.3V X7R 0402
C8754 1UF 10% 6.3V X7R 0402
C8753 0.1UF 10% 16V CER 0201 NOSTUFF
C8752 0.1UF 10% 16V CER 0201 NOSTUFF
C8751 0.1UF 10% 16V CER 0201
C8750 0.1UF 10% 16V CER 0201

L8760 FERR-30-OHM-2.2A-0.035-OHM 0402 — PP1V0_SSD_CORE_L12 (84 78)
C8761 1UF 10% 6.3V X7R 0402
C8760 0.1UF 10% 16V CER 0201
VOLTAGE=1.0V MIN_NECK_WIDTH=0.1200 MIN_LINE_WIDTH=0.2000

C8774 12PF 5% 25V NP0-C0G 0201
C8773 3.0PF +/-0.1PF 25V NP0-C0G 0201
C8772 1UF 10% 6.3V X7R 0402
C8771 0.22UF 10% 16V CERM 402
C8770 0.1UF 10% 16V CER 0201
PP1V2_SSD_DRAM_L12 (84 78 77)

C877B 12PF 5% 25V NP0-C0G 0201
C877A 3.0PF +/-0.1PF 25V NP0-C0G 0201
C8779 1UF 10% 6.3V X7R 0402
C8778 1UF 10% 6.3V X7R 0402
C8777 1UF 10% 6.3V X7R 0402
C8776 0.1UF 10% 16V CER 0201
C8775 0.1UF 10% 16V CER 0201
PP1V2_SSD_DRAM (84 78 77)

C8791 1UF 10% 6.3V X7R 0402
C8790 1UF 10% 6.3V X7R 0402
PP1V8_SSD_DRAM (84 80 78 77)

C8784 1UF 10% 6.3V X7R 0402
C8783 1UF 10% 6.3V X7R 0402
C8782 1UF 10% 6.3V X7R 0402
C8781 0.22UF 10% 16V CERM 402
C8780 0.1UF 10% 16V CER 0201
PP1V8_SSD_FMC (114 84 83 82 81 80 78 77 15)

C870A 12PF 5% 25V NP0-C0G 0201
C870B 3.0PF +/-0.1PF 25V NP0-C0G 0201
PP3V3_SSD_NAND (84 83 82)

BOM_COST_GROUP=SSD

PAGE TITLE: POLARIS POWER

Apple Inc.

DRAWING NUMBER: 051-00789
SIZE: D
REVISION: PROTO1A
BRANCH: dvt-fab10
PAGE: 87 OF 145
SHEET: 78 OF 121

OMIT_TABLE

U8605

KG10000C2E-A200TAB

BGA

SYM 5 OF 5

CRITICAL

A1	
A2	
A10	
A24	
A25	
B1	
B2	
B6	
B12	
B14	
B21	
B24	
B25	
C4	
C8	
C14	
C16	
C18	
C20	
D10	
D12	
D15	
D23	
E25	
F7	
F9	
F14	
G10	
G15	
G19	
G22	
G24	
H2	
J6	
J7	
J8	
J10	
J12	
J14	
J16	
K19	
K23	
K25	
L6	
L7	
L8	VSSI
L10	
L12	
L14	
L16	
M3	
M8	
M18	
N16	
N23	
N25	
R12	
R14	
R16	
R19	
R24	
U12	
U14	
U16	
U23	
V9	
V11	
V19	
V25	
W10	
W14	
W17	
Y23	
AA25	
AB16	
AB20	
AB23	
AC9	
AC13	
AD11	
AD17	
AD22	
AD24	
AD25	
AE24	
AE25	

L1	
M2	
N2	
N3	
N4	
N6	
N7	
N8	
P1	
P3	
R3	
R6	
T2	
T3	
T6	
T8	
U1	
U3	
U4	
U7	
V3	
V4	VSSIO
V6	
W2	
W3	
W4	
W8	
Y1	
Y2	
Y3	
Y4	
AA1	
AA3	
AB3	
AB5	
AC2	
AC3	
AC4	
AC5	
AD1	
AD2	
AD5	
AD6	
AE1	
AE2	
AE3	
AE6	
AE7	
F3	VSS18_OSC
P7	
V7	VSS_LVDS

BOM_COST_GROUP=SSD

PAGE TITLE

PAGE_TITLE=POLARIS GND

Apple Inc.

DRAWING NUMBER 051-00789

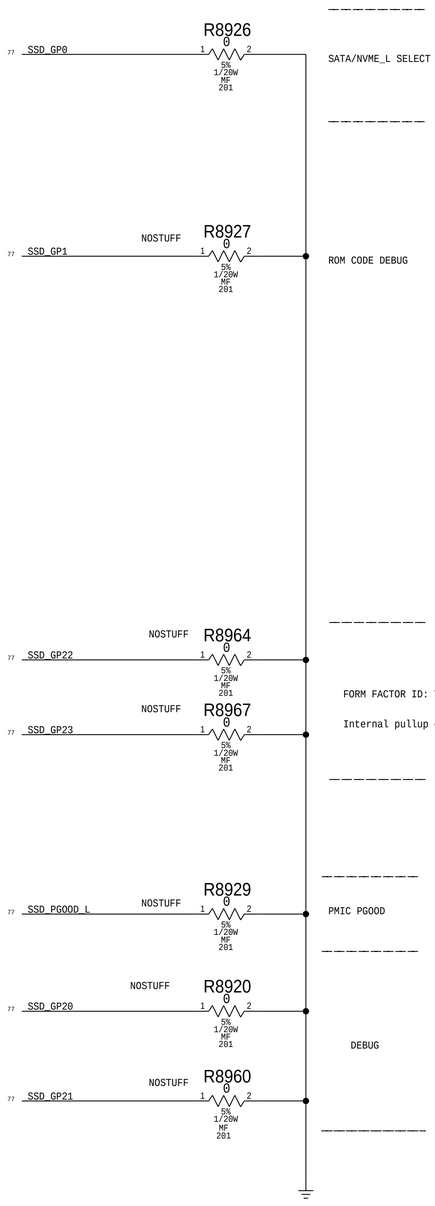
SIZE D

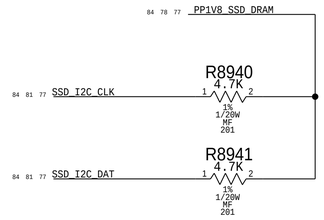
REVISION PROTO1A

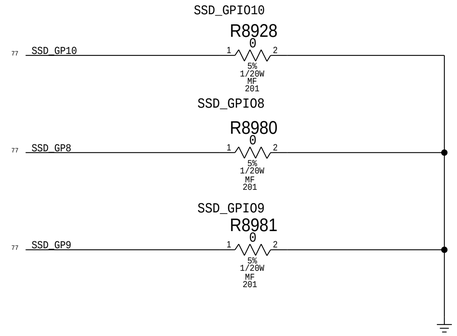
BRANCH dvt-fab10

PAGE 88 OF 145

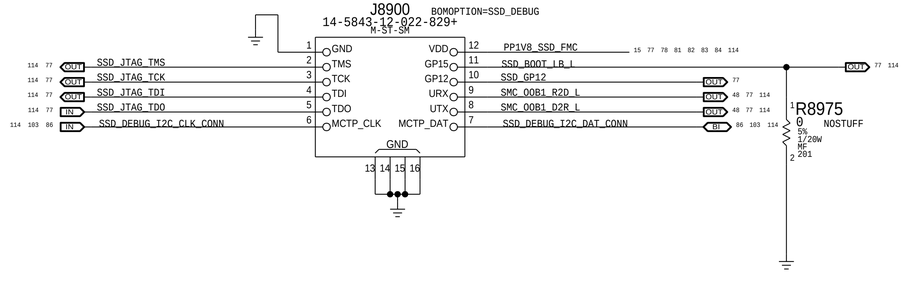
SHEET 79 OF 121







SSD DENSITY



SSD RELATED BOM Groups

BOM GROUP	BOM OPTIONS
SSD_CONFIG:256GB	SSD_GPIO9,NAND_TYPE:256GB,SSD_CTRL_TYPE:4GBIT
SSD_CONFIG:512GB	SSD_GPIO8,NAND_TYPE:512GB,SSD_CTRL_TYPE:4GBIT
SSD_CONFIG:1TB	NAND_TYPE:1TB,SSD_CTRL_TYPE:8GBIT
SSD_CONFIG:2TB	SSD_GPIO10,NAND_TYPE:2TB,SSD_CTRL_TYPE:8GBIT

NAND Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00149	4	NAND,1Z,64GBM,TOGG DDR2,64G,SS,BGA 168	U9100,U9110,U9200,U9210	CRITICAL	NAND_TYPE:256GB
335S00204	4	NAND,V3,128GBM,TOGG DDR2,256G,SSBGA 168	U9100,U9110,U9200,U9210	CRITICAL	NAND_TYPE:512GB
335S00205	4	NAND,V3,256GBM,TOGG DDR2,256G,SS,BGA 168	U9100,U9110,U9200,U9210	CRITICAL	NAND_TYPE:1TB
335S00219	4	NAND,V3,512GBM,TOGG DDR2,256G,SS,BGA 168	U9100,U9110,U9200,U9210	CRITICAL	NAND_TYPE:2TB

SSD Controller Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
339S00154	1	POP,POLARIS+4GBIT,SSD CTRL,A2,BGA516	U8605	CRITICAL	SSD_CTRL_TYPE:4GBIT
339S00155	1	POP,POLARIS+8GBIT,SSD CTRL,A2,BGA516	U8605	CRITICAL	SSD_CTRL_TYPE:8GBIT

SSD CONFIGURATIONS

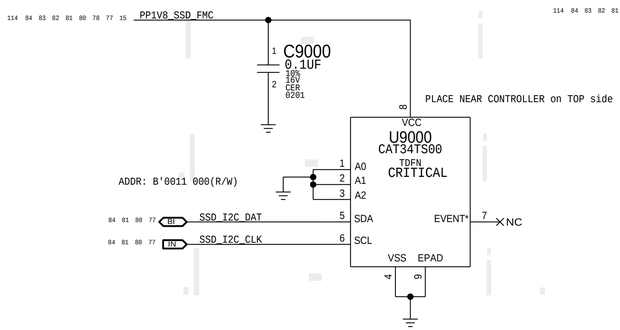
CAPACITY	NAND APN	CONTROLLER APN	R8980/GPIO8	R8981/GPIO9	R8928/GPIO10
128 GB	-	-	STUFF-0	STUFF-0	STUFF-0
256 GB	335S00149	339S00154 (A2 4GB DRAM)	NOSTUFF-1	STUFF-0	NOSTUFF-1
512 GB	335S00204	339S00154 (A2 4GB DRAM)	STUFF-0	NOSTUFF-1	NOSTUFF-1
1 TB	335S00205	339S00155 (A2 8GB DRAM)	NOSTUFF-1	NOSTUFF-1	NOSTUFF-1
2 TB	335S00219	339S00155 (A2 8GB DRAM)	NOSTUFF-1	NOSTUFF-1	STUFF-0

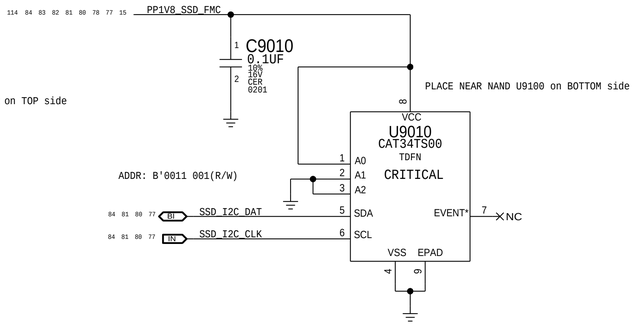
BOM_COST_GROUP=SSD

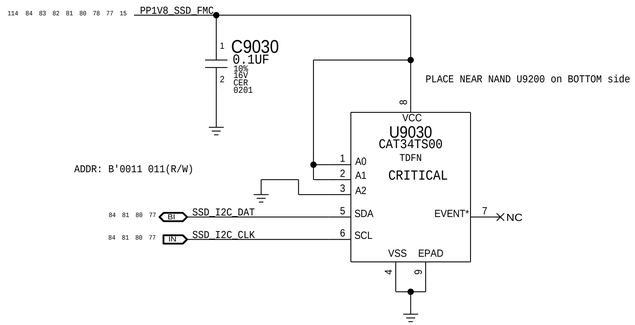
PAGE TITLE: Connector

Apple Inc.

DRAWING NUMBER: 051-00789
SIZE: D
REVISION: PROTO1A
BRANCH: dvt-fab10
PAGE: 89 OF 145
SHEET: 80 OF 121







BOM_COST_GROUP=SSD

PAGE TITLE

PAGE_TITLE=TEMP SENSORS

Apple Inc.

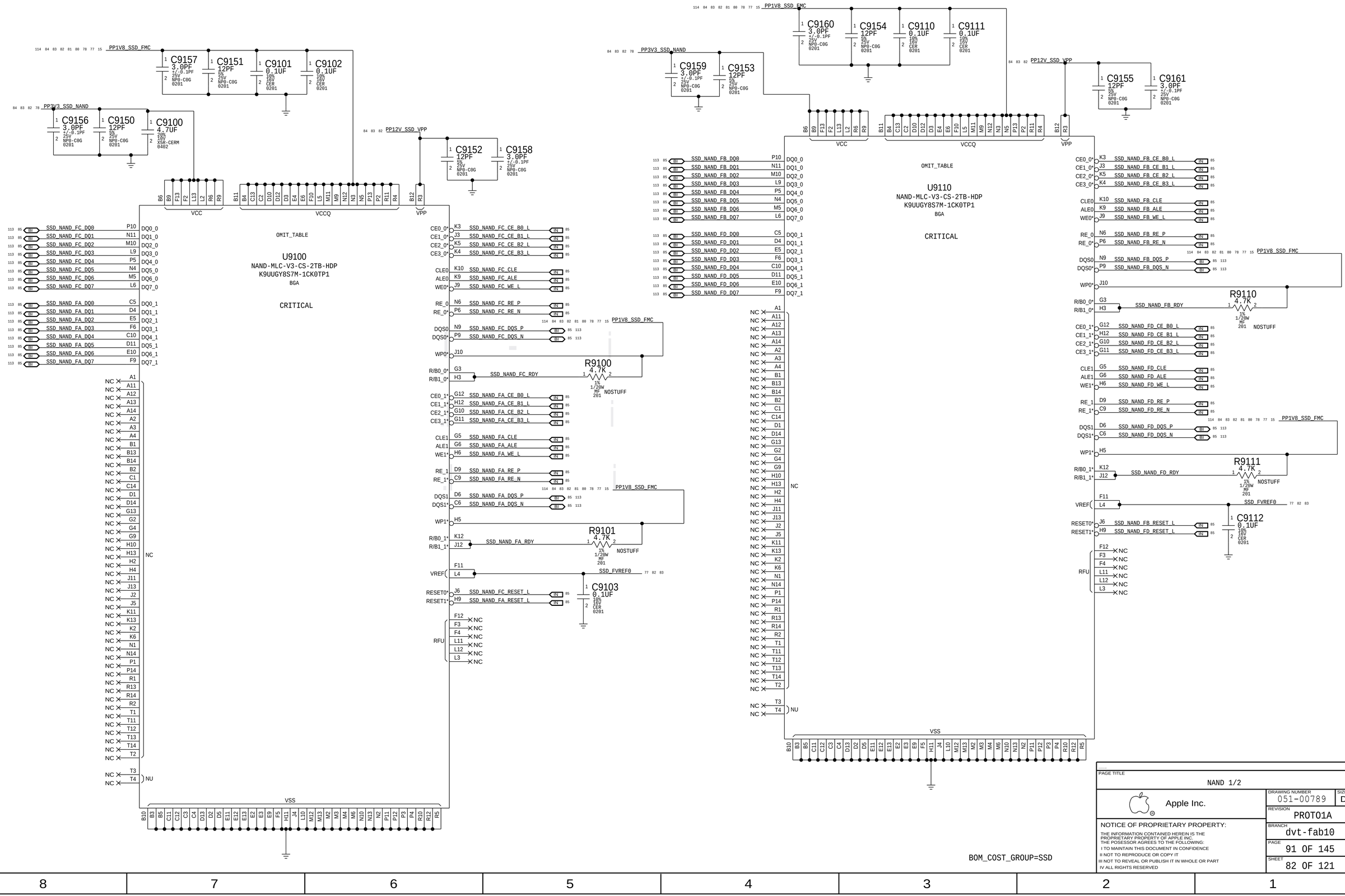
DRAWING NUMBER 051-00789 SIZE D

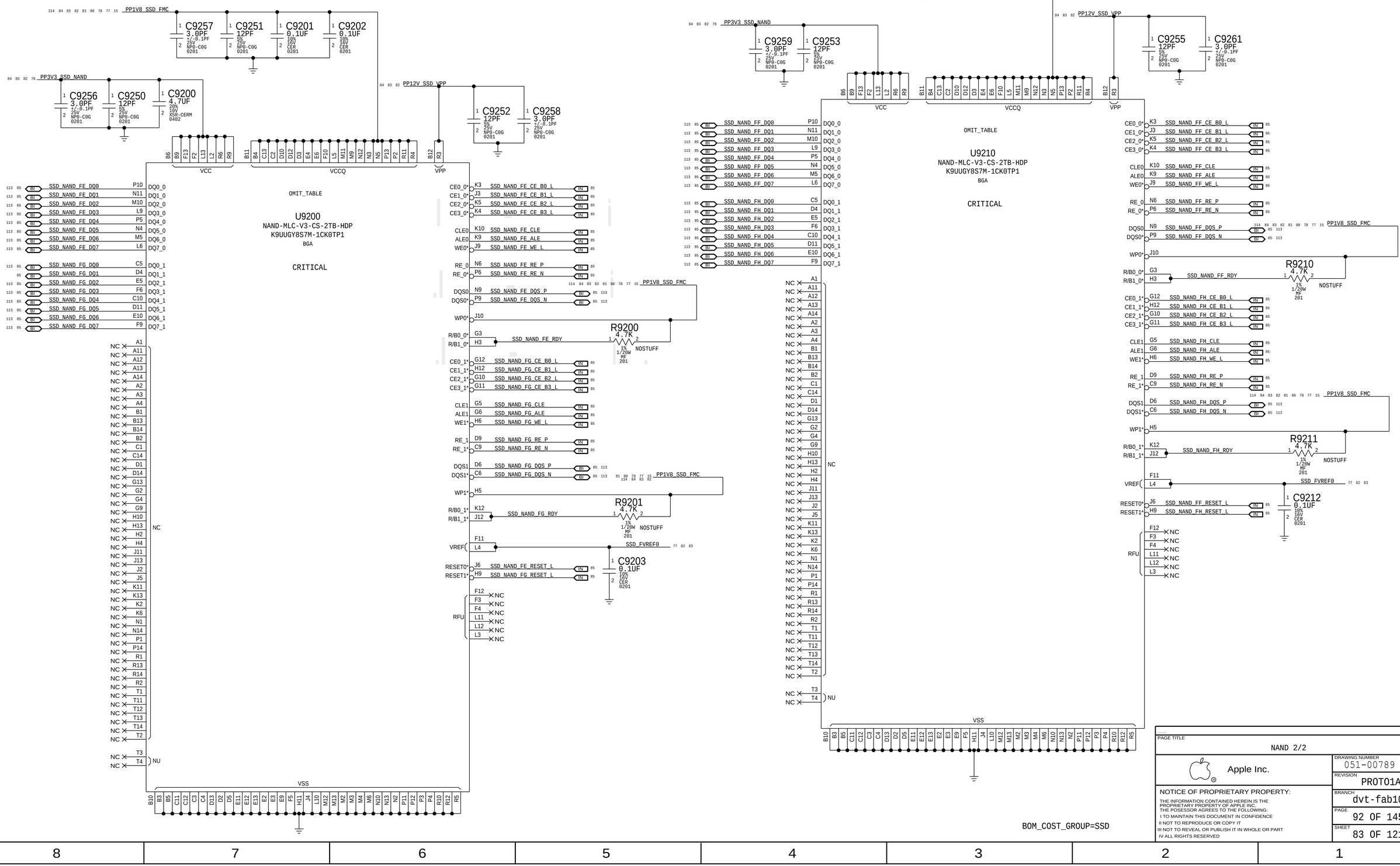
REVISION PROTO1A

BRANCH dvt-fab10

PAGE 90 OF 145

SHEET 81 OF 121


PP1V8_SSD_FMC
C9157 3.0PF +/-0.1PF 25V NP0-C0G 0201
C9151 12PF 5% 25V NP0-C0G 0201
C9101 0.1UF 10% 16V CER 0201
C9102 0.1UF 10% 16V CER 0201
PP3V3_SSD_NAND
C9156 3.0PF +/-0.1PF 25V NP0-C0G 0201
C9150 12PF 5% 25V NP0-C0G 0201
C9100 4.7UF 20% 10V X5R-CERM 0402
PP12V_SSD_VPP
C9152 12PF 5% 25V NP0-C0G 0201
C9158 3.0PF +/-0.1PF 25V NP0-C0G 0201
VCC
VCCQ
VPP
OMIT_TABLE
U9100
NAND-MLC-V3-CS-2TB-HDP
K9UUGY8S7M-1CK0TP1
BGA
CRITICAL
SSD_NAND_FC_DQ0
SSD_NAND_FC_DQ1
SSD_NAND_FC_DQ2
SSD_NAND_FC_DQ3
SSD_NAND_FC_DQ4
SSD_NAND_FC_DQ5
SSD_NAND_FC_DQ6
SSD_NAND_FC_DQ7
SSD_NAND_FA_DQ0
SSD_NAND_FA_DQ1
SSD_NAND_FA_DQ2
SSD_NAND_FA_DQ3
SSD_NAND_FA_DQ4
SSD_NAND_FA_DQ5
SSD_NAND_FA_DQ6
SSD_NAND_FA_DQ7
NC
NU
VSS
SSD_NAND_FC_CE_B0_L
SSD_NAND_FC_CE_B1_L
SSD_NAND_FC_CE_B2_L
SSD_NAND_FC_CE_B3_L
SSD_NAND_FC_CLE
SSD_NAND_FC_ALE
SSD_NAND_FC_WE_L
SSD_NAND_FC_RE_P
SSD_NAND_FC_RE_N
SSD_NAND_FC_DQS_P
SSD_NAND_FC_DQS_N
SSD_NAND_FC_RDY
R9100 4.7K 1% 1/20W MF 201 NOSTUFF
SSD_NAND_FA_CE_B0_L
SSD_NAND_FA_CE_B1_L
SSD_NAND_FA_CE_B2_L
SSD_NAND_FA_CE_B3_L
SSD_NAND_FA_CLE
SSD_NAND_FA_ALE
SSD_NAND_FA_WE_L
SSD_NAND_FA_RE_P
SSD_NAND_FA_RE_N
SSD_NAND_FA_DQS_P
SSD_NAND_FA_DQS_N
SSD_NAND_FA_RDY
R9101 4.7K 1% 1/20W MF 201 NOSTUFF
SSD_FVREF0
SSD_NAND_FC_RESET_L
SSD_NAND_FA_RESET_L
C9103 0.1UF 10% 16V CER 0201
RFU
PP1V8_SSD_FMC
C9160 3.0PF +/-0.1PF 25V NP0-C0G 0201
C9154 12PF 5% 25V NP0-C0G 0201
C9110 0.1UF 10% 16V CER 0201
C9111 0.1UF 10% 16V CER 0201
PP3V3_SSD_NAND
C9159 3.0PF +/-0.1PF 25V NP0-C0G 0201
C9153 12PF 5% 25V NP0-C0G 0201
PP12V_SSD_VPP
C9155 12PF 5% 25V NP0-C0G 0201
C9161 3.0PF +/-0.1PF 25V NP0-C0G 0201
OMIT_TABLE
U9110
NAND-MLC-V3-CS-2TB-HDP
K9UUGY8S7M-1CK0TP1
BGA
CRITICAL
SSD_NAND_FB_DQ0
SSD_NAND_FB_DQ1
SSD_NAND_FB_DQ2
SSD_NAND_FB_DQ3
SSD_NAND_FB_DQ4
SSD_NAND_FB_DQ5
SSD_NAND_FB_DQ6
SSD_NAND_FB_DQ7
SSD_NAND_FD_DQ0
SSD_NAND_FD_DQ1
SSD_NAND_FD_DQ2
SSD_NAND_FD_DQ3
SSD_NAND_FD_DQ4
SSD_NAND_FD_DQ5
SSD_NAND_FD_DQ6
SSD_NAND_FD_DQ7
NC
NU
VSS
SSD_NAND_FB_CE_B0_L
SSD_NAND_FB_CE_B1_L
SSD_NAND_FB_CE_B2_L
SSD_NAND_FB_CE_B3_L
SSD_NAND_FB_CLE
SSD_NAND_FB_ALE
SSD_NAND_FB_WE_L
SSD_NAND_FB_RE_P
SSD_NAND_FB_RE_N
SSD_NAND_FB_DQS_P
SSD_NAND_FB_DQS_N
SSD_NAND_FB_RDY
R9110 4.7K 1% 1/20W MF 201 NOSTUFF
SSD_NAND_FD_CE_B0_L
SSD_NAND_FD_CE_B1_L
SSD_NAND_FD_CE_B2_L
SSD_NAND_FD_CE_B3_L
SSD_NAND_FD_CLE
SSD_NAND_FD_ALE
SSD_NAND_FD_WE_L
SSD_NAND_FD_RE_P
SSD_NAND_FD_RE_N
SSD_NAND_FD_DQS_P
SSD_NAND_FD_DQS_N
SSD_NAND_FD_RDY
R9111 4.7K 1% 1/20W MF 201 NOSTUFF
SSD_FVREF0
SSD_NAND_FB_RESET_L
SSD_NAND_FD_RESET_L
C9112 0.1UF 10% 16V CER 0201
RFU
BOM_COST_GROUP=SSD
PAGE TITLE
NAND 1/2
Apple Inc.
DRAWING NUMBER 051-00789
SIZE D
REVISION PROTO1A
BRANCH dvt-fab10
PAGE 91 OF 145
SHEET 82 OF 121
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



PAGE TITLE

NAND 2/2

Apple Inc.

DRAWING NUMBER 051-00789

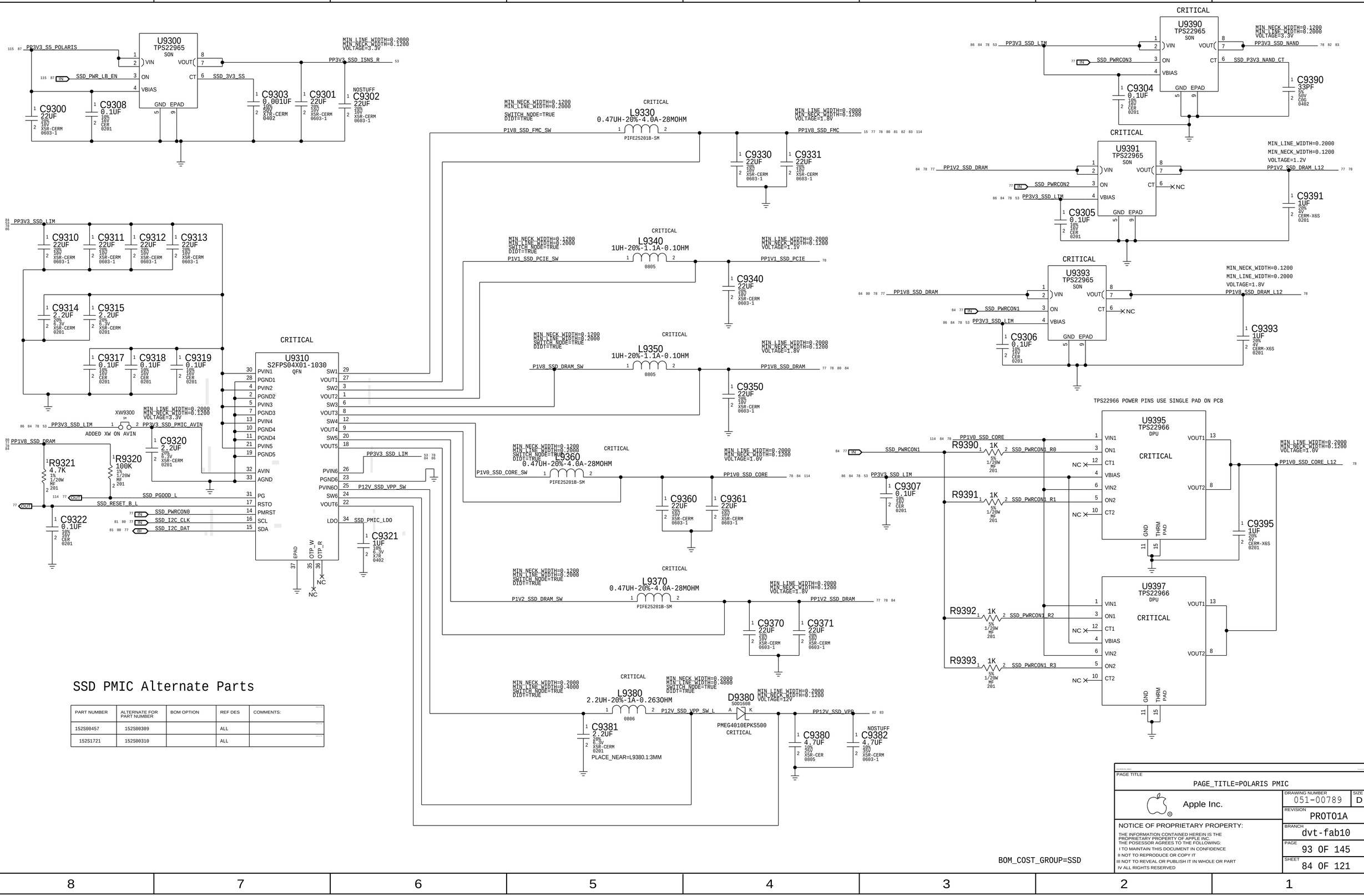
SIZE D

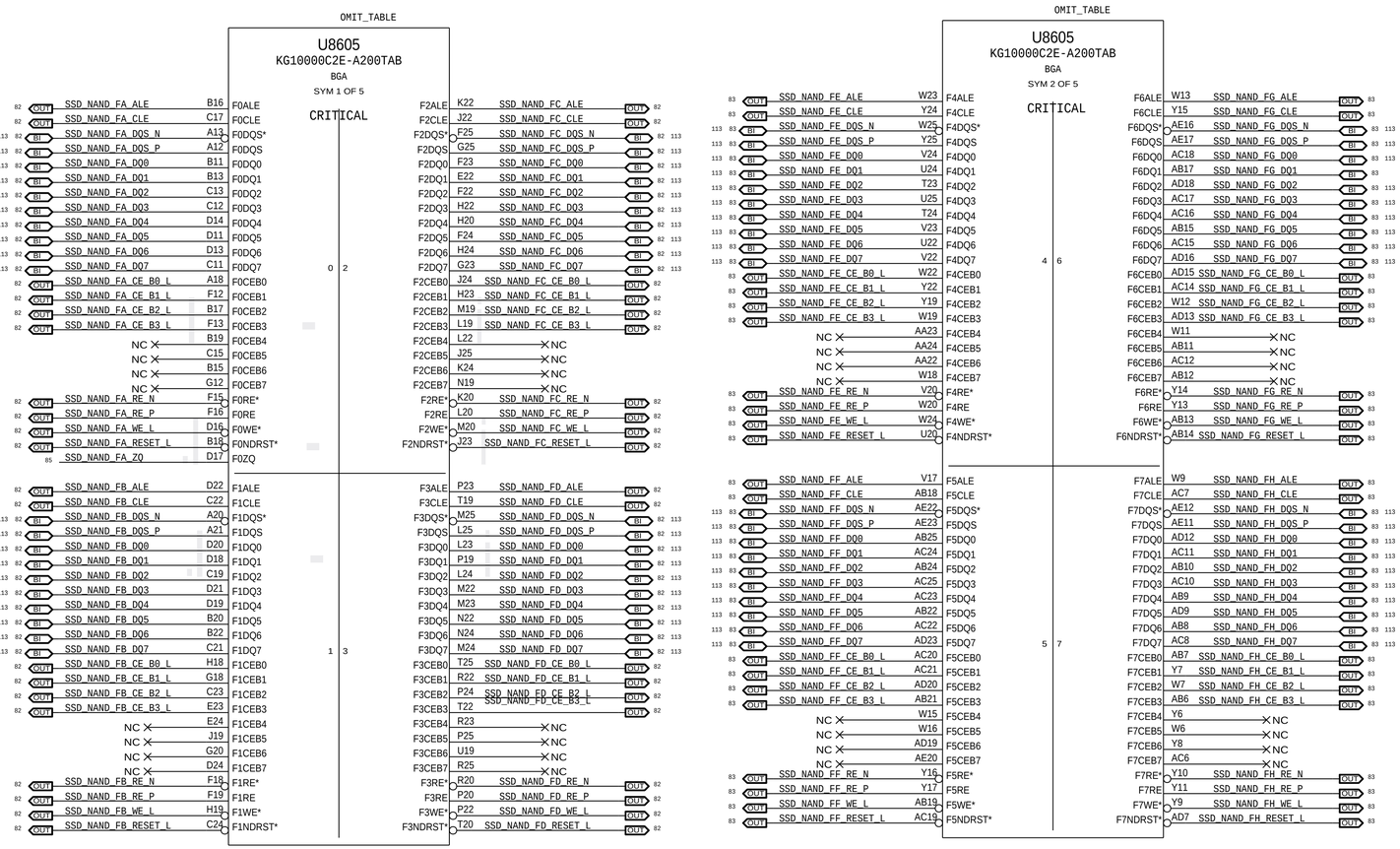
REVISION PR0T01A

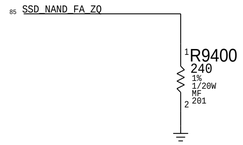
BRANCH dvt-fab10

PAGE 92 OF 145

SHEET 83 OF 121


U9300
TPS22965
SON
PP3V3_S5_POLARIS
SSD_PWR_LB_EN
SSD_3V3_SS
PP3V3_SSD_ISNS_R
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V
C9300 22UF
C9308 0.1UF
C9303 0.001UF
C9301 22UF
C9302 22UF NOSTUFF
U9310
S2FPS04X01-1030
QFN
PP3V3_SSD_LIM
XW9300
ADDED XW ON AVIN
PP3V3_SSD_PMIC_AVIN
PP1V8_SSD_DRAM
R9321 4.7K
R9320 100K
C9320 2.2UF
C9322 0.1UF
SSD_PGOOD_L
SSD_RESET_B_L
SSD_PWRCON0
SSD_I2C_CLK
SSD_I2C_DAT
PP3V3_SSD_LDO
P12V_SSD_VPP_SW
C9310 22UF
C9311 22UF
C9312 22UF
C9313 22UF
C9314 2.2UF
C9315 2.2UF
C9317 0.1UF
C9318 0.1UF
C9319 0.1UF
C9321 1UF
L9330 0.47UH-20%-4.0A-28MOHM
P1V8_SSD_FMC_SW
PP1V8_SSD_FMC
C9330 22UF
C9331 22UF
L9340 1UH-20%-1.1A-0.10HM
P1V1_SSD_PCIE_SW
PP1V1_SSD_PCIE
C9340 22UF
L9350 1UH-20%-1.1A-0.10HM
P1V8_SSD_DRAM_SW
PP1V8_SSD_DRAM
C9350 22UF
L9360 0.47UH-20%-4.0A-28MOHM
P1V0_SSD_CORE_SW
PP1V0_SSD_CORE
C9360 22UF
C9361 22UF
L9370 0.47UH-20%-4.0A-28MOHM
P1V2_SSD_DRAM_SW
PP1V2_SSD_DRAM
C9370 22UF
C9371 22UF
L9380 2.2UH-20%-1A-0.2630HM
D9380 PMEG4010EPKS500
P12V_SSD_VPP_SW_L
PP12V_SSD_VPP
C9380 4.7UF
C9382 4.7UF NOSTUFF
C9381 2.2UF
PLACE_NEAR=L9380.1:3MM
CRITICAL
U9390
TPS22965
SON
PP3V3_SSD_LIM
SSD_PWRCON3
PP3V3_SSD_NAND
SSD_P3V3_NAND_CT
C9304 0.1UF
C9390 33PF
U9391
TPS22965
SON
PP1V2_SSD_DRAM
SSD_PWRCON2
PP1V2_SSD_DRAM_L12
C9305 0.1UF
C9391 1UF
U9393
TPS22965
SON
PP1V8_SSD_DRAM
SSD_PWRCON1
PP1V8_SSD_DRAM_L12
C9306 0.1UF
C9393 1UF
TPS22966 POWER PINS USE SINGLE PAD ON PCB
U9395
TPS22966
DPU
PP1V0_SSD_CORE
SSD_PWRCON1
R9390 1K
R9391 1K
C9307 0.1UF
PP1V0_SSD_CORE_L12
C9395 1UF
U9397
TPS22966
DPU
R9392 1K
R9393 1K
SSD_PWRCON1_R2
SSD_PWRCON1_R3
SSD PMIC Alternate Parts
PART NUMBER
ALTERNATE FOR PART NUMBER
BOM OPTION
REF DES
COMMENTS:
152S00457
152S00309
ALL
152S1721
152S00310
ALL
BOM_COST_GROUP=SSD
PAGE TITLE
PAGE_TITLE=POLARIS PMIC
Apple Inc.
DRAWING NUMBER
051-00789
SIZE
D
REVISION
PROTO1A
BRANCH
dvt-fab10
PAGE
93 OF 145
SHEET
84 OF 121
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



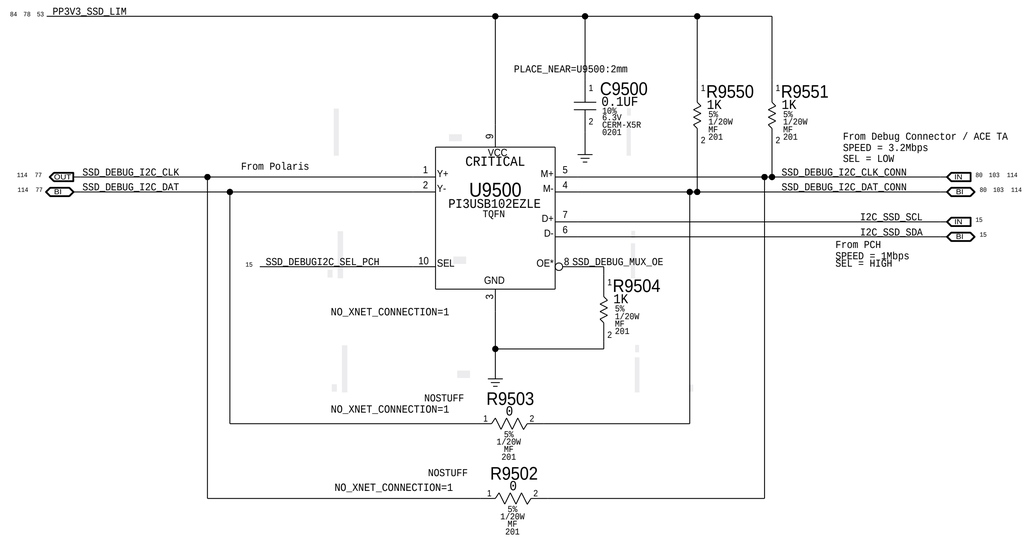


BOM_COST_GROUP=SSD

PAGE TITLE
SSD NAND VR

Apple Inc.

DRAWING NUMBER 051-00789
SIZE D
REVISION PR0T01A
BRANCH dvt-fab10
PAGE 94 OF 145
SHEET 85 OF 121



BOM_COST_GROUP=SSD

PAGE TITLE

SSD SUPPORT

Apple Inc.

DRAWING NUMBER 051-00789

SIZE D

REVISION PROTO1A

BRANCH dvt-fab10

PAGE 95 OF 145

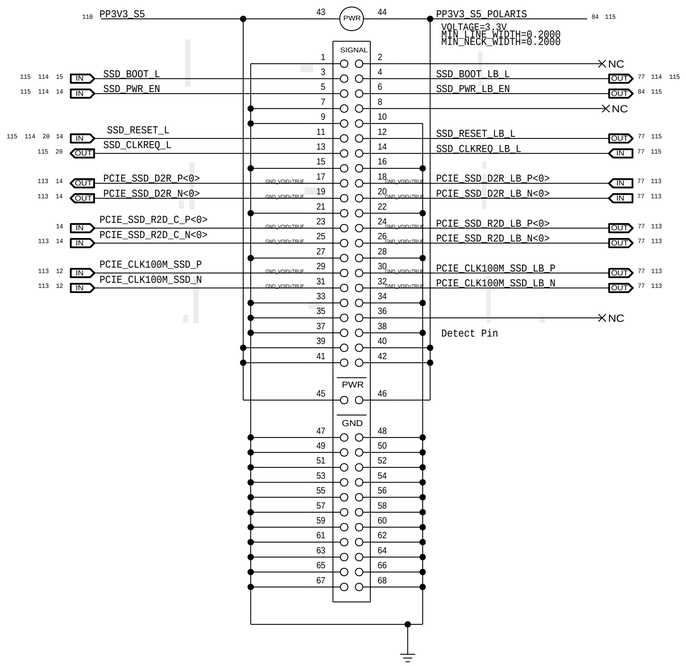
SHEET 86 OF 121

LIFEBOAT

J9600
20759-042E-02
F-ST-SM

PCH Side

SSD Side



BOM_COST_GROUP=SSD

SYNC_MASTER=X363_BBABADI SYNC_DATE=01/20/2016

PAGE TITLE

Lifeboat

Apple Inc.

DRAWING NUMBER 051-00789 SIZE D

REVISION PROTO1A

BRANCH dvt-fab10

PAGE 96 OF 145

SHEET 87 OF 121

8	7	6	5	4	3	2	1

D

C

B

A

PAGE TITLE

Constraints

Apple Inc.

DRAWING NUMBER 051-00789

SIZE D

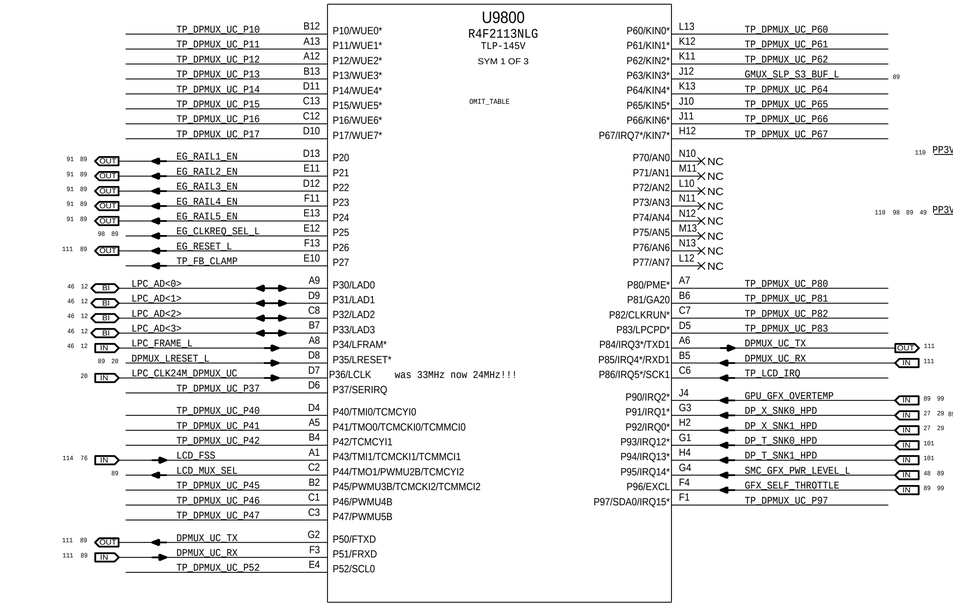
REVISION PROTO1A

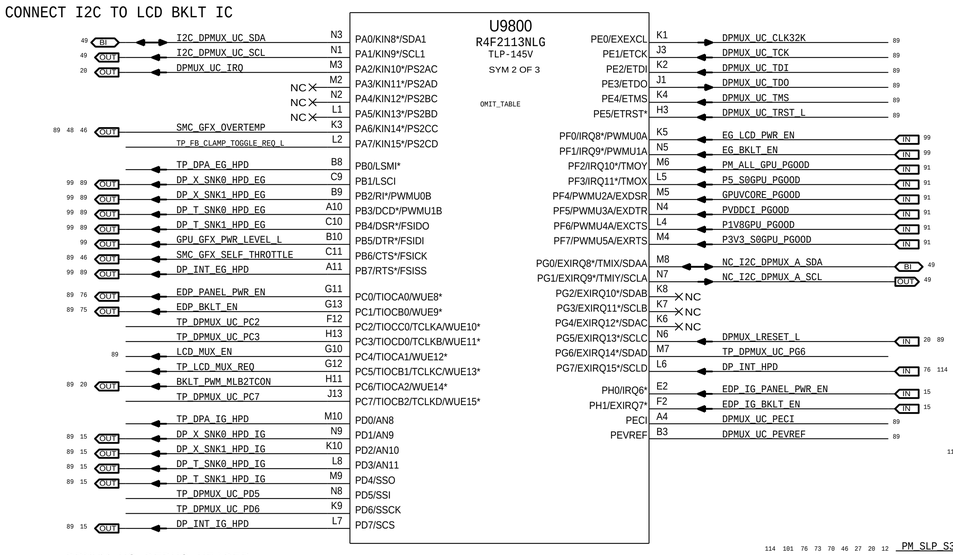
BRANCH dvt-fab10

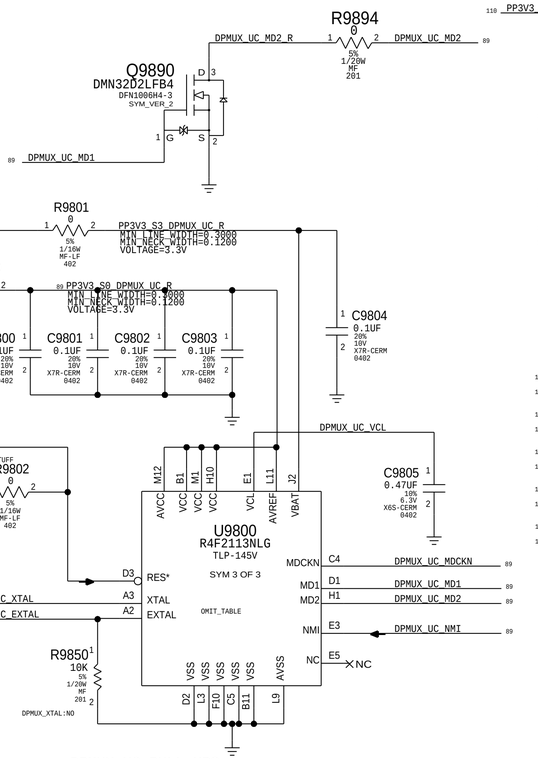
PAGE 97 OF 145

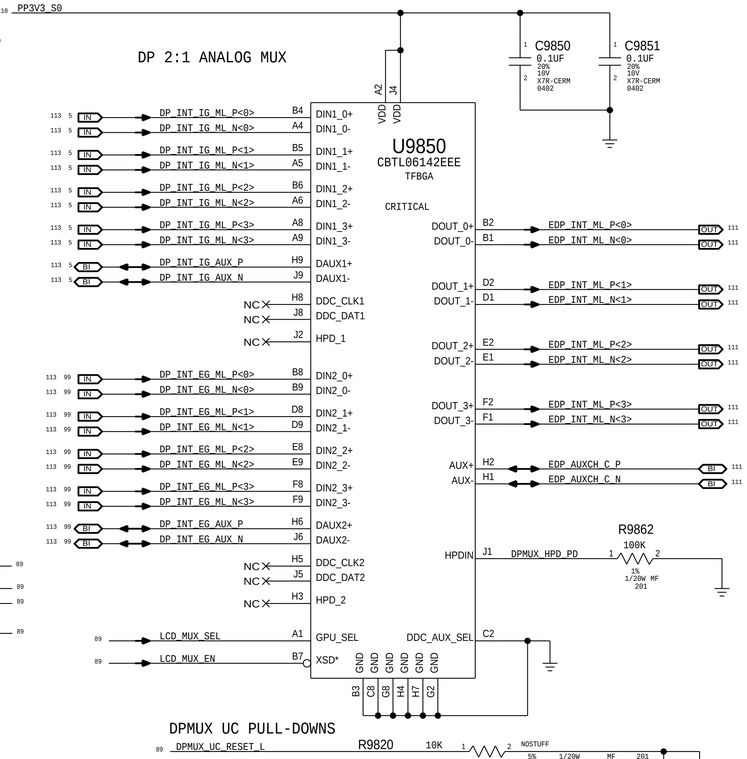
SHEET 88 OF 121

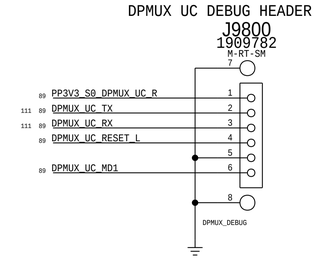
8 7 6 5 4 3 2 1

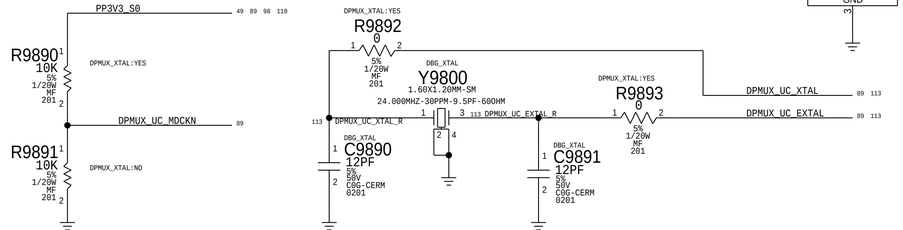


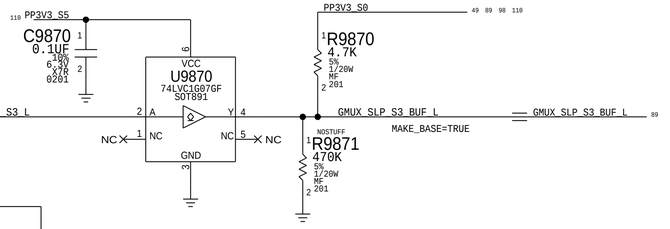


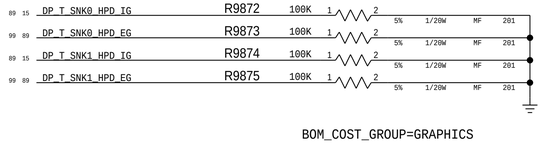












SYNC_MASTER=dpmux SYNC_DATE=08/22/2015

PAGE TITLE: eDP Mux

Apple Inc.

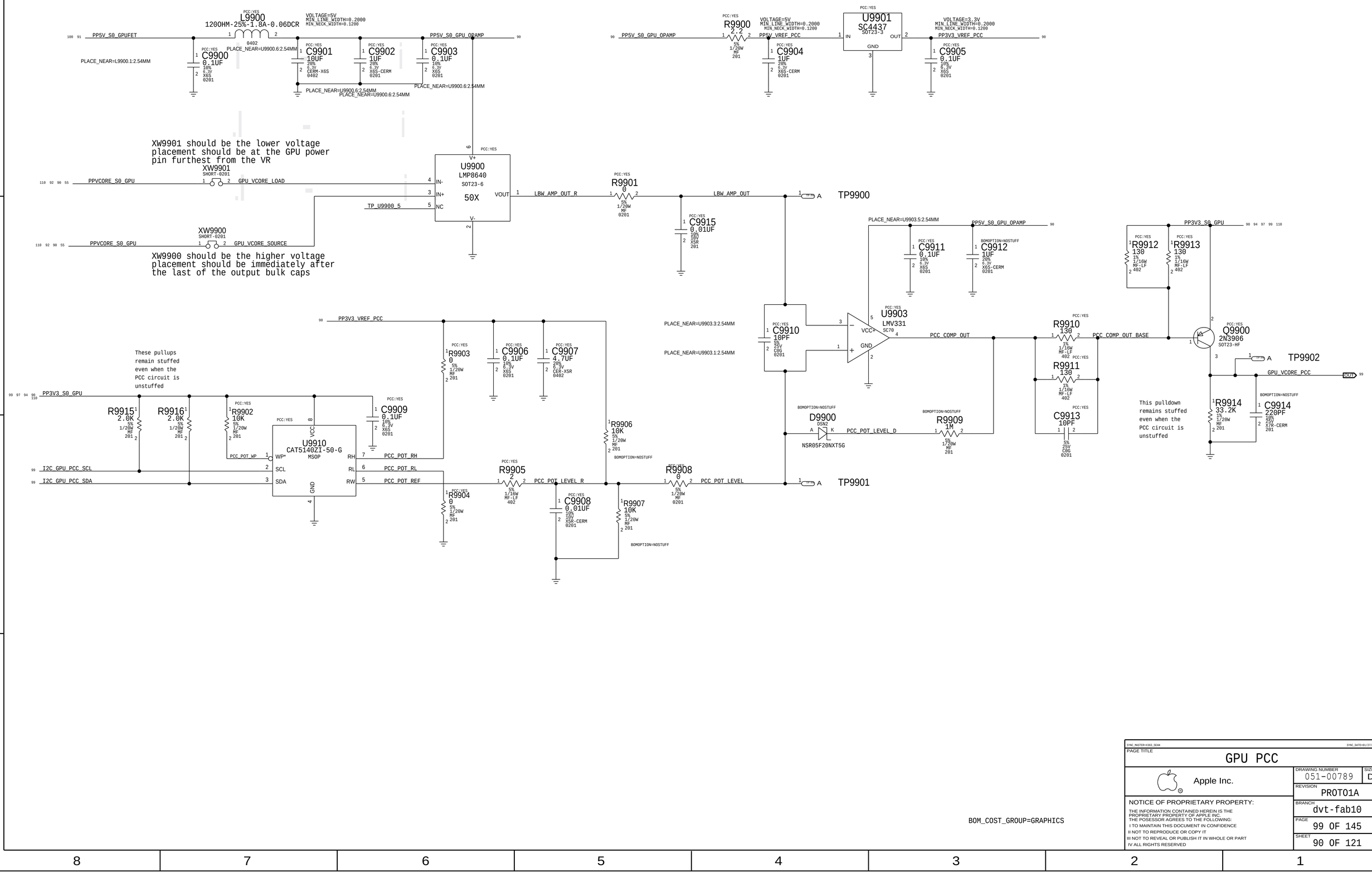
DRAWING NUMBER 051-00789 SIZE D

REVISION PROTO1A

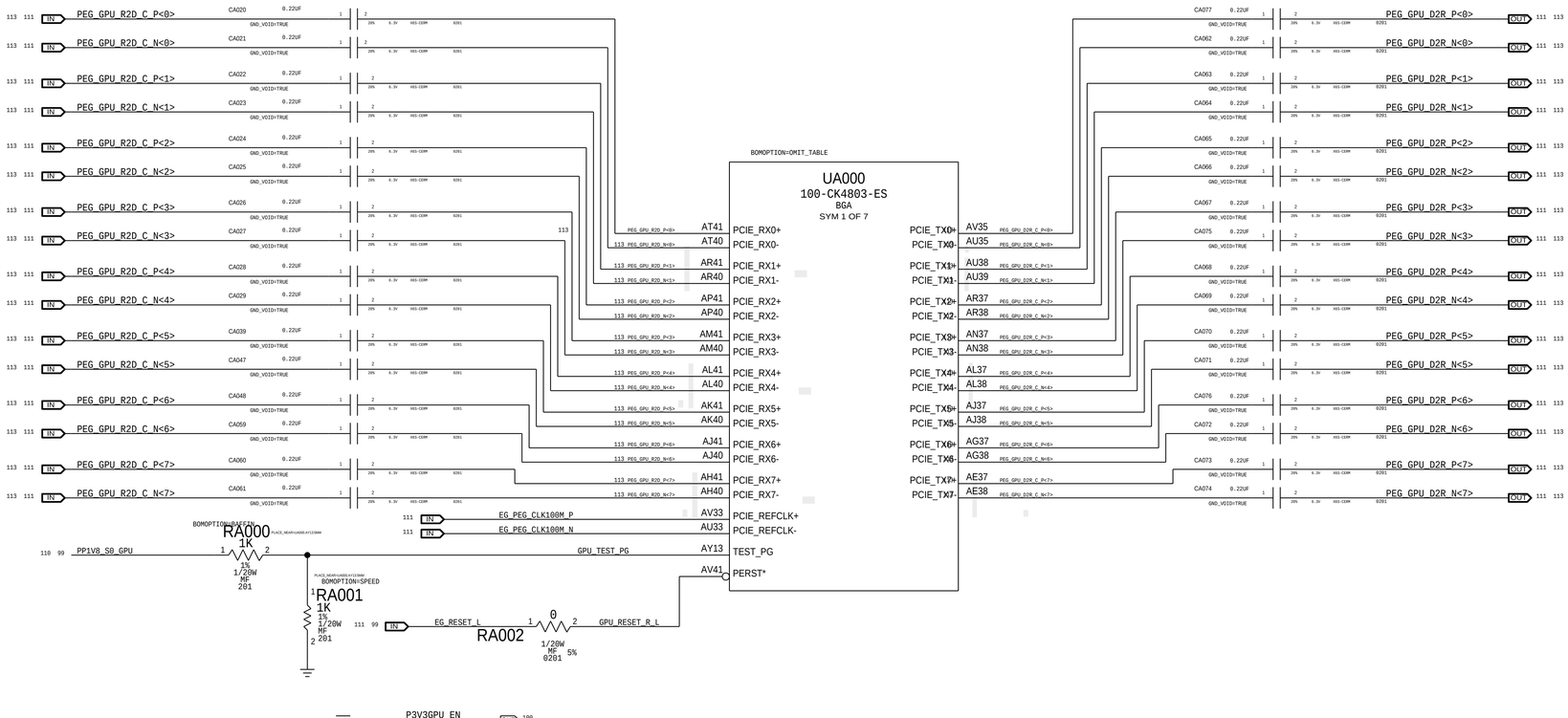
BRANCH dvt-fab10

PAGE 98 OF 145

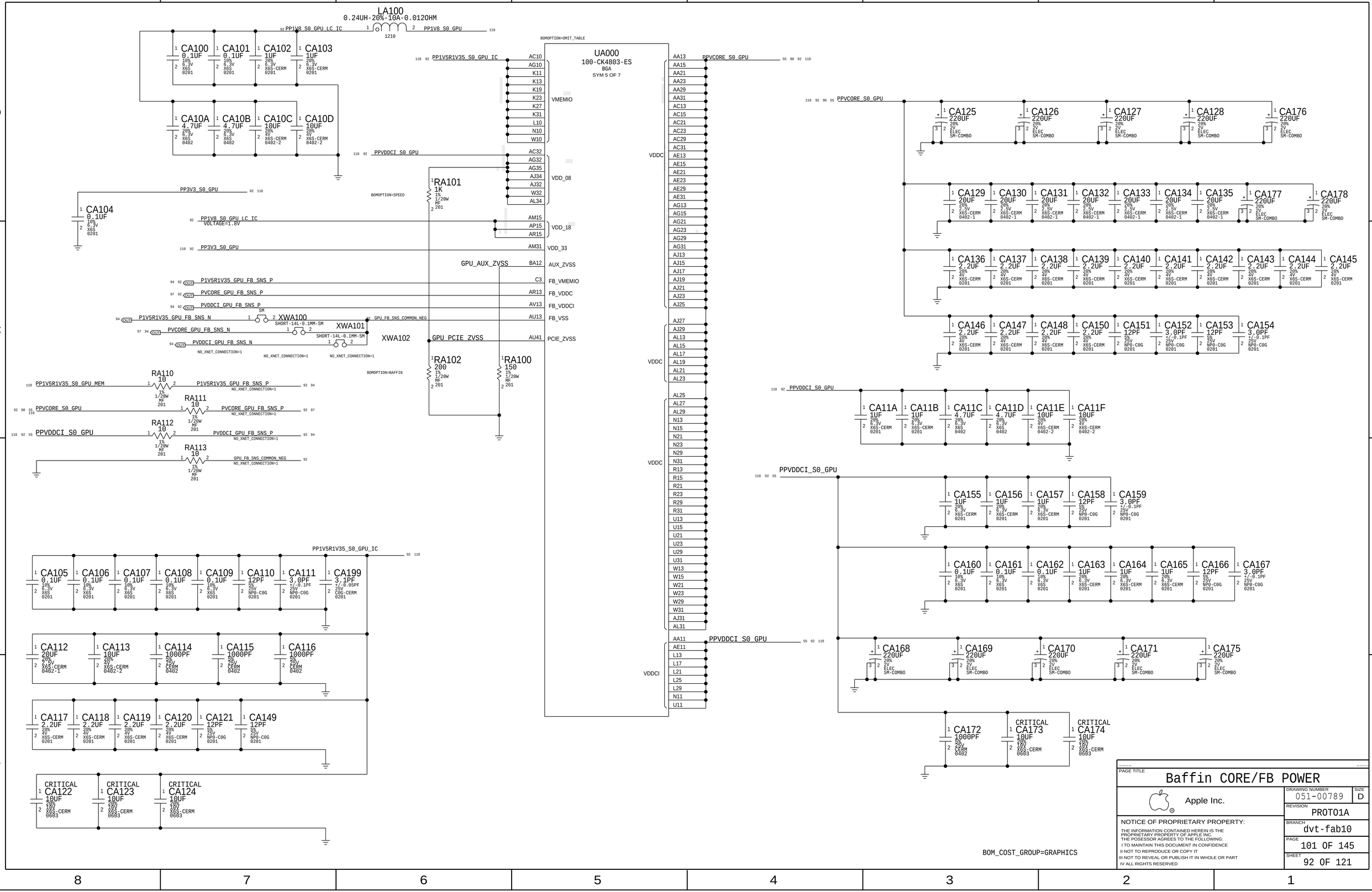
SHEET 89 OF 121

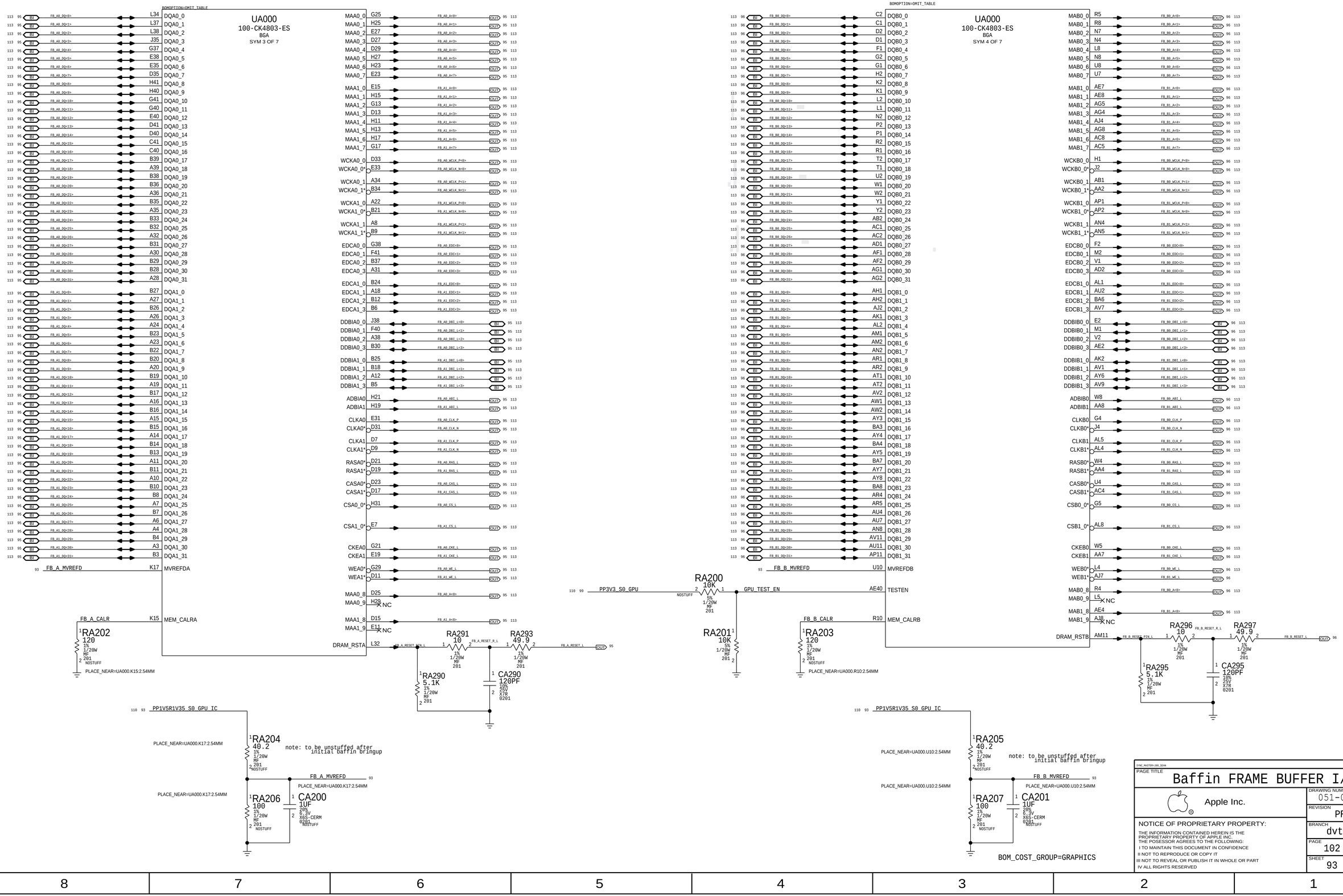


SYNC_MASTER=X863_SEAN	SYNC_DATE=01/27/2016
PAGE TITLE	GPU PCC
Apple Inc.	DRAWING NUMBER 051-00789 SIZE D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	REVISION PROTO1A BRANCH dvt-fab10 PAGE 99 OF 145 SHEET 90 OF 121



PAGE TITLE	BAFFIN PCI-E
Apple Inc.	DRAWING NUMBER 051-00789
	SIZE D
	REVISION PROTO1A
	BRANCH dvt-fab10
	PAGE 100 OF 145
	SHEET 91 OF 121


LA100
0.24UH-20%-10A-0.0120HM
PP1V8_S0_GPU_LC_IC
PP1V8_S0_GPU
CA100 0.1UF 10% 6.3V X6S 0201
CA101 0.1UF 10% 6.3V X6S 0201
CA102 1UF 20% 6.3V X6S-CERM 0201
CA103 1UF 20% 6.3V X6S-CERM 0201
CA10A 4.7UF 20% 6.3V X6S 0402
CA10B 4.7UF 20% 6.3V X6S 0402
CA10C 10UF 20% 4V X6S-CERM 0402-2
CA10D 10UF 20% 4V X6S-CERM 0402-2
CA104 0.1UF 10% 6.3V X6S 0201
PP3V3_S0_GPU
UA000
100-CK4803-ES
BGA
SYM 5 OF 7
BOMOPTION=OMIT_TABLE
PP1V5R1V35_S0_GPU_IC
PPVDDCI_S0_GPU
RA101 1K 1% 1/20W MF 201
BOMOPTION=SPEED
PP1V8_S0_GPU_LC_IC
VOLTAGE=1.8V
PP3V3_S0_GPU
GPU_AUX_ZVSS
P1V5R1V35_GPU_FB_SNS_P
PVCORE_GPU_FB_SNS_P
PVDDCI_GPU_FB_SNS_P
P1V5R1V35_GPU_FB_SNS_N
PVCORE_GPU_FB_SNS_N
PVDDCI_GPU_FB_SNS_N
XWA100
SHORT-14L-0.1MM-SM
XWA101
XWA102
GPU_FB_SNS_COMMON_NEG
GPU_PCIE_ZVSS
RA102 200 1% 1/20W MF 201
RA100 150 1% 1/20W MF 201
BOMOPTION=BAFFIN
NO_XNET_CONNECTION=1
RA110 10 1% 1/20W MF 201
RA111 10 1% 1/20W MF 201
RA112 10 1% 1/20W MF 201
RA113 10 1% 1/20W MF 201
PP1V5R1V35_S0_GPU_MEM
PPVCORE_S0_GPU
PPVDDCI_S0_GPU
VMEMIO
VDD_08
VDD_18
VDD_33
AUX_ZVSS
FB_VMEMIO
FB_VDDC
FB_VDDCI
FB_VSS
PCIE_ZVSS
VDDC
VDDCI
PPVCORE_S0_GPU
PPVDDCI_S0_GPU
CA125 220UF 20% 2V ELEC SM-COMBO
CA126 220UF 20% 2V ELEC SM-COMBO
CA127 220UF 20% 2V ELEC SM-COMBO
CA128 220UF 20% 2V ELEC SM-COMBO
CA176 220UF 20% 2V ELEC SM-COMBO
CA129 20UF 20% 2.5V X6S-CERM 0402-1
CA130 20UF 20% 2.5V X6S-CERM 0402-1
CA131 20UF 20% 2.5V X6S-CERM 0402-1
CA132 20UF 20% 2.5V X6S-CERM 0402-1
CA133 20UF 20% 2.5V X6S-CERM 0402-1
CA134 20UF 20% 2.5V X6S-CERM 0402-1
CA135 20UF 20% 2.5V X6S-CERM 0402-1
CA177 220UF 20% 2V ELEC SM-COMBO
CA178 220UF 20% 2V ELEC SM-COMBO
CA136 2.2UF 20% 4V X6S-CERM 0201
CA137 2.2UF 20% 4V X6S-CERM 0201
CA138 2.2UF 20% 4V X6S-CERM 0201
CA139 2.2UF 20% 4V X6S-CERM 0201
CA140 2.2UF 20% 4V X6S-CERM 0201
CA141 2.2UF 20% 4V X6S-CERM 0201
CA142 2.2UF 20% 4V X6S-CERM 0201
CA143 2.2UF 20% 4V X6S-CERM 0201
CA144 2.2UF 20% 4V X6S-CERM 0201
CA145 2.2UF 20% 4V X6S-CERM 0201
CA146 2.2UF 20% 4V X6S-CERM 0201
CA147 2.2UF 20% 4V X6S-CERM 0201
CA148 2.2UF 20% 4V X6S-CERM 0201
CA150 2.2UF 20% 4V X6S-CERM 0201
CA151 12PF 5% 25V NP0-C0G 0201
CA152 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA153 12PF 5% 25V NP0-C0G 0201
CA154 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA11A 1UF 20% 6.3V X6S-CERM 0201
CA11B 1UF 20% 6.3V X6S-CERM 0201
CA11C 4.7UF 20% 6.3V X6S 0402
CA11D 4.7UF 20% 6.3V X6S 0402
CA11E 10UF 20% 4V X6S-CERM 0402-2
CA11F 10UF 20% 4V X6S-CERM 0402-2
CA155 1UF 20% 6.3V X6S-CERM 0201
CA156 1UF 20% 6.3V X6S-CERM 0201
CA157 1UF 20% 6.3V X6S-CERM 0201
CA158 12PF 5% 25V NP0-C0G 0201
CA159 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA160 0.1UF 10% 6.3V X6S 0201
CA161 0.1UF 10% 6.3V X6S 0201
CA162 0.1UF 10% 6.3V X6S 0201
CA163 1UF 20% 6.3V X6S-CERM 0201
CA164 1UF 20% 6.3V X6S-CERM 0201
CA165 1UF 20% 6.3V X6S-CERM 0201
CA166 12PF 5% 25V NP0-C0G 0201
CA167 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA168 220UF 20% 2V ELEC SM-COMBO
CA169 220UF 20% 2V ELEC SM-COMBO
CA170 220UF 20% 2V ELEC SM-COMBO
CA171 220UF 20% 2V ELEC SM-COMBO
CA175 220UF 20% 2V ELEC SM-COMBO
CA172 1000PF 5% 25V C0G 0402
CRITICAL CA173 10UF 20% 10V X6S-CERM 0603
CRITICAL CA174 10UF 20% 10V X6S-CERM 0603
PPVDDCI_S0_GPU
CA105 0.1UF 10% 6.3V X6S 0201
CA106 0.1UF 10% 6.3V X6S 0201
CA107 0.1UF 10% 6.3V X6S 0201
CA108 0.1UF 10% 6.3V X6S 0201
CA109 0.1UF 10% 6.3V X6S 0201
CA110 12PF 5% 25V NP0-C0G 0201
CA111 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA199 3.1PF +/-0.05PF 25V C0G-CERM 0201
CA112 20UF 20% 2.5V X6S-CERM 0402-1
CA113 10UF 20% 4V X6S-CERM 0402-2
CA114 1000PF 5% 25V C0G 0402
CA115 1000PF 5% 25V C0G 0402
CA116 1000PF 5% 25V C0G 0402
CA117 2.2UF 20% 4V X6S-CERM 0201
CA118 2.2UF 20% 4V X6S-CERM 0201
CA119 2.2UF 20% 4V X6S-CERM 0201
CA120 2.2UF 20% 4V X6S-CERM 0201
CA121 12PF 5% 25V NP0-C0G 0201
CA149 12PF 5% 25V NP0-C0G 0201
CRITICAL CA122 10UF 20% 10V X6S-CERM 0603
CRITICAL CA123 10UF 20% 10V X6S-CERM 0603
CRITICAL CA124 10UF 20% 10V X6S-CERM 0603
BOM_COST_GROUP=GRAPHICS
PAGE TITLE
Baffin CORE/FB POWER
Apple Inc.
DRAWING NUMBER 051-00789
SIZE D
REVISION PROTO1A
BRANCH dvt-fab10
PAGE 101 OF 145
SHEET 92 OF 121
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED


BOMOPTION=OMIT_TABLE
UA000
100-CK4803-ES
BGA
SYM 3 OF 7
FB_A0_DQ<0>
FB_A0_DQ<1>
FB_A0_DQ<2>
FB_A0_DQ<3>
FB_A0_DQ<4>
FB_A0_DQ<5>
FB_A0_DQ<6>
FB_A0_DQ<7>
FB_A0_DQ<8>
FB_A0_DQ<9>
FB_A0_DQ<10>
FB_A0_DQ<11>
FB_A0_DQ<12>
FB_A0_DQ<13>
FB_A0_DQ<14>
FB_A0_DQ<15>
FB_A0_DQ<16>
FB_A0_DQ<17>
FB_A0_DQ<18>
FB_A0_DQ<19>
FB_A0_DQ<20>
FB_A0_DQ<21>
FB_A0_DQ<22>
FB_A0_DQ<23>
FB_A0_DQ<24>
FB_A0_DQ<25>
FB_A0_DQ<26>
FB_A0_DQ<27>
FB_A0_DQ<28>
FB_A0_DQ<29>
FB_A0_DQ<30>
FB_A0_DQ<31>
DQA0_0
DQA0_1
DQA0_2
DQA0_3
DQA0_4
DQA0_5
DQA0_6
DQA0_7
DQA0_8
DQA0_9
DQA0_10
DQA0_11
DQA0_12
DQA0_13
DQA0_14
DQA0_15
DQA0_16
DQA0_17
DQA0_18
DQA0_19
DQA0_20
DQA0_21
DQA0_22
DQA0_23
DQA0_24
DQA0_25
DQA0_26
DQA0_27
DQA0_28
DQA0_29
DQA0_30
DQA0_31
FB_A1_DQ<0>
FB_A1_DQ<1>
FB_A1_DQ<2>
FB_A1_DQ<3>
FB_A1_DQ<4>
FB_A1_DQ<5>
FB_A1_DQ<6>
FB_A1_DQ<7>
FB_A1_DQ<8>
FB_A1_DQ<9>
FB_A1_DQ<10>
FB_A1_DQ<11>
FB_A1_DQ<12>
FB_A1_DQ<13>
FB_A1_DQ<14>
FB_A1_DQ<15>
FB_A1_DQ<16>
FB_A1_DQ<17>
FB_A1_DQ<18>
FB_A1_DQ<19>
FB_A1_DQ<20>
FB_A1_DQ<21>
FB_A1_DQ<22>
FB_A1_DQ<23>
FB_A1_DQ<24>
FB_A1_DQ<25>
FB_A1_DQ<26>
FB_A1_DQ<27>
FB_A1_DQ<28>
FB_A1_DQ<29>
FB_A1_DQ<30>
FB_A1_DQ<31>
DQA1_0
DQA1_1
DQA1_2
DQA1_3
DQA1_4
DQA1_5
DQA1_6
DQA1_7
DQA1_8
DQA1_9
DQA1_10
DQA1_11
DQA1_12
DQA1_13
DQA1_14
DQA1_15
DQA1_16
DQA1_17
DQA1_18
DQA1_19
DQA1_20
DQA1_21
DQA1_22
DQA1_23
DQA1_24
DQA1_25
DQA1_26
DQA1_27
DQA1_28
DQA1_29
DQA1_30
DQA1_31
FB_A_MVREFD
MVREFDA
MAA0_0
MAA0_1
MAA0_2
MAA0_3
MAA0_4
MAA0_5
MAA0_6
MAA0_7
MAA1_0
MAA1_1
MAA1_2
MAA1_3
MAA1_4
MAA1_5
MAA1_6
MAA1_7
WCKA0_0
WCKA0_0*
WCKA0_1
WCKA0_1*
WCKA1_0
WCKA1_0*
WCKA1_1
WCKA1_1*
EDCA0_0
EDCA0_1
EDCA0_2
EDCA0_3
EDCA1_0
EDCA1_1
EDCA1_2
EDCA1_3
DDBIA0_0
DDBIA0_1
DDBIA0_2
DDBIA0_3
DDBIA1_0
DDBIA1_1
DDBIA1_2
DDBIA1_3
ADBIA0
ADBIA1
CLKA0
CLKA0*
CLKA1
CLKA1*
RASA0*
RASA1*
CASA0*
CASA1*
CSA0_0*
CSA1_0*
CKEA0
CKEA1
WEA0*
WEA1*
MAA0_8
MAA0_9
MAA1_8
MAA1_9
DRAM_RSTA
FB_A_CALR
MEM_CALRA
RA202
120
1%
1/20W
MF
201
NOSTUFF
PLACE_NEAR=UA000.K15:2.54MM
FB_A_RESET_PIN_L
RA291
10
FB_A_RESET_R_L
RA293
49.9
FB_A_RESET_L
RA290
5.1K
CA290
120PF
10%
25V
X7R
0201
PP1V5R1V35_S0_GPU_IC
PLACE_NEAR=UA000.K17:2.54MM
RA204
40.2
note: to be unstuffed after initial baffin bringup
RA206
100
CA200
1UF
20%
6.3V
X6S-CERM
0201
BOMOPTION=OMIT_TABLE
UA000
100-CK4803-ES
BGA
SYM 4 OF 7
FB_B0_DQ<0>
FB_B0_DQ<1>
FB_B0_DQ<2>
FB_B0_DQ<3>
FB_B0_DQ<4>
FB_B0_DQ<5>
FB_B0_DQ<6>
FB_B0_DQ<7>
FB_B0_DQ<8>
FB_B0_DQ<9>
FB_B0_DQ<10>
FB_B0_DQ<11>
FB_B0_DQ<12>
FB_B0_DQ<13>
FB_B0_DQ<14>
FB_B0_DQ<15>
FB_B0_DQ<16>
FB_B0_DQ<17>
FB_B0_DQ<18>
FB_B0_DQ<19>
FB_B0_DQ<20>
FB_B0_DQ<21>
FB_B0_DQ<22>
FB_B0_DQ<23>
FB_B0_DQ<24>
FB_B0_DQ<25>
FB_B0_DQ<26>
FB_B0_DQ<27>
FB_B0_DQ<28>
FB_B0_DQ<29>
FB_B0_DQ<30>
FB_B0_DQ<31>
DQB0_0
DQB0_1
DQB0_2
DQB0_3
DQB0_4
DQB0_5
DQB0_6
DQB0_7
DQB0_8
DQB0_9
DQB0_10
DQB0_11
DQB0_12
DQB0_13
DQB0_14
DQB0_15
DQB0_16
DQB0_17
DQB0_18
DQB0_19
DQB0_20
DQB0_21
DQB0_22
DQB0_23
DQB0_24
DQB0_25
DQB0_26
DQB0_27
DQB0_28
DQB0_29
DQB0_30
DQB0_31
FB_B1_DQ<0>
FB_B1_DQ<1>
FB_B1_DQ<2>
FB_B1_DQ<3>
FB_B1_DQ<4>
FB_B1_DQ<5>
FB_B1_DQ<6>
FB_B1_DQ<7>
FB_B1_DQ<8>
FB_B1_DQ<9>
FB_B1_DQ<10>
FB_B1_DQ<11>
FB_B1_DQ<12>
FB_B1_DQ<13>
FB_B1_DQ<14>
FB_B1_DQ<15>
FB_B1_DQ<16>
FB_B1_DQ<17>
FB_B1_DQ<18>
FB_B1_DQ<19>
FB_B1_DQ<20>
FB_B1_DQ<21>
FB_B1_DQ<22>
FB_B1_DQ<23>
FB_B1_DQ<24>
FB_B1_DQ<25>
FB_B1_DQ<26>
FB_B1_DQ<27>
FB_B1_DQ<28>
FB_B1_DQ<29>
FB_B1_DQ<30>
FB_B1_DQ<31>
DQB1_0
DQB1_1
DQB1_2
DQB1_3
DQB1_4
DQB1_5
DQB1_6
DQB1_7
DQB1_8
DQB1_9
DQB1_10
DQB1_11
DQB1_12
DQB1_13
DQB1_14
DQB1_15
DQB1_16
DQB1_17
DQB1_18
DQB1_19
DQB1_20
DQB1_21
DQB1_22
DQB1_23
DQB1_24
DQB1_25
DQB1_26
DQB1_27
DQB1_28
DQB1_29
DQB1_30
DQB1_31
FB_B_MVREFD
MVREFDB
MAB0_0
MAB0_1
MAB0_2
MAB0_3
MAB0_4
MAB0_5
MAB0_6
MAB0_7
MAB1_0
MAB1_1
MAB1_2
MAB1_3
MAB1_4
MAB1_5
MAB1_6
MAB1_7
WCKB0_0
WCKB0_0*
WCKB0_1
WCKB0_1*
WCKB1_0
WCKB1_0*
WCKB1_1
WCKB1_1*
EDCB0_0
EDCB0_1
EDCB0_2
EDCB0_3
EDCB1_0
EDCB1_1
EDCB1_2
EDCB1_3
DDBIB0_0
DDBIB0_1
DDBIB0_2
DDBIB0_3
DDBIB1_0
DDBIB1_1
DDBIB1_2
DDBIB1_3
ADBIB0
ADBIB1
CLKB0
CLKB0*
CLKB1
CLKB1*
RASB0*
RASB1*
CASB0*
CASB1*
CSB0_0*
CSB1_0*
CKEB0
CKEB1
WEB0*
WEB1*
MAB0_8
MAB0_9
MAB1_8
MAB1_9
DRAM_RSTB
FB_B_CALR
MEM_CALRB
RA203
120
RA200
10K
NOSTUFF
PP3V3_S0_GPU
GPU_TEST_EN
TESTEN
RA201
10K
RA296
10
RA297
49.9
RA295
5.1K
CA295
120PF
PP1V5R1V35_S0_GPU_IC
PLACE_NEAR=UA000.U10:2.54MM
RA205
40.2
note: to be unstuffed after initial baffin bringup
RA207
100
CA201
1UF
BOM_COST_GROUP=GRAPHICS
SYNC_MASTER=J80_SEAN
SYNC_DATE=04/29/2015
PAGE TITLE
Baffin FRAME BUFFER I/F
Apple Inc.
DRAWING NUMBER
051-00789
SIZE
D
REVISION
PROTO1A
BRANCH
dvt-fab10
PAGE
102 OF 145
SHEET
93 OF 121
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PAGE TITLE

Baffin 1V05 GPU / 1V35 FB Power Supply

Apple Inc.

DRAWING NUMBER 051-00789 SIZE D

REVISION PROTO1A

BRANCH dvt-fab10

PAGE 103 OF 145

SHEET 94 OF 121

8 7 6 5 4 3 2 1

D C B A

UA400
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)
OMIT_TABLE

UA450
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)
OMIT_TABLE

UA400
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(2 OF 2)
OMIT_TABLE

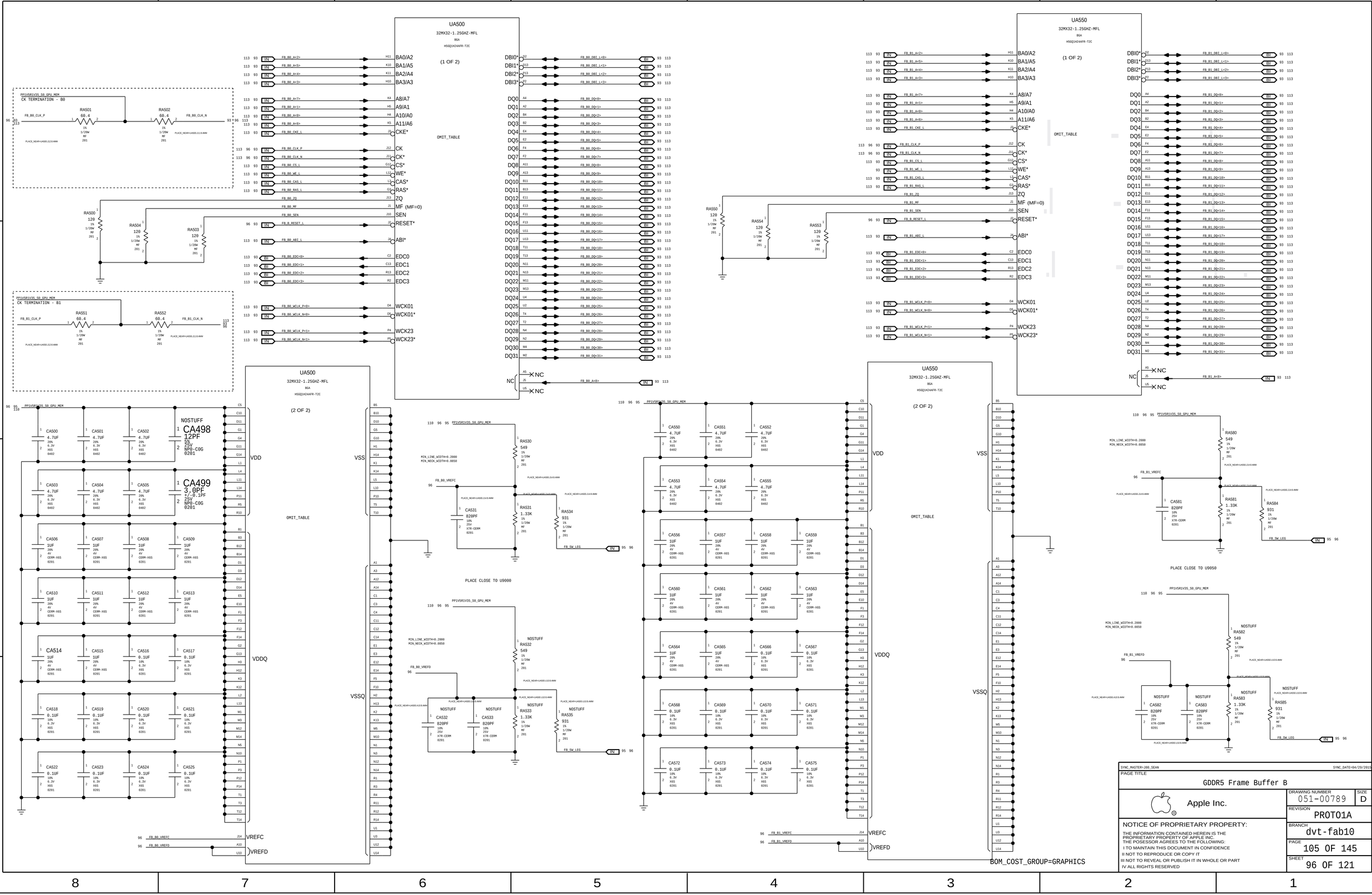
UA450
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(2 OF 2)
OMIT_TABLE

PLACE CLOSE TO U9000

PLACE CLOSE TO U9050

BOM_COST_GROUP=GRAPHICS

SYNC_MASTER=J80_SEAN	SYNC_DATE=04/29/2015
PAGE TITLE	GDDR5 Frame Buffer A
Apple Inc.	DRAWING NUMBER 051-00789 SIZE D
	REVISION PROTO1A
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	BRANCH dvt-fab10
	PAGE 104 OF 145
	SHEET 95 OF 121



SYNC_MASTER=J80_SEAN	SYNC_DATE=04/29/2015
PAGE TITLE	GDDR5 Frame Buffer B
Apple Inc.	DRAWING NUMBER 051-00789 · SIZE D
	REVISION PROTO1A
	BRANCH dvt-fab10
	PAGE 105 OF 145
	SHEET 96 OF 121

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S00174	2	MOSFET,CTRL+SYNC,25V,4.1/1.4MO,QFN32,6x6	QA640,QA650	CRITICAL	

GPU CORE SUPPLY

VOUT = 0.75-1.00V

64.2A MAX OUTPUT

F = 450 KHZ

TABLE 6. PRE-PWROK METAL VID CODES

SVC	SVD	OUTPUT VOLTAGE (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

ISL6277A datasheet (December 19,2012)

BOM_COST_GROUP=GRAPHICS

PAGE TITLE: GFX IMVP VCore Regulator [106]

Apple Inc.

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

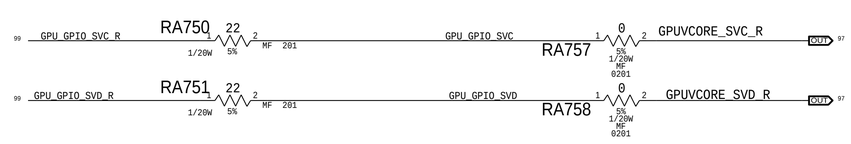
DRAWING NUMBER: 051-00789 | SIZE: D
REVISION: PROTO1A
BRANCH: dvt-fab10
PAGE: 106 OF 145
SHEET: 97 OF 121

former site of the SPEED MLPS STRAPS

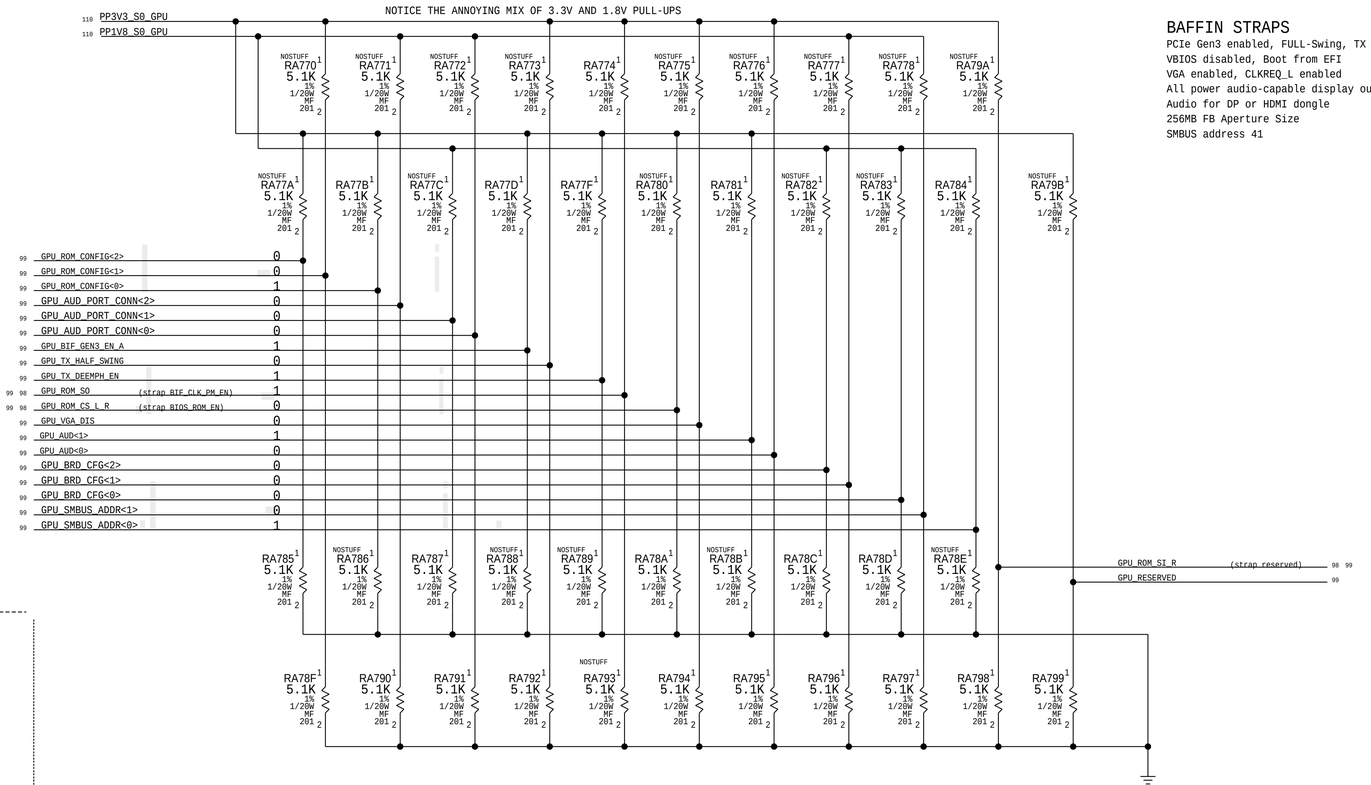
PCIe Gen3 enabled, Half-Swing, TX De-emp enabled
VBIOS disabled, Boot from EFI
VGA enabled
All power audio-capable display output
256MB FB Aperture Size

PS_0:	01001	82nF	8.45k	2k
PS_1:	10001	10nF	8.45k	2k
PS_2:	10000	10nF	NC	4.75k
PS_3:	00000	680nF	NC	4.75k

Former site of the GPU SVI2 VOLTAGE TRANSLATION SPEED ONLY



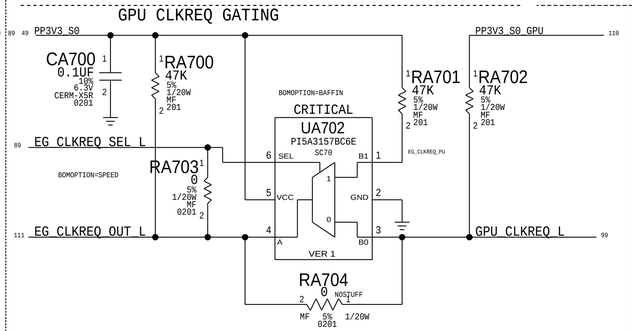
NOTICE THE ANNOYING MIX OF 3.3V AND 1.8V PULL-UPS



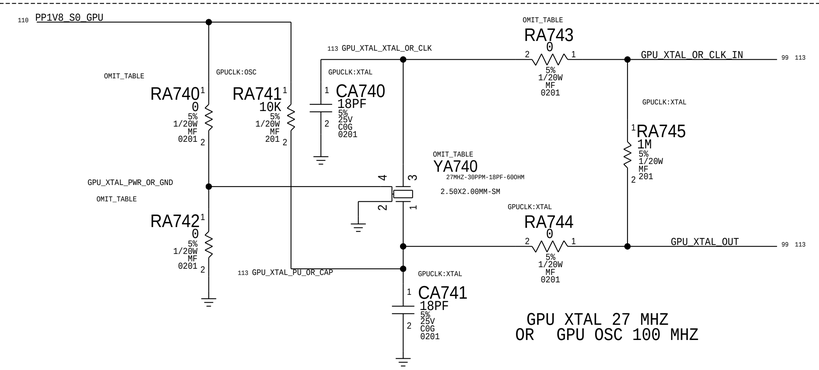
BAFFIN STRAPS

PCIe Gen3 enabled, FULL-Swing, TX De-emp enabled
VBIOS disabled, Boot from EFI
VGA enabled, CLKREQ_L enabled
All power audio-capable display output
Audio for DP or HDMI dongle
256MB FB Aperture Size
SMBUS address 41

GPU CLKREQ GATING

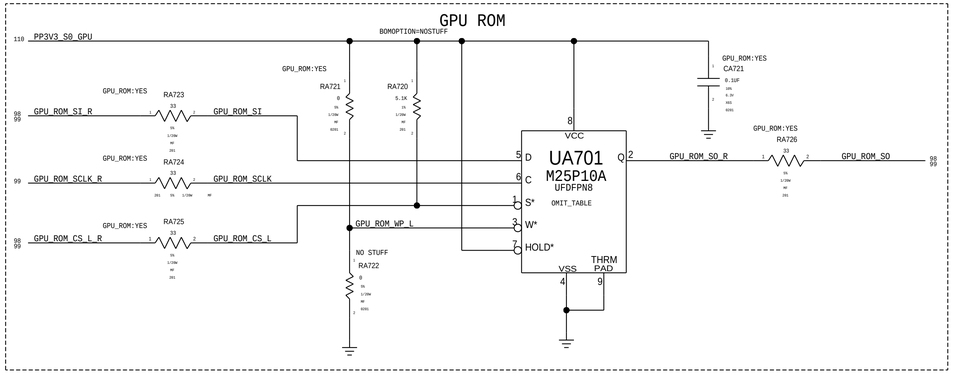


SEL = 0 : PCH CLKREQ CONNECTED TO GPU
SEL = 1 : PCH CLKREQ TIED TO PULLUP

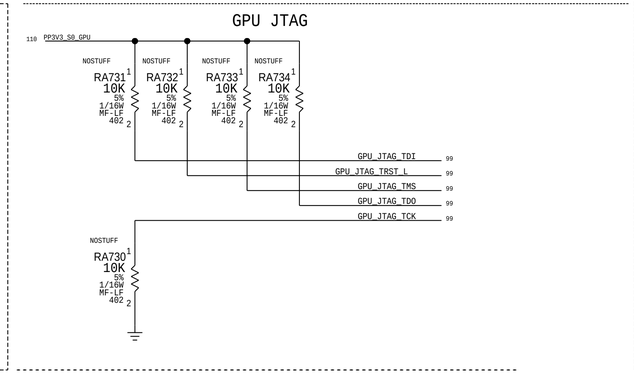


GPU XTAL 27 MHZ
OR GPU OSC 100 MHZ

GPU ROM



GPU JTAG



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
197S0499	1	XTAL,27.000MHZ,30PPM,12PF,2.5x2.0MM	YA740	CRITICAL	GPUCLK:XTAL
197S00056	1	OSC,MEMS,100MHZ,+/-20PPM,1.8V,2520	YA740	CRITICAL	GPUCLK:OSC
117S0201	1	RES,0 OHM,5%,0201	RA743	CRITICAL	GPUCLK:XTAL
117S0080	1	RES,33 OHM,5%,0201	RA743	CRITICAL	GPUCLK:OSC
155S0387	1	FERRITE BEAD, 4700HM,0.1A,1.5MOHM DCR,060	RA740	CRITICAL	GPUCLK:OSC
117S0201	1	RES,0 OHM,5%,0201	RA742	CRITICAL	GPUCLK:XTAL
132S0444	1	CAP,CER,X5R,0.1UF,10%,6.3V,0201	RA742	CRITICAL	GPUCLK:OSC

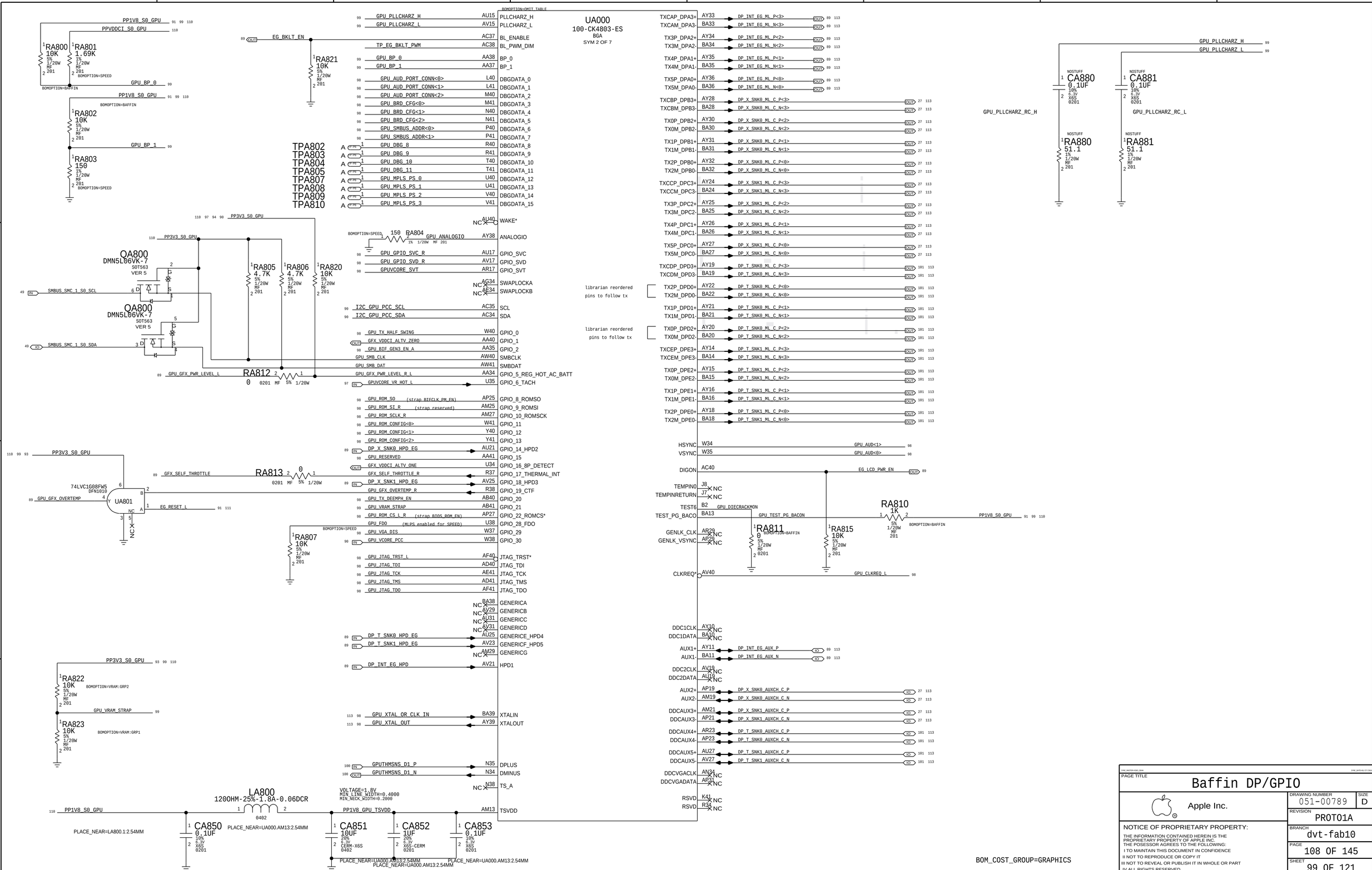
BOM_COST_GROUP=GRAPHICS

SYNC_MASTER=KIRAS_DEAN
SYNC_DATE=01/29/2015

PAGE TITLE
Baffin GPIOs,CLK & Straps

Apple Inc.

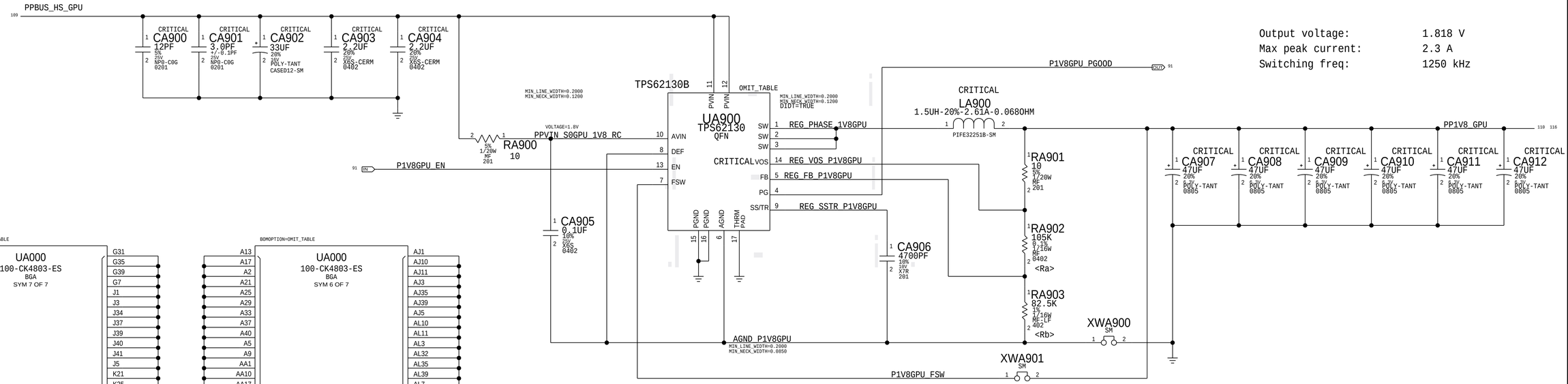
DRAWING NUMBER 051-00789
SIZE D
REVISION PROTO1A
BRANCH dvt-fab10
PAGE 107 OF 145
SHEET 98 OF 121



PAGE TITLE: Baffin DP/GPIO

Apple Inc.

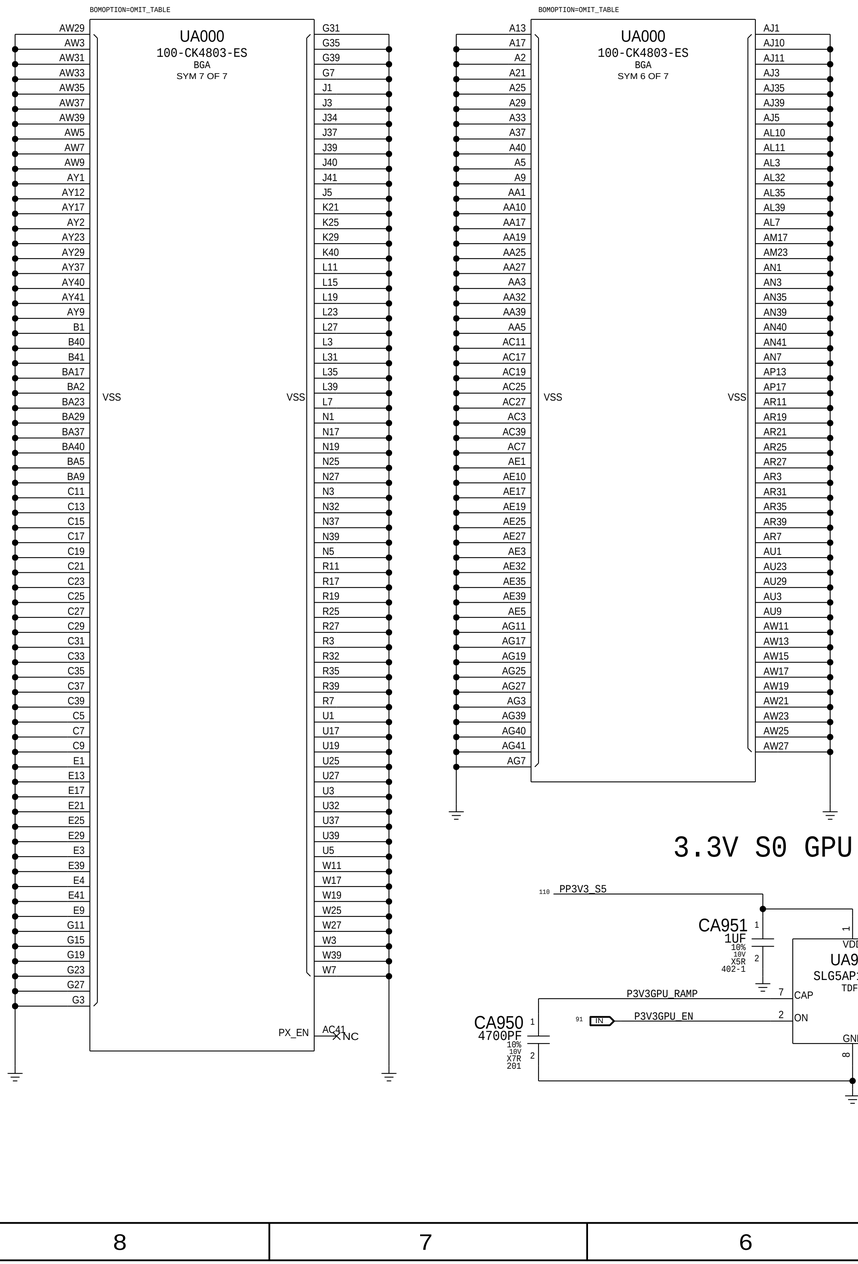
DRAWING NUMBER: 051-00789 | SIZE: D
REVISION: PROTO1A
BRANCH: dvt-fab10
PAGE: 108 OF 145
SHEET: 99 OF 121



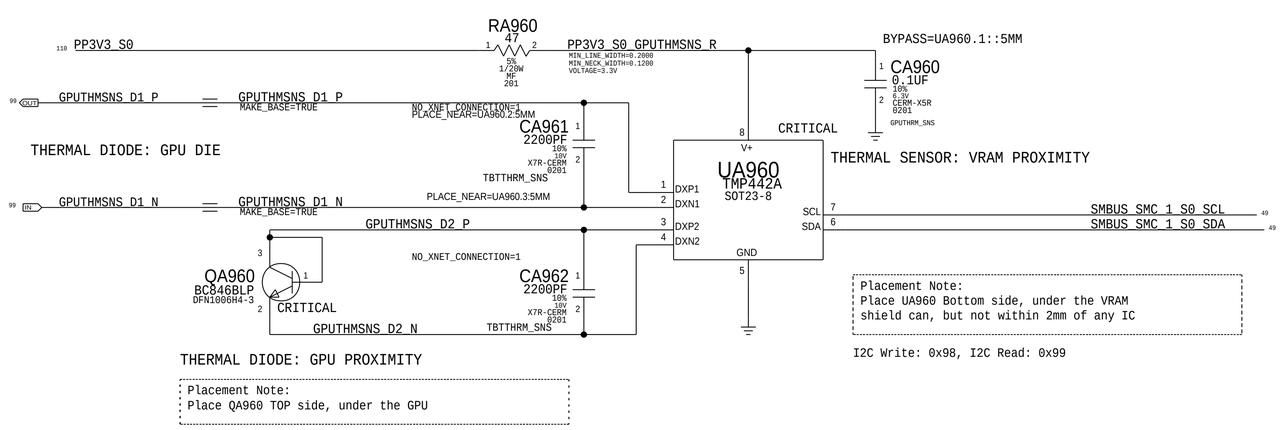
Output voltage: 1.818 V
Max peak current: 2.3 A
Switching freq: 1250 kHz

Vout = 0.8V * (Ra + Rb) / Rb

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00897	1	IC,TPS62130B-S,3A BUCK CNVTRT,QFN16,3X3M	UA900	CRITICAL	



GPU THERMAL

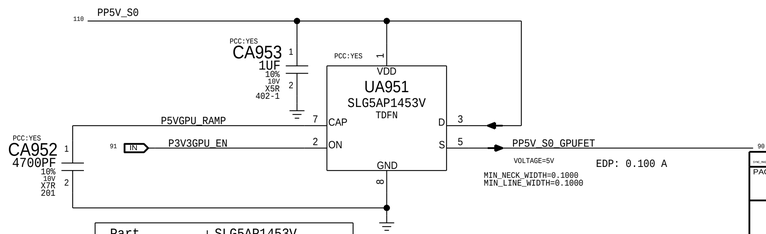


3.3V S0 GPU Switch

UA950

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 5.3A	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A Max

5V S0 GPU Switch



UA951

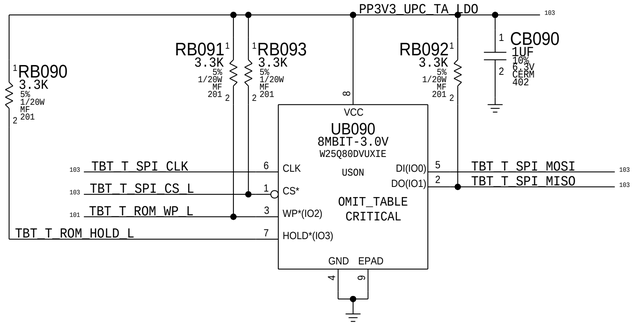
Part	SLG5AP1453V
Type	Load Switch
R(on) @ 5.3A	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A Max

BOM_COST_GROUP=GRAPHICS

PAGE TITLE: Baffin VSS & MISC

Apple Inc.

DRAWING NUMBER: 051-00789
SIZE: D
REVISION: PROTO1A
BRANCH: dvt-fab10
PAGE: 109 OF 145
SHEET: 100 OF 121



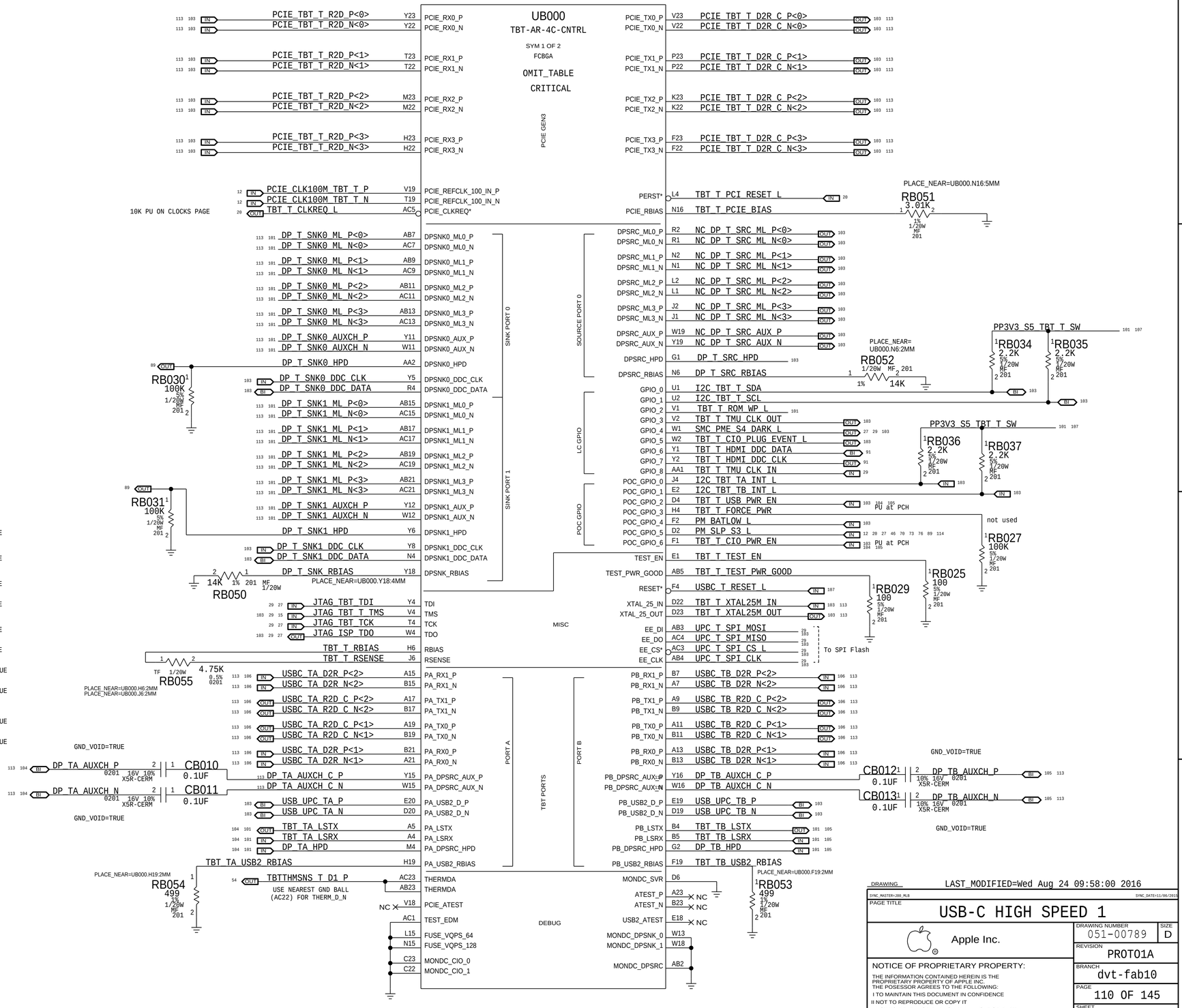
SNK0 AC Coupling

DP_T_SNK0_ML_C_P<0>	CB020	0.1UF	DP_T_SNK0_ML_P<0>	GND_VOID=TRUE	
DP_T_SNK0_ML_C_N<0>	CB021	0.1UF	DP_T_SNK0_ML_N<0>	GND_VOID=TRUE	
DP_T_SNK0_ML_C_P<1>	CB022	0.1UF	DP_T_SNK0_ML_P<1>	GND_VOID=TRUE	
DP_T_SNK0_ML_C_N<1>	CB023	0.1UF	DP_T_SNK0_ML_N<1>	GND_VOID=TRUE	
DP_T_SNK0_ML_C_P<2>	CB024	0.1UF	DP_T_SNK0_ML_P<2>	GND_VOID=TRUE	
DP_T_SNK0_ML_C_N<2>	CB025	0.1UF	DP_T_SNK0_ML_N<2>	GND_VOID=TRUE	
DP_T_SNK0_ML_C_P<3>	CB026	0.1UF	DP_T_SNK0_ML_P<3>	GND_VOID=TRUE	
DP_T_SNK0_ML_C_N<3>	CB027	0.1UF	DP_T_SNK0_ML_N<3>	GND_VOID=TRUE	
DP_T_SNK0_AUXCH_C_P	CB028	0.1UF	DP_T_SNK0_AUXCH_P	GND_VOID=TRUE	
DP_T_SNK0_AUXCH_C_N	CB029	0.1UF	DP_T_SNK0_AUXCH_N	GND_VOID=TRUE	

SNK1 AC Coupling

DP_T_SNK1_ML_C_P<0>	CB030	0.1UF	DP_T_SNK1_ML_P<0>	GND_VOID=TRUE	
DP_T_SNK1_ML_C_N<0>	CB031	0.1UF	DP_T_SNK1_ML_N<0>	GND_VOID=TRUE	
DP_T_SNK1_ML_C_P<1>	CB032	0.1UF	DP_T_SNK1_ML_P<1>	GND_VOID=TRUE	
DP_T_SNK1_ML_C_N<1>	CB033	0.1UF	DP_T_SNK1_ML_N<1>	GND_VOID=TRUE	
DP_T_SNK1_ML_C_P<2>	CB034	0.1UF	DP_T_SNK1_ML_P<2>	GND_VOID=TRUE	
DP_T_SNK1_ML_C_N<2>	CB035	0.1UF	DP_T_SNK1_ML_N<2>	GND_VOID=TRUE	
DP_T_SNK1_ML_C_P<3>	CB036	0.1UF	DP_T_SNK1_ML_P<3>	GND_VOID=TRUE	
DP_T_SNK1_ML_C_N<3>	CB037	0.1UF	DP_T_SNK1_ML_N<3>	GND_VOID=TRUE	
DP_T_SNK1_AUXCH_C_P	CB038	0.1UF	DP_T_SNK1_AUXCH_P	GND_VOID=TRUE	
DP_T_SNK1_AUXCH_C_N	CB039	0.1UF	DP_T_SNK1_AUXCH_N	GND_VOID=TRUE	

RB062	100K	DP_TA_HPD
RB072	100K	DP_TB_HPD
RB060	1M	TBT_TA_LSTX
RB061	1M	TBT_TA_LSRX
RB070	1M	TBT_TB_LSTX
RB071	1M	TBT_TB_LSRX



DRAWING LAST_MODIFIED=Wed Aug 24 09:58:00 2016

SYNC_MASTER=J89_MLB SYNC_DATE=11/06/2015

PAGE TITLE

USB-C HIGH SPEED 1

Apple Inc.

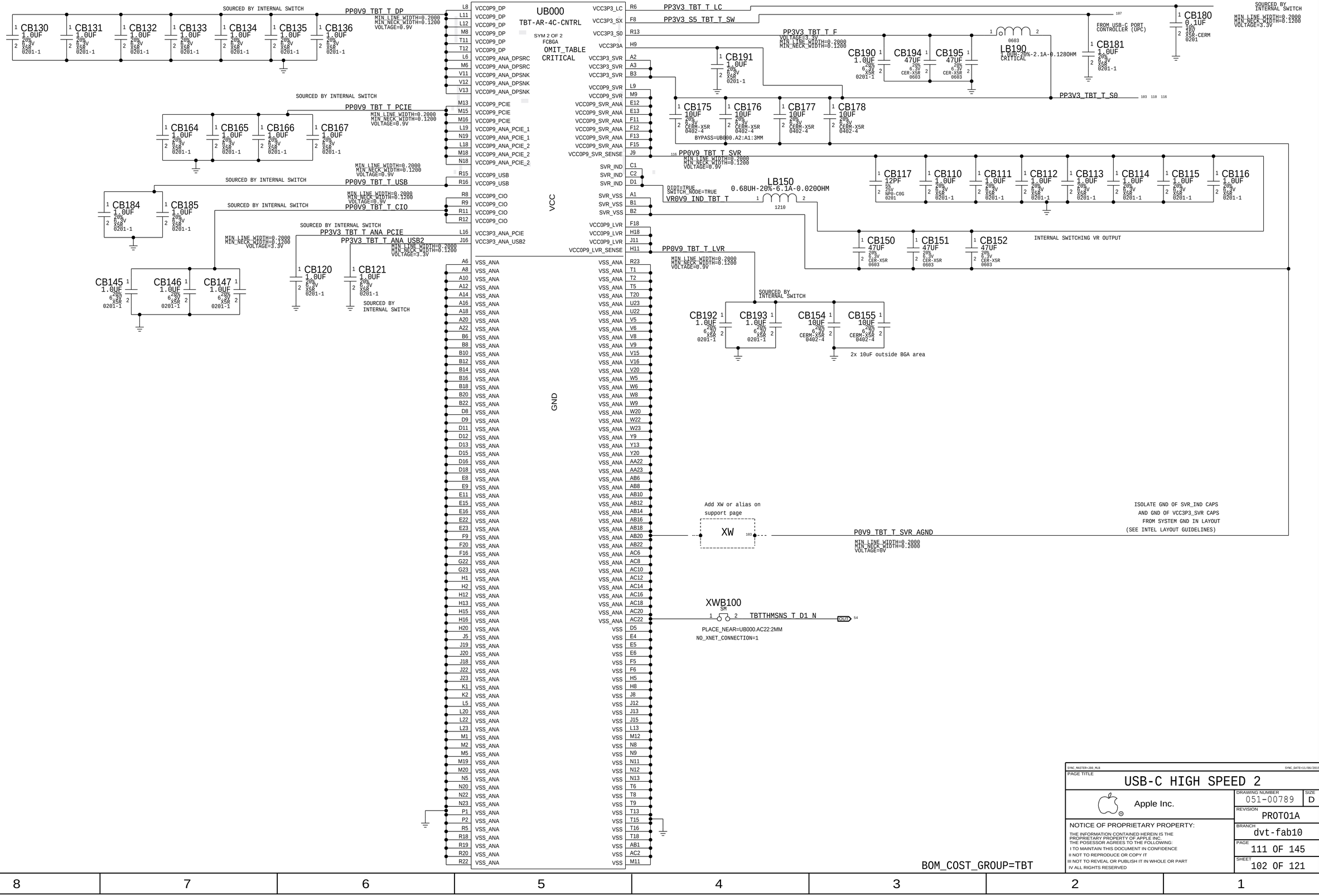
DRAWING NUMBER 051-00789 SIZE D

REVISION PROTO1A

BRANCH dvt-fab10

PAGE 110 OF 145

SHEET 101 OF 121



SYNC_MASTER=J80_MLB	SYNC_DATE=11/06/2015
PAGE TITLE	USB-C HIGH SPEED 2
Apple Inc.	DRAWING NUMBER 051-00789 · SIZE D
	REVISION PROTO1A
	BRANCH dvt-fab10
	PAGE 111 OF 145
	SHEET 102 OF 121

TMU CLKs

TBT_T_TMU_CLK_OUT → RB225 15 (MAKE_BASE=TRUE, 5% 1/20W MF 201, PLACE_NEAR=UB000.V2:5mm) → TBT_X_TMU_CLK_IN (MAKE_BASE=TRUE)

TBT_X_TMU_CLK_IN → RB226 100K (5% 1/20W MF 201)

DP SRC OPTIONS

IF DP SRC NOT USED

DP_T_SRC_HPD → RB240 1M (5% 1/20W MF 201)

NC_DP_T_SRC_ML_P<3..0>	NC_DP_T_SRC_ML_P<3..0> (MAKE_BASE=TRUE, NO_TEST=1)
NC_DP_T_SRC_ML_N<3..0>	NC_DP_T_SRC_ML_N<3..0> (MAKE_BASE=TRUE, NO_TEST=1)
NC_DP_T_SRC_AUX_P	NC_DP_T_SRC_AUX_P (MAKE_BASE=TRUE)
NC_DP_T_SRC_AUX_N	NC_DP_T_SRC_AUX_N (MAKE_BASE=TRUE)

FUSES FOR UPC

PP20V_USBC_TA_VBUS → FB200 (PLACE_NEAR=QB300:5MM, CRITICAL, 0603, 6AMP-32V-0.0095OHM) → PP20V_USBC_TA_VBUS_F

PP20V_USBC_TB_VBUS → FB201 (PLACE_NEAR=QB400:5MM, CRITICAL, 0603, 740S0135, 6AMP-32V-0.0095OHM) → PP20V_USBC_TB_VBUS_F

25MHz xtal

TBT_T_XTALIN25M_OUT → RB207 0 (5% 1/20W MF 201) → TBT_T_XTALIN25M_OUT_R

NOSTUFF RB206 1M (5% 1/20W MF 201) to/from Ridge

CRITICAL YB200 25MHZ-25PPM-20PF-50OHM 2.00X1.60-SM

CB202 20PF (5% 25V C0G 0201)

CB203 20PF (5% 25V C0G 0201)

TBT_T_XTALIN25M_OUT

AR/ACE SPI BUS SERIES R'S

ROM: TBT_T_SPI_CLK, TBT_T_SPI_CS_L, TBT_T_SPI_MOSI, TBT_T_SPI_MISO

RB290 100 (5% 1/20W MF 201) TBT_T_SPI_CLK_DBG

RB280 15	UPC_TA_SPI_CLK	Ace
RB281 15	UPC_TA_SPI_CS_L	Ace
RB282 15	UPC_TA_SPI_MOSI	Ace
RB283 15	UPC_TA_SPI_MISO	Ace
RB284 15	UPC_T_SPI_CLK	AR
RB285 15	UPC_T_SPI_CS_L	AR
RB286 15	UPC_T_SPI_MOSI	AR
RB287 15	UPC_T_SPI_MISO	AR

(5% 1/20W MF 201)

TP UPC TA SWD DATA / CLK, TP UPC TB SWD DATA / CLK

TP UPC TA SWD DATA → TPB201 (TP-P5)

TP UPC TA SWD CLK → TPB202 (TP-P5)

TP UPC TB SWD DATA → TPB203 (TP-P5)

TP UPC TB SWD CLK → TPB204 (TP-P5)

ACE Debug Support

OMIT RB289 NOSTUFF 402: TP_UPC_TA_DBG_UART_TX → TP_UPC_TA_DBG_UART_RX

OMIT RB288 NOSTUFF 402: TP_UPC_TB_DBG_UART_TX → TP_UPC_TB_DBG_UART_RX

USBC 5V EN PD

UPC_T_5V_EN → RB232 100K (5% 1/20W MF 201)

ACE A/B RPD STRAPPING

USBC_TA_CC1	USBC_TA_CC1 (MAKE_BASE=TRUE)
USBC_TB_CC1	USBC_TB_CC1 (MAKE_BASE=TRUE)
USBC_TA_CC2	USBC_TA_CC2 (MAKE_BASE=TRUE)
USBC_TB_CC2	USBC_TB_CC2 (MAKE_BASE=TRUE)

Ridge PDs

DP_T_SNK0_DDC_CLK	RB267 100K	DP_T_SNK0_DDC_CLK (MAKE_BASE=TRUE)
DP_T_SNK0_DDC_DATA	RB268 100K	DP_T_SNK0_DDC_DATA (MAKE_BASE=TRUE)
DP_T_SNK1_DDC_CLK	RB269 100K	DP_T_SNK1_DDC_CLK (MAKE_BASE=TRUE)
DP_T_SNK1_DDC_DATA	RB270 100K	DP_T_SNK1_DDC_DATA (MAKE_BASE=TRUE)

(5% 1/20W MF 201)

ACE PDs

UPC_TA_DBG3	RB260 100K
UPC_TA_DBG4	RB261 100K
UPC_TB_DBG3	RB262 100K
UPC_TB_DBG4	RB263 100K
UPC_TA_DBG1	RB264 100K
UPC_TA_DBG2	RB265 100K
UPC_TA_HPD_RX	RB233 100K
UPC_TB_HPD_RX	RB234 100K

(5% 1/20W MF 201)

ACE FET DCIN Bypass Caps

PPDCIN_G3H → CB211 0.1UF, CB212 0.1UF, CB213 0.1UF, CB214 0.1UF (10% 35V CER-X5R 0201)

RIDGE 0.9V SVR XW

XWB200 SM: P0V9_TBT_T_SVR_AGND → NO_XNET_CONNECTION=1

I2C SERIES R'S

SMBUS_SMC_4_G3H_SDA → RB241 33 (PLACE_NEAR=U5000:5mm) → I2C_UPC_T_SDA2

SMBUS_SMC_4_G3H_SCL → RB242 33 (PLACE_NEAR=U5000:5mm) → I2C_UPC_T_SCL2

(5% 1/20W MF 201)

ACE DEBUG CONN

Place on bottom

USBC_DBG JB200 505070-1220 M-ST-SM

I2C_TBT_TB_INT_L	I2C_TBT_TA_INT_L
I2C_UPC_T_SCL2	I2C_TBT_T_SDA
I2C_UPC_T_SDA2	I2C_TBT_T_SCL
SMC_USBC_INT_L	TBT_T_CIO_PWR_EN
TBT_T_SPI_CLK_DBG	TBT_T_USB_PWR_EN
UPC_TA_UART_TX	UPC_TA_UART_RX

TBT to ACE

TBT (Alpine Ridge U2800, MASTER) ↔ Pri ACE (U3100, Write: 0x70 Read: 0x71)

I2C_TBT_T_SCL	I2C_TBT_T_SCL
I2C_TBT_T_SDA	I2C_TBT_T_SDA
I2C_TBT_TA_INT_L	I2C_TBT_TA_INT_L
I2C_TBT_TB_INT_L	

Sec ACE (U3200, Write: 0x7E Read: 0x7F)

I2C_TBT_T_SCL	I2C_TBT_T_SCL
I2C_TBT_T_SDA	I2C_TBT_T_SDA
I2C_TBT_TB_INT_L	I2C_TBT_TB_INT_L

Ridge PCIE Caps

R2D

PCIE_TBT_T_R2D_C_P<0>	CB240 0.22UF → PCIE_TBT_T_R2D_P<0>
PCIE_TBT_T_R2D_C_N<0>	CB241 0.22UF → PCIE_TBT_T_R2D_N<0>
PCIE_TBT_T_R2D_C_P<1>	CB242 0.22UF → PCIE_TBT_T_R2D_P<1>
PCIE_TBT_T_R2D_C_N<1>	CB243 0.22UF → PCIE_TBT_T_R2D_N<1>
PCIE_TBT_T_R2D_C_P<2>	CB244 0.22UF → PCIE_TBT_T_R2D_P<2>
PCIE_TBT_T_R2D_C_N<2>	CB245 0.22UF → PCIE_TBT_T_R2D_N<2>
PCIE_TBT_T_R2D_C_P<3>	CB246 0.22UF → PCIE_TBT_T_R2D_P<3>
PCIE_TBT_T_R2D_C_N<3>	CB247 0.22UF → PCIE_TBT_T_R2D_N<3>

(GND_VOID=TRUE, 0201 X5R 6.3V 20%)

D2R

PCIE_TBT_T_D2R_C_P<0>	CB250 0.22UF → PCIE_TBT_T_D2R_P<0>
PCIE_TBT_T_D2R_C_N<0>	CB251 0.22UF → PCIE_TBT_T_D2R_N<0>
PCIE_TBT_T_D2R_C_P<1>	CB252 0.22UF → PCIE_TBT_T_D2R_P<1>
PCIE_TBT_T_D2R_C_N<1>	CB253 0.22UF → PCIE_TBT_T_D2R_N<1>
PCIE_TBT_T_D2R_C_P<2>	CB254 0.22UF → PCIE_TBT_T_D2R_P<2>
PCIE_TBT_T_D2R_C_N<2>	CB255 0.22UF → PCIE_TBT_T_D2R_N<2>
PCIE_TBT_T_D2R_C_P<3>	CB256 0.22UF → PCIE_TBT_T_D2R_P<3>
PCIE_TBT_T_D2R_C_N<3>	CB257 0.22UF → PCIE_TBT_T_D2R_N<3>

(GND_VOID=TRUE, 0201 X5R 6.3V 20%)

USB_UPC_TB_P / TB_N / TA_P / TA_N

RB250 0	USB_UPC_TB_P	NOSTUFF
RB251 0	USB_UPC_TB_N	NOSTUFF
RB354 0	USB_UPC_TA_P	NOSTUFF
RB255 0	USB_UPC_TA_N	NOSTUFF

(5% 1/20W MF 0201)

POWER ALIASES

PP3V3_UPC_TA_LDO	PP3V3_UPC_TA_LDO (MAKE_BASE=TRUE)
PP20V_USBC_TA_VBUS	PP20V_USBC_TA_VBUS (MAKE_BASE=TRUE)
PP20V_USBC_TB_VBUS	PP20V_USBC_TB_VBUS (MAKE_BASE=TRUE)
PP3V3_UPC_TB_LDO	PP3V3_UPC_TB_LDO (MAKE_BASE=TRUE)
PP5V_S4_T_USBC	PP5V_S4_T_USBC (MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=5V)
PP3V3_TBT_T_S0	PP3V3_TBT_T_S0 (MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=3.3V)

NO TEST

NC_UPC_TB_I2C_ADDR

GND ALIASES

GND → GND (MAKE_BASE=TRUE) → BOM_COST_GROUP=TBT

SIGNAL ALIASES

USB2_UPC_TB_P	USB_UPC_PCH_TB_P
USB2_UPC_TB_N	USB_UPC_PCH_TB_N
USB2_UPC_TA_P	USB_UPC_PCH_TA_P
USB2_UPC_TA_N	USB_UPC_PCH_TA_N
TBT_T_CIO_PWR_EN	TBT_T_CIO_PWR_EN
TBT_T_USB_PWR_EN	TBT_T_USB_PWR_EN
PM_BATLOW_L	PM_BATLOW_L
SMC_PME_S4_DARK_L	SMC_PME_S4_DARK_L
UPC_T_5V_EN	UPC_T_5V_EN
JTAG_ISP_TDO	JTAG_ISP_TDO
SMC_USBC_INT_L	SMC_USBC_INT_L
SMC_USBC_INT_L	
SSD_DEBUG_I2C_CLK_CONN	SSD_DEBUG_I2C_CLK_CONN
SSD_DEBUG_I2C_DAT_CONN	SSD_DEBUG_I2C_DAT_CONN
TBT_T_CIO_PLUG_EVENT_L	TBT_T_CIO_PLUG_EVENT_L
UPC_TA_FAULT_L	XDP_PCH_OBSDATA_C2 (RB258 0)
UPC_TB_FAULT_L	XDP_PCH_OBSDATA_C3 (RB259 0)
JTAG_TBT_T_TMS	JTAG_TBT_T_TMS
PP3V3_S4	PP3V3_S4
PP3V3_S4	
TP_USBC_TB_RESET_L	TP_USBC_TB_RESET_L
TBT_POC_RESET	TBT_POC_RESET

(MAKE_BASE=TRUE)

PRIMARY ACE USB-C PORT CONTROLLER (UPC)

QB300
FDPC4044
PWR-CLIP-33
FUSE
Add on support page
PP20V_USBC_TA_VBUS_F
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=20V
NC
PP20V_USBC_TA_VBUS
CB301
1UF
10%
35V
X5R
0402
UPC_TA_GATE1
TP_QB300_DRAIN
UPC_TA_GATE2
PPDCIN_G3H
MAX 100uF TOTAL ON RAIL
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V
PP3V3_UPC_TA_LDO
P3V3_TBT_T_SX_EN_R
VOUT_3V3 FOR RIDGE, OR FLOAT IF UNUSED
PP1V8_UPC_TA_LDOA
PP1V8_UPC_TA_LDOD
PP1V1_UPC_TA_LDO_BMC
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.1V
PP3V3_UPC_TA_LDO
PP3V3_G3H
GND
PP5V_S4_T_USBC
CAP FOR PP_5V0 ON VR PAGE
CB300
10UF
20%
6.3V
CERM-X5R
0402-1
CB305
1.0UF
20%
6.3V
X5R
0201-1
CB308
10UF
20%
6.3V
CERM-X5R
0402-1
CB304
2.2UF
20%
4V
X5R-CERM
0201
CB306
0.47UF
10%
6.3V
CERM-X5R
0201
PULL R3109 AND R3108 UP TO ACEs LDOs FOR 1ST RIDGE'S ACES
PULL R3109 AND R3108 DOWN TO GND FOR 2ND RIDGE'S ACES
GND
RB309
1M
5% 1/20W MF 201
I2C_UPC_TA_DBG_CTL_SCL
RB308
1M
5% 1/20W MF 201
I2C_UPC_TA_DBG_CTL_SDA
TESTPOINTS MUST BE PRESENT FOR GPIO0, GPIO1 (EVEN IN PRODUCTION)
USE GPIO2 FOR USB-C ANALOG AUDIO SUPPORT ON DESIGNS WITHOUT AN AUDIO JACK CONNECTOR
USE GPIO3 FOR POWER_GATE_EN ON BANSURI DESIGNS
TBT_POC_RESET
USBC_T_RESET_L_R
TP_UPC_TA_DBG_UART_TX
TP_UPC_TA_DBG_UART_RX
TBT_T_CIO_PWR_EN
TBT_T_USB_PWR_EN
DP_TA_HPD
UPC_TA_HPD_RX
UPC_T_5V_EN
SMC_PME_S4_DARK_L
UPC_TA_FAULT_L
GND
PRIMARY ONLY
PRIMARY ONLY
UB300
CD3215A
BGA
CRITICAL
OMIT_TABLE
MRESET
RESET*
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
BUSPOWERZ
I2C_ADDR
R_OSC
DEBUG_CTL1
DEBUG_CTL2
I2C_SDA1
I2C_SCL1
I2C_IRQ1*
I2C_SDA2
I2C_SCL2
I2C_IRQ2*
SPI_CLK
SPI_MOSI
SPI_MISO
SPI_SSZ
SWD_DATA
SWD_CLK
UART_RX
UART_TX
LSX_R2P
LSX_P2R
USB_RP_P
USB_RP_N
AUX_P
AUX_N
DEBUG1
DEBUG2
DEBUG3
DEBUG4
PP_5V0
PP_HV
PP_CABLE
VBUS
VIN_3V3
VDDIO
LDO_3V3
VOUT_3V3
LDO_1V8A
LDO_1V8D
LDO_BMC
HV FET/SENSE
DIGITAL CORE I/O AND CONTROL
TYPE-C
PORT MUX
SS
SENSEP
SENSEN
HV_GATE1
HV_GATE2
UPC_TA_SS
CB309
0.47UF
10%
6.3V
CERM-X5R
0201
C_CC1
C_CC2
RPD_G1
RPD_G2
C_USB_TP
C_USB_TN
C_USB_BP
C_USB_BN
C_SBU1
C_SBU2
NC
USBC_TA_CC1
USBC_TA_CC2
USBC_TA_CC1
USBC_TA_CC2
USBC_TA_USB_TOP_P
USBC_TA_USB_TOP_N
USBC_TA_USB_BOT_P
USBC_TA_USB_BOT_N
USBC_TA_SBU1
USBC_TA_SBU2
GROUND
NC or GND to dissipate heat
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
CB314
220PF
10%
16V
CER-X7R
0201
CB313
220PF
10%
16V
CER-X7R
0201
GND I2C ADDR PRIMARY ONLY
RB302
0
5%
1/20W
MF
201
CRITICAL
RB303
15K
0.1%
1/20W
TF-LF
0201
NEED 0.1%
UPC_TA_I2C_ADDR
UPC_TA_R_OSC
I2C_UPC_TA_DBG_CTL_SCL
I2C_UPC_TA_DBG_CTL_SDA
I2C_TBT_T_SDA
I2C_TBT_T_SCL
I2C_TBT_TA_INT_L
I2C_UPC_T_SDA2
I2C_UPC_T_SCL2
SMC_USBC_INT_L
TO SMC
RB305
1M
5% 1/20W MF 201
UPC_TA_UART_RX
REAR PORT: CONNECT UPC SPI TO ROM
FRONT PORT: GROUND UPC SPI
UPC_TA_SPI_CLK
UPC_TA_SPI_MOSI
UPC_TA_SPI_MISO
UPC_TA_SPI_CS_L
TP_UPC_TA_SWD_DATA
TP_UPC_TA_SWD_CLK
UPC_TA_UART_RX
UPC_TA_UART_TX
TBT_TA_LSTX
TBT_TA_LSRX
LB300
90-OHM-0.1A
EXCX4CE
USB2_UPC_TA_P
USB2_UPC_TA_N
PLACE_NEAR=UB300.L5:5mm
PLACE_NEAR=UB300.K5:5mm
USB_UPC_TA_F_P
USB_UPC_TA_F_N
DP_TA_AUXCH_P
DP_TA_AUXCH_N
PP3V3_S4
PU to PP3V3_S4 if convenient for layout, Otherwise PU to PP3V3_UPC_XA_LDO
NO_XNET_CONNECTION=1
RB310
100K
5%
1/20W
MF
201
RB311
100K
5%
1/20W
MF
201
NO_XNET_CONNECTION=1
UPC_TA_DBG1
UPC_TA_DBG2
UPC_TA_DBG3
UPC_TA_DBG4
GND
GND
PIN D6 IS UNDOCUMENTED RESET
CAN GROUND PIN D6 IN PRODUCTION
BOM_COST_GROUP=USB-C

PAGE TITLE

USB-C PORT CONTROLLER A

Apple Inc.

DRAWING NUMBER: 051-00789 | SIZE: D

REVISION: PROTO1A

BRANCH: dvt-fab10

PAGE: 113 OF 145

SHEET: 104 OF 121

SECONDARY ACE USB-C PORT CONTROLLER (UPC)

QB400
FDPC4044
PWR-CLIP-33
FUSE
Add on support page
PP20V_USBC_TB_VBUS_F
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=20V
PP20V_USBC_TB_VBUS
PPDCIN_G3H
MAX 100uF TOTAL ON RAIL
UPC_TB_GATE1
TP_QB400_DRAIN
UPC_TB_GATE2
CB401
1UF
PP3V3_UPC_TB_LDO
PP3V3_G3H
GND
PP5V_S4_T_USBC
CAP FOR PP_5V0 ON VR PAGE
P3V3_TBT_T_SX_EN_R
VOUT_3V3 FOR RIDGE, OR FLOAT IF UNUSED
PP1V8_UPC_TB_LDOA
PP1V8_UPC_TB_LDOD
PP1V1_UPC_TB_LDO_BMC
CB400
10UF
CB405
1.0UF
CB408
10UF
CB404
2.2UF
CB406
0.47UF
UB400
CD3215A
BGA
CRITICAL
OMIT_TABLE
TBT_POC_RESET
TP_USBC_TB_RESET_L
TESTPOINTS MUST BE PRESENT FOR GPIO0, GPIO1 (EVEN IN PRODUCTION)
TP_UPC_TB_DBG_UART_TX
TP_UPC_TB_DBG_UART_RX
TBT_T_CIO_PWR_EN
TBT_T_USB_PWR_EN
DP_TB_HPD
UPC_TB_HPD_RX
UPC_T_5V_EN
SMC_PME_S4_DARK_L
UPC_TB_FAULT_L
PULL R3209 AND R3208 UP TO ACEs LDOs FOR 1ST RIDGE'S ACES
PULL R3209 AND R3208 DOWN TO GND FOR 2ND RIDGE'S ACES
RB409
1M
I2C_UPC_TB_DBG_CTL_SCL
RB408
1M
I2C_UPC_TB_DBG_CTL_SDA
NC_UPC_TB_I2C_ADDR
UPC_TB_R_OSC
CRITICAL
RB403
15K
NEED 0.1%
I2C_TBT_T_SDA
I2C_TBT_T_SCL
I2C_TBT_TB_INT_L
RB405
1M
UPC_TA_UART_TX
I2C_UPC_T_SDA2
I2C_UPC_T_SCL2
SMC_USBC_INT_L
TO SMC
REAR PORT: CONNECT UPC SPI TO ROM
FRONT PORT: GROUND UPC SPI
TP_UPC_TB_SWD_DATA
TP_UPC_TB_SWD_CLK
UPC_TA_UART_RX
TBT_TB_LSTX
TBT_TB_LSRX
LB400
90-OHM-0.1A
USB2_UPC_TB_P
USB2_UPC_TB_N
PLACE_NEAR=UB400.L5:5mm
PLACE_NEAR=UB400.K5:5mm
USB_UPC_TB_F_P
USB_UPC_TB_F_N
DP_TB_AUXCH_P
DP_TB_AUXCH_N
PP3V3_S4
PU to PP3V3_S4 if convenient for layout, Otherwise PU to PP3V3_UPC_XA_LDO
RB410
100K
NO_XNET_CONNECTION=1
RB411
100K
SSD_DEBUG_I2C_CLK_CONN
SSD_DEBUG_I2C_DAT_CONN
UPC_TB_DBG3
UPC_TB_DBG4
UPC_TB_SS
CB409
0.47UF
USBC_TB_CC1
USBC_TB_CC2
CB414
220PF
CB413
220PF
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
UPC_TB_USB_TOP_P
UPC_TB_USB_TOP_N
UPC_TB_USB_BOT_P
UPC_TB_USB_BOT_N
USBC_TB_SBU1
USBC_TB_SBU2
GROUND
NC or GND to dissipate heat
HV FET/SENSE
DIGITAL CORE I/O AND CONTROL
TYPE-C
PORT MUX
PIN D6 IS UNDOCUMENTED RESET
CAN GROUND PIN D6 IN PRODUCTION

BOM_COST_GROUP=USB-C

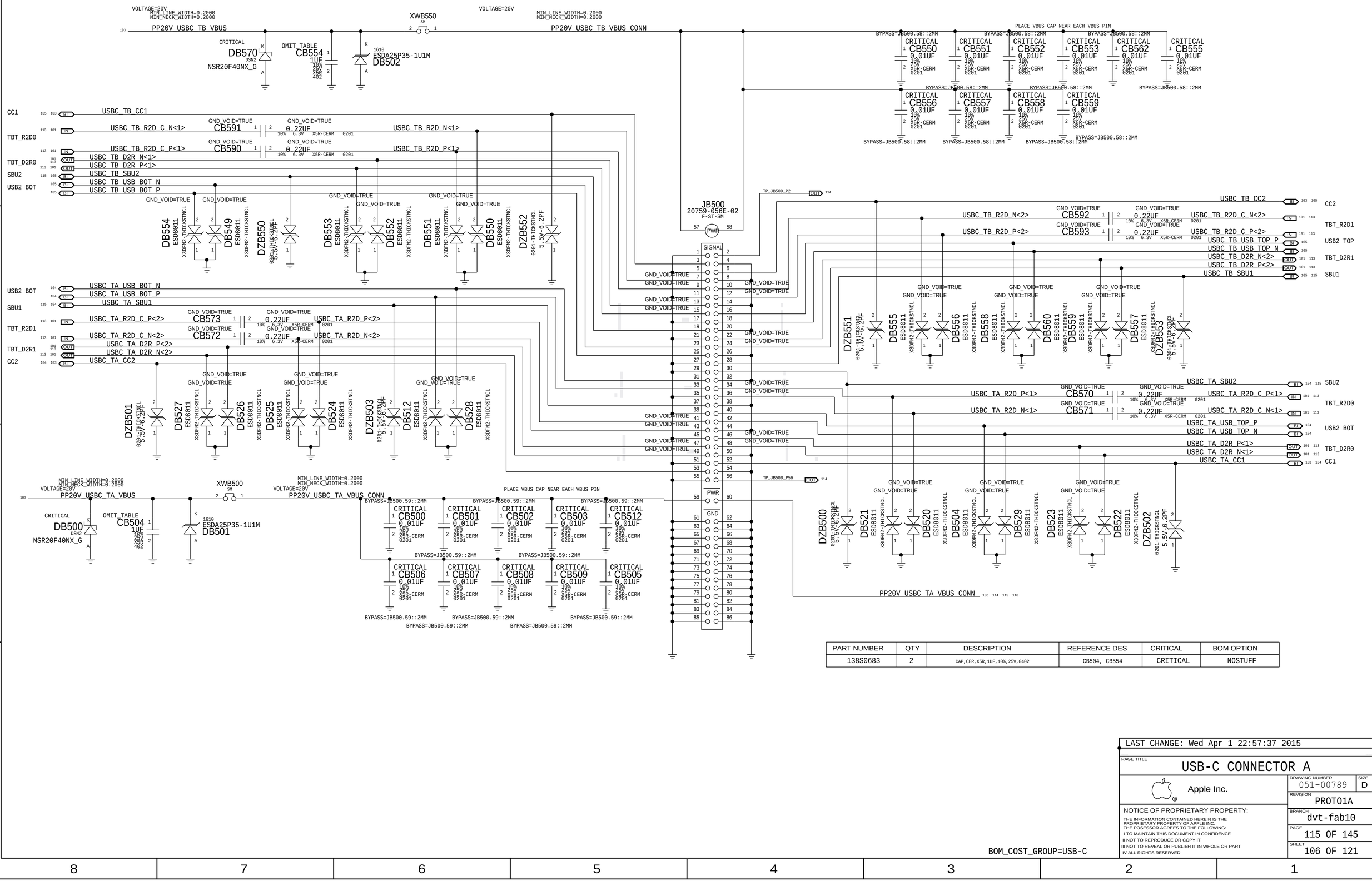
PAGE TITLE
USB-C PORT CONTROLLER B

Apple Inc.

DRAWING NUMBER 051-00789 SIZE D

REVISION PROTO1A

BRANCH dvt-fab10



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0683	2	CAP,CER,X5R,1UF,10%,25V,0402	CB504, CB554	CRITICAL	NOSTUFF

BOM_COST_GROUP=USB-C

LAST CHANGE: Wed Apr 1 22:57:37 2015

PAGE TITLE

USB-C CONNECTOR A

Apple Inc.

DRAWING NUMBER 051-00789 SIZE D

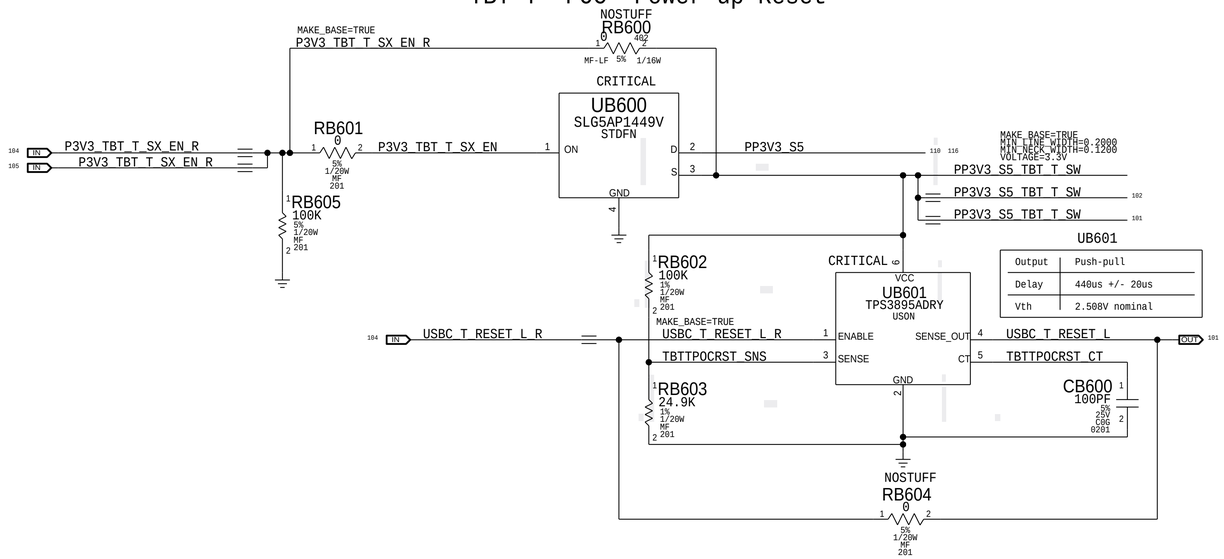
REVISION PROTO1A

BRANCH dvt-fab10

PAGE 115 OF 145

SHEET 106 OF 121

TBT T "POC" Power-up Reset



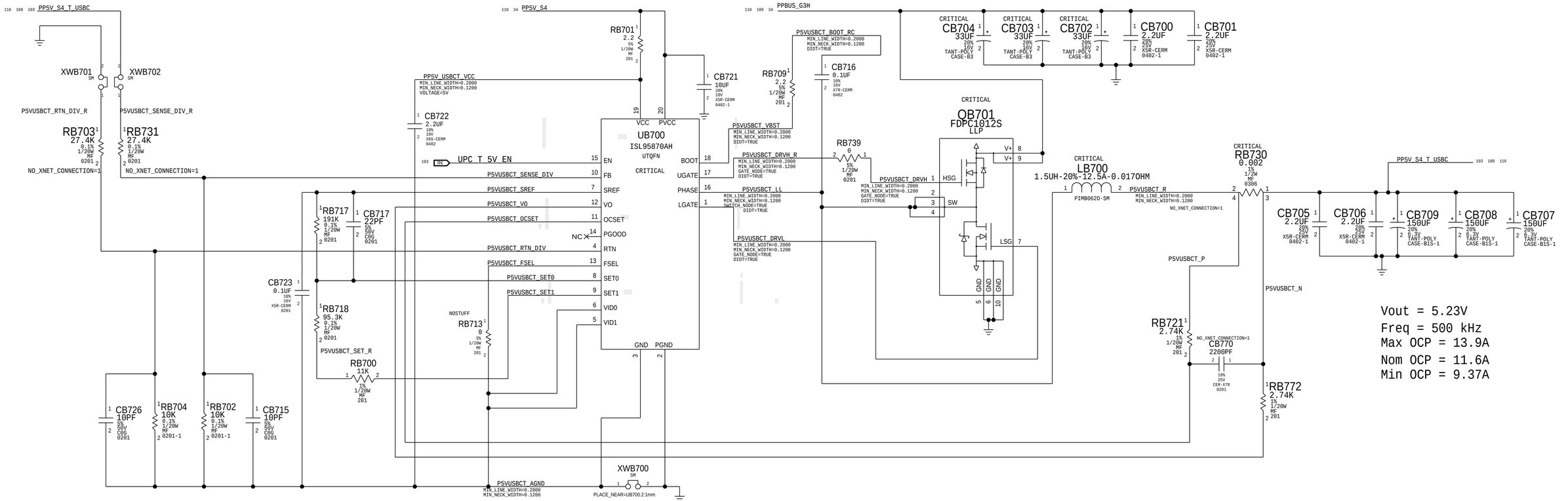
BOM_COST_GROUP=USB-C

DESIGN: j130/dev_mlb_u
LAST CHANGE: Wed Apr 1 22:57:37 2015

PAGE TITLE
USB-C CONNECTOR B

Apple Inc.

DRAWING NUMBER 051-00789
SIZE D
REVISION PROTO1A
BRANCH dvt-fab10
PAGE 116 OF 145
SHEET 107 OF 121



PAGE TITLE

TBT 5V REGULATOR

Apple Inc.

DRAWING NUMBER 051-00789 | SIZE D

REVISION PROTO1A

BRANCH dvt-fab10

PAGE 117 OF 145

SHEET 108 OF 121

PBUS Rails

116 64 PPBUS_G3H
- PPBUS_G3H — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=13.1V, MAKE_BASE=TRUE — 114
- PPBUS_G3H — 50
- PPBUS_G3H — 50
- PPBUS_G3H — 50
- PPBUS_G3H — 75
- PPBUS_G3H — 50
- PPBUS_G3H — 50
- PPBUS_G3H — 70
- PPBUS_G3H — 63
- PPBUS_G3H — 72
- PPBUS_G3H — 34 108 116
- PPBUS_G3H — 55
- PPBUS_G3H — 60 61
- PPBUS_G3H — 72

50 PPBUS_HS_CPU
- PPBUS_HS_CPU — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.2000, VOLTAGE=13.1V, MAKE_BASE=TRUE — 117
- PPBUS_HS_CPU — 66
- PPBUS_HS_CPU — 67
- PPBUS_HS_CPU — 68
- PPBUS_HS_CPU — 71
- PPBUS_HS_CPU — 71
- PPBUS_HS_CPU — 65

55 PPBUS_HS_GPU
- PPBUS_HS_GPU — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=13.1V, MAKE_BASE=TRUE — 97
- PPBUS_HS_GPU — 94
- PPBUS_HS_GPU — 97
- PPBUS_HS_GPU — 94
- PPBUS_HS_GPU — 100

50 PPBUS_HS_OTH5V
- PPBUS_HS_OTH5V — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=13.1V, MAKE_BASE=TRUE
- PPBUS_HS_OTH5V — 69 117

117 50 PPBUS_HS_OTH3V3
- PPBUS_HS_OTH3V3 — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=13.1V, MAKE_BASE=TRUE
- PPBUS_HS_OTH3V3 — 69 117

50 PPBUS_S4_HS_TPAD
- PPBUS_S4_HS_TPAD — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=13.1V, MAKE_BASE=TRUE
- PPBUS_S4_HS_TPAD — 43

3V3 G3H Rails

63 PP3V3_G3H
- PP3V3_G3H — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=3.3V, MAKE_BASE=TRUE — 114
- PP3V3_G3H — 57
- PP3V3_G3H — 46 47 76
- PP3V3_G3H — 48
- PP3V3_G3H — 64
- PP3V3_G3H — 43 48
- PP3V3_G3H — 49
- PP3V3_G3H — 48
- PP3V3_G3H — 47
- PP3V3_G3H — 20
- PP3V3_G3H — 49
- PP3V3_G3H — 30
- PP3V3_G3H — 31
- PP3V3_G3H — 29
- PP3V3_G3H — 104
- PP3V3_G3H — 105

RTC Rails

70 PP3V0_G3H
- PP3V0_G3H — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=3.0V, MAKE_BASE=TRUE
- PP3V0_G3H — 12 16 17
- PP3V0_G3H — 70

IMVP Rails

66 PPVCC_S0_CPU
- PPVCC_S0_CPU — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.8V, MAKE_BASE=TRUE — 114
- PPVCC_S0_CPU — 6 8 55
- PPVCC_S0_CPU — 10

67 PPVCCSA_S0_CPU
- PPVCCSA_S0_CPU — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.15V, MAKE_BASE=TRUE
- PPVCCSA_S0_CPU — 8 53
- PPVCCSA_S0_CPU — 11

68 PPVCCGT_S0_CPU
- PPVCCGT_S0_CPU — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.8V, MAKE_BASE=TRUE
- PPVCCGT_S0_CPU — 8 55
- PPVCCGT_S0_CPU — 11 116

CPU VCCIO Rails

117 71 PPVCCIO_S0_CPU
- PPVCCIO_S0_CPU — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=0.95V, MAKE_BASE=TRUE
- PPVCCIO_S0_CPU — 10
- PPVCCIO_S0_CPU — 5 8

1V2 Rails

117 74 71 PP1V2_S3
- PP1V2_S3 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.2V, MAKE_BASE=TRUE
- PP1V2_S3 — 22 23 24 25 116
- PP1V2_S3 — 71 117
- PP1V2_S3 — 21
- PP1V2_S3 — 22 23 24 25
- PP1V2_S3 — 22 23 24 25 116
- PP1V2_S3 — 51
- PP1V2_S3 — 74

51 PP1V2_S3_CPUDDR
- PP1V2_S3_CPUDDR — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.2V, MAKE_BASE=TRUE
- PP1V2_S3_CPUDDR — 8
- PP1V2_S3_CPUDDR — 10 116

74 PP1V2_S0SW
- PP1V2_S0SW — MIN_LINE_WIDTH=0.5000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.2V, MAKE_BASE=TRUE
- PP1V2_S0SW — 8

0V6 Rails

117 71 PP0V6_S0_DDRVTT
- PP0V6_S0_DDRVTT — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=0.6V, MAKE_BASE=TRUE
- PP0V6_S0_DDRVTT — 26 116
- PP0V6_S0_DDRVTT — 26 116

21 PP0V6_S3_MEM_VREFDQ_A
- PP0V6_S3_MEM_VREFDQ_A — MAKE_BASE=TRUE, VOLTAGE=0.6V — 22 23

109 21 PP0V6_S3_MEM_VREFCA_A
- PP0V6_S3_MEM_VREFCA_A — MAKE_BASE=TRUE, VOLTAGE=0.6V — 22 23

21 PP0V6_S3_MEM_VREFDQ_B
- PP0V6_S3_MEM_VREFDQ_B — MAKE_BASE=TRUE, VOLTAGE=0.6V — 24 25

109 21 PP0V6_S3_MEM_VREFCA_A
- PP0V6_S3_MEM_VREFCA_A — MAKE_BASE=TRUE, VOLTAGE=0.6V — 24 25

1V8 Rails

117 72 PP1V8_SUS
- PP1V8_SUS — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.8V, MAKE_BASE=TRUE
- PP1V8_SUS — 74
- PP1V8_SUS — 74
- PP1V8_SUS — 15 16 17

74 PP1V8_S4
- PP1V8_S4 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.8V, MAKE_BASE=TRUE
- PP1V8_S4 — 38 42
- PP1V8_S4 — 20

74 PP1V8_S3
- PP1V8_S3 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.8V, MAKE_BASE=TRUE
- PP1V8_S3 — 53
- PP1V8_S3 — 70

53 PP1V8_S3_MEM
- PP1V8_S3_MEM — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.8V, MAKE_BASE=TRUE
- PP1V8_S3_MEM — 22 23 24 25 116

74 PP1V8_S0
- PP1V8_S0 — MIN_LINE_WIDTH=0.5000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.8V, MAKE_BASE=TRUE — 61 114
- PP1V8_S0 — 16 17
- PP1V8_S0 — 58 60 61
- PP1V8_S0 — 37 38 42
- PP1V8_S0 — 73
- PP1V8_S0 — 19
- PP1V8_S0 — 37 42
- PP1V8_S0 — 37

SYNC_MASTER=J08_MLB SYNC_DATE=08/16/2016

PAGE TITLE

Power Aliases - 1

Apple Inc.

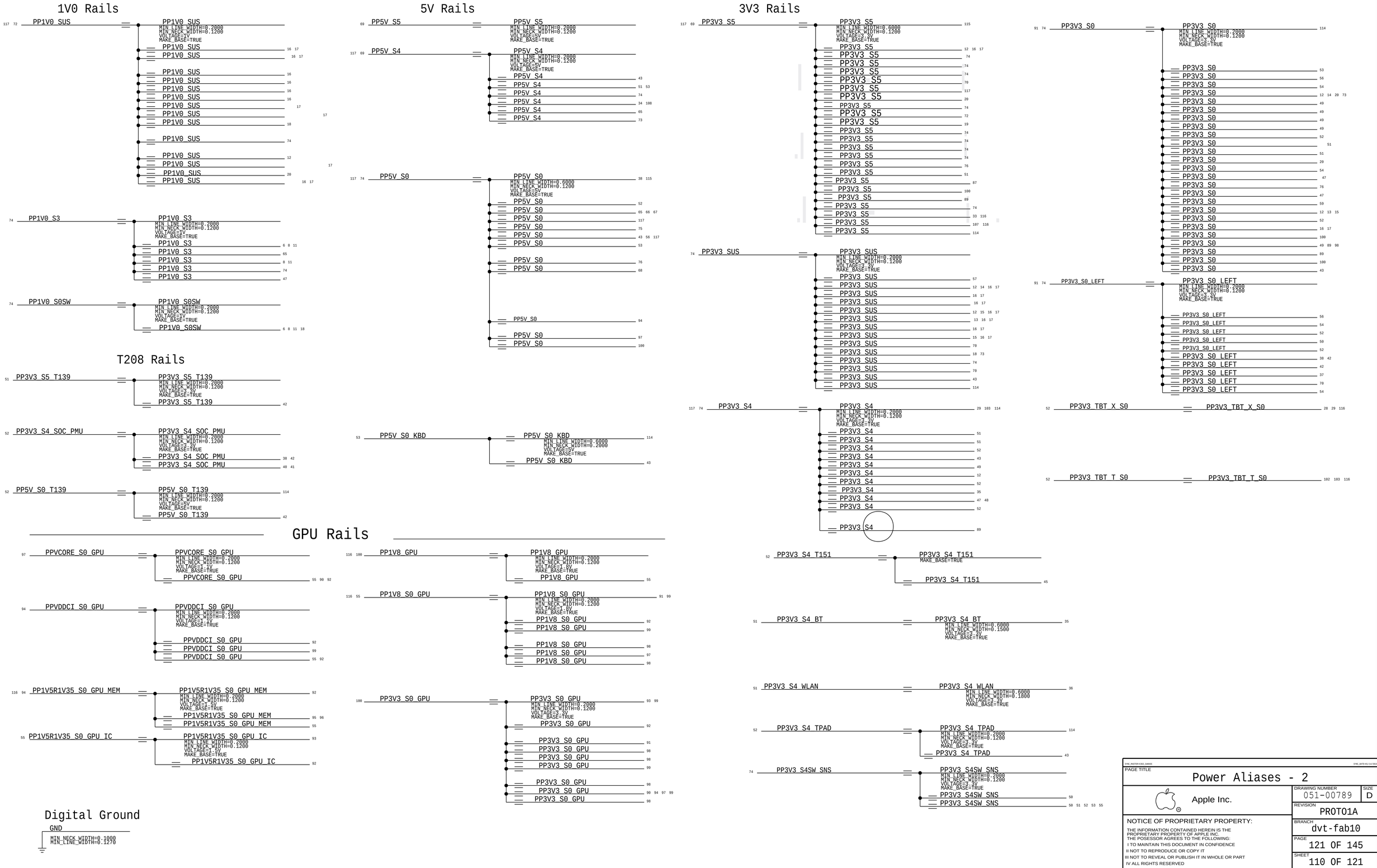
DRAWING NUMBER 051-00789 | SIZE D

REVISION PROTO1A

BRANCH dvt-fab10

PAGE 120 OF 145

SHEET 109 OF 121



PAGE TITLE	Power Aliases - 2
	Apple Inc.
DRAWING NUMBER	051-00789
SIZE	D
REVISION	PROTO1A
BRANCH	dvt-fab10
PAGE	121 OF 145
SHEET	110 OF 121

SIGNAL ALIAS

NC ALIASES 2

111	12	NC_CLKOUT_PCIE_1_N	NC_CLKOUT_PCIE_1_N	12	111
111	12	NC_CLKOUT_PCIE_1_P	NC_CLKOUT_PCIE_1_P	12	111
111	12	NC_CLKOUT_PCIE_2_N	NC_CLKOUT_PCIE_2_N	12	111
111	12	NC_CLKOUT_PCIE_2_P	NC_CLKOUT_PCIE_2_P	12	111
111	12	NC_CLKOUT_PCIE_6_N	NC_CLKOUT_PCIE_6_N	12	111
111	12	NC_CLKOUT_PCIE_6_P	NC_CLKOUT_PCIE_6_P	12	111
111	12	NC_CLKOUT_PCIE_8_N	NC_CLKOUT_PCIE_8_N	12	111
111	12	NC_CLKOUT_PCIE_8_P	NC_CLKOUT_PCIE_8_P	12	111
111	12	NC_CLKOUT_PCIE_9_N	NC_CLKOUT_PCIE_9_N	12	111
111	12	NC_CLKOUT_PCIE_9_P	NC_CLKOUT_PCIE_9_P	12	111
111	12	NC_CLKOUT_PCIE_10_N	NC_CLKOUT_PCIE_10_N	12	111
111	12	NC_CLKOUT_PCIE_10_P	NC_CLKOUT_PCIE_10_P	12	111
111	12	NC_CLKOUT_PCIE_11_N	NC_CLKOUT_PCIE_11_N	12	111
111	12	NC_CLKOUT_PCIE_11_P	NC_CLKOUT_PCIE_11_P	12	111
111	12	NC_CLKOUT_PCIE_12_N	NC_CLKOUT_PCIE_12_N	12	111
111	12	NC_CLKOUT_PCIE_12_P	NC_CLKOUT_PCIE_12_P	12	111
111	12	NC_CLKOUT_PCIE_14_N	NC_CLKOUT_PCIE_14_N	12	111
111	12	NC_CLKOUT_PCIE_14_P	NC_CLKOUT_PCIE_14_P	12	111
111	12	NC_CLKOUT_PCIE_15_N	NC_CLKOUT_PCIE_15_N	12	111
111	12	NC_CLKOUT_PCIE_15_P	NC_CLKOUT_PCIE_15_P	12	111

15	NC_TP_PCH_GPP_G1	NC_TP_PCH_GPP_G1	15
15	NC_TP_PCH_GPP_G2	NC_TP_PCH_GPP_G2	15
15	NC_TP_PCH_GPP_G3	NC_TP_PCH_GPP_G3	15
15	NC_TP_PCH_GPP_G4	NC_TP_PCH_GPP_G4	15
15	NC_TP_PCH_GPP_G5	NC_TP_PCH_GPP_G5	15
15	NC_TP_PCH_GPP_G6	NC_TP_PCH_GPP_G6	15
15	NC_TP_PCH_GPP_G7	NC_TP_PCH_GPP_G7	15
15	NC_TP_PCH_GPP_G8	NC_TP_PCH_GPP_G8	15

14	NC_PCH_GPP_F15	NC_PCH_GPP_F15	14
14	NC_PCH_GPP_F16	NC_PCH_GPP_F16	14
14	NC_PCH_GPP_F17	NC_PCH_GPP_F17	14
14	NC_PCH_GPP_F18	NC_PCH_GPP_F18	14

GPU PEG Lanes

113	91	PEG_GPU_D2R_P<7..0>	=PEG_D2R_P<7..0>	5	113
113	91	PEG_GPU_D2R_N<7..0>	=PEG_D2R_N<7..0>	5	113
113	91	PEG_GPU_R2D_C_P<7..0>	=PEG_R2D_C_P<7..0>	5	113
113	91	PEG_GPU_R2D_C_N<7..0>	=PEG_R2D_C_N<7..0>	5	113

Thunderbolt Signals Through PEG

113	29	PCIE_TBT_X_D2R_P<3..0>	=PEG_D2R_P<11..8>	5	113
113	29	PCIE_TBT_X_D2R_N<3..0>	=PEG_D2R_N<11..8>	5	113
113	29	PCIE_TBT_X_R2D_C_P<3..0>	=PEG_R2D_C_P<11..8>	5	113
113	29	PCIE_TBT_X_R2D_C_N<3..0>	=PEG_R2D_C_N<11..8>	5	113
113	103	PCIE_TBT_T_D2R_P<3..0>	=PEG_D2R_P<15..12>	5	113
113	103	PCIE_TBT_T_D2R_N<3..0>	=PEG_D2R_N<15..12>	5	113
113	103	PCIE_TBT_T_R2D_C_P<3..0>	=PEG_R2D_C_P<15..12>	5	113
113	103	PCIE_TBT_T_R2D_C_N<3..0>	=PEG_R2D_C_N<15..12>	5	113

GPU ALIAS

12	EG_CLKREQ_OUT_L	EG_CLKREQ_OUT_L	98		
12	EG_PEG_CLK100M_N	EG_PEG_CLK100M_N	91		
12	EG_PEG_CLK100M_P	EG_PEG_CLK100M_P	91		
89	EG_RESET_L	EG_RESET_L	91	99	

CPU Display Aliases

		eDP conn	DPMUX		
114	76	EDP_INT_ML_P<3..0>	EDP_INT_ML_P<3..0>	89	
114	76	EDP_INT_ML_N<3..0>	EDP_INT_ML_N<3..0>	89	
113	76	EDP_AUXCH_C_P	EDP_AUXCH_C_P	89	
113	76	EDP_AUXCH_C_N	EDP_AUXCH_C_N	89	

NC_DDI1_ML_C_P<3..0>	NO_TEST=1	NC_DDI1_ML_C_P<3..0>		5
NC_DDI1_ML_C_N<3..0>	NO_TEST=1	NC_DDI1_ML_C_N<3..0>		5
NC_DDI1_AUXCH_C_P		NC_DDI1_AUXCH_C_P		5
NC_DDI1_AUXCH_C_N		NC_DDI1_AUXCH_C_N		5
NC_DDI2_ML_C_P<3..0>	NO_TEST=1	NC_DDI2_ML_C_P<3..0>		5
NC_DDI2_ML_C_N<3..0>	NO_TEST=1	NC_DDI2_ML_C_N<3..0>		5
NC_DDI2_AUXCH_C_P		NC_DDI2_AUXCH_C_P		5
NC_DDI2_AUXCH_C_N		NC_DDI2_AUXCH_C_N		5
NC_DDI3_ML_P<3..0>	NO_TEST=1	NC_DDI3_ML_P<3..0>		5
NC_DDI3_ML_N<3..0>	NO_TEST=1	NC_DDI3_ML_N<3..0>		5
NC_DDI3_AUXCH_P		NC_DDI3_AUXCH_P		5
NC_DDI3_AUXCH_N		NC_DDI3_AUXCH_N		5

89	DPMUX_UC_RX		DPMUX_UC_RX	89
89	DPMUX_UC_TX		DPMUX_UC_TX	89
15	NC_EDP_IG_BKLT_PWM		NC_EDP_IG_BKLT_PWM	

EPD PANEL

75	I2C_BKLT_SCL	TRUE	I2C_BKLT_SCL	76	114
75	I2C_BKLT_SDA	TRUE	I2C_BKLT_SDA	76	114

UNUSED SIGNALS

12	NC_PCH_SLP_WLAN_L		NC_PCH_SLP_WLAN_L
13	NC_SPI_CS1_L		NC_SPI_CS1_L
13	NC_SPI_CS2_L		NC_SPI_CS2_L

SYNC_MASTER=X363_SAMXOC SYNC_DATE=01/13/2016

PAGE TITLE

Signal Aliases

Apple Inc.

DRAWING NUMBER 051-00789 SIZE D

REVISION PROTO1A

BRANCH dvt-fab10

PAGE 122 OF 145

SHEET 111 OF 121

LPDDR3 COMMAND/ADDRESS

Memory Bit/Byte Swizzle

BDW-H LPDDR3 NET	BIT SWIZZLE
MAKE_BASE=TRUE	
MEM_A_DQ<0>	MEM_A_DQ<0>
MEM_A_DQ<1>	MEM_A_DQ<1>
MEM_A_DQ<2>	MEM_A_DQ<2>
MEM_A_DQ<3>	MEM_A_DQ<3>
MEM_A_DQ<4>	MEM_A_DQ<4>
MEM_A_DQ<5>	MEM_A_DQ<5>
MEM_A_DQ<6>	MEM_A_DQ<6>
MEM_A_DQ<7>	MEM_A_DQ<7>
MEM_A_DQ<8>	MEM_A_DQ<8>
MEM_A_DQ<9>	MEM_A_DQ<9>
MEM_A_DQ<10>	MEM_A_DQ<10>
MEM_A_DQ<11>	MEM_A_DQ<11>
MEM_A_DQ<12>	MEM_A_DQ<12>
MEM_A_DQ<13>	MEM_A_DQ<13>
MEM_A_DQ<14>	MEM_A_DQ<14>
MEM_A_DQ<15>	MEM_A_DQ<15>
MEM_A_DQ<16>	MEM_A_DQ<16>
MEM_A_DQ<17>	MEM_A_DQ<17>
MEM_A_DQ<18>	MEM_A_DQ<18>
MEM_A_DQ<19>	MEM_A_DQ<19>
MEM_A_DQ<20>	MEM_A_DQ<20>
MEM_A_DQ<21>	MEM_A_DQ<21>
MEM_A_DQ<22>	MEM_A_DQ<22>
MEM_A_DQ<23>	MEM_A_DQ<23>
MEM_A_DQ<24>	MEM_A_DQ<24>
MEM_A_DQ<25>	MEM_A_DQ<25>
MEM_A_DQ<26>	MEM_A_DQ<26>
MEM_A_DQ<27>	MEM_A_DQ<27>
MEM_A_DQ<28>	MEM_A_DQ<28>
MEM_A_DQ<29>	MEM_A_DQ<29>
MEM_A_DQ<30>	MEM_A_DQ<30>
MEM_A_DQ<31>	MEM_A_DQ<31>
MEM_A_DQ<32>	MEM_A_DQ<32>
MEM_A_DQ<33>	MEM_A_DQ<33>
MEM_A_DQ<34>	MEM_A_DQ<34>
MEM_A_DQ<35>	MEM_A_DQ<35>
MEM_A_DQ<36>	MEM_A_DQ<36>
MEM_A_DQ<37>	MEM_A_DQ<37>
MEM_A_DQ<38>	MEM_A_DQ<38>
MEM_A_DQ<39>	MEM_A_DQ<39>
MEM_A_DQ<40>	MEM_A_DQ<40>
MEM_A_DQ<41>	MEM_A_DQ<41>
MEM_A_DQ<42>	MEM_A_DQ<42>
MEM_A_DQ<43>	MEM_A_DQ<43>
MEM_A_DQ<44>	MEM_A_DQ<44>
MEM_A_DQ<45>	MEM_A_DQ<45>
MEM_A_DQ<46>	MEM_A_DQ<46>
MEM_A_DQ<47>	MEM_A_DQ<47>
MEM_A_DQ<48>	MEM_A_DQ<48>
MEM_A_DQ<49>	MEM_A_DQ<49>
MEM_A_DQ<50>	MEM_A_DQ<50>
MEM_A_DQ<51>	MEM_A_DQ<51>
MEM_A_DQ<52>	MEM_A_DQ<52>
MEM_A_DQ<53>	MEM_A_DQ<53>
MEM_A_DQ<54>	MEM_A_DQ<54>
MEM_A_DQ<55>	MEM_A_DQ<55>
MEM_A_DQ<56>	MEM_A_DQ<56>
MEM_A_DQ<57>	MEM_A_DQ<57>
MEM_A_DQ<58>	MEM_A_DQ<58>
MEM_A_DQ<59>	MEM_A_DQ<59>
MEM_A_DQ<60>	MEM_A_DQ<60>
MEM_A_DQ<61>	MEM_A_DQ<61>
MEM_A_DQ<62>	MEM_A_DQ<62>
MEM_A_DQ<63>	MEM_A_DQ<63>

BDW-H LPDDR3 NET	BIT SWIZZLE
MAKE_BASE=TRUE	
MEM_B_DQ<0>	MEM_B_DQ<0>
MEM_B_DQ<1>	MEM_B_DQ<1>
MEM_B_DQ<2>	MEM_B_DQ<2>
MEM_B_DQ<3>	MEM_B_DQ<3>
MEM_B_DQ<4>	MEM_B_DQ<4>
MEM_B_DQ<5>	MEM_B_DQ<5>
MEM_B_DQ<6>	MEM_B_DQ<6>
MEM_B_DQ<7>	MEM_B_DQ<7>
MEM_B_DQ<8>	MEM_B_DQ<8>
MEM_B_DQ<9>	MEM_B_DQ<9>
MEM_B_DQ<10>	MEM_B_DQ<10>
MEM_B_DQ<11>	MEM_B_DQ<11>
MEM_B_DQ<12>	MEM_B_DQ<12>
MEM_B_DQ<13>	MEM_B_DQ<13>
MEM_B_DQ<14>	MEM_B_DQ<14>
MEM_B_DQ<15>	MEM_B_DQ<15>
MEM_B_DQ<16>	MEM_B_DQ<16>
MEM_B_DQ<17>	MEM_B_DQ<17>
MEM_B_DQ<18>	MEM_B_DQ<18>
MEM_B_DQ<19>	MEM_B_DQ<19>
MEM_B_DQ<20>	MEM_B_DQ<20>
MEM_B_DQ<21>	MEM_B_DQ<21>
MEM_B_DQ<22>	MEM_B_DQ<22>
MEM_B_DQ<23>	MEM_B_DQ<23>
MEM_B_DQ<24>	MEM_B_DQ<24>
MEM_B_DQ<25>	MEM_B_DQ<25>
MEM_B_DQ<26>	MEM_B_DQ<26>
MEM_B_DQ<27>	MEM_B_DQ<27>
MEM_B_DQ<28>	MEM_B_DQ<28>
MEM_B_DQ<29>	MEM_B_DQ<29>
MEM_B_DQ<30>	MEM_B_DQ<30>
MEM_B_DQ<31>	MEM_B_DQ<31>
MEM_B_DQ<32>	MEM_B_DQ<32>
MEM_B_DQ<33>	MEM_B_DQ<33>
MEM_B_DQ<34>	MEM_B_DQ<34>
MEM_B_DQ<35>	MEM_B_DQ<35>
MEM_B_DQ<36>	MEM_B_DQ<36>
MEM_B_DQ<37>	MEM_B_DQ<37>
MEM_B_DQ<38>	MEM_B_DQ<38>
MEM_B_DQ<39>	MEM_B_DQ<39>
MEM_B_DQ<40>	MEM_B_DQ<40>
MEM_B_DQ<41>	MEM_B_DQ<41>
MEM_B_DQ<42>	MEM_B_DQ<42>
MEM_B_DQ<43>	MEM_B_DQ<43>
MEM_B_DQ<44>	MEM_B_DQ<44>
MEM_B_DQ<45>	MEM_B_DQ<45>
MEM_B_DQ<46>	MEM_B_DQ<46>
MEM_B_DQ<47>	MEM_B_DQ<47>
MEM_B_DQ<48>	MEM_B_DQ<48>
MEM_B_DQ<49>	MEM_B_DQ<49>
MEM_B_DQ<50>	MEM_B_DQ<50>
MEM_B_DQ<51>	MEM_B_DQ<51>
MEM_B_DQ<52>	MEM_B_DQ<52>
MEM_B_DQ<53>	MEM_B_DQ<53>
MEM_B_DQ<54>	MEM_B_DQ<54>
MEM_B_DQ<55>	MEM_B_DQ<55>
MEM_B_DQ<56>	MEM_B_DQ<56>
MEM_B_DQ<57>	MEM_B_DQ<57>
MEM_B_DQ<58>	MEM_B_DQ<58>
MEM_B_DQ<59>	MEM_B_DQ<59>
MEM_B_DQ<60>	MEM_B_DQ<60>
MEM_B_DQ<61>	MEM_B_DQ<61>
MEM_B_DQ<62>	MEM_B_DQ<62>
MEM_B_DQ<63>	MEM_B_DQ<63>

MAKE_BASE		
TRUE	MEM_A_DQS_P<0>	MEM_A_DQS_P<0>
TRUE	MEM_A_DQS_N<0>	MEM_A_DQS_N<0>
TRUE	MEM_A_DQS_P<1>	MEM_A_DQS_P<1>
TRUE	MEM_A_DQS_N<1>	MEM_A_DQS_N<1>
TRUE	MEM_A_DQS_P<2>	MEM_A_DQS_P<2>
TRUE	MEM_A_DQS_N<2>	MEM_A_DQS_N<2>
TRUE	MEM_A_DQS_P<3>	MEM_A_DQS_P<3>
TRUE	MEM_A_DQS_N<3>	MEM_A_DQS_N<3>
TRUE	MEM_A_DQS_P<4>	MEM_A_DQS_P<4>
TRUE	MEM_A_DQS_N<4>	MEM_A_DQS_N<4>
TRUE	MEM_A_DQS_P<5>	MEM_A_DQS_P<5>
TRUE	MEM_A_DQS_N<5>	MEM_A_DQS_N<5>
TRUE	MEM_A_DQS_P<6>	MEM_A_DQS_P<6>
TRUE	MEM_A_DQS_N<6>	MEM_A_DQS_N<6>
TRUE	MEM_A_DQS_P<7>	MEM_A_DQS_P<7>
TRUE	MEM_A_DQS_N<7>	MEM_A_DQS_N<7>

MAKE_BASE		
TRUE	MEM_B_DQS_P<0>	MEM_B_DQS_P<0>
TRUE	MEM_B_DQS_N<0>	MEM_B_DQS_N<0>
TRUE	MEM_B_DQS_P<1>	MEM_B_DQS_P<1>
TRUE	MEM_B_DQS_N<1>	MEM_B_DQS_N<1>
TRUE	MEM_B_DQS_P<2>	MEM_B_DQS_P<2>
TRUE	MEM_B_DQS_N<2>	MEM_B_DQS_N<2>
TRUE	MEM_B_DQS_P<3>	MEM_B_DQS_P<3>
TRUE	MEM_B_DQS_N<3>	MEM_B_DQS_N<3>
TRUE	MEM_B_DQS_P<4>	MEM_B_DQS_P<4>
TRUE	MEM_B_DQS_N<4>	MEM_B_DQS_N<4>
TRUE	MEM_B_DQS_P<5>	MEM_B_DQS_P<5>
TRUE	MEM_B_DQS_N<5>	MEM_B_DQS_N<5>
TRUE	MEM_B_DQS_P<6>	MEM_B_DQS_P<6>
TRUE	MEM_B_DQS_N<6>	MEM_B_DQS_N<6>
TRUE	MEM_B_DQS_P<7>	MEM_B_DQS_P<7>
TRUE	MEM_B_DQS_N<7>	MEM_B_DQS_N<7>

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE: Memory Bit/Byte Swizzle

Apple Inc.

DRAWING NUMBER: 051-00789 SIZE: D

REVISION: PROTO1A

BRANCH: dvt-fab10

PAGE: 123 OF 145

SHEET: 112 OF 121

High Speed NO_TEST

DMI

- DMI_S2N_P<3..0>
- DMI_S2N_N<3..0>
- DMI_N2S_P<3..0>
- DMI_N2S_N<3..0>

DP - CPU/ACE

- DP_X_SNK0_ML_C_N<3..0>
- DP_X_SNK0_ML_C_P<3..0>
- DP_X_SNK0_ML_N<3..0>
- DP_X_SNK0_ML_P<3..0>
- DP_X_SNK1_ML_C_N<3..0>
- DP_X_SNK1_ML_C_P<3..0>
- DP_X_SNK1_ML_N<3..0>
- DP_X_SNK1_ML_P<3..0>
- DP_T_SNK0_ML_C_N<3..0>
- DP_T_SNK0_ML_C_P<3..0>
- DP_T_SNK0_ML_N<3..0>
- DP_T_SNK0_ML_P<3..0>
- DP_T_SNK1_ML_C_N<3..0>
- DP_T_SNK1_ML_C_P<3..0>
- DP_T_SNK1_ML_N<3..0>
- DP_T_SNK1_ML_P<3..0>
- DP_X_SNK0_AUXCH_C_P
- DP_X_SNK0_AUXCH_C_N
- DP_T_SNK0_AUXCH_C_P
- DP_T_SNK0_AUXCH_C_N
- DP_X_SNK0_AUXCH_P
- DP_X_SNK0_AUXCH_N
- DP_T_SNK0_AUXCH_P
- DP_T_SNK0_AUXCH_N
- DP_X_SNK1_AUXCH_C_P
- DP_X_SNK1_AUXCH_C_N
- DP_T_SNK1_AUXCH_C_P
- DP_T_SNK1_AUXCH_C_N
- DP_X_SNK1_AUXCH_P
- DP_X_SNK1_AUXCH_N
- DP_T_SNK1_AUXCH_P
- DP_T_SNK1_AUXCH_N

CPU/EDP

- EDP_AUXCH_C_N
- EDP_AUXCH_C_P

PCH/AR

- PCIE_AP_D2R_P
- PCIE_AP_D2R_N
- PCIE_AP_R2D_P
- PCIE_AP_R2D_N

- PCIE_AP_R2D_C_P
- PCIE_AP_R2D_C_N

PCH/SSD

- PCIE_SSD_D2R_N<3..0>
- PCIE_SSD_D2R_P<3..0>
- PCIE_SSD_R2D_N<3..0>
- PCIE_SSD_R2D_N<3..0>
- PCIE_SSD_D2R_C_N<3..0>
- PCIE_SSD_R2D_C_N<3..0>
- PCIE_SSD_D2R_N<0>
- PCIE_SSD_D2R_P<0>
- PCIE_SSD_D2R_C_P<3..0>
- PCIE_SSD_R2D_C_N<3..0>
- PCIE_SSD_D2R_LB_P<0>
- PCIE_SSD_R2D_LB_N<0>
- PCIE_SSD_D2R_P<3>
- PCIE_SSD_D2R_LB_N<0>
- PCIE_SSD_D2R_N<3>
- PCIE_SSD_R2D_LB_P<0>

USB-C X

- USBC_XB_D2R_N<2..1>
- USBC_XB_D2R_P<2..1>
- USBC_XA_D2R_P<2..1>
- USBC_XB_R2D_C_P<2..1>
- DP_XA_AUXCH_P
- USBC_XA_D2R_N<2..1>
- USBC_XB_R2D_C_N<2..1>
- USBC_XA_R2D_C_P<2..1>
- DP_XB_AUXCH_P
- USBC_XA_R2D_C_N<2..1>
- DP_XB_AUXCH_N
- DP_XA_AUXCH_N
- DP_XA_AUXCH_C_N
- DP_XA_AUXCH_C_P
- DP_XB_AUXCH_C_P
- DP_XB_AUXCH_C_N

PEG

- PEG_GPU_D2R_N<7..0>
- PEG_GPU_D2R_P<7..0>
- PEG_GPU_R2D_C_N<7..0>
- PEG_GPU_R2D_C_P<7..0>
- PCIE_TBT_X_D2R_P<3..0>
- PCIE_TBT_X_D2R_N<3..0>
- PCIE_TBT_X_R2D_C_P<3..0>
- PCIE_TBT_X_R2D_C_N<3..0>
- PCIE_TBT_T_D2R_P<3..0>
- PCIE_TBT_T_D2R_N<3..0>
- PCIE_TBT_T_D2R_C_P<3..0>
- PCIE_TBT_T_D2R_C_N<3..0>
- PCIE_TBT_X_D2R_C_P<3..0>
- PCIE_TBT_X_D2R_C_N<3..0>
- PCIE_TBT_X_R2D_P<3..0>
- PCIE_TBT_X_R2D_N<3..0>
- PCIE_TBT_T_R2D_P<3..0>
- PCIE_TBT_T_R2D_N<3..0>
- PCIE_TBT_T_R2D_C_P<3..0>
- PCIE_TBT_T_R2D_C_N<3..0>
- PEG_GPU_D2R_C_N<7..0>
- PEG_GPU_D2R_C_P<7..0>
- PEG_GPU_R2D_N<7..0>
- PEG_GPU_R2D_P<7..0>

PCH/DFR

- USB_CAMERA_DFR_N
- USB_CAMERA_DFR_P

BAFFIN FRAME BUFFER

- FB_A1_CS_L
- FB_A0_CKE_L
- FB_A1_CKE_L
- FB_A0_WE_L
- FB_A1_WE_L
- FB_B1_CS_L
- FB_B0_CKE_L
- FB_B1_CKE_L
- FB_B0_WE_L
- FB_B0_WE_L
- FB_B0_CLK_P
- FB_B1_CLK_N
- FB_B1_CLK_P
- FB_B0_RAS_L
- FB_B1_RAS_L
- FB_B0_CAS_L
- FB_B1_CAS_L
- FB_B0_CS_L
- FB_A0_DQ<31..0>
- FB_A1_DQ<31..0>
- FB_A0_A<8..0>
- FB_A1_A<8..0>
- FB_A0_WCLK_N<1..0>
- FB_A0_WCLK_P<1..0>
- FB_A1_WCLK_N<1..0>
- FB_A1_WCLK_P<1..0>
- FB_A0_EDC<3..0>
- FB_A1_EDC<3..0>
- FB_A0_DBI_L<3..0>
- FB_A1_DBI_L<3..0>
- FB_A0_ABI_L
- FB_A1_ABI_L
- FB_A0_CLK_N
- FB_A0_CLK_P
- FB_A1_CLK_N
- FB_A1_CLK_P
- FB_A0_RAS_L
- FB_A1_RAS_L
- FB_A0_CAS_L
- FB_A1_CAS_L
- FB_A0_CS_L
- FB_B0_CLK_N
- FB_B0_DQ<31..0>
- FB_B1_DQ<31..0>
- FB_B0_A<8..0>
- FB_B1_A<8..0>
- FB_B0_WCLK_N<1..0>
- FB_B0_WCLK_P<1..0>
- FB_B1_WCLK_N<1..0>
- FB_B1_WCLK_P<1..0>
- FB_B0_EDC<3..0>
- FB_B1_EDC<3..0>
- FB_B0_DBI_L<3..0>
- FB_B1_DBI_L<3..0>
- FB_B0_ABI_L
- FB_B1_ABI_L

CPU/PCH CLK

- CPU_CLK24M_NSSC_CLK_N
- CPU_CLK24M_NSSC_CLK_P
- CPU_CLK100M_PCIBCLK_N
- CPU_CLK100M_PCIBCLK_P
- CPU_CLK100M_BCLK_N
- CPU_CLK100M_BCLK_P
- PCIE_CLK100M_SSD_N
- PCIE_CLK100M_SSD_P
- PCIE_CLK100M_SSD_LB_N
- PCIE_CLK100M_SSD_LB_P
- NC_ITPXDP_CLK100MN
- NC_ITPXDP_CLK100MP
- PCIE_CLK100M_AP_P
- PCIE_CLK100M_AP_N

MUX

- DP_INT_IG_ML_N<3..0>
- DP_INT_IG_ML_P<3..0>
- DP_INT_IG_AUX_N
- DP_INT_IG_AUX_P
- DP_INT_EG_ML_N<3..0>
- DP_INT_EG_ML_P<3..0>
- DP_INT_EG_AUX_N
- DP_INT_EG_AUX_P

DP MUX CRYSTAL

- DPMUX_UC_XTAL
- DPMUX_UC_EXTAL
- DPMUX_UC_EXTAL_R
- DPMUX_UC_XTAL_R

XTAL

- GPU_XTAL_PU_OR_CAP
- NC_PCH_CLK24M_XTALOUT
- SYSCLK_CLK24M_X2
- SYSCLK_CLK24M_X2_R
- SYSCLK_CLK24M_X1

- TBT_X_XTAL25M_OUT
- TBT_X_XTAL25M_OUT_R
- TBT_X_XTAL25M_IN
- TBT_T_XTAL25M_OUT
- TBT_T_XTAL25M_OUT_R
- SOC_XTAL_24M_O
- TBT_T_XTAL25M_IN
- SOC_XTAL_24M_I
- SOC_XTAL_24M_O_R
- SSD_CLKIN
- SSD_CLKOUT
- SSD_CLKOUT_R
- GPU_XTAL_OUT
- GPU_XTAL_OR_CLK_IN
- GPU_XTAL_XTAL_OR_CLK

MEM

- MEM_A_CAA<9..0>
- MEM_A_CLK_P<1..0>
- MEM_A_CLK_N<1..0>
- MEM_A_DQ<63..0>
- MEM_B_DQ<63..0>
- MEM_A_DQS_P<7..0>
- MEM_A_DQS_N<7..0>
- MEM_B_DQS_P<7..0>
- MEM_B_DQS_N<7..0>
- MEM_A_CAB<9..0>
- MEM_B_CAA<9..0>
- MEM_B_CAB<9..0>
- MEM_B_CLK_P<1..0>
- MEM_B_CLK_N<1..0>

WIFI

- 50_0_ANT
- 50_1_ANT
- 50_2_ANT
- 50_0_COM
- 50_1_COM
- 50_2_COM
- 50_A_0_DIPLEXER
- 50_A_0_MATCH
- 50_G_0_DIPLEXER
- 50_G_0_MATCH
- 50_A_1_DIPLEXER
- 50_A_1_MATCH
- 50_G_1_DIPLEXER
- 50_G_1_MATCH
- 50_A_2_DIPLEXER
- 50_A_2_MATCH
- 50_G_2_DIPLEXER
- 50_G_2_MATCH

USB-C T

- USBC_TA_D2R_P<2..1>
- USBC_TA_D2R_N<2..1>
- USBC_TA_R2D_C_P<2..1>
- USBC_TA_R2D_C_N<2..1>
- DP_TA_AUXCH_P
- DP_TA_AUXCH_N
- DP_TA_AUXCH_C_P
- DP_TA_AUXCH_C_N
- USBC_TB_D2R_P<2..1>
- USBC_TB_D2R_N<2..1>
- USBC_TB_R2D_C_P<2..1>
- USBC_TB_R2D_C_N<2..1>
- DP_TB_AUXCH_P
- DP_TB_AUXCH_N
- DP_TB_AUXCH_C_P
- DP_TB_AUXCH_C_N
- SSD_NAND_FH_DQ4
- SSD_NAND_FH_DQ0
- SSD_NAND_FH_DQS_P
- SSD_NAND_FH_DQ5
- SSD_NAND_FH_DQ6
- SSD_NAND_FH_DQ7
- SSD_NAND_FH_DQS_N

NAND

- SSD_NAND_FA_DQ0
- SSD_NAND_FA_DQ1
- SSD_NAND_FA_DQ2
- SSD_NAND_FA_DQ3
- SSD_NAND_FA_DQ4
- SSD_NAND_FA_DQ5
- SSD_NAND_FA_DQ6
- SSD_NAND_FA_DQ7
- SSD_NAND_FA_DQS_N
- SSD_NAND_FA_DQS_P
- SSD_NAND_FB_DQ0
- SSD_NAND_FB_DQ1
- SSD_NAND_FB_DQ2
- SSD_NAND_FB_DQ3
- SSD_NAND_FB_DQ4
- SSD_NAND_FB_DQ5
- SSD_NAND_FB_DQ6
- SSD_NAND_FB_DQ7
- SSD_NAND_FB_DQS_N
- SSD_NAND_FB_DQS_P
- SSD_NAND_FC_DQ0
- SSD_NAND_FC_DQ1
- SSD_NAND_FC_DQ2
- SSD_NAND_FC_DQ3
- SSD_NAND_FC_DQ4
- SSD_NAND_FC_DQ5
- SSD_NAND_FC_DQ6
- SSD_NAND_FC_DQ7
- SSD_NAND_FC_DQS_N
- SSD_NAND_FC_DQS_P
- SSD_NAND_FD_DQ0
- SSD_NAND_FD_DQ1
- SSD_NAND_FD_DQ2
- SSD_NAND_FD_DQ3
- SSD_NAND_FD_DQ4
- SSD_NAND_FD_DQ5
- SSD_NAND_FD_DQ6
- SSD_NAND_FD_DQ7
- SSD_NAND_FD_DQS_N
- SSD_NAND_FD_DQS_P
- SSD_NAND_FE_DQ0
- SSD_NAND_FE_DQ1
- SSD_NAND_FE_DQ2
- SSD_NAND_FE_DQ3
- SSD_NAND_FE_DQ4
- SSD_NAND_FE_DQ5
- SSD_NAND_FE_DQ6
- SSD_NAND_FE_DQ7
- SSD_NAND_FE_DQS_N
- SSD_NAND_FE_DQS_P
- SSD_NAND_FF_DQ0
- SSD_NAND_FF_DQ1
- SSD_NAND_FF_DQ2
- SSD_NAND_FF_DQ3
- SSD_NAND_FF_DQ4
- SSD_NAND_FF_DQ5
- SSD_NAND_FF_DQ6
- SSD_NAND_FF_DQ7
- SSD_NAND_FF_DQS_N
- SSD_NAND_FF_DQS_P
- SSD_NAND_FG_DQ0
- SSD_NAND_FG_DQ2
- SSD_NAND_FG_DQ3
- SSD_NAND_FG_DQ4
- SSD_NAND_FG_DQ5
- SSD_NAND_FG_DQ6
- SSD_NAND_FG_DQ7
- SSD_NAND_FG_DQS_N
- SSD_NAND_FG_DQS_P
- SSD_NAND_FH_DQ1
- SSD_NAND_FH_DQ2
- SSD_NAND_FH_DQ3

SYNC_MASTER=X363_SAKKOC SYNC_DATE=04/14/2016

PAGE TITLE

ICT & FCT 1

Apple Inc.

DRAWING NUMBER 051-00789 SIZE D

REVISION PROTO1A

BRANCH dvt-fab10

PAGE 124 OF 145

SHEET 113 OF 121

MESA CONNECTOR

45	IN	PP3V0_MESA_CONN	FUNC_TEST=TRUE
45	IN	MESA_SPI_MISO_CONN	FUNC_TEST=TRUE
45	IN	MESA_SNSR_INT_CONN	FUNC_TEST=TRUE
45	IN	MESA_BOOST_EN_CONN	FUNC_TEST=TRUE
45 37	IN	MESA_I2C_SDA	FUNC_TEST=TRUE
45 37	IN	MESA_I2C_SCL	FUNC_TEST=TRUE
45	IN	PP1V8_MESA_CONN	FUNC_TEST=TRUE
45	IN	MESA_SPI_MOSI_CONN	FUNC_TEST=TRUE
45	IN	MENU_KEY_L	FUNC_TEST=TRUE
45	IN	MESA_SPI_CLK_CONN	FUNC_TEST=TRUE
45	IN	PP16V0_MESA_CONN	FUNC_TEST=TRUE
		GND	

SPI ROM

114 109	IN	PP3V3_G3H	FUNC_TEST=TRUE
57	IN	SPI_ALT_IO0_MOSI	FUNC_TEST=TRUE
57	IN	SPI_ALT_IO1_MISO	FUNC_TEST=TRUE
57	IN	SPI_ALT_IO2_WP_L	FUNC_TEST=TRUE
57	IN	SPI_ALT_IO3_HOLD_L	FUNC_TEST=TRUE
76 64 57 48 29 114	IN	SMC_RESET_L	FUNC_TEST=TRUE
57	IN	SPI_ALT_CLK	FUNC_TEST=TRUE
57	IN	SPI_ALT_CS_L	FUNC_TEST=TRUE
57 15	IN	SPIROM_USE_MLB	FUNC_TEST=TRUE
57 47 46	IN	SMC_TMS	FUNC_TEST=TRUE
57 47 46	IN	SMC_TCK	FUNC_TEST=TRUE
		GND	

AUDIO AMP

61	IN	SPKRCONN_TR_OUT_POS	FUNC_TEST=TRUE
61	IN	SPKRCONN_TR_OUT_NEG	FUNC_TEST=TRUE
61	IN	SPKRCONN_WR_OUT_POS	FUNC_TEST=TRUE
61	IN	SPKRCONN_WR_OUT_NEG	FUNC_TEST=TRUE
60	IN	SPKRCONN_TL_OUT_POS	FUNC_TEST=TRUE
60	IN	SPKRCONN_TL_OUT_NEG	FUNC_TEST=TRUE
60	IN	SPKRCONN_WL_OUT_POS	FUNC_TEST=TRUE
60	IN	SPKRCONN_WL_OUT_NEG	FUNC_TEST=TRUE
61 58	IN	SPKR_ID0	FUNC_TEST=TRUE
		GND	FUNC_TEST=

DFR Touch Conn

42	IN	DFR_TOUCH_LID	FUNC_TEST=TRUE
42 38	IN	DFR_TOUCH_GPIO2	FUNC_TEST=TRUE
42 37	IN	DFR_TOUCH_SPI_CS_L	FUNC_TEST=TRUE
42	IN	DFR_TOUCH_SPI_MOSI_R	FUNC_TEST=TRUE
42 38 37	IN	DFR_TOUCH_ROM_I2C_SCL	FUNC_TEST=TRUE
42 38 37	IN	DFR_TOUCH_ROM_I2C_SDA	FUNC_TEST=TRUE
42 37	IN	DFR_TOUCH_RESET_L	FUNC_TEST=TRUE
114 42 37	IN	PP1V8_S0SW_DFR	X2 FUNC_TEST=TRUE
110	IN	PP5V_S0_T139	FUNC_TEST=TRUE
42 38	IN	DFR_TOUCH_PANEL_DETECT	FUNC_TEST=TRUE
114 42 38	IN	DFR_DISP_VSYNC	FUNC_TEST=TRUE
42	IN	DFR_TOUCH_SPI_MISO_R	FUNC_TEST=TRUE
42	IN	DFR_TOUCH_SPI_CLK_R	FUNC_TEST=TRUE
42 38	IN	DFR_TOUCH_INT_L	FUNC_TEST=TRUE
42 38	IN	DFR_CLKIN_RESET_L	FUNC_TEST=TRUE
42 38	IN	DFR_TOUCH_ROM_WC	FUNC_TEST=TRUE
		GND	X4

DFR Disp Conn

114 42 38	IN	DFR_DISP_VSYNC	FUNC_TEST=TRUE
42 38	IN	DFR_DISP_TE	FUNC_TEST=TRUE
42 38	IN	DFR_DISP_INT	FUNC_TEST=TRUE
42	IN	DFR_DISP_RESET_L	FUNC_TEST=TRUE
42	IN	PP3V3_S0SW_DFR	X3 FUNC_TEST=TRUE
42 38	IN	MIPID_CLK_P	FUNC_TEST=TRUE
42 38	IN	MIPID_CLK_N	FUNC_TEST=TRUE
42 38	IN	MIPID_DATA_P	FUNC_TEST=TRUE
42 38	IN	MIPID_DATA_N	FUNC_TEST=TRUE
114 42 37	IN	PP1V8_S0SW_DFR	X2 FUNC_TEST=TRUE
42 38 37	IN	DFRDRV_I2C_SCL	FUNC_TEST=TRUE
42 38 37	IN	DFRDRV_I2C_SDA	FUNC_TEST=TRUE
		GND	X6

KBD CONNECTOR

43	IN	GND_FAN	X2 FUNC_TEST=TRUE
43	IN	PP5V_S0_FAN_CONN	X2 FUNC_TEST=TRUE
115 56 43	IN	FAN_LT_TACH	FUNC_TEST=TRUE
115 56 43	IN	FAN_LT_PWM	FUNC_TEST=TRUE
110	IN	PP5V_S0_KBD	X2 FUNC_TEST=TRUE
114 109	IN	PP3V3_G3H	FUNC_TEST=TRUE
114 43	IN	KBD_BLC_GSSOUT	FUNC_TEST=TRUE
114 43	IN	KBD_BLC_GSLAT	FUNC_TEST=TRUE
110 103 29	IN	PP3V3_S4	FUNC_TEST=TRUE
114 43	IN	KBD_BLC_GSSIN	FUNC_TEST=TRUE
43	IN	KBD_BLC_XBLANK	FUNC_TEST=TRUE
115 56 43	IN	FAN_RT_TACH	FUNC_TEST=TRUE
115 56 43	IN	FAN_RT_PWM	FUNC_TEST=TRUE
114 43	IN	KBD_I2C_SDA	FUNC_TEST=TRUE
114 43	IN	KBD_INT_L	FUNC_TEST=TRUE
114 43	IN	KBD_I2C_SCL	FUNC_TEST=TRUE
114 48 43	IN	SMC_LSOC_RST_L	FUNC_TEST=TRUE
114 43	IN	KBD_BLC_GSSCK	FUNC_TEST=TRUE
		GND	X5

TPAD CONNECTOR

114 43	IN	KBD_I2C_SCL	FUNC_TEST=TRUE
114 43	IN	KBD_I2C_SDA	FUNC_TEST=TRUE
114 43	IN	KBD_INT_L	FUNC_TEST=TRUE
49 46	IN	SMBUS_SMC_3_SDA	FUNC_TEST=TRUE
49 46	IN	SMBUS_SMC_3_SCL	FUNC_TEST=TRUE
110	IN	PP3V3_S4_TPAD	FUNC_TEST=TRUE
43	IN	PP5V_S4_TPAD_CONN	FUNC_TEST=TRUE
43	IN	ACT_GND	X4 FUNC_TEST=TRUE
43	IN	PPVIN_S4_TPAD_FUSE	X4 FUNC_TEST=TRUE
43 13	IN	TPAD_SPI_CLK	FUNC_TEST=TRUE
43	IN	TPAD_SPI_IF_EN_CONN	FUNC_TEST=TRUE
43 13	IN	TPAD_SPI_MISO	FUNC_TEST=TRUE
43	IN	TPAD_SPI_CS_L_CONN	FUNC_TEST=TRUE
43 13	IN	TPAD_SPI_MOSI	FUNC_TEST=TRUE
43	IN	TPAD_SPI_INT_L_CONN	FUNC_TEST=TRUE
48 46	IN	SMC_ACTUATOR_DISABLE_L	FUNC_TEST=TRUE
48 47 46	IN	SMC_PME_S4_WAKE_L	FUNC_TEST=TRUE
48 47 43 42	IN	SMC_LID	FUNC_TEST=TRUE
114 43	IN	KBD_BLC_GSLAT	FUNC_TEST=TRUE
114 43	IN	KBD_BLC_GSSCK	FUNC_TEST=TRUE
114 43	IN	KBD_BLC_GSSOUT	FUNC_TEST=TRUE
46 43	IN	SMC_VIBE_L	FUNC_TEST=TRUE
114 43	IN	KBD_BLC_GSSIN	FUNC_TEST=TRUE
		GND	X3

eDP

116 76 75	IN	PPVOUT_S0_LCDBKLT	FUNC_TEST=TRUE
76	IN	PP3V3_S0SW_LCD	X2 FUNC_TEST=TRUE
76	IN	EDP_AUXCH_C_N	FUNC_TEST=TRUE
76	IN	EDP_AUXCH_C_P	FUNC_TEST=TRUE
111 76	IN	EDP_INT_ML_N<0>	FUNC_TEST=TRUE
111 76	IN	EDP_INT_ML_P<0>	FUNC_TEST=TRUE
111 76	IN	EDP_INT_ML_N<1>	FUNC_TEST=TRUE
111 76	IN	EDP_INT_ML_P<1>	FUNC_TEST=TRUE
111 76	IN	EDP_INT_ML_N<2>	FUNC_TEST=TRUE
111 76	IN	EDP_INT_ML_P<2>	FUNC_TEST=TRUE
111 76	IN	EDP_INT_ML_N<3>	FUNC_TEST=TRUE
111 76	IN	EDP_INT_ML_P<3>	FUNC_TEST=TRUE
38	IN	MIPIC_CLK_N	FUNC_TEST=TRUE
38	IN	MIPIC_CLK_P	FUNC_TEST=TRUE
76	IN	PP5V_S0SW_LCD	FUNC_TEST=TRUE
76 38	IN	PP5V_S0_ALSCAM_F	FUNC_TEST=TRUE
76 42	IN	I2C_ALS_SDA	FUNC_TEST=TRUE
76 42	IN	I2C_ALS_SCL	FUNC_TEST=TRUE
76 38 37	IN	I2C_CAM_SCL	FUNC_TEST=TRUE
76 38 37	IN	I2C_CAM_SDA	FUNC_TEST=TRUE
111 76	IN	I2C_BKLT_SDA	FUNC_TEST=TRUE
111 76	IN	I2C_BKLT_SCL	FUNC_TEST=TRUE
49 46	IN	SMBUS_SMC_0_S0_SDA	FUNC_TEST=TRUE
49 46	IN	SMBUS_SMC_0_S0_SCL	FUNC_TEST=TRUE
76 48	IN	BKLT_PWM_TCON2MLB	FUNC_TEST=TRUE
76 20	IN	BKLT_PWM_MLB2TCON	FUNC_TEST=TRUE
89 76	IN	LCD_FSS	FUNC_TEST=TRUE
76 15	IN	LCD_IRQ_L	FUNC_TEST=TRUE
76	IN	BUF_EDP_PANEL_PWR_EN	FUNC_TEST=TRUE
89 76	IN	DP_INT_HPD	FUNC_TEST=TRUE
		GND	X3
76 49	IN	SMBUS_SMC_0_S0_SCL	FUNC_TEST=TRUE
76 49	IN	SMBUS_SMC_0_S0_SDA	FUNC_TEST=TRUE
38	IN	MIPIC_DATA_P	FUNC_TEST=TRUE
38	IN	MIPIC_DATA_N	FUNC_TEST=TRUE

AUDIO JACK

62	IN	AUD_CONN_HP_LEFT	FUNC_TEST=TRUE
62	IN	AUD_CONN_HP_RIGHT	FUNC_TEST=TRUE
62	IN	AUD_CONN_RING2	FUNC_TEST=TRUE
62	IN	AUD_CONN_SLEEVE	FUNC_TEST=TRUE
62	IN	AUD_CONN_HP_SENSE_L	FUNC_TEST=TRUE
62	IN	AUD_CONN_HP_SENSE_R	FUNC_TEST=TRUE
62	IN	AUD_CONN_TIP_SENSE	FUNC_TEST=TRUE
62	IN	AUD_CONN_SLEEVE_XW	FUNC_TEST=TRUE
62	IN	AUD_CONN_RING2_XW	FUNC_TEST=TRUE
		GND	X2

BATTERY TUBA

64 63	IN	PPVBAT_G3H_CONN	X7 FUNC_TEST=TRUE
49 46	IN	SMBUS_SMC_5_G3_SCL	FUNC_TEST=TRUE
49 46	IN	SMBUS_SMC_5_G3_SDA	FUNC_TEST=TRUE
63	IN	TP_BMON_IOUT	FUNC_TEST=TRUE
64 56	IN	CHGR_AMON	FUNC_TEST=TRUE
64 56	IN	CHGR_BMON	FUNC_TEST=TRUE
63	IN	SYS_DETECT_L	FUNC_TEST=TRUE
		GND	X5
114 48 43	IN	SMC_LSOC_RST_L	FUNC_TEST=TRUE
64	IN	TBA_COMP	FUNC_TEST=TRUE
64	IN	TBA_VDDA	FUNC_TEST=TRUE
64	IN	TBA_LX1	FUNC_TEST=TRUE
64	IN	TBA_LX2	FUNC_TEST=TRUE
		GND	X2
64	IN	PPVBAT_G3H_CHGR_REG	X5 FUNC_TEST=TRUE
116 64 63	IN	PPDCIN_G3H_CHGR	X5 FUNC_TEST=TRUE

USB_C

TP_UPC_XA_SWD_DATA	---------->	TP3001
TP_UPC_XA_SWD_CLK	---------->	TP3002
TP_UPC_XB_SWD_DATA	---------->	TP3003
TP_UPC_XB_SWD_CLK	---------->	TP3004

104 103	IN	TP_UPC_TA_DBG_UART_TX	FUNC_TEST=TRUE
104 103	IN	TP_UPC_TA_DBG_UART_RX	FUNC_TEST=TRUE
105 103	IN	TP_UPC_TB_DBG_UART_TX	FUNC_TEST=TRUE
105 103	IN	TP_UPC_TB_DBG_UART_RX	FUNC_TEST=TRUE
30 29	IN	UPC_XA_DBG_UART_TX	FUNC_TEST=TRUE
30 29	IN	UPC_XA_DBG_UART_RX	FUNC_TEST=TRUE
31 29	IN	TP_UPC_XB_DBG_UART_TX	FUNC_TEST=TRUE
31 29	IN	TP_UPC_XB_DBG_UART_RX	FUNC_TEST=TRUE
116 115 106	IN	PP20V_USBC_TB_VBUS_CONN	X5 FUNC_TEST=TRUE
116 115 106	IN	PP20V_USBC_TA_VBUS_CONN	X5 FUNC_TEST=TRUE
		GND	X5
116 115 32	IN	PP20V_USBC_XB_VBUS_CONN	X4 FUNC_TEST=TRUE
116 115 32	IN	PP20V_USBC_XA_VBUS_CONN	X5 FUNC_TEST=TRUE
		GND	X5

SSD DEBUG CONNECTOR

115 87 77	IN	SSD_BOOT_LB_L	FUNC_TEST=TRUE
80 77	IN	SSD_BOOT_LB_L	FUNC_TEST=TRUE
103 86 80	IN	SSD_DEBUG_I2C_CLK_CONN	FUNC_TEST=TRUE
103 86 80	IN	SSD_DEBUG_I2C_DAT_CONN	FUNC_TEST=TRUE
80 77 48	IN	SMC_OOB1_R2D_L	FUNC_TEST=TRUE
80 77 48	IN	SMC_OOB1_D2R_L	FUNC_TEST=TRUE
83 82 81 80 78 77 85 80	IN	PP1V8_SSD_FMC	
		GND	

MIC

58	IN	DMIC1_CLK	FUNC_TEST=TRUE
58	IN	DMIC1_DATA	FUNC_TEST=TRUE
58	IN	DMIC2_CLK	FUNC_TEST=TRUE
58	IN	DMIC2_DATA	FUNC_TEST=TRUE
109 61	IN	PP1V8_S0	FUNC_TEST=TRUE
		GND	

USB-C PROBE BLOCK TESTING

32	IN	TP_J3300_P2	FUNC_TEST=TRUE	TPAC580
32	IN	TP_J3300_P56	FUNC_TEST=TRUE	TPAC581
106	IN	TP_JB500_P2		TPAC582
106	IN	TP_JB500_P56	FUNC_TEST=TRUE	TPAC583

ADDITIONAL TPs

110	IN	PP3V3_S5	FUNC_TEST=TRUE	TPAC584
110	IN	PP3V3_SUS	FUNC_TEST=TRUE	TPAC585

Wifi & SSD fixture Test Points
(row,col)=(4,2) Diameter=0.6mm Pitch=1mm

Right Side - Top Layer

	SSD_JTAG_TMS	TPAC528
80 77	SSD_JTAG_TCK	TPAC519
80 77	SSD_JTAG_TDI	TPAC520
80 77	SSD_JTAG_TDO	TPAC521
86 77	SSD_DEBUG_I2C_CLK	TPAC522
86 77	SSD_DEBUG_I2C_DAT	TPAC523
84 77	SSD_PGOOD_L	TPAC524
		TPAC535

(row,col)=(2,6) Diameter=0.6mm Pitch=1mm

Left Side - Top Layer

50 114	PPDCIN_G3H	TPAC500
50 114	PPDCIN_G3H	TPAC501
50 114	PPDCIN_G3H	TPAC502
50 114	PPDCIN_G3H	TPAC503
		TPAC504
		TPAC505
		TPAC506
		TPAC507
	GND (TRUE)	TPAC529
64	HPWR_EN_L	TPAC512
110	PP3V3_S0	TPAC536
114 109	PP3V3_G3H	TPAC518

(row,col)=(5,5) Diameter=0.6mm Pitch=1mm

Middle - Top Layer

46 48 45 47	SMC_ONOFF_L	TPAC517
		TPAC538
28 20 114	SMC_RESET_L	TPAC539
		TPAC527
14	USB3_TEST_D2R_N	TPAC510
14	USB3_TEST_D2R_P	TPAC511
		TPAC595
		TPAC596
84 78	PP1V0_SSD_CORE	TPAC598
109	PPVCC_S0_CPU	TPAC597
109	PPBUS_G3H	TPAC599
14	USB3_TEST_R2D_N	TPAC525
14	USB3_TEST_R2D_P	TPAC526
20 35	AP_RESET_L	TPAC537
14	USB_TEST_P	TPAC530
14	USB_TEST_N	TPAC531
20 115	SSD_RESET_L	TPAC532
46 12 75	PM_PCH_SYS_PWROK	TPAC533
87 14 115	SSD_PWR_EN	TPAC534
46 29 47	SMC_DEBUGPRT_TX_L	TPAC508
46 29 47	SMC_DEBUGPRT_RX_L	TPAC509
87 15 115 101	SSD_BOOT_L	TPAC513
73 72 57 49 89 76	PM_SLP_S3_L	TPAC514
48	SMC_DEV_SUPPLY_R_L	TPAC515
20 32 35	PLT_RST_L	TPAC516

PAGE TITLE
ICT & FCT 2

Apple Inc.

DRAWING NUMBER 051-00789 SIZE D
REVISION PROTO1A
BRANCH dvt-fab10
PAGE 125 OF 145
SHEET 114 OF 121

OTHER TEST POINTS / NC

NC with No Testpoint Property

13	NC_CLINK_CLK	1	TRUE	NC_CLINK_CLK	
13	NC_CLINK_DATA	1	TRUE	NC_CLINK_DATA	
13	NC_CLINK_RESET_L	1	TRUE	NC_CLINK_RESET_L	
113 18 12	NC_ITPXDP_CLK100MN	1	TRUE	NC_ITPXDP_CLK100MN	
113 18 12	NC_ITPXDP_CLK100MP	1	TRUE	NC_ITPXDP_CLK100MP	
13	NC_HDA_SDIN1	1	TRUE	NC_HDA_SDIN1	

I11	1	NC_SPI_SMC_MOSI	48
I12	1	NC_SPI_SMC_MISO	48
I14	1	NC_SPI_SMC_CS_L	48
I13	1	NC_SPI_SMC_CLK	48
I17		NC_PCH_CLK32K_RTCX2	20

FAN Test Points

I125	TRUE	FAN_LT_PWM	43 56 114
I126	TRUE	FAN_LT_TACH	43 56 114
I127	TRUE	PP5V_S0	38 110 115
I128	TRUE	FAN_RT_PWM	43 56 114
I129	TRUE	FAN_RT_TACH	43 56 114
I130	TRUE	PP5V_S0	38 110 115

XDP Test-Points

I152	TRUE	XDP_CPU_TCK	6 18
I153	TRUE	XDP_PCH_TCK	13 18
I157	TRUE	XDP_CPU_TDI	6 18
I156	TRUE	XDP_CPU_TDO	6 18
I155	TRUE	XDP_CPU_TRST_L	6 13 18
I154	TRUE	XDP_CPU_TMS	6 18
I158	TRUE	XDP_PCH_TMS	13 18
I162	TRUE	XDP_PCH_TDI	13 18
I161	TRUE	XDP_PCH_TDO	13 18
I160	TRUE	XDP_CPU_PREQ_L	6 13 18
I159	TRUE	XDP_CPU_PRDY_L	6 13 18
I163	TRUE	PM_RSMRST_L	12 18 46 73
I164	TRUE	PM_PCH_PWROK	12 70
I165	TRUE	PM_SYSRST_L	12 18 46
I166	TRUE	CPU_CFG<3>	6 18

CPU (Refer to CPU pages)

CPU_DC_B2_C1	TP0501
CPU_DC_B38_C38	TP0502
CPU_DC_BR2_BR1	TP0503
CPU_DC_C1_B2	TP0504
CPU_DC_C38_B38	TP0505
CPU_DC_BR1_BR2	TP0610
CPU_DC_BR38_BT36	TP0900
CPU_DC_BT36_BR38	TP0901

PCH (Refer to PCH pages)

XDP_PCH_OBSDATA_A0	TP1883
XDP_PCH_OBSDATA_A1	TP1884
XDP_PCH_OBSDATA_A2	TP1870
XDP_PCH_OBSDATA_A3	TP1871
XDP_PCH_OBSDATA_B0	TP1872
XDP_PCH_OBSDATA_B1	TP1885
XDP_PCH_OBSDATA_B2	TP1886
XDP_PCH_OBSDATA_B3	TP1887
XDP_PCH_OBSDATA_D0	TP1877
XDP_PCH_OBSDATA_D1	TP1878
XDP_PCH_OBSDATA_D2	TP1879
XDP_PCH_OBSDATA_D3	TP1880
XDP_PCH_OBSFN_C0	TP1882
XDP_BPM_L<0>	TP1800
XDP_BPM_L<1>	TP1801
XDP_BPM_L<2>	TP1802
XDP_BPM_L<3>	TP1803
NC_USB_EXTA_OC_L	TP1873
NC_USB_EXTB_OC_L	TP1874
NC_USB_EXTC_OC_L	TP1875
NC_USB_EXTD_OC_L	TP1876

TPs on BOTTOM to check USB-C Instalation

I175	USBC_XA_SBU1	FUNC_TEST=TRUE	30 32
I176	USBC_XB_SBU1	FUNC_TEST=TRUE	31 32
I177	USBC_XA_SBU2	FUNC_TEST=TRUE	30 32
I178	USBC_XB_SBU2	FUNC_TEST=TRUE	31 32
I179	USBC_TA_SBU1	FUNC_TEST=TRUE	104 106
I180	USBC_TB_SBU1	FUNC_TEST=TRUE	105 106
I181	USBC_TA_SBU2	FUNC_TEST=TRUE	104 106
I182	USBC_TB_SBU2	FUNC_TEST=TRUE	105 106
I183	PP20V_USBC_XA_VBUS_CONN	FUNC_TEST=TRUE	32 114 116
I186	PP20V_USBC_XB_VBUS_CONN	FUNC_TEST=TRUE	32 114 116
I185	PP20V_USBC_TA_VBUS_CONN	FUNC_TEST=TRUE	106 114 116
I184	PP20V_USBC_TB_VBUS_CONN	FUNC_TEST=TRUE	106 114 116

TPs to check LifeBoat Instalation

I188	PP3V3_S5_POLARIS	FUNC_TEST=TRUE	84 87
I187	PP3V3_S5	FUNC_TEST=TRUE	110
I190	SSD_PWR_EN	FUNC_TEST=TRUE	14 87 114
I189	SSD_PWR_LB_EN	FUNC_TEST=TRUE	84 87
I191	SSD_BOOT_L	FUNC_TEST=TRUE	15 87 114
I192	SSD_BOOT_LB_L	FUNC_TEST=TRUE	77 87 114
I193	SSD_RESET_L	FUNC_TEST=TRUE	14 20 87 114
I195	SSD_RESET_LB_L	FUNC_TEST=TRUE	77 87
I194	SSD_CLKREQ_L	FUNC_TEST=TRUE	20 87
I196	SSD_CLKREQ_LB_L	FUNC_TEST=TRUE	77 87

SYNC_MASTER=K363_BBABAD1 SYNC_DATE=01/26/2016

PAGE TITLE

NC & No Test

Apple Inc.

DRAWING NUMBER 051-00789 SIZE D

REVISION PROTO1A

BRANCH dvt-fab10

PAGE 126 OF 145

SHEET 115 OF 121

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
131S00041	6	CAP,CER,12PF,5%,100V,C0G,0402	CC784,CC785,CC786,CC787,CC788	CRITICAL	

PAGE TITLE

Desense Caps

Apple Inc.

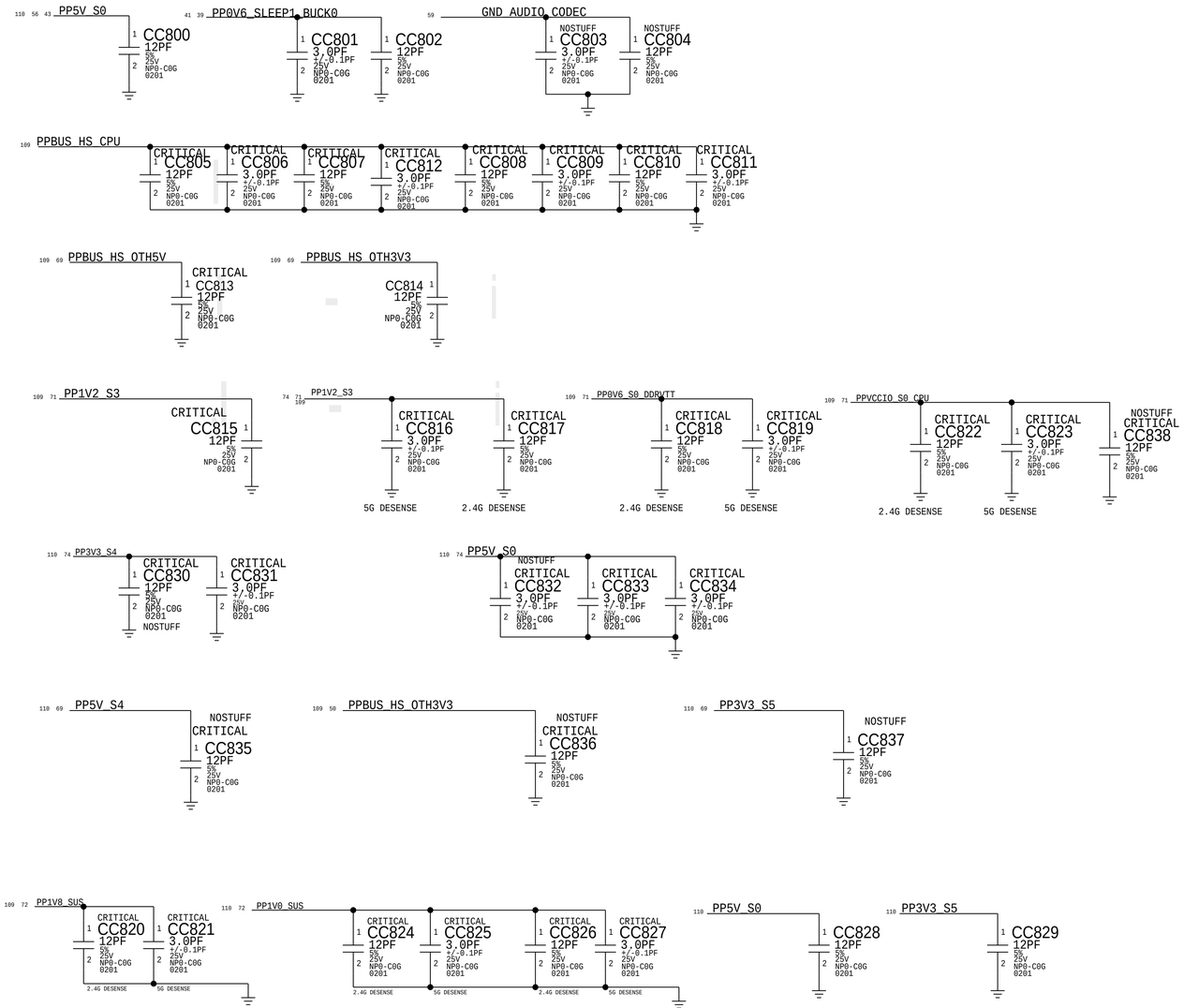
DRAWING NUMBER 051-00789 SIZE D

REVISION PR0T01A

BRANCH dvt-fab10

PAGE 127 OF 145

SHEET 116 OF 121



BOM_COST_GROUP=WIRELESS

PAGE TITLE: Desense Caps

Apple Inc.

DRAWING NUMBER: 051-00789
SIZE: D
REVISION: PROTO1A
BRANCH: dvt-fab10
PAGE: 128 OF 145
SHEET: 117 OF 121

SYNC_MASTER=X363_ZIFENGSHEN SYNC_DATE=06/02/2016

PAGE TITLE

Project Specific Constraints

Apple Inc.

DRAWING NUMBER 051-00789

SIZE D

REVISION PROTO1A

BRANCH dvt-fab10

PAGE 130 OF 145

SHEET 118 OF 121

BOM Variants

BOM Variants, Power/Socket Configs

BOM NUMBER	BOM NAME	BOM OPTIONS
639-01966	PCBA,MLB,NONE,SM-16,FB4-SM,S256,X363	BASE_BOM,DEVEL_BOM,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,SSD_CONFIG:256GB
639-01967	PCBA,MLB,SKT,VDDC,SM-16,FB4-SM,S256,X363	BASE_BOM,DEVEL_BOM,STARDUST:VDDC,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,SSD_CONFIG:256GB
639-01968	PCBA,MLB,SKT,MVDD,SM-16,FB4-SM,S256,X363	BASE_BOM,DEVEL_BOM,STARDUST:VDDCI_MVDD,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,SSD_CONFIG:256GB
639-01969	PCBA,MLB,SKT,CPU,SM-16,FB4-SM,S256,X363	BASE_BOM,DEVEL_BOM,CPU_SKL:SOCKET,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,SSD_CONFIG:256GB

SYNC_MASTER=J80_MLB SYNC_DATE=07/23/2015

PAGE TITLE

639 BOM Configuration

Apple Inc.

DRAWING NUMBER 051-00789 SIZE D

REVISION PROTO1A

BRANCH dvt-fab10

PAGE 141 OF 145

SHEET 119 OF 121

BOM Variants

SYNC_MASTER=J80_MLB SYNC_DATE=07/23/2015

PAGE TITLE

639 BOM Configuration 2

Apple Inc.

DRAWING NUMBER 051-00789

SIZE D

REVISION PROTO1A

BRANCH dvt-fab10

PAGE 142 OF 145

SHEET 120 OF 121

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
740S0144	740S0118		ALL		
740S00003	740S0135		ALL		
376S1089	376S1128		ALL		
376S1080	376S0820		ALL		
376S00086	376S0761		ALL		
376S00074	376S0855		ALL		
376S00014	376S0761		ALL		
372S0186	372S0185		ALL		
371S0713	371S0558		ALL		
311S00060	311S0273		ALL		
311S00004	311S0370		ALL		
155S0914	155S0897		ALL		
155S0694	155S0387		ALL		
155S0660	155S0513		ALL		
155S00154	155S0398		ALL		
155S00007	155S0667		ALL		
138S0863	138S0853		ALL		
138S0775	138S0860		ALL		<rdar://problem/23155097> for IG <rdar://problem/23564467> for EG
138S0703	138S0648		ALL		<rdar://problem/23118084> for IG <rdar://problem/> for EG
132S00064	132S0409		ALL		
128S0325	128S0397		ALL		
128S00029	128S00007		ALL		
128S00026	128S00011		ALL		
128S00070	128S00007		ALL		<rdar://problem/25329164>
128S00009	128S00007		ALL		
107S0249	107S0251		ALL		
107S00071	107S00053		ALL		
107S00070	107S0085		ALL		
107S00033	107S00034		ALL		BLC
107S00015	107S00011		ALL		
376S1106	376S0678		ALL	Fairchild alt to Vishay	BLC
138S0738	138S1101		ALL	Samsung alt to Murata	
138S0846	138S0811		ALL	Samsung alt to Murata	
376S1053	376S0604		ALL	Diodes alt to Fairchild	
152S00359	152S00253		ALL	Chillisin alt to Cyntec	
740S00027	740S0159		ALL	Bourns alt to Little Fuse	
371S0704	371S00077		ALL	NXP alt to Diodes	
138S00032	138S0831		ALL		
138S00049	138S0831		ALL		
998-04070	998-04071		OFF	Hynix alt to SS	220uF 2.0V D-case, 128S00044 DQ - T208
128S00010	128S00011		ALL		
128S00031	128S00011		ALL		
138S00084	138S0060		ALL		<rdar://problem/23118634> for IG <rdar://problem/23527737> for EG
155S00155	155S0441		OFF		(Stale; delete later after page sync)
155S00190	155S0897		ALL		
353S00107	353S3239		ALL		
353S00525	353S4471		ALL		
376S1193	376S00037		OFF		
740S00028	740S0118		ALL		
152S00369	152S00268		ALL	Cyntec w/ NEC	<rdar://problem/23405116> for IG <rdar://problem/23542193> for EG
128S0296	128S0487		ALL	NEC w/ pana	<rdar://problem/23422212> for IG <rdar://problem/23527282> for EG
128S00012	128S0487		ALL	NEC w/ Rohm	
155S00188	155S0275		ALL	Murata w/ Taiyo	<rdar://problem/23446936> for IG <rdar://problem/23542939> for EG
155S00018	155S0664		ALL	Murata w/ Taiyo	<rdar://problem/23447549> for IG <rdar://problem/23543068> for EG
152S00388	152S00182		ALL		<rdar://problem/23542023>
107S0240	107S0255		ALL		<rdar://problem/23520324>
128S00062	128S00067		ALL	NEC for Panasonic	150uF 6.3V B12
138S0660	138S0684		ALL		<rdar://problem/24316249>
155S00204	155S0731		ALL		<rdar://problem/24310837>

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
311S0271	311S00008		ALL	NXP w/ Diodes	(Stale; delete later after page sync) <rdar://problem/23117984> for IG <rdar://problem/24316367> for EG
197S00046	197S00036		ALL	Epson w/ TXC	<rdar://problem/23117749> for IG <rdar://problem/23543146> for EG
197S00047	197S00036		ALL	Kyocera w/ TXC	
197S00048	197S00036		ALL	Murata w/ TXC	
197S00053	197S00050		ALL	Kyocera w/ TXC	<rdar://problem/23117849> for IG <rdar://problem/23543858> for EG
197S00054	197S00050		ALL	NDK w/ TXC	
197S00055	197S00050		ALL	Murata w/ TXC	
311S0596	311S0593		ALL	NXP w/ Diodes	<rdar://problem/23118093> for IG <rdar://problem/23544824> for EG
107S0276	107S00020		ALL	Cyntec w/ TFT	<rdar://problem/23117951> for IG <rdar://problem/23542980> for EG
107S00021	107S0284		ALL	TFT w/ Yageo	<rdar://problem/23129685> for IG <rdar://problem/23519943> for EG
132S00012	132S0401		ALL	Taiyo w/ Murata&TDK	<rdar://problem/23118402> for IG <rdar://problem/23527525> for EG
152S00343	152S1682		ALL	NXP w/ Diodes	<rdar://problem/23541694> for IG <rdar://problem/23541871> for EG
107S00087	107S00029		ALL	TFT w/ Yageo	<rdar://problem/23121290> for IG <rdar://problem/23520039> for EG
128S00057	128S00018		ALL	NEC w/ Vishay	<rdar://problem/23363718> for IG <rdar://problem/23526361> for EG
128S00058	128S00018		ALL	NEC w/ Rohm	
128S0364	128S0264		ALL	Kemet w/ Panasonic	<rdar://problem/23366105> for IG <rdar://problem/23527232> for EG
138S0641	138S0700		ALL	Murata w/ SS&Taiyo	<rdar://problem/23118759> for IG <rdar://problem/23528188> for EG
138S0739	138S0706		ALL	NEC w/ Vishay	<rdar://problem/23118915> for IG <rdar://problem/23528364 for EG
138S0945	138S0706		ALL	NEC w/ Rohm	
152S00358	152S00208		ALL	Murata w/ Chillisin	<rdar://problem/23119390> for IG <rdar://problem/23542869> for EG
152S00389	152S00241		OFF	Cyntec w/ Vishay	<rdar://problem/23342644> for IG <rdar://problem/> for EG
152S00390	152S00265		OFF	Cyntec w/ Vishay	<rdar://problem/23342719> for IG <rdar://problem/> for EG
152S00400	152S1872		ALL	Murata w/ Cyntec	
152S1872	152S00361		ALL	Murata w/ Cyntec	<rdar://problem/23132240> for IG <rdar://problem/23542412> for EG
155S00034	155S0706		ALL	Taiyo w/ Murata	<rdar://problem/23118020> for IG <rdar://problem/23543015> for EG
371S00082	371S00046		ALL	On-Semi w/ Diodes	<rdar://problem/23341512> for IG <rdar://problem/23545301> for EG
376S00146	376S1061		ALL	NXP w/ Diodes	<rdar://problem/23341674> for IG <rdar://problem/23545469> for EG
353S00711	353S2073		ALL	On Semi w/ TI	<rdar://problem/23605939> for IG <rdar://problem/23605957> for EG
740S00019	740S00007		ALL	Bourns w/ Polytronics	<rdar://problem/23137505> for IG <rdar://problem/23545479> for EG
155S00189	155S0342		ALL	Murata w/ Taiyo	<rdar://problem/23117986> for IG <rdar://problem/23543015> for EG
132S0438	132S0428		ALL	Murata w/ Taiyo&TDK	<rdar://problem/23118548> for IG <rdar://problem/23527609> for EG
138S0714	138S0713		ALL	Murata w/ Samsung	<rdar://problem/23118842> for IG <rdar://problem/23528300> for EG
138S0715	138S0732		ALL	Murata w/ Samsung	<rdar://problem/23118873> for IG <rdar://problem/23528349> for EG
107S00086	107S00056		ALL	TFT w/ Cyntec	<rdar://problem/23121312> for IG <rdar://problem/23520074> for EG
138S0875	138S0678		ALL	Taiyo w/ Mur&SS	<rdar://problem/23129763> for IG <rdar://problem/23528106> for EG
138S0786	138S0705		ALL	Murata w/ Samsung	<rdar://problem/23129934> for IG <rdar://problem/23528216> for EG
155S0382	155S0659		ALL	Murata w/ TDK	<rdar://problem/23132624> for IG <rdar://problem/23543045> for EG
152S2052	152S1954		ALL	Taiyo w/ Cyntec	<rdar://problem/23135833> for IG <rdar://problem/23542478> for EG
152S2015	152S1958		ALL	Taiyo w/ Cyntec	<rdar://problem/23137154> for IG <rdar://problem/23542579> for EG
128S00055	128S00002		ALL	Kemet w/ Panasonic	<rdar://problem/23148659> for IG <rdar://problem/23526236> for EG
138S0748	138S0751		ALL	Murata w/ SS	<rdar://problem/23155052> for IG <rdar://problem/23528417> for EG
138S00102	138S0773		ALL	Murata w/ Taiyo	<rdar://problem/23155089> for IG <rdar://problem/23529046> for EG
138S0789	138S0941		ALL	Murata w/ SS	<rdar://problem/23155132> for IG <rdar://problem/23529142> for EG
107S00101	107S00005		ALL	Cyntec w/ Yageo	<rdar://problem/23193801> for IG <rdar://problem/23519872> for EG
107S00102	107S00017		ALL	Cyntec w/ Yageo	<rdar://problem/23194019> for IG <rdar://problem/23519914> for EG
107S00100	107S00057		ALL	Cyntec w/ TFT	<rdar://problem/23224358> for IG <rdar://problem/23520119> for EG
107S00103	107S00058		ALL	Cyntec w/ Yageo	<rdar://problem/23228523> for IG <rdar://problem/23520163> for EG
107S00104	107S00061		ALL	Cyntec w/ Yageo	<rdar://problem/23229217> for IG <rdar://problem/23520193> for EG
107S00105	107S00062		ALL	Cyntec w/ Yageo	<rdar://problem/23230371> for IG <rdar://problem/23520241> for EG
152S00403	152S00322		ALL	Murata w/ Chillisin	<rdar://problem/23341061> for IG <rdar://problem/23542282> for EG
353S00852	353S4262		ALL	TI w/ OnSemi	<rdar://problem/23341158> for IG <rdar://problem/23542282> for EG
138S00104	138S0978		ALL		<rdar://problem/23583487>
128S00069	128S00067		ALL	Rohm for Panasonic	150uF 6.3V B12 <rdar://problem/23527054>
138S0759	138S0762		ALL		<rdar://problem/23582324>
377S0077	377S0183		ALL		<rdar://problem/23640745>
152S00363	152S00048		ALL		<rdar://problem/23541533>
138S00111	138S00036		ALL		<rdar://problem/23546425>
138S00097	138S0750		ALL		<rdar://problem/23581953>
155S00203	155S0894		ALL		<rdar://problem/24285018>
116S00006	116S0175		ALL		<rdar://problem/23524119>
311S00104	311S00091		ALL		<rdar://problem/23640575>

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
311S00013	311S0508		ALL	Part will be stuffed in production	<rdar://problem/24316400>
311S00118	311S0489		ALL		<rdar://problem/27623384>
311S00072	311S0657		ALL		<rdar://problem/23595055>
311S00090	311S00028		ALL		<rdar://problem/23602138>
353S00750	353S00877		ALL		<rdar://problem/23545068>
353S00878	353S00599		ALL		<rdar://problem/23545040>
311S00105	311S0233		ALL		<rdar://problem/24316381>
353S00880	353S3452		ALL		<rdar://problem/23545099>
311S00007	311S0426		ALL		<rdar://problem/23597412>
128S0445	128S0392		ALL		<rdar://problem/23566873>
152S00415	152S00140		ALL		<rdar://problem/23766197>
128S0436	128S0392		ALL		<rdar://problem/23566873>
343S00135	343S00136		ALL	T208	
343S00137	343S00136		ALL	T208	
343S00138	343S00136		ALL	T208	
138S00105	138S00037		ALL		<rdar://problem/23640133>
152S00434	152S1829		ALL		<rdar://problem/23825631>
353S3527	353S3528		ALL		<rdar://problem/24492801>
353S3526	353S3528		ALL		<rdar://problem/24492801>
353S00135	353S00034		ALL		<rdar://problem/24534121>
353S2220	353S00034		ALL		<rdar://problem/24534121>
353S00769	353S4398		ALL		<rdar://problem/24534714>
353S00879	353S00754		ALL		<rdar://problem/23545080>
104S00012	155S0398		ALL		<rdar://problem/25180014>
353S4342	353S00854		ALL		<rdar://problem/23621422>
152S00543	152S00484		ALL		<rdar://problem/24780681>
371S00089	371S00085		ALL		<rdar://problem/24806090>
107S00111	107S00110		ALL		<rdar://problem/24968171>
335S00213	335S0888		ALL		<rdar://problem/24985900>
311S0437	311S00112		ALL		<rdar://problem/24747570>
377S0178	377S00031		ALL		<rdar://problem/25118595>
371S00091	371S00083		ALL		<rdar://problem/24827333>
197S00069	197S00068		ALL		<rdar://problem/24473517>
138S0698	138S00113		ALL		<rdar://problem/23528153>
152S00461	152S00112		ALL		<rdar://problem/24417973>
371S00074	371S0602		ALL		<rdar://problem/25919460>
197S00082	197S00081		ALL		
353S00991	353S00920		ALL		
131S00134	131S00041		ALL		<rdar://problem/24316117>

PAGE TITLE

Alternates BOM Table

Apple Inc.

DRAWING NUMBER 051-00789 | SIZE D

REVISION PROTO1A

BRANCH dvt-fab10

PAGE 145 OF 145

SHEET 121 OF 121