COMPAL CONFIDENTIAL

MODEL NAME : CAZ20

PCB NO : LA-E131P

BOM P/N : 431A4331L0X

Steamboat 14" AR

Kabylake U

2016-11-9

REV : 1.0 (A00)

@ : Nopop Component

EMI@ : EMI Component
@EMI@ : EMI Nopop Component
ESD@ : ESDComponent
@ESD@ : ESD Nopop Component
RF@ : RF Component
@RF@ : RF Nopop Component
CXDP@ : XDP Component
CONN@ : Connector Component
ESPI@ : ESPI interface Component
LPC@ : External ESPI Component (SHD)
GT3@ : KBL-U 2+3e Component
INFI@ : Infinity SKU Component

For Compal only

MB PCB

Part Number	Description
DA800188010	PCB 1S1 LA-E131P REV0 MB AR 1

Layout Dell logo

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REV:A00
PWB:

Power CKT : 1107

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Title: Cover Sheet

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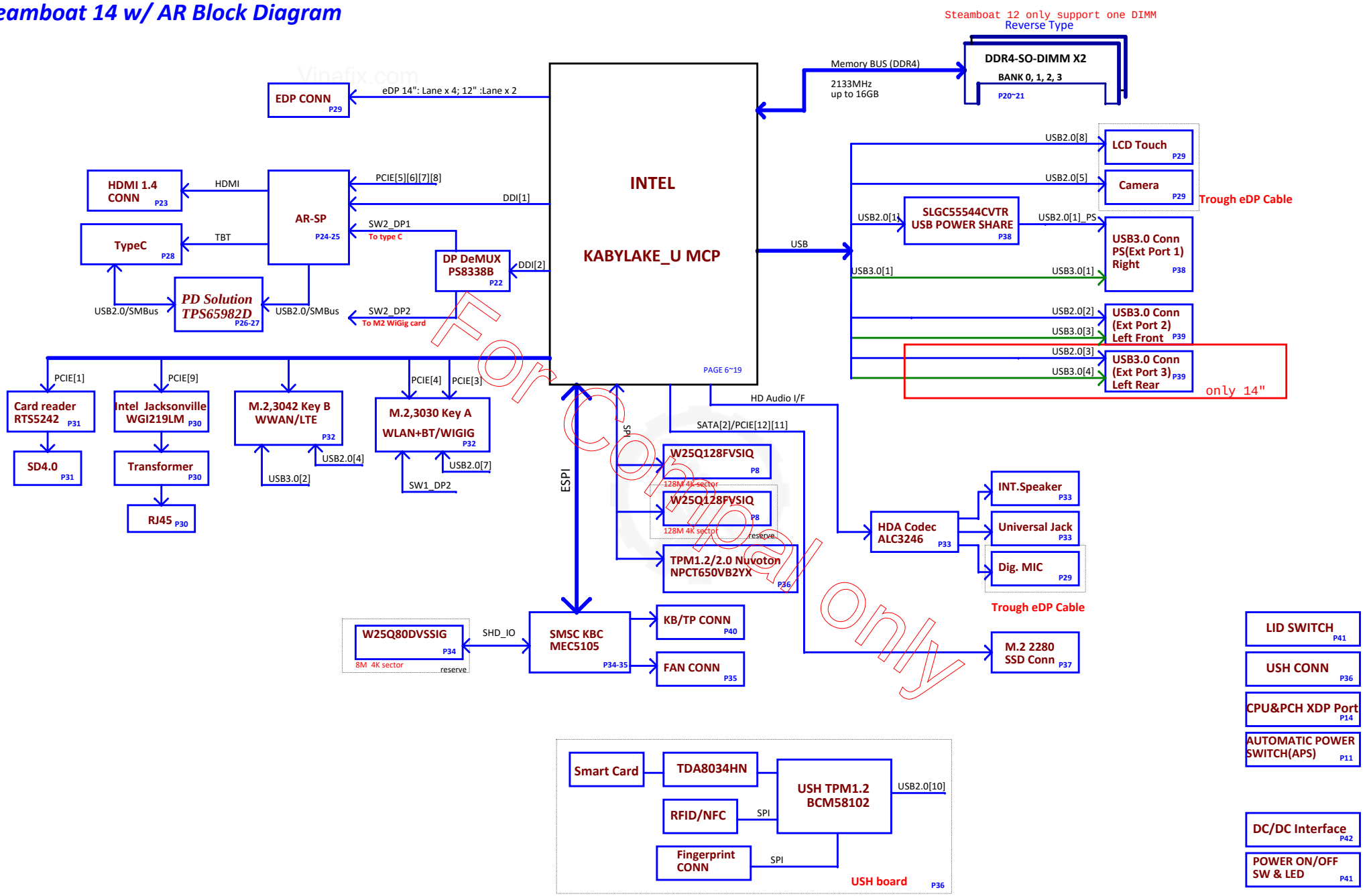
Steamboat 14 w/ AR Block Diagram



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Title: Block diagram

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AR config

POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ power plane	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT	+3.3V_CV2 +1.2V_MEM +2.5V_MEM +1.0V_VCCST	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.8V_RUN +VCC_CORE +VCC_GT +VCC_SA +1.0VS_VCCIO
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF

USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				JUSB1-->Right
USB3.0-2	SSIC			M.2 3042(LTE)
USB3.0-3				JUSB2-->Left Front
USB3.0-4				JUSB3-->Left Rear (SB14 only)
USB3.0-5		PCIE-1		Card Reader (PCIE)
USB3.0-6		PCIE-2		NA
		PCIE-3		M.2 3030(WLAN)
		PCIE-4		M.2 3030(WIGIG)
		PCIE-5		Alpine Ridge - SP
		PCIE-6		
		PCIE-7	SATA-0	
		PCIE-8	SATA-1	
		PCIE-9		LOM
		PCIE-10		NA
		PCIE-11	SATA-1*	M.2 2280 SSD (PCIex2 or SATA)
		PCIE-12	SATA-2	

12" not support JUSB3

USB PORT#	DESTINATION
1	JUSB1-->Right
2	JUSB2-->Left Front
3	JUSB3-->Left Rear (SB14 only)
4	M2 3042(WWAN)
5	Camera
6	NA
7	M.2 3030(BT)
8	Touch Screen
9	NA
10	USH

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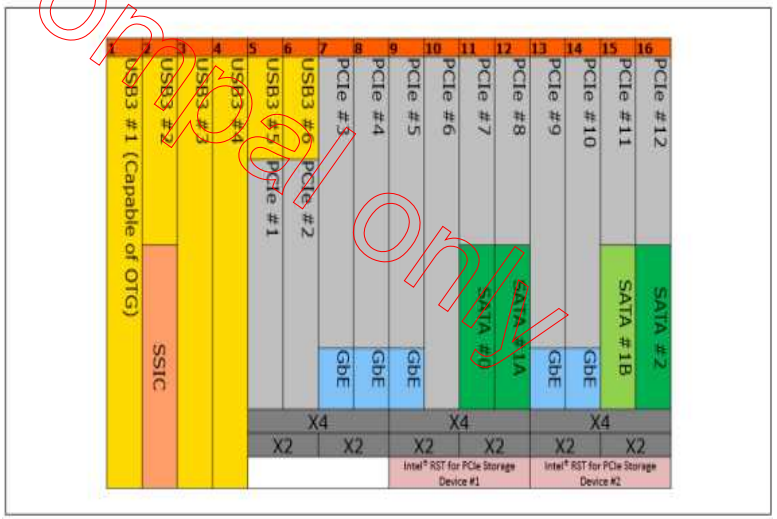
High Speed I/O (HSIO) Lane Multiplexing in KBL U



Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	GA-150LL	0.50
			Add Plating		0.95
1	Top		Copper foil	0.5oz	0.65
		3.7	Prepreg	1080 or1086	2.75
2	GND/PWR		Copper foil	0.5oz	0.60
		4	Core	4mil	4.00
3	Sig 1		Copper foil	0.5oz	0.60
		4.1	Prepreg	7628HRC	7.70
4	GND/PWR		Copper foil	1.0oz	1.25
		3.8	Core	4mil	4.00
5	Sig2		Copper foil	1.0oz	1.25
		4	Prepreg	7628	7.10
6	Sig3		Copper foil	0.5oz	0.60
		3.8	Core	4mil	4.00
7	GND/PWR		Copper foil	0.5oz	0.60
		3.7	Prepreg	1080 or1086	2.75
8	Bottom		Copper foil	0.5oz	0.65
			Add Plating		0.95
			SolderMask		0.50
	Overall Thickness (1.0mm ± 10%)		39.4		41.40000

1.05156

AR use 1086PP
Non AR use 1080PP

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Title: Port assignment

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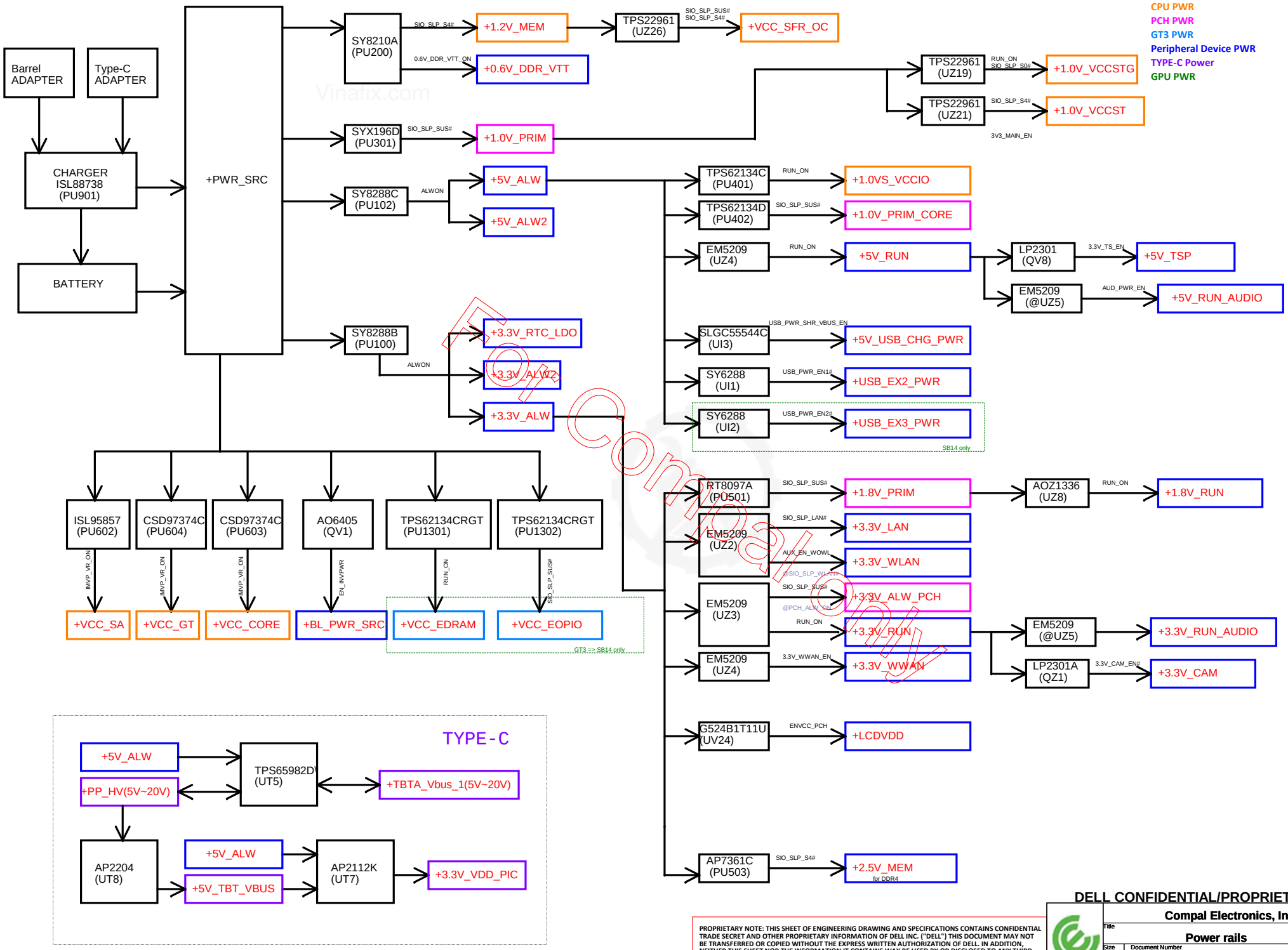

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Title	Power rails	
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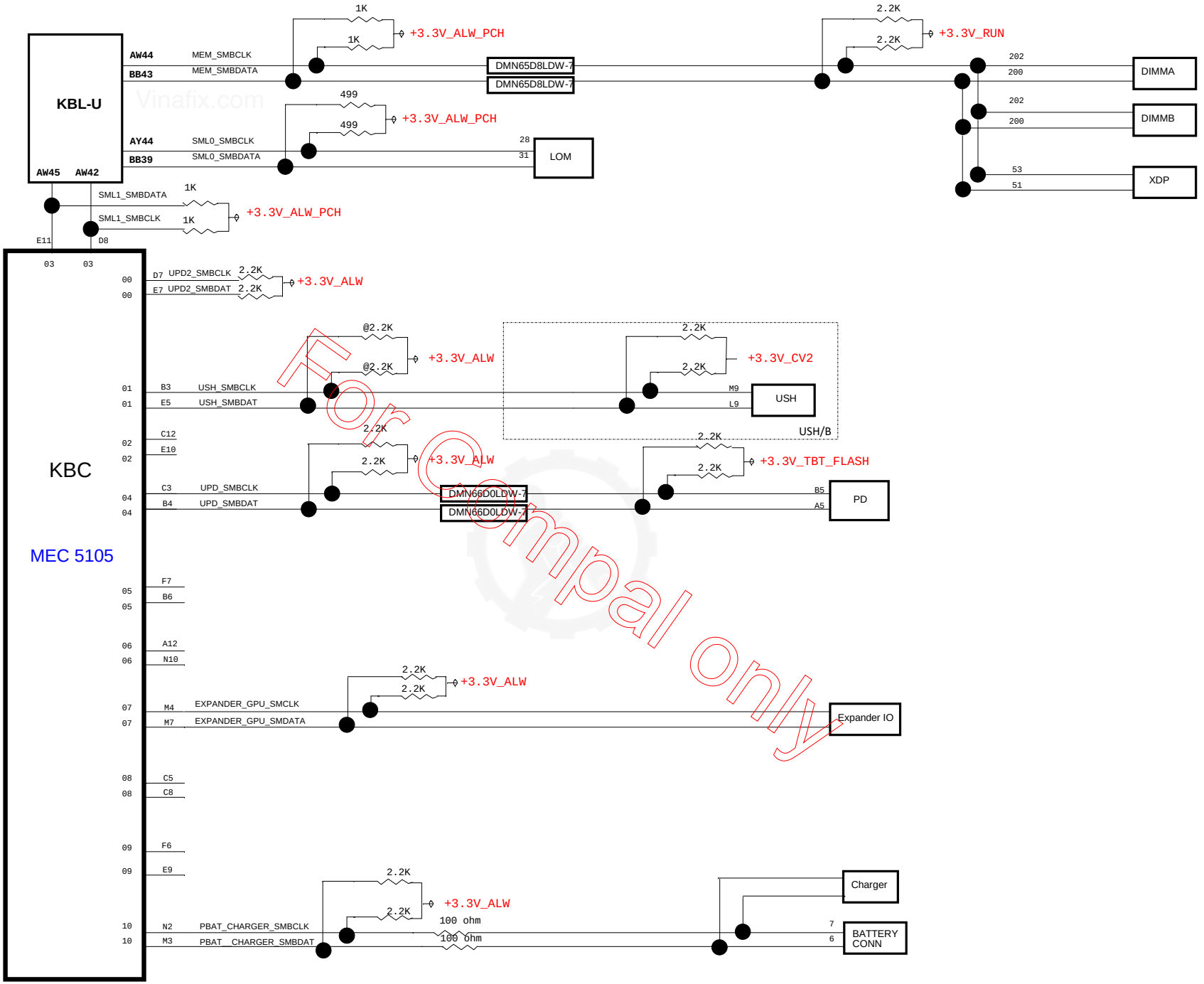

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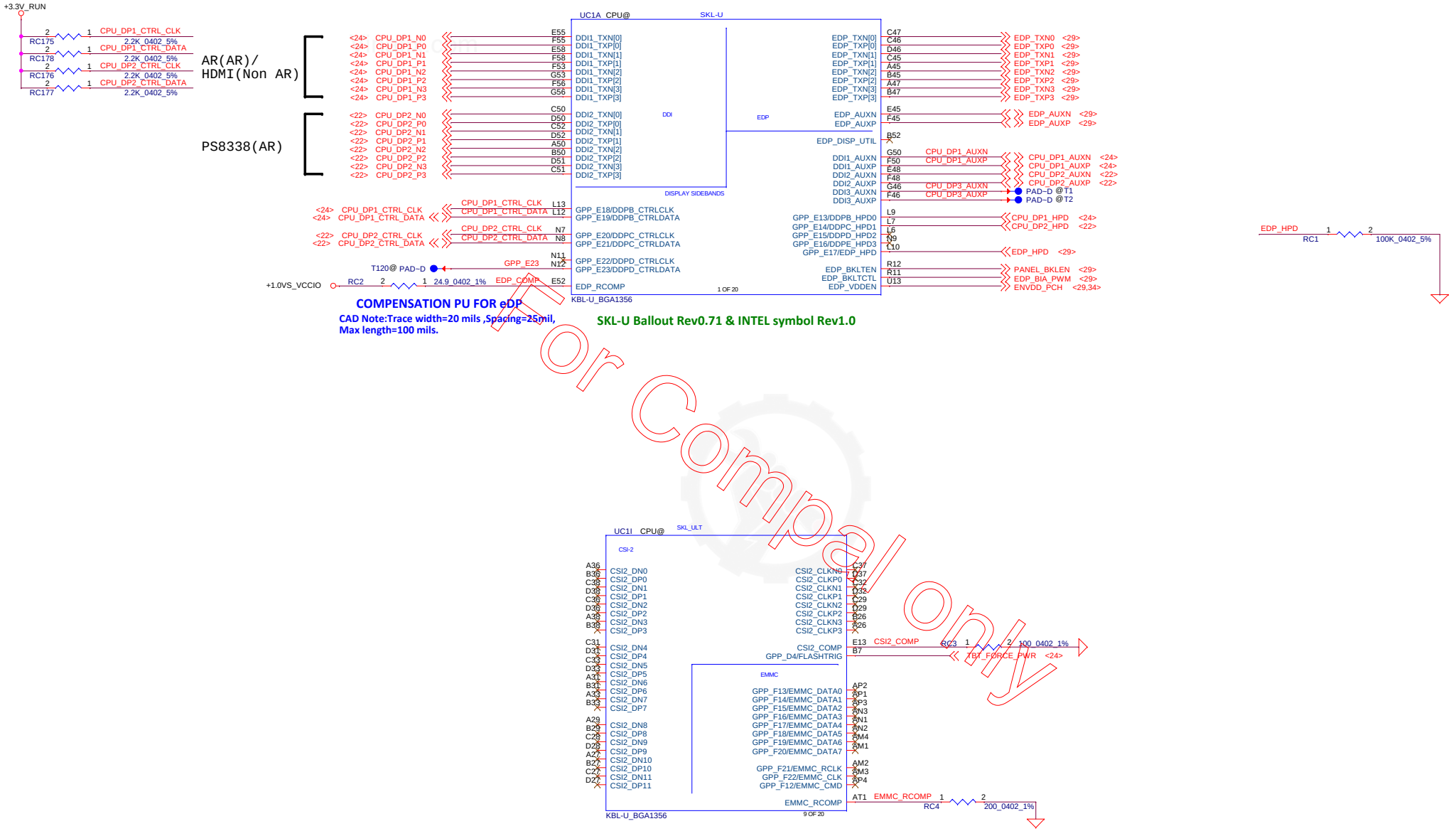

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Title: CPU (1/14)

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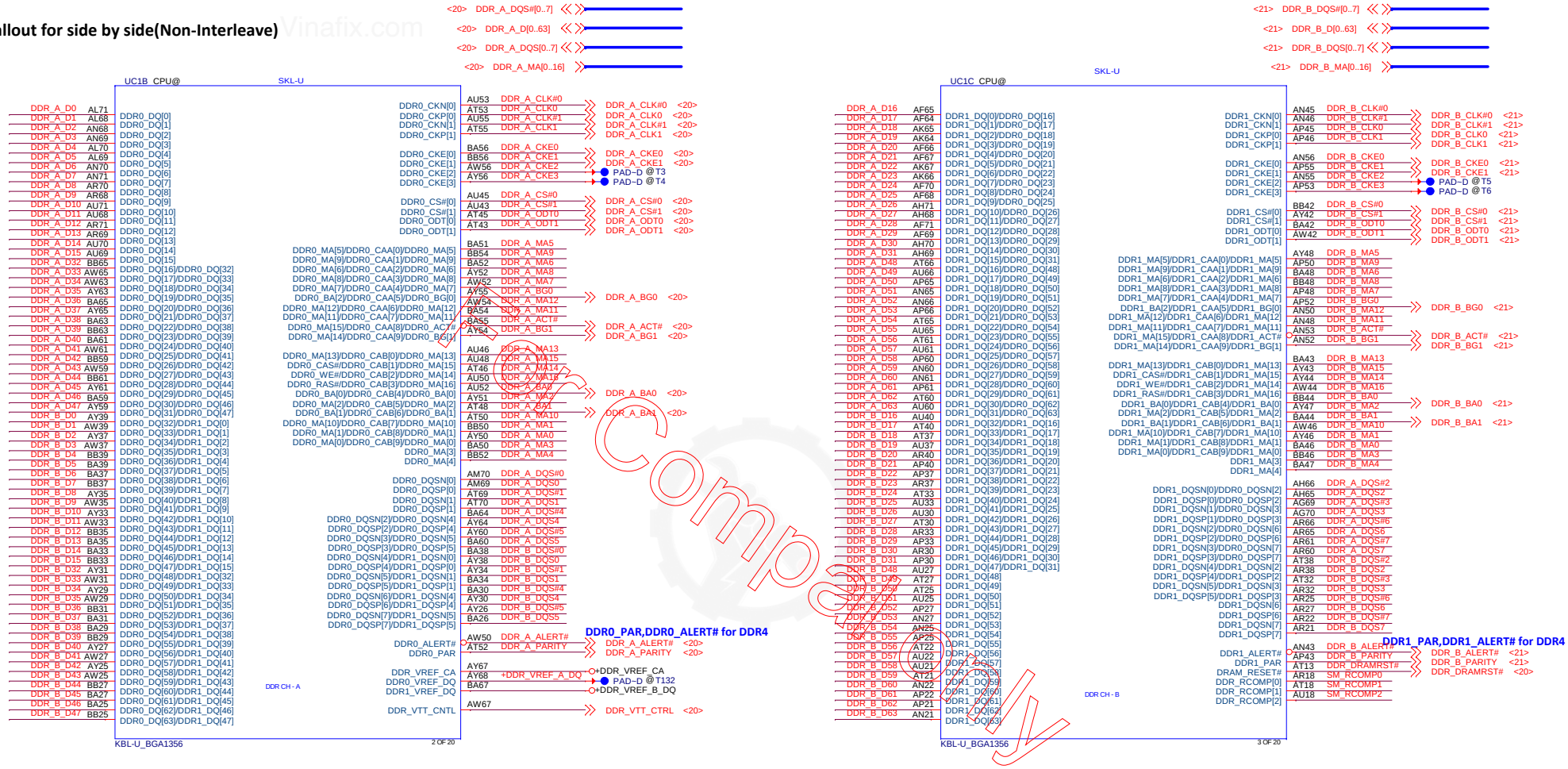
For DDR4

DDR4, Ballout for side by side(Non-Interleave)



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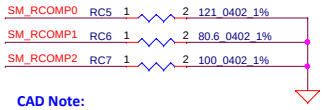
DDR4 COMPENSATION SIGNALS



CAD Note:
Trace width=12~15 mil, Spacing=20 mils
Max trace length= 500 mil

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Title: CPU (2/14)

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SPI_MOSI= SPI_IO0
SPI_MISO= SPI_IO1
PCH EDS R0.7 p.235~236

For BR/SB

UC1E CPU@ SKL-U

SPI - FLASH

SPI - TOUCH

C LINK

SMBUS, SMLINK

LPC

KBL-U_BGA1356

5 OF 20

+1.8V?

SOFTWARE TAA

RF Request

Place close CPU side

128Mb Flash ROM

W25Q128FVSIQ_SO8

03/02:follow Intel MOW_2015WW06

TLS CONFIDENTIALITY

HIGH	ENABLE
LOW(DEFAULT)	DISABLE

WEAK INTERNAL 20K PD

EC interface

HIGH	ESPI
LOW(DEFAULT)	LPC

WEAK INTERNAL 20k PD

EXI BOOT STALL BYPASS

HIGH	ENABLED
LOW(DEFAULT)	DIABLED

WEAK INTERNAL PD

CHECK LPC_CLK FOR DEBUG CARD?

Reserve

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Title: CPU (3/14)

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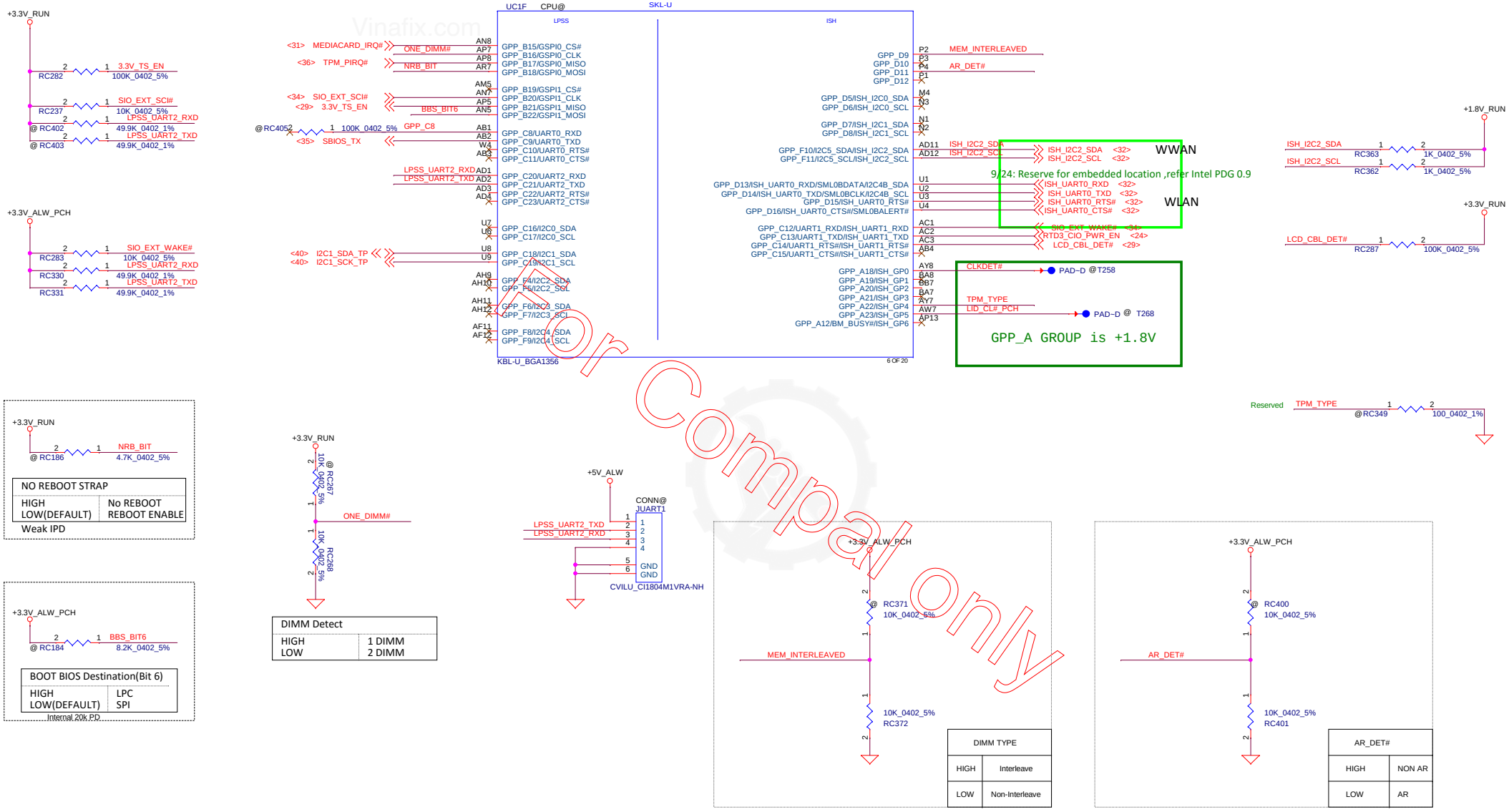
For BR/SB



NO REBOOT STRAP	
HIGH	No REBOOT
LOW(DEFAULT)	REBOOT ENABLE

Weak IPD

BOOT BIOS Destination(Bit 6)	
HIGH	LPC
LOW(DEFAULT)	SPI

Internal 20k PD

DIMM Detect	
HIGH	1 DIMM
LOW	2 DIMM

DIMM TYPE	
HIGH	Interleave
LOW	Non-Interleave

AR_DET#	
HIGH	NON AR
LOW	AR

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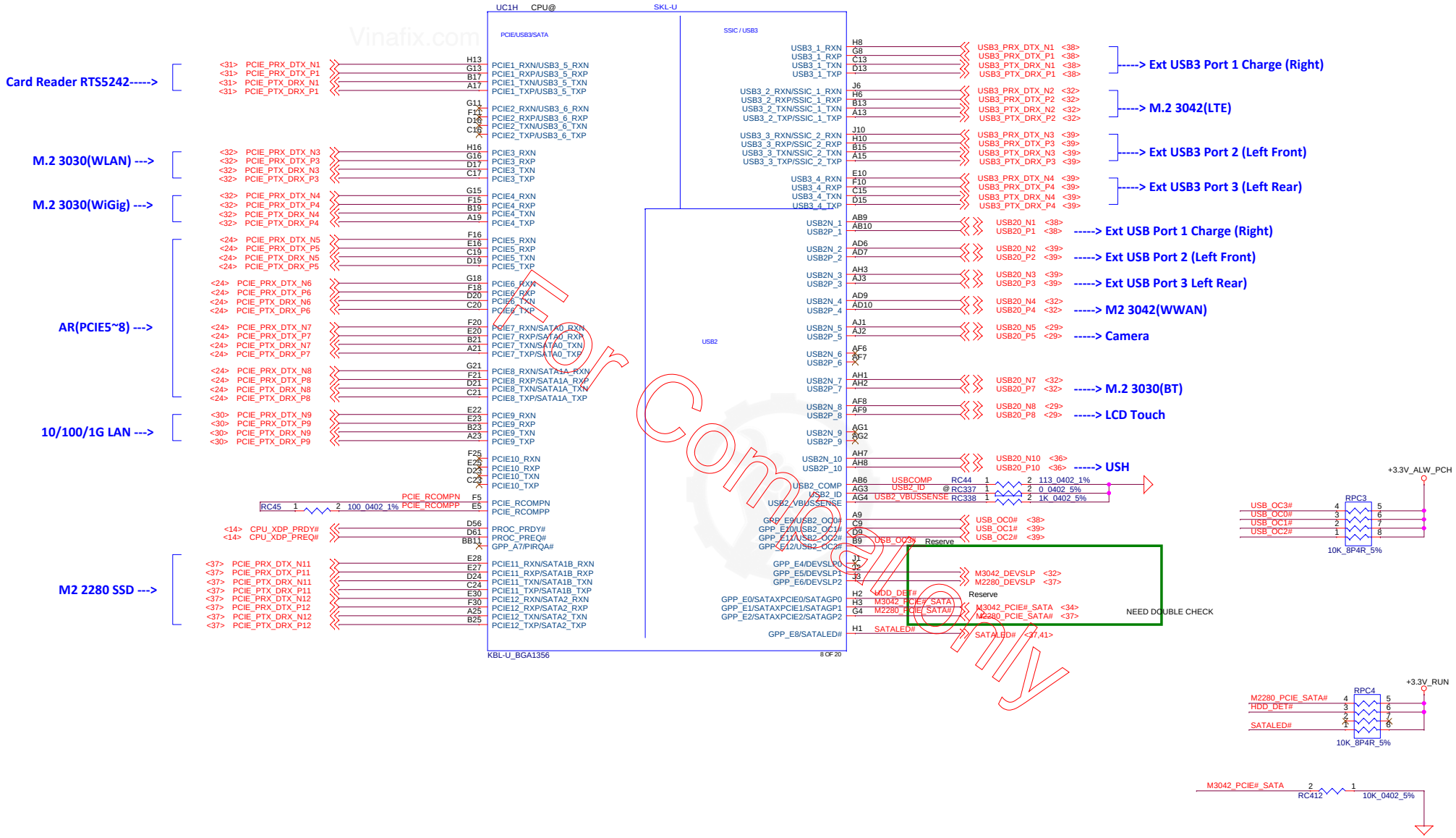
For AR,Steamboat12/14



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Title: CPU (5/14)

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For SB/KW UMA w AR

Cardreader--->
WLAN--->
WIGIG--->
M.2 SDD--->
LAN--->
AR --->

UC1J CPU@ SKL_ULT
CLOCK SIGNALS
KBL-U_BGA1356
10 OF 20

CC21 12P_0402_50V8J
YC1 24MHZ_12PF_X3G024000DC1H
CC22 12P_0402_50V8J
RC46 1M_0402_1%
XTAL24_IN
XTAL24_OUT
XTAL24_OUT_R
0_0402_5%
For Skylake,YC1 24 MHz (50 Ohm ESR)
For Cannonlake,YC1 38.4 MHz (30 Ohm ESR)
546765_546765_2014WW48_Skylake_MOW_Rev_1_0

CC23 15P_0402_50V8J
YC2 32.768KHZ_12.5PF_9H03200042
ESR MAX=50k ohm
CC26 12P_0402_50V8J
RC54 10M_0402_5%
PCH_RTCX1
PCH_RTCX2
PCH_RTCX2_R

RC52 2.7K_0402_1%
RC324 59_0402_1%
For Skylake, pop RC52,depop RC324
For Cannonlake, pop RC324,depop RC52
546765_546765_2014WW48_Skylake_MOW_Rev_1_0
+1.0V_CLK5
+RTC_CELL
CC24 1U_0402_6.3V6K
CC25 1U_0402_6.3V6K
RC56 20K_0402_5%
RC57 20K_0402_5%
SHORT PADS-D
@CMOS1
CMOS1 must take care short & touch risk on layout placement

8/21 can change to 10K for merge to RP
PCH_BATLOW# RC72 8.2K_0402_5%
AC_PRESENT RC243 10K_0402_5%
+3.3V_ALW_DSW

INTRUDER# RC69 1M_0402_5%
MPHYP_PWR_EN @RC387 10K_0402_5%
VRALERT# @RC73 10K_0402_5%
@RC344 10K_0402_5%
SIO_SLP_LAN# @RC68 10K_0402_5%
SUSCLK @RC48 1K_0402_5%

+3.3V_LAN
@RL70 LAN_WAKE# 10K_0402_5%
+3.3V_ALW_DSW
RC323 10K_0402_5%
RC67 PCH_PCIE_WAKE# 1K_0402_5%
+1.0V_VCCST
RC71 VCCST_PWRGD 1K_0402_5%
+3.3V_ALW_PCH
@RC74 ME_SUS_PWR_ACK 10K_0402_5%
10/6 depop, prevent singal step.
@RC411 PCH_PWROK 10K_0402_5%

PCH_PLTRST# @RC62 0_0402_5% PLTRST_LAN# <30>
@RC244 0_0402_5% PCH_PLTRST#_EC <35>
+3.3V_ALW_PCH
UC7 TC7SH08FU_SSOP5-D
PCH_PLTRST#_AND
PCH_PLTRST#_AND <24,31,32,36,37>
@RC65 100K_0402_5%

PCH_PLTRST# @RC60 0_0402_5% PLTRST_TPM# <36>
PCH_PLTRST#_AND @RC325 0_0402_5%

UC1K CPU@ SKL-U
SYSTEM POWER MANAGEMENT
KBL-U_BGA1356
11 OF 20

PCH_PLTRST# SYS_RESET# PCH_RSMRST#_AND
<14,40> PCH_RSMRST#_AND
T9 @ PAD-D <14,34,35> VCCST_PWRGD
H_CPUPWRGD_R @RC77 1K_0402_5%
RC78 60.4_0402_1%
H_CPUPWRGD
VCCST_PWRGD_CPU
<14,34> SYS_PWROK
<49> PCH_PWROK
<35> PCH_DPWROK
<34> ME_SUS_PWR_ACK
<34> SUSACK#
<34,35> PCH_PCIE_WAKE#
<30,34> LAN_WAKE#
<30> PM_LANPHY_ENABLE
<29> 3.3V_CAM_EN#
RC311 10K_0402_5%

GPP_B12/SLP_S0# AT11 SIO_SLP_S0#
GPD4/SLP_S3# AP15
GPD5/SLP_S4# BA16
GPD10/SLP_S5# AY16
SLP_SUS# AN15
SLP_LAN# AW15
GPD9/SLP_WLAN# BB17
GPD6/SLP_A# AN16
GPD3/PWRBTN# BA15
GPD1/ACPRESENT AY15
GPD0/BATLOW# AU13 PCH_BATLOW#
GPP_A11/PME# AU11 PME#
INTRUDER# AP16 INTRUDER#
GPP_B11/EXT_PWR_GATE# AM10 MPHYP_PWR_EN
GPP_B2/VRALERT# AM11 VRALERT#
PAD-D @T115
connect to VCCMPHYGTAON_1P0 enable pin

SIO_SLP_S0# <17,36,47>
SIO_SLP_S3# <24,34,35>
SIO_SLP_S4# <17,34,45,48>
SIO_SLP_S5# <34>
SIO_SLP_SUS# <17,34,42,46,47,48,54>
SIO_SLP_LAN# <34,42>
SIO_SLP_WLAN# <34,42>
SIO_SLP_A# <34>
SIO_PWRBTN# <14,34>
AC_PRESENT <34>

JAPS1
+3.3V_ALW_PCH SIO_SLP_S3#
+3.3V_ALW SIO_SLP_S5#
SIO_SLP_S4#
SIO_SLP_A#
+3.3V_ALW
PCH_RTCRST#
<35,41> POWER_SW#_MB
SYS_RESET#
SIO_SLP_S0#
GND GND
CONN@ ACES_50506-01841-P01

H_CPUPWRGD ESD@ 100P_0402_50V8J CC300
VCCST_PWRGD ESD@ 100P_0402_50V8J CC301
ESD Request:place near CPU side

SYS_RESET# @ESD@ 0.1U_0402_25V6 CC302
ESD Request:place near CPU side

RC215
POP NO Support Deep sleep
DE-POP Support Deep sleep

PCH_DPWROK @RC215 0_0402_5% PCH_RSMRST#_AND
@CC266 0.01UF_0402_25V7K
RC220 100K_0402_1%
RC75 10K_0402_5%

<14> XDP_DBRESET# XDP_DBRESET#
@RC290 0_0402_5%
+3.3V_RUN
@RC225 8.2K_0402_5%
@RC227 8.2K_0402_5%
ME_RESET#
@UC12 74AHC1G09GW_TSSOP5
SYS_RESET#_R RC224 1K_0402_5%
SYS_RESET#
RC291 @ 10K_0402_5%
if pop UC12, RC291 also need pop(74AHC1G09GW is OD output)

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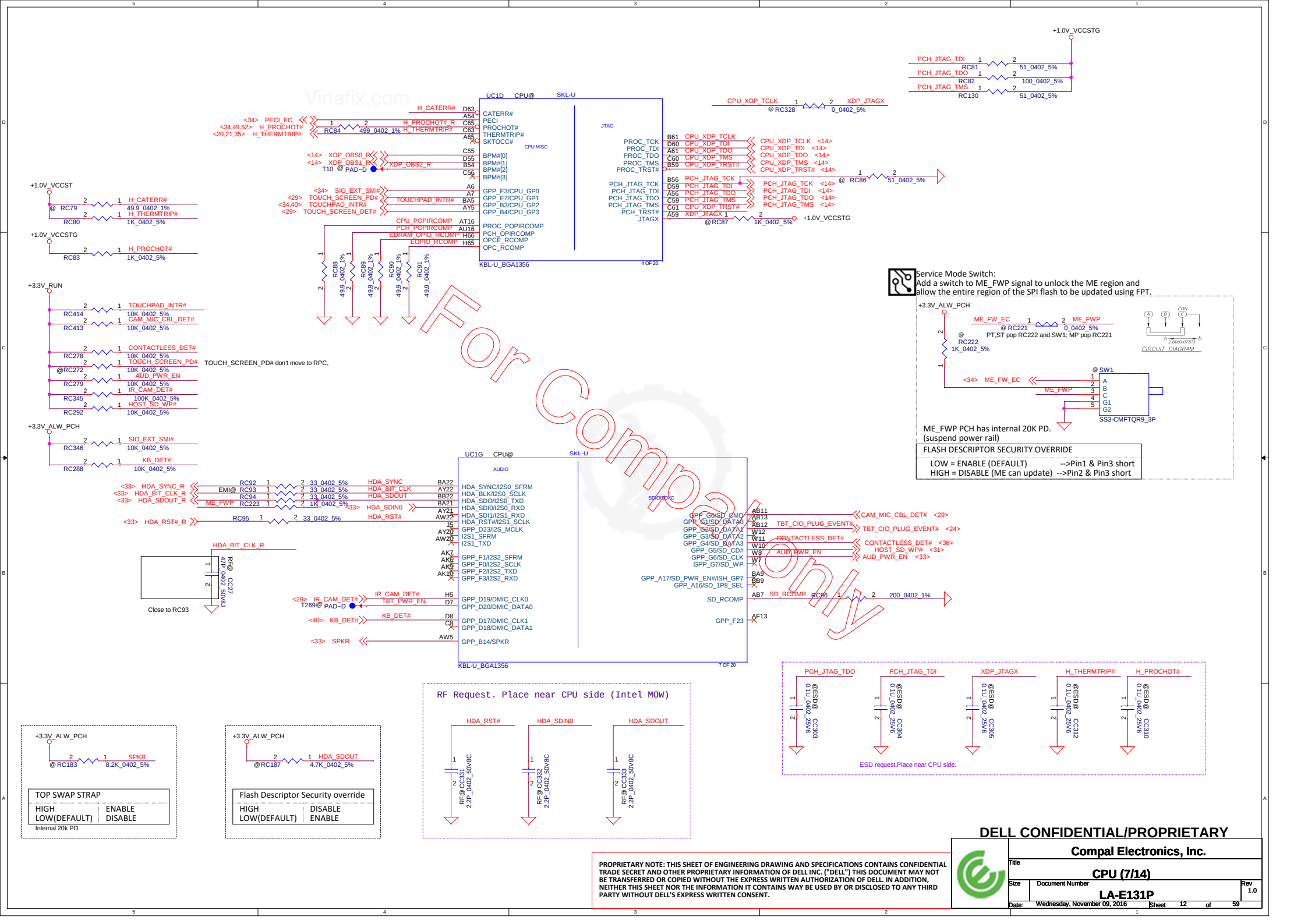
+1.0V_VCCSTG
PCH_JTAG_TDI RC81 51_0402_5%
PCH_JTAG_TDO RC82 100_0402_5%
PCH_JTAG_TMS RC130 51_0402_5%
UC1D CPU@ SKL-U
JTAG
CPU MISC
CPU_XDP_TCLK @ RC328 0_0402_5%
XDP_JTAGX
H_CATERR#
PECI
PROCHOT#
THERMTRIP#
SKTOCC#
BPM#[0]
BPM#[1]
BPM#[2]
BPM#[3]
GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3
PROC_POPIRCOMP
PCH_OPIRCOMP
OPCE_RCOMP
OPC_RCOMP
KBL-U_BGA1356
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PROC_TCK
PROC_TDI
PROC_TDO
PROC_TMS
PROC_TRST#
PCH_JTAG_TCK
PCH_JTAG_TDI
PCH_JTAG_TDO
PCH_JTAG_TMS
PCH_TRST#
JTAGX
@ RC86 51_0402_5%
@ RC87 1K_0402_5%
+1.0V_VCCSTG
+1.0V_VCCST
H_CATERR# 49.9_0402_1%
H_THERMTRIP# 1K_0402_5%
H_PROCHOT# 1K_0402_5%
+3.3V_RUN
TOUCHPAD_INTR# 10K_0402_5%
CAM_MIC_CBL_DET# 10K_0402_5%
CONTACTLESS_DET# 10K_0402_5%
TOUCH_SCREEN_PD# 10K_0402_5%
AUD_PWR_EN 10K_0402_5%
IR_CAM_DET# 100K_0402_5%
HOST_SD_WP# 10K_0402_5%
TOUCH_SCREEN_PD# don't move to RPC,
+3.3V_ALW_PCH
SIO_EXT_SMI# 10K_0402_5%
KB_DET# 10K_0402_5%
RC88 RC89 RC90 RC91 49.9_0402_1%
Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FPT.
ME_FW_EC @ RC221 0_0402_5%
PT,ST pop RC222 and SW1; MP pop RC221
RC222 1K_0402_5%
SW1 SS3-CMFTQR9_3P
ME_FWP PCH has internal 20K PD. (suspend power rail)
FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = ENABLE (DEFAULT) -->Pin1 & Pin3 short
HIGH = DISABLE (ME can update) -->Pin2 & Pin3 short
UC1G CPU@ SKL-U
AUDIO
SDIO/SDXC
HDA_SYNC/I2S0_SFRM
HDA_BIT_CLK/I2S0_SCLK
HDA_SDO/I2S0_TXD
HDA_SDI0/I2S0_RXD
HDA_SDI1/I2S1_RXD
HDA_RST#/I2S1_SCLK
GPP_D23/I2S_MCLK
I2S1_SFRM
I2S1_TXD
GPP_F1/I2S2_SFRM
GPP_F0/I2S2_SCLK
GPP_F2/I2S2_TXD
GPP_F3/I2S2_RXD
GPP_D19/DMIC_CLK0
GPP_D20/DMIC_DATA0
GPP_D17/DMIC_CLK1
GPP_D18/DMIC_DATA1
GPP_B14/SPKR
KBL-U_BGA1356
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GPP_G0/SD_CMD
GPP_G1/SD_DATA0
GPP_G2/SD_DATA1
GPP_G3/SD_DATA2
GPP_G4/SD_DATA3
GPP_G5/SD_CD#
GPP_G6/SD_CLK
GPP_G7/SD_WP
GPP_A17/SD_PWR_EN#/ISH_GP7
GPP_A16/SD_1P8_SEL
SD_RCOMP
GPP_F23
CAM_MIC_CBL_DET# <29>
TBT_CIO_PLUG_EVENT# <24>
CONTACTLESS_DET# <36>
HOST_SD_WP# <31>
AUD_PWR_EN <33>
SD_RCOMP RC96 200_0402_1%
HDA_SYNC_R RC92 33_0402_5%
HDA_BIT_CLK_R RC93 33_0402_5%
HDA_SDOUT_R RC94 33_0402_5%
ME_FWP RC223 1K_0402_5%
HDA_SDIN0
HDA_RST#_R RC95 33_0402_5%
HDA_RST#
HDA_BIT_CLK_R
RF@ CC27 47P_0402_50V8J
Close to RC93
IR_CAM_DET# T269@ PAD-D
TBT_PWR_EN
KB_DET#
SPKR
RF Request. Place near CPU side (Intel MOW)
HDA_RST# RF@ CC331 2.2P_0402_50V8C
HDA_SDIN0 RF@ CC332 2.2P_0402_50V8C
HDA_SDOUT RF@ CC333 2.2P_0402_50V8C
PCH_JTAG_TDO @ESD@ CC303 0.1U_0402_25V6
PCH_JTAG_TDI @ESD@ CC304 0.1U_0402_25V6
XDP_JTAGX @ESD@ CC305 0.1U_0402_25V6
H_THERMTRIP# @ESD@ CC312 0.1U_0402_25V6
H_PROCHOT# @ESD@ CC310 0.1U_0402_25V6
ESD request,Place near CPU side.
+3.3V_ALW_PCH
@ RC183 SPKR 8.2K_0402_5%
TOP SWAP STRAP
HIGH ENABLE
LOW(DEFAULT) DISABLE
Internal 20k PD
@ RC187 HDA_SDOUT 4.7K_0402_5%
Flash Descriptor Security override
HIGH DISABLE
LOW(DEFAULT) ENABLE
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<14> CFG[0..19]

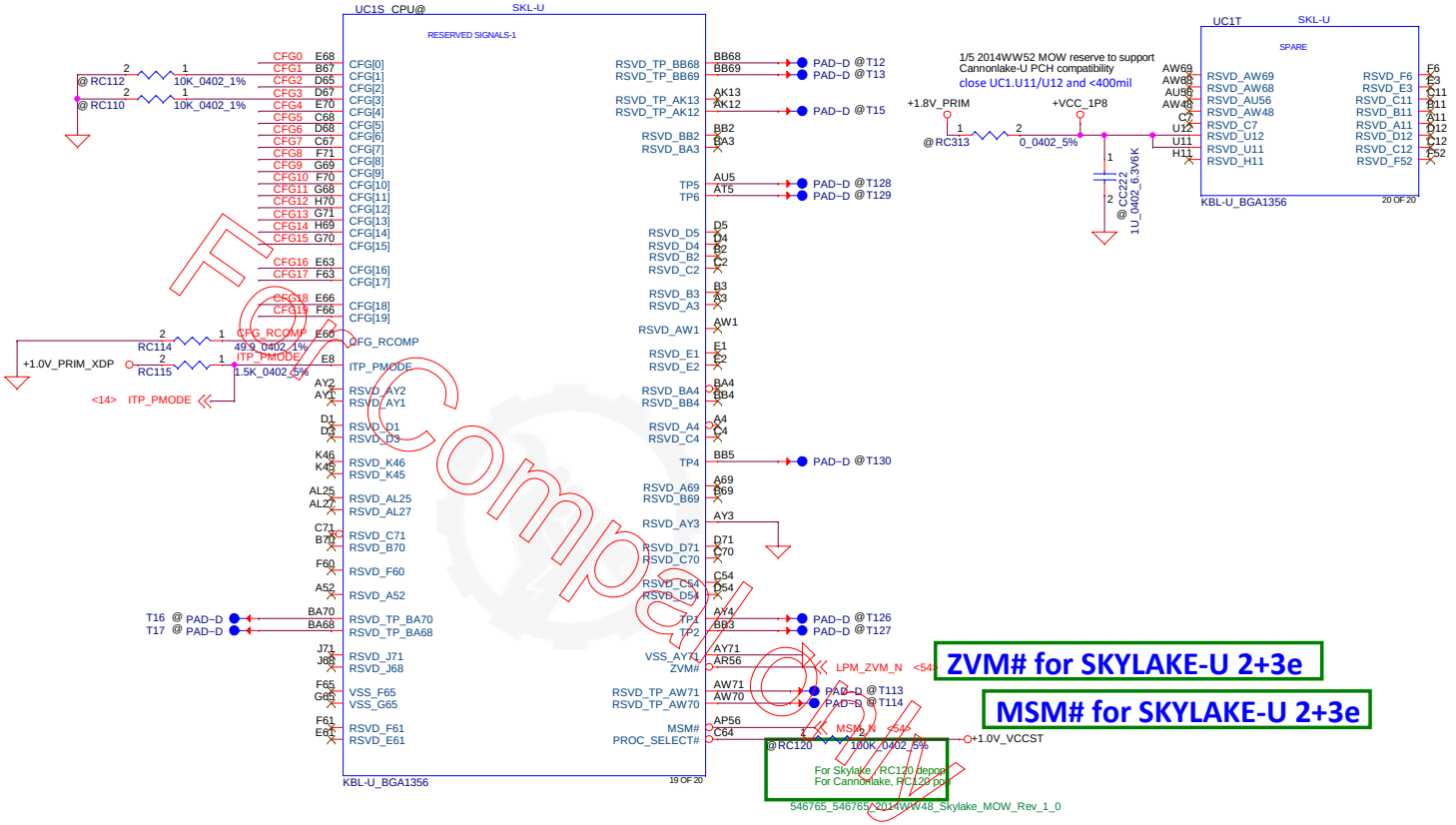
CFG[2][5][6][7] for SKYLAKE-H CPU CFG strap pin

2 1 CFG0
@ RC113 10K_0402_1%

Stall reset sequence	
HIGH(DEFAULT)	No stall(Normal Operation)
LOW	stall

2 1 CFG4
RC109 1K_0402_5%

eDP enable	
HIGH(DEFAULT)	Disabled
LOW	Enabled



ZVM# for SKYLAKE-U 2+3e

MSM# for SKYLAKE-U 2+3e

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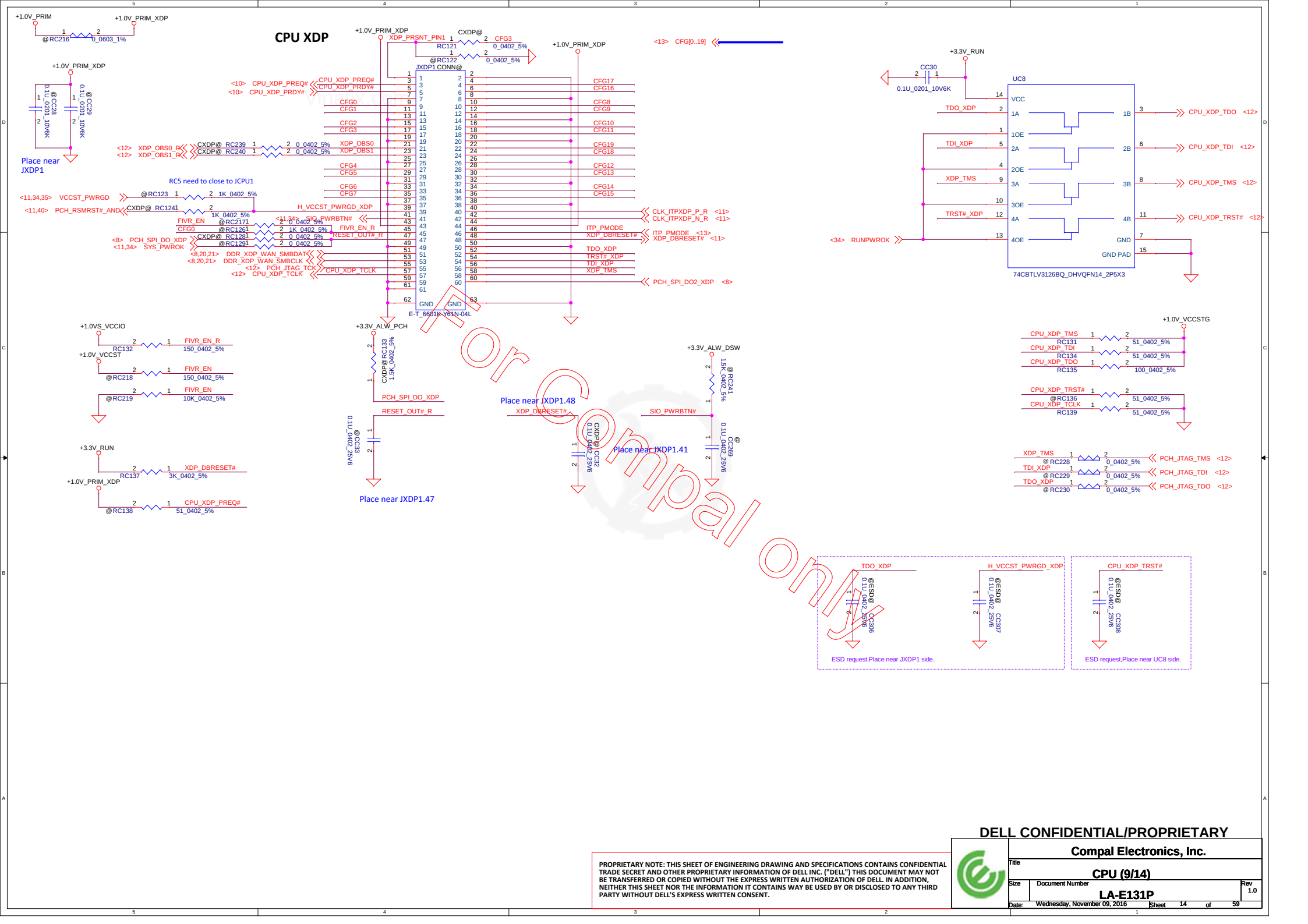

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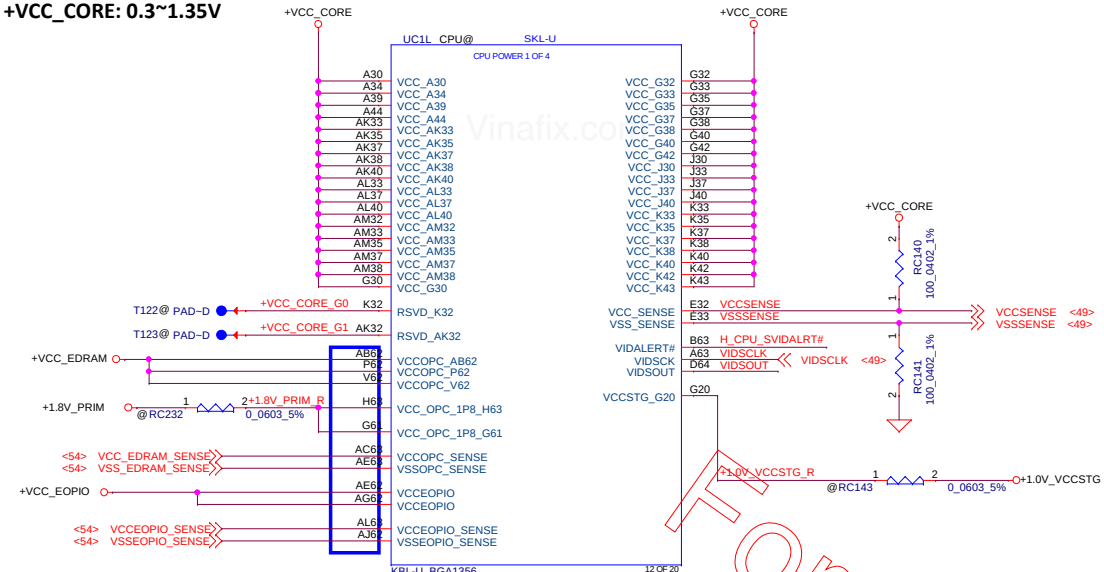
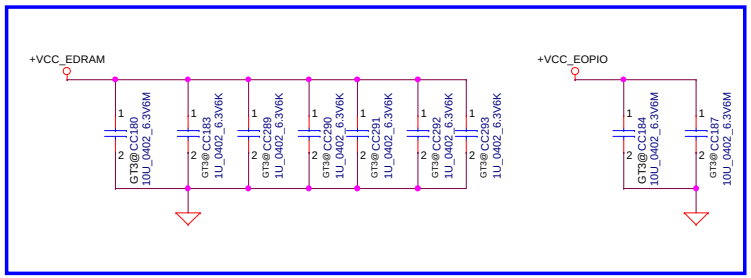
+VCC_CORE: 0.3~1.35V



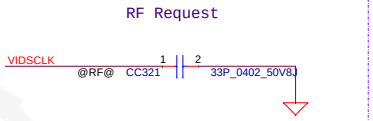
PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps >Power source

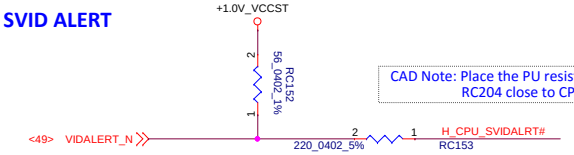
VCCOPC,VCCOPC_1P8,VCCEOPIO for SKYLAKE-U 2+3e (w/ on package cache)



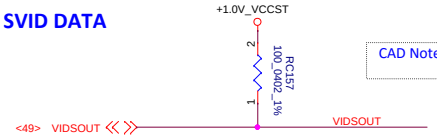
RF Request



SVID ALERT



SVID DATA



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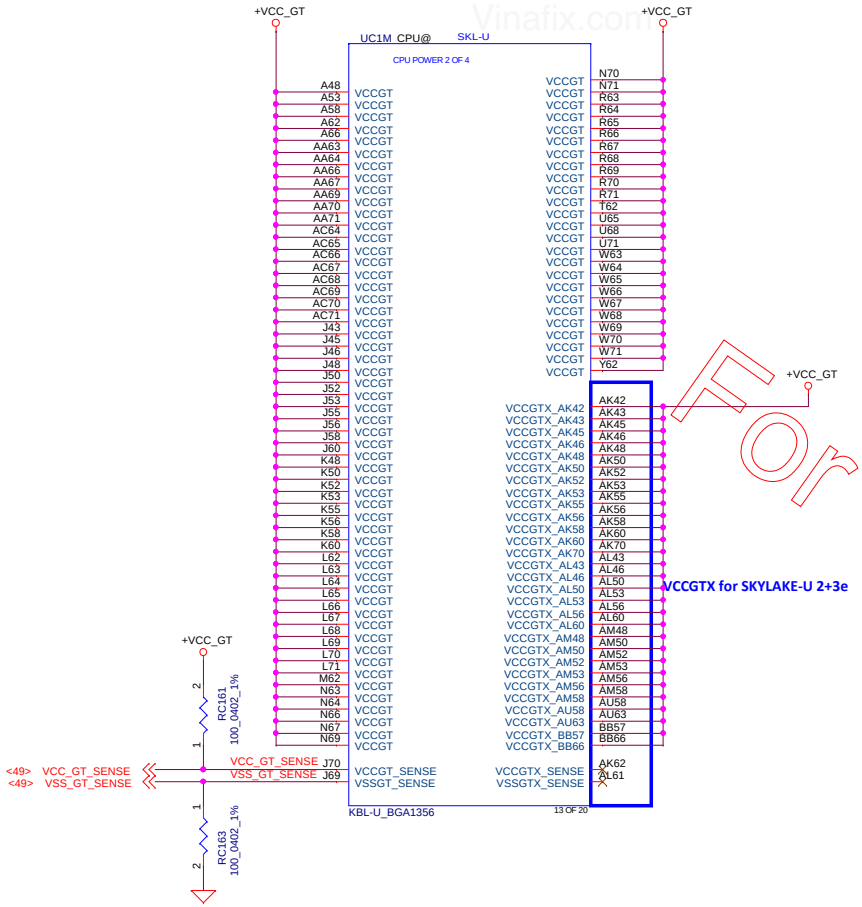
+VCCGT: 0.3~1.35V
+VCCGTX : 0.3~1.35V



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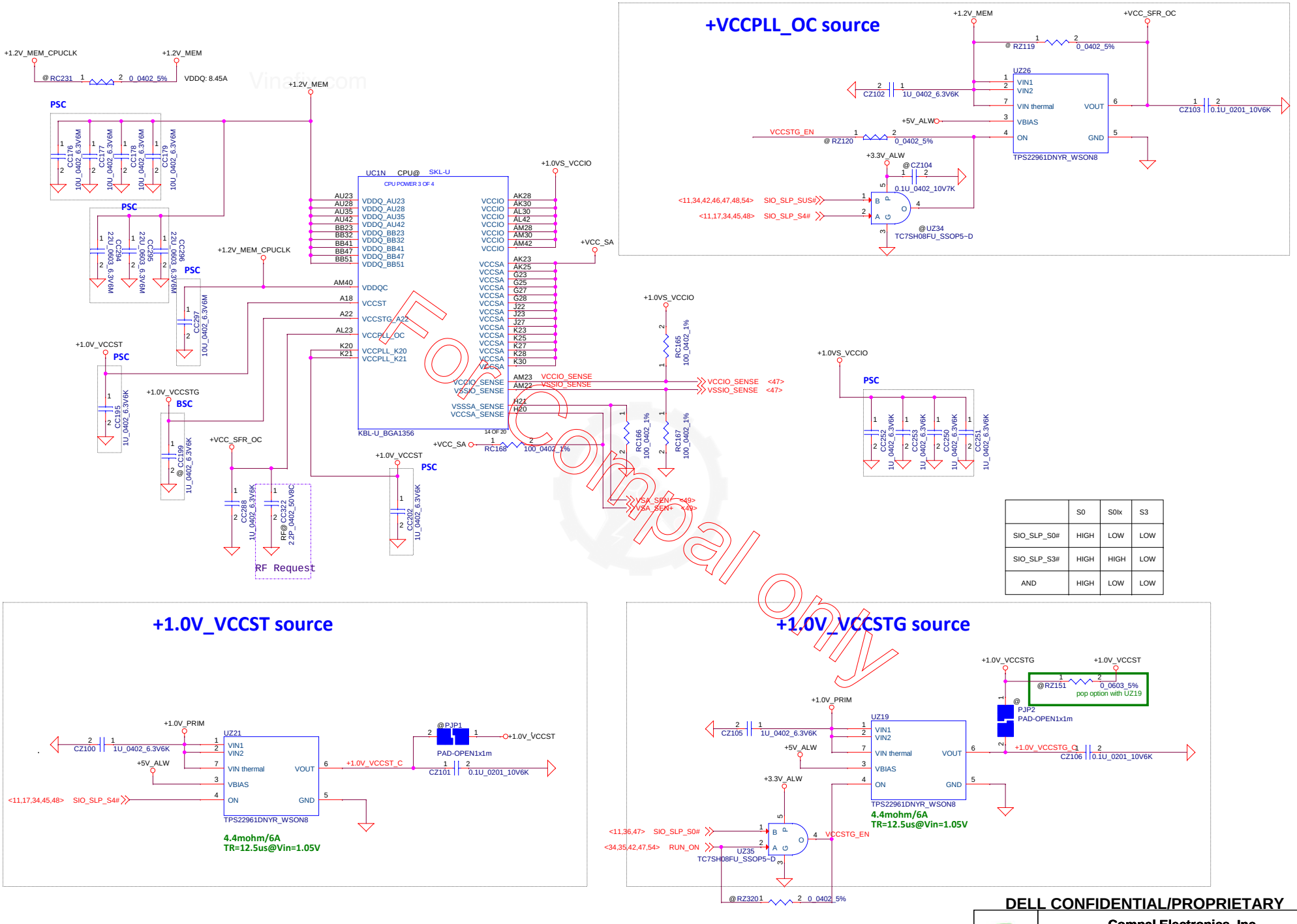
+VCCPLL_OC source
+1.2V_MEM_CPUCLK
+1.2V_MEM
VDDQ: 8.45A
@RC231
0_0402_5%
PSC
CC176 10U_0402_6.3V6M
CC177 10U_0402_6.3V6M
CC178 10U_0402_6.3V6M
CC179 10U_0402_6.3V6M
CC294 22U_0603_6.3V6M
CC295 22U_0603_6.3V6M
CC296 22U_0603_6.3V6M
CC297 10U_0402_6.3V6M
UC1N CPU@ SKL-U
CPU POWER 3 OF 4
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VDDQ_AU23
VDDQ_AU28
VDDQ_AU35
VDDQ_AU42
VDDQ_BB23
VDDQ_BB32
VDDQ_BB41
VDDQ_BB47
VDDQ_BB51
VDDQC
VCCST
VCCSTG_A22
VCCPLL_OC
VCCPLL_K20
VCCPLL_K21
VCCIO
VCCSA
VCCIO_SENSE
VSSIO_SENSE
VSSSA_SENSE
VCCSA_SENSE
+1.0VS_VCCIO
+VCC_SA
+1.0V_VCCST
+1.0V_VCCSTG
BSC
CC195 1U_0402_6.3V6K
CC199 @ 1U_0402_6.3V6K
+VCC_SFR_OC
CC288 1U_0402_6.3V6K
RF@ CC222 2.2P_0402_50V0C
CC202 1U_0402_6.3V6K
RF Request
RC168 100_0402_1%
RC165 100_0402_1%
RC166 100_0402_1%
RC167 100_0402_1%
VCCIO_SENSE <47>
VSSIO_SENSE <47>
VSA_SEN- <49>
VSA_SEN+ <49>
CC252 1U_0402_6.3V6K
CC253 1U_0402_6.3V6K
CC250 1U_0402_6.3V6K
CC251 1U_0402_6.3V6K
+1.2V_MEM
+VCC_SFR_OC
@RZ119
0_0402_5%
UZ26
VIN1
VIN2
VIN thermal
VBIAS
ON
VOUT
GND
TPS22961DNYR_WSON8
CZ102 1U_0402_6.3V6K
CZ103 0.1U_0201_10V6K
VCCSTG_EN
@RZ120
+5V_ALW
+3.3V_ALW
@CZ104
0.1U_0402_10V7K
<11,34,42,46,47,48,54> SIO_SLP_SUS#
<11,17,34,45,48> SIO_SLP_S4#
@UZ34
TC7SH08FU_SSOP5-D
SO SOIx S3
SIO_SLP_S0# HIGH LOW LOW
SIO_SLP_S3# HIGH HIGH LOW
AND HIGH LOW LOW
+1.0V_VCCST source
+1.0V_PRIM
CZ100 1U_0402_6.3V6K
UZ21
+1.0V_VCCST_C
@PJP1
PAD-OPEN1x1m
CZ101 0.1U_0201_10V6K
4.4mohm/6A
TR=12.5us@Vin=1.05V
+1.0V_VCCSTG source
@RZ151
0_0603_5%
pop option with UZ19
@PJP2
CZ105 1U_0402_6.3V6K
UZ19
+1.0V_VCCSTG_Q1
CZ106 0.1U_0201_10V6K
<11,36,47> SIO_SLP_S0#
<34,35,42,47,54> RUN_ON
UZ35
TC7SH08FU_SSOP5-D
VCCSTG_EN
@RZ320
0_0402_5%
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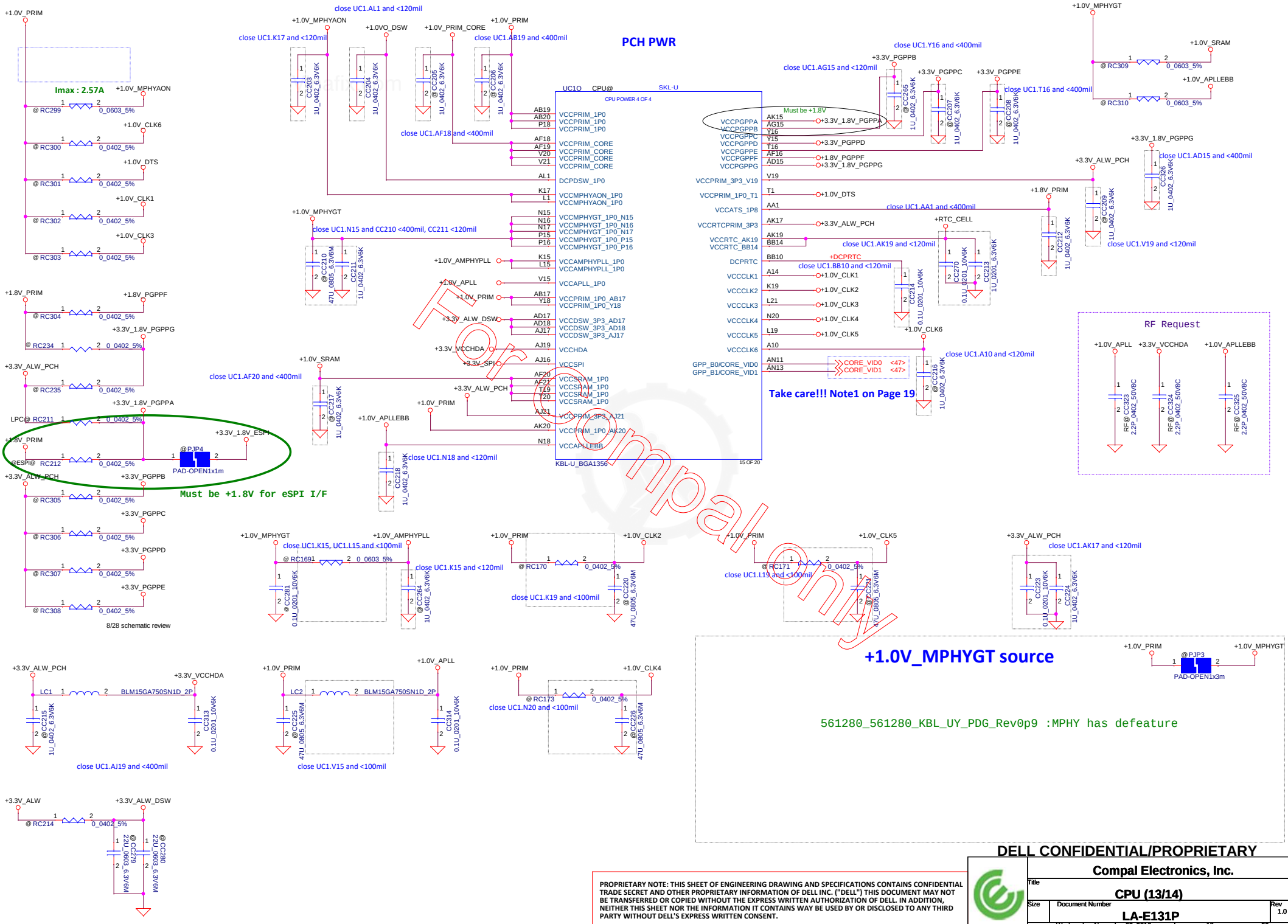
PCH PWR
Imax : 2.57A
Must be +1.8V for eSPI I/F
Take care!!! Note1 on Page 19
RF Request
+1.0V_MPHYGT source
561280_561280_KBL_UY_PDG_Rev0p9 :MPHY has defeature
8/28 schematic review
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Compal Electronics, Inc.
CPU (13/14)
LA-E131P
Wednesday, November 09, 2016
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CPU@
UC1P SKL-U

GND 1 OF 3

A5	VSS	VSS	AL65
A67	VSS	VSS	AL66
A70	VSS	VSS	AM13
AA2	VSS	VSS	AM21
AA4	VSS	VSS	AM25
AA65	VSS	VSS	AM27
AA68	VSS	VSS	AM43
AB15	VSS	VSS	AM45
AB16	VSS	VSS	AM46
AB18	VSS	VSS	AM55
AB21	VSS	VSS	AM60
AB8	VSS	VSS	AM61
AD13	VSS	VSS	AM68
AD16	VSS	VSS	AM71
AD19	VSS	VSS	AM8
AD20	VSS	VSS	AN20
AD21	VSS	VSS	AN23
AD62	VSS	VSS	AN28
AD8	VSS	VSS	AN30
AE64	VSS	VSS	AN32
AE65	VSS	VSS	AN33
AE66	VSS	VSS	AN35
AE67	VSS	VSS	AN37
AE68	VSS	VSS	AN38
AE69	VSS	VSS	AN40
AF1	VSS	VSS	AN42
AF10	VSS	VSS	AN58
AF15	VSS	VSS	AN63
AF17	VSS	VSS	AP10
AF2	VSS	VSS	AP18
AF4	VSS	VSS	AP20
AF63	VSS	VSS	AP23
AG16	VSS	VSS	AP28
AG17	VSS	VSS	AP32
AG18	VSS	VSS	AP35
AG19	VSS	VSS	AP38
AG20	VSS	VSS	AP42
AG21	VSS	VSS	AP58
AG71	VSS	VSS	AP63
AH13	VSS	VSS	AP68
AH6	VSS	VSS	AP70
AH63	VSS	VSS	AR11
AH64	VSS	VSS	AR15
AH67	VSS	VSS	AR16
AJ15	VSS	VSS	AR20
AJ18	VSS	VSS	AR23
AJ20	VSS	VSS	AR28
AJ4	VSS	VSS	AR35
AK11	VSS	VSS	AR42
AK16	VSS	VSS	AR43
AK18	VSS	VSS	AR45
AK21	VSS	VSS	AR46
AK22	VSS	VSS	AR48
AK27	VSS	VSS	AR5
AK63	VSS	VSS	AR50
AK68	VSS	VSS	AR52
AK69	VSS	VSS	AR53
AK8	VSS	VSS	AR55
AL2	VSS	VSS	AR58
AL28	VSS	VSS	AR63
AL32	VSS	VSS	AR8
AL35	VSS	VSS	AT2
AL38	VSS	VSS	AT20
AL4	VSS	VSS	AT23
AL45	VSS	VSS	AT28
AL48	VSS	VSS	AT35
AL52	VSS	VSS	AT4
AL55	VSS	VSS	AT42
AL58	VSS	VSS	AT56
AL64	VSS	VSS	AT58

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CPU@
UC1Q SKL-U

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AT63	VSS	VSS	BA49
AT68	VSS	VSS	BA53
AT71	VSS	VSS	BA57
AU10	VSS	VSS	BA6
AU15	VSS	VSS	BA62
AU20	VSS	VSS	BA66
AU32	VSS	VSS	BA71
AU38	VSS	VSS	BB18
AV1	VSS	VSS	BB26
AV68	VSS	VSS	BB30
AV69	VSS	VSS	BB34
AV70	VSS	VSS	BB38
AV71	VSS	VSS	BB43
AW10	VSS	VSS	BB55
AW12	VSS	VSS	BB6
AW14	VSS	VSS	BB60
AW16	VSS	VSS	BB64
AW18	VSS	VSS	BB67
AW21	VSS	VSS	BB70
AW23	VSS	VSS	C1
AW26	VSS	VSS	C25
AW28	VSS	VSS	C5
AW30	VSS	VSS	D10
AW32	VSS	VSS	D11
AW34	VSS	VSS	D14
AW36	VSS	VSS	D18
AW38	VSS	VSS	D22
AW41	VSS	VSS	D25
AW43	VSS	VSS	D26
AW45	VSS	VSS	D30
AW47	VSS	VSS	D34
AW49	VSS	VSS	D39
AW51	VSS	VSS	D44
AW53	VSS	VSS	D45
AW55	VSS	VSS	D47
AW57	VSS	VSS	D48
AW6	VSS	VSS	D53
AW60	VSS	VSS	D58
AW62	VSS	VSS	D6
AW64	VSS	VSS	D62
AW66	VSS	VSS	D66
AW8	VSS	VSS	D69
AY66	VSS	VSS	E11
B10	VSS	VSS	E15
B14	VSS	VSS	E18
B18	VSS	VSS	E21
B22	VSS	VSS	E46
B30	VSS	VSS	E50
B34	VSS	VSS	E53
B39	VSS	VSS	E56
B44	VSS	VSS	E6
B48	VSS	VSS	E65
B53	VSS	VSS	E71
B58	VSS	VSS	F1
B62	VSS	VSS	F13
B66	VSS	VSS	F2
B71	VSS	VSS	F22
BA1	VSS	VSS	F23
BA10	VSS	VSS	F27
BA14	VSS	VSS	F28
BA18	VSS	VSS	F32
BA2	VSS	VSS	F33
BA23	VSS	VSS	F35
BA28	VSS	VSS	F37
BA32	VSS	VSS	F38
BA36	VSS	VSS	F4
F68	VSS	VSS	F40
BA45	VSS	VSS	F42
		VSS	BA41

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CPU@
UC1R SKL-U

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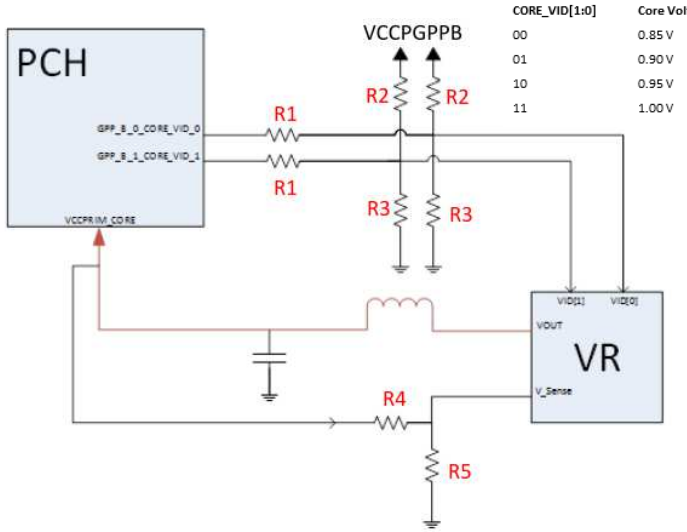
F8	VSS	VSS	L18
G10	VSS	VSS	L2
G22	VSS	VSS	L20
G43	VSS	VSS	L4
G45	VSS	VSS	L8
G48	VSS	VSS	N10
G5	VSS	VSS	N13
G52	VSS	VSS	N19
G55	VSS	VSS	N21
G58	VSS	VSS	N6
G6	VSS	VSS	N65
G60	VSS	VSS	N68
G63	VSS	VSS	P17
G66	VSS	VSS	P19
H15	VSS	VSS	P20
H18	VSS	VSS	P21
H71	VSS	VSS	R13
J11	VSS	VSS	R6
J13	VSS	VSS	T15
J25	VSS	VSS	T17
J28	VSS	VSS	T18
J32	VSS	VSS	T2
J35	VSS	VSS	T21
J38	VSS	VSS	T4
J42	VSS	VSS	U10
J8	VSS	VSS	U63
K16	VSS	VSS	U64
K18	VSS	VSS	U66
K22	VSS	VSS	U67
K61	VSS	VSS	U69
K63	VSS	VSS	U70
K64	VSS	VSS	V16
K65	VSS	VSS	V17
K66	VSS	VSS	V18
K67	VSS	VSS	W13
K68	VSS	VSS	W6
K70	VSS	VSS	W9
K71	VSS	VSS	Y17
L11	VSS	VSS	Y19
L16	VSS	VSS	Y20
L17	VSS	VSS	Y21

KBL-U_BGA1356 18 OF 20

Note1: VCCPRIM_CORE Implementation with PCH CORE_VID Recommendation

R1: PR408,PR411 ; R2: PR417,PR418 ; R3,PR419,PR420 ; R4: PR423 ; R5: PR424



CORE_VID[1:0]	Core Voltage ID
00	0.85 V
01	0.90 V
10	0.95 V
11	1.00 V

For Pre-ES Parts: Disconnect PCH CORE_VID[1:0] to the VR and fix PCH VCCPRIM_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

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Compal Electronics, Inc.

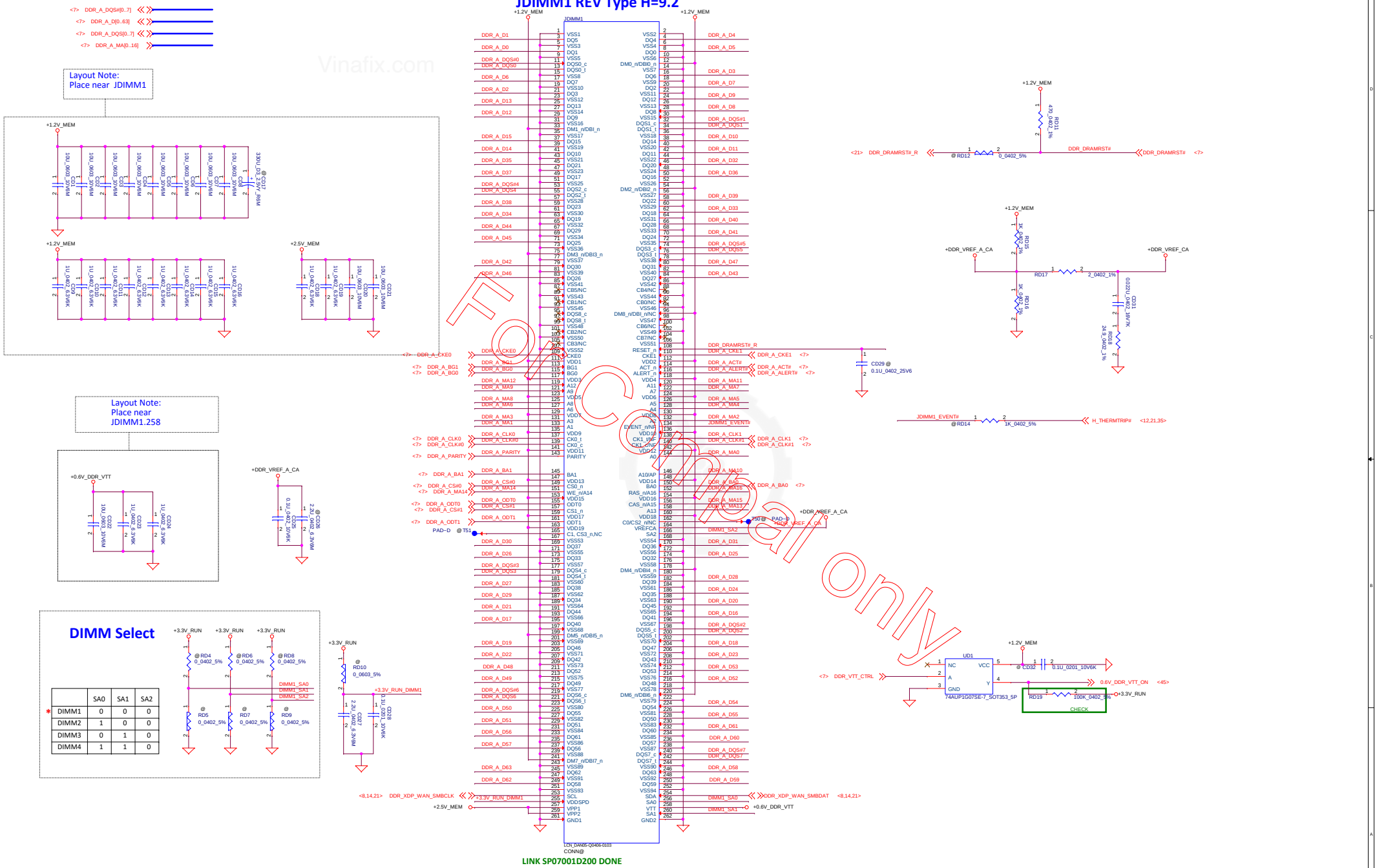
Title: CPU (14/14)

Size | Document Number: LA-E131P | Rev: 1.0

Date: Wednesday, November 09, 2016 | Sheet 19 of 59

For DDR4

JDIMM1 REV Type H=9.2



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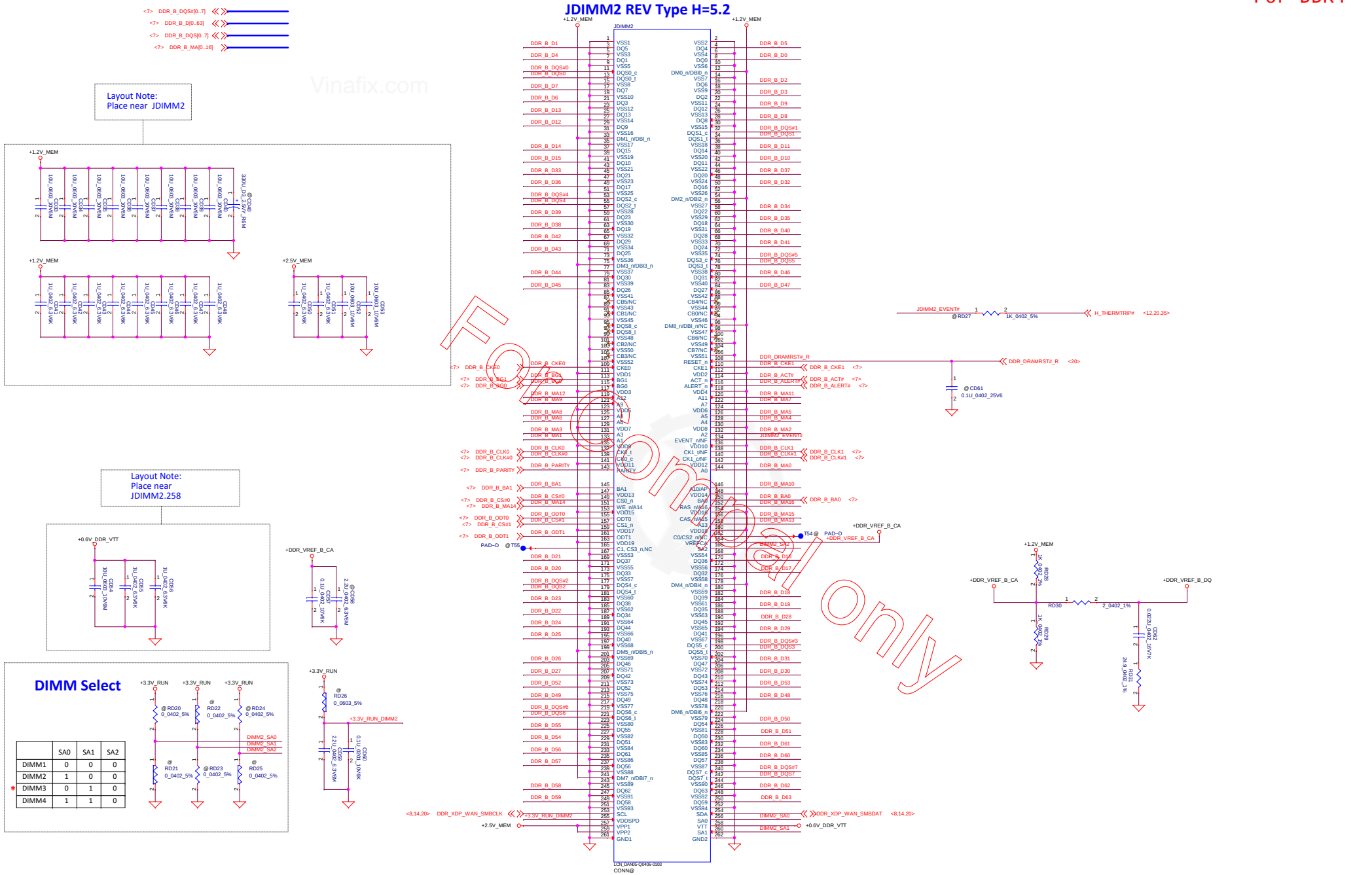
Compal Electronics, Inc.	
Title	DDR4
Size	Document Number: LA-E131P
Rev	1.0
Date:	Wednesday, November 09, 2016
Sheet	20 of 59

For DDR4

JDIMM2 REV Type H=5.2



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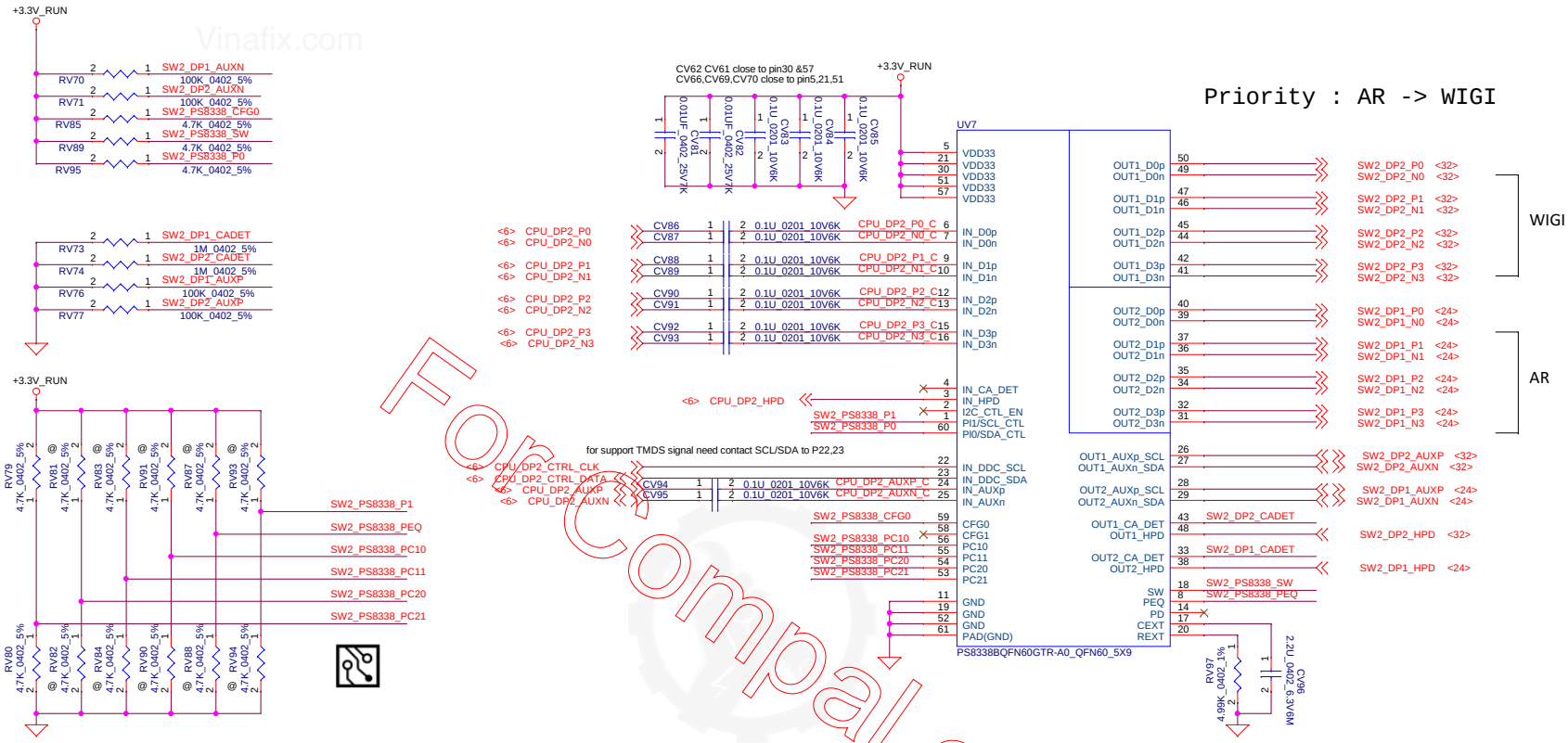
Compal Electronics, Inc.

Title: DDR4

Size: Document Number: LA-E131P Rev: 1.0

Date: Wednesday, November 09, 2016 Sheet 21 of 59



For Compal only

Port switching control or priority configuration. Internal pull down ~150KΩ,
3.3V I/O
For Control Switching Mode (CFG0 = L):
SW = L: Port1 is selected (default)
SW = H: Port2 is selected
For Automatic Switching Mode (CFG0 = H):
SW = L: Port1 has higher priority when both ports are plugged
SW = H: Port2 has higher priority when both ports are plugged (default)

vender suggest MUX use LLEQ PEQ=M and PI0=H !!

Programmable input equalization levels, Internal pull down at ~150Kohm,3.3V I/O
PEQ =
L: default,LEQ, compensate channel loss up to 11.5dB @HBR2
H: HEQ, compensate channel loss up to 14.5dB @HBR2
M:LLEQ, compensate channel loss up to 8.5dB @HBR2

PI0:Automatic EQ disable, Internal pull down ~150K ohm, 3.3V I/O
PI0 = L: Automatic EQ enable(default)
H: Automatic EQ disable

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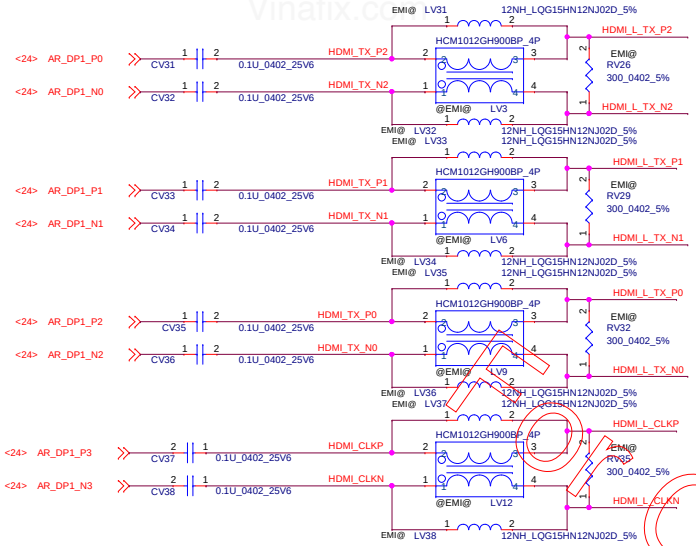
Compal Electronics, Inc.

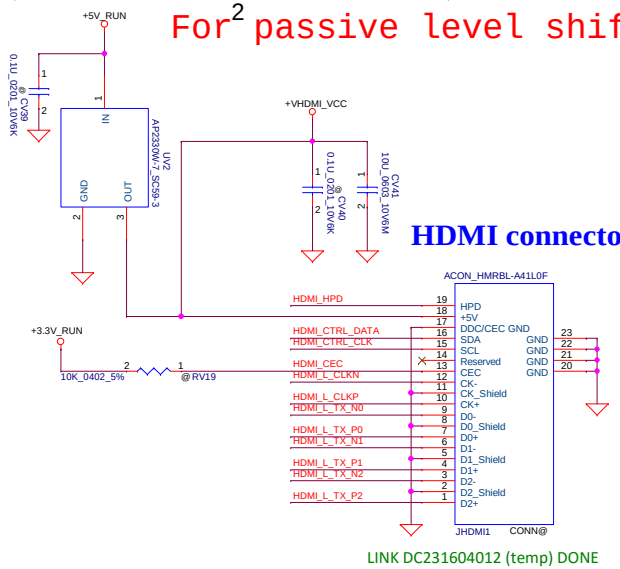
Title: DP SW2 PS8338

Size | Document Number: LA-E131P | Rev: 1.0

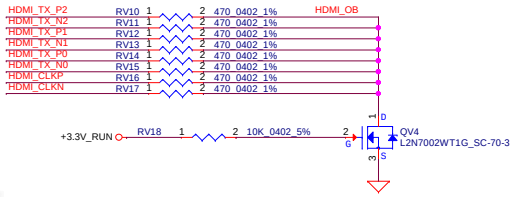
Date: Wednesday, November 09, 2016 | Sheet 22 of 59

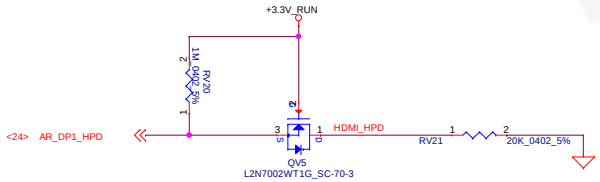
For passive level shifter from AR

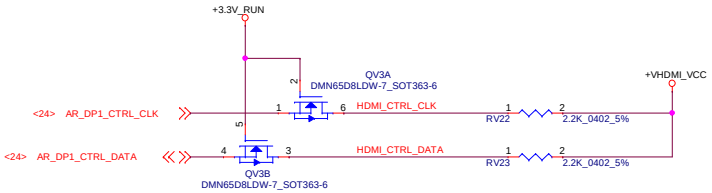




LINK DC231604012 (temp) DONE







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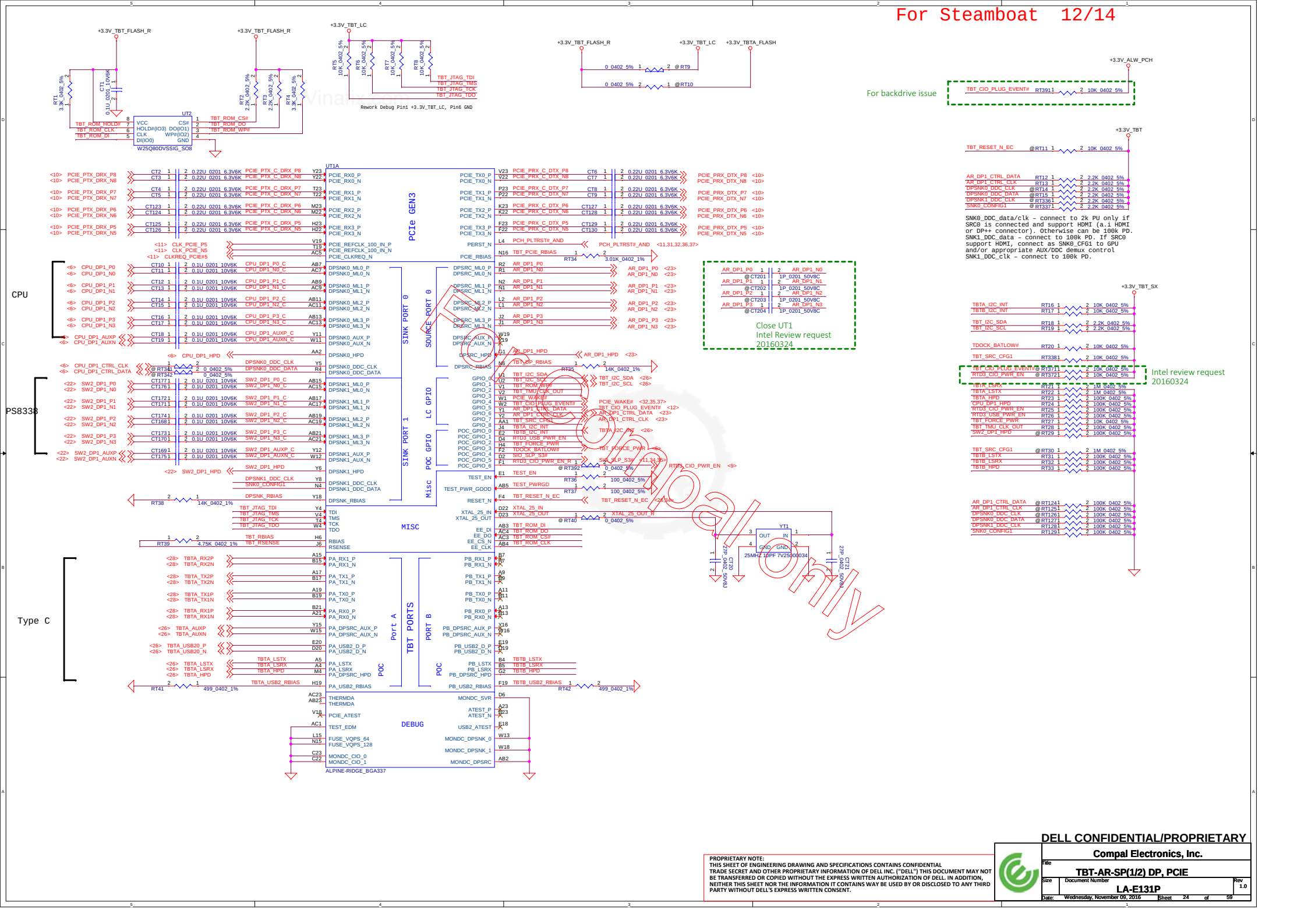
Compal Electronics, Inc.		
Title: HDMI CONN		
Size	Document Number: LA-E131P	Rev: 1.0
Date: Wednesday, November 09, 2016	Sheet 23 of 59	

For Steamboat 12/14



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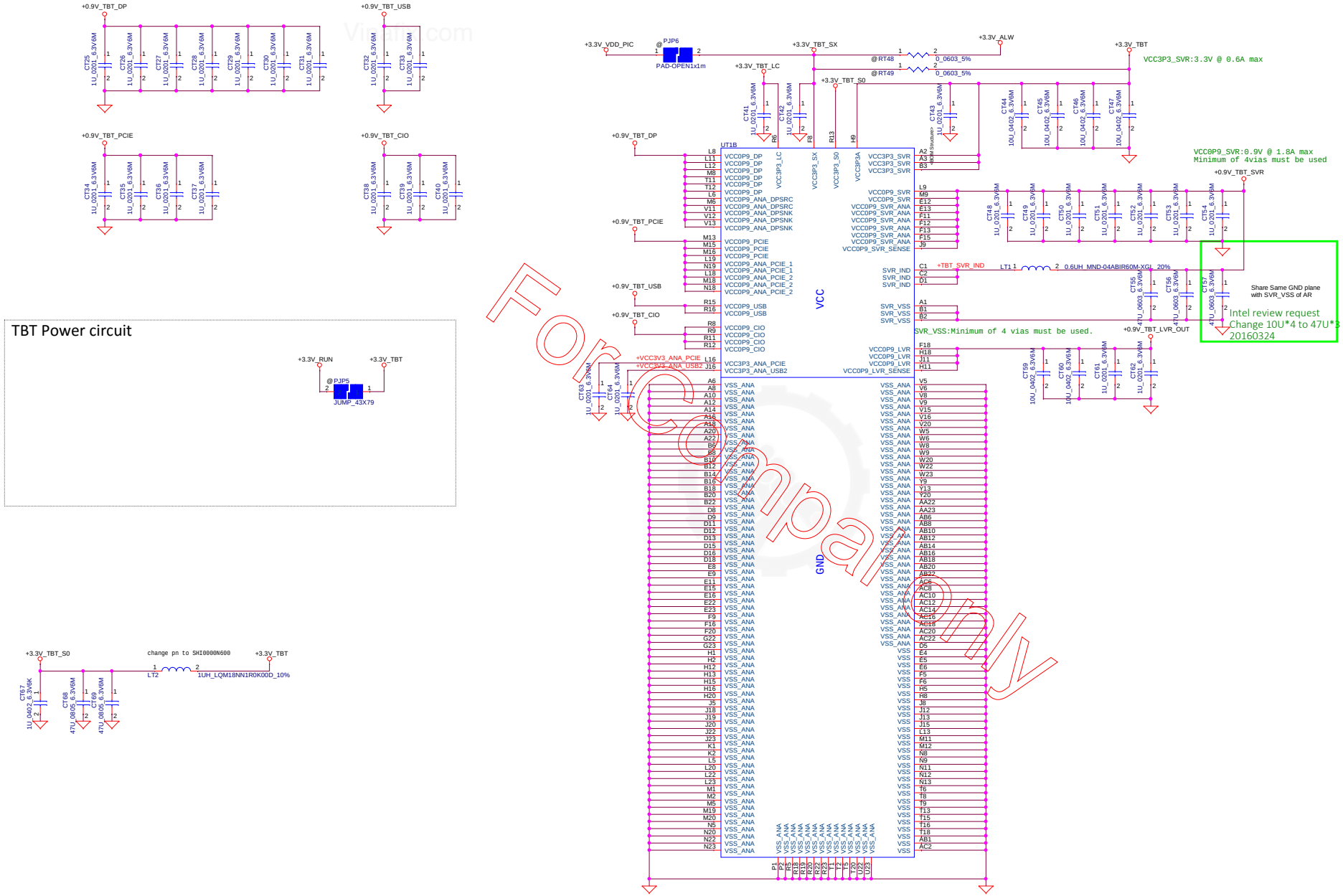
Compal Electronics, Inc.

Title: TBT-AR-SP(1/2) DP, PCIE

Size: | Document Number: LA-E131P | Rev: 1.0

Date: Wednesday, November 09, 2016 | Sheet 24 of 59



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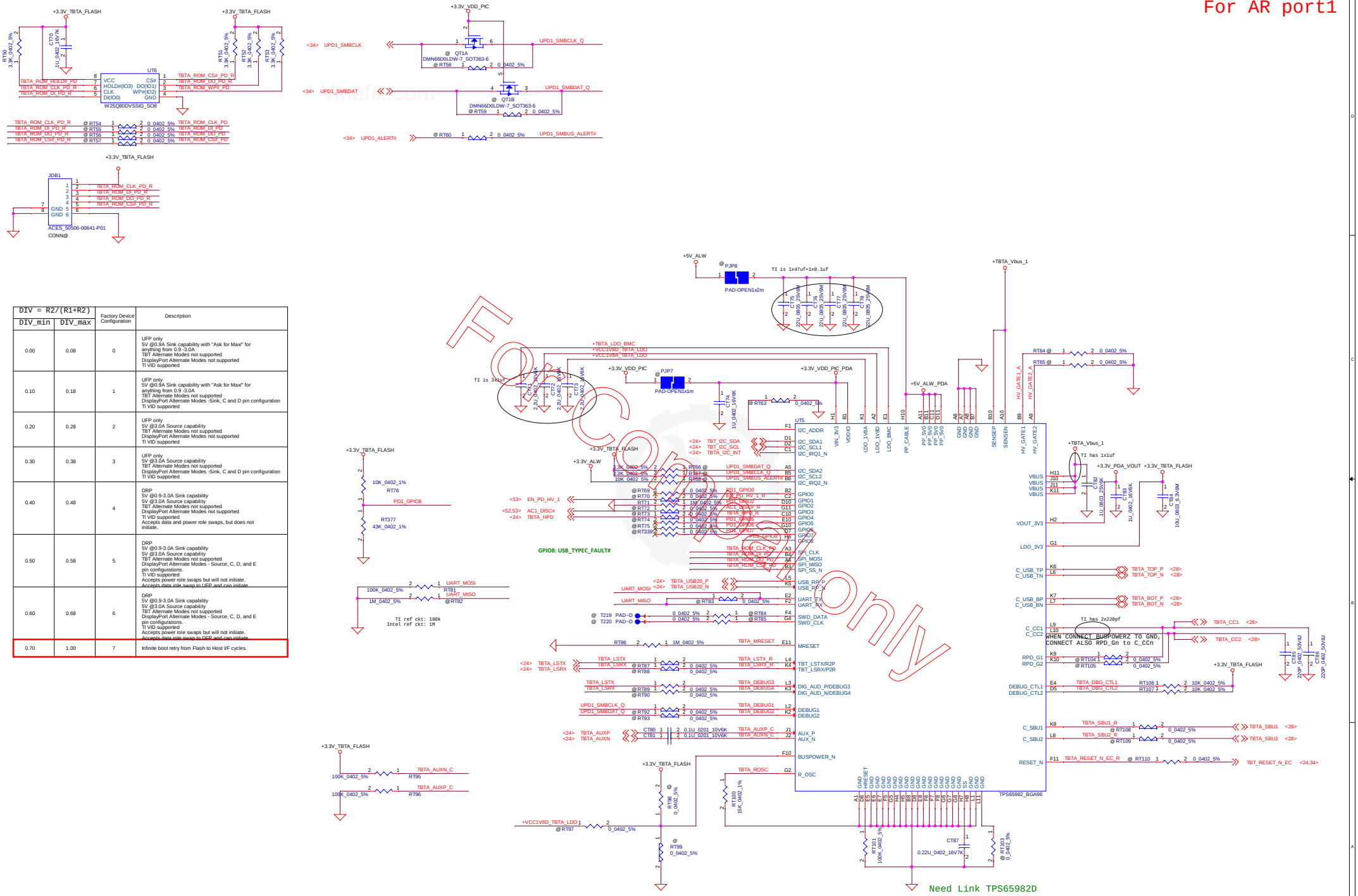
Compal Electronics, Inc.

Title	TBT-AR-SP(2/2) PWR,VSS	
Size	Document Number LA-E131P	Rev 1.0
Date: Wednesday, November 09, 2016	Sheet 25 of 59	

For AR port1



DIV = R2/(R1+R2)			
DIV_min	DIV_max	Factory Device Configuration	Description
0.00	0.08	0	UFP only 5V @0.9A Sink capability with "Ask for Max" for anything from 0.9 -3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.10	0.18	1	UFP only 5V @0.5A Sink capability with "Ask for Max" for anything from 0.9 -3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes -Sink, C and D pin configuration TI VID supported
0.20	0.28	2	UFP only 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.30	0.38	3	UFP only 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes -Sink, C and D pin configuration TI VID supported
0.40	0.48	4	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported Accepts data and power role swaps, but does not initiate.
0.50	0.58	5	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations. TI VID supported Accepts power role swaps but will not initiate. Accepts data role swap to UFP and can initiate
0.60	0.68	6	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations. TI VID supported Accepts power role swaps but will not initiate. Accepts data role swap to UFP and can initiate
0.70	1.00	7	Infinite boot retry from Flash to Host I/F cycles.

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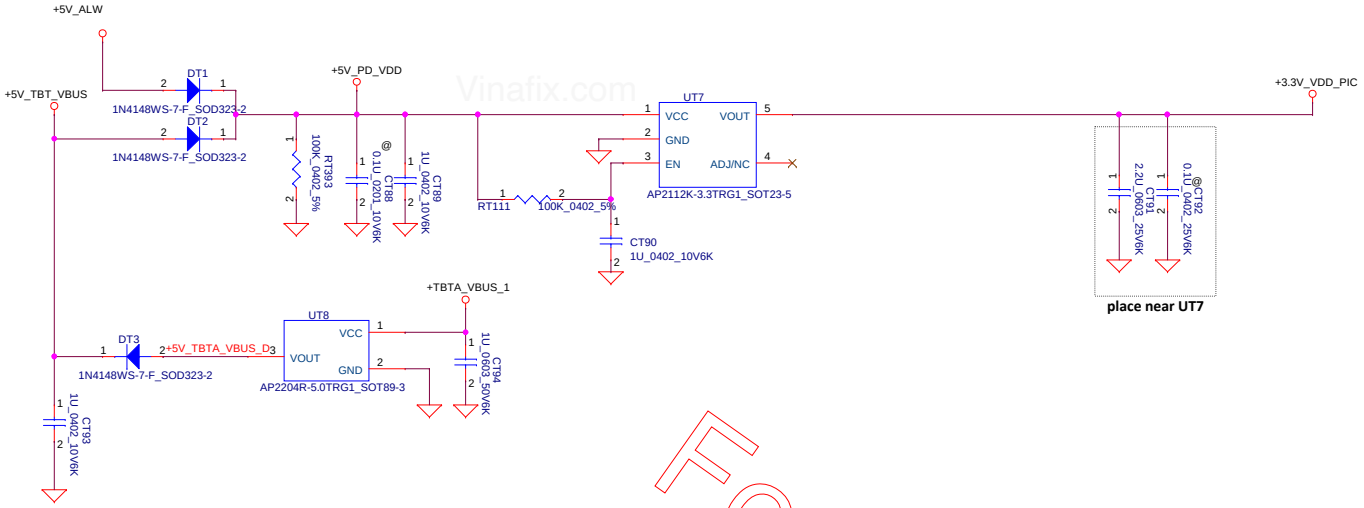
Compal Electronics, Inc.

Title: [Type C]PD Controller TI

Size: | Document Number: LA-E131P | Rev: 1.0

Date: Wednesday, November 09, 2016 | Sheet 26 of 59



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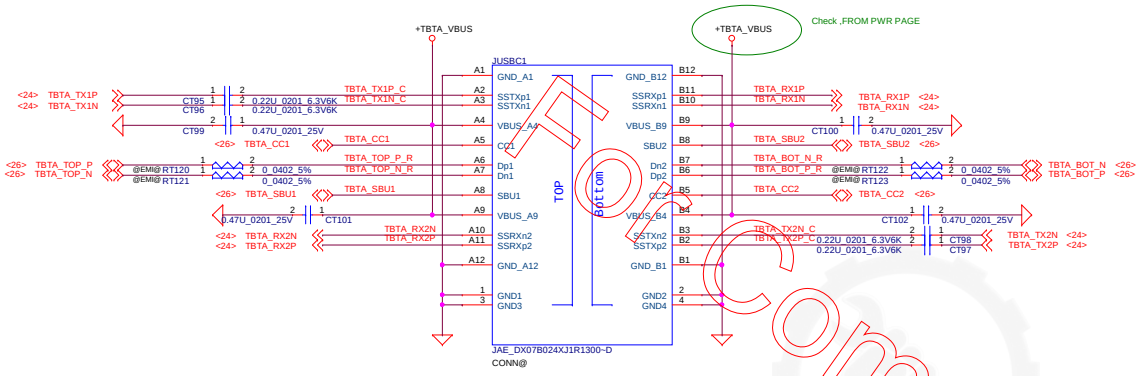
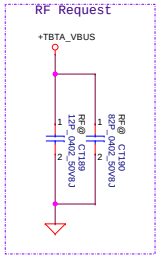
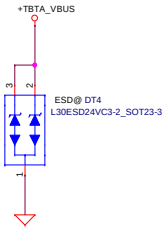
Compal Electronics, Inc.	
Title	[Type C]PD Power
Size	Document Number: LA-E131P
Rev	1.0
Date: Wednesday, November 09, 2016	Sheet 27 of 59

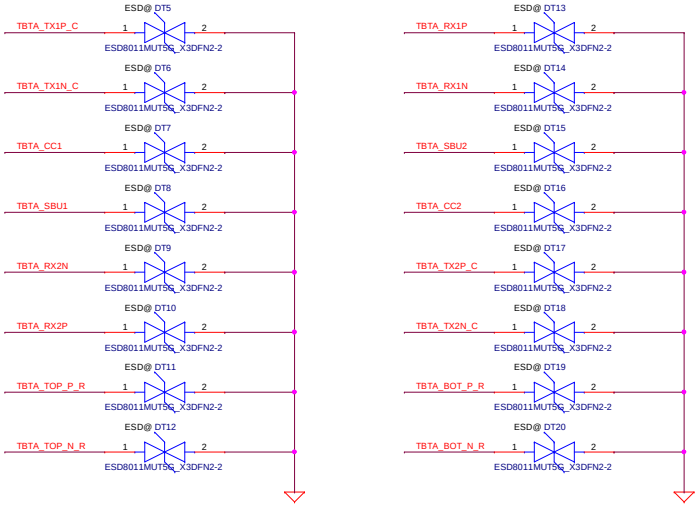
For AR Config

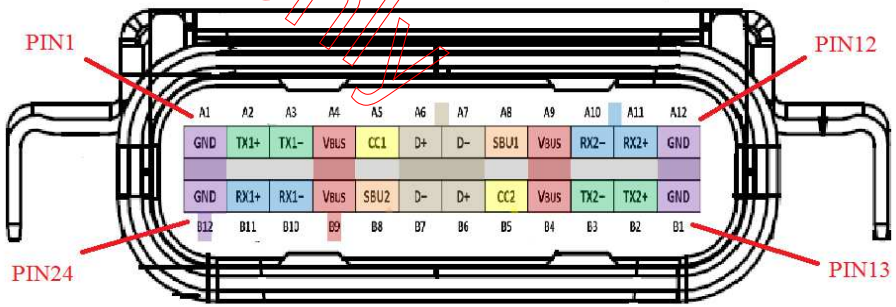






Premium 12/14/15 UMA:Check SBU1/SBU2 connect to PD or PS8740B
Link DC23300MEBL Done





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Compal Electronics, Inc.

Title: USB 3.0 CONN TYPE C

Size | Document Number: LA-E131P | Rev: 1.0

Date: Wednesday, November 09, 2016 | Sheet 28 of 59

For 4LANE EDP &5V_TSP,Steamboat14

LINK 50398-04041-001 DONE

Due to SB12/14 Mic. receive path is different between Touch and Non-Touch Panel, so add TOUCH_SCREEN_DET# pin for different verb table

Link E-T_4260K-Q06N-23L DONE

EMI Request

RF Request

ESD depop location

For Touchscreen

LCDVDD POWER

WebCAM

Backlight POWER

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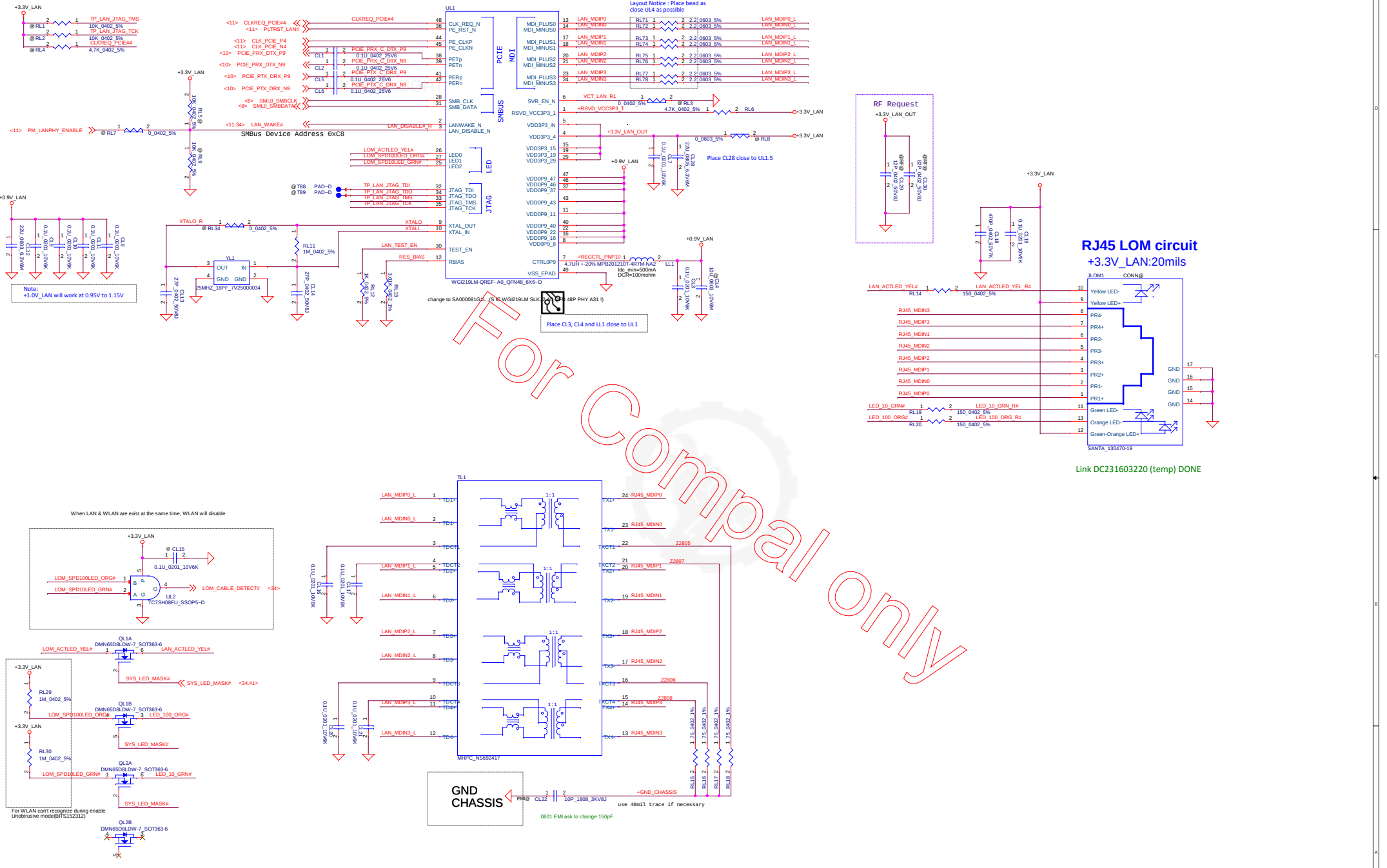
Compal Electronics, Inc.

Title: eDP CONN & Touch screen

Size: | Document Number: LA-E131P | Rev: 1.0

Date: Wednesday, November 09, 2016 | Sheet 29 of 59



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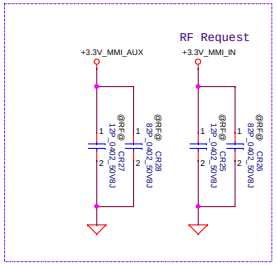
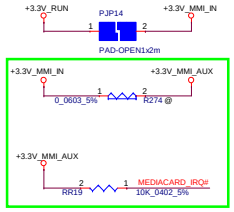
Compal Electronics, Inc.	
Title	LAN Clarkvillie & RJ45
Size	Document Number: LA-E131P
Rev	1.0
Date:	Wednesday, November 09, 2016
Sheet	30 of 59

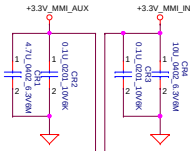
For PCIE Interface

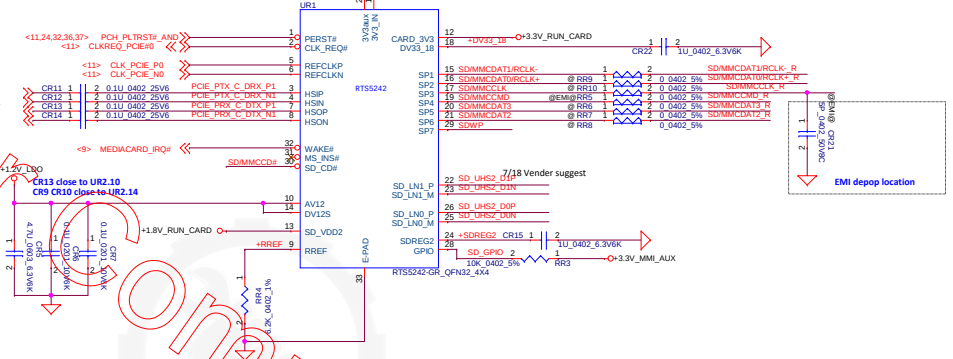




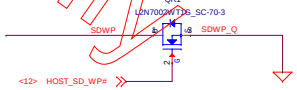
support D3 Hot(if D3 cold PIN11,PIN27 need Add MOS on/off 3V3AUX)

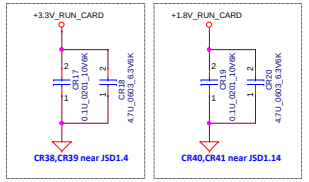
7/18 Vender suggest.

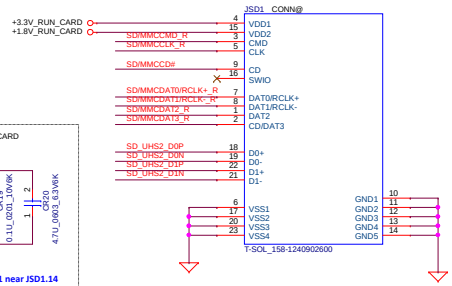




HOST_SD_WP#	SDWP_Q	SDWP	STATUS
High	Low	Low	Write Enable
Low	Low	High	Write Protect(FW LOCK)







LINK SP071603151 (temp) DONE

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Compal Electronics, Inc.

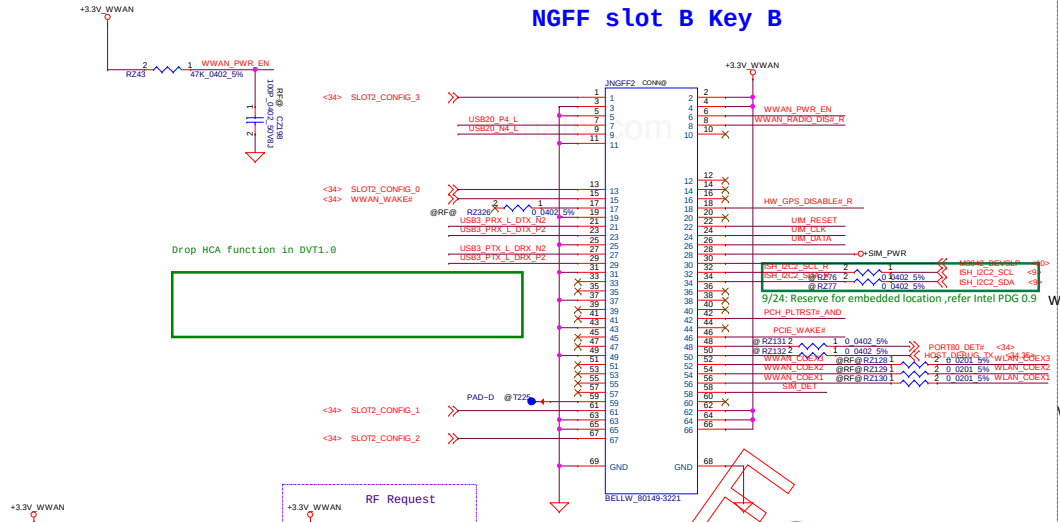
Title: Card Reader RTS5242

Size: | Document Number: LA-E131P | Rev: 1.0

Date: Wednesday, November 09, 2016 | Sheet 31 of 59

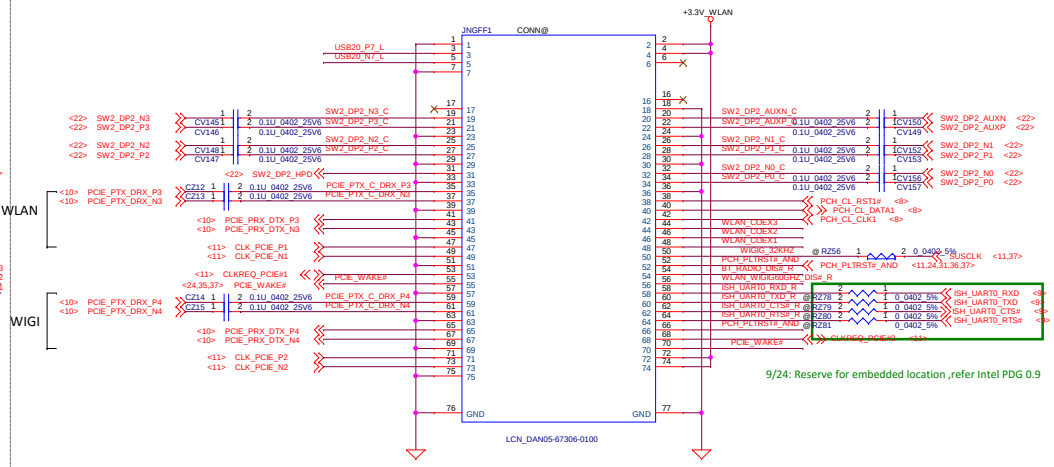
for AR Steamboat

NGFF slot B Key B

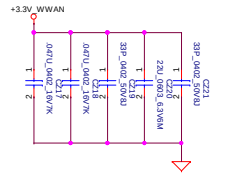


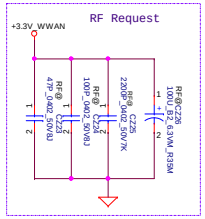
80149-3221 LINK DONE

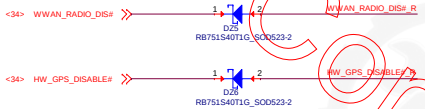
NGFF slot A Key A

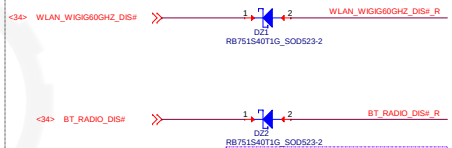


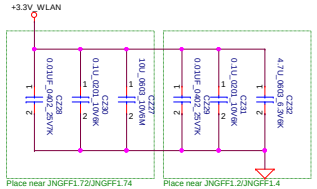
SP070019F00 LINK DONE

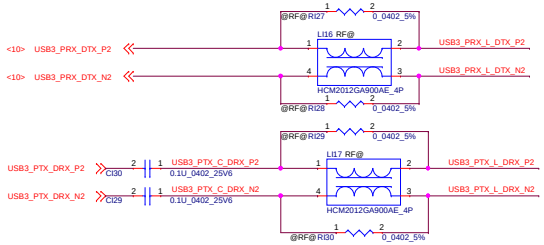


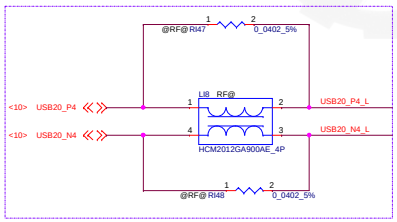


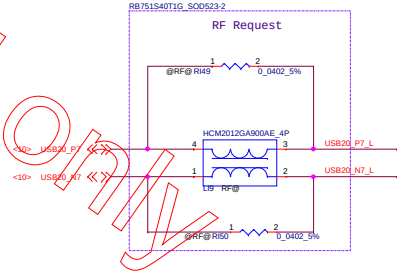


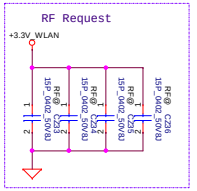




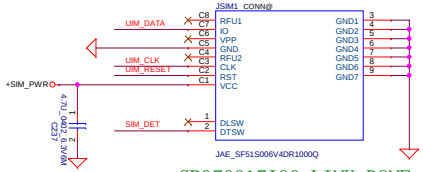






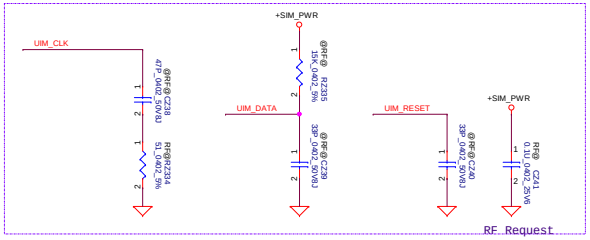


SIM Card Push-Push



SP070017I00 LINK DONE

STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
0	GND	GND	GND	GND	SSD-SATA
1	GND	HIGH	GND	GND	SSD-PCIE(2 lane)
8	HIGH	GND	GND	GND	WWAN
14	HIGH	GND	HIGH	HIGH	HCA-PCIE(1 lane)
15	HIGH	HIGH	HIGH	HIGH	NA



Power Rating TBD

PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V				

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Compal Electronics, Inc.

Title: NGFF Card

Size: | Document Number: LA-E131P | Rev: 1.0

Date: Wednesday, November 09, 2016 | Sheet 32 of 59

1W x 1ch, 4ohm (Transducer spec is 8Ohm/0.5Watt per unit, there are two transducer units in one speaker box.)

Internal Speakers Header

40 mils trace keep 20 mil spacing

ACES_50271-0040N-001

Link SP02000TS00 DONE

Close to UA1

Close to UA1 pin6

place close to UA1 pin3

Place closely to Pin 13.

Add for solve pop noise and detect issue

place at AGND and DGND plane

CLASS-D POWER DOWN CONTROL CIRCUIT

HDA_Link is 3.3V,no need level shift circuit

RE313@one control line if DVDD is 3.3V
DE2@two control lines1

Power sequence +5V_RUN_AUDIO(501us) > +3.3V_RUN_AUDIO(1204 us) > +1.5V_RUN

Reserve for support D3 cold

2.5A

500mA

EM5209VF_SON14_2X3

Place CA29 close to Codec

SLEEVE/RING2 please keep 40 mils trace width

AUD_HP_OUT_L/ AUD_HP_OUT_Rplease keep 15 mils trace width

Add this Filter to avoid other components/chips be influenced

HP-Out-Right

HP-Out-Left

Nokia-MIC

iPhone-MIC

Global Headset

Universal Jack

Normal

Open

Only BR15U UMA use LA2,LA3,because 6L

Link DC23000DG10 DONE

RF Request

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Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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Compal Electronics, Inc.	
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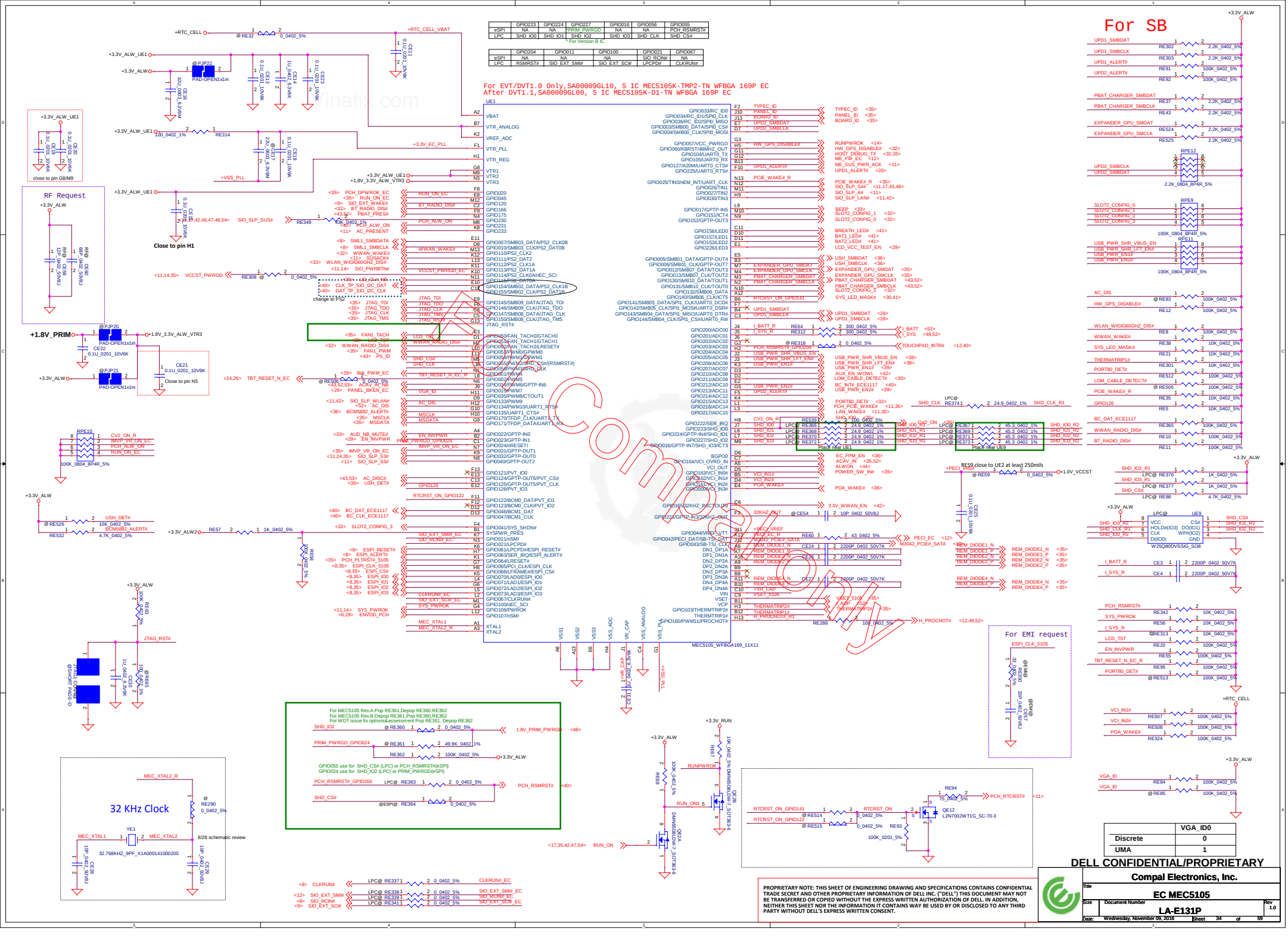
Size	C
Document Number	LA-E131P
Rev	1.0
Date:	Wednesday, November 09, 2016
Sheet	33 of 59

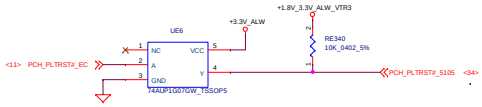


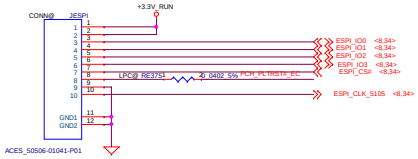
	GPIO223	GPIO224	GPIO227	GPIO016	GPIO056	GPIO055
eSPI	NA	NA	PRIM_PWRGD	NA	NA	PCH_RSMRST#
LPC	SHD_IO0	SHD_IO1	SHD_IO2	SHD_IO3	SHD_CLK	SHD_CS#

* For Version B IC

	GPIO204	GPIO011	GPIO100	GPIO021	GPIO067
eSPI	NA	NA	NA	SIO_RCIN#	NA
LPC	RSMRST#	SIO_EXT_SMI#	SIO_EXT_SCI#	LPCPD#	CLKRUN#

VGA_ID0	
Discrete	0
UMA	1

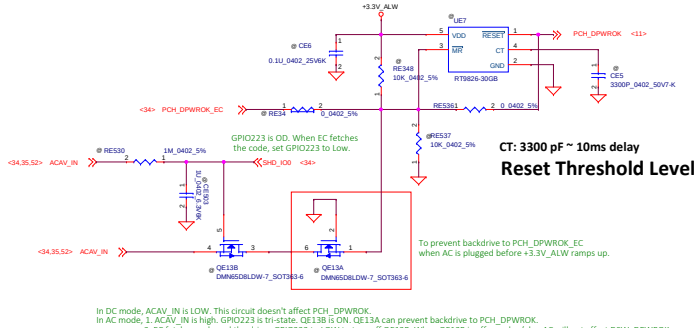




LPC 80Port Debug	LPC	ESPI
1	+3.3V_RUN	+3.3V_RUN
2	+3.3V_RUN	+3.3V_RUN
3	LPC_LAD0	ESPI_IO0
4	LPC_LAD1	ESPI_IO1
5	LPC_LAD2	ESPI_IO2
6	LPC_LAD3	ESPI_IO3
7	LPC_FRAME#	ESPI_CS#
8	PCH_PLTRST#	NA
9	GND	GND
10	LPC_CLOCK	ESPI_CLK

PAGE	ESPI	LPC
8	RC25_10K	RC8_15ohm RC13/RC27_8.2K
18	RC212_0ohm 0603	RC211_0ohm 0603
31		RE337,RE338 RE339,RE340, RE341 0_ohm
32	RE2 / RE3 0_ohm	

WDT option	
MEC5105 rev.B	Pop RE361, QE13, CE503, RE530, UE7, CE5,CE6, RE348 Depop RE362, RE536, RE537
MEC5105 rev.C	Pop RE362, RE536 Depop RE361, QE13, CE503, RE530, UE7, CE5,CE6, RE348, RE537



CT: 3300 pF ~ 10ms delay

Reset Threshold Level 3.0V

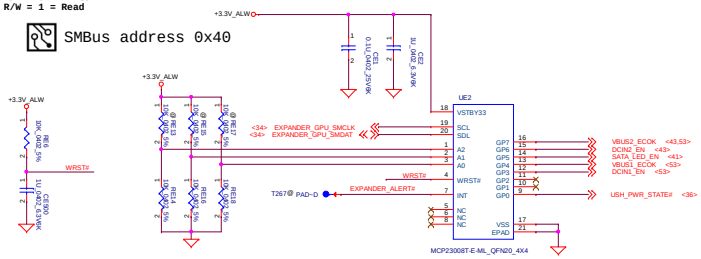
In DC mode, ACAV_IN is LOW. This circuit doesn't affect PCH_DPWROK.
In AC mode, 1. ACAV_IN is high. GPIO223 is tri-state. QE13B is ON. QE13A can prevent backdrive to PCH_DPWROK.
2. EC fetches code and the drives GPIO223 to LOW to turn off QE13B. When QE13B is off, un-plug/plug AC will not affect DSW_DPWROK.
3. When WDT occurs, GPIO223 is tri-state (EC reset). ACAV_IN charges CE503. When AC is removed, ACAV_IN goes LOW immediately. QE13B still keeps on according to RC discharging rate. PCH_DPWROK is LOW because ACAV_IN is LOW.

Control Byte

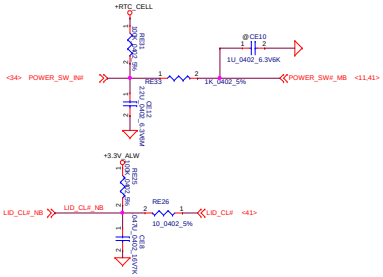
0	1	0	0	A2	A1	A0	R/W

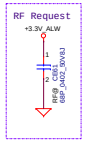
R/W = 0 = Write
R/W = 1 = Read

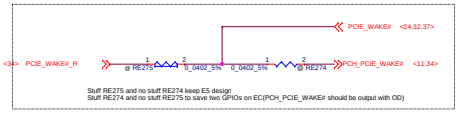
SMBus address 0x40

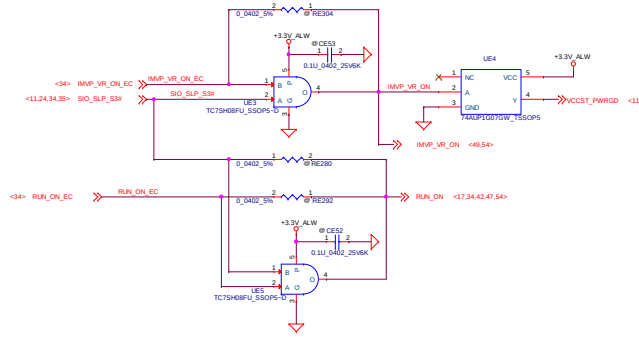


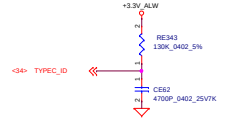
Link Microchip MCP23008 SA0000ADQ00 OK (9/6)





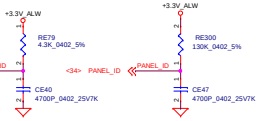






RE343	CE62	REV
240K	4700p	Single Port ACE w/o AR
130K	4700p	Single Port ACE w/AR
62K	4700p	Dual Port ACE w/o AR
33K	4700p	Dual Port ACE w/AR
8.2K	4700p	Dual Port ACE (w/AR +w/o AR)
4.3K	4700p	.
2K	4700p	
1K	4700p	

PD_ACE_DET# rise time is measured from 5%~68%.

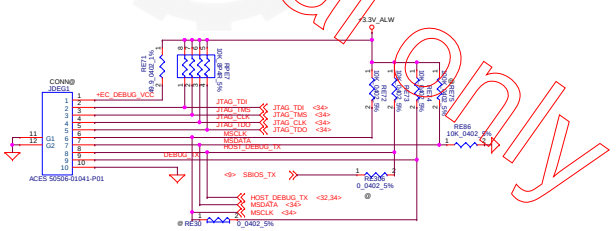


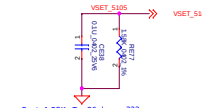
RE79	CE40	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	X04
4.3K	4700p	A00
2K	4700p	
1K	4700p	

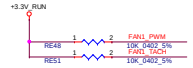
BOARD_ID rise time is measured from 5%~68%.

RE300	CE47	PANEL SIZE
240K	4700p	12"
130K	4700p	14"
33K	4700p	15"
4.3K	4700p	17"

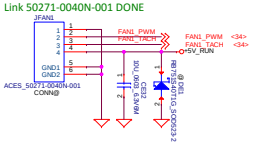
PANEL_ID rise time is measured from 5%~68%.







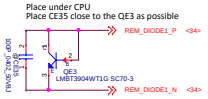
Link 50271-0040N-001 DONE



Thermal diode mapping

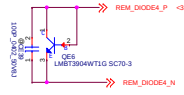
5105 Channel	Location
DP1/DN1	CPU (QE3)
DP2/DN2	WiGig (QE5)
DN2a/DP2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)

Place under CPU
Place CE35 close to the QE3 as possible

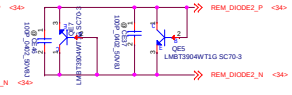


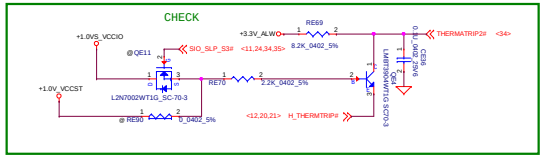
DP2/DN2 for WiGig on QE5, place QE5 close to WiGig and CE37 close to QE5

DP4/DN4 for Skin on QE6, place QE6 close to Vcore VR choke.



DN2a/DP2a for DDR on QE7, place QE7 close to DDR and CE46 close to QE7





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Title	MEC5105 support	
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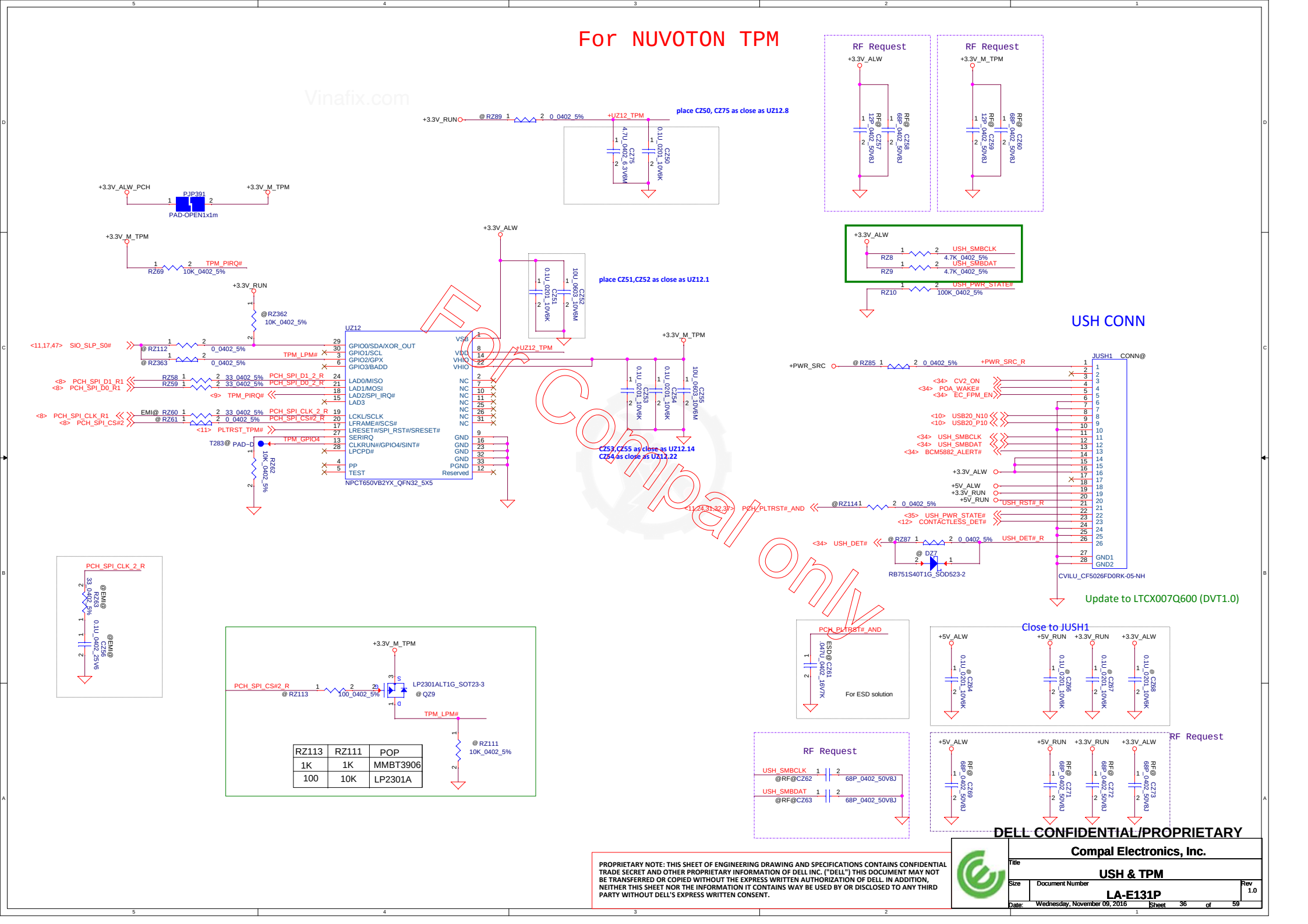

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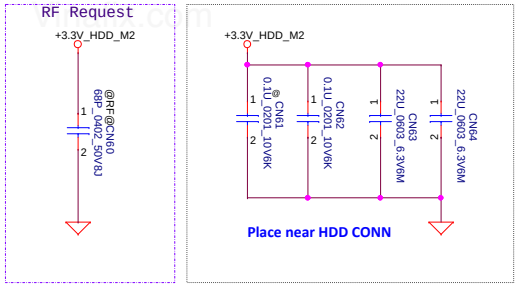
Title: USH & TPM

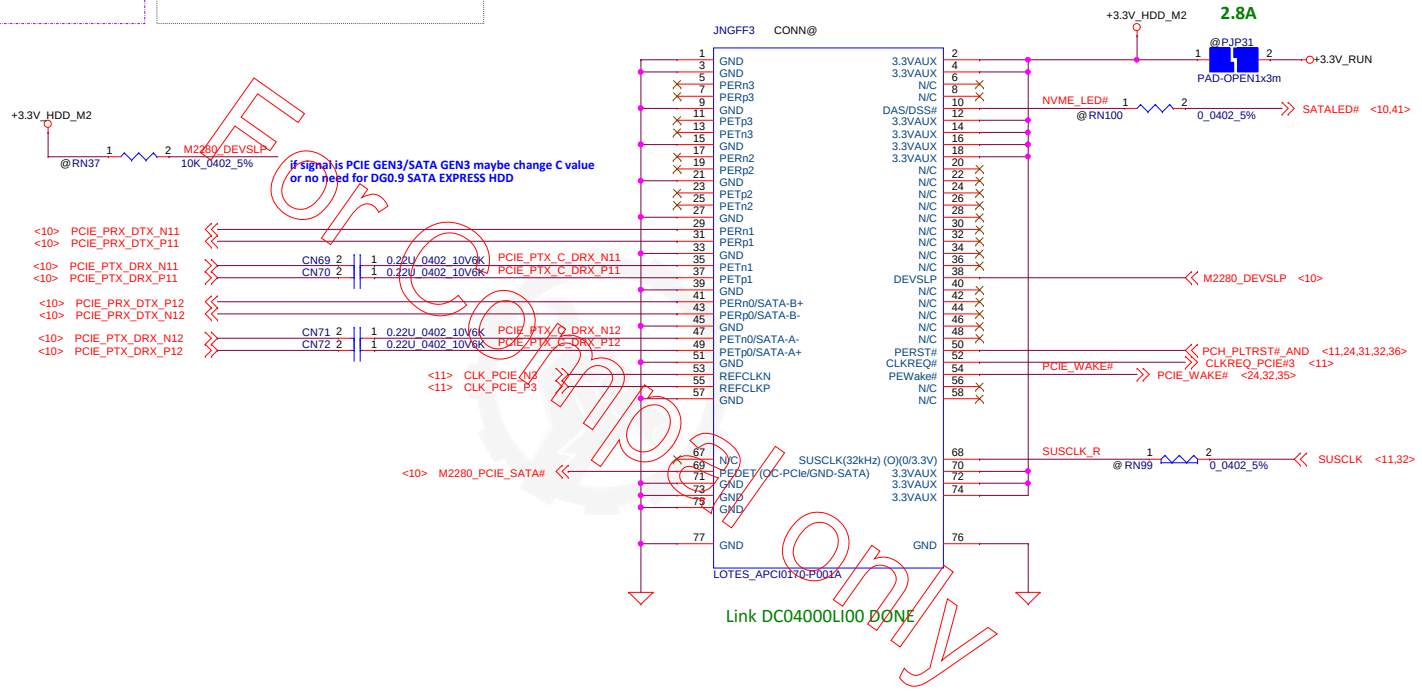
Size | Document Number: LA-E131P | Rev: 1.0

Date: Wednesday, November 09, 2016 | Sheet 36 of 59



2280 SSD

NGFF slot C Key M



Link DC04000LI00 DONE

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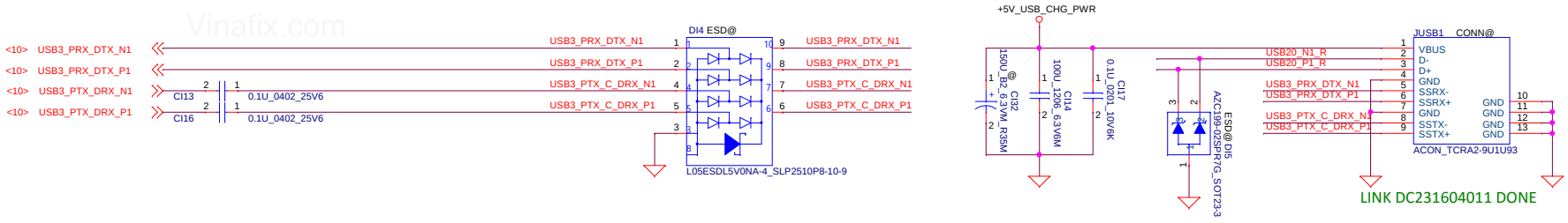
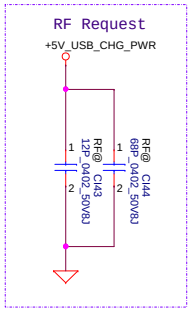
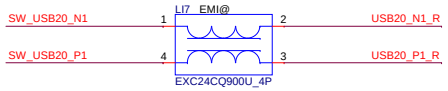
Title: M2 2280 Socket

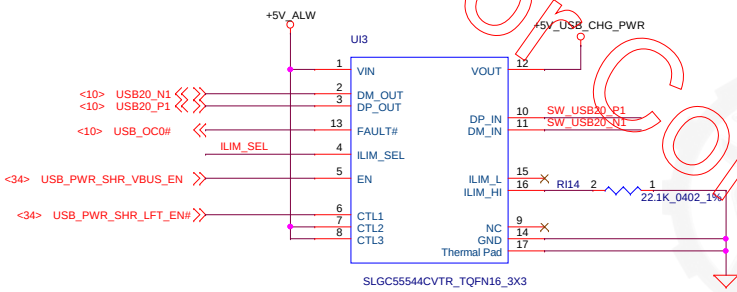
Size | Document Number: LA-E131P | Rev: 1.0

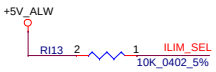
Date: Wednesday, November 09, 2016 | Sheet 37 of 59

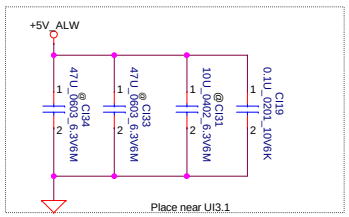












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Compal Electronics, Inc.

Title: JUSB1+PS

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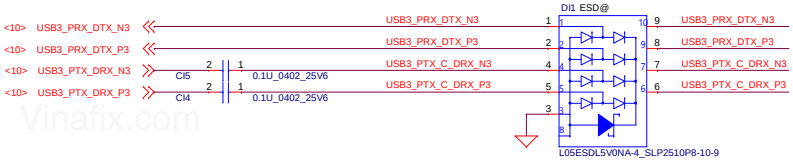
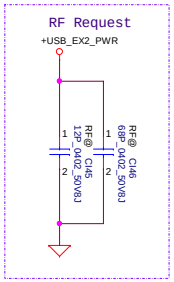
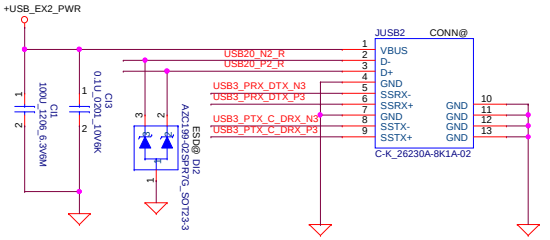
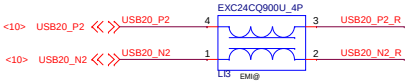
For Breckenridge 14&15/Steamboat 14



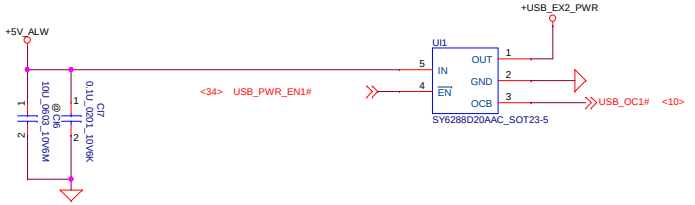




Link DC231604112(Temp) DONE

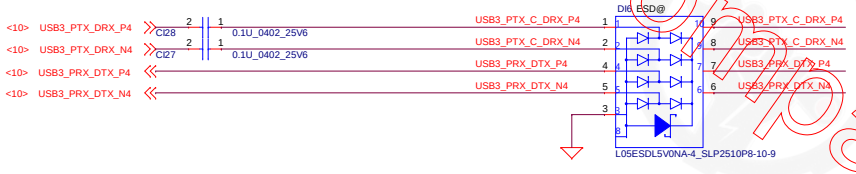


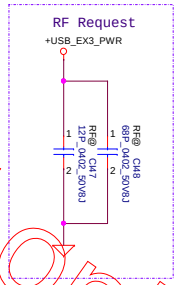
DFB request:
main SM070003Z00 (INPAQ_MCM1012B900F06BP_4P)
Footprint use 2nd source SM070004400 (PANAS_EXC24CQ900U_4P)
Pitch change from 0.5mm to 0.55mm

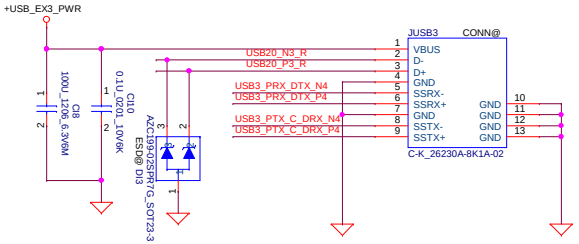


For Compal only

12" not support







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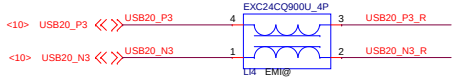

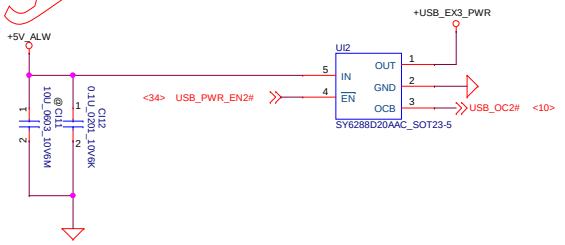

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Title: JUSB2&JUSB3

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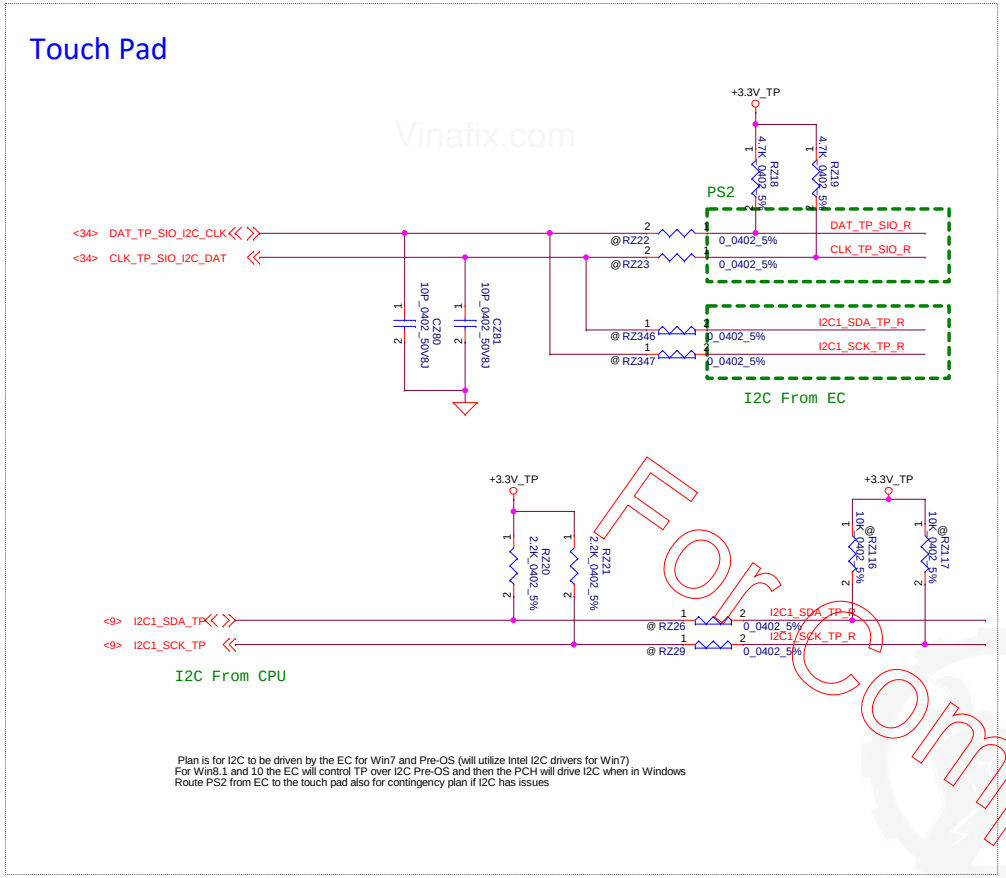
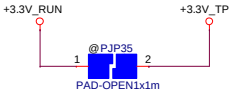
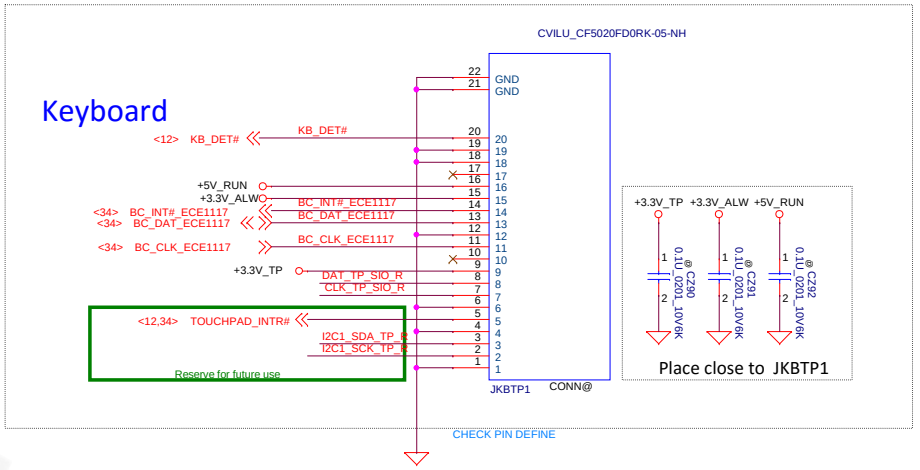
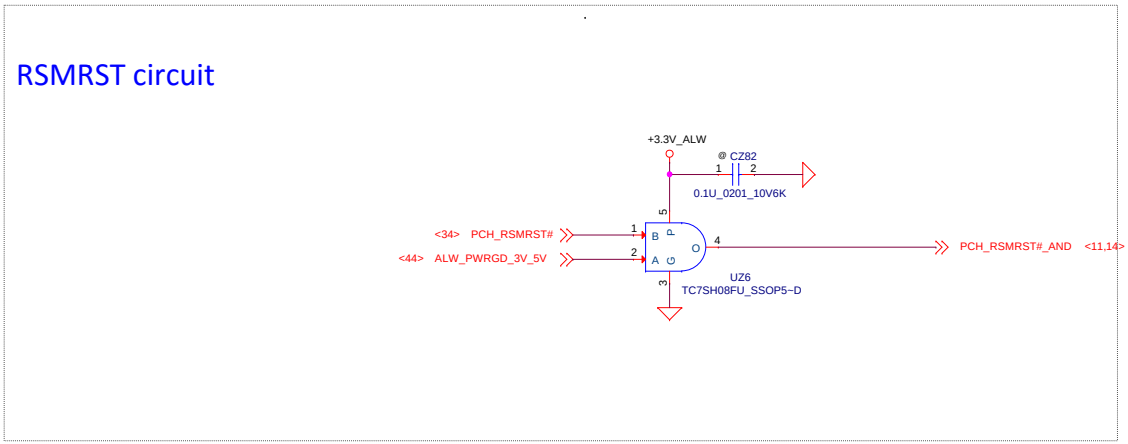
Date: Wednesday, November 09, 2016 | Sheet 39 of 59









@EDP Cable nonTS_HD-HD Cam

Part Number	Description
DC02C00DX00	H-CONN SET 1S1 MB-LCD-CAM HD NTS

@EDP Cable nonTS_FHD-HD Cam

Part Number	Description
DC02C00DW00	H-CONN SET 1S1 MB-LCD-CAM FHD NTS

@EDP Cable nonTS_FHD-IR

Part Number	Description
DC02C00DY00	H-CONN SET 1S1 MB-LCD-CAM FHD IR NTS

@EDP Cable TS_FHD-HD Cam

Part Number	Description
DC02C00E300	H-CONN SET 1S1 MB-LCD-CAM FHD TS

@EDP Cable infinity nonTS_FHD-3mm RGB

Part Number	Description
DC02C00DZ00	H-CONN SET 1S1 MB-LCD-CAM FHD INF NTS

@EDP Cable infinity TS_FHD-3mm RGB

Part Number	Description
DC02C00E400	H-CONN SET 1S1 MB-LCD-CAM FHD INF TS

@EDP Cable infinity TS_QHD-3mm RGB

Part Number	Description
DC02C00E500	H-CONN SET 1S1 MB-LCD-CAM QHD INF TS

@LED Cable

Part Number	Description
DC02002LY00	H-CONN SET 1S1 MB-LED/B

@FP FFC

Part Number	Description
NBX00023800	FFC 12P F P=0.5 PAD=0.3 66MM FP-USH 1S1

@TP FFC

Part Number	Description
NBX00023900	FFC 20P F P=0.5 PAD=0.3 118MM MB-TP 1S1

@USH Board FFC

Part Number	Description
NBX00023A00	FFC 26P F P=0.5 PAD=0.3 50MM MB-USH 1S1

@RTC BATT

Part Number	Description
GC02001DS00	BATT CR2032 3V 225MAH PA 5 W/C 30MM

@FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

@Speak

Part Number	Description
PK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

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Compal Electronics, Inc.

Title: Keyboard

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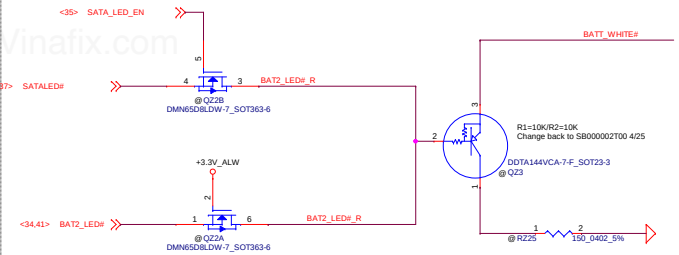
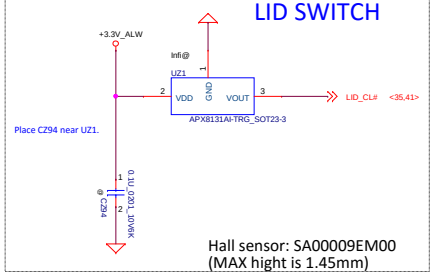
HDD LED MUX

means EC can switch battery white led and HDD LED by hot key "Fn+H"

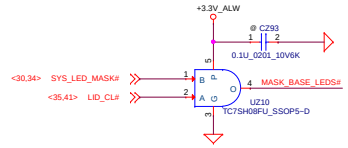


Battery LED

LID SWITCH

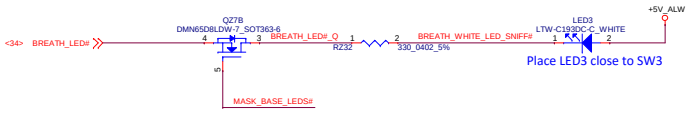


Hall sensor: SA00009EM00
(MAX hight is 1.45mm)

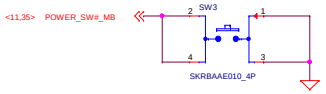


Breath LED

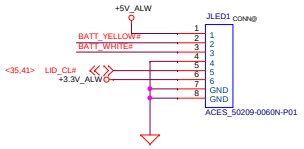
LED P/N change to SCS0000FL00 from SCS0000BA00



POWER & INSTANT ON SWITCH



LED board CONN



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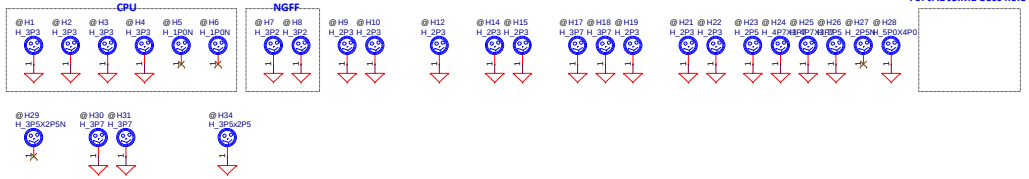
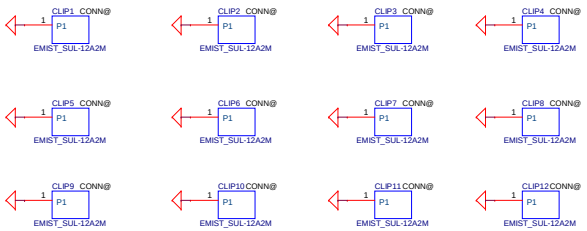
Fiducial Mark

@FD1 FIDUCIAL MARK~D
@FD2 FIDUCIAL MARK~D
@FD3 FIDUCIAL MARK~D
@FD4 FIDUCIAL MARK~D

LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1





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Compal Electronics, Inc.

Title: PAD, LED

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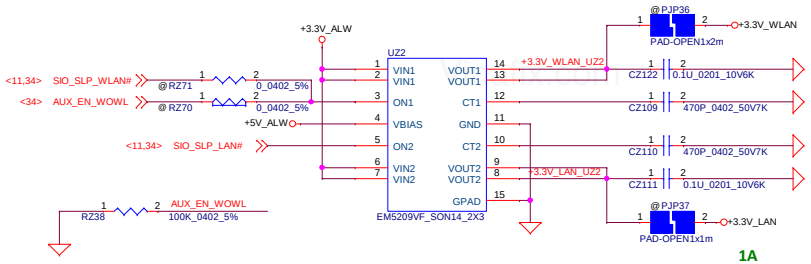
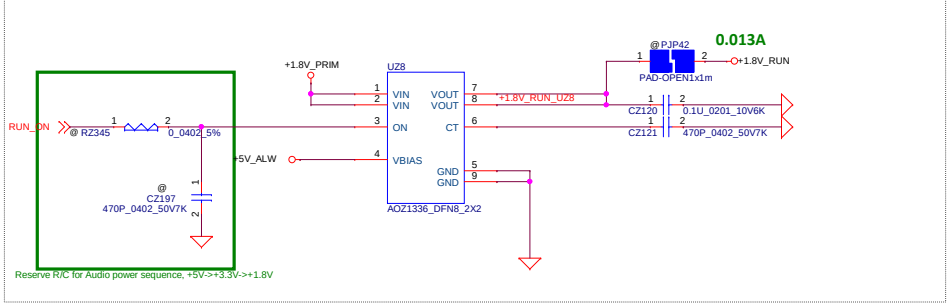
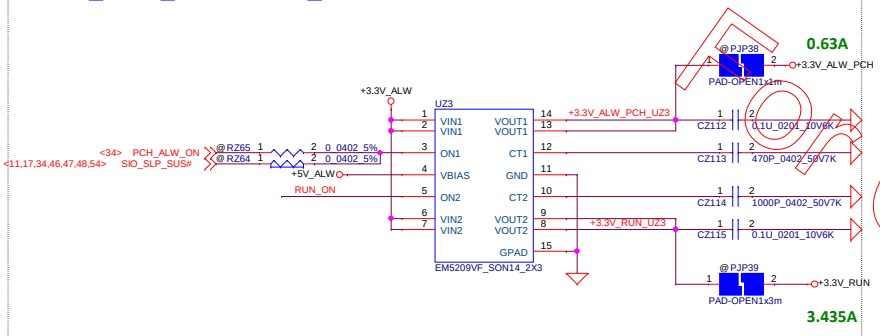
+3.3V_WLAN/+3.3V_LAN source



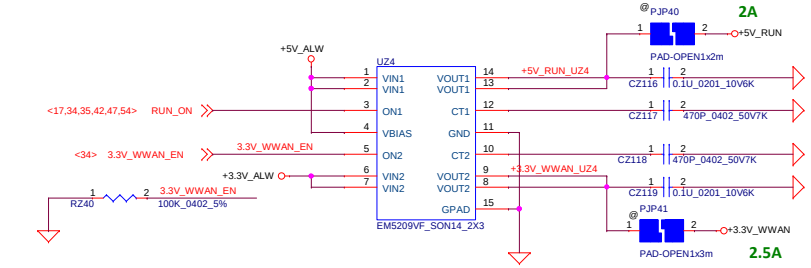
+1.8V_RUN source

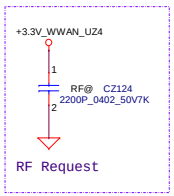


+3.3V_ALW_PCH/+3.3V_RUN source



+5V_RUN/+3.3V_WWAN source





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Compal Electronics, Inc.

Title: Power control

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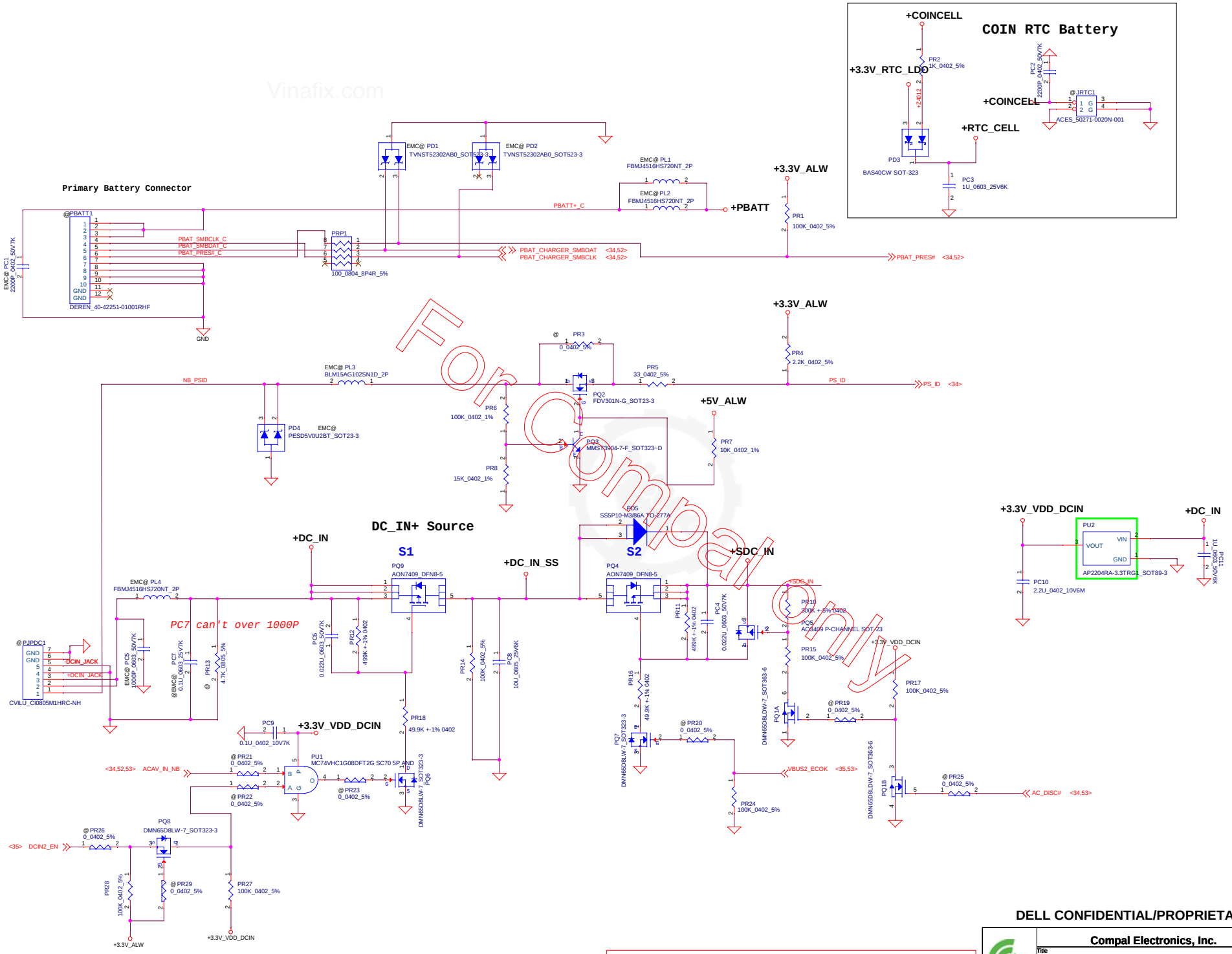
Date: Wednesday, November 09, 2016 | Sheet 42 of 59



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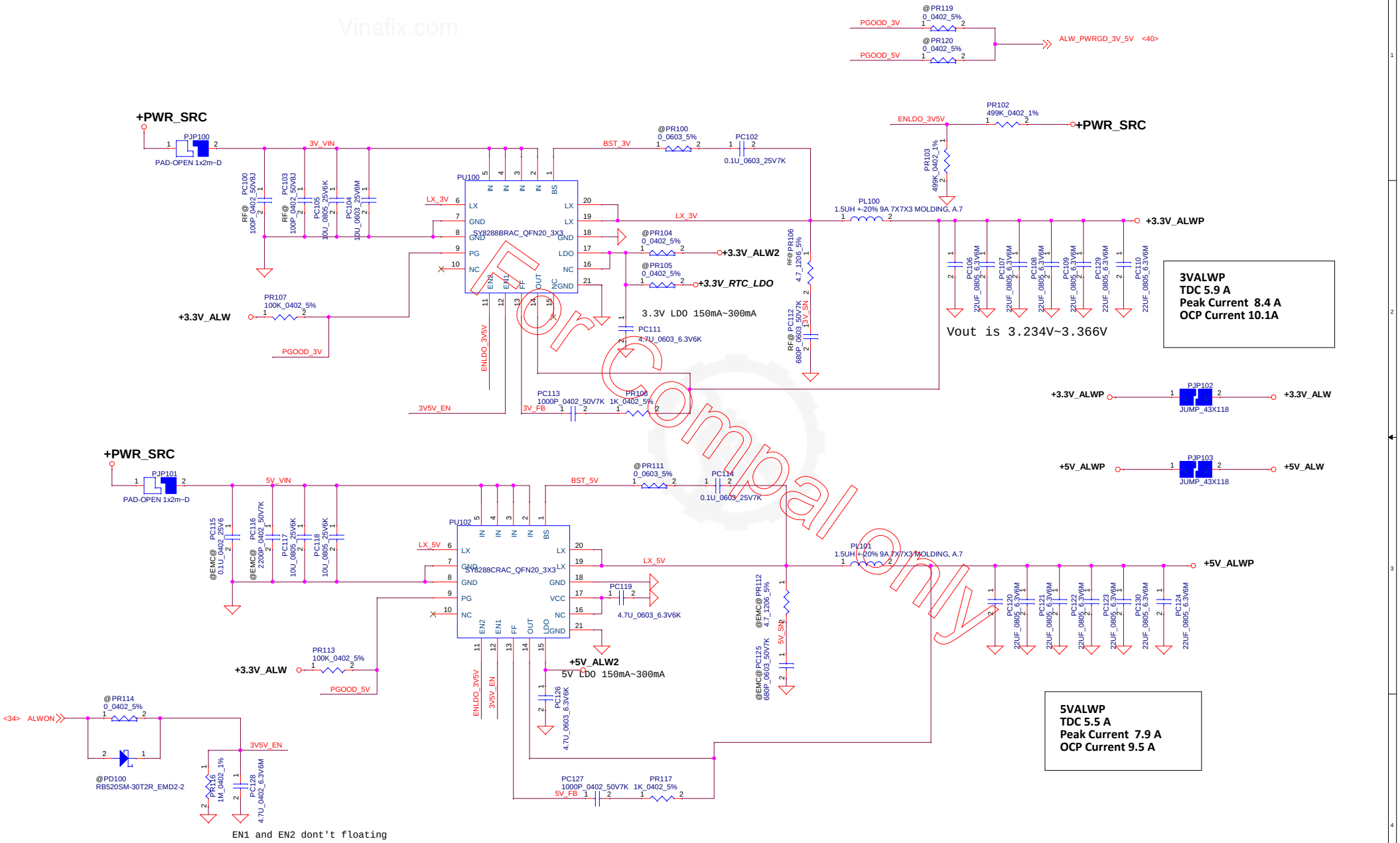
Title: +DCIN			
Size	Document Number: LA-E131P		Rev: 1.0
Date: Wednesday, November 09, 2016	Sheet 43 of 59		



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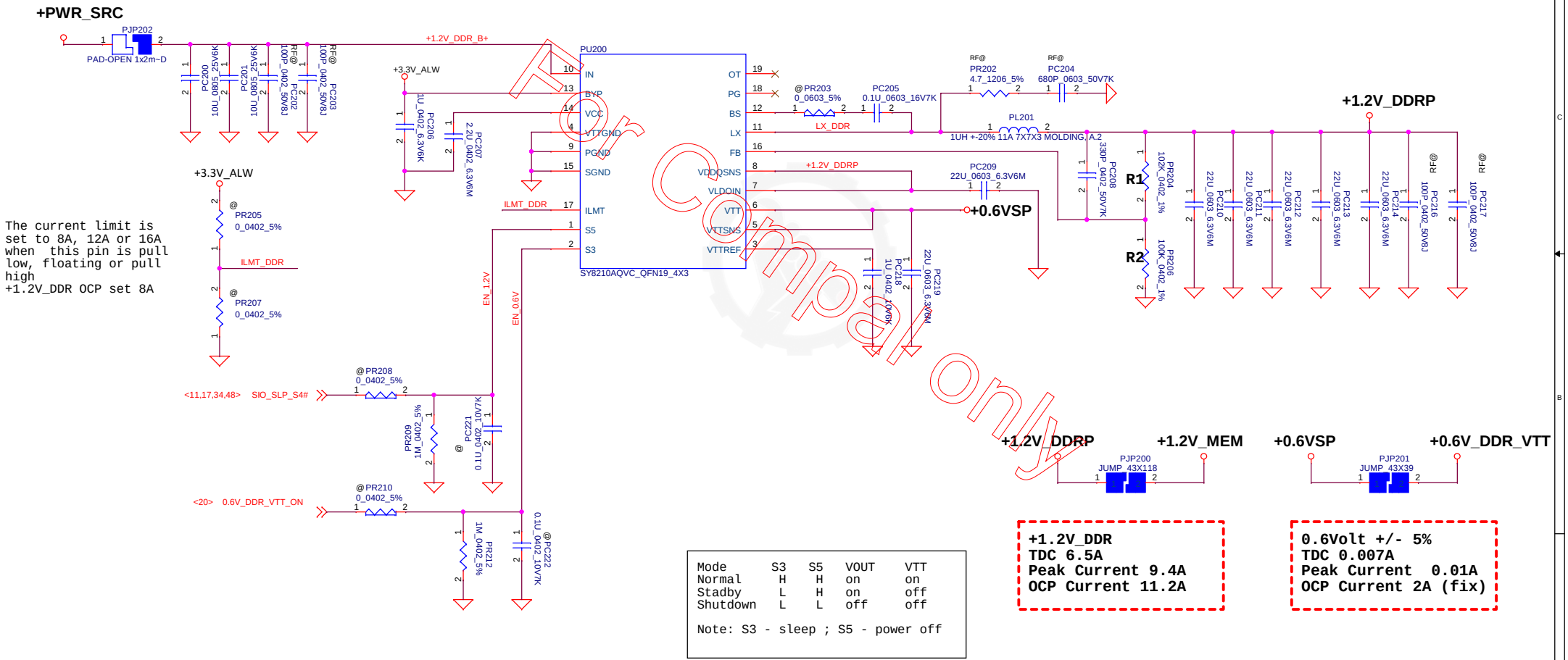
Compal Electronics, Inc.		
Title: +5V_ALW/3.3V_ALW		
Size	Document Number: LA-E131P	Rev: 1.0
Date: Wednesday, November 09, 2016	Sheet 44 of 59	



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Compal Electronics, Inc.	
Title	+1.2V_MEN/+0.6V_DDR_VTT
Size	Document Number: LA-E131P
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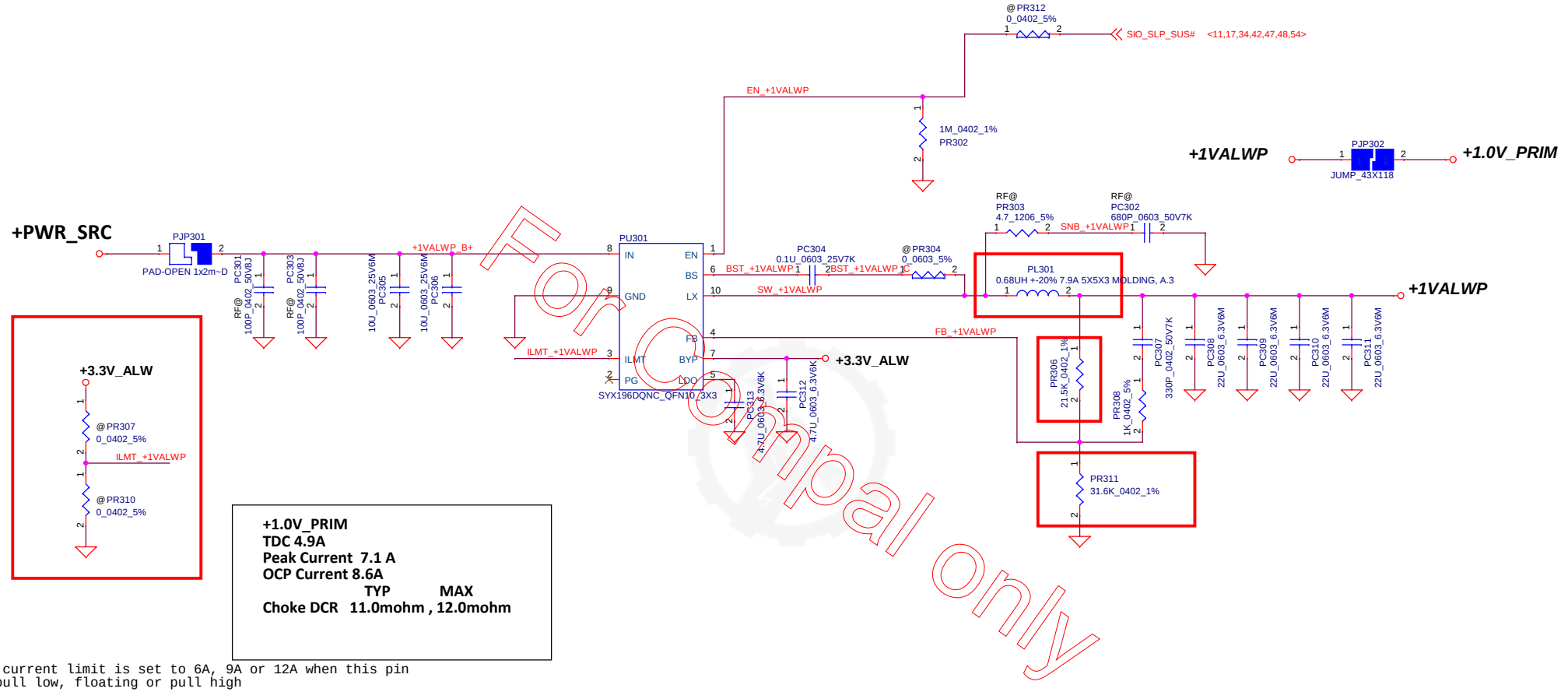

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Compal Electronics, Inc.	
Title	+1VALWP
Size	Document Number: LA-E131P
Rev	1.0
Date:	Wednesday, November 09, 2016
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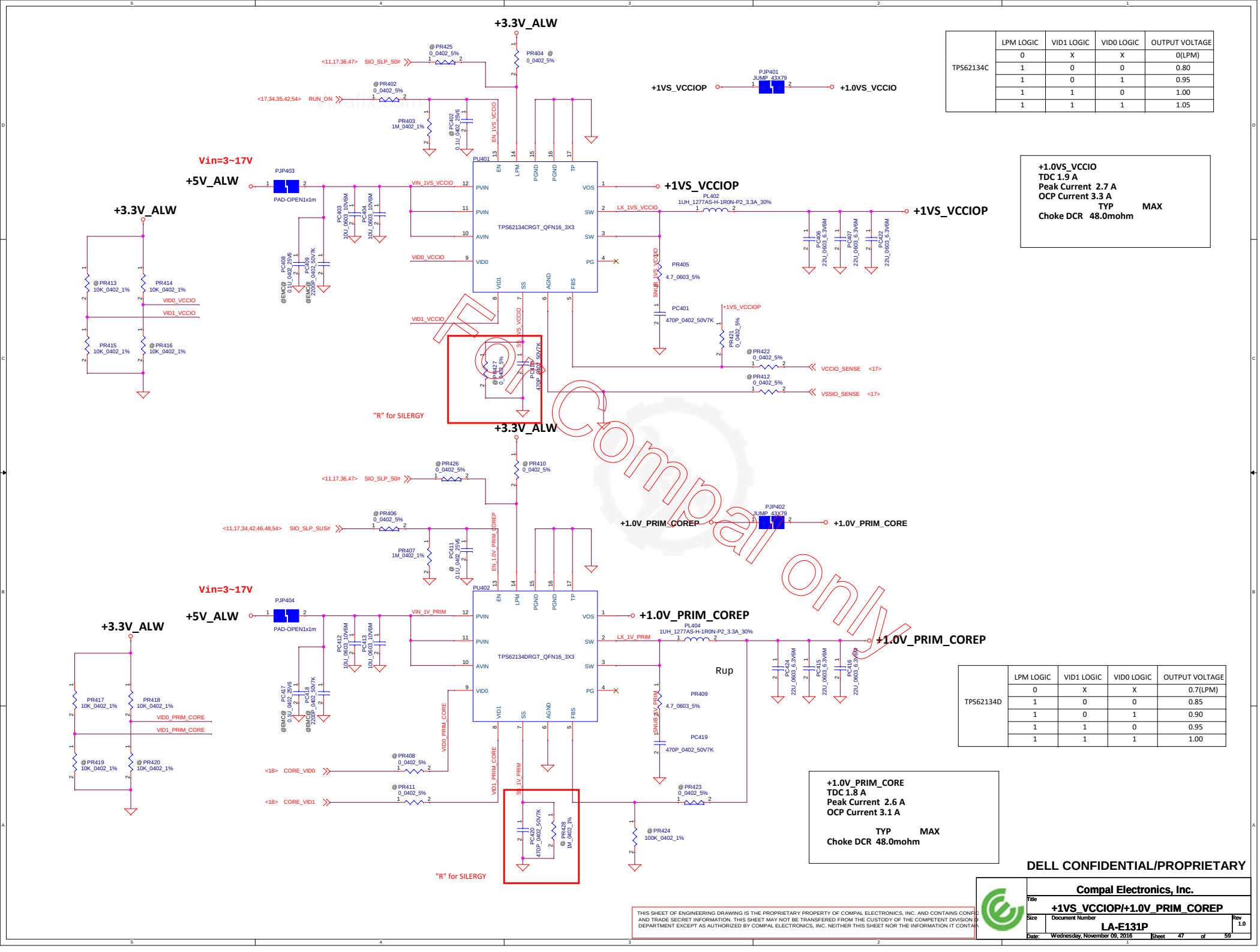

TPS62134C	LPM LOGIC	VID1 LOGIC	VID0 LOGIC	OUTPUT VOLTAGE
	0	X	X	0(LPM)
	1	0	0	0.80
	1	0	1	0.95
	1	1	0	1.00
	1	1	1	1.05

+1.0VS_VCCIO
TDC 1.9 A
Peak Current 2.7 A
OCP Current 3.3 A

	TYP	MAX
Choke DCR	48.0mohm	

TPS62134D	LPM LOGIC	VID1 LOGIC	VID0 LOGIC	OUTPUT VOLTAGE
	0	X	X	0.7(LPM)
	1	0	0	0.85
	1	0	1	0.90
	1	1	0	0.95
	1	1	1	1.00

+1.0V_PRIM_CORE
TDC 1.8 A
Peak Current 2.6 A
OCP Current 3.1 A

	TYP	MAX
Choke DCR	48.0mohm	

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Title: +1VS_VCCIOP/+1.0V_PRIM_COREP

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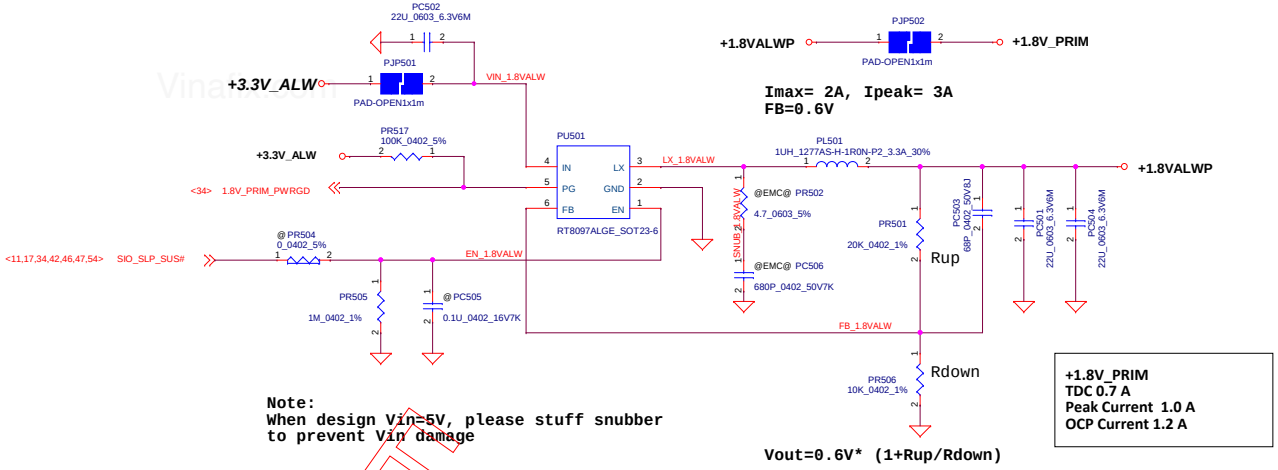

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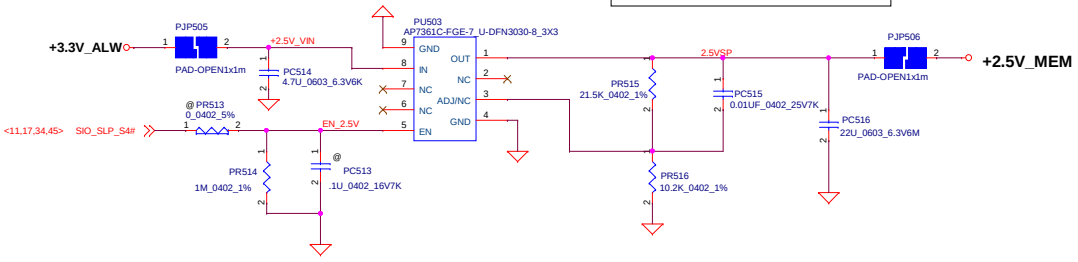

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Title: +1.8VALWP/+1.5VSP		
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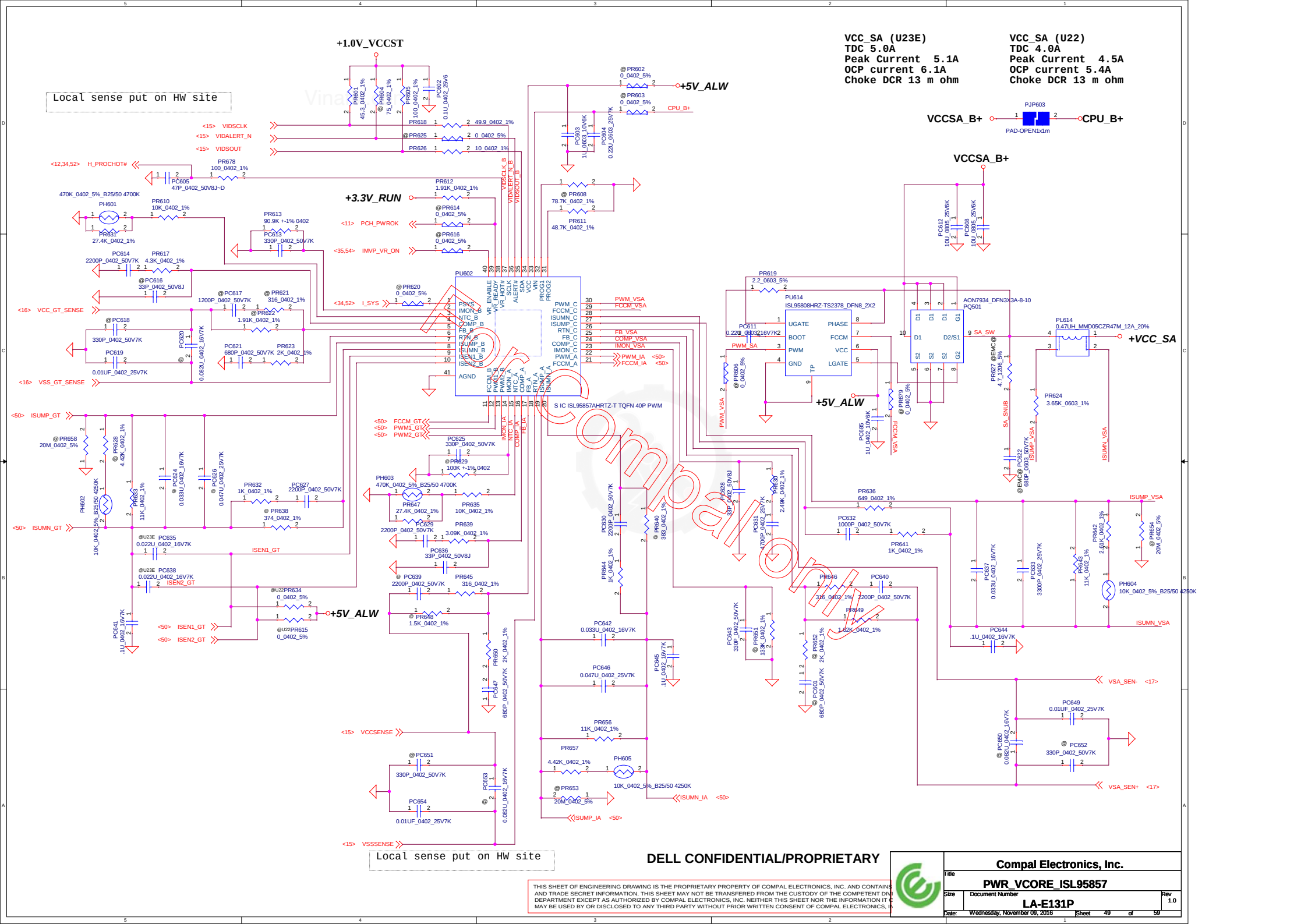
VCC_SA (U23E)
TDC 5.0A
Peak Current 5.1A
OCP current 6.1A
Choke DCR 13 m ohm
VCC_SA (U22)
TDC 4.0A
Peak Current 4.5A
OCP current 5.4A
Choke DCR 13 m ohm
Local sense put on HW site
+1.0V_VCCST
+5V_ALW
+3.3V_RUN
VCCSA_B+
CPU_B+
PJP603
PAD-OPEN1x1m
PU602
PU614
ISL95808HRZ-TS2378_DFN8_2X2
AON7934_DFN3X3A-8-10
PQ501
+VCC_SA
S IC ISL95857AHRTZ-T TQFN 40P PWM
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Compal Electronics, Inc.
PWR_VCORE_ISL95857
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VCC_core (U22)
TDC 21A
Peak Current 32A
OCP current 38.4A
Choke DCR 0.9 +-7%m ohm

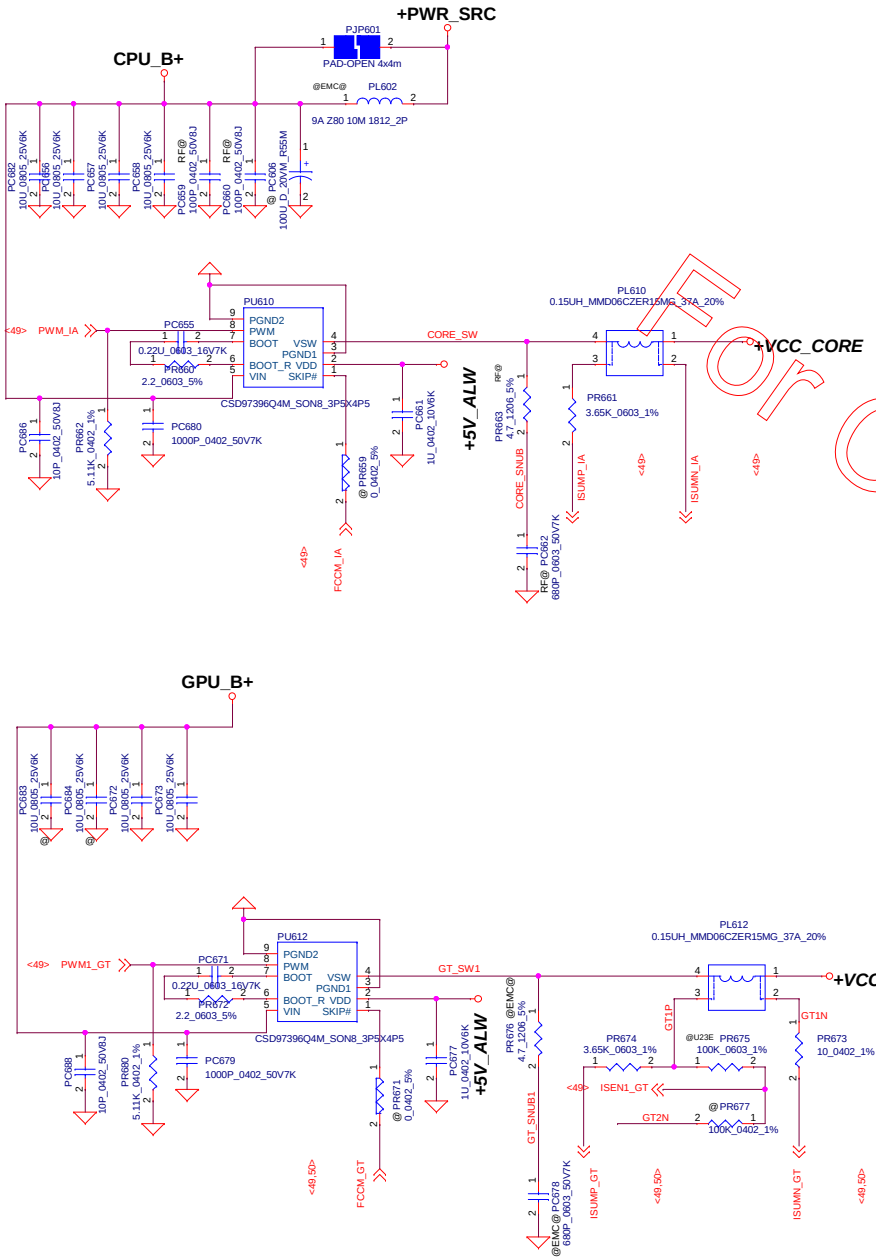
VCC_core (U23E)
TDC 22A
Peak Current 29A
OCP current 34.8A
Choke DCR 0.9 +-7%m ohm

U23E

PR628 @U23E	PR651 @U23E	PC626 @U23E	PR621 @U23E	PR608 @U23E	PR648 @U23E	PR622 @U23E
4.99K +-1% 0402	78.7K +-1% 0402	0.022U_0402_16V7K	1K +-1% 0402	100K +-1% 0402	1.5K +-1% 0402	2.55K_0402_1%
PR640 @U23E	PR638 @U23E	PR629 @U23E	PC624 @U23E	PC616 @U23E	PC617 @U23E	PC639 @U23E
383 +-1% 0402	470 +-1% 0402	86.6K +-1% 0402	0.1U 25V 0402	68P 50V J 0402	220P 50V 0402	2200P 50V 0402

U22

PR628 @U22	PR651 @U22	PC626 @U22	PR621 @U22	PR608 @U22	PR648 @U22	PR622 @U22
4.42K +-1% 0402	133K +-1% 0402	0.047U_0402_25V7K	316 +-1% 0402	78.7K +-1% 0402	1.5K +-1% 0402	1.91K +-1% 0402
PR640 @U22	PR638 @U22	PR629 @U22	PC624 @U22	PC616 @U22	PC617 @U22	PC639 @U22
383 +-1% 0402	374 +-1% 0402	100K +-1% 0402	.033U 16V 0402	33P 50V J 0402	1200P 50V 0402	1500P 50V K 0402



VCC_GT (U22)
TDC 18A
Peak Current 31A
OCP current 37.2A
Choke DCR 0.9 +-7%m ohm

VCC_GT (U23E)
TDC 38A
Peak Current 57A
OCP current 68.4A
Choke DCR 0.9 +-7%m ohm

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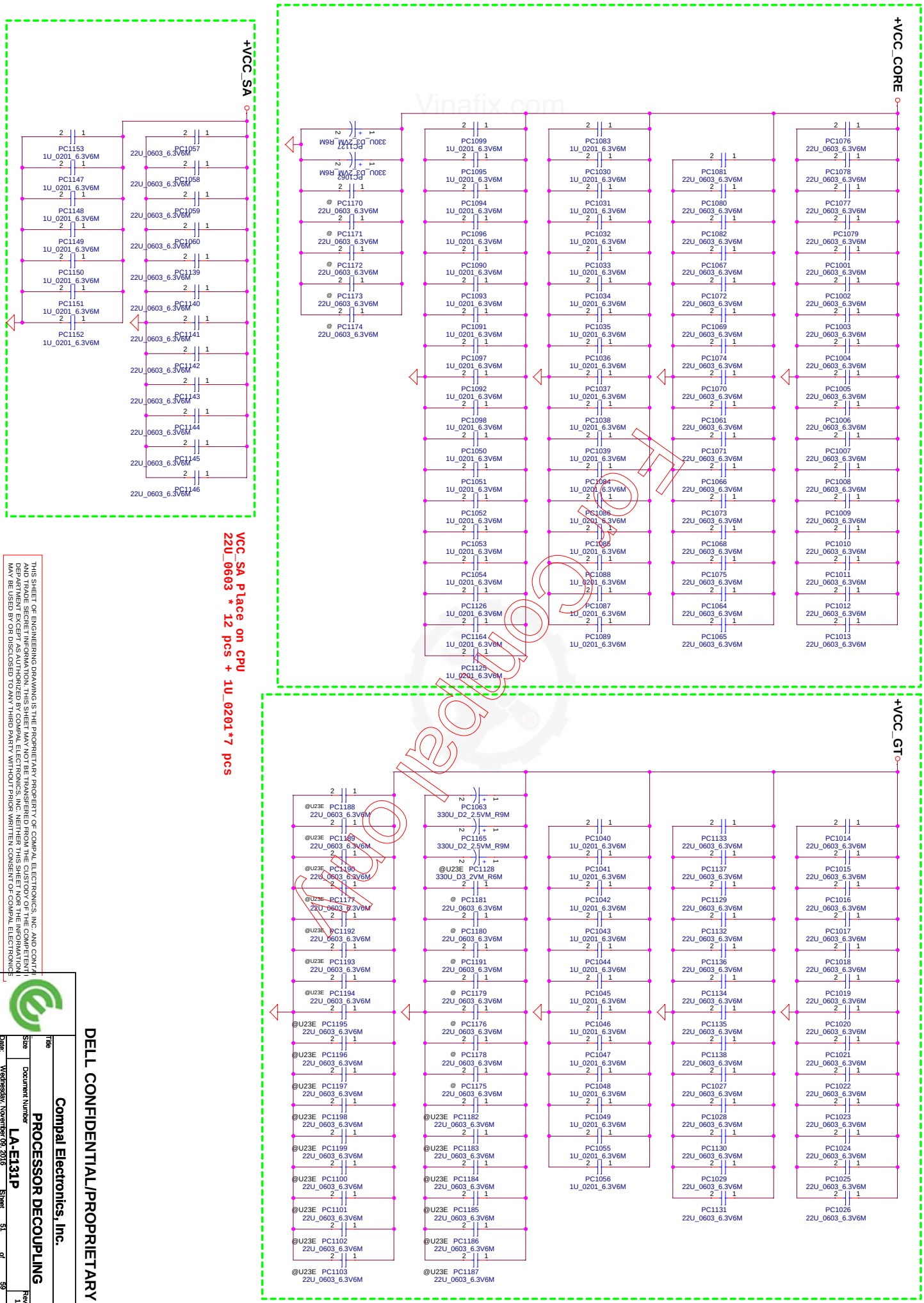

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Title: PROCESSOR DECOUPLING			
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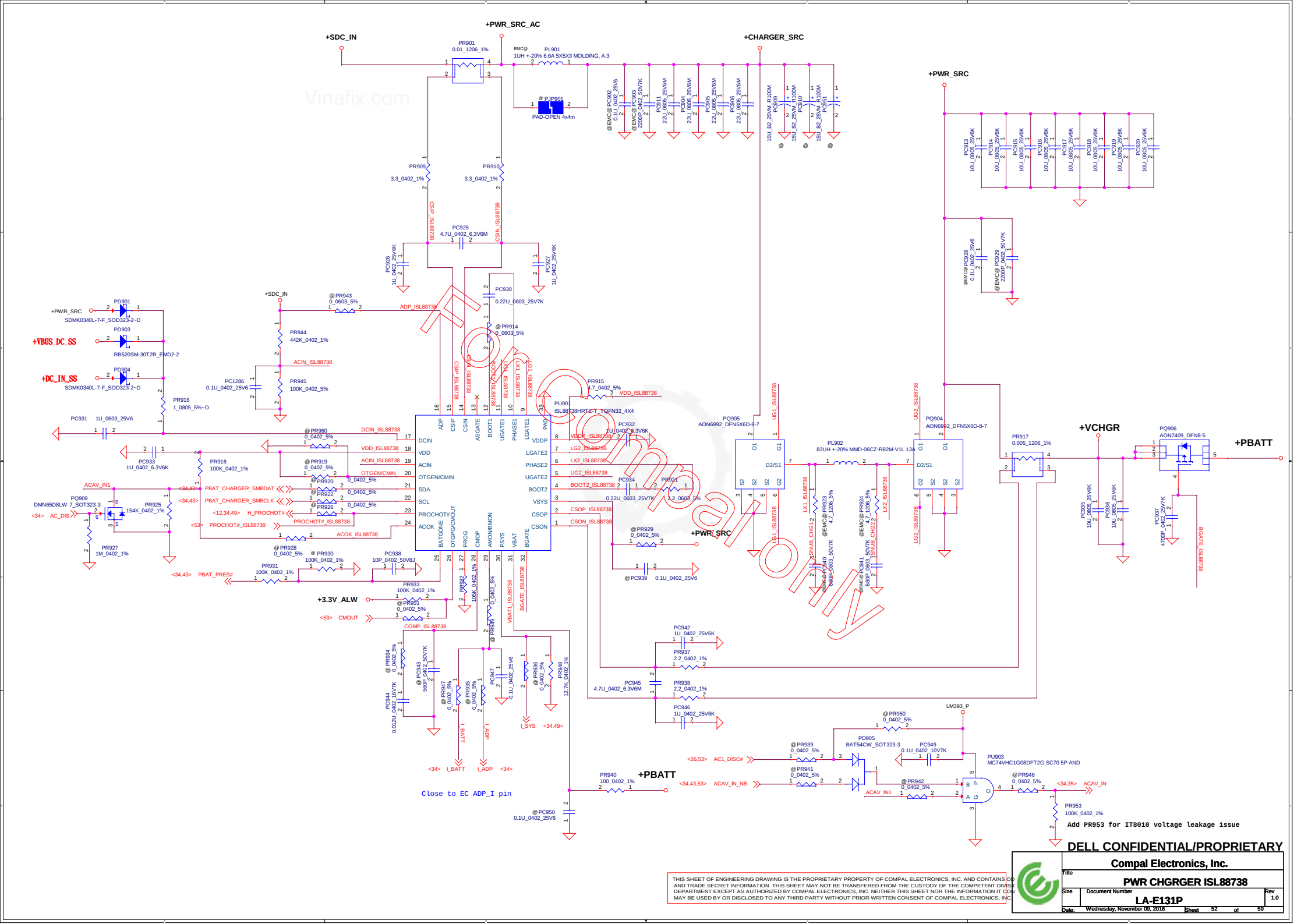
+SDC_IN
+PWR_SRC_AC
+CHARGER_SRC
+PWR_SRC
+VBUS_DC_SS
+DC_IN_SS
+3.3V_ALW
+PBATT
+VCHGR
PR901 0.01_1206_1%
PL901 1UH +-20% 6.6A 5X5X3 MOLDING, A.3
PR909 3.3_0402_1%
PR910 3.3_0402_1%
PC925 4.7U_0402_6.3V6M
PD901 SDMK0340L-7-F_SOD323-2-D
PD903 RB520SM-30T2R_EMD2-2
PD904 SDMK0340L-7-F_SOD323-2-D
PR916 1_0805_5%~D
PC931 1U_0603_25V6
PR944 442K_0402_1%
PR945 100K_0402_5%
PC1286 0.1U_0402_25V6
PR943 0_0603_5%
PC930 0.22U_0603_25V7K
PR914 0_0603_5%
PR915 4.7_0402_5%
PU901 ISL88738HRTZ-T_TQFN32_4X4
PC932 1U_0402_6.3V6K
PC933 1U_0402_6.3V6K
PR918 100K_0402_1%
PR960 0_0402_5%
PR919 0_0402_5%
PR920 0_0402_5%
PR922 0_0402_5%
PR926 0_0402_5%
PR928 0_0402_5%
PR930 100K_0402_1%
PC938 10P_0402_50V8J
PR931 100K_0402_1%
PR933 100K_0402_1%
PR921 0_0402_5%
PR932 100K_0402_1%
PR929 0_0402_5%
PC939 0.1U_0402_25V6
PC934 0.22U_0603_25V7K
PR934 0_0402_5%
PC943 560P_0402_50V7K
PC944 0.012U_0402_16V7K
PR947 0_0402_5%
PR935 0_0402_5%
PC947 0.1U_0402_25V6
PR936 0_0402_5%
PR948 12.7K_0402_1%
PR939 0_0402_5%
PR940 100_0402_1%
PC950 0.1U_0402_25V6
PQ905 AON6992_DFN5X6D-8-7
PQ904 AON6992_DFN5X6D-8-7
PL902 .82UH +-20% MMD-06CZ-R82M-V1L 13A
PR923 4.7_1206_5%
PR924 4.7_1206_5%
PC941 680P_0603_50V7K
PC942 1U_0402_25V6K
PR937 2.2_0402_1%
PC945 4.7U_0402_6.3V6M
PR938 2.2_0402_1%
PC946 1U_0402_25V6K
PR917 0.005_1206_1%
PQ906 AON7409_DFN8-5
PC935 10U_0805_25V6K
PC936 10U_0805_25V6K
PC937 470P_0402_25V7K
PR950 0_0402_5%
PD905 BAT54CW_SOT323-3
PC949 0.1U_0402_10V7K
PR941 0_0402_5%
PR942 0_0402_5%
PU903 MC74VHC1G08DFT2G SC70 5P AND
PR946 0_0402_5%
PR953 100K_0402_1%
PC913 10U_0805_25V6K
PC914 10U_0805_25V6K
PC915 10U_0805_25V6K
PC916 10U_0805_25V6K
PC917 10U_0805_25V6K
PC918 10U_0805_25V6K
PC919 10U_0805_25V6K
PC920 10U_0805_25V6K
PC928 0.1U_0402_25V6
PC929 2200P_0402_50V7K
PR909 DMN65D8LW-7_SOT323-3
PR925 154K_0402_1%
PR927 1M_0402_1%
PC926 1U_0402_25V6K
PC927 1U_0402_25V6K
PC1286 0.1U_0402_25V6
PC933 1U_0402_6.3V6K
PC944 0.012U_0402_16V7K
PC945 4.7U_0402_6.3V6M
PC946 1U_0402_25V6K
PC947 0.1U_0402_25V6
PC950 0.1U_0402_25V6
PC939 0.1U_0402_25V6
PC941 680P_0603_50V7K
PC942 1U_0402_25V6K
PC945 4.7U_0402_6.3V6M
PC946 1U_0402_25V6K
PC949 0.1U_0402_10V7K
PC928 0.1U_0402_25V6
PC929 2200P_0402_50V7K
PC913 10U_0805_25V6K
PC914 10U_0805_25V6K
PC915 10U_0805_25V6K
PC916 10U_0805_25V6K
PC917 10U_0805_25V6K
PC918 10U_0805_25V6K
PC919 10U_0805_25V6K
PC920 10U_0805_25V6K
PC935 10U_0805_25V6K
PC936 10U_0805_25V6K
PC937 470P_0402_25V7K
ADP_ISL88738
CSIP_ISL88738
CSIN_ISL88738
VDD_ISL88738
ACIN_ISL88738
OTGEN/CMIN
PBAT_CHARGER_SMBDAT
PBAT_CHARGER_SMBCLK
H_PROCHOT#
PROCHOT#_ISL88738
ACOK_ISL88738
PBAT_PRES#
CMOUT
COMP_ISL88738
DCIN_ISL88738
LGATE1_ISL88738
LGATE2_ISL88738
PHASE2_ISL88738
UGATE2_ISL88738
BOOT2_ISL88738
CSOP_ISL88738
CSON_ISL88738
BGATE_ISL88738
VBAT1_ISL88738
UG1_ISL88738
UG2_ISL88738
LX1_ISL88738
LX2_ISL88738
LG1_ISL88738
LG2_ISL88738
I_SYS
I_BATT
I_ADP
ACAV_IN1
ACAV_IN_NB
AC1_DISC#
AC_DIS
LM393_P
Close to EC ADP_I pin
Add PR953 for IT8010 voltage leakage issue
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Compal Electronics, Inc.
PWR CHGRGER ISL88738
LA-E131P
Wednesday, November 09, 2016
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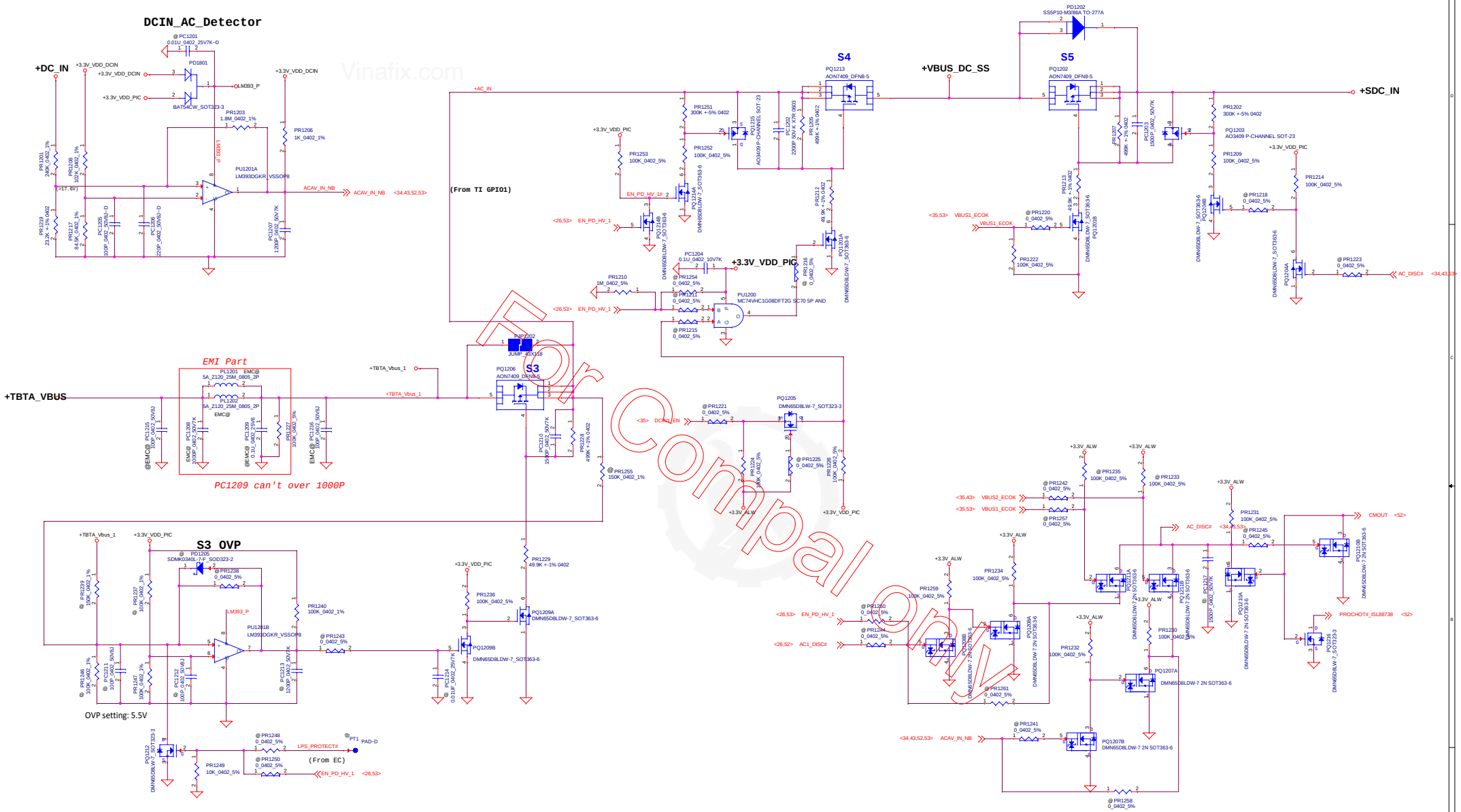

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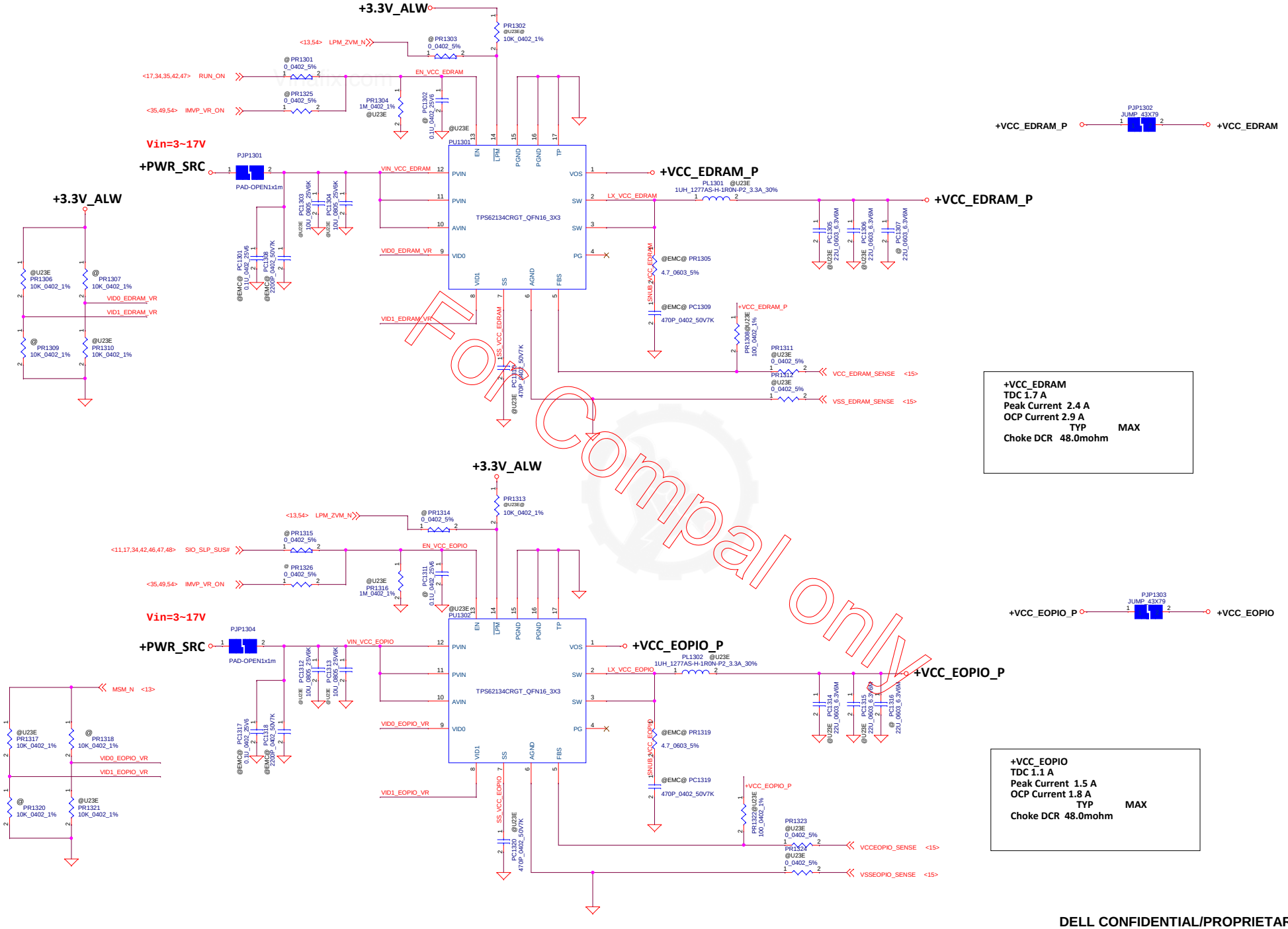

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Title	PWR-VCCEDRAM/EOPIO
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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	56	Change CPU VR version	2016 05/24	Compal	change solution version to fix PS4 funciton issue	change ISL95857HRTZ to ISL95857AHRTZ	X01
2	60	Change the S4 fast turn off circuit to avoid the leakage	2016 05/30	Compal	Change the S4 fast turn off circuit to avoid the leakage	Re-connect the PR1251.1 and PQ1215.3 from +VBUS_DC_SS to +AC_IN	X01
3	59	Add the Circuit for Multiple Input Detach detection & PROCHOT#	2016 05/30	Compal	Add the Circuit for Multiple Input Detach detection & PROCHOT#	Charger:Add PR960 and depop PR919 let the PU901.20 CMIN connect to GND. Add 1 net PROCHOT# ISL88738 TypeC: Add PQ1216 to drive the PROCHOT# and PC1217 to do the reserve.	X01
4	50	MOS leakage problem	2016 05/30	Compal	To solve the MOS leakage problem to avoid the error active	PR12, PR11, PR1205, PR1207 and PR1228 change to 499K from 1M ohm PR16, PR18, PR1212, PR1213 and PR1229 change to 49.9K from 1M ohm PR10, PR1251 and PR1202 change to 300K from 100K ohm.	X01
5	60	Reserve the OVP function	2016 05/30	Compal	Reserve the OVP function to protect the typeC device.	Depop PJP1202, PR1255, PR1239, PR1246, PC1211, PR1237, PC1212, PD1205, PC1213, PC1214 and PR1248 Change the PR1247 from 200K_0402_1% to 100K_0402_5% ohm	X01
6	59	Decrease the charger input leakage voltage	2016 05/30	Compal	To decrease the charger input leakage voltage for TypeC AC	Change the PD903 from SCS0340L010 to SCS00006C00.	X01
7	51	Reduce footprint size for DFX request	2016 07/14	Compal	Reduce PC104 footprint size for DFX request	Change PC104 from 0805 change 0603 size for DFX request	X01
8	60	Fine tune the DC-IN detect voltage	2016 07/14	Compal	For Temp/Voltage test to fine tune the DC-IN detect voltage from 17.6V to 16.9V	PR1219 change from 22.6K to 23.2K. SD034232280	X02
9	59	Change Charger version	2016 07/14	Compal	Charger IC update version	1. Change the charger version to B version from A version 2. Change the PC926, PC927, PC942 and PC946 from 0 to 1uF/0402_25V 3. Change the PC925 and PC945 from 1uF to 4.7uF/0402_10V. 4. Change the PR909 and PR910 from 1 Ohm to 3.3 Ohm. 5. Change the PR937 and PR938 from 1 Ohm to 2.2 Ohm. 6. Change the PC944 from 47nF to 12nF. 7. Change from PR932 from 118K to 105K 8. Change PD901 pull up source from +PBATT to +PWR_SRC 9. Add PC1286 0.1U_0402_25V	X02
10	57	Location Alignment	2016 07/20	Compal	Location Alignment	VCCSA change the PU606 to PU614 and PL601 to PL614 IA change the PU603 to PU610 and PL603 to PL610 GT change the PU604 to PU612 and PL604 to PL612	X02
11	56	SA OVP	2016 08/29	Compal	SA OVP when C status change	1. Change the PL614 from 1uH to 0.47uH 2. Change the PR651 from 124K to 133K 3. Change the PR636 from 1.24K to 649 4. Change the PC633 from 6800p to 3300p 5. Change the PR630 from 7.32K to 2.49K 6. Change the PC628 from 10p to 33p 7. Change the PC632 from 2200p to 1000p 8. Change the PC631 from 1200p to 4700p 9. Remove PC601 & PR652	X02
12	59	S5 power consumption	2016 08/29	Compal	S5 Power consumption fail because UE1 pin C7 has leakage	Add PR952 pull down 100K resistor to discharge UE1 pin C7 leakage	X02
13	54	Enable LPM mode	2016 08/29	Compal	Enable PRIM_CORE low power mode	Remove : PR410 Stuff : PR426	X02
14	51	For EMI request	2016 09/08	Compal	Add some parts for EMI request	stuff : PR106,PR202,PR303,PR663 stuff : PC112,PC204,PC302,PC662 stuff : PC100,PC103,PC202,PC203,PC216,PC217,PC301,PC303,PC659,PC660 stuff : PL901	X03
15	60	Modify symbol to 2nd source	2016 09/08	Compal	Modify PD1202,PD5 to 2nd source because vendor EOL	Modify PD1202,PD5 to 2nd source(SCS00005X00) because vendor EOL	X03
16	57	For U23e CPU modify	2016 09/23	Compal	Modify PR628 / PC626 value after Intel Validation test for U23e CPU	1. Change the PR628 from 2.61K to 4.99K for U23 CPU 2. Change the PC626 from 0.047u to 0.022u for U23 CPU 3. Change the PR622 from 2.49K to 2.55K for U23 CPU 4. Change the PR651 from 82K to 78.8K for U23 CPU	X03
17	51	Reserve symbol footprint	2016 09/26	Compal	Reserve symbol 3 pcs footprint	1. Reserve symbol PD100 footprint for 3V/5V enable 2. Reserve PR1325 / PR1326 footprint for sequence	X03
18	61	Enable LPM mode	2016 09/26	Compal	Enable EDRAM / EOPIO low power mode	1. Un-pop : PR1302 / PR1313 2. Stuff : PR1303 / PR1314	X03
19	59	Max. Power up to 125W	2016 09/26	Compal	Modify PR948 value for Max. Power 125W	1. Change the PR948 from 10.5K to 12.7K	X03
20	51	Type-C connector voltage droop	2016 10/05	Compal	Type-C connector voltage droop	Add PR121 0 ohm for Type-C connector voltage droop issue	X04
21	54	VCCIO design modify	2016 10/05	Compal	VCCIO design modify	1. VCCIO use local sense: PR421 change to 0 ohm, de-pop PR422,PR412 2. VCCIO change to 0.95V: De-pop PR413,PR416, pop PR415,PR414	X04
22	54		2016 11/02	Compal	Delete reserve resistor	Delete PR121	A00
23							

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PWR P.I.R

LA-E093P

Rev 1.0

Wednesday, November 02, 2016

Version Change List (P. I. R. List) LA-E131P

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	24	TBT-AR-SP(1/2) DP,PCIE	2016/05/23	EE	CPU_DP1_HPD need to PD for AR config	Pop RT24	0.2(X01)
2	26	[Type C]PD Controller TI	2016/05/23	EE	UT5.D6 need to PD for TI suggestion	Pop RT101	0.2(X01)
3	26	[Type C]PD Controller TI	2016/05/23	EE	Schematic align	Add net name UT5.B2 : PD1_GPIO0 UT5.C2 : EN_PD_HV_1_R UT5.D10 : PD1_GPIO2 UT5.G11 : AC1_DISC#_R UT5.C10 : TBTA_HPD_R UT5.E10 : PD1_GPIO5 UT5.G10 : PD1_GPIO6 UT5.D7 : PD1_GPIO7	0.2(X01)
4	27	[Type C]PD Power	2016/05/23	EE	TypeC PD solution (dead battery mode)	RT111 change from 10K to 100K (SD028100380) CT90 change from 100P to 1U (SE00000QL10)	0.2(X01)
5	33	Codec ALC3246	2016/05/23	EMI	EMI request	CA2/CA3 change from 2200P to 330P (SE000006I80)	0.2(X01)
6	24	TBT-AR-SP(1/2) DP,PCIE	2016/05/23	EE	WLAN antenna noise effect AR Crystal, cause TBT- AR no display	Change YT1 from SJ10000JC00 to SJ10000NW00 (metal shielding)	0.2(X01)
7	41	PAD, LED	2016/05/23	EE	Remove HDD LED MUX feature	Add RZ361 and depop QZ3, QZ2, RZ25	0.2(X01)
8	34	EC MEC5105	2016/05/23	EE	Schematic align	Add net VCI_IN1# and add PU RE507 Add net VCI_IN2# and add PU RE508	0.2(X01)
9	36	USH & TPM	2016/05/23	EE	Atmel request for current TPM silicon	Add CZ74 (pop) and RZ72(depop) for UZ12.7	0.2(X01)
10	9	CPU (4/14)	2016/05/23	EE	Cardreader change to RTS5242 (PCIE)	Add net MEDIACARD_IRQ# to UC1.AN8	0.2(X01)
11	31	Card Reader	2016/05/23	EE	Cardreader change to RTS5242 (PCIE)	Cardreader schematic change from RTS5330 (USB) to RTS5242 (PCIE)	0.2(X01)
12	10	CPU (5/14)	2016/05/23	EE	Cardreader change to RTS5242 (PCIE)	Change net from USB3.0 port 5 to PCIE port1 Delete USB2.0 port 6	0.2(X01)
13	10	CPU (5/14)	2016/05/23	EE	No support M.2 3042 (HCA)	Remove PCIE port 10	0.2(X01)
14	11	CPU (6/14)	2016/05/23	EE	No support M.2 3042 (HCA)	Assign CLKREQ_PCIE#0 to Cardreader	0.2(X01)
15	32	NGFF Card	2016/05/23	EE	No support M.2 3042 (HCA)	Remove PCIE port 10, CZ10, CZ11	0.2(X01)
16	37	M2 2280 Socket	2016/05/23	EE	Remove HDD LED MUX feature	Depop RN100	0.2(X01)
17	34	EC MEC5105	2016/05/23	EE	PORT80_DET#	Change location RE510 to RE512 Reserve RE513 100k (SD028100380) to GND	0.2(X01)
18	6	CPU (1/14)	2016/05/23	EE	Follow Intel PDG AUX topology	Delete RC179/RC180/RC181/RC182	0.2(X01)
19	17	CPU (12/14)	2016/05/23	EE	S0ix(modern standy) support for VCCPLL_OC	Pop RZ120 and Depop UZ34 Add net name VCCSTG_EN(UZ19.4) and connect to RZ120.1	0.2(X01)
20	34	EC MEC5105	2016/05/25	EE	Symbol pin name change	UE1.C1 pin name change to GPIO024_nRESETI	0.2(X01)
21	26	[Type C]PD Controller TI	2016/05/25	EE	Symbol pin name change	UT5.A6/A7/A8/B7 pin name change to GND, UT5.D6 pin name change to HRESET	0.2(X01)

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
22	36 40	USH & TPM Keyboard	2016/05/25	ME	Connector update	JUSH1 change to LTCX007Q600 JKBTP1 change to LTCX007Q500	0.2(X01)
23	41	PAD, LED	2016/05/25	ME	MB ME drawing change	Remove H11 and change H28 to H_5P0X4P0	0.2(X01)
24	6	CPU (1/14)	2016/05/31	EE	DP HPD base on INTEL PDG	Delete RC312/RC242	0.2(X01)
25	32	NGFF Card	2016/06/01	EE	Intel reviwe result	CZ28,CZ29 change from 0.047uF to 0.01uF CZ27 change from 0.1uF(@)_0201 to 10uF_0603 CZ32/CZ31/CZ29 place near JNGFF1.2/JNGFF1.4 CZ27/CZ30/CZ28 place near JNGFF1.72/JNGFF1.74	0.2(X01)
26	30	LAN Clarkvillie & RJ45	2016/06/01	EE	EMI request	Change CL22 from 1500P to 150P (SE00000FA80)	0.2(X01)
27	33	Codec ALC3246	2016/06/01	EE	Audio EA modify (meet GS mark)	Change RA7, RA8 from 24.9ohm to 16.2ohm (SD00001U900)	0.2(X01)
28	11 24	CPU (6/14) TBT-AR-SP(1/2) DP, PCIE	2016/06/01	EE	Crystal EA modify	Change CC21, CC22 from 15pf to 12pf Change CT20, CT21 from 20pf to 8.2pf	0.2(X01)
29	36	USH & TPM	2016/06/01	EE	TPM change to Nuvoton NPCT650JBAYX	All page	0.2(X01)
30	36	USH & TPM	2016/06/04	EE	Vendor schematic review	UZ12 change to NPCT650JB2YX (SA00008EL70) Add CZ75 4.7uF (SE00000SO00) for +UZ12_TPM	0.2(X01)
31	12	CPU (7/14)	2016/06/04	RF	Intel MOW request	Add CC331 2.2PF (SE07122AC80) for HDA_RST# Add CC332 2.2PF (SE07122AC80) for HDA_SDIN0 Add CC333 2.2PF (SE07122AC80) for HDA_SDOUT	0.2(X01)
32	32	NGFF Card	2016/06/04	RF	Intel reviwe result (WWAN Coex feature support)	Add RZ128 0 ohm connect WWAN_COEX3 and WLAN_COEX3 Add RZ129 0 ohm connect WWAN_COEX2 and WLAN_COEX2 Add RZ130 0 ohm connect WWAN_COEX1 and WLAN_COEX1	0.2(X01)
33	33	Codec ALC3246	2016/06/04	ESD	ESD request	Change LA10, LA11 to SM01000OZ00	0.2(X01)
34	29	eDP CONN& Touch screen	2016/06/04	EMI	EMI request	Change LV1 to SM01000NY00	0.2(X01)
35	32	NGFF Card	2016/06/06	EE	Debug card reserve	Add RZ131, RZ132 for PORT80_DET# and HOST_DEBUG_TX	0.2(X01)
36	13 18	CPU (8/14) CPU (13/14)	2016/06/06	EE	For RF noise issue layout modify-SB14 only	Change CC213 to 0201 size (SE00000YB00) and remove T14	0.2(X01)
37	36	USH & TPM	2016/06/07	EE	Schematic align	Change loaction RZ90 to RZRZ362	0.2(X01)
38	24	USH & TPM	2016/06/14	EE	TPM pre-config	Reserve RZ363 ohm for GPIO2 and SIO_SLP_S3#	0.2(X01)
39	36	TBT-AR-SP(1/2) DP, PCIE	2016/06/14	EE	BOM change	Change UT1 from SA00009YL0L to SA00009YL2L (C1)	0.2(X01)
40	12	CPU (7/14)	2016/06/14	RF	RF request	Change CC27 from 22pf to 47pf (SE071470J80)	0.2(X01)
41	23	HDMI CONN	2016/06/14	EMI	EMI request	Change RV24,RV25,RV27,RV28,RV30,RV31,RV33,RV34 to 12nH (SHI0000PJ00) Change RV26,RV29,RV32,RV35 to SHI0000PJ00 to 300ohm (SD028300080)	0.2(X01)
42	20	DDR4	2016/06/14	EE	2nd source align	Change UD1 from SA00007WE00 to SA00007UR00	0.2(X01)
43	34	EC MEC5105	2016/07/13	EE	For MEC5105K-D1-TN EC sample	Change UE1 to SA00009GL00 & Depop RE361,Pop RE360,RE362	0.3(X02)
44	36	USH & TPM	2016/07/13	EE	TPM pre-config	Pop RZ363 and depop (@) RZ111,RZ112, RZ113,QZ9	0.3(X02)

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
45	35	EC MEC5105 Support	2016/07/13	EE	Board ID	Change RE79 to 62Kohm (SD028620280)	0.3(X02)
46	34	EC MEC5105	2016/07/13	EE	GPIO map update	1.UE1.F11 add RTCRST_ON_GPIO122 & reserve RE515@ to QE12.2 2.UE1.B6 change to RTCRST_ON_GPIO141 and add RE514 to QE12.2	0.3(X02)
47	33	Codec ALC3246	2016/07/13	EE	ESD request (2nd source align)	Change LA10, LA11 back to SM01000NA00	0.3(X02)
48	36	USH & TPM	2016/07/13	EE	USH BOM modify	1.RZ10 changed to 100K -Let USH_PWR_STATE# keep low at S5 2.DZ7 depop and pop RZ87 - X8 have no difference JUSH1 pin define with X7	0.3(X02)
49	32	NGFF Card	2016/07/13	EE	Symbol error	Re-link JSIM1 symbol and change SIM_DET to JSIM1.2	0.3(X02)
50	26	[Type C]PD Controller TI	2016/07/13	EE	For PD sample	Change UT5 from SA00009W200 to SA00009W210	0.3(X02)
51	35	EC MEC5105 Support	2016/07/13	EE	Vendor schematic review	Add net WRST# to UE2.4 and CE500 1uf (SE000000K80)	0.3(X02)
52	23	HDMI CONN	2016/07/13	EMI	EMI request	Change RV24 to LV31, RV25 to LV32, RV27 to LV33, RV28 to LV34, RV30 to LV35, RV31 to LV36, RV33 to LV37, RV34 to LV38 and from SHI0000PJ00 to SHI00006Q00	0.3(X02)
53	24	TBT-AR-SP(1/2) DP, PCIE	2016/07/13	EE	Intel reviwe result	1.Change YT1 from SJ10000NW00 to SJ10000NC00 2.TBT_CIO_PLUG_EVENT# add RT391 PU to +3.3V_ALW_PCH and depop RT371 for back-driver issue 3.RTD3_CIO_PWR_EN add RT392 and Pop RT25,depop RT372	0.3(X02)
54	41	PAD, LED	2016/07/20	EE	Intel suggestion	H5, H6 cnage from 1.1mm to 1.0mm	0.3(X02)
55	29	eDP CONN & Touch screen	2016/07/20	ME	Factory request	Change JIR1 to SP01001YO00 to avoid JTS1 and JIR1 assembly error	0.3(X02)
56	30	LAN Clarkvillie & RJ45	2016/07/21	EMI	EMI request	Change CL22 from 150P to 10P (SE167100J80)	0.3(X02)
57	35	EC MEC5105 Support	2016/07/21	EE	Vendor schematic review	Add RE523 0 ohm for UE2 power pin soft start	0.3(X02)
58	29	eDP CONN & Touch screen	2016/07/22	ESD	ESD request	Reserve the ESD diode DV7 on USB20_N5 and USB_P5 for system damage issue	0.3(X02)
59	29	eDP CONN & Touch screen	2016/07/25	ESD	ESD request (layout limit)	Change DV7 to DV7 and DV8 (SC40000AR00)	0.3(X02)
60	34	EC MEC5105	2016/07/25	EE	Vendor schematic review	Change RPE12.1 to RE524 (10Kohm) for EXPANDER_GPU_SMDAT Change RPE12.2 to RE524 (10Kohm) for EXPANDER_GPU_SMCLK	0.3(X02)
61	27	[Type C]PD Power	2016/07/25	EE	For UT7 2nd source issue	Add RT393 PD 100K ohm to +5V_PD_VDD for discharging instantly	0.3(X02)
62	35	EC MEC5105 Support	2016/08/01	EE	Vendor schematic review	Change RE14,RE15,RE18 from 100k ohm to 10k ohm	0.3(X02)
63	40	Keyboard	2016/08/01	EE	Touchpad I2C EA	Chagne RZ20, RZ21 from 4.7k ohm to 2.2k ohm Change CZ80, CZ81 from 330pf to 10pf	0.3(X02)
64	14	CPU (9/14)	2016/08/01	EE	Intel suggestion	Change RC137 from 1k ohm to 3k ohm	0.3(X02)
65	25	TBT-AR-SP (1/2) DP, PCIE	2016/08/01	EE	Crystal EA modify	Change CT20, CT21 from 8.2pf to 27pf	0.3(X02)
66	36	USH & TPM	2016/09/06	EE	TPM change NPCT650VB2YX	Change UZ12 from to SA00008EL70 to SA00008EL80	0.4(X03)
67	35 34	EC MEC5105 Support EC MEC5105	2016/09/06	EE	Expander I/O change to Microchip MCP23008	Change UE2 from SA00009VL00 to SA0000ADQ00, remove RE523 Change RE524, RE525 from 10Kohm to 2.2Kohm	0.4(X03)
68	35	EC MEC5105 Support	2016/09/06	EE	Board ID	Change RE79 to 33kohm (SD028330280)	0.4(X03)

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69	35	EC MEC5105 Support	2016/09/06	EE	EC watchdog reserve	Add QE13,RE530,RE531	0.4(X03)
70	34	EC MEC5105	2016/09/06	EE	Schematic align	Reserve RE526(10K) PU for USH_DET# to +3.3V_ALW	0.4(X03)
71	34	EC MEC5105	2016/09/08	EE	EC request for GPIO setting	Reserve RE505 PU for LOM_CABLE_DETECT# Add RE532 PU for BCM5882_ALERT#	0.4(X03)
72	36	USH & TPM	2016/09/13	EE	EC request for GPIO setting	Pop RZ8, RZ9 for USH_SMBCLK and USH_SMBDAT	0.4(X03)
73	35	EC MEC5105 Support	2016/09/13	EE	EC watchdog delete	Delete QE13,RE530,RE531	0.4(X03)
74	33	Codec ALC3246	2016/09/13	RF	RF request	Pop CA54 82pf for DMIC_CLK0	0.4(X03)
75	35	EC MEC5105 Support	2016/09/26	EE	Dell request	Reserve RE536/RE537 for resistors for PCH_DPWROK circuit	0.5(X04)
76	34	EC MEC5105	2016/09/26	EE	WDT schematic option 2	Use Option2: pop RE361 / depop RE362	0.5(X04)
77	35	EC MEC5105 Support	2016/09/29	EE	WDT schematic	Add QE13, CE503, RE530	0.5(X04)
78	35	EC MEC5105 Support	2016/09/30	EE	Board ID	Change RE79 to 8.2kohm (SD028820180)	0.5(X04)
79	35	EC MEC5105 Support	2016/09/30	EE	BITS294007	Change CE12 to 2.2uf and RE33 to 1Kohm	0.5(X04)
80	34	EC MEC5105	2016/10/05	EE	Prevent EOS issue on MEC5105	Add 100ohm serial resistor on CV2_ON close to UE1.H8	0.5(X04)
81	34	EC MEC5105 Support	2016/11/04	EE	Board ID	Change RE79 to 4.3kohm (SD028820180)	1.0(A00)
82	33	EC MEC5105	2016/11/04	EE	MEC5105 change from revB to revC	Change MEC5105 CPN to SA00009GL30 Depop RE361,Pop RE362	1.0(A00)
83	34	EC MEC5105 Support	2016/11/04	EE	MEC5105 revC WDT schematic	Pop RE536, Depop QE13, CE503, RE530, UE7, CE5,CE6, RE348	1.0(A00)
84	All	All page	2016/11/04	EE	0 ohm short pad	Change 0 ohm to short pad	1.0(A00)
85	12	CPU (7/14)	2016/11/04	EE	Service Mode Switch remove	Depop SW1, RC222 and pop RC221	1.0(A00)

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