FOOSE 14" nVIDIA NB9M Schematics Document

uFCPGA Mobile Penryn

Intel Cantiga-PM + ICH9M

2009-04-07

REV : -1

DY : Nopop Component
B_TPM : Use LOM TPM
C_TPM : Use China TPM

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Title	*Foose Intel Discrete*	
Size: A3	Document Number: *Cover Page*	Rev: *-1*
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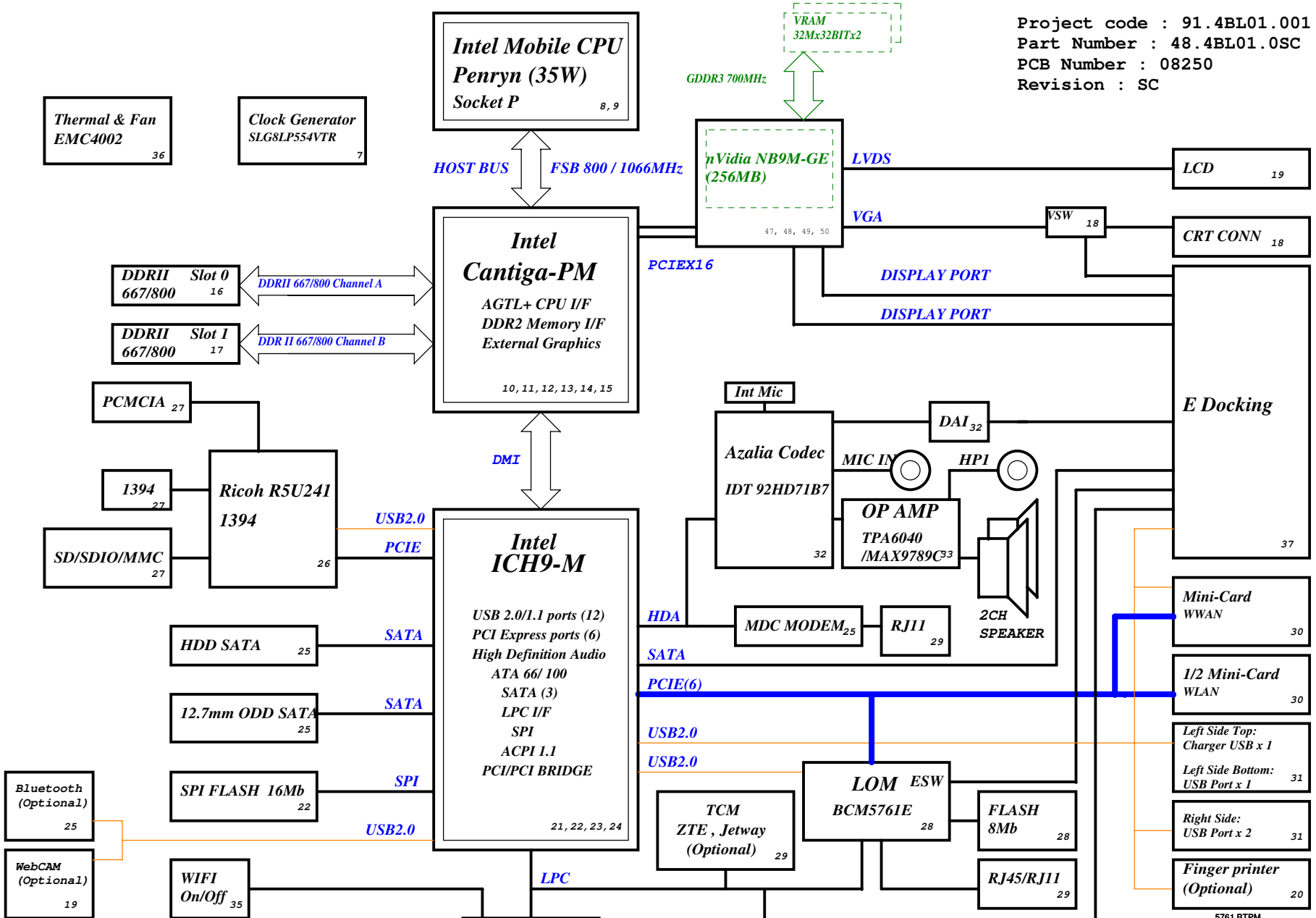
Foose Intel 14" Discrete Block Diagram

Project code : 91.4BL01.001
Part Number : 48.4BL01.0SC
PCB Number : 08250
Revision : SC



CPU DC/DC ISL6260	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

GPU DC/DC TPS51511	
INPUTS	OUTPUTS
+PWR_SRC +1.8V_SUS	+GPU_CORE +1.1V_GFX_PCIE

SYSTEM DC/DC SN0608098	
INPUTS	OUTPUTS
+PWR_SRC	+3.3V_ALW +5V_ALW

SYSTEM DC/DC TPS5117	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VCCP

SYSTEM DC/DC RT9035(LDO)	
INPUTS	OUTPUTS
+1.8V_SUS	+1.5V_RUN

SYSTEM DC/DC TPS5116	
INPUTS	OUTPUTS
+PWR_SRC	+1.8V_SUS

SYSTEM DC/DC TPS5116(LDO)	
INPUTS	OUTPUTS
+1.8V_SUS	+V_DDR_MCH_REF +0.9V_DDR_VTT

SYSTEM DC/DC EMC4002(LDO)	
INPUTS	OUTPUTS
+3.3V_RUN	+2.5V_RUN

TI CHARGER BQ24745	
INPUTS	OUTPUTS
+DC_IN +VCHGR	+PWR_SRC

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Size: A3 | Document Number: System Block Diagram | Rev: -1

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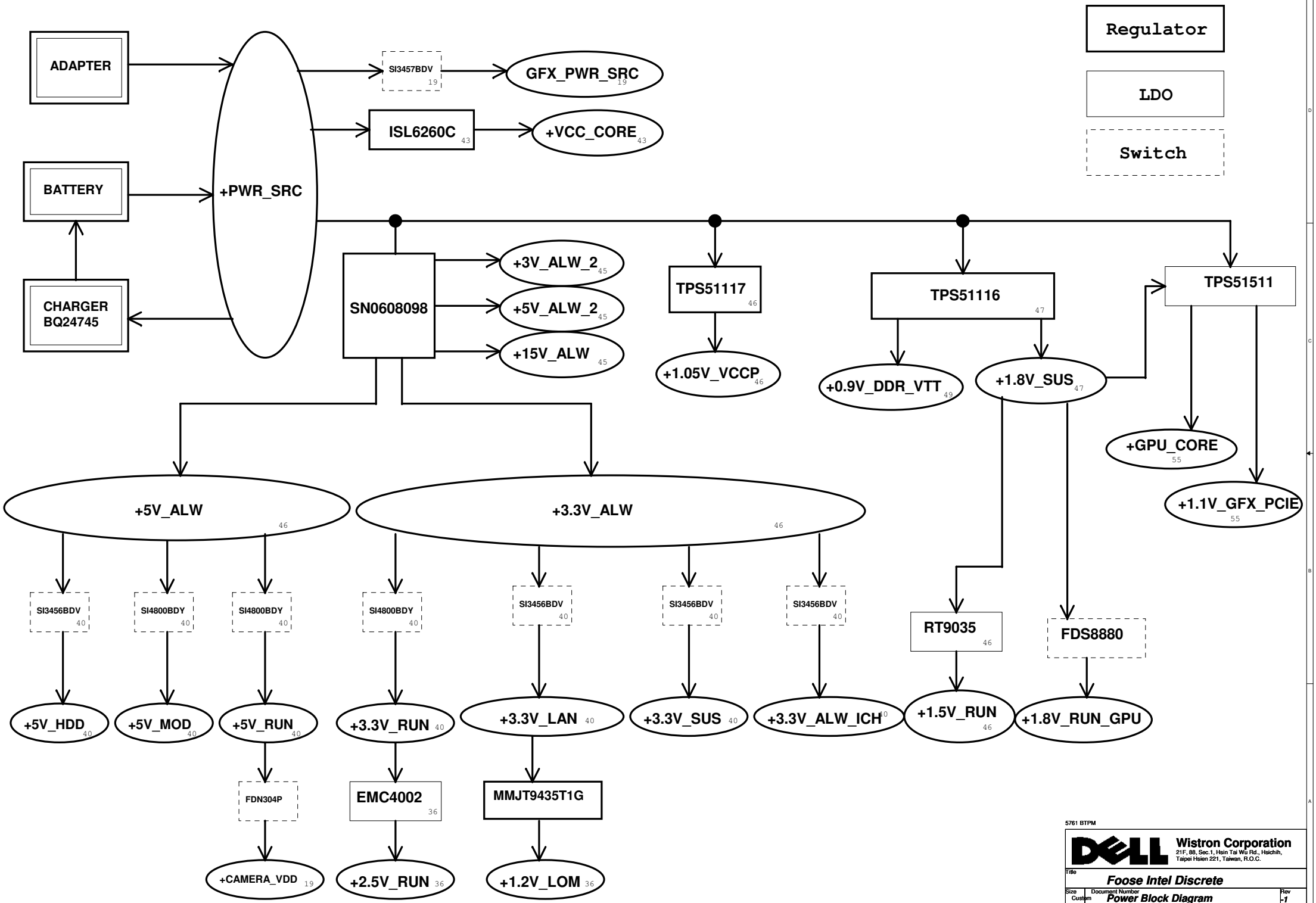

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Size: Custom | Document Number: *Power Block Diagram* | Rev: -1

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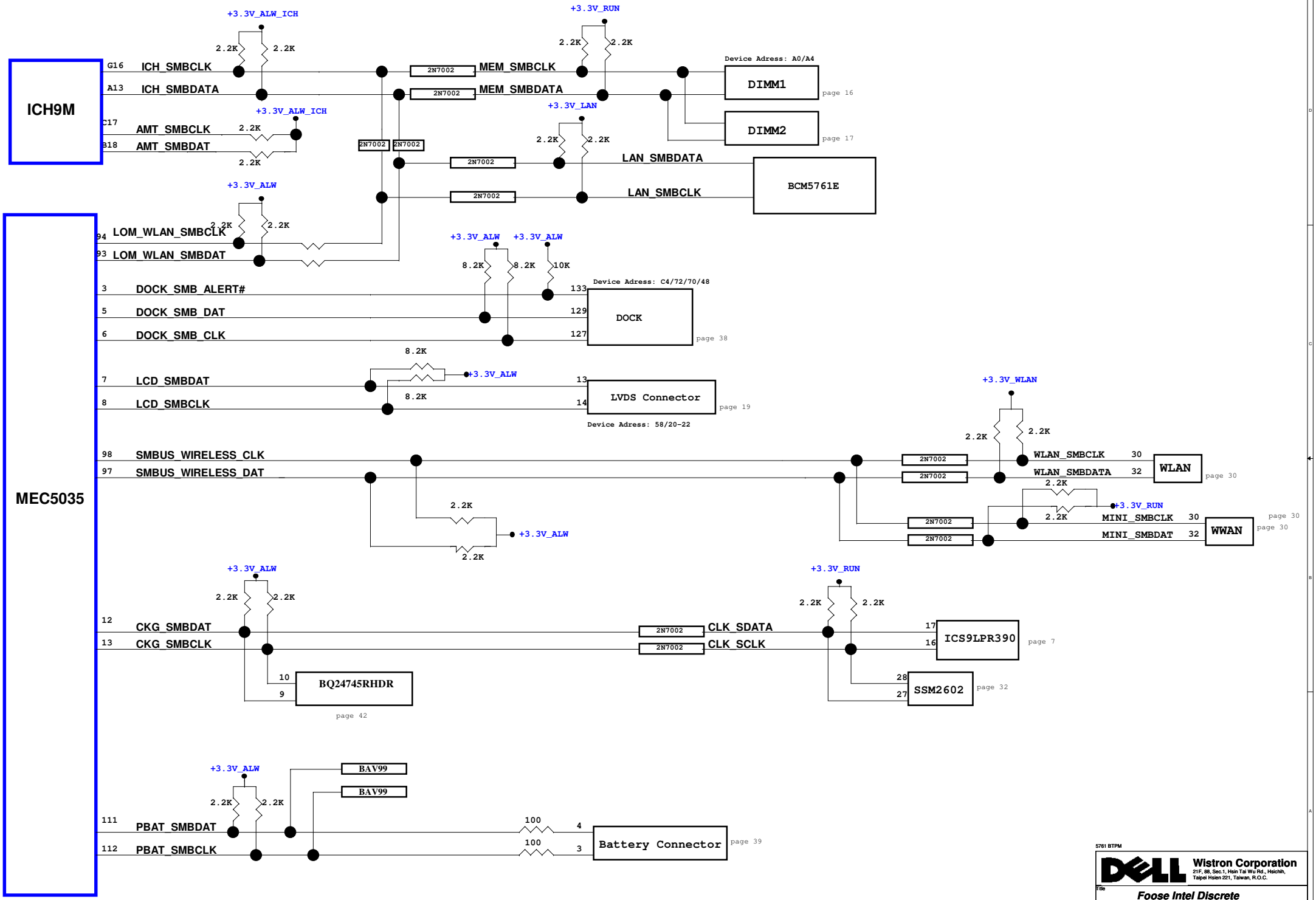
ICH9M
MEC5035
G16 ICH_SMBCLK
A13 ICH_SMBDATA
C17 AMT_SMBCLK
B18 AMT_SMBDAT
+3.3V_ALW_ICH
+3.3V_RUN
+3.3V_LAN
+3.3V_ALW
2.2K
2N7002
MEM_SMBCLK
MEM_SMBDATA
Device Adress: A0/A4
DIMM1
page 16
DIMM2
page 17
LAN_SMBDATA
LAN_SMBCLK
BCM5761E
94 LOM_WLAN_SMBCLK
93 LOM_WLAN_SMBDAT
8.2K
10K
3 DOCK_SMB_ALERT#
5 DOCK_SMB_DAT
6 DOCK_SMB_CLK
Device Adress: C4/72/70/48
133
129
127
DOCK
page 38
7 LCD_SMBDAT
8 LCD_SMBCLK
13
14
LVDS Connector
page 19
Device Adress: 58/20-22
+3.3V_WLAN
98 SMBUS_WIRELESS_CLK
97 SMBUS_WIRELESS_DAT
WLAN_SMBCLK 30
WLAN_SMBDATA 32
WLAN
page 30
MINI_SMBCLK 30
MINI_SMBDAT 32
WWAN
page 30
12 CKG_SMBDAT
13 CKG_SMBCLK
CLK_SDATA
CLK_SCLK
17
16
ICS9LPR390
page 7
10
9
BQ24745RHDR
page 42
28
27
SSM2602
page 32
BAV99
111 PBAT_SMBDAT
112 PBAT_SMBCLK
100
4
3
Battery Connector
page 39
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Document Number
SMBus Block Diagram
Rev -1
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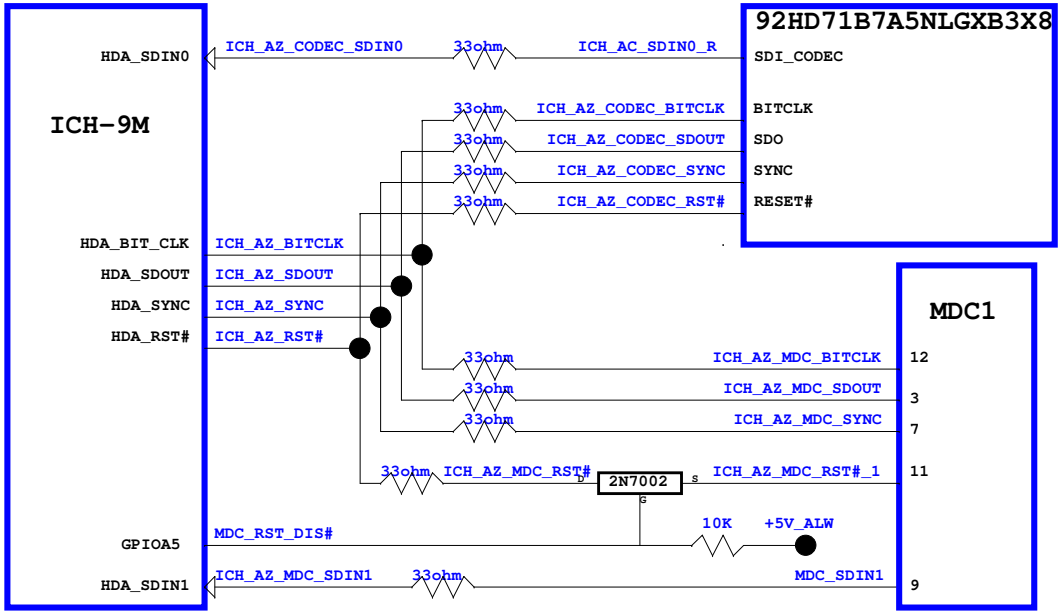
AZALIA BLOCK DIAGRAM



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INTEL ICH9-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit 1 of RPC.PC (Chipset Config Registers: Offset224h).This signal has a weak internal pull-down.
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit 0 of RPC.PC (Chipset Config Registers: Offset 224h)
GNT2# / GPIO53	PCIE Port Config 2 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit 2 of RPC.PC2 (Chipset Config Registers:Offset 0224h) when sampled low.
GPIO20	Reserved	This signal has a weak internal pull-down. NOTE: This signal should not be pulled high
GNT1#/ GPIO51	ESI Strap, Rising Edge of PWROK.	Tying this strap low configures DMI for ESI compatible operation. This signal has a weak internal pull-up. NOTE: ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3# / GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	The signal has a weak internal pull-up. If the signal is sampled low, this indicates that the system is strapped to the "top-block swap" mode (IntelR ICH9 inverts A16 for all cycles targeting BIOS space). The status of this strap is readable via the Top Swap bit (Chipset Config Registers:Offset 3414h:bit 0). Note that software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	This field determines the destination of accesses to the BIOS memory range. Signals have weak internal pull-ups. Also controllable via Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:bit 11).This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	Signal has weak internal pull-up.Sets bit 27 of MPC.LR (Device 28: Function 0: Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	The signal has a weak internal pull-down. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status of this strap is readable via the NO REBOOT bit (Chipset Config Registers:Offset 3410h:bit 5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	See IntelR ICH9 Family XOR Chains In-Circuit Tester Package for functionality information. This signal has a weak internal pull-up. NOTE: This signal should not be pulled low unless using XOR Chain testing.
GPIO33 / HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	This signal has a weak internal pull-up resistor. If sampled low, the Flash Descriptor Security will be overridden. If high, the security measures defined in the Flash Descriptor will be in effect.NOTE: This strap should only be enabled in manufacturing environments.
GPIO49	DMI Termination Voltage Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SPI_MOSI	Integrated TPM Enable Rising Edge of PWROK.	This signal has a weak internal pull-down resistor. When the signal is sampled low the Integrated TPM will be disabled. When the signal is sampled high the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enabled.NOTE: This signal is required to be floating or pulled low for desktop applications.

XOR Chain Entrance Strap

ICH_RSVD tp3	AZ_DOUT_ICH	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIE port cofig bit1

A16 swap override strap

PCI_GNT#3	low = A16 swap override enable
	high = default

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

Enable VccSus1_05,VccSus1_5,VccCL1_5

SM_INTVRMEN	High=Enable	Low=Disable

integrated VccLan1_05VccCL1_05

LAN100_SLP	High=Enable	Low=Disable

No Reboot Strap

SPKR	LOW = Defaule
	High=No Reboot

PCIE Routing

LANE1	MiniCard WWAN
LANE2	MiniCard WLAN
LANE3	R5U241
LANE4	No use
LANE5	GIGA LAN
LANE6	No use

SATA Routing

SATA0	HDD
SATA1	ODD
SATA4	No use
SATA5	Dock eSATA

PCI ROUTING

	IDSEL	INT	REQ	GNT
No use	AD17	1	B C D	1

USB TABLE

USB	
Pair	Device
0	Charge USB (LEFT SIDE TOP)
1	USB1(LEFT SIDE BOTTOM)
2	USB2(RIGHT SIDE TOP)
3	USB3(RIGHT SIDE BOTTOM)
4	WebCAM
5	WWAN
6	Bluetooth
7	R5U241
8	DOCK1
9	DOCK2
10	Biometric
11	BCM5761E

ICH9-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 10K
DPRSLPVR/GPIO16	PULL-DOWN 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LAD[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

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Size: A3 | Document Number: Table of Content | Rev: -1

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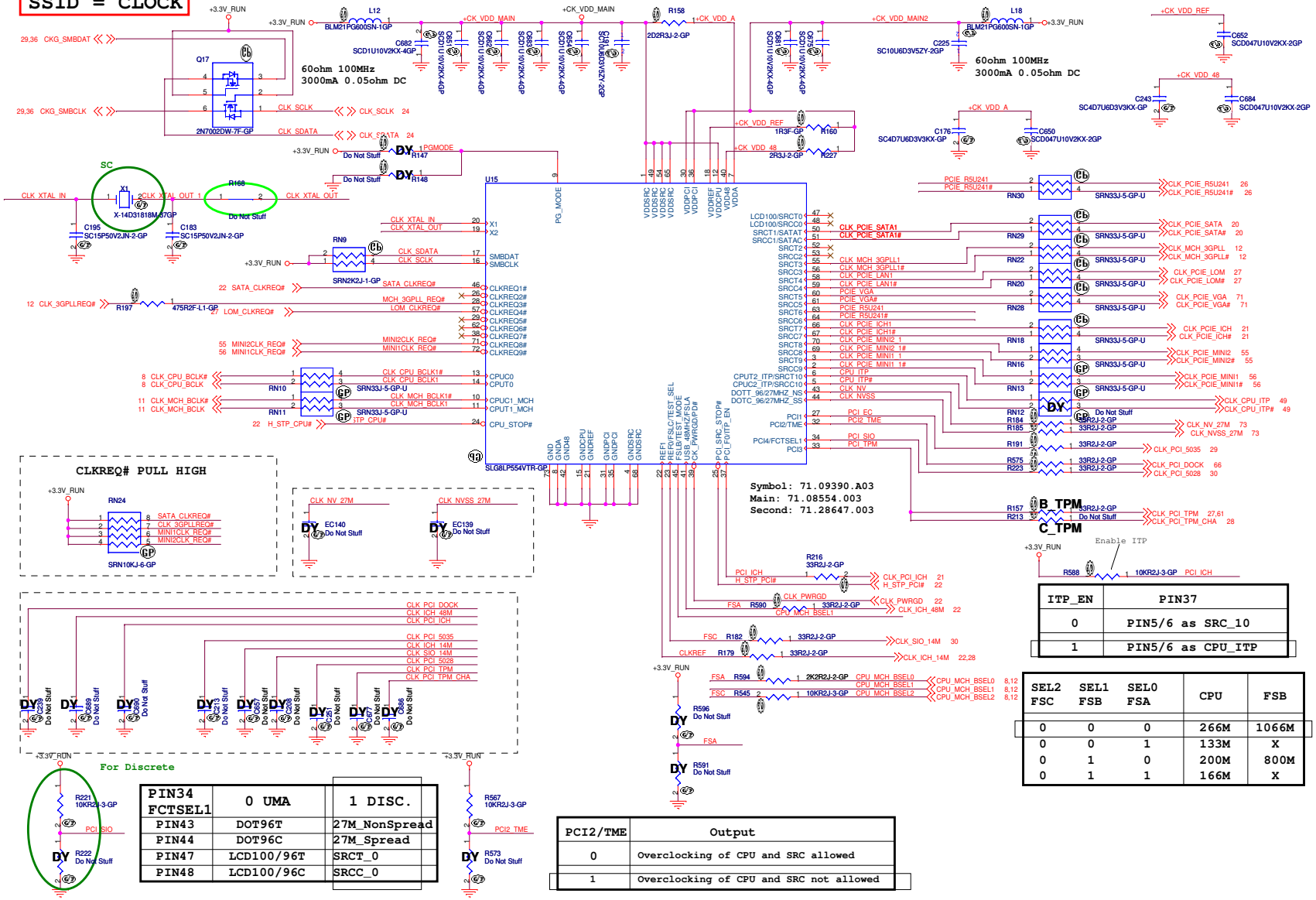
SSID = CLOCK



ITP_EN	PIN37
0	PIN5/6 as SRC_10
1	PIN5/6 as CPU_ITP

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
0	0	0	266M	1066M
0	0	1	133M	X
0	1	0	200M	800M
0	1	1	166M	X

PIN34 FCTSEL1	0 UMA	1 DISC.
PIN43	DOT96T	27M_NonSpread
PIN44	DOT96C	27M_Spread
PIN47	LCD100/96T	SRCT_0
PIN48	LCD100/96C	SRCC_0

PCI2/TME	Output
0	Overclocking of CPU and SRC allowed
1	Overclocking of CPU and SRC not allowed

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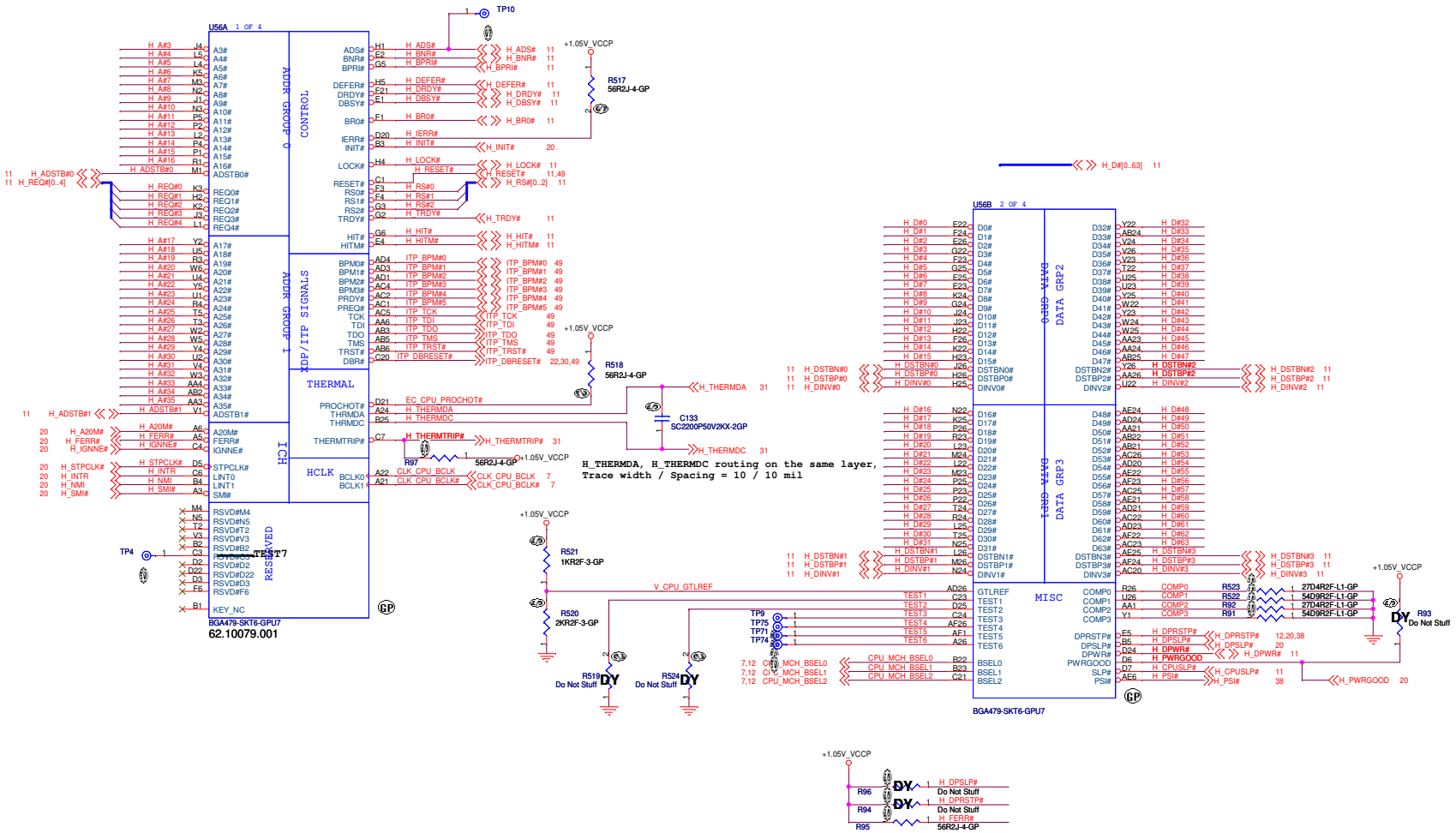
Size: C | Document Number: Clock Generator | Rev: -1

Date: Tuesday, April 07, 2009 | Sheet 7 of 79

SSID = CPU



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Title: ***Foose Intel Discrete***

Size	Document Number	Rev
C	*CPU-FSB(1/2)*	-1

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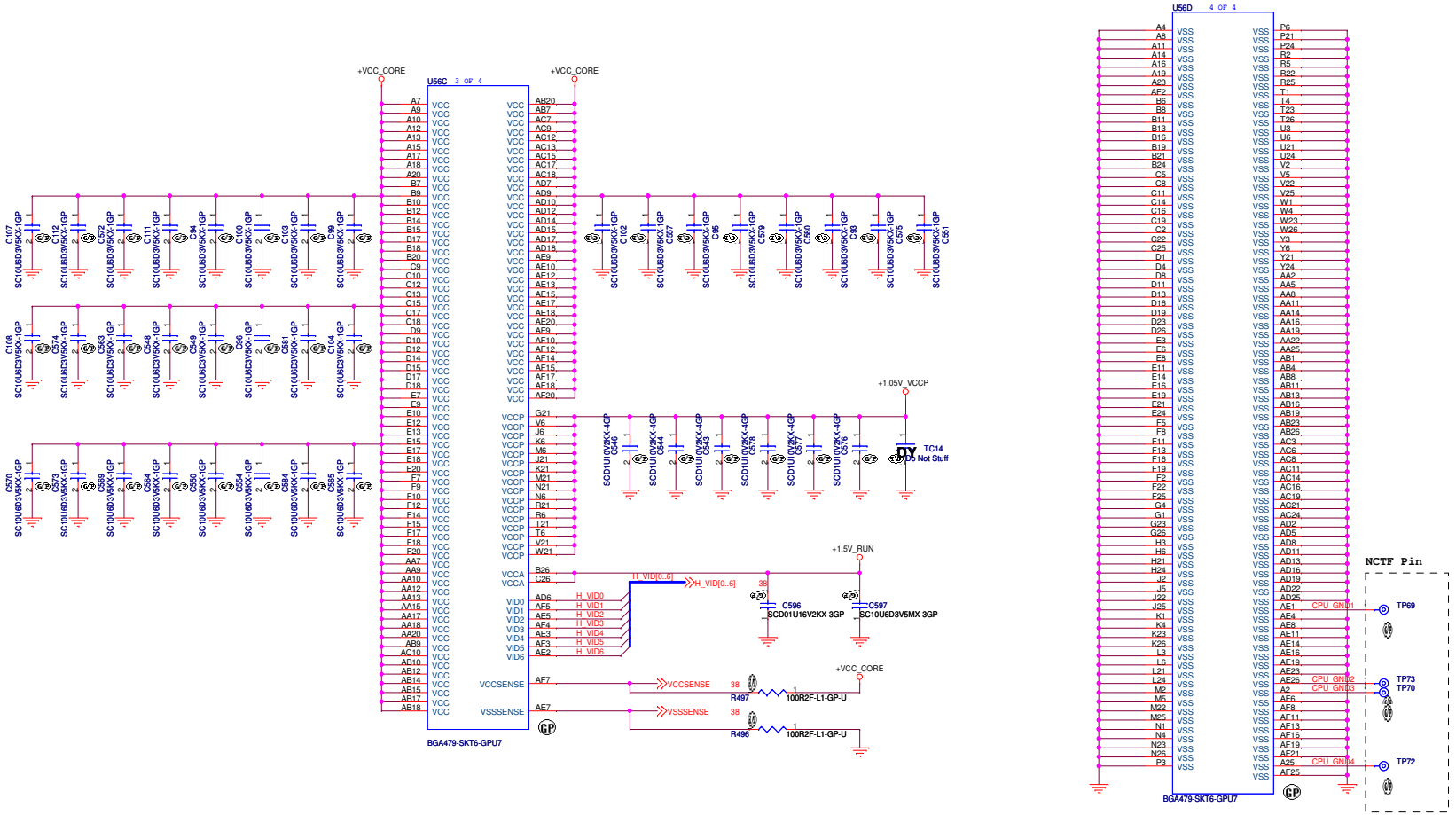
SSID = CPU



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Title		
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Size: C	Document Number: CPU-Power(2/2)	Rev: -1
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Title: Foose Intel Discrete

Size	Document Number	Rev
C	Reserve for Calpella	-1

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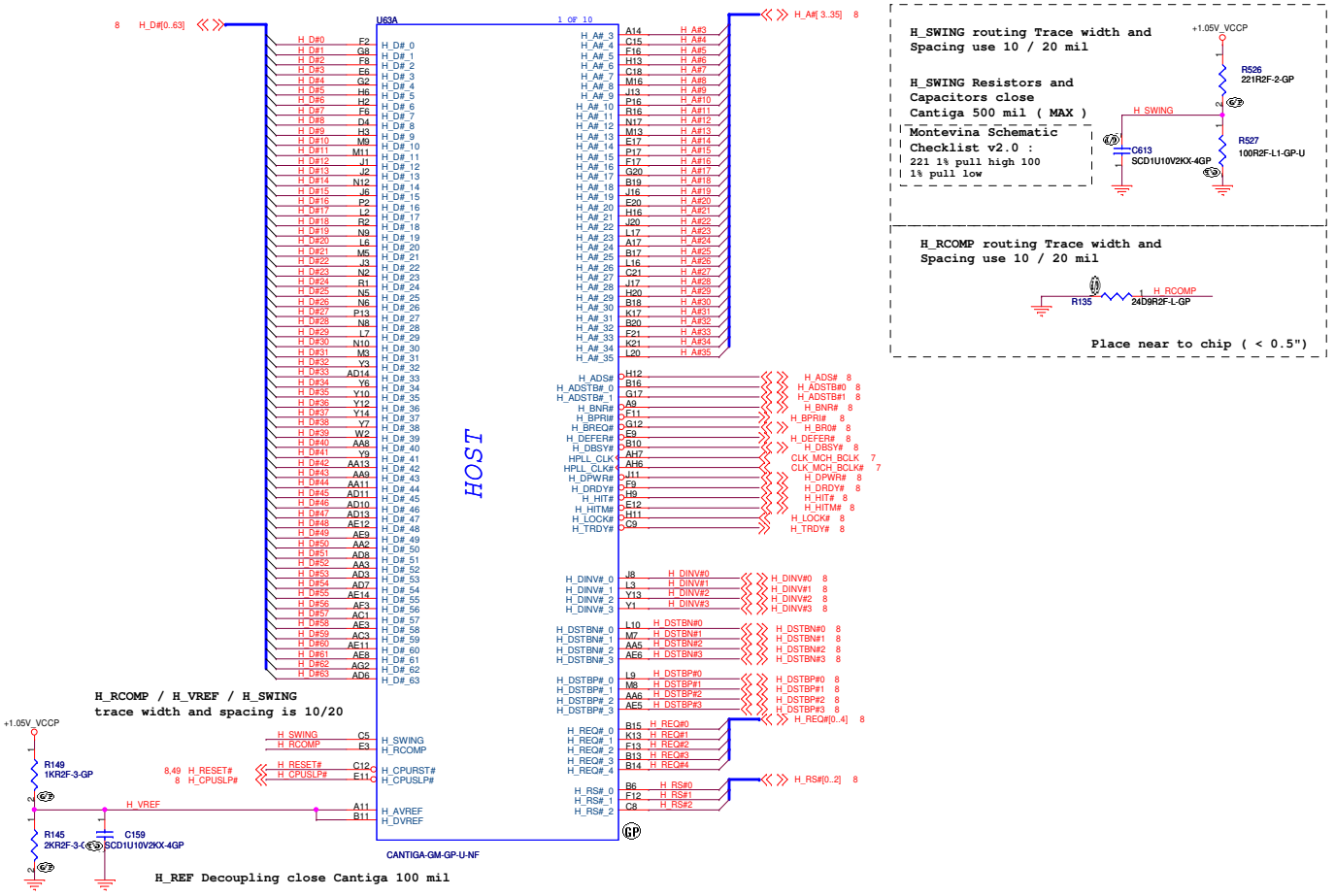
SSID = MCH



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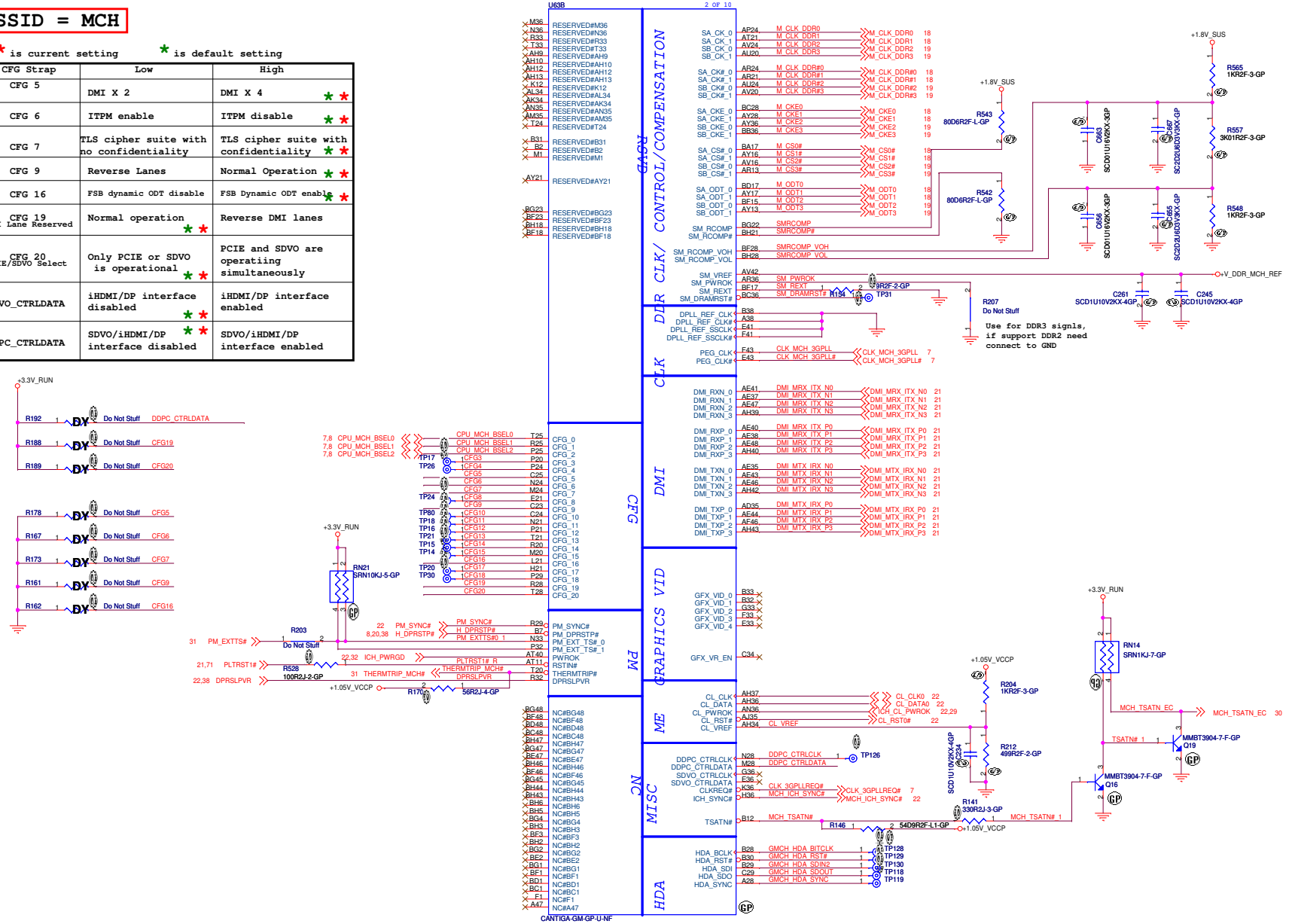
Size	Document Number	Rev
C	*Cantiga-FSB(1/6)*	-1

Date: Tuesday, April 07, 2009 Sheet 11 of 79

SSID = MCH

* is current setting * is default setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 * *
CFG 6	ITPM enable	ITPM disable * *
CFG 7	TLS cipher suite with no confidentiality	TLS cipher suite with confidentiality * *
CFG 9	Reverse Lanes	Normal Operation * *
CFG 16	FSB dynamic ODT disable	FSB Dynamic ODT enable * *
CFG 19 DMI Lane Reserved	Normal operation * *	Reverse DMI lanes
CFG 20 PCIE/SDVO Select	Only PCIE or SDVO is operational * *	PCIE and SDVO are operatiing simultaneously
SDVO_CTRLDATA	iHDMI/DP interface disabled * *	iHDMI/DP interface enabled
DDPC_CTRLDATA	SDVO/iHDMI/DP interface disabled * *	SDVO/iHDMI/DP interface enabled



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Size	Document Number	Rev
C	Cantiga-DMI/CFG(2/6)	-1

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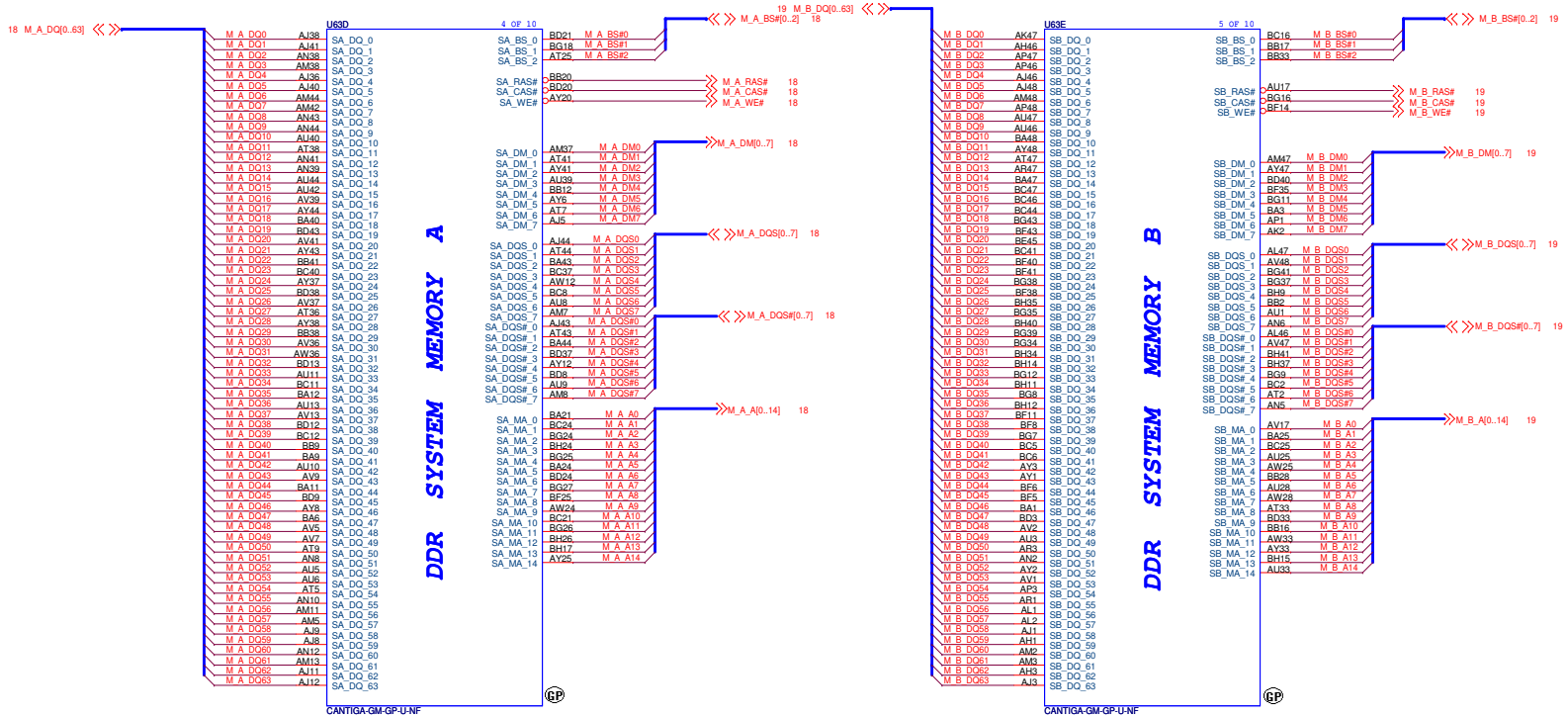
SSID = MCH



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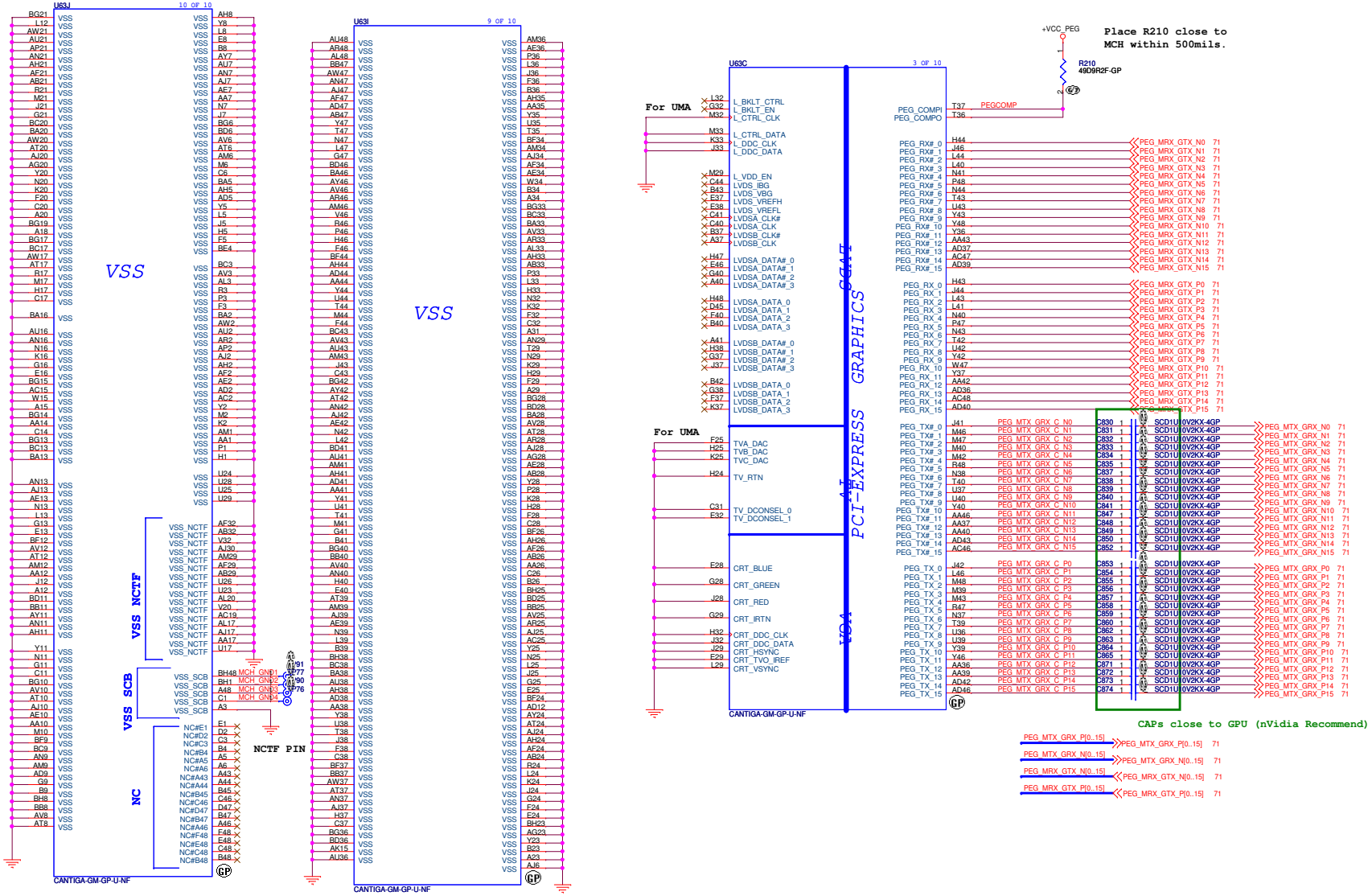
SSID = MCH



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Title: Foose Intel Discrete		
Size: C	Document Number: Cantiga-GND/LVDS/VGA(4/6)	Rev: -1
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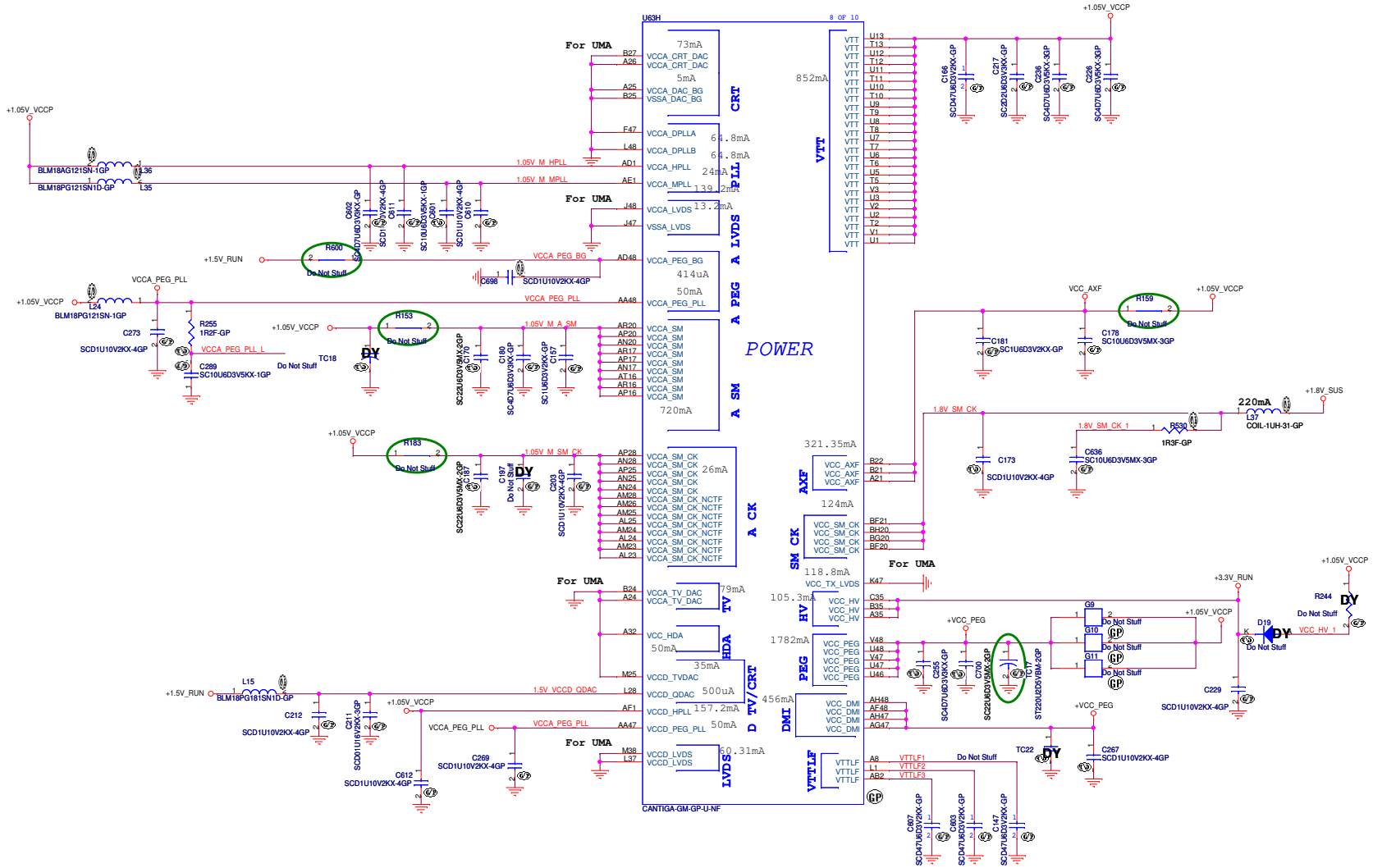
SSID = MCH



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Size	Document Number	Rev
C	*Cantiga-Power/Filter(5/6)*	-1

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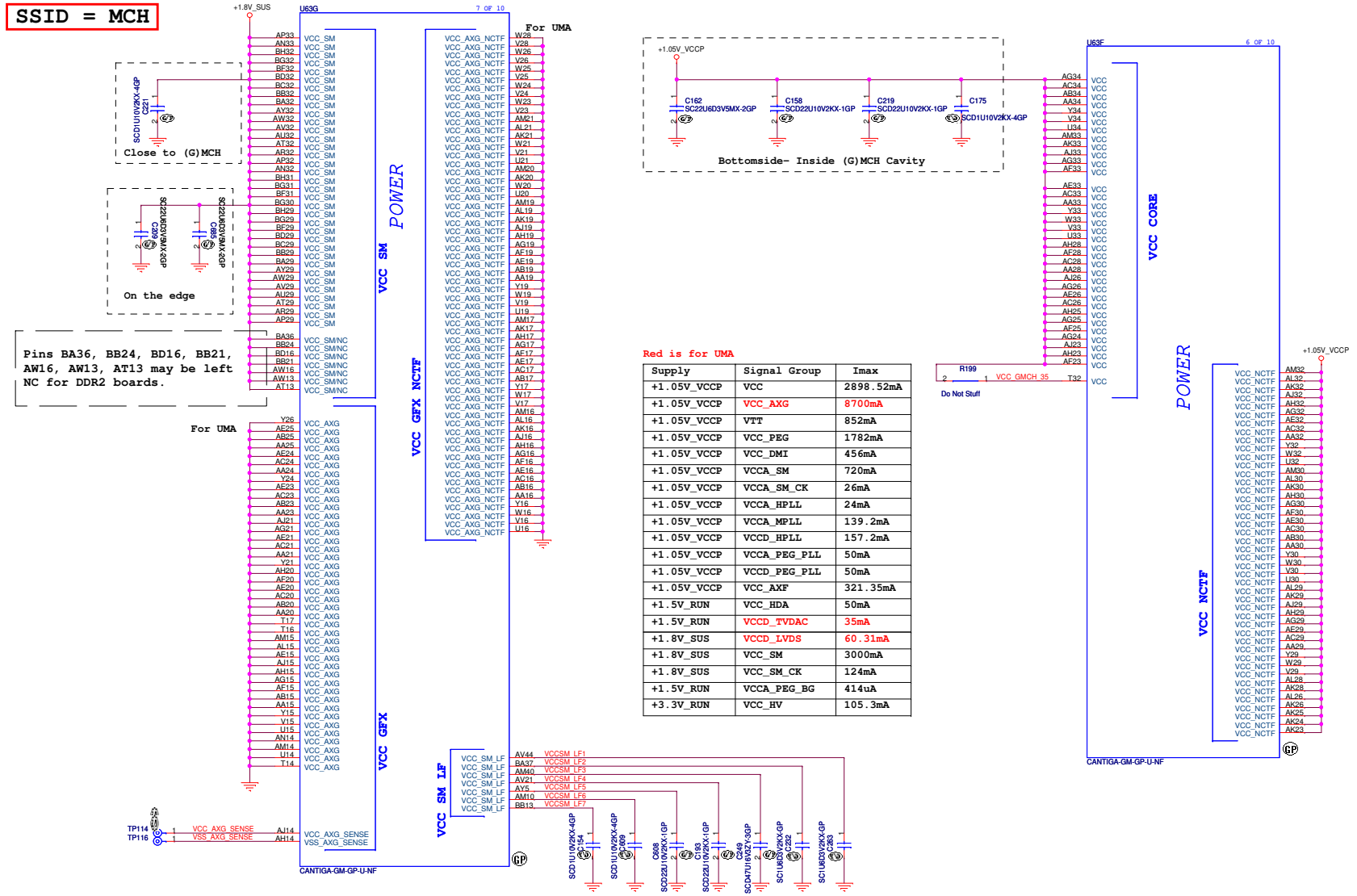
SSID = MCH



Red is for UMA

Supply	Signal Group	Imax
+1.05V_VCCP	VCC	2898.52mA
+1.05V_VCCP	VCC_AXG	8700mA
+1.05V_VCCP	VTT	852mA
+1.05V_VCCP	VCC_PEG	1782mA
+1.05V_VCCP	VCC_DMI	456mA
+1.05V_VCCP	VCCA_SM	720mA
+1.05V_VCCP	VCCA_SM_CK	26mA
+1.05V_VCCP	VCCA_HPLL	24mA
+1.05V_VCCP	VCCA_MPLL	139.2mA
+1.05V_VCCP	VCCD_HPLL	157.2mA
+1.05V_VCCP	VCCA_PEG_PLL	50mA
+1.05V_VCCP	VCCD_PEG_PLL	50mA
+1.05V_VCCP	VCC_AXF	321.35mA
+1.5V_RUN	VCC_HDA	50mA
+1.5V_RUN	VCCD_TVDAC	35mA
+1.8V_SUS	VCCD_LVDS	60.31mA
+1.8V_SUS	VCC_SM	3000mA
+1.8V_SUS	VCC_SM_CK	124mA
+1.5V_RUN	VCCA_PEG_BG	414uA
+3.3V_RUN	VCC_HV	105.3mA

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Size: C | Document Number: *Cantiga-Power(6/7)* | Rev: -1

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Size	Document Number	Rev
C	Reserve for Calpella	-1

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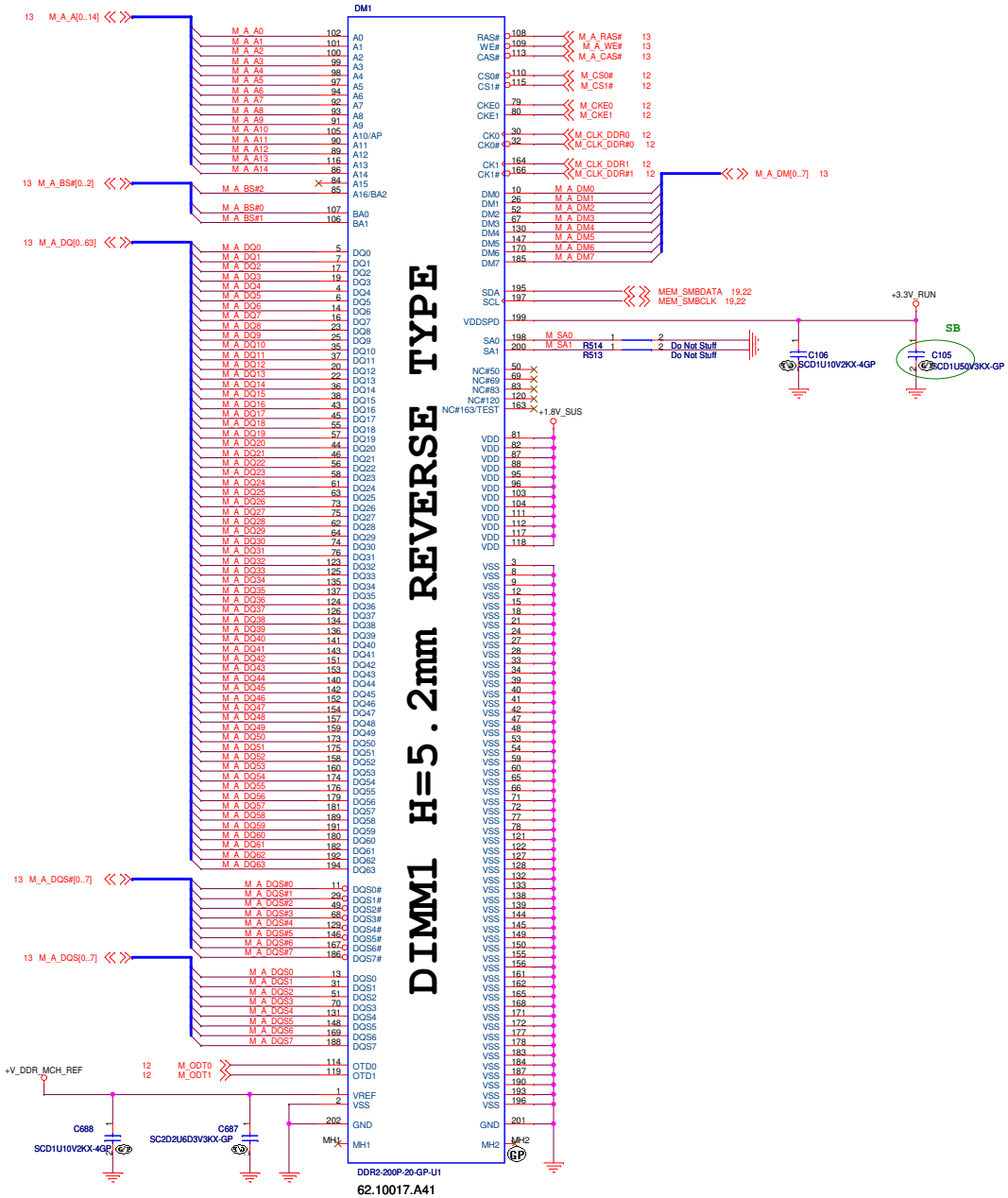
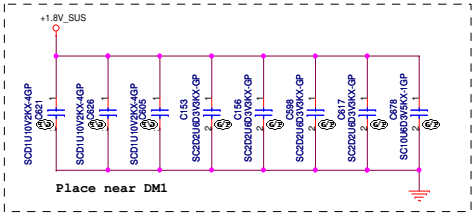
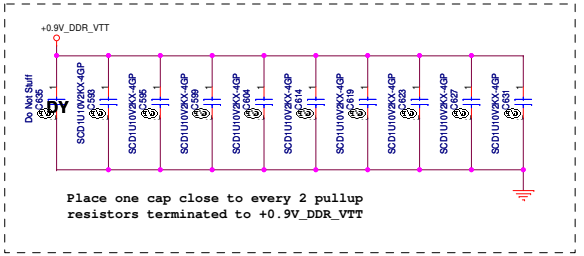
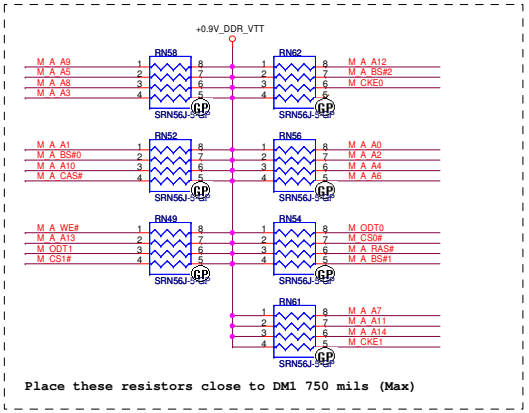
SSID = MEMORY

DIMM1 H=5.2mm REVERSE TYPE









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Title: Foose Intel Discrete

Size	Document Number	Rev
C	DDRII-SODIMM Slot1	-1

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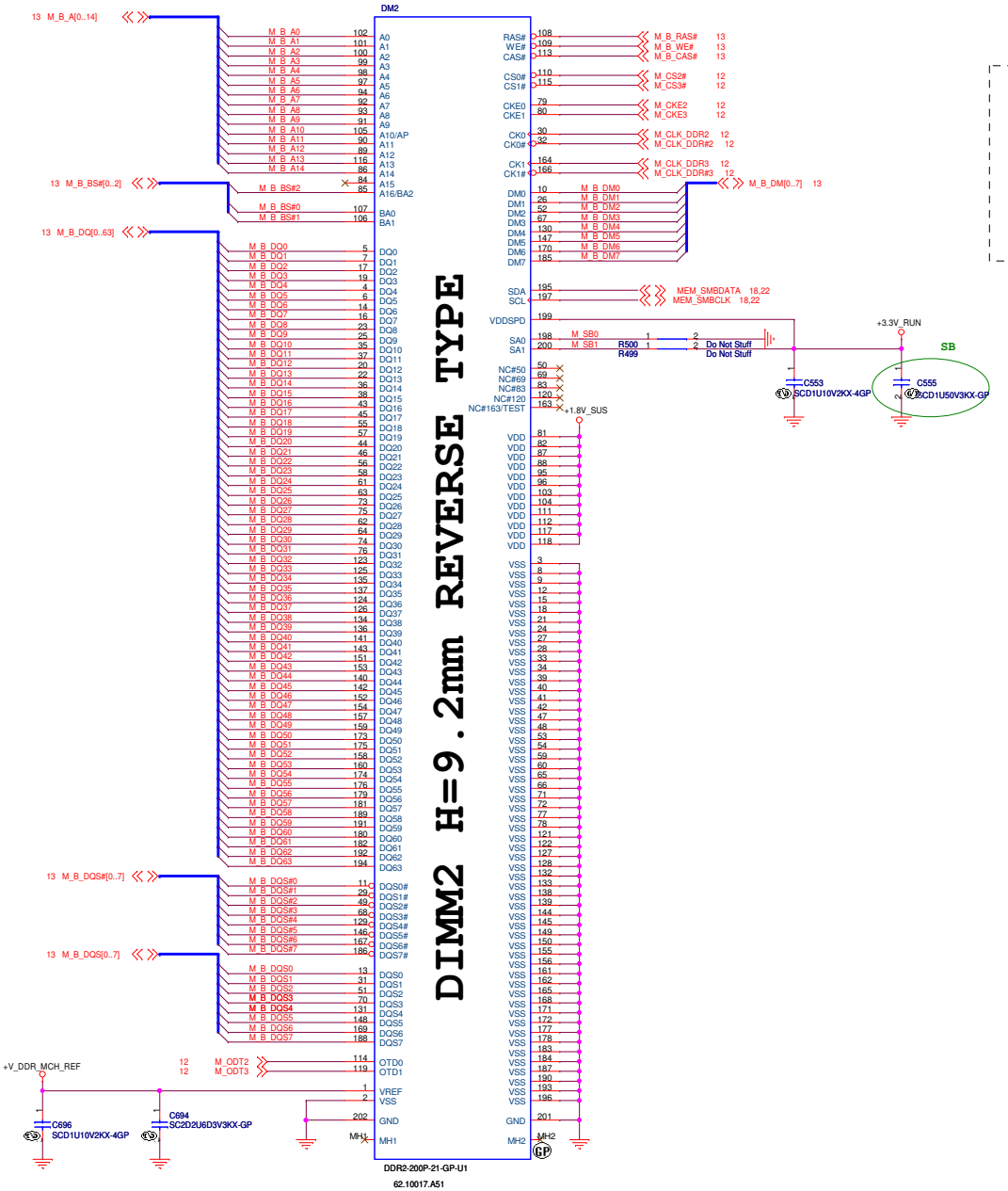
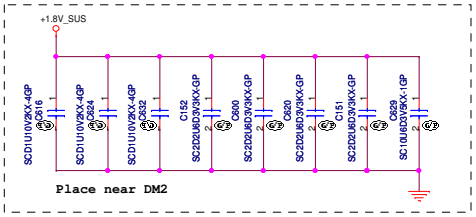
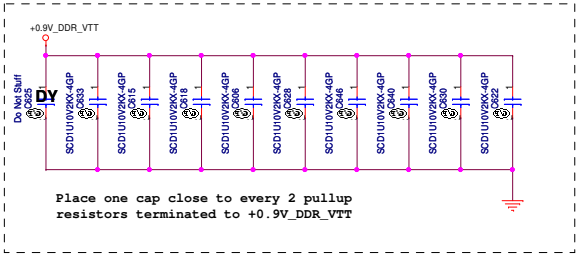
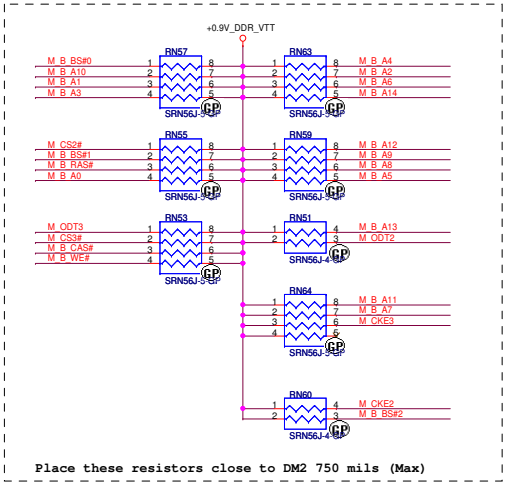
SSID = MEMORY

DIMM2 H=9.2mm REVERSE TYPE









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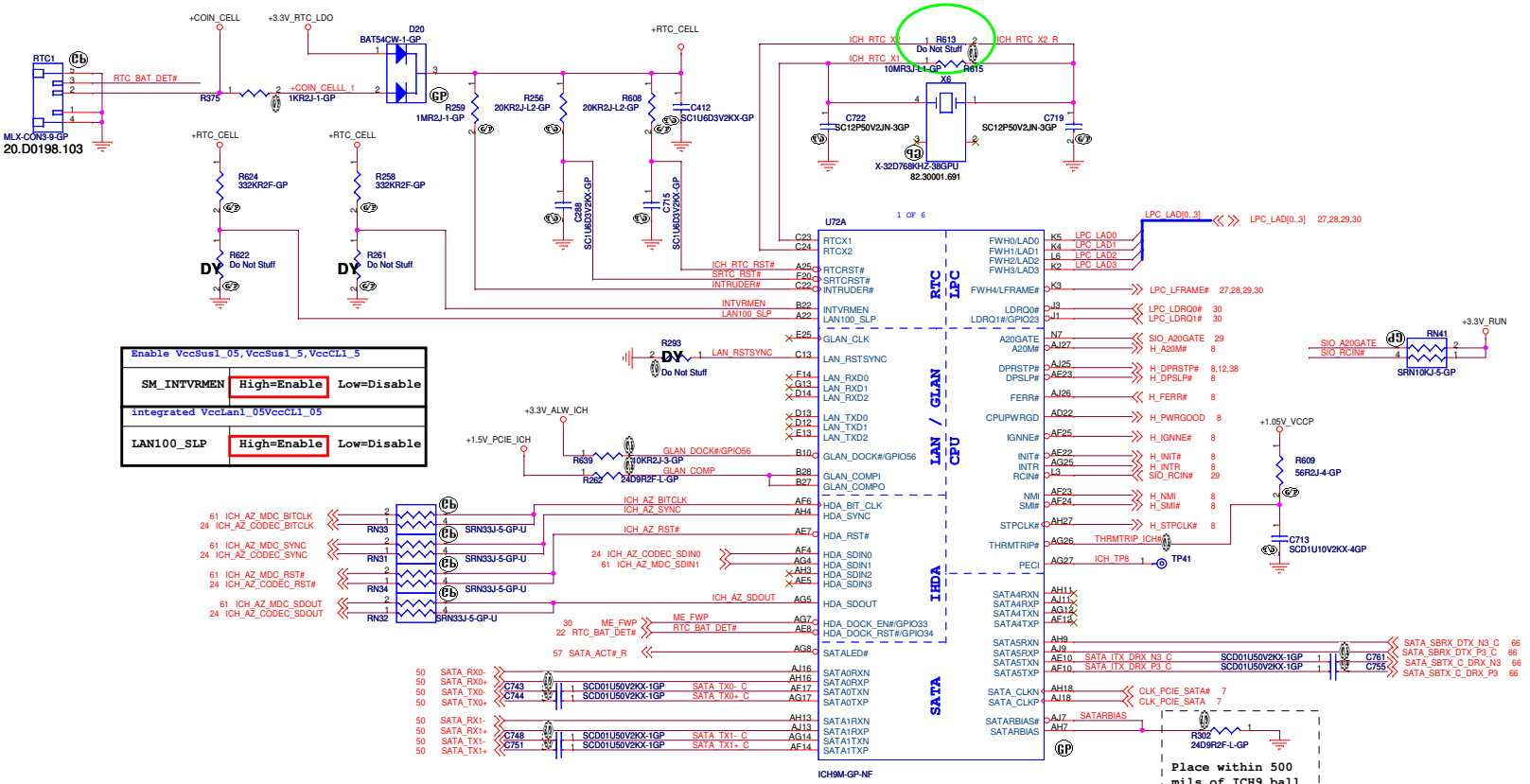
Title: *Foose Intel Discrete*

Size: C | Document Number: DDRII-SODIMM Slot2 | Rev: -1

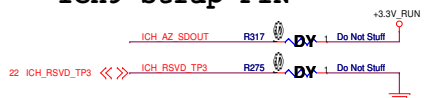
Date: Tuesday, April 07, 2009 | Sheet 19 of 79

SSID = ICH



Enable VccSus1_05,VccSus1_5,VccCL1_5		
SM_INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

ICH9-Strap PIN



XOR Chain Entrance Strap		
ICH_RSVD tp3	AZ_DOUT_ICH	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIE port cofig bit1

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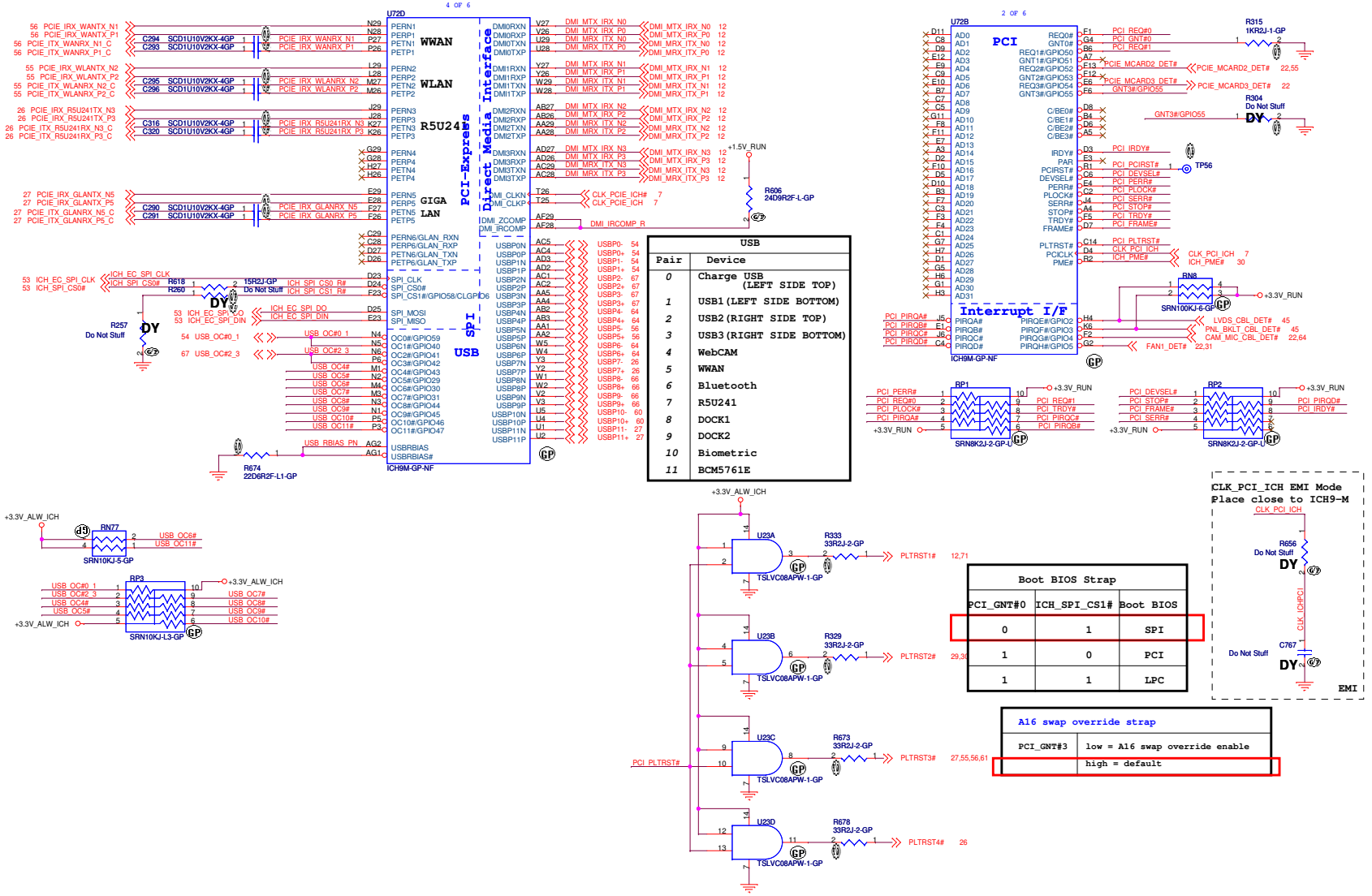
Title: *Foose Intel Discrete*

Size: C | Document Number: *ICH9-LAN/HDA/SATA/LPC(1/4)* | Rev: -1

Date: Tuesday, April 07, 2009 | Sheet 20 of 79

SSID = ICH



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Title: *Foose Intel Discrete*

Size	Document Number	Rev
C	*ICH9-PCI/PCIE/DMI/USB(2/4)*	-1

Date: Tuesday, April 07, 2009 Sheet 21 of 79

SSID = ICH

CLK_ICH_48M and CLK_ICH_14M EMI Mode
Place close to ICH8-M

EMI

CTPM and Disable BTPM

B_TPM

C_TPM

TPM_ID	ID0=0	ID0=1
ID1=0	C_TPM	RSVD
ID1=1	NONE	B_TPM

R626 need remove manually if use CTPM

No Reboot Strap	
SPKR	LOW = Defaule
	High=No Reboot

Option to " Disable " clkrun. Pulling it down will keep the clks running.

ICH9M-GP-NF

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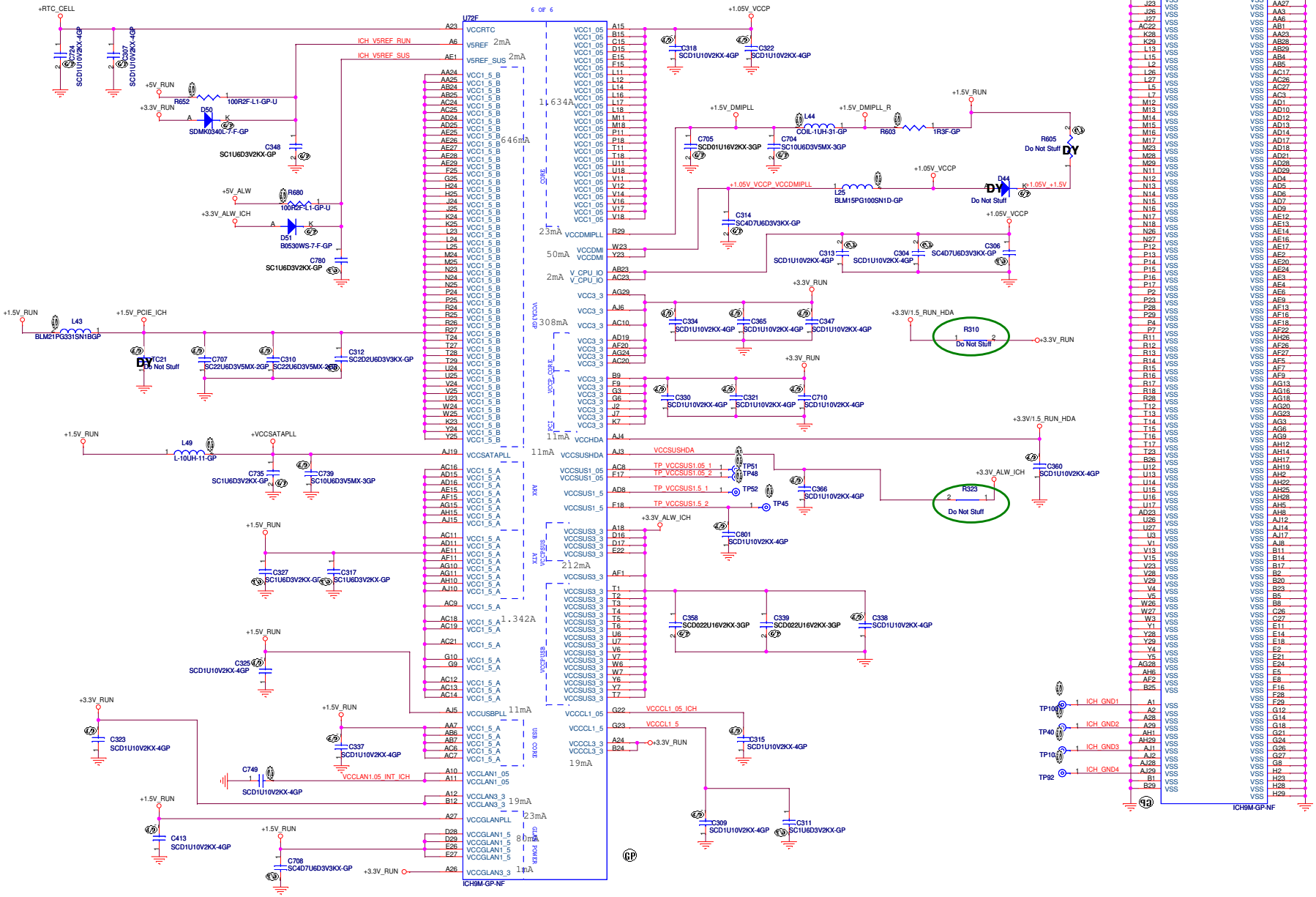
Title: Foose Intel Discrete

Size: C | Document Number: ICH9-CL/PM/GPIO(3/4) | Rev: -1

Date: Tuesday, April 07, 2009 | Sheet 22 of 79

SSID = ICH



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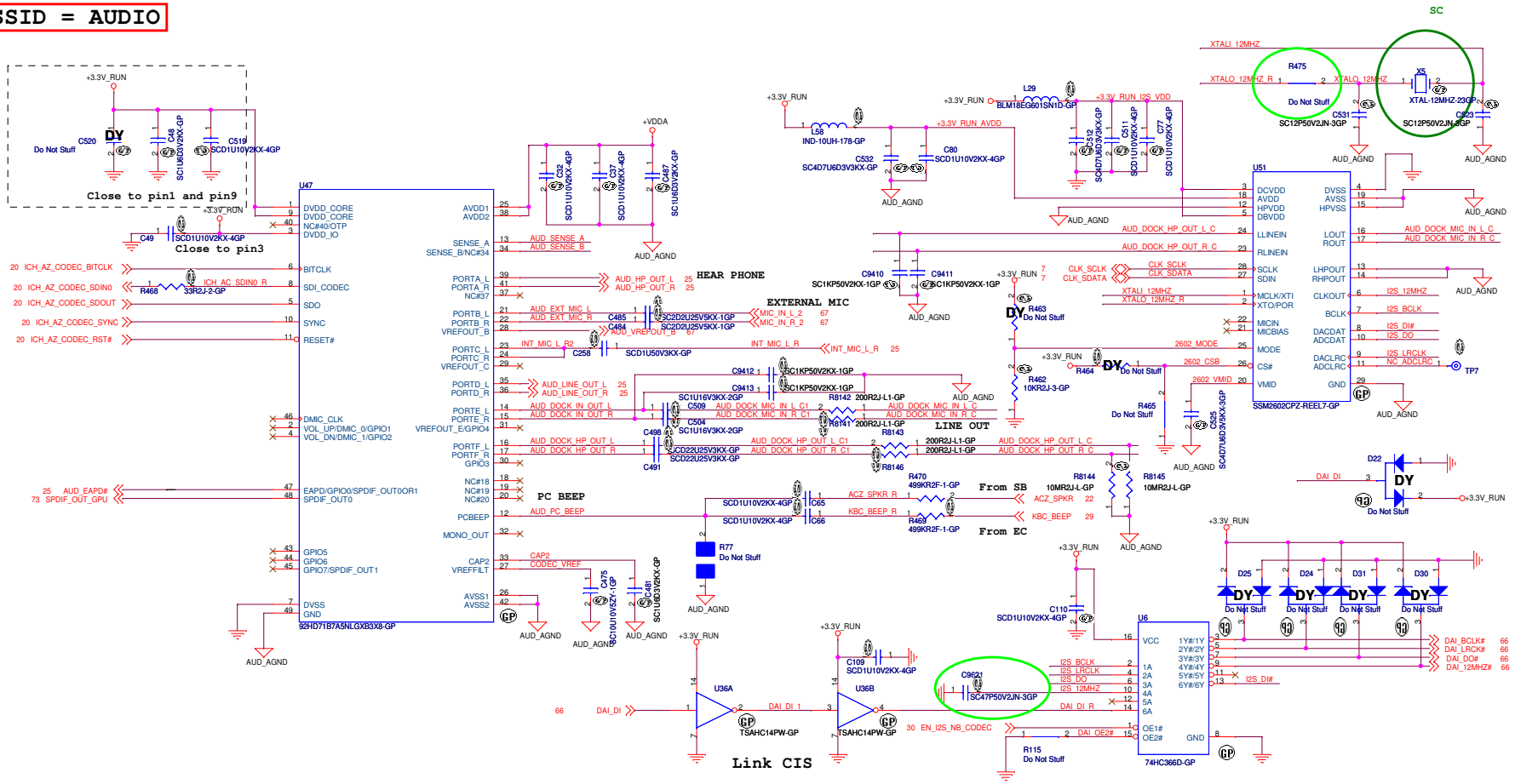
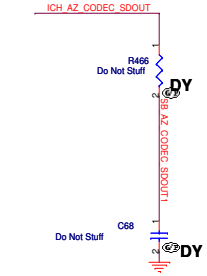
Title: Foose Intel Discrete

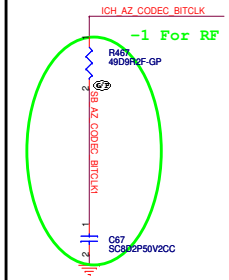
Size	Document Number	Rev
C	ICH9-POWER&GND(4/4)	-1

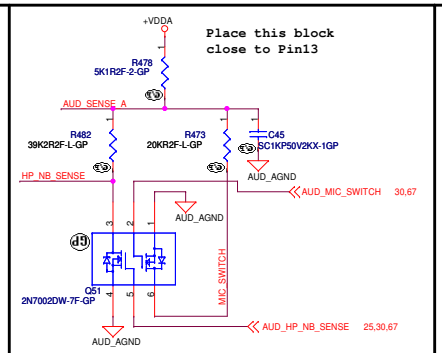
Date: Tuesday, April 07, 2009 Sheet 23 of 79

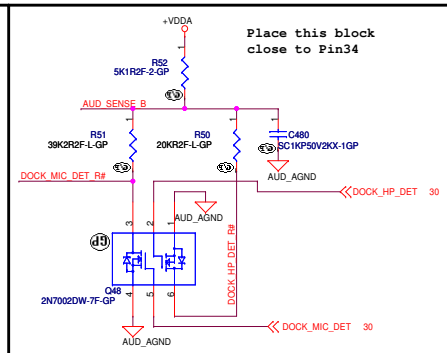
SSID = AUDIO











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Title: *Foose Intel Discrete*

Size	Document Number	Rev
C	*Audio Codec-92HD71B7*	-1

Date: Wednesday, April 08, 2009 Sheet 24 of 79

SSID = AUDIO

Symbol: 74.06040.013
Main: 74.09789.B13
Second: 74.06040.013

60ohm 100MHz
3000mA 0.05ohm DC

Close to Pin8

close to Pin18

Close to Pin9

1st TPA6040A:74.06040.013
2nd MAX9789C:74.09789.B13

NOTE: For MAX9789C
No-stuff R479,C537,C47
stuff R480,R493,R454

GAIN SETTING

GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

AND Gate for HP Mute Function

Signal inverter for speaker shutdown

From EC

From CODEC

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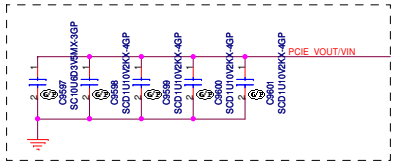
Title: Foose Intel Discrete

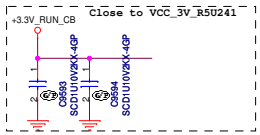
Size: C | Document Number: Audio AMP-MAX9789C | Rev: -1

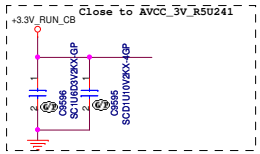
Date: Tuesday, April 07, 2009 | Sheet 25 of 79

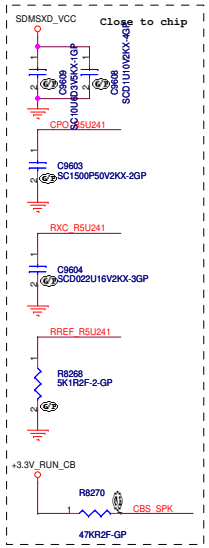
SSID = 1394

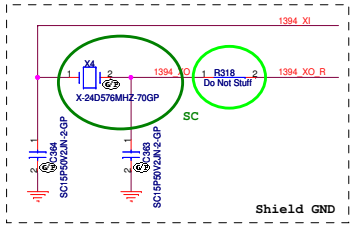
CAPs close to chip
SC: Change 0.01uF to 0.1uF for ES2









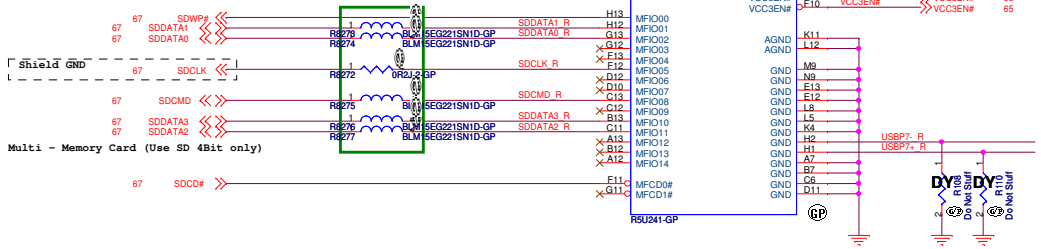


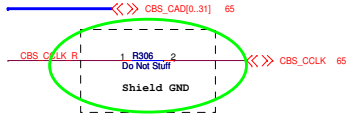
Xtal for XO/XI as close as possible to R5U241

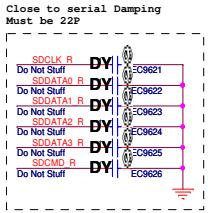
SDMSXD_VCC trace = 40mil

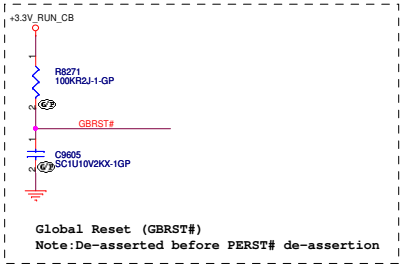
SC: For SD card issue

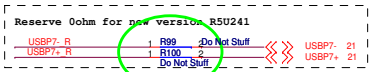
Multi - Memory Card (Use SD 4Bit only)











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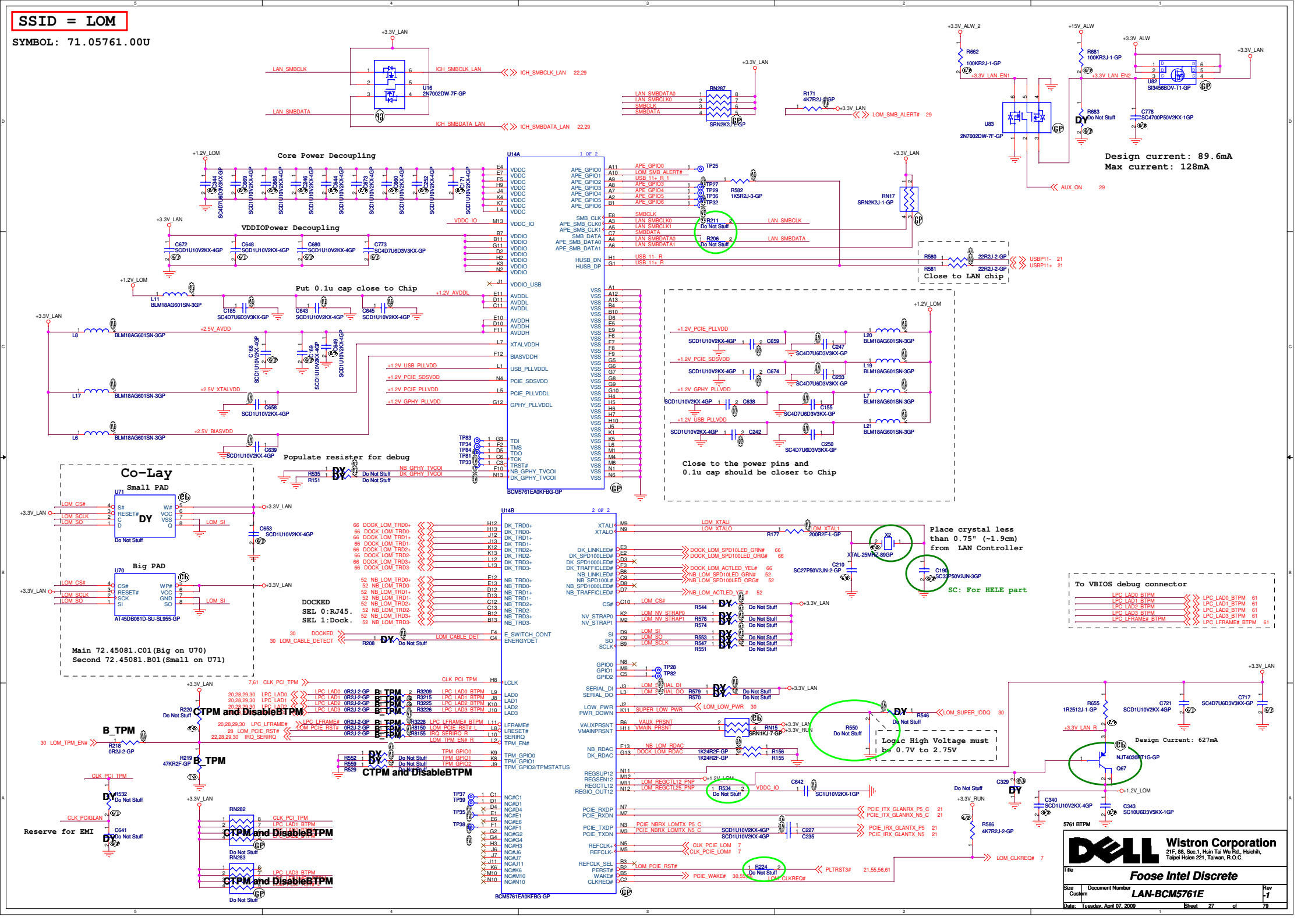
Title: Foose Intel Discrete

Size: C | Document Number: Card Reader-R5U241 | Rev: -1

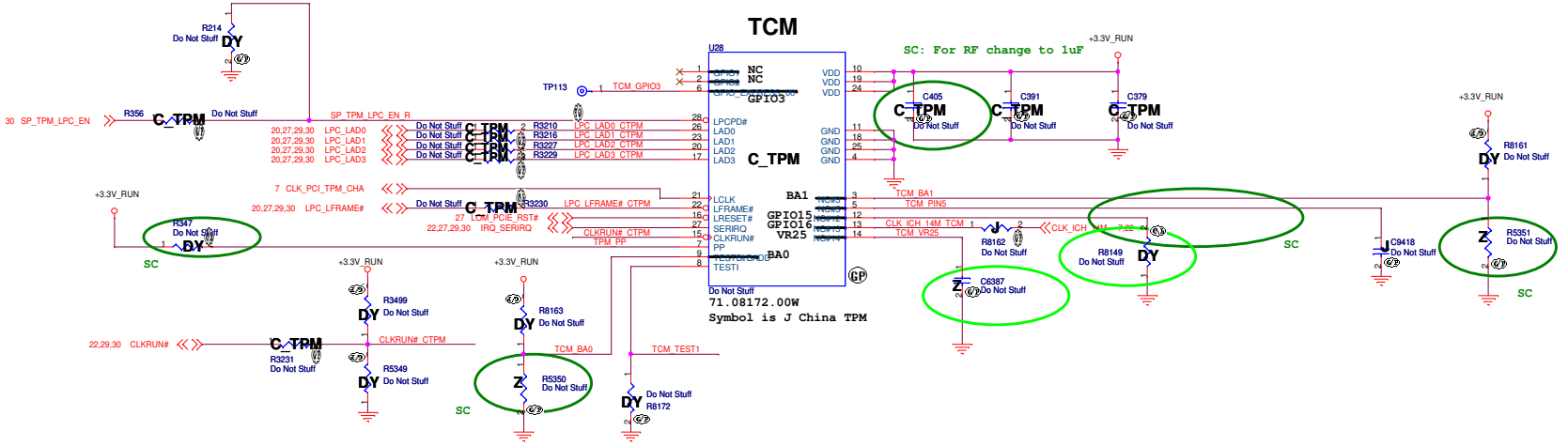
Date: Tuesday, April 07, 2009 | Sheet 26 of 79

SSID = LOM

SYMBOL: 71.05761.00U



SSID = TCM



Z

Base Address	BA1 PIN3	BA0 PIN9
EE/EF	0	0
7E/7F	0	1
2E/2F	1	0
4E/4F	1	1

Default EE/EF as Amy recommended

J

	1(default)	0
PIN12	FLASH	SRAM

J has internal PU with PIN12.

J

Status	PIN8	PIN9
Normal mode	0	X
Jtag mode	1	0
Normal mode	1	1

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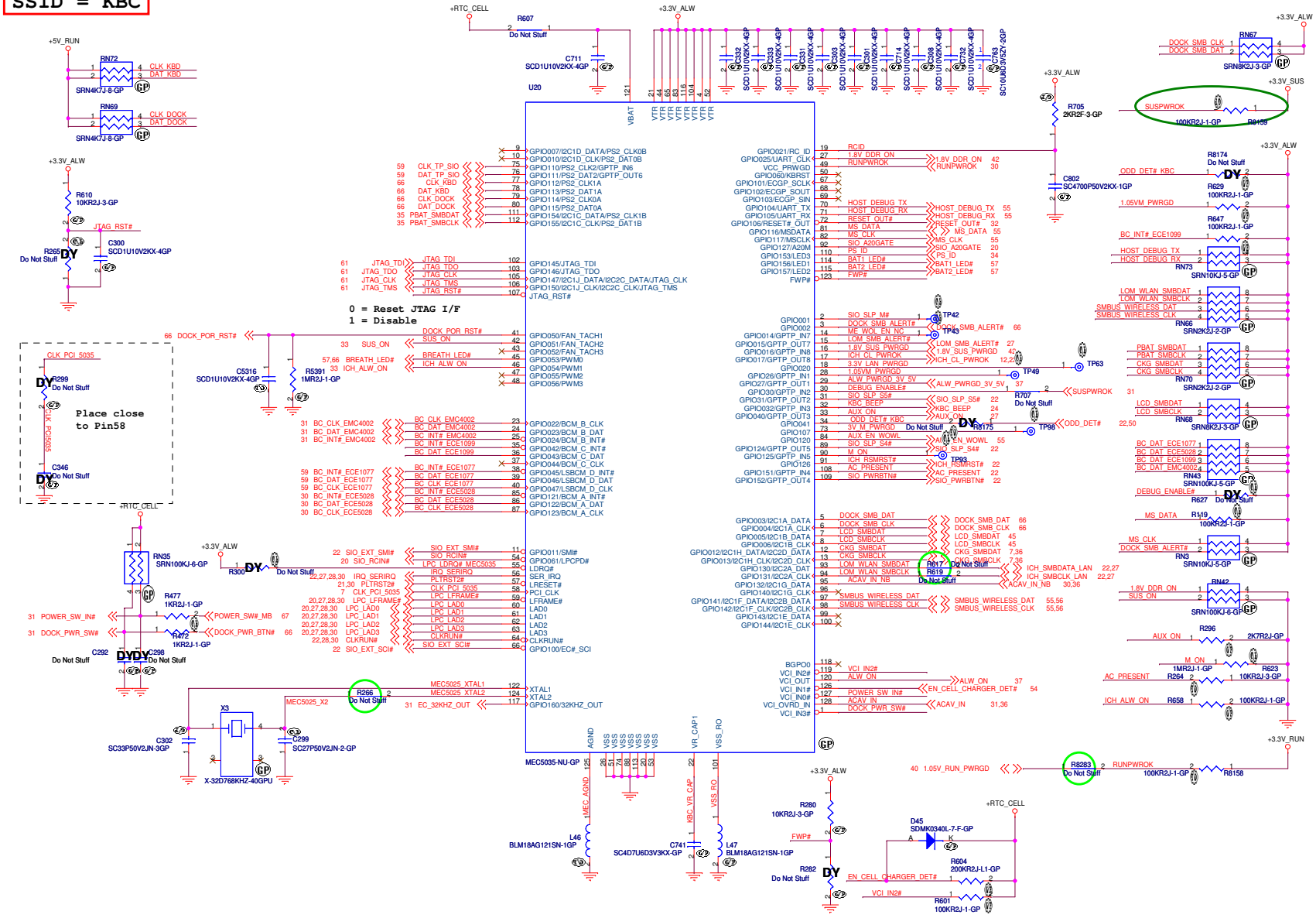
Title: *Foose Intel Discrete*

Size: C | Document Number: *TCM* | Rev: -1

Date: Tuesday, April 07, 2009 | Sheet 28 of 79

SSID = KBC



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Title: ***Foose Intel Discrete***

Size	Document Number	Rev
C	KBC-MEC5035	-1

Date: Tuesday, April 07, 2009 Sheet 29 of 79

SSID = KBC

SC: For RF

Wireless Switch

Board ID

VGA IDENTITY
1= Discrete GFX
0=UMA

Place close to Pin56

Place close to Pin64

BID2	BID1	BID0	REV
0	0	0	X00
0	0	1	X01
0	1	0	X02
0	1	1	A00

CHIPSET_ID1	CHIPSET_ID0	NOTE
0	0	Intel CPU and Intel chipset
0	1	AMD CPU and AMD chipset

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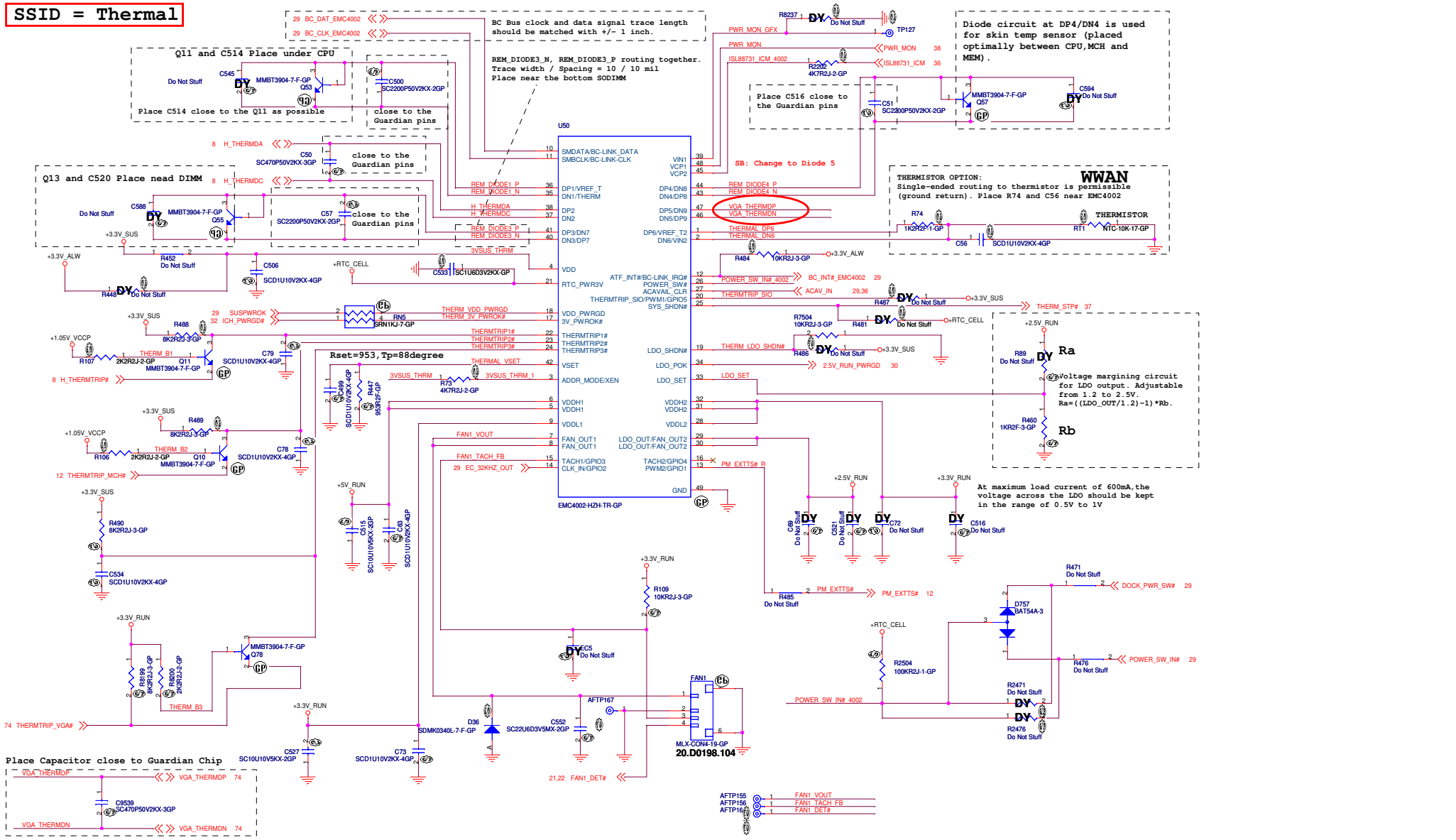
Title: Foose Intel Discrete

Size: C | Document Number: SIO-ECE5028 | Rev: -1

Date: Tuesday, April 07, 2009 | Sheet 30 of 79

SSID = Thermal



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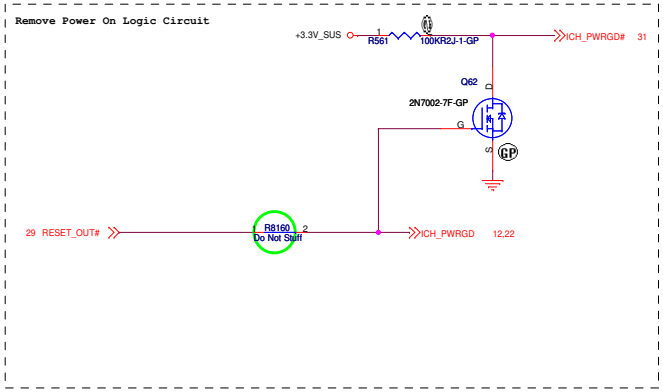
Title: Foose Intel Discrete

Size	Document Number	Rev
C	Thermal/FAN-EMC4002	-1

Date: Tuesday, April 07, 2009 Sheet 31 of 79

SSID = Reset.Suspend



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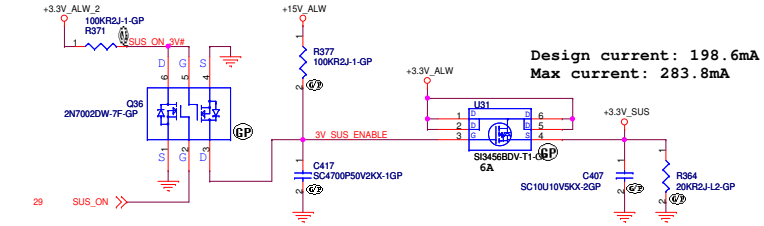
Title: *Foose Intel Discrete*

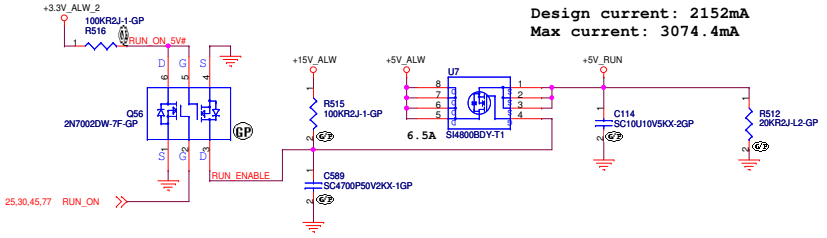
Size	Document Number	Rev
C	*Power On Logic*	-1

Date: Tuesday, April 07, 2009 Sheet 32 of 79

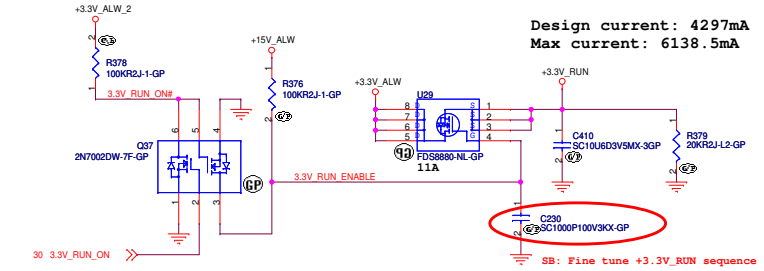
SSID = Reset.Suspend



Design current: 198.6mA
Max current: 283.8mA

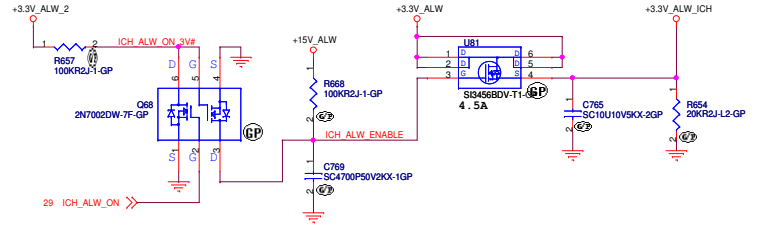


Design current: 2152mA
Max current: 3074.4mA



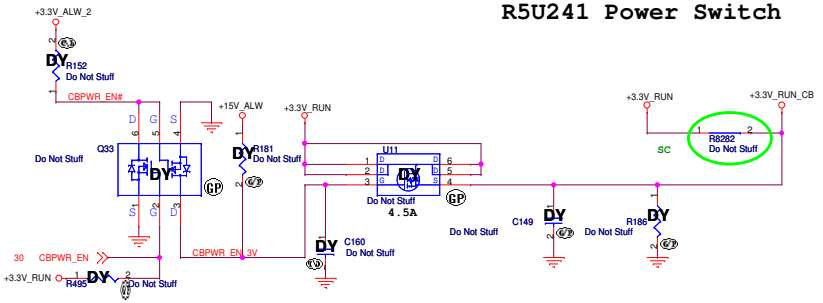
Design current: 4297mA
Max current: 6138.5mA

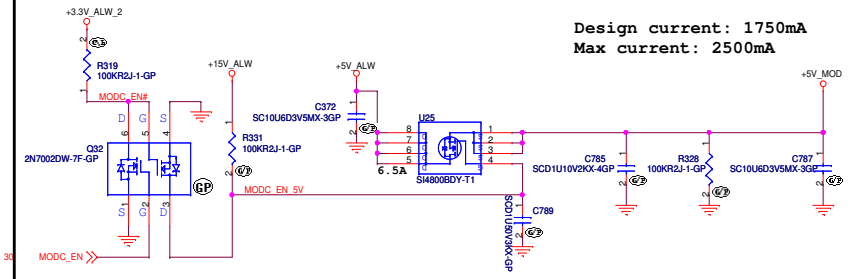
SB: Fine tune +3.3V_RUN sequence



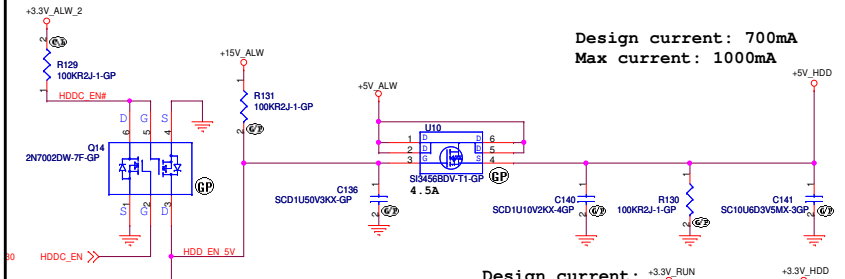
Design current: 682mA

R5U241 Power Switch

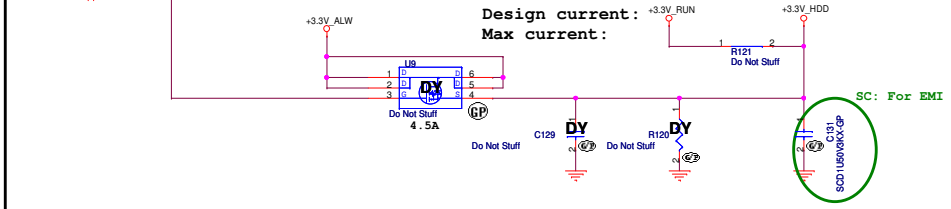




Design current: 1750mA
Max current: 2500mA



Design current: 700mA
Max current: 1000mA



Design current:
Max current:

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Title: Foose Intel Discrete

Size: C | Document Number: Power Plane Enable | Rev: -1

Date: Tuesday, April 07, 2009 | Sheet 33 of 79

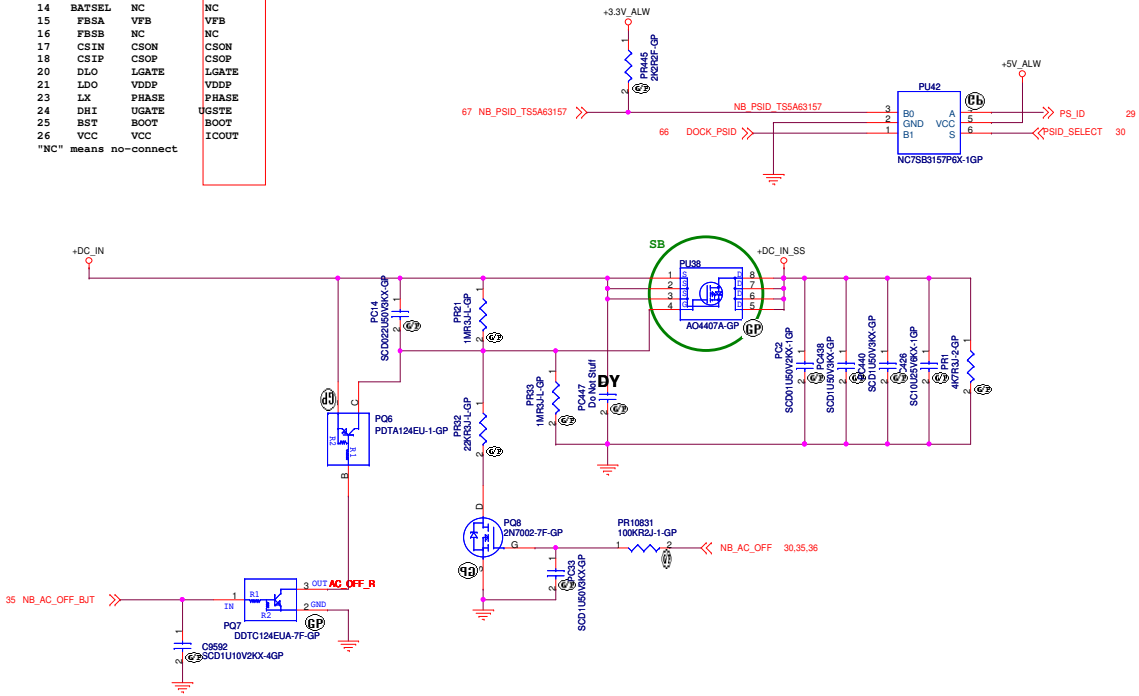
SSID = PWR.Support

TABLE MAXIM & INTERSIL BOM DIFFERENCES REF DES	MAXIM	INTERSIL	TI
R411	8.45K 1%	DUMMY	DUMMY
C98	0.01uF	0.1uF	0.1uF
C459	0.1uF 10V	DUMMY	200P 10V
C5	1uF 10V	DUMMY	1uF 10V
R16	365K 1%	215K 1%	309K 1%
R434	0 5%	10 5%	0 5%
R414	0 5%	10 5%	0 5%
C473	DUMMY	0.22uF	0.1uF
C457	DUMMY	0.22uF	0.1uF
C442	0.01uF	DUMMY	DUMMY
C453	0.1uF 10V	DUMMY	DUMMY
C36	220pF 50V	DUMMY	DUMMY
D23	RB751V-40	DUMMY	RB751V-40
C58	3.3nF	DUMMY	DUMMY
R64	1 1%	0 5%	0 5%
R394	100 5%	0 5%	0 5%
R110	0 5%	8.45K 1%	8.45K 1%
R401	10K 5%	2.2K 5%	4.7K 5%
C441	0.01uF	0.01uF	DUMMY
C449	0.01uF	0.01uF	DUMMY
R397	1K 5%	DUMMY	DUMMY
Q41	ISS355	DUMMY	DUMMY
C16	1uF 10V	1uF 10V	DUMMY
R30	33 1%	33 1%	DUMMY
R408	DUMMY	DUMMY	0 5%
R400	DUMMY	DUMMY	200K 5%
R403	DUMMY	DUMMY	7.5K 5%
C450	DUMMY	DUMMY	51P 10V
C444	DUMMY	DUMMY	2000P 10V
C448	DUMMY	DUMMY	130P 10V
C446	DUMMY	DUMMY	0.1uF
C483	DUMMY	DUMMY	0.1uF
R438	10K 1%	10K 1%	DUMMY
R412	DUMMY	DUMMY	10k 5%
R440	15.8K 1%	15.8K 1%	DUMMY
R407	DUMMY	10K 5%	DUMMY
R9	0 5%	10 5%	0 5%
C482	DUMMY	DUMMY	DUMMY
C12	DUMMY	DUMMY	DUMMY
R435	0 5%	10 5%	0 5%

PIN NAME DIFFERENCES

PIN	MAXIM	INTERSIL	BQ24745
1	GND	NC	ICREF
3	REF	VREF	VREF
4	CCS	ICOMP	EAO
5	CCI	NC	EAI
6	CCV	VCOMP	FBO
7	DAC	NC	CE
8	IINP	ICM	VICM
11	VDD	VDDSMB	VDDSMB
14	BATSEL	NC	NC
15	FBSA	VFB	VFB
16	FBSB	NC	NC
17	CSIN	CSON	CSON
18	CSIP	CSOP	CSOP
20	DLO	LGATE	LGATE
21	LDO	VDDP	VDDP
23	LX	PHASE	PHASE
24	DHI	UGATE	UGSTE
25	BST	BOOT	BOOT
26	VCC	VCC	ICOUT

"NC" means no-connect



MAX 8731A/ISL88731

Adapter (W)	Trip Current (A)	R416	R502	R501	R504
65	3.17	57.6K	13.0K	105	24.9K
90	4.43	51.1K	17.8K	348	33.2K

*R504 is populated if ADAPT_TRIP_SEL is used to program for the next lower adapter.

BQ247451

Adapter (W)	Trip Current (A)	R416	R502	R501	R504
65	3.17	57.6K	12.4K	205	24.3K
90	4.43	51.1K	16.9K	499	32.4K

*R504 is populated if ADAPT_TRIP_SEL is used to program for the next lower adapter.

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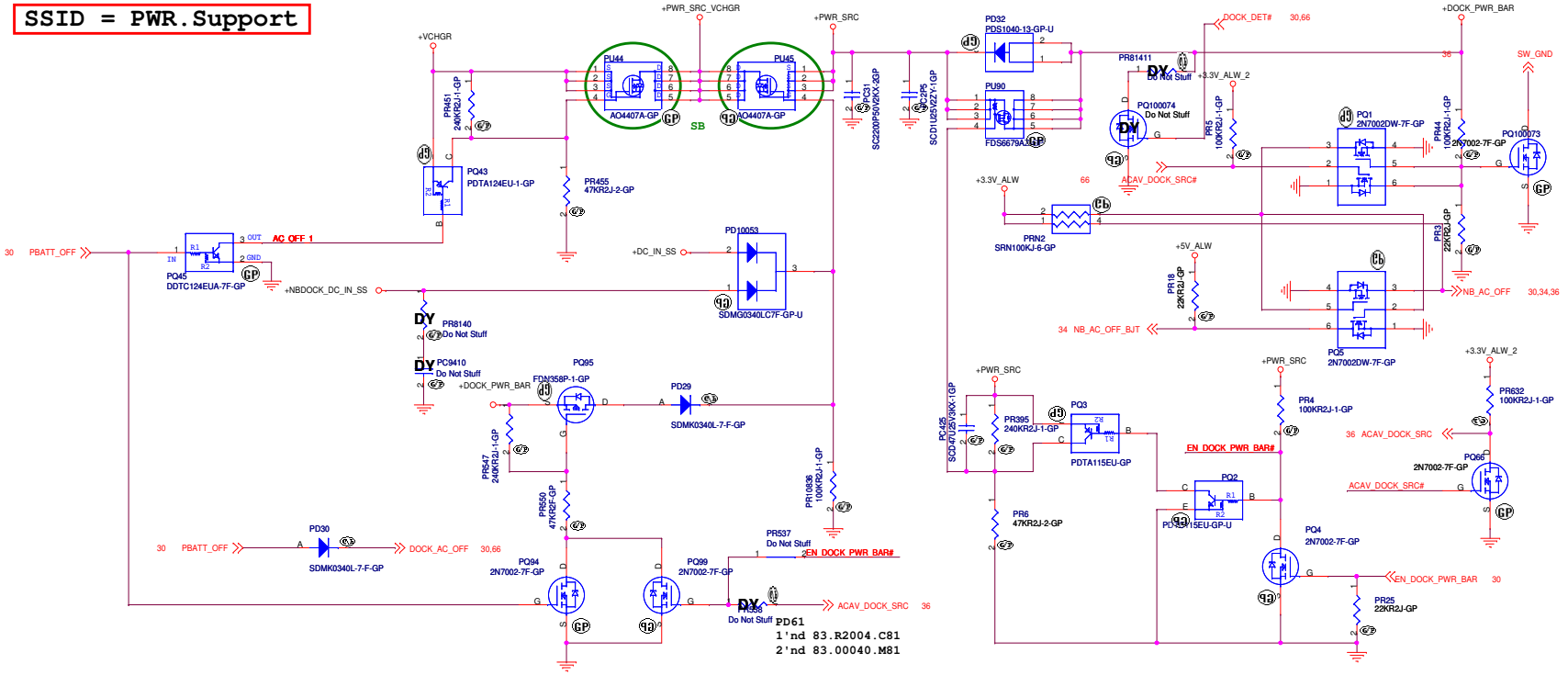
Taipei Hsien 221, Taiwan, R.O.C.

Title: Foose Intel Discrete

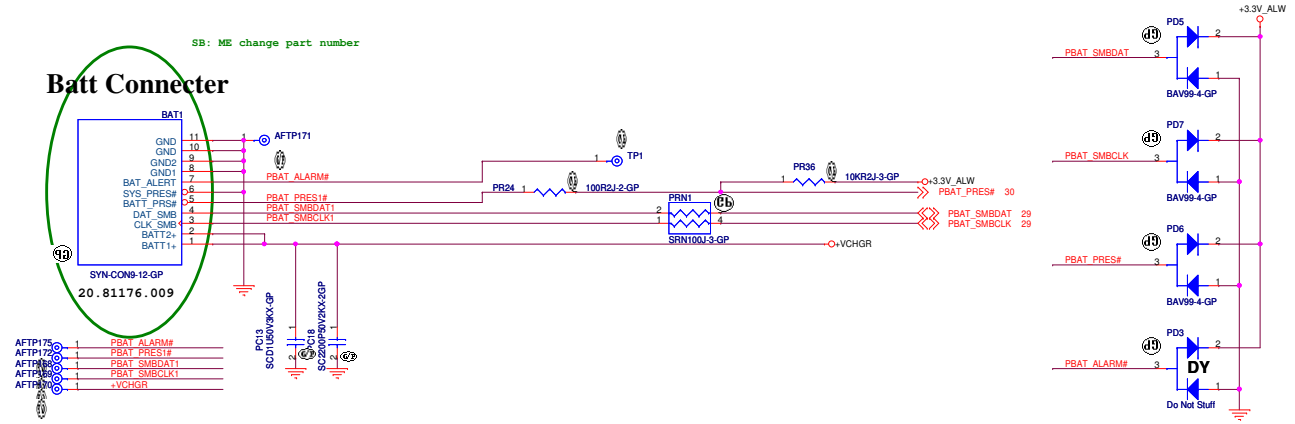
Size: C | Document Number: DCIN | Rev: -1

Date: Tuesday, April 07, 2009 | Sheet 34 of 79

SSID = PWR.Support



SSID = RBATT



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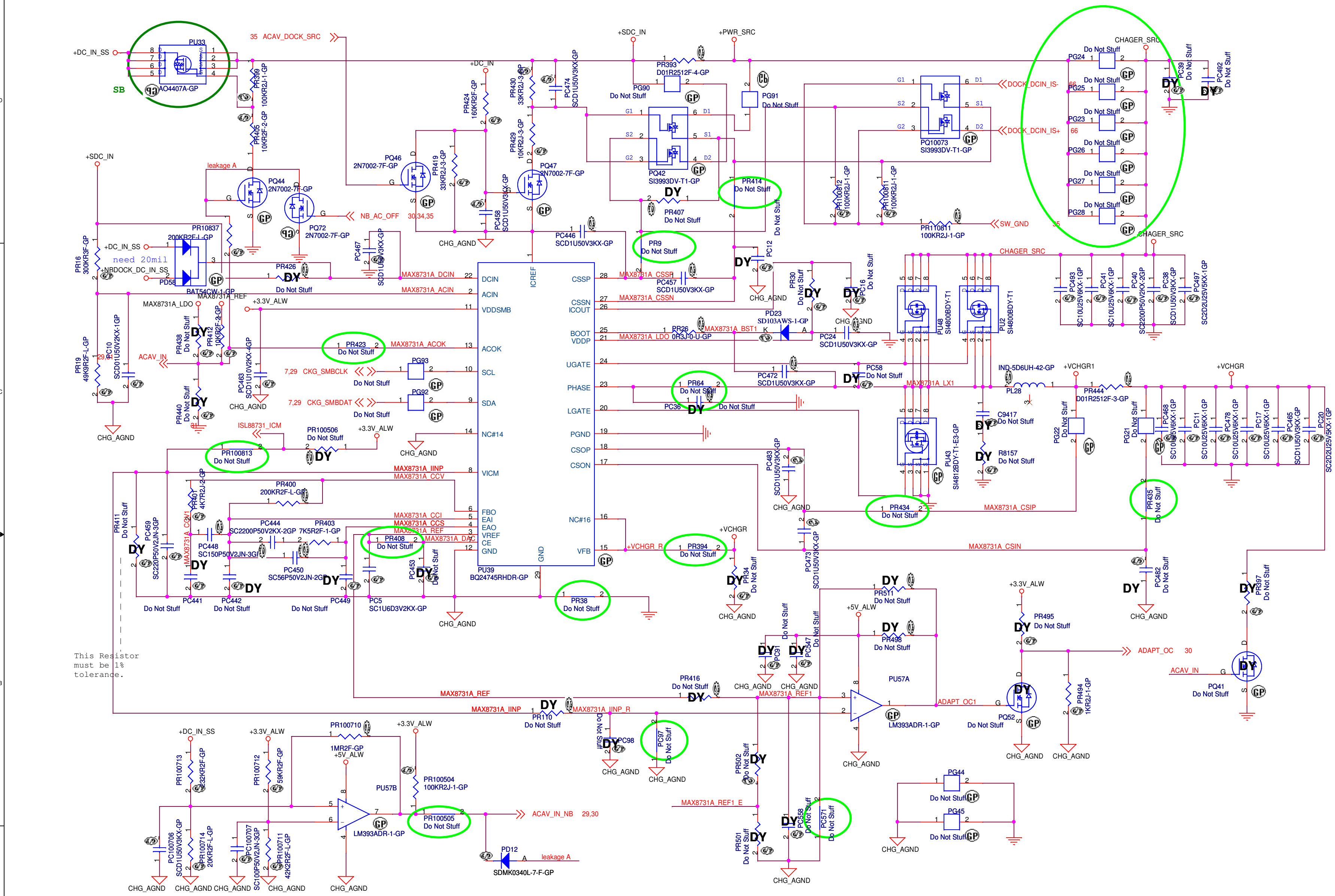
Title: Foose Intel Discrete

Size: C | Document Number: DOCK DCIN/BATT Connector | Rev: -1

Date: Tuesday, April 07, 2009 | Sheet 35 of 79

SSID = Charger



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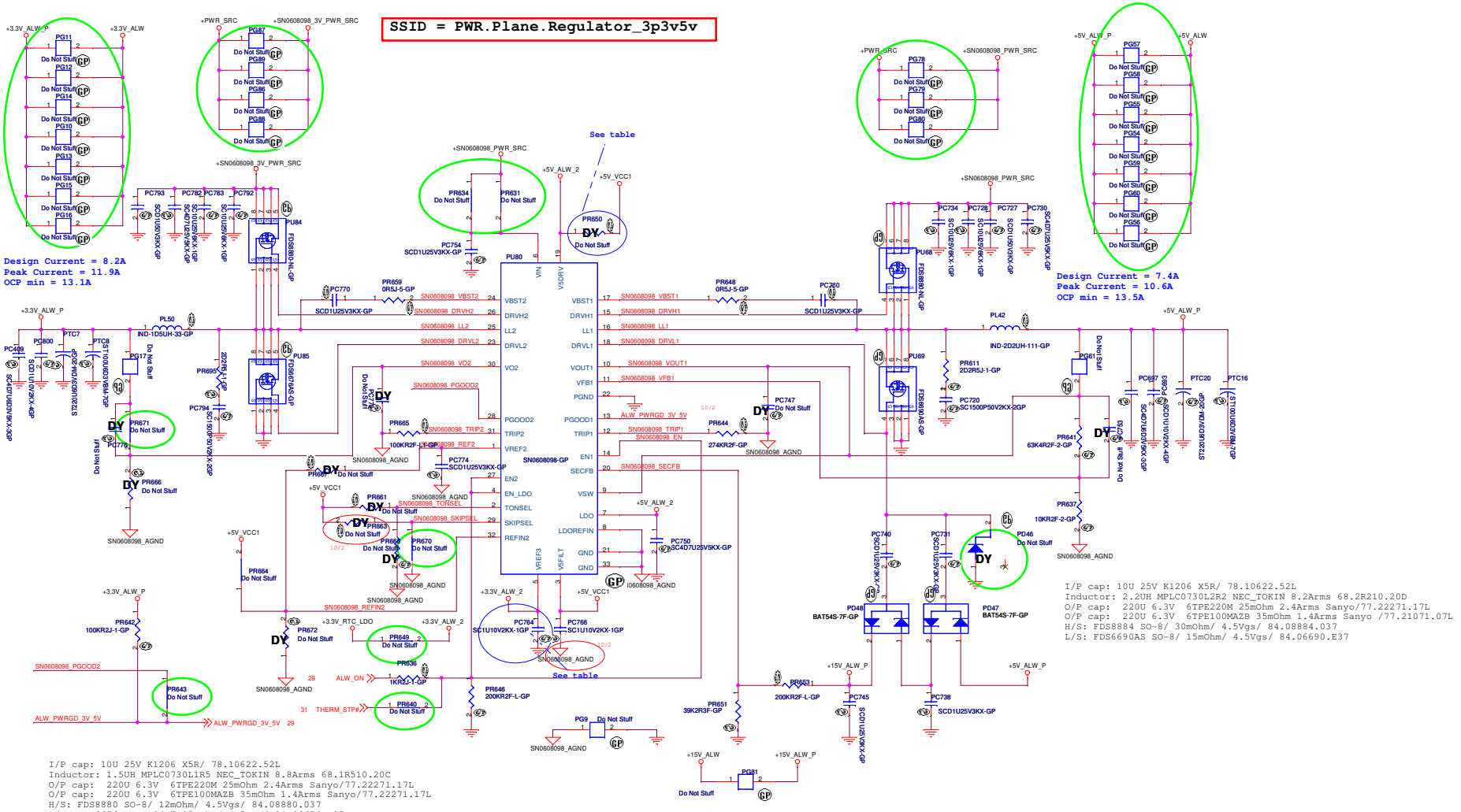
Title	Foose Intel Discrete	
Size C	Document Number Charger-BQ24745	Rev -1
Date: Tuesday, April 07, 2009	Sheet 36 of 79	

SSID = PWR.Plane.Regulator_3p3v5v



SKIPSEL	GND	FLOAT/VREF2	V5IN
Operating Mode	Auto Skip	OATM	PWM

TONSEL	GND	VREF2 or Float	V5FILT
CH1 Freq	400kHz	400kHz	200kHz
CH2 Freq	500kHz	300kHz	300kHz

	TABLE1		
	MAXIM ,INTERSIL & TI BOM differences		
	MAXIM	INTERSIL	TI
R	10ohm	NO STUFF	NO STUFF
C	1uF	0.1uF	1uF

		Min	Typ	Max
VOUT2 Output	3.3V Preset Output: REFIN2 = 5V, VIN = 5.5V to 28V, SKIPSEL = 5V	3.285 (-1.4%)	3.33	3.375 (+1.4%)
	1.05V Preset Output: REFIN2 = 3.3V, VIN = 5.5V to 28V, SKIPSEL=5V	1.038 (-1.2%)	1.05	1.062 (+1.2%)
	Tracking Output: REFIN2 = 1.0V, VIN = 5.5V to 28V, SKIPSEL = 5V	0.99 (-1%)	1.00	1.01 (+1%)

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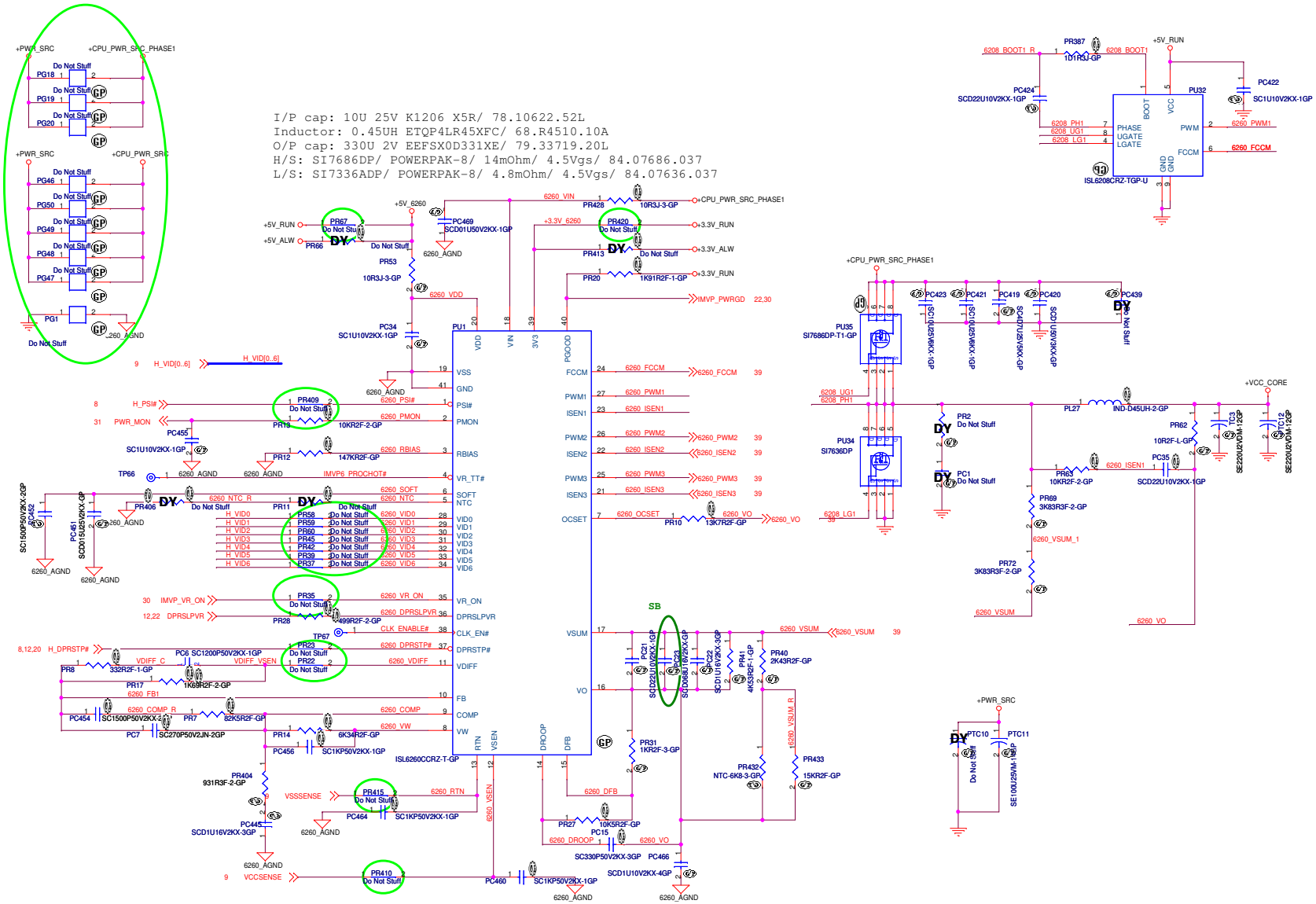
Title: Foose Intel Discrete

Size	Document Number	Rev
A2	DCDC 5V/3V-SN0608098	-1

Date: Tuesday, April 07, 2009 Sheet 37 of 79

SSID = CPU.Regulator



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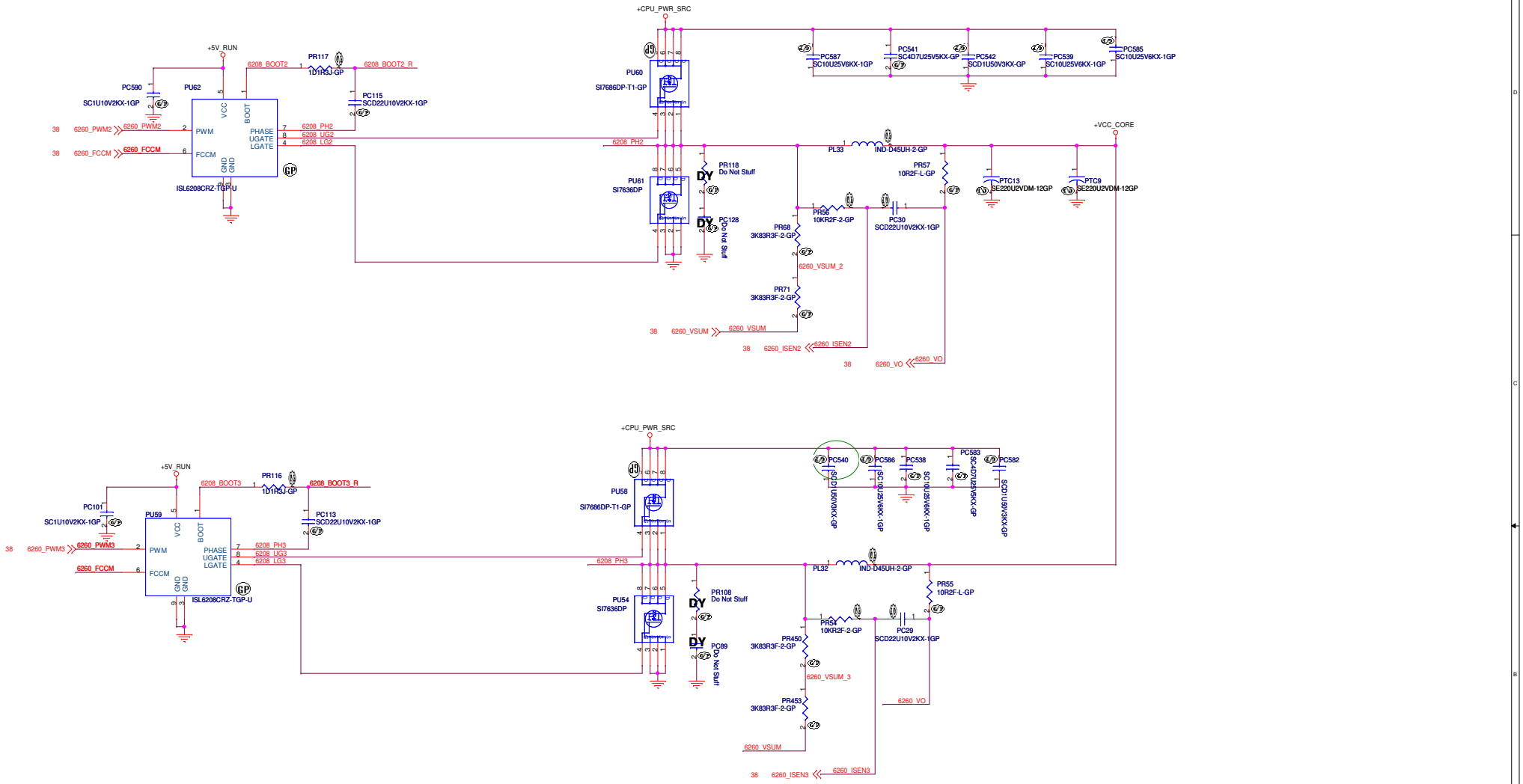
Title: *Foose Intel Discrete*

Size	Document Number	Rev
C	CPU Core-ISL6260(1/2)	-1

Date: Tuesday, April 07, 2009 Sheet 38 of 79

SSID = CPU.Regulator



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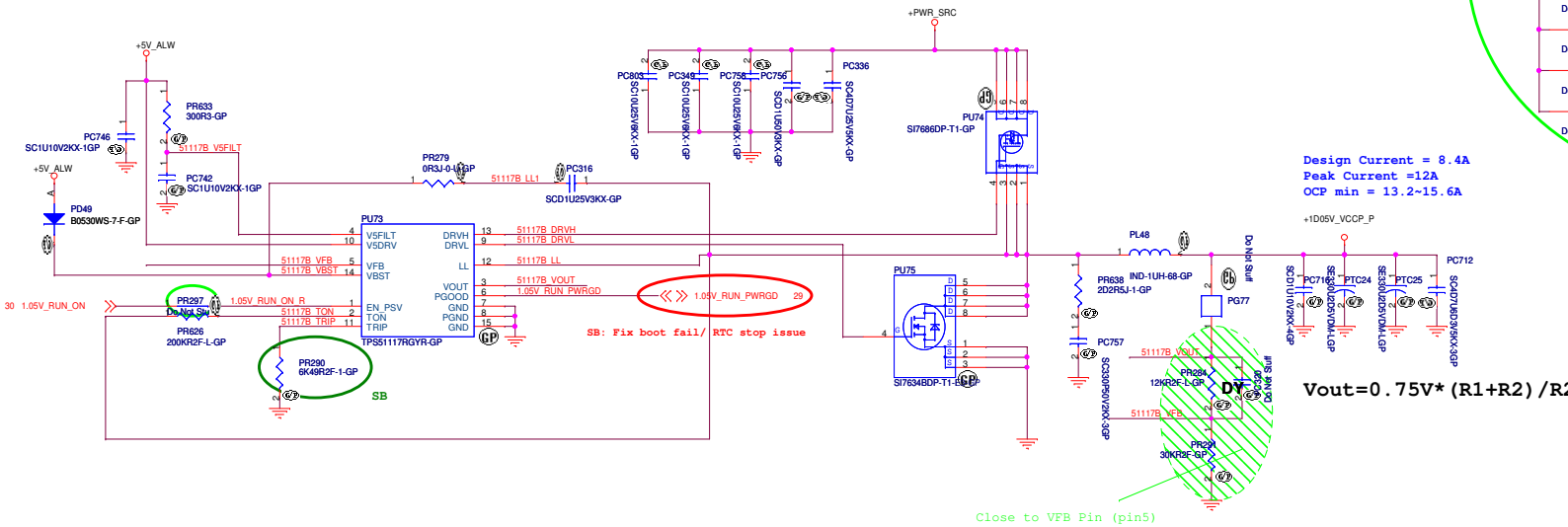
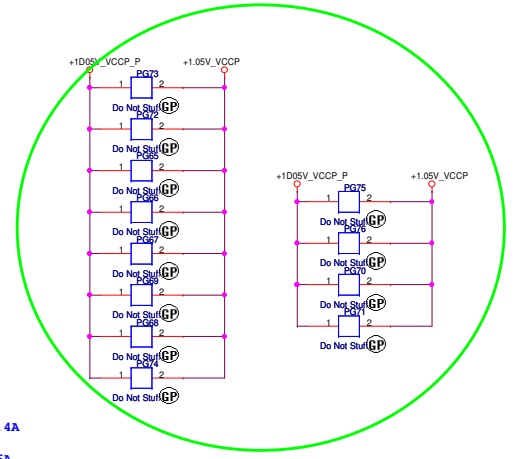
Title: Foose Intel Discrete

Size	Document Number	Rev
C	CPU Core-ISL6260(2/2)	-1

Date: Tuesday, April 07, 2009 Sheet 39 of 79

SSID = PWR.Plane.Regulator_1p05v





I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH MPLC1040L1R0 NEC_TOKIN 16.2Arms 68.1R01A.20D
O/P cap: 330U 2.5V 2R5TPE330MF 15mOhm 3.1Arms Sanyo/ 77.23371.L01
H/S: SI7686DP PowerPAK/ 11mOhm/ 4.5Vgs/ 84.07686.037
L/S: SI7636DP PowerPAK/ 4mOhm/ 4.5Vgs/ 84.07636.037
Switching freq-->400KHz

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Title: Foose Intel Discrete

Size	Document Number	Rev
C	DCDC 1D05-TPS5117	-1

Date: Tuesday, April 07, 2009 Sheet 40 of 79

SSID = PWR.Plane.Regulator_1p5v

Change BOM manually

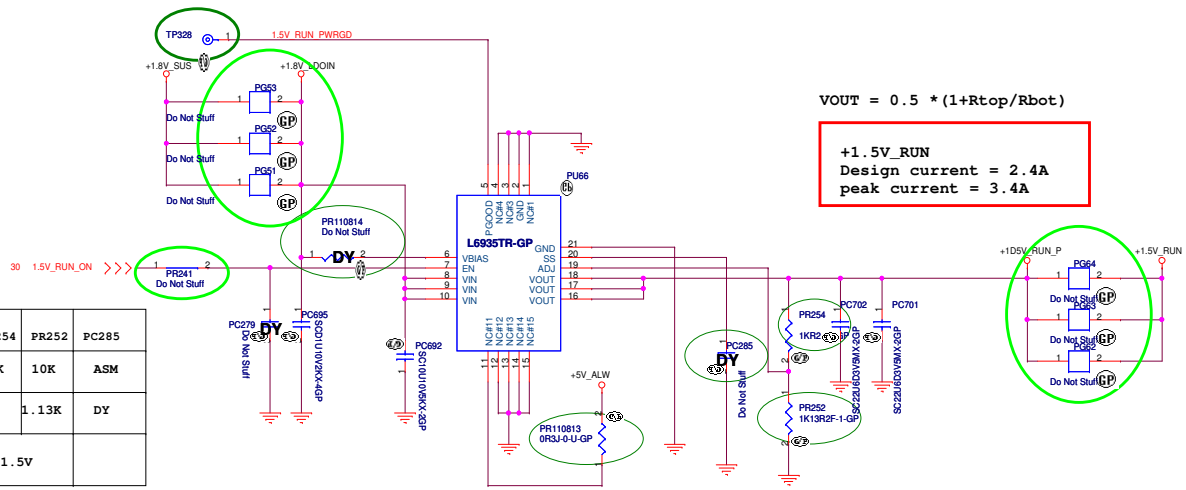
Main Source:
RT9035: 74.09035.033

Second Source:
L6935: 74.06935.033
PR254: 64.20025.6DL(20K)
PR252: 64.10025.6DL(10K)
PR110814: 63.00000.00L
PC285: 78.10224.2FL
PR110813: Dummy

Vendor	PIN6	PIN11	PIN20
L6935	VBIAS	N.C.	SS
RT9035	N.C.	VBIAS	N.C.

Vendor	PR110813	PR110814	PR254	PR252	PC285
L6935	DY	ASM	20K	10K	ASM
RT9035	ASM	DY	1K	1.13K	DY
			1.5V		

Remove Power On Logic Circuit



VOUT = 0.5 *(1+Rtop/Rbot)

+1.5V_RUN
Design current = 2.4A
peak current = 3.4A

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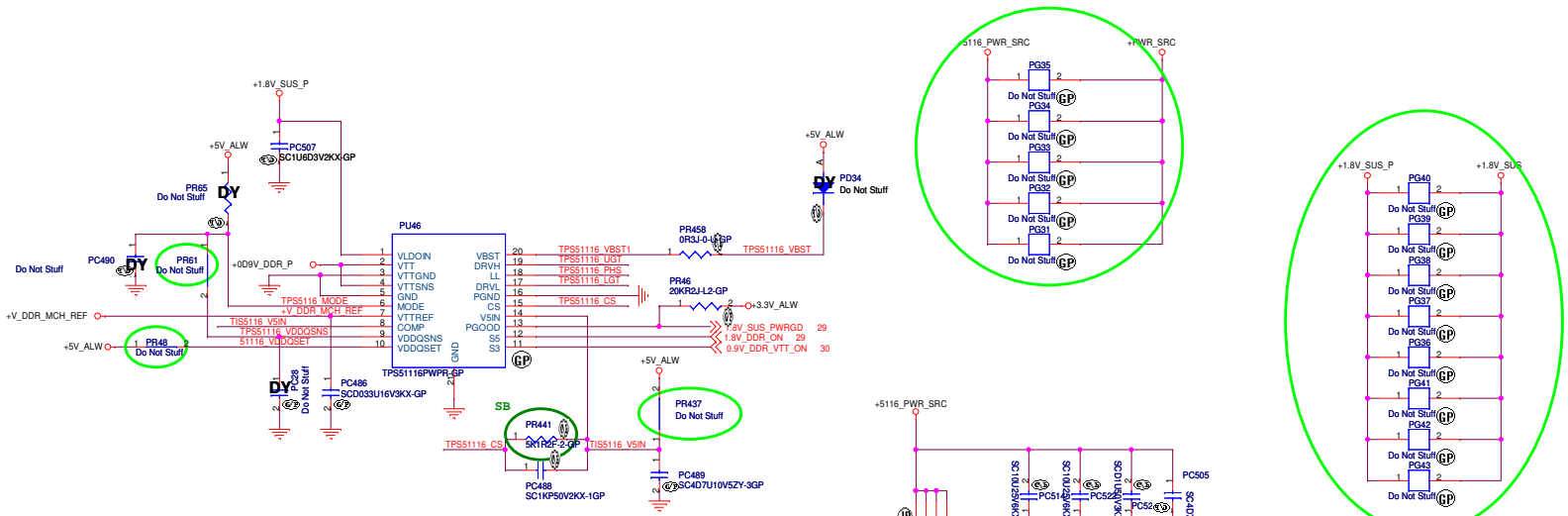
Title: Foose Intel Discrete

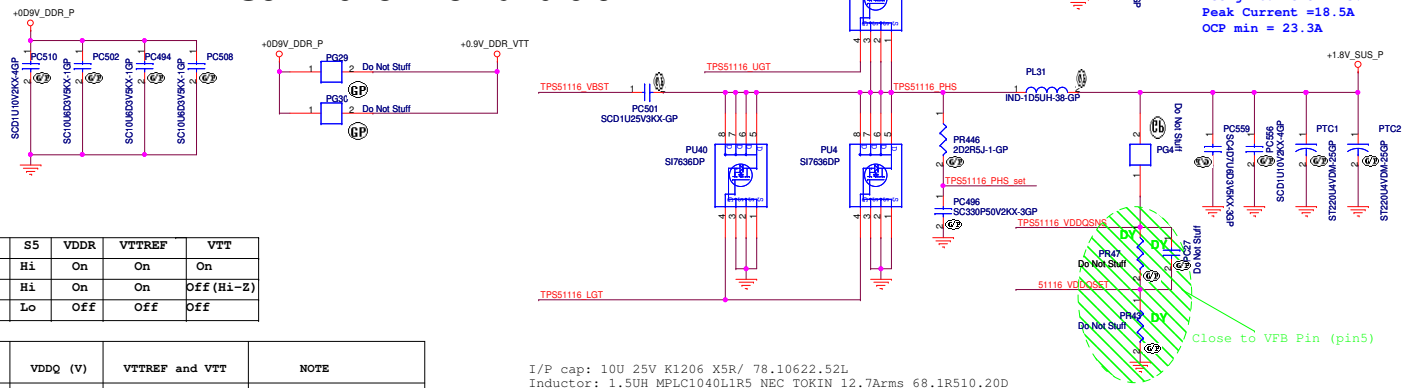
Size: C | Document Number: DCDC 1D5V-RT9035 | Rev: -1

Date: Tuesday, April 07, 2009 | Sheet 41 of 79

SSID = PWR.Plane.Regulator_1p8v0p9v



TI TPS51116 for 1.8V and 0.9V



Design Current = 13.7A
Peak Current =18.5A
OCP min = 23.3A

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH MPLC1040L1R5 NEC_TOKIN 12.7Arms 68.1R510.20D
O/P cap: 220U 4V ST220U4VDM 40mOhm 1.9Arms Sanyo/77.22271.19L
H/S: FDS8880 SO-8/ 12mOhm/ 4.5Vgs/ 84.08880.037
L/S: FDS6676AS SO-8/ 7.25mOhm/ 4.5Vgs/ 84.06676.A37
Switching freq-->400KHz

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Title: Foose Intel Discrete

Size	Document Number	Rev
C	DCDC 1.8V/0.9V-TPS5116	-1

Date: Tuesday, April 07, 2009 Sheet 42 of 79

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Title: Foose Intel

Size	Document Number	Rev
C	Reserve for Power team	-1

Date: Tuesday, April 07, 2009 Sheet 43 of 79

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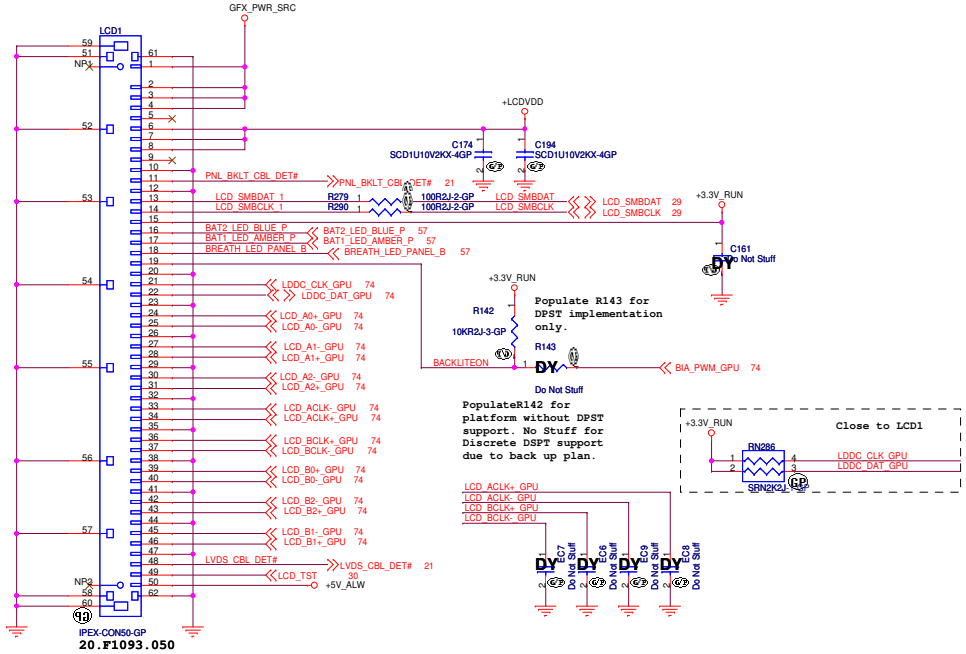
Title: Foose Intel

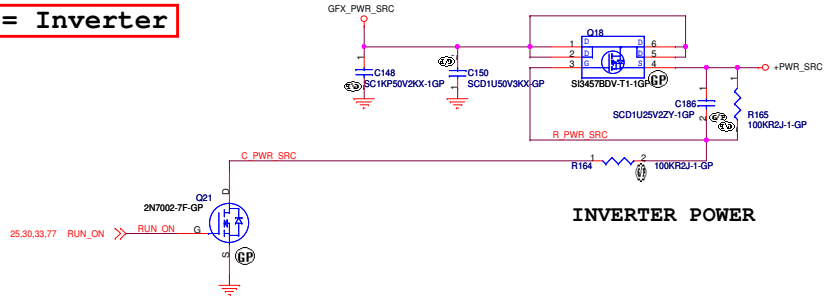
Size	Document Number	Rev
C	Reserve for Power team	-1

Date: Tuesday, April 07, 2009 Sheet 44 of 79

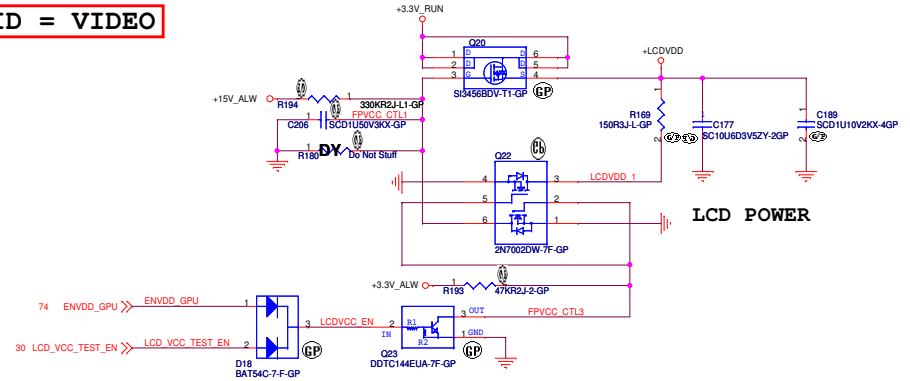
SSID = VIDEO



SSID = Inverter



SSID = VIDEO



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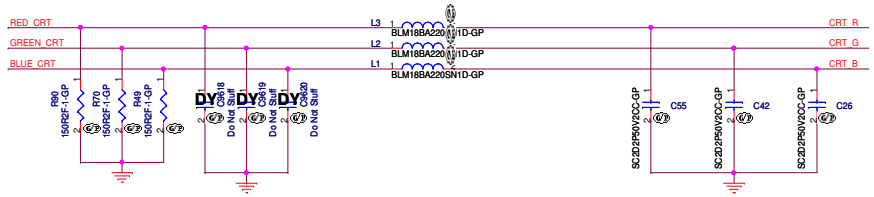
Title: Foose Intel Discrete

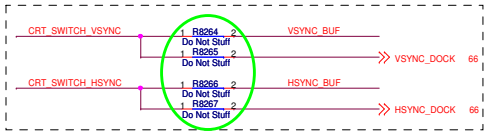
Size	Document Number	Rev
C	LCD	-1

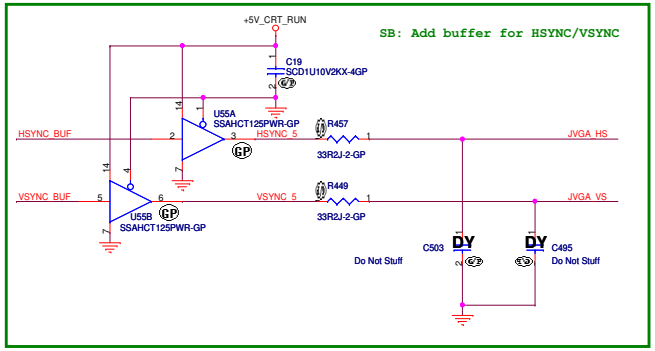
Date: Tuesday, April 07, 2009 Sheet 45 of 79

SSID = VIDEO

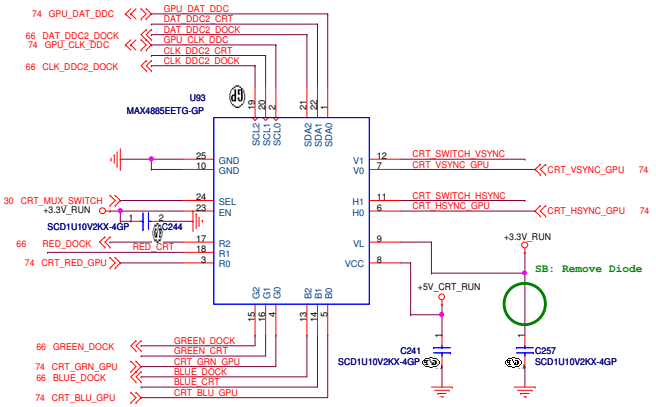
RGB

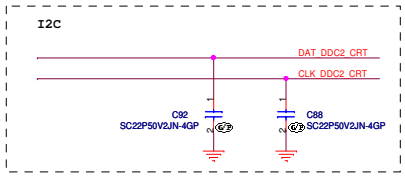




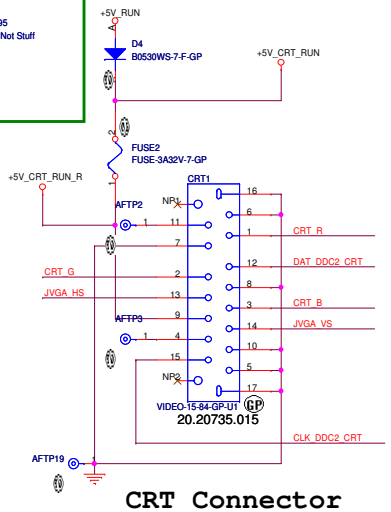


Layout Note:
*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.

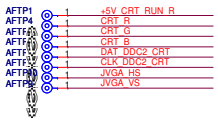




MAX4885E has internal ESD protection and internal level shift



CRT Connector



CRT_MUX_SWITCH	CRT display
0	MB
1	Dock

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Title: Foose Intel Discrete

Size	Document Number	Rev
C	CRT/CRT Switch	-1

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Title: Foose Intel

Size	Document Number	Rev
C	Display Port(Reserve)	-1

Date: Tuesday, April 07, 2009 Sheet 47 of 79

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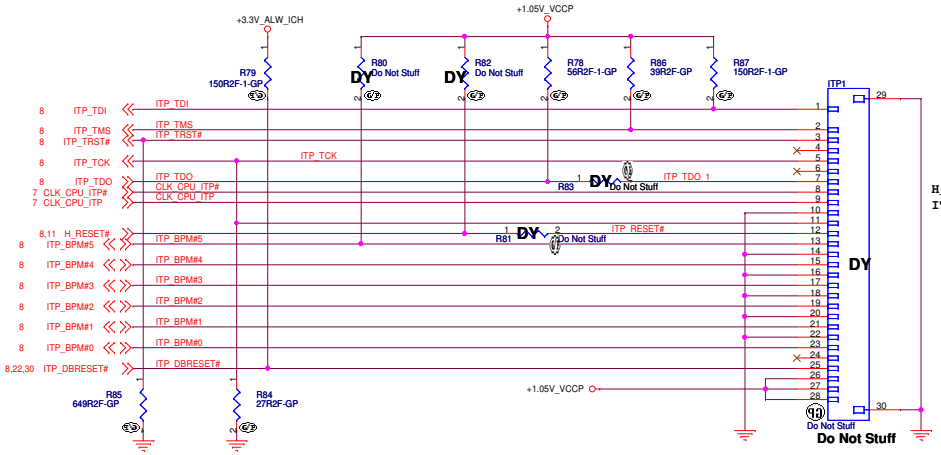
Title: Foose Intel

Size	Document Number	Rev
C	HDMI/DVI(Reserve)	-1

Date: Tuesday, April 07, 2009 Sheet 48 of 79

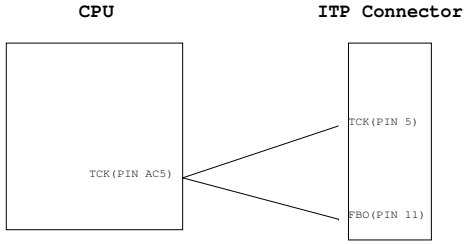
SSID = User.interface

ITP Debug Connector



H_RESET# use pull-up Resistor close
ITP connector 500 mil (max)

+1.05V_VCCP use Decoupling Capacitor close
ITP connector 100 mil (max)



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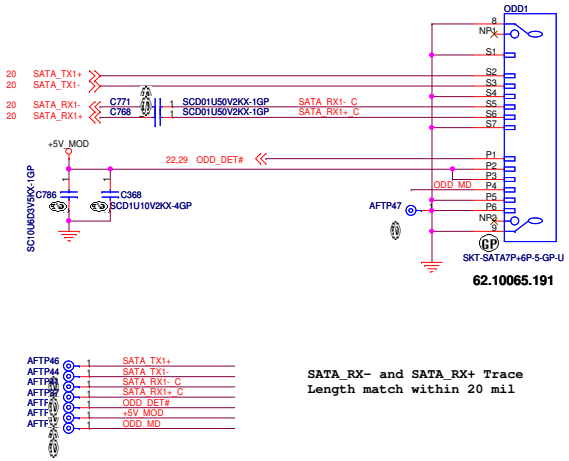
Title: Foose Intel Discrete

Size	Document Number	Rev
C	ITP Debug Connector	-1

Date: Tuesday, April 07, 2009 Sheet 49 of 79

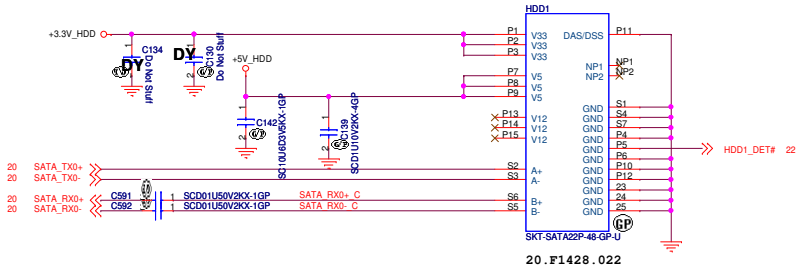
SSID = SATA SATA ODD Connector



62.10065.191

SATA_RX- and SATA_RX+ Trace
Length match within 20 mil

SSID = SATA SATA HDD Connector



20.F1428.022

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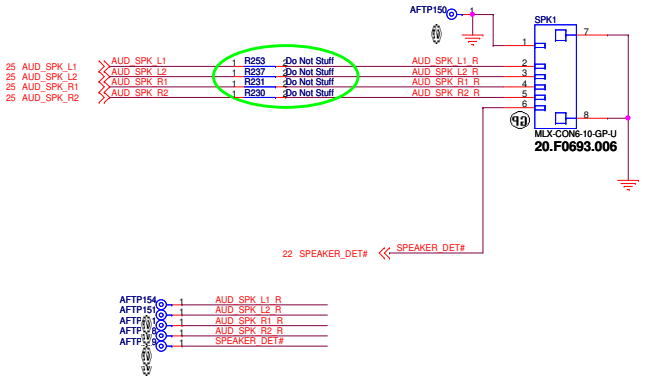
Title: Foose Intel Discrete

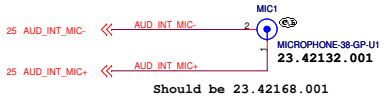
Size	Document Number	Rev
C	HDD/ODD Connector	-1

Date: Wednesday, April 06, 2009 Sheet 50 of 79

SSID = AUDIO Speaker



SSID = AUDIO Internal MIC



Should be 23.42168.001

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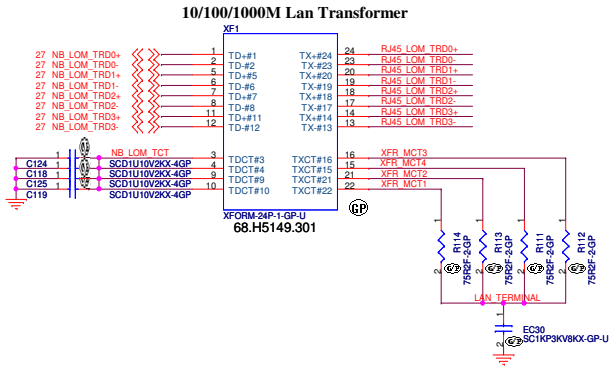
Title: Foose Intel

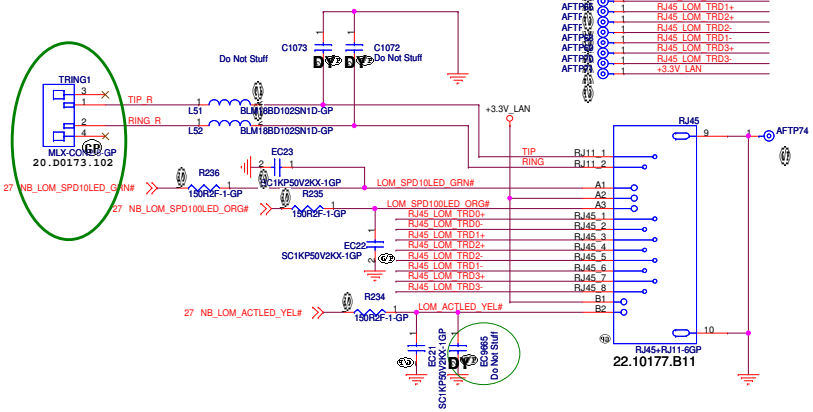
Size	Document Number	Rev
C	Micro Phone/Speaker	-1

Date: Tuesday, April 07, 2009 Sheet 51 of 79

SSID = LOM

LAN Connector





The blowout from the LAN magnetics to the RJ45 connector maintining the distance between the two to be within 1 inch.

Hipot layout guide line update space > 50mil

Rj11 layout guide line update > 100mil

1.Route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.Pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

Green LED:Speed 10
Orange LED:Speed 100
Yellow LED:GigaLAN

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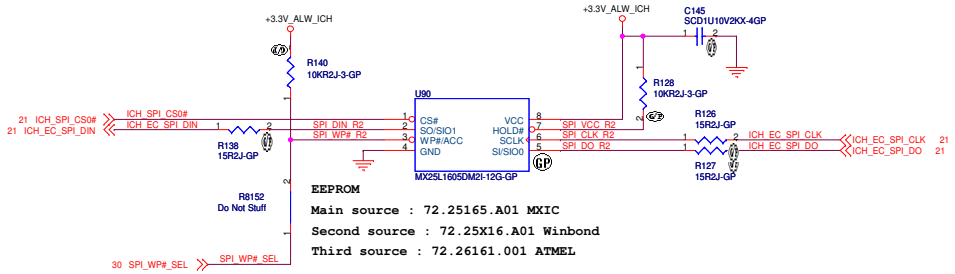
Taipei Hsien 221, Taiwan, R.O.C.

Title: Foose Intel Discrete

Size: C | Document Number: LAN Connector | Rev: -1

Date: Tuesday, April 07, 2009 | Sheet 52 of 79

SSID = Flash.ROM



EEPROM

Main source : 72.25165.A01 MXIC

Second source : 72.25X16.A01 Winbond

Third source : 72.26161.001 ATMEL

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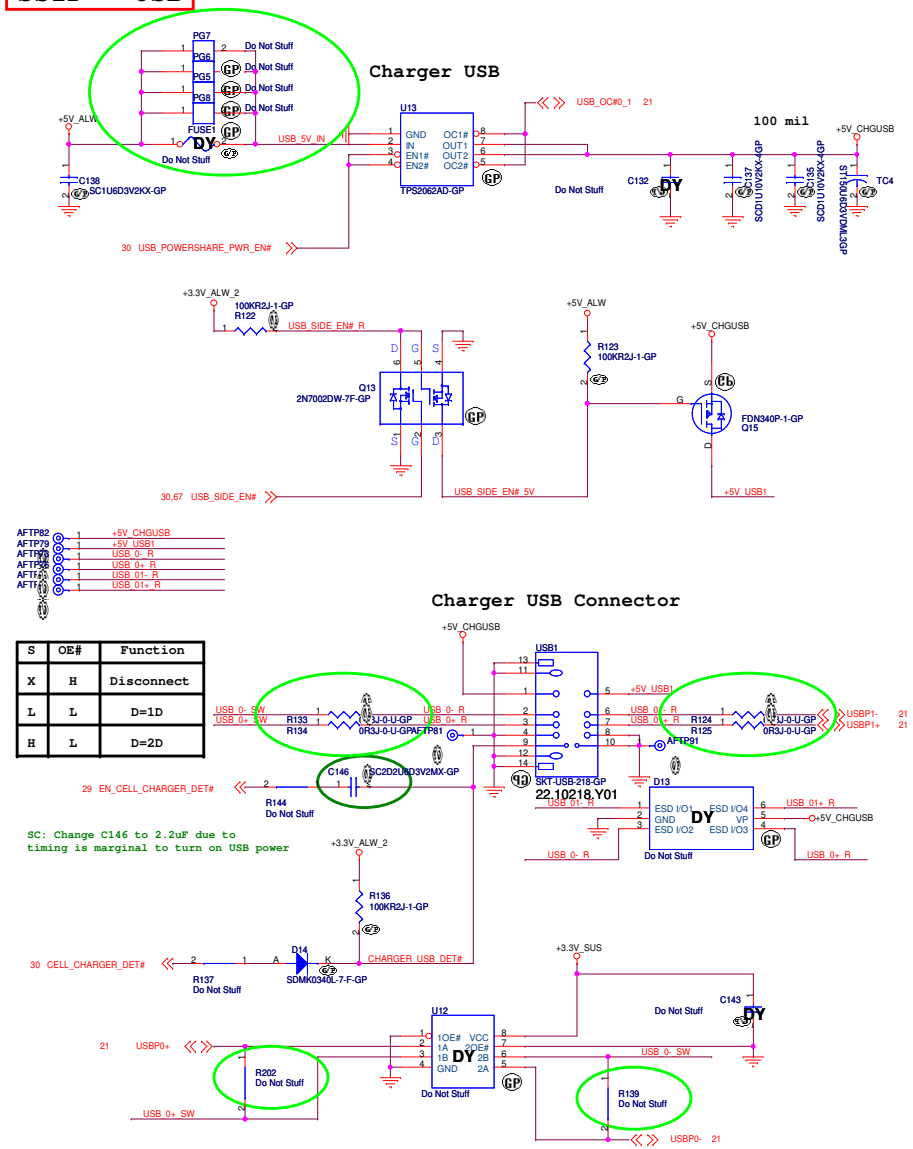
Title: *Foose Intel*

Size	Document Number	Rev
C	*Flash/EEPROM*	*-1*

Date: Tuesday, April 07, 2009 Sheet 53 of 79

SSID = USB



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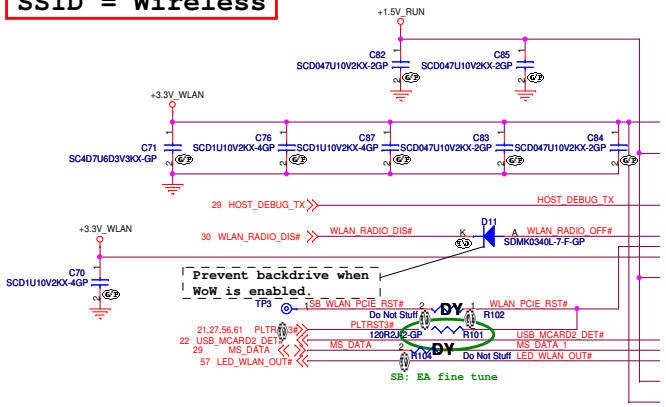
Title: *Foose Intel Discrete*

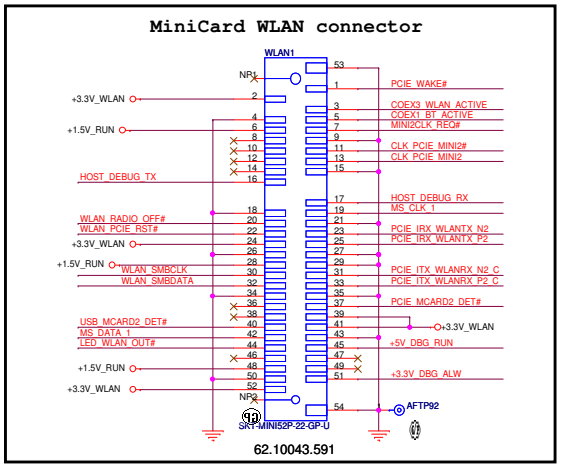
Size: C | Document Number: *USB Port (Power Share)* | Rev: -1

Date: Tuesday, April 07, 2009 | Sheet 54 of 79

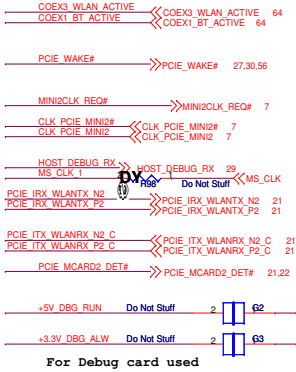
SSID = Wireless



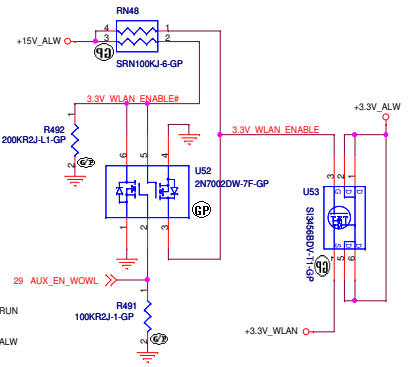
MiniCard WLAN connector

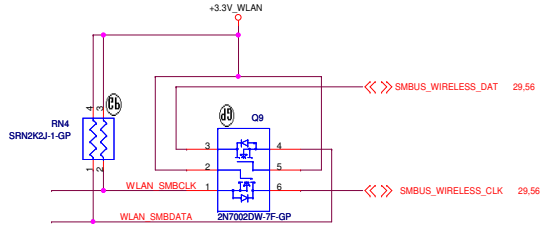


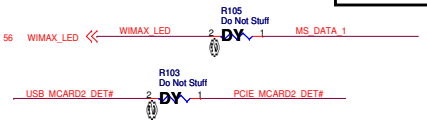
62.10043.591



For Debug card used only.







JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81

DEBUG PINS

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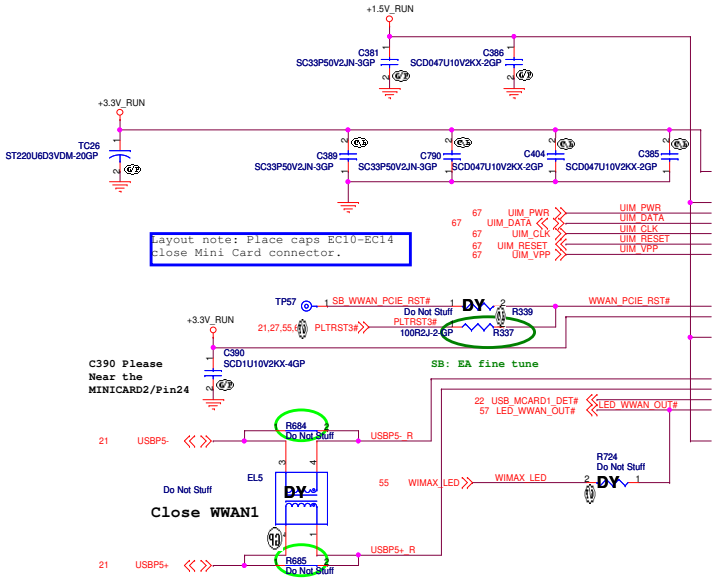
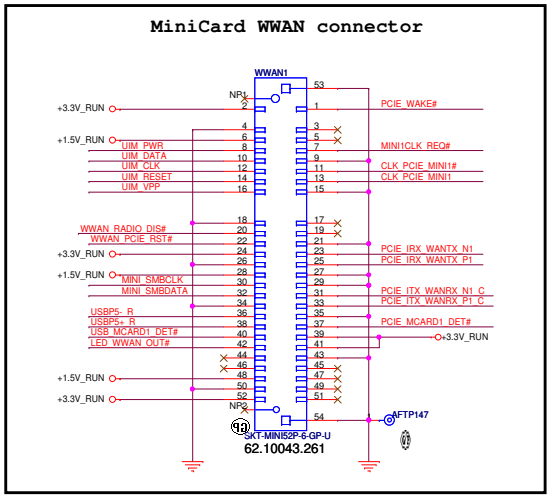
Title: ***Foose Intel Discrete***

Size: C | Document Number: ***WLAN/Serial out Connector*** | Rev: -1

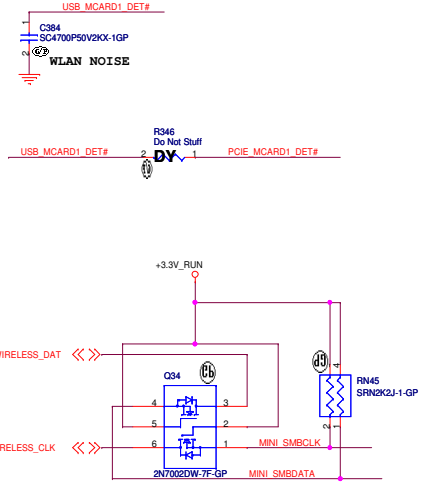
Date: Tuesday, April 07, 2009 | Sheet 55 of 79

SSID = Wireless





WWAN_RADIO_DIS# 30
PCIE_WAKE# PCIE_WAKE# 27,30,55
MINI1CLK_REQ# MINI1CLK_REQ# 7
CLK_PCIE_MINI1# CLK_PCIE_MINI1# 7
CLK_PCIE_MINI1 CLK_PCIE_MINI1 7
PCIE_IRX_WANTX_N1 PCIE_IRX_WANTX_N1 21
PCIE_IRX_WANTX_P1 PCIE_IRX_WANTX_P1 21
PCIE_ITX_WANRX_N1_C PCIE_ITX_WANRX_N1_C 21
PCIE_ITX_WANRX_P1_C PCIE_ITX_WANRX_P1_C 21
PCIE_MCARD1_DET# PCIE_MCARD1_DET# 22



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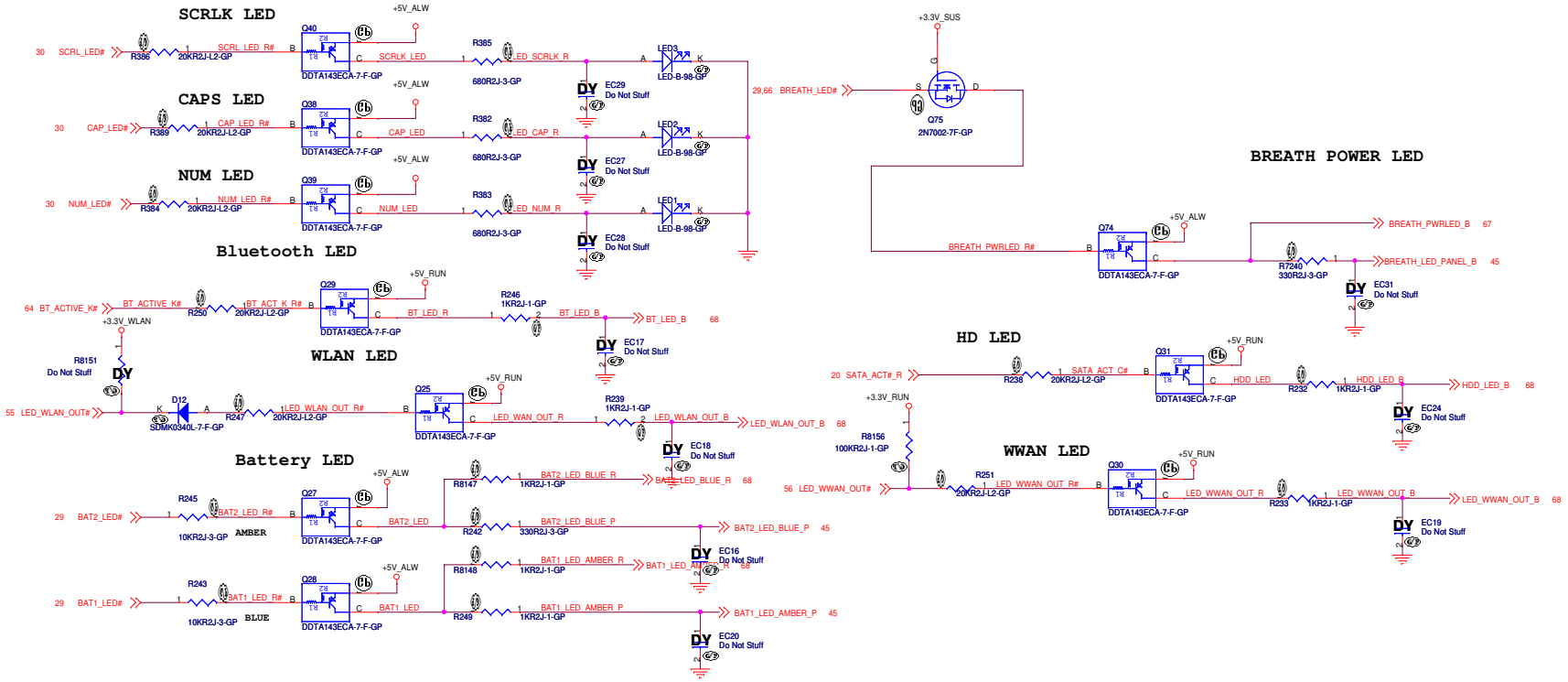
Title: Foose Intel Discrete

Size	Document Number	Rev
C	WWAN Connector	-1

Date: Tuesday, April 07, 2009 Sheet 56 of 79

SSID = User.interface



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Title: Foose Intel Discrete

Size	Document Number	Rev
C	LED	-1

Date: Tuesday, April 07, 2009 Sheet 57 of 79

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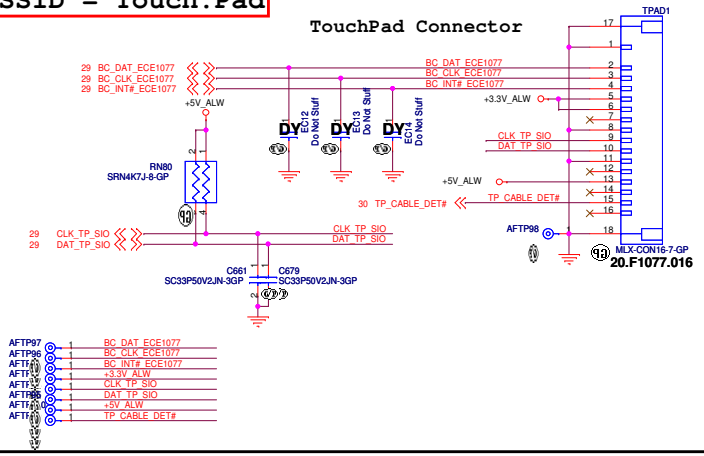
Title: Foose Intel

Size	Document Number	Rev
C	Reserve	-1

Date: Tuesday, April 07, 2009 Sheet 58 of 79

SSID = Touch.Pad

TouchPad Connector



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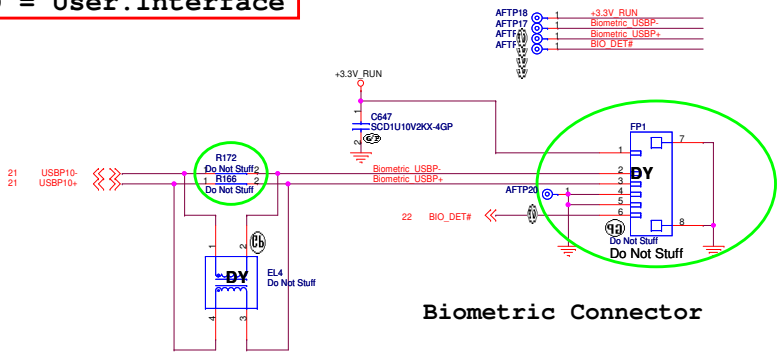
Title: ***Foose Intel Discrete***

Size	Document Number	Rev
C	***Keyboard/Touch pad***	-1

Date: Tuesday, April 07, 2009 Sheet 59 of 79

SSID = User.Interface



Biometric Connector

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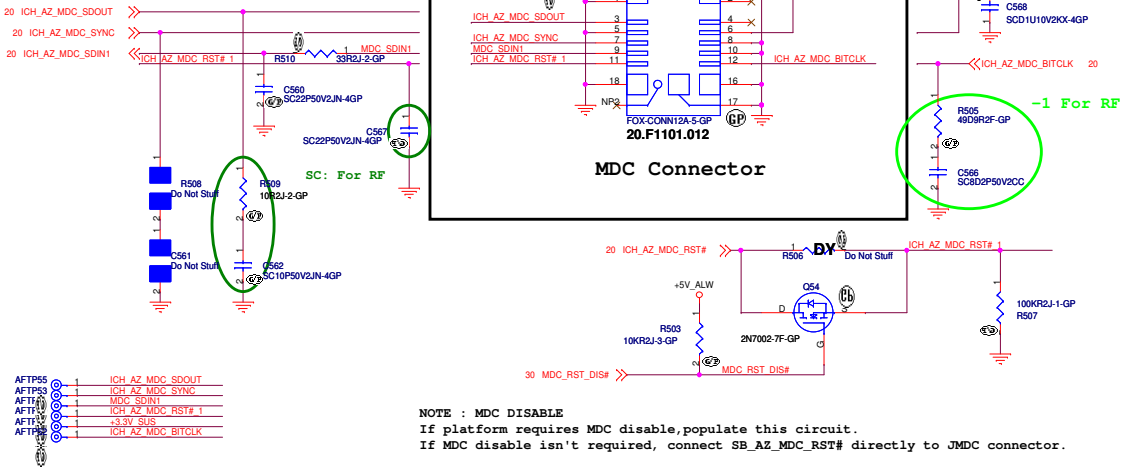
Title: Foose Intel Discrete

Size	Document Number	Rev
C	Finger Printer Connector	-1

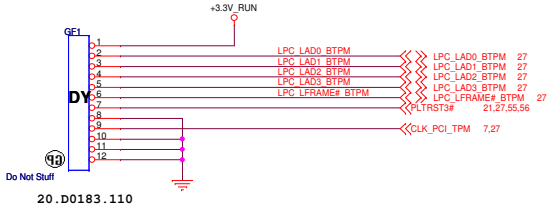
Date: Tuesday, April 07, 2009 Sheet 60 of 79

SSID = Modem



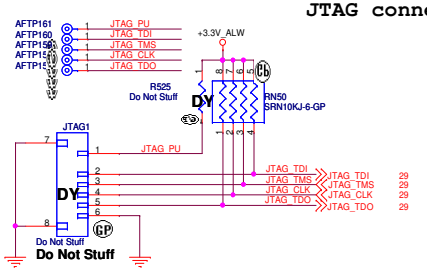
NOTE : MDC DISABLE
If platform requires MDC disable,populate this circuit.
If MDC disable isn't required, connect SB_AZ_MDC_RST# directly to JMDC connector.

VBIOS Debug port



20.D0183.110

JTAG connector



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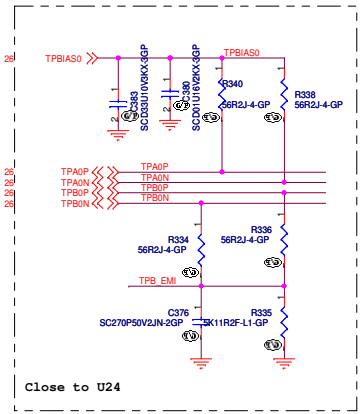
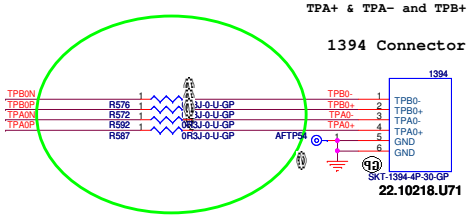
Title: Foose Intel Discrete

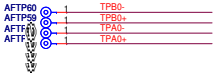
Size	Document Number	Rev
C	Debug port/JTAG/MDC	-1

Date: Tuesday, April 07, 2009 Sheet 61 of 79

SSID = 1394







Shield GND separately for pairs of TPA+ & TPA- and TPB+ & TPB-

1394 Connector

22.10218.U71

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Title: *Foose Intel Discrete*

Size	Document Number	Rev
C	*1394 Connector*	-1

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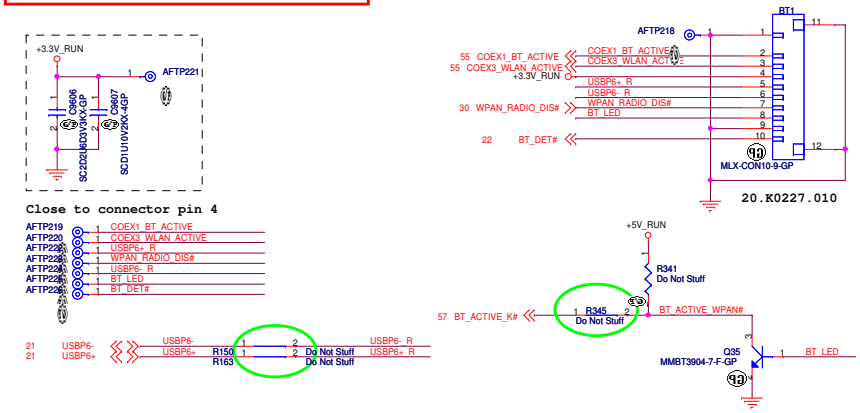
Title: Foose Intel

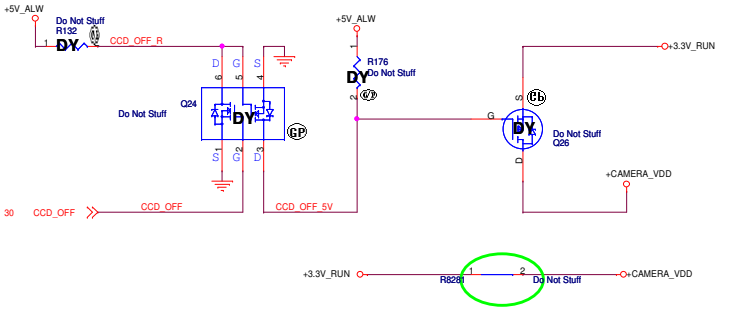
Size	Document Number	Rev
C	Express Card(Reserve)	-1

Date: Tuesday, April 07, 2009 Sheet 63 of 79

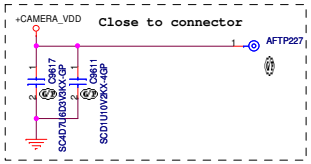
SSID = User.interface

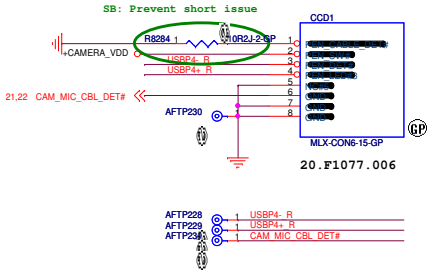


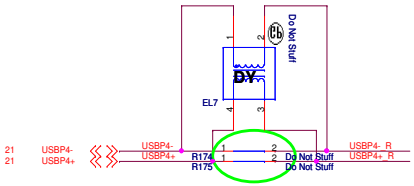
Webcam PWR CTRL



SSID = User.interface







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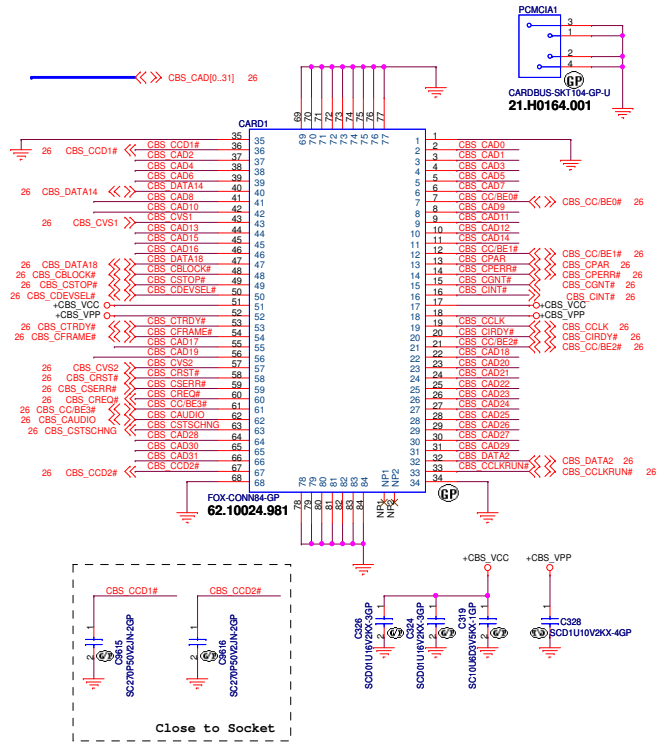
Title: Foose Intel Discrete

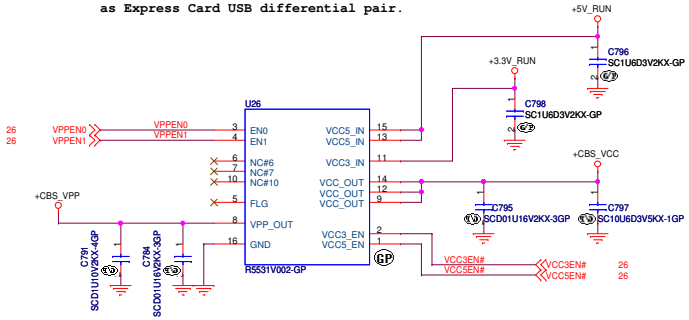
Size	Document Number	Rev
C	Bluetooth/Camera	-1

Date: Tuesday, April 07, 2009 Sheet 64 of 79

SSID = CARDBUS



CBS_CAD13, CBS_CAD15 Can be used
as Express Card USB differential pair.



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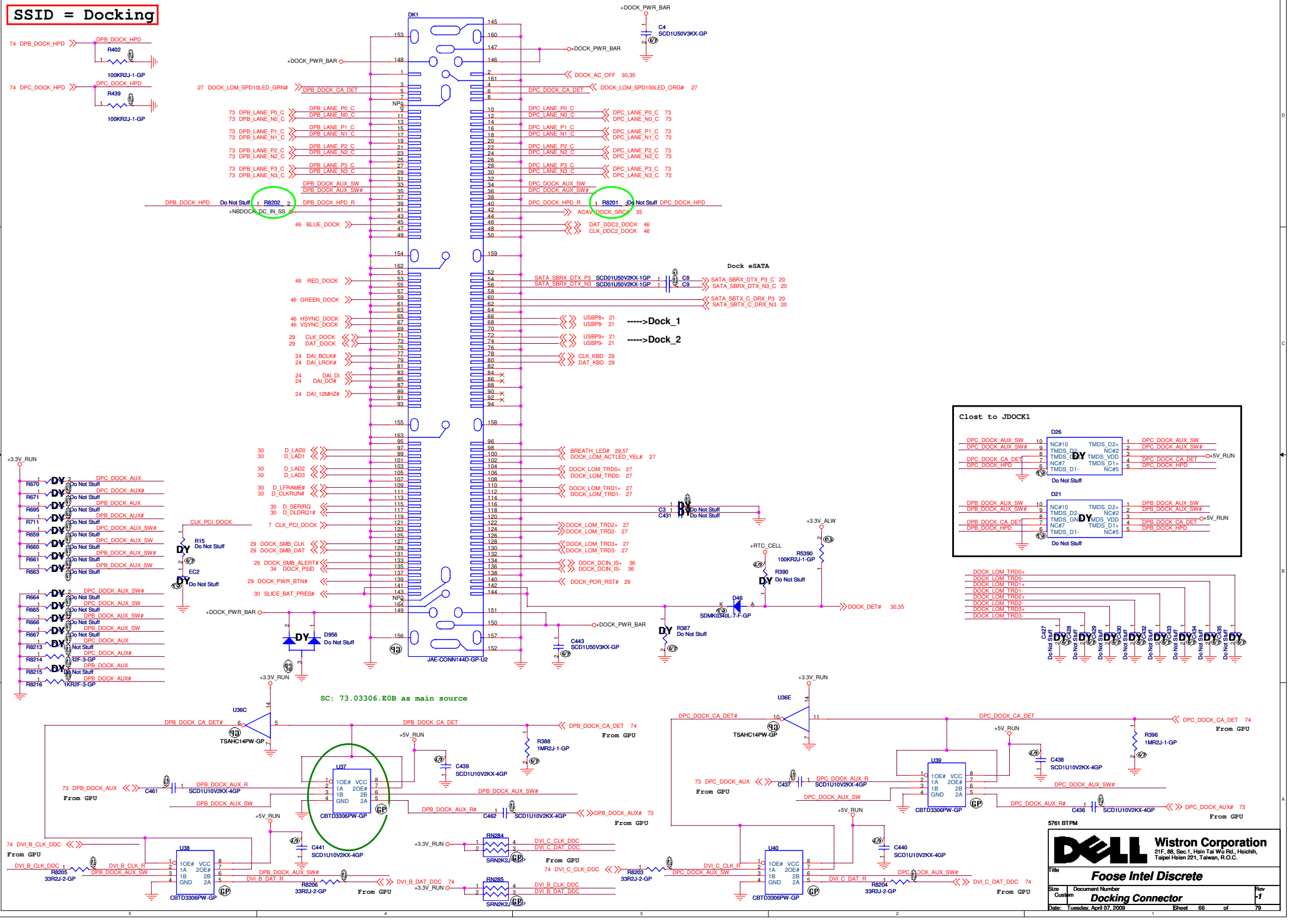
Title: Foose Intel Discrete

Size: C | Document Number: PCMCIA Card | Rev: -1

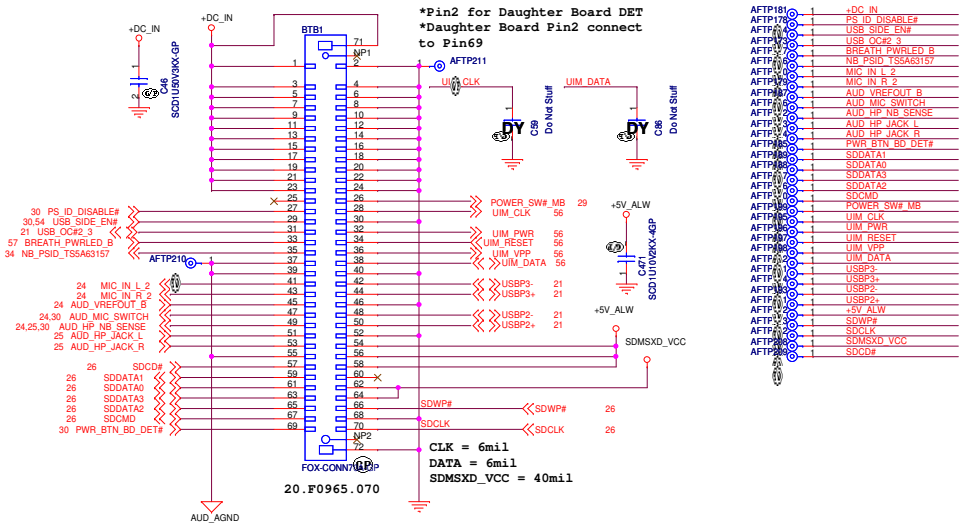
Date: Tuesday, April 07, 2009 | Sheet 65 of 79

SSID = Docking



SSID = User.Interface

IO Board Connector



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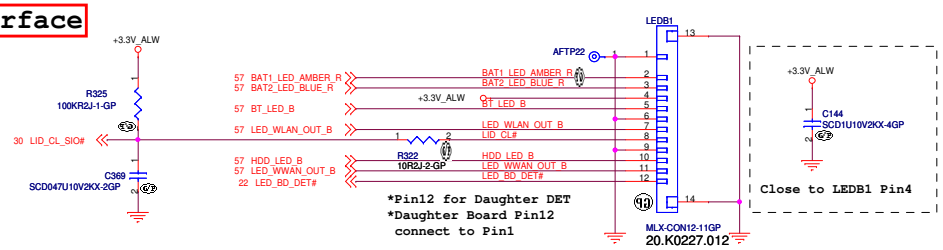
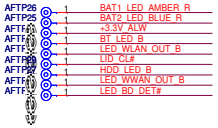
Title: *Foose Intel Discrete*		
Size: C	Document Number: *IO Board Connector*	Rev: -1
Date: Tuesday, April 07, 2009	Sheet 67 of 79	

SSID = User.interface





LED BD Connetor

LED Location from left to right

HDD	BATTERY	WLAN	BLUE TOOTH	WWAN

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Title: *Foose Intel Discrete*

Size: C | Document Number: *LED Board Connector* | Rev: -1

Date: Tuesday, April 07, 2009 | Sheet 68 of 79

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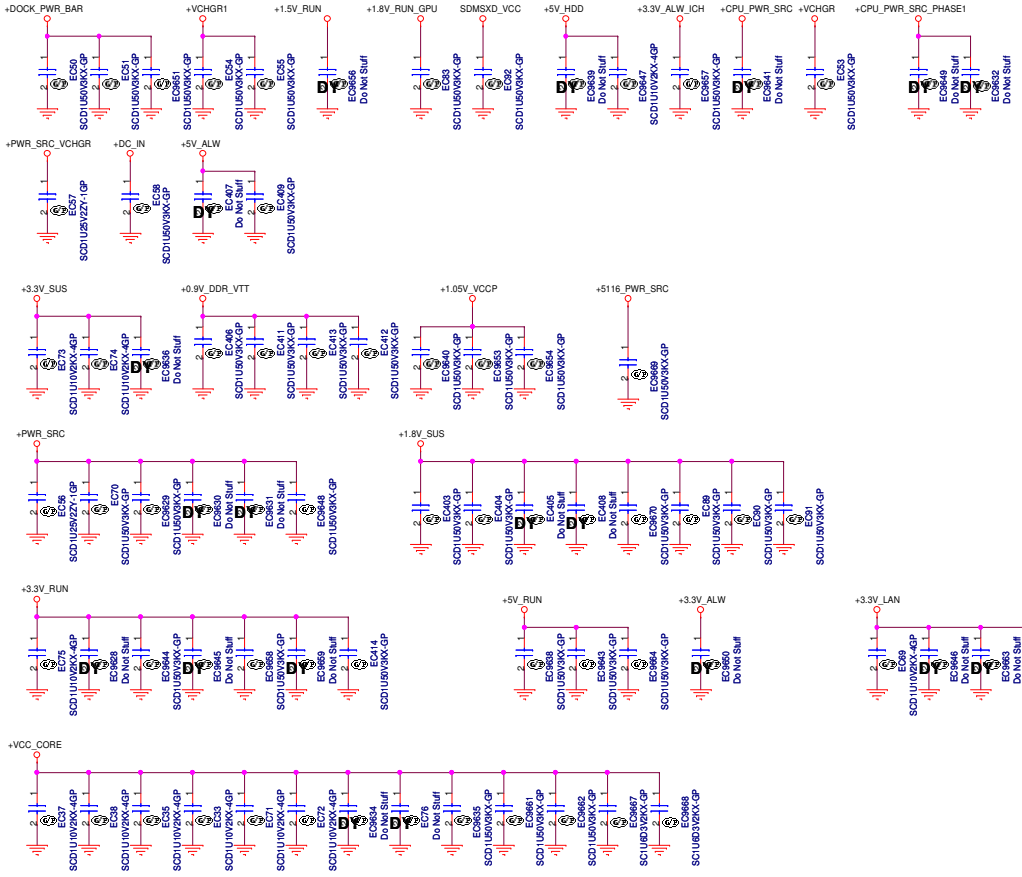
Title: Foose Intel Discrete

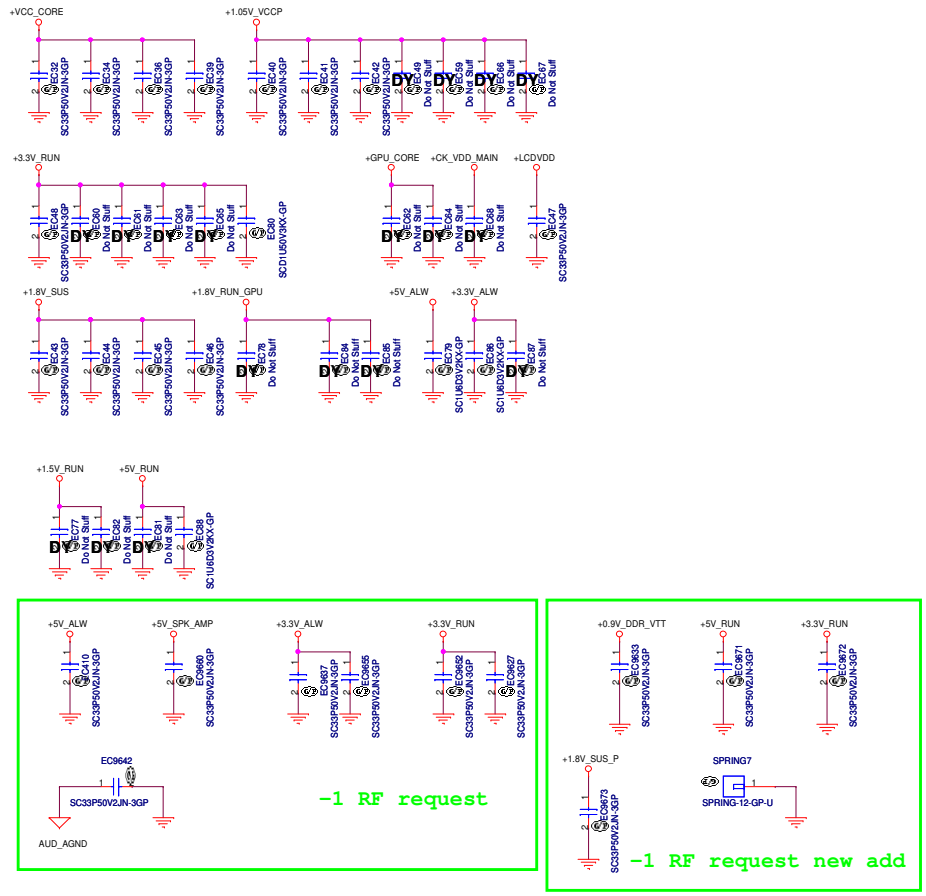
Size	Document Number	Rev
C	Reserve	-1

Date: Tuesday, April 07, 2009 Sheet 69 of 79

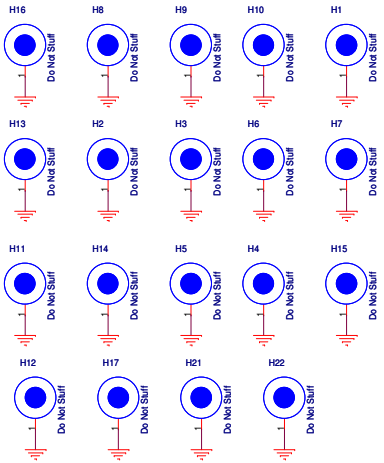
For EMI



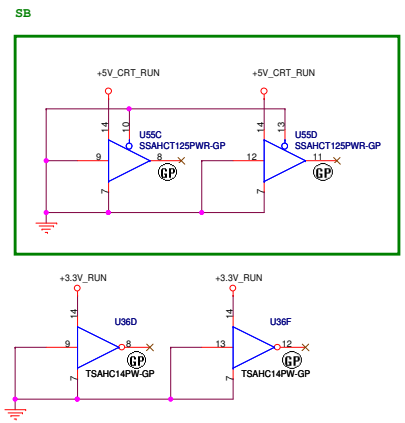
For RF



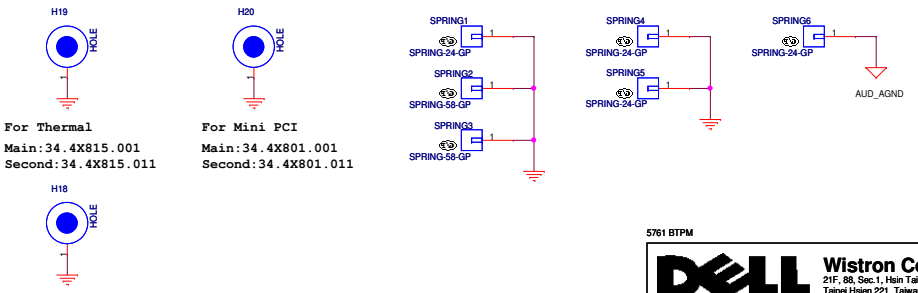
SSID = Mechanical



SSID = VIDEO



SSID = Mechanical



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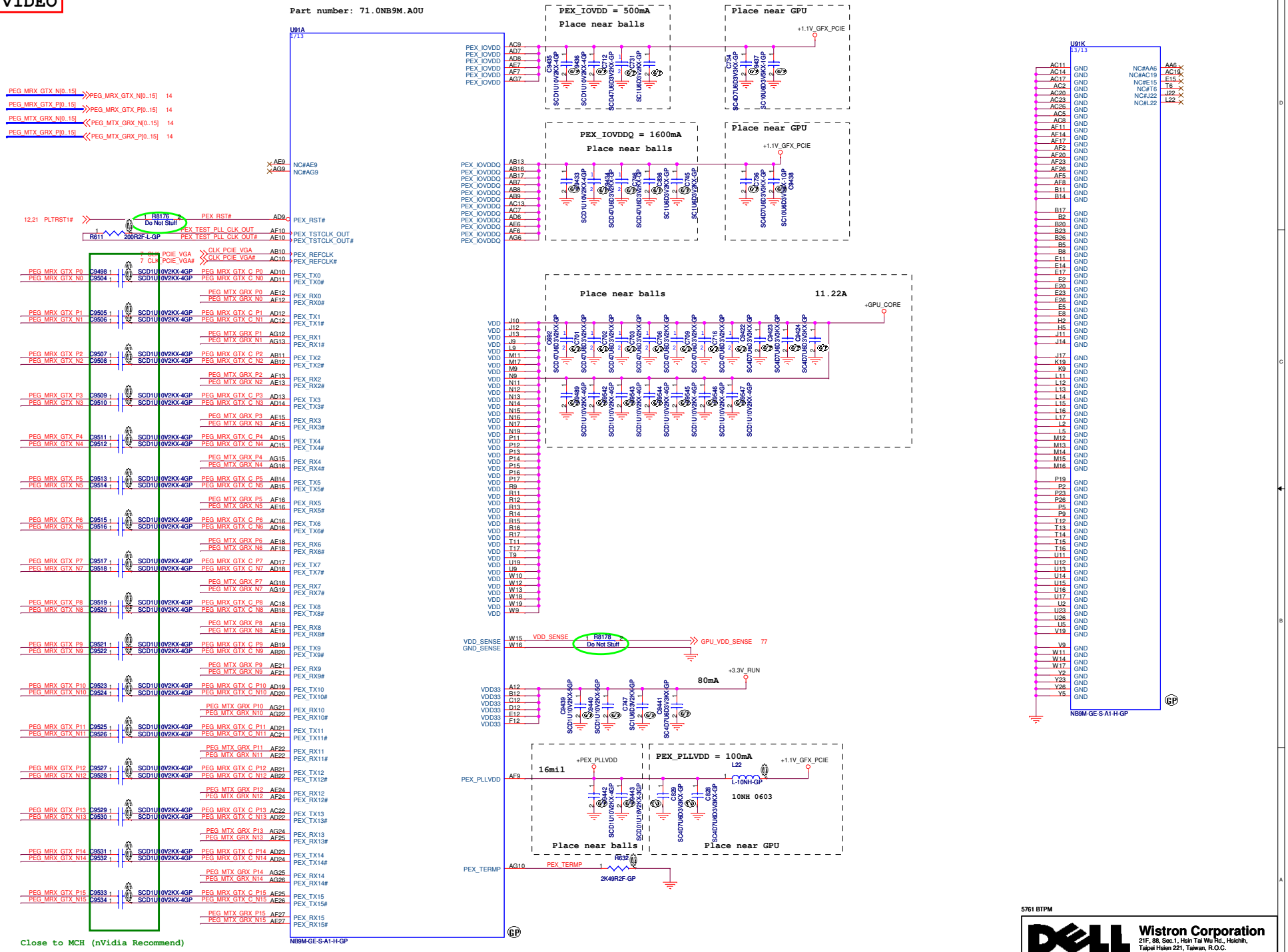
Title: *Foose Intel Discrete*

Size: C | Document Number: *Unused Parts/EMI RF CAPs* | Rev: -1

Date: Tuesday, April 07, 2009 | Sheet 70 of 79

SSID = VIDEO

Part number: 71.0NB9M.A0U



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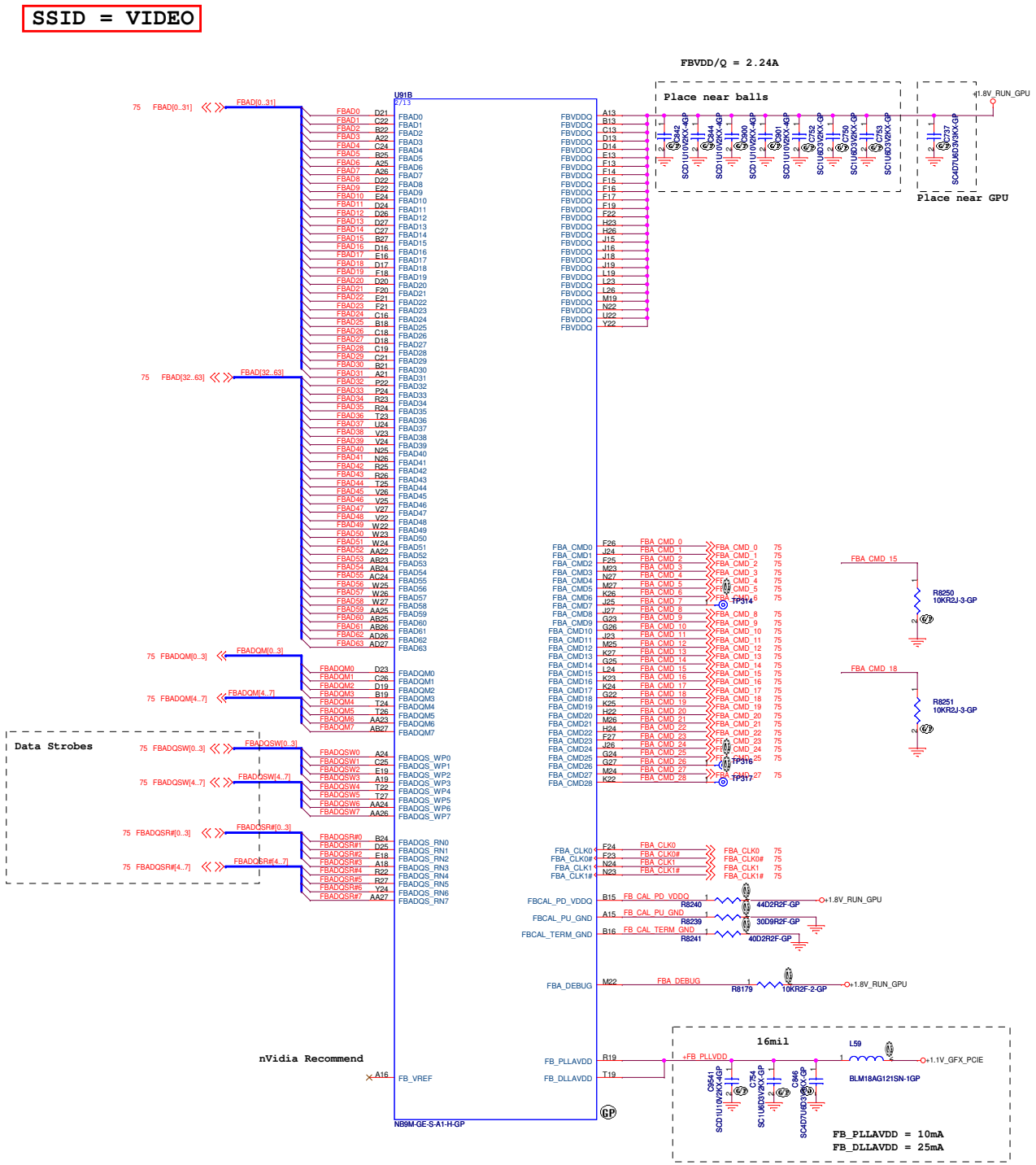
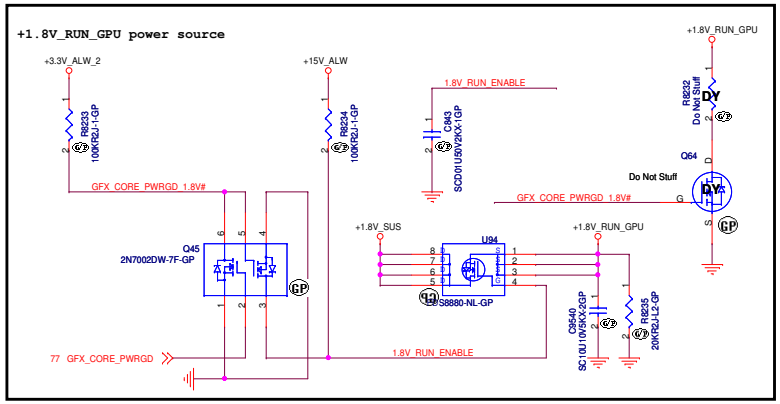
Title: Foose Intel Discrete

Size	Document Number	Rev
C	VGA PCIE(1/4)	-1

Date: Tuesday, April 07, 2009 Sheet 71 of 79

SSID = VIDEO





Mapping Mode B

	0-31	31-63	
CMD0	A4		
CMD1	RAS*	RAS*	
CMD2	A5		
CMD3	BA1	BA1	
CMD4		A2	
CMD5		A4	
CMD6		A3	
CMD7	CS1*	CS1*	NO USE
CMD8	CS0*	CS0*	
CMD9	A11	A11	
CMD10	CAS*	CAS*	
CMD11	WE*	WE*	
CMD12	BA0	BA0	
CMD13		A5	
CMD14	A12	A12	
CMD15	RST/ODT	RST/ODT	
CMD16	A7	A7	
CMD17	A10	A10	
CMD18	CKE	CKE	
CMD19	A0	A0	
CMD20	A9	A9	
CMD21	A6	A6	
CMD22	A2		
CMD23	A8	A8	
CMD24	A3		
CMD25	A1	A1	
CMD26	A13	A13	NO USE
CMD27	BA2	BA2	

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Title: *Foose Intel Discrete*

Size	Document Number	Rev
C	VGA VRAM(2/4)	-1

Date: Tuesday, April 07, 2009 Sheet 72 of 79

SSID = VIDEO

GPU_PLLVDD = 65mA

Single end

Design Guide is 2.2Kohm

Part number: 72.24C16.Z01

SB: Change to SO8 package

IFPCE_IOVDD = 385mA
IFPCE_PLLVDD = 160mA

Close to Docking connector (nVidia Recommend)

Close to Docking connector (nVidia Recommend)

Strap pin resistor need use 1% resistor (NV Design Guide)

Strap pin define

Logical Strap Bit Mapping

Resistor	Pull-Up	Pull-Down
5Kohms	1000	0000
10Kohms	1001	0001
15Kohms	1010	0010
20Kohms	1011	0011
25Kohms	1100	0100
30Kohms	1101	0101
35Kohms	1110	0110
45Kohms	1111	0111

Strap0		Strap1		Strap2	
USER_BIT0	1	3GIO_PADCFG_LUT_ADR0	1	PCI_DEVID_0	0
USER_BIT1	1	3GIO_PADCFG_LUT_ADR1	0	PCI_DEVID_1	0
USER_BIT2	1	3GIO_PADCFG_LUT_ADR2	0	PCI_DEVID_2	0
USER_BIT3	1	3GIO_PADCFG_LUT_ADR3	0	PCI_DEVID_3	1
EDID is used		Notebook POR		NB9M-GE = 0x606E8	

ROM_SI_GPU	ROM_SO_GPU		ROM_SCLK_GPU
RAM_CFG0	TV_MODE_BIT0	0	PEX_PLL_EN_TERM100 0
RAM_CFG1	TV_MODE_BIT1	0	SLOT_CLK_CONFIG 1
RAM_CFG2	TV_MODE_BIT2	0	SUB_VENDOR 0
RAM_CFG3	XCLK_277	1	PCI_DEVID_EXT 0

Default setting: SAMSUNG 32MX32BIT

RAM_CFG[3:0]	Config	FB_BUS Width	Definitions
0000		64Bit	Reserved
0001	16MX32 GDDR3	64Bit	Qimonda
0010	16MX32 GDDR3	64Bit	Hynix
0011	16MX32 GDDR3	64Bit	Samsung
0100		64Bit	Reserved
0101	32MX32 GDDR3	64Bit	Qimonda
0110	32MX32 GDDR3	64Bit	Hynix
0111	32MX32 GDDR3	64Bit	Samsung

If use Qimonda 32MX32BIT, R8227 change to 30Kohm (64.30025.6DL)

SUB_VENDOR	XCLK_277	PEX_PLL_EN_TERM
0 No VBIOS ROM	0 Reserved	0 Disable (POR)
1 BIOS ROM present	1 27MHz(POR)	1 Enable

3GIO_PADCFG	USER[3:0]
0000 Desktop	1111 Use EDID to detect panel settings
0001 Notebook (POR)	

SLOT_CLOCK_CFG
0 GPU and MCH do not share a common reference clock
1 GPU and MCH share a common reference clock (POR)

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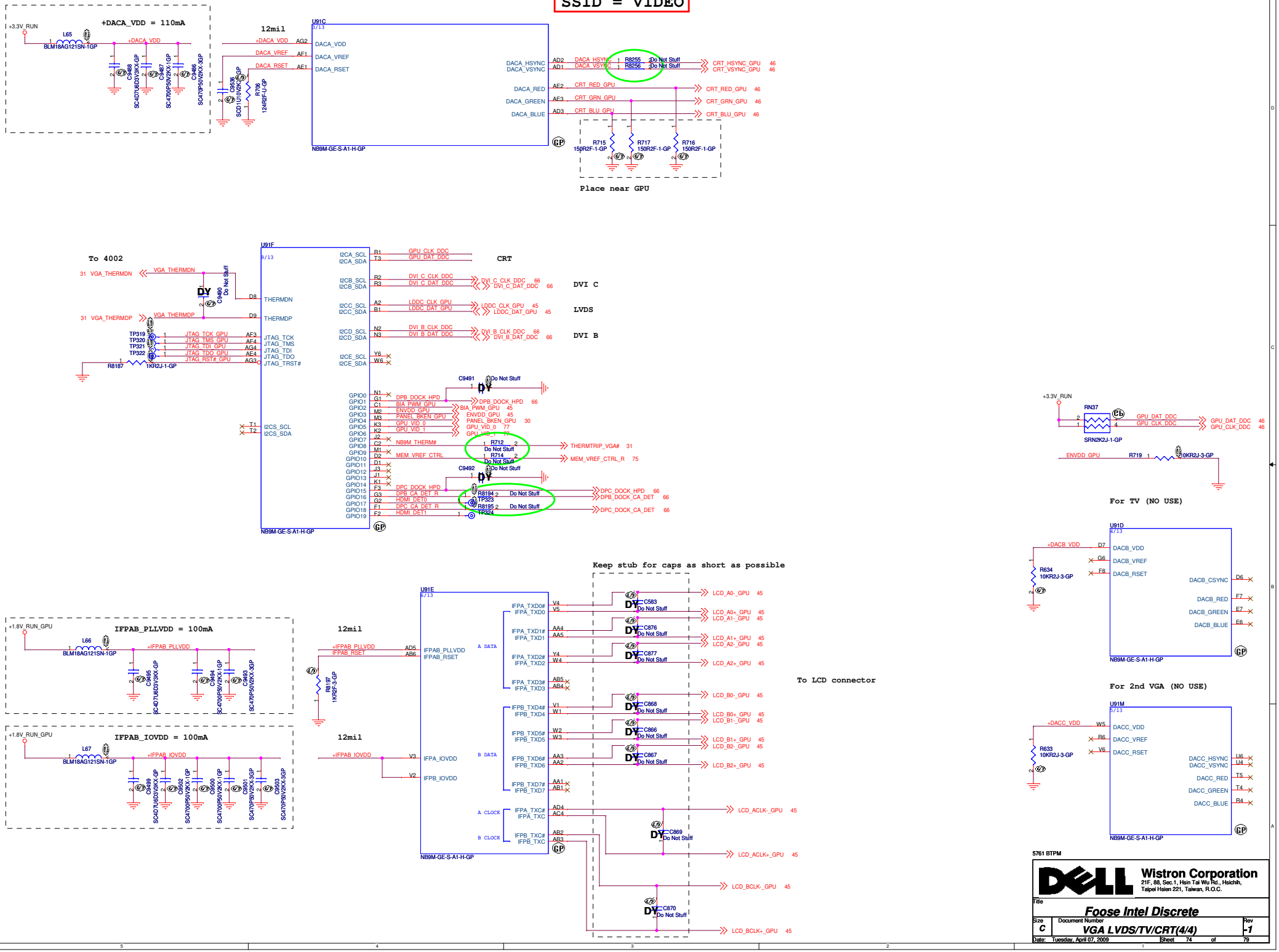
SSID = VIDEO


+DACA_VDD = 110mA
+3.3V_RUN
L65
BLM18AG121SN-1GP
+DACA_VDD
C9488
SC4D7U6D3V3KX-GP
C9487
SC470P50V2KX-1GP
C9486
SC470P50V2KX-3GP
12mil
+DACA_VDD
DACA_VREF
DACA_RSET
C9535
SCD1U10V2KX-GP
R708
124R2F-U-GP
U91C
9/13
DACA_VDD
DACA_VREF
DACA_RSET
AG2
AF1
AE1
DACA_HSYNC
DACA_VSYNC
DACA_RED
DACA_GREEN
DACA_BLUE
AD2
AD1
AE2
AE3
AD3
R8255
R8256
Do Not Stuff
CRT_HSYNC_GPU
CRT_VSYNC_GPU
CRT_RED_GPU
CRT_GRN_GPU
CRT_BLU_GPU
46
NB9M-GE-S-A1-H-GP
R715
150R2F-1-GP
R717
150R2F-1-GP
R716
150R2F-1-GP
Place near GPU
To 4002
31 VGA_THERMDN
31 VGA_THERMDP
VGA_THERMDN
VGA_THERMDP
C9490
Do Not Stuff
D8
D9
THERMDN
THERMDP
TP319
TP320
TP321
TP322
JTAG_TCK_GPU
JTAG_TMS_GPU
JTAG_TDI_GPU
JTAG_TDO_GPU
JTAG_RST#_GPU
AF3
AF4
AG4
AE4
AG3
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TRST#
R8187
1KR2J-1-GP
U91F
9/13
I2CA_SCL
I2CA_SDA
I2CB_SCL
I2CB_SDA
I2CC_SCL
I2CC_SDA
I2CD_SCL
I2CD_SDA
I2CE_SCL
I2CE_SDA
I2CS_SCL
I2CS_SDA
R1
T3
R2
R3
A2
B1
N2
N3
Y6
W6
T1
T2
GPU_CLK_DDC
GPU_DAT_DDC
DVI_C_CLK_DDC
DVI_C_DAT_DDC
LDDC_CLK_GPU
LDDC_DAT_GPU
DVI_B_CLK_DDC
DVI_B_DAT_DDC
CRT
DVI C
LVDS
DVI B
C9491
C9492
Do Not Stuff
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
GPIO16
GPIO17
GPIO18
GPIO19
N1
G1
C1
M2
M3
K3
K2
J2
C2
M1
D2
D1
J3
J1
K1
F3
G3
G2
F1
F2
DPB_DOCK_HPD
BIA_PWM_GPU
ENVDD_GPU
PANEL_BKEN_GPU
GPU_VID_0
GPU_VID_1
NB9M_THERM#
MEM_VREF_CTRL
DPC_DOCK_HPD
DPB_CA_DET_R
HDMI_DET0
DPC_CA_DET_R
HDMI_DET1
R712
R714
R8194
R8195
TP323
TP324
THERMTRIP_VGA#
MEM_VREF_CTRL_R
DPC_DOCK_CA_DET
NB9M-GE-S-A1-H-GP
+3.3V_RUN
RN37
SRN2K2J-1-GP
ENVDD_GPU
R719
10KR2J-3-GP
For TV (NO USE)
U91D
4/13
+DACB_VDD
R634
10KR2J-3-GP
DACB_VDD
DACB_VREF
DACB_RSET
DACB_CSYNC
DACB_RED
DACB_GREEN
DACB_BLUE
D7
G6
F8
D6
F7
E7
E6
NB9M-GE-S-A1-H-GP
For 2nd VGA (NO USE)
U91M
5/13
+DACC_VDD
R633
10KR2J-3-GP
DACC_VDD
DACC_VREF
DACC_RSET
DACC_HSYNC
DACC_VSYNC
DACC_RED
DACC_GREEN
DACC_BLUE
W5
R6
V6
U6
U4
T5
T4
R4
NB9M-GE-S-A1-H-GP
+1.8V_RUN_GPU
IFPAB_PLLVDD = 100mA
L66
BLM18AG121SN-1GP
+IFPAB_PLLVDD
C9495
SC4D7U6D3V3KX-GP
C9494
SC470P50V2KX-1GP
C9493
SC470P50V2KX-3GP
+1.8V_RUN_GPU
IFPAB_IOVDD = 100mA
L67
BLM18AG121SN-1GP
+IFPAB_IOVDD
C9499
SC4D7U6D3V3KX-GP
C9502
SC470P50V2KX-1GP
C9500
SC470P50V2KX-1GP
C9501
SC470P50V2KX-3GP
C9503
SC470P50V2KX-3GP
Keep stub for caps as short as possible
12mil
+IFPAB_PLLVDD
IFPAB_RSET
R8197
1KR2F-3-GP
12mil
+IFPAB_IOVDD
U91E
6/13
IFPAB_PLLVDD
IFPAB_RSET
IFPA_IOVDD
IFPB_IOVDD
AD5
AB6
V3
V2
A DATA
B DATA
A CLOCK
B CLOCK
IFPA_TXD0#
IFPA_TXD1#
IFPA_TXD2#
IFPA_TXD3#
IFPB_TXD4#
IFPB_TXD5#
IFPB_TXD6#
IFPB_TXD7#
IFPA_TXC#
IFPB_TXC#
V4
V5
AA4
AA5
Y4
W4
AB5
AB4
V1
W1
W2
W3
AA3
AA2
AA1
AB1
AD4
AC4
AB2
AB3
C583
C876
C877
C868
C866
C867
C869
C870
Do Not Stuff
LCD_A0-_GPU
LCD_A0+_GPU
LCD_A1-_GPU
LCD_A1+_GPU
LCD_A2-_GPU
LCD_A2+_GPU
LCD_B0-_GPU
LCD_B0+_GPU
LCD_B1-_GPU
LCD_B1+_GPU
LCD_B2-_GPU
LCD_B2+_GPU
LCD_ACLK-_GPU
LCD_ACLK+_GPU
LCD_BCLK-_GPU
LCD_BCLK+_GPU
45
To LCD connector
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Title
Foose Intel Discrete
Size
C
Document Number
VGA LVDS/TV/CRT(4/4)
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SSID = VIDEO

VRAM2 NONMIRRORED

VRAM1 MIRRORED

32M*32BIT
72.41032.C0U(F001C$AA) SAMSUNG GDDR3 32M*32BIT
72.18321.B0U QIMONDA GDDR3 32M*32BIT(Disqualified)

Low power VREF switch

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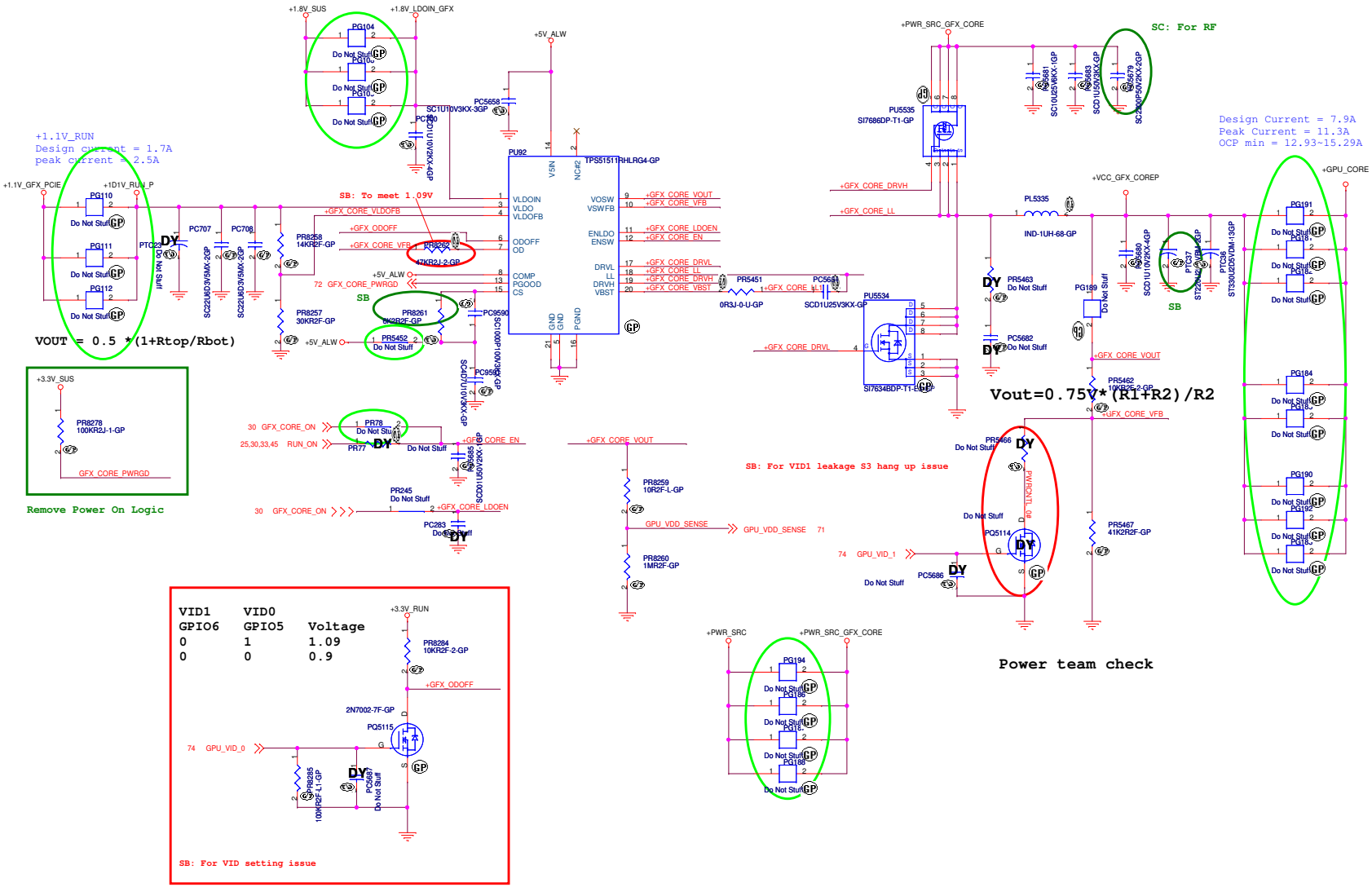
SSID = PWR.Plane.Regulator_GFX



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C	Reserve	-1

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Version Change List

Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
1	51	20081215	Wistron	Display port and HDMI no sound/ HDCP key fail	Change HDCP ROM package to SO8	
2	36	20081215	Wistron	Can't read VGA temperature from 4002 diode5	Swap VGA thermal DP/DN to match 4002 Dide5	
3	34, 46	20081215	Wistron	Boot fail/ RTC stop issue	Connect RUNPWROK to 1.05V_PWRGD	
4	55	20081215	Wistron	GPU_CORE can't meet 1.09V	Change PR8262 to 47K	
5	55	20081215	Wistron	GPU_VID_1 leakage and S3 hang up issue	Add inverter circuit for GPU_VID_0 and dummy PQ5114 and PR5466	
6	40	20081215	Wistron	Fine tune +3.3V_RUN sequence	Change C230 to 1000pF	
7	18	20081215	Wistron	MAX4885E doesn't have leakage	Remove D954	
8	19	20081215	Wistron	Prevent connector CCD1 pin1 power pin short to GND issue	Add 10ohm between pin1 and GND	
9	19	20081217	Wistron	WebCAM power control circuit is unnecessary	Dummy WebCAM power control circuit	
10	18	20081217	Wistron	CRT EA HSYNC/VSYNC fall time fail	Add buffer for HSYNC/VSYNC	
11	30	20081225	Wistron	WLAN/WWAN reset EA fail	Change R101 to 120ohm and R337 to 100ohm	
12	48	20081225	Wistron		Add EMI CAPs	
13	46	20081229	Wistron		Add L6935 as 1.5V power second source	
14	48	20081230	Wistron		Add EMI/RF CAPs	
15	43, 46, 47, 55	20081231	Wistron		Change PR441,PR290,PR8261, PC23 resistor value	
16	26	20090212	Wistron	For R5U241 ES2 sample	Change R5U241 power CAPs to 0.1uF for ES2 sample and install R99/R100 and dummy R110/R108	
17	26	20090223	DELL	For TCM circuit update	Change R5350&R5351 to 1K, dummy R347, remove R8171	
18	54	20090224	DELL	For USB power share circuit update	Change C146 to 2.2uF	
19	70	20090225	Wistron		Add EMI/RF input	
20	70	20090227	Wistron	For SD card issue	Change R8273/R8274/R8275/R8276/R8277 to 68.00084.C21	
21	61	20090330	Wistron	For RF noise	Change R505 to 64.49R95.6DL C566 to 78.8R274.1F1	-1
22	28	20090401	DELL	For TCM circuit update	Change C6387 to 78.10424.2BL and dummy R8149	-1
23	24	20090401	Wistron	For RF noise	Add RF CAP change R467 R505 to 64.49R95.6DL Change C67 C566 to 78.8R274.1F1	-1
24	70	20090402	Wistron	For RF noise	Add RF CAPs and SPRING7	-1
25	37	20090407	Wistron	For Power team request	Dummy PD46	-1
26	60	20090407	Wistron	Dummy FP1	Dummy FP1	-1

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Date: Wednesday, April 08, 2009 | Sheet 79 of 79