First International Computer,Inc

Portable Computer Group HW Department

Board name : MotherBoard Schematic

Project : **MR055 / MR056**

Version : 0.2

Initial Date : May. 04 , 2007

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2. PCI & IRQ & DMA Description :
3. Block Diagram :
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1. Schematic Page Description :

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2. PCI & IRQ & DMA Description :

IDSEL	CHIP
AD17	Mini PCI (Wireless LAN)
AD27	X
AD29	Lan (Realtek RTL8101L)

BUSMASTER

REQ	CHIP
REQ0 / GNT0	X
REQ1 / GNT1	LAN (Realtek RTL8101L)
REQ2 / GNT2	X
REQ3 / GNT3	X
REQ4 / GNT4	X

IRQ Channel	Desciption
IRQ0	System timer
IRQ1	Keyboard
IRQ2	(Casacde)
IRQ3	LAN / MODEM
IRQ4	~~Serial Port~~
IRQ5	AUDIO / VGA / USB
IRQ6	~~FLOPPY DISK~~
IRQ7	~~LPT~~
IRQ8	RTC
IRQ9	ACPI
IRQ10	FIR (Disable by default) (MODEM/LAN)
IRQ11	~~Cardbus~~
IRQ12	PS/2 mouse
IRQ13	FPU
IRQ14	HDD
IRQ15	CDROM

DMA Channel	Device
DMA0	FIR (disable by default) (MODEM / LAN)
DMA1	~~ECP~~
DMA2	~~FLOPPY DISK~~
DMA3	AUDIO
DMA4	(Cascade)
DMA5	Unused
DMA6	Unused
DMA7	Unused

PCIINT	CHIP
IRQA	IEEE1394 (VIA VT6311S)
IRQB	LAN (Realtek RTL8101L)
IRQC	X
IRQD	X
IRQE / GPIO2	LAN (Realtek RTL8101L)
IRQE / GPIO3	X
IRQE / GPIO4	PASS0
IRQE / GPIO5	CRISIS

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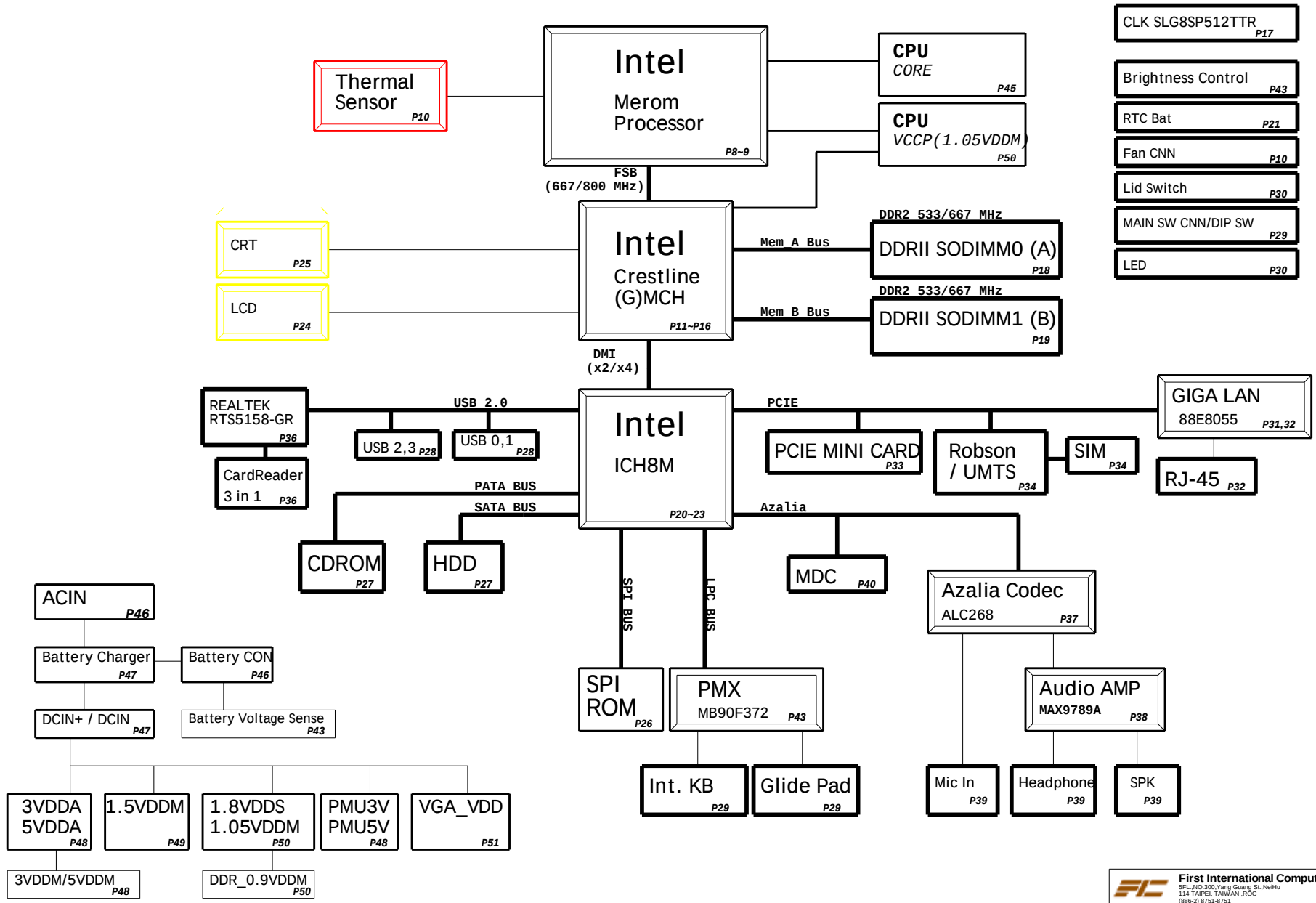
3. Block Diagram :



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4. Nat name Description :

Voltage Rails

DCIN	Primary DC system power supply
PMU5V	5.0V always on power rail by LATCH or ACIN
PMU3V	3.3V always on power rail by LATCH or ACIN
5VDDA	5.0V always on power rail by DCON
3VDDA	3.3V always on power rail by DCON
3VDDS	3.3V power rail by PSUSC#
5VDDS	5.0V power rail by PSUSC#
3VDDM	3.3V switched power rail by SUSTAT_B#
5VDDM	5.0V switched power rail by SUSTAT_B#
VCC_CORE	Core Voltage for CPU
1.05VDDM	1.05V power rail for AGTL+ termination/Core for GMCH by SUSTAT_B#
1.5VDDM	1.5V power rail for CPU PLL/DMI;PCIE;DDRII DLLs for GMCH/Core;PCIE for ICH7m by SUSTAT_B#
1.8VDDS	1.8V power rail for DDRII by PSUSC#
0.9VDDT_DDRII	0.9V DDRII Termination Voltage by SUSTAT_B#

Part Naming Conventions

C = Capacitor
CN = Connector
D = Diode
F = Fuse
L = Inductor
Q = Transistor
R = Resistor
RP = Resistor Pack
U = Arbitrary Logic Device
Y = Crystal and Osc

Net Name Suffix

= Active Low signal

5. Board Stack up Description

PCB Layers

Layer 1	Component Side, Microstrip signal Layer
Layer 2	Ground Plane
Layer 3	Stripline Layer(High Speed)
Layer 4	Stripline Layer(High Speed)
Layer 5	Power Plane
Layer 6	Solder Side,Microstrip signal Layer

	Single End Impedance	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
SRC Clock	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
Host Bus	55 ohm +/- 15%		
DDR2 CLK	42 ohm +/- 15%	70 ohm +/- 20%	70 ohm +/- 20%
DDR2 Strobe	55 ohm +/- 15%		85 ohm +/- 20%
DDR2 Bus	55 ohm +/- 15%		
DMI Bus	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
PCIE Bus	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
SATA		95 ohm +/- 15%	100 ohm +/- 15%
SDVO	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
LVDS		100 ohm +/- 15%	100 ohm +/- 15%
USB		90 ohm +/- 15%	90 ohm +/- 15%
IEEE1394		110 ohm +/- 15%	110 ohm +/- 15%
Lan	50 ohm +/- 15%		

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6.Schematic modify Item and History :

Power Rail	Ball Name	Destination	Voltage	S0 Current
VCC_CORE		Merom HFM: LFM:	1.0375V~?~1.3000V TBD~TBD	44A TBD
1.05VDDM	VCCP VTT(VCCP) VCC VCC_PEG VCCR_RX_DMI VCC_AXM VCC1_05 VCCSUS1_05 VCCCL1_05 VCCLAN1_05	Merom: AGTL+ termination Crestline: AGTL+ termination Crestline: Core chipset Crestline: PCI Express Based Graphics Crestline: Rx and I/O Logic for DMI Crestline: Controller Link/ME voltage supply ICH8M: ICH8 Core ICH8M: ICH8M: ICH8M:	1.00V~1.05V~1.10V 0.9975V~1.05V~1.1025V 0.9975V~1.05V~1.1025V	4.5A 0.8A 1.3A
1.25VDDM	VCCA_SM VCCA_SM_CK VCCA_PEG_PLL VCCD_PEG_PLL VCC_DMI VCCA_HPLL VCCD_HPLL VCCA_MPLL VCCA_DPLLA VCCA_DPLLB VCC_AXG VCC_AXF VCC_DMI	Crestline: Crestline: Crestline: Crestline: Crestline: Crestline: Crestline: Crestline: Crestline: Crestline: Crestline: Crestline: ICH8M:		
1.5VDDM	VCCA VCCD_QDAC VCCD_TVDAC VCCD_CRT VCCD_QDAC VCC1_5_A VCC1_5_B VCCSUS1_5 VCCGLAN1_5 VCCCL1_5 VCCUSBPLL VCCDMIPLL VCCSATAPLL VCCGLANPLL +1.5V TBD	Merom PLL Crestline: TV DAC Crestline: TV DAC Crestline: CRT Crestline: CRT ICH8M: I/O ICH8M: I/O ICH8M: Resume well I/O ICH8M: Integrated Gigabit LAN I/O ICH8M: Controller Link ICH8M: USB PLL ICH8M: DMI PLL ICH8M: SATA PLL ICH8M: Integrated Gigabit LAN PLL Mini Card: Express Card:	1.425V~1.5V~1.575V 1.425V~1.5V~1.575V 1.425V~1.5V~1.575V 1.425V~1.5V~1.575V 1.425V~1.5V~1.575V 1.7V~1.8V~1.9V	130mA 1.5A 60mA 24mA 320mA
1.8VDDS:	VCC_SM VCC_SM_CK VCCD_LVDS VCC_TX_LVDS VCCA_LVDS 1.8VDDS:	Crestline: I/O Voltage Crestline: Clock I/O Voltage Crestline: Crestline: Crestline: SO-DIMM:		3.1A
0.9VDDT_DDRII:		DDRII Terminator:	0.855V~0.9V~0.945V	1.0A

Need Modify

Power Rail	Ball Name	Destination	Voltage	S0 Current
2.5VDDM		945GM: PCIE analog 945GM: LVDS analog 945GM: LVDS I/O 945GM: CRT DAC CH7307:	2.32V~2.5V~2.625V 2.375V~2.5V~2.625V 2.375V~2.5V~2.625V 2.32V~2.5V~2.625V	2mA 10mA 60mA 70mA
3VDDM	VCCA_PEG_BG VCC_HV VCC_SYNC VCCA_CRT_DAC VCCA_TVA_DAC VCCA_TVB_DAC VCCA_TVC_DAC VCCA_DAC_BG	Crestline: PCI Express Base Graphics Crestline: HV buffer power Crestline: H/VSYNC power Crestline: CRT DAC Crestline: TV Out Crestline: TV Out Crestline: TV Out Crestline: TV DAC ICH7m: Mini Card: Express Card: CLK Generator: ICS954226 KBC: KB3886 Flash ROM: BIOS Azalia Codec: ALC260 Azalia MDC: HDD: SATA	3.135V~3.3V~3.465V 3.135V~3.3V~3.465V 3.135V~3.3V~3.465V 3.0V~3.3V~3.6V	40mA 120mA 400mA
3VDDS		Lan: Broadcom BCM4401 Card Reader: SD/MMC/MS Azalia MDC: For wake up	3.0V~3.3V~3.6V	
3VDDA		ICH7m: ICH7m: ICH7m: LCD:	 3.0V~3.3V~3.6V	 1.0A
5VDDM		Azalia Codec: ALC260 Azalia MDC: HDD: SATA ODD: PATA Audio AMP: G1420 Inverter:	3.0V~3.3V~3.6V 4.75V~5.0V~5.25V 4.75V~5.0V~5.25V	 Max: 1.0A ; R/W Max: 1.8A ; R/W: 900mA
5VDDS		USB: x 4 ports	5V	2.0A
PMU3V		EC: PMU08 ICH7m: RTC		

Page22 RF_ON# change to RF_ON
Page22 UMTS_ON change to UMTS_OFF#
Page43 VOR0 change to VOR#

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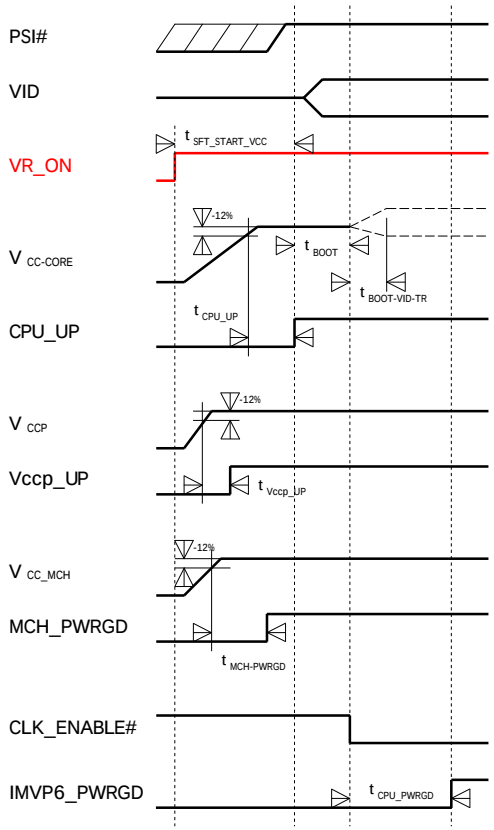
7. power on & off & S3 Sequence :

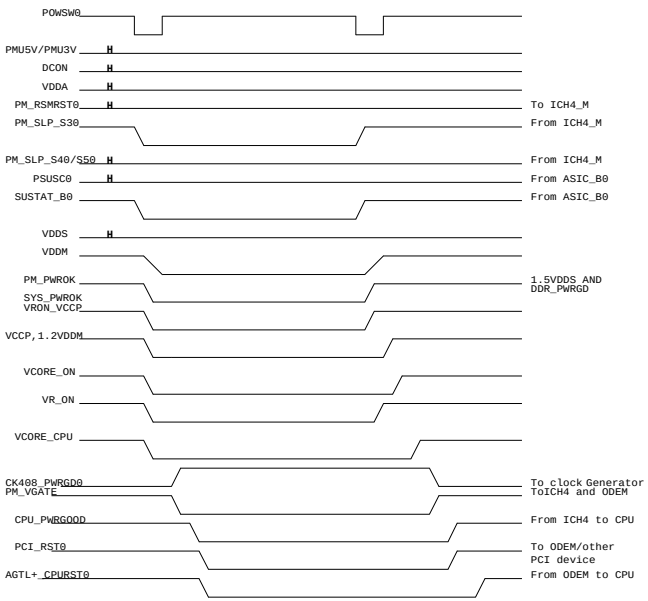
Power On Sequencing Timing Diag ram

20060117A - DATA FROM NO.16809

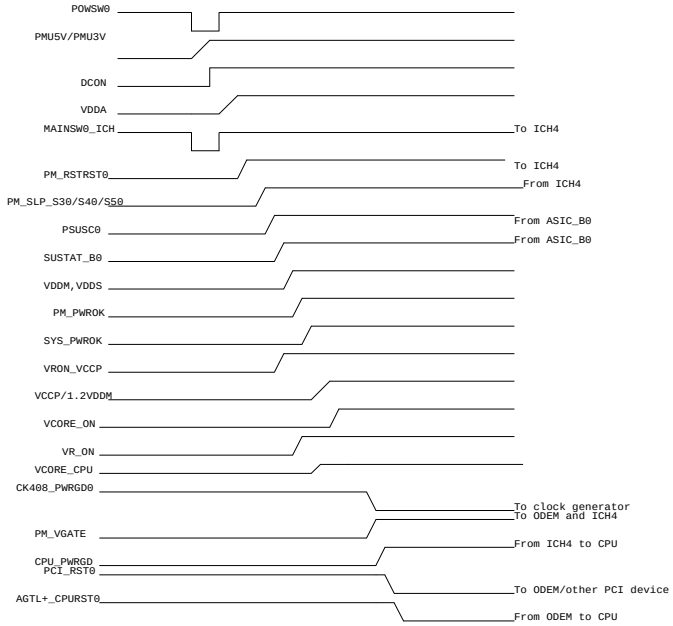


$t_{SFT\_START\_VCC}$	Max = 3 ms
t_{BOOT}	Min = 10 us , Max = 100 us
$t_{BOOT-VID-TR}$	Max = 100 us
t_{CPU_UP}	Min = 10 us , Max = 30 us
t_{Vccp_UP}	Min = 10 us , Max = 30 us
$t_{MCH-PWRGD}$	Min = 10 us , Max = 30 us
t_{CPU_PWRGD}	Min = 3 ms , Max = 20 ms

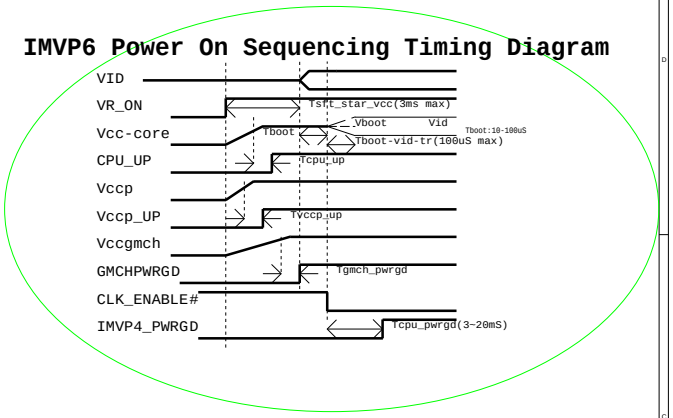
S3 SUSPEND AND RESUME TIMING



BATTERY ONLY POWER ON TIMING



IMVP6 Power On Sequencing Timing Diagram



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8. Layout Guideline :

Crestline DDRII Layout Guidelines

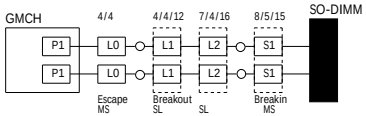
DDRII Signal Groups

Group	Signal Name
Data	SA_DQ[63..0]/SB_DQ[63..0] SA_DM[7..0]/SB_DM[7..0] SA_DQS[7..0]/SA_DQS#[7..0] SB_DQS[7..0]/SB_DQS#[7..0]
Address	SA_MA[13..0]/SB_MA[13..0] SA_BS[2..0]/SB_BS[2..0] SA_RAS#/SB_RAS# SA_CAS#/SB_CAS# SA_WE#/SB_WE#
Control	SM_CS#[3..0] SM_CKE[3..0] SM_ODT[3..0]
Clock	SM_CK[3..0] SM_CK#[3..0]
FeedBack	SA_RCVENOUT#/SB_RCVENOUT# SA_RCVENIN#/SB_RCVENIN#

Length Matching and Length Formulas

Signal Group	Minimum Length	Maximum Length
Control-to-Clock	Clock - 1.0"	Clock - 0.0"
Command-to-Clock	Clock - 1.0"	Clock + 1.0"
Strobe-to-Clock	Clock - 0.5"	Clock + 1.0"
Data-to-Strobe	Strobe - 220mils	Strobe - 180mils

CLK group : SM_CK[3..0],SM_CK#[3..0]

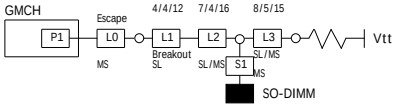


Topology	Differential Pair Point-to-Point
Reference Plane	Ground
Single Ended Trace Impedance	42 +/- 15%
Differential Mode Impedance	70 +/- 20%
Nominal Trace Width	Inner Layer : 7 mils Outer Layer : 8 mils
Nominal CK to CK# Spacing (edge to edge)	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum Serpentine Spacing	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Spacing to Other DDR2	Inner Layer : 16 mils Outer Layer : 20 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length Range - P1	1000 mils +/- 250 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1	Min = 500 mils Max = 4000 mils
Total Length - P1 + L0 + L1 + L2 + S1	Max = 4500 mils Total Length for Channel A : X0 Total Length for Channel B : X1
Maximim Via Count	2 (Per side)
SCK to SCK# Length Matching	Match total length to within 5 mils
Clock to Clock Length Match (Total Length)	Match Channel A clocks to X0 +/- 20mils Match Channel A clocks to X1 +/- 20mils
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4/12 mils to other DDR2 Outer Layer : 5/15 mils to other DDR2 Max. breakout length is 500 mils
Breakin Exceptions (Reduce geometries for SO-DIMM break-in region)	CK to CK# spacing rule waived at connector spacing of 15 mils to other DDR2 Max. breakin length is 200 mils

Feedback group : SA_RCVENIN#],SA_RCVENOUT#,SB_RCVENIN#],SB_RCVENOUT#

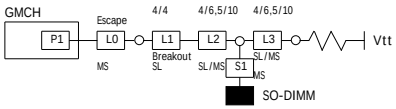
These signals are routed internally on the GMCH package and don't require any routing on the MB. As a result, can be left as NC.

Control group : SM_CKE[3..0],SM_CS#[3..0],SM_ODT[3..0]



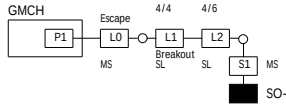
Topology	Point-to-Point with parallel termination
Reference Plane	Ground
Character istic Trace Impedance	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum CTRL Trace Spacing	Inner Layer : 8 mils Outer Layer : 10 mils
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length P1	750 mils +/- 200 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Parallel Termination Resistor	56 +/- 5%
Maximim Via Count	3
CTRL to SCK/SCK# Length Matching (Total Length including package)	(CLK-1.0") </= CTRL </= (CLK-0.0")
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Max. breakout length is 500 mils

Command group : SA_MA[13..0],SB_MA[13..0],SA_BS[2..0],SB_BS[2..0],SA_RAS#, SB_RAS#,SA_CAS#,SB_CAS#,SA_WE#,SB_WE#



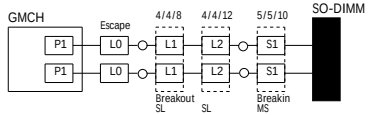
Topology	Point-to-Point with parallel termination
Reference Plane	Ground
Character istic Trace Impedance	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum CMD Bus Trace Spacing	Inner Layer : 6 mils Outer Layer : 10 mils
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length P1	750 mils +/- 350 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Parallel Termination Resistor	56 +/- 5%
Maximim Via Count	3
CTRL to SCK/SCK# Length Matching (Total Length including package)	(CLK-1.0") </= CMD </= (CLK+1.0")
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Max. breakout length is 500 mils

Data group : SA_DQ[63..0],SB_DQ[63..0],SA_DM[7..0],SB_DM[7..0]



Topology	Point-to-Point
Reference Plane	Ground
Characteristic Trace Impedance	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum DQ Bus Trace Spacing	Inner Layer : 6 mils Outer Layer : 8 mils
Minimum Serpentine Spacing	Same as DQ-to-DQ routing
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length P1	750 mils +/- 350 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Maximim Via Count	2
DQ/DM to DQS Length Matching (Total Length including package)	Match DQ/DM to [SDQS - 200mils] +/- 20mils, per byte lane
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Max. breakout length is 500 mils

Data Strobe group : SA_DQS[7..0],SA_DQS[7..0]#,SB_DQS[7..0],SB_DQS[7..0]#



Topology	Differential Pair Point-to-Point
Reference Plane	Ground
Single Ended Trace Impedance	55 +/- 15%
Differential Mode Impedance	85 +/- 20%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Nominal DQS to DQS# Spacing (edge to edge)	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum DQS to DQ Spacing	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Serpentine Spacing	Inner Layer : 8 mils Outer Layer : 10 mils
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length Range - P1	750 mils +/- 350 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Maximim Via Count	2 (Per side)
DQS to DQS# Length Matching	Match total length to within 5 mils
Clock to Clock Length Match (Total Length include package)	(CLK-0.5") </= DQS </= (CLK+1.0")
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 8 mils to other DDR2 Outer Layer : 10 mils to other DDR2 Max. breakout length is 500 mils
Breakin Exceptions (Reduce geometries for SO-DIMM break-in region)	DQS to DQS# spacing rule waived at connector spacing of 10 mils to other DDR2 Max. breakin length is 200 mils

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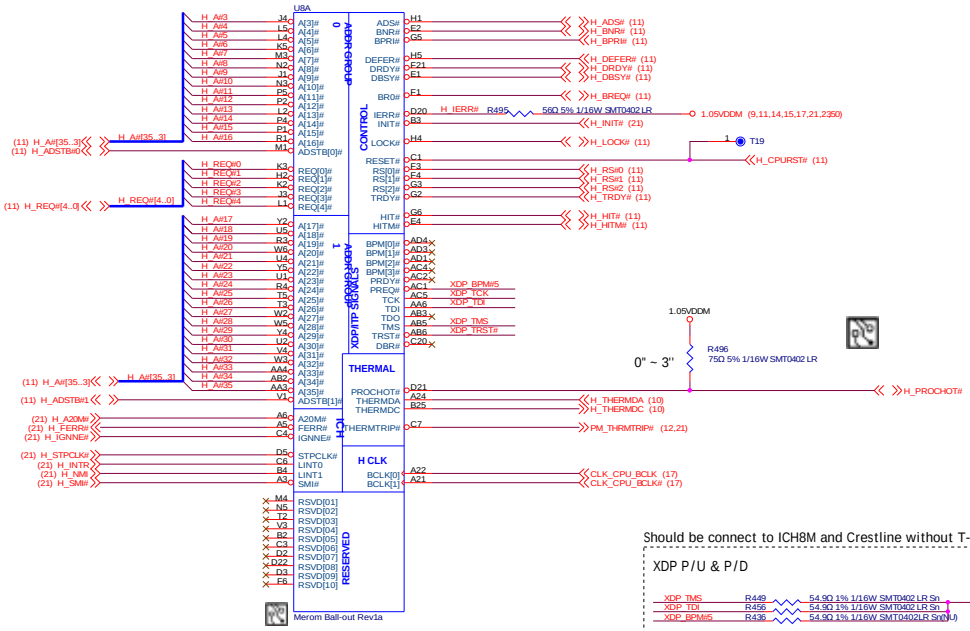
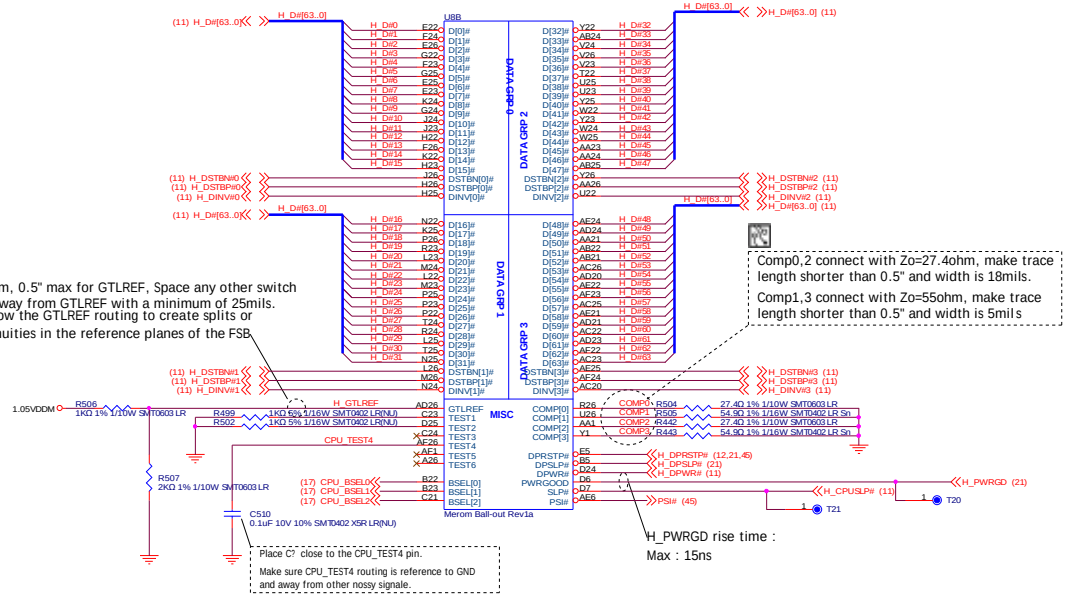


Rout to TP via and place gnd via w/in 100mils

A#[32-39], APM#[0-1]:Leave escape routing on for future functionality



Zo=55ohm, 0.5" max for GTLREF, Space any other switch signals away from GTLREF with a minimum of 25mils.
Don't allow the GTLREF routing to create splits or discontinuities in the reference planes of the FSB signals

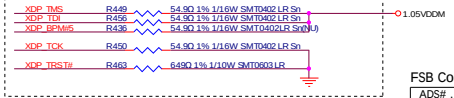
Comp0,2 connect with Zo=27.4ohm, make trace length shorter than 0.5" and width is 18mils.
Comp1,3 connect with Zo=55ohm, make trace length shorter than 0.5" and width is 5mils

Place C? close to the CPU_TEST4 pin.
Make sure CPU_TEST4 routing is reference to GND and away from other nossy signale.

H_PWRGD rise time :
Max : 15ns

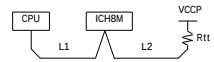
Should be connect to ICH8M and Crestline without T-ing(no stub)

XDP P/U & P/D

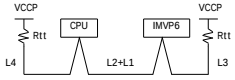


VCCP=1.05VDDM

Topology : FERR#

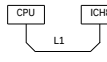


L1	L2	Rtt	Transmission Line
0.5" - 12"	0" - 3.0"	56 +/-5%	Microstrip
0.5" - 12"	0" - 3.0"	56 +/-5%	Stripline



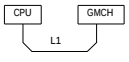
L1	L2	L3	L4	Rtt	Transmission Line
0.5" - 6.5"	0.5" - 6.5"	0" - 3.0"	0" - 3.0"	75 +/-5%	Micro-strip
0.5" - 6.5"	0.5" - 6.5"	0" - 3.0"	0" - 3.0"	75 +/-5%	Strip-line

Topology : PWRGOOD



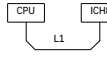
L1	Transmission Line
0.5" - 12"	Micro-strip
0.5" - 12"	Strip-line

Topology : CPUSLP#



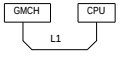
L1	Transmission Line
0.5" - 12"	Micro-strip
0.5" - 12"	Strip-line

Topology : INTR , NMI , A20M# , DPSLP# , IGNNE# , INIT# , SMI# , STPCLK#



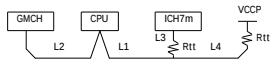
L1	Transmission Line
0.5" - 12"	Micro-strip
0.5" - 12"	Strip-line

Topology : RESET#



L1	Transmission Line
1" - 6"	Micro-strip
1" - 6"	Strip-line

Topology : THERMTRIP#



L1	L2	L1+L3	L3	L4	Rss	Rtt	Transmission Line
1" - 12"	1" - 6"	1" - 12"	0" - 3.0"	0" - 3.0"	24 +/-5%	56 +/-5%	Micro-strip
1" - 12"	1" - 6"	1" - 12"	0" - 3.0"	0" - 3.0"	24 +/-5%	56 +/-5%	Strip-line

Processor ITP Signal Default Strapping When ITP-XDP & ITP700FLEX Dedbug Port Not Used.

Signal	Resistor Value	Connect To	Resistor Placement
TDI	54.9 OHM +/-5%	VCCP	Within 2.0" of the CPU
TMS	54.9 OHM +/-5%	VCCP	Within 2.0" of the CPU
TRST#	649 OHM +/-5%	GND	Within 2.0" of the CPU
TCK	54.9 OHM +/-5%	GND	Within 2.0" of the CPU
TDO	OPEN	NC	N/A

FSB Common Clock Signal Layout Guide :

ADS# , BNR# , BPRI# , BR0# , DBSY# , DEFER# , DPWR# , DRDY# , HIT# , HITM# , LOCK# , RS[2..0]# , TRDY# , RESET#.

Transmission Line Type	Total Trace Length	Normal Impedance	Spacing (mils)
Strip-line(Int. Layer)	1.0 ~ 6.5 inch	55+/-15%	4 & 8 mils
Micro-strip(Ext. Layer)			5 & 10 mils

FSB Source Synchronous Data Length Variation and Strobe Matching Requirements :

Signals Name	Signals Matching	Strobes associated with the group	Strobe-to-Strobe Complement Matching
DATA#[15..0] , DINV0#	+/- 100 mils	DSTBP0#,DSTBN0#	+/- 25 mils
DATA#[31..16] , DINV1#	+/- 100 mils	DSTBP1#,DSTBN1#	+/- 25 mils
DATA#[47..32] , DINV2#	+/- 100 mils	DSTBP2#,DSTBN2#	+/- 25 mils
DATA#[63..48] , DINV3#	+/- 100 mils	DSTBP3#,DSTBN3#	+/- 25 mils

FSB Source Synchronous Data Signal Routing Topology#1 :

Signal Name	Transmission Line Type	Total Trace Length	Normal Impedance	Width & Spacing (mils)	
				Data-to-Data,Strobe-to-strobe	Strobe-to-Data
DINV#[3..0]	Strip-line	0.5 ~ 5.5 inch	55+/-15%	4 & 8 mils	N/A
DATA#[63..0]	Strip-line	0.5 ~ 5.5 inch	55+/-15%	4 & 8 mils	N/A
DSTBN#[3..0]	Strip-line	0.5 ~ 5.5 inch	55+/-15%	4 & 12 mils	4 & 12 mils
DSTBP#[3..0]	Strip-line	0.5 ~ 5.5 inch	55+/-15%	4 & 12 mils	4 & 12 mils

FSB Source Synchronous Address Length Variation and Strobe Matching Requirements :

Signals Name	Signals Matching	Strobes associated with the group	Strobe to Assoc. Address Signal Matching
A#[16..3] , REQ#[4..0]	+/- 200 mils	ADSTB0#	+/- 200 mils
A#[31..17]	+/- 200 mils	ADSTB1#	+/- 200 mils

*** No length matching requirements exist between ADSTB0# and ADSTB1#

FSB Source Synchronous Address Signal Routing :

Signal Name	Transmission Line Type	Total Trace Length	Normal Impedance	Width & Spacing (mils)
Address#[31..3]	Strip-line	0.5 ~ 6.5 inch	55+/-15%	4 & 8 mils
REQ#[4..0]	Strip-line	0.5 ~ 6.5 inch	55+/-15%	4 & 8 mils
ADSTB#[1..0]	Strip-line	0.5 ~ 6.5 inch	55+/-15%	4 & 8 mils

(9,11,14,15,17,21,23,50) 1.05VDDM — 1.05VDDM

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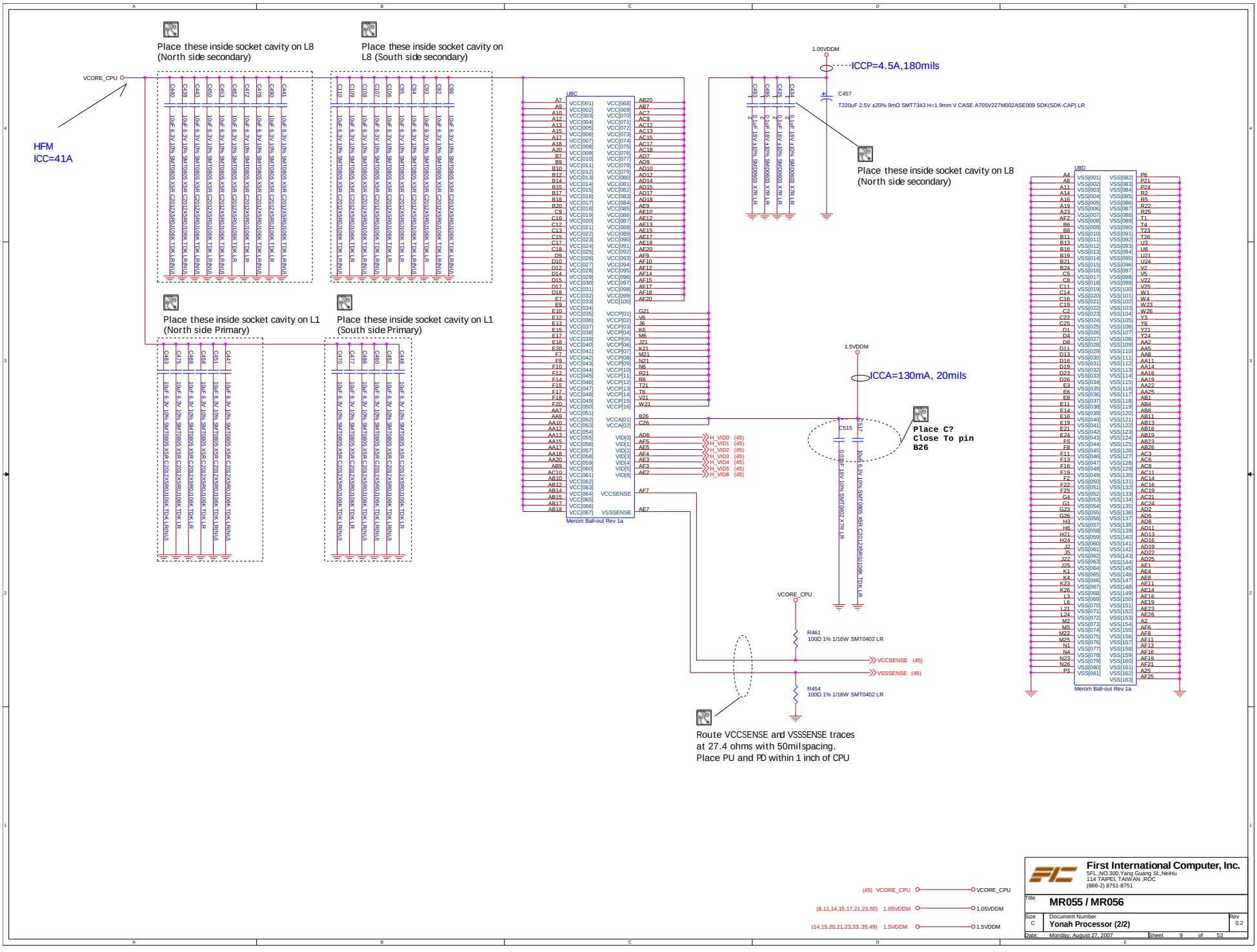

hexainf@hotmail.com

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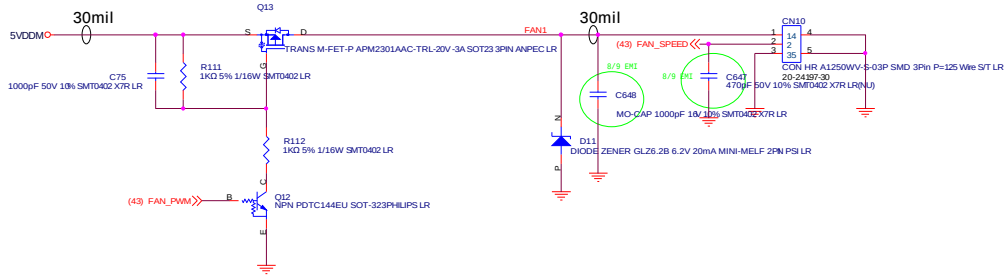
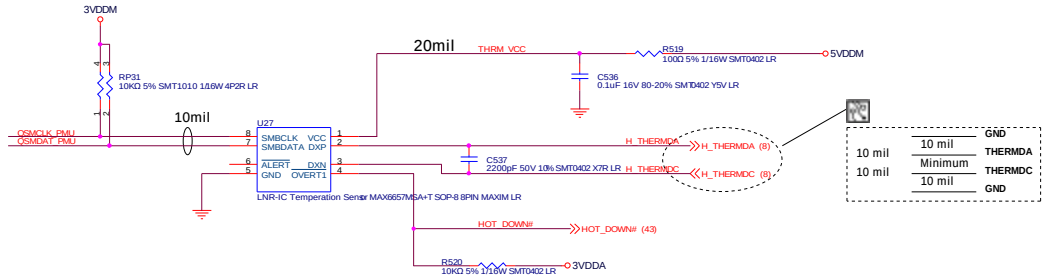
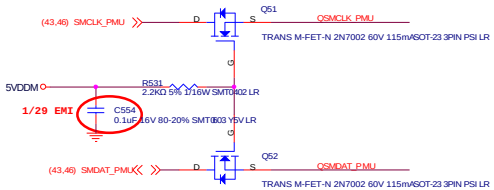


THERMAL SENSOR





(20..24,26,30,31,33..35,40,43,46,48,50) 3VDDA — 3VDDA
(12,15,17..20,22..27,29..31,33..35,37,43,45,48,51) 3VDDM — 3VDDM
(23,25,27,29,30,36,38,39,46) 5VDDM — 5VDDM

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Size	Document Number	Rev
C	CPU Thermal	0.2

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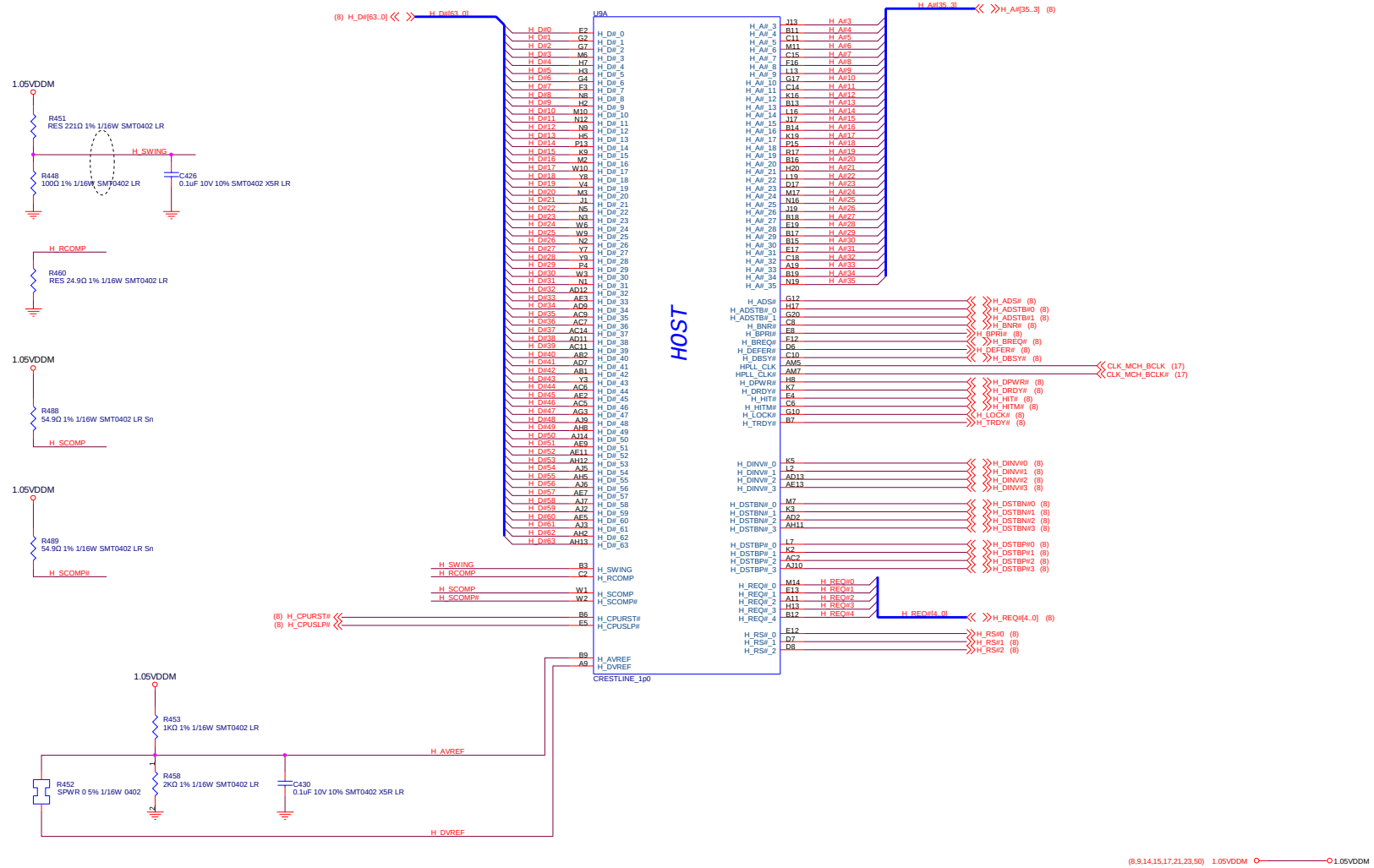
NB GL960：05-23843-01
NB GM965：05-23798-01 (REV. C0)



Title	First International Computer, Inc. 5FL.,NO.300,Yang Guang St.,NeiHu 114 TAIPEI, TAIWAN ,ROC (886-2)8751-8751 Confidential		
	MR055 / MR056		
Size C	Document Number Crestline Host (1/6)		Rev 0.2
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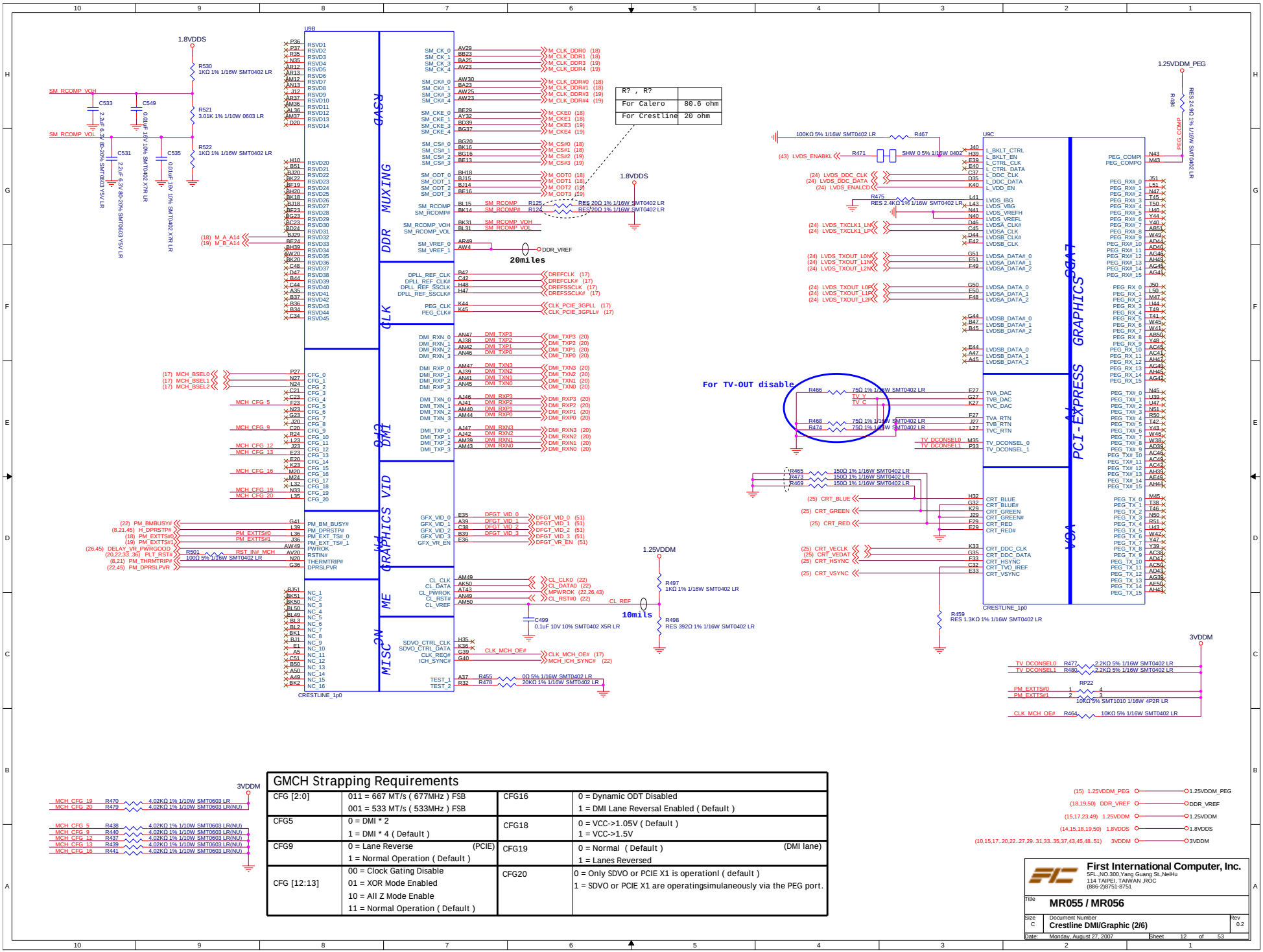
U9B
U9C
1.8VDDS
1.25VDDM_PEG
3VDDM
DDR_VREF
SM_RCOMP_VOH
SM_RCOMP_VOL
SM_RCOMP
SM_RCOMP#
R530 1KΩ 1% 1/16W SMT0402 LR
R521 3.01K 1% 1/10W 0603 LR
R522 1KΩ 1% 1/16W SMT0402 LR
R? , R?
For Calero 80.6 ohm
For Crestline 20 ohm
20miles
10mils
For TV-OUT disable
DDR MUXING
CLK
DMI
GRAPHICS VID
MISC
PCI-EXPRESS GRAPHICS
VGA
CRESTLINE_1p0
GMCH Strapping Requirements
CFG [2:0] 011 = 667 MT/s (677MHz) FSB
001 = 533 MT/s (533MHz) FSB
CFG16 0 = Dynamic ODT Disabled
1 = DMI Lane Reversal Enabled (Default)
CFG5 0 = DMI * 2
1 = DMI * 4 (Default)
CFG18 0 = VCC->1.05V (Default)
1 = VCC->1.5V
CFG9 0 = Lane Reverse (PCIE)
1 = Normal Operation (Default)
CFG19 0 = Normal (Default) (DMI lane)
1 = Lanes Reversed
CFG [12:13] 00 = Clock Gating Disable
01 = XOR Mode Enable
10 = All Z Mode Enable
11 = Normal Operation (Default)
CFG20 0 = Only SDVO or PCIE X1 is operationl (default)
1 = SDVO or PCIE X1 are operatingsimulaneously via the PEG port.
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Title MR055 / MR056
Size C
Document Number Crestline DMI/Graphic (2/6)
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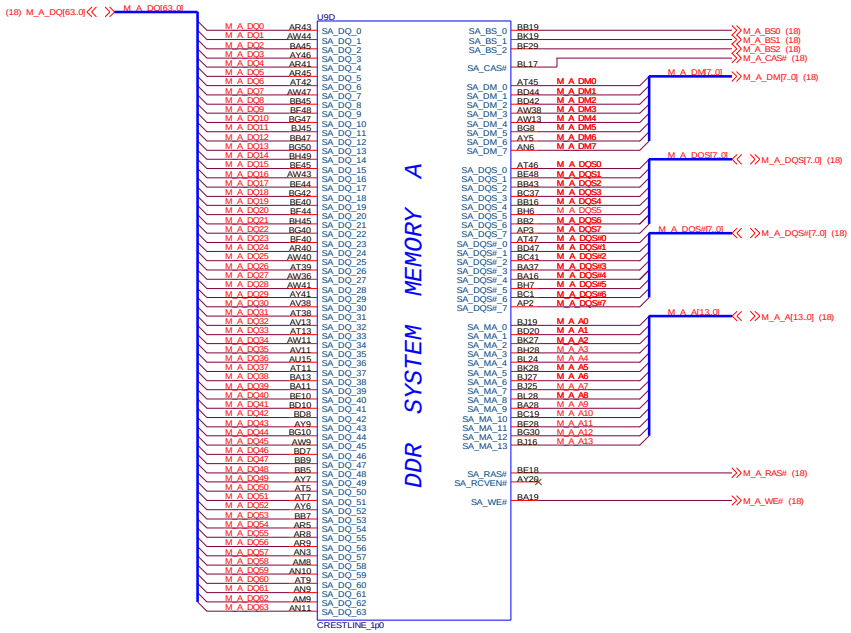
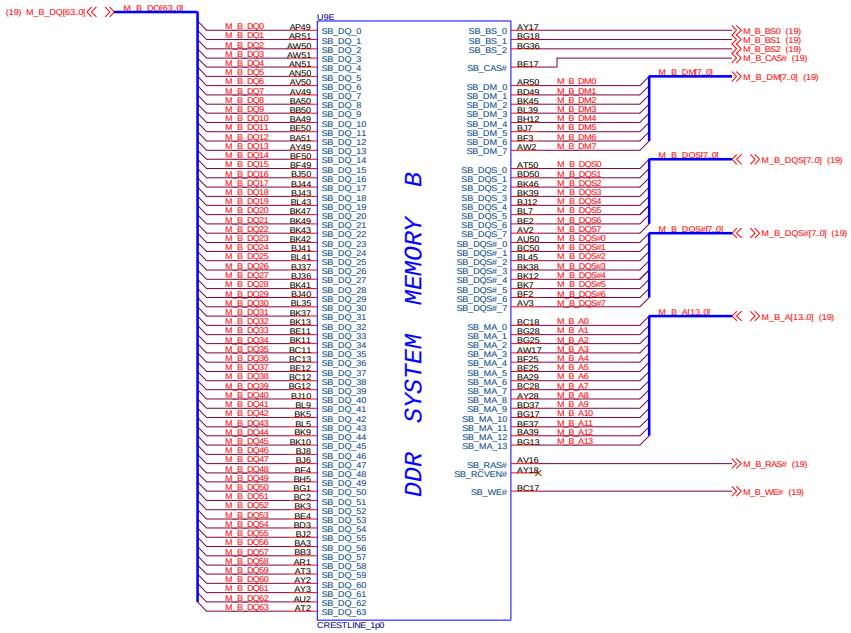
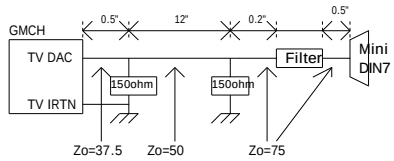




TV DAC Routing Guideline

1. The minimum spacing between each RGB is 40-mils while 50-mils is preferred
2. RGB signals should be routed on the same layer, have a similar number of bends, same number of vias
3. All routing should be done with ground referencing as well
4. TV DAC route lengths should be lenght match to within 200 mils



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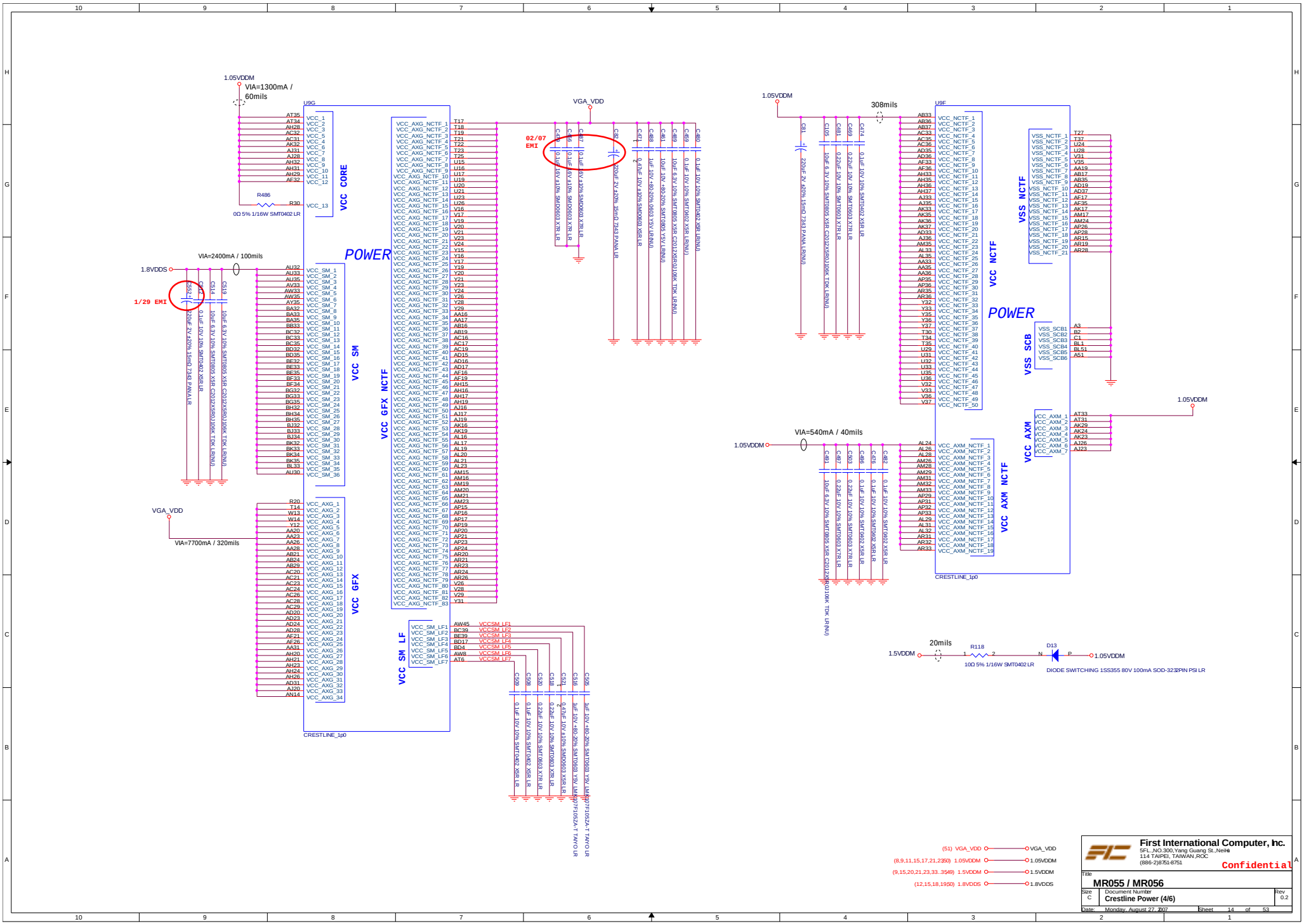
1.05VDDM
VIA=1300mA / 60mils
U9G
VCC CORE
R486
0Ω 5% 1/16W SMT0402 LR
POWER
VCC SM
VCC GFX NCTF
VCC GFX
VCC SM LF
VIA=2400mA / 100mils
1.8VDDS
1/29 EMI
VGA_VDD
VIA=7700mA / 320mils
CRESTLINE_1p0
02/07 EMI
VIA=540mA / 40mils
308mils
U9F
VCC NCTF
VSS NCTF
VSS SCB
VCC AXM
VCC AXM NCTF
20mils
R118
10Ω 5% 1/16W SMT0402 LR
D13
DIODE SWITCHING 1SS355 80V 100mA SOD-323PIN PSI LR
1.5VDDM
(51) VGA_VDD
(8,9,11,15,17,21,2350) 1.05VDDM
(9,15,20,21,23,33..3549) 1.5VDDM
(12,15,18,1950) 1.8VDDS
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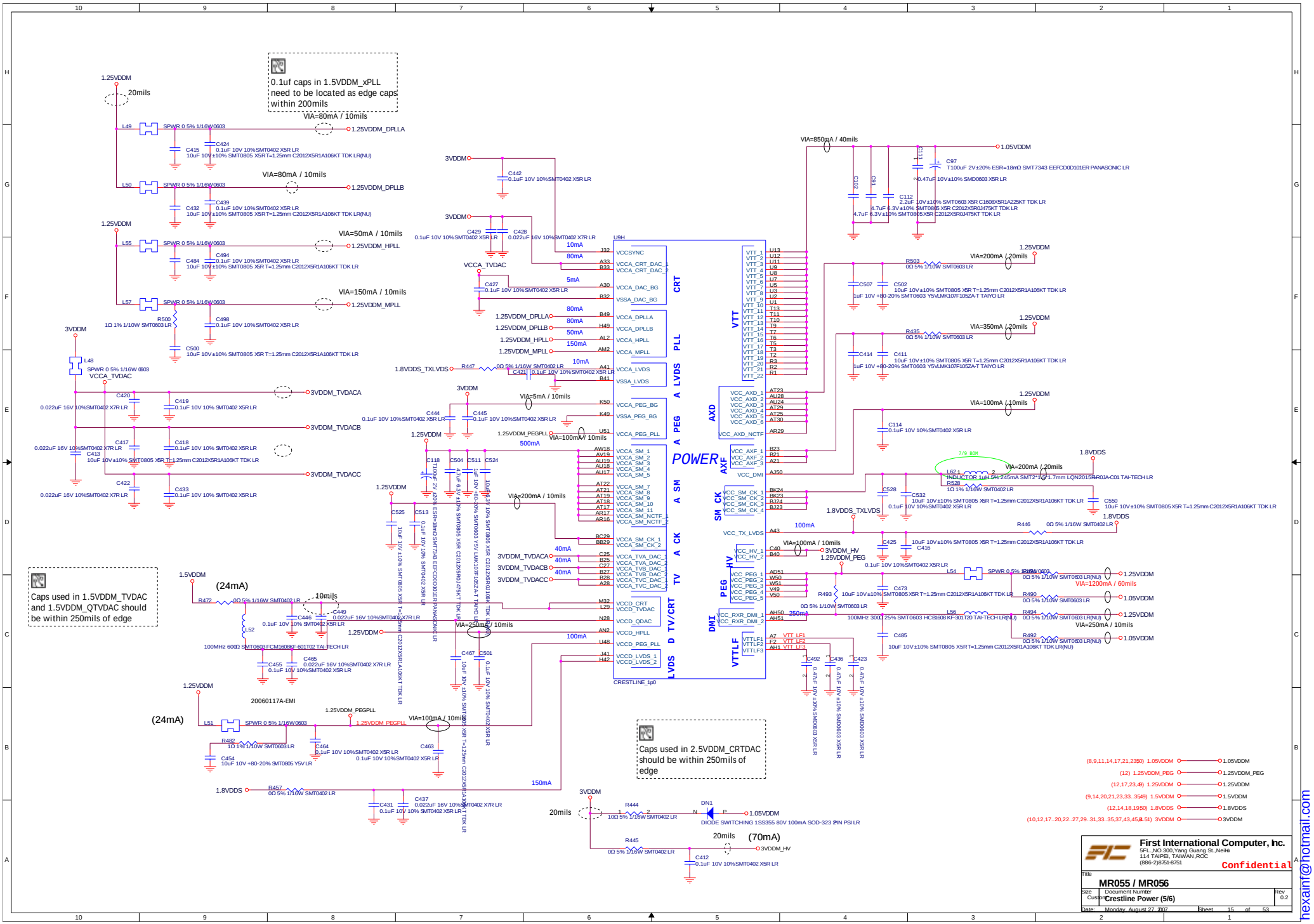
0.1uf caps in 1.5VDDM_xPLL need to be located as edge caps within 200mils
Caps used in 1.5VDDM_TVDAC and 1.5VDDM_QTVDAC should be within 250mils of edge
Caps used in 2.5VDDM_CRTDAC should be within 250mils of edge
POWER
CRESTLINE_1p0
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hexainf@hotmail.com

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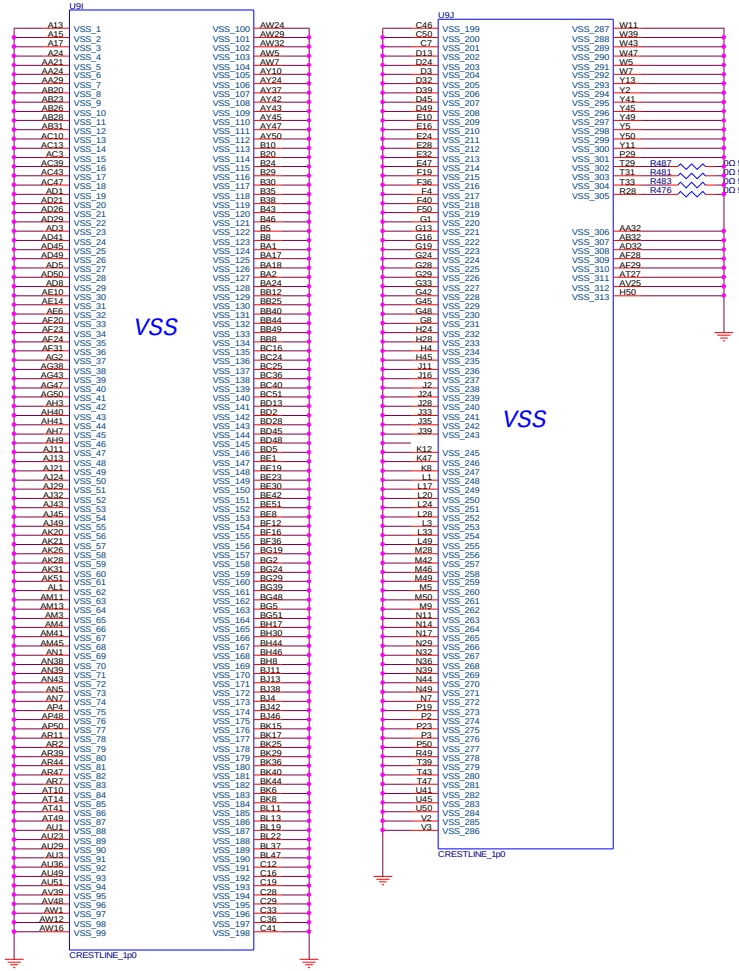
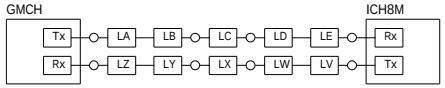


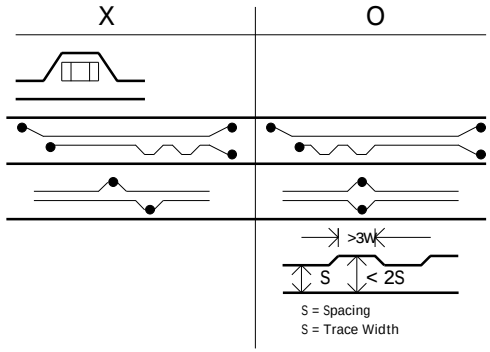
DMI Routing Guideline



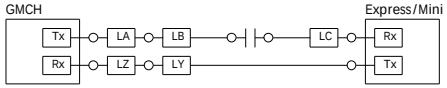
Breakout/in LA/LZ	Main Route LB/LY	Main Route LD/LW	Breakout/in LE/LV
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Didderential Pair-Pitch	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 22 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane spli ts No routing over voids	
Trace Length-LA (GMCH Breakout)	Max = 400 mils	
Trace Length-LB (GMCH Breakout to Via2)	Max = 3600 mils	
Trace Length-LC (Via2 to Via3)	Max = 5900 mils	
Trace Length-LD (Via3 to ICH7m Breakout)	Max = 3600 mils	
Trace Length-LE (ICH7m Breakout)	Max = 400 mils	
Trace Length-L1 (LA+LB+L C+LD+LE)	Max = 8000 mils	
Trace Length-LV (ICH7m Breakout)	Max = 400 mils	
Trace Length-LW (ICH7m Breakout to Via2)	Max = 3600 mils	
Trace Length-LX (Via2 to Via3)	Max = 5900 mils	
Trace Length-LY (Via3 to GMCH Breakout)	Max = 3600 mils	
Trace Length-LZ (GMCH Breakout)	Max = 400 mils	
Trace Length-L2 (LV+LW+LX+LY+LZ)	Max = 8000 mils	

*** When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane
*** Match the trace lengths of the complementary signals within each differenti al pair to +/- 5 mils



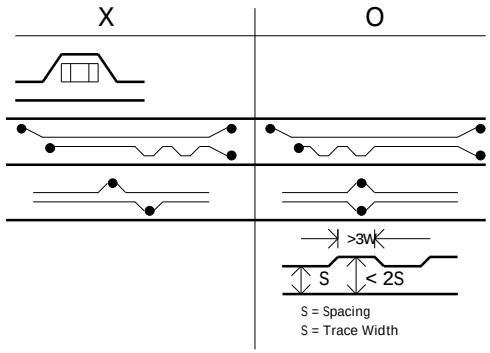
PCIE Routing Guideline



Breakout/in LA/LZ	Main Route LB/LC/LY	Main Route LD/LW	Breakout/in LE/LV
Stripline	Microstrip	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Differential Trace Space	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 20 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane spli ts No routing over voids	
Trace Length-LA (ICH7m Breakout)	Max = 400 mils	
Trace Length-LB (ICH7m Breakout to AC cap)	Max = 10750 mils	
Trace Length-LC (AC cap to PCIe CN)	Max = 10750 mils	
Trace Length-L1 (LA+LB+LC)	Max = 12000 mils	
Trace Length-LY (PCIe CN to ICH7m Breakout)	Max = 11950 mils	
Trace Length-LZ (ICH7m Breakout)	Max = 400 mils	
Trace Length-L2 (LY+LZ)	Max = 12000 mils	

*** When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane
*** Match the trace lengths of the complementary signals within each differenti al pair to +/- 5 mils



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Title: MR055 / MR056

Size: C | Document Number: Crestline Ground (6/6) | Rev: 0.2

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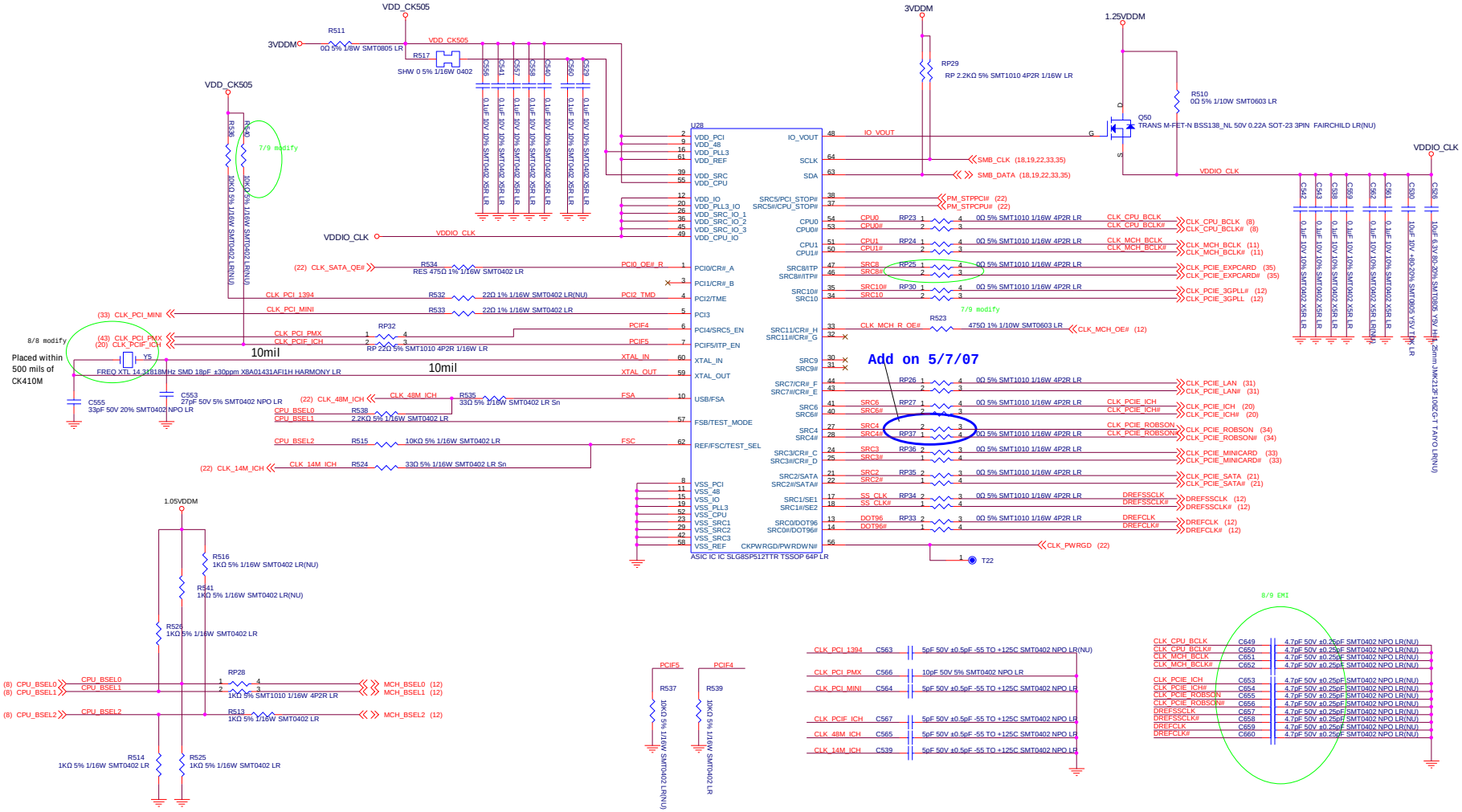
檔



FSC	FSB	FSA	Host Clock
CPU_BSEL2	CPU_BSEL1	CPU_BSEL0	Frequency MHz
0	1	1	166
0	1	0	200

SS3	SS2	SS1	SS0	Spread Mode	Spread Amount %
0	0	0	0	DOWN	0.8
0	0	0	1	DOWN	1.0
0	0	1	0	DOWN	1.25
0	0	1	1	DOWN	1.5
0	1	0	0	DOWN	1.75
0	1	0	1	DOWN	2.0
0	1	1	0	DOWN	2.5
0	1	1	1	DOWN	3.0

SS3	SS2	SS1	SS0	Spread Mode	Spread Amount %
1	0	0	0	Center	+/- 0.3
1	0	0	1	Center	+/- 0.4
1	0	1	0	Center	+/- 0.5
1	0	1	1	Center	+/- 0.6
1	1	0	0	Center	+/- 0.8
1	1	0	1	Center	+/- 1.0
1	1	1	0	Center	+/- 1.25
1	1	1	1	Center	+/- 1.5

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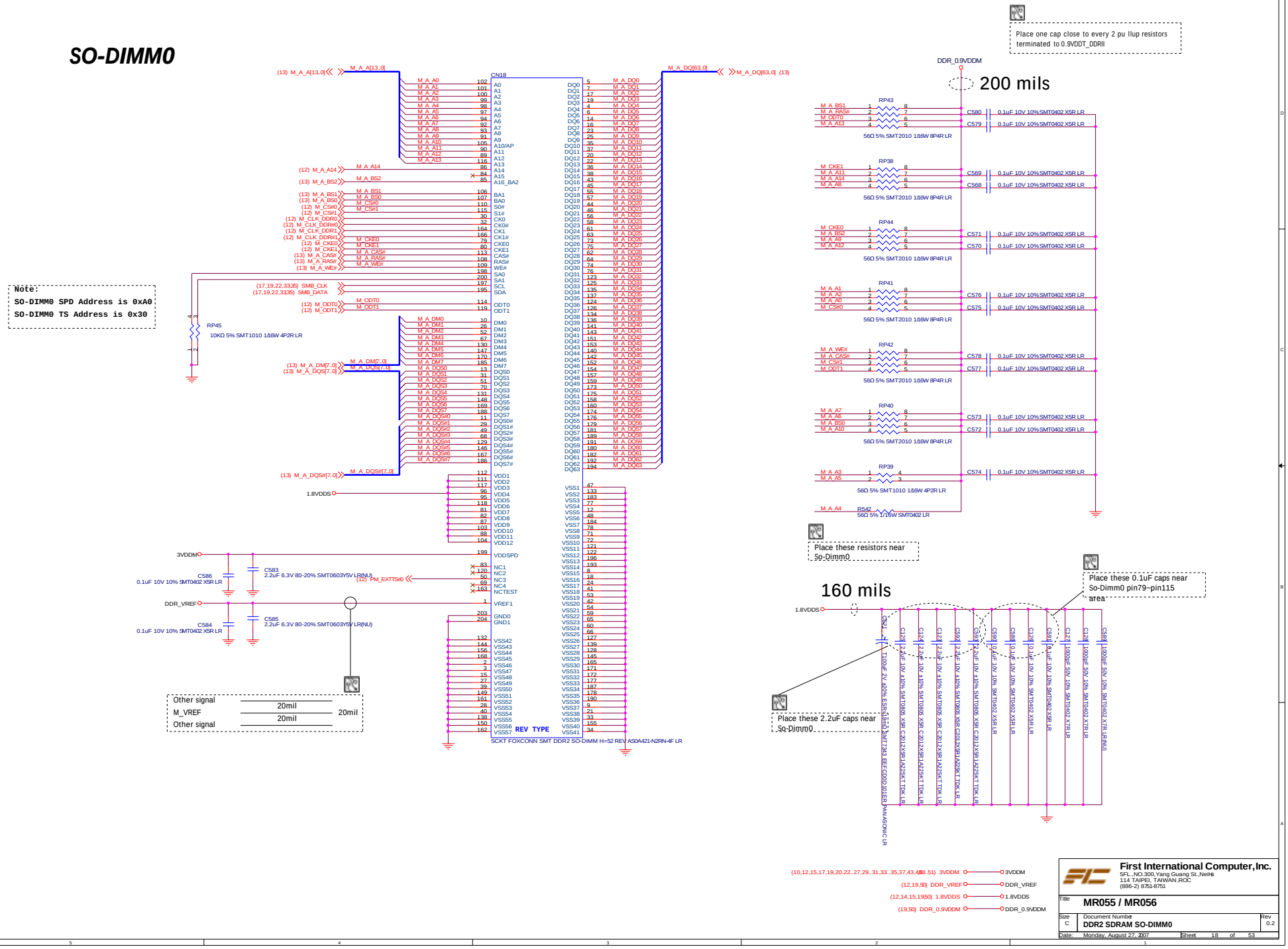
檔

SO-DIMM0



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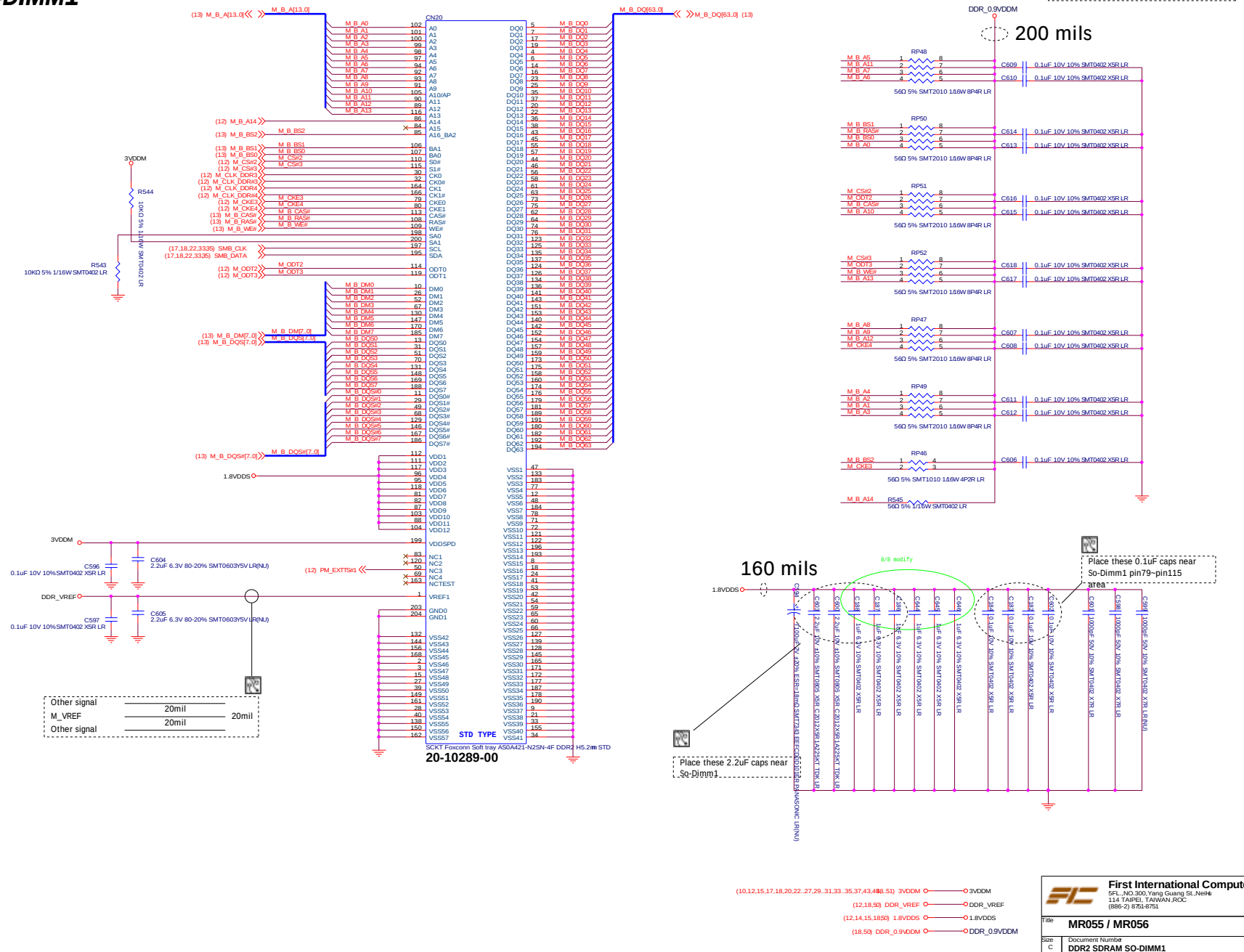
SO-DIMM1



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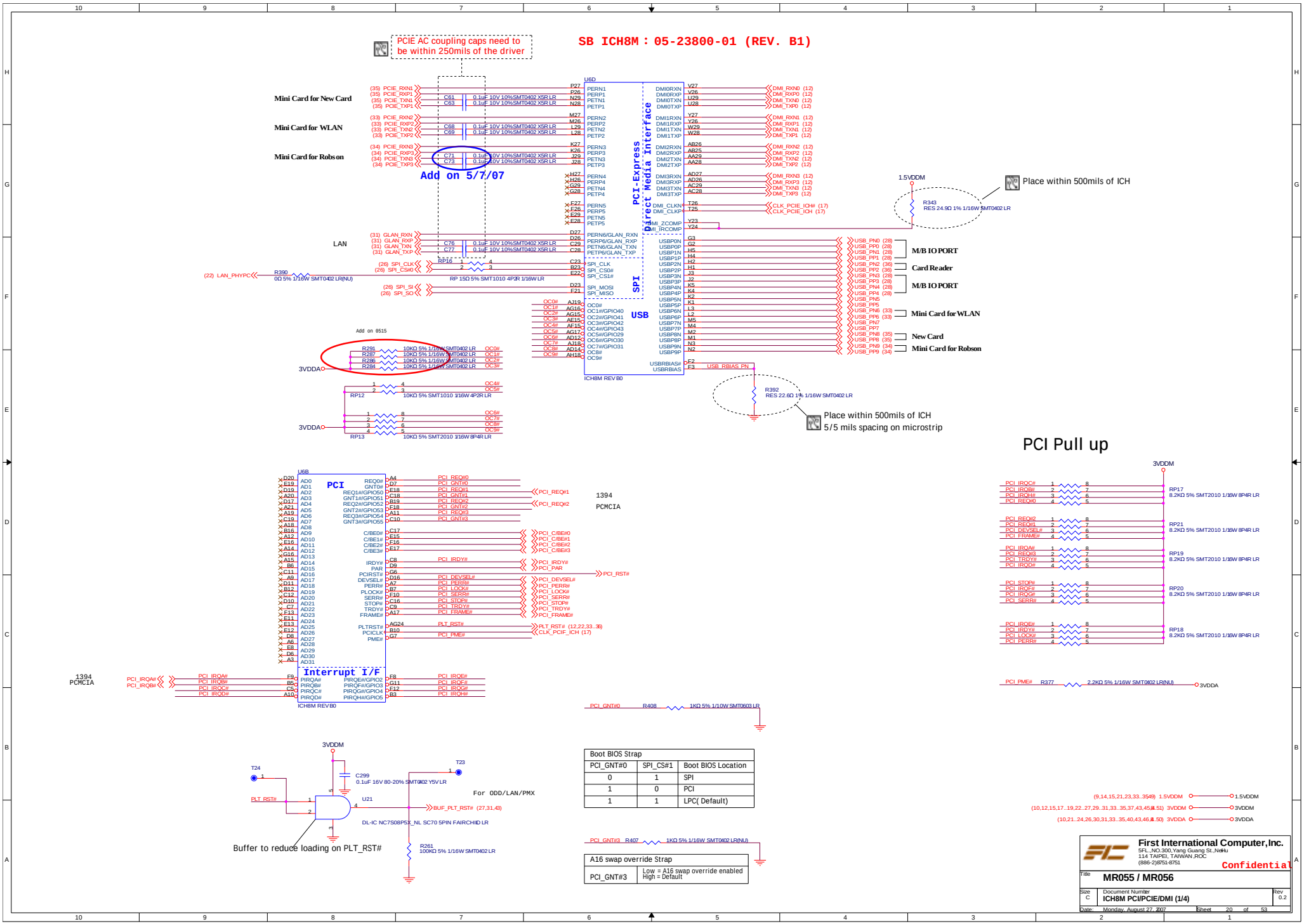
SB ICH8M：05-23800-01 (REV. B1)
PCIE AC coupling caps need to be within 250mils of the driver
Mini Card for New Card
Mini Card for WLAN
Mini Card for Robson
Add on 5/7/07
LAN
PCI-Express Direct Media Interface
SPI
USB
ICH8M REV B0
M/B IO PORT
Card Reader
M/B IO PORT
Mini Card for WLAN
New Card
Mini Card for Robson
1.5VDDM
Place within 500mils of ICH
Place within 500mils of ICH
5/5 mils spacing on microstrip
Add on 0515
3VDDA
PCI Pull up
3VDDM
PCI
Interrupt I/F
1394
PCMCIA
For ODD/LAN/PMX
Buffer to reduce loading on PLT_RST#
Boot BIOS Strap
PCI_GNT#0
SPI_CS#1
Boot BIOS Location
0
1
SPI
1
0
PCI
1
1
LPC(Default)
A16 swap override Strap
PCI_GNT#3
Low = A16 swap override enabled
High = Default
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MR055 / MR056
ICH8M PCI/PCIE/DMI (1/4)
Monday, August 27, 2007

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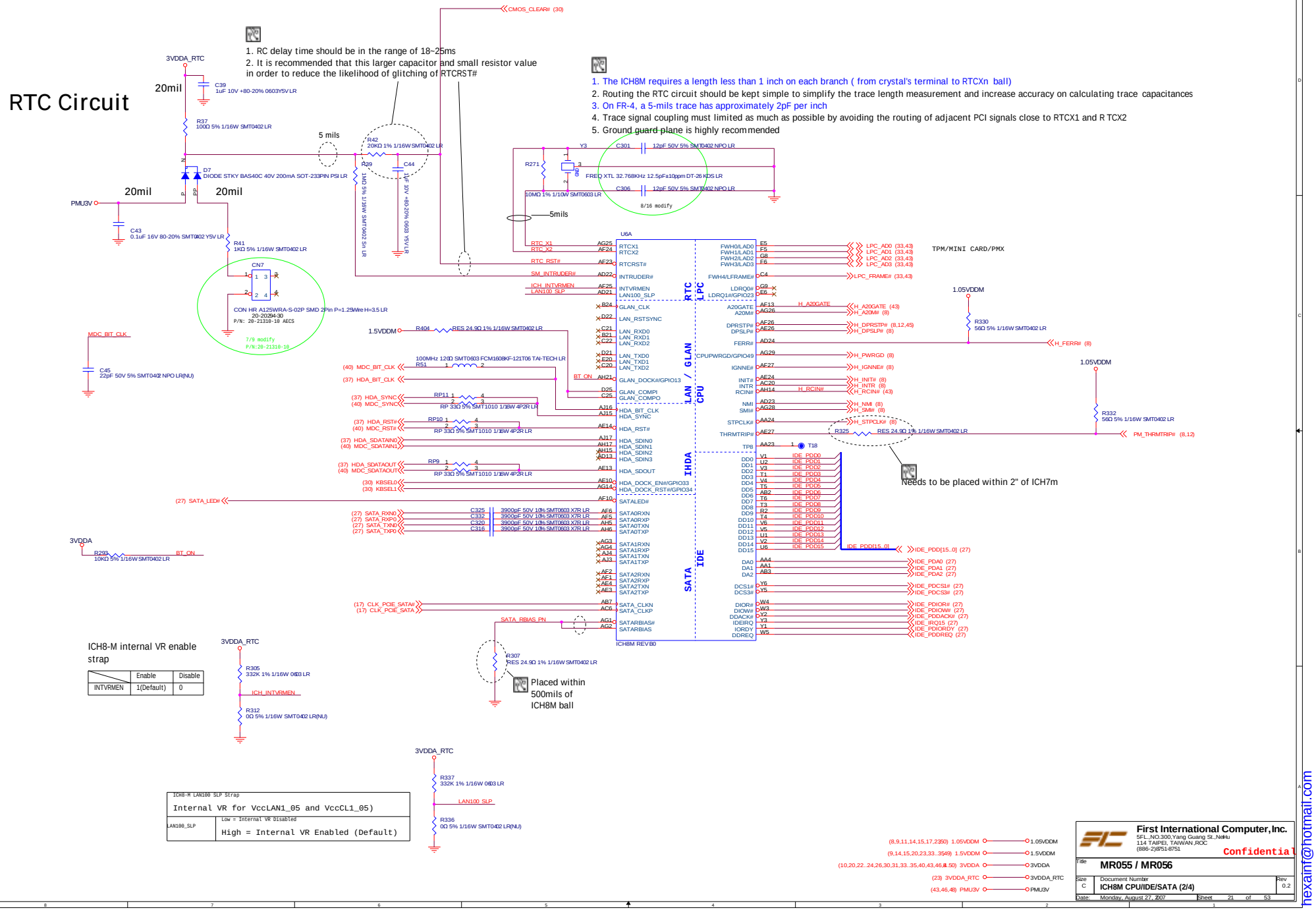
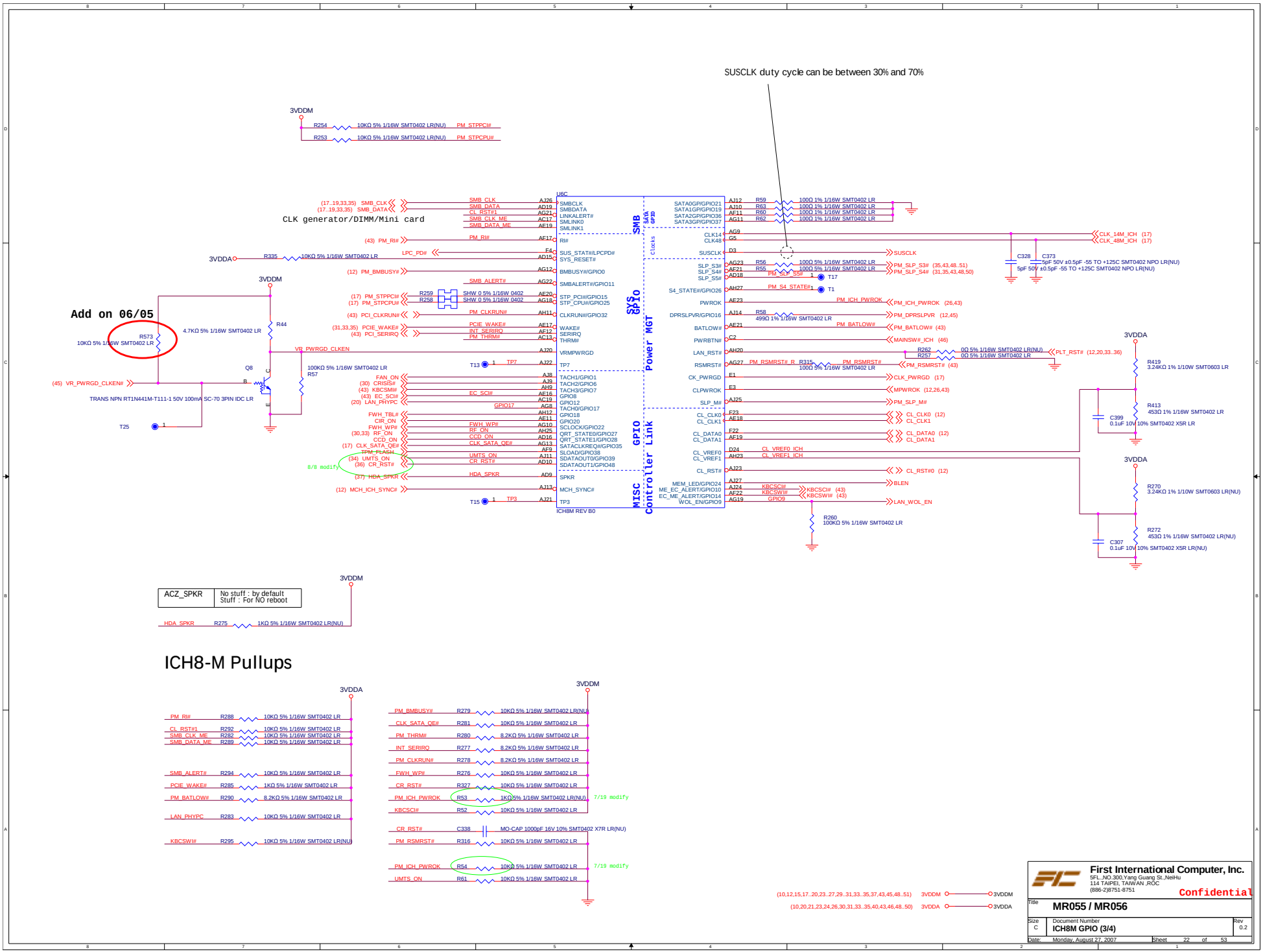
RTC Circuit



	Enable	Disable
INTVRMEN	1(Default)	0

ICH8-M LAN100_SLP Strap	
Internal VR for VccLAN1_05 and VccCL1_05)	
LAN100_SLP	Low = Internal VR Disabled
	High = Internal VR Enabled (Default)

檔


SUSCLK duty cycle can be between 30% and 70%
3VDDM
R254 10KΩ 5% 1/16W SMT0402 LR(NU) PM_STPPCI#
R253 10KΩ 5% 1/16W SMT0402 LR(NU) PM_STPCPU#
CLK generator/DIMM/Mini card
3VDDA
R335 10KΩ 5% 1/16W SMT0402 LR
Add on 06/05
R573 10KΩ 5% 1/16W SMT0402 LR
4.7KΩ 5% 1/16W SMT0402 LR
R44
VR_PWRGD_CLKEN
Q8
TRANS NPN RT1N441M-T111-1 50V 100mA SC-70 3PIN IDC LR
100KΩ 5% 1/16W SMT0402 LR
R57
T25
T13
TP7
T15
TP3
U6C
ICH8M REV B0
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD#
SYS_RESET#
BMBUSY#/GPIO0
SMBALERT#/GPIO11
STP_PCI#/GPIO15
STP_CPU#/GPIO25
CLKRUN#/GPIO32
WAKE#
SERIRQ
THRM#
VRMPWRGD
TP7
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
GPIO12
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
QRT_STATE0/GPIO27
QRT_STATE1/GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
SPKR
MCH_SYNC#
TP3
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA2GP/GPIO36
SATA3GP/GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST#
MEM_LED/GPIO24
ME_EC_ALERT/GPIO10
EC_ME_ALERT/GPIO14
WOL_EN/GPIO9
CLK_14M_ICH (17)
CLK_48M_ICH (17)
C328
C373
5pF 50V ±0.5pF -55 TO +125C SMT0402 NPO LR(NU)
PM_SLP_S3# (35,43,48..51)
PM_SLP_S4# (31,35,43,48,50)
PM_ICH_PWROK (26,43)
PM_DPRSLPVR (12,45)
PM_BATLOW# (43)
MAINSW#_ICH (46)
PLT_RST# (12,20,33..36)
PM_RSMRST# (43)
CLK_PWRGD (17)
MPWROK (12,26,43)
PM_SLP_M#
CL_CLK0 (12)
CL_CLK1
CL_DATA0 (12)
CL_DATA1
CL_VREF0_ICH
CL_VREF1_ICH
CL_RST#0 (12)
BLEN
KBCSC# (43)
KBCSW# (43)
LAN_WOL_EN
R260 100KΩ 5% 1/16W SMT0402 LR
3VDDA
R419 3.24KΩ 1% 1/10W SMT0603 LR
R413 453Ω 1% 1/16W SMT0402 LR
C399 0.1uF 10V 10% SMT0402 X5R LR
R270 3.24KΩ 1% 1/10W SMT0603 LR(NU)
R272 453Ω 1% 1/16W SMT0402 LR(NU)
C307 0.1uF 10V 10% SMT0402 X5R LR(NU)
ACZ_SPKR
No stuff : by default
Stuff : For NO reboot
HDA_SPKR R275 1KΩ 5% 1/16W SMT0402 LR(NU)
ICH8-M Pullups
PM_RI# R288 10KΩ 5% 1/16W SMT0402 LR
CL_RST#1 R292 10KΩ 5% 1/16W SMT0402 LR
SMB_CLK_ME R282 10KΩ 5% 1/16W SMT0402 LR
SMB_DATA_ME R289 10KΩ 5% 1/16W SMT0402 LR
SMB_ALERT# R294 10KΩ 5% 1/16W SMT0402 LR
PCIE_WAKE# R285 1KΩ 5% 1/16W SMT0402 LR
PM_BATLOW# R290 8.2KΩ 5% 1/16W SMT0402 LR
LAN_PHYPC R283 10KΩ 5% 1/16W SMT0402 LR
KBCSW# R295 10KΩ 5% 1/16W SMT0402 LR(NU)
PM_BMBUSY# R279 10KΩ 5% 1/16W SMT0402 LR(NU)
CLK_SATA_QE# R281 10KΩ 5% 1/16W SMT0402 LR
PM_THRM# R280 8.2KΩ 5% 1/16W SMT0402 LR
INT_SERIRQ R277 8.2KΩ 5% 1/16W SMT0402 LR
PM_CLKRUN# R278 8.2KΩ 5% 1/16W SMT0402 LR
FWH_WP# R276 10KΩ 5% 1/16W SMT0402 LR
CR_RST# R327 10KΩ 5% 1/16W SMT0402 LR
PM_ICH_PWROK R53 1KΩ 5% 1/16W SMT0402 LR(NU) 7/19 modify
KBCSCI# R52 10KΩ 5% 1/16W SMT0402 LR
CR_RST# C338 MO-CAP 1000pF 16V 10% SMT0402 X7R LR(NU)
PM_RSMRST# R316 10KΩ 5% 1/16W SMT0402 LR
PM_ICH_PWROK R54 10KΩ 5% 1/16W SMT0402 LR 7/19 modify
UMTS_ON R61 10KΩ 5% 1/16W SMT0402 LR
(10,12,15,17..20,23..27,29..31,33..35,37,43,45,48..51) 3VDDM 3VDDM
(10,20,21,23,24,26,30,31,33..35,40,43,46,48..50) 3VDDA 3VDDA
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Size C
Document Number ICH8M GPIO (3/4)
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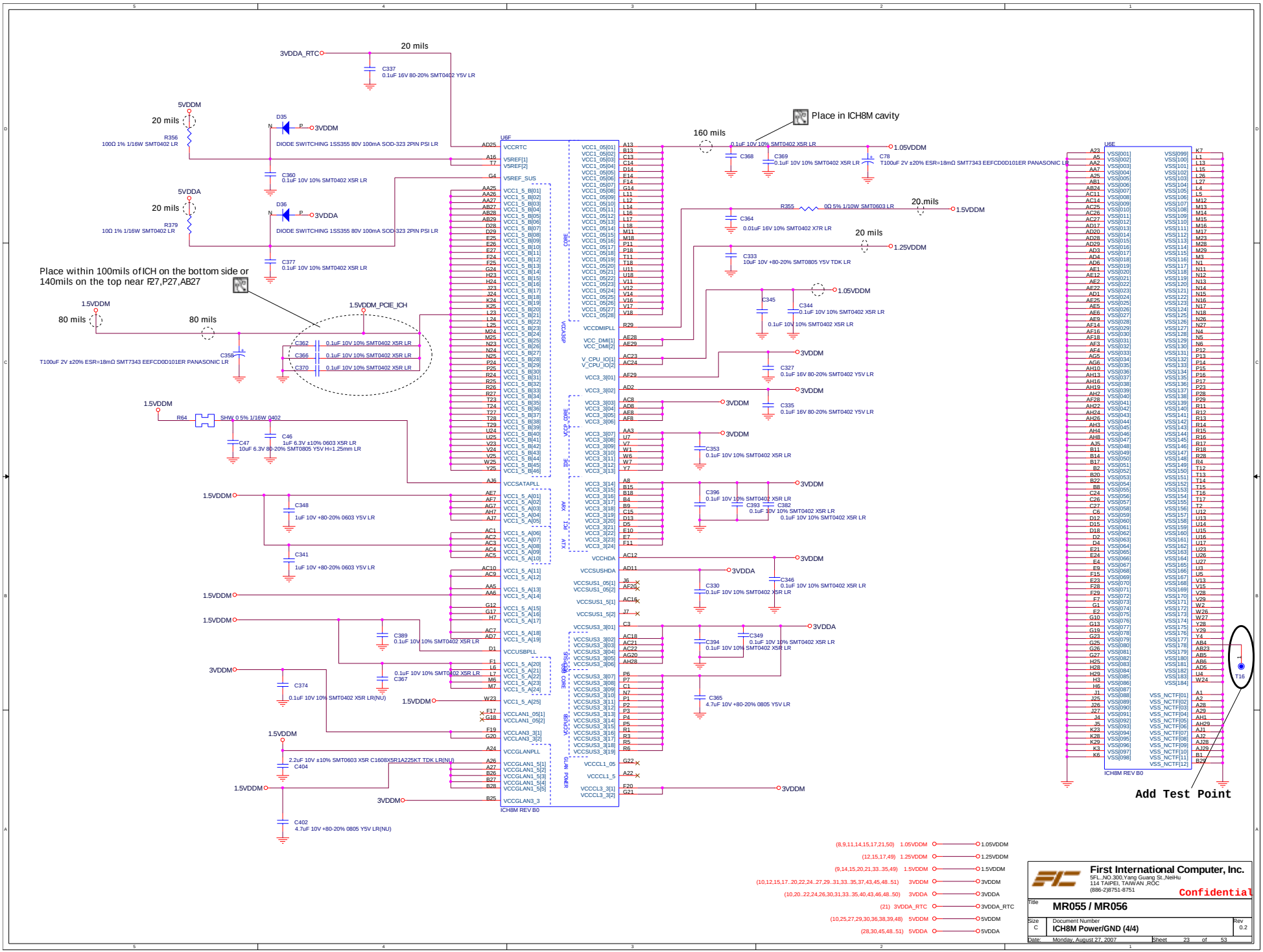

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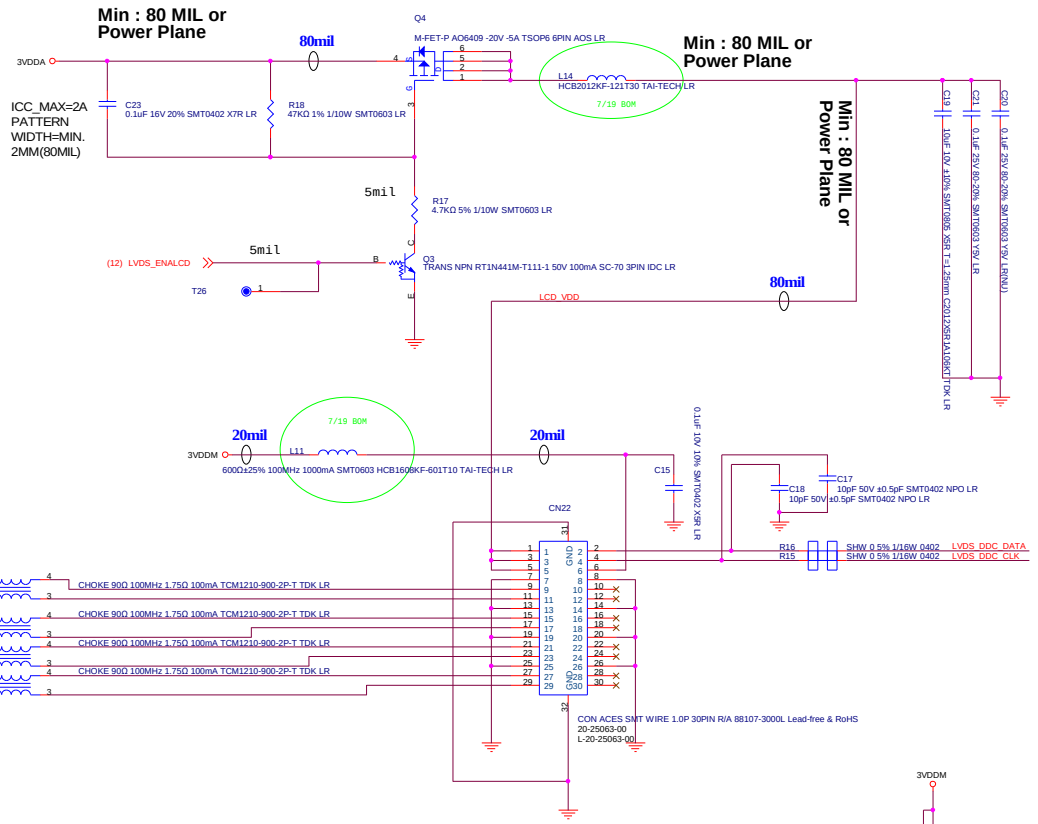
LVDS Interface



LVDS Signal Group Routing Guideline

GMCH — P1 — TL1 — LVDS CN

Topology	Differential Pair Point-to-Point
Reference Plane	Ground
Differential Mode Impedance	100 +/- 20%
Nominal Trace Width	4 mils
Nominal Pair Spacing (Edge to edge)	7 mils
Minimum Pair-to-Pair Spacing	20 mils
Minimum Serpentine Spacing	20 mils
Minimum Spacing to Other LVDS	20 mils
Minimum Isolation Spacing to non-LVDS	20 mils
Maximim Via Count	2 (per line)
Package Length Range - P1	750 mils +/- 250 mils
Total MB Length - TL1	Max = 10"
Length Matching with Pair	Matching to within +/- 20mils
Clock to Data Length Matching (Total Length)	Matching Data to Clock within +/- 20mils
Clock A to Clock B Length Matching	Match Clock A to B within +/- 20mils
Breakout Exceptions (Reduce geometries for GMCH break-out region)	4/4 mils spacing allowed and 10 mils Pair-to-Pair spacing allowed Max. breakout length is 500 mils

***Cable Length must be less than 16"

(10,20..23,26,30,31,33..35,40,43,46,48..50) 3VDDA — 3VDDA
(10,12,15,17..20,22,23,25..27,29..31,33..35,37,43,45,48..51) 3VDDM — 3VDDM
(45..51) DCIN — DCIN

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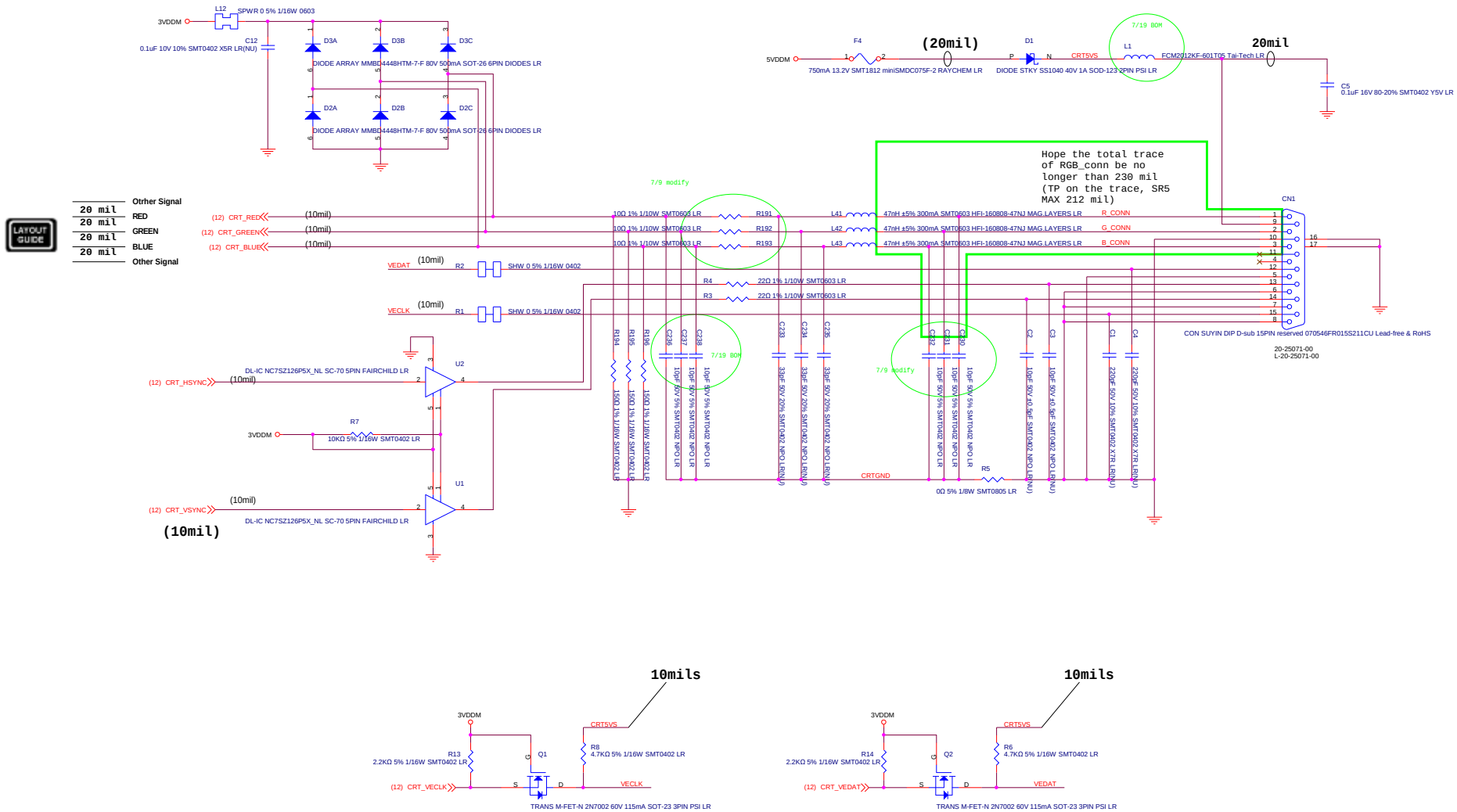

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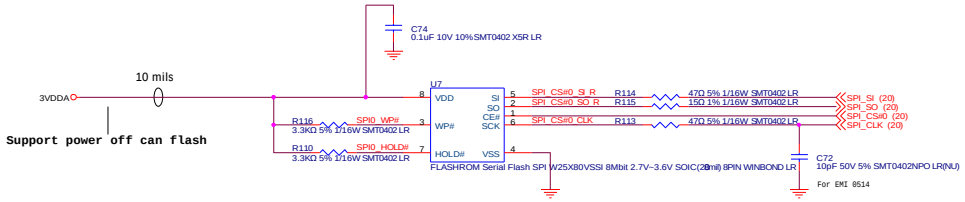
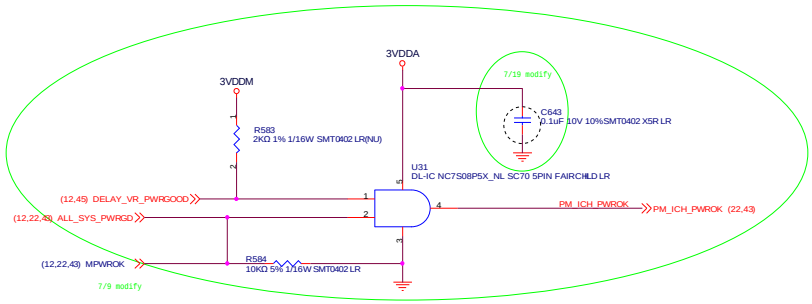
SPI Interface





(10,12,15,17..20,22..25,27,29..31,33..35,37,43,45,48,51) 3VDDM — 3VDDM

(10,20..24,30,31,33..35,40,43,46,48,50) 3VDDA — 3VDDA

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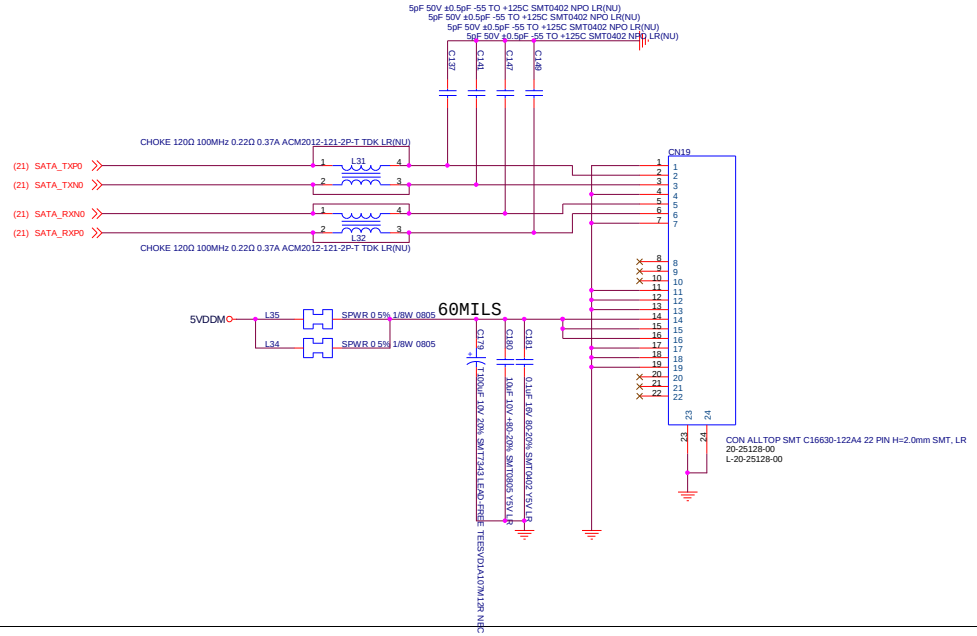
NOTE

SATA differential stripline 20:5:6:5:20
SATA differential mircostripline 20:6:6:6:20
請包GROUND

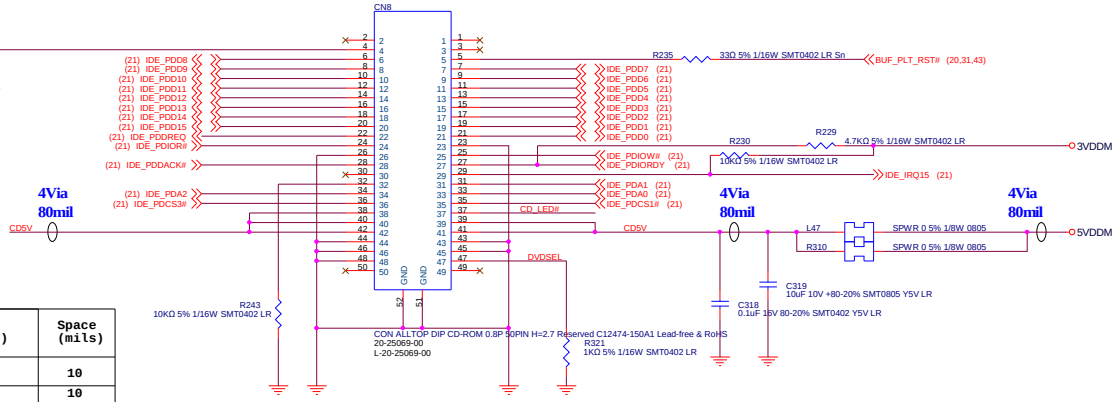
SATA Layout Note:

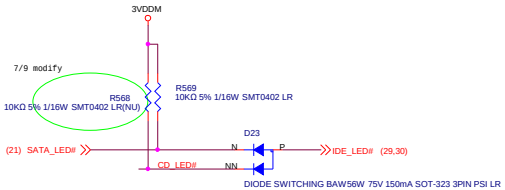
MS or SL:

* Zdif = 100 Ohm +/- 10%. TX & RX should refer GND.No via & stubs.The Best layer is Top.
* TX/RX trace length < 2 inchs.
* TX+/- need matching trace ±10 mils length.
* RX+/- need matching trace ±10 mils length.
* SATA Pair to Pair Trace matching trace ±10 mils length.



CD-ROM CNN





(10,12,15,17..20,22..26,29..31,33..35,37,43,45,48..51) 3VDDM → 3VDDM
(10,23,25,29,30,36,38,39,48) 5VDDM → 5VDDM

IDE Signals

Signals	MAX Length (inch)	Width (mils)	Space (mils)
IDE_PDD[15:0]	8	5	10
IDE_SDD[15:0]	8	5	10
IDE_PDA0-2	8	5	10
IDE_SDA0-2	8	5	10
IDE_PDCS 10-30#	8	5	10
IDE_PDDREQ	8	5	10
IDE_SDDREQ	8	5	10
IDE_PDIOW#	8	5	10
IDE_PATADET	8	5	10
IDE_SATADET	8	5	10
IDE_PDDACK#	8	5	10
IDE_SDDACK#	8	5	10

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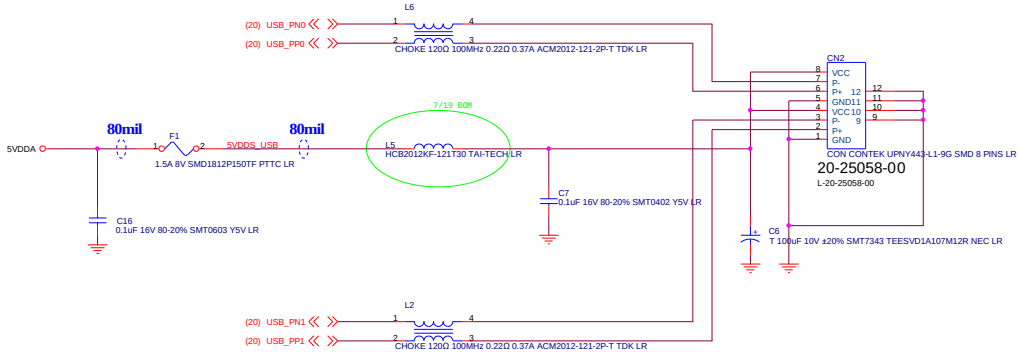
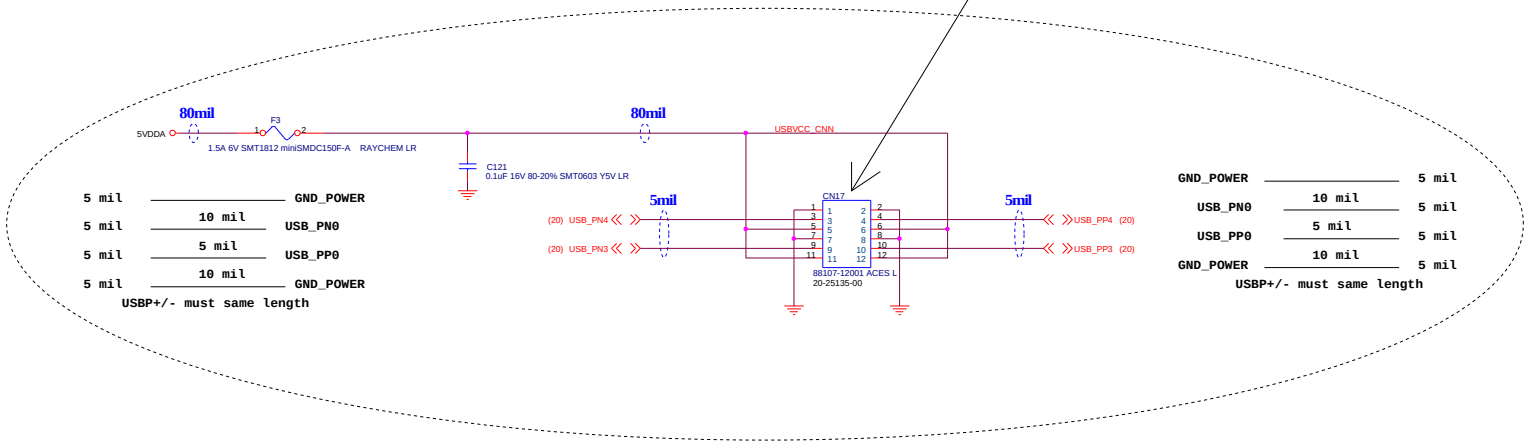
5 mil — GND_POWER
10 mil
5 mil — USB20_P+
5 mil
5 mil — USB20_P-
10 mil
5 mil — GND_POWER

USBP+/- must same length



Add on 5/4/07

X,Y follow PA354 CN12



5 mil — GND_POWER
10 mil
5 mil — USB_PN0
5 mil
5 mil — USB_PP0
10 mil
5 mil — GND_POWER

USBP+/- must same length

GND_POWER — 5 mil
10 mil
USB_PN0 — 5 mil
5 mil
USB_PP0 — 5 mil
10 mil
GND_POWER — 5 mil

USBP+/- must same length

(23,30,45,48..51) 5VDDA — 5VDDA

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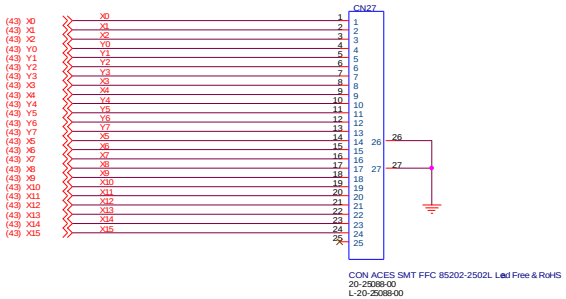
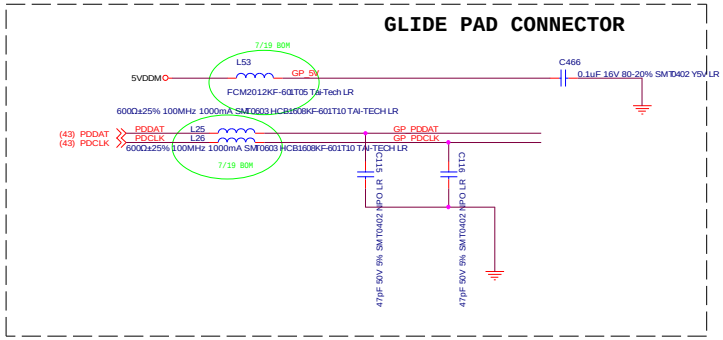
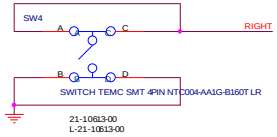
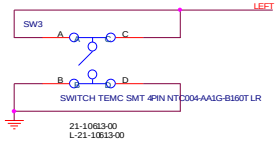
INT KB CNN

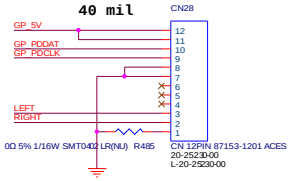


GLIDE PAD CONNECTOR

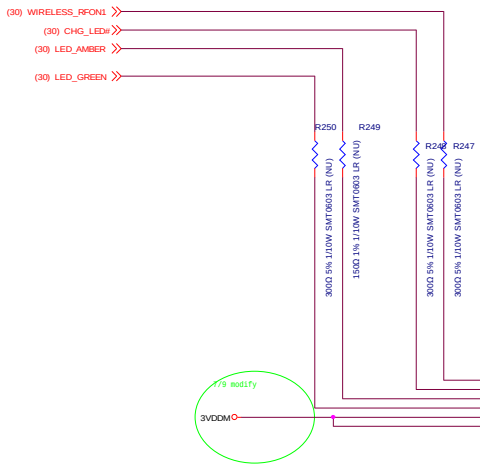


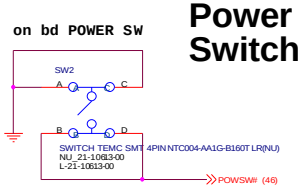


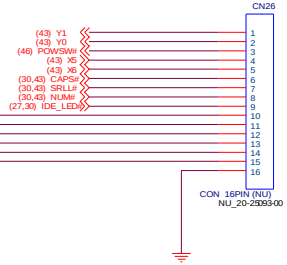




Power Switch

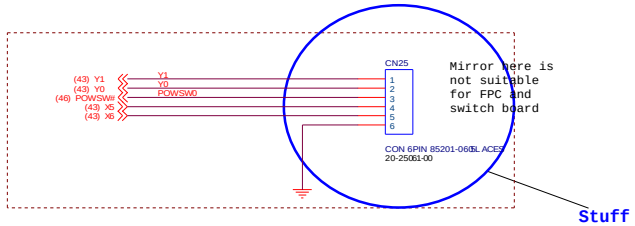






switch board con ID3

switch board con ID2



(10,12,15,17..20,22..27,30,31,33..35,37,43,48..51) 3VDDM → 3VDDM

(10,23,25,27,30,36,38,39,48) 5VDDM → 5VDDM

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Title	MR055 / MR056
Size C	Document Number: INT K/B / GP / SW CNN
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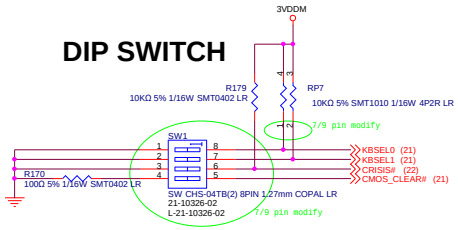
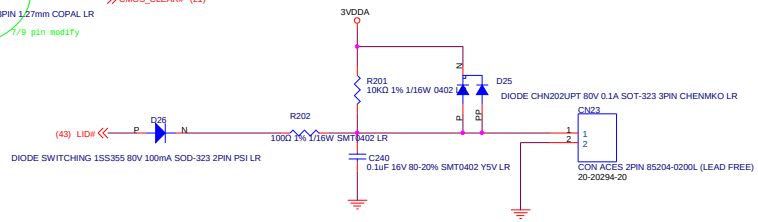
檔

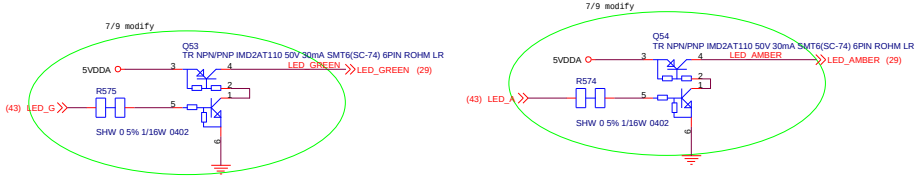
DIP SWITCH



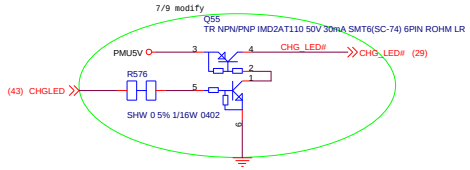
LID Switch



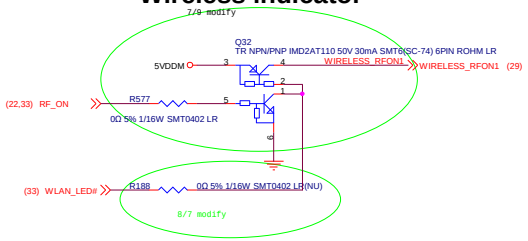
Power indicator



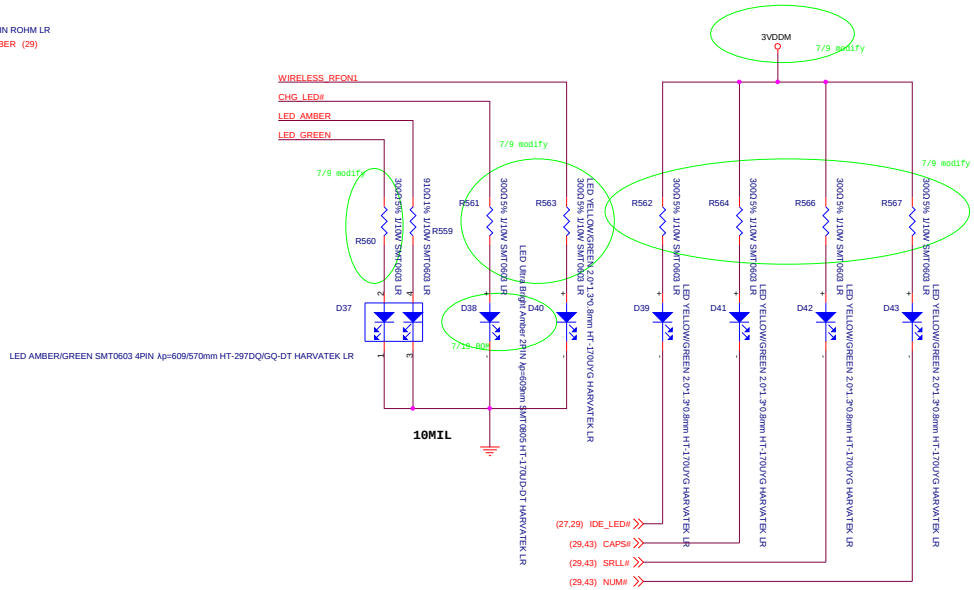
Charge indicator



Wireless indicator



LED indicator control logic



(43,48) PMU5V — PMU5V
(10,20..24,26,31,33..35,40,43,46,48..50) 3VDDA — 3VDDA
(23,28,45,48..51) 5VDDA — 5VDDA
(10,12,15,17..20,22..27,29,31,33..35,37,43,45,48..51) 3VDDM — 3VDDM
(10,23,25,27,29,36,38,39,48) 5VDDM — 5VDDM

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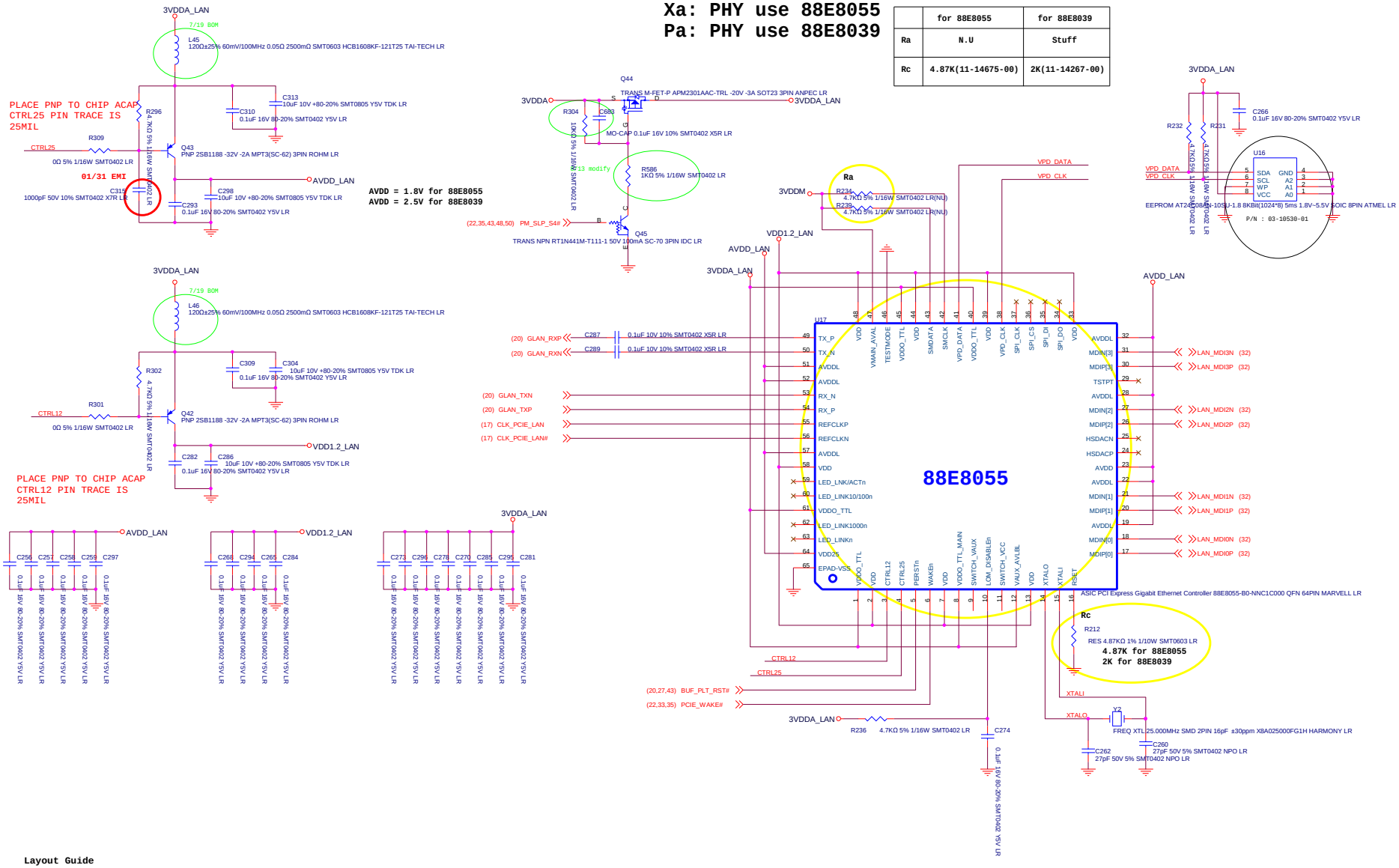
Xa: PHY use 88E8055
Pa: PHY use 88E8039

	for 88E8055	for 88E8039
Ra	N.U	Stuff
Rc	4.87K(11-14675-00)	2K(11-14267-00)



Layout Guide

1.The Lan Chip should be placed as close as possible to the transfer.
2. The resistor connected to RSET pin should be placed near to the Lan Chip,and away from signal traces(ex:MDI0+/-) and clock signals as far as possible.
3. The transfer should be placed as close as possible to the RJ45 connector.
4. The crystal should be placed far away from I/O ports and high frequency signal.
5. The termination resistors and capacitors should be placed closely to the Lan Chip.
6. The decoupling capacitors should be placed as close as possible to the power pins,such that the distance from IC power pin to the capacitor is within 200mils.
7. Traces routed from the Lan Chip to the transfer,and to the RJ45 connector should be as short as possible.
8. The 10-12cm maximum lenghth between Lan Chip and transfer is achievable only when there's no interferences around.
9. All 4 pairs of the differential resister(49.9k) must close to Lan Chip,and make them(4pairs) as same as distant.
10.PLACE GND PLANE AS LARGE AS POSSIBLE
11.If power pins are next to each other and there is not much room to accommodate multipe capacitors,then the power pins can share the same capacitors.
12.It's important to separate digital signals from analog signals.If it is unavoidable to cross digtal signals with analong power do it at 90 degree angle.
13. The digital power plane should be separated from analog areas.
14. All analog decoupling capacitors should be placed as close to the IC as possible and the traces should be short.
15.The Lan Chip pin 1 facing the transformer,then you can make the signal shorter.

(32) AVDD_LAN → AVDD_LAN
(10,12,15,17..20,22..27,29,30,33..35,37,43,45,48..51) 3VDDM → 3VDDM
(10,20..24,26,30,33..35,40,43,46,48..50) 3VDDA → 3VDDA

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Title	MR055 / MR056	
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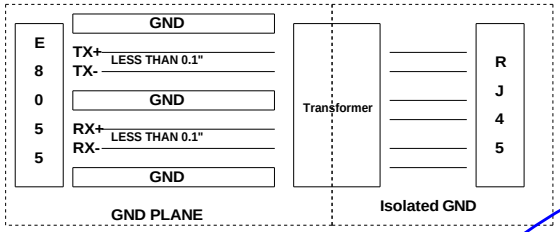
檔

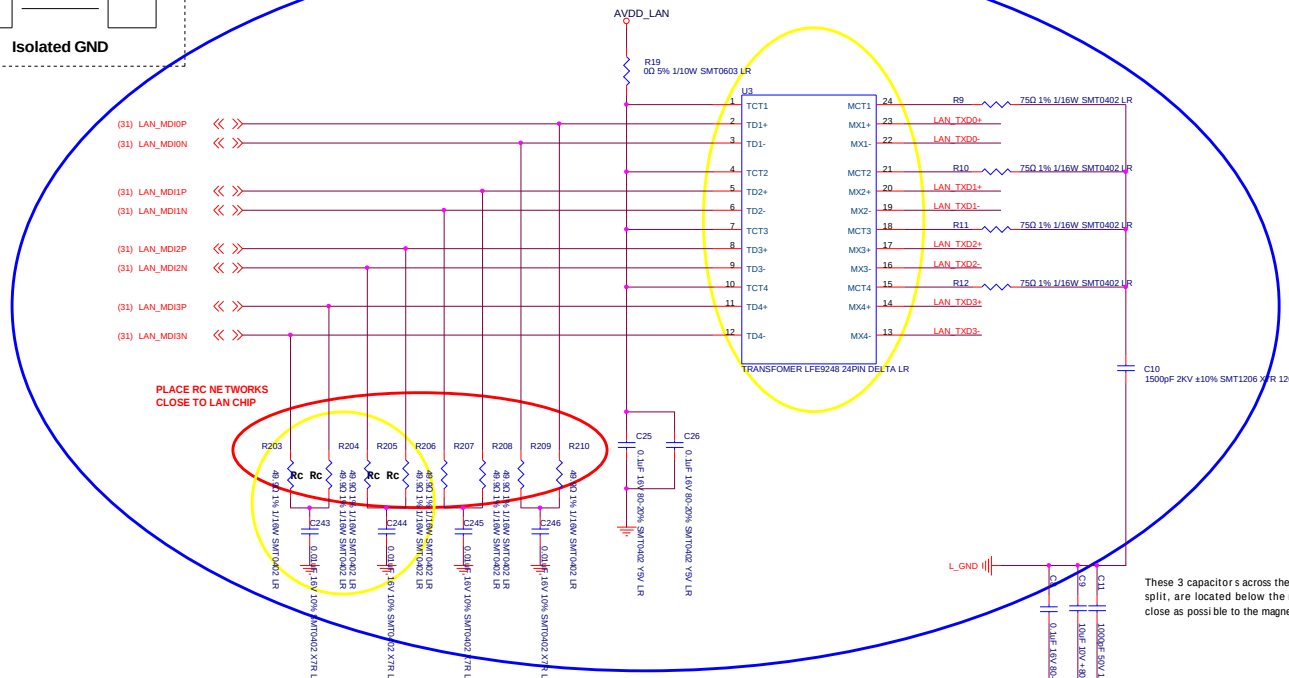
TX
RX 100 ohm ---> trace 4 mil , space 10 mil
50 mil space from other signals
Total Tace Length no more thans 4.8"
2 Differential pairs must have the same length



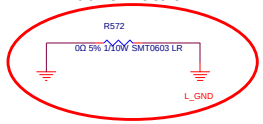
Xa: Transformer use LFE9248(12-01904-01)

Pa: Transformer use LFE8466(12-02109-01)

Add on 5/7/07

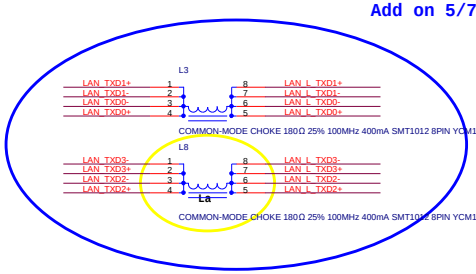


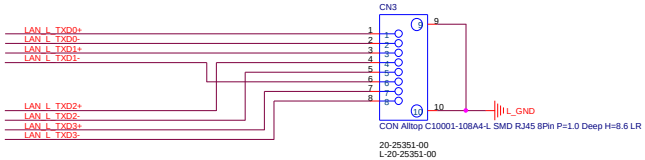
Add on 06/04



	for 88E8055	for 88E8039
Rc	STUFF	NU
La	STUFF	NU

Add on 5/7/07





(31) AVDD_LAN — AVDD_LAN

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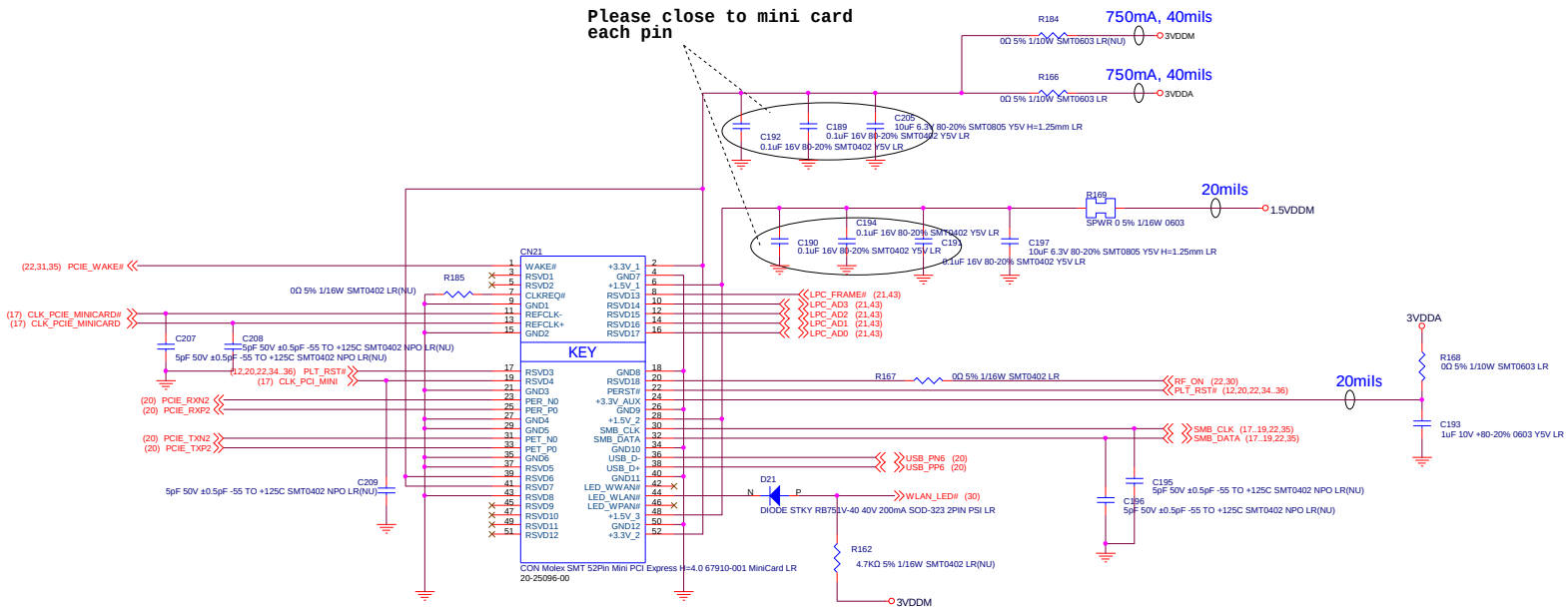
PCIE Mini Card for Wireless Lan



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Title: MR055 / MR056

Size: C | Document Number: PCIE Mini Card | Rev: 0.2

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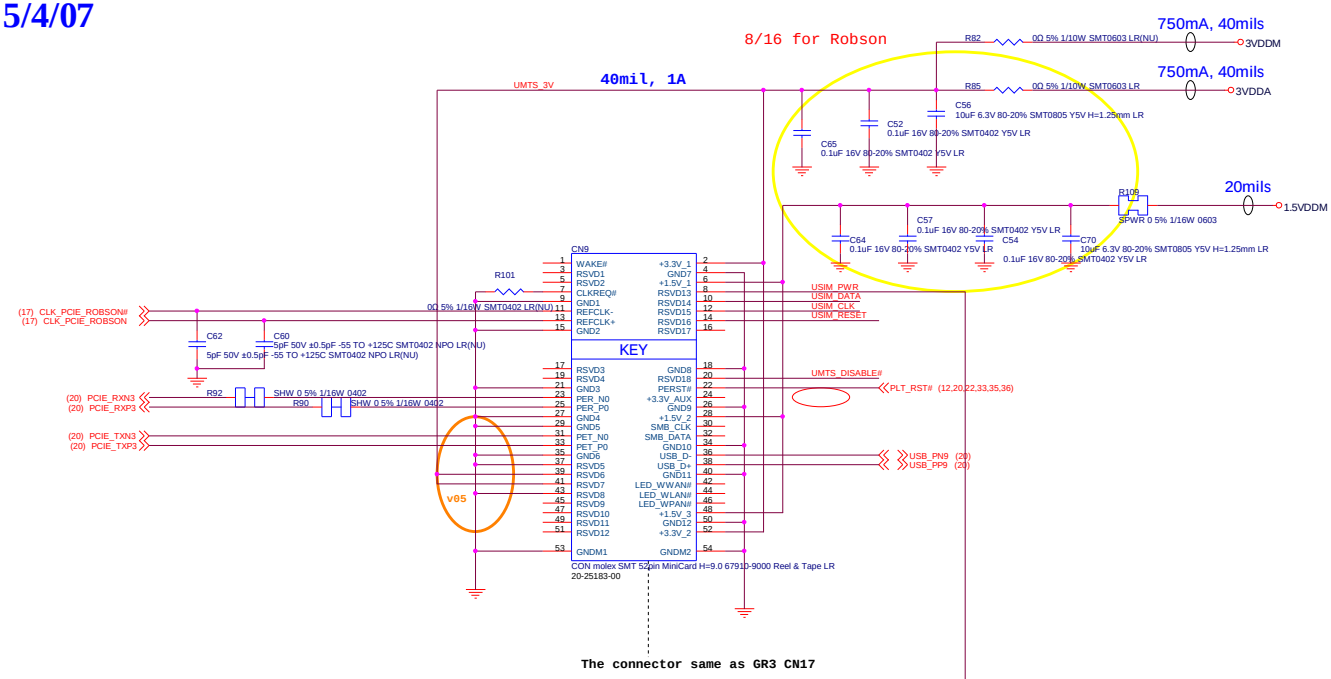
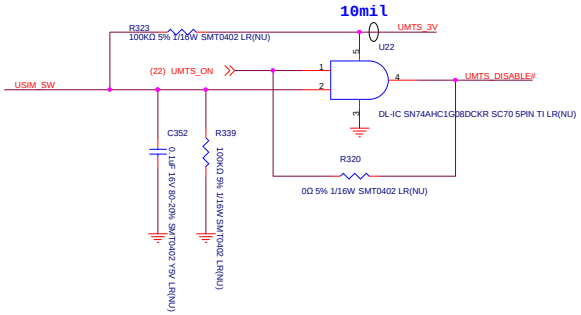
檔

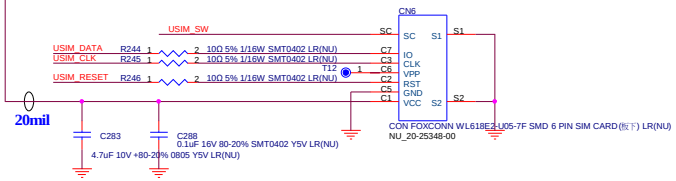
Robson / UMTS
Add on 5/4/07



The connector same as GR3 CN17

SIM Card Switch





SIM Card CN

(9,14,15,20,21,23,33,35,49) 1.5VDDM → 1.5VDDM
(10,12,15,17..20,22..27,29..31,33,35,37,43,45,48..51) 3VDDM → 3VDDM
(10,20..24,26,30,31,33,35,40,43,46,48..50) 3VDDA → 3VDDA
(23,28,30,45,48..51) 5VDDA → 5VDDA

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Title: MR055 / MR056

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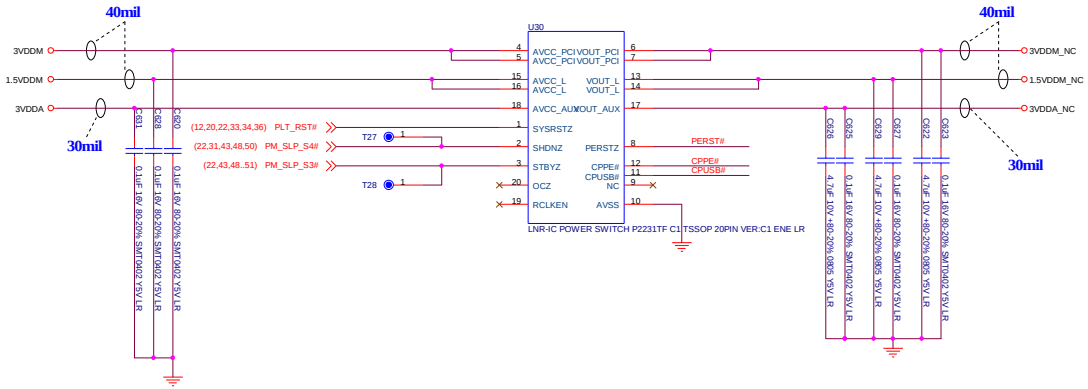
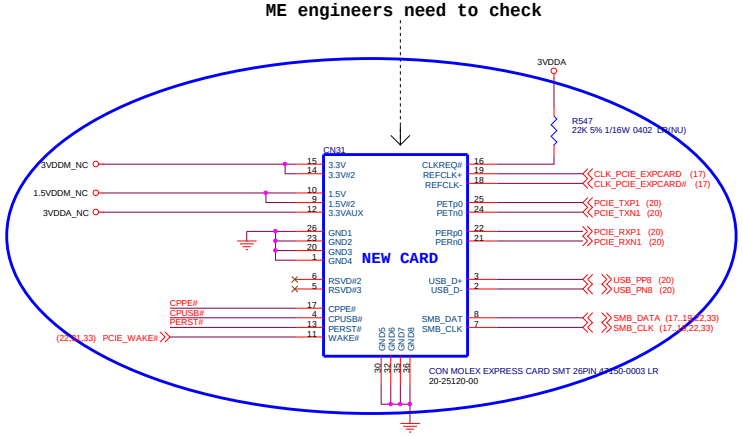
New Card(express card)



X,Y follow LM10W ME drawing 5/10

ME engineers need to check



(10,20..24,26,30,31,33,34,40,43,46,48..50) 3VDDA — 3VDDA

(9,14,15,20,21,23,33,34,49) 1.5VDDM — 1.5VDDM

(10,12,15,17..20,22..27,29..31,33,34,37,43,45,48..51) 3VDDM — 3VDDM

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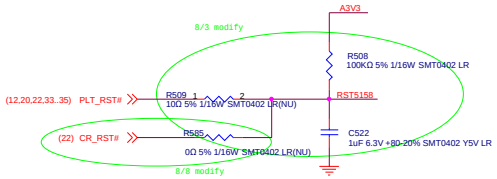
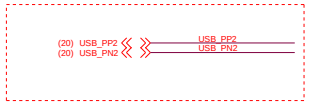
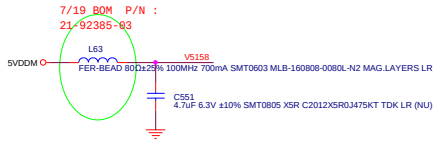
New add on 5/4/07

X,Y follow PA354

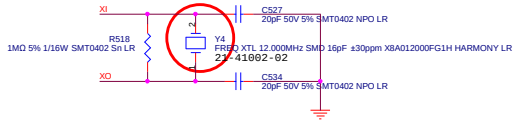


INTERFACE





change package on 0525



(10,23,25,27,29,30,38,39,48) 5VDDM — 5VDDM

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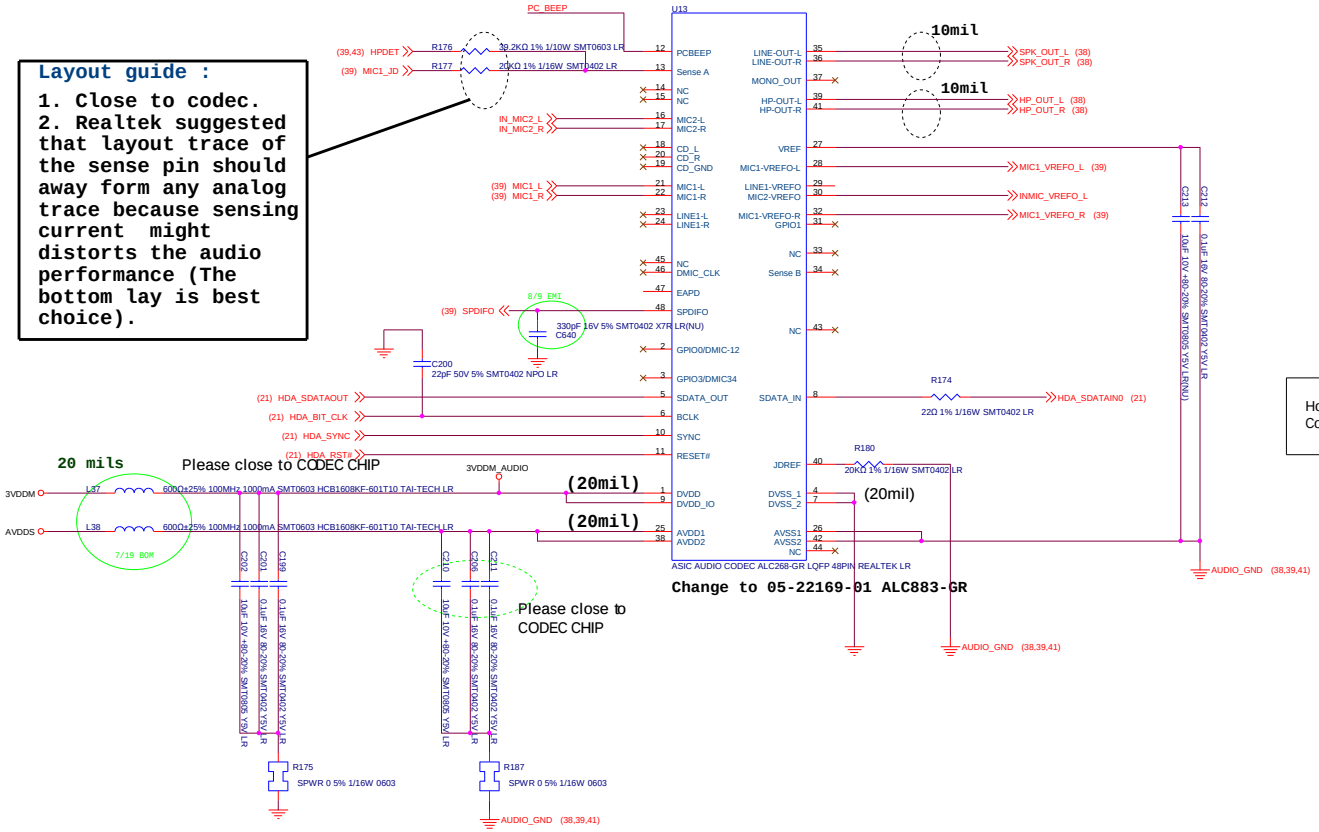
AC97/AZALIA CODEC DUAL LAYOUT

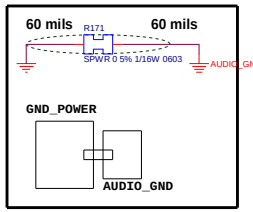
USE AL883 GR / AZALIA

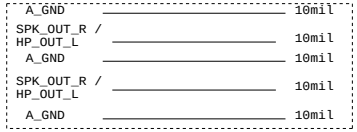
10mil GND_POWER
10mil AZALIA_PCBEEP 10mil
10mil GND_POWER 10mil
10mil GND_POWER 10mil 14MCLK_AZALIA
10mil GND_POWER 10mil
10mil GND_POWER
10mil AZALIA_BITCLK 10mil
10mil GND_POWER 10mil

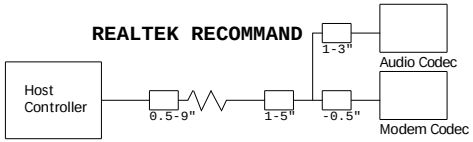
Layout guide :

1. Close to codec.
2. Realtek suggested that layout trace of the sense pin should away form any analog trace because sensing current might distorts the audio performance (The bottom lay is best choice).

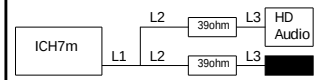








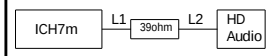
HD Audio-ACZ_SDOUT/ACZ_SYNC/ACZ_BITCLK/ACZ_RESET#



Trace Impedance	Routing Requirement	Trace Length
55 +/- 15%	4 on 7(stripline) 5 on 7(microstrip)	L1 = 0.5"~2.5" L2 <= 0.1" L3 = 1"~8"

*** L3 can be extened up to 15" if HD Audio docking is not used

HD Audio-ACZ_SDIN

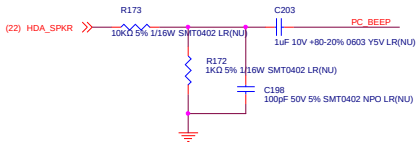


Trace Impedance	Routing Requirement	Trace Length
55 +/- 15%	4 on 7(stripline) 5 on 7(microstrip)	L1 = 0.1"~15" L2 <= 0.5"

*** Breakout can be routed 4 on 4 up to 500 mils

Layout guide :

1. The codec is partitioned into a digital and analog sections to help isolated noisy digital circuitry form quiet analog circuitry.
2. The layout separates the analog and digital planes with a 60 to 100 mils gap and connect them at one point beneath the codec with a 50 mils wide blink.
3. Never route digital traces or digital planes under the analog ground areas. Analog components should be located over analog planes (ground and power planes) and digital components should be located over digital planes.



(10,12,15,17..20,22..27,29..31,33..35,43,45,48..51) 3VDDM → 3VDDM
(38) AVDDS → AVDDS

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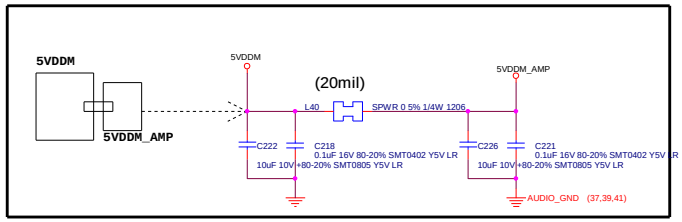
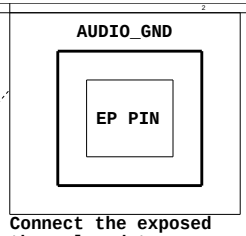
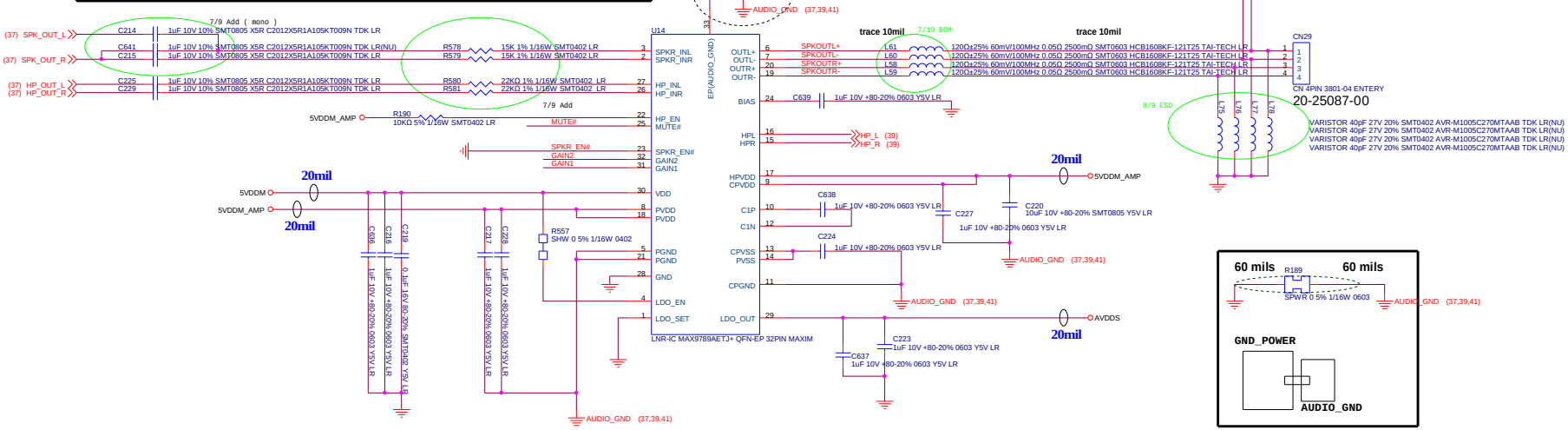


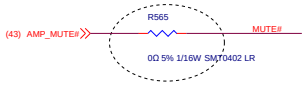


Connect the exposed thermal pad to AUDIO_GND

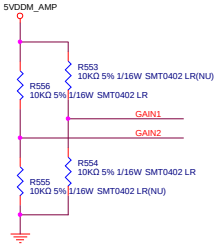


SPKR_EN# = High :Disable Speaker Amplifiers
HP_EN = Low :Disable the Headphone Amplifiers

AMP MUTE#



L Mute Enable



Speaker Mode gain(Max)

GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

(10,12,15,17..20,22..27,29..31,33..35,37,43,45,48..51) 3VDDM → 3VDDM
(10,23,25,27,29,30,36,39,48) 5VDDM → 5VDDM
(37) AVDDS → AVDDS

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檔

Modify on 5/23
Follow PA354

Audio board need stuff

CN32
CN 15PIN 88282-1501 ACES LR.Normal
20-25229-00
SPDIFO
SPDIFO (37)
HPDET (37,43)
MIC1_JD (37)
HP_L_CN
HP_R_CN
MIC1_L_CN
MIC1_R_CN
15mil
5VDDM
AUDIO_GND (37,38,41)

Audio board need stuff

R550
1KΩ 5% 1/16W SMT0402 LR
AUDIO_GND (37,38,41)

NOTE
HP_L,HP_R請包AGROUND

Audio board need stuff

(37,43) HPDET
HPDET
C619
0.1uF 25V 80-20% SMT0603 Y5V LR(NU)
R548
0Ω 5% 1/10W SMT0603 LR(NU)
L64
600Ω±25% 100MHz 150mA SMT0603 MLB-160808-0600A-N2 MAG.LAYERS LR(NU)
AUDIO_GND (37,38,41)
R549
0Ω 5% 1/10W SMT0603 LR(NU)
CN33
7/9 modify
(38) HP_L
(38) HP_R
R552
R551
47Ω 5% 1/16W SMT0402 LR
HP_L_CN
HP_R_CN
600Ω±25% 100MHz 150mA SMT0603 MLB-160808-0600A-N2 MAG.LAYERS LR(NU)
L66
L65
L73
L74
SPDIFO
SPDIF_PWR
5VDDM
C624
C630
1000pF 50V 10% SMT0402 X7R LR (NU)
7/9 modify
C642
0.1uF 16V 80-20% SMT0402 Y5V LR(NU)
R182
0Ω 5% 1/10W SMT0603 LR(NU)
AUDIO_GND (37,38,41)
HEADPHONE JACK
CN SINGATRON SMT 2SJ-A373-001 LR(NU)
NU_20-24459-90
L-20-24459-90
R546
0Ω 5% 1/10W SMT0603 LR(NU)
AUDIO_GND (37,38,41)

Audio board need stuff

8/15 modify
RP53
4.7KΩ 5% 1010 1/16W 4P2R LR
MIC1_VREFO_L (37)
MIC1_VREFO_R (37)
R558
0Ω 5% 1/10W SMT0603 LR(NU)
L39
600Ω±25% 100MHz 150mA SMT0603 MLB-160808-0600A-N2 MAG.LAYERS LR(NU)
CN34
CON SINGATRON DIP 6PIN 2SJ-R820-007 PHONE JACK LR(NU)
NU_20-25295-00
L-20-25295-00
L67
L68
600Ω±25% 100MHz 150mA SMT0603 MLB-160808-0600A-N2 MAG.LAYERS LR(NU)
MIC1_L_CN
MIC1_R_CN
MIC1_JD
C633
C634
4.7uF 25V ±20% SMT0805 X5R C2012X5R1E475MT TDK LR
MIC1_L (37)
MIC1_R (37)
MIC1_JD (37)
C632
1000pF 50V 10% SMT0402 X7R LR(NU)
C635
1000pF 50V 10% SMT0402 X7R LR(NU)
MAGND
MIC IN

NOTE
MIC1IN,MIC2IN, MIC_JD,請包AGROUND

R186
0Ω 5% 1/10W SMT0603 LR(NU)
MAGND
AUDIO_GND (37,38,41)

(10,23,25,27,29,30,36,38,48) 5VDDM
5VDDM

R18
MIC CNN
L_CASEGND
MAGND
AGND
L10
R2

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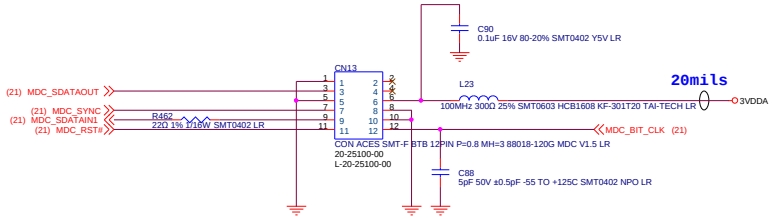
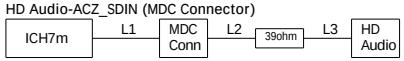
檔

MDC 1.5 CNN

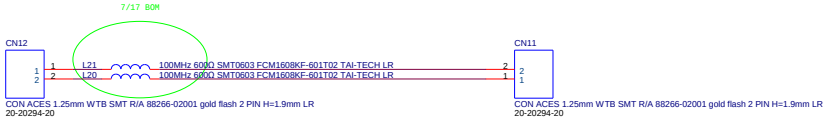


HD Audio-ACZ_SDIN (MDC Connector)



Trace Impedance	Routing Requirement	Trace Length
55 +/- 15%	4 on 7(stripline)	L1 = 0.1"~15" L2 = 0.5"~1.5" L3 = 0.5"

*** Breakout can be routed 4 on 4 up to 400 mils



(10,20..24,26,30,31,33..35,43,46,48..50) 3VDDA — 3VDDA

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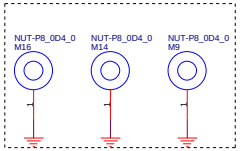
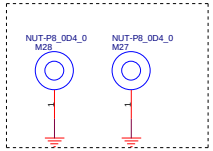
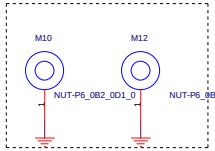
stuff
P/N:24-10966-51
For CPU Heat Sink



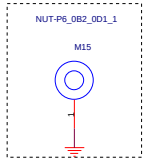
stuff
P/N:24-10966-51
For FAN



stuff
P/N:24-10732-21
For MDC

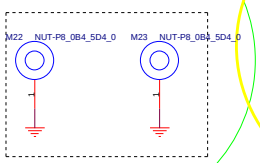


stuff
P/N:24-10732-21
For NB heat sink

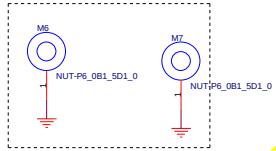


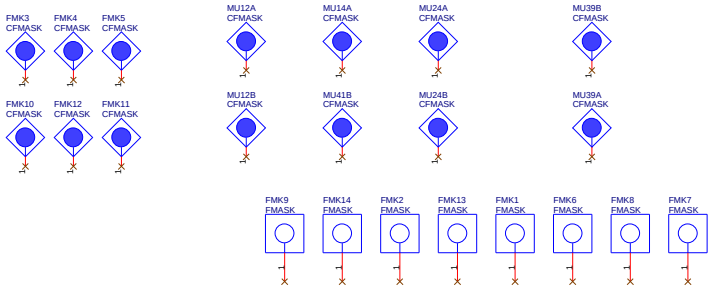
7/9 modify

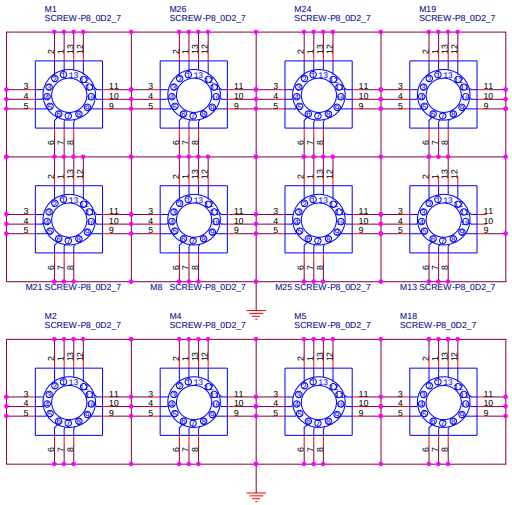
stuff
P/N:24-11743-50
For mini car

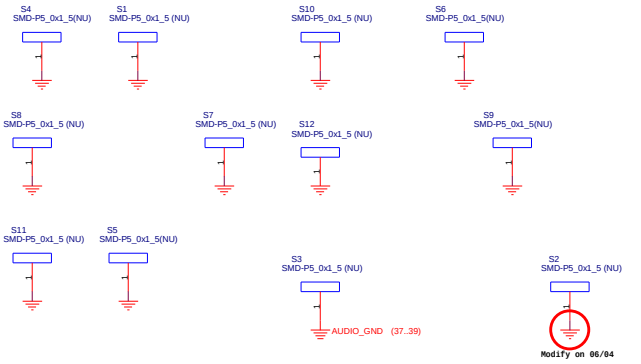


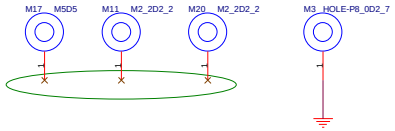
Add on 5/7/07
Not stuff 8/16 for Robson
P/N:24-11618-50
For Robson connector NUT





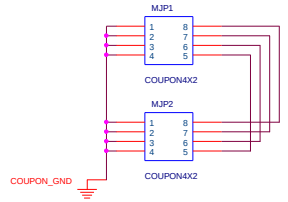






9/26 Change not connect to GND

COUPON4X2



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EMI Solution

C682 : VGA_VDD ---- P.51
C681 : Q19 pin4 --- P.45
C680 : R200 pin 1 -- P.46
C679 : 3VDDA ------- P.48
C678 : DCIN -------- P.47
C677 : DCIN -------- P.47
C676 : DCIN -------- P.47
C675 : DCIN -------- P.47
C674 : 3VDDA ------- P.48

C673 : 1.5VDDM ----- P.49
C672 : 1.25VDDM ---- P.49
C671 : 1.5VDDM ----- P.49
C670 : 1.5VDDM ----- P.49
C669 : DCIN -------- P.47
C668 : ADPIN ------- P.46
C667 : 1.05VDDM ---- P.50

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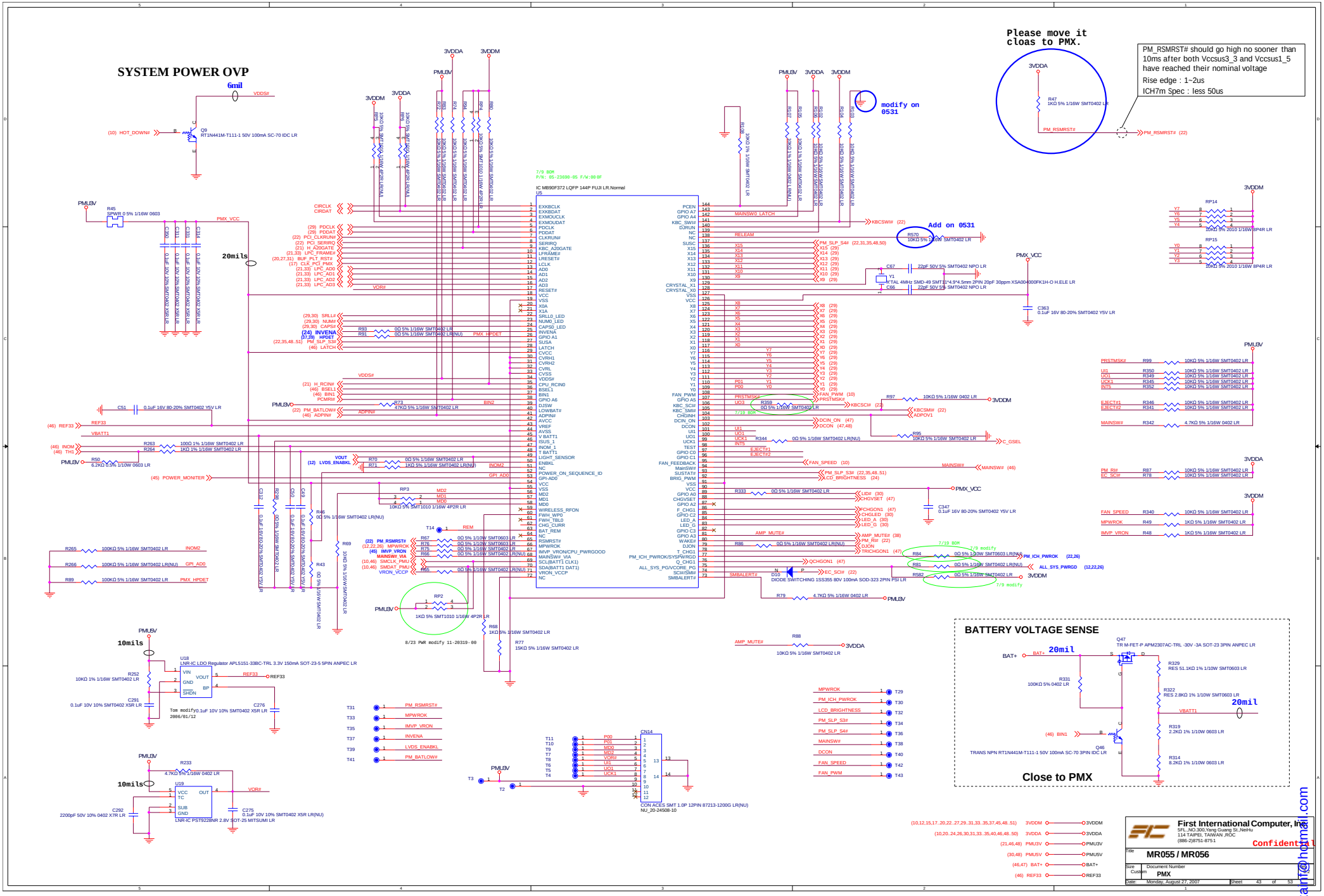

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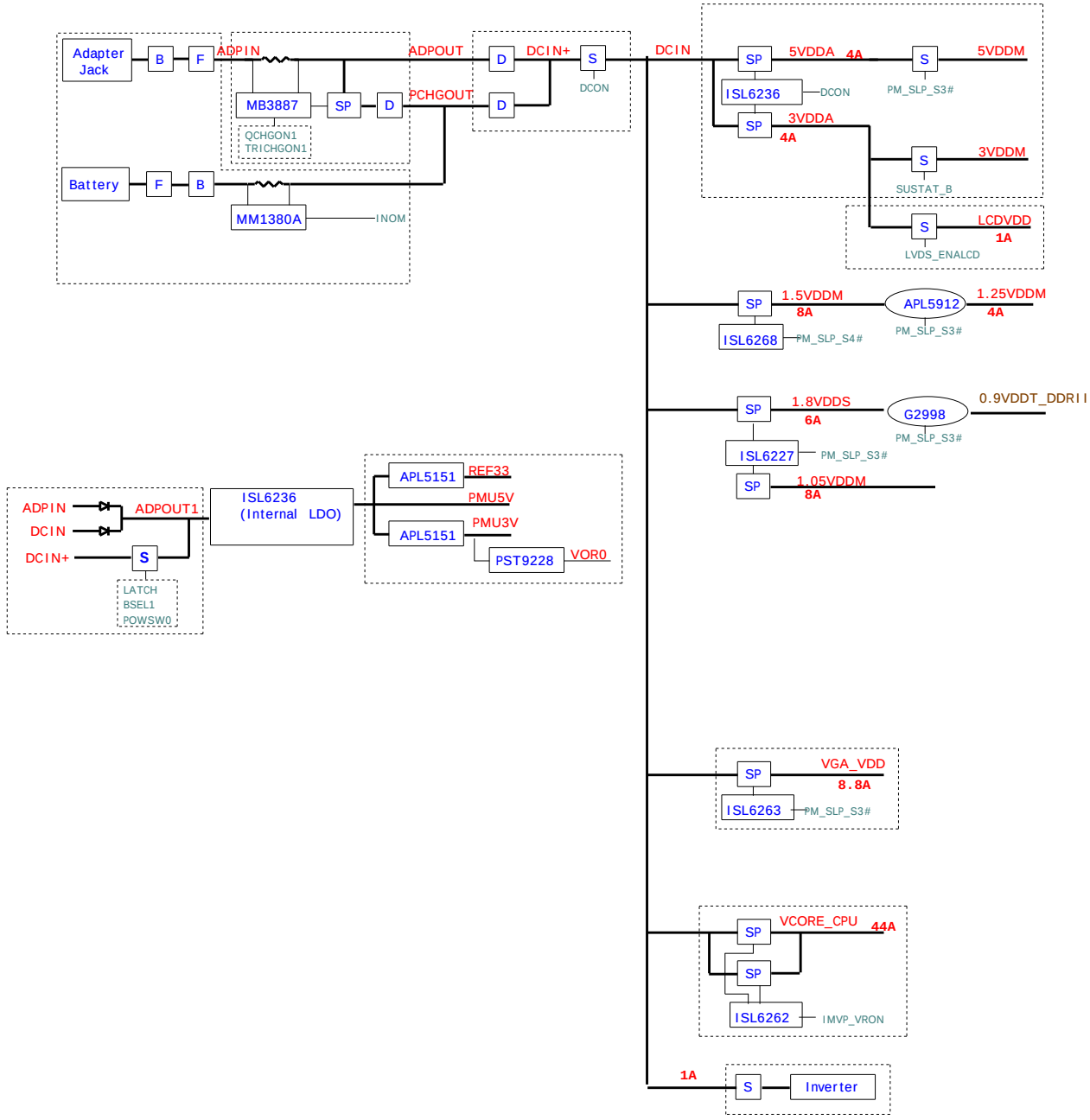
MR055/MR056 Power Block



Signal
Power Path
LDO
Amplifier
B Bead
D Diode
F Fuse
S Switch
SP Switching Power Converter

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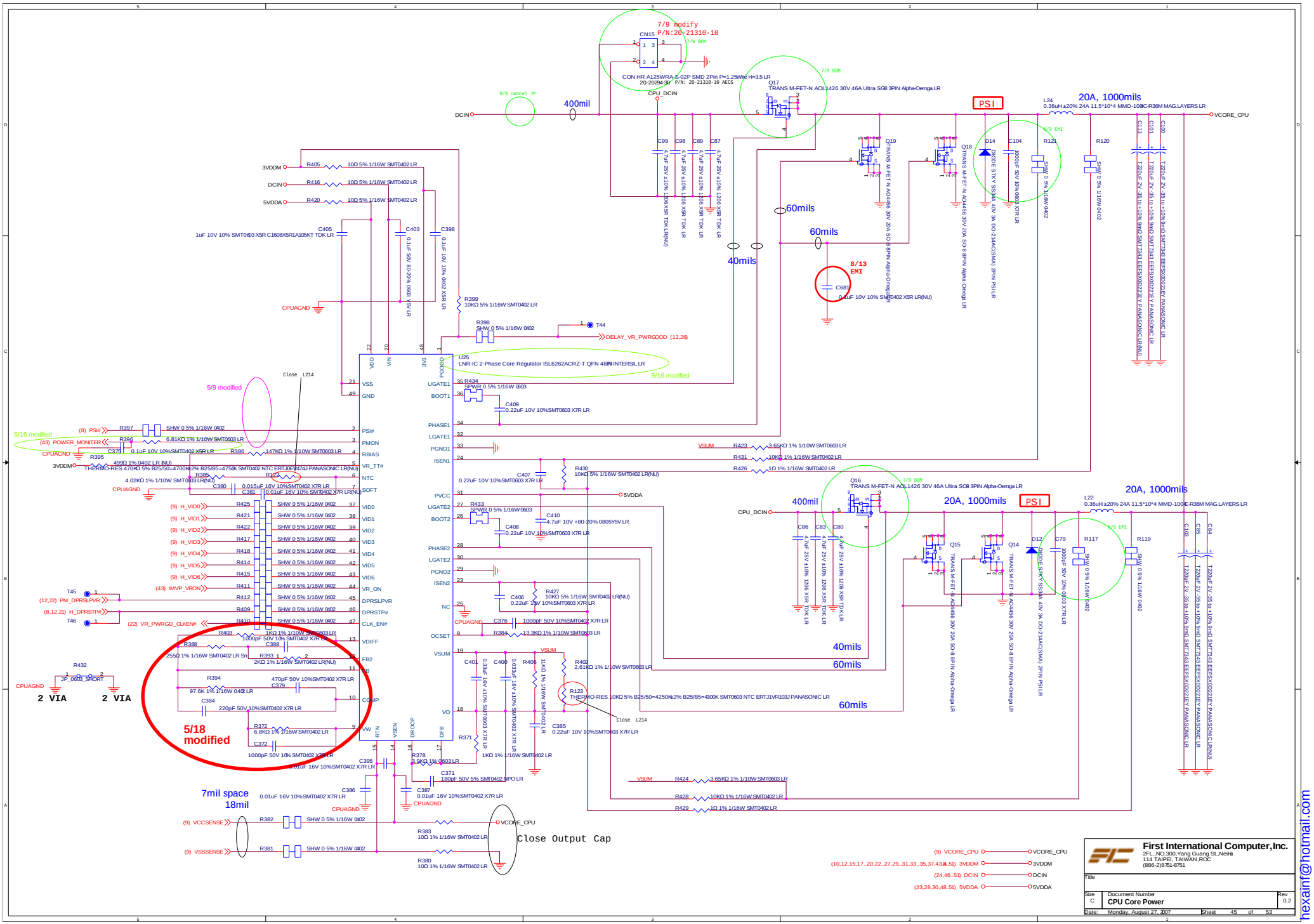

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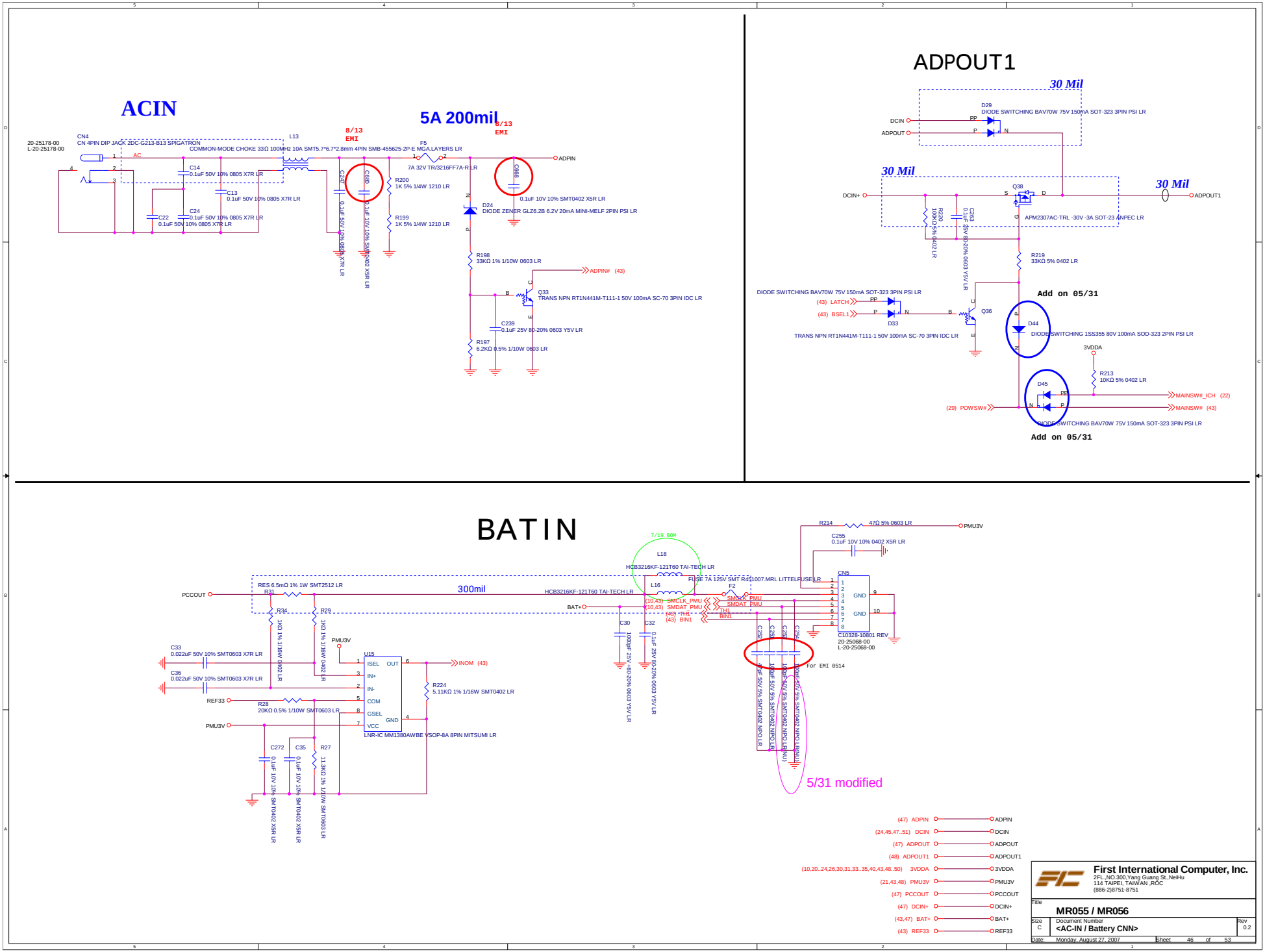
ACIN
5A 200mil
8/13 EMI
8/13 EMI
CN4
CN 4PIN DIP JACK 2DC-G213-B13 SPIGATRON
20-25178-00
L-20-25178-00
L13
COMMON-MODE CHOKE 33Ω 100MHz 10A SMT5.7*6.7*2.8mm 4PIN SMB-455625-2P-E MGA LAYERS LR
F5
7A 32V TR/3216FF7A-R LR
AC
C14 0.1uF 50V 10% 0805 X7R LR
C13 0.1uF 50V 10% 0805 X7R LR
C22 0.1uF 50V 10% 0805 X7R LR
C24 0.1uF 50V 10% 0805 X7R LR
C227 0.1uF 50V 10% 0805 X7R LR
C680 0.1uF 10V 10% SMT0402 X5R LR
R200 1K 5% 1/4W 1210 LR
R199 1K 5% 1/4W 1210 LR
C669 0.1uF 10V 10% SMT0402 X5R LR
ADPIN
D24 DIODE ZENER GLZ6.2B 6.2V 20mA MINI-MELF 2PIN PSI LR
R198 33KΩ 1% 1/10W 0603 LR
ADPIN# (43)
Q33 TRANS NPN RT1N441M-T111-1 50V 100mA SC-70 3PIN IDC LR
C239 0.1uF 25V 80-20% 0603 Y5V LR
R197 6.2KΩ 0.5% 1/10W 0603 LR
ADPOUT1
30 Mil
D29 DIODE SWITCHING BAV70W 75V 150mA SOT-323 3PIN PSI LR
DCIN
ADPOUT
30 Mil
30 Mil
DCIN+
Q38 APM2307AC-TRL -30V -3A SOT-23 ANPEC LR
ADPOUT1
R220 100KΩ 5% 0402 LR
C263 0.1uF 25V 80-20% 0603 Y5V LR
R219 33KΩ 5% 0402 LR
DIODE SWITCHING BAV70W 75V 150mA SOT-323 3PIN PSI LR
(43) LATCH
(43) BSEL1
D33
TRANS NPN RT1N441M-T111-1 50V 100mA SC-70 3PIN IDC LR
Q36
Add on 05/31
D44 DIODE SWITCHING 1SS355 80V 100mA SOD-323 2PIN PSI LR
3VDDA
R213 10KΩ 5% 0402 LR
D45
(29) POWSW#
MAINSW#_ICH (22)
MAINSW# (43)
DIODE SWITCHING BAV70W 75V 150mA SOT-323 3PIN PSI LR
Add on 05/31
BATIN
7/19 BOM
L18
HCB3216KF-121T60 TAI-TECH LR
L16
HCB3216KF-121T60 TAI-TECH LR
FUSE 7A 125V SMT R451007.MRL LITTELFUSE LR
F2
300mil
PCCOUT
RES 6.5mΩ 1% 1W SMT2512 LR
R31
R34 1KΩ 1% 1/16W 0402 LR
R29 1KΩ 1% 1/16W 0402 LR
BAT+
(10,43) SMCLK_PMU
(10,43) SMDAT_PMU
(45) TH1
(43) BIN1
SMCLK_PMU
SMDAT_PMU
TH1
BIN1
C30 1000pF 25V +80-20% 0603 Y5V LR
C32 0.1uF 25V 80-20% 0603 Y5V LR
R214 47Ω 5% 0603 LR
PMU3V
C255 0.1uF 10V 10% 0402 X5R LR
CN5
GND
GND
C10328-10801 REV
20-25068-00
L-20-25068-00
C252 1uF 25V 10% SMT0603 X5R LR
C253 1uF 25V 10% SMT0603 X5R LR
C254 1uF 25V 10% SMT0603 X5R LR
C256 1uF 25V 10% SMT0603 X5R LR
For EMI 0514
5/31 modified
C33 0.022uF 50V 10% SMT0603 X7R LR
C36 0.022uF 50V 10% SMT0603 X7R LR
PMU3V
U15
ISEL
IN+
IN-
COM
GSEL
VCC
OUT
GND
INOM (43)
R224 5.11KΩ 1% 1/16W SMT0402 LR
REF33
R28 20KΩ 0.5% 1/10W SMT0603 LR
LNR-IC MM1380AWBE YSOP-8A 8PIN MITSUMI LR
C272 0.1uF 10V 10% SMT0402 X5R LR
C35 0.1uF 10V 10% SMT0402 X5R LR
R27 11.3KΩ 1% 1/10W SMT0603 LR
(47) ADPIN
(24,45,47..51) DCIN
(47) ADPOUT
(48) ADPOUT1
(10,20..24,26,30,31,33..35,40,43,48..50) 3VDDA
(21,43,48) PMU3V
(47) PCCOUT
(47) DCIN+
(43,47) BAT+
(43) REF33
ADPIN
DCIN
ADPOUT
ADPOUT1
3VDDA
PMU3V
PCCOUT
DCIN+
BAT+
REF33
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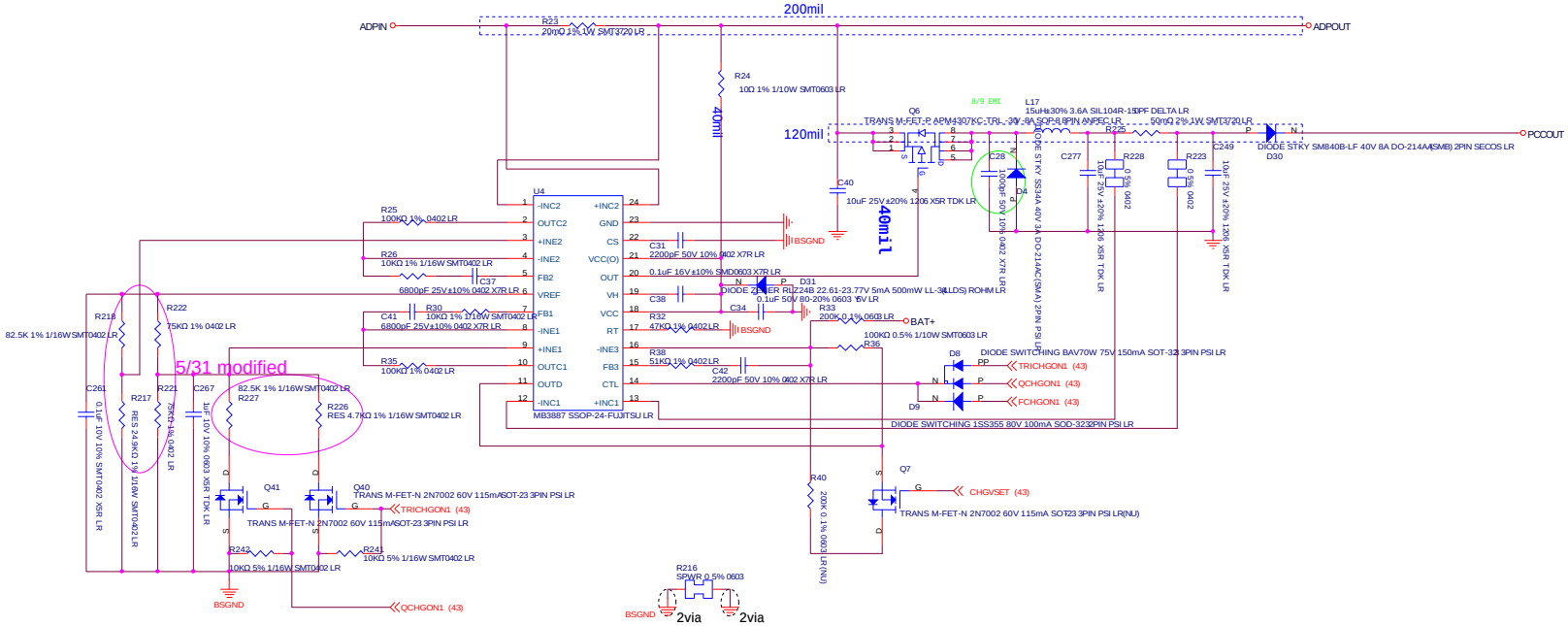
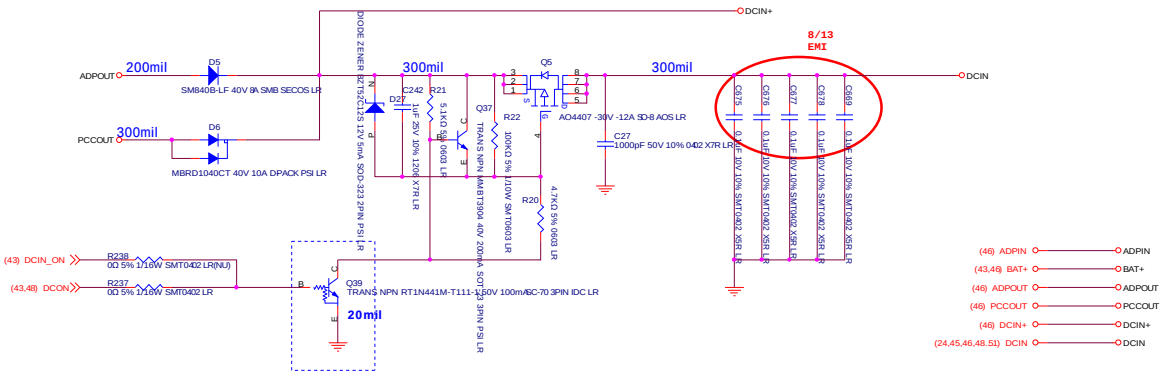
Charger



DCIN



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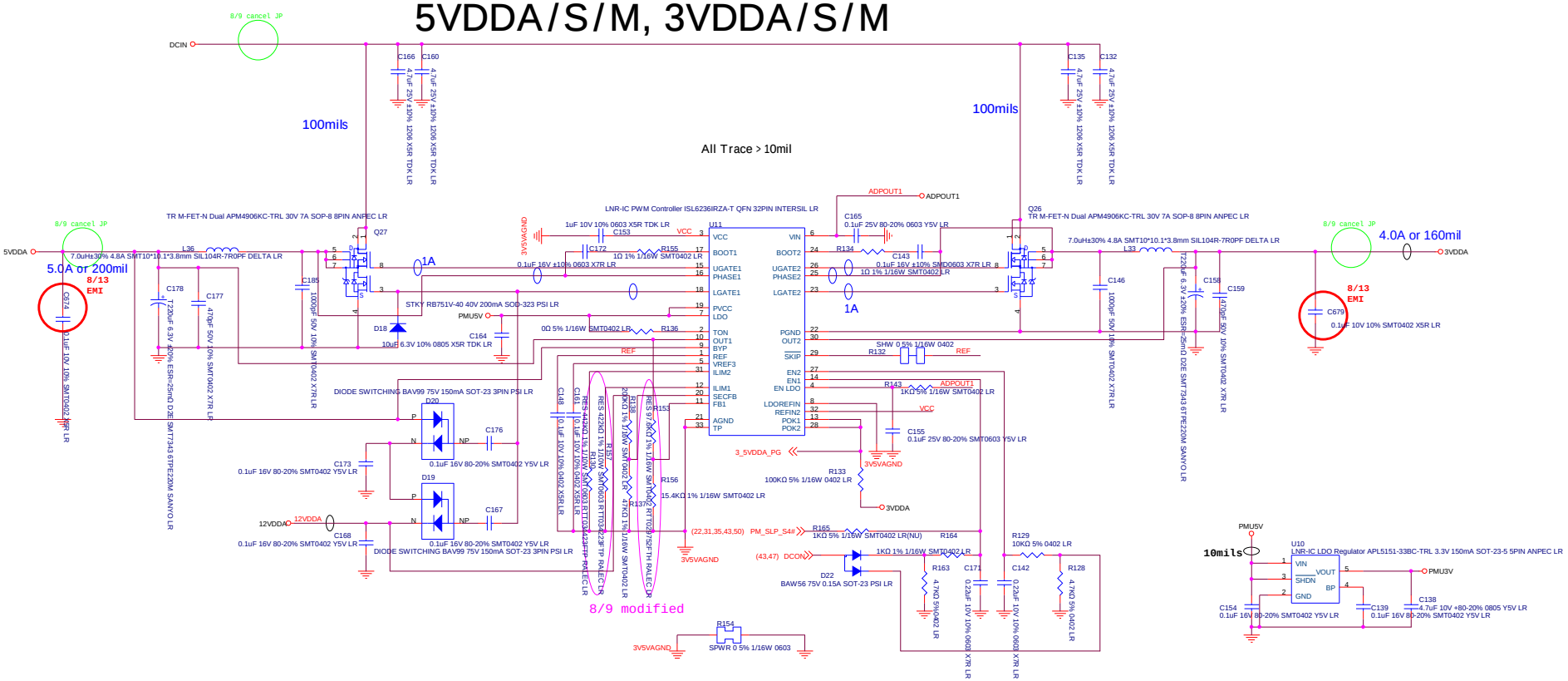
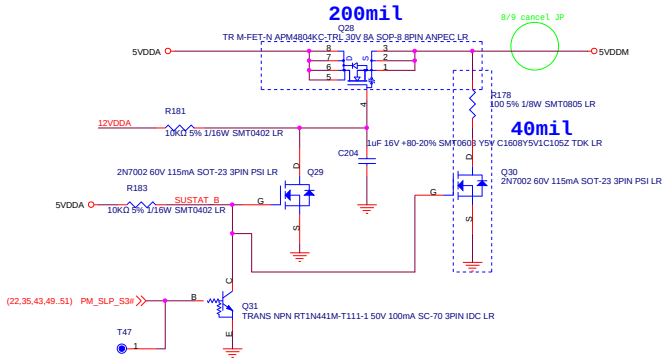
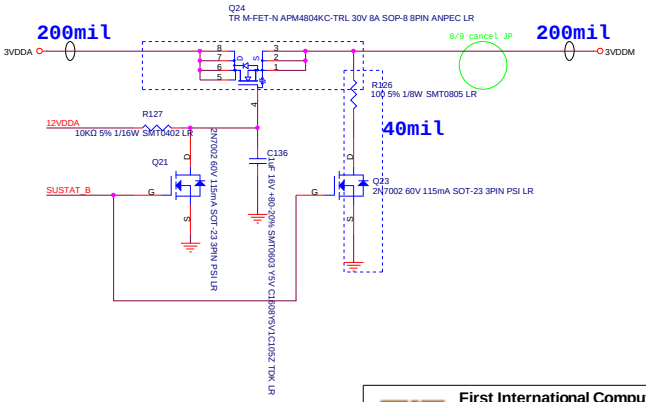
5VDDA/S/M, 3VDDA/S/M



5VDDS/5VDDM



3VDDS/3VDDM



(46) ADPOUT1	ADPOUT1
(24,45..47,49..51) DCIN	DCIN
(30,43) PMU5V	PMU5V
(21,43,46) PMU3V	PMU3V
(23,28,30,45,49..51) 5VDDA	5VDDA
(10,20..24,26,30,31,33..35,40,43,46,49,50) 3VDDA	3VDDA
(10,12,15,17..20,22..27,29..31,33..35,37,43,45,49..51) 3VDDM	3VDDM
(10,23,25,27,29,30,36,38,39) 5VDDM	5VDDM

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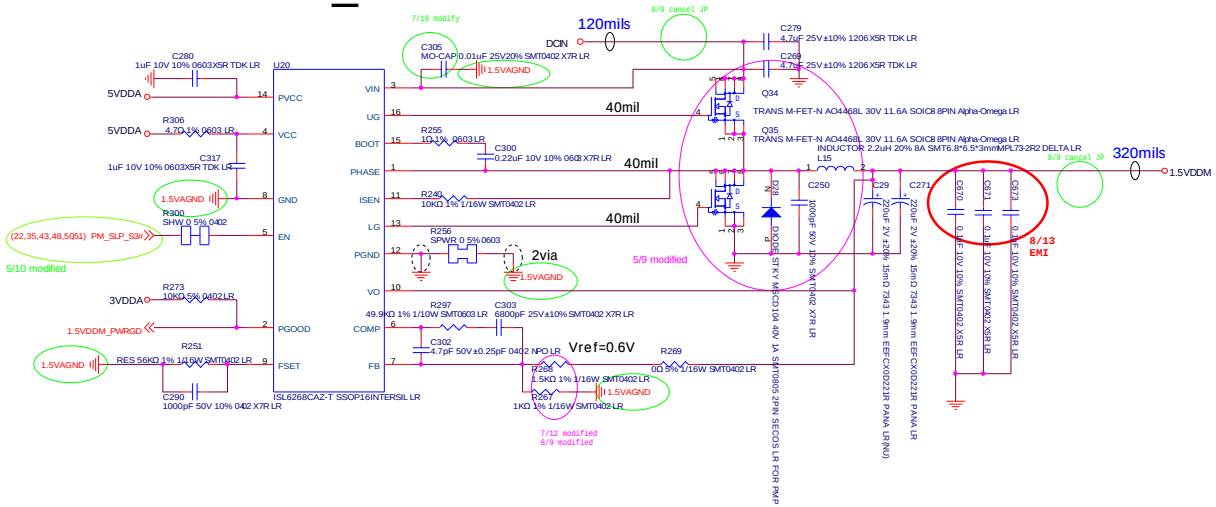
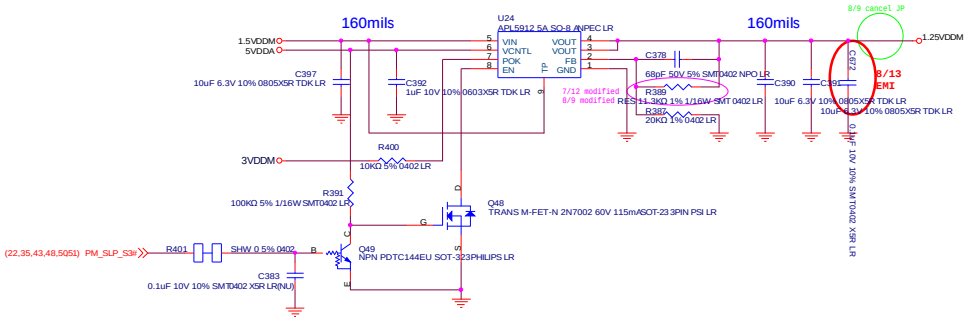
VCORE_GMCH



1.25VDDM



(24,45..48,50,51) DCIN — DCIN
(23,28,30,45,48,5051) 5VDDA — 5VDDA
(10,20..24,26,30,31,33..35,40,43,46,48,50) 3VDDA — 3VDDA
(9,14,15,20,21,23,33,35) 1.5VDDM — 1.5VDDM
(12,15,17,23) 1.25VDDM — 1.25VDDM
(10,12,15,17..20,22..27,29..31,33..35,37,43,45,48,50,51) 3VDDM — 3VDDM

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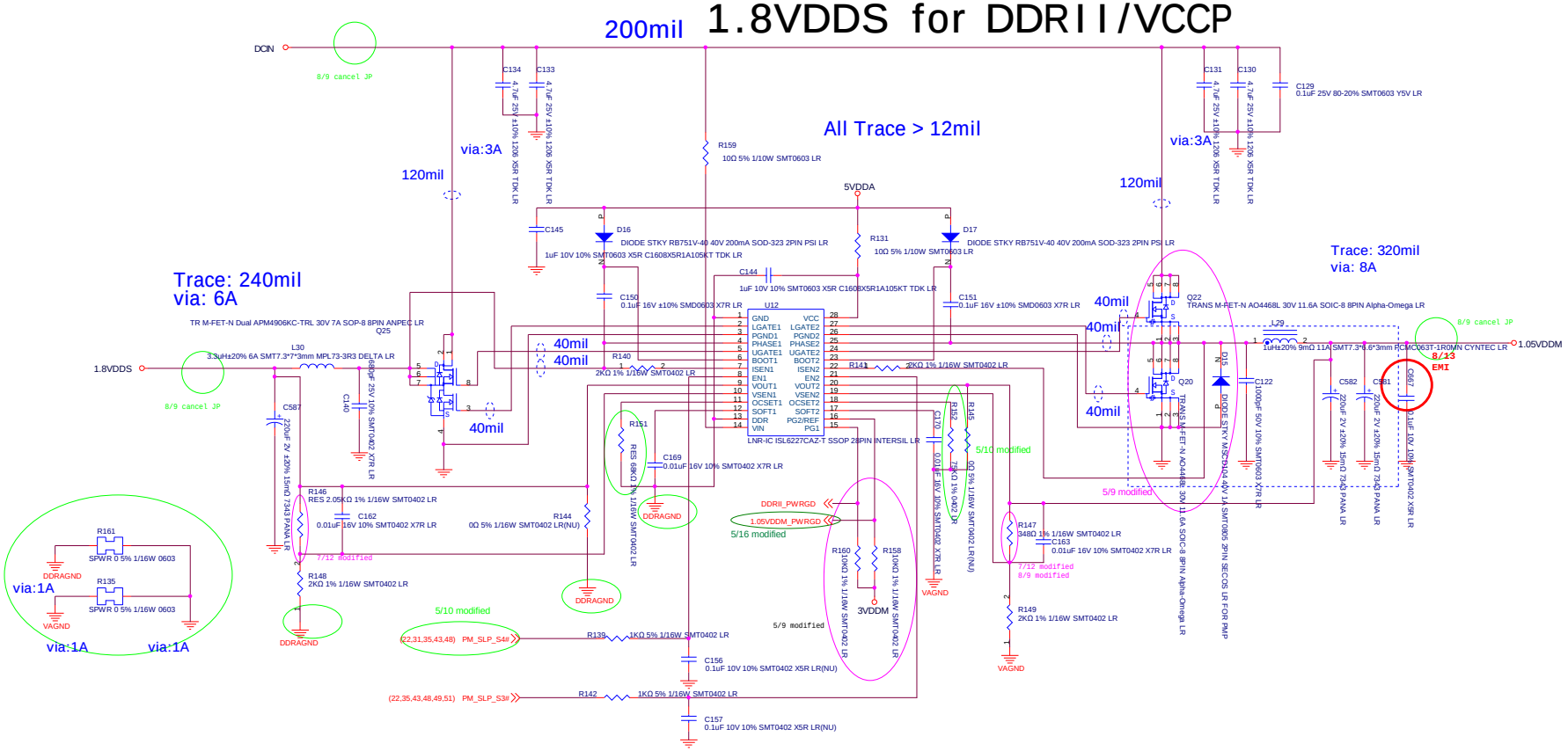
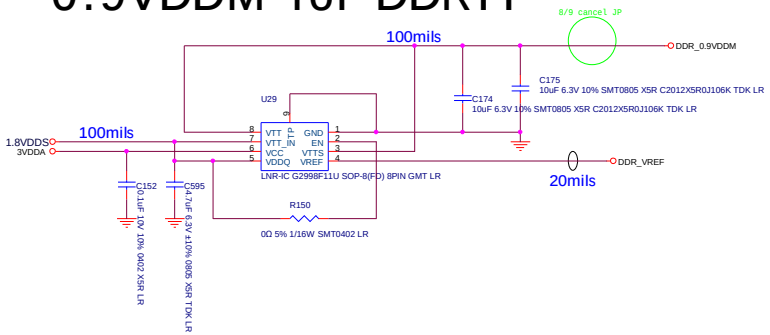
1.8VDDS for DDRII/VCCP



0.9VDDM for DDRII



(10,12,15,17..20,22..27,29..31,33..35,37,43,45,48,49,51) 3VDDM → 3VDDM
(8,9,11,14,15,17,21,23) 1.05VDDM → 1.05VDDM
(10,20..24,26,30,31,33..35,40,43,46,48,49) 3VDDA → 3VDDA
(23,28,30,45,48,49,51) 5VDDA → 5VDDA
(24,45..49,51) DCIN → DCIN
(12,18,19) DDR_VREF → DDR_VREF
(18,19) DDR_0.9VDDM → DDR_0.9VDDM
(12,14,15,18,19) 1.8VDDS → 1.8VDDS

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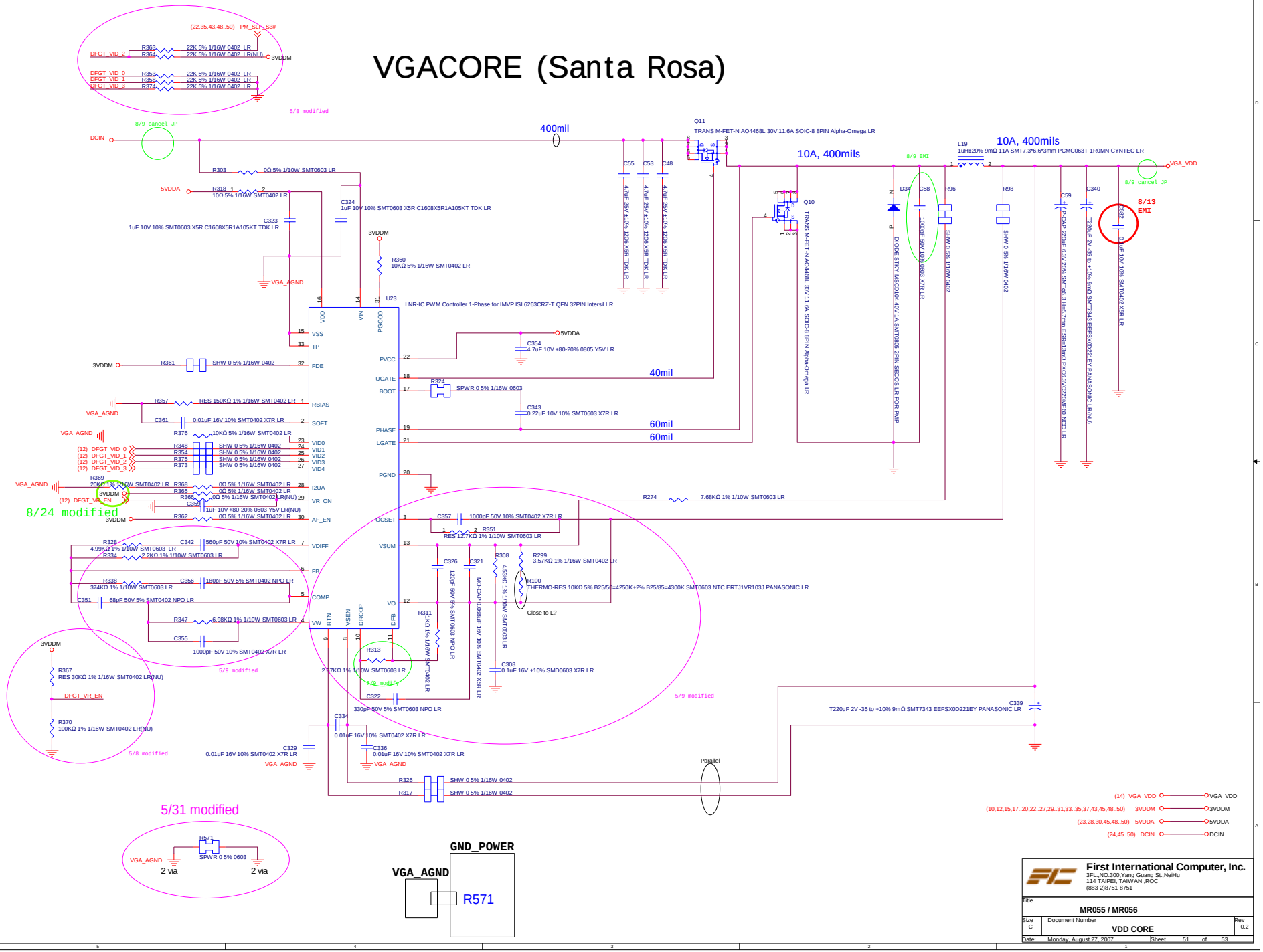

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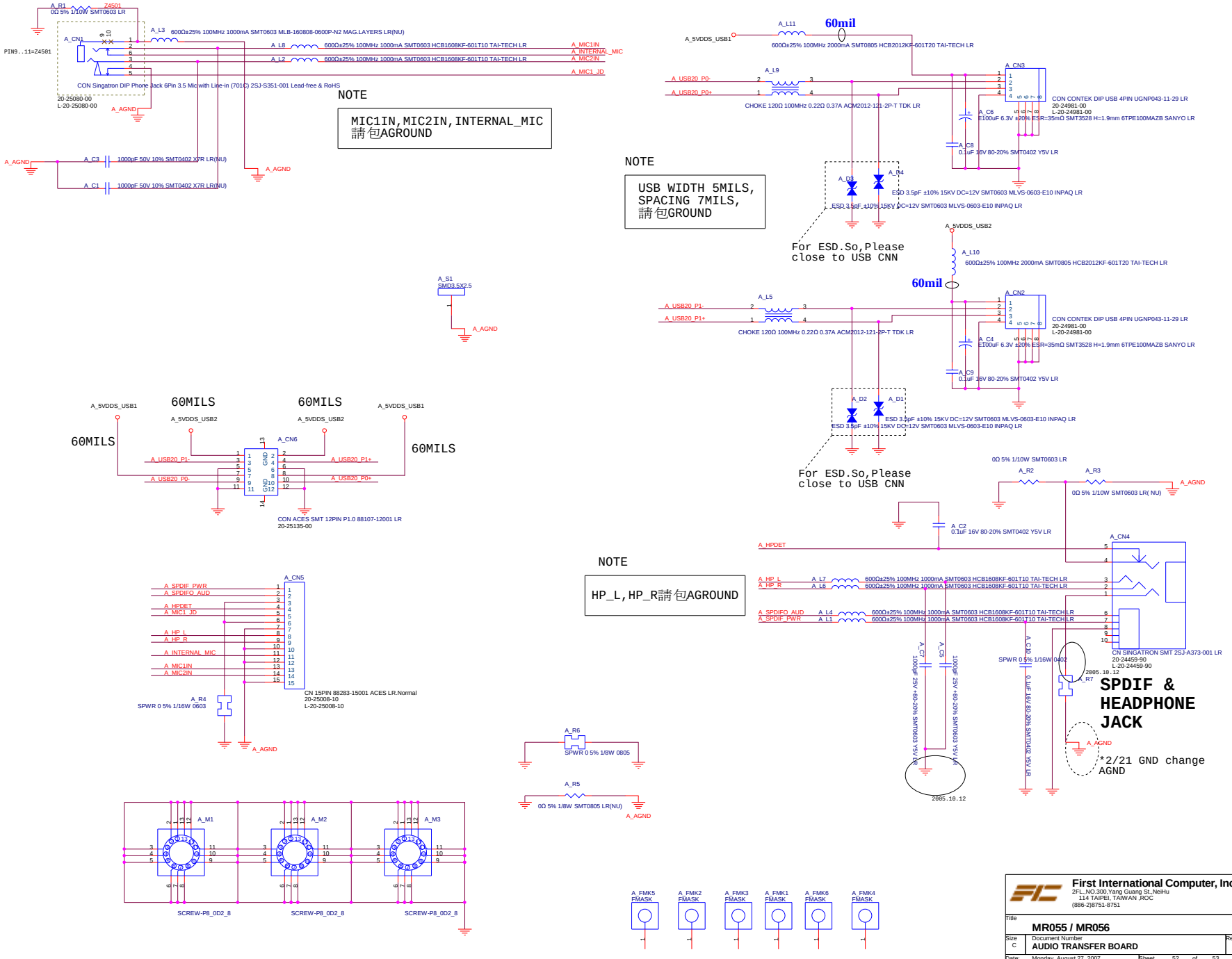
A_R1
Z4501
0Ω 5% 1/10W SMT0603 LR
A_CN1
PIN9..11=Z4501
A_L3
600Ω±25% 100MHz 1000mA SMT0603 MLB-160808-0600P-N2 MAG.LAYERS LR(NU)
A_L8
600Ω±25% 100MHz 1000mA SMT0603 HCB1608KF-601T10 TAI-TECH LR
A_L2
600Ω±25% 100MHz 1000mA SMT0603 HCB1608KF-601T10 TAI-TECH LR
A_MIC1IN
A_INTERNAL_MIC
A_MIC2IN
A_MIC1_JD
CON Singatron DIP Phone Jack 6Pin 3.5 Mic with Line-in (701C) 2SJ-S351-001 Lead-free & RoHS
20-25080-00
L-20-25080-00
A_AGND
A_C3
1000pF 50V 10% SMT0402 X7R LR(NU)
A_C1
1000pF 50V 10% SMT0402 X7R LR(NU)
NOTE
MIC1IN,MIC2IN,INTERNAL_MIC
請包AGROUND
A_5VDDS_USB1
A_L11
60mil
600Ω±25% 100MHz 2000mA SMT0805 HCB2012KF-601T20 TAI-TECH LR
A_CN3
A_USB20_P0-
A_USB20_P0+
A_L9
CHOKE 120Ω 100MHz 0.22Ω 0.37A ACM2012-121-2P-T TDK LR
CON CONTEK DIP USB 4PIN UGNP043-11-29 LR
20-24981-00
L-20-24981-00
A_C6
E100uF 6.3V ±20% ESR=35mΩ SMT3528 H=1.9mm 6TPE100MAZB SANYO LR
A_C8
0.1uF 16V 80-20% SMT0402 Y5V LR
A_D1
A_D4
ESD 3.5pF ±10% 15KV DC=12V SMT0603 MLVS-0603-E10 INPAQ LR
NOTE
USB WIDTH 5MILS,
SPACING 7MILS,
請包GROUND
For ESD.So,Please
close to USB CNN
A_5VDDS_USB2
A_L10
600Ω±25% 100MHz 2000mA SMT0805 HCB2012KF-601T20 TAI-TECH LR
60mil
A_CN2
A_USB20_P1-
A_USB20_P1+
A_L5
CHOKE 120Ω 100MHz 0.22Ω 0.37A ACM2012-121-2P-T TDK LR
CON CONTEK DIP USB 4PIN UGNP043-11-29 LR
20-24981-00
L-20-24981-00
A_C4
E100uF 6.3V ±20% ESR=35mΩ SMT3528 H=1.9mm 6TPE100MAZB SANYO LR
A_C9
0.1uF 16V 80-20% SMT0402 Y5V LR
A_D2
A_D1
ESD 3.5pF ±10% 15KV DC=12V SMT0603 MLVS-0603-E10 INPAQ LR
For ESD.So,Please
close to USB CNN
A_S1
SMD3.5X2.5
A_AGND
A_5VDDS_USB1
60MILS
A_5VDDS_USB2
60MILS
A_5VDDS_USB2
60MILS
A_5VDDS_USB1
60MILS
A_CN6
A_USB20_P1-
A_USB20_P0-
A_USB20_P1+
A_USB20_P0+
CON ACES SMT 12PIN P1.0 88107-12001 LR
20-25135-00
0Ω 5% 1/10W SMT0603 LR
A_R2
A_R3
0Ω 5% 1/10W SMT0603 LR(NU)
A_AGND
A_C2
0.1uF 16V 80-20% SMT0402 Y5V LR
A_HPDET
A_CN4
NOTE
HP_L,HP_R請包AGROUND
A_HP_L
A_HP_R
A_L7
A_L6
600Ω±25% 100MHz 1000mA SMT0603 HCB1608KF-601T10 TAI-TECH LR
A_SPDIFO_AUD
A_SPDIF_PWR
A_L4
A_L1
CN SINGATRON SMT 2SJ-A373-001 LR
20-24459-90
L-20-24459-90
A_C5
1000pF 25V +80-20% SMT0603 Y5V LR
A_C53
SPWR 0.5% 1/16W 0402
0.1uF 16V 80-20% SMT0402 Y5V LR
2005.10.12
A_R7
SPDIF &
HEADPHONE
JACK
A_AGND
*2/21 GND change
AGND
A_CN5
A_SPDIF_PWR
A_SPDIFO_AUD
A_HPDET
A_MIC1_JD
A_HP_L
A_HP_R
A_INTERNAL_MIC
A_MIC1IN
A_MIC2IN
CN 15PIN 88283-15001 ACES LR.Normal
20-25008-10
L-20-25008-10
A_R4
SPWR 0 5% 1/16W 0603
A_AGND
A_R6
SPWR 0 5% 1/8W 0805
A_R5
0Ω 5% 1/8W SMT0805 LR(NU)
A_AGND
A_M1
A_M2
A_M3
SCREW-P8_0D2_8
SCREW-P8_0D2_8
SCREW-P8_0D2_8
A_FMK5
FMASK
A_FMK2
FMASK
A_FMK3
FMASK
A_FMK1
FMASK
A_FMK6
FMASK
A_FMK4
FMASK
First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
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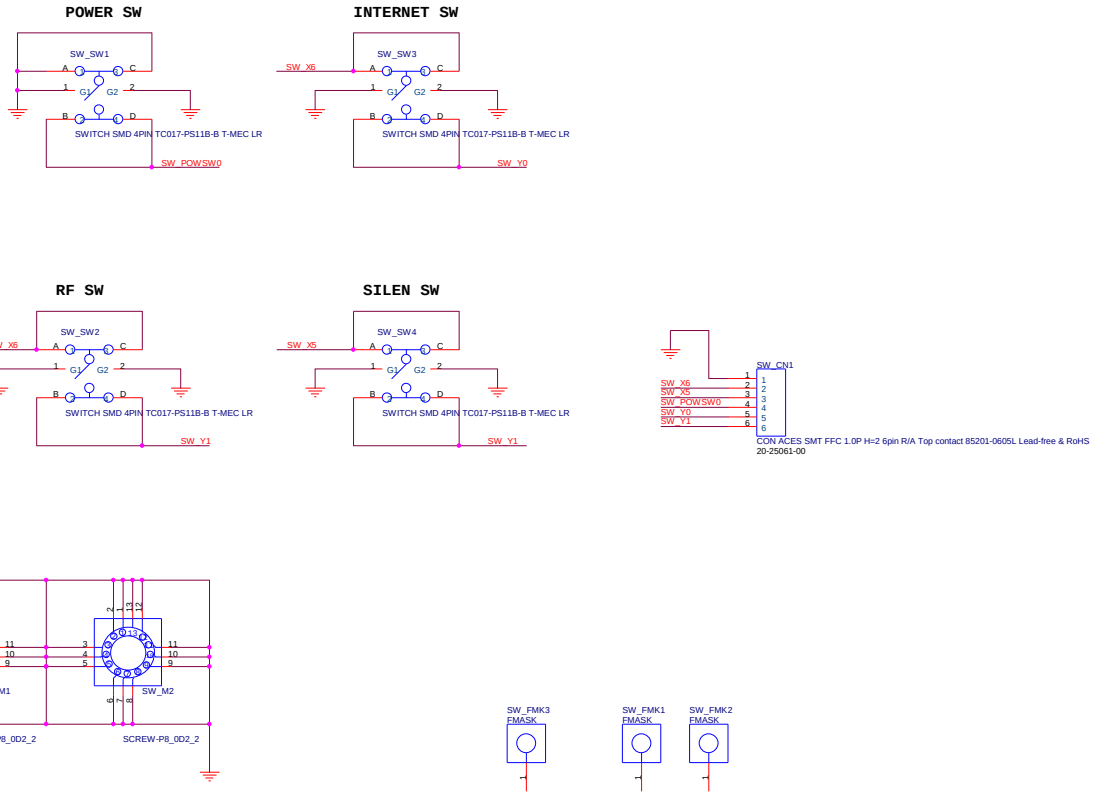

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