Shark Bay Platform

PCB Version	-1
Project name	General-SFF
Project Code	91.3KZ01.001
PCB Number	12127
PCB Size	244mmX 200mm, t=1.6mm, 4-layers
PCB P/N	48.3KZ06.011
SCH Ver	A00

On Board Header and Jump setting

CONN	Default	DESCRIPTION
MECLR1	1-X	FOR AUD_LINK_SDO_R ENABLE AND FLASH
CMCLR1	1-3	Reset CMOS data (Debug Only)
PWCLR1	1-3	PASSWORD CLEAR
USBF3		2X10 pin USB3.0 header
USBF1		2X5 pin USB2.0 header
AUDF1		2X5 Front Panel Audio header
FNCPU1		1X4 pin CPU FAN
ATX1		2X12 ATX POWER CONN
XDPC1		60 pin XDP connector for CPU
LPC1		2X7 LPC debug port header (Debug Only)
LEDH1		2X6 Front Panel Header
USBF2		2X5 pin USB2.0 header
ATX12V		2X2 ATX12V POWER CONN

Board ID

[4..1]	Description
1110	

Major IC version/part number/vender

FUNCTION	Description	Version	WST P/N	Vendor
PCH		C1		INTEL
Realtek Lan	IC LAN RTL8151GD-CG QFN 32P(DELL)		71.08151.M06	REALTEK
SIO	IC SUPER IO IT8772E/EX LQFP 64P		71.08772.B0G	ITE
Audio Codec	IC AUDIO CODEC ALC3600-CG LQFP 48P		71.03600.00G	REALTEK

Index

BOM Configuration
Unmount:(R)

<Variant Name>

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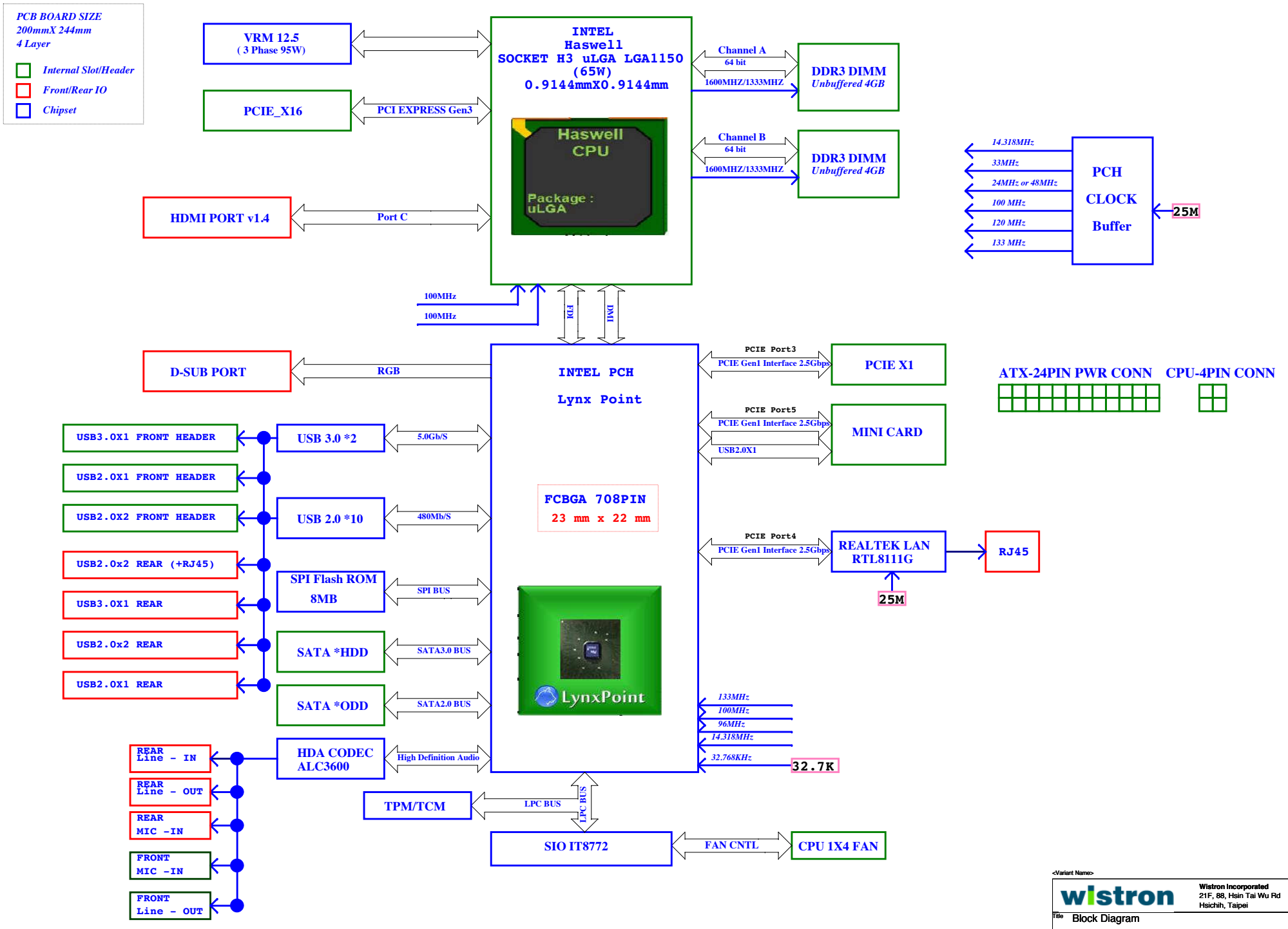
Title: Cover Page

Size: C | Document Number: ROSA General-SFF | Rev: -1A

Date: Monday, September 09, 2013 | Sheet 1 of 51



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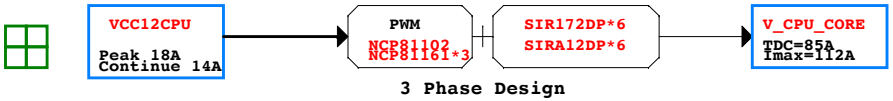
Title: Block Diagram

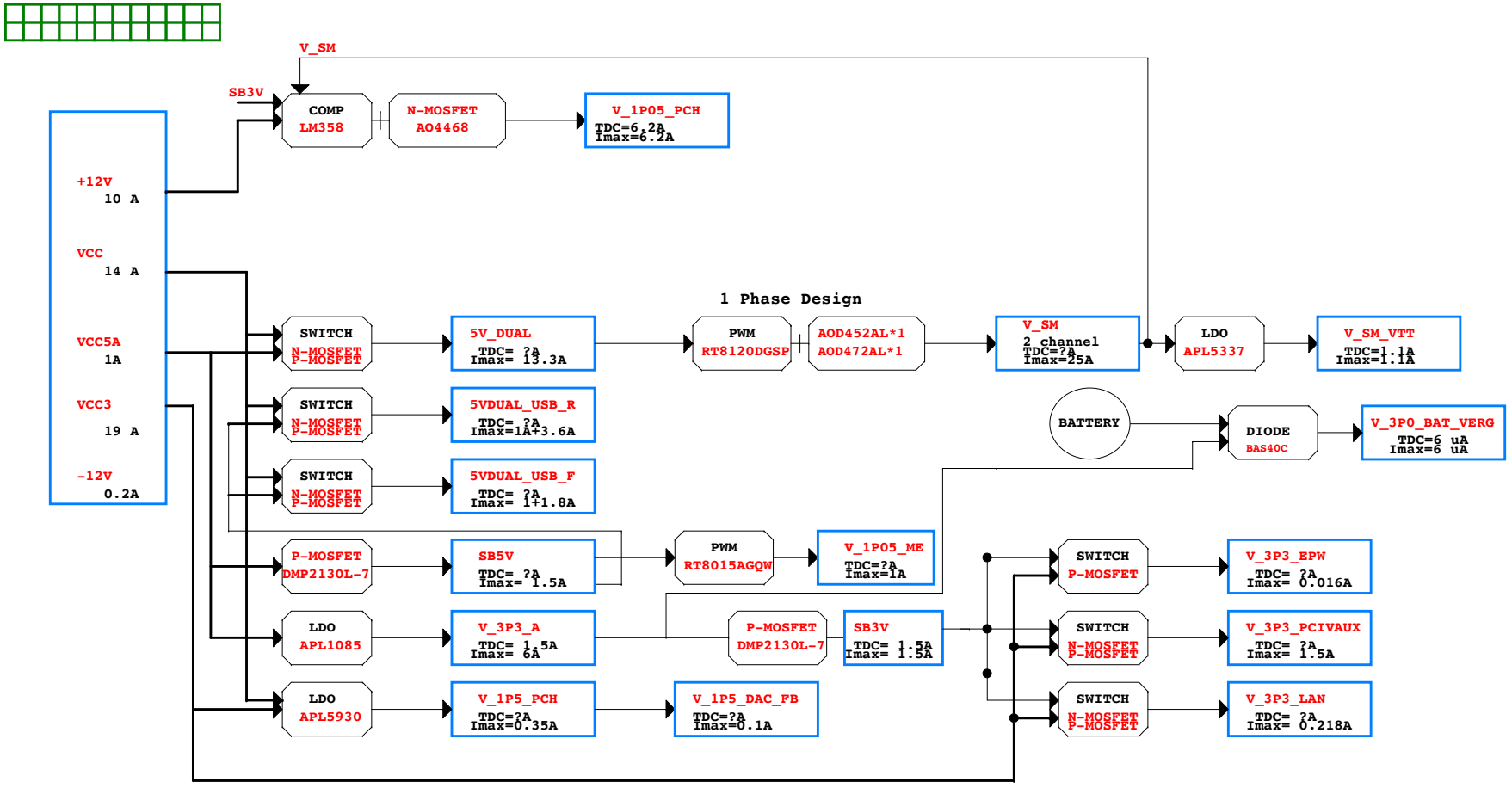
Size	Document Number	Rev
C	ROSA General-SFF	-1A

Date: Thursday, August 15, 2013 Sheet 2 of 51

CPU 2X2 POWER CONN



ATX 2X12 POWER CONN



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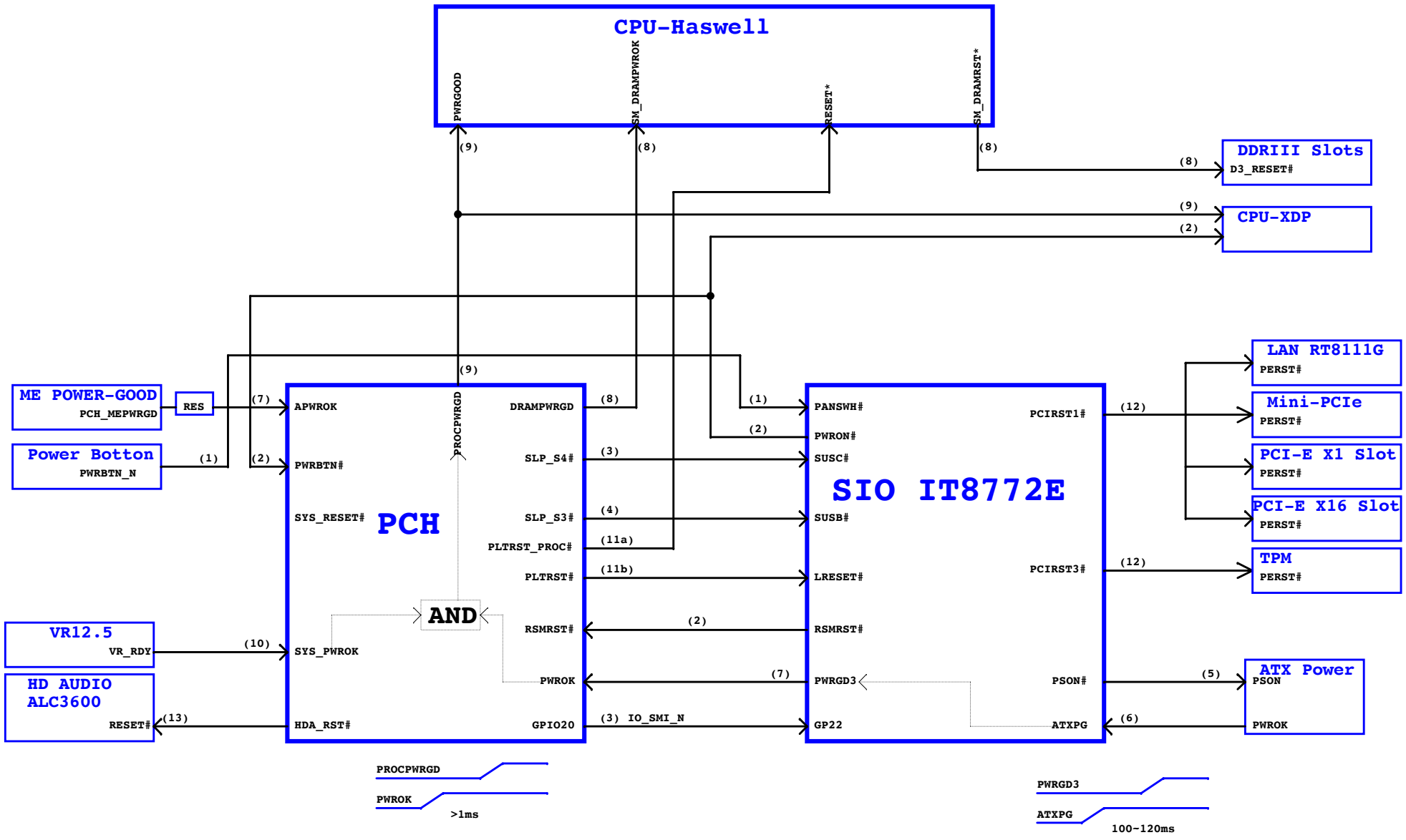
Title: Power Delivery

Size	Document Number	Rev
C	ROSA General-SFF	-1A

Date: Thursday, August 15, 2013 Sheet 3 of 51

RESET / Power Good MAP



<Variant Name>

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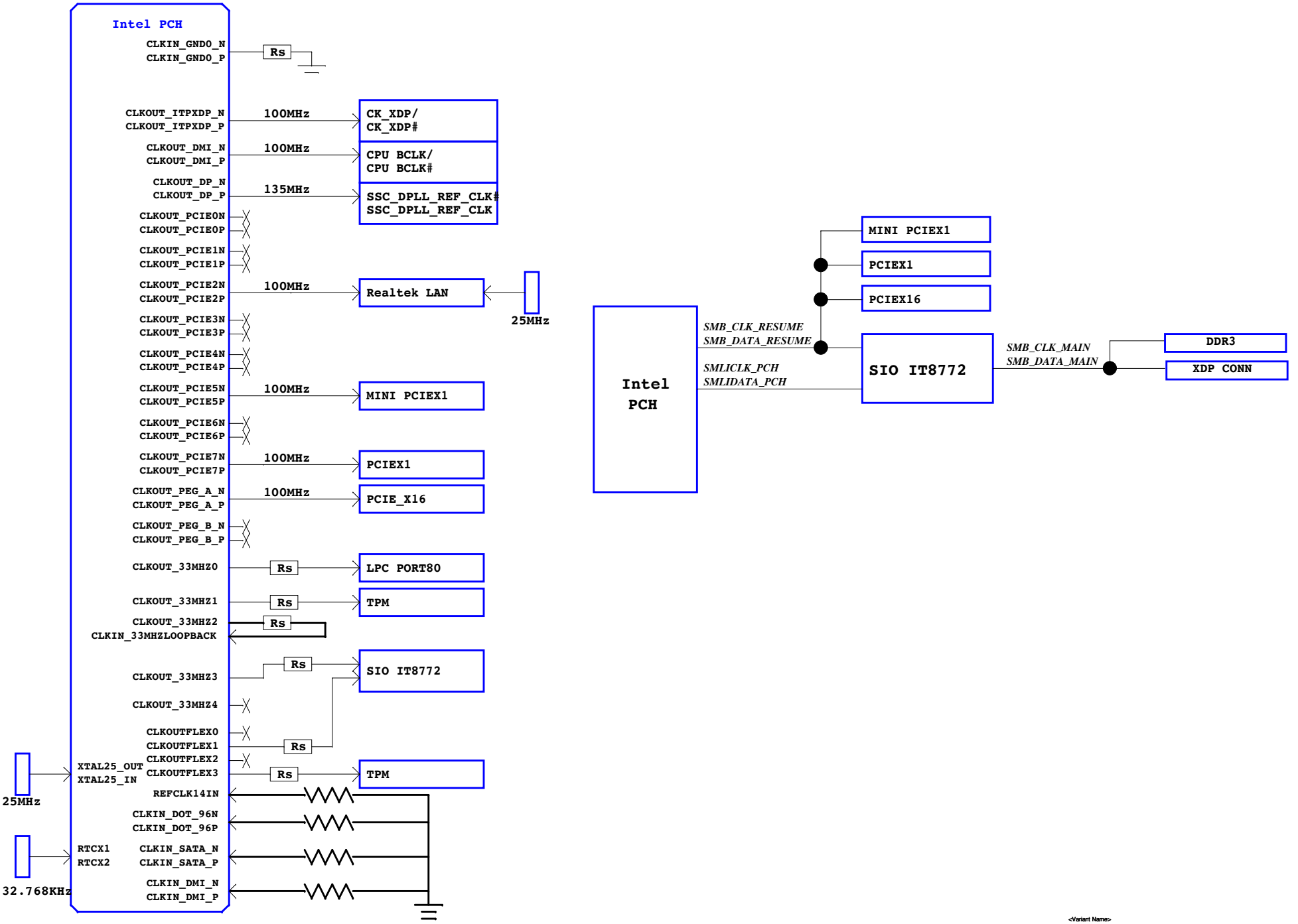
Title: RESET / Power Good MAP

Size	Document Number	Rev
C	ROSA General-SFF	-1A

Date: Thursday, August 15, 2013 Sheet 4 of 51



Note: .... is Reserve

Note: Rs is series resister

<Variant Name>

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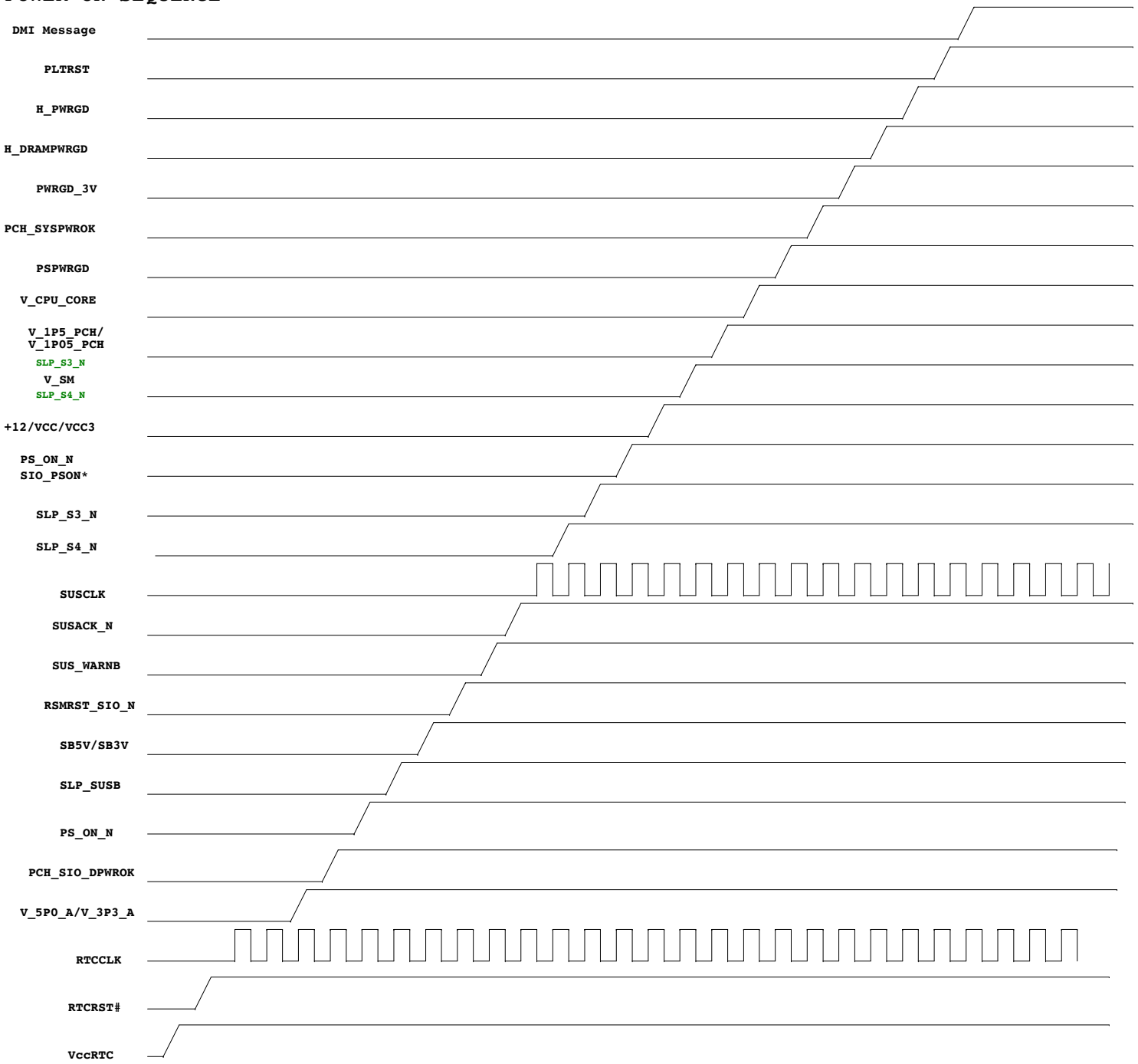
Title: Clock Diagram

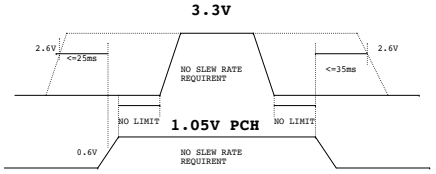
Size: C | Document Number: ROSA General-SFF | Rev: -1A

Date: Thursday, August 15, 2013 | Sheet 5 of 51

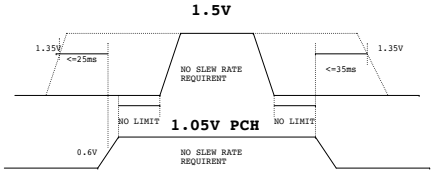
POWER ON SEQUENCE



Sequencing Requirements between PCH VCC3_3 and VCC Core Rail



Sequencing Requirements between PCH VCC3_3 and VCC Core Rail



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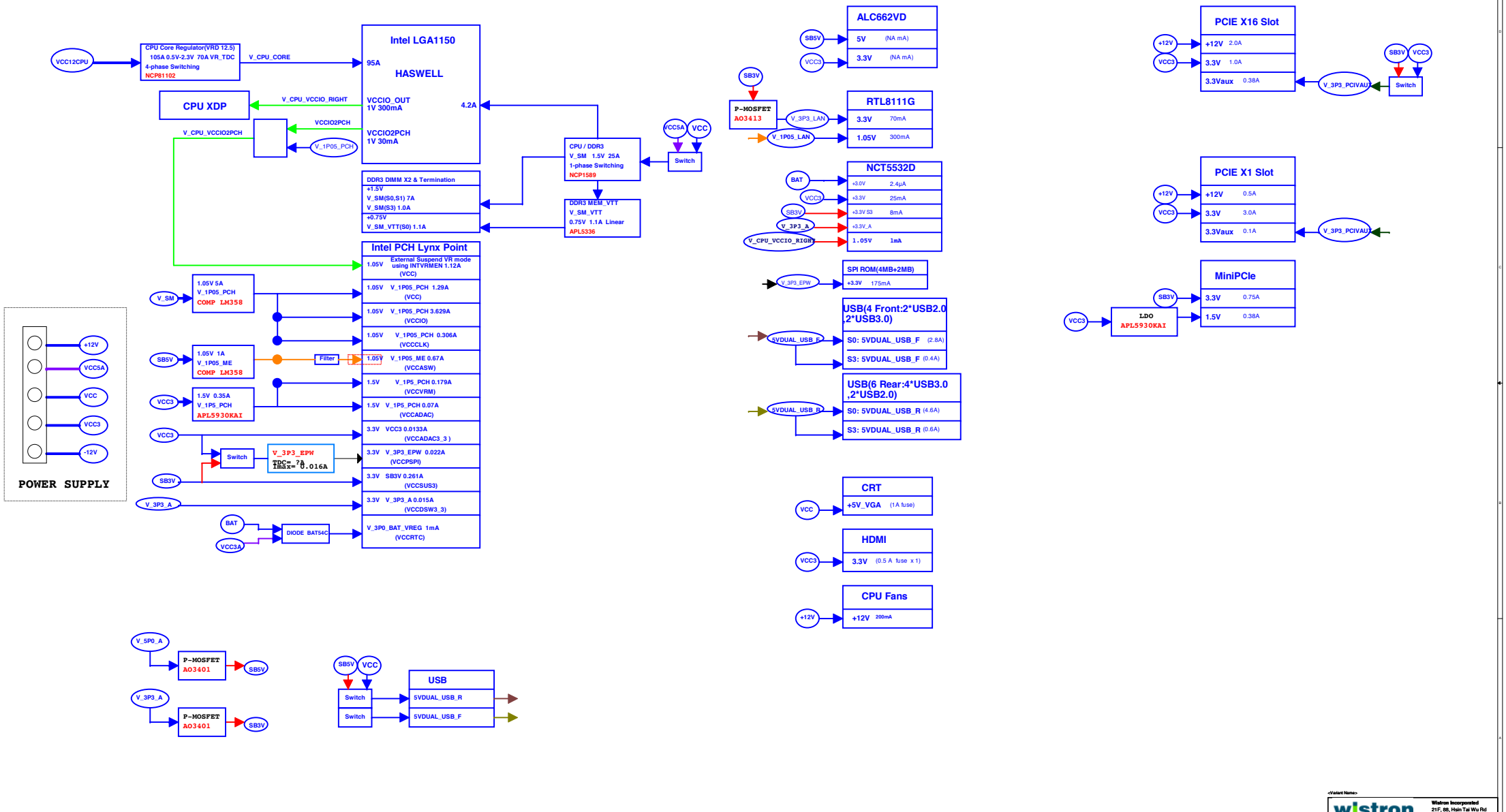
Title: Power Sequence

Size	Document Number	Rev
C	ROSA General-SFF	-1A

Date: Thursday, August 15, 2013 Sheet 6 of 51



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Title: Power Map

Size	Document Number	Rev
D	ROSA General-SFF	-1A

Date: Thursday, August 15, 2013 Sheet 7 of 51

TBD

<Variant Name>

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Title

Size	Document Number	Rev
A	ROSA General-SFF	-1A

Date: Thursday, August 15, 2013 Sheet 8 of 51

TBD

<Variant Name>

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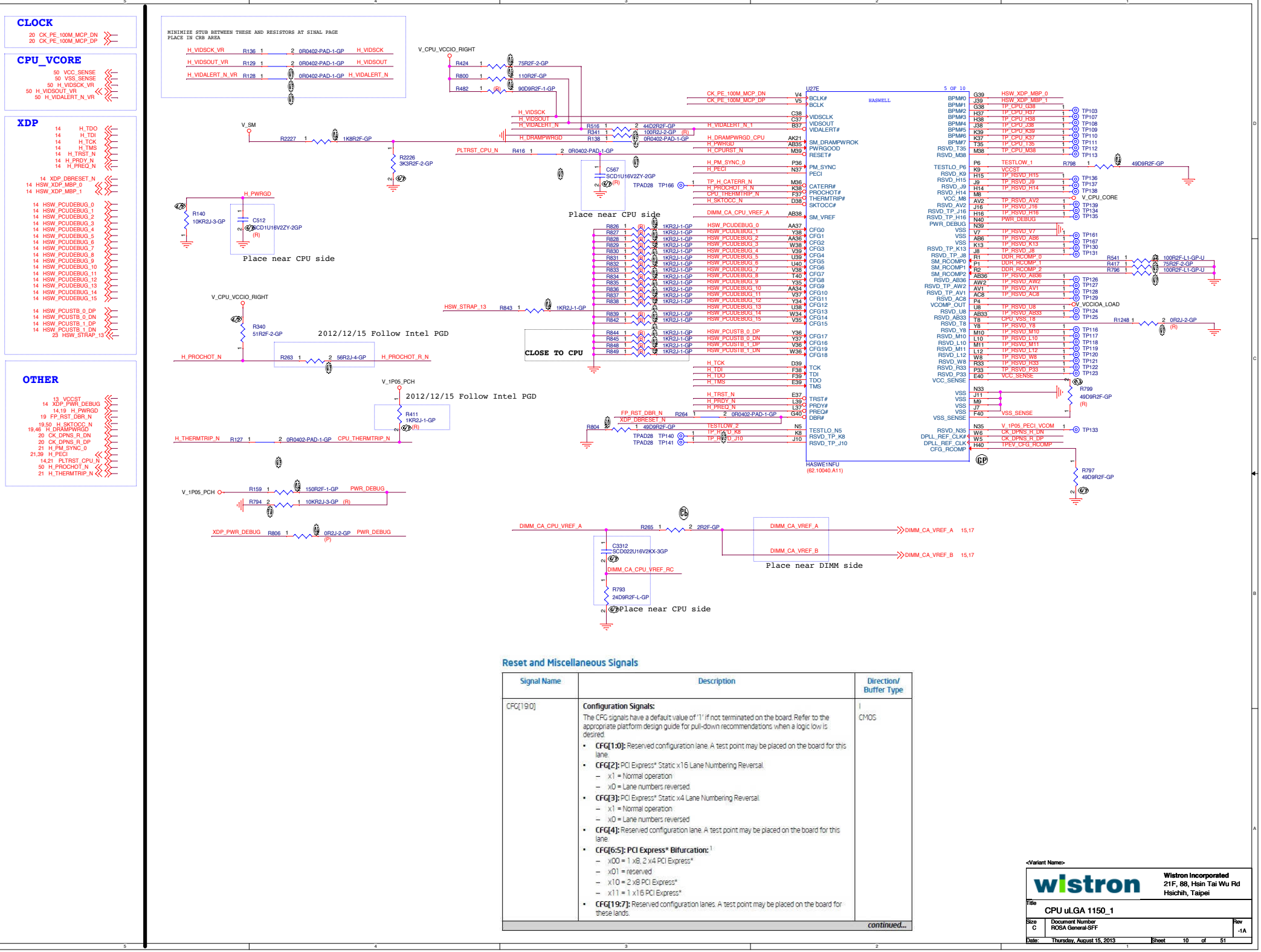
Title	TBD	
Size: A	Document Number: ROSA General-SFF	Rev: -1A
Date: Thursday, August 15, 2013	Sheet 9 of 51	



Reset and Miscellaneous Signals

Signal Name	Description	Direction/ Buffer Type
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. • **CFG[1:0]:** Reserved configuration lane. A test point may be placed on the board for this lane. • **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal. – x1 = Normal operation – x0 = Lane numbers reversed • **CFG[3]:** PCI Express* Static x4 Lane Numbering Reversal. – x1 = Normal operation – x0 = Lane numbers reversed • **CFG[4]:** Reserved configuration lane. A test point may be placed on the board for this lane. • **CFG[6:5]: PCI Express* Bifurcation:** [1] – x00 = 1 x8, 2 x4 PCI Express* – x01 = reserved – x10 = 2 x8 PCI Express* – x11 = 1 x16 PCI Express* • **CFG[19:7]:** Reserved configuration lanes. A test point may be placed on the board for these lands.	I CMOS

continued...

<Variant Name>

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Title: CPU uLGA 1150_1

Size	Document Number	Rev
C	ROSA General-SFF	-1A

Date: Thursday, August 15, 2013 Sheet 10 of 51

PCIEX16

26 EXP_A_TX_DP[0..15]
26 EXP_A_TX_DN[0..15]
26 EXP_A_RX_DP[0..15]
26 EXP_A_RX_DN[0..15]

DMI

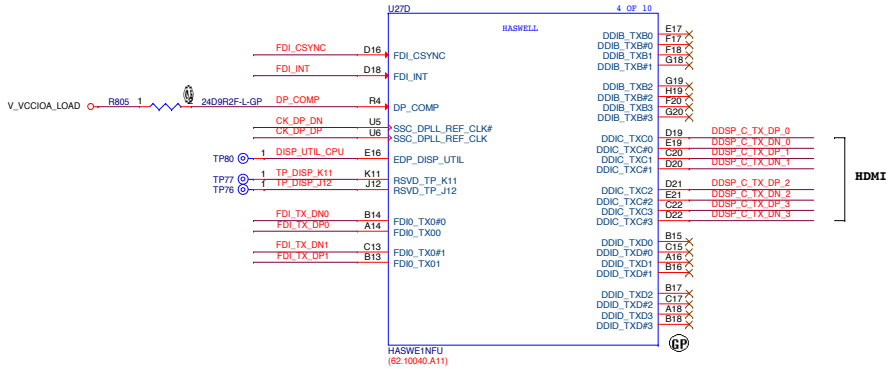
22 DMI_IT_MR_DP[0..3]
22 DMI_IT_MR_DN[0..3]
22 DMI_MT_IR_DP[0..3]
22 DMI_MT_IR_DN[0..3]

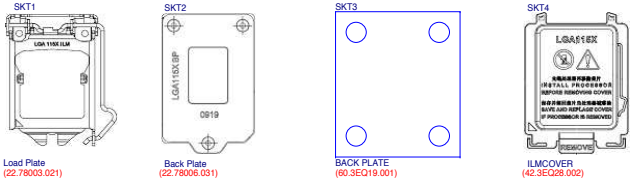
FDI

22 FDI_CSYNC
22 FDI_INT
22 FDI_TX_DN[0..1]
22 FDI_TX_DP[0..1]
20 CK_DP_DP
20 CK_DP_DN

HDMI

28 DDSP_C_TX_DP_0
28 DDSP_C_TX_DN_0
28 DDSP_C_TX_DP_1
28 DDSP_C_TX_DN_1
28 DDSP_C_TX_DP_2
28 DDSP_C_TX_DN_2
28 DDSP_C_TX_DP_3
28 DDSP_C_TX_DN_3





<Variant Name>

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Title: CPU uLGA 1150_2

Size	Document Number	Rev
C	ROSA General-SFF	-1A

Date: Thursday, August 15, 2013 Sheet 11 of 51

DDR DATA

15 M_DATA_A[0..63]
17 M_DATA_B[0..63]

15 M_DQS_A_DP[0..7]
15 M_DQS_A_DN[0..7]

17 M_DQS_B_DP[0..7]
17 M_DQS_B_DN[0..7]

DDR CMD/ADD

15 M_MAA_A[0..15]
17 M_MAA_B[0..15]

15 M_WE_A_N
15 M_CAS_A_N
15 M_RAS_A_N
15 M_SBS_A0
15 M_SBS_A1
15 M_SBS_A2

17 M_WE_B_N
17 M_CAS_B_N
17 M_RAS_B_N
17 M_SBS_B0
17 M_SBS_B1
17 M_SBS_B2

DDR CTRL

15 M_SCS_A_N0
15 M_SCS_A_N1

15 M_SCKE_A0
15 M_SCKE_A1

15 M_ODT_A0
15 M_ODT_A1

17 M_SCS_B_N0
17 M_SCS_B_N1

17 M_SCKE_B0
17 M_SCKE_B1

17 M_ODT_B0
17 M_ODT_B1

DDR CLOCK

15 CK_M_DDR0_A_DP
15 CK_M_DDR0_A_DN
15 CK_M_DDR1_A_DP
15 CK_M_DDR1_A_DN

17 CK_M_DDR0_B_DP
17 CK_M_DDR0_B_DN
17 CK_M_DDR1_B_DN
17 CK_M_DDR1_B_DN

DDR OTHERS

15,17 DDR3_DRAMRST_N

17 DIMM_DQ_CPU_VREF_B
15 DIMM_DQ_CPU_VREF_A

Other

14,19,21,39 PWRGD_3V

U27A — 1 OF 10 — HASWELL

M_DATA_A0	AD38	SA_DQ0	SA_MA0	AU13	M_MAA_A0
M_DATA_A1	AD39	SA_DQ1	SA_MA1	AV16	M_MAA_A1
M_DATA_A2	AF38	SA_DQ2	SA_MA2	AU16	M_MAA_A2
M_DATA_A3	AF39	SA_DQ3	SA_MA3	AW17	M_MAA_A3
M_DATA_A4	AD37	SA_DQ4	SA_MA4	AU17	M_MAA_A4
M_DATA_A5	AD40	SA_DQ5	SA_MA5	AW18	M_MAA_A5
M_DATA_A6	AF37	SA_DQ6	SA_MA6	AV17	M_MAA_A6
M_DATA_A7	AF40	SA_DQ7	SA_MA7	AT18	M_MAA_A7
M_DATA_A8	AH40	SA_DQ8	SA_MA8	AU18	M_MAA_A8
M_DATA_A9	AH39	SA_DQ9	SA_MA9	AT19	M_MAA_A9
M_DATA_A10	AK38	SA_DQ10	SA_MA10	AW11	M_MAA_A10
M_DATA_A11	AK39	SA_DQ11	SA_MA11	AV19	M_MAA_A11
M_DATA_A12	AH37	SA_DQ12	SA_MA12	AU19	M_MAA_A12
M_DATA_A13	AH38	SA_DQ13	SA_MA13	AY10	M_MAA_A13
M_DATA_A14	AK37	SA_DQ14	SA_MA14	AT20	M_MAA_A14
M_DATA_A15	AK40	SA_DQ15	SA_MA15	AU21	M_MAA_A15
M_DATA_A16	AM40	SA_DQ16			
M_DATA_A17	AM39	SA_DQ17	SA_ODT0	AW10	M_ODT_A0
M_DATA_A18	AP38	SA_DQ18	SA_ODT1	AY8	M_ODT_A1
M_DATA_A19	AP39	SA_DQ19	SA_ODT2	AW9	
M_DATA_A20	AM37	SA_DQ20	SA_ODT3	AU8	
M_DATA_A21	AM38	SA_DQ21			
M_DATA_A22	AP37	SA_DQ22			
M_DATA_A23	AP40	SA_DQ23	SA_ECC_CB0	AW33	
M_DATA_A25	AV37	SA_DQ24	SA_ECC_CB1	AV33	
M_DATA_A29	AW37	SA_DQ25	SA_ECC_CB2	AU31	
M_DATA_A26	AU35	SA_DQ26	SA_ECC_CB3	AV31	
M_DATA_A27	AV35	SA_DQ27	SA_ECC_CB4	AT33	
M_DATA_A28	AT37	SA_DQ28	SA_ECC_CB5	AU33	
M_DATA_A24	AU37	SA_DQ29	SA_ECC_CB6	AT31	
M_DATA_A30	AT35	SA_DQ30	SA_ECC_CB7	AW31	
M_DATA_A31	AW35	SA_DQ31			
M_DATA_A33	AY6	SA_DQ32	SA_BS0	AV12	M_SBS_A0
M_DATA_A37	AU6	SA_DQ33	SA_BS1	AY11	M_SBS_A1
M_DATA_A34	AV4	SA_DQ34	SA_BS2	AT21	M_SBS_A2
M_DATA_A35	AU4	SA_DQ35			
M_DATA_A36	AW6	SA_DQ36	SA_CKE0	AV22	M_SCKE_A0
M_DATA_A32	AV6	SA_DQ37	SA_CKE1	AT23	M_SCKE_A1
M_DATA_A38	AW4	SA_DQ38	SA_CKE2	AU22	
M_DATA_A39	AY4	SA_DQ39	SA_CKE3	AU23	
M_DATA_A41	AR1	SA_DQ40			
M_DATA_A45	AR4	SA_DQ41	SA_CS#0	AU14	M_SCS_A_N0
M_DATA_A42	AN3	SA_DQ42	SA_CS#1	AV9	M_SCS_A_N1
M_DATA_A43	AN4	SA_DQ43	SA_CS#2	AU10	
M_DATA_A44	AR2	SA_DQ44	SA_CS#3	AW8	
M_DATA_A40	AR3	SA_DQ45			
M_DATA_A46	AN2	SA_DQ46	SA_CK0	AY15	CK_M_DDR0_A_DP
M_DATA_A47	AN1	SA_DQ47	SA_CK#0	AY16	CK_M_DDR0_A_DN
M_DATA_A49	AL1	SA_DQ48	SA_CK1	AW15	CK_M_DDR1_A_DP
M_DATA_A53	AL4	SA_DQ49	SA_CK#1	AV15	CK_M_DDR1_A_DN
M_DATA_A50	AJ3	SA_DQ50	SA_CK2	AV14	
M_DATA_A51	AJ4	SA_DQ51	SA_CK#2	AW16	
M_DATA_A52	AJ2	SA_DQ52	SA_CK3	AW13	
M_DATA_A48	AL3	SA_DQ53	SA_CK#3	AY13	
M_DATA_A54	AJ2	SA_DQ54			
M_DATA_A55	AJ1	SA_DQ55	RSVD_AW12	AW12	TP_RSVD_AW12 1 TP34
M_DATA_A57	AG1	SA_DQ56			
M_DATA_A61	AG4	SA_DQ57			
M_DATA_A58	AE3	SA_DQ58			
M_DATA_A59	AE4	SA_DQ59			
M_DATA_A60	AG2	SA_DQ60			
M_DATA_A56	AG3	SA_DQ61			
M_DATA_A62	AE2	SA_DQ62			
M_DATA_A63	AE1	SA_DQ63			
M_DQS_A_DP0	AE39	SA_DQS0			
M_DQS_A_DP1	AJ39	SA_DQS1			
M_DQS_A_DP2	AN39	SA_DQS2			
M_DQS_A_DP3	AV36	SA_DQS3			
M_DQS_A_DP4	AV5	SA_DQS4			
M_DQS_A_DP5	AP3	SA_DQS5			
M_DQS_A_DP6	AK3	SA_DQS6			
M_DQS_A_DP7	AF3	SA_DQS7			
	AV32	SA_DQS8			
M_DQS_A_DN0	AE38	SA_DQS#0			
M_DQS_A_DN1	AJ38	SA_DQS#1			
M_DQS_A_DN2	AN38	SA_DQS#2			
M_DQS_A_DN3	AU36	SA_DQS#3			
M_DQS_A_DN4	AW5	SA_DQS#4			
M_DQS_A_DN5	AP2	SA_DQS#5			
M_DQS_A_DN6	AK2	SA_DQS#6			
M_DQS_A_DN7	AF2	SA_DQS#7			
	AU32	SA_DQS#8			
			SA_RAS#	AU12	M_RAS_A_N
			SA_WE#	AU11	M_WE_A_N
			RSVD_AV20	AV20	TP_RSVD_AV20 1 TP32
			RSVD_AW27	AW27	TP_RSVD_AW27 1 TP33
			SA_CAS#	AU9	M_CAS_A_N
			SM_DRAMRST#	AK22	DDR3_DRAMRST_N

HASWE1NFU (62.10040.A11)

C520 SCD1U10V2KX-4GP (R)

U27B — 2 OF 10 — HASWELL

M_DATA_B0	AE34	SB_DQ0	SB_MA0	AL19	M_MAA_B0
M_DATA_B1	AE35	SB_DQ1	SB_MA1	AK23	M_MAA_B1
M_DATA_B2	AG35	SB_DQ2	SB_MA2	AM22	M_MAA_B2
M_DATA_B3	AH35	SB_DQ3	SB_MA3	AM23	M_MAA_B3
M_DATA_B4	AD34	SB_DQ4	SB_MA4	AP23	M_MAA_B4
M_DATA_B5	AD35	SB_DQ5	SB_MA5	AL23	M_MAA_B5
M_DATA_B6	AG34	SB_DQ6	SB_MA6	AY24	M_MAA_B6
M_DATA_B7	AH34	SB_DQ7	SB_MA7	AV25	M_MAA_B7
M_DATA_B8	AL34	SB_DQ8	SB_MA8	AU26	M_MAA_B8
M_DATA_B9	AL35	SB_DQ9	SB_MA9	AW25	M_MAA_B9
M_DATA_B10	AK31	SB_DQ10	SB_MA10	AP18	M_MAA_B10
M_DATA_B11	AL31	SB_DQ11	SB_MA11	AY25	M_MAA_B11
M_DATA_B12	AK34	SB_DQ12	SB_MA12	AV26	M_MAA_B12
M_DATA_B13	AK35	SB_DQ13	SB_MA13	AP15	M_MAA_B13
M_DATA_B14	AK32	SB_DQ14	SB_MA14	AV27	M_MAA_B14
M_DATA_B15	AL32	SB_DQ15	SB_MA15	AY28	M_MAA_B15
M_DATA_B17	AN34	SB_DQ16			
M_DATA_B21	AP34	SB_DQ17	SB_ODT0	AM17	M_ODT_B0
M_DATA_B19	AN31	SB_DQ18	SB_ODT1	AL16	M_ODT_B1
M_DATA_B23	AP31	SB_DQ19	SB_ODT2	AM16	
M_DATA_B20	AN35	SB_DQ20	SB_ODT3	AK15	
M_DATA_B16	AP35	SB_DQ21			
M_DATA_B18	AN32	SB_DQ22	SB_ECC_CB0	AM26	
M_DATA_B22	AP32	SB_DQ23	SB_ECC_CB1	AM25	
M_DATA_B25	AM29	SB_DQ24	SB_ECC_CB2	AP25	
M_DATA_B28	AM28	SB_DQ25	SB_ECC_CB3	AP26	
M_DATA_B27	AR29	SB_DQ26	SB_ECC_CB4	AL26	
M_DATA_B30	AR28	SB_DQ27	SB_ECC_CB5	AL25	
M_DATA_B24	AL29	SB_DQ28	SB_ECC_CB6	AP24	
M_DATA_B29	AL28	SB_DQ29	SB_ECC_CB7	AR24	
M_DATA_B26	AP29	SB_DQ30			
M_DATA_B31	AP28	SB_DQ31	SB_BS0	AK17	M_SBS_B0
M_DATA_B32	AR12	SB_DQ32	SB_BS1	AL18	M_SBS_B1
M_DATA_B33	AP12	SB_DQ33	SB_BS2	AW28	M_SBS_B2
M_DATA_B34	AL13	SB_DQ34			
M_DATA_B35	AL12	SB_DQ35	SB_CKE0	AW29	M_SCKE_B0
M_DATA_B36	AP13	SB_DQ36	SB_CKE1	AY29	M_SCKE_B1
M_DATA_B37	AP13	SB_DQ37	SB_CKE2	AU28	
M_DATA_B38	AM13	SB_DQ38	SB_CKE3	AU29	
M_DATA_B39	AM12	SB_DQ39			
M_DATA_B45	AP9	SB_DQ40			
M_DATA_B41	AP9	SB_DQ41			
M_DATA_B47	AR6	SB_DQ42			
M_DATA_B43	AP6	SB_DQ43			
M_DATA_B44	AR10	SB_DQ44	SB_CS#0	AP17	M_SCS_B_N0
M_DATA_B40	AP10	SB_DQ45	SB_CS#1	AN15	M_SCS_B_N1
M_DATA_B46	AR7	SB_DQ46	SB_CS#2	AN17	
M_DATA_B42	AP7	SB_DQ47	SB_CS#3	AL15	
M_DATA_B52	AM9	SB_DQ48			
M_DATA_B53	AL9	SB_DQ49	SB_CK0	AM20	CK_M_DDR0_B_DP
M_DATA_B50	AL6	SB_DQ50	SB_CK#0	AM21	CK_M_DDR0_B_DN
M_DATA_B55	AL7	SB_DQ51	SB_CK1	AP22	CK_M_DDR1_B_DP
M_DATA_B48	AM10	SB_DQ52	SB_CK#1	AP21	CK_M_DDR1_B_DN
M_DATA_B49	AL10	SB_DQ53			
M_DATA_B54	AM6	SB_DQ54	SB_CK2	AN20	
M_DATA_B51	AM7	SB_DQ55	SB_CK#2	AN21	
M_DATA_B61	AH6	SB_DQ56	SB_CK3	AP19	
M_DATA_B60	AH7	SB_DQ57	SB_CK#3	AP20	
M_DATA_B59	AE6	SB_DQ58			
M_DATA_B63	AE7	SB_DQ59	SB_CAS#	AP16	M_CAS_B_N
M_DATA_B56	AJ6	SB_DQ60	RSVD_AL20	AL20	
M_DATA_B57	AJ7	SB_DQ61	SB_RAS#	AM18	M_RAS_B_N
M_DATA_B58	AF6	SB_DQ62	SB_WE#	AK16	M_WE_B_N
M_DATA_B62	AF7	SB_DQ63			
M_DATA_B_DP0	AF35	SB_DQS0	SA_DIMM_VREFDQ	AB39	DIMM_DQ_CPU_VREF_A
M_DATA_B_DP1	AL33	SB_DQS1	SB_DIMM_VREFDQ	AB40	DIMM_DQ_CPU_VREF_B
M_DATA_B_DP2	AP33	SB_DQS2			
M_DATA_B_DP3	AN28	SB_DQS3			
M_DATA_B_DP4	AN12	SB_DQS4			
M_DATA_B_DP5	AP8	SB_DQS5			
M_DATA_B_DP6	AL8	SB_DQS6			
M_DATA_B_DP7	AG7	SB_DQS7			
	AN25	SB_DQS8			
M_DQS_B_DN0	AF34	SB_DQS#0			
M_DQS_B_DN1	AK33	SB_DQS#1			
M_DQS_B_DN2	AN33	SB_DQS#2			
M_DQS_B_DN3	AN29	SB_DQS#3			
M_DQS_B_DN4	AN13	SB_DQS#4			
M_DQS_B_DN5	AR8	SB_DQS#5			
M_DQS_B_DN6	AM8	SB_DQS#6			
M_DQS_B_DN7	AG6	SB_DQS#7			
	AN26	SB_DQS#8			

HASWE1NFU (62.10040.A11)

U27H — 8 OF 10 — HASWELL

PWRGD_3V

R2230 6K04R2F-GP (R)
R2231 2K67R2F-2-GP (R)

TP148	TP_RSVD_AY18	AY18	RSVD_AY18
TP149	TP_RSVD_AW24	AW24	RSVD_AW24
TP150	TP_RSVD_AW23	AW23	RSVD_AW23
TP151	TP_RSVD_AV29	AV29	RSVD_AV29
TP152	TP_RSVD_AV24	AV24	RSVD_AV24
TP153	TP_RSVD_AU39	AU39	RSVD_AU39
TP154	TP_RSVD_AU27	AU27	RSVD_AU27
TP155	TP_RSVD_AU1	AU1	RSVD_AU1
TP164	TP_RSVD_AT40	AT40	RSVD_AT40
TP160	TP_RSVD_AK20	AK20	RSVD_AK20
	VCCST_PWRGD	Y7	RSVD_Y7
TP162	TP_RSVD_T34	T34	RSVD_T34
TP163	TP_RSVD_R34	R34	RSVD_R34
TP156	TP_RSVD_J40	J40	RSVD_J40
TP157	TP_RSVD_J17	J17	RSVD_J17
TP158	TP_RSVD_J15	J15	RSVD_J15
TP159	TP_RSVD_H12	H12	RSVD_H12

RSVD_TP_K12	K12	TP_RSVD_K12	TP142
RSVD_TP_J13	J13	TP_RSVD_J13	TP143
RSVD_TP_P37	P37	TP_RSVD_P37	TP144
RSVD_TP_N38	N38	TP_RSVD_N38	TP145
RSVD_TP_R36	R36	TP_RSVD_R36	TP146
RSVD_TP_C39	C39	TP_RSVD_C39	TP147
VSS	U35		
VSS	P40		
VSS	R38		
VSS	T37		
VSS	V34		
VSS	R39		
VSS	T38		
VSS	U36		
VSS	P39		
VSS	T36		
VSS	R37		
VSS	J14		
RSVD_TP_N36	N36	TP_CPU_N36	TP165

HASWE1NFU (62.10040.A11)

<Variant Name>

wistron

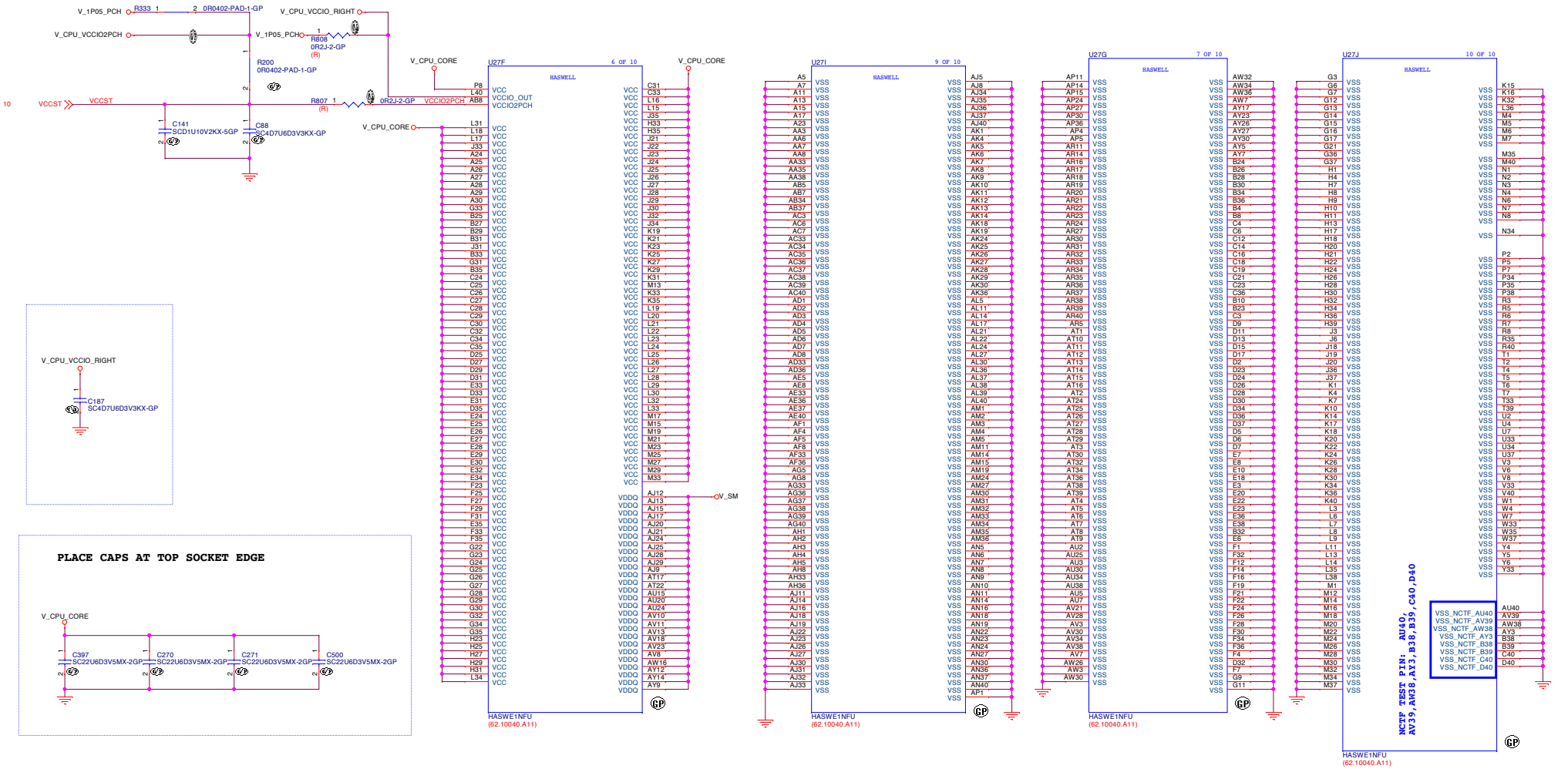
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU uLGA 1150_3

Size	Document Number	Rev
C	ROSA General-SFF	-1A

Date: Thursday, August 15, 2013 Sheet 12 of 51

Put R333 near PCH side for V_CPU_VCCIO2PCH is for PCH power



DEFENSIVE DESIGN PWR_DEBUG

2012/12/04 Ryan removed,

CPU Power Capacitor Quantity

Net	CAP	AMOUNT
Vcore	22uf 0805	22
V_SM	22uf 0805	4+5(R)

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU uLGA 1150_4

Size: C | Document Number: ROSA General-SFF | Rev: -1A

Date: Thursday, August 15, 2013 | Sheet 13 of 51

XDP for CPU

10 H_TDO
10 H_TDI
10 H_TMS
10 H_TCK
10 H_TRST_N
10 H_PREQ_N
10 H_PRDY_N
10 XDP_DBRESET_N
10,19 H_PWRGD

10 HSW_PCUDEBUG_0
10 HSW_PCUDEBUG_1
10 HSW_PCUDEBUG_2
10 HSW_PCUDEBUG_3
10 HSW_PCUDEBUG_4
10 HSW_PCUDEBUG_5
10 HSW_PCUDEBUG_6
10 HSW_PCUDEBUG_7
10 HSW_PCUDEBUG_8
10 HSW_PCUDEBUG_9
10 HSW_PCUDEBUG_10
10 HSW_PCUDEBUG_11
10 HSW_PCUDEBUG_12
10 HSW_PCUDEBUG_13
10 HSW_PCUDEBUG_14
10 HSW_PCUDEBUG_15

10 HSW_XDP_MBP_0
10 HSW_XDP_MBP_1

10 HSW_PCUSTB_0_DP
10 HSW_PCUSTB_0_DN
10 HSW_PCUSTB_1_DP
10 HSW_PCUSTB_1_DN

10 XDP_PWR_DEBUG

15,17,39 SMB_DATA_MAIN
15,17,39 SMB_CLK_MAIN

20 CK_100M_CPU_XDP_DN
20 CK_100M_CPU_XDP_DP

19,39 SW_ON_N

10,21 PLTRST_CPU_N

XDP for PCH

19 PCH_JTAG_RST_R
19 PCH_JTAG_TDO
19 PCH_JTAG_TDI
19 PCH_JTAG_TMS
19 PCH_JTAG_TCK

19,50 VR_READY
12,19,21,39 PWRGD_3V

LPC DEBUG PORT

19,39 L_AD0
19,39 L_AD1
19,39 L_AD2
19,39 L_AD3
19,39 L_FRAME_N
20 CK_P_33M_LPCP80
39 PCIRST3#

XDP for CPU

PLace Near XDP CONN
V_CPU_VCCIO_RIGHT
R640 1 (R) 51R2F-2-GP H_TDI
R639 1 (R) 51R2F-2-GP H_TMS
R663 1 (R) 51R2F-2-GP H_TCK
PLace Near CPU
H_TCK TERMINATION PLACE NEAR CPU WITHIN 1.1 INCH
R661 1 51R2F-2-GP H_TRST_N
PLace Any where

PLTRST_CPU_N R660 1 (R) 1KR2J-1-GP H_RSTOUT_XDP_N
VR_READY R819 1 2 0R0402-PAD-1-GP XDP_VR_READY

H_PWRGD R519 1 (R) 1KR2J-1-GP XDP_PWRGD
R518 1KR2F-3-GP (R)

SW_ON_N R637 1 2 0R0402-PAD-1-GP XDP_PLTRST_N

V_1P05_PCH VCC3
R2216 51R2F-2-GP
R2218 (R) 249R2F-GP H_TDO
R2217 (R) 825R2F-GP
R2219 (R) 100R2F-L1-GP-U
PLace Near XDP CONN

V_CPU_VCCIO_RIGHT XDPC1 MH1 V_CPU_VCCIO_RIGHT
H_PREQ_N HSW_PCUSTB_0_DP
H_PRDY_N HSW_PCUSTB_0_DN
HSW_PCUDEBUG_0 HSW_PCUDEBUG_8
HSW_PCUDEBUG_1 HSW_PCUDEBUG_9
HSW_PCUDEBUG_2 HSW_PCUDEBUG_10
HSW_PCUDEBUG_3 HSW_PCUDEBUG_11
HSW_XDP_MBP_0 HSW_PCUSTB_1_DP
HSW_XDP_MBP_1 HSW_PCUSTB_1_DN
HSW_PCUDEBUG_4 HSW_PCUDEBUG_12
HSW_PCUDEBUG_5 HSW_PCUDEBUG_13
HSW_PCUDEBUG_6 HSW_PCUDEBUG_14
HSW_PCUDEBUG_7 HSW_PCUDEBUG_15
XDP_PWRGD CK_XDP_S_DP
XDP_PLTRST_N CK_XDP_S_DN
XDP_PWR_DEBUG H_RSTOUT_XDP_N
XDP_VR_READY XDP_DBRESET_N
SMB_DATA_MAIN H_TDO
SMB_CLK_MAIN H_TRST_N
H_TCK H_TDI
H_TMS
PRIVACY_MSH_EN_N R867 1 (R) 1KR2J-1-GP HSW_PCUDEBUG_3
MH2
(R) SMC-CONN60A-GP

CK_100M_CPU_XDP_DN R820 1 0R0402-PAD-1-GP CK_XDP_S_DN
CK_100M_CPU_XDP_DP R821 1 2 0R0402-PAD-1-GP CK_XDP_S_DP

XDP_DBRESET_N
C576 SCD1U10V2KX-5GP (R)

LPC DEBUG PORT

VCC3
R638 4K7R2J-2-GP
CK_P_33M_LPCP80 LPC1 1 2 INIT_3V
PCIRST3# 3 4
L_AD0 5 6 FWH_ID0 VCC3
L_AD1 7 8 VCC
L_AD2 9 10
L_AD3 11 12
L_FRAME_N 13 14
JWT-CONN14A-S3-GP (R)
R662 10KR2J-3-GP (R)

Pin height 2.3mm

XDP for PCH

Place R817, R764, R766, R812 close to PCH
Place R811, R818 close to PCH XDP connector side

SB3V
R811 1 200R2F-L-GP PCH_JTAG_TDO
R817 1 200R2F-L-GP PCH_JTAG_TDI
R766 1 200R2F-L-GP PCH_JTAG_TMS

C575 2 1 SCD1U16V2ZY-2GP (R)
R816 2 1 51R2F-2-GP PCH_JTAG_TCK

R818 100R2F-L1-GP-U
R764 100R2F-L1-GP-U
R812 100R2F-L1-GP-U

PCH_JTAG_TDO 1 TP87 TPAD28
PCH_JTAG_TDI 1 TP105 TPAD28
PCH_JTAG_TMS 1 TP104 TPAD28

SB3V
PWRGD_3V R810 1 (R) 1KR2J-1-GP

SB3V
R765 20KR2F-L-GP
PCH_JTAG_RST_R
C1672 SC1U10V2KX-1GP (R)
R712 10KR2J-3-GP (R)

2012/12/15 delete reserve R815

<Variant Name>

wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: XDP/80 PORT HEADER/APS

Size	Document Number	Rev
C	ROSA General-SFF	-1A

Date: Thursday, August 15, 2013 Sheet 14 of 51

DDR DATA

12 M_DATA_A[0..63]
12 M_DQS_A_DP[0..7]
12 M_DQS_A_DN[0..7]

DDR CMD/ADD

12 M_MAA_A[0..15]

12 M_WE_A_N
12 M_CAS_A_N
12 M_RAS_A_N

12 M_SBS_A0
12 M_SBS_A1
12 M_SBS_A2

DDR CTRL

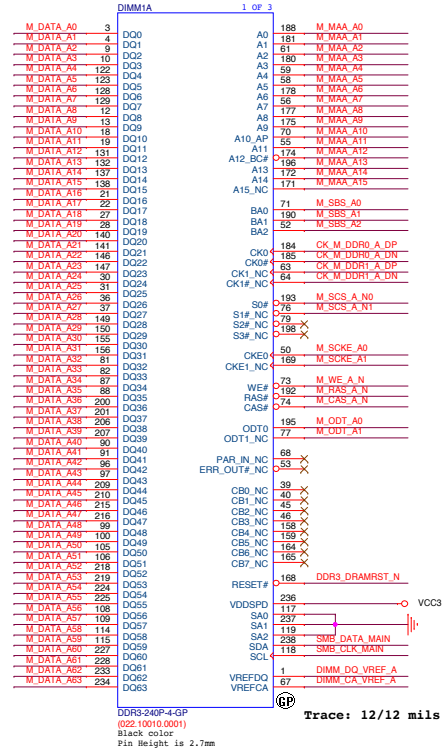
12 M_SCS_A_N0
12 M_SCS_A_N1
12 M_SCKE_A0
12 M_SCKE_A1
12 M_ODT_A0
12 M_ODT_A1

DDR CLOCK

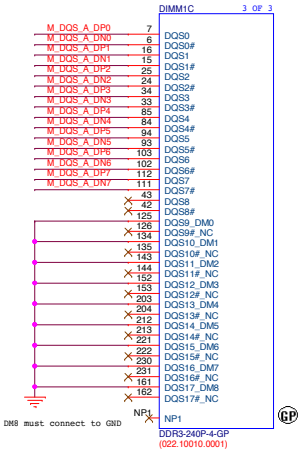
12 CK_M_DDR0_A_DP
12 CK_M_DDR0_A_DN
12 CK_M_DDR1_A_DP
12 CK_M_DDR1_A_DN

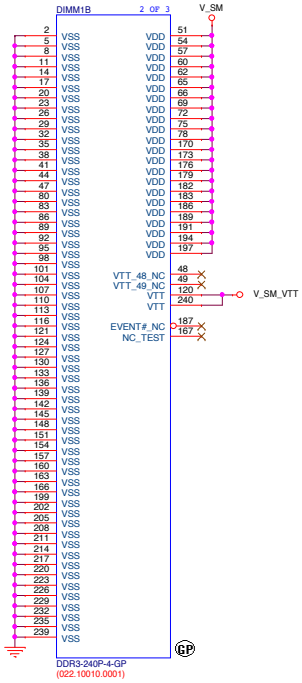
DDR OTHERS

14,17,39 SMB_DATA_MAIN
14,17,39 SMB_CLK_MAIN
12,17 DDR3_DRAMRST_N
12 DIMM_DQ_CPU_VREF_A
10,17 DIMM_CA_VREF_A



Trace: 12/12 mils

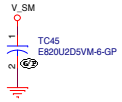




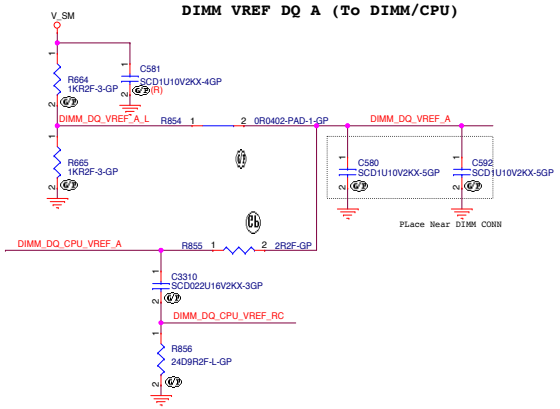
CHANNEL A DIMM1

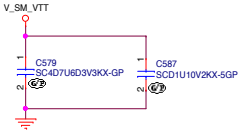
SMB ADDRESS: 000

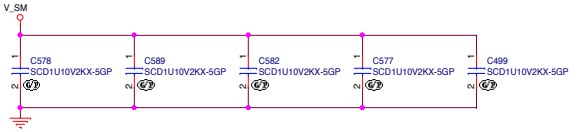
SPD R/W: 0*A1, 0*A0



DIMM VREF DQ A (To DIMM/CPU)



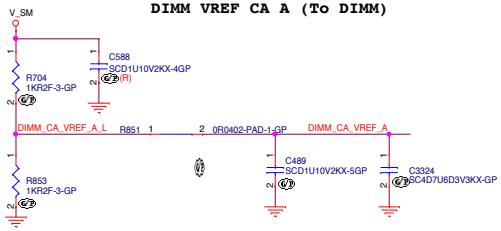




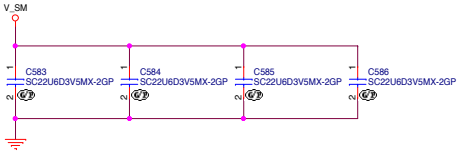
Place Near Power Pin

Net	CAP	Qty
V_SM	0.1uf 0402 X5R	5+4
V_SM_VTT	4.7uf 0603 X5R	1
V_SM_VTT	0.1uf 0402 X5R	1

DIMM VREF CA A (To DIMM)



CAPS FOR DIMM



<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: DDR3 CHA DIMM 0

Size: C | Document Number: ROSA General-SFF | Rev: -1A

Date: Thursday, August 15, 2013 | Sheet 15 of 51

TBD

<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	TBD	
Size: A	Document Number: ROSA General-SFF	Rev: -1A
Date: Thursday, August 15, 2013	Sheet 16 of 51	

DDR DATA

12 M_DATA_B[0..63]
12 M_DQS_B_DP[0..7]
12 M_DQS_B_DN[0..7]

DDR CMD/ADD

12 M_MAA_B[0..15]
12 M_WE_B_N
12 M_CAS_B_N
12 M_RAS_B_N
12 M_SBS_B0
12 M_SBS_B1
12 M_SBS_B2

DDR CTRL

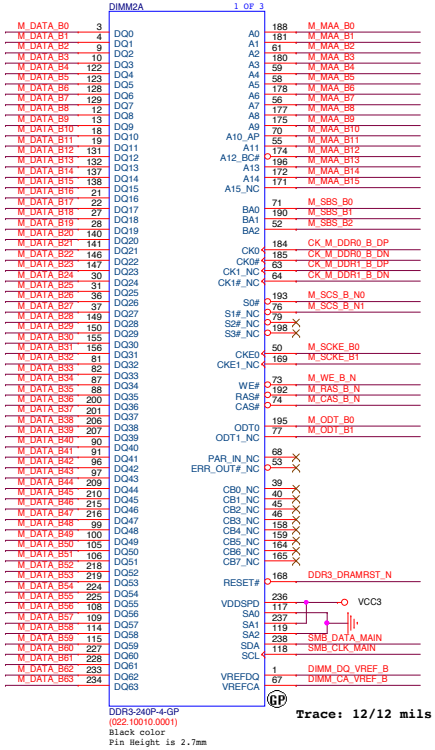
12 M_SCS_B_N0
12 M_SCS_B_N1
12 M_SCKE_B0
12 M_SCKE_B1
12 M_ODT_B0
12 M_ODT_B1

DDR CLOCK

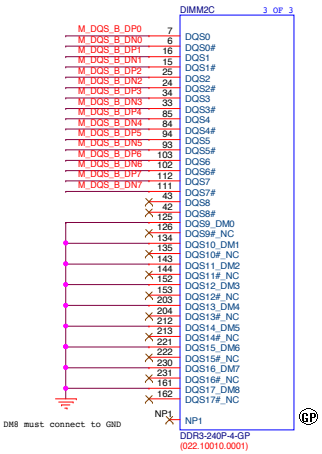
12 CK_M_DDR0_B_DP
12 CK_M_DDR0_B_DN
12 CK_M_DDR1_B_DP
12 CK_M_DDR1_B_DN

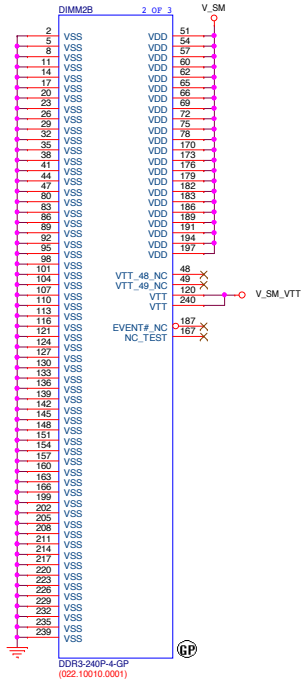
DDR OTHERS

14,15,39 SMB_DATA_MAIN
14,15,39 SMB_CLK_MAIN
12,15 DDR3_DRAMRST_N
12 DIMM_DQ_CPU_VREF_B
10,15 DIMM_CA_VREF_B



Trace: 12/12 mils



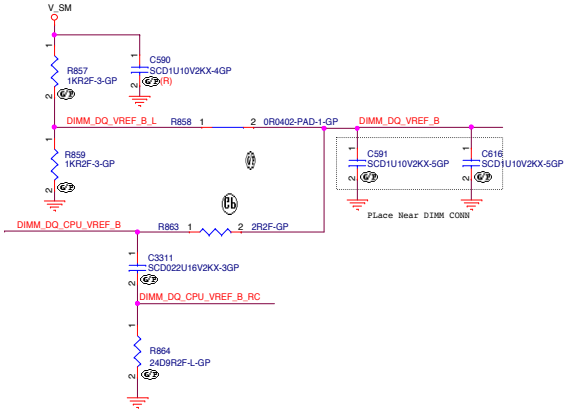


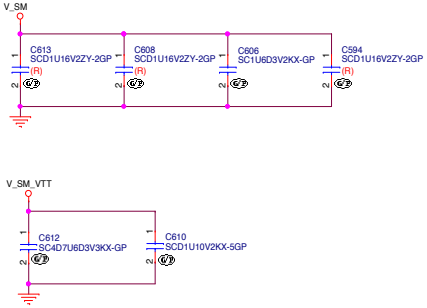
CHANNEL B DIMM1

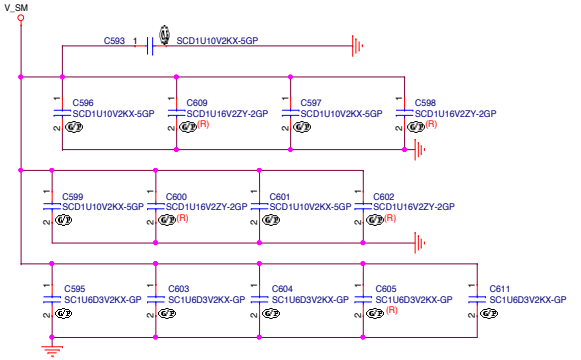
SMB ADDRESS: 010

SPD R/W: 0*A5, 0*A4

DIMM VREF DQ B (To DIMM/CPU)







DIMM VREF CA B (To DIMM)

Place Near Power Pin

Net	CAP	Qty
V_SM	0.1uf 0402 X5R	9
V_SM	1uf 0402 X5R	5
V_SM_VTT	0.1uf 0402 X5R	1
V_SM_VTT	4.7uf 0603 X5R	1

<Variant Name>

wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: DDR3 CHB DIMM 0

Size: C | Document Number: ROSA General-SFF | Rev: -1A

Date: Thursday, August 15, 2013 | Sheet 17 of 51

TBD

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	TBD	
Size: A	Document Number: ROSA General-SFF	Rev: -1A
Date: Thursday, August 15, 2013	Sheet 18 of 51	

LPC

14,39 L_AD0
14,39 L_AD1
14,39 L_AD2
14,39 L_AD3
14,39 L_FRAME_N

HD LINK

36 AUD_LINK_BCLK
36 AUD_LINK_RST_N
36 AUD_LINK_SDIN
36 AUD_LINK_SDO
36 AUD_LINK_SYNC
23 AUD_LINK_SDO_R

SMBUS

26,39,42,43 SMB_CLK_RESUME
26,39,42,43 SMB_DATA_RESUME
39 SMLICLK_PCH
39 SMLIDATA_PCH

JTAG

14 PCH_JTAG_RST_R
14 PCH_JTAG_TCK
14 PCH_JTAG_TDI
14 PCH_JTAG_TDO
14 PCH_JTAG_TMS

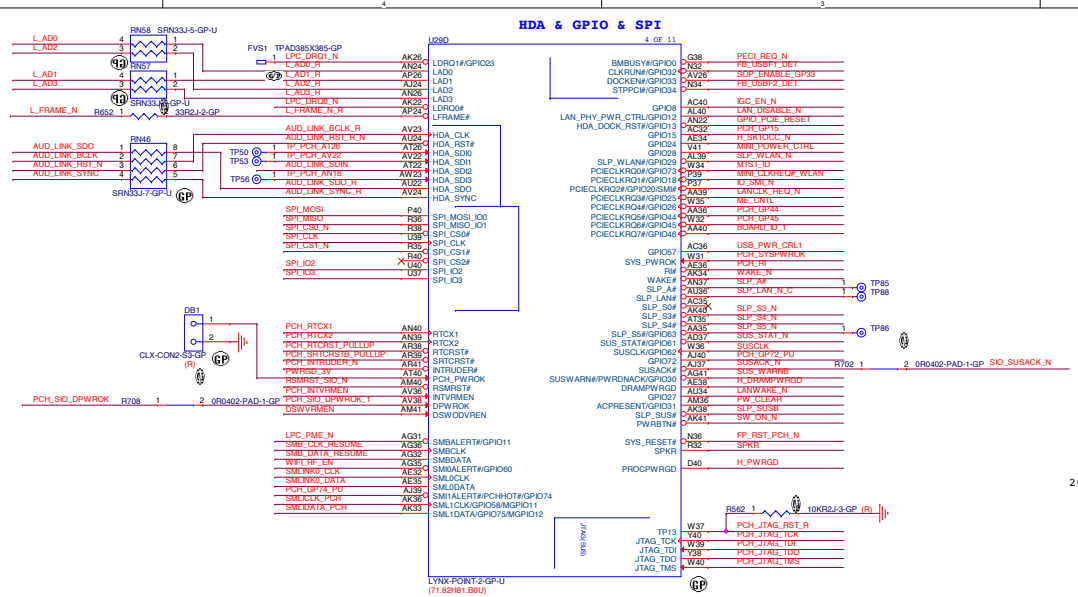
PWR MANAGER

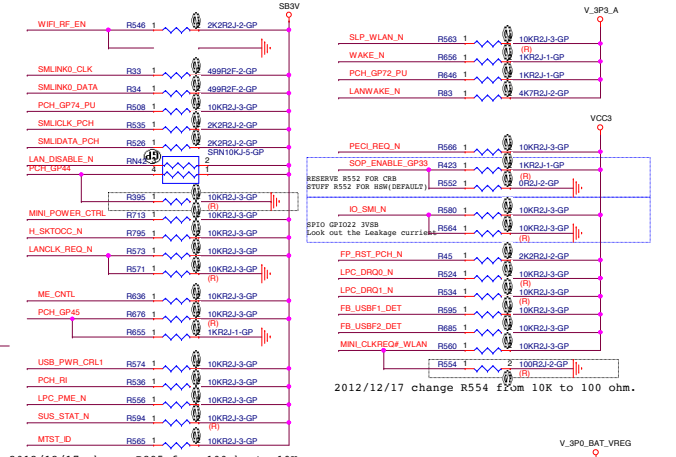
10,46 H_DRAMPWRGD
10,14 H_PWRGD
10 FP_RST_DBR_N
12,14,21,39 PWRGD_3V
39 RSMRST_SIO_N
14,50 VR_READY
39,46,48,50 SLP_S3_N
39,45,47 SLP_S4_N
14,39 SW_ON_N

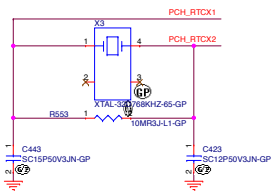
GPIO/MISC

10,50 H_SKTOCC_N
23 PCH_INTVRMEN
39 PCH_SIO_DPWROK
23 DSWVRMEN
39 LPC_PME_N
43 WIFI_RF_EN
34 FB_USBF1_DET
23 IGC_EN_N
35 LAN_DISABLE_N
26 GPIO_PCIE_RESET
23 PCH_GP15
46 MINI_POWER_CTRL
45 MTST_ID
43 MINI_CLKREQ#_WLAN
39 IO_SMI_N
35 LANCLK_REQ_N
22 BOARD_ID_1
46 USB_PWR_CRL1
26,35,42,43 WAKE_N
23 SUSCLK
39 SIO_SUSACK_N
39,46 SUS_WARNB
48 SLP_SUSB
23 SPKR
34 FB_USBF2_DET
43 FP_RST_PCH_N

HDA & GPIO & SPI





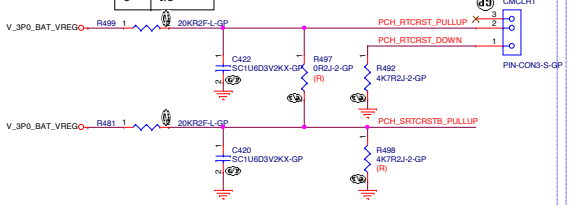


The 2nd source is 82.30001.A81

CLEAN CMOS

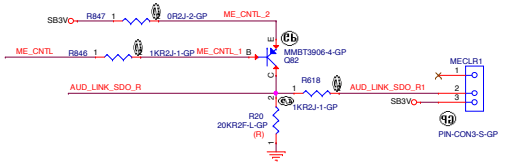
1	GND
2	RTC_RST
3	NC

1-2	CLR
2-3	NORMAL(DEFAULT)



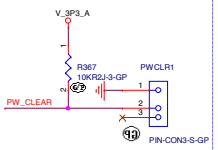
ME ENABLE/DISABLE

1	NC
2	AUD_LINK_SDO_R1
3	SB3V



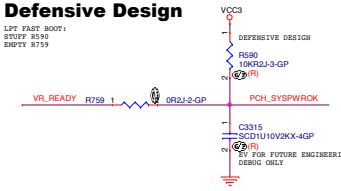
PASSWORD CLEAR

1-2	CLR PASSWORD
2-3	NORMAL(DEFAULT)



Defensive Design

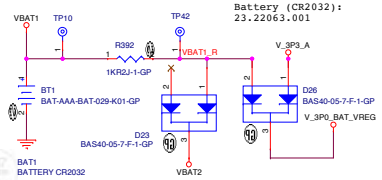
LPT FAST BOOT:
STUFF R590
EMPTY R759



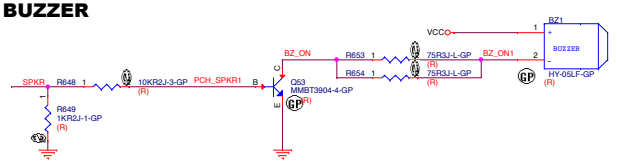
VCCRTC

Battery Socket
ST: 22.70017.051
FLAT: 22.70017.061

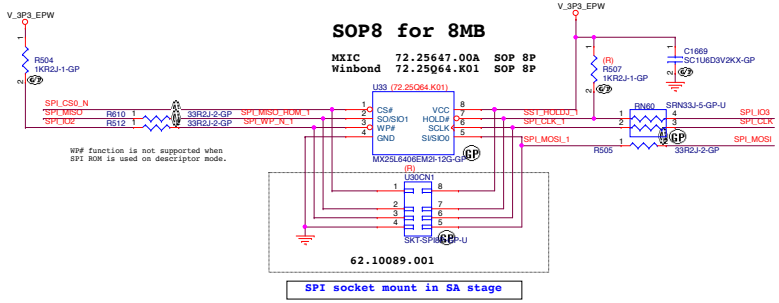
Battery (CR2032):
23.22063.001



BUZZER



SPI ROM



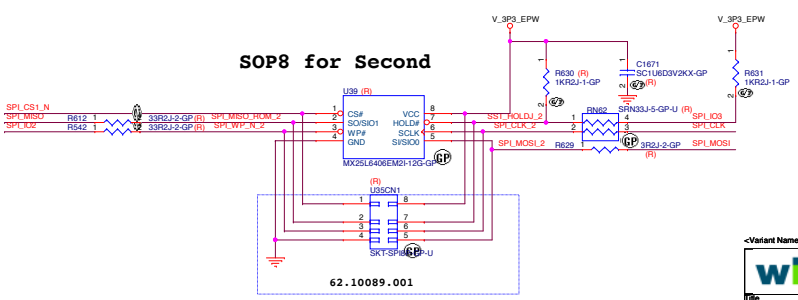
SOP8 for 8MB

MXIC 72.25647.00A SOP 8P
Winbond 72.25Q64.K01 SOP 8P

62.10089.001

SPI socket mount in SA stage

SOP8 for Second



62.10089.001

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Lynxpoint_AUDIO/GPIO/SPI

Size	Document Number	Rev
C	ROSA General-SFF	-1A

Date: Thursday, August 15, 2013 Sheet 19 of 51

CPU CLOCK

10 CK_PE_100M_MCP_DN
10 CK_PE_100M_MCP_DP

PCI CLOCK

39 CK_P_33M_TPM
14 CK_P_33M_LPCP80
22 CK_PCH_33M_FB
39 CK_P_33M_SIO

PCIE CLOCK

10 CK_DPNS_R_DN
10 CK_DPNS_R_DP

11 CK_DP_DN
11 CK_DP_DP

14 CK_100M_CPU_XDP_DN
14 CK_100M_CPU_XDP_DP

26 CK_PE_100M_16PORT_DN
26 CK_PE_100M_16PORT_DP

35 CK_GLAN_DN
35 CK_GLAN_DP

43 CK_PCIEX1_WLAN_DN
43 CK_PCIEX1_WLAN_DP

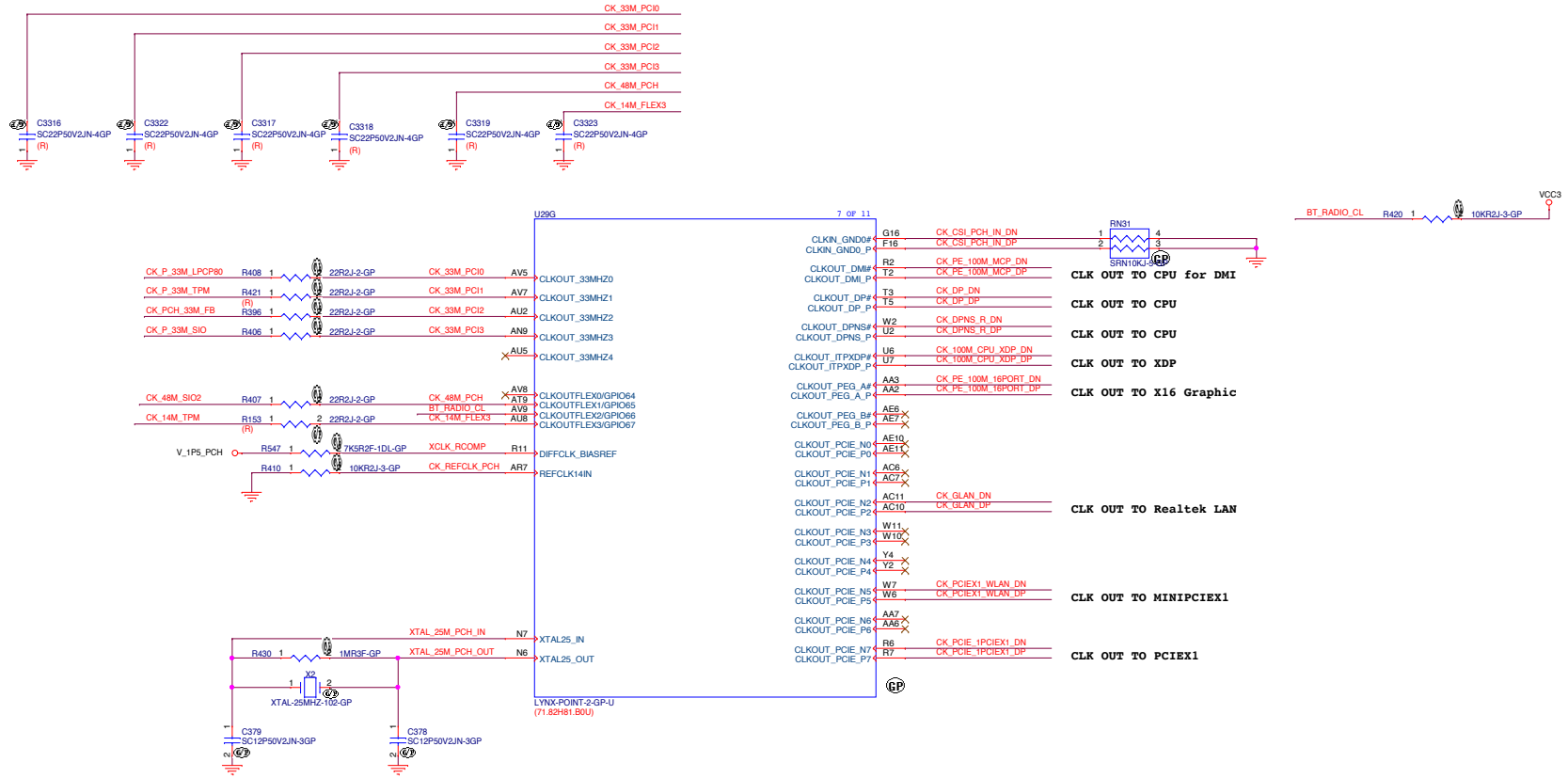
42 CK_PCIE_1PCIEX1_DN
42 CK_PCIE_1PCIEX1_DP

14M and 48M CLOCK

39 CK_48M_SIO2
39 CK_14M_TPM

GPIO

43 BT_RADIO_CL



<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Lynxpoint_CLK

Size	Document Number	Rev
C	ROSA General-SFF	-1A

Date: Thursday, August 15, 2013 Sheet 20 of 51

SATA

25 SATAHDR_RX_DN0
25 SATAHDR_RX_DP0
25 SATAHDR_TX_DN0
25 SATAHDR_TX_DP0

25 SATAHDR_RX_DN1
25 SATAHDR_RX_DP1
25 SATAHDR_TX_DN1
25 SATAHDR_TX_DP1

39,45 PCH_SATA_LED_N

Straps

23 SATA1GP
23 SATA2GP
23 SATA3GP

OTHERS

10 H_PM_SYNC_0
10,39 H_PECI
10 H_THERMTRIP_N
12,14,19,39 PWRGD_3V
36 FP_AUD_DETECT
39 A20GATE
39 KBRST_N
39 SER_IRQ
10,14 PLTRST_CPU_N
26 PCIEX16_PRSNT2_N
45 CHASSIS_ID_1
45 CHASSIS_ID_0
22 BOARD_ID_0
42 PCIEX1_PRSNT2_N

HDMI

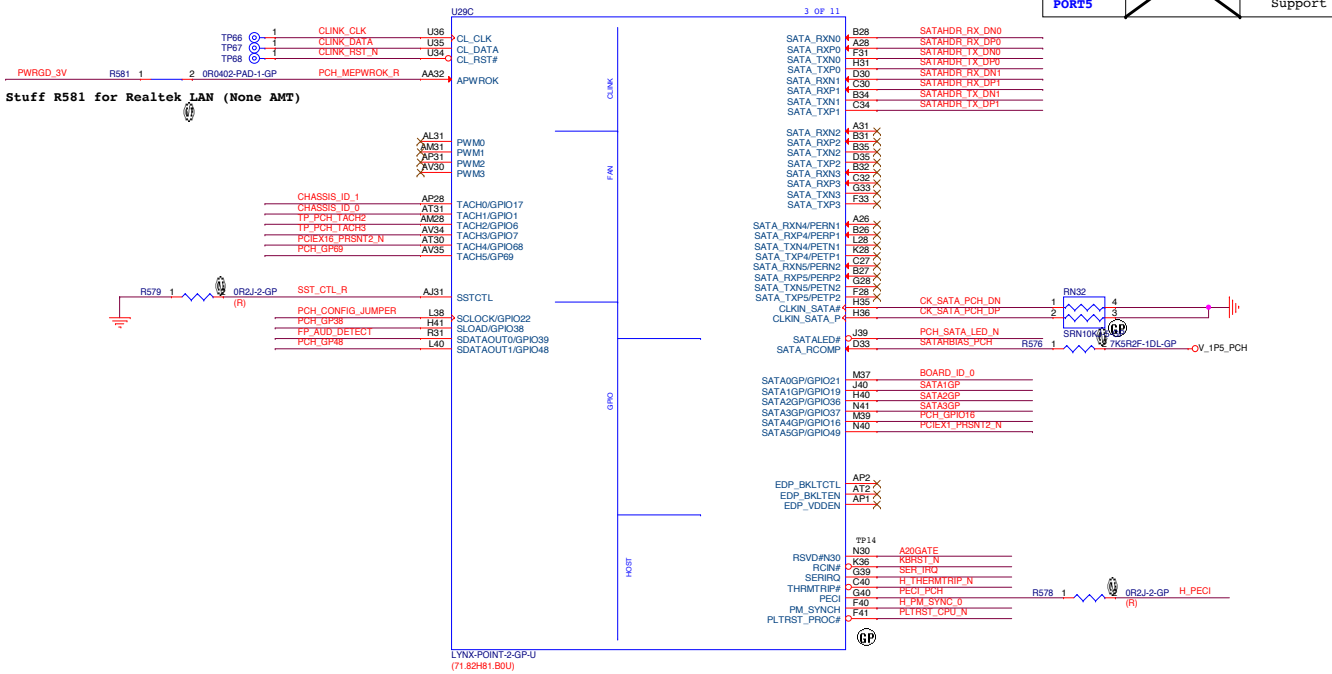
22,28 DDSP_C_HPD
28 DDPC_CTRL_CLK
28 DDPC_CTRL_DATA

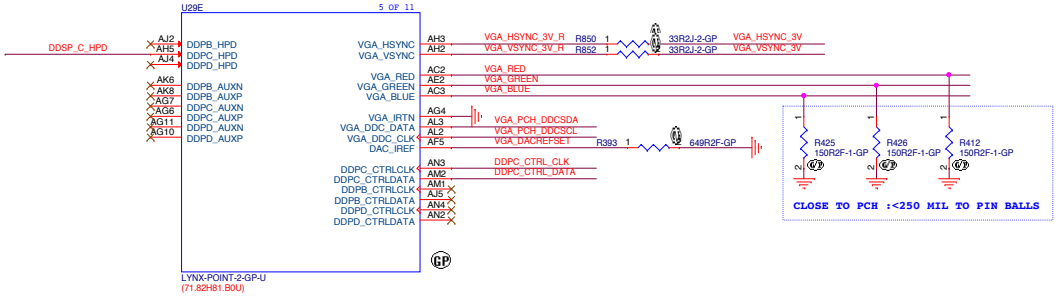
VGA

27 VGA_HSYNC_3V
27 VGA_VSYNC_3V
27 VGA_RED
27 VGA_GREEN
27 VGA_BLUE
27 VGA_PCH_DDCSDA
27 VGA_PCH_DDCSCL

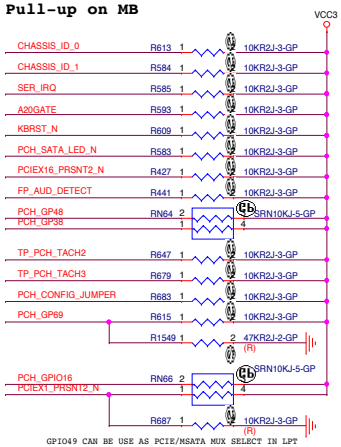
SATA5 Port (H81)

	SATA 3.0 PORT	SATA 2.0 Port
PORT0	Support	Support
PORT1	Support	Support
PORT2		Disabled
PORT3		Disabled
PORT4		Support
PORT5		Support





Pull-up on MB



<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Lynxpoint_SATA/FAN/DP/VGA

Size: C | Document Number: ROSA General-SFF | Rev: -1A

Date: Thursday, August 15, 2013 | Sheet 21 of 51

DMI

11 DMI_MT_IR_DN[0..3]
11 DMI_MT_IR_DP[0..3]
11 DMI_IT_MR_DN[0..3]
11 DMI_IT_MR_DP[0..3]

PCIE

42 HSI_DN3
42 HSI_DP3
42 HSO_C_DN3
42 HSO_C_DP3

43 HSI_DN4
43 HSI_DP4
43 HSO_C_DN4
43 HSO_C_DP4

35 HSI_DN5
35 HSI_DP5
35 HSO_C_DN5
35 HSO_C_DP5

USB2.0

33 USB_PCH_DN0
33 USB_PCH_DP0
33 USB_PCH_DN1
33 USB_PCH_DP1
34 USB_PCH_DN2
34 USB_PCH_DP2
34 USB_PCH_DN3
34 USB_PCH_DP3
34 USB_PCH_DN4
34 USB_PCH_DP4
43 USB_PCH_DN5
43 USB_PCH_DP5
31 USB_PCH_DN8
31 USB_PCH_DP8
31 USB_PCH_DN9
31 USB_PCH_DP9
30 USB_PCH_DN10
30 USB_PCH_DP10
30 USB_PCH_DN11
30 USB_PCH_DP11

33 USB_OC_01*
34 USB_OC_23*
34 USB_OC_45*
31 USB_OC_89*
30 USB_OC_1011*

USB3.0

30 USB3_TX2_C_DN
30 USB3_TX2_C_DP
33 USB3_TX1_C_DN
33 USB3_TX1_C_DP
33 USB3_TX0_C_DP
33 USB3_TX0_C_DN

30 USB3_RX2_DN
30 USB3_RX2_DP
33 USB3_RX1_DN
33 USB3_RX1_DP
33 USB3_RX0_DP
33 USB3_RX0_DN

FDI

11 FDI_TX_DN[0..1]
11 FDI_TX_DP[0..1]

11 FDI_INT
11 FDI_CSYNC

OTHERS

20 CK_PCH_33M_FB
43 W1_DETECT_USB
21,28 DDSP_C_HPD
27 VGA_DET

26,39 PLTRST_N
23 P_GNT_N1
23 P_GNT_N2
23 P_GNT_N3
21 BOARD_ID_0

PCIEX1 CONN

LAN

Mini PCIEX1 SLOT

2012/12/12
For Layout, swaping
OLD NET: NET 'USB3_TX1_C_DN' U29.B18
NEW NET: NET 'USB3_TX1_C_DN' U29.G18
OLD NET: NET 'USB3_RX2_DN' U29.G18
NEW NET: NET 'USB3_RX2_DN' U29.B15
OLD NET: NET 'USB3_TX1_C_DP' U29.C18
NEW NET: NET 'USB3_TX1_C_DP' U29.H18
OLD NET: NET 'USB3_RX2_DP' U29.H18
NEW NET: NET 'USB3_RX2_DP' U29.B16
OLD NET: NET 'USB3_TX2_C_DN' U29.B15
NEW NET: NET 'USB3_TX2_C_DN' U29.B18
OLD NET: NET 'USB3_TX2_C_DP' U29.B16
NEW NET: NET 'USB3_TX2_C_DP' U29.C18

FOR Front USB 3.0 header and Rear USB3.0 Connector Co-Layout

FOR Rear USB2.0 + USB 3.0

FOR Rear USB3.0
FOR Rear USB3.0
FOR Rear USB 2.0
FOR Rear USB 2.0
FOR Front USB2.0 header
FOR Mini PCIEx1 slot

FOR Rear USB+LAN
FOR Rear USB+LAN
FOR Front USB 2.0 header
FOR Front USB 3.0 header

USBRBIAS_PHY (R617): TIE TRACES TOGETHER CLOSE TO PINS, WITH LENGTH NO LONGER THAN 1 INCHE TO RESISTOR

05/03
Add Co-layout resistors

USB3_RX0_DN / USB3_RX0_DP; USB3_TX0_C_DN / USB3_TX0_C_DP from rear USB3.0 CONN
USB3_RX2_DN / USB3_RX2_DP; USB3_TX2_C_DN / USB3_TX2_C_DP from front USB 3.0

FOR LPT: GP70 STRAP - USB3 PORT4
GP71 - USB3 PORT5
SOFT STRAP TO DETERMINE NATIVE FUNCTION

BOARD ID

Board ID	Mission	Sawgrass
BOARD_ID_0	0	0
BOARD_ID_1	0	0

<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Lynxpoint_FDI/PCIE/DMI/USB

Size: C | Document Number: ROSA General-SFF | Rev: -1A

Date: Thursday, August 15, 2013 | Sheet 22 of 51

STRAP

21 SATA1GP
21 SATA2GP
21 SATA3GP
22 P_GNT_N1

10 HSW_STRAP_13
19 IGC_EN_N

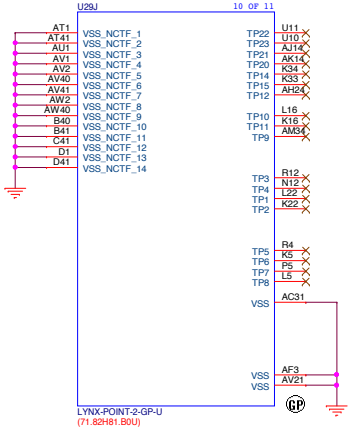
19 AUD_LINK_SDO_R
19 SUSCLK
19 SPKR

22 P_GNT_N2
22 P_GNT_N3

19 PCH_INTVRMEN

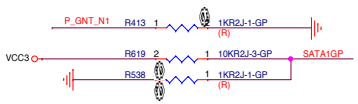
19 DSWVRMEN

19 PCH_GP15

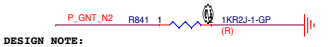


BOOT SELECT STRAPS

BOOT DEVICE	GNT1/ GPIO51	SATA1GP /GPIO19
LPC	0	0
SPI	1	1

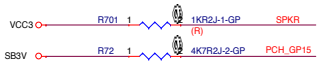


DESIGN NOTE:
WEAK INTERNAL PULLUPS ON GP51. DEFAULT SPI BOOT DEVICE.



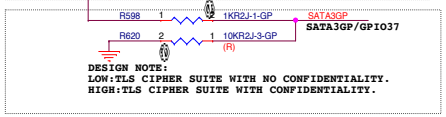
DESIGN NOTE:
FULL VOLTAGE MODE WHEN SAMPLED LOW
DMI AC COUPLING

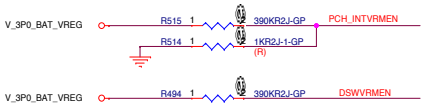
DESIGN NOTE:
A16 SWAP OVERRIDE OVERRIDE IF SAMPLED LOW

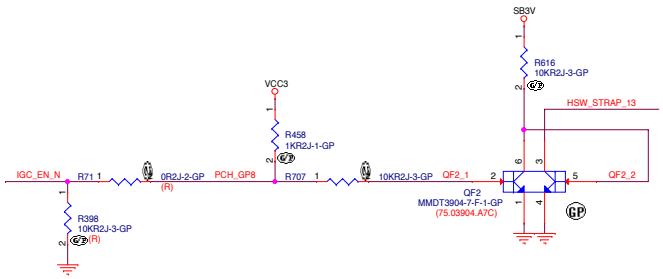


DESIGN NOTE:
SPI OVERRIDE PROTECTION

DESIGN NOTE:
OD PLL VR ENABLE
DISABLE WHEN SAMPLED LOW







PCH Functional Straps

PCH EDS,Page88,Table 2-27

SPKR	The signal has a weak internal pull-down. Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot"mode (Cougar Point will disable the TCO Timer system reboot feature). The status of this strap is readable via the NO REBOOT bit (Chipset Config Registers: Offset 3410h:Bit 5).
INIT3_3VB	This signal has a weak internal pull-up. Note: the internal pull-up is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled low
P_GNT_N3	Top-Block Swap Override The signal has a weak internal pull-up. If the signal is sampled low, this indicates that the system is strapped to the "topblock swap" mode
PCH_INTVRMEN	Integrated 1.05 V VRMs is enabled when high NOTE: This signal should always be pulled high
P_GNT_N1	Boot BIOS Destination Selection Signal has weak internal pull-ups.
SATA1GP (GPIO19)	Boot BIOS Destination Selection Signal has weak internal pull-ups.
P_GNT_N2	The signal has a weak internal pull-up.
AUD_LINK_SDO_R	Flash Descriptor Security Override Strap .
AUD_LINK_SYNC-R	The signal has a weak internal pull-down. On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low.
PCH_GP28_PU (GPIO28) USB_CH_M2	The signal has a weak internal pull-up. The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled.
DF_TVS	DMI and FDI Tx/Rx Termination Voltage The signal has a weak internal pull-down.
DSWVRMEN	Deep S4/S5 Well On-Die Voltage Regulator Enable If strap is sampled high, the Integrated Deep S4/S5 Well (DSW) On-Die VR mode is enabled.
CDC_DWN_DISABLE (SATA2GP/GPIO36)	DMI RX TERMINATION VOLTAGE OVERRIDE This signal has a weak internal pull-down
PCH_GP37 (SATA3GP/GPIO37)	FDI RX TERMINATION VOLTAGE OVERRIDE This signal has a weak internal pull-down
TLS_EN (GPIO15)	The signal has a weak internal pull-down. Low = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel ME Crypto TLS cipher suite with confidentiality A strong pull up may be needed for GPIO functionality

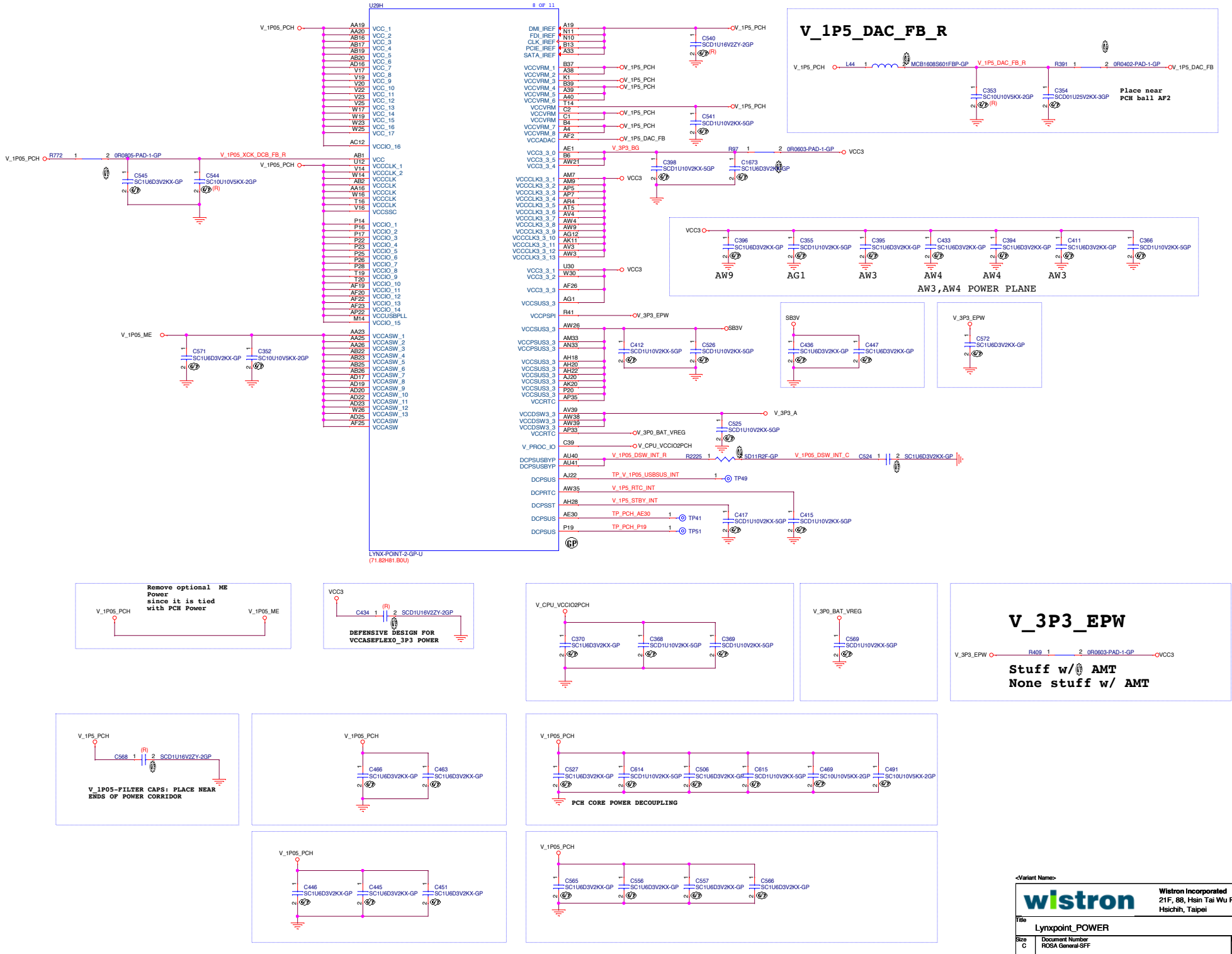
<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Lynxpoint_GND/STRAPS

Size: C | Document Number: ROSA General-SFF | Rev: -1A

Date: Thursday, August 15, 2013 | Sheet 23 of 51



<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Lynxpoint_POWER

Size: C | Document Number: ROSA General-SFF | Rev: -1A

Date: Thursday, August 15, 2013 | Sheet 24 of 51

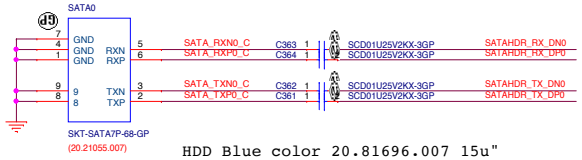
SATA

21 SATAHDR_RX_DP0
21 SATAHDR_RX_DN0

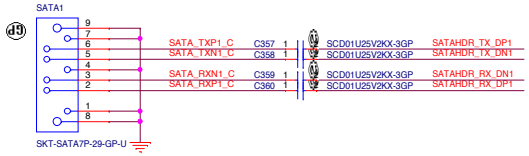
21 SATAHDR_TX_DN0
21 SATAHDR_TX_DP0

21 SATAHDR_RX_DP1
21 SATAHDR_RX_DN1

21 SATAHDR_TX_DN1
21 SATAHDR_TX_DP1



HDD Blue color 20.81696.007 15u"
Pin length 2.1mm



ODD White color 20.81274.007 15u"
Pin length 2.05mm

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: SATA Port

Size	Document Number	Rev
C	ROSA General-SFF	-1A

Date: Thursday, August 15, 2013 Sheet 25 of 51

PCIEX16

11 EXP_A_RX_DN[0..15]
11 EXP_A_RX_DP[0..15]

11 EXP_A_TX_DP[0..15]
11 EXP_A_TX_DN[0..15]

20 CK_PE_100M_16PORT_DP
20 CK_PE_100M_16PORT_DN

OTHERS

19,39,42,43 SMB_CLK_RESUME
19,39,42,43 SMB_DATA_RESUME

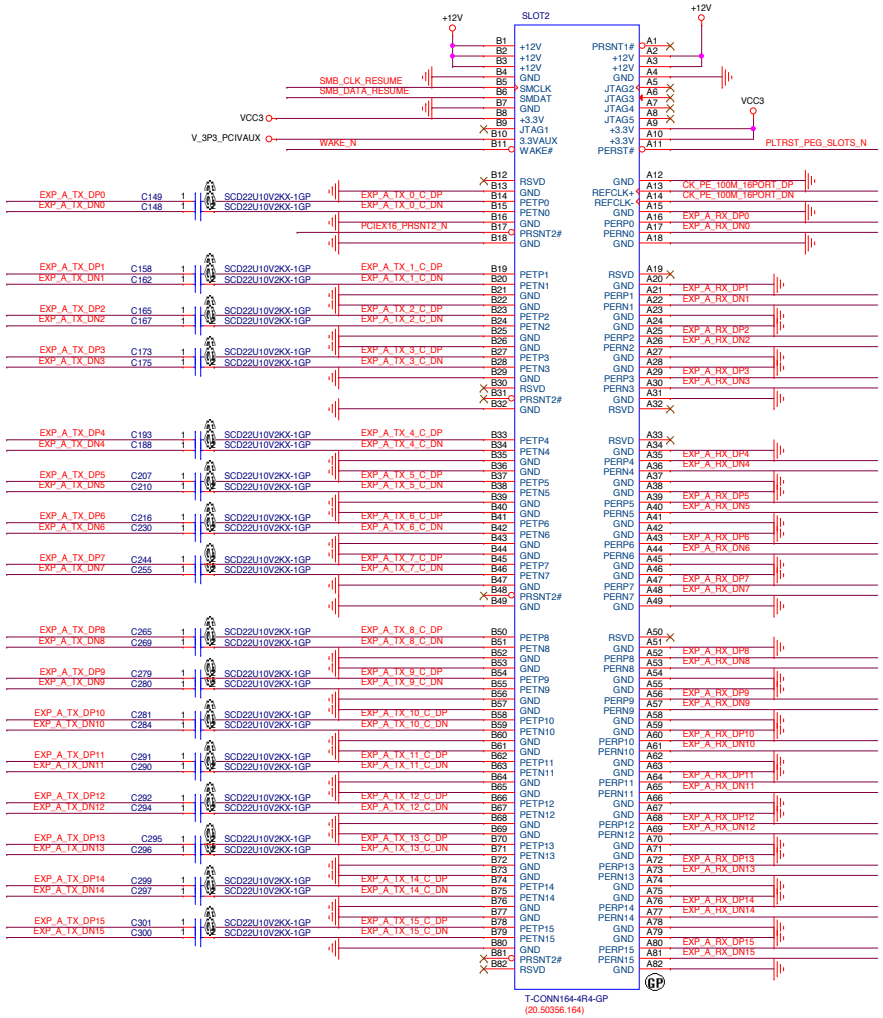
19,35,42,43 WAKE_N
21 PCIEX16_PRSNT2_N

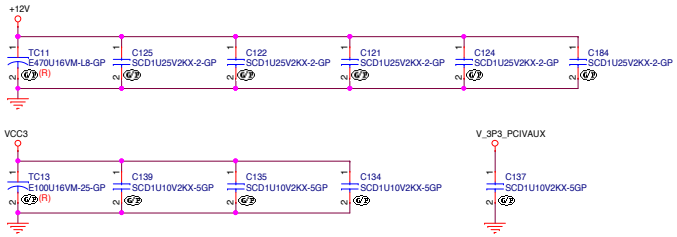
22,39 PLTRST_N
19 GPIO_PCIE_RESET

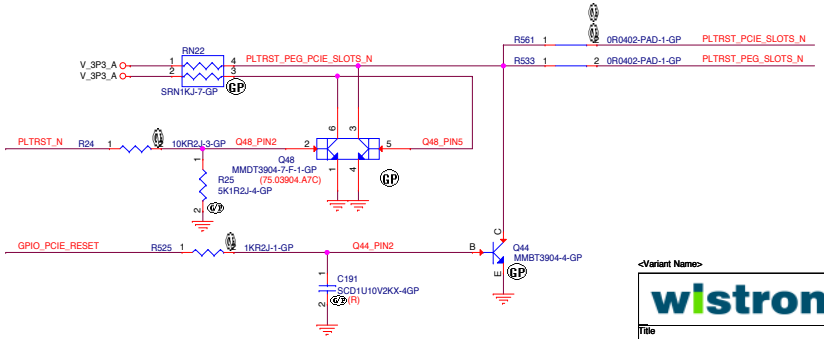
42,43 PLTRST_PCIE_SLOTS_N

w/o Latch: 20.50352.164
with Latch: 20.50356.164

PCIEx16 CONN may need LATCH if supporting 75W GFX Card







<Variant Name>

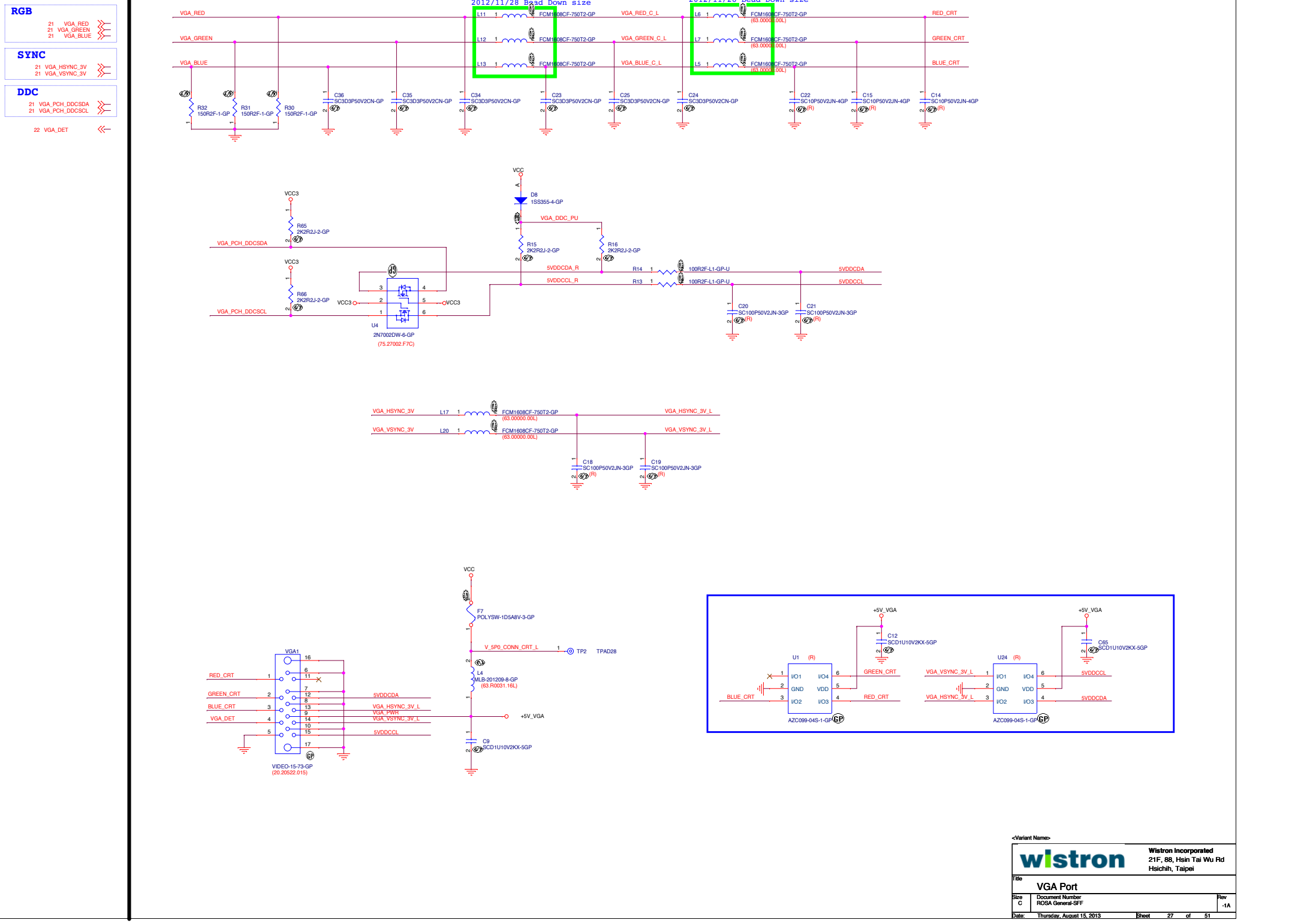
wistron

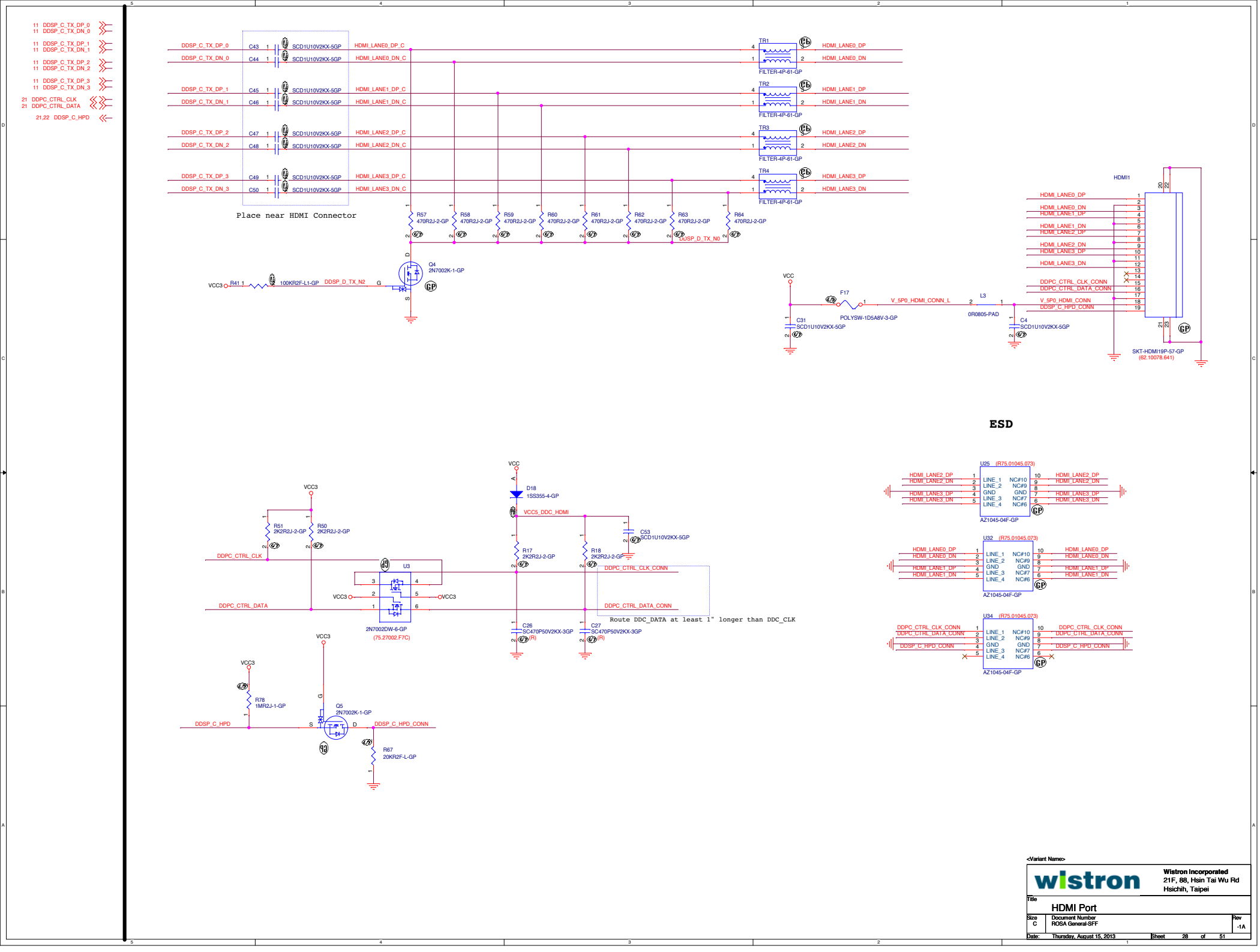
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: PCIEX16 CONNECTOR

Size	Document Number	Rev
C	ROSA General-SFF	-1A

Date: Thursday, August 15, 2013 Sheet 26 of 51


RGB
21 VGA_RED
21 VGA_GREEN
21 VGA_BLUE
SYNC
21 VGA_HSYNC_3V
21 VGA_VSYNC_3V
DDC
21 VGA_PCH_DDCSDA
21 VGA_PCH_DDCSCL
22 VGA_DET
2012/11/28 Bead Down size
2012/11/28 Bead Down size
VGA_RED
VGA_GREEN
VGA_BLUE
VGA_RED_C_L
VGA_GREEN_C_L
VGA_BLUE_C_L
RED_CRT
GREEN_CRT
BLUE_CRT
L11
L12
L13
L6
L7
L5
FCM1608CF-750T2-GP
(63.00000.00L)
R32 150R2F-1-GP
R31 150R2F-1-GP
R30 150R2F-1-GP
C36 SC3D3P50V2CN-GP
C35 SC3D3P50V2CN-GP
C34 SC3D3P50V2CN-GP
C23 SC3D3P50V2CN-GP
C25 SC3D3P50V2CN-GP
C24 SC3D3P50V2CN-GP
C22 SC10P50V2JN-4GP (R)
C15 SC10P50V2JN-4GP (R)
C14 SC10P50V2JN-4GP (R)
VCC
VCC3
D8 1SS355-4-GP
VGA_DDC_PU
R65 2K2R2J-2-GP
R66 2K2R2J-2-GP
R15 2K2R2J-2-GP
R16 2K2R2J-2-GP
VGA_PCH_DDCSDA
VGA_PCH_DDCSCL
5VDDCDA_R
5VDDCCL_R
R14 100R2F-L1-GP-U
R13 100R2F-L1-GP-U
5VDDCDA
5VDDCCL
C20 SC100P50V2JN-3GP (R)
C21 SC100P50V2JN-3GP (R)
U4
2N7002DW-6-GP
(75.27002.F7C)
VGA_HSYNC_3V
VGA_VSYNC_3V
L17
L20
VGA_HSYNC_3V_L
VGA_VSYNC_3V_L
C18 SC100P50V2JN-3GP (R)
C19 SC100P50V2JN-3GP (R)
F7 POLYSW-1D5A8V-3-GP
V_5P0_CONN_CRT_L
TP2 TPAD28
L4 MLB-201209-8-GP (63.R0031.16L)
+5V_VGA
C9 SCD1U10V2KX-5GP
VGA1
VIDEO-15-73-GP (20.20522.015)
VGA_PWR
VGA_DET
U1 (R)
U24 (R)
C12 SCD1U10V2KX-5GP
C65 SCD1U10V2KX-5GP
I/O1
I/O2
I/O3
I/O4
GND
VDD
AZC099-04S-1-GP
<Variant Name>
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
VGA Port
Size C
Document Number
ROSA General-SFF
Rev -1A
Date: Thursday, August 15, 2013
Sheet 27 of 51



<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: HDMI Port

Size: C | Document Number: ROSA General-SFF | Rev: -1A

Date: Thursday, August 15, 2013 | Sheet 28 of 51

TBD

<Variant Name>

wistron

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21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

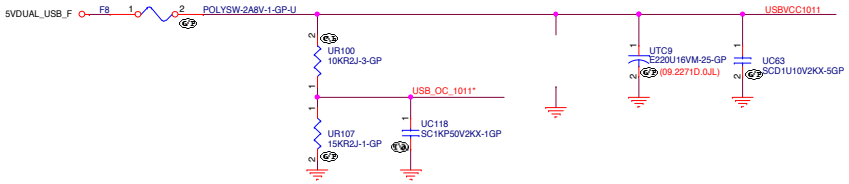
Title	TBD	
Size: A	Document Number: ROSA General-SFF	Rev: -1A
Date: Thursday, August 15, 2013	Sheet 29 of 51	

FRONT USB

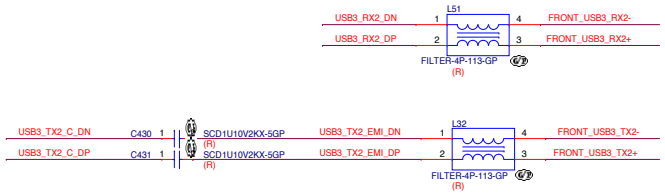
22 USB_PCH_DP10
22 USB_PCH_DN10
22 USB_PCH_DP11
22 USB_PCH_DN11

22 USB3_RX2_DN
22 USB3_RX2_DP
22 USB3_TX2_C_DN
22 USB3_TX2_C_DP

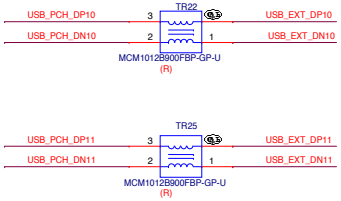
22 USB_OC_1011*
19 FB_USBF2_DET



USB 3.0



USB 2.0



ESD

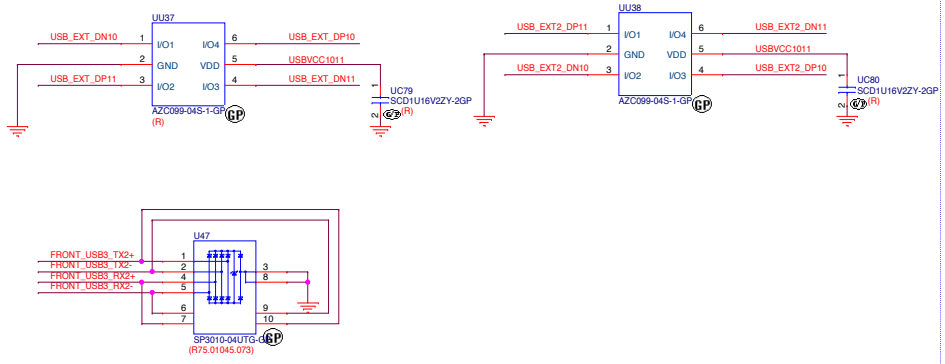
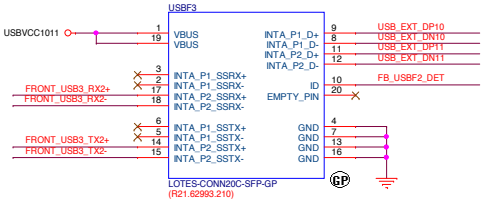
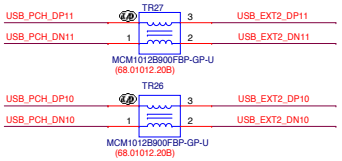
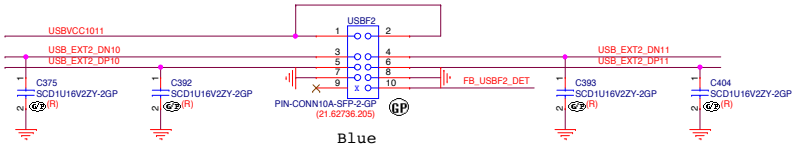


Table 2-1: USB3 ICC A Pin Assignment and Description

Pin No.	Signal	Description
1	Vbus	Power
2	IntA_P1_SSRX-	USB3 ICC Port1 SuperSpeed Rx-
3	IntA_P1_SSRX+	USB3 ICC Port1 SuperSpeed Rx+
4	GND	GND
5	IntA_P1_SSTX-	USB3 ICC Port1 SuperSpeed Tx-
6	IntA_P1_SSTX+	USB3 ICC Port1 SuperSpeed Tx+
7	GND	GND
8	IntA_P1_D-	USB3 ICC Port1 D- (USB2 Signal D-)
9	IntA_P1_D+	USB3 ICC Port1 D+ (USB2 Signal D+)
10	ID	Over Current Protection
11	IntA_P2_D+	USB3 ICC Port2 D+ (USB2 Signal D+)
12	IntA_P2_D-	USB3 ICC Port2 D- (USB2 Signal D-)
13	GND	GND
14	IntA_P2_SSTX+	USB3 ICC Port2 SuperSpeed Tx+
15	IntA_P2_SSTX-	USB3 ICC Port2 Super Speed Tx-
16	GND	GND
17	IntA_P2_SSRX+	USB3 ICC Port2 SuperSpeed Rx+
18	IntA_P2_SSRX-	USB3 ICC Port2 SuperSpeed Rx-
19	Vbus	Power







Blue
For Front USB2.0

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: FRONT USB3.0&2.0 HEADER

Size	Document Number	Rev
C	ROSA General-SFF	-1A

Date: Thursday, August 15, 2013 Sheet 30 of 51

REAR USB+LAN

22 USB_PCH_DN8
22 USB_PCH_DP8
22 USB_PCH_DN9
22 USB_PCH_DP9

35 LAN_MDI2_DP
35 LAN_MDI2_DN
35 LAN_MDI1_DP
35 LAN_MDI1_DN
35 LAN_MDI0_DP
35 LAN_MDI0_DN
35 LAN_MDI3_DP
35 LAN_MDI3_DN

35 SPEED_100_N
35 SPEED_1000_N
35 LINK_ACTIVITY_N

22 USB_OC_89*

5VDUAL_USB_R — F18 — POLYSW-1D5A8V-3-GP — USBVCC89

UTC5 E220U16VM-25-GP (09.2271D.0JL)
UC22 SCD1U10V2KX-5GP

UR118 10KR2J-3-GP
USB_OC_89*
UR119 15KR2J-1-GP
UC133 SC1KP50V2KX-1GP

TR9
USB_PCH_DN8 — USB_EXT_DN8
USB_PCH_DP8 — USB_EXT_DP8
MCM1012B900FBP-GP-U (68.01012.20B)

TR10
USB_PCH_DN9 — USB_EXT_DN9
USB_PCH_DP9 — USB_EXT_DP9
MCM1012B900FBP-GP-U (68.01012.20B)

UU12
USB_EXT_DP8 — I/O1 — I/O4 — USB_EXT_DN8
GND — VDD — USBVCC89
USB_EXT_DN9 — I/O2 — I/O3 — USB_EXT_DP9
AZC099-04S-1-GP
(R) UC132 SCD1U16V2ZY-2GP

USB+RJ45

RJ45
Orange — SPEED_1000 — UR108 249R2F-GP — SPEED_1000_N
Green — SPEED_100 — UR109 249R2F-GP — SPEED_100_N
USBVCC89
USB_EXT_DN9
USB_EXT_DN8
USB_EXT_DP9
USB_EXT_DP8
UP
LAN_MDI3_DN_C
LAN_MDI3_DP_C
LAN_MDI2_DN_C
LAN_MDI2_DP_C
LAN_MDI1_DN_C
LAN_MDI1_DP_C
LAN_MDI0_DN_C
LAN_MDI0_DP_C
LAN_CONN_CVT
RJ45_ACT — 0V_3P3_LAN
LINK_ACTIVITY — UR112 330R2J-3-GP
UC103 SC1U10V3KX-3GP (R)
UC104 SCD1U10V2KX-5GP
LINK_ACTIVITY_N — LINK_ACTIVITY_N 35
SKT-RJ45-USB-9-GP

	Giga	100	10
Link	Orange	Green	X
Act	Blink	Blink	Blink

TR14
LAN_MDI0_DP — LAN_MDI0_DP_C
LAN_MDI0_DN — LAN_MDI0_DN_C
MCM1012B900FBP-GP-U (66.R0036.04L)

TR12
LAN_MDI2_DP — LAN_MDI2_DP_C
LAN_MDI2_DN — LAN_MDI2_DN_C
MCM1012B900FBP-GP-U (66.R0036.04L)

TR13
LAN_MDI1_DP — LAN_MDI1_DP_C
LAN_MDI1_DN — LAN_MDI1_DN_C
MCM1012B900FBP-GP-U (66.R0036.04L)

TR11
LAN_MDI3_DP — LAN_MDI3_DP_C
LAN_MDI3_DN — LAN_MDI3_DN_C
MCM1012B900FBP-GP-U (66.R0036.04L)

U6
V_3P3_LAN
LAN_MDI1_DP_C — I/O1 — I/O4 — LAN_MDI0_DP_C
GND — VDD
LAN_MDI1_DN_C — I/O2 — I/O3 — LAN_MDI0_DN_C
AZC099-04S-1-GP (75.01215.07C)
C3325 SCD1U10V2KX-5GP (R)

U9
V_3P3_LAN
LAN_MDI3_DP_C — I/O1 — I/O4 — LAN_MDI2_DP_C
GND — VDD
LAN_MDI3_DN_C — I/O2 — I/O3 — LAN_MDI2_DN_C
AZC099-04S-1-GP (75.01215.07C)
C3326 SCD1U10V2KX-5GP (R)

U11
V_3P3_LAN
SPEED_1000 — I/O1 — I/O4 — LINK_ACTIVITY
GND — VDD
SPEED_100 — I/O2 — I/O3
AZC099-04S-1-GP (75.01215.07C)
C3327 SCD1U10V2KX-5GP (R)

<Variant Name>

wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: USB+RJ45
Size: C
Document Number: ROSA General-SFF
Rev: -1A
Date: Thursday, August 15, 2013
Sheet 31 of 51

TBD

<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

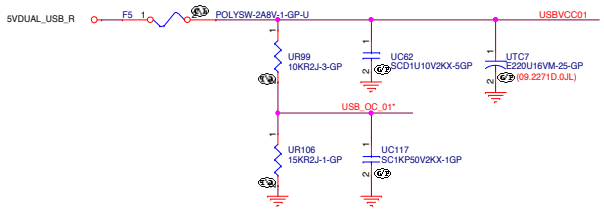
Title: TBD		
Size: A	Document Number: ROSA General-SFF	Rev: -1A
Date: Thursday, August 15, 2013	Sheet 32 of 51	

22 USB_PCH_DN0
22 USB_PCH_DP0
22 USB_PCH_DN1
22,30 USB_PCH_DN11

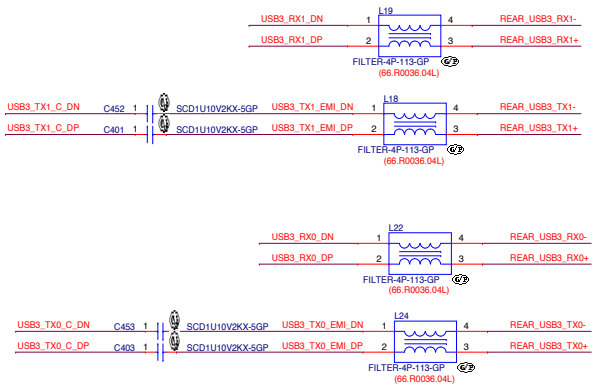
22 USB3_RX1_DN
22 USB3_RX1_DP
22 USB3_TX1_C_DN
22 USB3_TX1_C_DP
22 USB_PCH_DP1

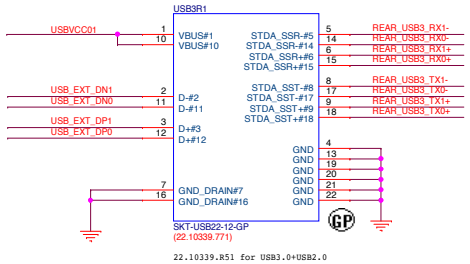
22 USB_OC_01*

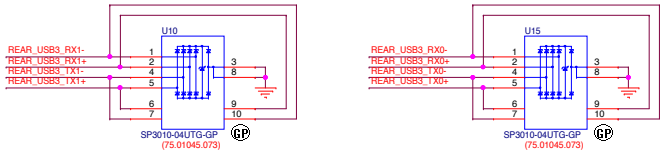
22 USB3_RX0_DN
22 USB3_RX0_DP
22 USB3_TX0_C_DN
22 USB3_TX0_C_DP



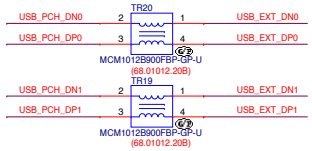
USB 3.0

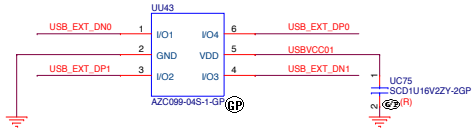






USB 2.0





<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

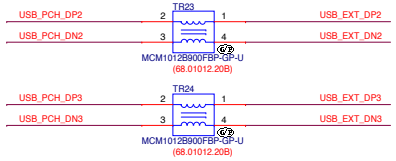
Title: REAR USB3.0

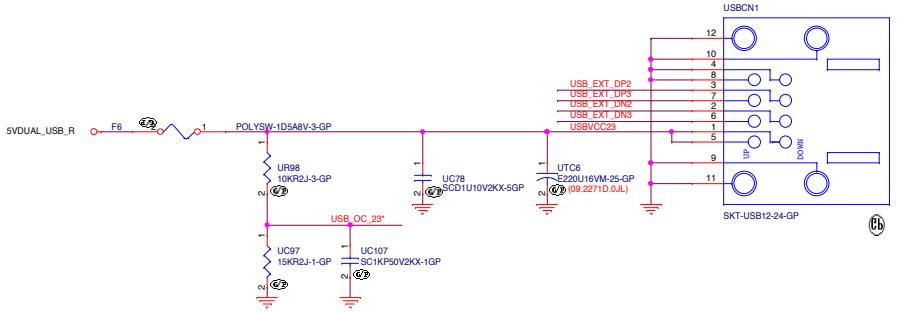
Size	Document Number	Rev
C	ROSA General-SFF	-1A

Date: Thursday, August 15, 2013 Sheet 33 of 51

22 USB_PCH_DP2
22 USB_PCH_DN2
22 USB_PCH_DP3
22 USB_PCH_DN3
22 USB_PCH_DN4
22 USB_PCH_DP4
22 USB_OC_23*
22 USB_OC_45*
19 FB_USBF1_DET

Rear USB 2.0





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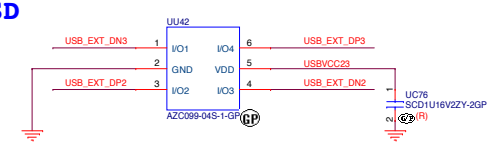
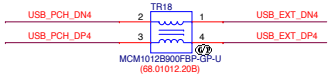
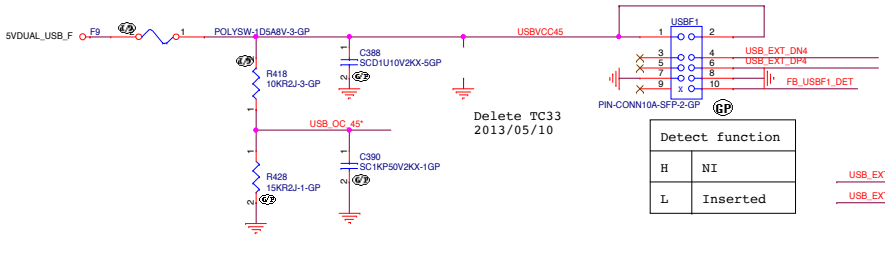
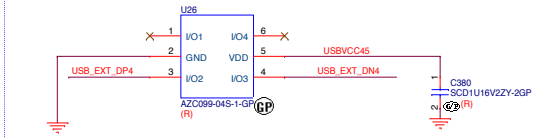


FRONT USB PORT





ESD



<Variant Name>

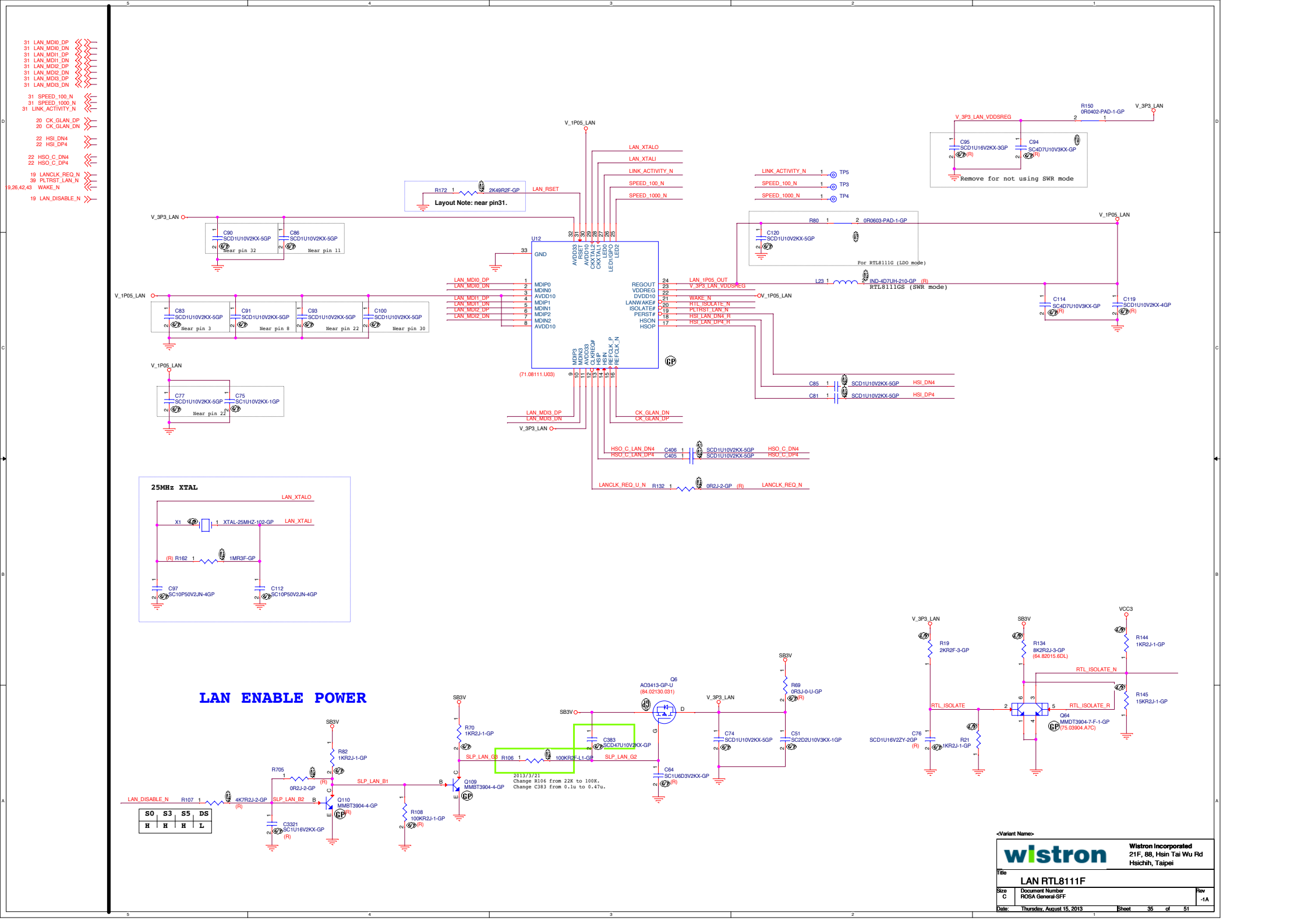
wistron

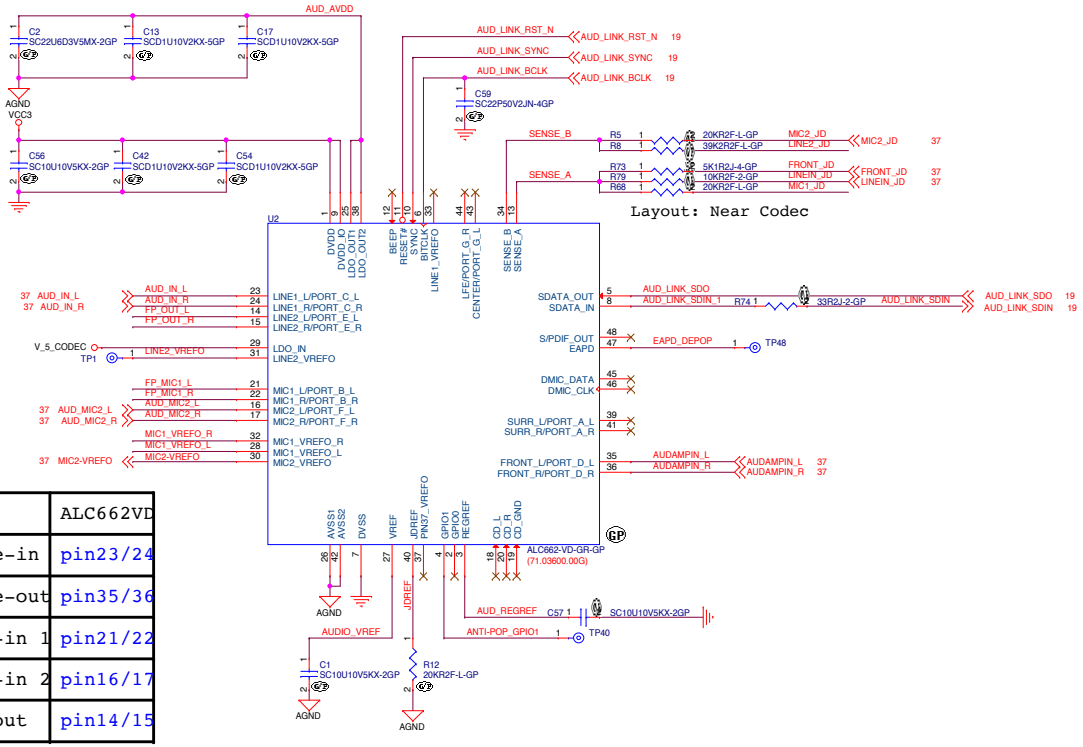
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: USB2.0

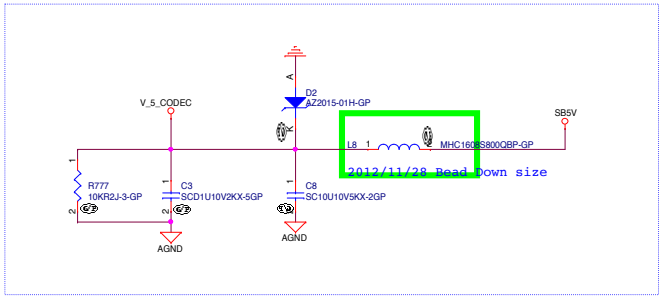
Size	Document Number	Rev
C	ROSA General-SFF	-1A

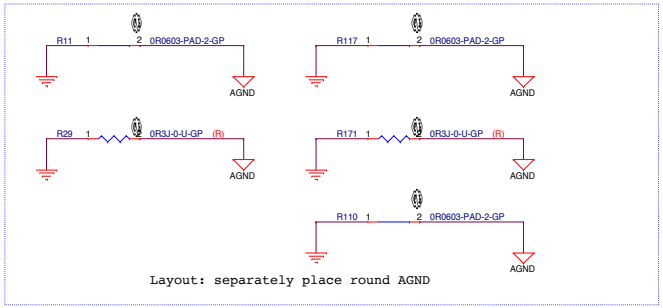
Date: Thursday, August 15, 2013 Sheet 34 of 51


LAN ENABLE POWER
25MHz XTAL
RTL8111GS (SWR mode)
Remove for not using SWR mode
Layout Note: near pin31.
2013/3/21
Change R106 from 22K to 100K.
Change C383 from 0.1u to 0.47u.
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
LAN RTL8111F
Size C
Document Number ROSA General-SFF
Rev -1A
Date: Thursday, August 15, 2013
Sheet 35 of 51

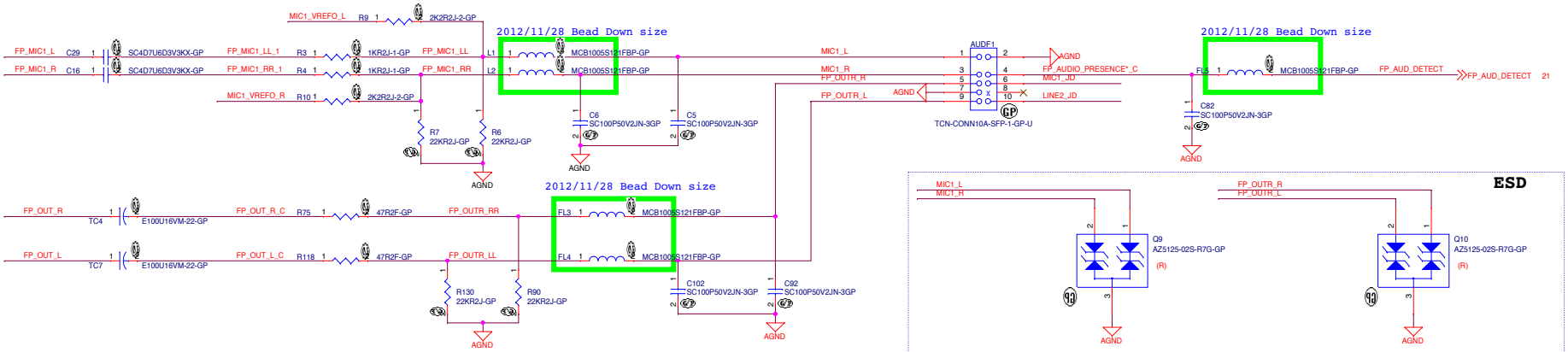


	ALC662VD
Line-in	pin23/24
Line-out	pin35/36
Mic-in 1	pin21/22
Mic-in 2	pin16/17
HP-out	pin14/15





Front Panel



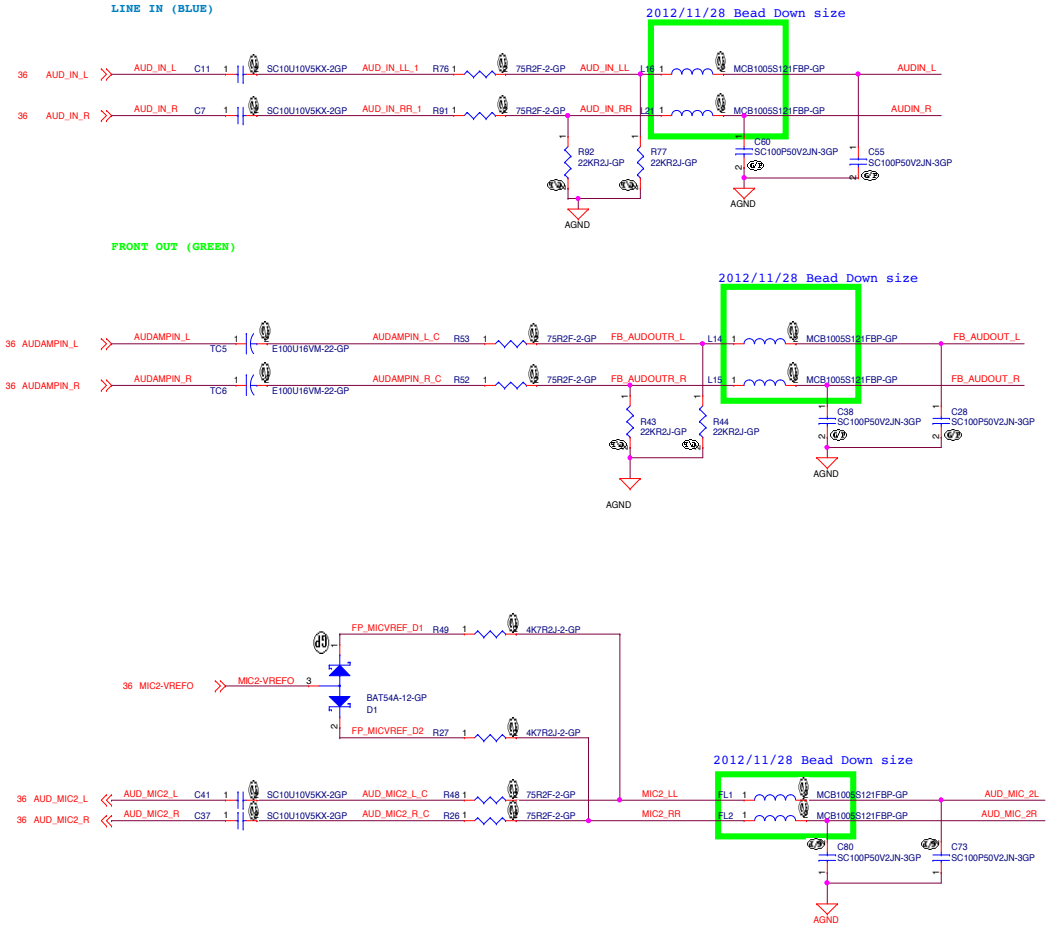
wistron

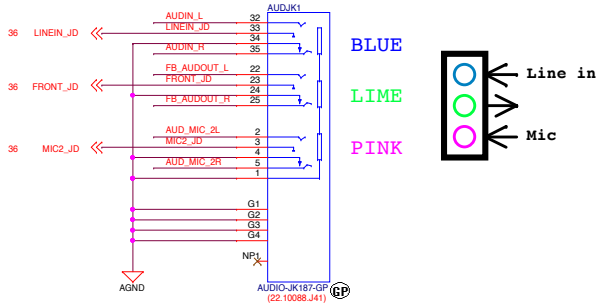
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

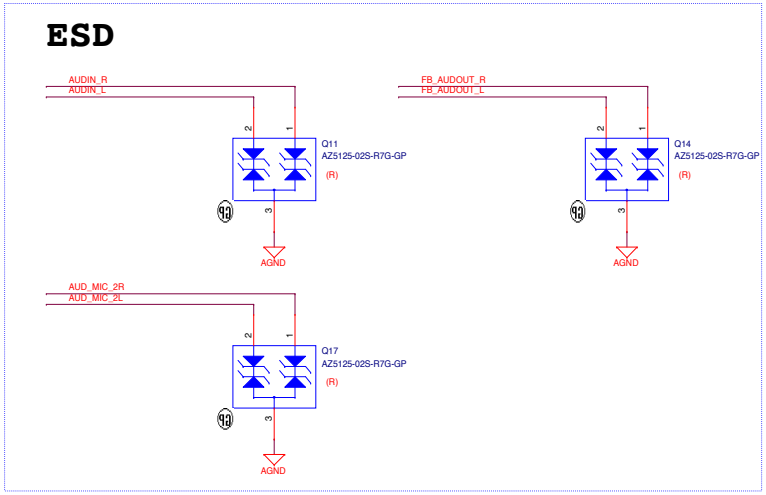
Title: AUDIO_ALC3600

Size: C | Document Number: ROSA General-SFF | Rev: -1A

Date: Thursday, August 15, 2013 | Sheet 36 of 51







<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: AUDIO_JACKS

Size	Document Number	Rev
C	ROSA General-SFF	-1A

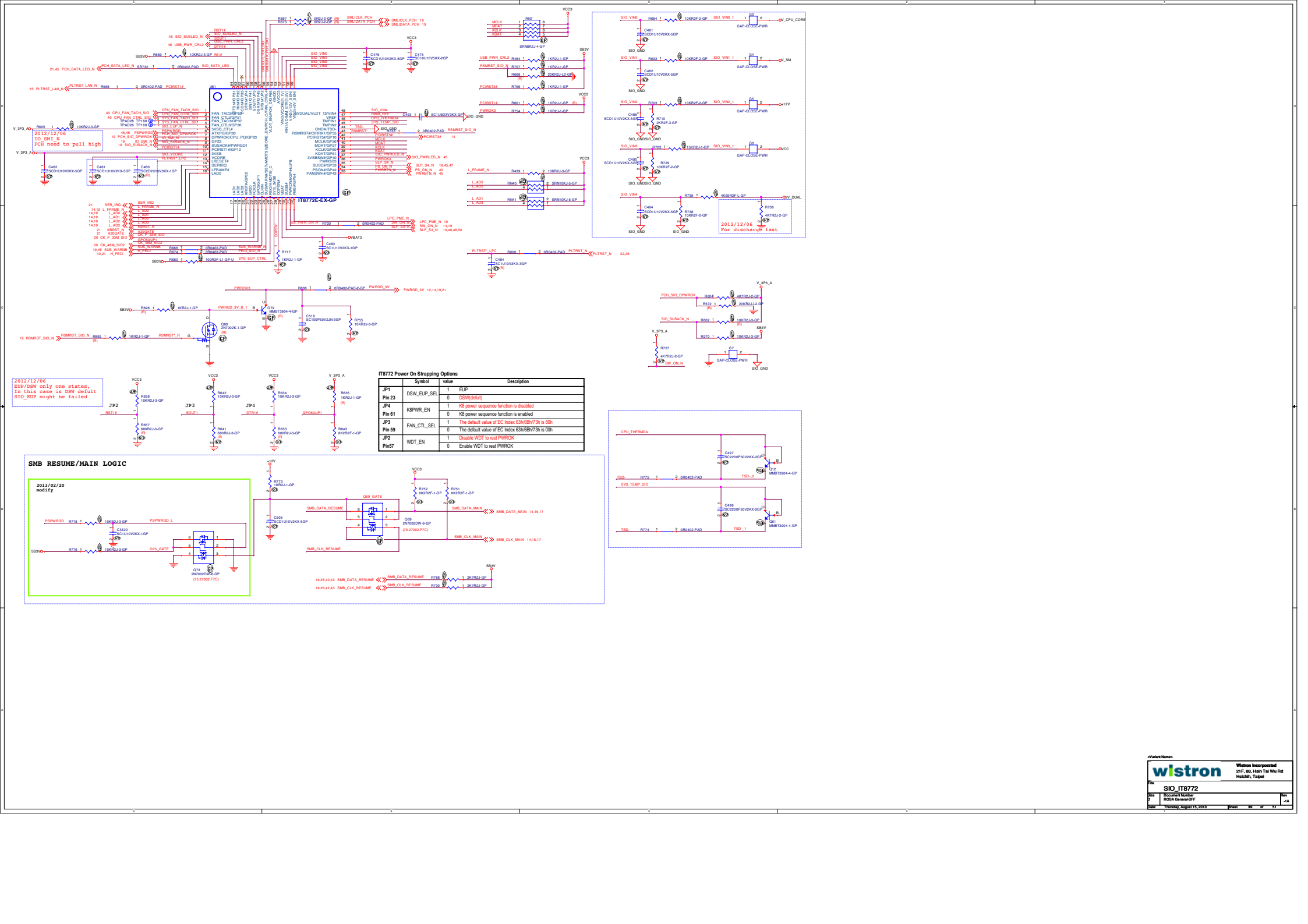
Date: Thursday, August 15, 2013 Sheet 37 of 51

TBD

<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

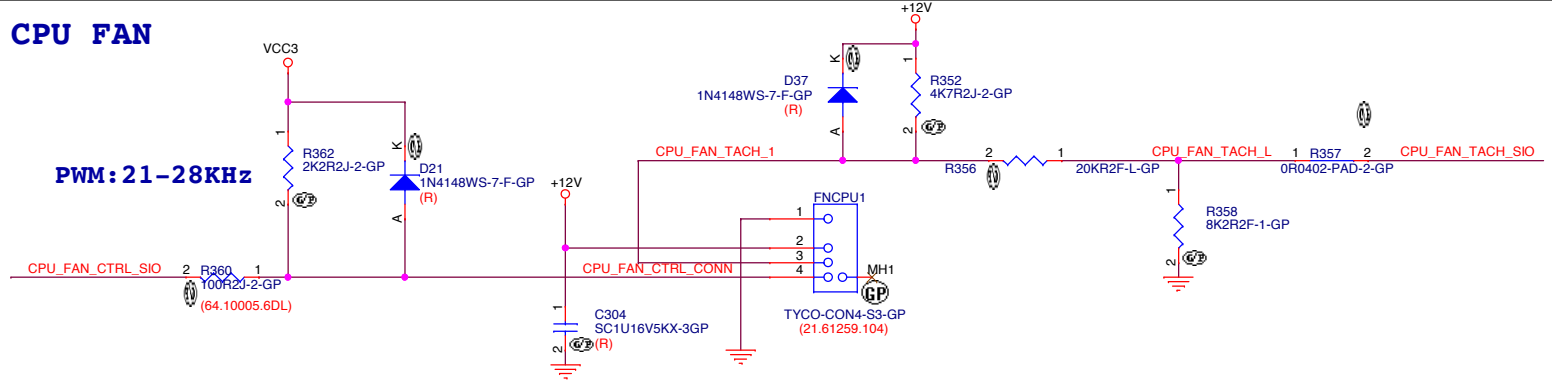
Title: DSW		
Size: A	Document Number: ROSA General-SFF	Rev: -1A
Date: Thursday, August 15, 2013	Sheet 38 of 51	


IT8772E-EX-GP
2012/12/06
IO_SMI_N
PCH need to pull high
2012/12/06
EUP/DSW only one states,
in this case is DSW defult
SIO_EUP might be failed
2012/12/06
For discharge fast
SMB RESUME/MAIN LOGIC
2013/02/20
modify
IT8772 Power On Strapping Options
JP1 DSW_EUP_SEL 1 EUP
Pin 23 0 DSW(defult)
JP4 K8PWR_EN 1 K8 power sequence function is disabled
Pin 61 0 K8 power sequence function is enabled
JP3 FAN_CTL_SEL 1 The default value of EC Index 63h/6Bh/73h is 80h
Pin 59 0 The default value of EC Index 63h/6Bh/73h is 00h
JP2 WDT_EN 1 Disable WDT to rest PWROK
Pin57 0 Enable WDT to rest PWROK
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
SIO_IT8772
Size D
Document Number ROSA General-SFF
Rev -1A
Date: Thursday, August 15, 2013
Sheet 39 of 51

SIO FAN CONTROL

39 CPU_FAN_CTRL_SIO
39 CPU_FAN_TACH_SIO

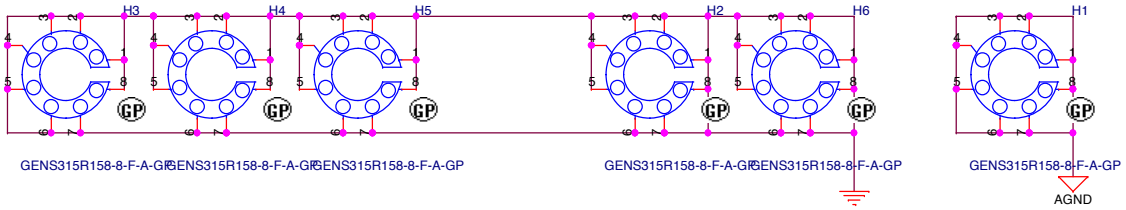
CPU FAN



SYS FAN

2012/12/04 Ryan removed, ME Height filed

PCB MOUNTING HOLES



<Variant Name>

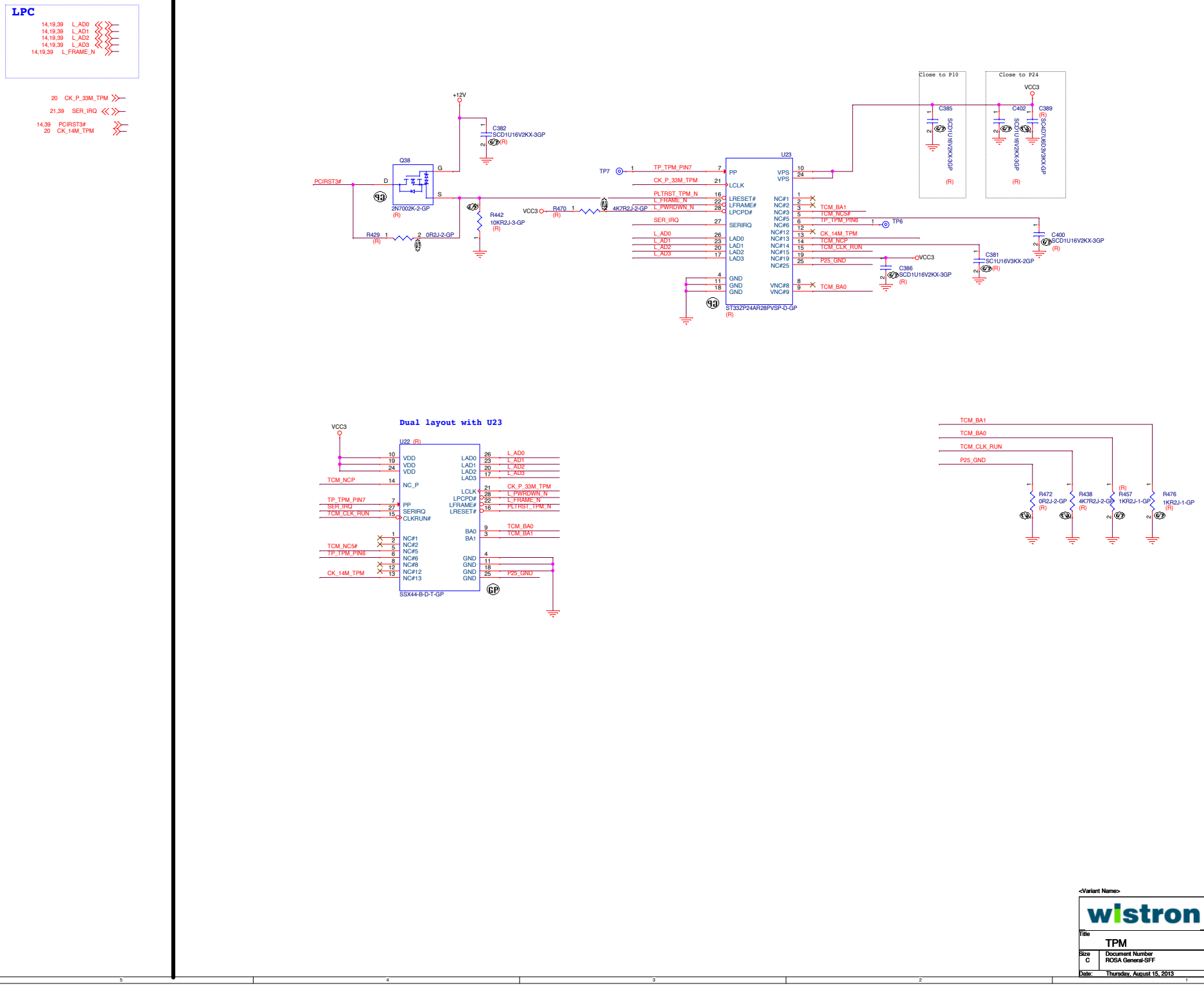
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: FAN CIRCUITS/HOLE

Size	Document Number	Rev
B	ROSA General-SFF	-1A

Date: Thursday, August 15, 2013 Sheet 40 of 51


LPC
14,19,39 L_AD0
14,19,39 L_AD1
14,19,39 L_AD2
14,19,39 L_AD3
14,19,39 L_FRAME_N
20 CK_P_33M_TPM
21,39 SER_IRQ
14,39 PCIRST3#
20 CK_14M_TPM
+12V
C382
SCD1U16V2KX-3GP
(R)
Q38
2N7002K-2-GP
(R)
PCIRST3#
R429
0R2J-2-GP
R442
10KR2J-3-GP
R470
4K7R2J-2-GP
VCC3
TP7
TP_TPM_PIN7
CK_P_33M_TPM
PLTRST_TPM_N
L_FRAME_N
L_PWRDWN_N
SER_IRQ
L_AD0
L_AD1
L_AD2
L_AD3
U23
PP
LCLK
LRESET#
LFRAME#
LPCPD#
SERIRQ
LAD0
LAD1
LAD2
LAD3
GND
VPS
NC#1
NC#2
NC#3
NC#5
NC#6
NC#12
NC#13
NC#14
NC#15
NC#19
NC#25
VNC#8
VNC#9
TCM_BA1
TCM_NCS#
TP_TPM_PIN6
CK_14M_TPM
TCM_NCP
TCM_CLK_RUN
P25_GND
TCM_BA0
ST33ZP24AR28PVSP-D-GP
(R)
TP6
Close to P10
Close to P24
C385
C402
C389
C400
C381
C386
SCD1U16V2KX-3GP
SC1U16V3KX-2GP
SC47U6D3V3KX-GP
Dual layout with U23
U22 (R)
VDD
NC_P
CLKRUN#
NC#1
NC#2
NC#5
NC#6
NC#8
NC#12
NC#13
BA0
BA1
SSX44-B-D-T-GP
R472
R438
R457
R476
0R2J-2-GP
4K7R2J-2-GP
1KR2J-1-GP
(R)
<Variant Name>
wistron
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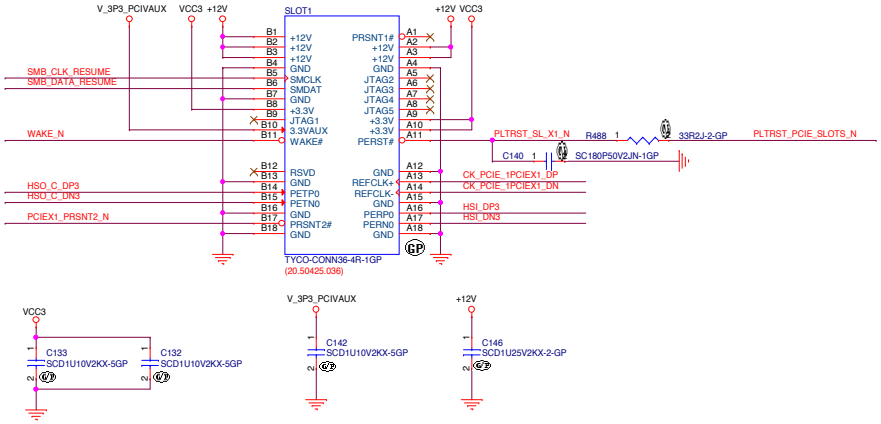
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
TPM
Size C
Document Number
ROSA General-SFF
Rev
-1A
Date: Thursday, August 15, 2013
Sheet 41 of 51

PCIEX1 CONN



22 HSO_C_DP3
22 HSO_C_DN3
22 HSI_DP3
22 HSI_DN3
20 CK_PCIE_1PCIEX1_DP
20 CK_PCIE_1PCIEX1_DN

19,26,39,43 SMB_CLK_RESUME
19,26,39,43 SMB_DATA_RESUME
19,26,35,43 WAKE_N
21 PCIEX1_PRSNT2_N
26,43 PLTRST_PCIE_SLOTS_N

<Variant Name>

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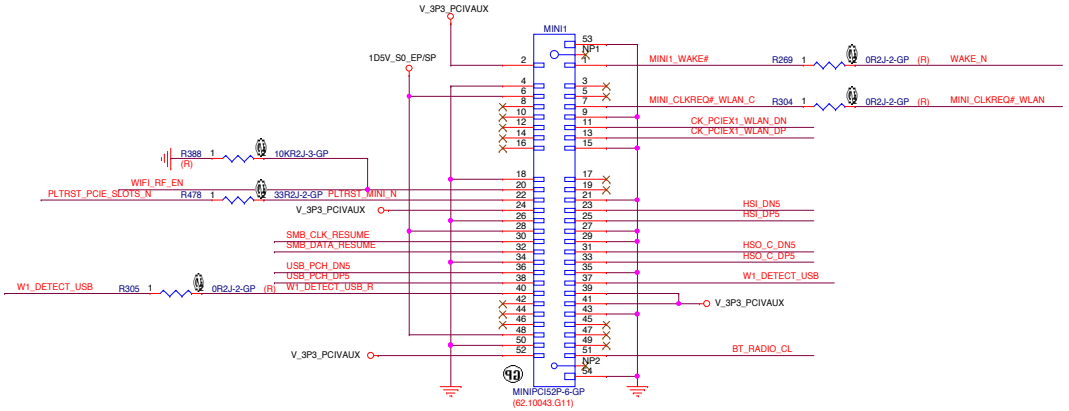
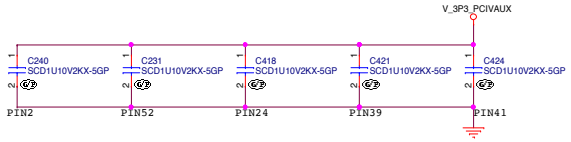
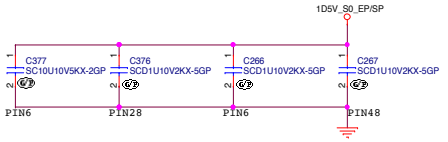
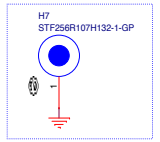
Title	PCIEX1 CONN	
Size C	Document Number ROSA General-SFF	Rev -1A
Date: Thursday, August 15, 2013	Sheet 42 of 51	

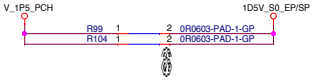
Wireless Card(Present support EP/SP)











19 WIFI_RF_EN
26,42 PLTRST_PCIE_SLOTS_N
19,26,39,42 SMB_CLK_RESUME
19,26,39,42 SMB_DATA_RESUME
22 USB_PCH_DN5
22 USB_PCH_DP5
22 W1_DETECT_USB
22 WAKE_N
19 MINI_CLKREQ#_WLAN
19 CK_PCIEX1_WLAN_DN
26,42 CK_PCIEX1_WLAN_DP
22 HSI_DN5
22 HSI_DP5
19 HSO_C_DN5
26,42 HSO_C_DP5
26,42 BT_RADIO_CL

<Variant Name>

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Title: MINI PCIC SLOT

Size: C | Document Number: ROSA General-SFF | Rev: -1A

Date: Thursday, August 15, 2013 | Sheet 43 of 51

TBD

<Variant Name>

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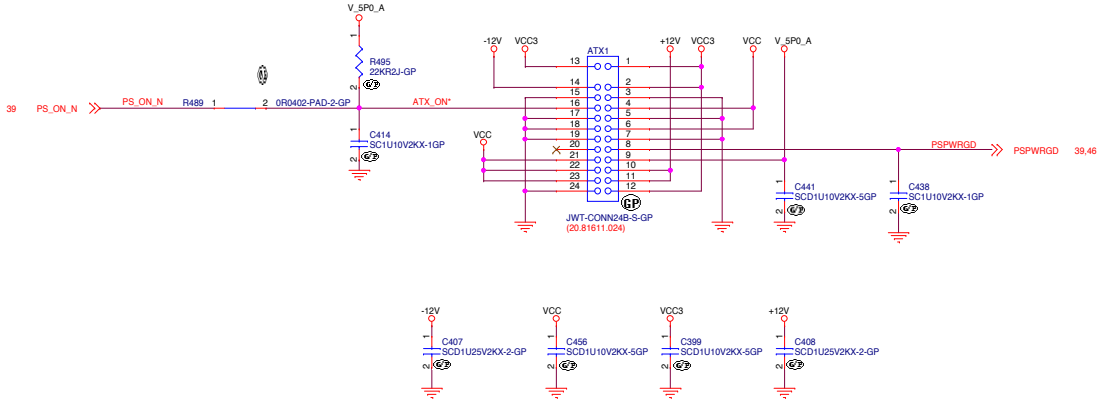
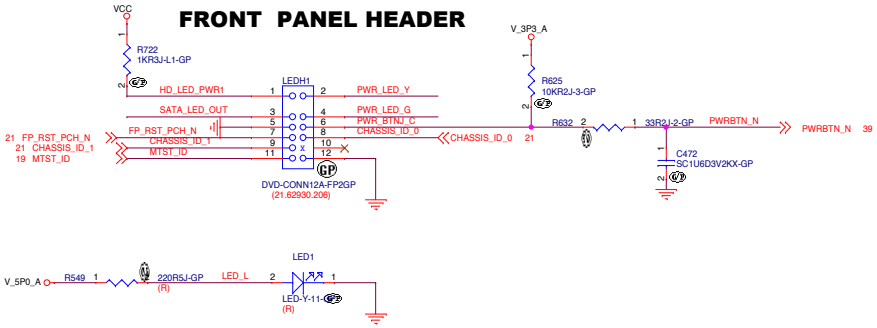
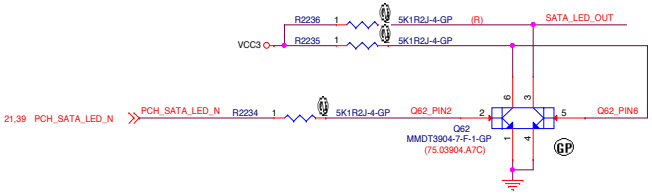
Title	EMC	
Size: A	Document Number: ROSA General-SFF	Rev: -1A
Date: Thursday, August 15, 2013	Sheet 44 of 51	

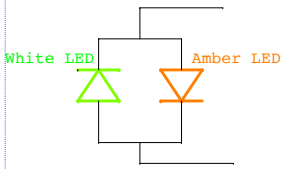
ATX CONNECTOR



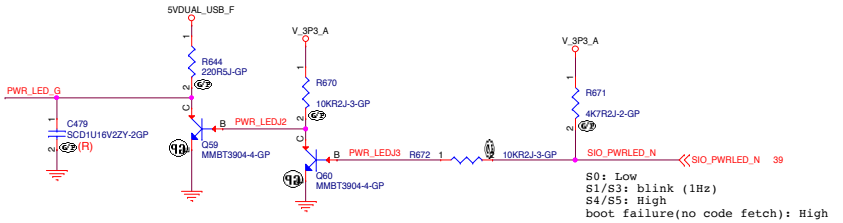
FRONT PANEL HEADER

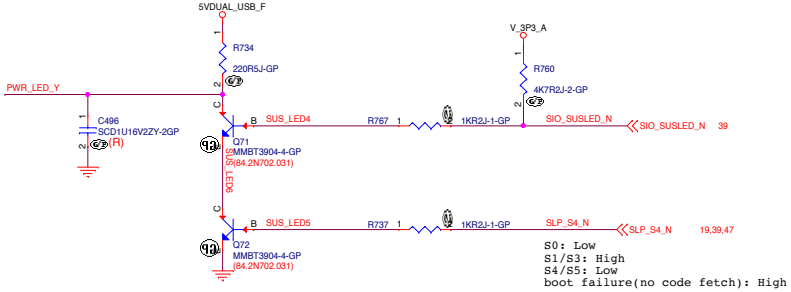






S0	White
S3	Amber
S4	LED off
No Post	Amber
Failure to Post	Amber (blinking)





<Variant Name>

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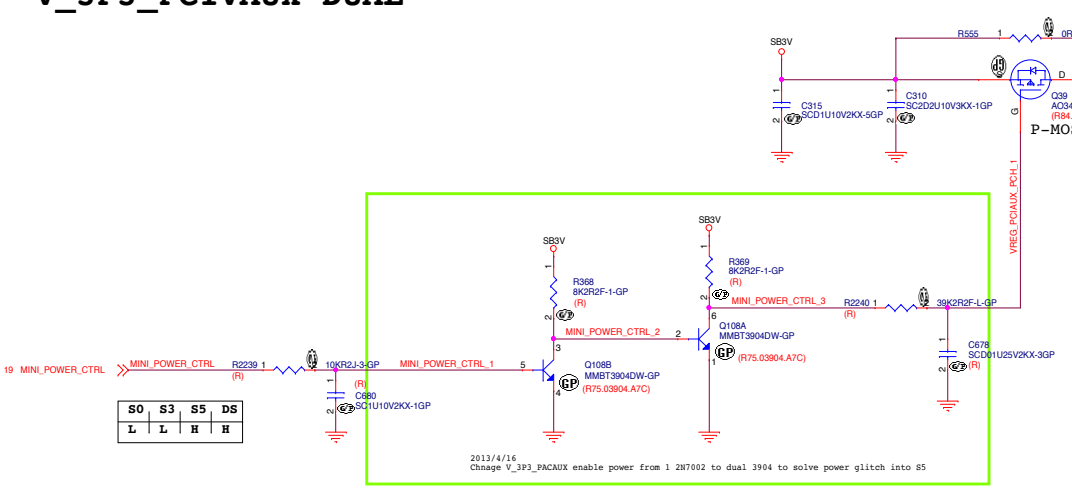
Title: PWR/FNT PNL

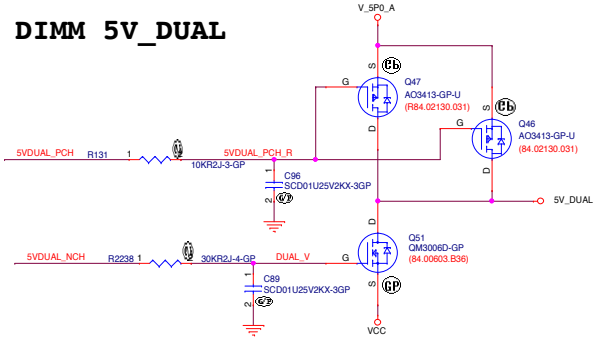
Size	Document Number	Rev
C	ROSA General-SFF	-1A

Date: Thursday, August 15, 2013 Sheet 45 of 51

V_3P3_PCIVAUX DUAL

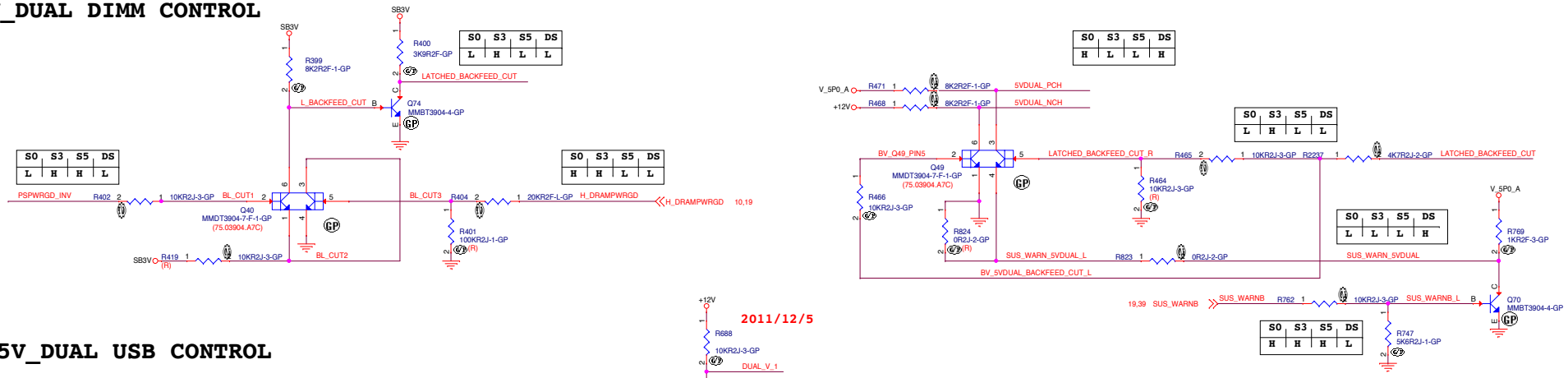


DIMM 5V_DUAL



	S0	S3	S5	DS
5V_DUAL	VCC	V_5P0_A	V_5P0_A	0

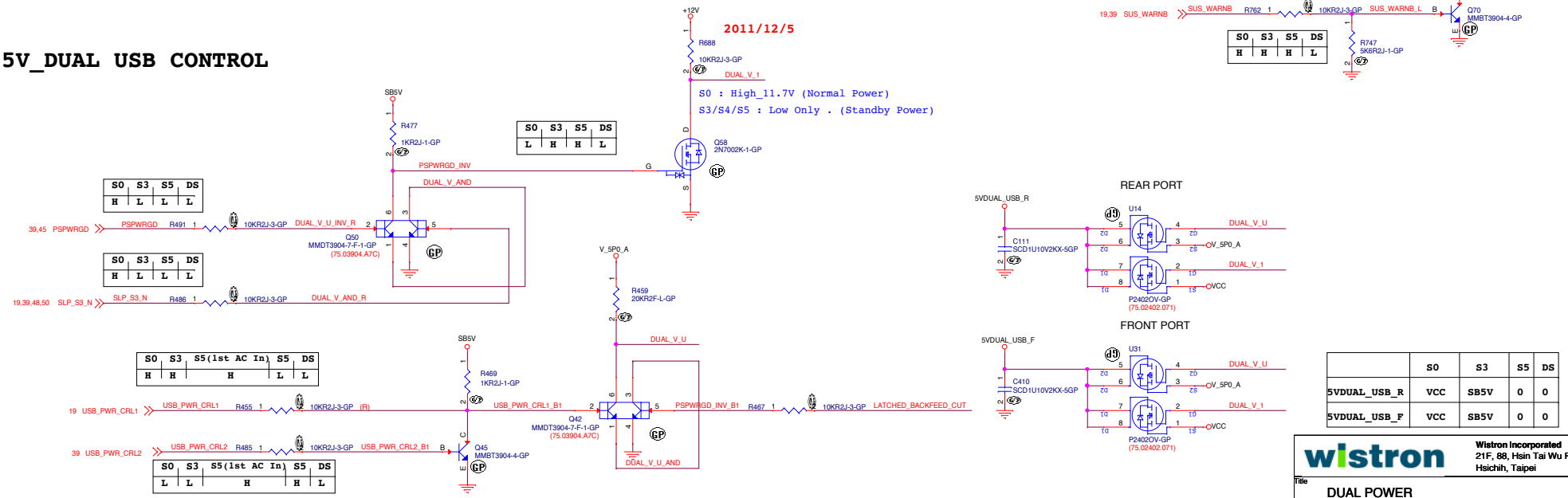
5V_DUAL DIMM CONTROL



5V_DUAL USB CONTROL

2011/12/5

S0 : High_11.7V (Normal Power)
S3/S4/S5 : Low Only . (Standby Power)



	S0	S3	S5	DS
5VDUAL_USB_R	VCC	SB5V	0	0
5VDUAL_USB_F	VCC	SB5V	0	0

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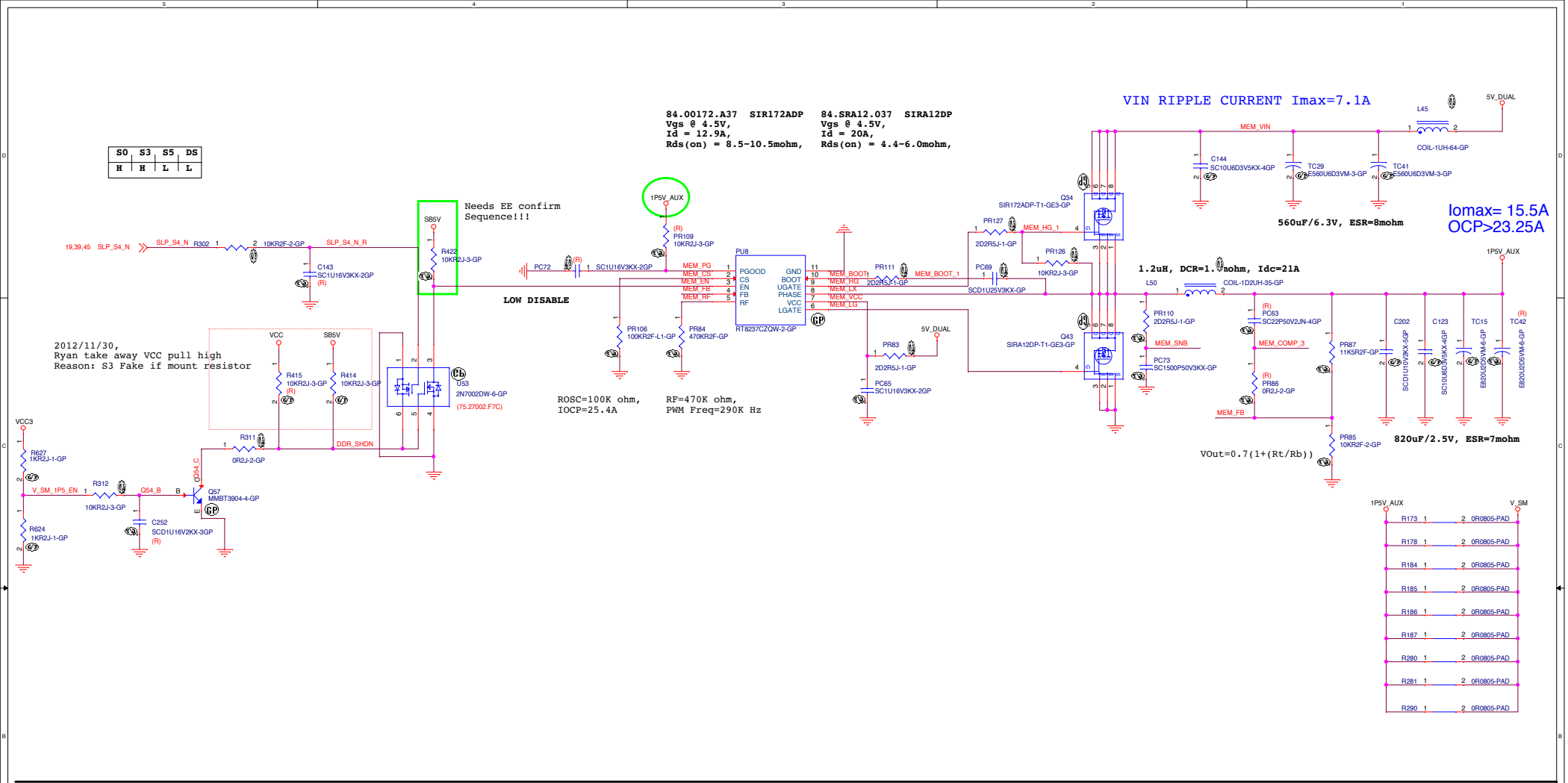
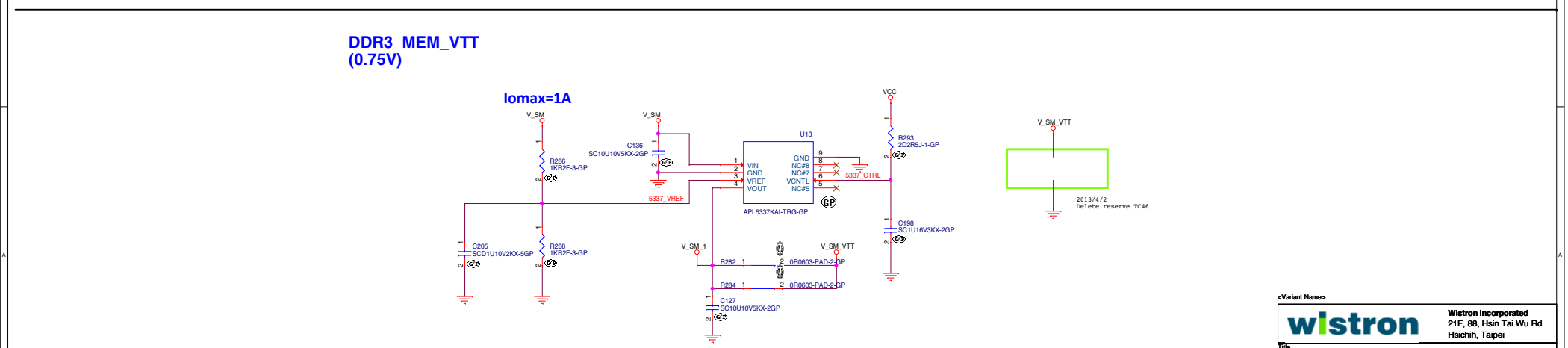
Title: DUAL POWER

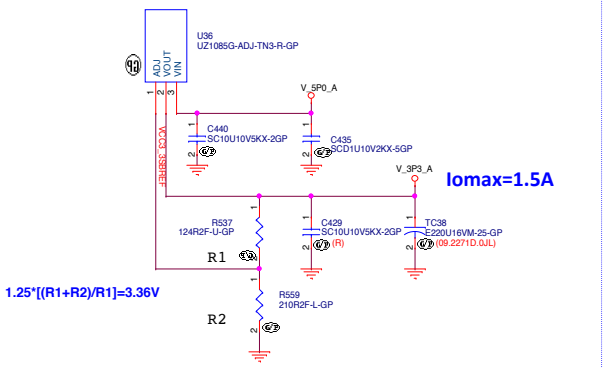
Size: C | Document Number: ROSA General-SFF | Rev: -1A

Date: Thursday, August 15, 2013 | Sheet 46 of 51

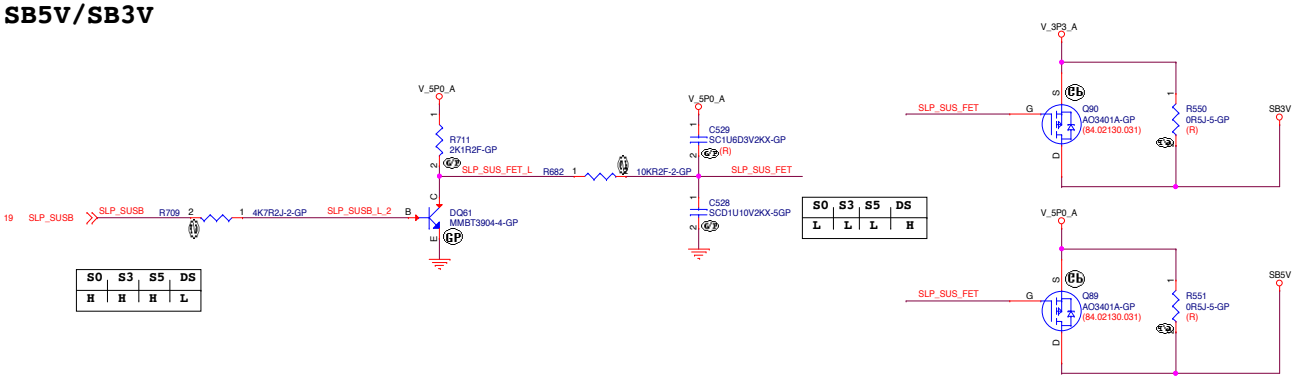

S0 S3 S5 DS
H H L L
84.00172.A37 SIR172ADP
Vgs @ 4.5V,
Id = 12.9A,
Rds(on) = 8.5-10.5mohm,
84.SRA12.037 SIRA12DP
Vgs @ 4.5V,
Id = 20A,
Rds(on) = 4.4-6.0mohm,
VIN RIPPLE CURRENT Imax=7.1A
Needs EE confirm Sequence!!!
LOW DISABLE
2012/11/30,
Ryan take away VCC pull high
Reason: S3 Fake if mount resistor
ROSC=100K ohm,
IOCP=25.4A
RF=470K ohm,
PWM Freq=290K Hz
1.2uH, DCR=1.5mohm, Idc=21A
560uF/6.3V, ESR=8mohm
820uF/2.5V, ESR=7mohm
Iomax= 15.5A
OCP>23.25A
VOut=0.7(1+(Rt/Rb))
RT8237CZQW-2-GP
SIR172ADP-T1-GE3-GP
SIRA12DP-T1-GE3-GP
2N7002DW-6-GP
MMBT3904-4-GP


DDR3 MEM_VTT
(0.75V)
Iomax=1A
APL5337KAI-TRG-GP
2013/4/2
Delete reserve TC46

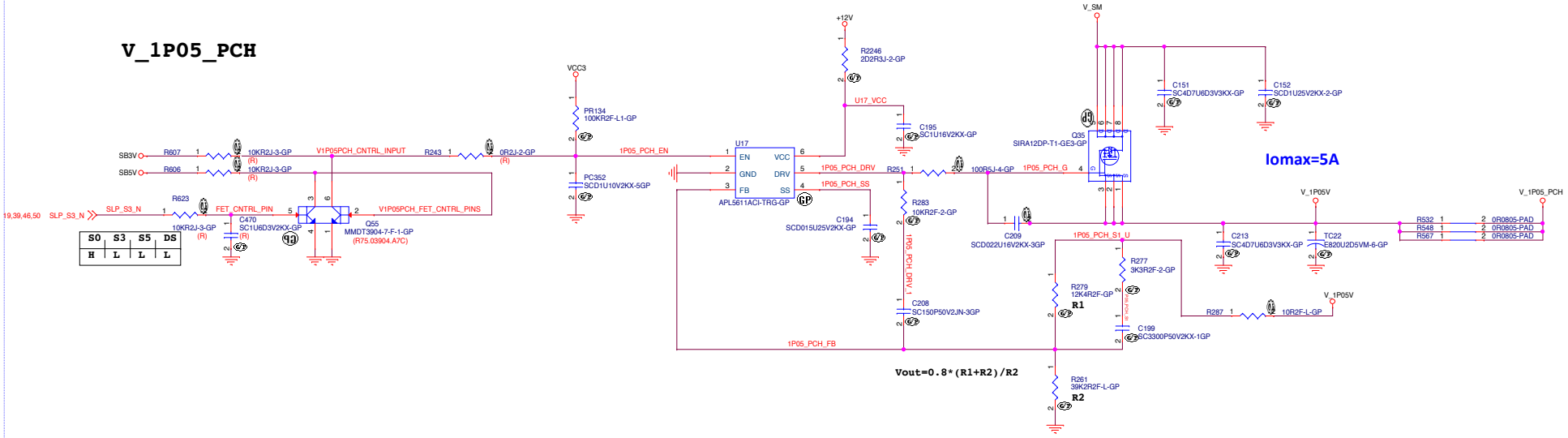
V_3P3_A 1.5A



SB5V/SB3V

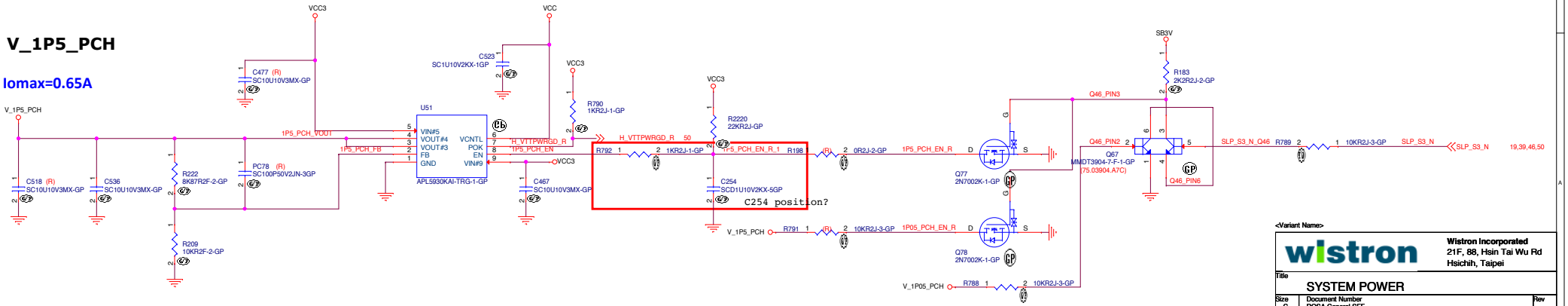


V_1P05_PCH



V_1P5_PCH

Iomax=0.65A



TBD

<Variant Name>

Wistron Incorporated
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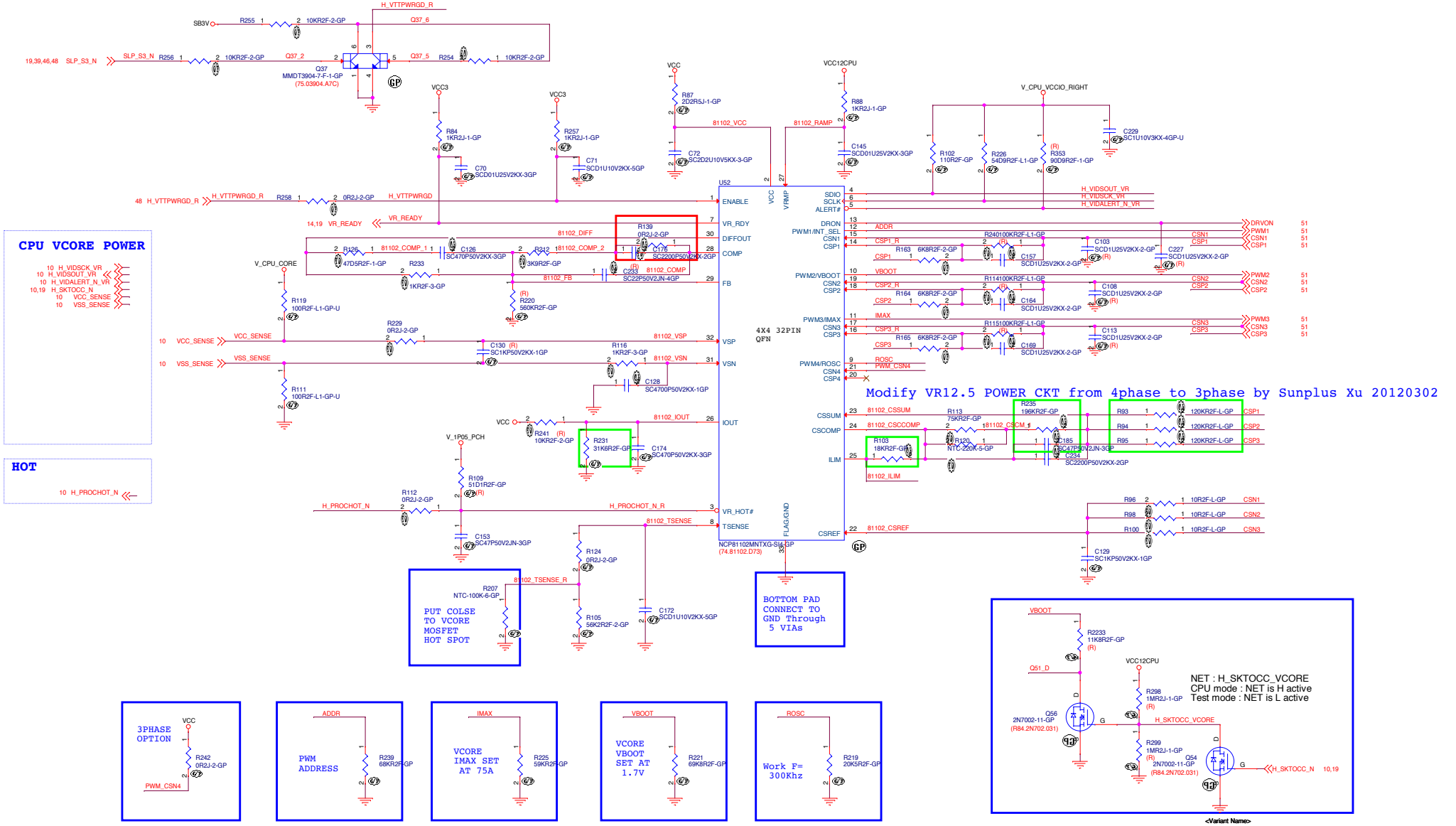
Title: ME POWER		
Size: A	Document Number: ROSA General-SFF	Rev: -1A
Date: Thursday, August 15, 2013	Sheet 49 of 51	

SharkBay VR12.5 POWER CKT - 3 PHASE



<variant_name>

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21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU_VRD 12-5_1

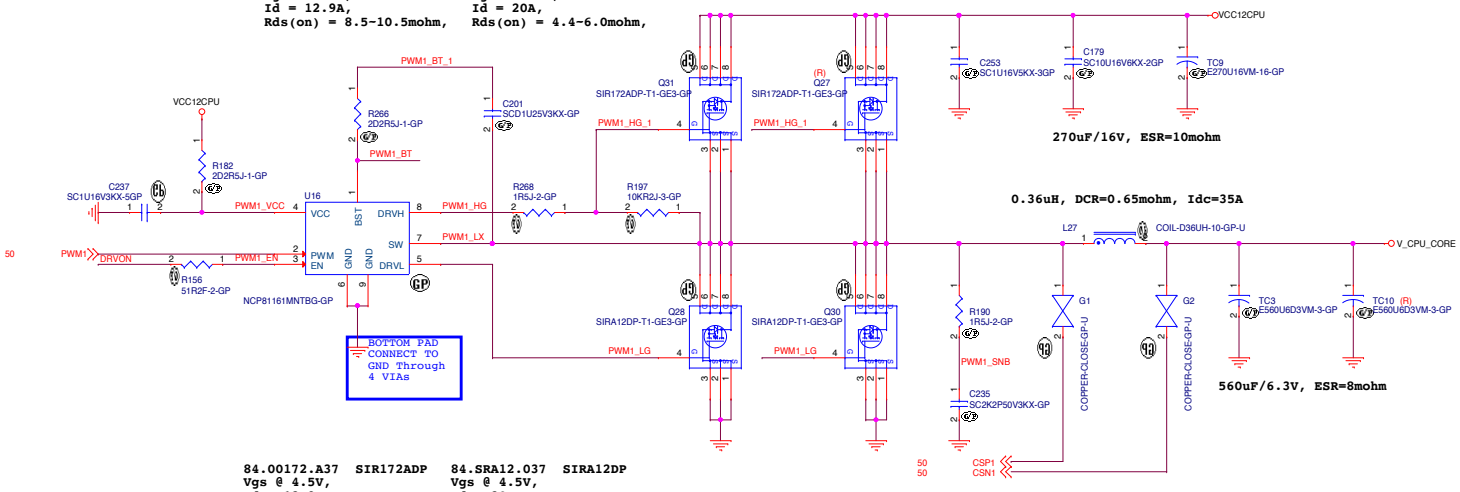
Size: C | Document Number: ROSA General-SFF | Rev: -1A

Date: Thursday, August 15, 2013 | Sheet 50 of 51

84.00172.A37 SIR172ADP
Vgs @ 4.5V,
Id = 12.9A,
Rds(on) = 8.5~10.5mohm,

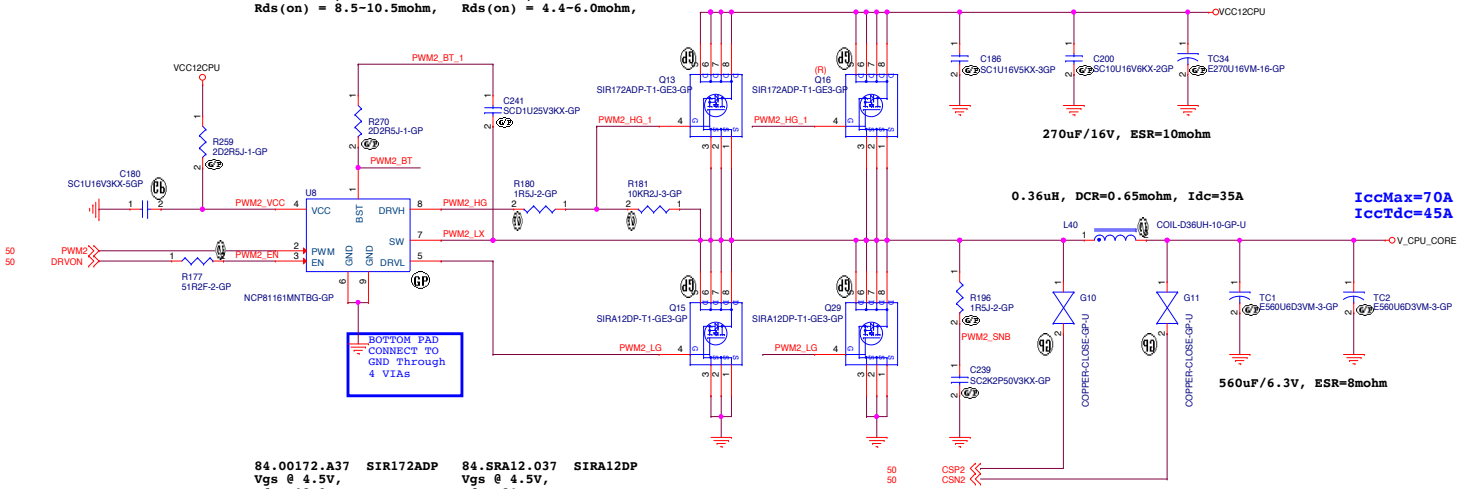
84.SRA12.037 SIRA12DP
Vgs @ 4.5V,
Id = 20A,
Rds(on) = 4.4~6.0mohm,

VIN RIPPLE CURRENT Imax=7.42A



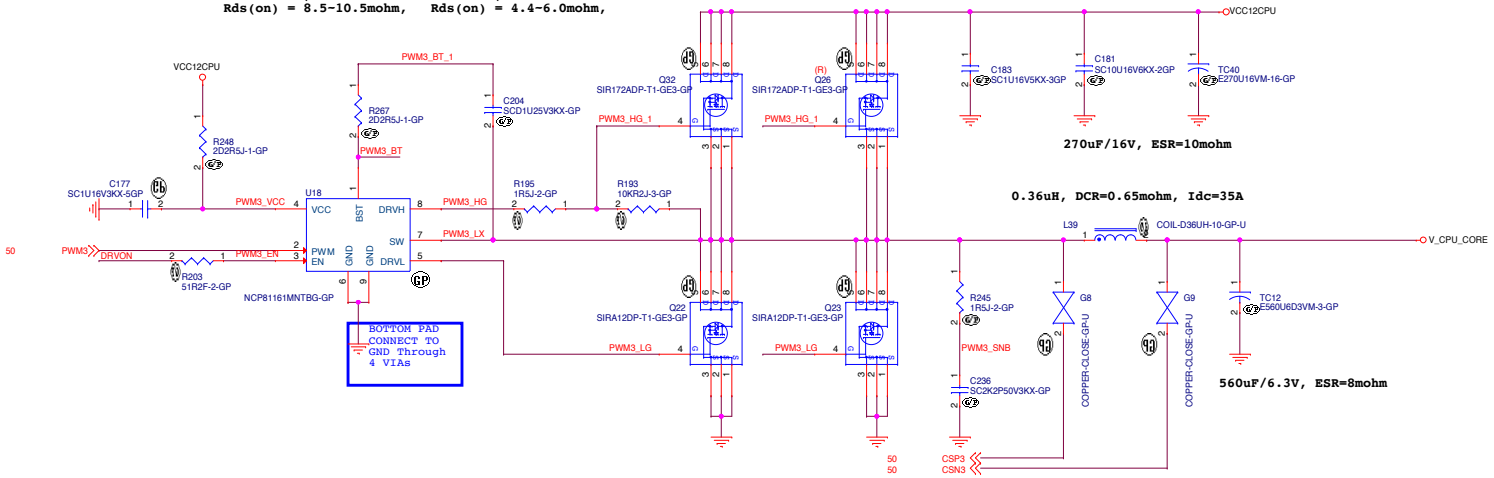
84.00172.A37 SIR172ADP
Vgs @ 4.5V,
Id = 12.9A,
Rds(on) = 8.5~10.5mohm,

84.SRA12.037 SIRA12DP
Vgs @ 4.5V,
Id = 20A,
Rds(on) = 4.4~6.0mohm,



84.00172.A37 SIR172ADP
Vgs @ 4.5V,
Id = 12.9A,
Rds(on) = 8.5~10.5mohm,

84.SRA12.037 SIRA12DP
Vgs @ 4.5V,
Id = 20A,
Rds(on) = 4.4~6.0mohm,



<Variant Name>

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Hsichih, Taipei

Title: CPU_VRD 12-5_2

Size	Document Number	Rev
C	ROSA General-SFF	-1A

Date: Thursday, August 15, 2013 Sheet 51 of 51