Essentials Oak 14 Schematic

Chief River

2012-09-05

REV : A00

DY : None Installed
UMA: UMA only installed
OPS: DISCRTE OPTIMUS installed

M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title		
	Cover Page	
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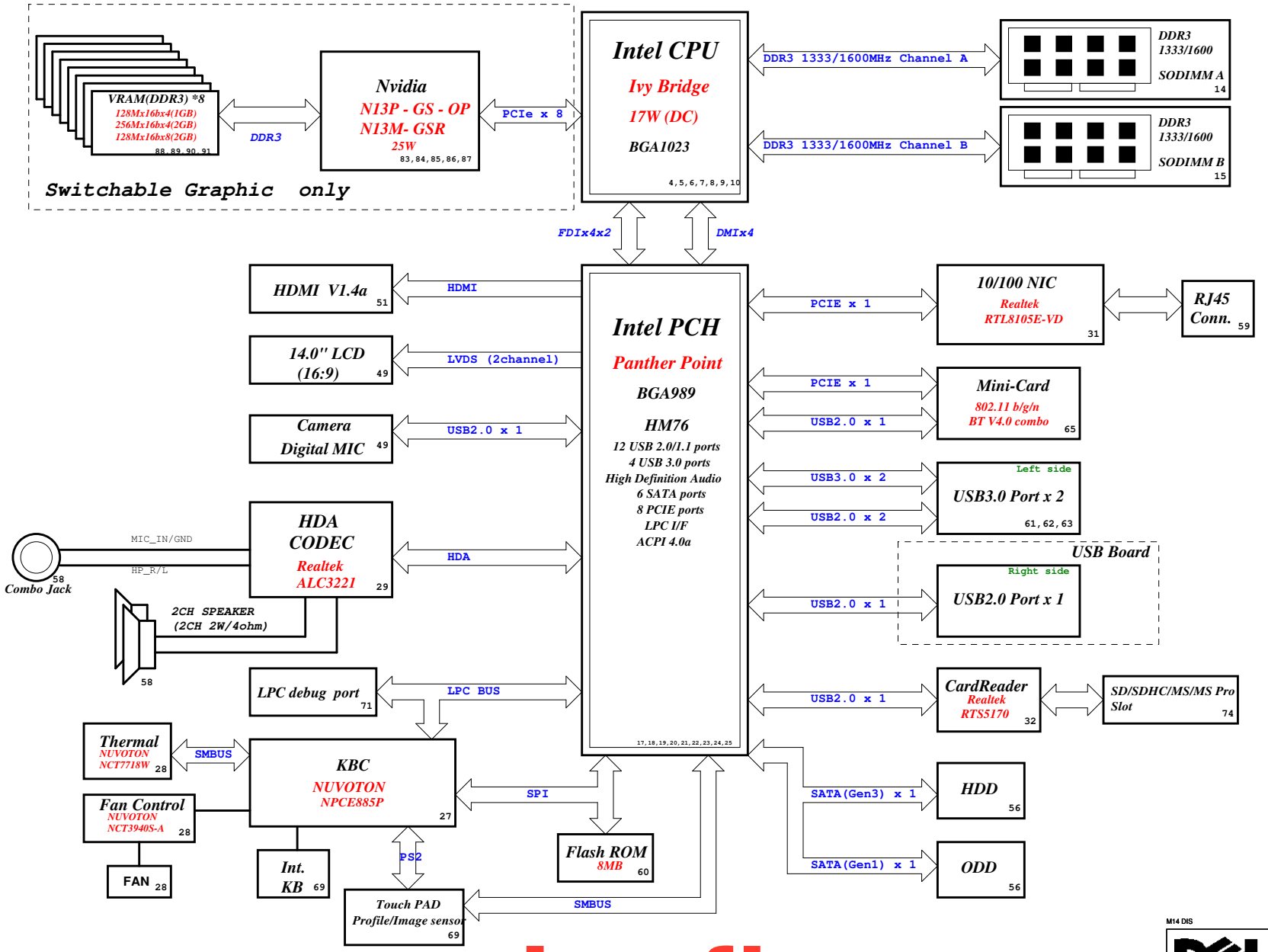
Project code: 91.4WT01.001
91.4XP01.001
PCB P/N : 12204
Revision: A00

Oak14 Block Diagram



CHARGER		
BQ24727		40
INPUTS	OUTPUTS	
AD+ BT+	DCBATOUT	

SYSTEM DC/DC		
TPS51225		41
INPUTS	OUTPUTS	
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5	

CPU Core/NB Power		
ISL95833		42~44
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE VCC_GFXCORE	

DDR3 SUS		
TPS51216		46
INPUTS	OUTPUTS	
DCBATOUT	1D5V_S3	

DDR3 VTT		
TPS51216		46
INPUTS	OUTPUTS	
DCBATOUT	0D75V_S0	

CPU VCCP_CPU		
TPS51219		45
INPUTS	OUTPUTS	
DCBATOUT	1D05V_S0	

Intel PCH 1D8V_S0		
SYW231		47
INPUTS	OUTPUTS	
3D3V_S5	1D8V_S0	

Intel CPU_VCCSA		
TPS51463		48
INPUTS	OUTPUTS	
5V_S5	0D85V_S0	

Nvidia VGA_CORE		
ADP3211MNR2G		92
INPUTS	OUTPUTS	
DCBATOUT	VGA_CORE	

Switches 36 93

INPUTS	OUTPUTS
1D5V_S3	1D5V_S0
5V_S5	5V_S0
3D3V_S5	3D3V_S0
VCCP_CPU	1D05V_VGA_S0
3D3V_S0	3D3V_VGA_S0
1D5V_S3	1D5V_VGA_S0

PCB LAYER

L1:Top	L4:Signal
L2:VCC	L5:GND
L3:Signal	L6:Bottom

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Title: Block Diagram

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PCH Strapping

Chief River Schematic Checklist Revision 1.5

Name	Schematics Notes
SPKR	The signal has a weak internal pull-down. Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the “No Reboot” mode (Panther Point will disable the TCO Timer system reboot feature).
INIT3_3V#	This signal has a weak internal pull-up. Note: The internal pull-up is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled low. Leave as "No Connect".
INTVRMEN	Integrated 1.05 V VRM Enable / Disable. Integrated 1.05 V VRMs is enabled when high NOTE: This signal should always be pulled high External 1.05 V VRM Enable / Disable. Integrated 1.05 V VRMs is enabled when Low. NOTE: This signal should be pulled down to GND through 330 kOhms resistor
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Used as GPIO only. Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail.
DF_TVS	This signal is a strap for selecting DMI and FDI termination voltage. For Ivy Bridge processor only implementation: DF_TVS needs to be pulled up to VccDFTERM power rail through 2.2 kOhms ±5% resistor. For future processor compatibility: It needs to be connected to PROC_SELECT through a 1.0 kOhms ±5% series resistor. The PROC_SELECT signal would need a 2.2 kOhms ±5% pull-up resistor to PCH VccDFTERM.
SATA1GP/ GPIO19	Bit11 Bit 10 Boot BIOS Destination 0 1 Reserved 1 0 PCI 1 1 SPI 0 0 LPC NOTE: If option 00 LPC is selected BIOS may still be placed on LPC, but all platforms with Panther Point require SPI flash connected directly to the Panther Point's SPI bus with a valid descriptor in order to boot. NOTE: Booting to PCI is intended for debut/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GbE LAN. NOTE: PCI Boot BIOS destination is not supported on mobile.
SATA2GP/ GPIO36	Reserved. This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled high when strap is sampled.
SATA3GP/ GPIO37	Reserved This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled high when strap is sampled.
HDA_DOCK_EN# /GPIO33	High Definition Audio Dock Enable: This signal controls the external Intel HD Audio docking isolation logic. This is an active-low-signal. When deasserted the external docking switch is in isolate mode. When asserted the external docking switch electrically connects the IntelR HD Audio dock signals to the corresponding Panther Point signals. This signal can instead be used as GPIO33.
HDA_SDO	Signal has a weak internal pull-down. If strap is sampled low, the security measures defined in the Flash Descriptor will be in effect (default).If sampled high, the Flash Descriptor Security will be overridden. This strap should only be asserted high via external pull-up in manufacturing/debug environments ONLY. Note: The weak internal pull-down is disabled after PLTRST# deasserts. Asserting the HDA_SDO high on the rising edge of PWROK will also halt Intel Management Engine after chipset bring up and disable runtime Intel Management Engine features. This is a debug mode and must not be asserted after manufacturing/ debug.This signal has a 20k internal pull down resistor.
HDA_SYNC	This signal has a weak internal pull-down. On Die PLL VR is supplied by 1.5 V from VCCVRM when sampled high, 1.8 V from VCCVRM when sampled low. Needs to be pulled High for Chief River platform. Note: HDA_SYNC signal also serves as a strap for selecting VRM voltage to the PCH. The strap is sampled on the rising edge of RSMRST# signal. Due to potential leakage on the codec (path to GND), the strap may not be able to achieve the Vihmin at PCH input.Therefore, platform may need to isolate this signal from the codec during the strap phase. Refer to the example circuits provided in the latest Chief River platform design guide.
GPIO15	TLS Confidentiality Low (0) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality This signal has a weak internal pull-down. NOTE:The weak internal pull-down is disabled after RSMRST# deasserts. NOTE: A strong pull-up may be needed for GPIO functionality
L_DDC_DATA	LVDS Detected. When '1'- LVDS is detected; When '0'- LVDS is not detected. This signal has a weak internal pull-down. NOTE:The internal pull-down is disabled after PLTRST# deasserts.
SDVO_CTRLDATA	Port B Detected When '1'- Port B is detected; When '0'- Port B is not detected This signal has a weak internal pull-down. NOTE:The internal pull-down is disabled after PLTRST# deasserts.
DDPC_CTRLDATA	Port C Detected. When '1'- Port C is detected; When '0'- Port C is not detected This signal has a weak internal pull-down. NOTE:The internal pull-down is disabled after PLTRST# deasserts.
DDPD_CTRLDATA	Port D Detected. When '1'- Port D is detected; When '0'- Port D is not detected This signal has a weak internal pull-down. NOTE:The internal pull-down is disabled after PLTRST# deasserts.
GPIO28	The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled.If not used, 8.2-kΩ to 10-kΩ pull-up to +V3.3A power-rail. GPIO28 signal also needs to be pulled up to 3.3V_SUS with 4.7K resistor to ensure proper strap setting when use as the chipset test interface.Refer to the latest platform debug design guide and platform design guide for more details. NOTE:This signal has a weak internal pull-up. The internal pull-up is disabled after RSMRST# deasserts.
GPIO29/ SLP_LAN#	GPIO29 is multiplexed with SLP_LAN#. If Intel LAN is implemented on the platform, SLP_LAN# must be used to control the power to the PHY LAN (no other implementation is supported). If integrated Intel LAN is not supported on the platform, GPIO29 can be used as a normal GPIO. A soft strap determines the functionality of GPIO29, either as SLP_LAN# or GPIO. By default, the soft strap enables SLP_LAN# functionality on the pin. If the soft trap is changed to enable GPIO functionality, then SLP_LAN# functionality is no longer available, and the signal can be used as a normal GPIO (default to GPI).

Processor Strapping

Chief River Schematic Checklist Revision 1.5

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[0]		Connect a series 1 kOhms resistor on the critical CFG[0] trace in a manner which does not introduce any stubs to CFG[0] trace. Route as needed from the opposite side of this series isolation resistor to the debug port. ITP will drive the net to GND.	
CFG[2]	**PCIe Static x16 Lane Numbering Reversal.**	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed	1
CFG[4]	**Display Port Presence strap**	1:Disabled – No Physical Display Port attached to Embedded DisplayPort No connect for disable 0:Enabled – An external Display Port device is connected to the Embedded Display Port Pull-down to GND through a 1kΩ ± 5% resistor to enable port	1
CFG[6:5]	**PCIE Port Bifurcation Straps**	00 = 1 x 8, 2 x 4 PCI Express 01 = reserved 10 = 2 x 8 PCI Express 11 = 1 x 16 PCI Express	1
CFG[17:7]	**Reserved configuration lands. A test point may be placed on the board for these lands.**		

Power Plane

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 – 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

Sandy Bridge + Ivy Bridge Compatibility Requirements

Chief River Schematic Checklist Revision 1.5

Pin Name	Configuration	Schematic Notes
DDR3 VREF	**Sandy Bridge + Ivy Bridge**	DDR3 VREF M1 and M3 Guidelines are required. Note: The M3 traces are routed to the Sandy Bridge Processor reserved pins.
	Ivy Bridge	No change.
PROC_SELECT# & DF_TVS	**Sandy Bridge + Ivy Bridge**	Connect DF_TVS signal of the PCH to PROC_SELECT# of the processor through a 1K±5% series resistor. PROC_SELECT# also needs a 2.2K±5% pull up resistor to PCH VccDFTERM rail.
	Ivy Bridge	No change.
VCCIO VR Implementation	**Sandy Bridge + Ivy Bridge**	The POR for Ivy Bridge mobile parts is now 1.05 V. There is no longer a requirement for a separate VCCIO VR for Sandy Bridge + Ivy Bridge compatibility.
	Ivy Bridge	No change.
VCCSA_SEL connection to VCCSA_VID[1:0] lines	**Sandy Bridge + Ivy Bridge**	VCCSA_SELECT[0:1] which should be connected to VID[1:0] of the System Agent (SA) VR controller.
	Ivy Bridge	No change.
Layout Requirement on PCI Express Gen3	**Sandy Bridge + Ivy Bridge**	The total motherboard length for a pair of consecutive PCI Express Tx lanes be length matched within 100 mils (2.54 mm)
	Ivy Bridge	No change.
GT Core VR Implementation	**Sandy Bridge + Ivy Bridge**	Depending on the PDDG specifications, some IVB GT2 SKUs may require a new VR controller and 2 phase VCC GT core VR.
	Ivy Bridge	No change.
Processor PCI Express Graphics Guidelines	**Sandy Bridge + Ivy Bridge (PCIe Gen3):**	To support Gen 3 PCI Express Graphic, the value of the AC coupling capacitor should be 180 – 265 nF.
	Ivy Bridge	No change.

PCIE Routing

LANE1	X
LANE2	X
LANE3	Mini Card1(WLAN)
LANE4	x
LANE5	X
LANE6	Onboard LAN
LANE7	X
LANE8	X

USB Table

Pair	Device
0	USB3.0 port1
1	USB3.0 port2, with Debug Port
2	USB2.0 port3
3	X
4	X
5	Touch Panel
6	HM76 NC
7	HM76 NC
8	X
9	X
10	CARD READER
11	Mini Card (WLAN)
12	X
13	CAMERA

SATA Table

SATA	
Pair	Device
0	HDD1
1	X
2	X
3	X
4	ODD1
5	X

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SSID = CPU

Layout Note:
Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

Layout Note:
DMI trace length 2000~8000mil

Layout Note:
FDI trace length 2000~6500mil

Layout Note:
Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

CPU1A — 1 OF 9

DMI_CPU_RXN_PCH_TXN[3:0] → DMI_RX#0..3 (M2, P6, P1, P10)
DMI_CPU_RXP_PCH_TXP[3:0] → DMI_RX0..3 (N3, P7, P3, P11)
DMI_CPU_TXN_PCH_RXN[3:0] → DMI_TX#0..3 (K1, M8, N4, R2)
DMI_CPU_TXP_PCH_RXP[3:0] → DMI_TX0..3 (K3, M7, P4, T3)

FDI_CPU_TXN_PCH_RXN[7:0] → FDI0_TX#0..3, FDI1_TX#0..3 (U7, W11, W1, AA6, W6, V4, Y2, AC9)
FDI_CPU_TXP_PCH_RXP[7:0] → FDI0_TX0..3, FDI1_TX0..3 (U6, W10, W3, AA7, W7, T4, AA3, AC8)

FDI_FSYNC0 (AA11), FDI_FSYNC1 (AC12) → FDI0_FSYNC, FDI1_FSYNC
FDI_INT (U11) → FDI_INT
FDI_LSYNC0 (AA10), FDI_LSYNC1 (AG8) → FDI0_LSYNC, FDI1_LSYNC

VCCP_CPU — R402 1 — 24D9R2F-L-GP — DP_COMP (AF3)

EDP_COMPIO (AD2), EDP_ICOMPO (AG11), EDP_HPD# (AG4), EDP_AUX# (AF4), EDP_AUX (AC3), EDP_TX#0..3 (AC4, AE11, AE7), EDP_TX0..3 (AC1, AA4, AE10, AE6)

IVY-BRIDGE-GP-NF
71.00IVY.A0U

DMI | Intel(R) FDI | eDP | PCI EXPRESS -- GRAPHICS

VCCP_CPU — R401 1 — 24D9R2F-L-GP — PEG_IRCOMP_R (G3)
PEG_ICOMPI (G1), PEG_ICOMPO (G4), PEG_RCOMPO

PEG_RX#0..15 (H22, J21, B22, D21, A19, D17, B14, D13, A11, B10, G8, A8, B6, H8, E5, K7)
CPU_RXN_C_dGPU_TXN7..0

PEG_RX0..15 (K22, K19, C21, D19, C19, D16, C13, D12, C11, C9, F8, C8, C5, H6, F6, K6)
CPU_RXP_C_dGPU_TXP7..0

CPU_RXN_C_dGPU_TXN[7..0] 83
CPU_RXP_C_dGPU_TXP[7..0] 83
dGPU_RXN_C_CPU_TXN[8..15] 83
dGPU_RXP_C_CPU_TXP[8..15] 83

PEG_TX#0..15 (G22, C23, D23, F21, H19, C17, K15, F17, F14, A15, J14, H13, M10, F10, D9, J4)
CPU_TXN_dGPU_RXN7..0

C401	SCD22U10V2KX-1GP	CPU_TXN_dGPU_RXN7	dGPU_RXN_C_CPU_TXN8
C402	SCD22U10V2KX-1GP	CPU_TXN_dGPU_RXN6	dGPU_RXN_C_CPU_TXN9
C403	SCD22U10V2KX-1GP	CPU_TXN_dGPU_RXN5	dGPU_RXN_C_CPU_TXN10
C404	SCD22U10V2KX-1GP	CPU_TXN_dGPU_RXN4	dGPU_RXN_C_CPU_TXN11
C405	SCD22U10V2KX-1GP	CPU_TXN_dGPU_RXN3	dGPU_RXN_C_CPU_TXN12
C406	SCD22U10V2KX-1GP	CPU_TXN_dGPU_RXN2	dGPU_RXN_C_CPU_TXN13
C407	SCD22U10V2KX-1GP	CPU_TXN_dGPU_RXN1	dGPU_RXN_C_CPU_TXN14
C408	SCD22U10V2KX-1GP	CPU_TXN_dGPU_RXN0	dGPU_RXN_C_CPU_TXN15

PEG_TX0..15 (F22, A23, D24, F21, G19, B18, K17, G17, F14, C15, K13, G13, K10, G10, D8, K4)
CPU_TXP_dGPU_RXP7..0

C409	SCD22U10V2KX-1GP	CPU_TXP_dGPU_RXP7	dGPU_RXP_C_CPU_TXP8
C410	SCD22U10V2KX-1GP	CPU_TXP_dGPU_RXP6	dGPU_RXP_C_CPU_TXP9
C411	SCD22U10V2KX-1GP	CPU_TXP_dGPU_RXP5	dGPU_RXP_C_CPU_TXP10
C412	SCD22U10V2KX-1GP	CPU_TXP_dGPU_RXP4	dGPU_RXP_C_CPU_TXP11
C413	SCD22U10V2KX-1GP	CPU_TXP_dGPU_RXP3	dGPU_RXP_C_CPU_TXP12
C414	SCD22U10V2KX-1GP	CPU_TXP_dGPU_RXP2	dGPU_RXP_C_CPU_TXP13
C415	SCD22U10V2KX-1GP	CPU_TXP_dGPU_RXP1	dGPU_RXP_C_CPU_TXP14
C416	SCD22U10V2KX-1GP	CPU_TXP_dGPU_RXP0	dGPU_RXP_C_CPU_TXP15

GP Note:
PEG with reversal type.

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Title	CPU(PCIE/DMI/FDI)	
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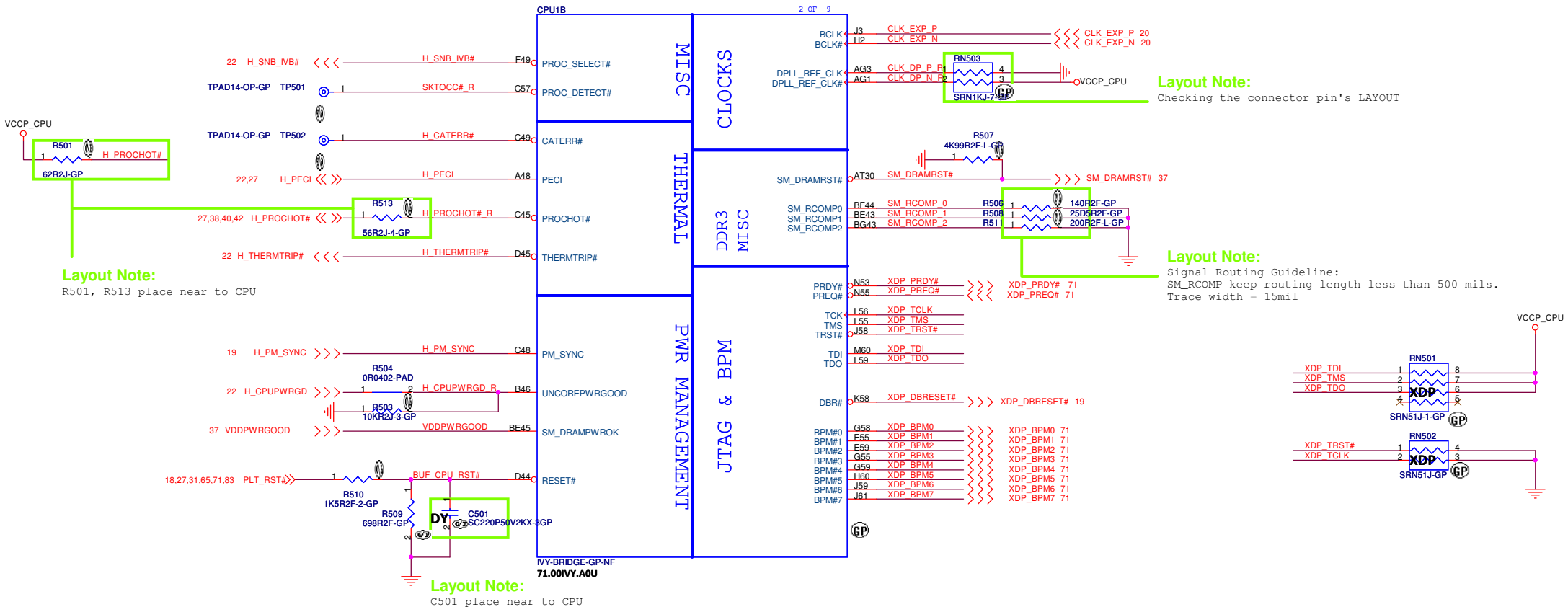
SSID = CPU

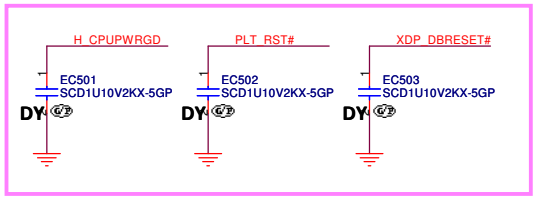


Layout Note:
R501, R513 place near to CPU

Layout Note:
C501 place near to CPU

Layout Note:
Checking the connector pin's LAYOUT

Layout Note:
Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.
Trace width = 15mil



reserve for EMI Request

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Title: **CPU(THERMAL/CLOCK/PM)**

Size	Document Number	Rev
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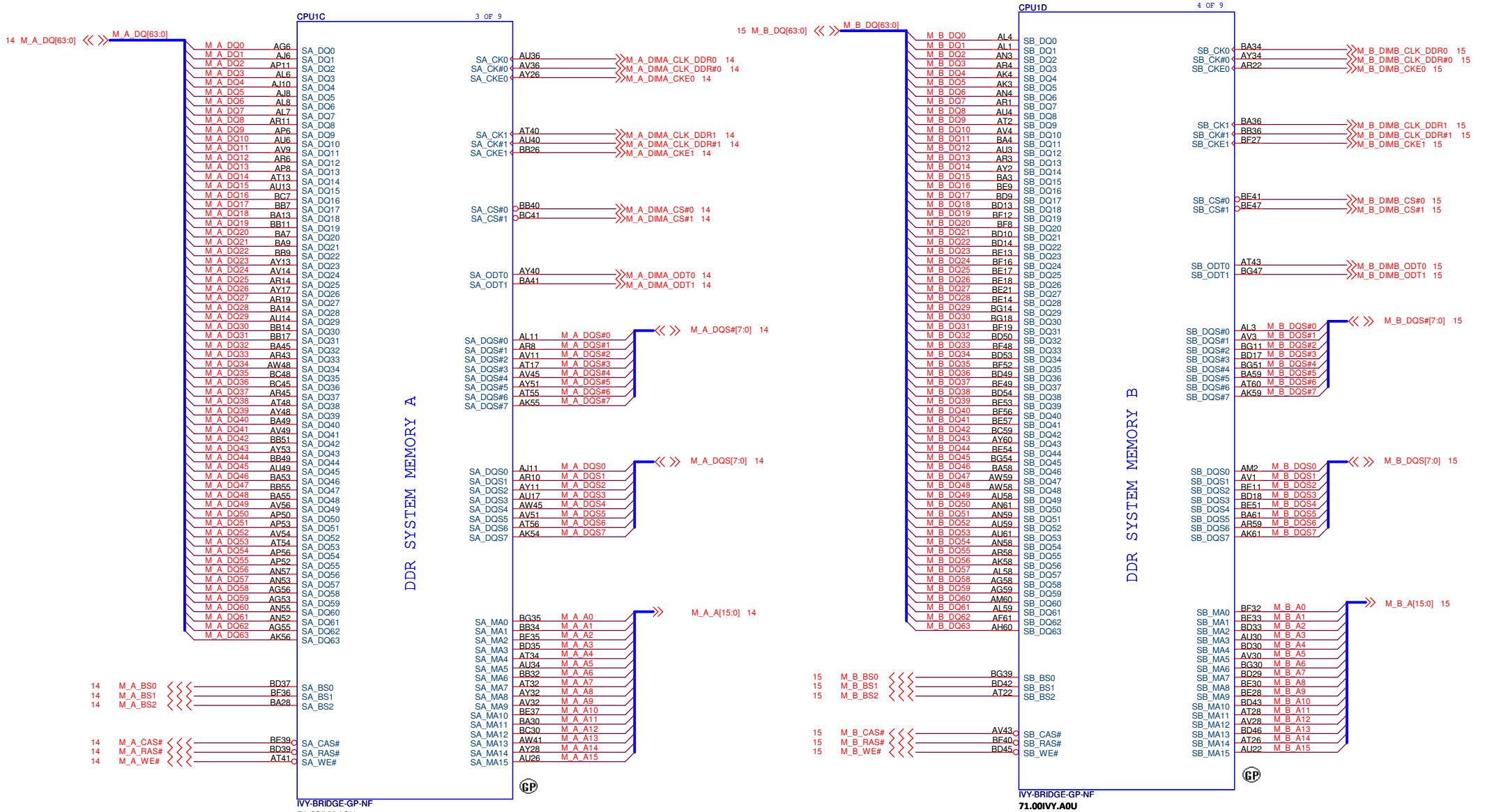
SSID = CPU



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Title: CPU (DDR)		
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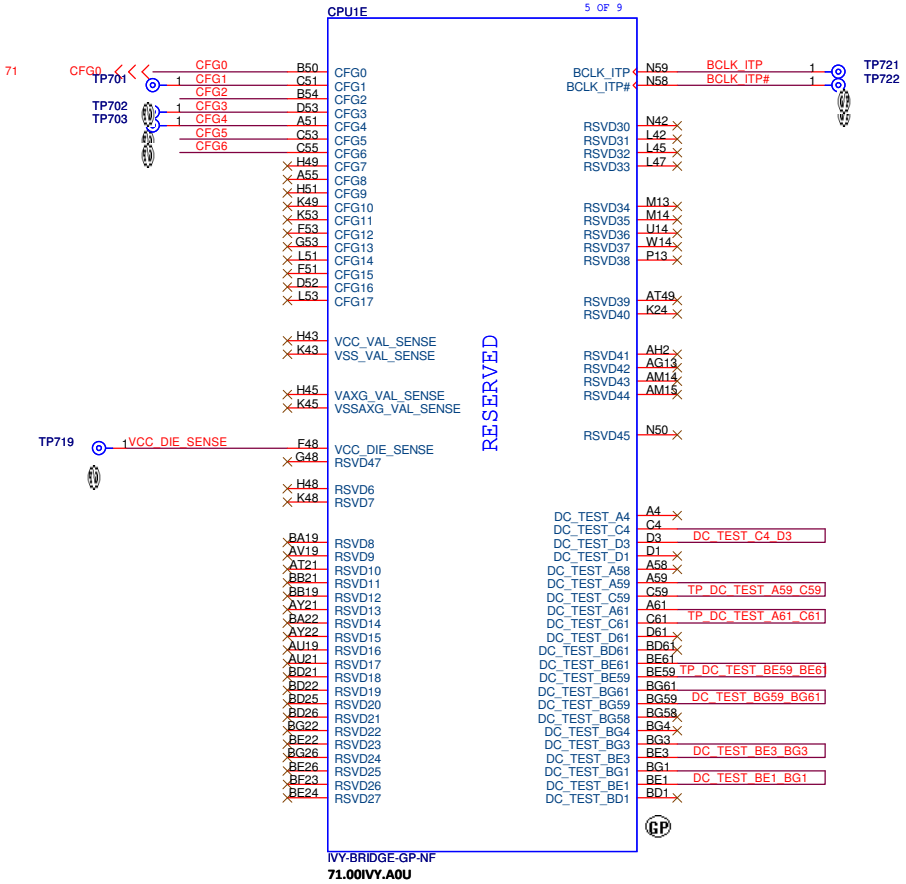
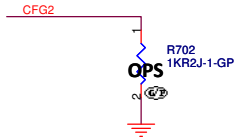
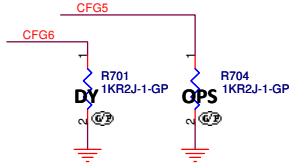
SSID = CPU





PEG Static Lane Reversal	
CFG[2]	1: Normal Operation; Lane # definition matches socket pin map definition
	0:Lane Reversed

Display Port Presence Strap	
CFG[4]	1: Disabled; No Physical Display Port attached to Embedded Display Port
	0: Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: 1x16 PCI Express
	10: 2 x8 - PCI Express
	01: Reserved
	00: 1x8, 2x4 PCI Express

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Title: CPU (RESERVED)

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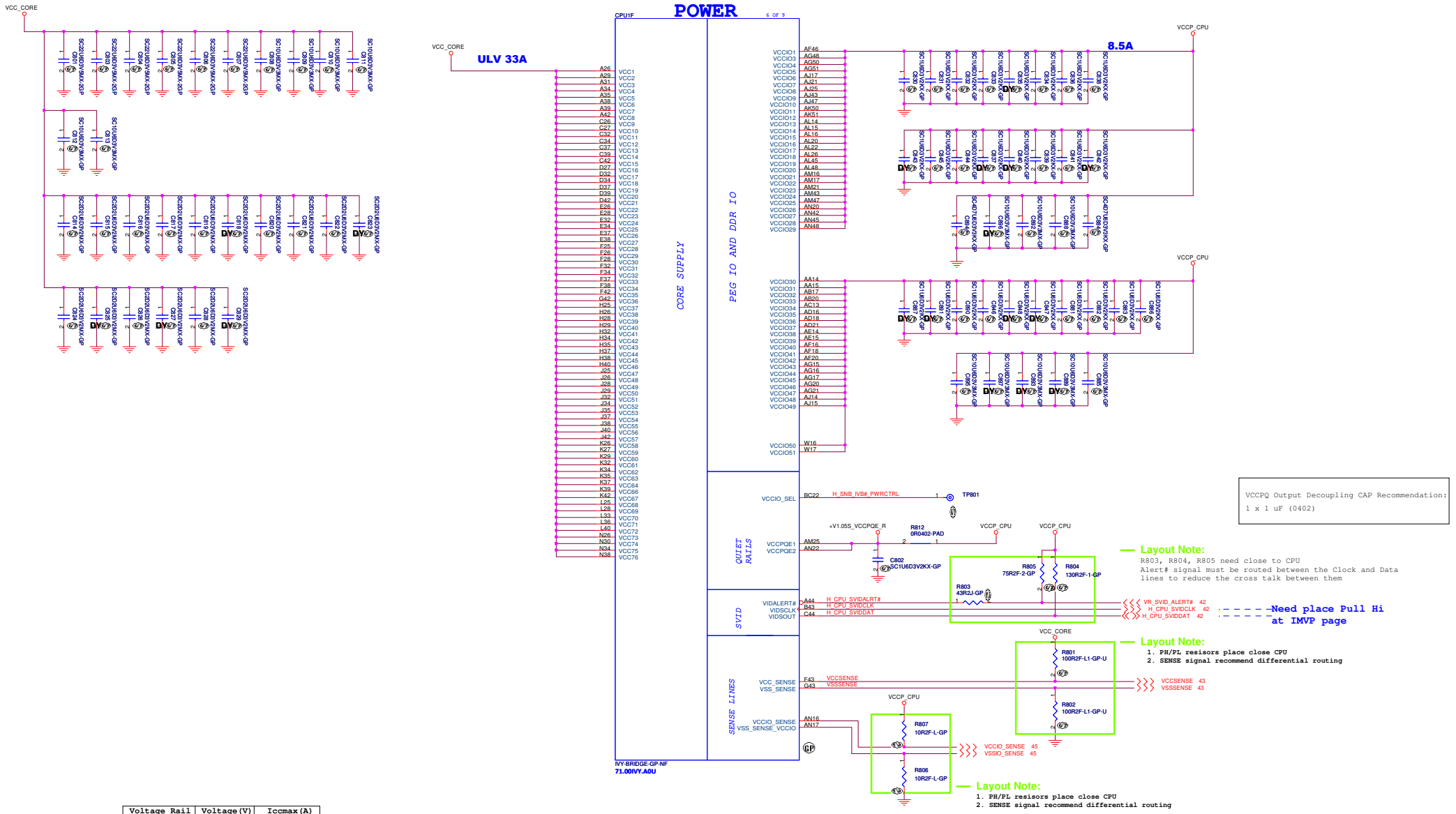
SSID = CPU



Voltage Rail	Voltage(V)	Iccmax(A)
VCC_CORE	0.3~1.52	33
VAXG	0~1.52	29 (GT2)
VCCIO	1.05	8.5
VDDQ	1.5	5
VCCSA	0.675~0.9	4
VCCPLL	1.8	1.2

Refer to CPU EDS V.1.7.5

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Title: CPU (VCC_CORE)

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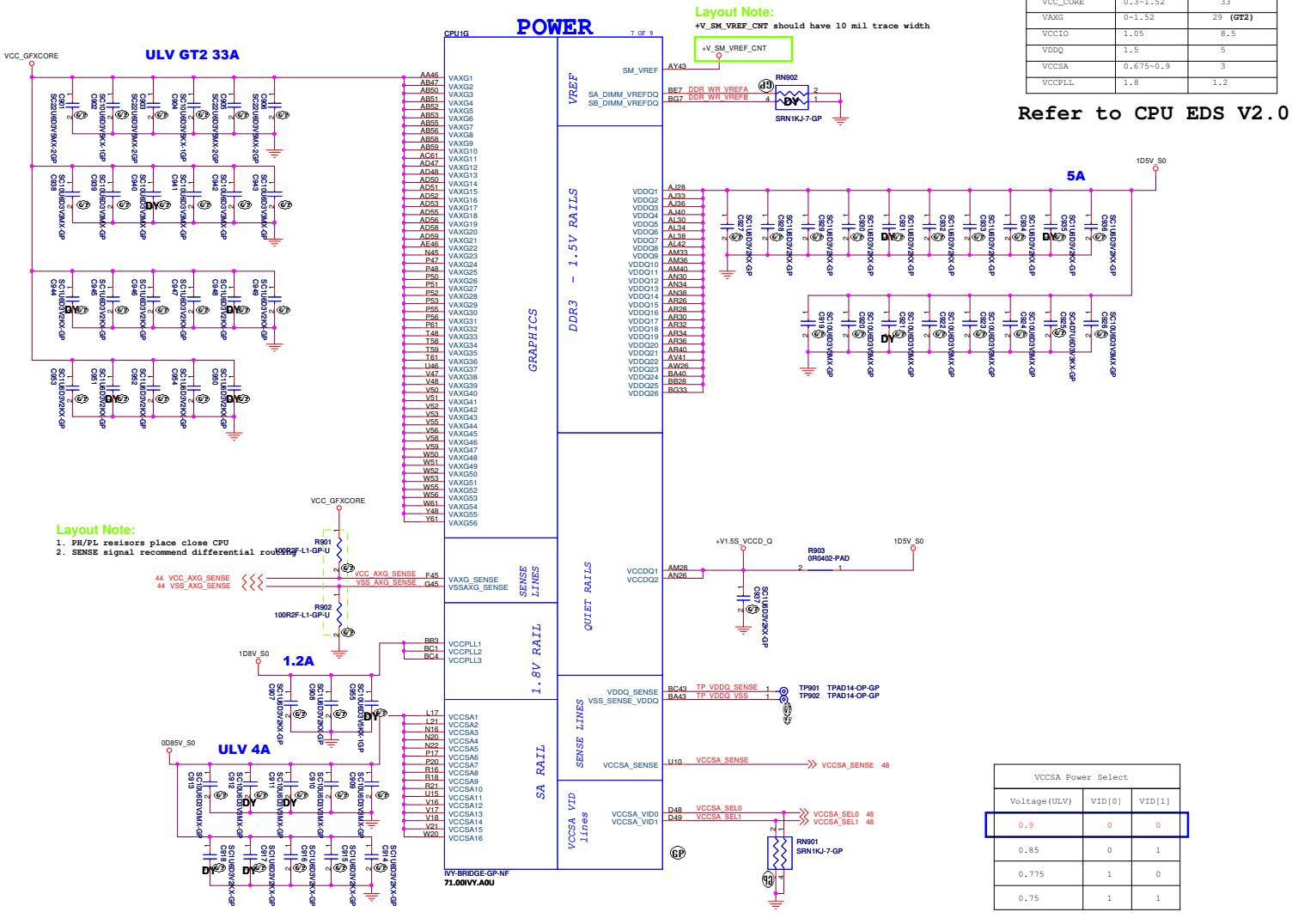
SSID = CPU



Voltage Rail	Voltage(V)	Iccmax(A)
VCC_CORE	0.3~1.52	33
VAXG	0~1.52	29 (GT2)
VCCIO	1.05	8.5
VDDQ	1.5	5
VCCSA	0.675~0.9	3
VCCPLL	1.8	1.2

Refer to CPU EDS V2.0

VCCSA Power Select		
Voltage(ULV)	VID[0]	VID[1]
0.9	0	0
0.85	0	1
0.775	1	0
0.75	1	1

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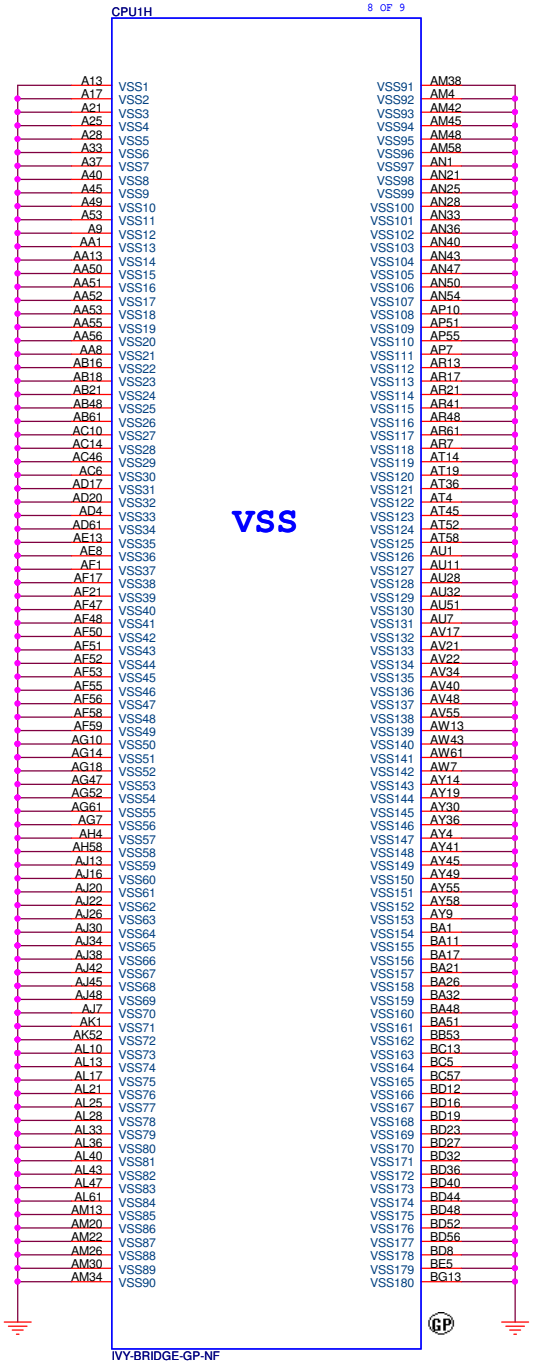
Taipei Hsien 221, Taiwan, R.O.C.

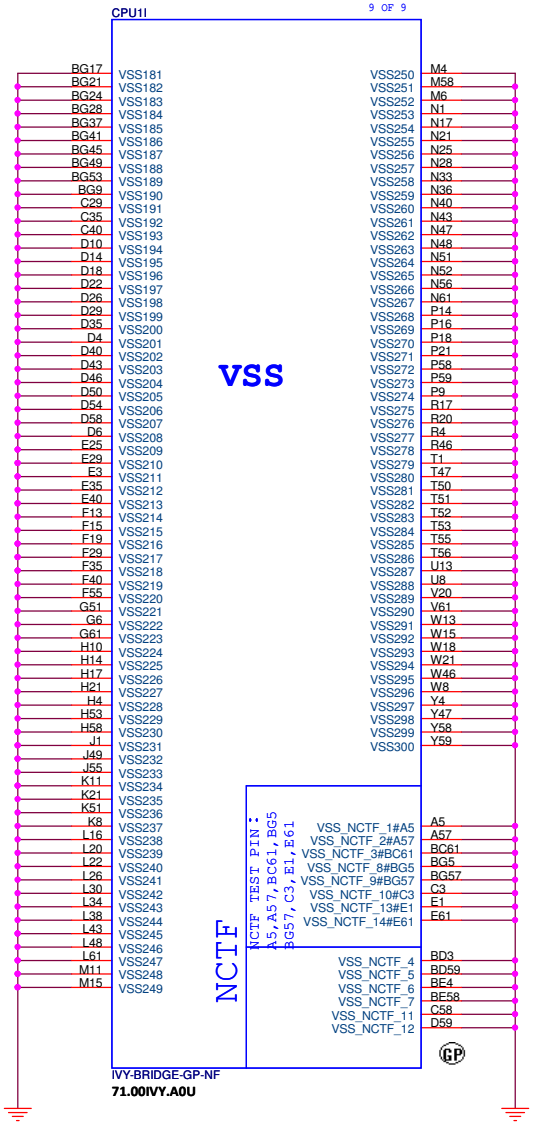
Title: CPU (VCC_GFXCORE)

Size: A2 | Document Number: OAK14 Chief River DIS | Rev: A00

Date: Wednesday, September 05, 2012 | Sheet 9 of 105

SSID = CPU





M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (VSS)**

Size: A3 | Document Number: **OAK14 Chief River DIS** | Rev: **A00**

Date: Wednesday, September 05, 2012 | Sheet 10 of 105

(Blanking)

M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: XDP

Size: A3 | Document Number: OAK14 Chief River DIS | Rev: A00

Date: Wednesday, September 05, 2012 | Sheet 11 of 105

(Blanking)

M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*OAK14 Chief River DIS*	*A00*

Date: Wednesday, September 05, 2012 Sheet 12 of 105

(Blanking)

M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

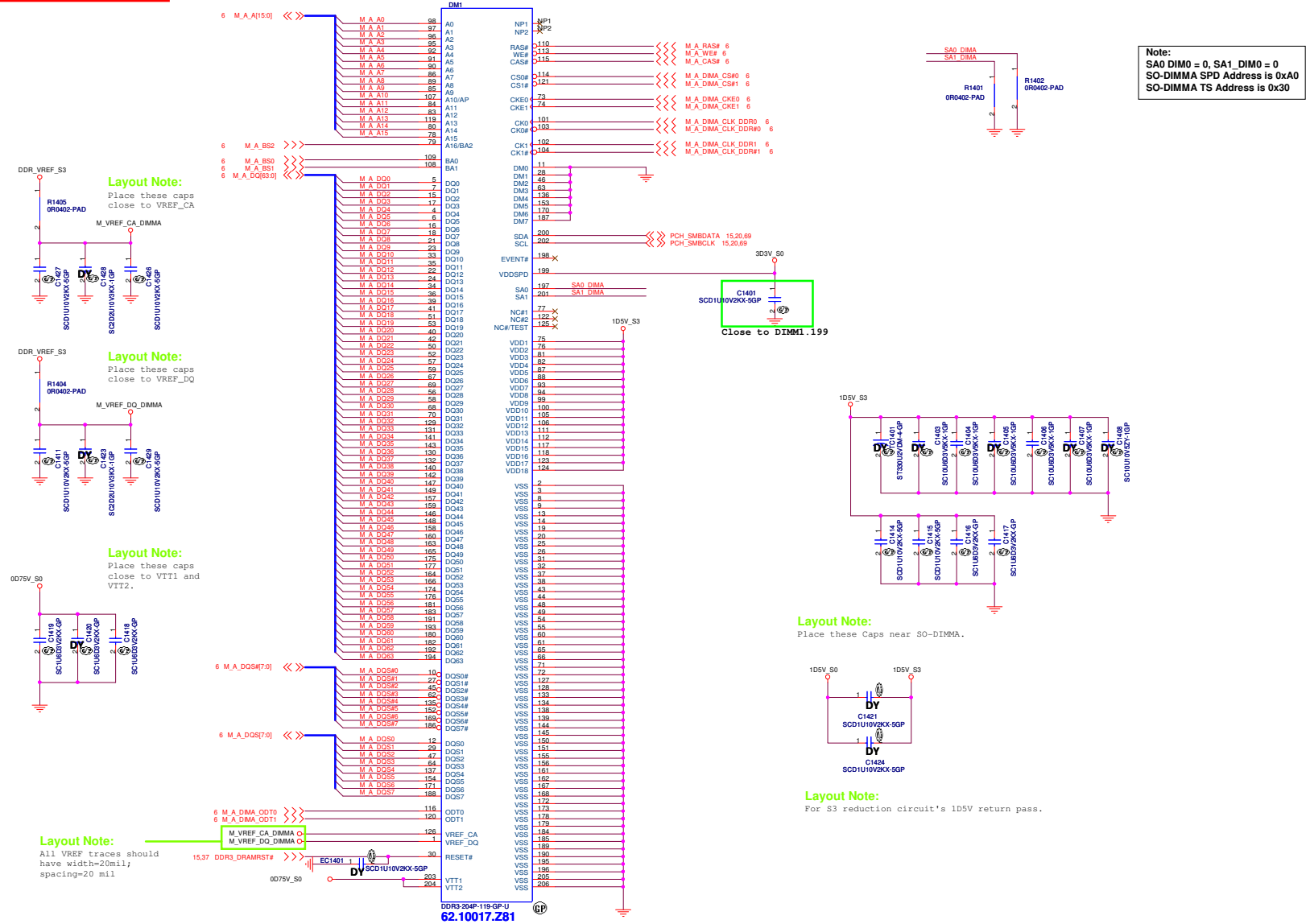
Title

(Reserved)

Size	Document Number	Rev
A3	*OAK14 Chief River DIS*	*A00*

Date: Wednesday, September 05, 2012 Sheet 13 of 105

SSID = MEMORY



M14 DIS

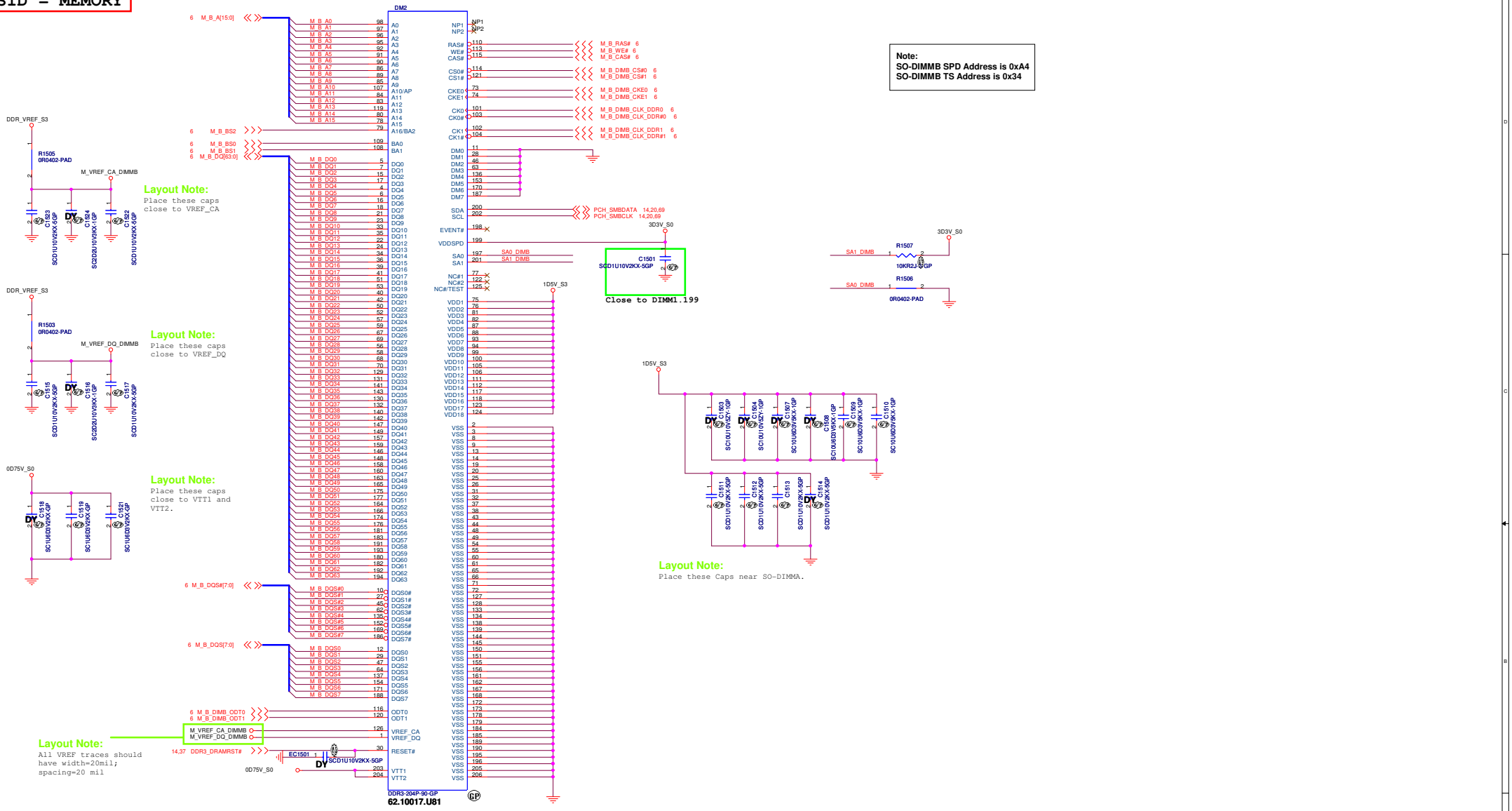
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1

Size	Document Number	Rev
A2	DNE40 14 CR DIS	A00

Date: Wednesday, September 05, 2012 Sheet 14 of 105

SSID = MEMORY



M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR3-SODIMM2***

Size	Document Number	Rev
A2	*OAK14 Chief River DIS*	*A00*

Date: Wednesday, September 05, 2012 Sheet 15 of 105

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M14 DIS

Wistron Corporation
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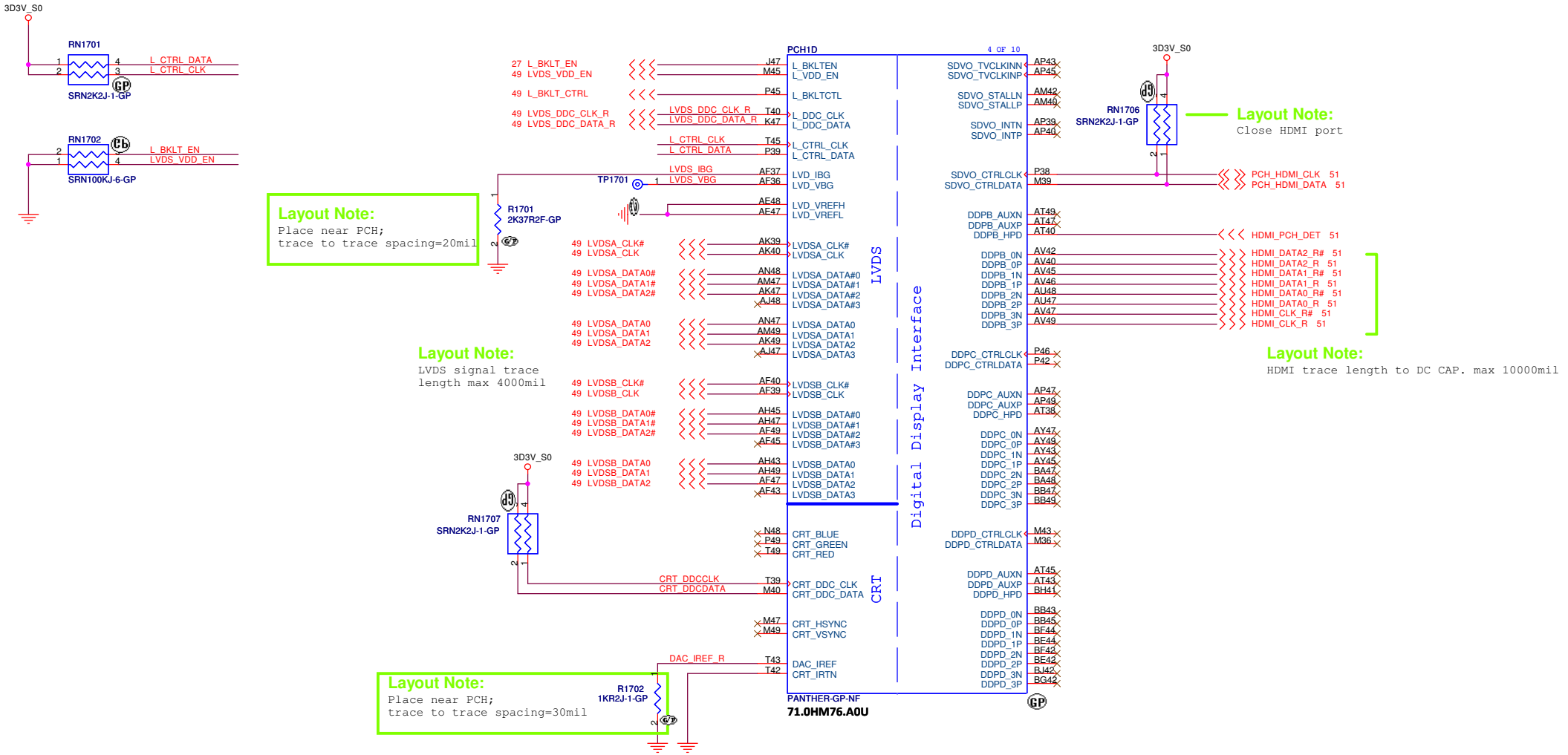
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A3	*OAK14 Chief River DIS*	*A00*

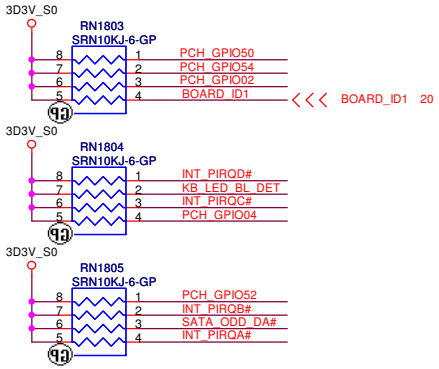
SSID = PCH



M14 DIS

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: PCH (LVDS/CRT/DDI)		
Size: A3	Document Number: OAK14 Chief River DIS	Rev: A00
Date: Wednesday, September 05, 2012	Sheet 17 of 105	

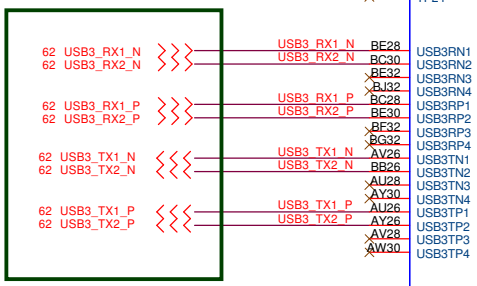
SSID = PCH

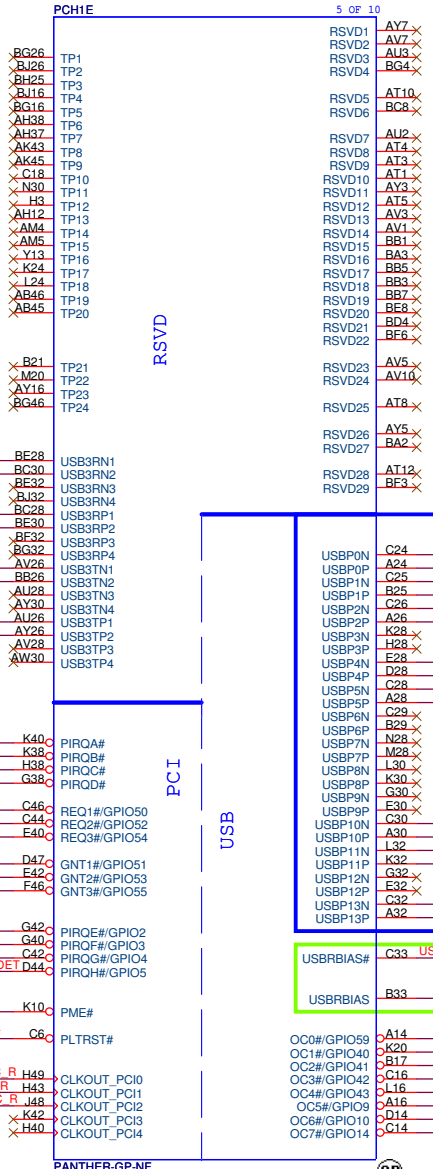


USB3.0/2.0 Mapping Table

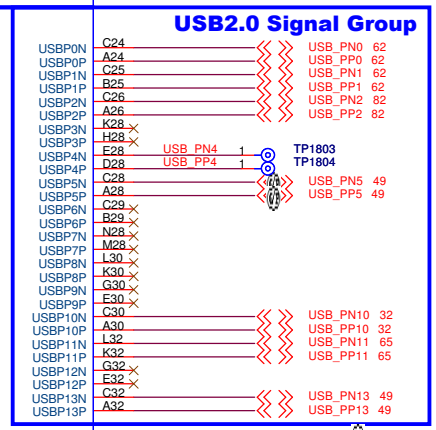
USB 3.0 Port	USB 2.0 port
Port 1	Port 0
Port 2	Port 1
Port 3	Port 2
Port 4	Port 3

Layout Note:
Trace Length :
PCH ~~9000mil~~Cap~~1000mil~~CONN





USB2.0 Signal Group



USB Table

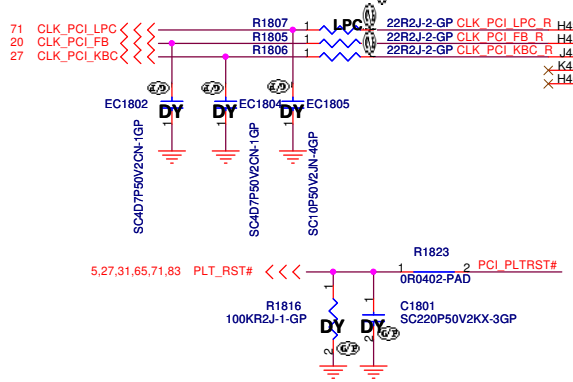
Pair	Device
0	USB3.0 port2
1	USB3.0 port1, with Debug Port
2	USB2.0 port3
3	NC
4	NC
5	Touch Panel
6	HM76 NC
7	HM76 NC
8	NC
9	NC
10	Card reader
11	WLAN
12	NC
13	CAMERA

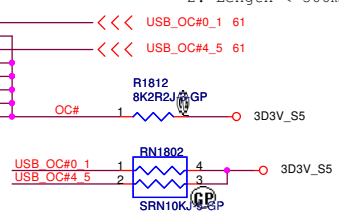
1. USB Ext. port 9 (HS) External debug port use on Chief River platform.
2. 2011 July; Microsoft will support USB3.0 debug--> Port1 useable.

Layout Note:
1. USBRBIAS/# use 50ohm single-ended impedance spacing to other signal=15mil
2. Length < 500mil

Boot Bios Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

A16 Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default





M14 DIS

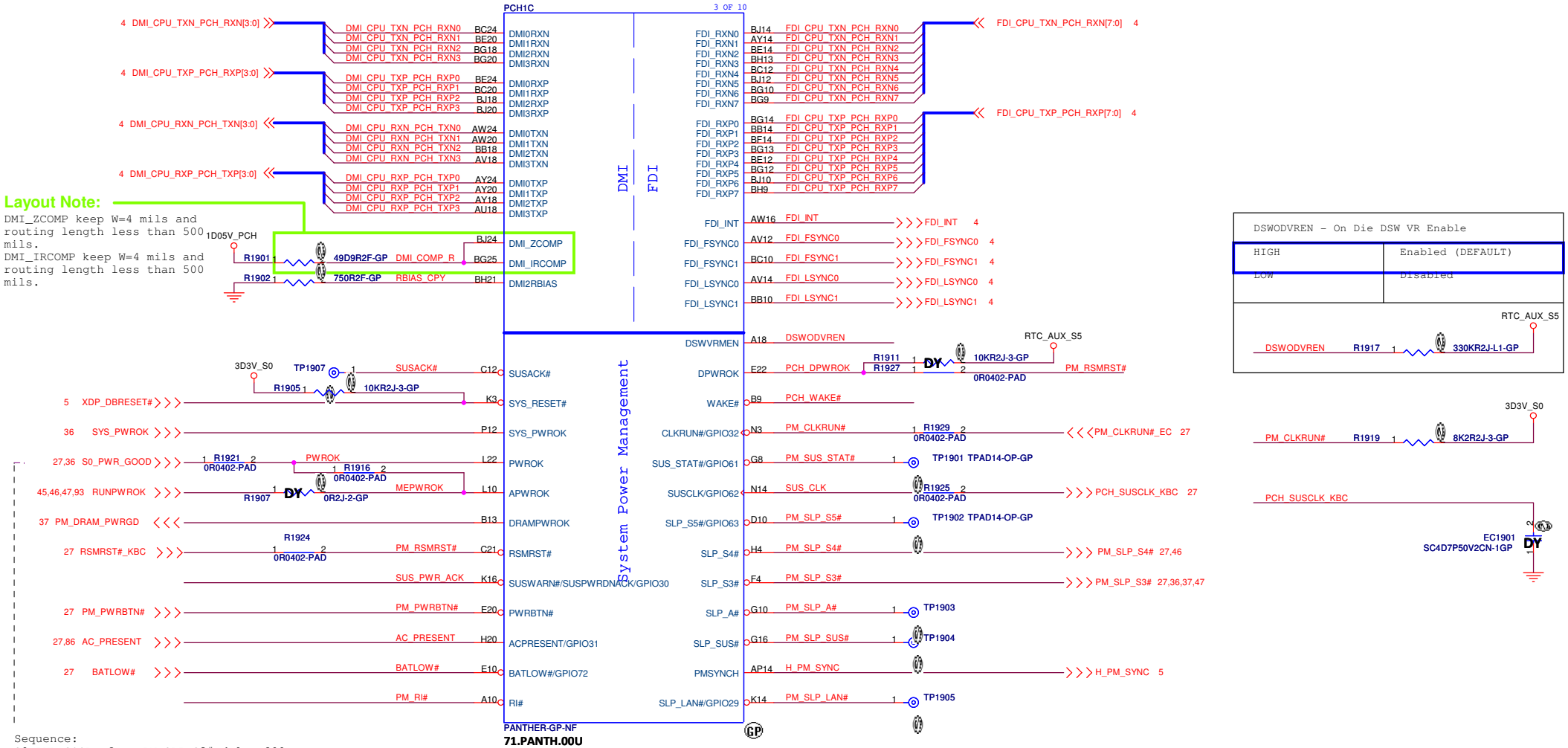
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI/USB/NVRAM)

Size	Document Number	Rev
A3	DNE40 14 CR DIS	A00

Date: Wednesday, September 05, 2012 Sheet 18 of 105

SSID = PCH

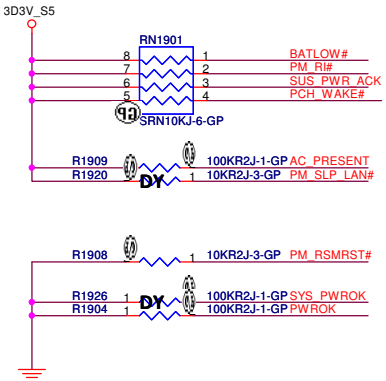


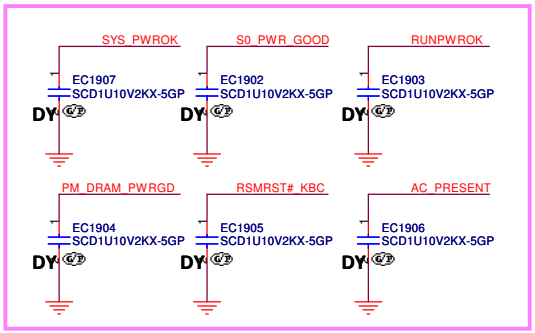
Layout Note:

DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

Sequence:
S0_PWR_GOOD after PM_SLP_S3# delay 200 ms

DSWODVREN – On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled





reserve for EMI Request

M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
PCH (DM I/FDI/PM)		
Size: A3	Document Number: DNE40 14 CR DIS	Rev: A00
Date: Wednesday, September 05, 2012	Sheet 19 of 105	

SSID = PCH

S5 power rail CLKREQ#:
PCIECLKRQ[0]#
PCIECLKRQ[7:3]#

S0 power rail CLKREQ#:
PCIECLKRQ[2:1]#

PCH1B — 2 OF 10

PCI-E* | SMBUS | CLOCKS | FLEX CLOCKS | Controller Link

PANTHER-GP-NF
71.PANTH.00U

Layout Note:
Layout trace < 14000mil

Layout Note:
CLKOUT termination
place close to PCH <500mil

Layout Note:
Can Place Far away PCH

Layout Note:
CLKOUT termination
place close to PCH <500mil

Layout Note:
1500mil < Layout trace < 10000mil

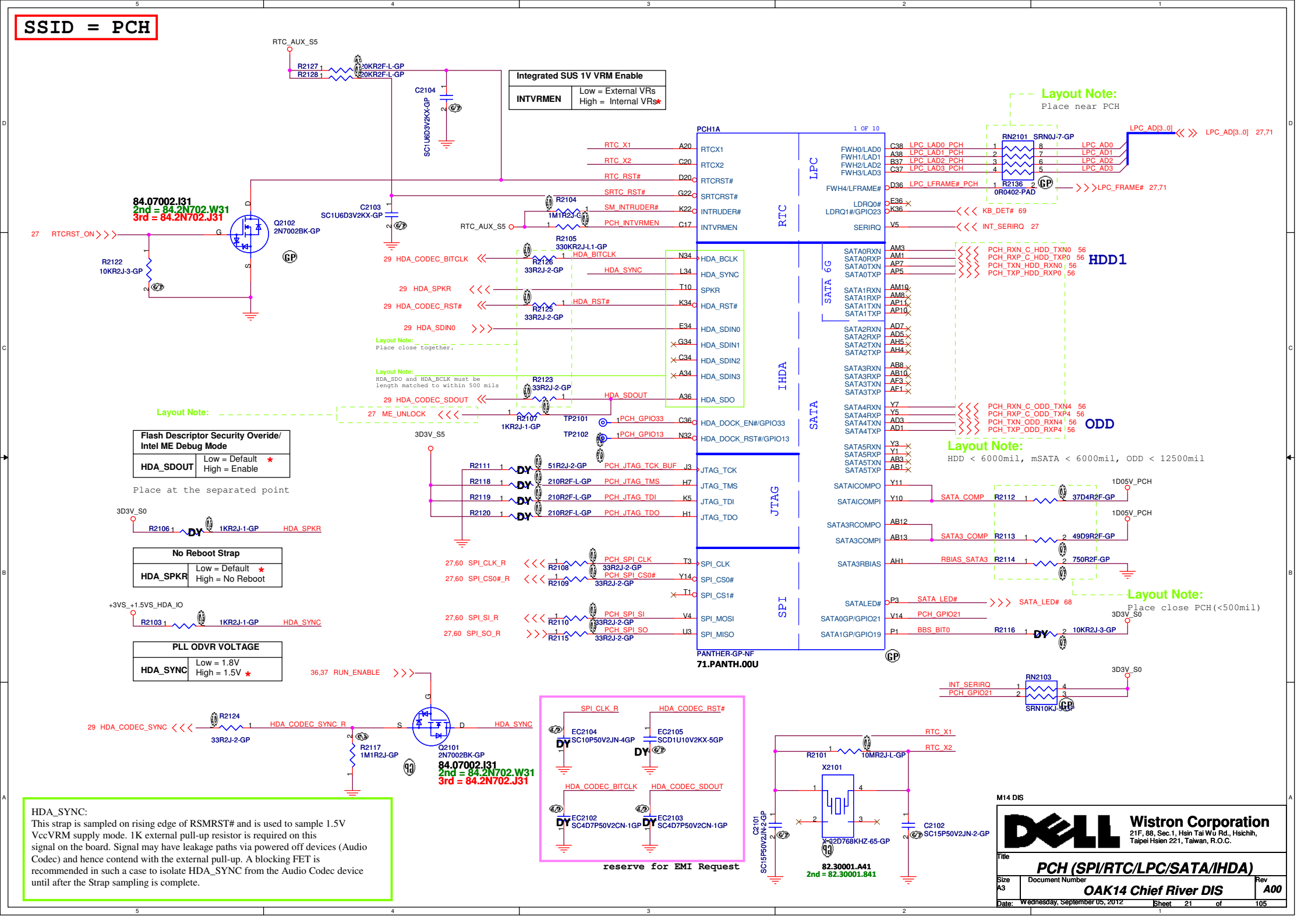
BIOS UMA/DIS Strap pin		
	BOARD_ID1	BOARD_ID2
~~PX(AMD)~~	~~0~~	~~0~~
~~DIS~~	~~0~~	~~1~~
UMA	1	0
Optimus(NV)	1	1

M14 DIS

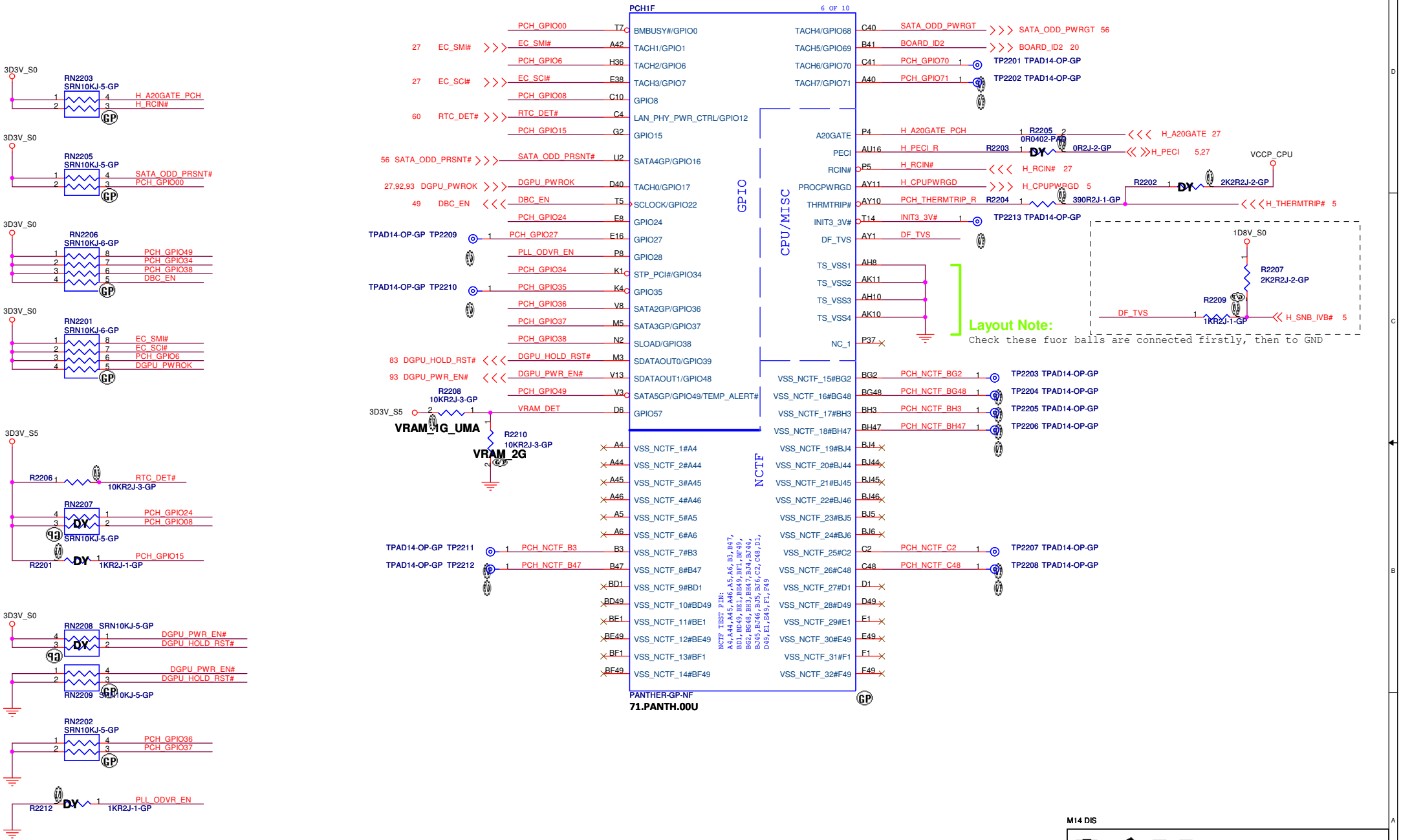
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (PCI-E/SMBUS/CLOCK/CL)**
Size: A3 | Document Number: **OAK14 Chief River DIS** | Rev: **A00**
Date: Wednesday, September 05, 2012 | Sheet 20 of 105

SSID = PCH


RTC_AUX_S5
R2127 20KR2F-L-GP
R2128 20KR2F-L-GP
C2104 SC1U6D3V2KX-GP
Integrated SUS 1V VRM Enable
INTVRMEN
Low = External VRs
High = Internal VRs
PCH1A
1 OF 10
RTC_X1 A20 RTCX1
RTC_X2 C20 RTCX2
RTC_RST# D20 RTCRST#
SRTC_RST# G22 SRTCRST#
SM_INTRUDER# K22 INTRUDER#
PCH_INTVRMEN C17 INTVRMEN
RTC
84.07002.I31
2nd = 84.2N702.W31
3rd = 84.2N702.J31
Q2102 2N7000BK-GP
27 RTCRST_ON
R2122 10KR2J-3-GP
C2103 SC1U6D3V2KX-GP
R2104 1M1R2J-GP
RTC_AUX_S5
R2105 330KR2J-L1-GP
29 HDA_CODEC_BITCLK
R2126 33R2J-2-GP
HDA_BITCLK
HDA_SYNC
29 HDA_SPKR
29 HDA_CODEC_RST#
R2125 33R2J-2-GP
HDA_RST#
29 HDA_SDIN0
Layout Note:
Place close together.
Layout Note:
HDA_SDO and HDA_BCLK must be length matched to within 500 mils
R2123 33R2J-2-GP
29 HDA_CODEC_SDOUT
HDA_SDOUT
27 ME_UNLOCK
R2107 1KR2J-1-GP
TP2101
TP2102
PCH_GPIO33 C36 HDA_DOCK_EN#/GPIO33
PCH_GPIO13 N32 HDA_DOCK_RST#/GPIO13
IHDA
HDA_BCLK N34
HDA_SYNC L34
SPKR T10
HDA_RST# K34
HDA_SDIN0 E34
HDA_SDIN1 G34
HDA_SDIN2 C34
HDA_SDIN3 A34
HDA_SDO A36
Layout Note:
Place at the separated point
Flash Descriptor Security Overide/ Intel ME Debug Mode
HDA_SDOUT
Low = Default
High = Enable
3D3V_S5
R2111 DY 51R2J-2-GP PCH_JTAG_TCK_BUF J3
R2118 DY 210R2F-L-GP PCH_JTAG_TMS H7
R2119 DY 210R2F-L-GP PCH_JTAG_TDI K5
R2120 DY 210R2F-L-GP PCH_JTAG_TDO H1
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG
3D3V_S0
R2106 DY 1KR2J-1-GP HDA_SPKR
No Reboot Strap
HDA_SPKR
Low = Default
High = No Reboot
27,60 SPI_CLK_R R2108 33R2J-2-GP PCH_SPI_CLK T3
27,60 SPI_CS0#_R R2109 33R2J-2-GP PCH_SPI_CS0# Y14
T1
27,60 SPI_SI_R R2110 33R2J-2-GP PCH_SPI_SI V4
27,60 SPI_SO_R R2115 33R2J-2-GP PCH_SPI_SO U3
SPI_CLK
SPI_CS0#
SPI_CS1#
SPI_MOSI
SPI_MISO
SPI
+3VS_+1.5VS_HDA_IO
R2103 1KR2J-1-GP HDA_SYNC
PLL ODVR VOLTAGE
HDA_SYNC
Low = 1.8V
High = 1.5V
PANTHER-GP-NF
71.PANTH.00U
LPC
FWH0/LAD0 C38 LPC_LAD0_PCH
FWH1/LAD1 A38 LPC_LAD1_PCH
FWH2/LAD2 B37 LPC_LAD2_PCH
FWH3/LAD3 C37 LPC_LAD3_PCH
FWH4/LFRAME# D36 LPC_LFRAME#_PCH
LDRQ0# E36
LDRQ1#/GPIO23 K36
SERIRQ V5
RN2101 SRN0J-7-GP
R2136 0R0402-PAD
LPC_AD[3..0] 27,71
LPC_FRAME# 27,71
KB_DET# 69
INT_SERIRQ 27
Layout Note:
Place near PCH
SATA 6G
SATA0RXN AM3
SATA0RXP AM1
SATA0TXN AP7
SATA0TXP AP5
SATA1RXN AM10
SATA1RXP AM8
SATA1TXN AP11
SATA1TXP AP10
SATA2RXN AD7
SATA2RXP AD5
SATA2TXN AH5
SATA2TXP AH4
SATA3RXN AB8
SATA3RXP AB10
SATA3TXN AF3
SATA3TXP AF1
SATA4RXN Y7
SATA4RXP Y5
SATA4TXN AD3
SATA4TXP AD1
SATA5RXN Y3
SATA5RXP Y1
SATA5TXN AB3
SATA5TXP AB1
PCH_RXN_C_HDD_TXN0 56
PCH_RXP_C_HDD_TXP0 56
PCH_TXN_HDD_RXN0 56
PCH_TXP_HDD_RXP0 56
HDD1
PCH_RXN_C_ODD_TXN4 56
PCH_RXP_C_ODD_TXP4 56
PCH_TXN_ODD_RXN4 56
PCH_TXP_ODD_RXP4 56
ODD
Layout Note:
HDD < 6000mil, mSATA < 6000mil, ODD < 12500mil
SATA
SATAICOMPO Y11
SATAICOMPI Y10
SATA_COMP R2112 37D4R2F-GP
SATA3RCOMPO AB12
SATA3COMPI AB13
SATA3_COMP R2113 49D9R2F-GP
SATA3RBIAS AH1
RBIAS_SATA3 R2114 750R2F-GP
1D05V_PCH
SATALED# P3
SATA_LED# 68
SATA0GP/GPIO21 V14
PCH_GPIO21
SATA1GP/GPIO19 P1
BBS_BIT0
R2116 DY 10KR2J-3-GP
3D3V_S0
Layout Note:
Place close PCH(<500mil)
INT_SERIRQ
PCH_GPIO21
RN2103
SRN10KJ-5-GP
36,37 RUN_ENABLE
29 HDA_CODEC_SYNC
R2124 33R2J-2-GP
HDA_CODEC_SYNC_R
R2117 1M1R2J-GP
Q2101 2N7002BK-GP
84.07002.I31
2nd = 84.2N702.W31
3rd = 84.2N702.J31
SPI_CLK_R
HDA_CODEC_RST#
EC2104 DY SC10P50V2JN-4GP
EC2105 DY SCD1U10V2KX-5GP
HDA_CODEC_BITCLK
HDA_CODEC_SDOUT
EC2102 DY SC4D7P50V2CN-1GP
EC2103 DY SC4D7P50V2CN-1GP
reserve for EMI Request
RTC_X1
RTC_X2
R2101 10MR2J-L-GP
X2101 X32D768KHZ-65-GP
C2101 SC15P50V2JN-2-GP
C2102 SC15P50V2JN-2-GP
82.30001.A41
2nd = 82.30001.841
HDA_SYNC:
This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.
M14 DIS
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (SPI/RTC/LPC/SATA/IHDA)
Size A3
Document Number
OAK14 Chief River DIS
Rev A00
Date: Wednesday, September 05, 2012
Sheet 21 of 105

SSID = PCH



PLL ON DIE VR ENABLE	
GPIO28 (PLL_ODVR_EN)	Weakly internal pull up 20k. High - Enable LOW - Disable

M14 DIS

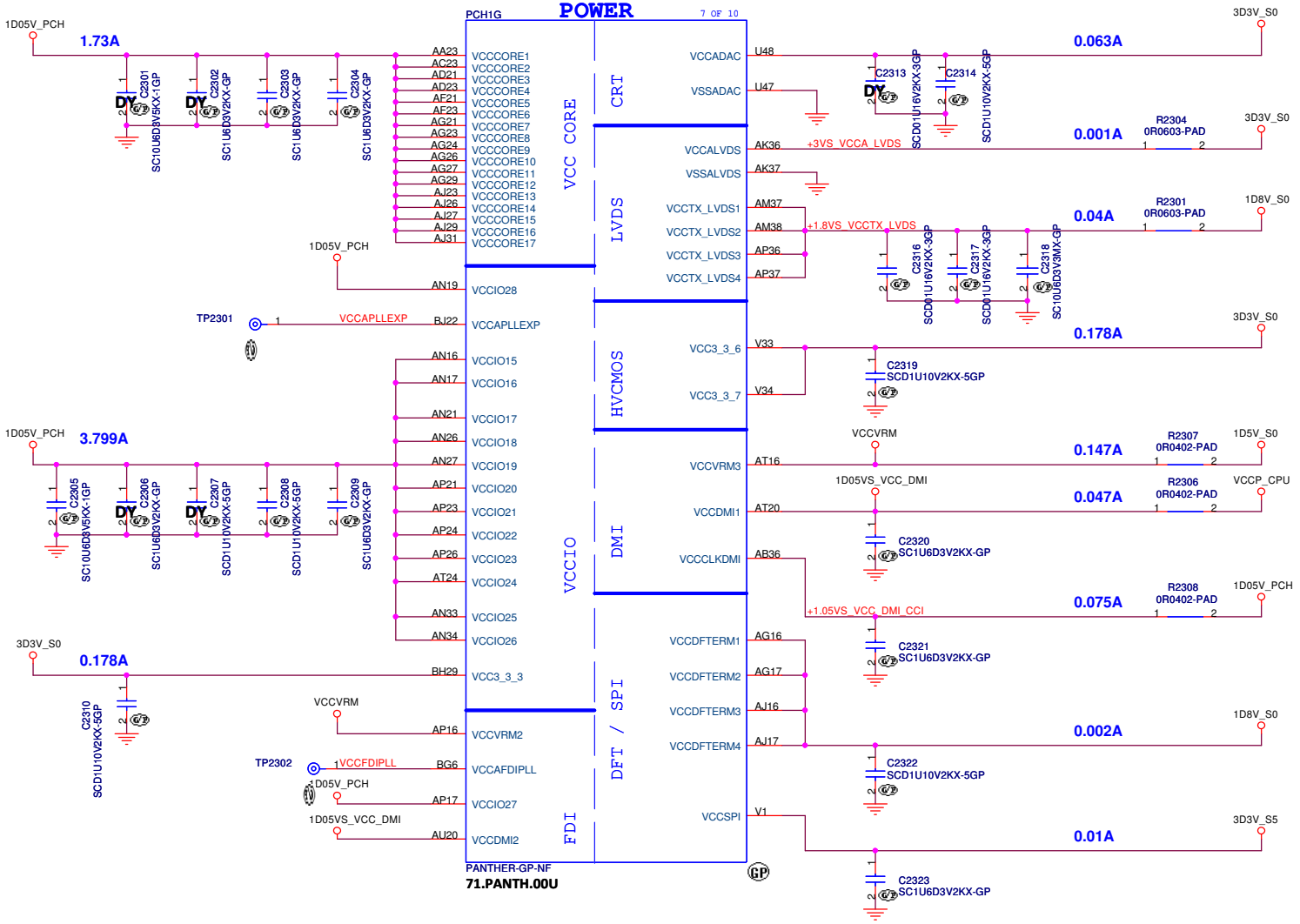
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (GPIO/CPU)

Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00

Date: Wednesday, September 05, 2012 Sheet 22 of 105

SSID = PCH



Voltage Rail	Voltage(V)	Iccmax(A)
V_PROC_IO	1.05/1.0	0.002
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.178
VccADAC	3.3	0.063
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.73
VccDMI	1.1	0.047
VccIO	1.05	3.799
VccASW	1.05	0.803
VccSPI	3.3	0.01
VccDSW3_3	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3	0.01
VccVRM	1.5	0.147
VccClkDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.05
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

Refer to chipset EDS V.1.8

check

M14 DIS

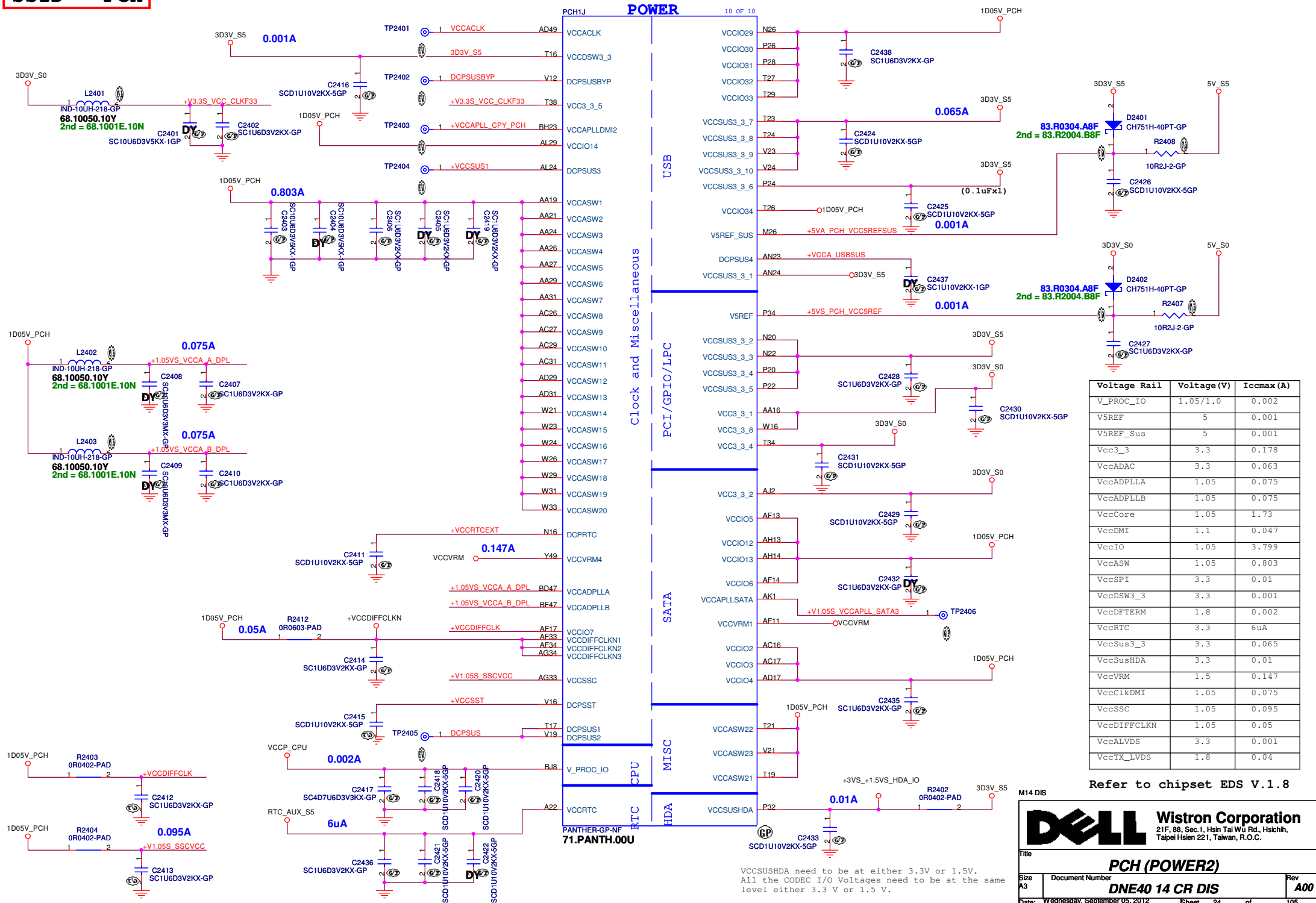
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (POWER1)**

Size: A3 | Document Number: **OAK14 Chief River DIS** | Rev: **A00**

Date: Wednesday, September 05, 2012 | Sheet 23 of 105

SSID = PCH



Voltage Rail	Voltage(V)	Iccmax(A)
V_PROC_IO	1.05/1.0	0.002
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.178
VccADAC	3.3	0.063
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.73
VccDMI	1.1	0.047
VccIO	1.05	3.799
VccASW	1.05	0.803
VccSPI	3.3	0.01
VccDSW3_3	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3	0.01
VccVRM	1.5	0.147
VccClkDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.05
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

Refer to chipset EDS V.1.8

M14 DIS

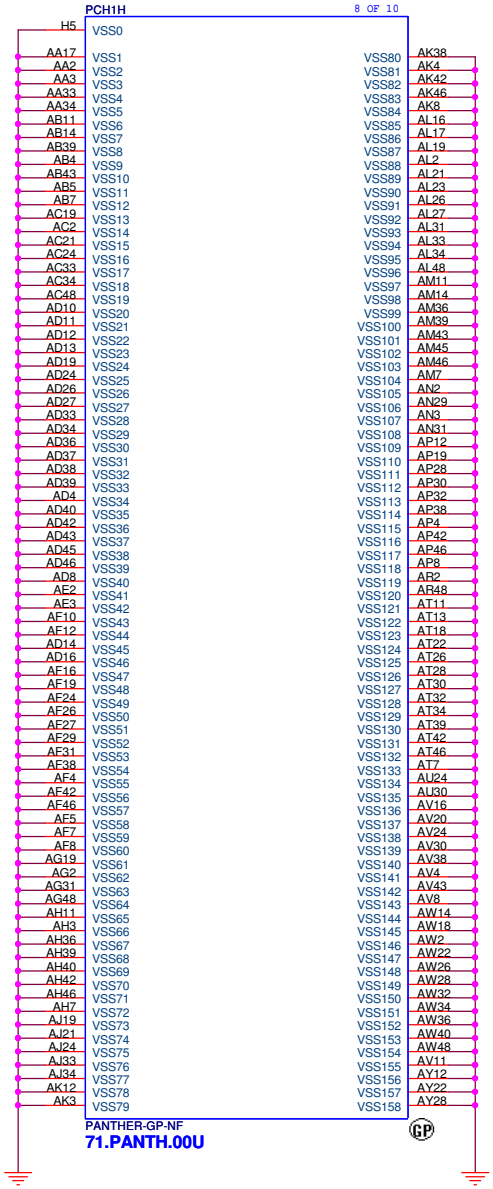
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

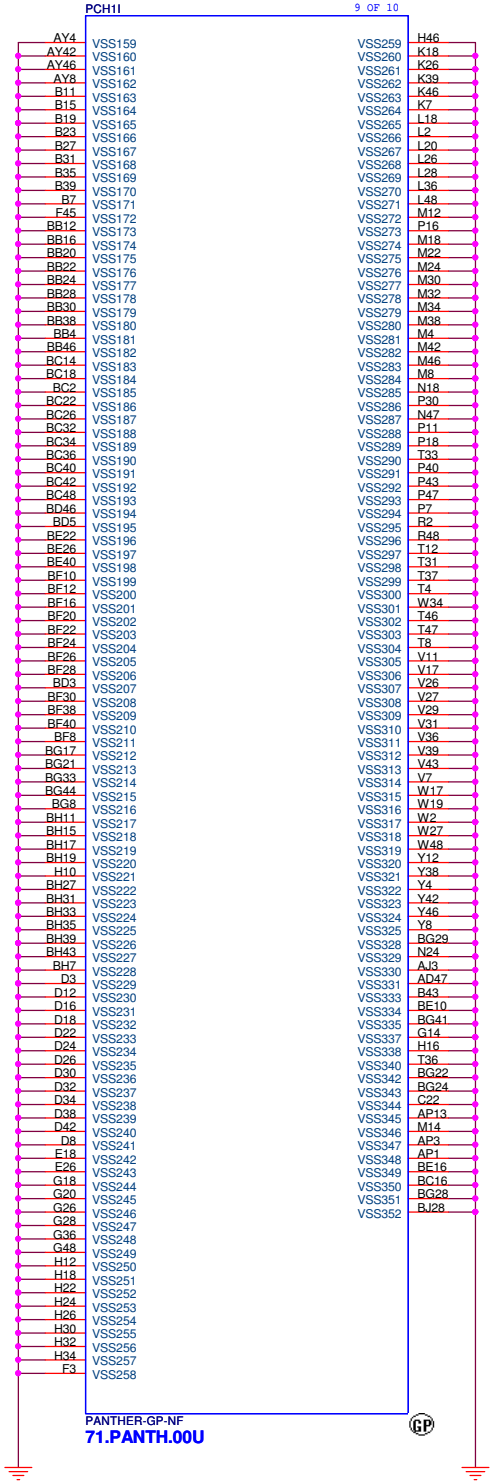
Title: PCH (POWER2)

Size	Document Number	Rev
A3	DNE40 14 CR DIS	A00

Date: Wednesday, September 05, 2012 Sheet 24 of 105

SSID = PCH





M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (VSS)

Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00

Date: Wednesday, September 05, 2012 Sheet 25 of 105

(Blanking)

M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: OAK14 Chief River DIS | Rev: A00

Date: Wednesday, September 05, 2012 | Sheet 26 of 105

SSID = KBC

PCB VER AD(GPIO91)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.0V
X01	100.0K	20.0K	2.75V
X02	100.0K	33.0K	2.48V
A00	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

MODEL_ID_DET(GPIO07)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
OAK14_UMA	100.0K	10.0K(64.10025.6DL)	3.0V
OAK14_DIS_N13P	100.0K	20.0K(64.20025.6DL)	2.75V
OAK14_DIS_N13M	100.0K	33.0K(64.33025.6DL)	2.48V
TBD	100.0K	47.0K(64.47025.6DL)	2.24V
TBD	100.0K	64.9K(64.64925.6DL)	2.0V
TBD	100.0K	76.8K(64.76825.6DL)	1.87V
TBD	100.0K	100.0K(64.10035.6DL)	1.65V
TBD	100.0K	143.0K(64.14335.6DL)	1.358V
TBD	100.0K	174.0K(64.17435.6DL)	1.204V
TBD	100.0K	215.0K(64.21535.6DL)	1.048V

Layout Note:
Need very close to EC

Layout Note:
Need very close to EC

Layout Note:
Connect GND and AGND planes via either 0R resistor or connect directly.

Layout Note:
Need very close to EC

<------ TP
<------ BATTERY / CHARGER
<------PCH / eDP

EC_GPIO23 High Active

84.07002.I31
2nd = 84.2N702.W31
3rd = 84.2N702.J31
C502 : check list 1.5

Power Switch Logic(PSL)

84.02130.031
2nd = 84.00102.031
3rd = 84.03413.A31
4th = 84.02301.G31

84.07002.I31
2nd = 84.2N702.W31
3rd = 84.2N702.J31

EC GPIO standard PH/PL

X00 0608

84.T3906.A11
2nd = 84.03906.F11

83.00016.K11
2nd = 83.00016.F11

83.00016.K11
2nd = 83.00016.F11

83.00016.K11
2nd = 83.00016.F11

M14 DIS

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Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC Nuvoton NPCE885

Size: A2 | Document Number: OAK14 Chief River DIS | Rev: A00

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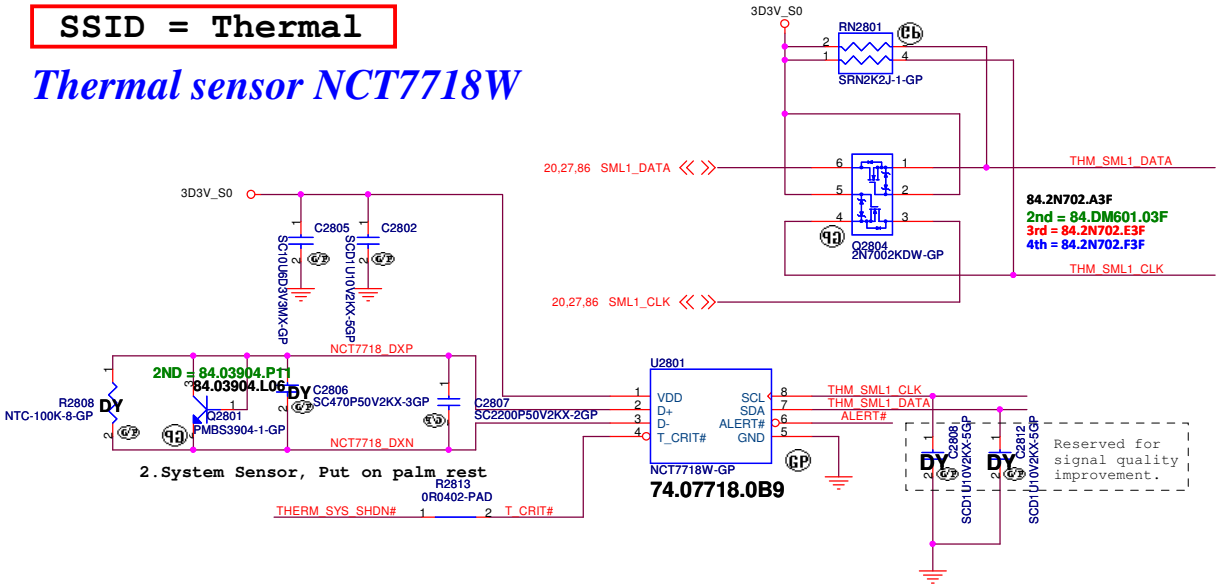
SSID = Thermal

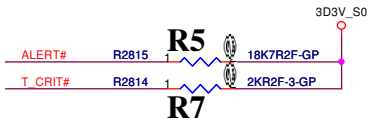
Thermal sensor NCT7718W



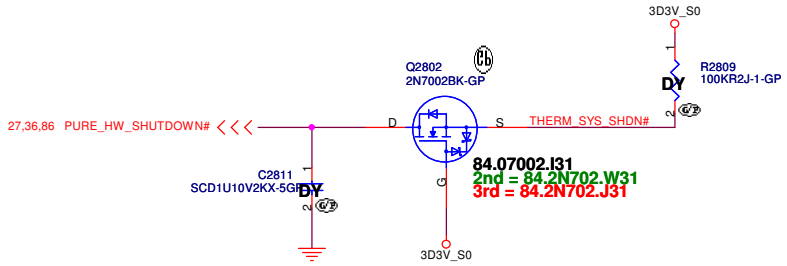
ALERT# /T_CRIT# Pull-up Resistor

R5 \ R7	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77℃	87℃	97℃	107℃	117℃
7.5Kohm	79℃	89℃	99℃	109℃	119℃
10.5Kohm	81℃	91℃	101℃	111℃	121℃
14Kohm	83℃	93℃	103℃	113℃	123℃
18.7Kohm	85℃	95℃	105℃	115℃	125℃

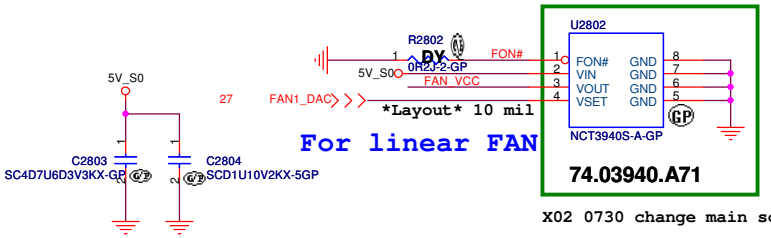
T_CRIT temperature strapping point



Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing. and route has to be away from the high noise area.
Put the C2807 2200pF to close the NCT7718W

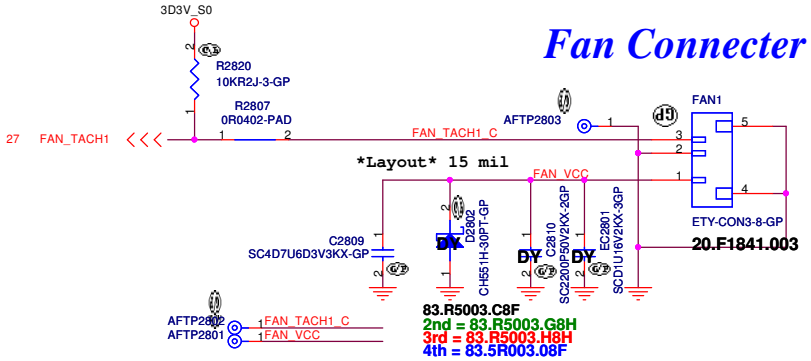


Fan controller NCT3940S-A



X02 0730 change main source

Fan Connecter



M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal NCT7718W/Fan Controllor P2793

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A3	OAK14 Chief River DIS	A00

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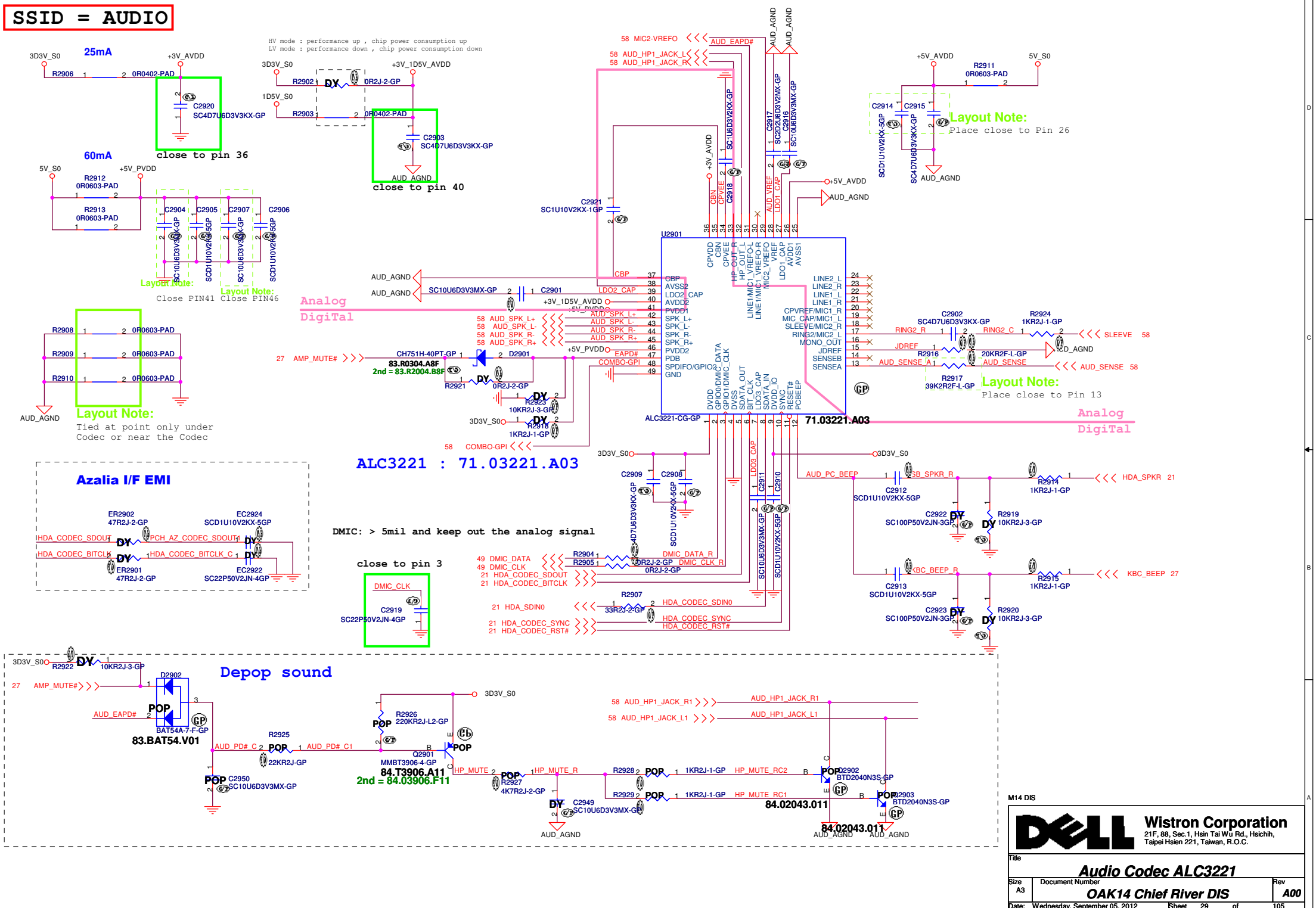
SSID = AUDIO



M14 DIS

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec ALC3221

Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00

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(Blanking)

M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

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LAN CHIP

1mS < +3D3V_LAN_S5 Rising time (10%~90%) <100mS

40 mils

close to pin 27 39 47 48

251mA

main: 84.00102.031
2nd: 84.03403.031

71.08105.B03

DY close to pin 21 22

M14 DIS

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Taipei Hsien 221, Taiwan, R.O.C.

Title: LOM

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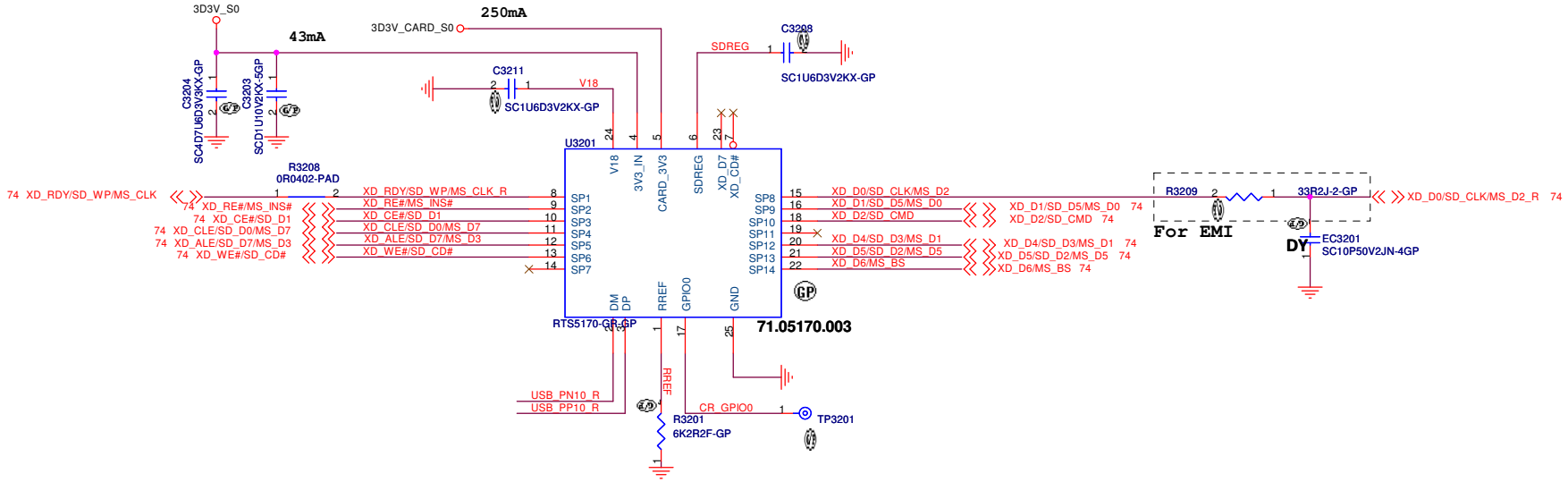
SSID = SDIO



Close U3201

M14 DIS

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Title	Card Reader-RTS5170	
Size: A3	Document Number: OAK14 Chief River DIS	Rev: A00
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(Blanking)

M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*OAK14 Chief River DIS*	*A00*

(Blanking)

M14 DIS

Wistron Corporation
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Title: *Reserved*

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(Blanking)

M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *OAK14 Chief River DIS* | Rev: *A00*

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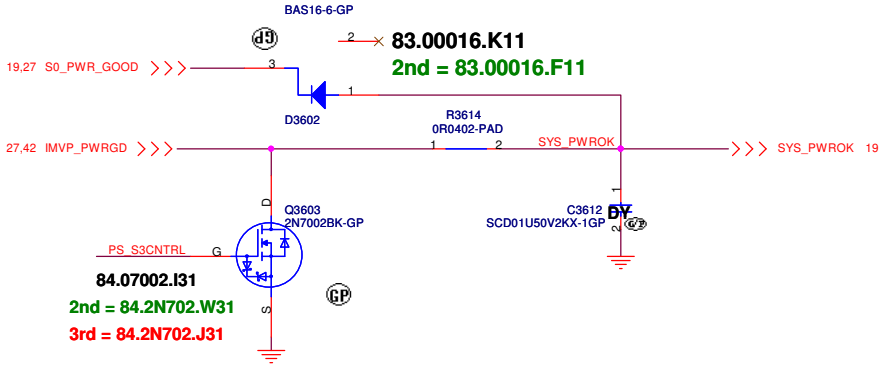
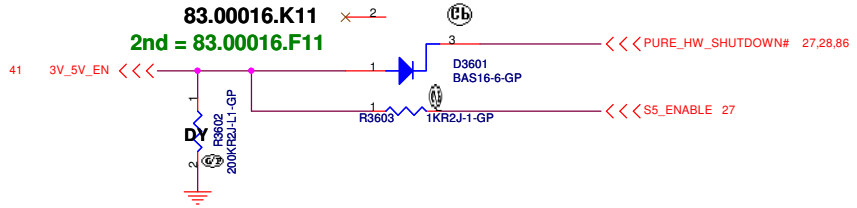
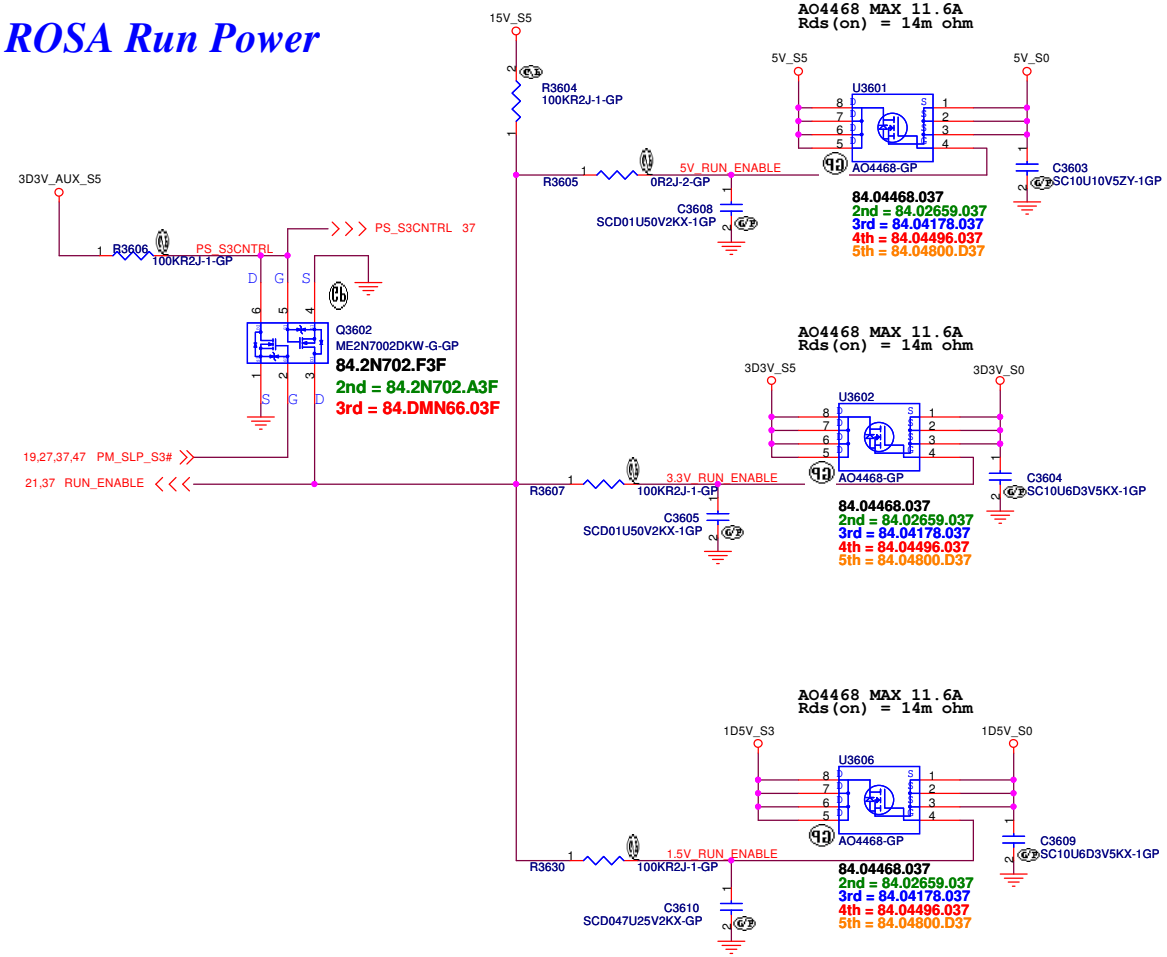
SSID = Reset.Suspend





ROSA Run Power



5V_S0

+5V_RUN Comsumption
Peak current ?A
Design current ?A

3D3V_S0

+3.3V_RUN Comsumption
Peak current ?A
Design current ?A

1D5V_S0

+1.5V_RUN Comsumption
Peak current ?A
Design current ?A

M14 DIS

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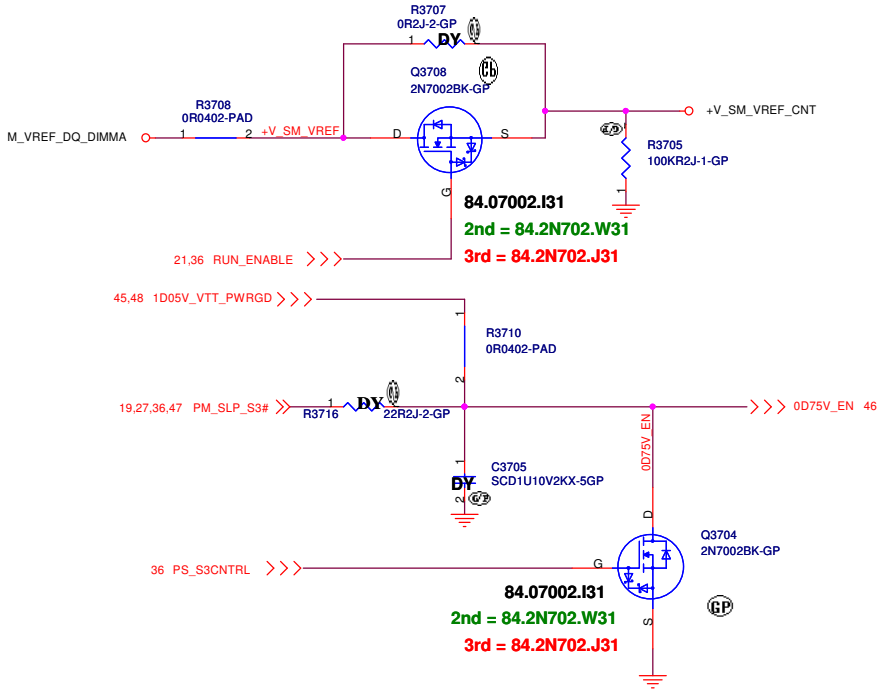
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Power Plane Enable*

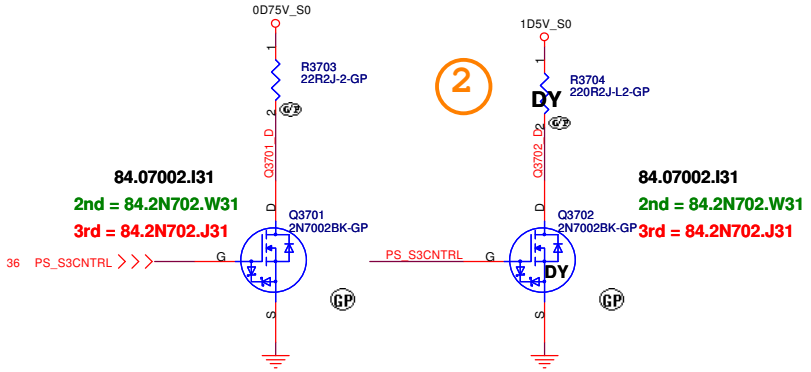
Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00

Date: Wednesday, September 05, 2012 Sheet 36 of 105

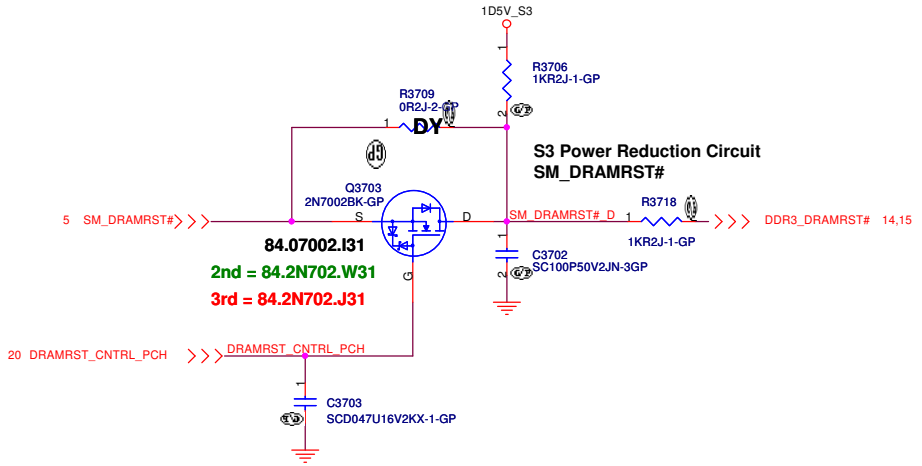
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



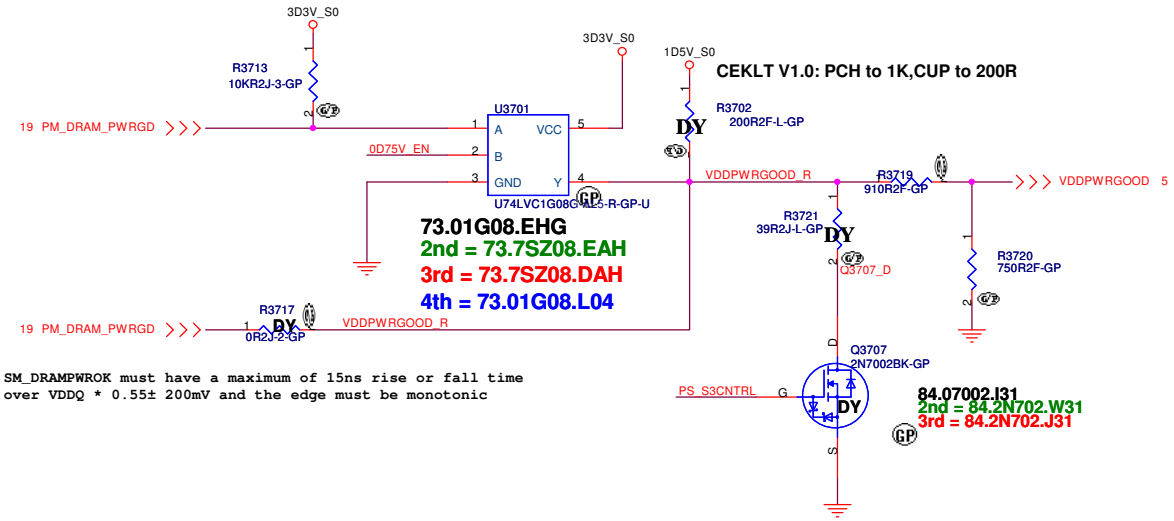
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



SM_DRAMPWROK must have a maximum of 15ns rise or fall time
over VDDQ * 0.55± 200mV and the edge must be monotonic

M14 DIS

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Title: S3 Reduction Circuit

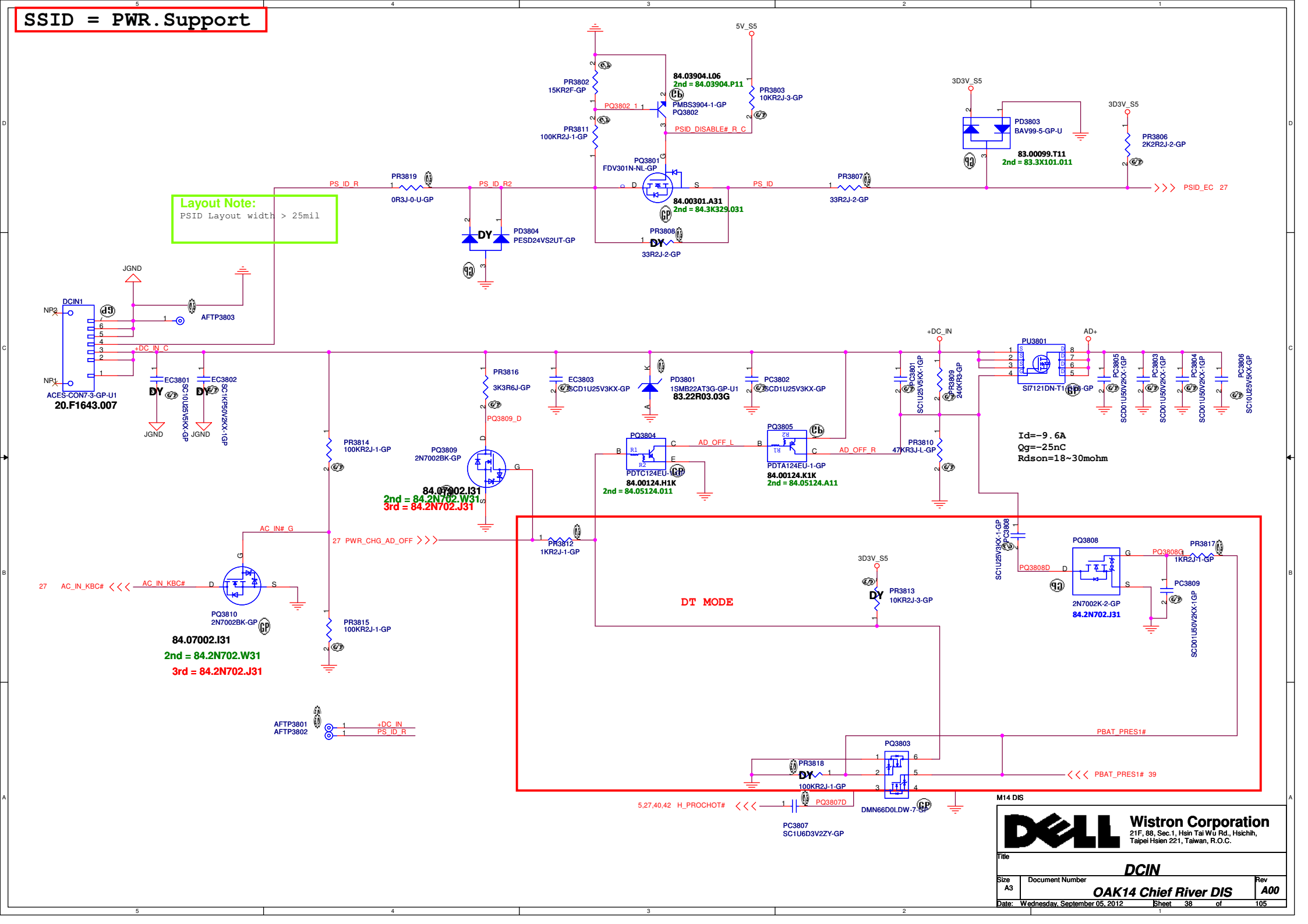
Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00

Date: Wednesday, September 05, 2012 Sheet 37 of 105

SSID = PWR.Support

Layout Note:
PSID Layout width > 25mil

DT MODE



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Title	DCIN	
Size A3	Document Number OAK14 Chief River DIS	Rev A00
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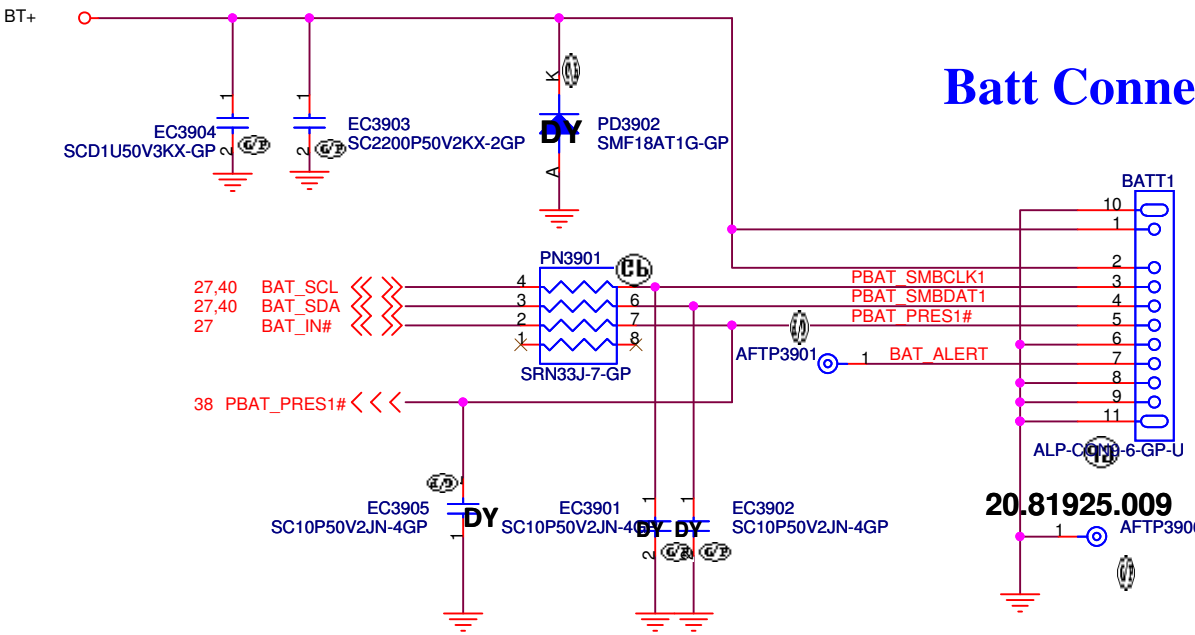
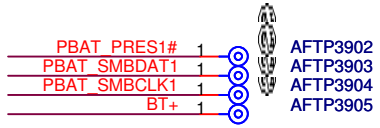
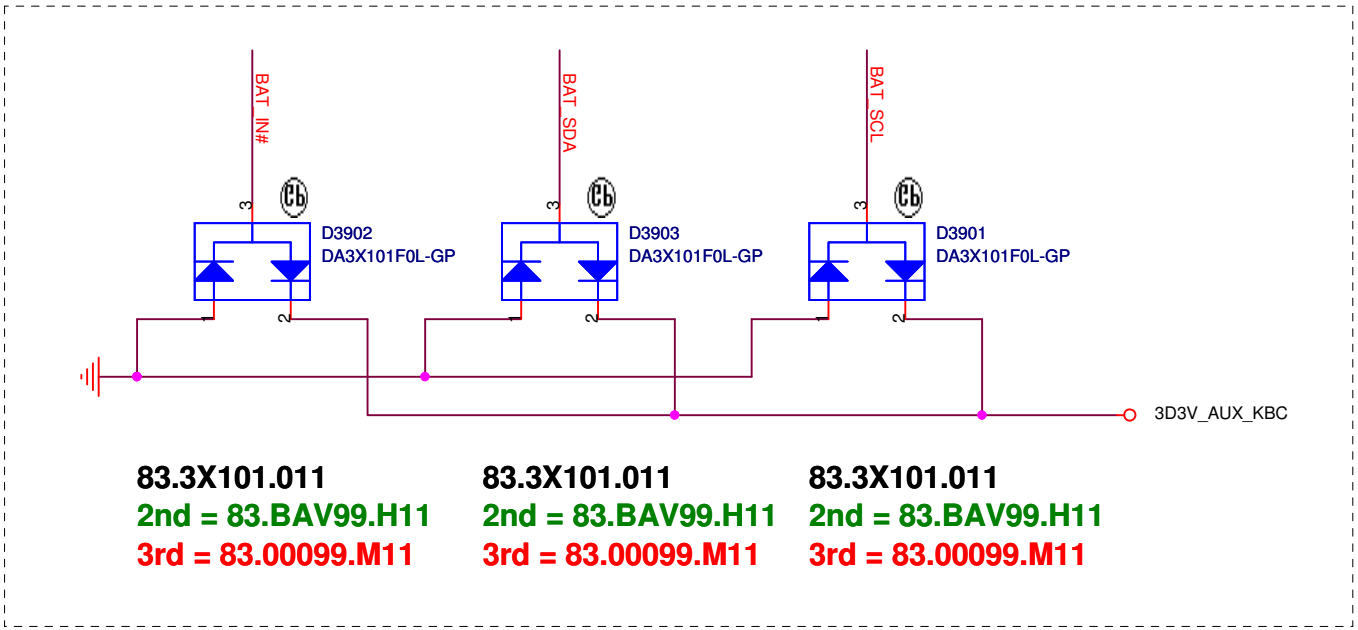
SSID = PWR.Support

Batt Connecter





Placement: Close to Batt Connector



83.3X101.011
2nd = 83.BAV99.H11
3rd = 83.00099.M11

83.3X101.011
2nd = 83.BAV99.H11
3rd = 83.00099.M11

83.3X101.011
2nd = 83.BAV99.H11
3rd = 83.00099.M11

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **BATT CONN**

Size	Document Number	Rev
A4	OAK14 Chief River DIS	A00

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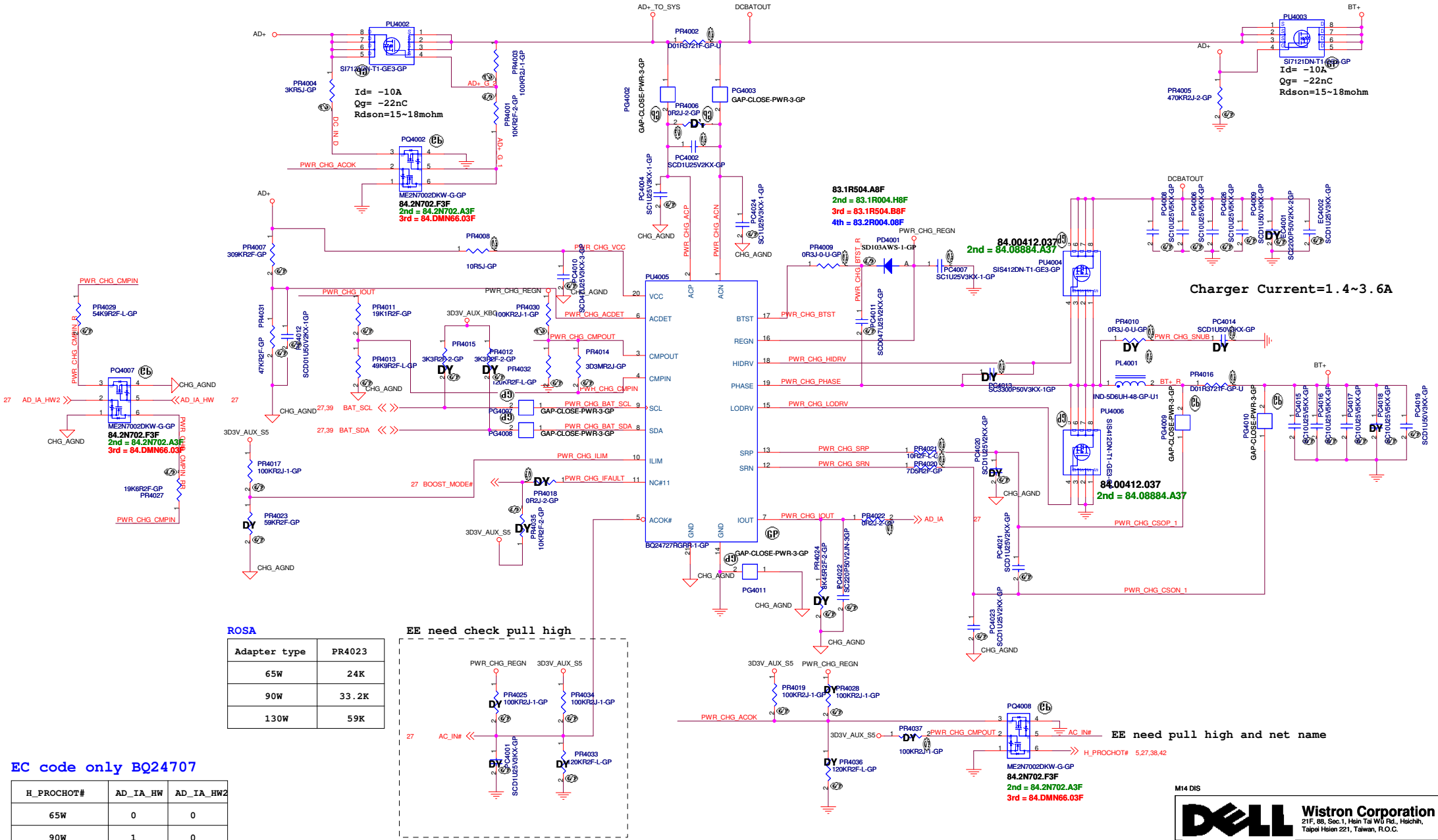
SSID = Charger



Adapter type	PR4023
65W	24K
90W	33.2K
130W	59K

H_PROCHOT#	AD_IA_HW	AD_IA_HW2
65W	0	0
90W	1	0
130W	0	1

M14 DIS

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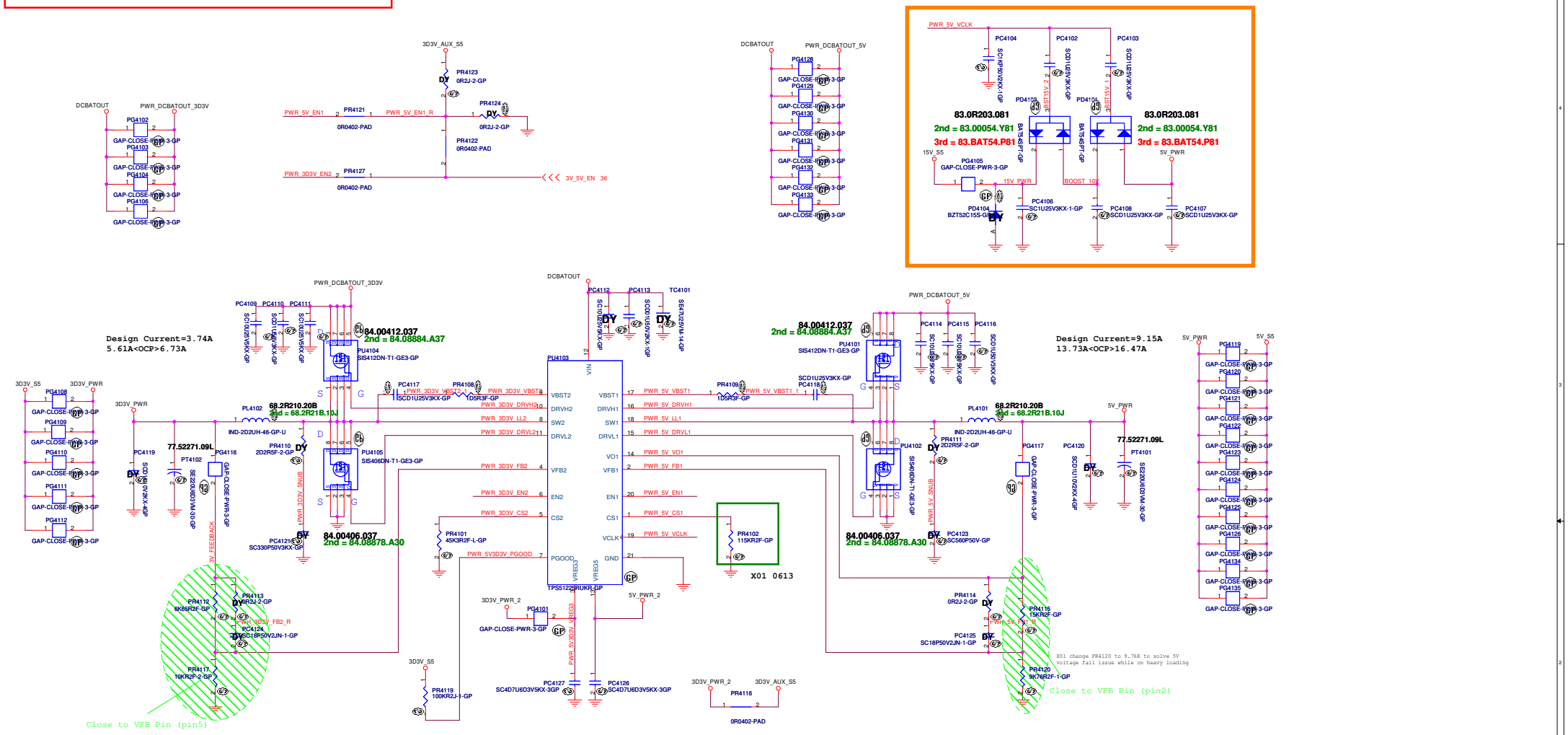
Title: CHARGER BQ24727

Size: Custom | Document Number: DNE40 14 CR DIS | Rev: A00

Date: Wednesday, September 05, 2012 | Sheet 40 of 105

SSID = PWR.Plane.Regulator_5v3p3v



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsuti/ 17mOhm / 77.52271.09L
H/S:SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS406DN-T1-GE3 / 11.5mOhm/14.5mOhm@4.5Vgs / 84.00406.037

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsuti/ 17mOhm / 77.52271.09L
H/S:SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS406DN-T1-GE3 / 11.5mOhm/14.5mOhm@4.5Vgs / 84.00406.037

M14 DIS

Wistron Corporation
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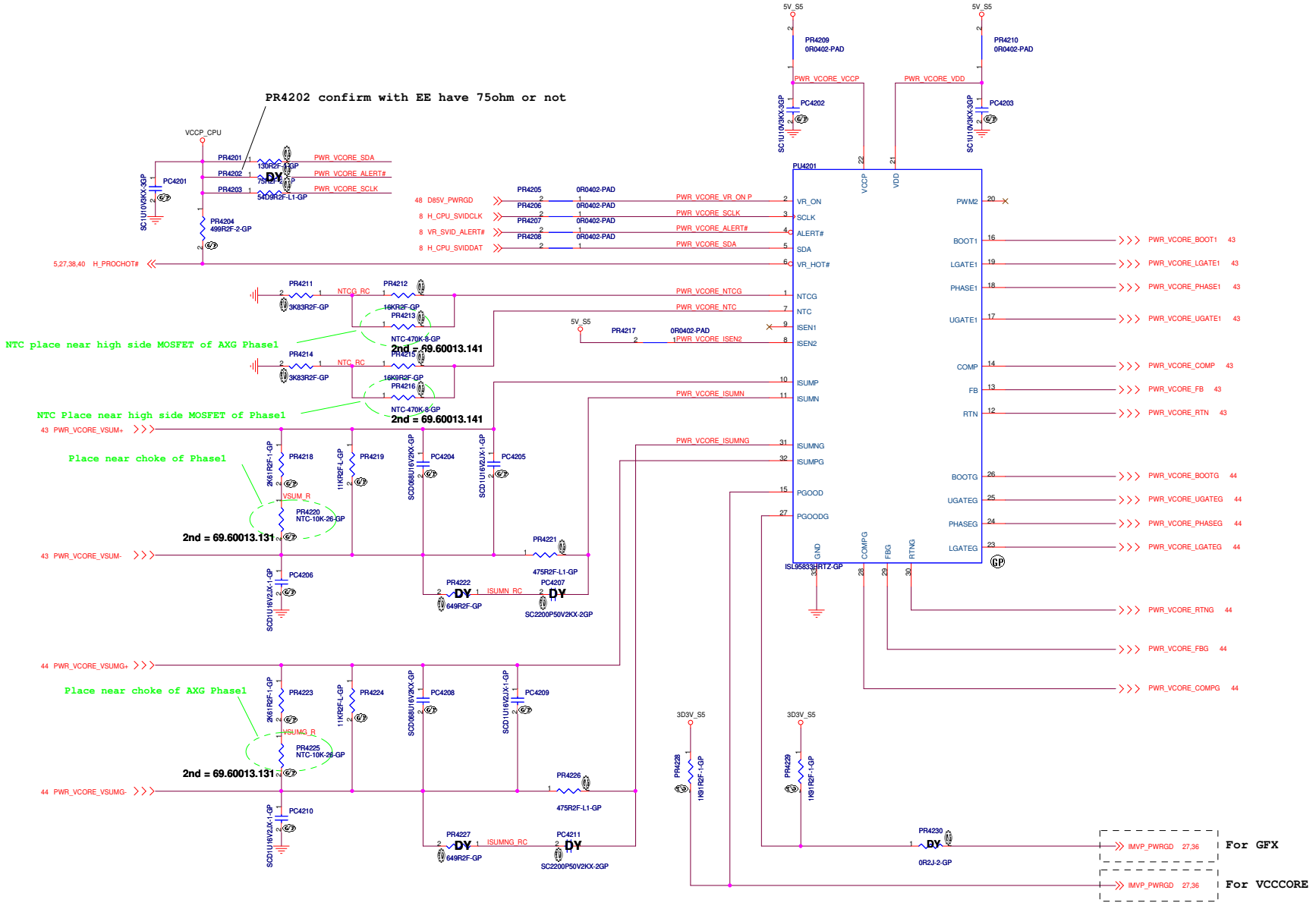
Taipei Hsien 221, Taiwan, R.O.C.

Title: 3V/5V TPS51225

Size: A2 | Document Number: OAK14 Chief River DIS | Rev: A00

Date: Wednesday, September 05, 2012 | Sheet 41 of 105

SSID = CPU.Regulator



M14 DIS

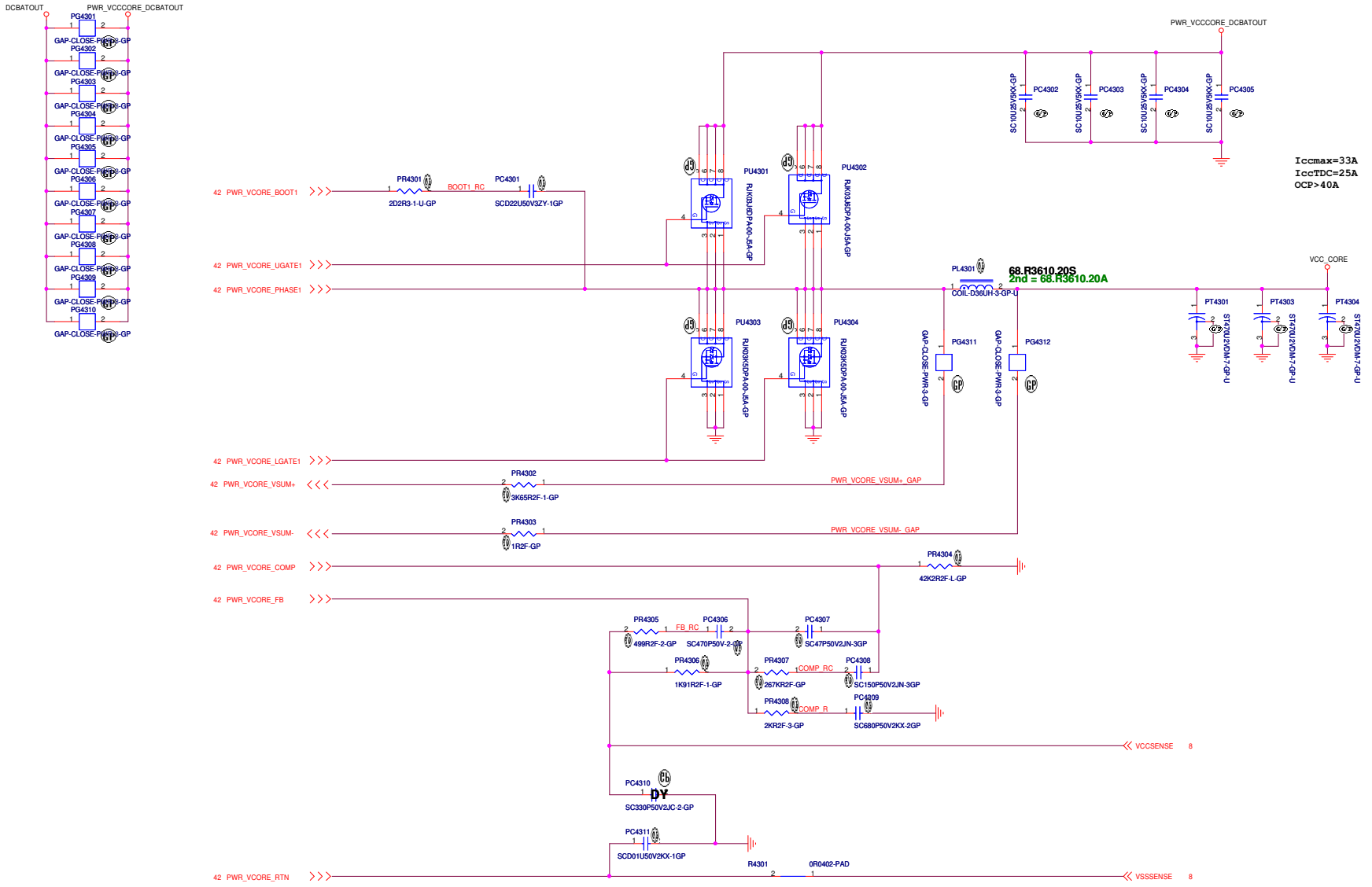
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95833_CPU_CORE(1/3)

Size	Document Number	Rev
C	OAK14 Chief River DIS	A00

Date: Wednesday, September 05, 2012 Sheet 42 of 105

SSID = CPU.Regulator



I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHK 0.36UH PCMC104T-R36MH 1.05mohm/ Isat =60A rms68.R3610.20S
O/P cap: CHIP CAP EL 470U 2V 7.3*4.3 ESR=0.0045 3.8Arms Panasonic/79.47719.9BL
H/S: RJK03J6DPA-00#J5A / 10mohm/13mOhm@4.5Vgs/ 84.00036.037
L/S: RJK03K5DPA-00#J5A / 3mohm/3.9mOhm@4.5Vgs/ 84.00035.037

M14 DIS

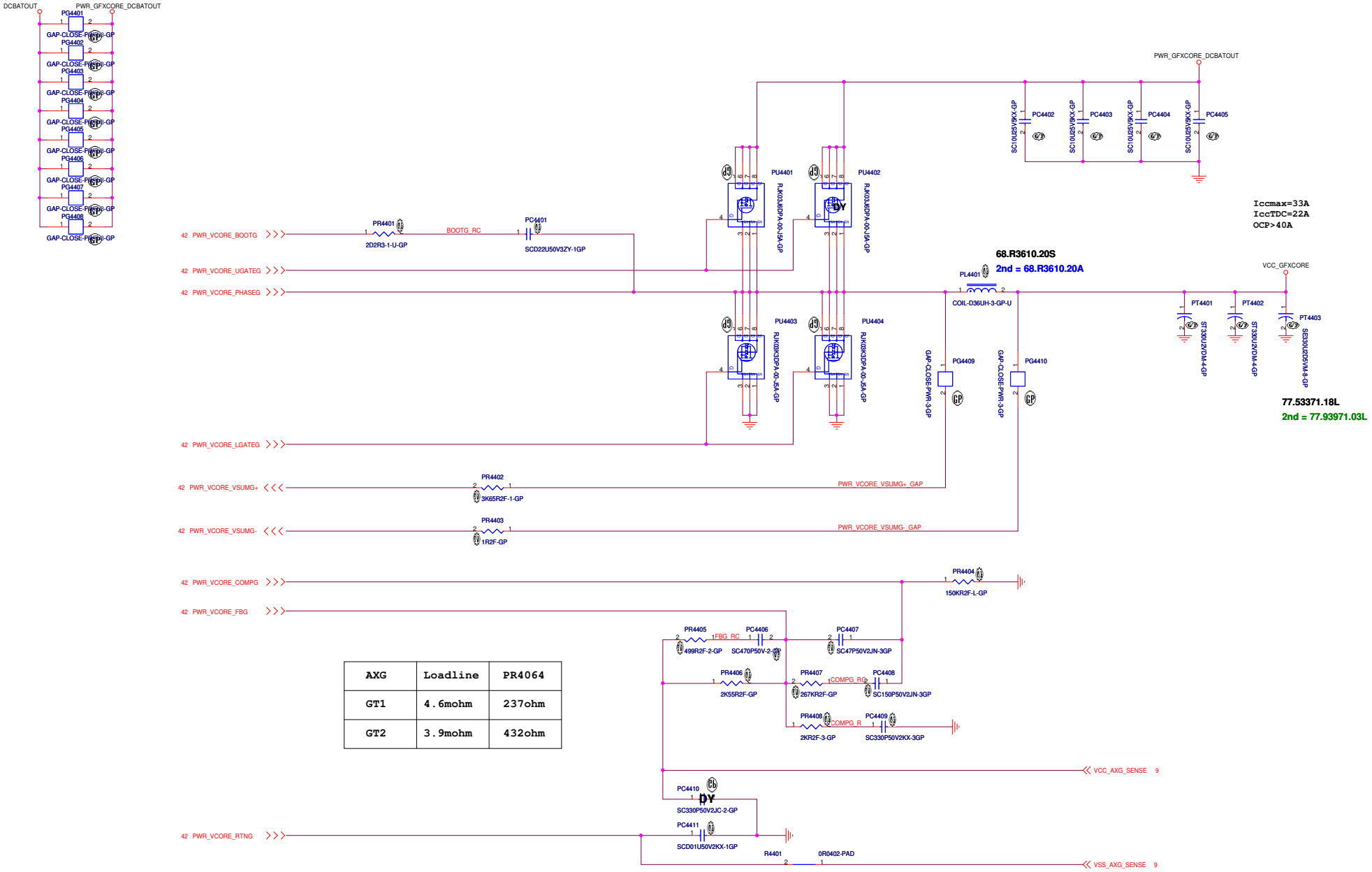
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95833_CPU_CORE(2/3)

Size	Document Number	Rev
C	OAK14 Chief River DIS	A00

Date: Wednesday, September 05, 2012 Sheet 43 of 105

SSID = CPU.Regulator



AXG	Loadline	PR4064
GT1	4.6mohm	237ohm
GT2	3.9mohm	432ohm

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHK 0.36UH PCMC104T-R36MH 1.05mohm/ Isat =60A rms68.R3610.20S
O/P cap: CHIP CAP 330U 2V EEFSX0D331XE 3.5Arms Panasonic/79.33719.20L
H/S: RJK03J6DPA-00#J5A / 10mohm/13mOhm@4.5Vgs/ 84.00036.037
L/S: RJK03K3DPA-00#J5A / 4.9mohm/6.1mOhm@4.5Vgs/ 84.003K3.037

M14 DIS

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

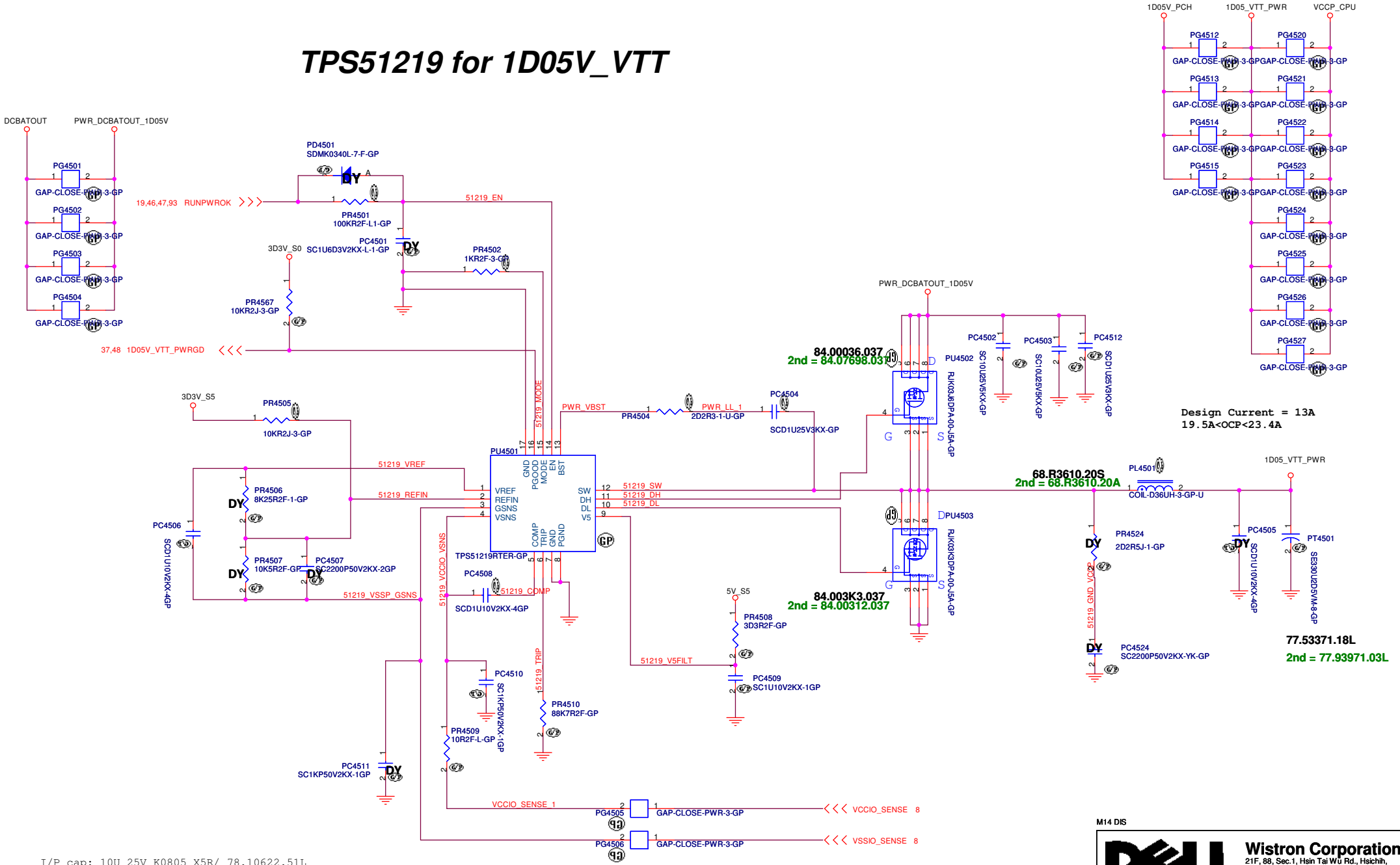
Title: ISL95833_CPU_CORE(3/3)

Size	Document Number	Rev
C	OAK14 Chief River DIS	A00

Date: Wednesday, September 05, 2012 Sheet 44 of 105

SSID = PWR.Plane.Regulator_1p05v_pch/vccp_cpu

TPS51219 for 1D05V_VTT



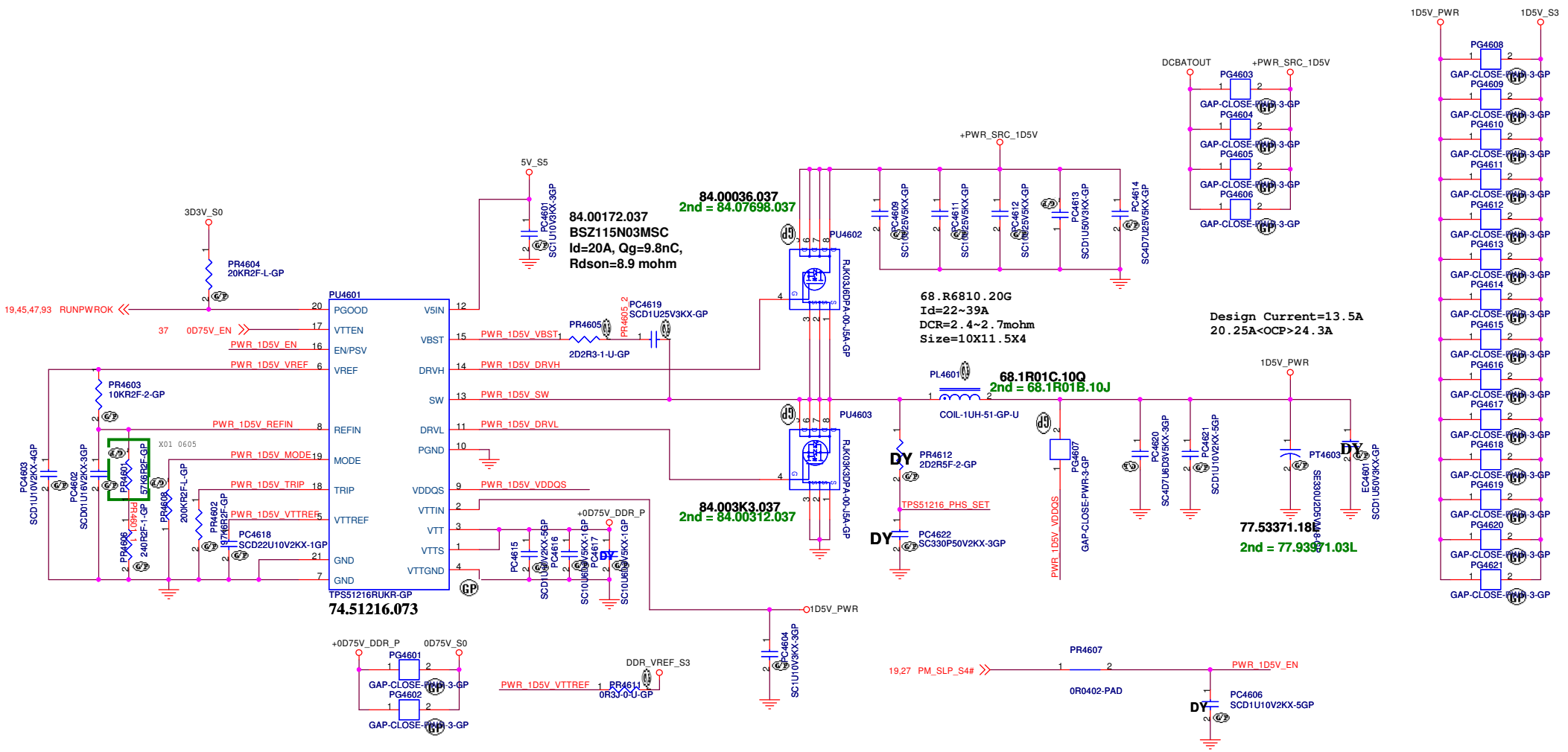
I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHK 0.36UH PCMC104T-R36MH 1.05mohm/ Isat =60A rms68.R3610.20S
O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L
H/S: RJK03J6DPA-00#J5A / 10mohm/13mOhm@4.5Vgs/ 84.00036.037
L/S: RJK03K3DPA-00#J5A / 4.9mohm/6.1mOhm@4.5Vgs/ 84.003K3.037

M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	TPS51219 1D05V_VTT	
Size A3	Document Number DNE40 14 CR DIS	Rev A00
Date: Wednesday, September 05, 2012	Sheet 45 of 105	

SSID = PWR.Plane.Regulator 1p5v0p75v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE

PR4608	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 1.0UH PCMB104T-1R0M/ 3.3mohm/ Isat =28A rms /68.1R01C.10Q
O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L
H/S: RJK03J6DPA-00#J5A / 10mohm/13mOhm@4.5Vgs/ 84.00036.037
L/S: RJK03K3DPA-00#J5A / 4.9mohm/6.1mOhm@4.5Vgs/ 84.003K3.037

M14 DIS

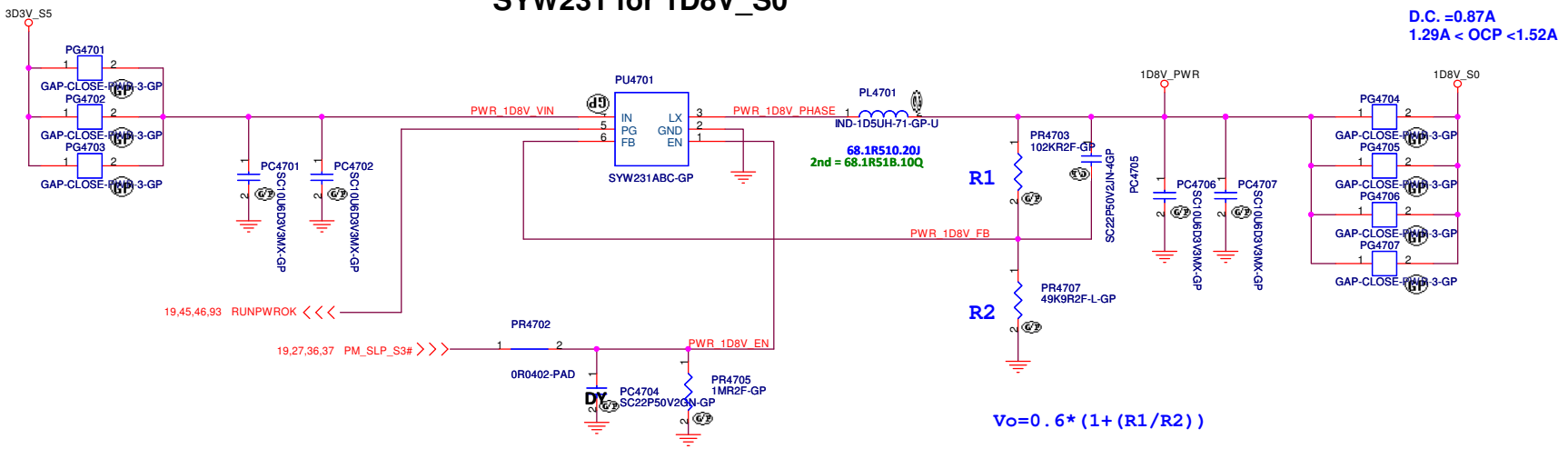
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51216_+1.5V_SUS

Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00

Date: Wednesday, September 05, 2012 Sheet 46 of 105

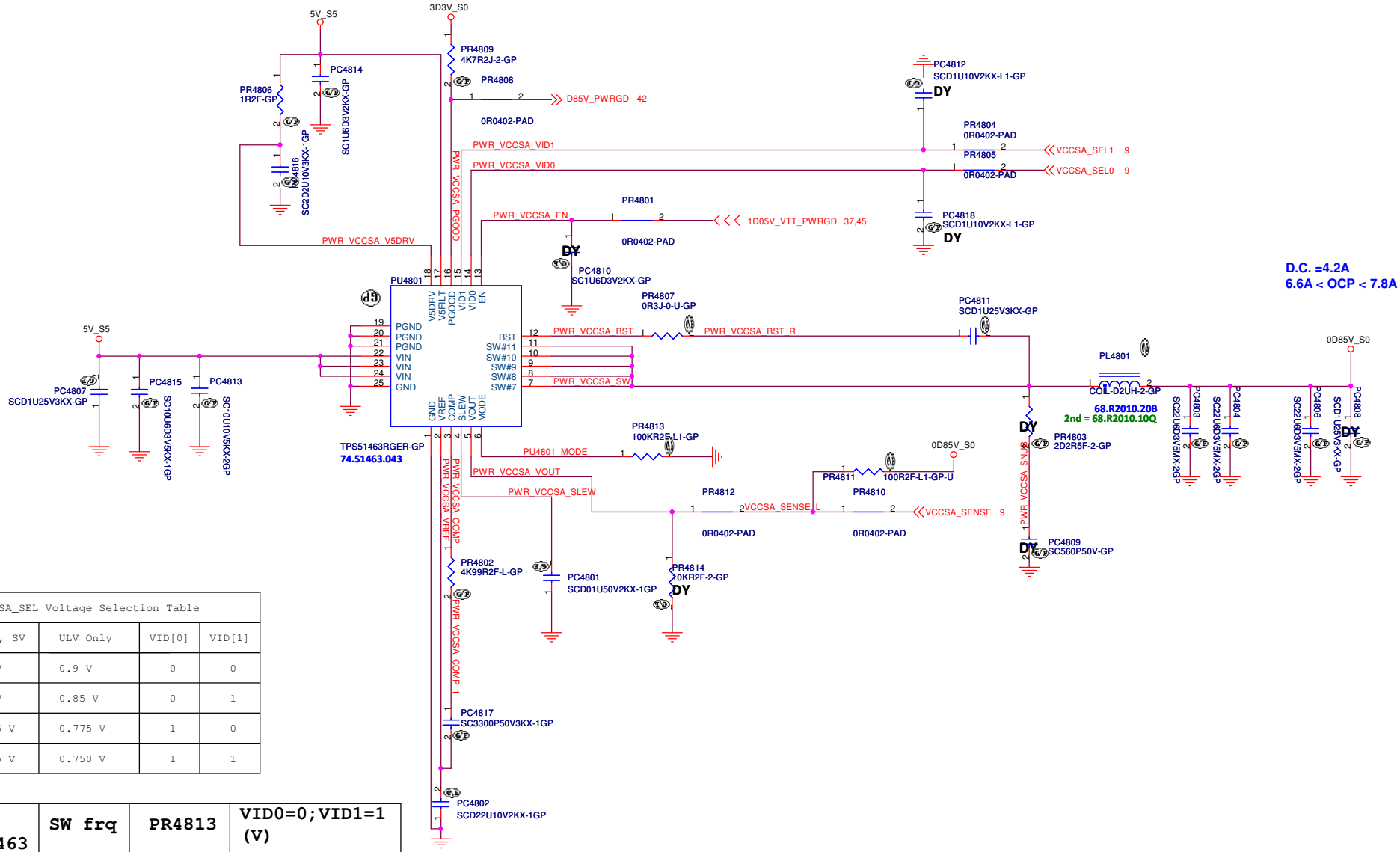
SYW231 for 1D8V_S0



M14 DIS

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *SYW231_1D8V_S0*		
Size: A3	Document Number: *OAK14 Chief River DIS*	Rev: *A00*
Date: Wednesday, September 05, 2012	Sheet 47 of 105	

SSID = PWR.Plane.Regulator_0p85v



VCCSA_SEL Voltage Selection Table			
XE, QC, SV	ULV Only	VID[0]	VID[1]
0.9 V	0.9 V	0	0
0.8 V	0.85 V	0	1
0.725 V	0.775 V	1	0
0.675 V	0.750 V	1	1

	SW frq	PR4813	VID0=0;VID1=1 (V)
TPS51463 for ULV	700KHz	100K	0.85
	1MHz	Open	0.85

M14 DIS

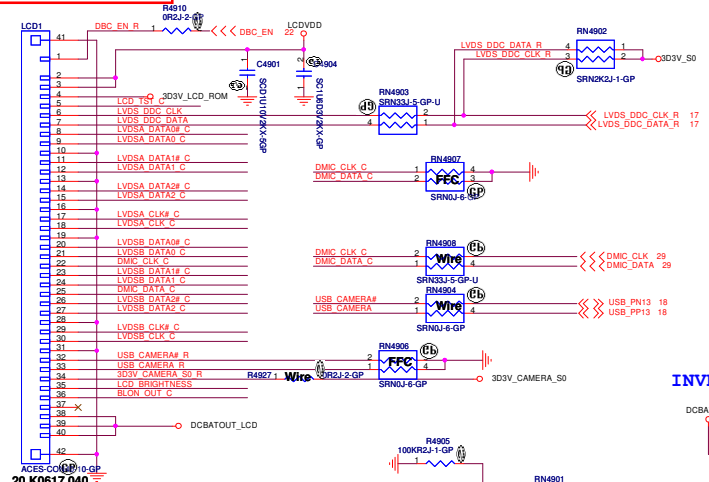
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51463_VCCSA

Size: A3 | Document Number: OAK14 Chief River DIS | Rev: A00

Date: Wednesday, September 05, 2012 | Sheet 48 of 105

SSID = VIDEO

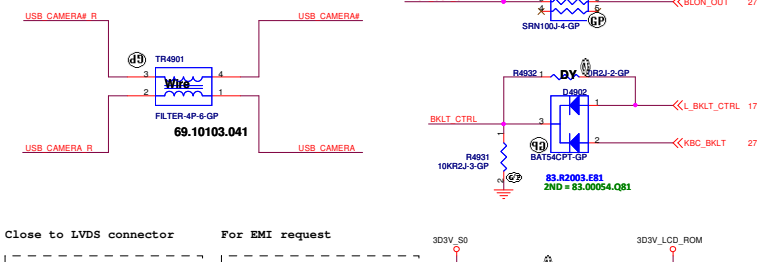


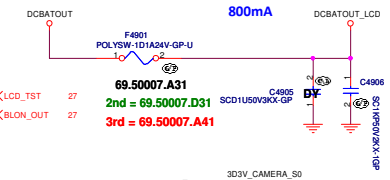
CN Table	
1	Diag_loop
2	USB+
3	USB-
4	3.3V
5	MIC_CLK
6	MIC_GND
7	MIC_SIG
8	DGND

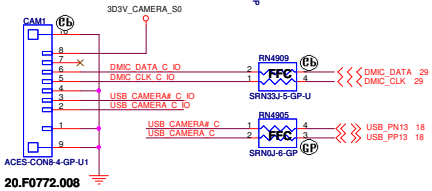
MB Connecter		是否接線	Wire (40 PIN)	FFC(40 PIN)
Pin 10	GND	Y	Pin 10(GND 實體線)	Pin 10 GND
Pin 13	GND	Y	Pin 13(GND 實體線)	Pin 13 GND
Pin 16	GND	Y	Pin 16 (GND實體線)	Pin 16 GND
Pin 19	GND	Y	Camera Module Pin 6 DMIC_GND(實體線)	Pin 19 GND
Pin 22	GND	Y	Camera Module Pin 5 AUD_DMIC_CLK	Pin 22 GND
Pin 25	GND	Y	Camera Module Pin 7 AUD_DMIC_IN0	o
Pin 28	GND	Y	Camera Module Pin 8 CCD GND(實體線)	Pin 28 GND
Pin 31	GND	Y	Pin 31 (實體線)	Pin 31 GND
Pin 32	GND	Y	Camera Module Pin 3 USB_CAMERA#	Pin 32 GND
Pin 33	GND	Y	Camera Module Pin 2 USB_CAMERA	Pin 33 GND
Pin 34	3D3V_CAMERA_S0	Y	Camera Module Pin 4 3D3V_CAMERA_S0	NC(0 ohm DY)

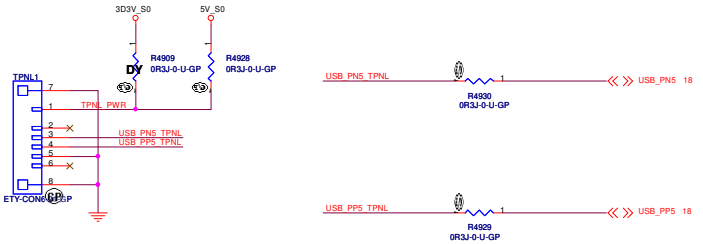
PIN	MB Connecter	是否接線	PIN	Camera Module Conn
1	DGND	Y	8	DGND
2	USB_CAMERA_C (USB+)	Y	2	USB_CAMERA_C (USB+)
3	USB_CAMERA#_C (USB-)	Y	3	USB_CAMERA#_C (USB-)
4	DMIC_GND	Y	6	DMIC_GND
5	DMIC_CLK_C	Y	5	DMIC_CLK_C
6	DMIC_DATA_C	Y	7	DMIC_DATA_C
7	NC	N	1	NC
8	3D3V_CAMERA_S0	Y	4	3D3V_CAMERA_S0

INVERTER POWER

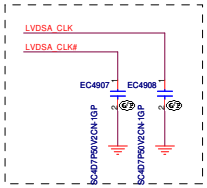




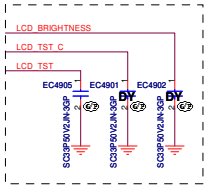


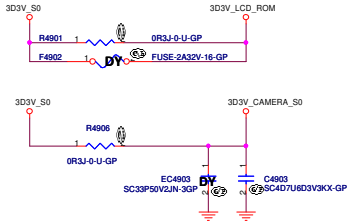


Close to LVDS connector

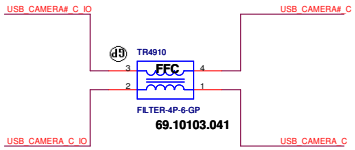


For EMI request

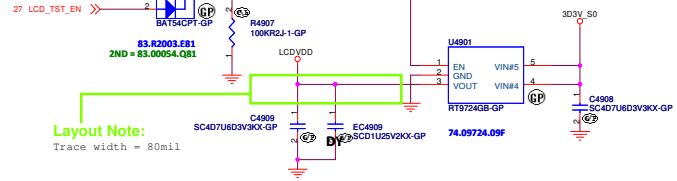




Close to Camera connector



SSID = VIDEO



M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD Connector

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(Blanking)

M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Connector

Size: A3 | Document Number: OAK14 Chief River DIS | Rev: A00

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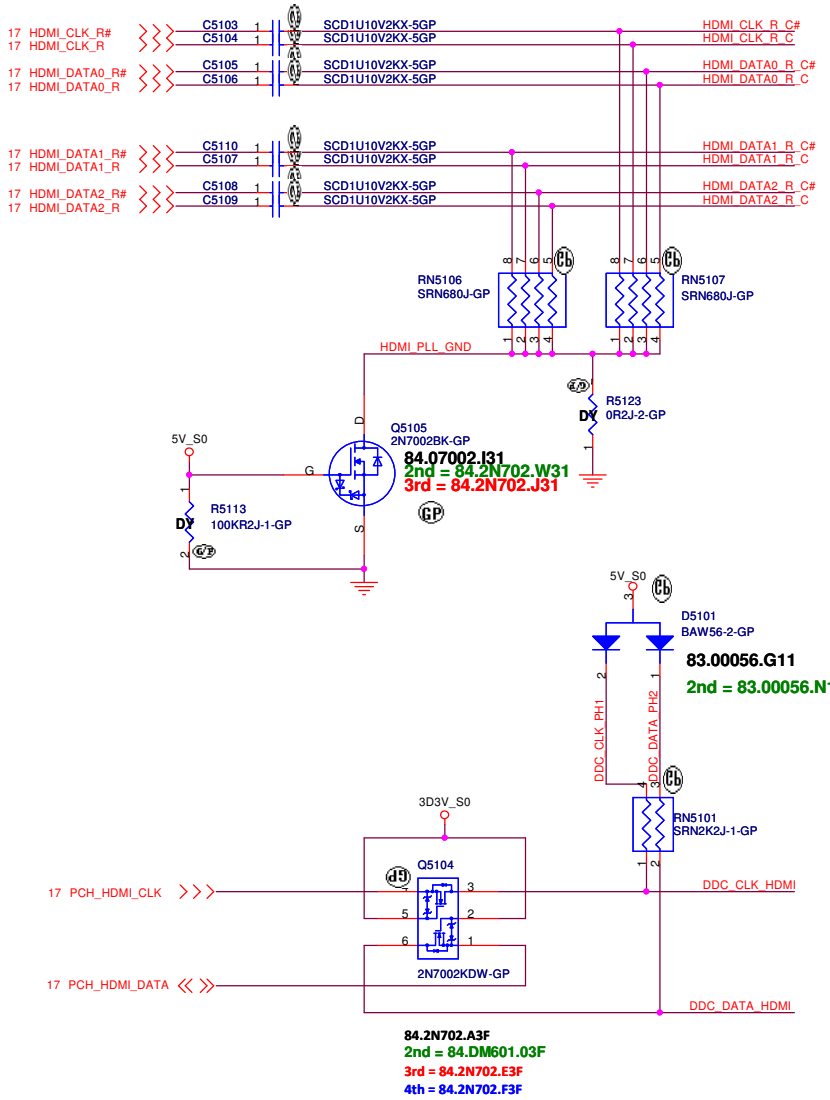
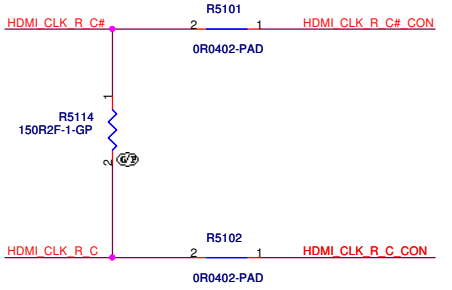
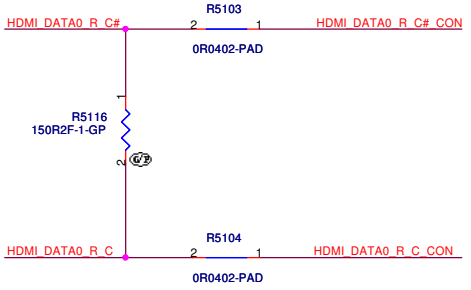
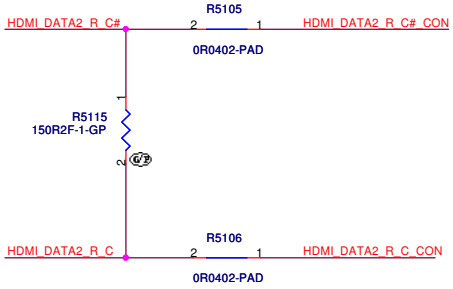
SSID = VIDEO

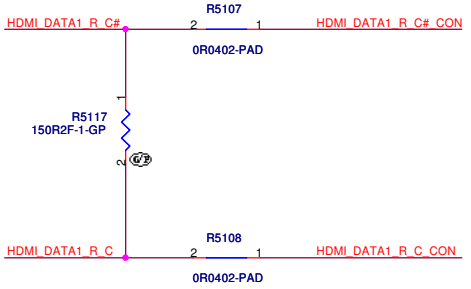
HDMI Level Shifter

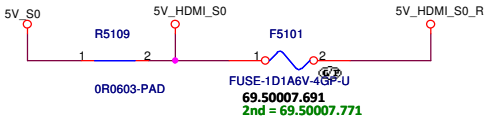




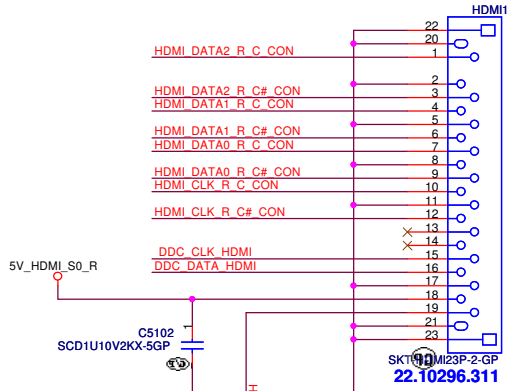


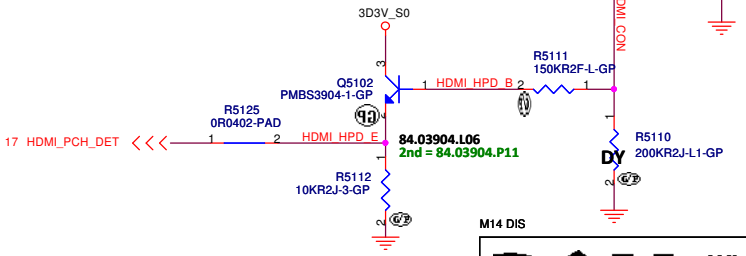






HDMI CONN





M14 DIS

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDMI Level Shifter/Connector		
Size: A3	Document Number: OAK14 Chief River DIS	Rev: A00
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(Blanking)

M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *OAK14 Chief River DIS* | Rev: *A00*

Date: Wednesday, September 05, 2012 | Sheet 52 of 105

(Blanking)

M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LVDS_Switch*

Size: A3 | Document Number: *OAK14 Chief River DIS* | Rev: *A00*

Date: Wednesday, September 05, 2012 | Sheet 53 of 105

(Blanking)

M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A3	*OAK14 Chief River DIS*	*A00*

SSID = User.Interface

(Blanking)

M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ITP/Fan Connector

Size: A3 | Document Number: OAK14 Chief River DIS | Rev: A00

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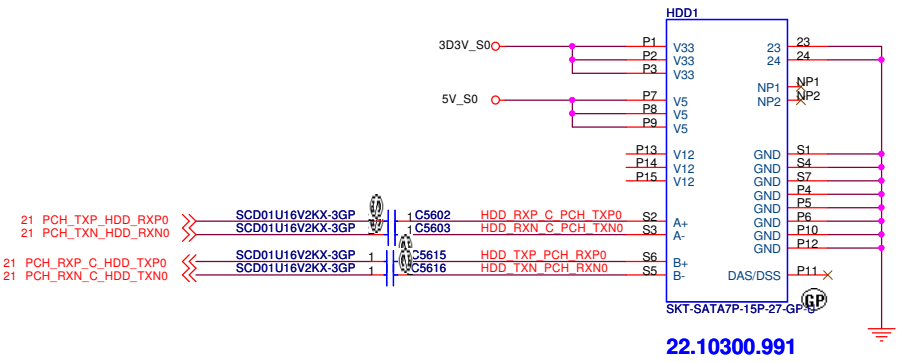
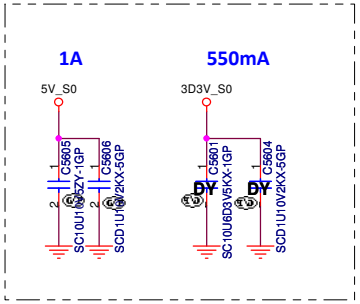
SSID = SATA

SATA HDD Connector

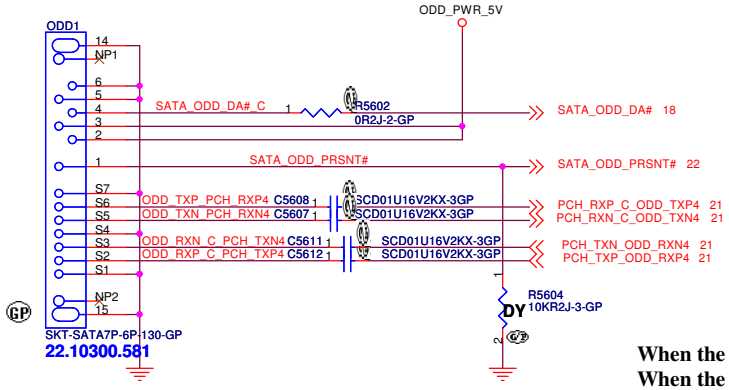


22.10300.991

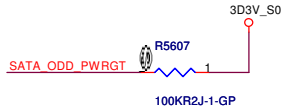


Close to HDD1

ODD Connector



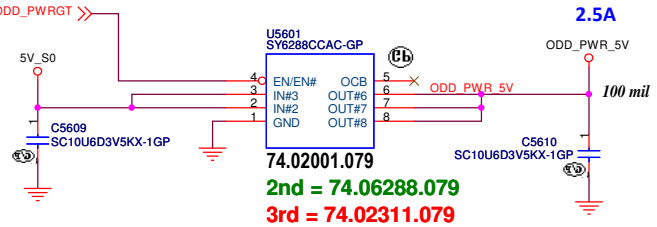
22.10300.581



follow CKL1.5

SUPPORT ZERO SATA ODD

SATA Zero Power ODD



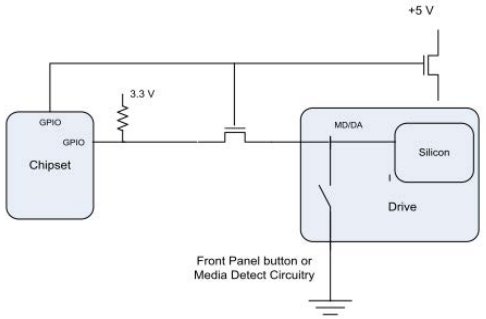
74.02001.079

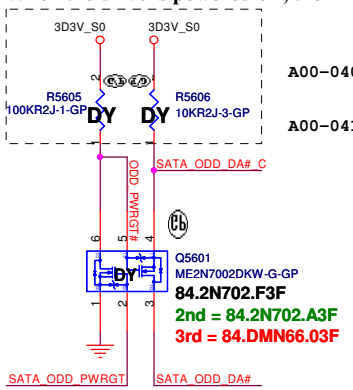
2nd = 74.06288.079

3rd = 74.02311.079

Current limit
Active High
typ =>2.5A

When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON





84.2N702.F3F

2nd = 84.2N702.A3F

3rd = 84.DMN66.03F

A00-0408 Add R5606 to pull high 3.3V_S0
Change pull high to 3.3V_S0

A00-0415 Dummy R5606

M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

Size: A3 | Document Number: OAK14 Chief River DIS | Rev: A00

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SSID = ESATA

(Blanking)

M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ESATA

Size: A3 | Document Number: OAK14 Chief River DIS | Rev: A00

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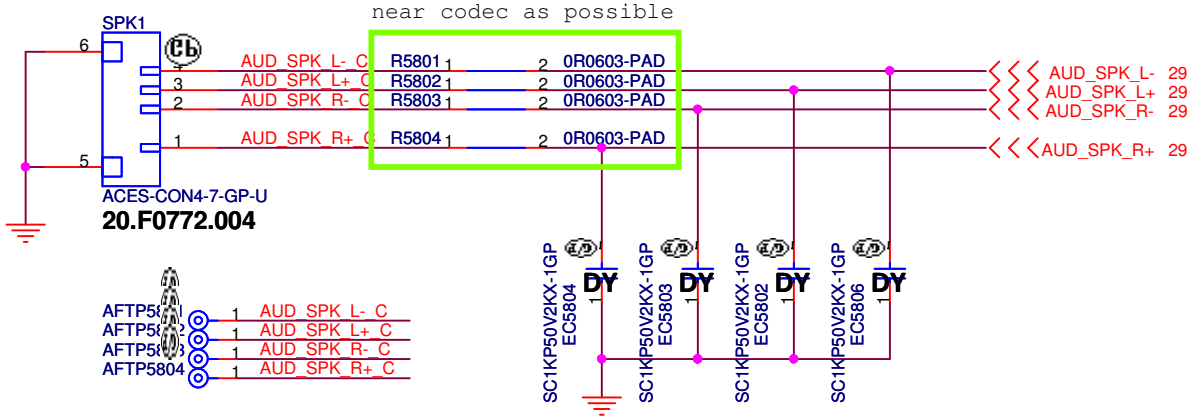
SSID = AUDIO

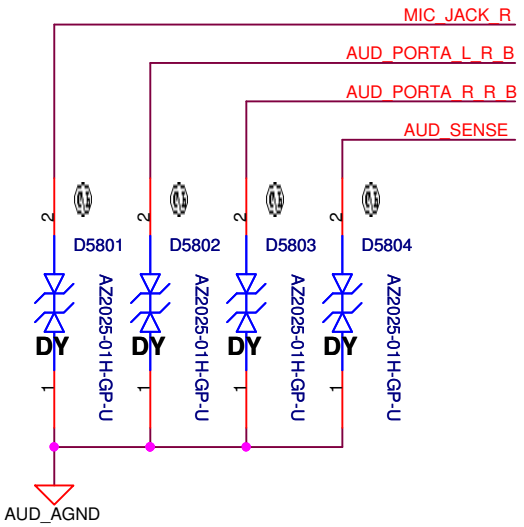
X01 0605

Speaker

Layout Note:
trace width=30mil

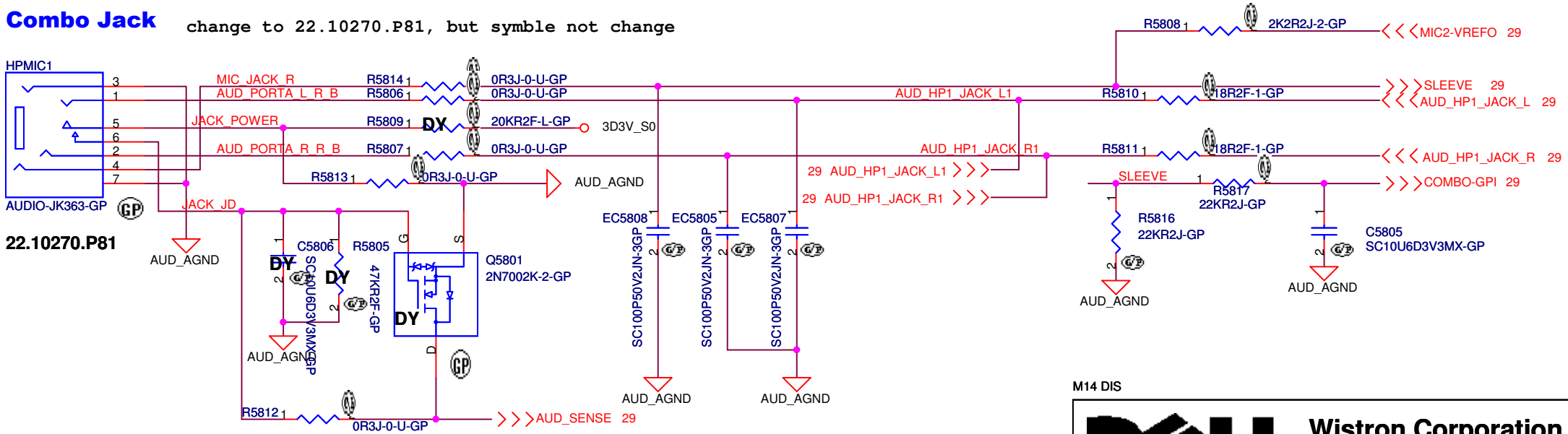
R5801~R5804 and EC5804~EC5806
near codec as possible





Combo Jack

change to 22.10270.P81, but symble not change



M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Speaker/HPMIC CONN**

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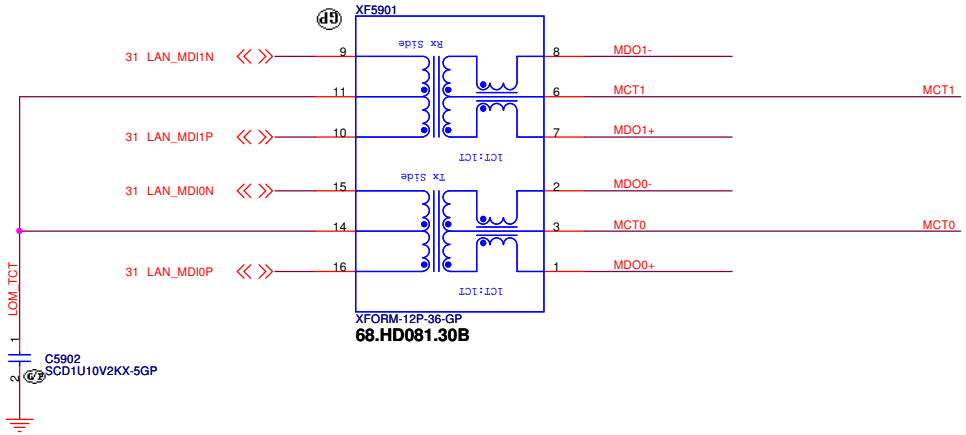
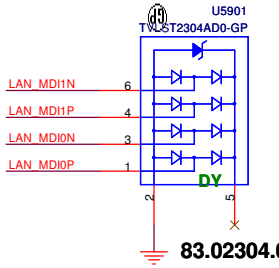
Date: Wednesday, September 05, 2012 Sheet 58 of 105

SSID = LOM

LAN TransFormer

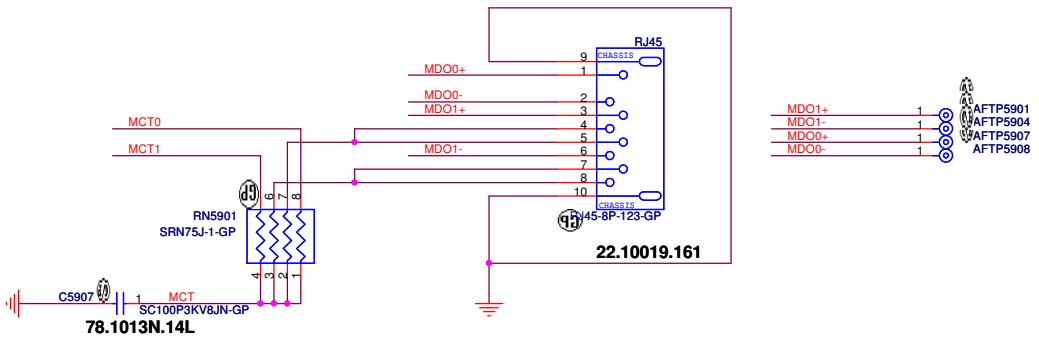


X01 0605



83.02304.0AE
2nd = 83.42236.0AE
3rd = 83.08902.0AE
4th = 83.09904.AAE

RJ45



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: XFOM&RJ45

Size: A3 | Document Number: OAK14 Chief River DIS | Rev: A00

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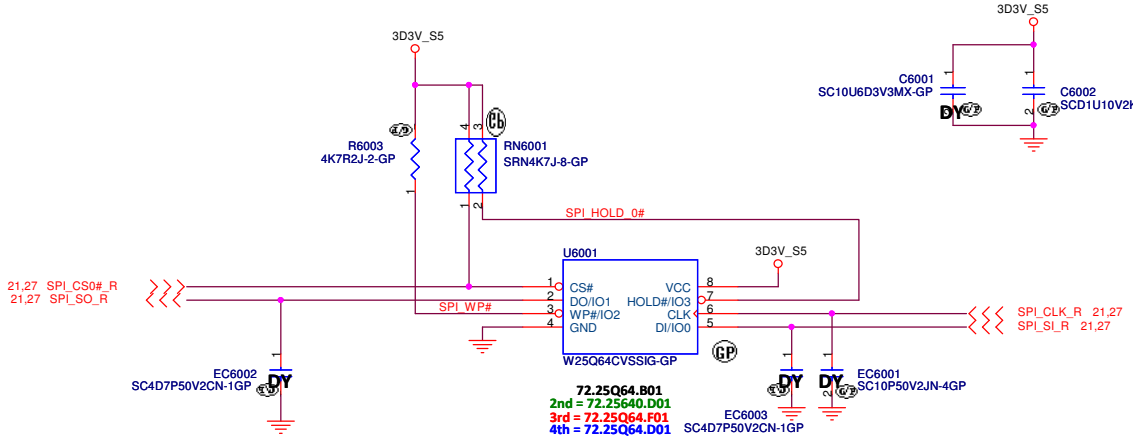
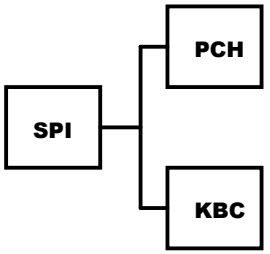
SSID = Flash.ROM

SPI Flash ROM(8M) for PCH

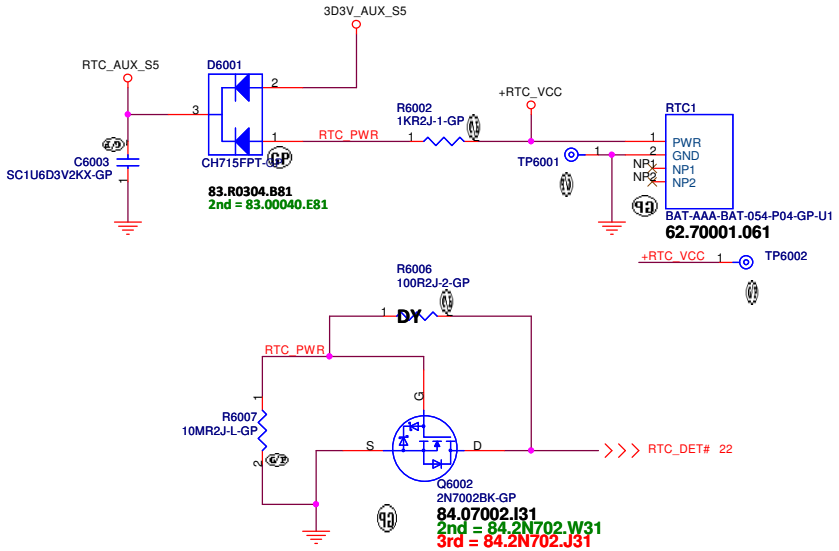




Layout Note:

KBC----10"----PCH
KBC----1.5"~6.5"----SPI
PCH----0.5"~6.5"----SPI

SSID = RBATT



M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC		
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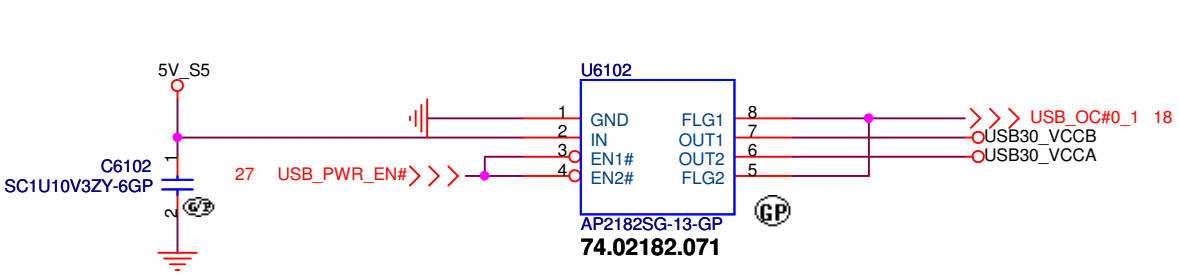
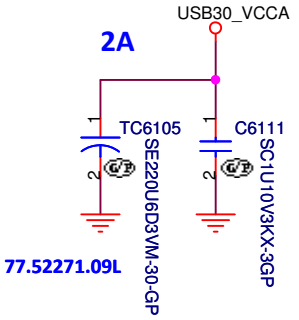
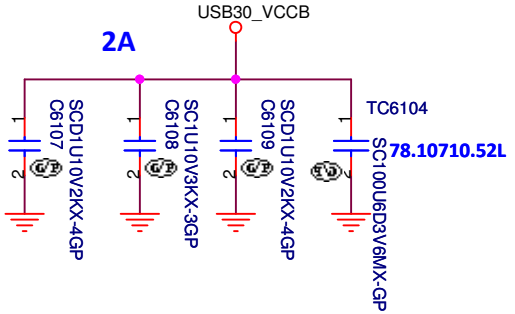




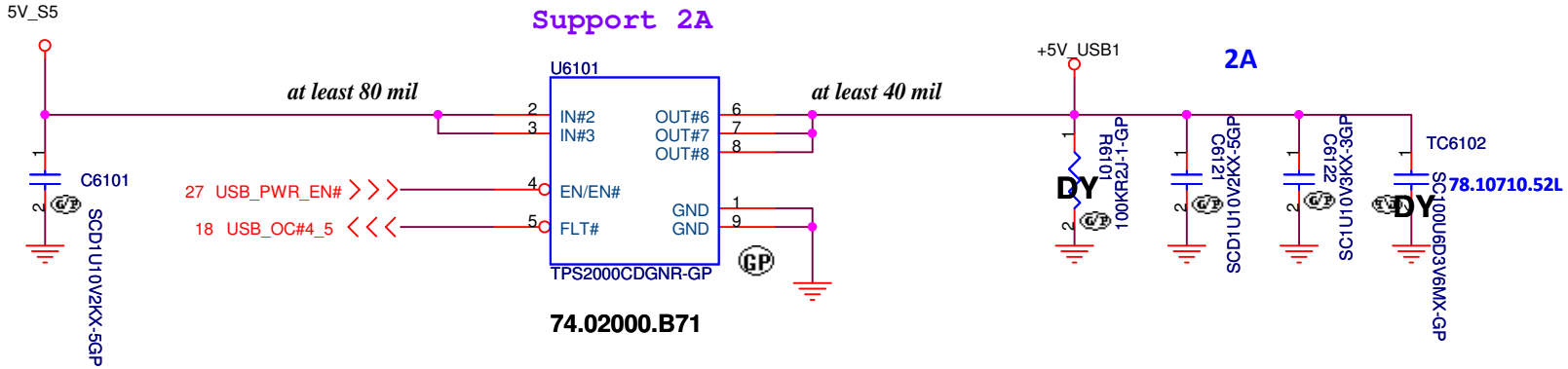
USB3.0 Port1



USB3.0 Port2

Right USB Power x1

Support 2A

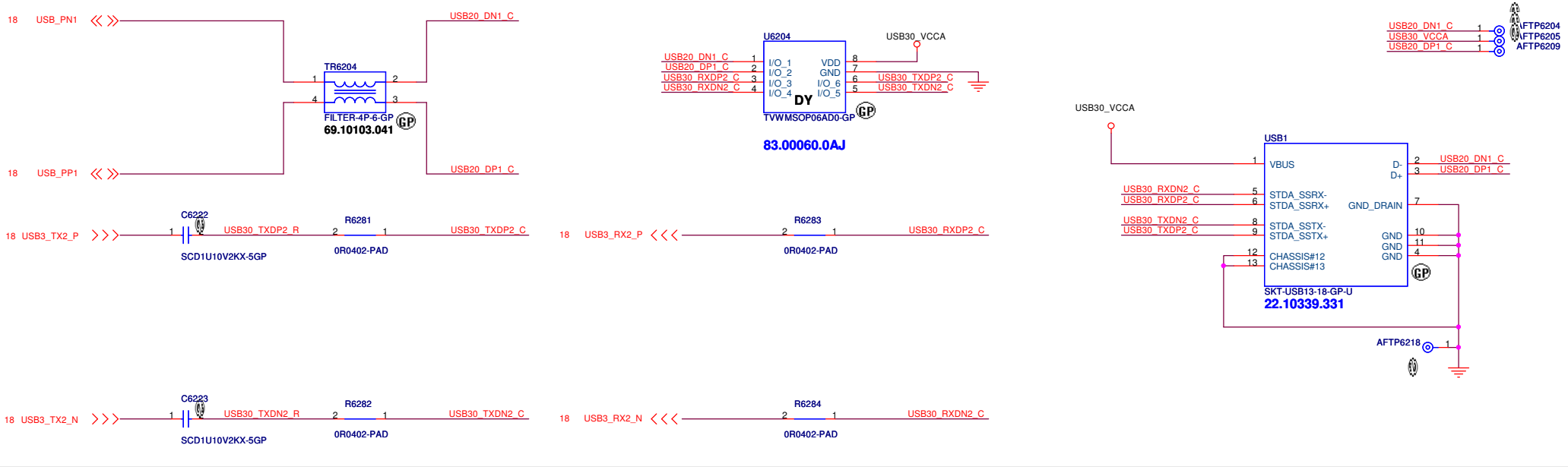


M14 DIS

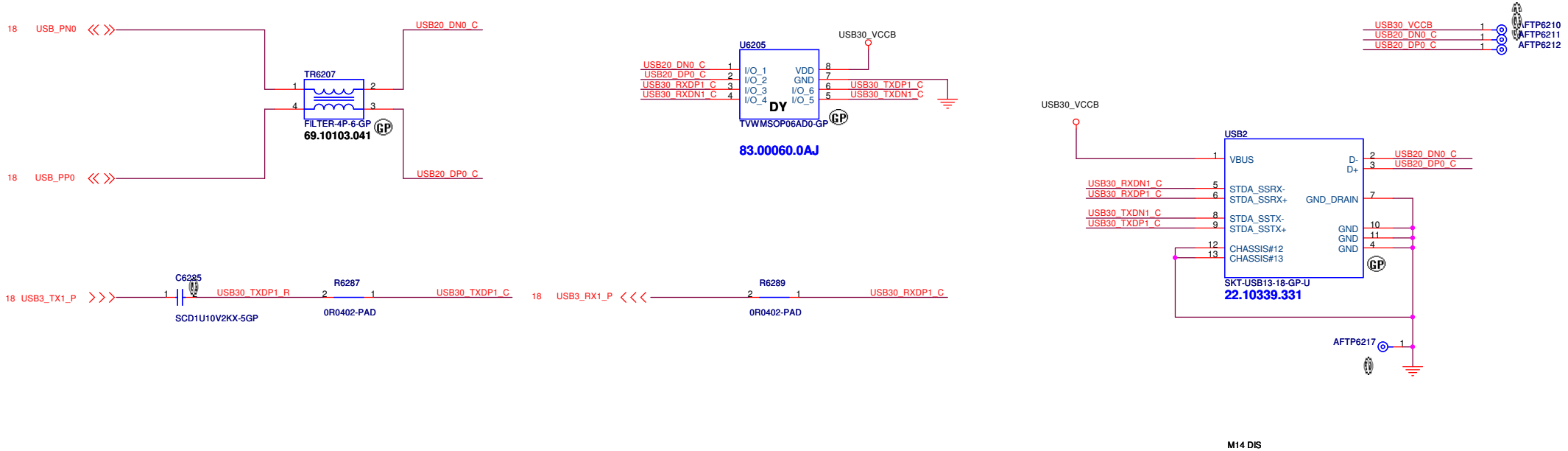
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *USB Power SW*		
Size	Document Number: *OAK14 Chief River DIS*	Rev: *A00*
Date: Wednesday, September 05, 2012	Sheet 61 of 105	

SSID = USB

USB3.0 Port1



USB3.0 Port2



M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB 3.0

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SSID = USB

(Blanking)

M14 DIS

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB3.0 PORT

Size: A3 | Document Number: OAK14 Chief River DIS | Rev: A00

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(Blanking)

M14 DIS

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Title: *RESERVED*

Size: A3 | Document Number: *OAK14 Chief River DIS* | Rev: *A00*

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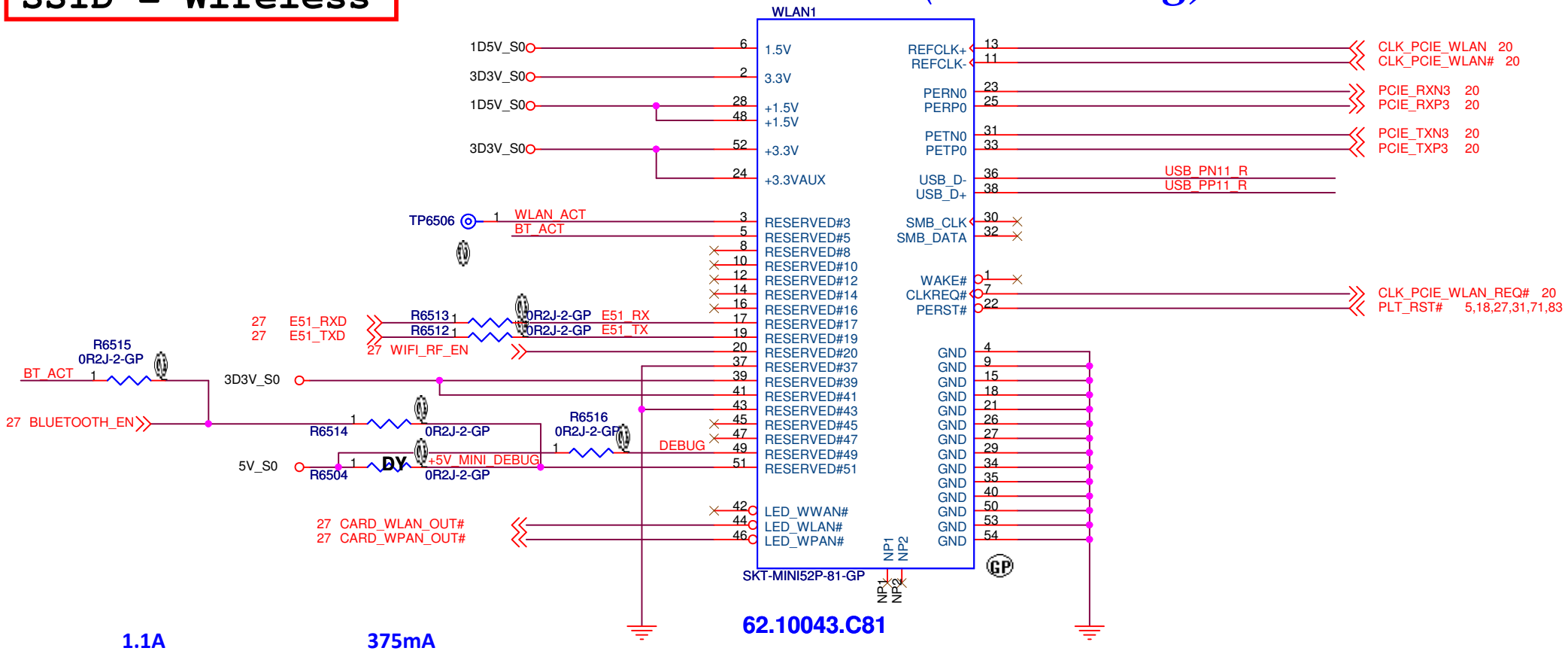
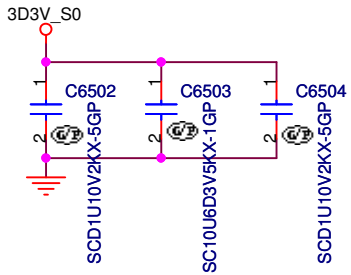
Mini Card Connector(802.11a/b/g)

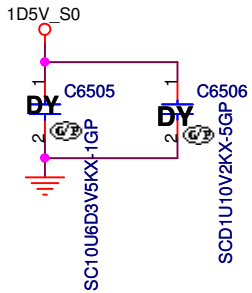
SSID = Wireless

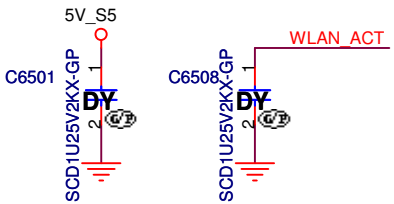


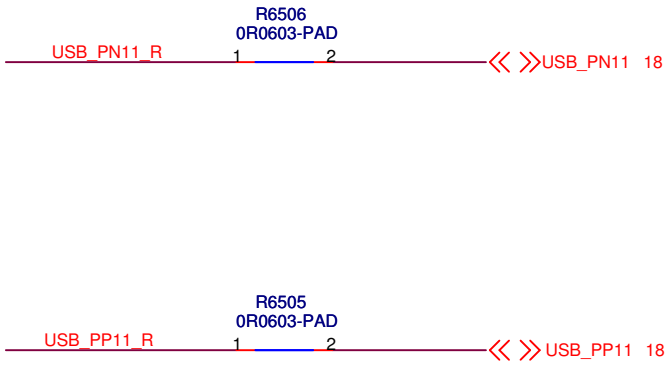
1.1A



375mA







M14 DIS

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINICARD(WLAN)/ITP CONN

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M14 DIS

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Title

Reserved

Size	Document Number	Rev
A3	*OAK14 Chief River DIS*	*A00*

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M14 DIS

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Title

Reserved

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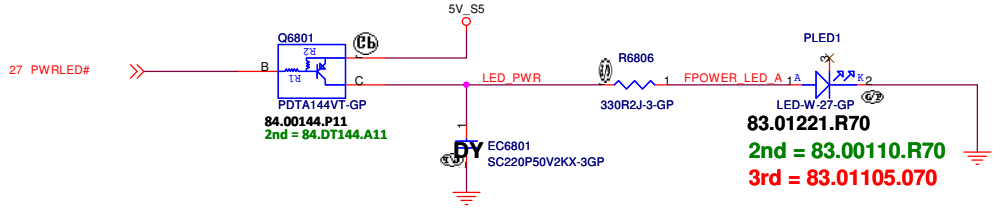
SSID = User.Interface

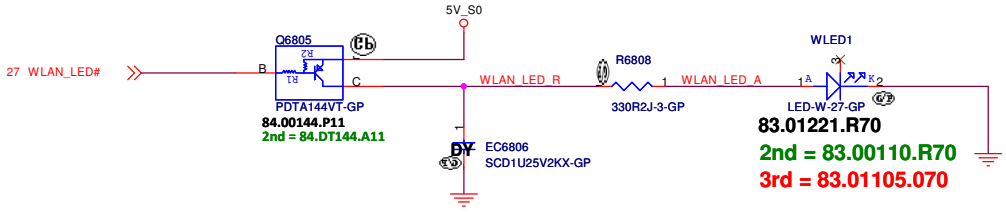
FRONT POWER LED

Low actived from KBC GPIO



Wireless LED

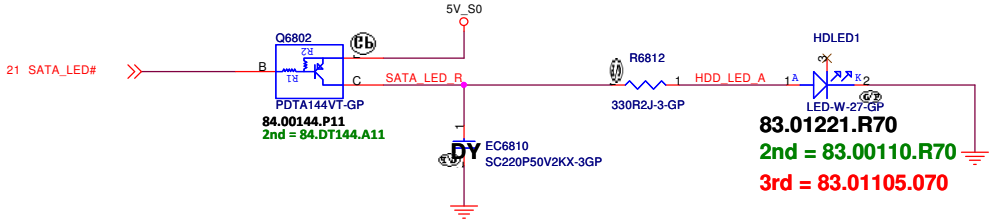
Low actived from KBC GPIO



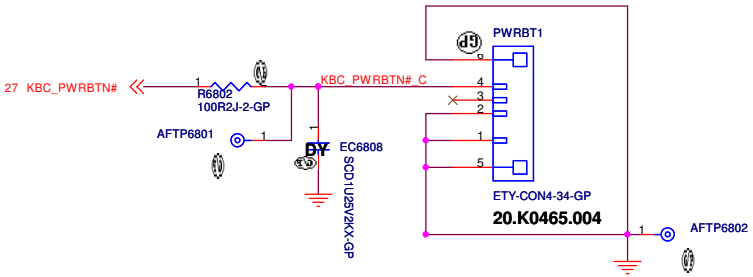
Place EC6806 near WLED1

SATA HDD LED(White)

Low actived from PCH GPIO

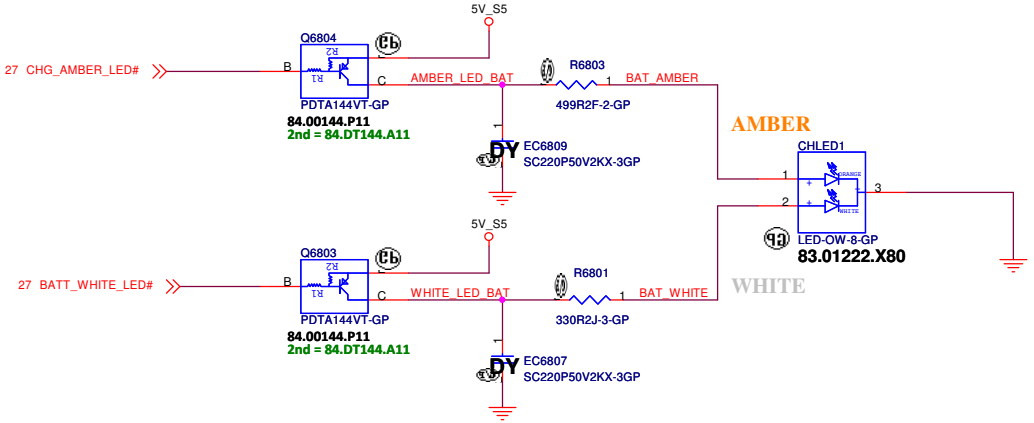


Power button



Battery LED1 (AMBER_LED)

Low actived from KBC GPIO



Battery LED2 (WHITE_LED)

Low actived from KBC GPIO

M14 DIS

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Title: LED Bard/Power Button

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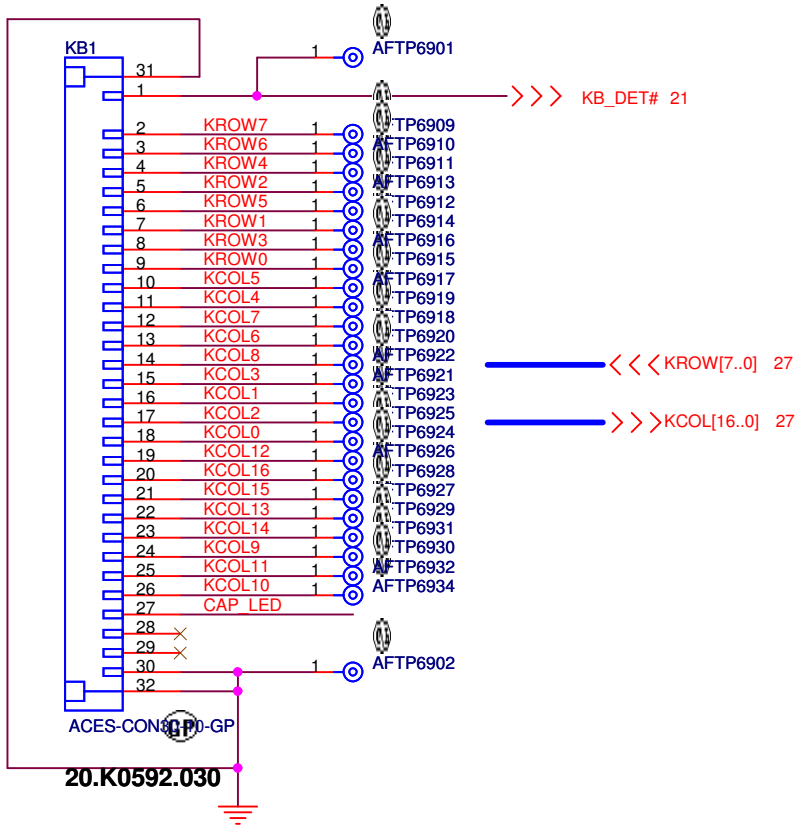
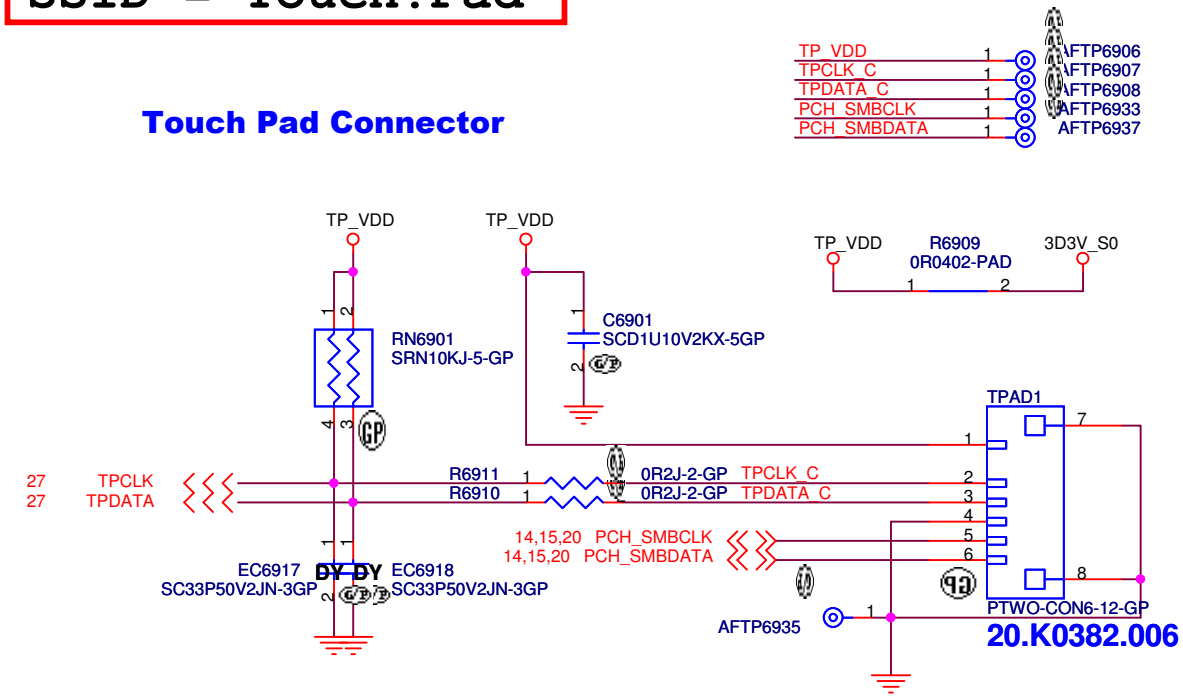
SSID = KBC

Internal Keyboard Connector



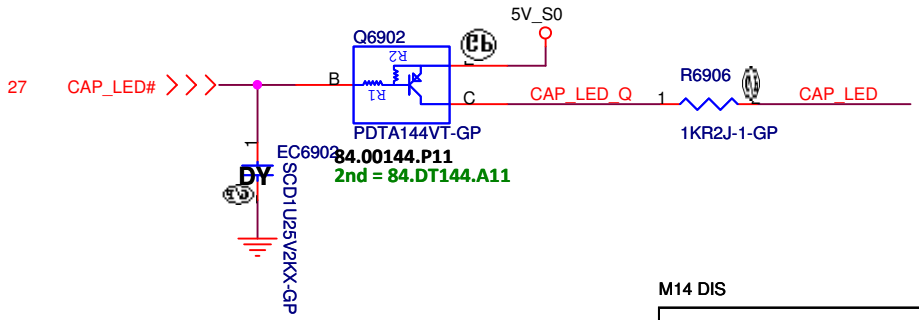
SSID = Touch.Pad

Touch Pad Connector



CAP LED Control

LOW actived from KBC GPIO



M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board/Touch Pad

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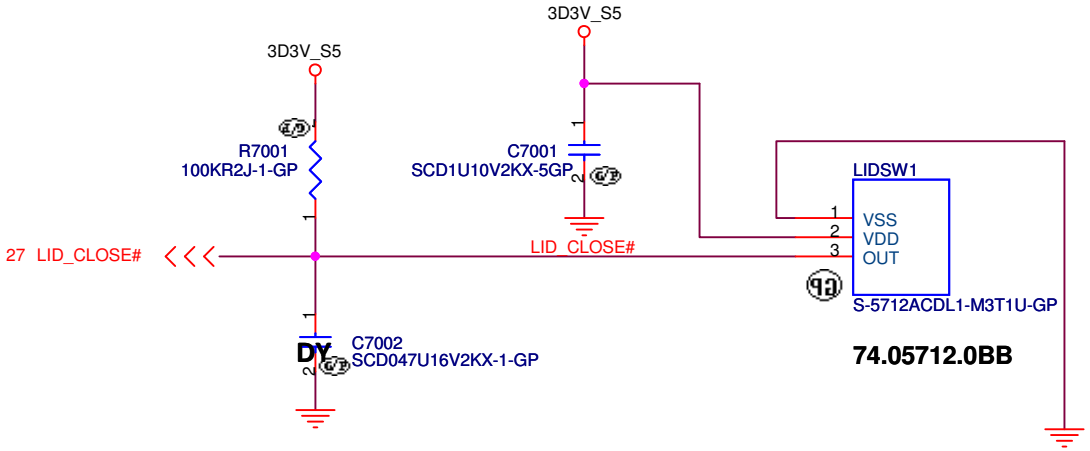
SSID = User.Interface



M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Hall Sensor

Size	Document Number	Rev
A4	OAK14 Chief River DIS	A00

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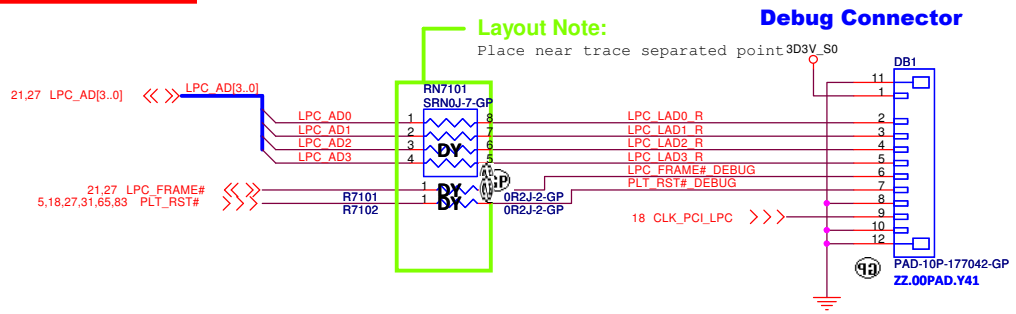
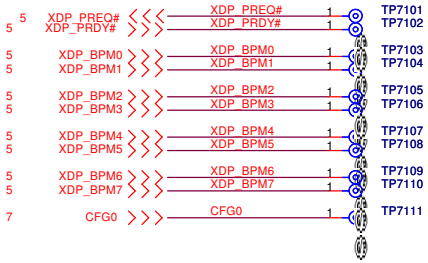
SSID = DEBUG PORT



SSID = CPU

CPU XDP



M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: Dubug connector

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M14 DIS

Wistron Corporation
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Title: *Reserved*

Size	Document Number	Rev
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M14 DIS

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Title

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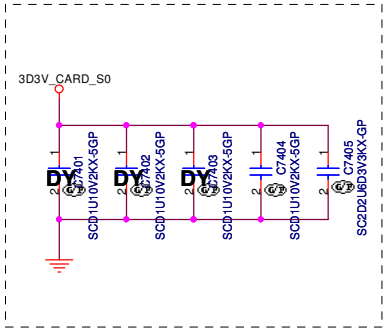
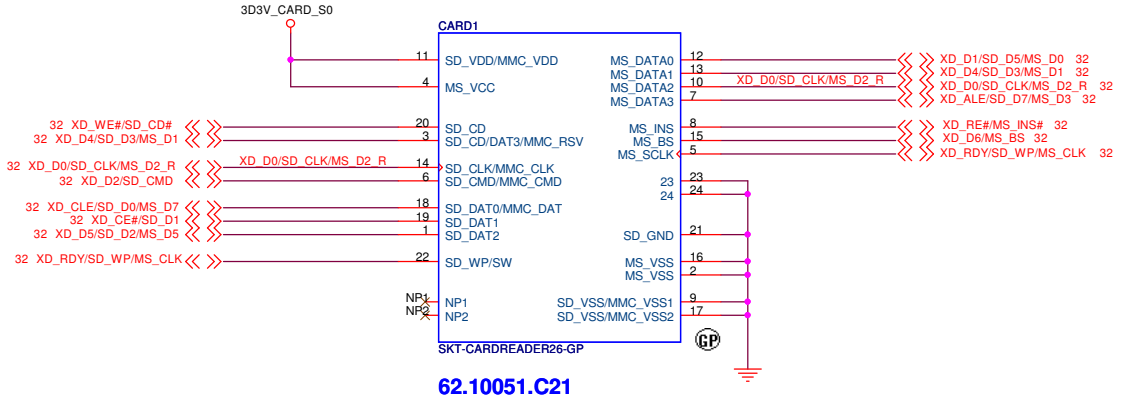
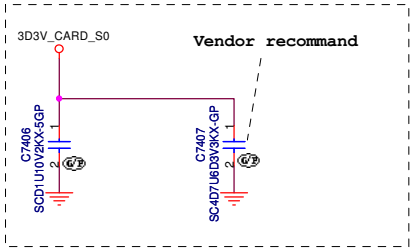
SSID = SDIO

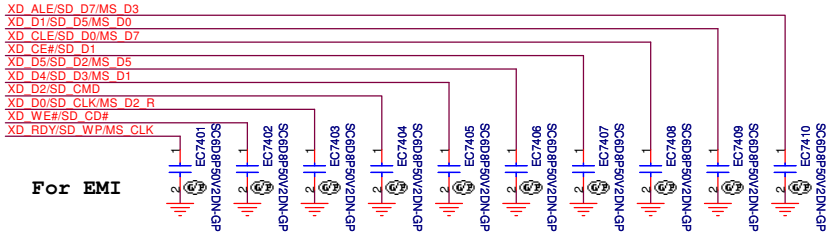




62.10051.C21

Close to Socket





M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SD/XD/MS/MMC Card CONN

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M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Express Card*

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M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *OAK14 Chief River DIS* | Rev: *A00*

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M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *OAK14 Chief River DIS* | Rev: *A00*

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M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

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M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Free Fall Sensor*

Size: A3 | Document Number: *OAK14 Chief River DIS* | Rev: *A00*

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M14 DIS

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *OAK14 Chief River DIS* | Rev: *A00*

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M14 DIS

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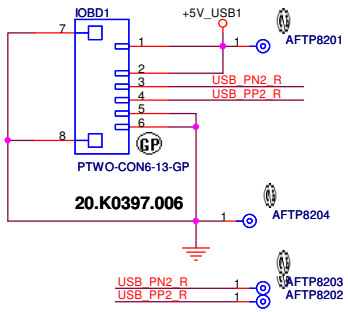
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

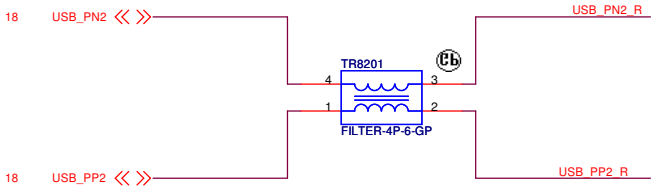
Title

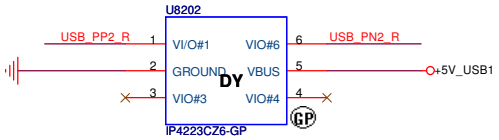
Reserved

Size	Document Number	Rev
A3	*OAK14 Chief River DIS*	*A00*

SSID = User.Interface







M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size: A3 | Document Number: OAK14 Chief River DIS | Rev: A00

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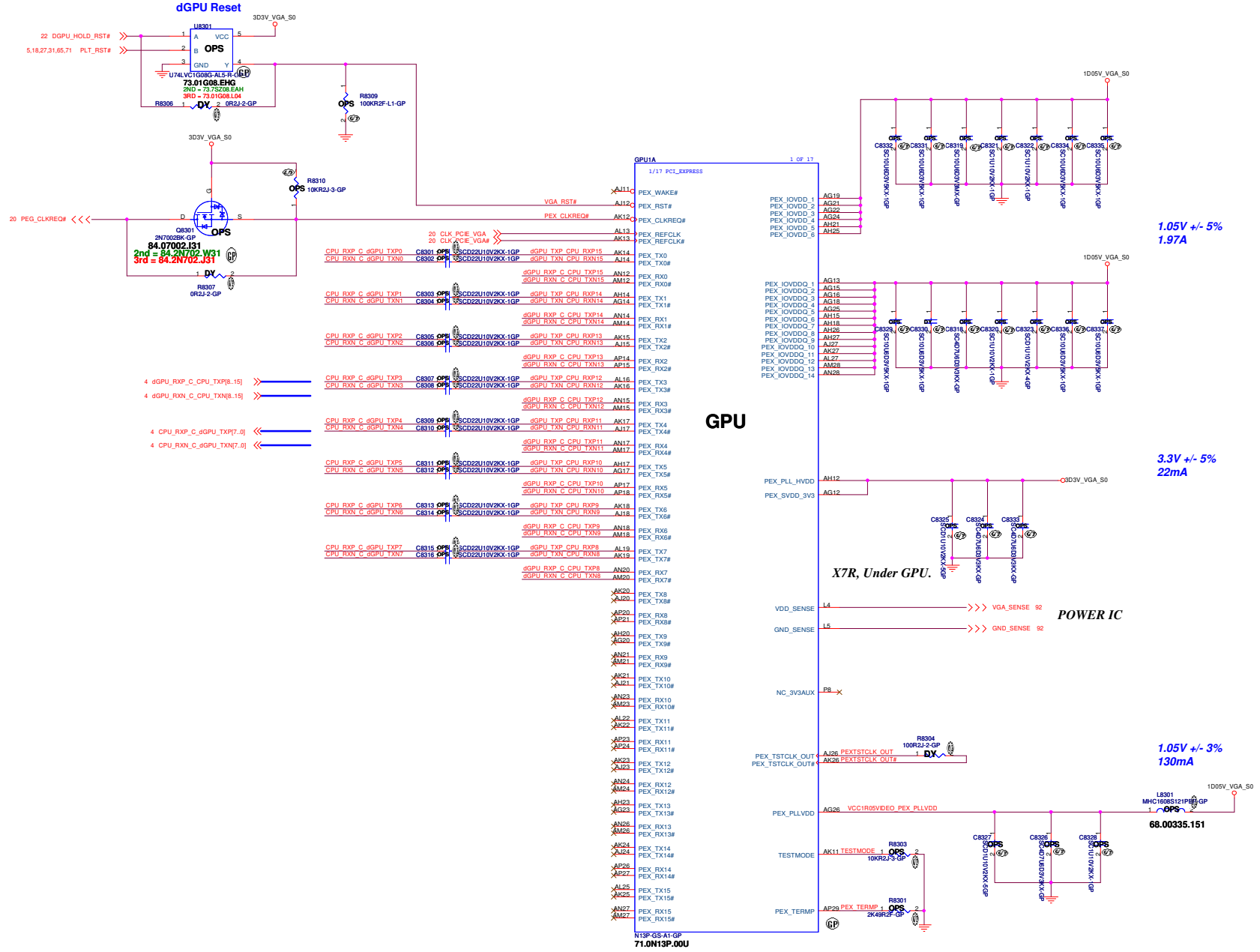

M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_PCIE/STRAPPING(1/5)

Size: A2 | Document Number: OAK14 Chief River DIS | Rev: A00

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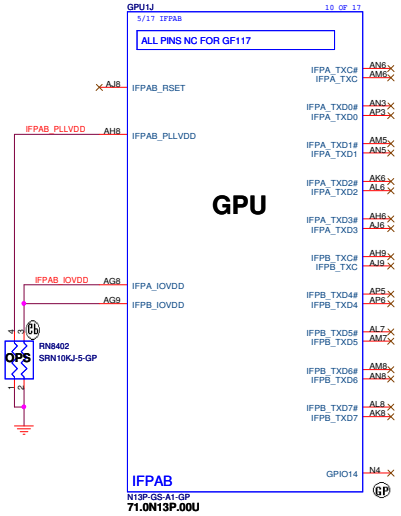
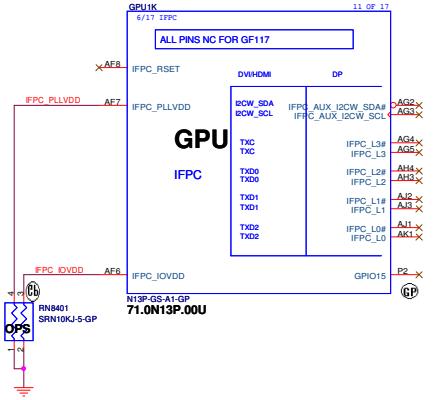
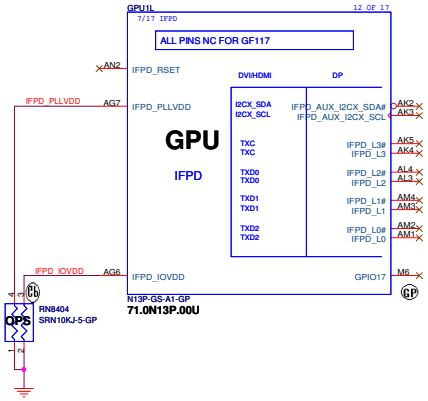
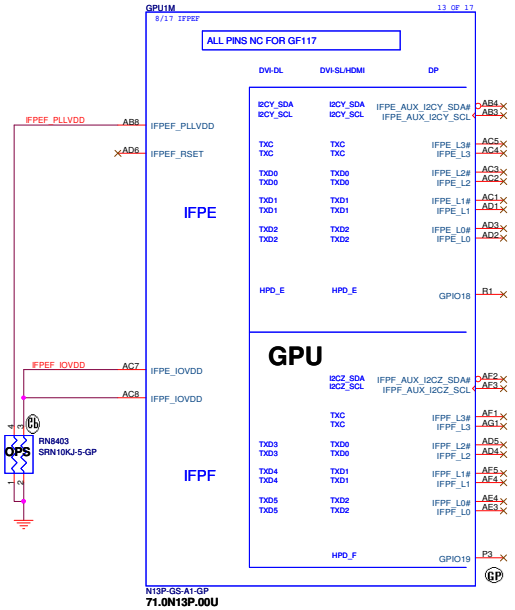
LVDS Interface





HDMI Interface





M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU Memory(2/5)*

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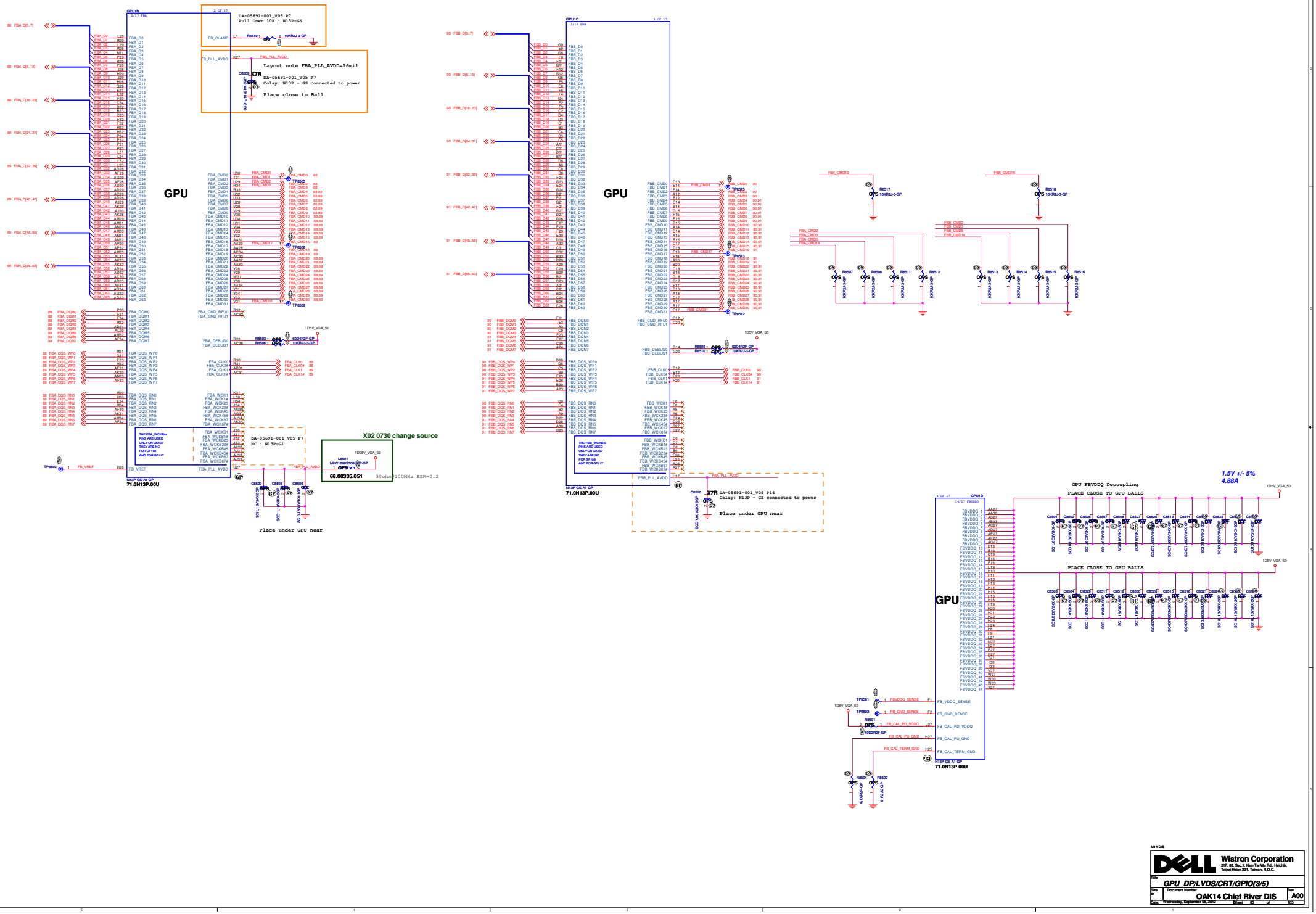

M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU_DP/LVDS/CRT/GPIO(3/5)*

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A3	OAK14 Chief River DIS	A00

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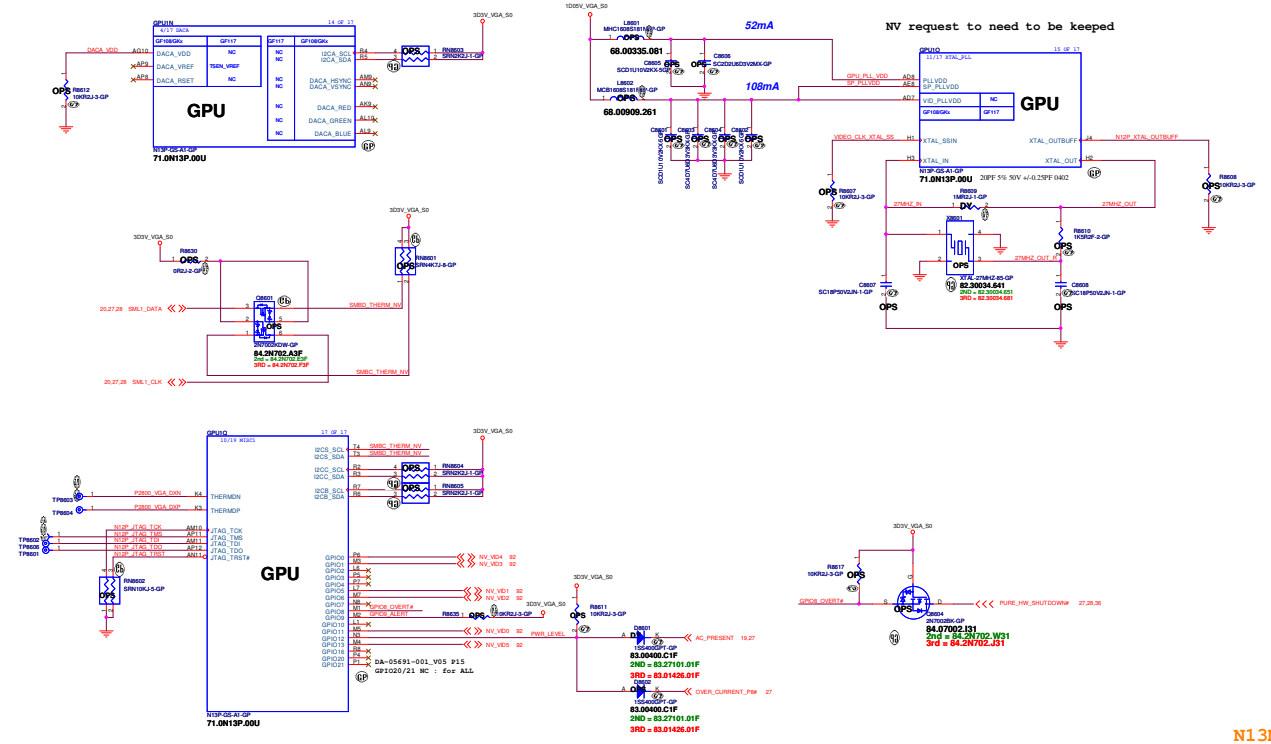
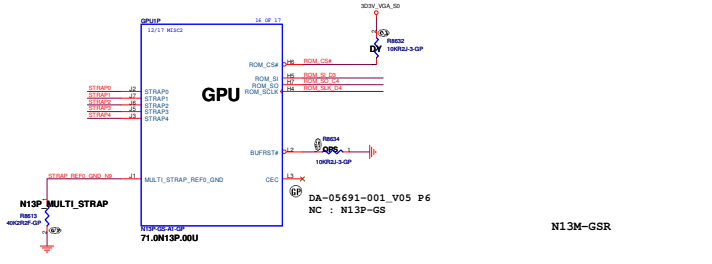
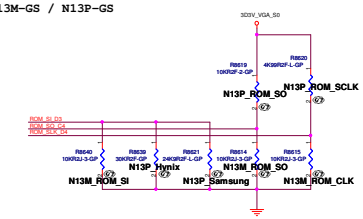
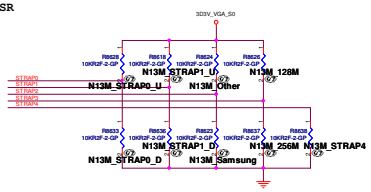




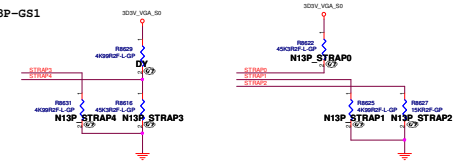
N13M-GS / N13P-GS



N13M-GSR



N13P-GS1



N13P-GS1

N13P-GS

Strap Pin Nmae	Logical strapping name bit#3	Logical strapping name bit#2	Logical strapping name bit#1	Logical strapping name bit#0	
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TER_M	
		0		0	
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[2]	RAMCFG[0]	
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE	
	1	0	0	1	10K ohm pull-up
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	
	1	1	1	1	45K ohm pull-up
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	
	0	0	0	0	5K ohm pull-down
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	
	0	0	0	0	5K ohm pull-down
STRAP4	RESERVED	PCI_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V	
	0	1	1	1	45K ohm pull-down

Part Reference	Part Number	Value	PCB Footprint
R8621(DIS_ROM SI)	64.20025.6DL	20KR2F-L-GP	R402H16
R8621	64.15025.6DL	15KR2F-GP	R402H16
R8621	64.34825.6DL	34K8R2F-1-GP	R402H16
R8621	64.45325.6DL	45K3R2F-L-GP	R402H16
R8621	64.30125.6DL	30K1R2F-L-GP	R402H16
R8621	64.24925.6DL	24K9R2F-L-GP	R402H16

GPU	N13P-GS
STRAP 0	PULL UP 45.3K
STRAP 1	PULL DOWN 4.99K
STRAP 2	PULL DOWN 15K
STRAP 3	PULL DOWN 4.99K
STRAP 4	PULL DOWN 45.3K
ROM_SO	PULL UP 10K
ROM_SCLK	PULL UP 4.99K
VRAM	ROM_SI pin
128M*16 DDR3 Samsung K4W2G1646E-BC11	Pull down 24.9K ohm
128M*16 DDR3 Hynix H5TQ2G63DFR-11C	Pull down 30K ohm

N13M-GSR

Table 4. Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10k Ω	Pull-down to GND
ROM_SI	SUB_VENDOR	10k Ω	Pull-up to 3V3 if VBIOS ROM exists Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10k Ω	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10k Ω	See Note
STRAP1	RAM_CFG[1]	10k Ω	See Note
STRAP2	RAM_CFG[2]	10k Ω	See Note
STRAP3	RAM_CFG[3]	10k Ω	See Note
STRAP4	PCIE_MAX_SPEED	10k Ω	Pull-down to GND

GPU	N13M-GS				
STRAP 4	PULL DOWN 10K				
ROM_SCLK	PULL DOWN 10K				
ROM_SO	PULL DOWN 10K				
ROM_SI	PULL DOWN 10K				
VRAM	STRAP 0	STRAP 1	STRAP 2	STRAP 3	
128M*16 DDR3 Samsung	PULL UP 10K	PULL UP 10K	PULL DOWN 10K	PULL UP 10K	0xB
128M*16 DDR3 Hynix	PULL DOWN 10K	PULL DOWN 10K	PULL UP 10K	PULL UP 10K	0xC
256M*16 DDR3 Samsung	PULL UP 10K	PULL DOWN 10K	PULL DOWN 10K	PULL DOWN 10K	0x1
256M*16 DDR3 Micron	PULL UP 10K	PULL DOWN 10K	PULL UP 10K	PULL DOWN 10K	0x5

4/9 update GPU strappin

M14 DIS

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Title: GPU_POWER(4/5)

Size: Custom | Document Number: OAK14 Chief River DIS | Rev: A00

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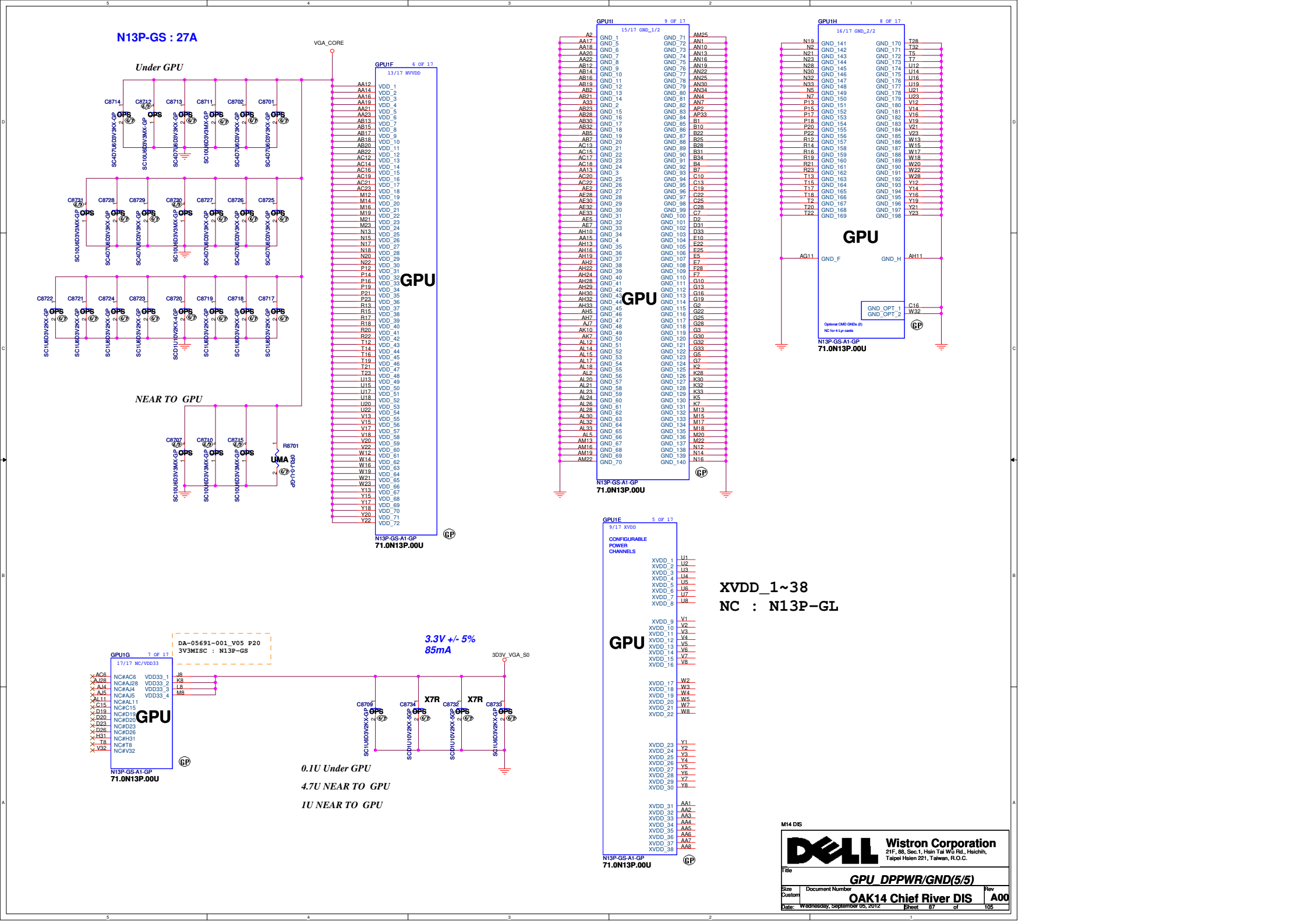

M14 DIS

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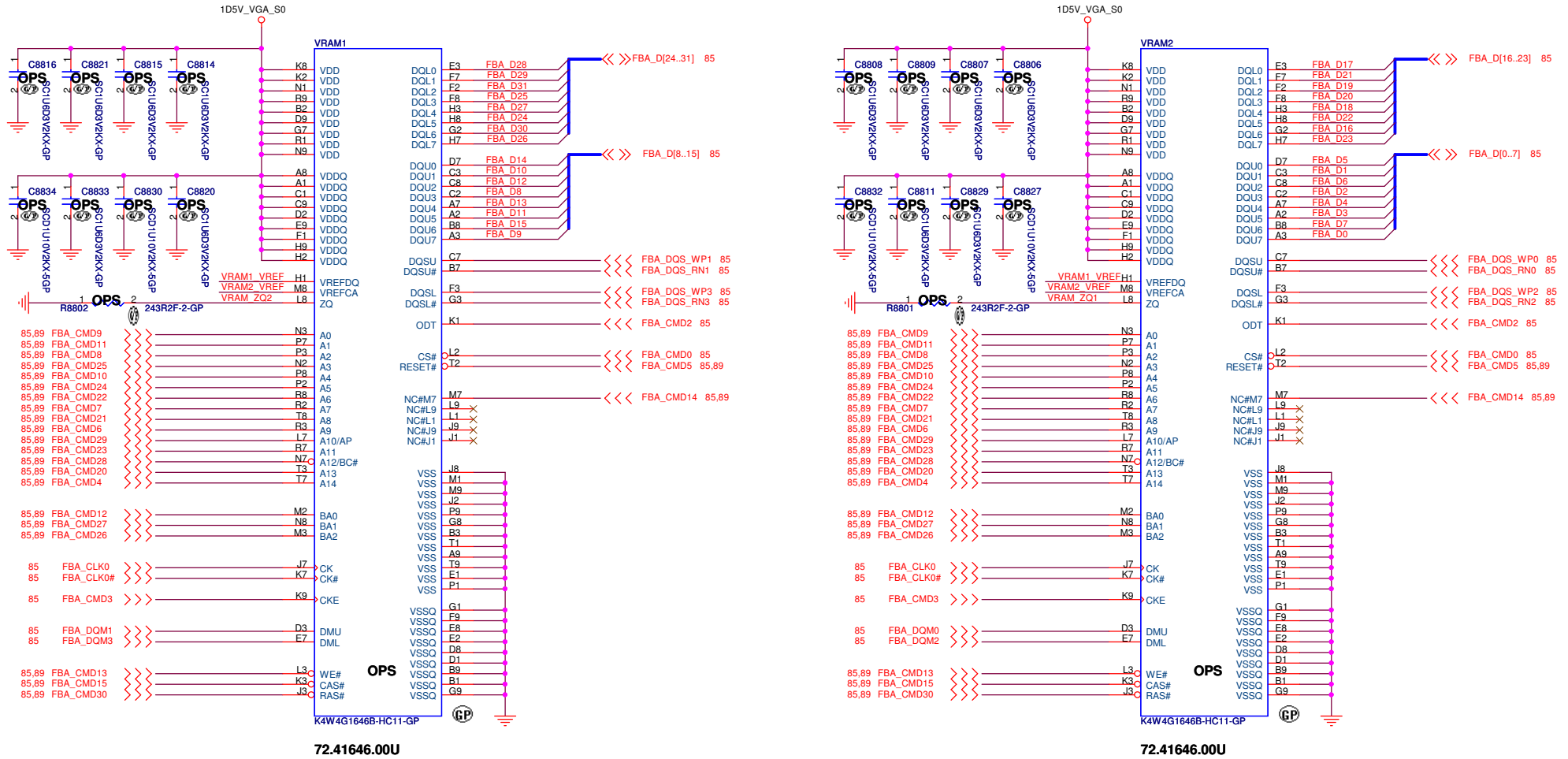
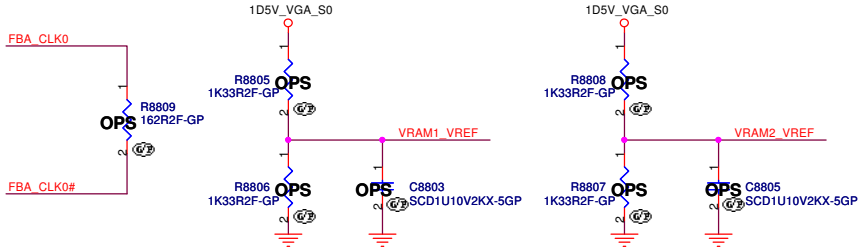
Title: *GPU_DPPWR/GND(5/5)*		
Size: Custom	Document Number: OAK14 Chief River DIS	Rev: A00
Date: Wednesday, September 05, 2012	Sheet 87 of 105	

Frame Buffer Patition A-Lower Half



72.41646.00U

72.41646.00U



M14 DIS

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Title: *GPU-VRAM1,2 (1/4)*

Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00

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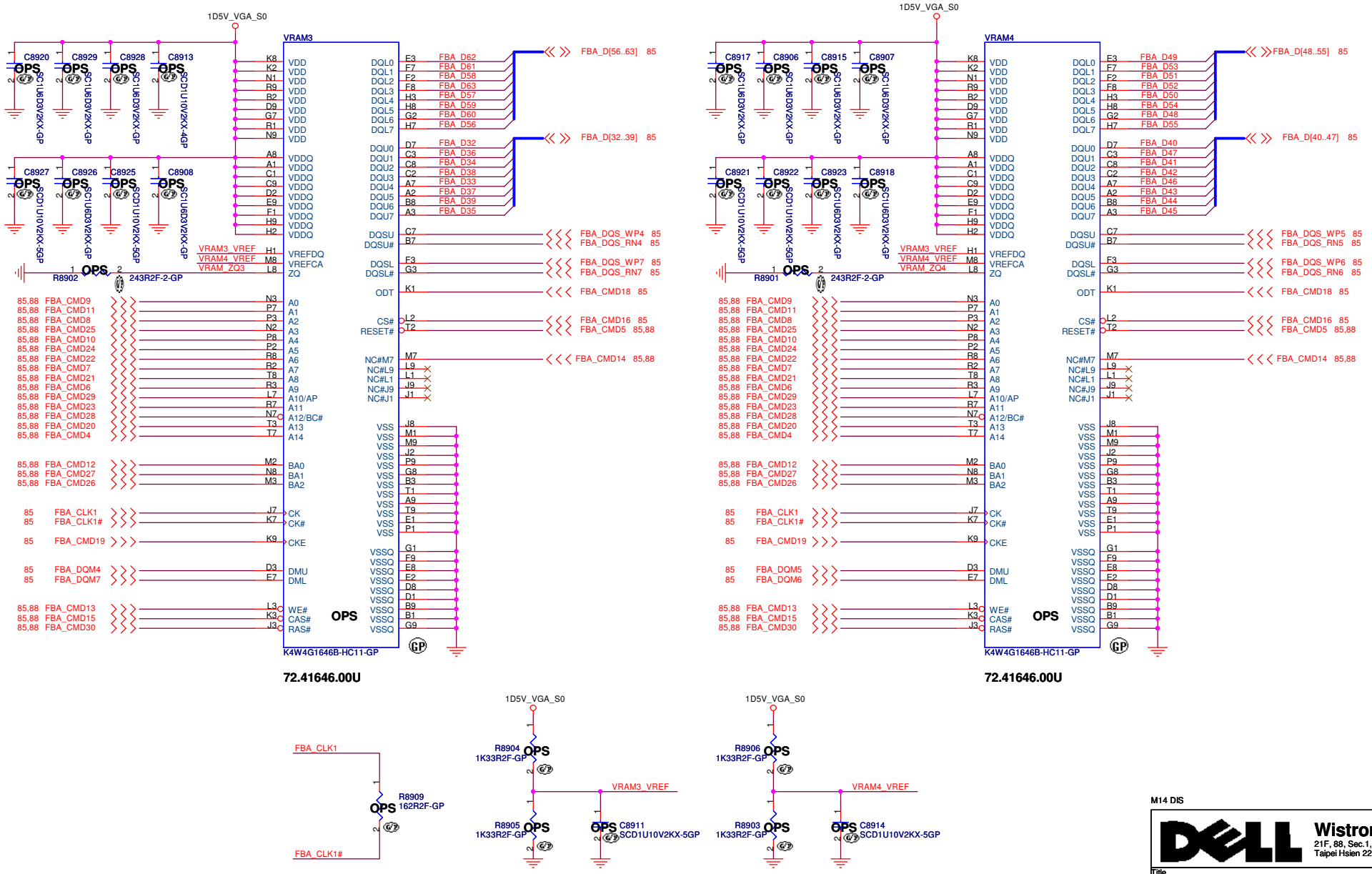
Frame Buffer Patition A-Upper Half



M14 DIS

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU-VRAM3,4 (2/4)*

Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00

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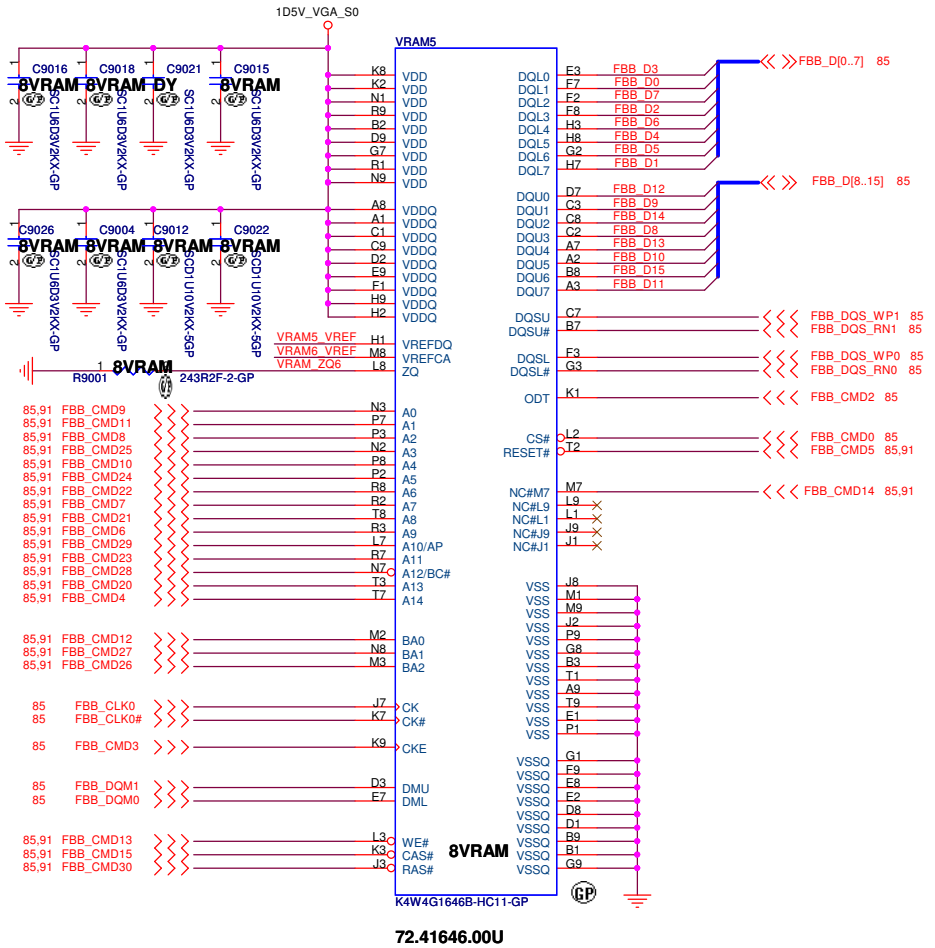
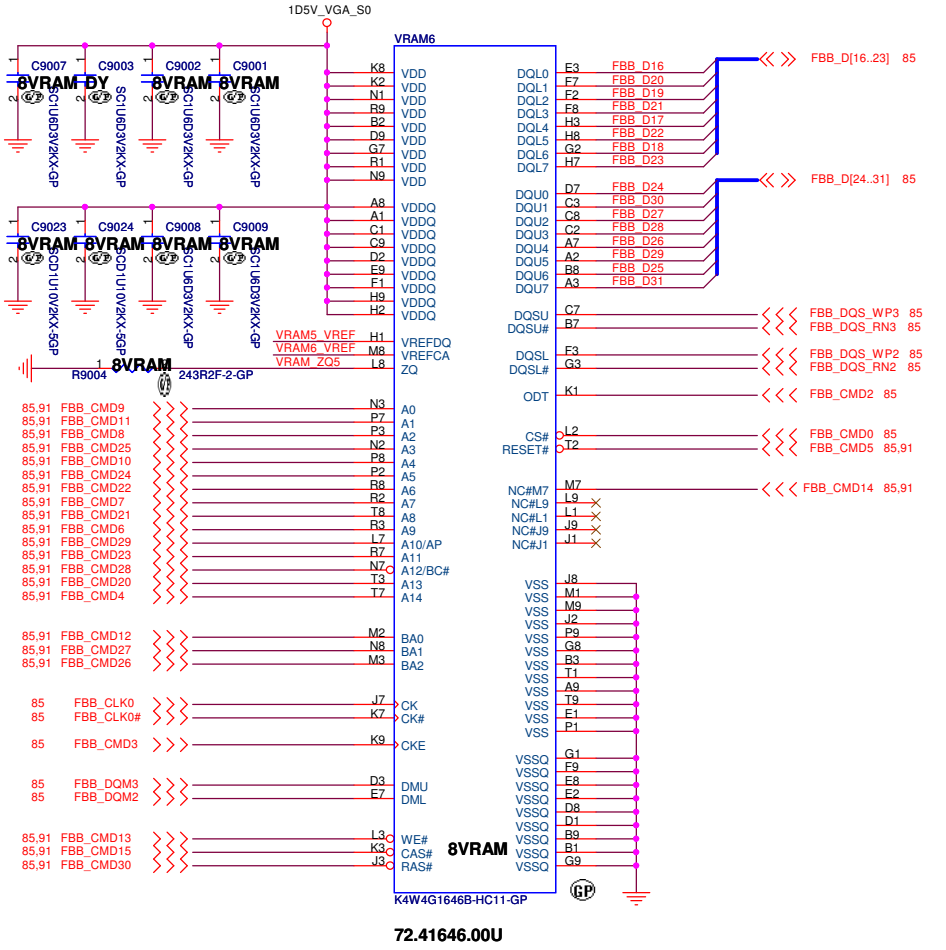
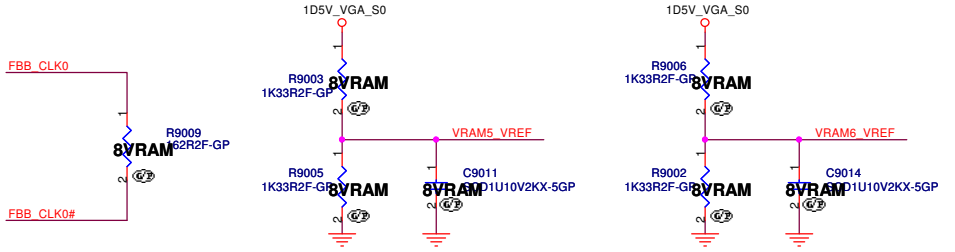
Frame Buffer Patition B-Lower Half



72.41646.00U



72.41646.00U



M14 DIS

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU-VRAM5,6 (3/4)*

Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00

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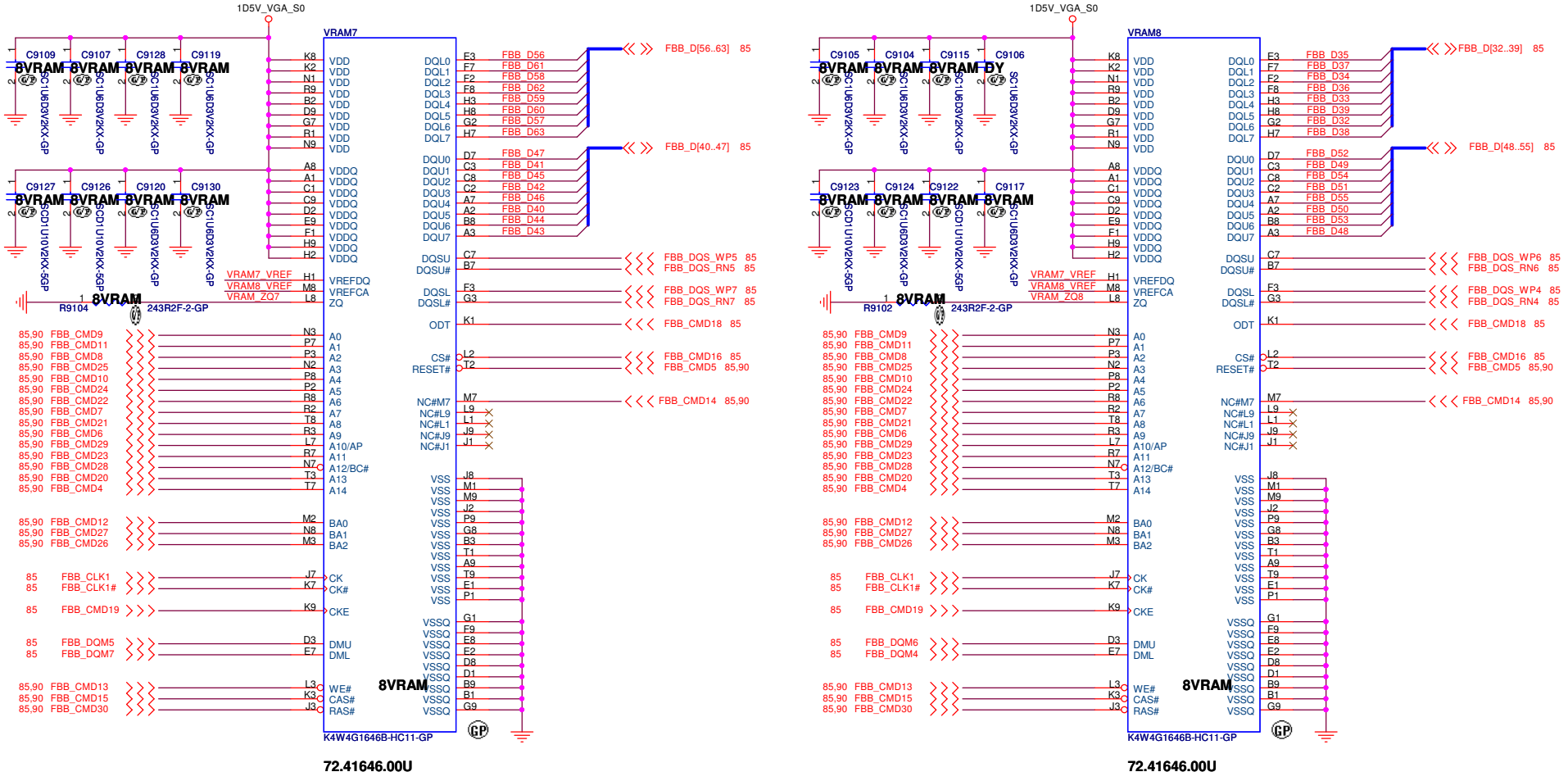
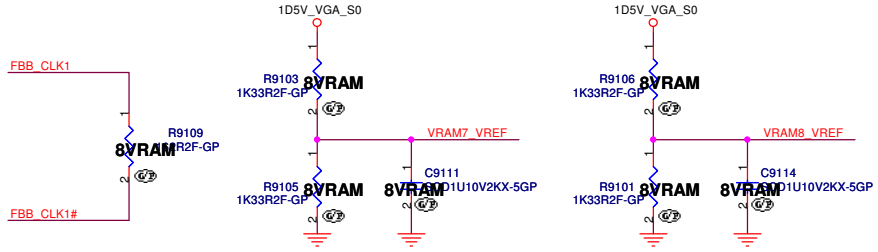
Frame Buffer Patition B-Upper Half





M14 DIS

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Title: GPU-VRAM7,8 (4/4)

Size	Document Number	Rev
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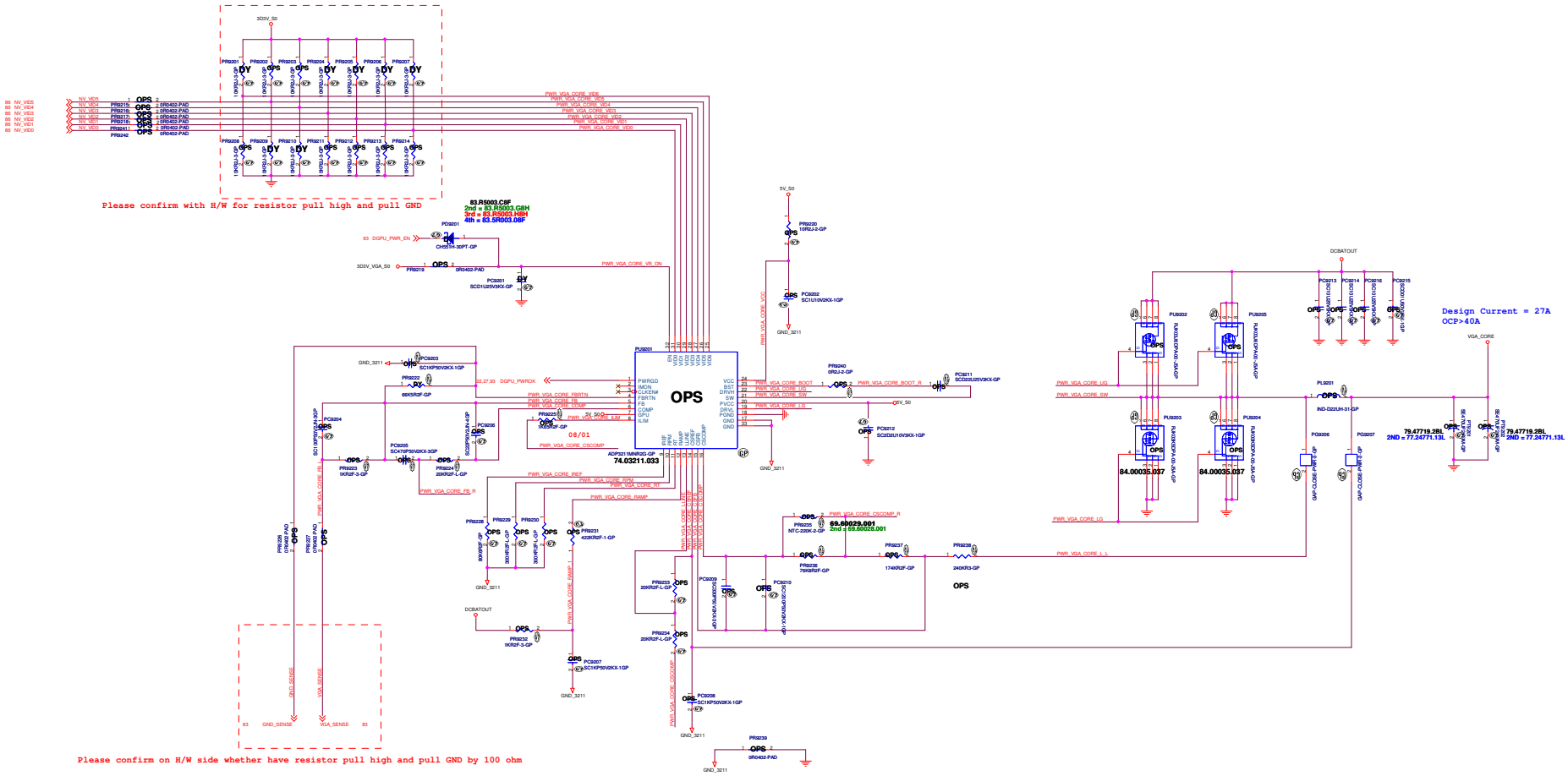
V-BOOT	VID0	VID1	VID2	VID3	VID4	VID5	VID6
0.9000V	0	0	0	0	1	1	0



I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHK 0.360H PCMC104T-R36MH 1.05mohm/ Isat =60A rms68.R3610.20S
O/P cap: CHIP CAP 470UF 2V EEFSX0D471X/ 3.5Arms Panasonic/79.47719.2BL
H/S: RJK03J6DPA-00#J5A / 10mohm/13mOhm@4.5Vgs/ 84.00036.037
L/S: RJK03K5DPA-00#J5A / 3mohm/3.9mOhm@4.5Vgs/ 84.00035.037

M14 DIS

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Title: ADP3211 +VGA_CORE

Size	Document Number	Rev
Custom	DNE40 14 CR DIS	A00

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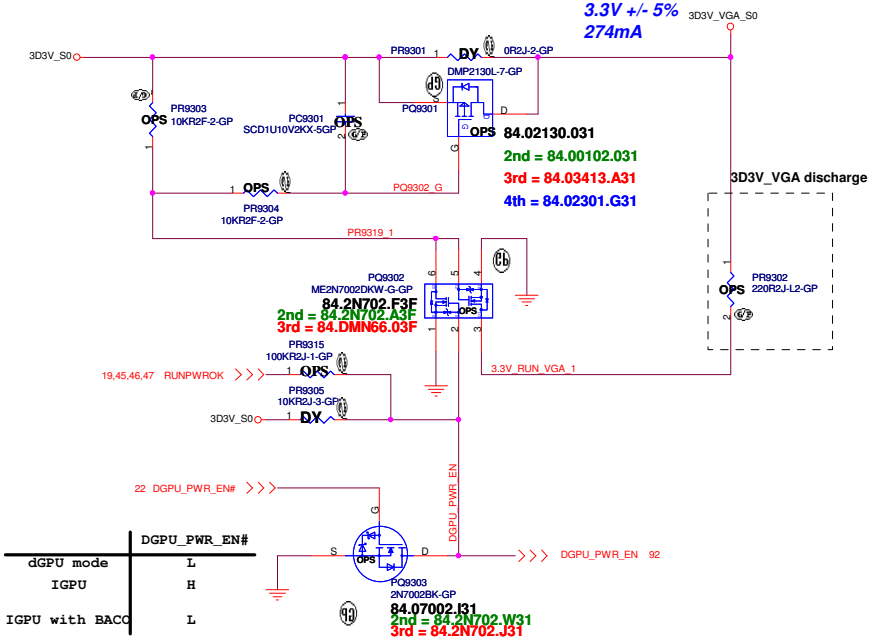
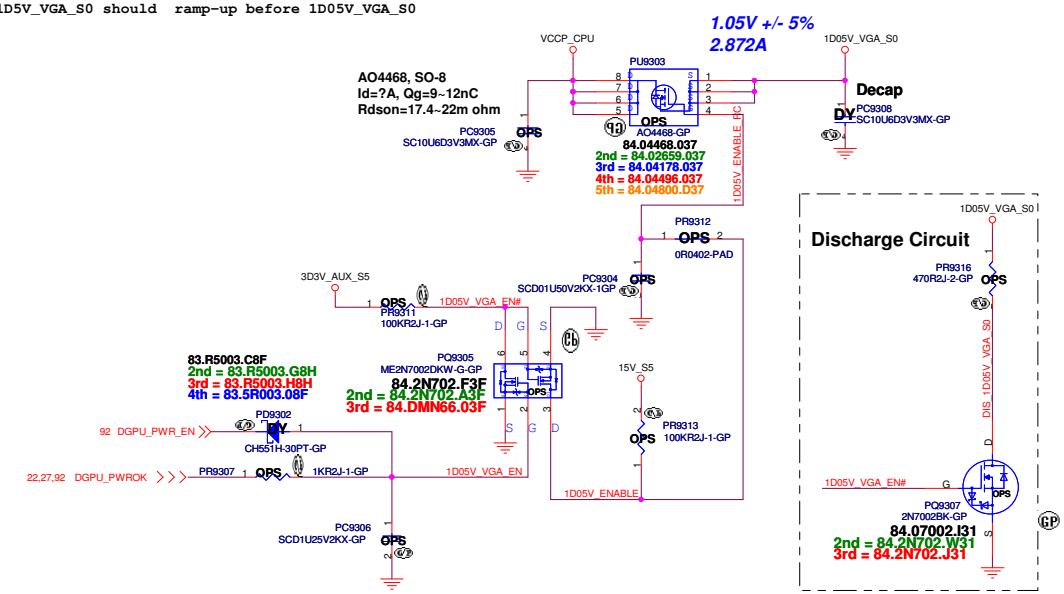
3D3V_VGA_S0



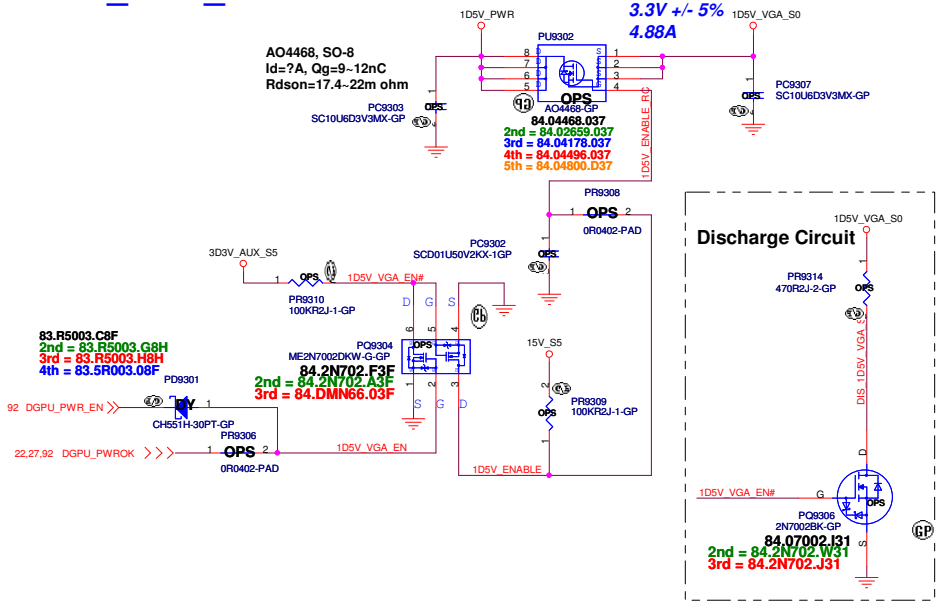
DGPU_PWR_EN#	
dGPU mode	L
IGPU	H
IGPU with BACO	L

1D05V_VGA_S0

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1D5V_VGA_S0
1D5V_VGA_S0 should ramp-up before 1D05V_VGA_S0



1D5V_VGA_S0



NV do not need 1.8V

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Title	DISCRETE VGA POWER	
Size: Custom	Document Number: OAK14 Chief River DIS	Rev: A00
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(Blanking)

M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LVDS_Switch*

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(Blanking)

M14 DIS

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Title: *CRT_Switch*

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SSID = SDIO

(Blanking)

M14 DIS

Wistron Corporation
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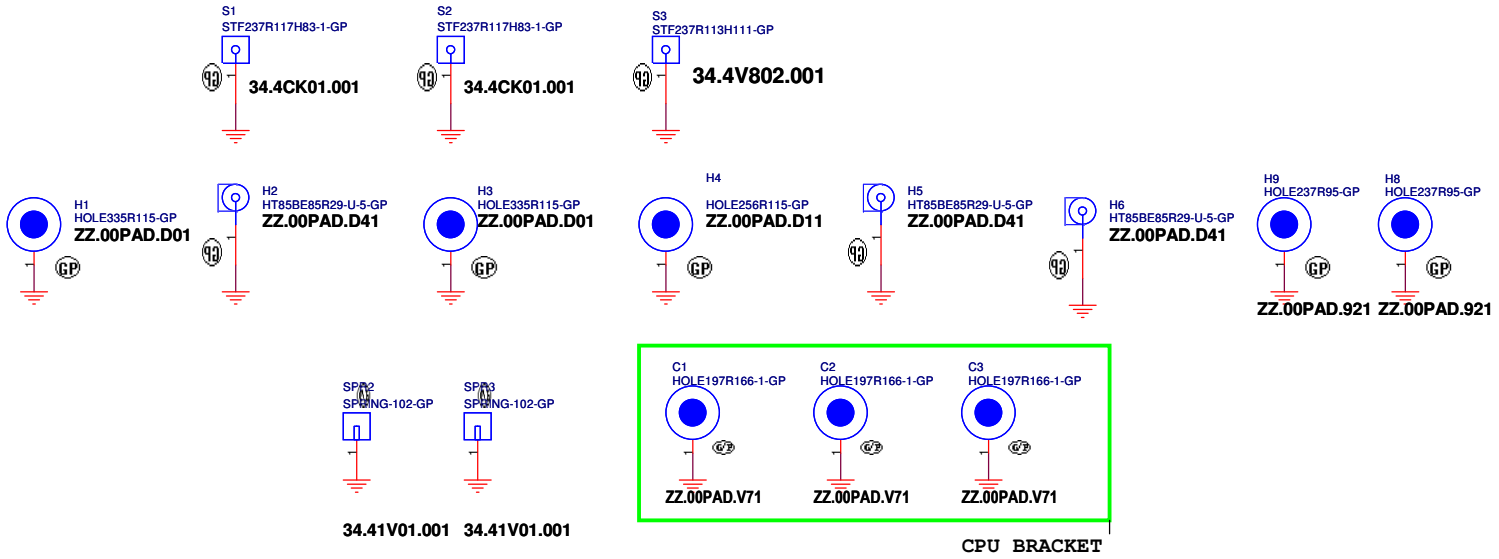
Taipei Hsien 221, Taiwan, R.O.C.

Title: TOUCH PANEL

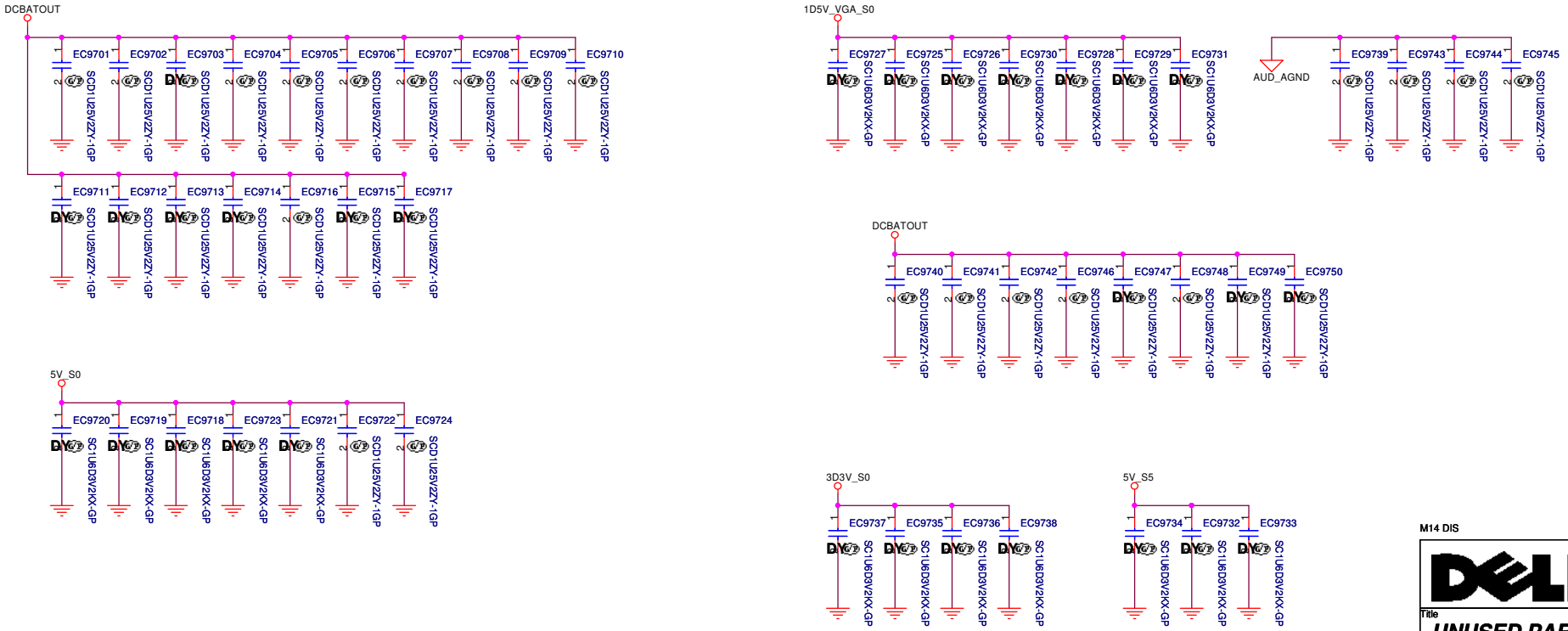
Size: A3 | Document Number: OAK14 Chief River DIS | Rev: A00

Date: Wednesday, September 05, 2012 | Sheet 96 of 105

SSID = Mechanical



SSID = EMI



M14 DIS

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Title: *UNUSED PARTS/EMI Capacitors*

Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00

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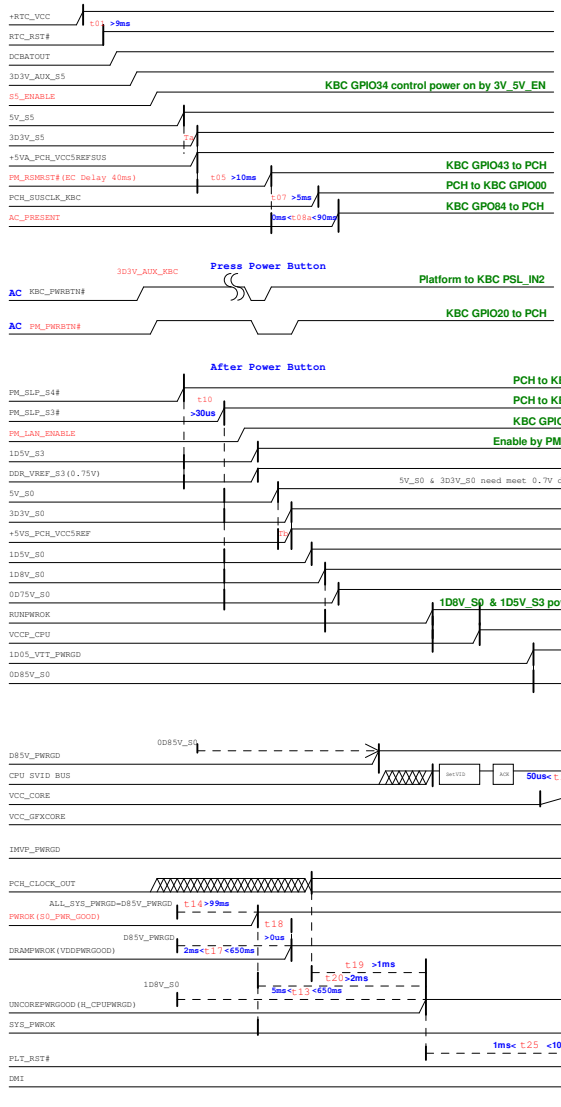
Chief River Platform Power Sequence

(AC mode)

Red Words: Controlled by EC GPIO



Within logic high level and disable if it is less than the logic low level.

Ta
VSAGF_bus must be powered up before Vccdsa3_3, or after Vccdsa3_3 within 0.7 V. Also, VSAGF_bus must power down after Vccdsa3_3, or before Vccdsa3_3 within 0.7 V.

Not floating.

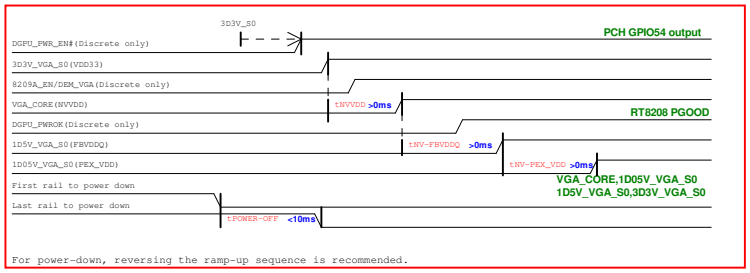
Sense the power button status

This signal has an internal pull-up resistor and has an internal 1k ms de-bounce on the input.

Tb
VSAGF must be powered up before Vccd_3, or after Vccd_3 within 0.7 V. Also, VSAGF must power down after Vccd_3, or before Vccd_3 within 0.7 V.

This signal represents the Power Good for all the non-CORE and non-graphics power rails.

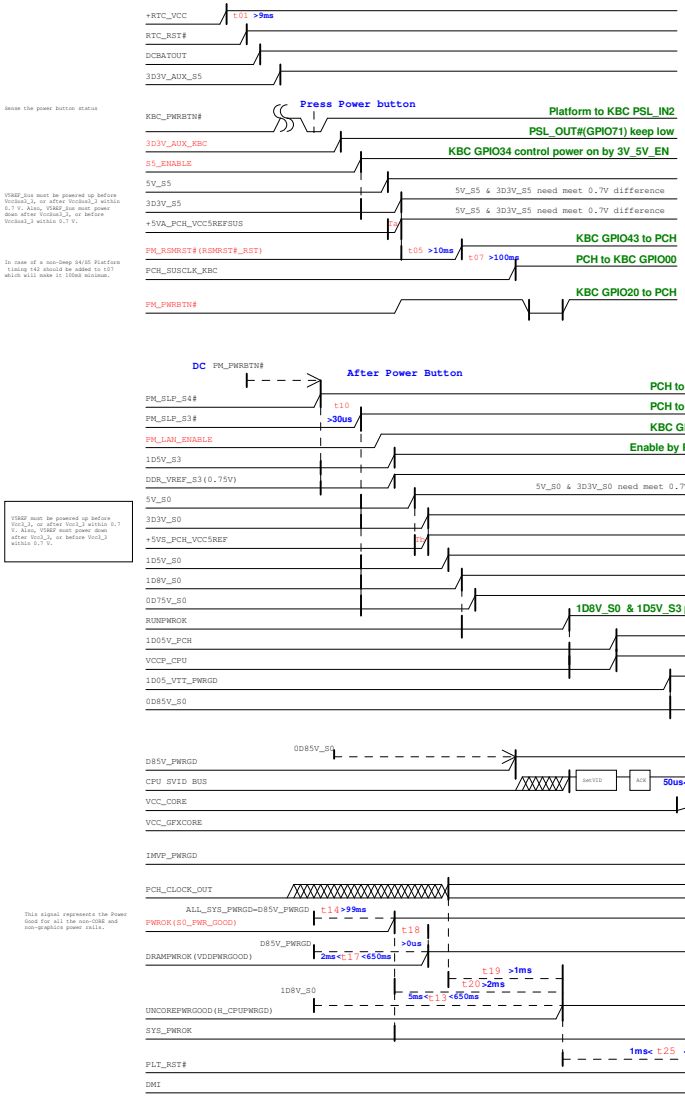
N13M-GS Power-Up/Down Sequence



For power-down, reversing the ramp-up sequence is recommended.

(DC mode)

Red Words: Controlled by EC GPIO



VSAGF_bus must be powered up before Vccdsa3_3, or after Vccdsa3_3 within 0.7 V. Also, VSAGF_bus must power down after Vccdsa3_3, or before Vccdsa3_3 within 0.7 V.

In case of a non-Deep S4/S5 Platform timing t42 should be added to t57 which will make it 100mS minimum.

VSAGF must be powered up before Vccd_3, or after Vccd_3 within 0.7 V. Also, VSAGF must power down after Vccd_3, or before Vccd_3 within 0.7 V.

This signal represents the Power Good for all the non-CORE and non-graphics power rails.

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Title: Power Sequence

Size	Document Number	Rev
A1	OAK14 Chief River DIS	A00

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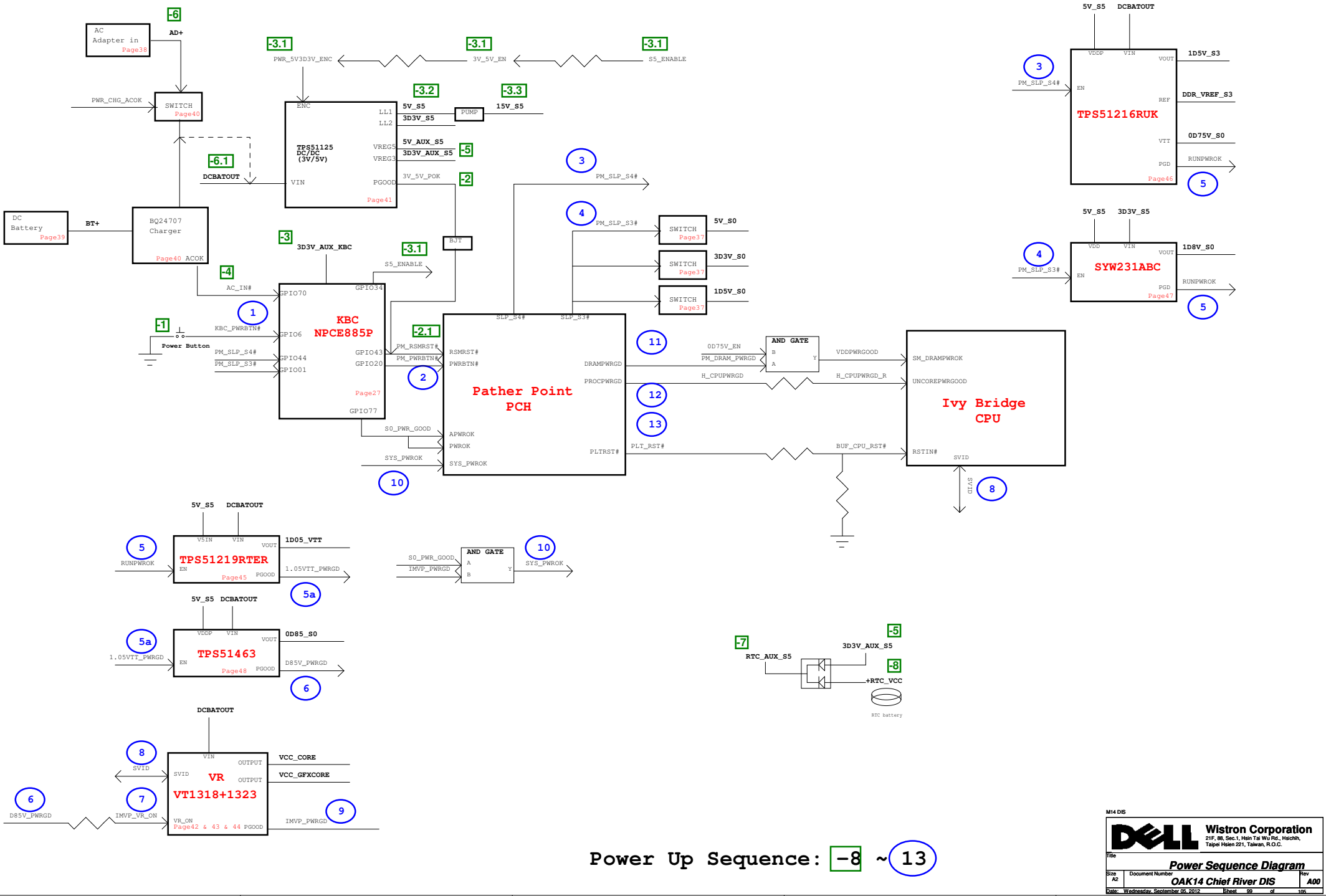
OAK14 Chief River POWER UP SEQUENCE DIAGRAM



Power Up Sequence: -8 ~ 13

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Title: Power Sequence Diagram

Size	Document Number	Rev
A2	OAK14 Chief River DIS	A00

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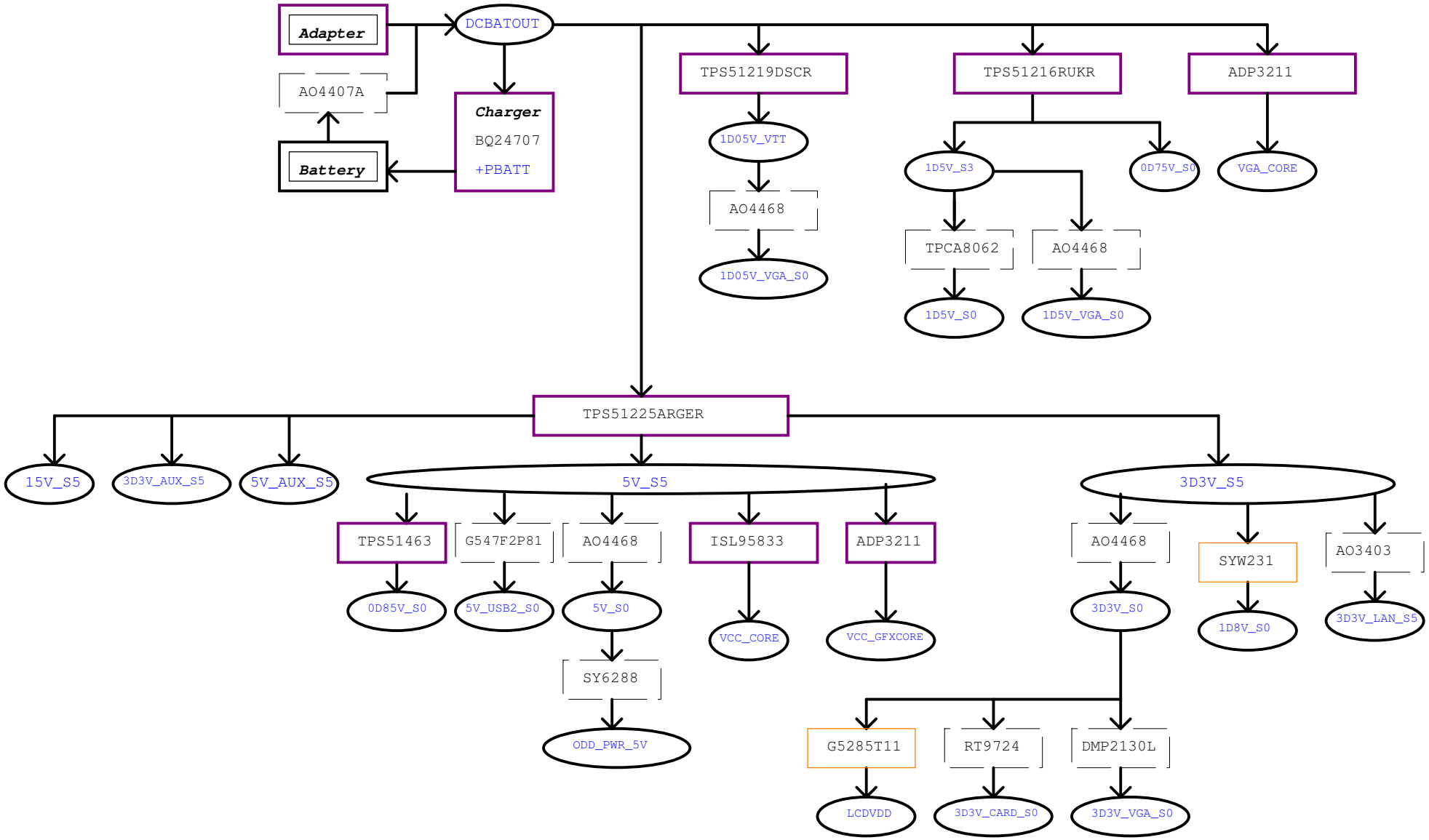

Power Shape

Regulator	LDO	Switch

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Title: **Power Block Diagram**

Size	Document Number	Rev
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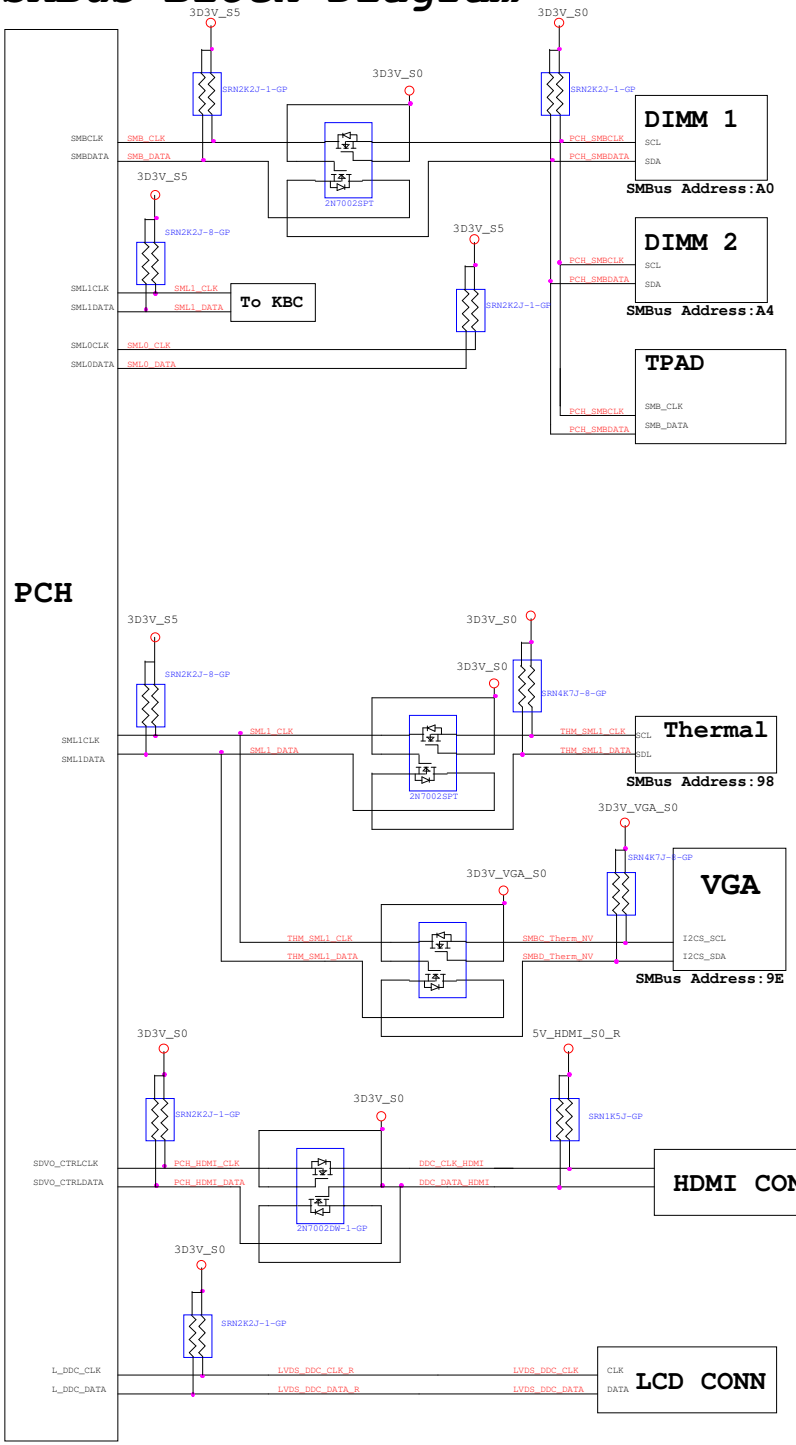
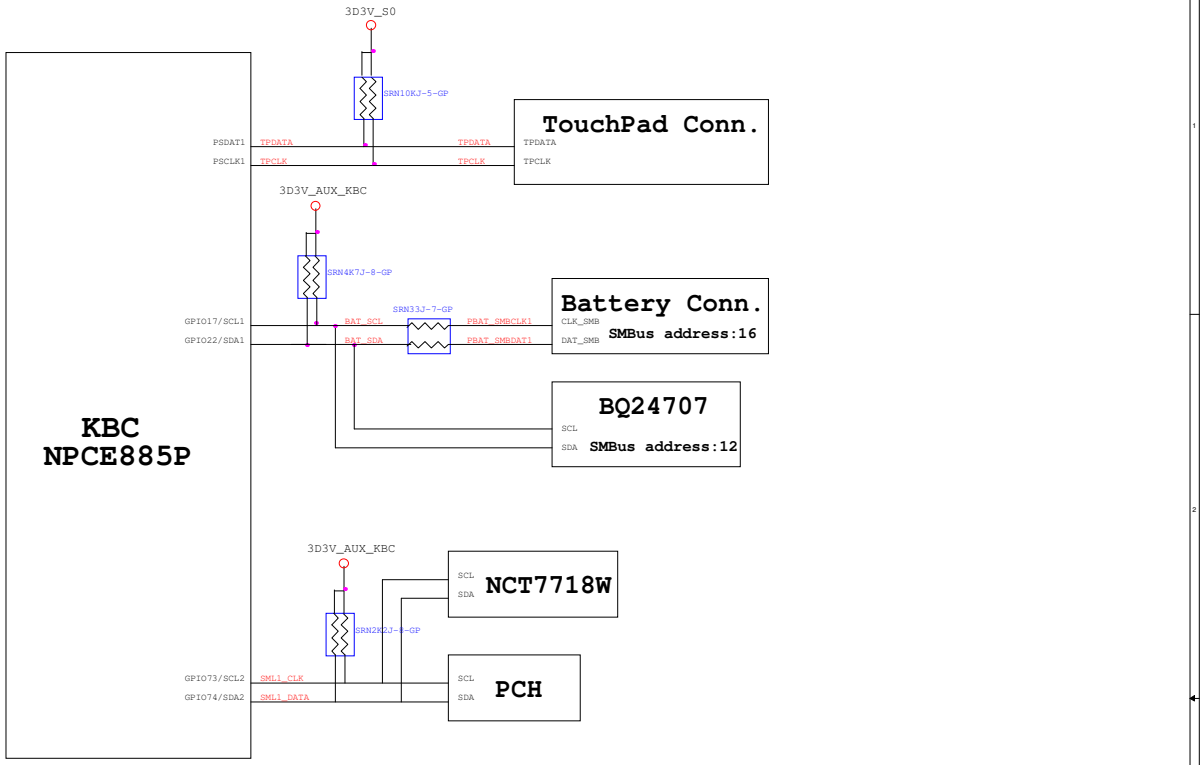
PCH SMBus Block Diagram



KBC SMBus Block Diagram



M14 DIS

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Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS Block Diagram

Size	Document Number	Rev
A2	OAK14 Chief River DIS	A00

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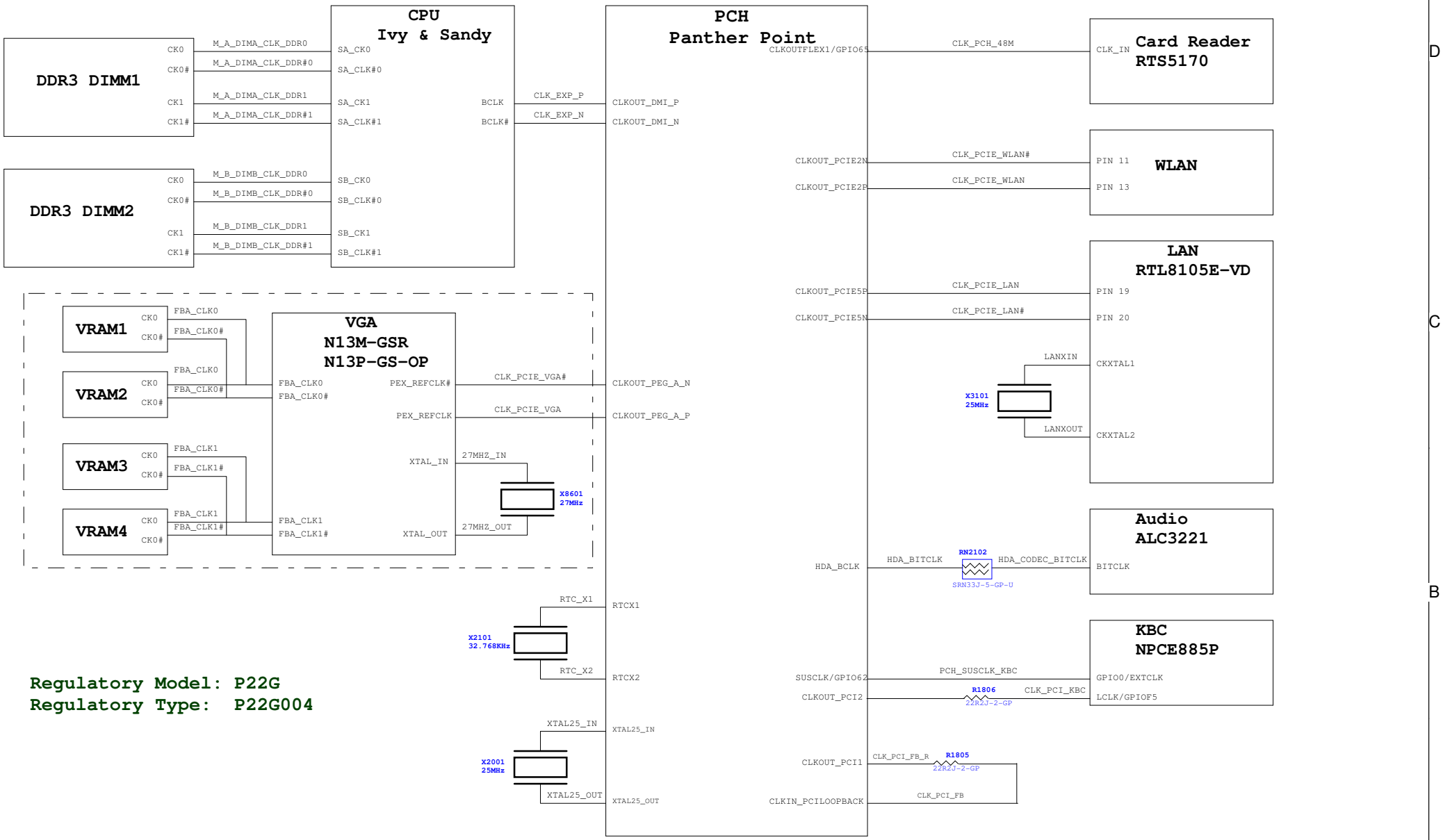
OAK14 DIS CLK Block Diagram



Regulatory Model: P22G
Regulatory Type: P22G004

M14 DIS

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Title		
CLK Block Diagram		
Size: A2	Document Number: OAK14 Chief River DIS	Rev: A00
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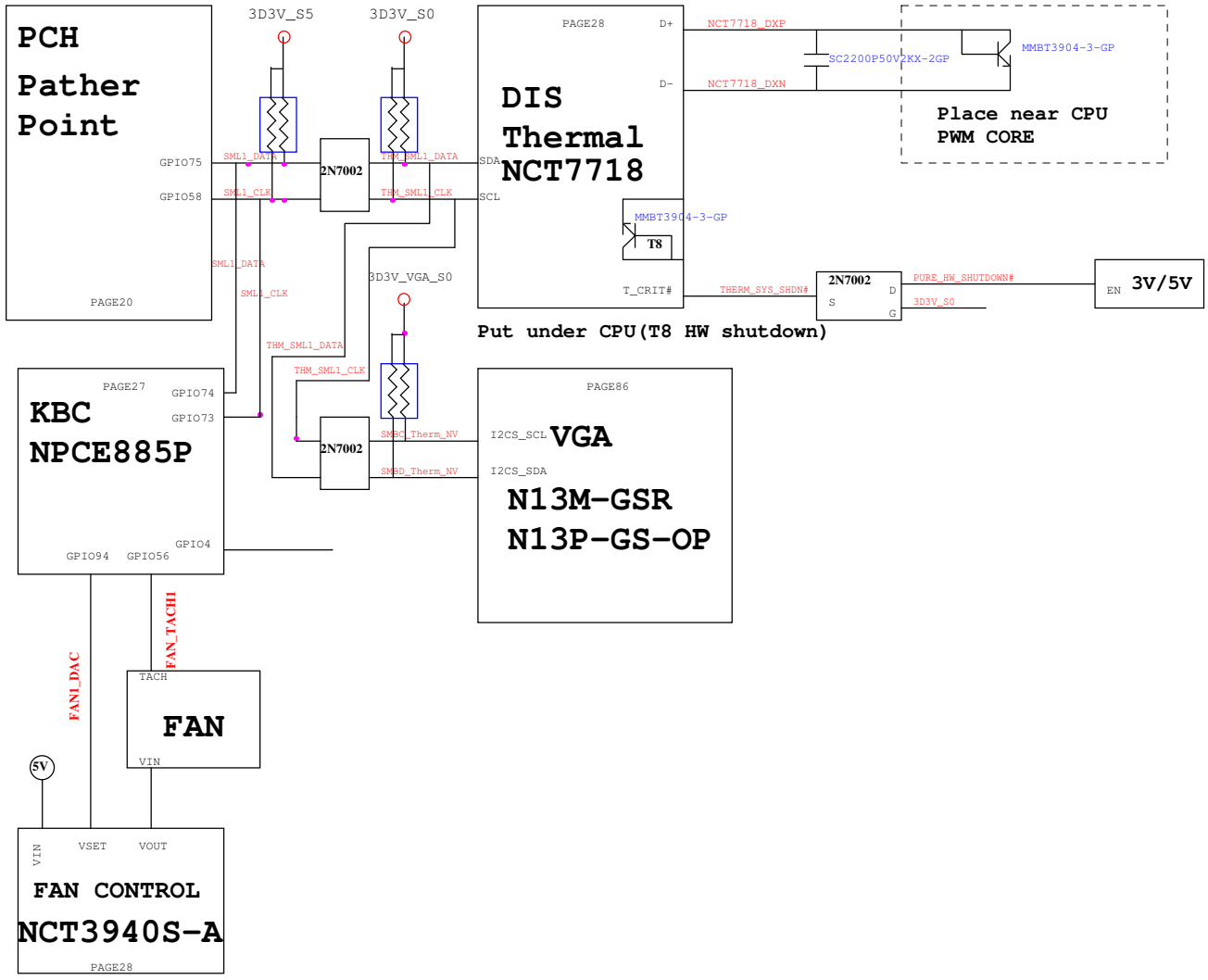
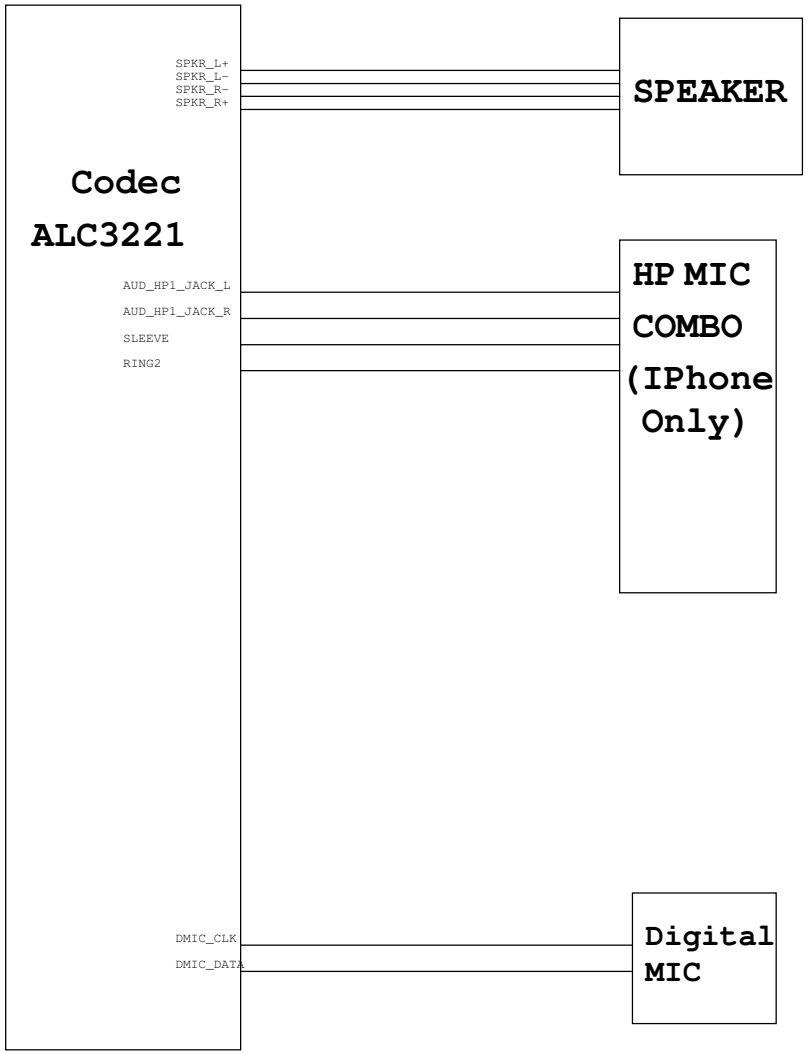
Thermal Block Diagram



Audio Block Diagram



M14 DIS

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Title	Thermal/Audio Block Diagram	
Size: Custom	Document Number: OAK14 Chief River DIS	Rev: A00
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Version	Date	PAGE	Description of Required Change
X01	5/10	P38	Dummy R3818 R3813 for DT Mode
X01	5/10	P20	Change CLK_PCIE_WLAN_REQ# PU from 3D3V_S5 to 3D3V_S0 & change port 3 to port 2(non AOAC)
X01	5/10	P86	Dummy R8613 (for N13M-GS1 strappin)
X01	5/28		Update connector list(5/28) for X01
X01	5/30	P49	Add TPNL1 (USB20 port#3)
X01	5/30	P29	Add delay circuit for Audio Jack JD pin
X01	5/30	P59	Change RJ45 Conn
X01	6/1	P38	Stuff PQ3801 PR3814 PR3815 for DT mode
X01	6/1	P37	Change R3713 to 10k for sequence timming
X01	6/1	P31	Change R3118 to 20k for sequence timming
X01	6/1	P69	Add KBL1 and keyboard backlight function
X01	6/1	P27	Change PCB version from X00 to X01
X01	6/5	P46	Fine tune the level of 1d5v_vga_s0: PR4601 (47K -> 57.6K)
X01	6/5	P58	Add TVS at combo JACK & RJ45 for EMI request
X01	6/5	P18	Move the KB_LED_BL_DET from GPIO5 to GPIO4
X01	6/11		Implement EMI change request 6/11
X01	6/11	P27	Delete RN2702 , DY R2716, Stuff R2717 For DT Mode
X01	6/11	P21	Add VRAM detect circuit at PCH_GPIO57
X01	6/11	P51	Change D5101 to 83.00056.G11 for lower internal cap
X01	6/12	P18	Move USB2.0 from port4# to port2#
X01	6/12	P49	Modify CAMERA1 to CAM1
X01	6/13	P61	Separate the USB3.0 PWR to USB30_VCCA & USB30_VCCB
X01	6/14	P49	Add LCD Back Light control circuit from KBC GPIO33
X01	6/14	P40	implement Power team request item
X01	6/15	P31	Change C3102=C3103=18pf for Xtal vendor request
X01	6/15	P62	Modify cap value for USB30_VCCA & USB30_VCCB
X01	6/18	P69	DY the Keyboard back light parts, add R6916 for PU
X01	6/18	P61	Change TC6102 & TC6104 to 78.10710.52L; TC6103 to 79.10710.60L
X01	6/18	P20	Move WLAN from PCIE 4# to PCIE 3#
X01	6/18	P51	implement EMI team request item (6/15)
X01	6/18	P69	Remove R6916 Stuff R6912
X01	6/18	P69	Change Q6801~Q6805 & Q6902 to 84.00144.P11

M14 DIS

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Title: *Change History*

Size: A3 | Document Number: *OAK14 Chief River DIS* | Rev: *A00*

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Version	Date	PAGE	Description of Required Change
X02	7/30	P58	Add delay circuit at Audio Combo Jack
X02	7/30		update the connector symble, base on ME connector list 7/16
X02	7/30	P69	Remove the Key board back ligh circuit
X02	7/31		Modify 0 ohm to short PAD
X02	7/31	P71	Dummy DB1 circuit
X02	8/1	P58	Change HPMIC1 source and related circuit
X02	8/1		update power team request change 8/1
X02	8/6	P27	Move SERIES_ID to GPIO5

M14 DIS

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Change History*

Size	Document Number	Rev
A3	*OAK14 Chief River DIS*	*A00*

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Version	Date	PAGE	Description of Required Change
A00	9/4		change 0 ohm to short pad
A00	9/4		combine CM choke & 0 ohm
A00	9/4		change close gap & DB1 to symble with solder mask
A00	9/4	27	change PCB version from SC to -1
A00	9/4	74	Replace EC7401 ~ EC7410 from 10p to 6.8p
A00	9/4	61	Remove CM Choke at USB3.0 side, dummy U6204 U6205

M14 DIS

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Title: *Change History*

Size: A3 | Document Number: *OAK14 Chief River DIS* | Rev: *A00*

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