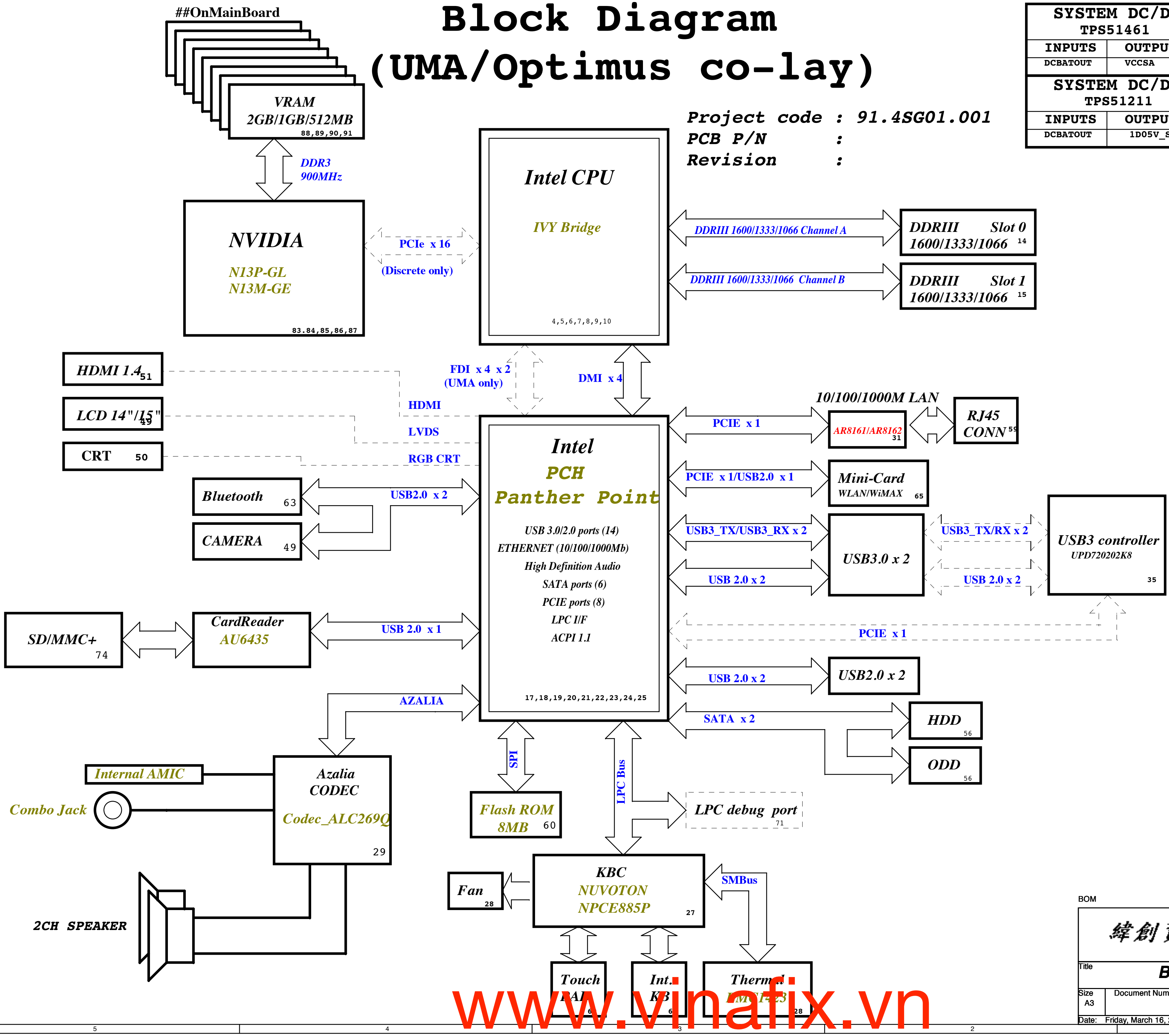
Block Diagram (UMA/Optimus co-lay)

Project code : 91.4SG01.001
PCB P/N :
Revision :



SYSTEM DC/DC TPS51461 48	
INPUTS	OUTPUTS
DCBATOUT	VCCSA

CPU DC/DC TPS51640RSLR 42~44	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51211 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

SYSTEM DC/DC G977F 45	
INPUTS	OUTPUTS
DCBATOUT	1D0V_S0

SYSTEM DC/DC TPS51123 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC RT8207 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

GFX DC/DC TPS51640RSLR 42~44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

VGA ISL62882C 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

CHARGER BQ24745 40	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC RT9025 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

VGA switchs 93	
INPUTS	OUTPUTS
1D5V_S3 3D3V_S0 1D05V_VTT	1D5V_VGA_S0 3D3V_VGA_S0 1D05V_VGA_S0

Switches	
INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0

PCB LAYER

L1:Top	L4:Signal
L2:VCC	L5:GND
L3:Signal	L6:Bottom

BOM

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Title	Block Diagram	
Size A3	Document Number LG4858_UMA	Rev -1
Date: Friday, March 16, 2012	Sheet 2 of 103	

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PCH Strapping Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ – 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) – Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) – Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) – Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) – Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled – No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled – An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 – Device 1 functions 1 and 2 disabled 10 : x8, x8 – Device 1 function 1 enabled ; function 2 disabled 01 : Reserved – (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 – Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

All Not update

Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 – 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

USB Table

Pair	Device
0	X
1	USB3.0 ext port 1
2	USB2.0 ext port 4
3	USB3.0 ext port 2
4	BLUETOOTH
5	CARD READER
6	X
7	X
8	X
9	USB2.0 ext port 3
10	X
11	WLAN(Bluetooth)
12	CAMERA
13	X

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Onboard LAN
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA

Pair	Device
0	N/A
1	HDD1
2	N/A
3	N/A
4	ODD
5	N/A

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

BOM

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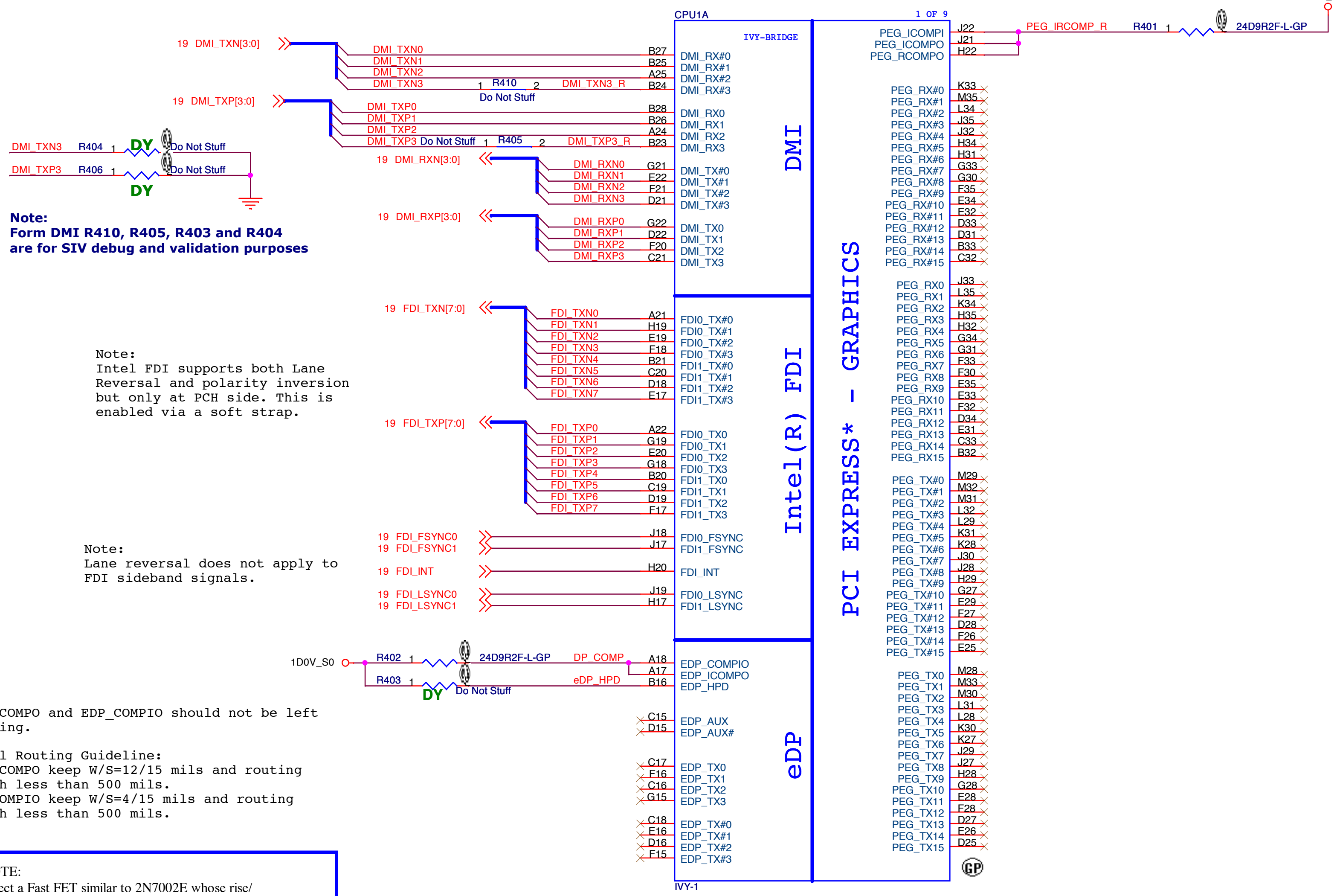
SSID = CPU

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect



Note:
Form DMI R410, R405, R403 and R404 are for SIV debug and validation purposes

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

Note:
EDP_ICOMPO and EDP_COMPIO should not be left floating.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE:
Select a Fast FET similar to 2N7002E whose rise/fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

62.10040.821

BOM_CTRL

1st = 22.10252.171

2nd = 62.10040.821

3rd = 62.10055.551

BOM

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Title	CPU (PCIE/DMI/FDI)	
Size A3	Document Number LG4858_UMA	Rev -1
Date: Friday, March 16, 2012	Sheet 4 of 103	

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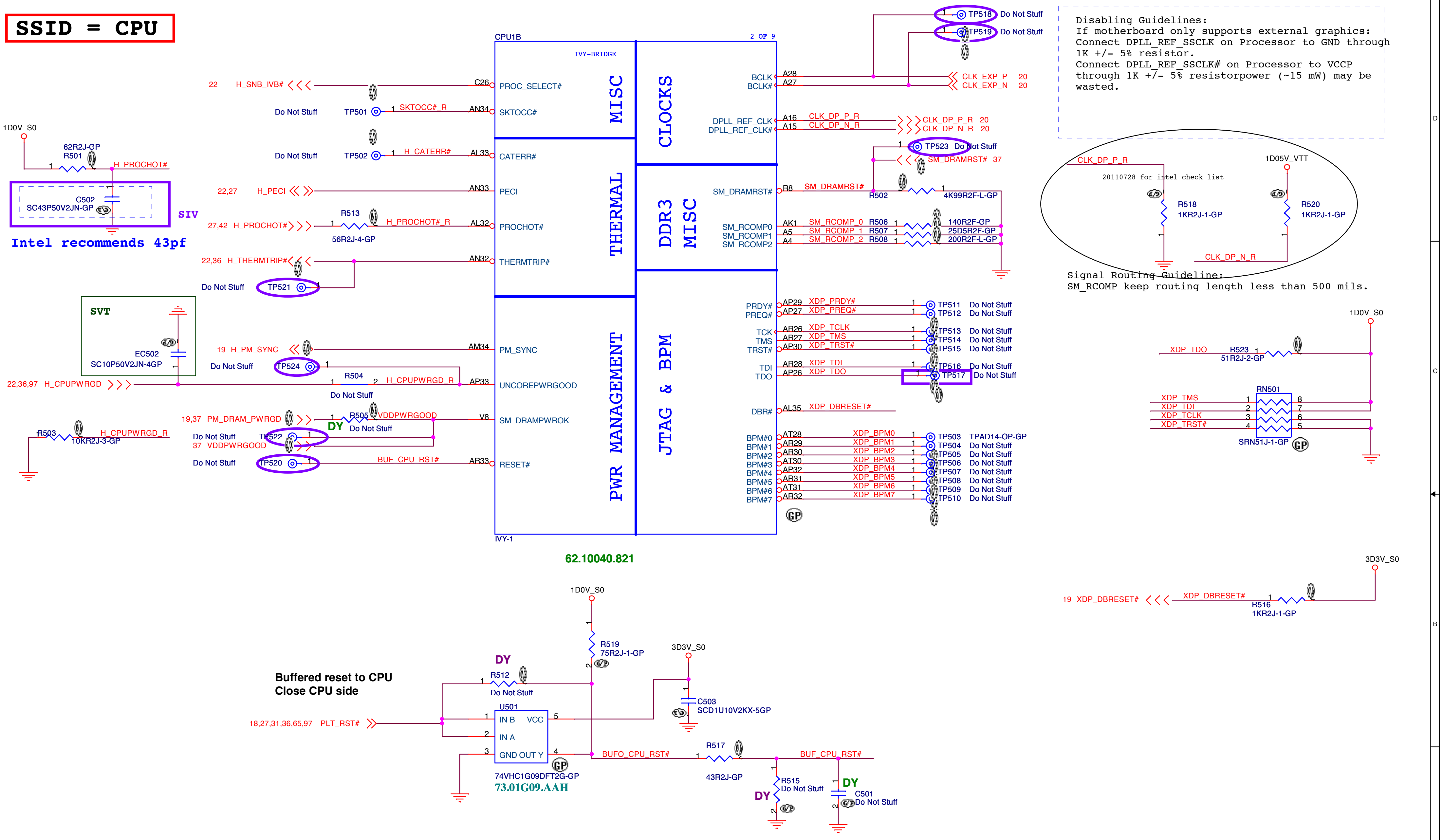
SSID = CPU



NOTE

	U501	R512	R519	R517	R515	C503	C501
HR	DY	0 ohm 63.R0034.1DL	DY	1.5K ohm 64.15015.6DL	750 ohm 64.75005.6DL	DY	DY
CRV	73.01G09.AAH	DY	75 ohm 63.75034.1DL	43 ohm 63.43034.1DL	DY	0.1uF 78.10423.2FL	DY

Default CRV

BOM

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Title: THERMAL/CLOCK/PM

Size: A3 | Document Number: LG4858_UMA | Rev: -1

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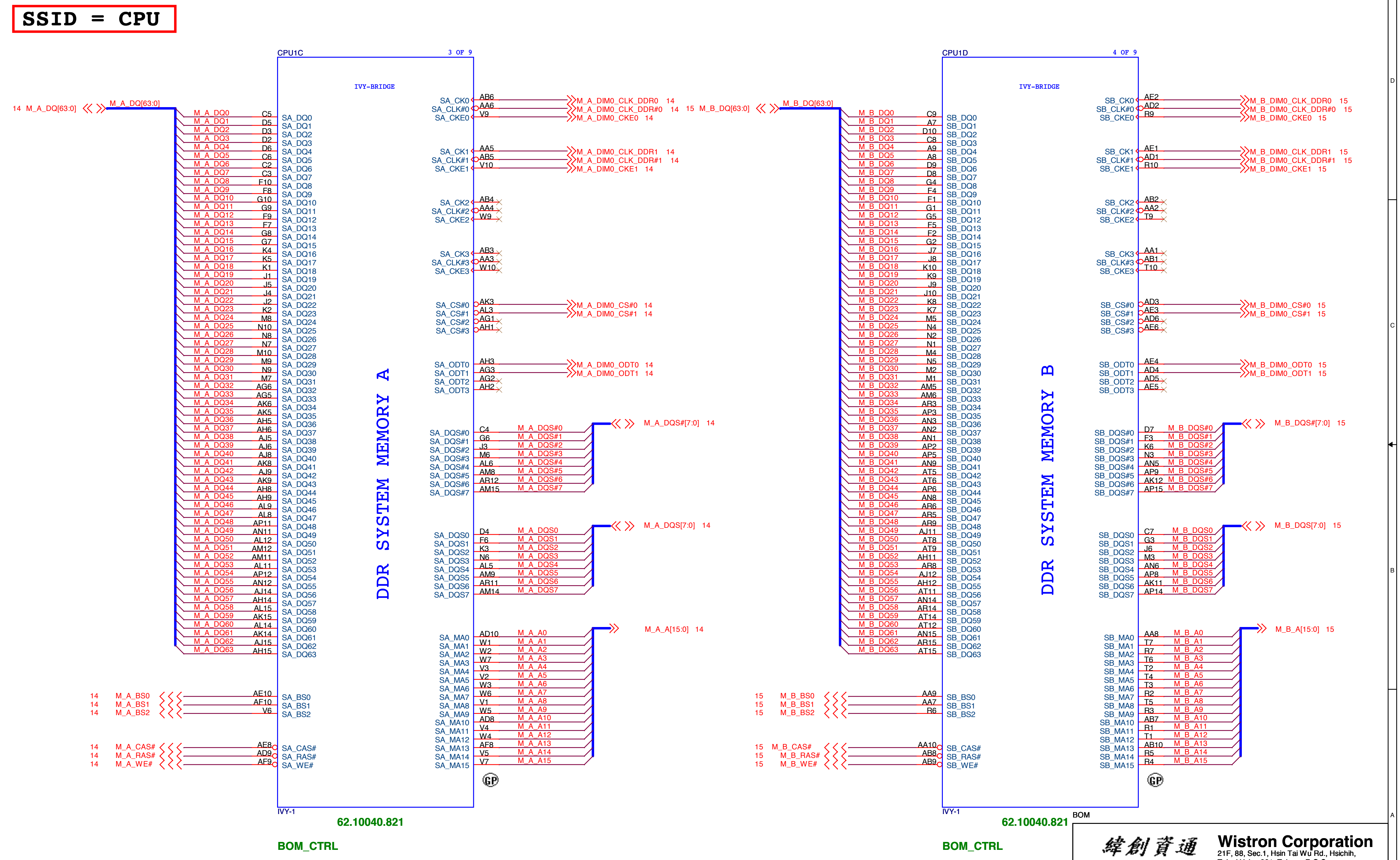

BOM

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (DDR)**

Size	Document Number	Rev
A3	LG4858_UMA	-1

Date: Friday, March 16, 2012 Sheet 6 of 103

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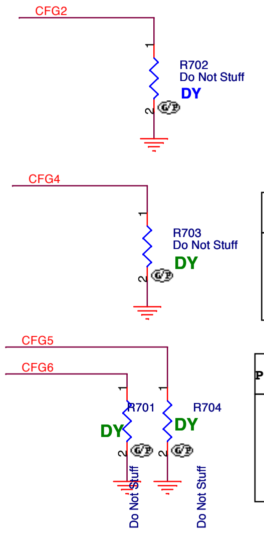
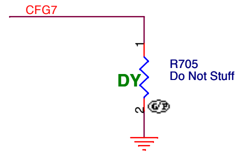
SSID = CPU



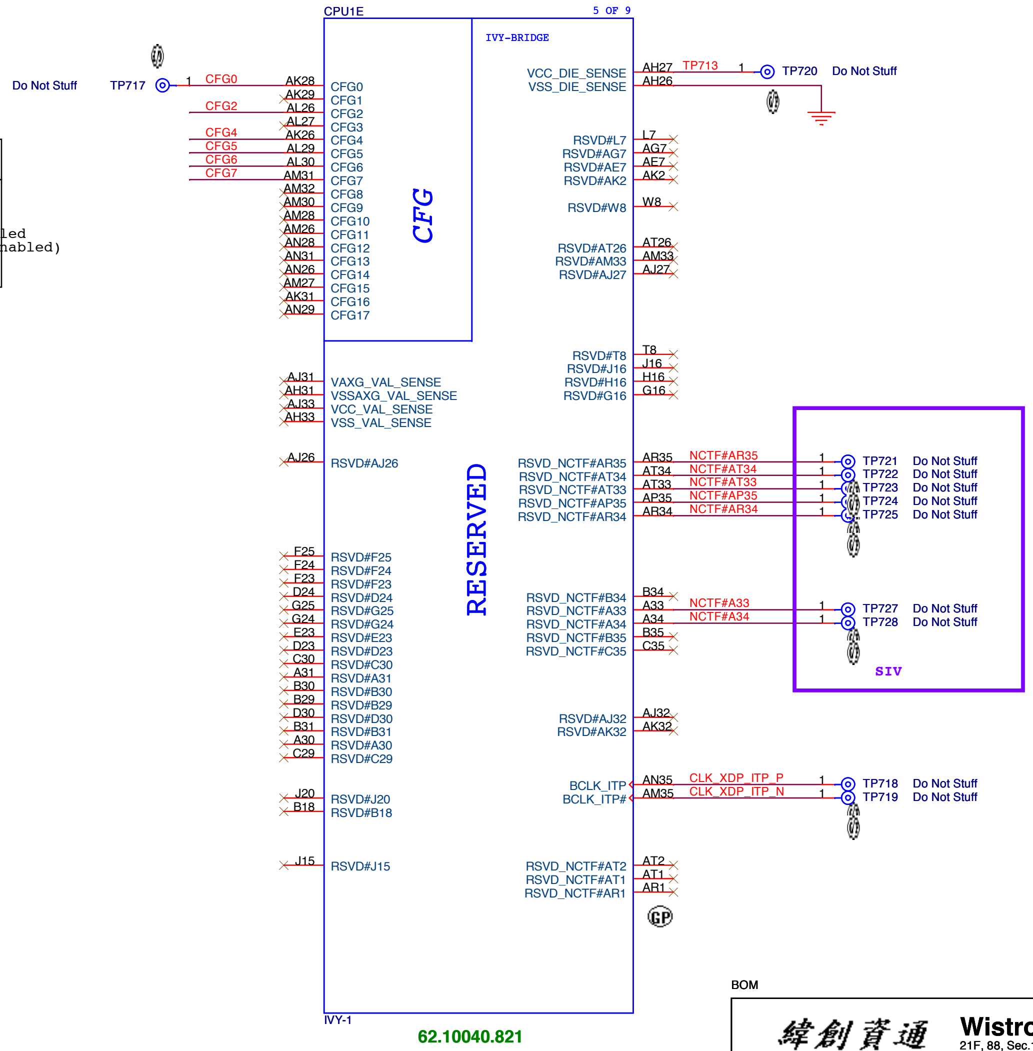
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	0:Lane Reversed

Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port
	0: Enabled; An external Display Port device is connected to the Embedded Display Port

PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled
	10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
	01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
	00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion
	0: PEG Wait for BIOS for training



62.10040.821

BOM_CTRL

BOM

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Title: CPU (RESERVED)		
Size: A3	Document Number: LG4858_UMA	Rev: -1
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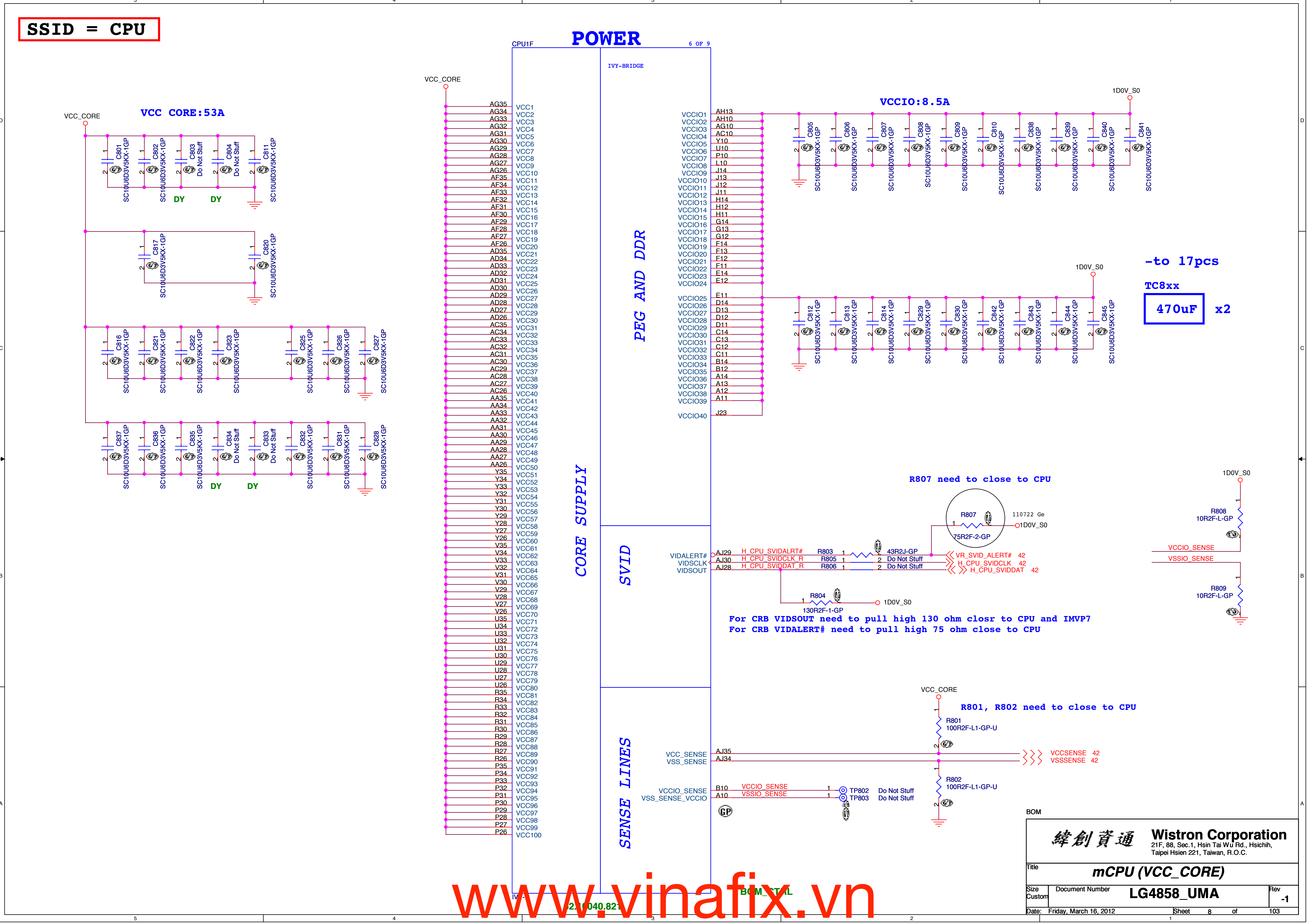

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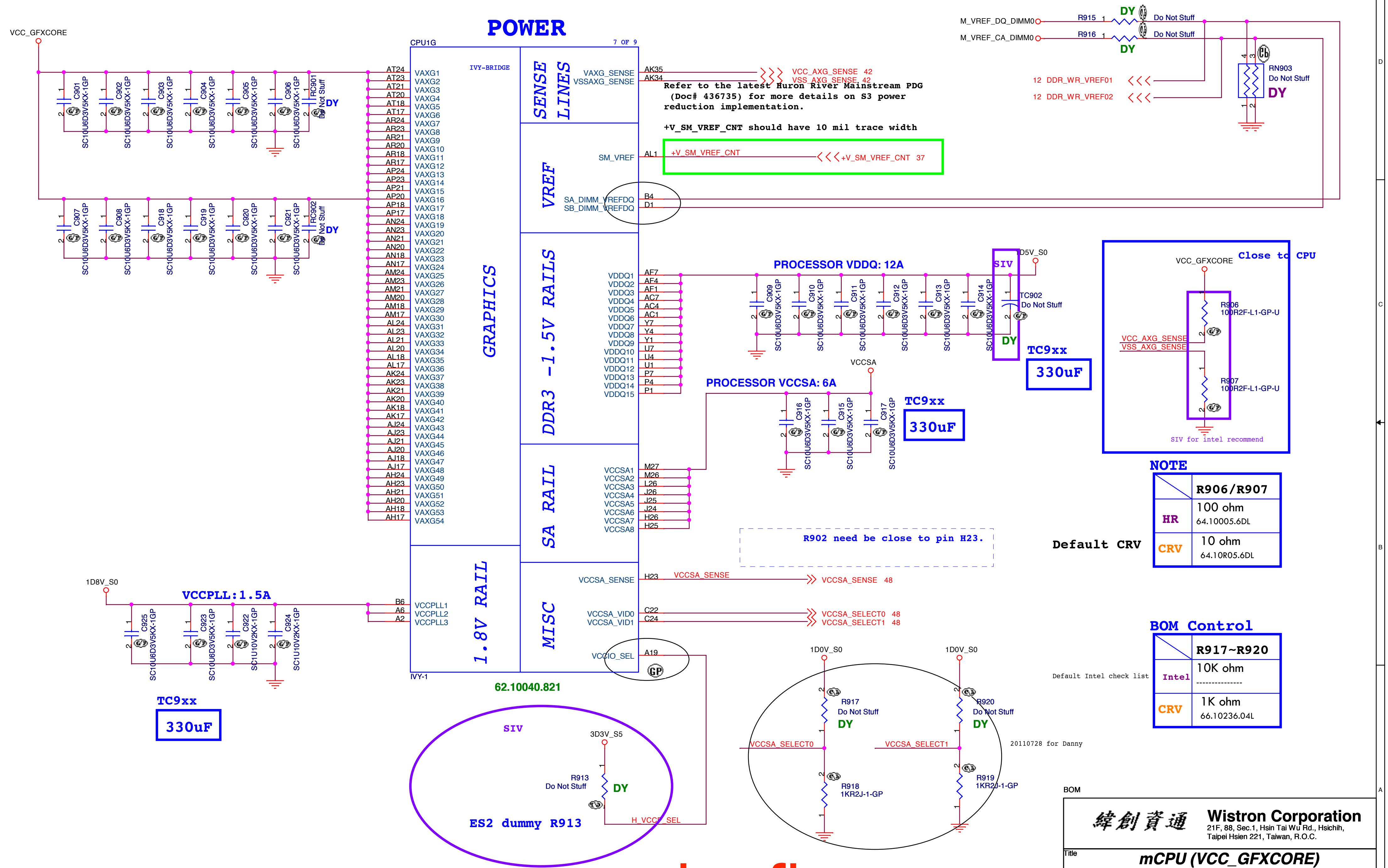
SSID = CPU

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

M3 - Processor Generated SO-DIMM VREF_DQ



NOTE

	R906/R907
HR	100 ohm 64.10005.6DL
CRV	10 ohm 64.10R05.6DL

Default CRV

BOM Control

	R917~R920
Intel	10K ohm --------------
CRV	1K ohm 66.10236.04L

Default Intel check list

BOM

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Title	mCPU (VCC_GFXCORE)		
Size A3	Document Number LG4858_UMA		Rev -1
Date: Friday, March 16, 2012		Sheet 9 of 103	

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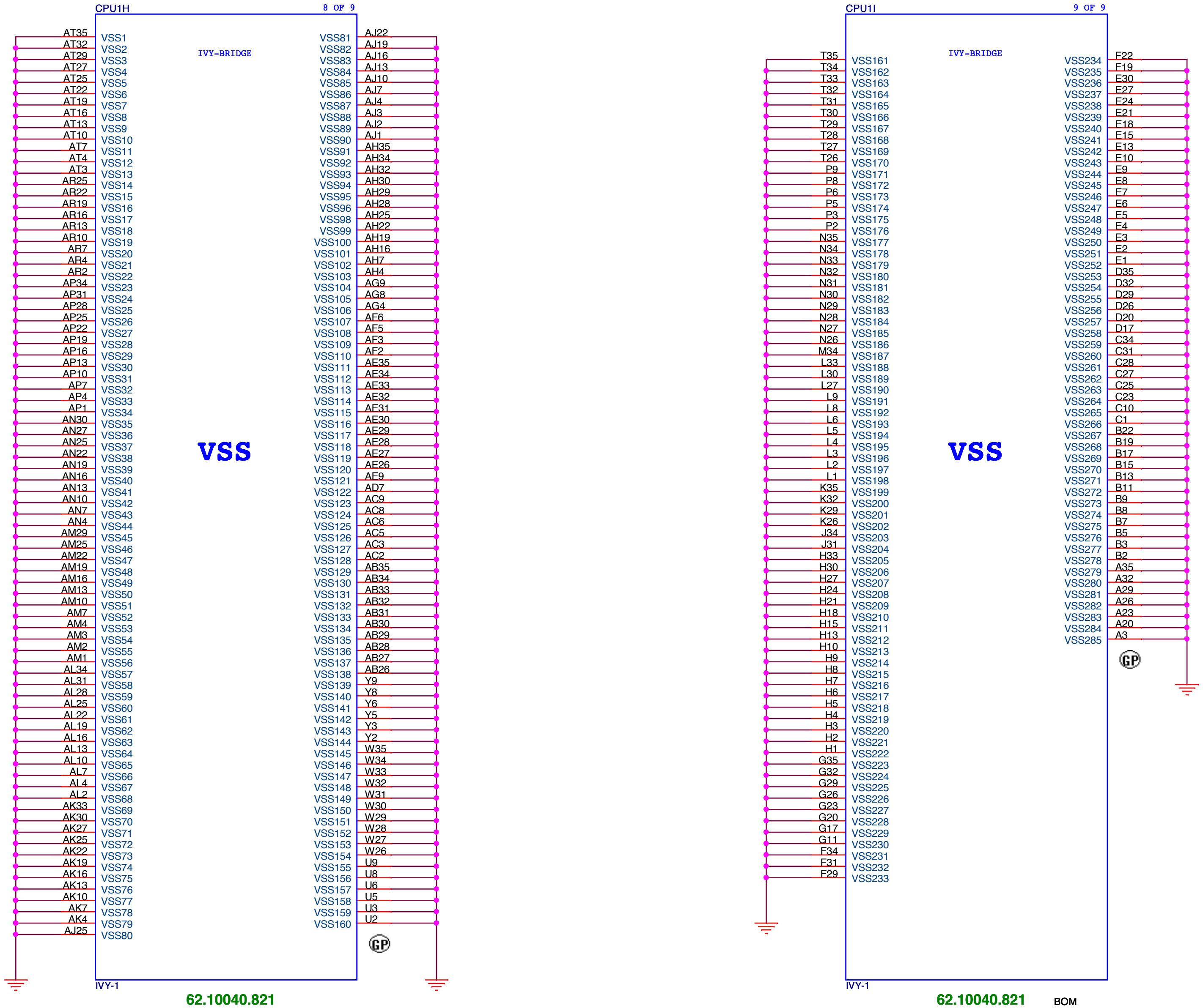
SSID = CPU



BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**CPU(VSS)**
Size A3	Document Number **LG4858_UMA** Rev -1
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5 4 3 2 1

D

C

(Reserved)

B

A

BOM

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Title	***XDP***
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Date: Friday, March 16, 2012	Sheet 11 of 103

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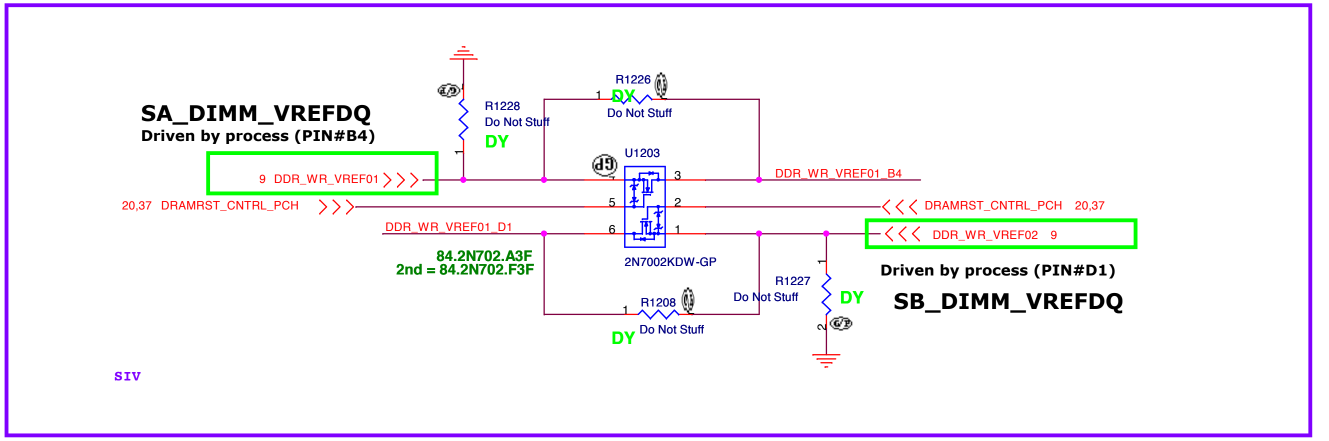
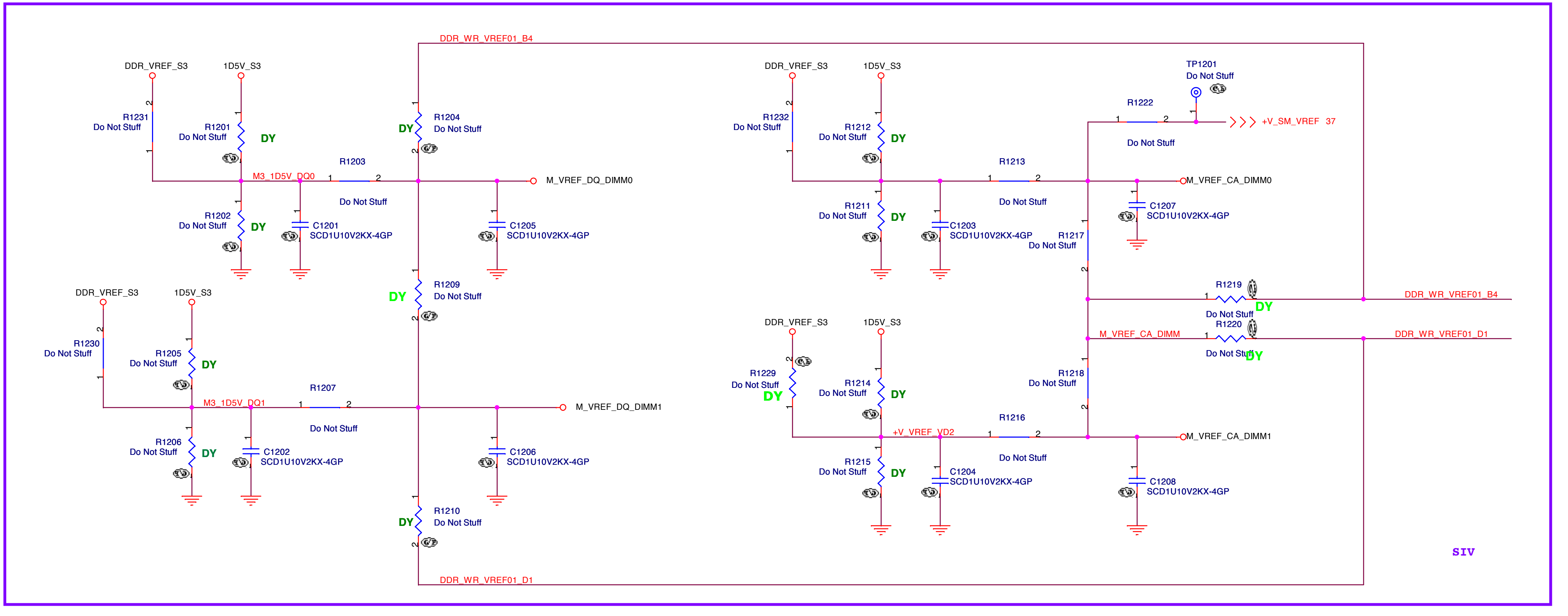
5 4 3 2 1

VREF circuit -M1 (Voltage Driver Network) & M3 (Driven by Processor) Implementation

For CRV:





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Title	M1 & M3 Implementation		
Size	Document Number	LG4858_UMA	Rev -1
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5 4 3 2 1

D

C

(Blanking)

B

A

BOM

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Title	***Reserved***	
Size	Document Number **LG4858_UMA**	Rev **-1**
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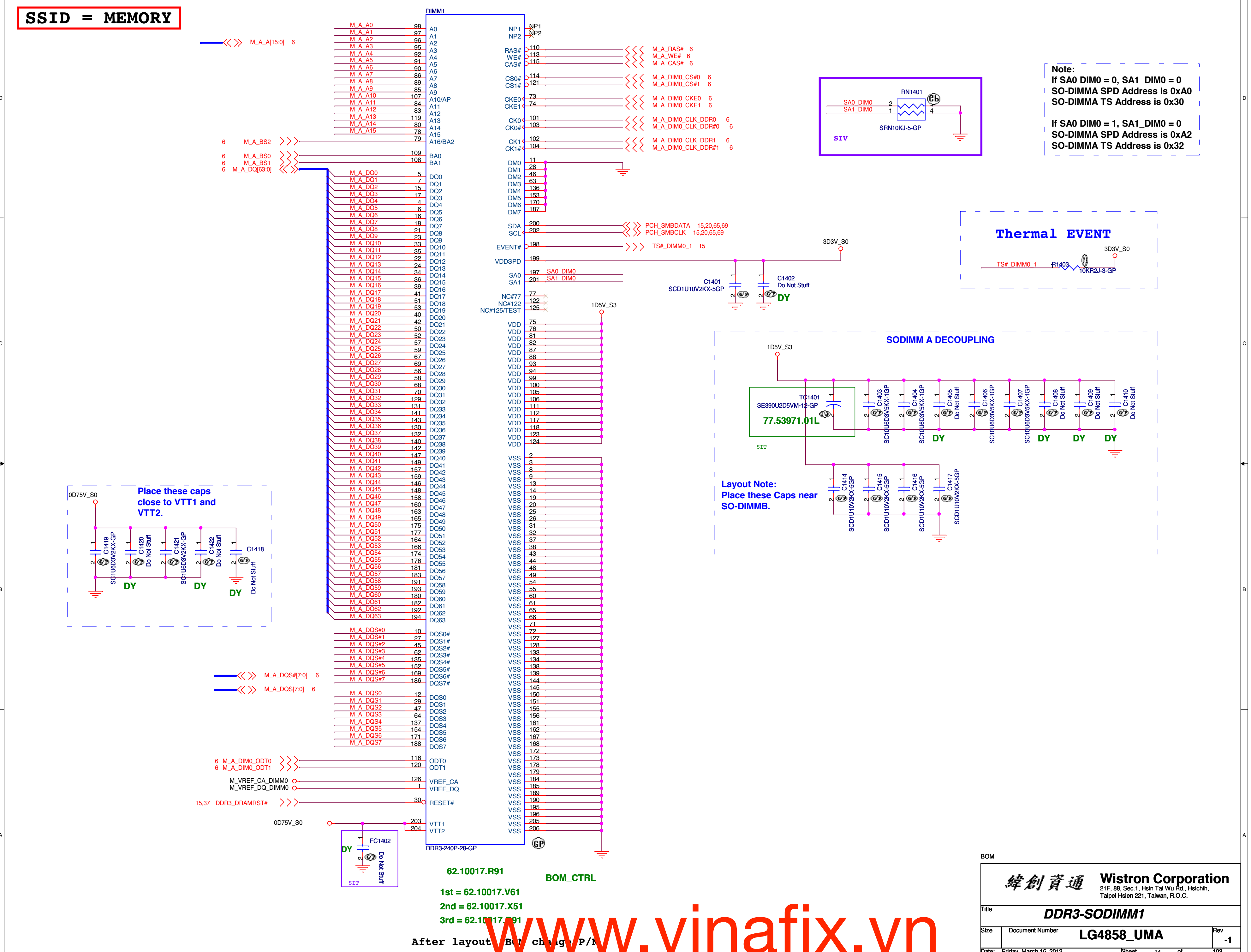
5 4 3 2 1



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Title	DDR3-SODIMM1	
Size	Document Number: LG4858_UMA	Rev: -1
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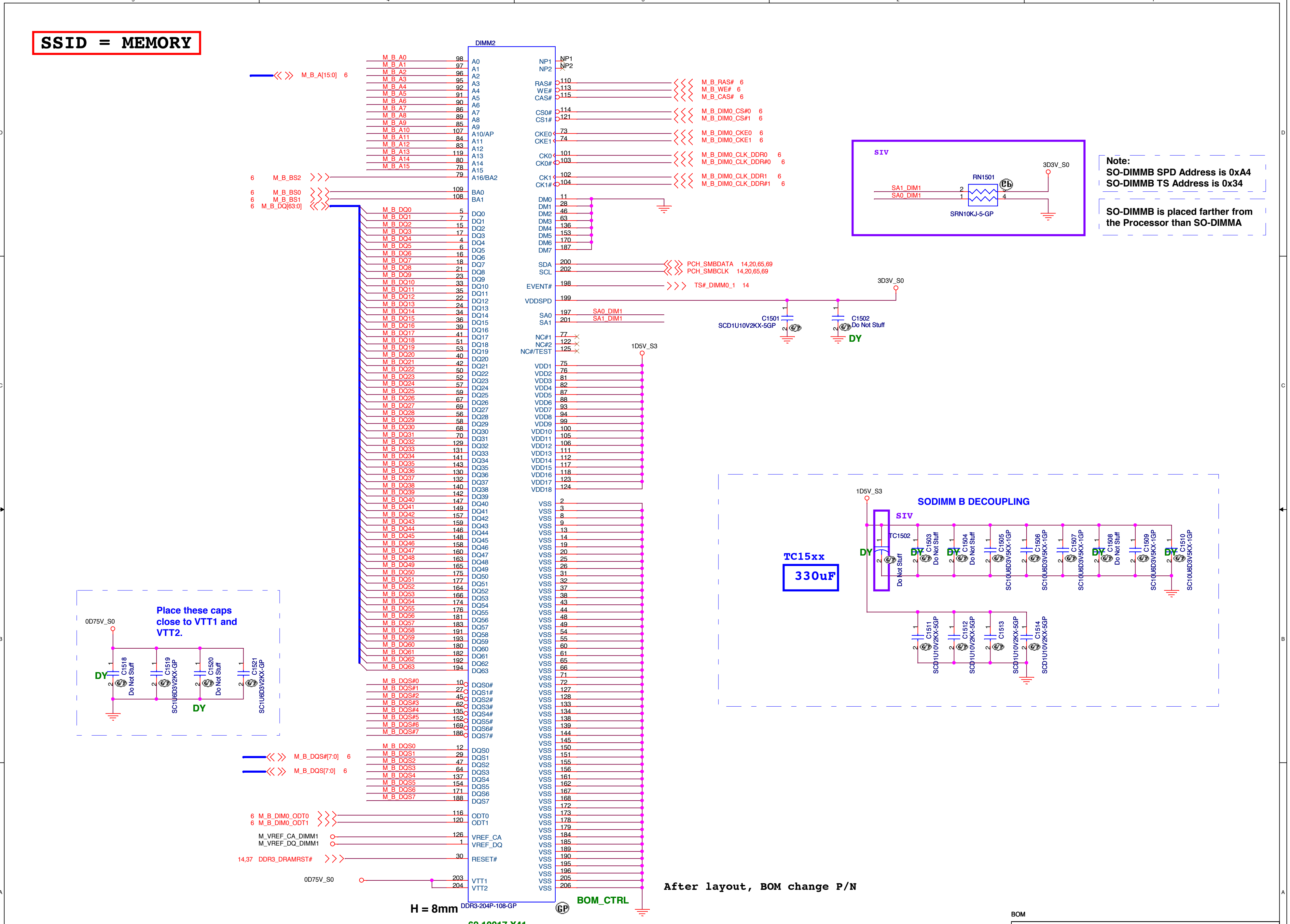

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Title	DDR3-SODIMM2
Size / Document Number	LG4858_UMA
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Title	DDR3-SODIMM3		
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Date: Friday, March 16, 2012	Sheet 16 of 103		

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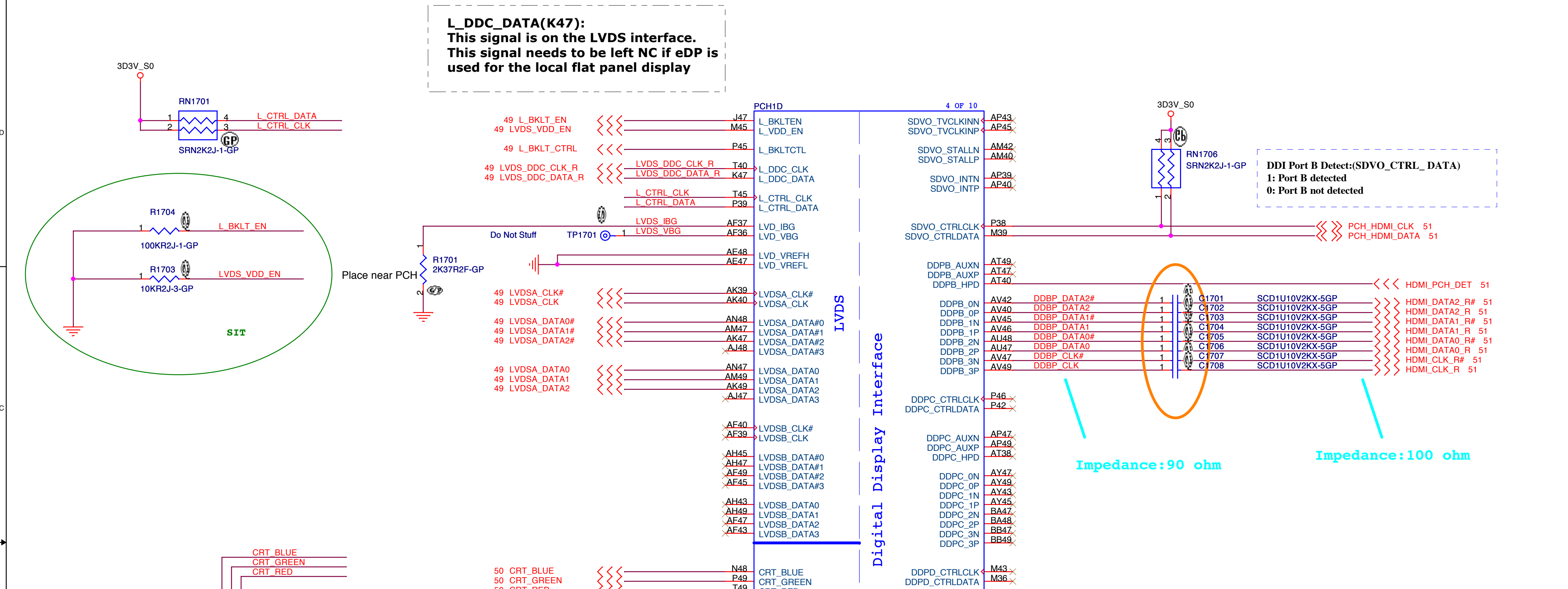

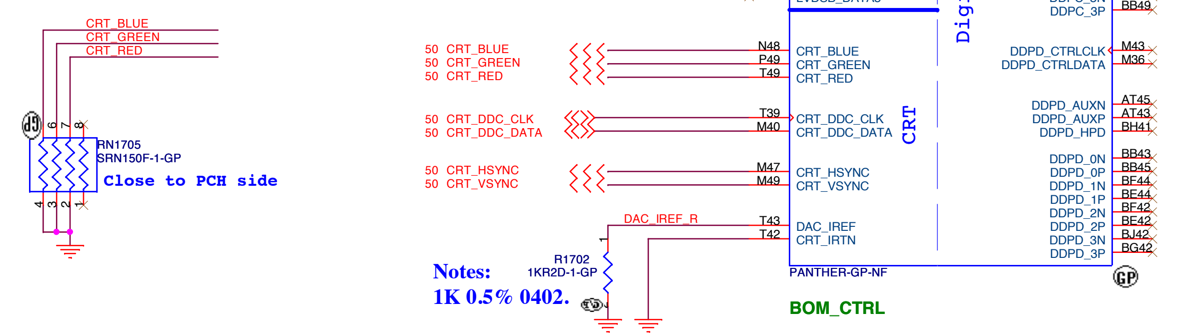

BOM_CTRL

SIV = 71.PANTH.D0U

PCH料號： 71.PANTH.D0U

Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMIB_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIB_CTRLDATA

Digital Display Ports Enable and Disable Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
LVDS	L_DDC_DATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port B	SDVO_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port C	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port D	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect

NOTE: LVDS and eDP on processor can not be enabled at the same time.

BOM

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Title	PCH (LVDS/CRT/HDMI)
Size / Document Number	LG4858_UMA
Rev	-1
Date:	Friday, March 16, 2012
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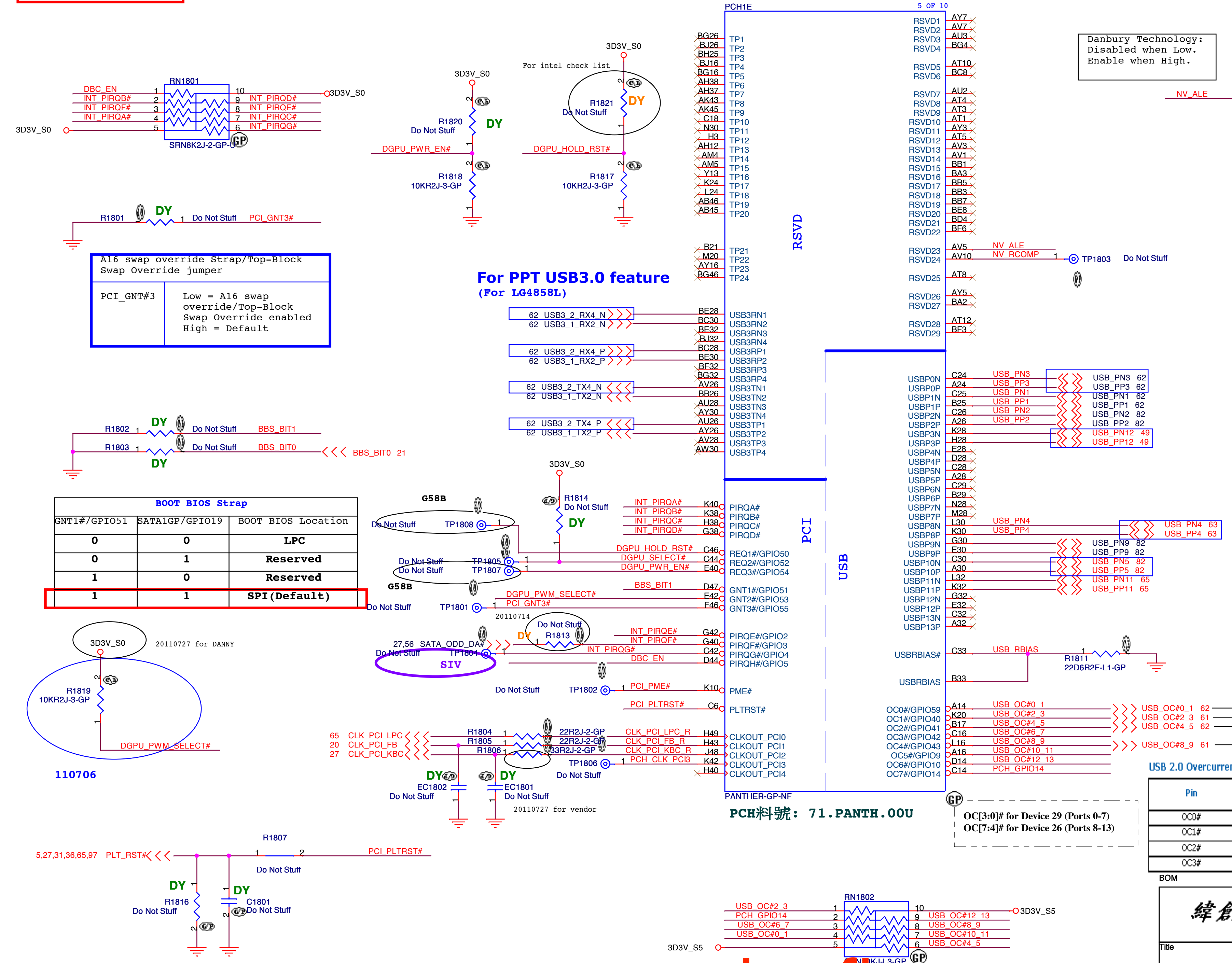
SSID = PCH



A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

BOOT BIOS Strap

GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

USB Table
(For LG4858L)

Pair	Device
0	USB3.0 ext port 2
1	USB3.0 ext port 1
2	USB2.0 ext port 4
3	CAMERA
4	X
5	X
6	X
7	X
8	BLUETOOTH
9	USB2.0 ext port 3
10	CARD READER
11	WLAN(Bluetooth)
12	X
13	X

Utilize Port 9 for USB debug

PCH料號: 71.PANTH.00U

OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

BOM

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Title: **PCH (PCI/USB/NVRAM)**

Size | Document Number: **LG4858_UMA** | Rev: -1

Date: Friday, March 16, 2012 | Sheet 18 of 103

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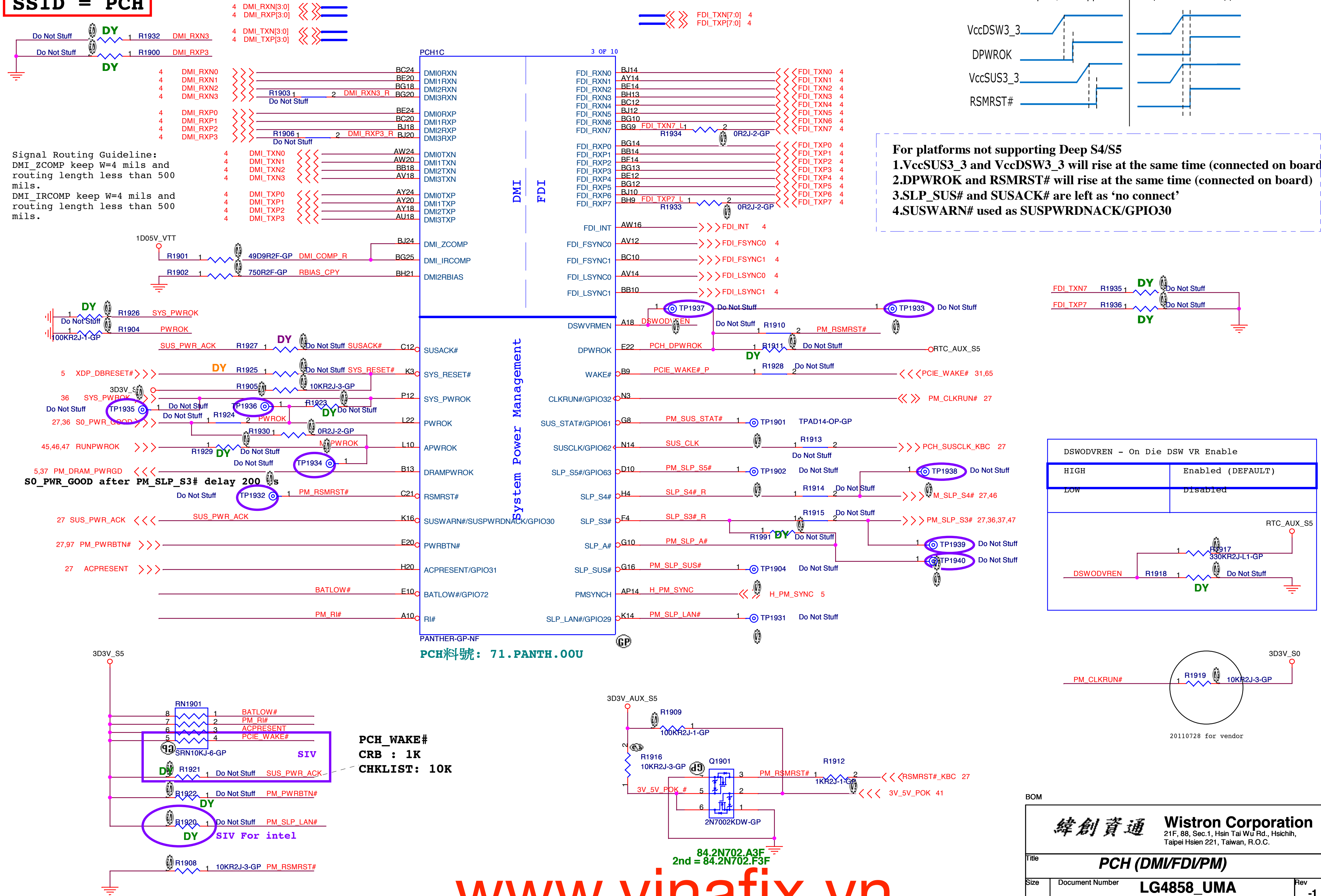
SSID = PCH



Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

For platforms not supporting Deep S4/S5
1. VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2. DPWROK and RSMRST# will rise at the same time (connected on board)
3. SLP_SUS# and SUSACK# are left as 'no connect'
4. SUSWARN# used as SUSPWRDNACK/GPIO30

DSWODVREN - On Die DSW VR Enable

HIGH	Enabled (DEFAULT)
LOW	Disabled

BOM

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Title	PCH (DMI/FDI/PM)		
Size	Document Number: LG4858_UMA		Rev -1
Date: Friday, March 16, 2012	Sheet 19 of 103		

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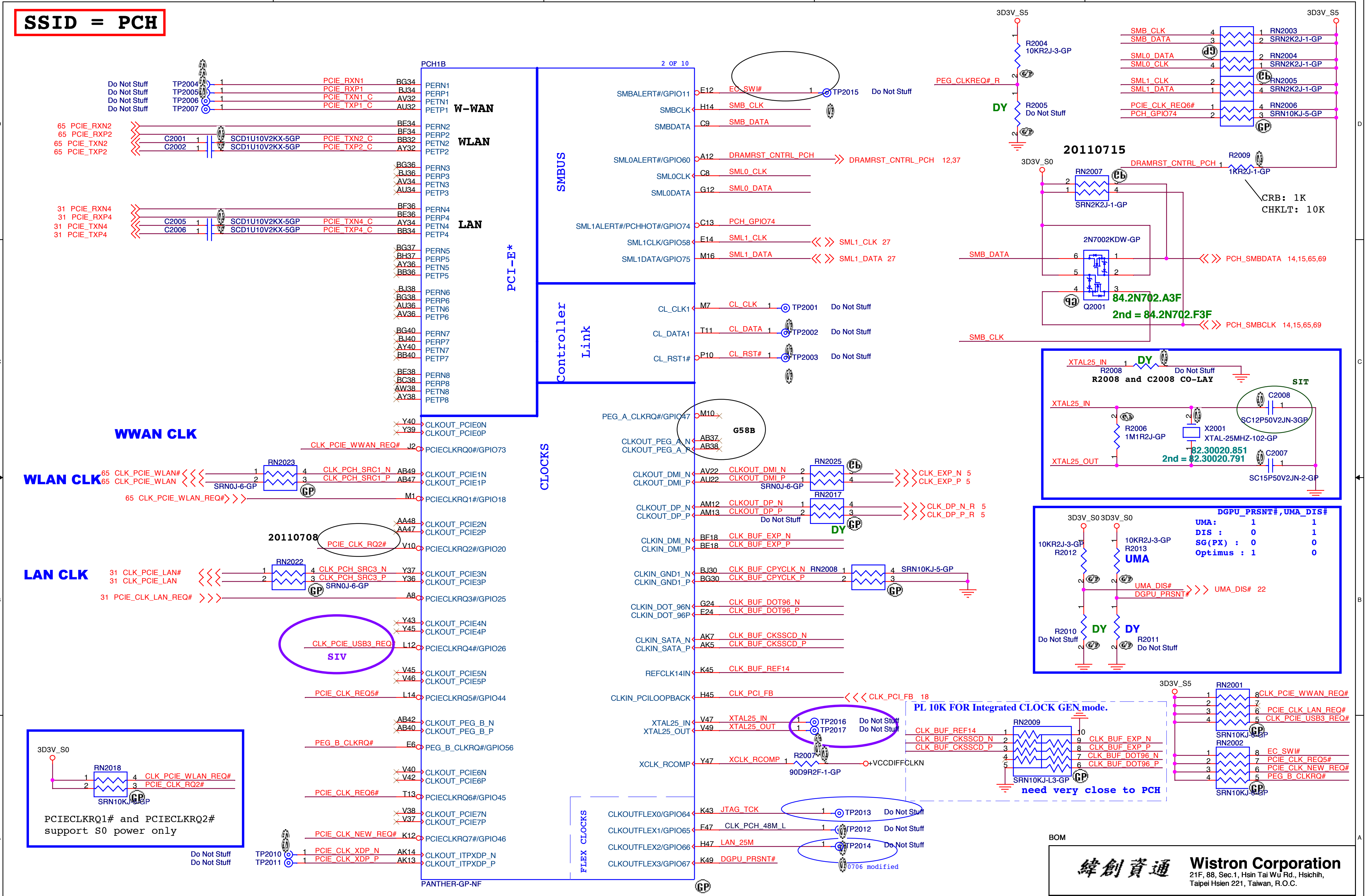
SSID = PCH



– Prioritize 27/14/24/48/25-MHz FLEX on FLEX1 and FLEX3
– Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0 and FLEX2 if more than 2 PCI clocks + PCI loopback are routed.

PCH料號: 71.PANTH.00U

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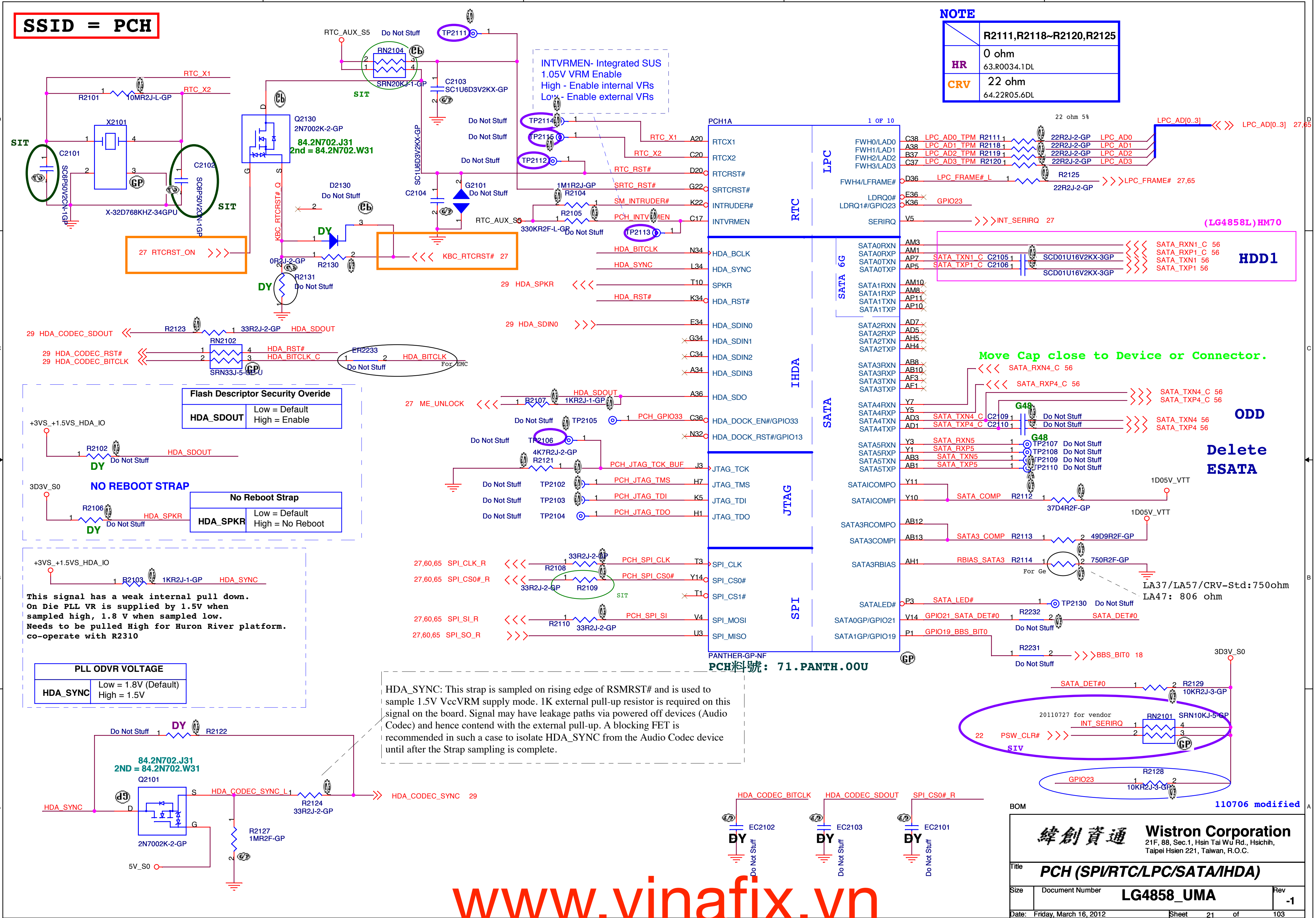
Title	PCH (PCI-E/SMBUS/CLOCK/CL)		
Size	Document Number: LG4858_UMA		Rev -1
Date: Friday, March 16, 2012	Sheet 20 of 103		



	R2111,R2118~R2120,R2125
HR	0 ohm 63.R0034.1DL
CRV	22 ohm 64.22R05.6DL

Flash Descriptor Security Overide	
HDA_SDOUT	Low = Default High = Enable

No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot

This signal has a weak internal pull down.
On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low.
Needs to be pulled High for Huron River platform.
co-operate with R2310

PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V

HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

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Title	PCH (SPI/RTC/LPC/SATA/IHDA)		
Size	Document Number: LG4858_UMA		Rev -1
Date: Friday, March 16, 2012		Sheet 21 of 103	

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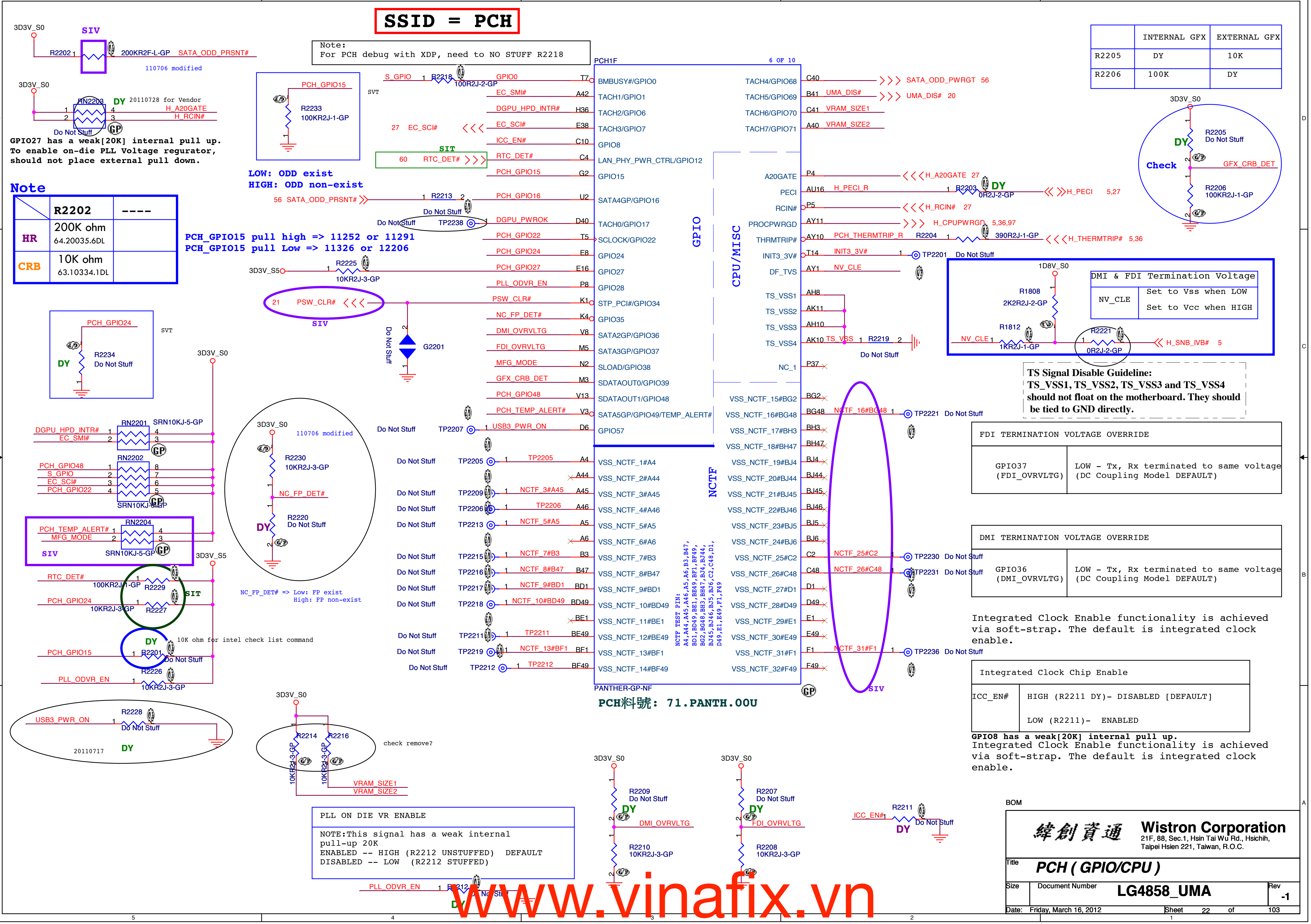
SSID = PCH

Note:
For PCH debug with XDP, need to NO STUFF R2218



GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.

LOW: ODD exist
HIGH: ODD non-exist

PCH_GPIO15 pull high => 11252 or 11291
PCH_GPIO15 pull Low => 11326 or 12206

Note

	R2202	----
HR	200K ohm 64.20035.6DL	
CRB	10K ohm 63.10334.1DL	

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

PCH料號: 71.PANTH.00U

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

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Title	PCH (GPIO/CPU)
Size / Document Number	LG4858_UMA
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Date:	Friday, March 16, 2012
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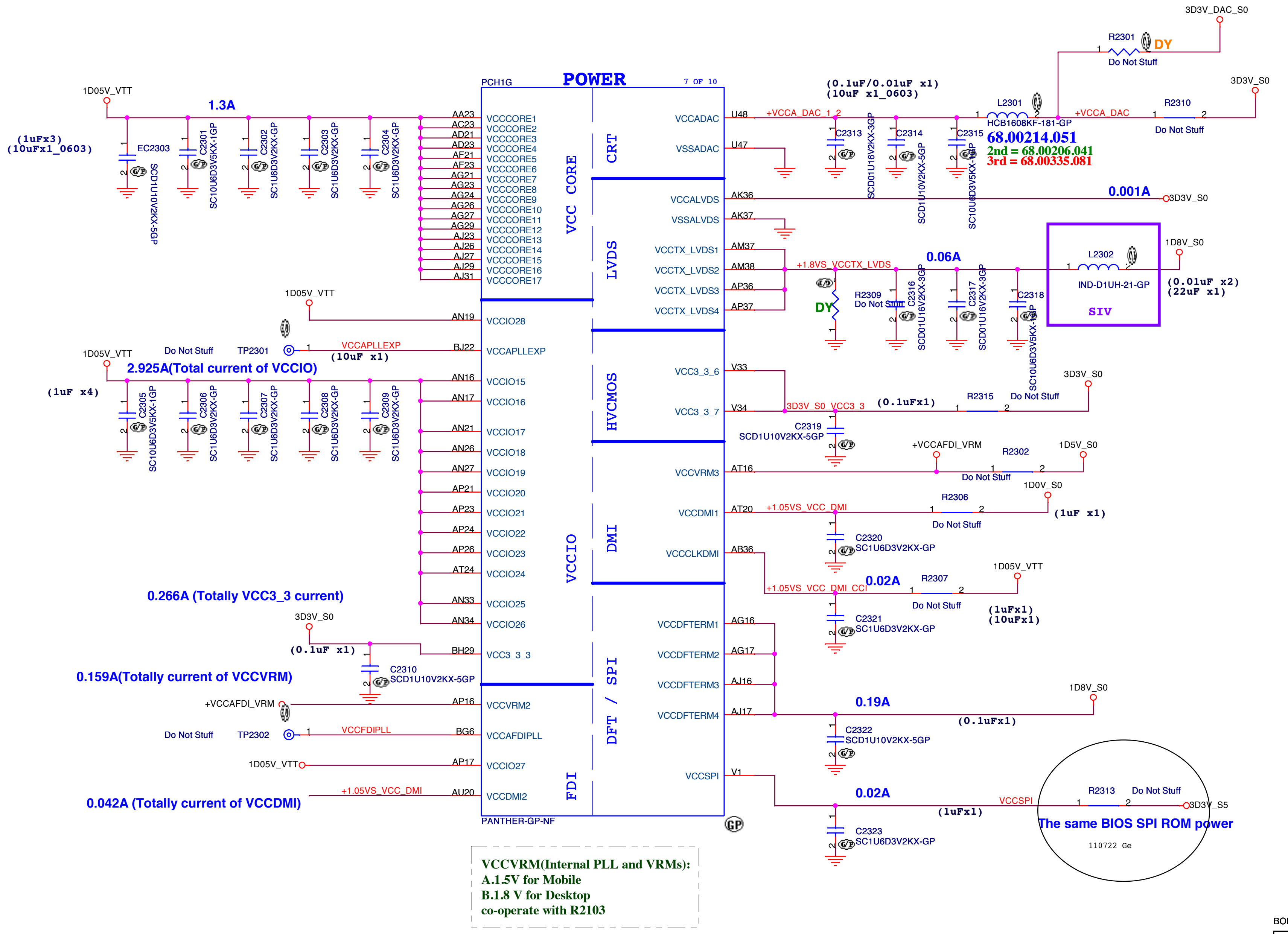
SSID = PCH 6A



VCCVRM(Internal PLL and VRMs):
A.1.5V for Mobile
B.1.8 V for Desktop
co-operate with R2103

Voltage Rail	Voltage	Iccmax
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.1	0.042
VccIO3	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW3_3	3.3	0.002
VccDFTERM	1.8	0.19
VccRTC	3.3	6u
VccSus3_3	3.3	0.097
VccSusHDA	3.3	0.01
VccVRM	1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS3	1.8	0.06

Refer to NPCE795 shared SPI flash architecture

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Title: PCH (POWER1)
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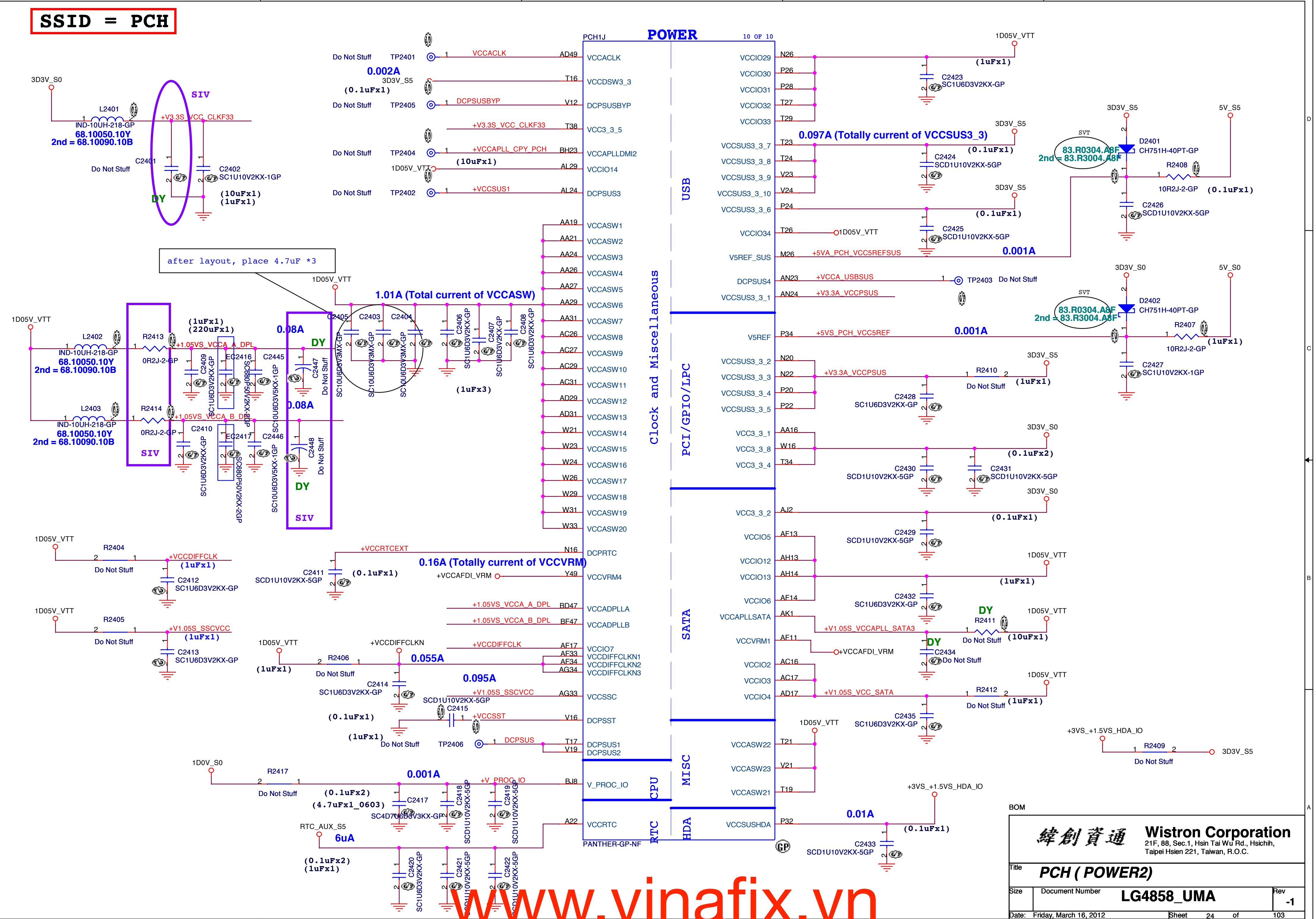

BOM

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Taipei Hsien 221, Taiwan, R.O.C.

Title	PCH (POWER2)	
Size	Document Number: LG4858_UMA	Rev: -1
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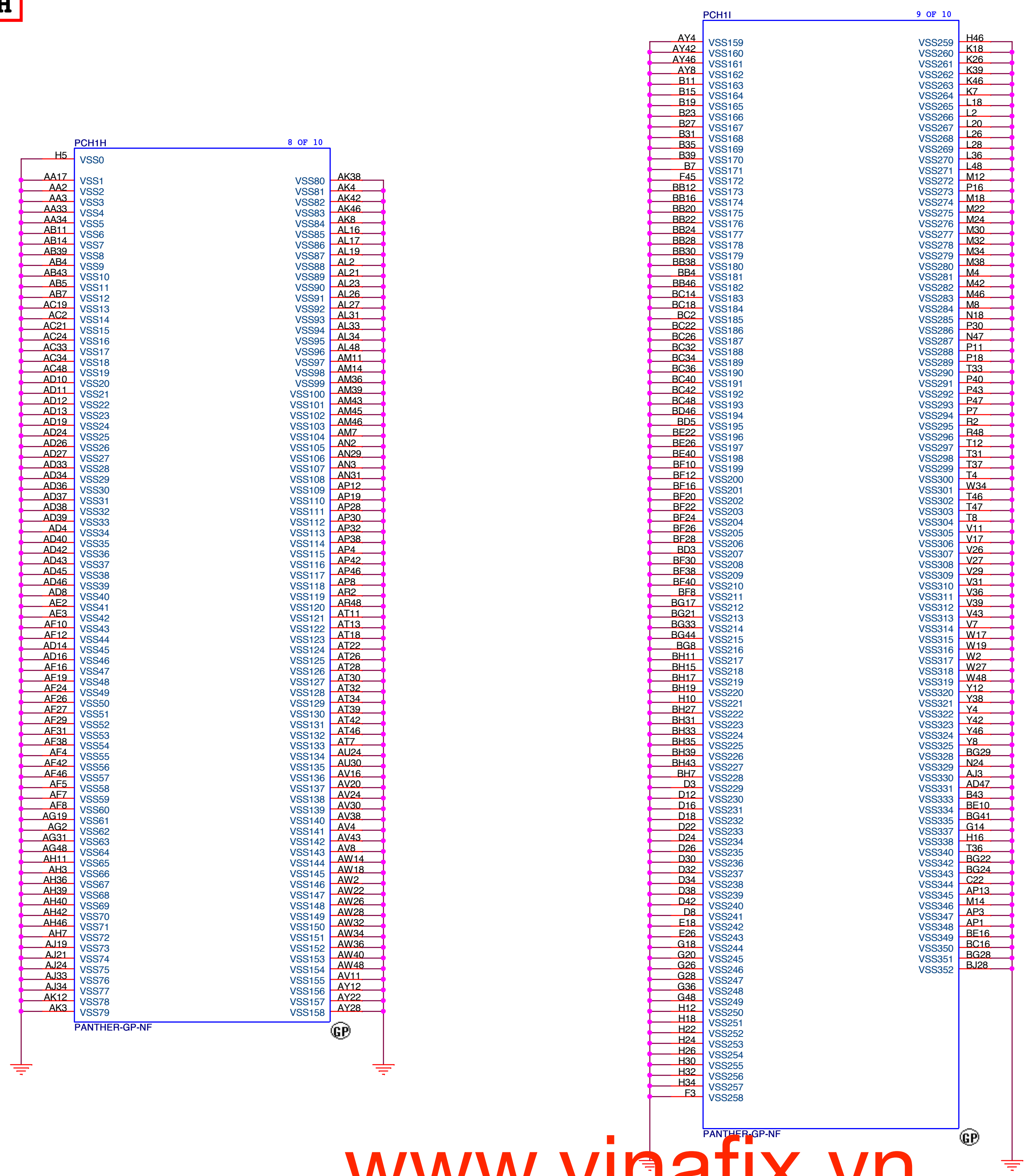
SSID = PCH



BOM

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Title	*PCH (VSS)*		
Size	Document Number: LG4858_UMA		Rev: -1
Date: Friday, March 16, 2012	Sheet 25	of	103

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Title	***Reserved***		
Size	Document Number	**LG4858_UMA**	Rev **-1**
Date:	Friday, March 16, 2012	Sheet 26 of 103	

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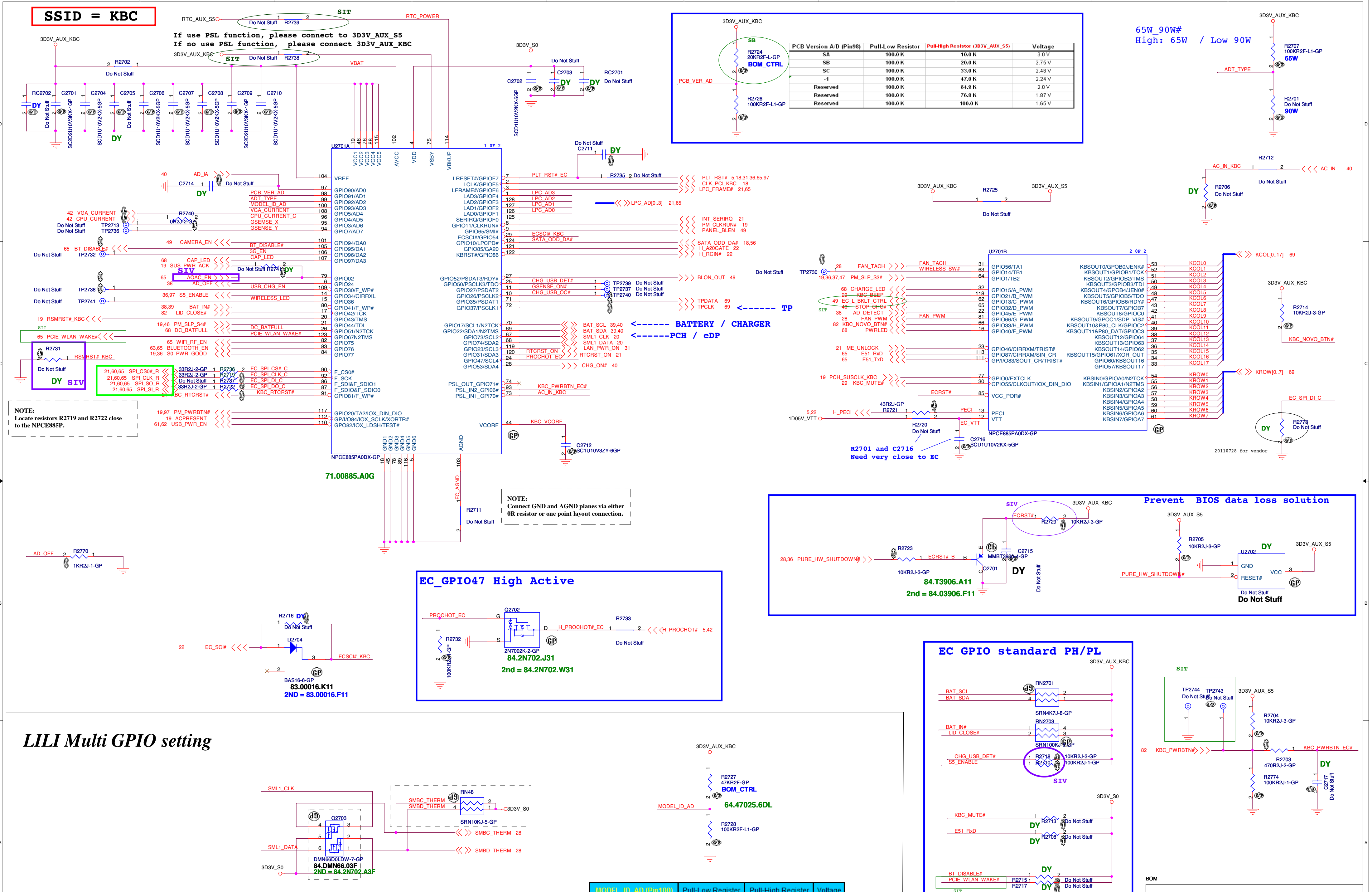
5 4 3 2 1



PCB Version A/D (Pin98)	Pull-Low Resistor	Pull-High Resistor (3D3V_AUX_S5)	Voltage
SA	100.0 K	10.0 K	3.0 V
SB	100.0 K	20.0 K	2.75 V
SC	100.0 K	33.0 K	2.48 V
-1	100.0 K	47.0 K	2.24 V
Reserved	100.0 K	64.9 K	2.0 V
Reserved	100.0 K	76.8 K	1.87 V
Reserved	100.0 K	100.0 K	1.65 V

MODEL_ID_AD (Pin100)	Pull-Low Register	Pull-High Register	Voltage	
LG48 UMA	100.0 K	10.0 K	3.000 V	64.10025.6DL
LG48 OPTIMUS	100.0 K	20.0 K	2.750 V	64.20025.6DL
LG58 UMA	100.0 K	33[illegible] K	2.481 V	64.33025.6DL
LG[illegible] OPT[illegible]MUS	[illegible]0.0 [illegible]	47[illegible] K	2.[illegible]5 V	64.[illegible]025.[illegible]DL

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Title: KBC Nuvoton NPCE795

Size | Document Number: LG4858_UMA | Rev: -1

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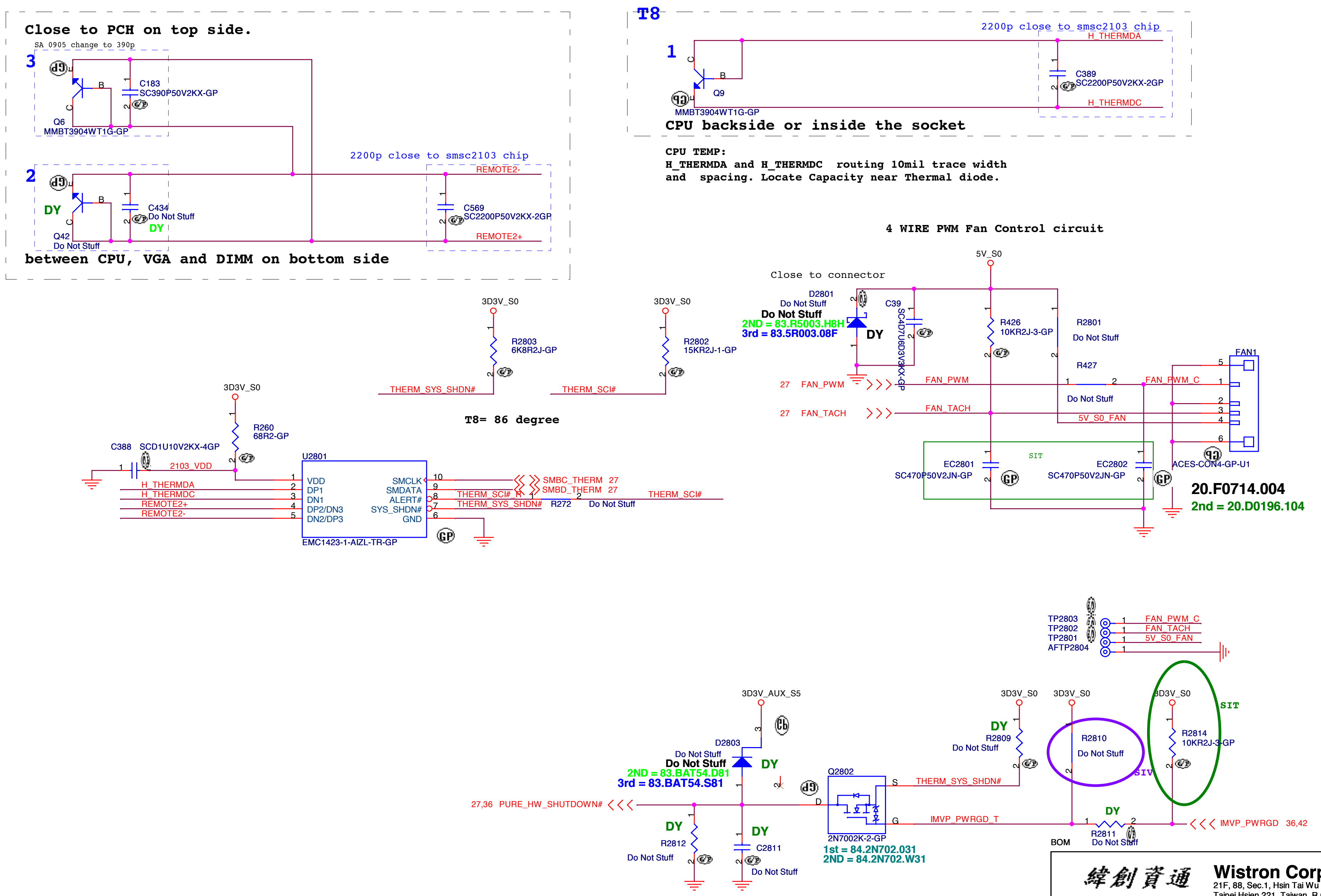
SSID = Thermal

Thermal sensor



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Title	THERMAL EMC1423	
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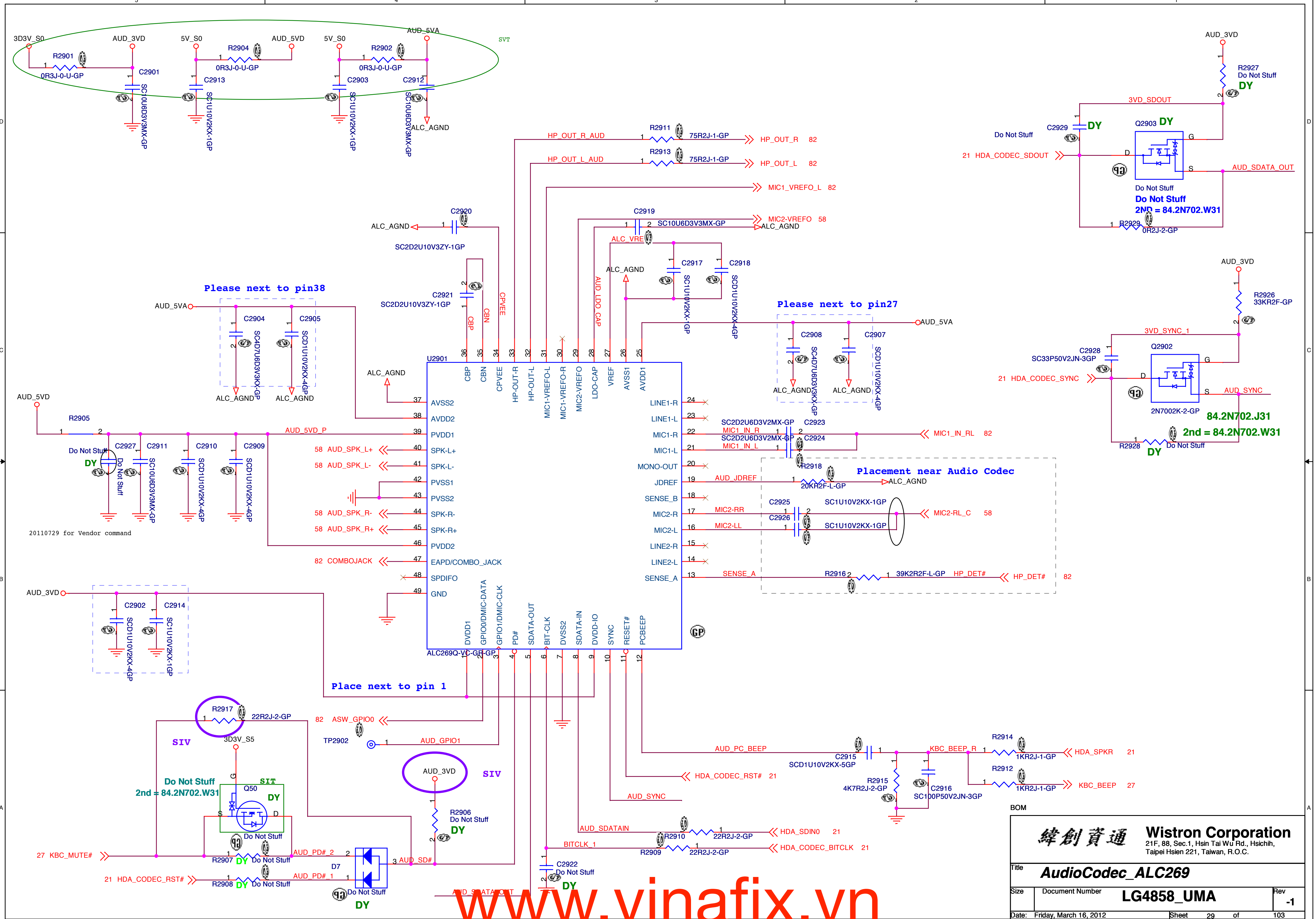

BOM

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Title	AudioCodec_ALC269	
Size	Document Number: LG4858_UMA	Rev: -1
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Title	***Audio_AMP***	
Size	Document Number **LG4858_UMA**	Rev **-1**
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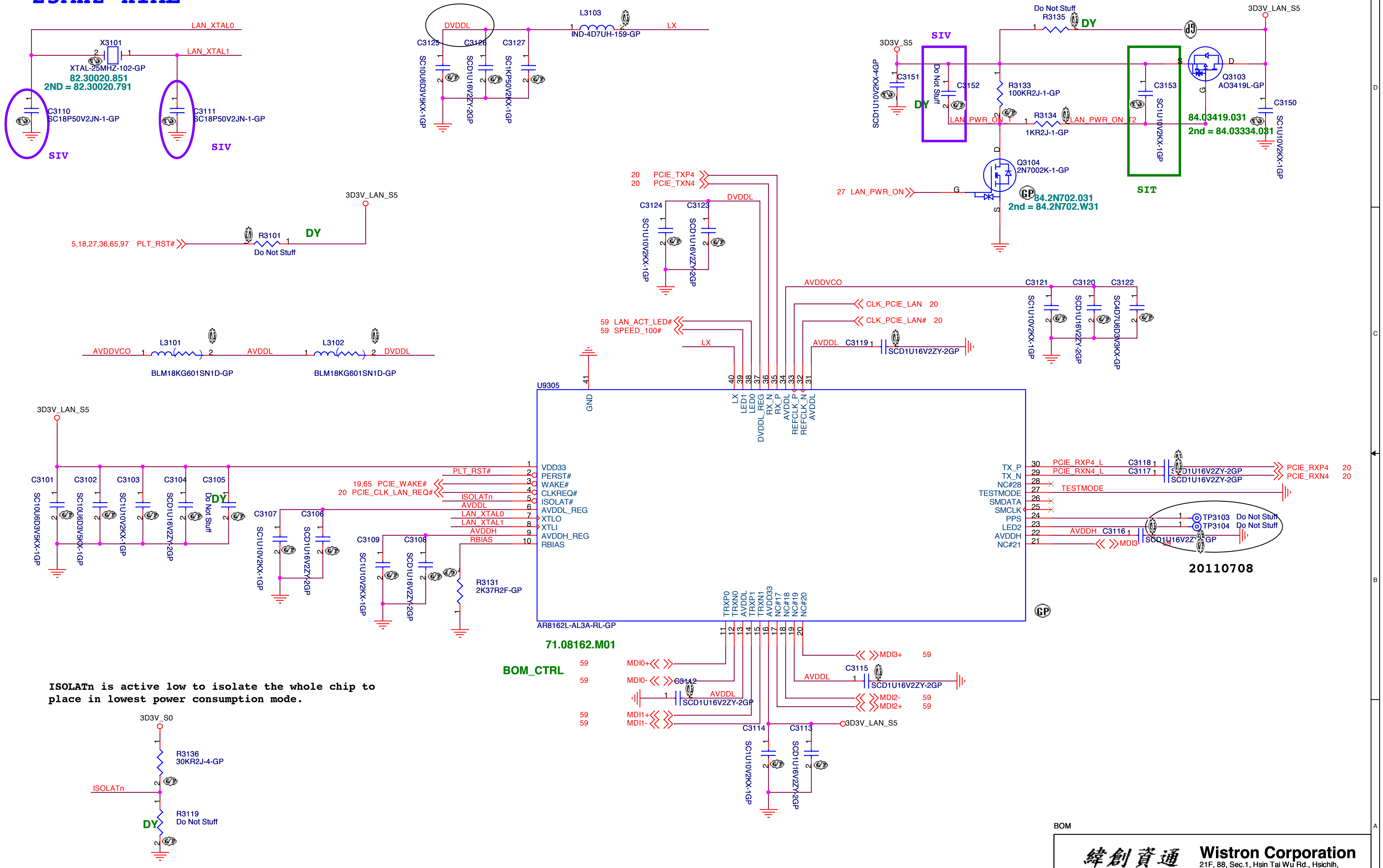
25MHz XTAL



ISOLATn is active low to isolate the whole chip to place in lowest power consumption mode.

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Title	LOM		
Size	Document Number	LG4858_UMA	Rev -1
Date:	Friday, March 16, 2012	Sheet 31 of 103	

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Title	***Card reader***	
Size	Document Number **LG4858_UMA**	Rev **-1**
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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*1394*	
Size	Document Number **LG4858_UMA**	Rev **-1**
Date: Friday, March 16, 2012	Sheet 33 of 103	

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Title	*Smart card*		
Size	Document Number	LG4858_UMA	Rev -1
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BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	***USB 3.0 CONTROLLER***		
Size	Document Number	**LG4858_UMA**	Rev **-1**
Date: Friday, March 16, 2012		Sheet 35 of 103	

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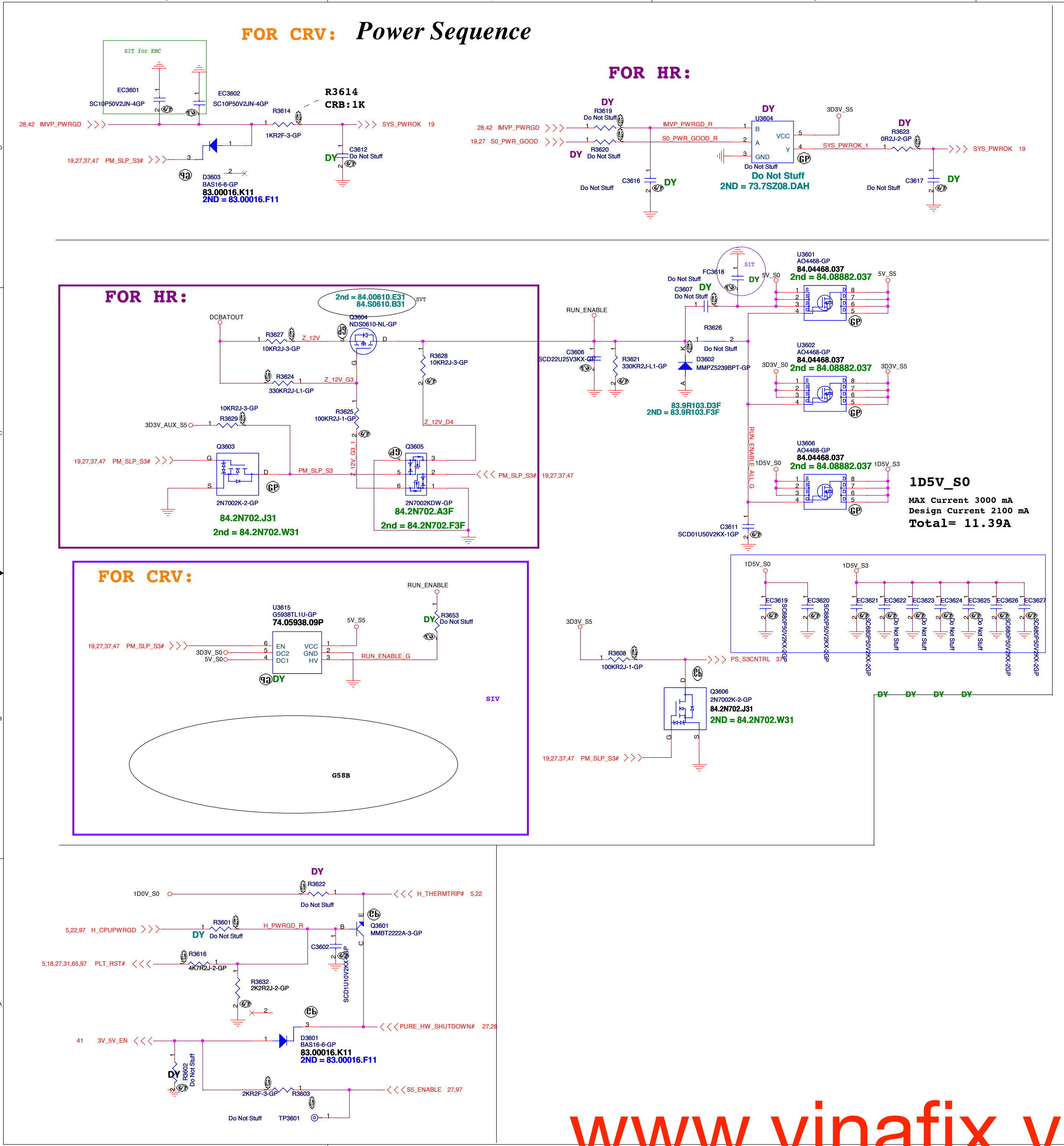

BOM

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	PowerPlane Enable&Sequence	
Size	Document Number: LG4858_UMA	Rev: -1
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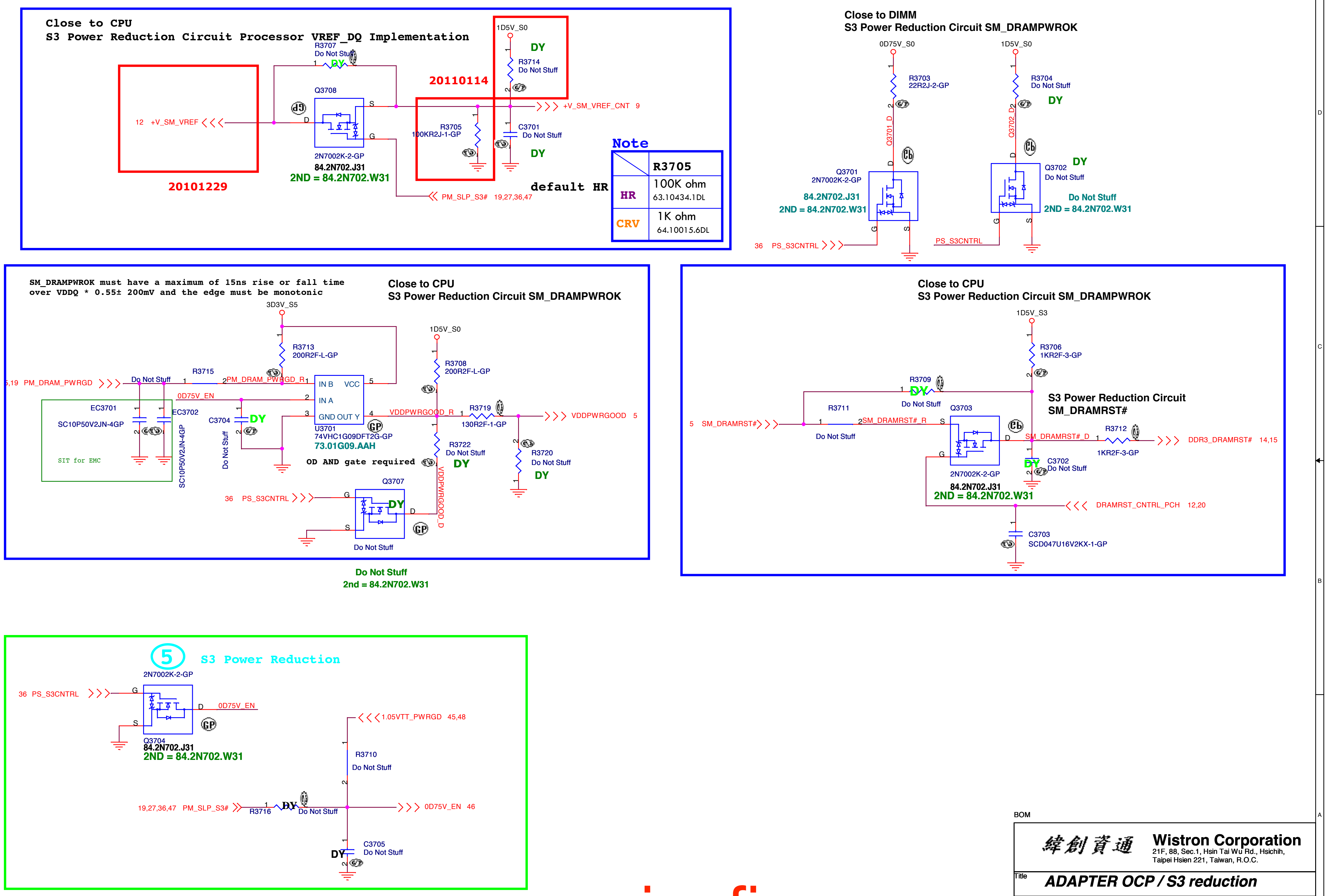

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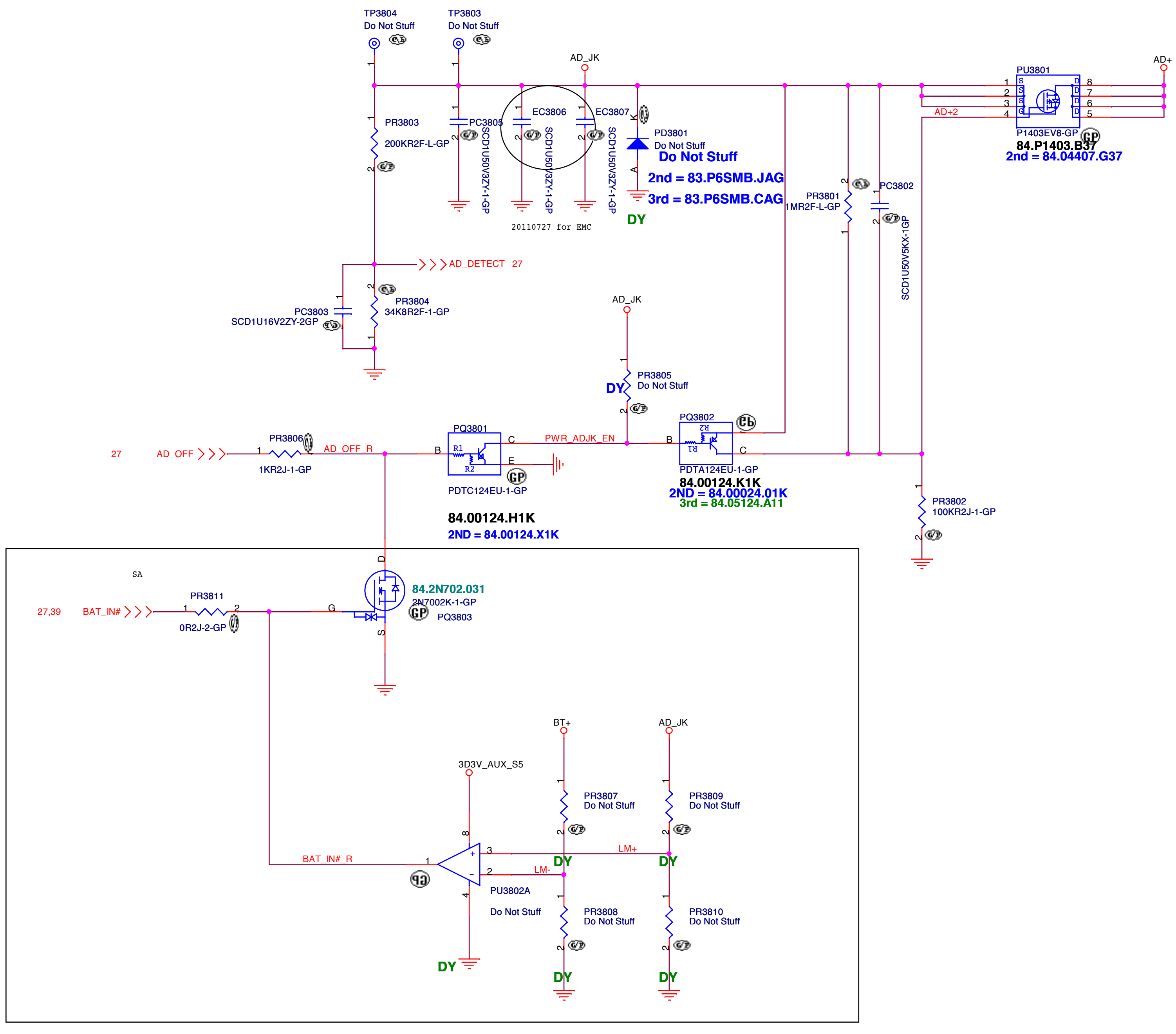
Adaptor in to generate DCBATOUT



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Title	DCIN JACK		
Size	Document Number: LG4858_UMA		Rev: -1
Date: Friday, March 16, 2012	Sheet 38 of 103		

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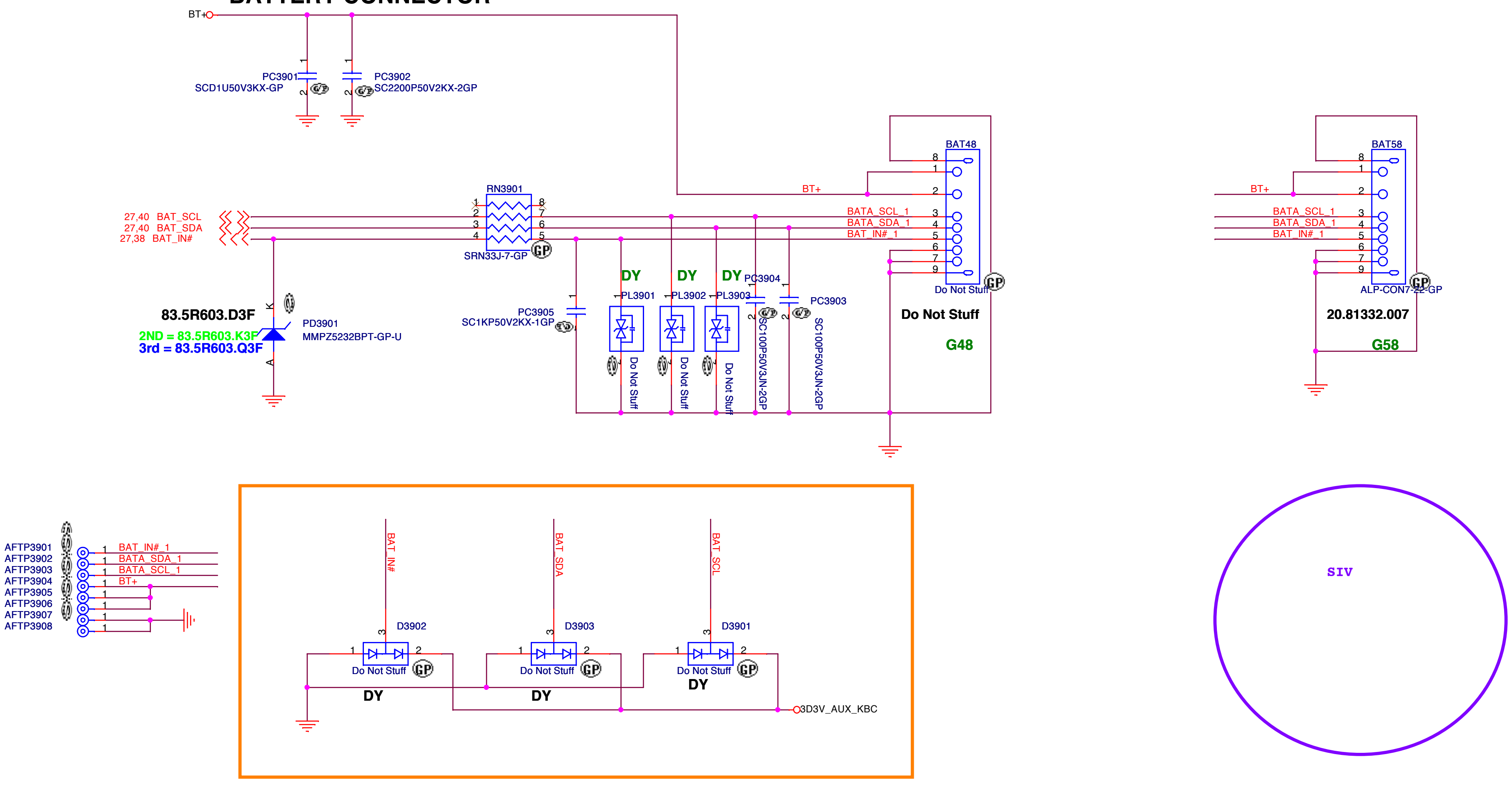
BATTERY CONNECTOR



BOM

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Title	BATT CONN		
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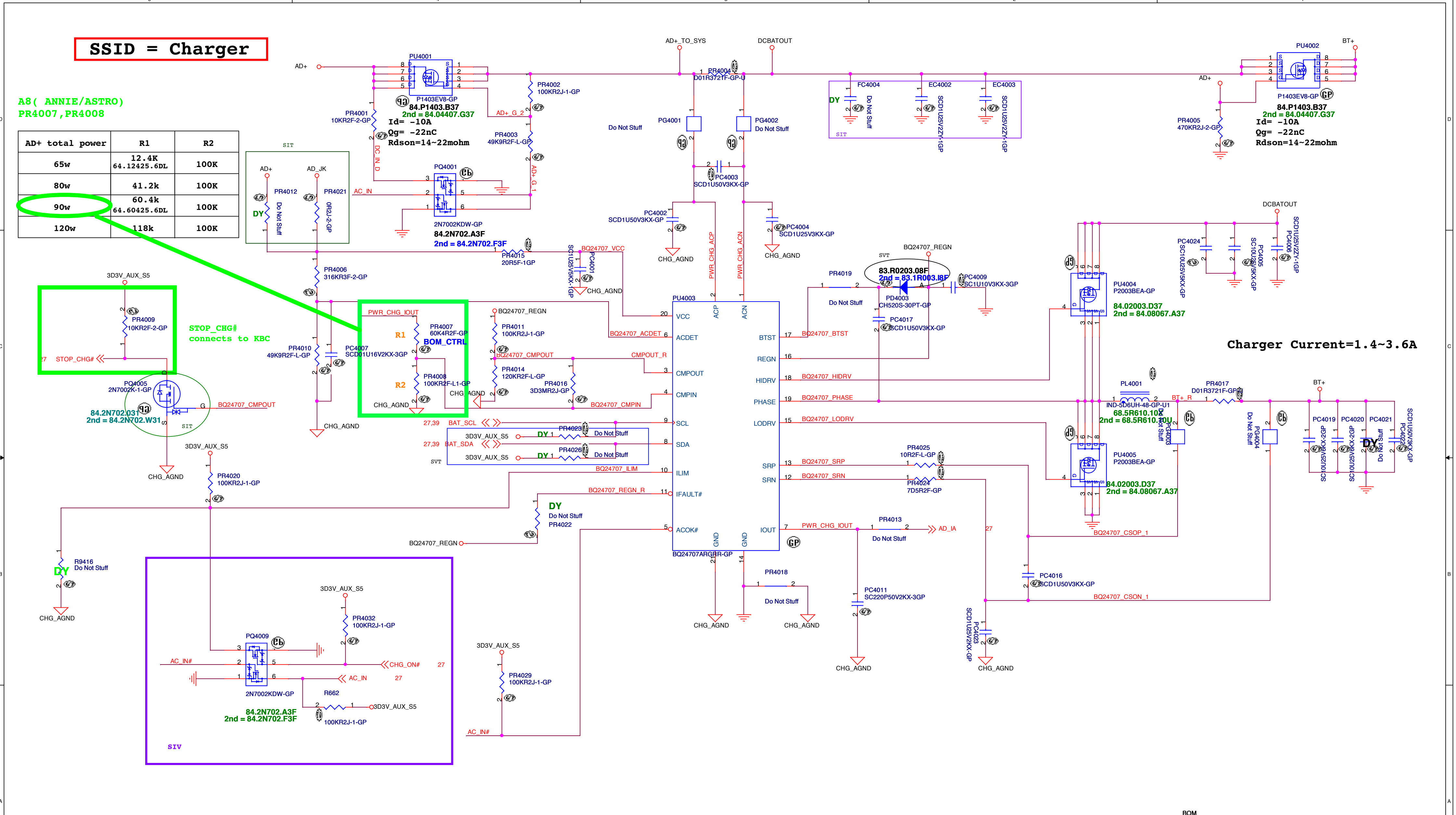
SSID = Charger

A8(ANNIE/ASTRO)
PR4007,PR4008

AD+ total power	R1	R2
65w	12.4K 64.12425.6DL	100K
80w	41.2k	100K
90w	60.4k 64.60425.6DL	100K
120w	118k	100K

STOP_CHG#
connects to KBC



Charger Current=1.4~3.6A

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Taipei Hsien 221, Taiwan, R.O.C.

Title	BQ24745_Charger	
Size	Document Number: LG4858_UMA	Rev -1
Date: Friday, March 16, 2012	Sheet 40 of 103	

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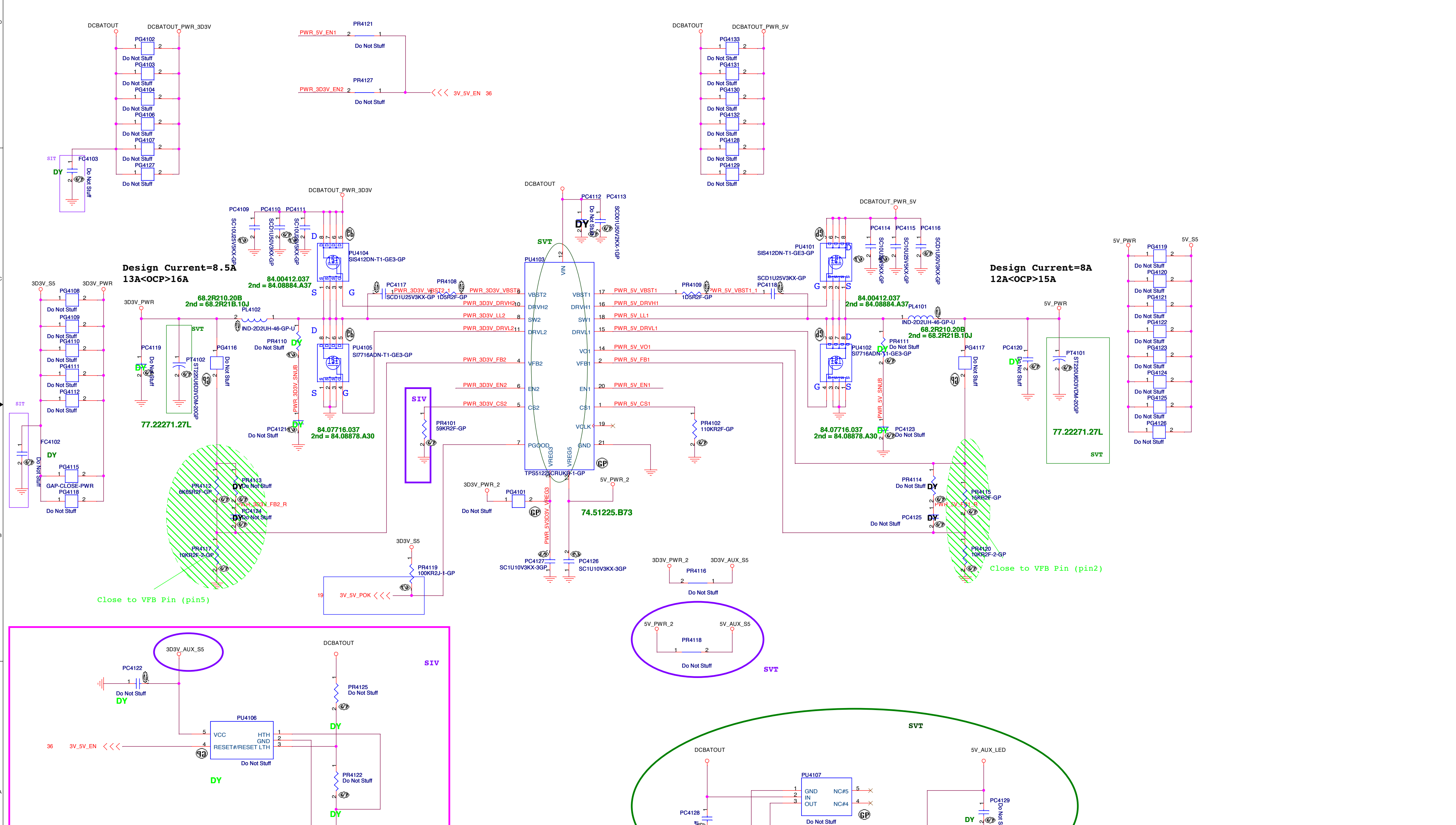
SSID = PWR.Plane.Regulator_5v3p3v



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	TPS51123_5V_3D3V	
Size	Document Number: LG4858_UMA	Rev: -1
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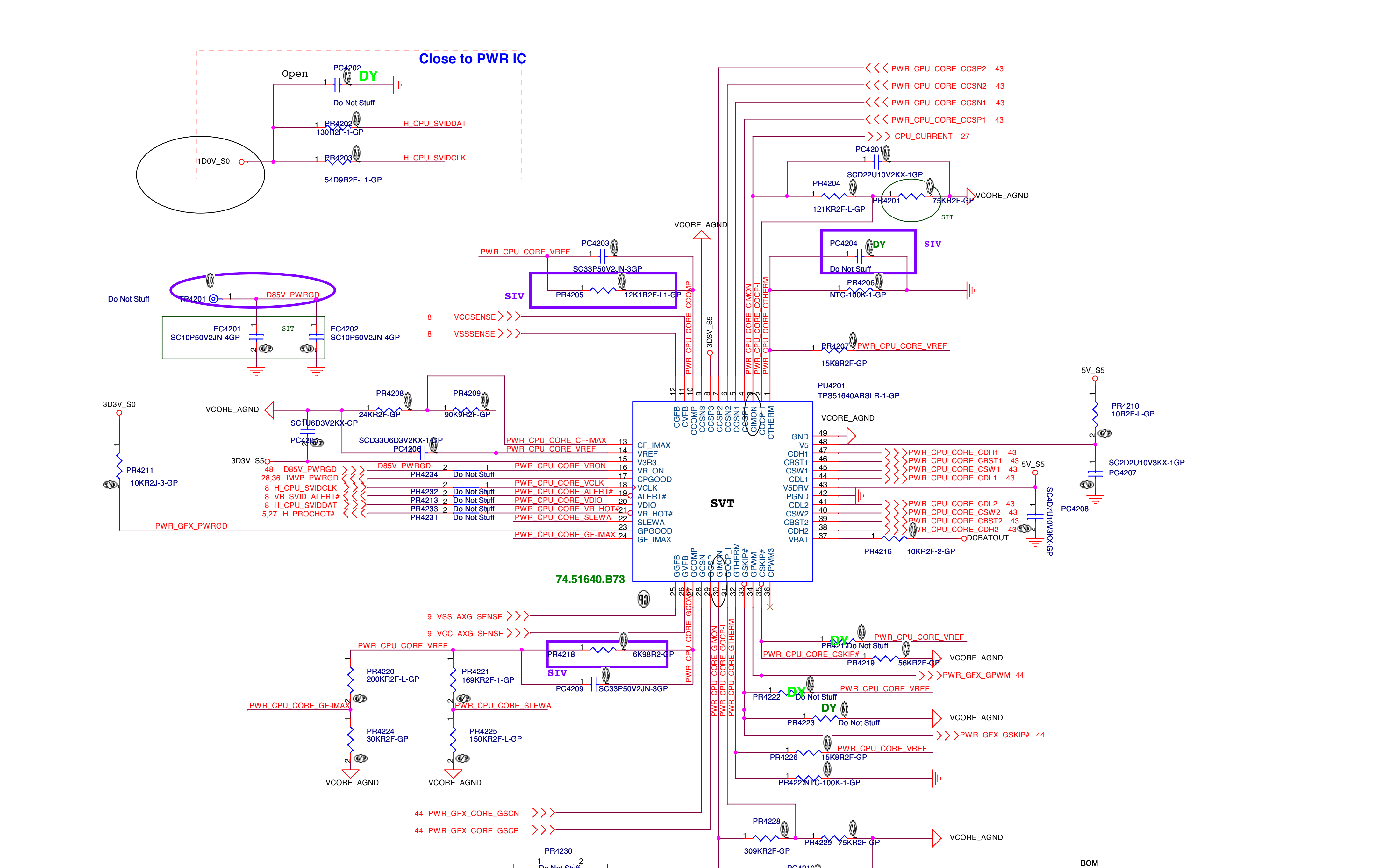

BOM

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Title	ISL95836_CPU_CORE(1/3)	
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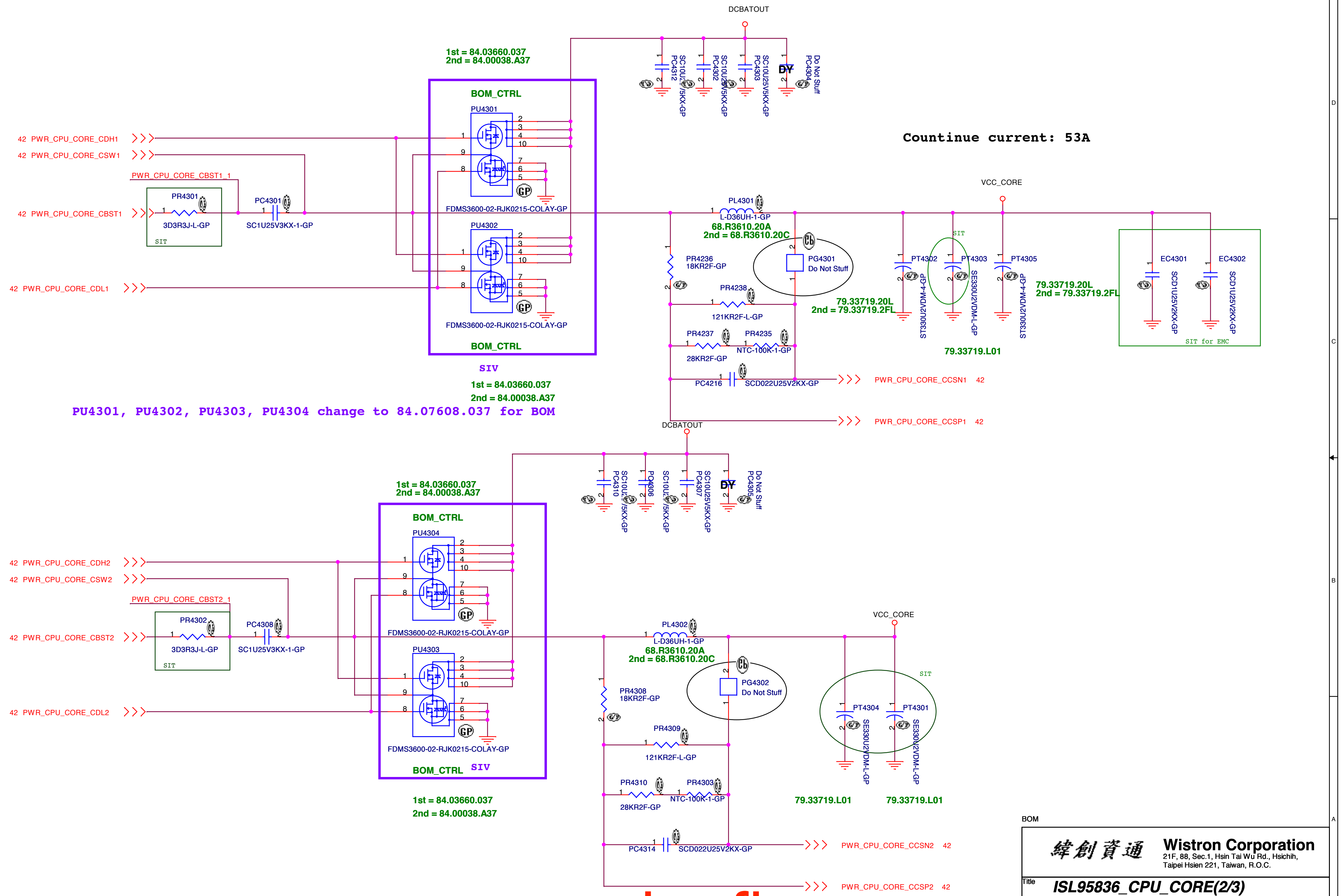

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Title	ISL95836_CPU_CORE(2/3)
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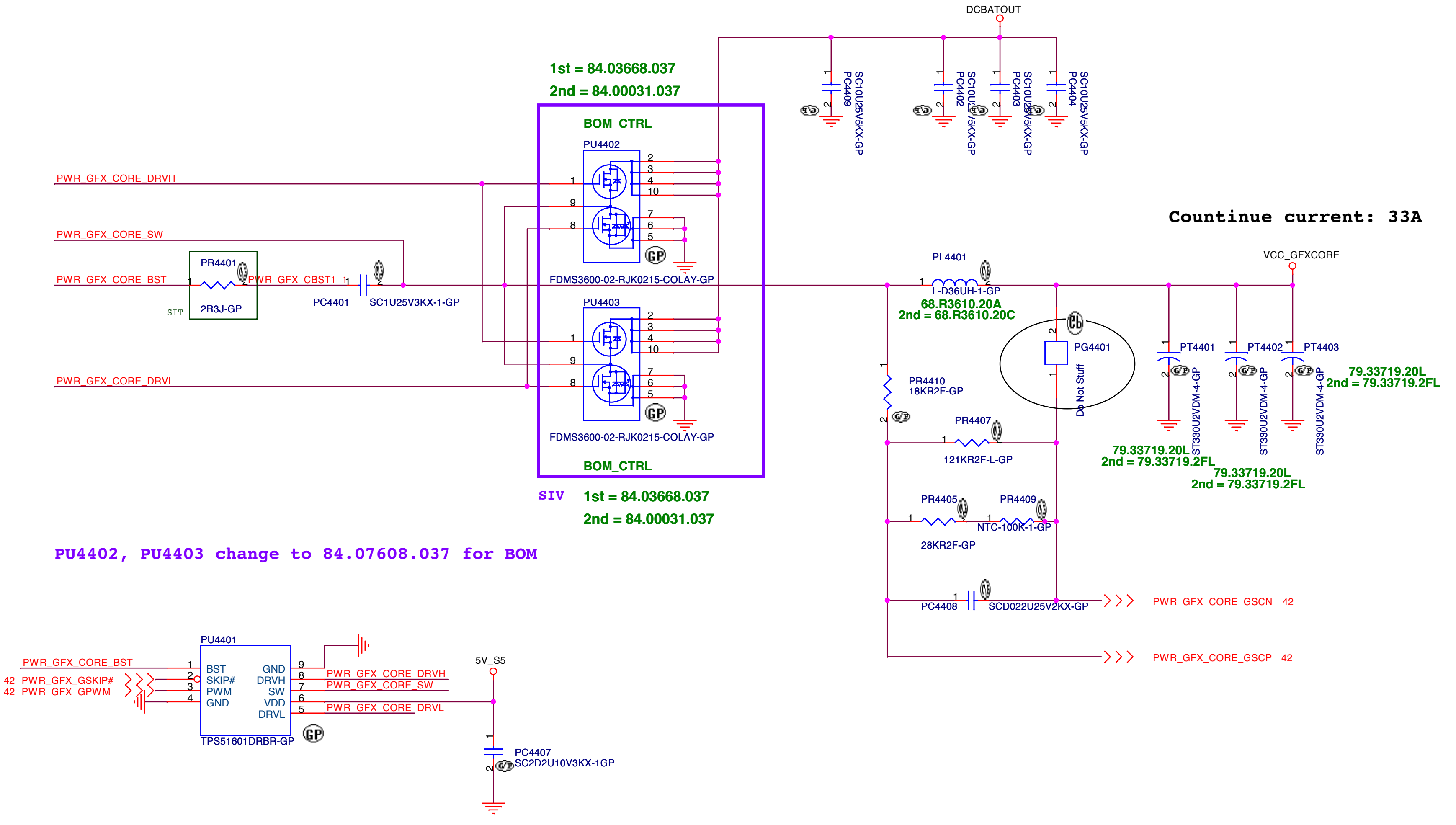

BOM

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Title	ISL95836_CPU_CORE(3/3)
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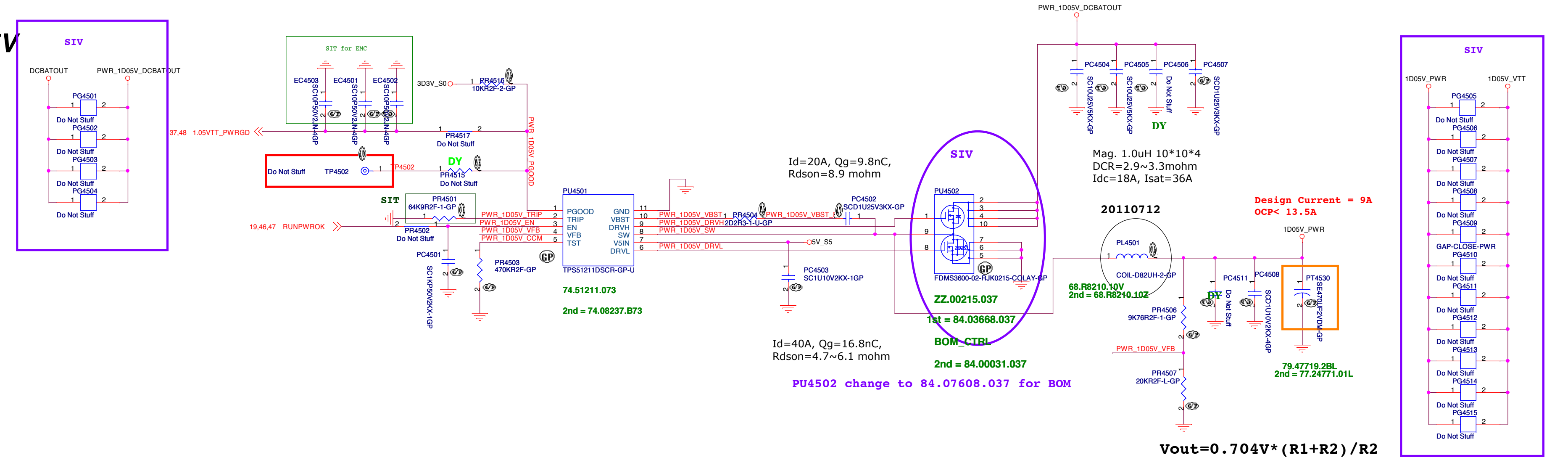
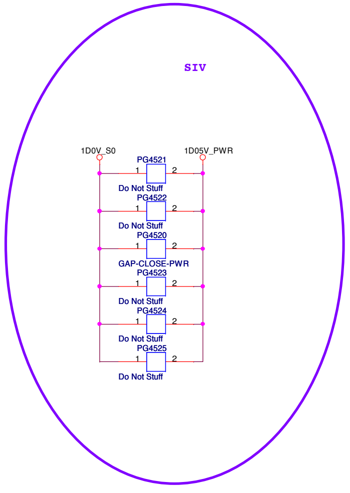
TPS51211 for 1D05V



APL5916 for 1D0V



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Title	TPS51211_1D05V&TPS51219_1D0V
Size / Document Number	LG4858_UMA
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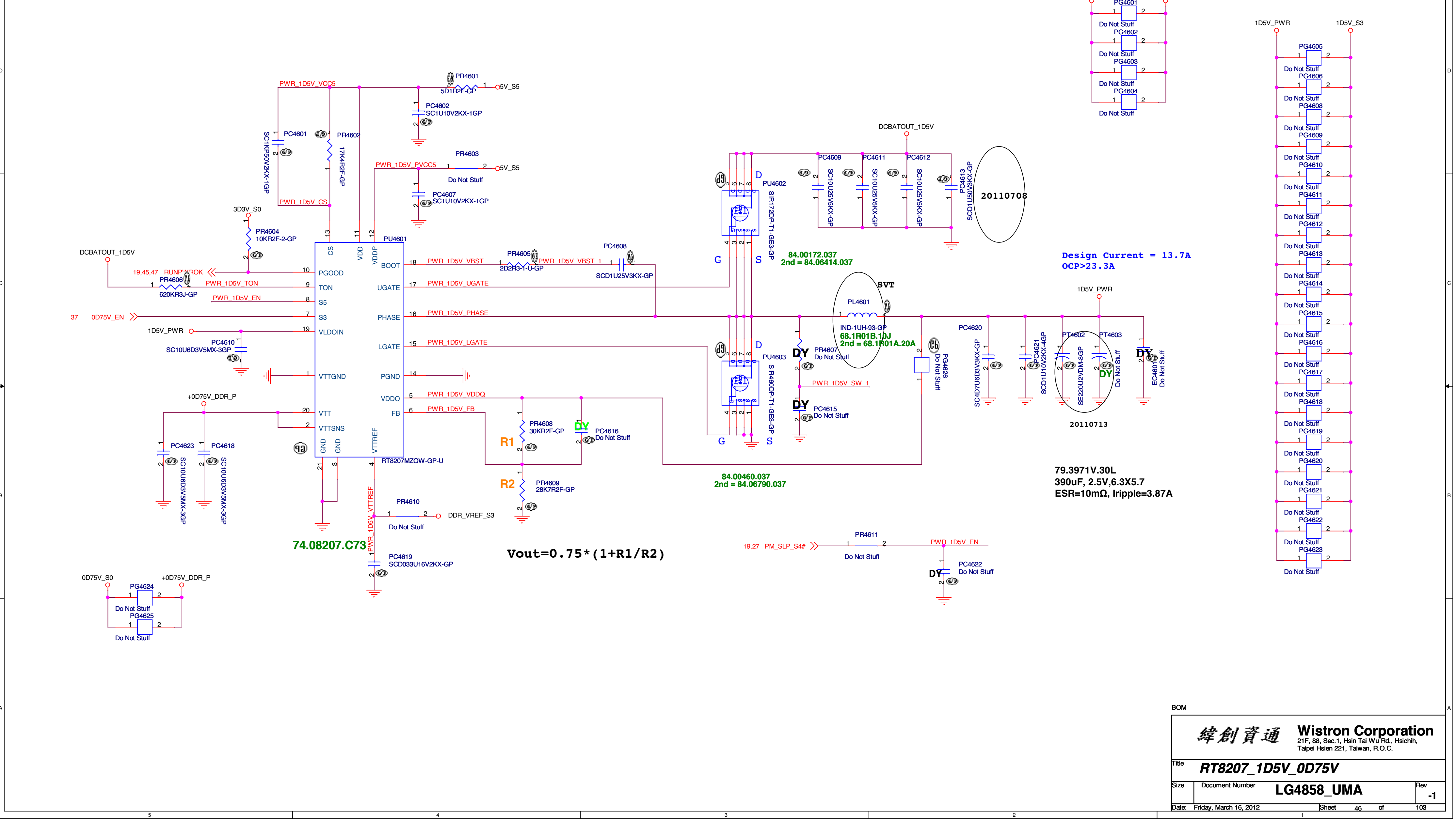
SSID = PWR.Plane.Regulator_1p5v0p75v



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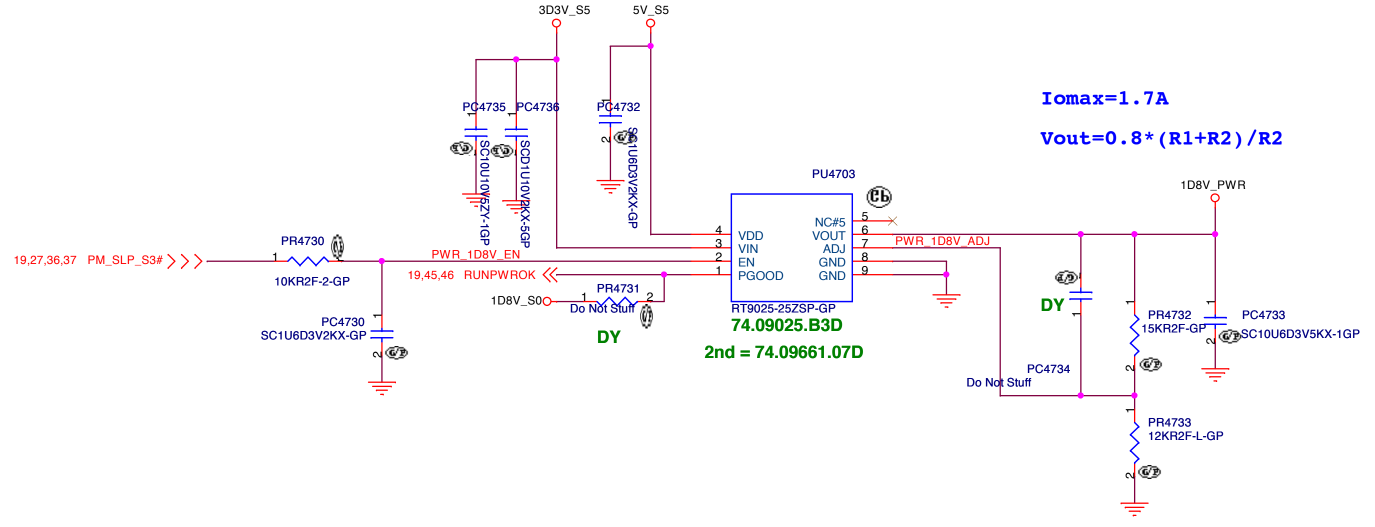
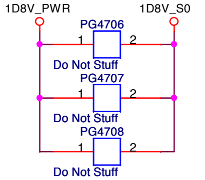
RT9025 for 1D8V_S0



Iomax=1.7A

Vout=0.8*(R1+R2)/R2



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Title	RT9205_1D8V
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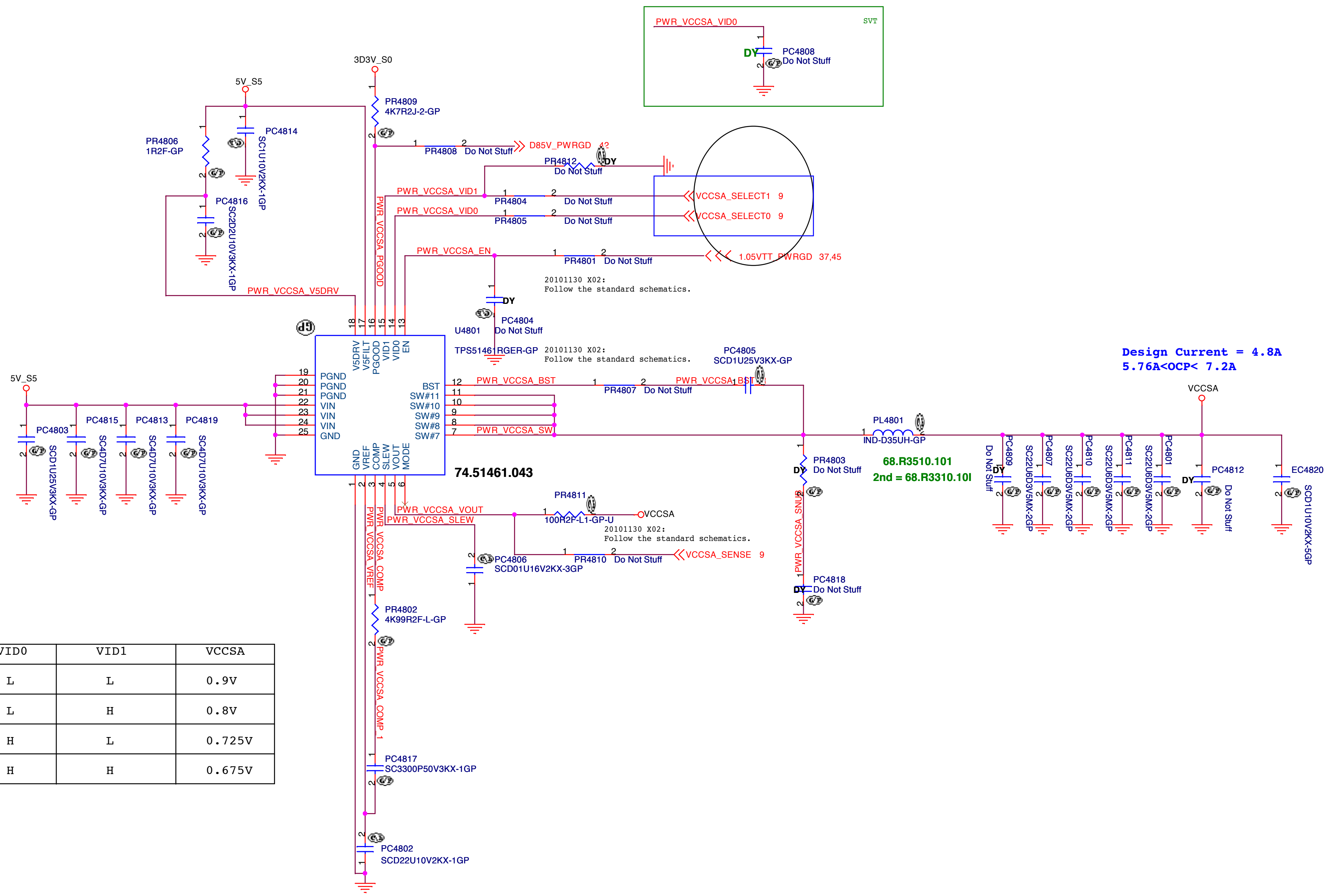
TPS51461 for VCCSA



VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

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Title	VCCSA_TPS51461		
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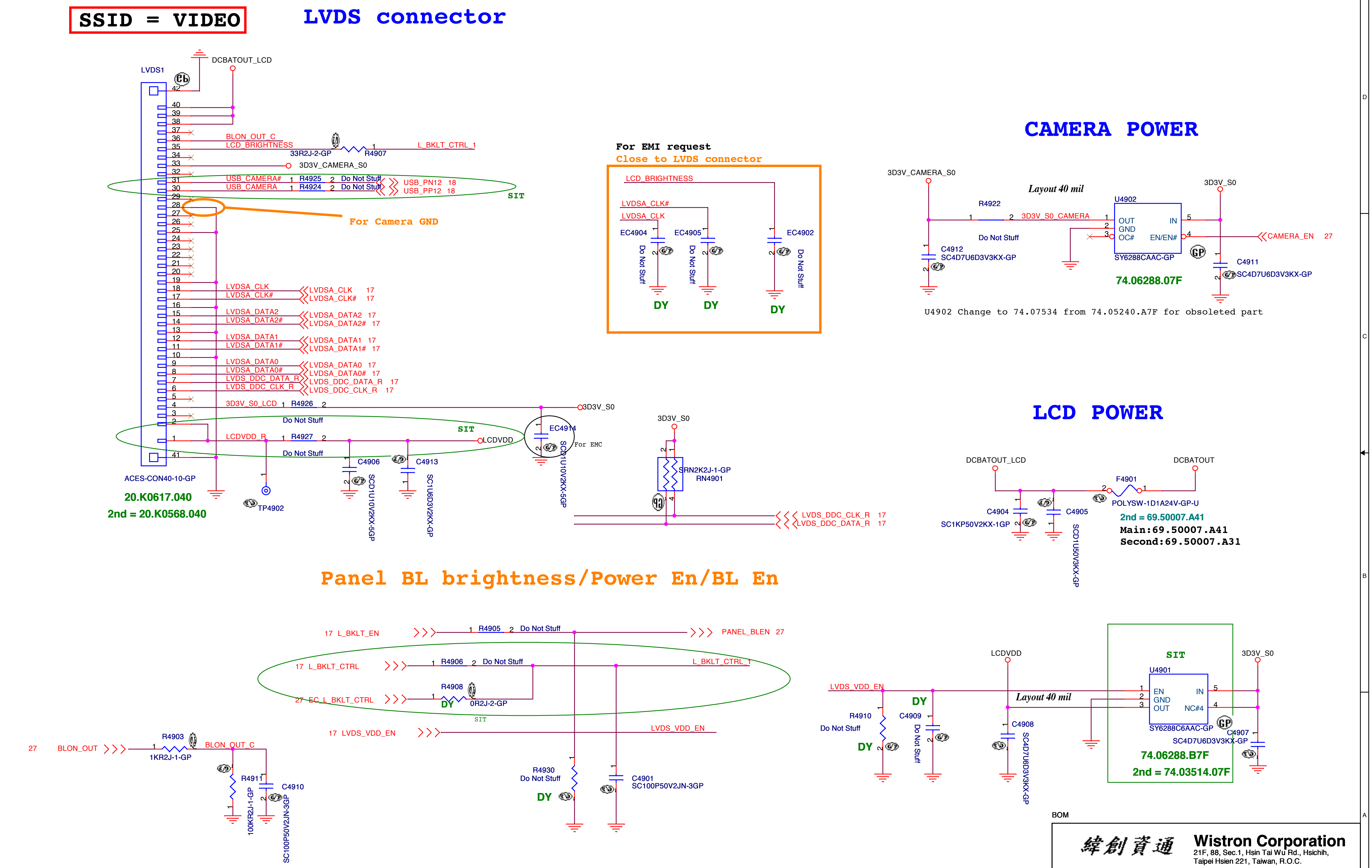

BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	LCD/Inverter Connector	
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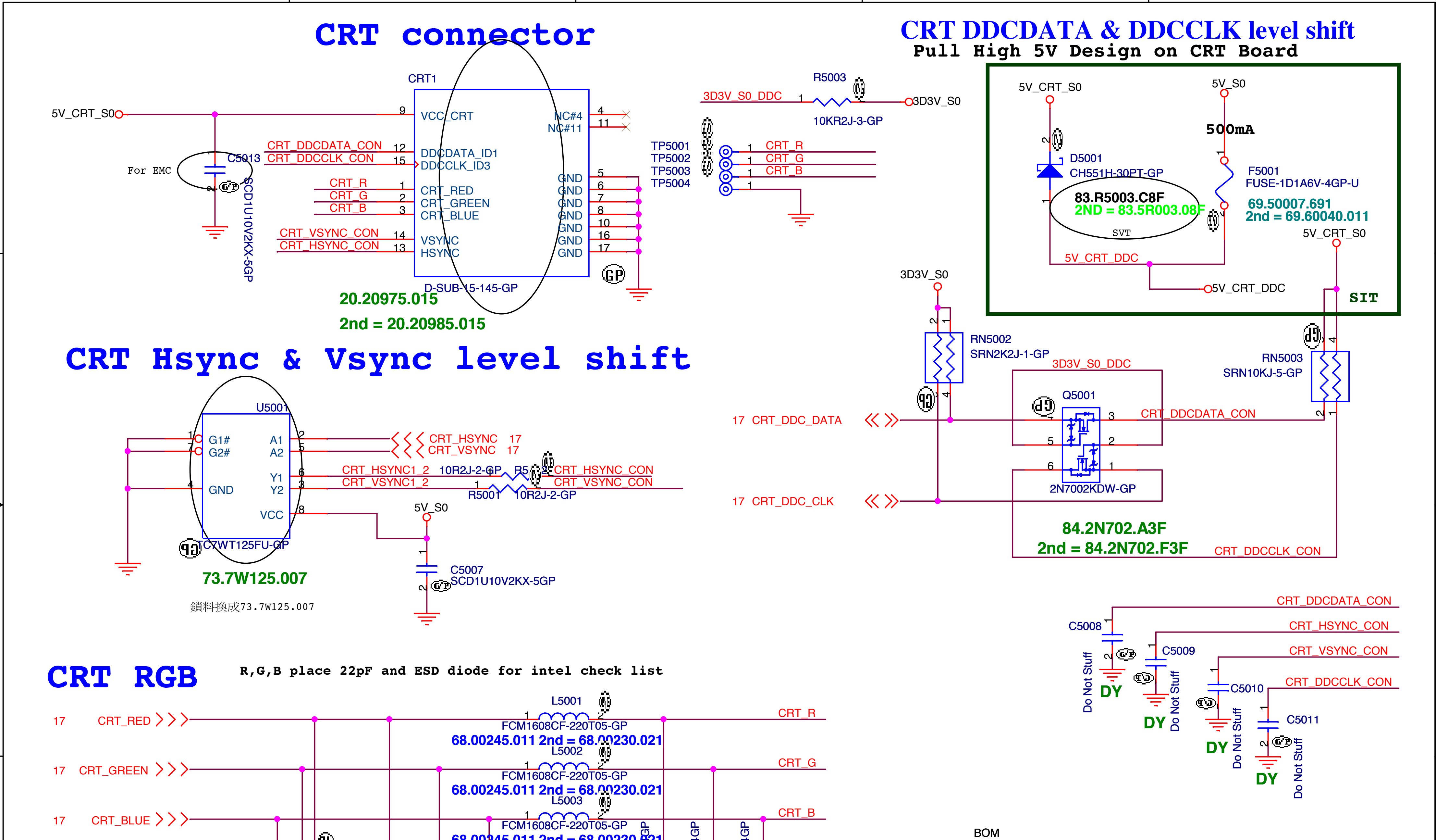

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CRT Board Connector		
Size	Document Number: LG4858_UMA		Rev: -1
Date: Friday, March 16, 2012		Sheet 50 of 103	

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SSID = VIDEO

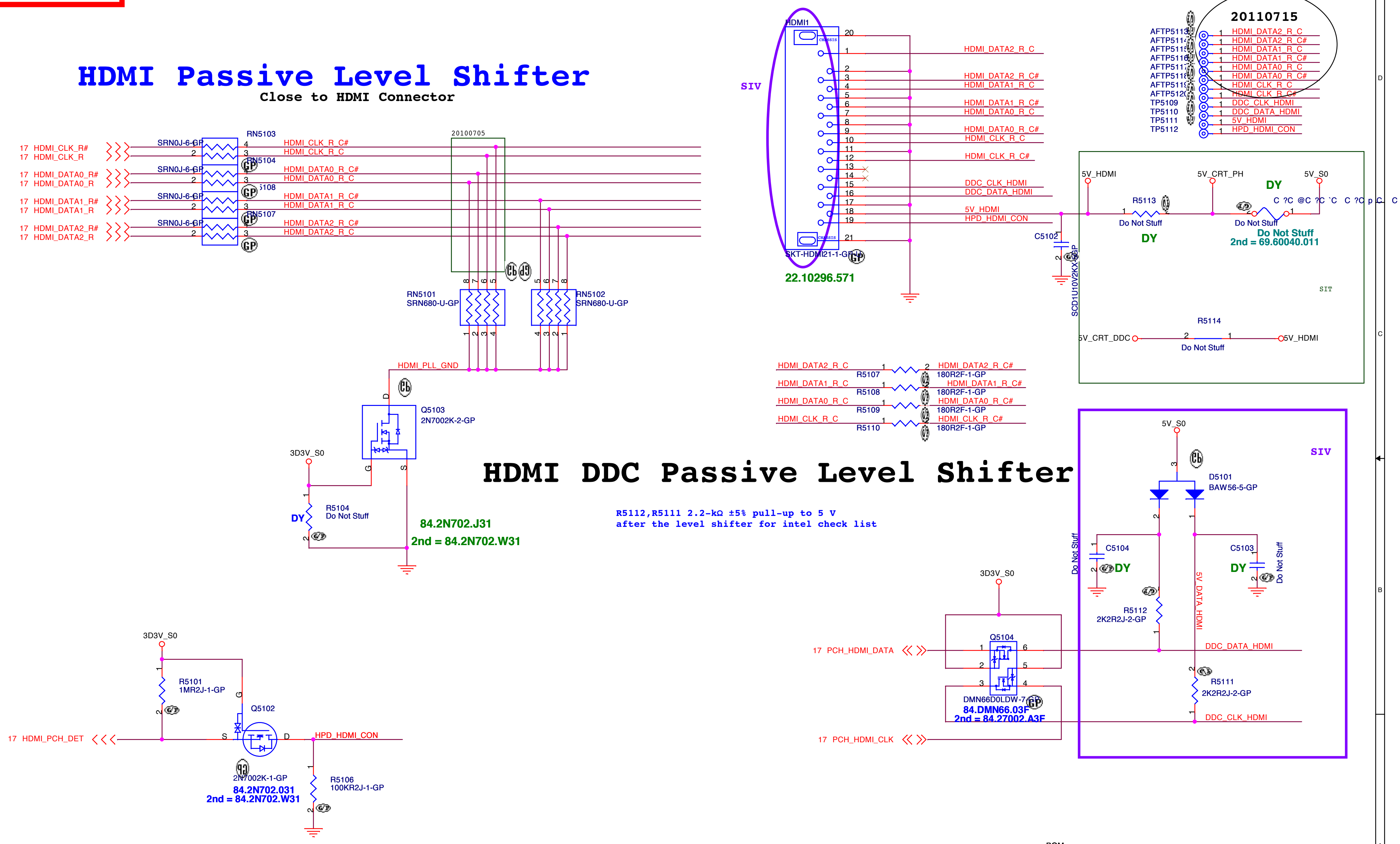
HDMI CONNECTOR

HDMI Passive Level Shifter

Close to HDMI Connector

HDMI DDC Passive Level Shifter

R5112,R5111 2.2-kΩ ±5% pull-up to 5 V after the level shifter for intel check list



BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	HDMI Level Shifter/Conn
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Date:	Friday, March 16, 2012
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緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.				
Title	(Reserved)Display Port				
Size	Document Number	LG4858_UMA			Rev -1
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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*(Reserved)S-Video*		
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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title	*(Reserved)DVI*			
Size	Document Number	LG4858_UMA	Rev	-1
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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*(Reserved)ITP*	
Size	Document Number **LG4858_UMA**	Rev **-1**
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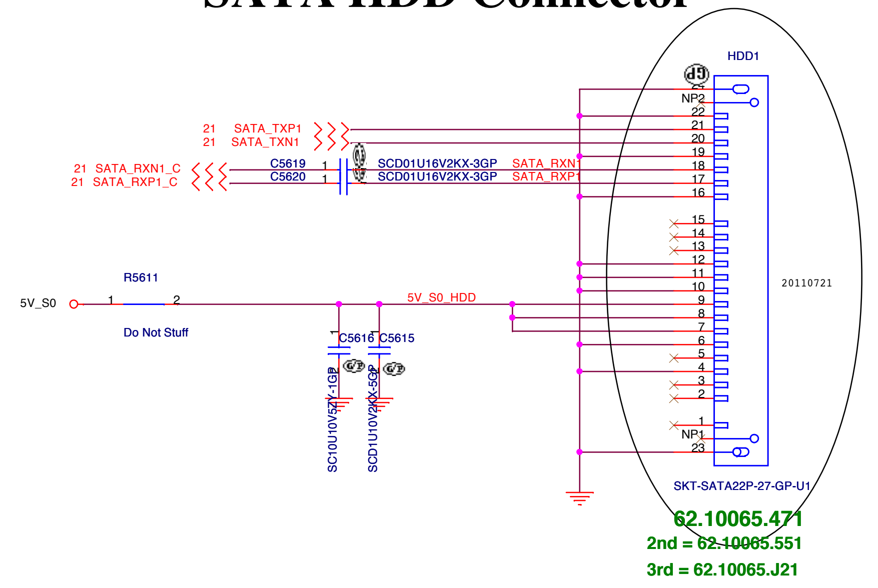
SSID = SATA

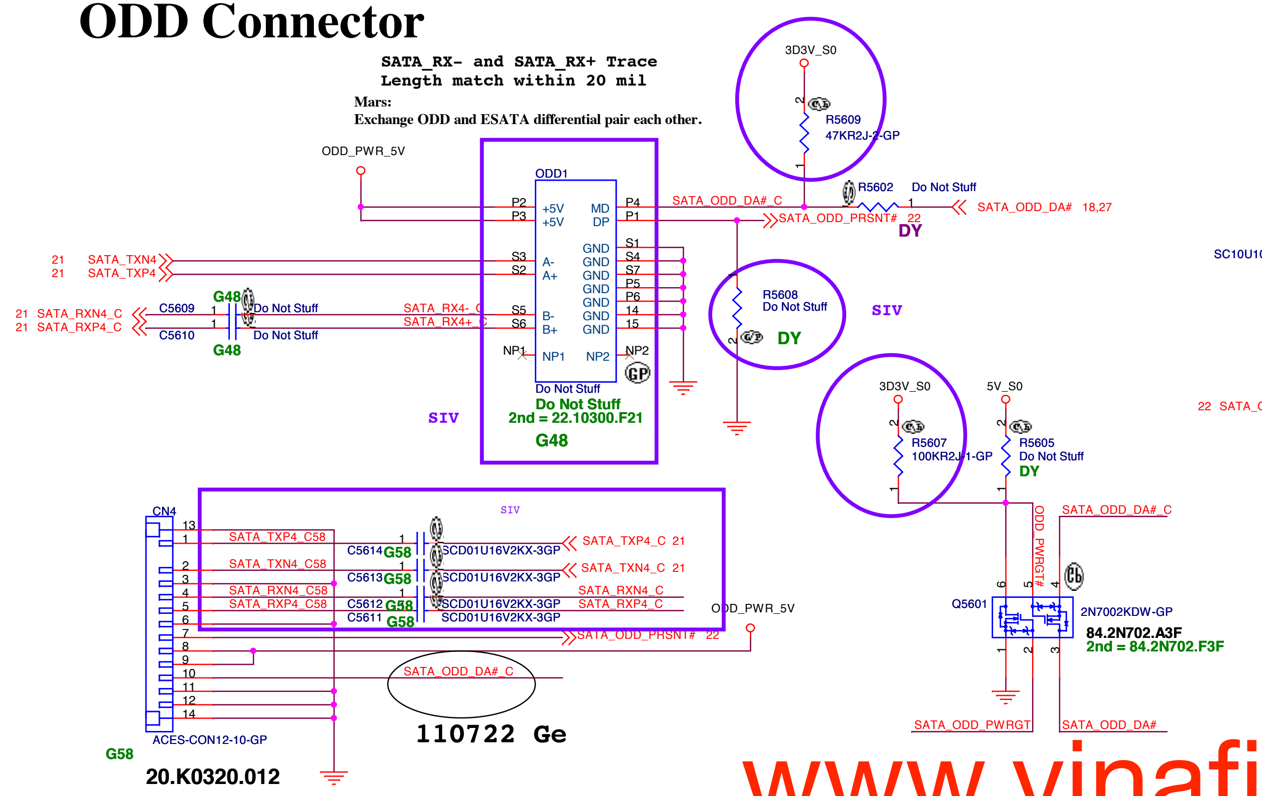
SATA HDD Connector



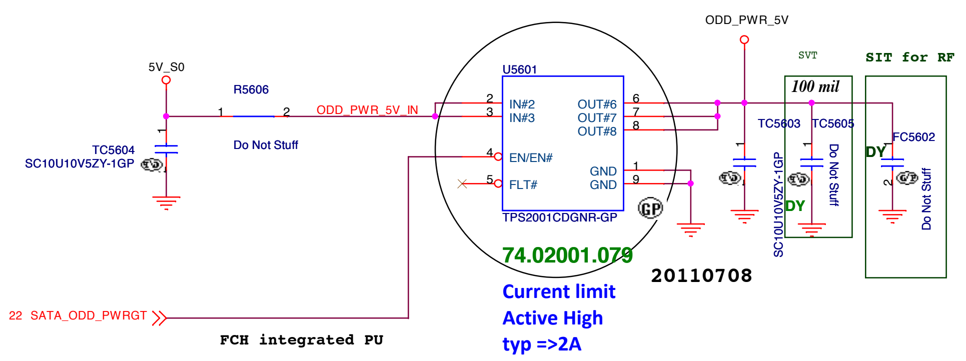
ODD Connector

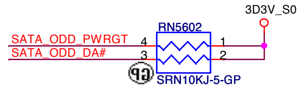
SATA_RX- and SATA_RX+ Trace Length match within 20 mil

Mars:
Exchange ODD and ESATA differential pair each other.



SATA Zero Power ODD





SUPPORT ZERO SATA ODD

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	HDD/ODD	
Size	Document Number: LG4858_UMA	Rev: -1
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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***(Reserved)E-SATA***	
Size	Document Number **LG4858_UMA**	Rev **-1**
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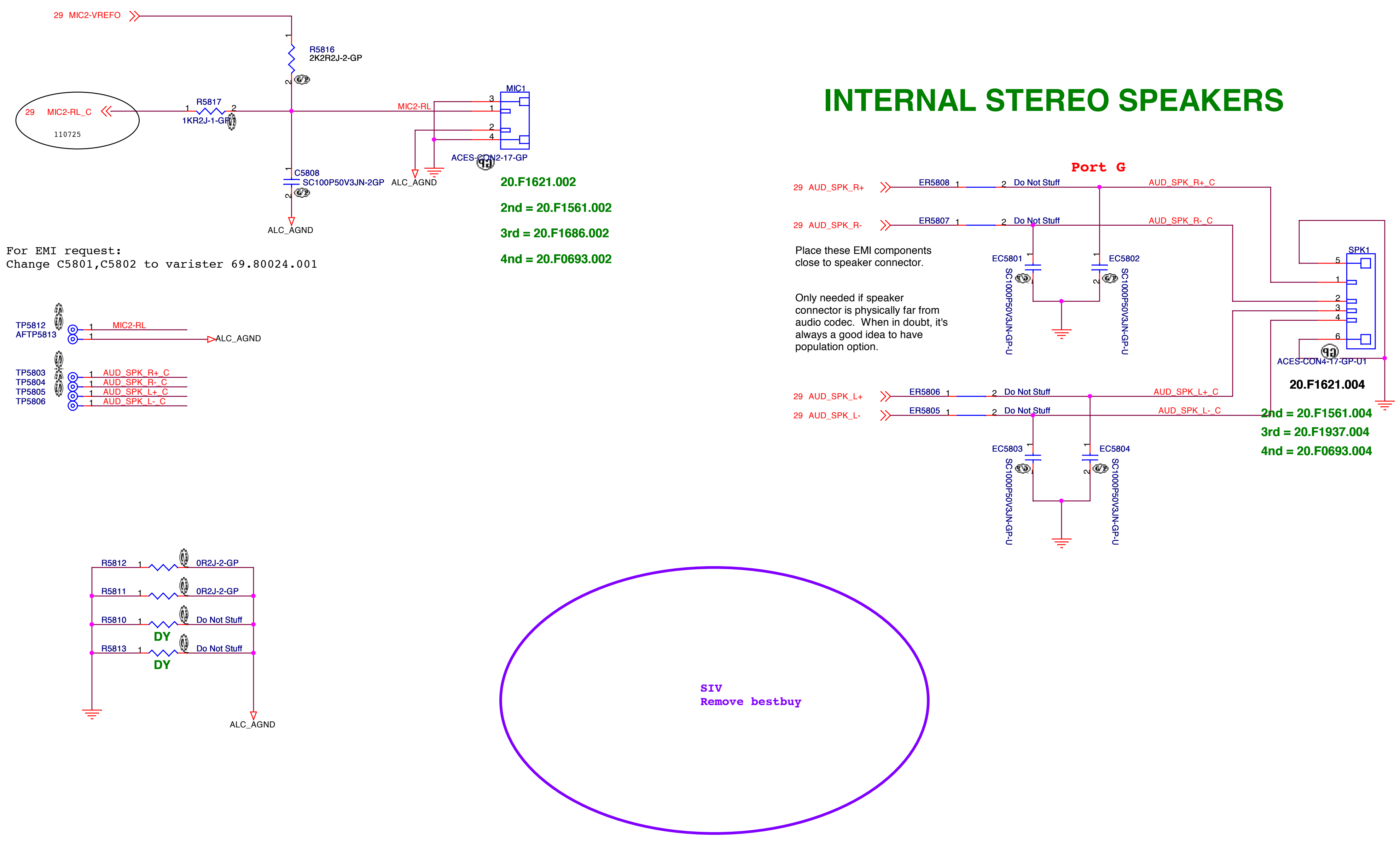
Analog Internal Mic

INTERNAL STEREO SPEAKERS



BOM	
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	MIC/SPEAKER/AUDIO JACK
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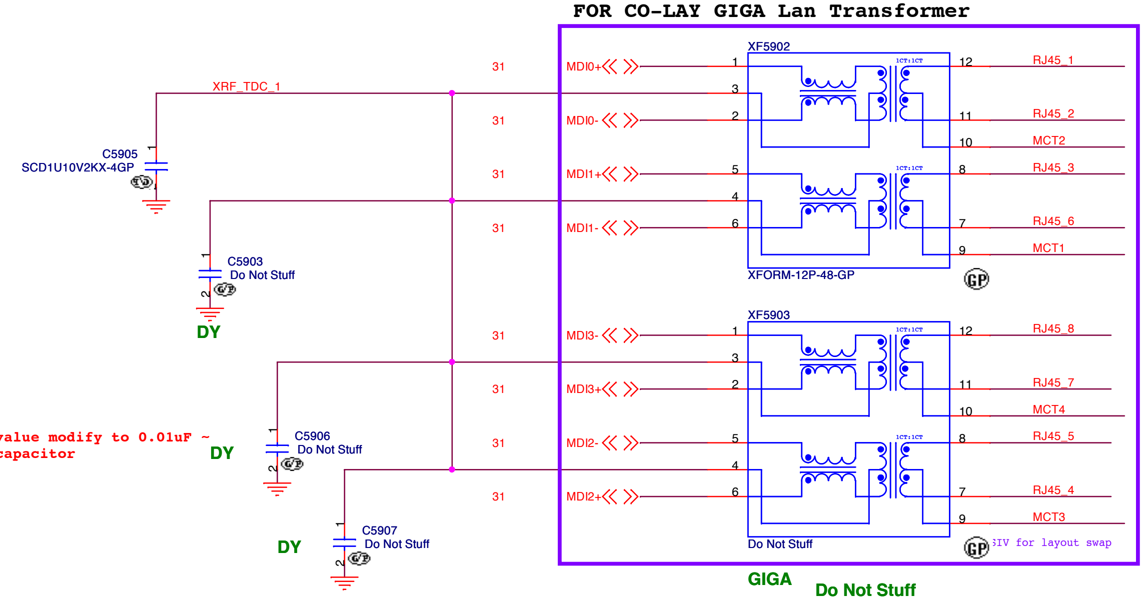
10/100M Lan Transformer

FOR CO-LAY GIGA Lan Transformer



C5903 value modify to 0.01uF ~ 0.4uF capacitor

68.68167.30D

2nd = 68.0NS14.301

3rd = 68.HD081.30B

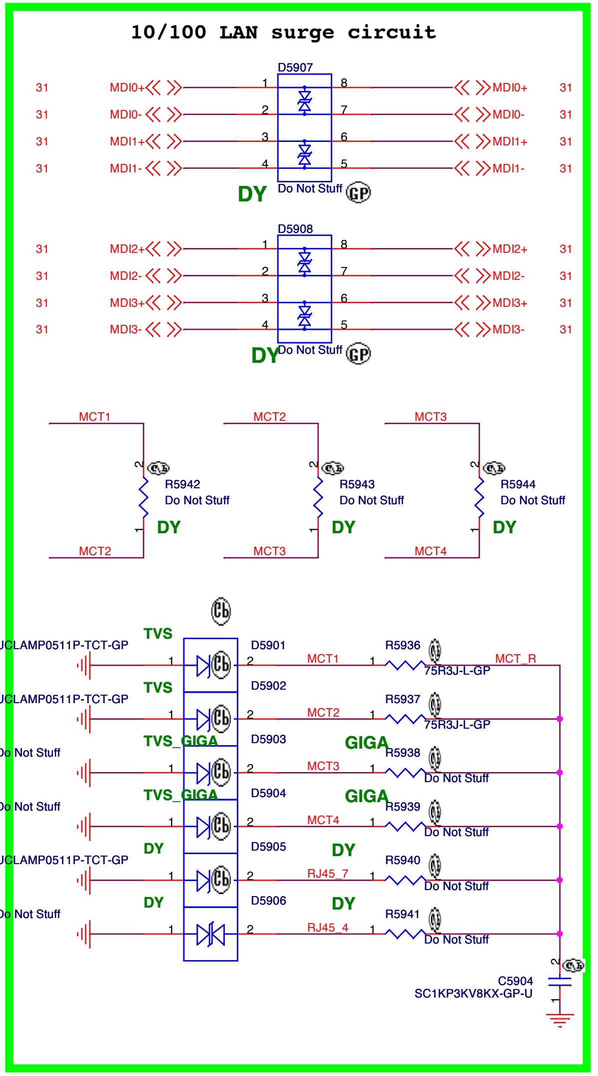
Do Not Stuff

2nd = 68.0NS14.301

3rd = 68.HD081.30B

1. route as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width,12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat,except RJ-45 moat.

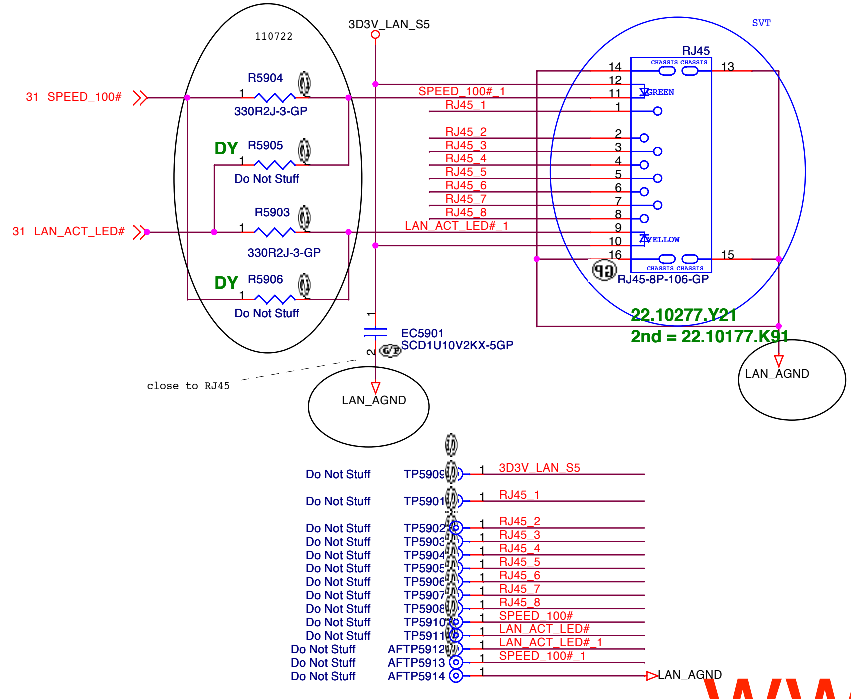
10/100 LAN surge circuit

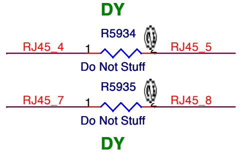


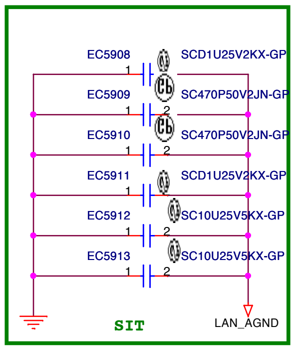
For AR8162(10/100M): C5906, C5907,R5938, R5939 can be DY.

For AR8161(GIGA): Dummy R5934, R5935, R5940,R5941

LAN Connector







BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	RJ45		
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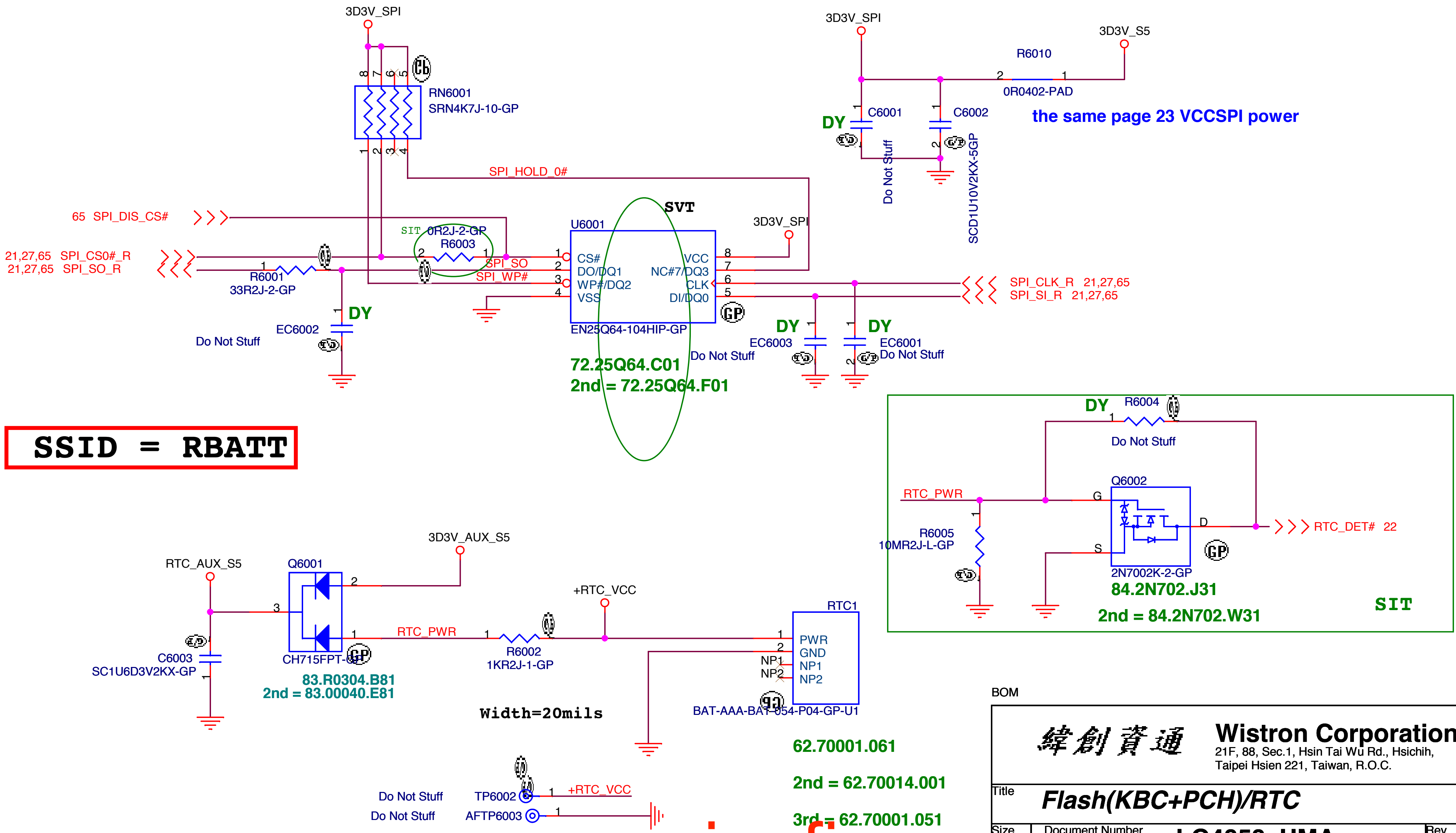
SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH

SSID = RBATT



BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*Flash(KBC+PCH)/RTC*
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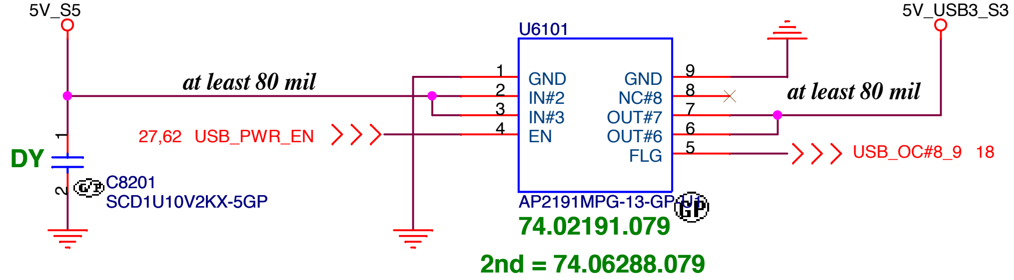
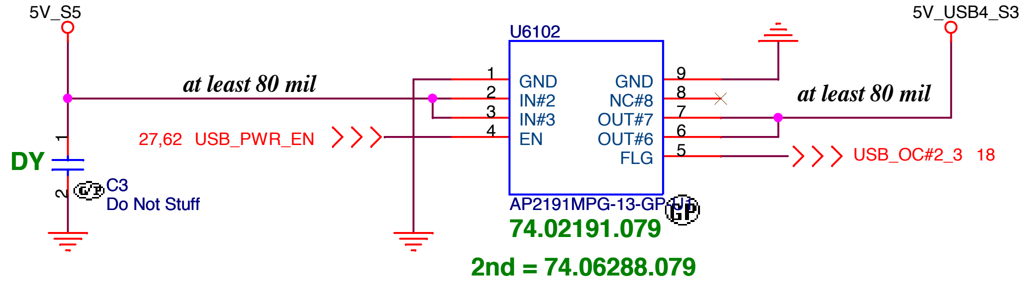
SSID = USB

USB Ext. port3 power SW



U6101 place near to USBCN3

USB Ext. port4 power SW



U6102 place near to CDRCN2

BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***USB2.0 Port Power SW***
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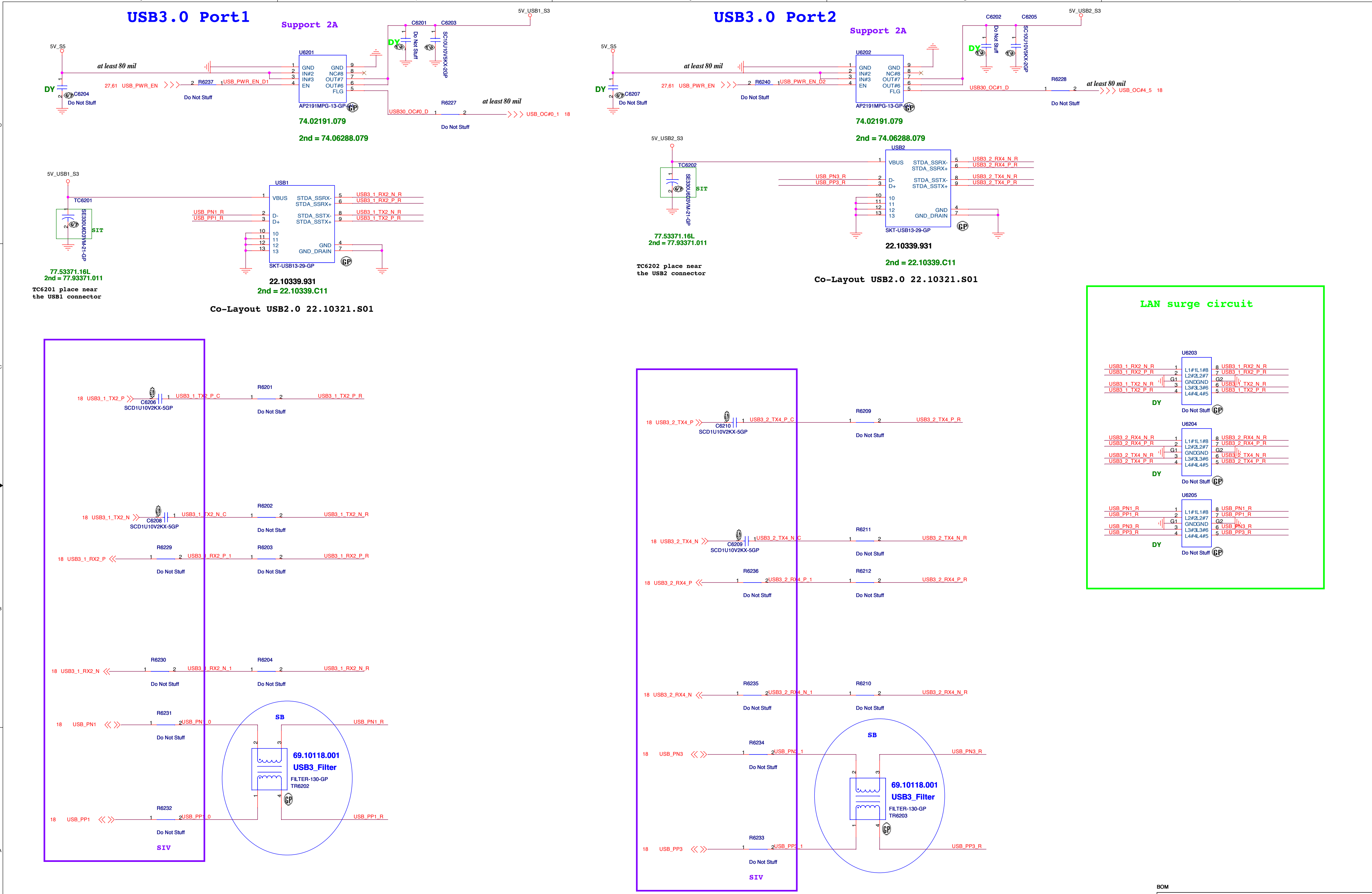

BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	USB3.0 Port1/2		
Size	Document Number	LG4858_UMA	Rev -1
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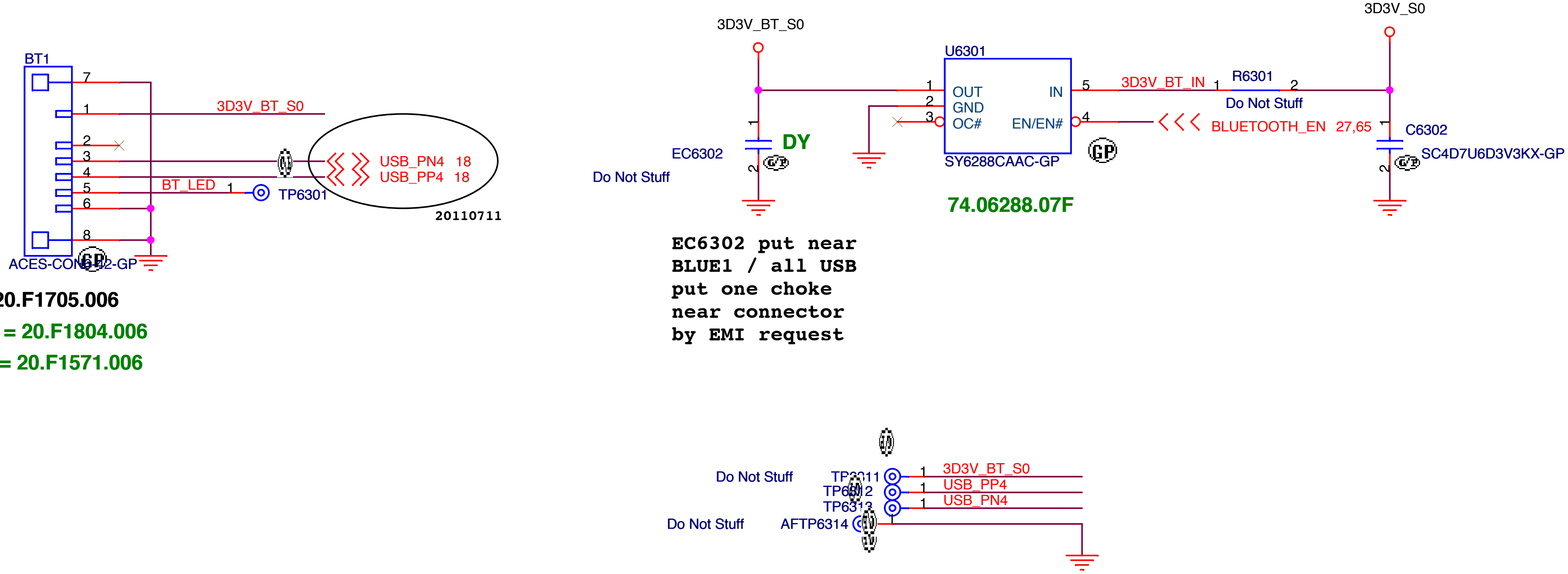
SSID = User.Interface

Bluetooth conn.



BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**BLUETOOTH**
Size / Document Number	LG4858_UMA
Rev	-1
Date:	Friday, March 16, 2012
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Title	***(Reserved)Finger Print Con.***
Size	Document Number **LG4858_UMA**
Rev	**-1**
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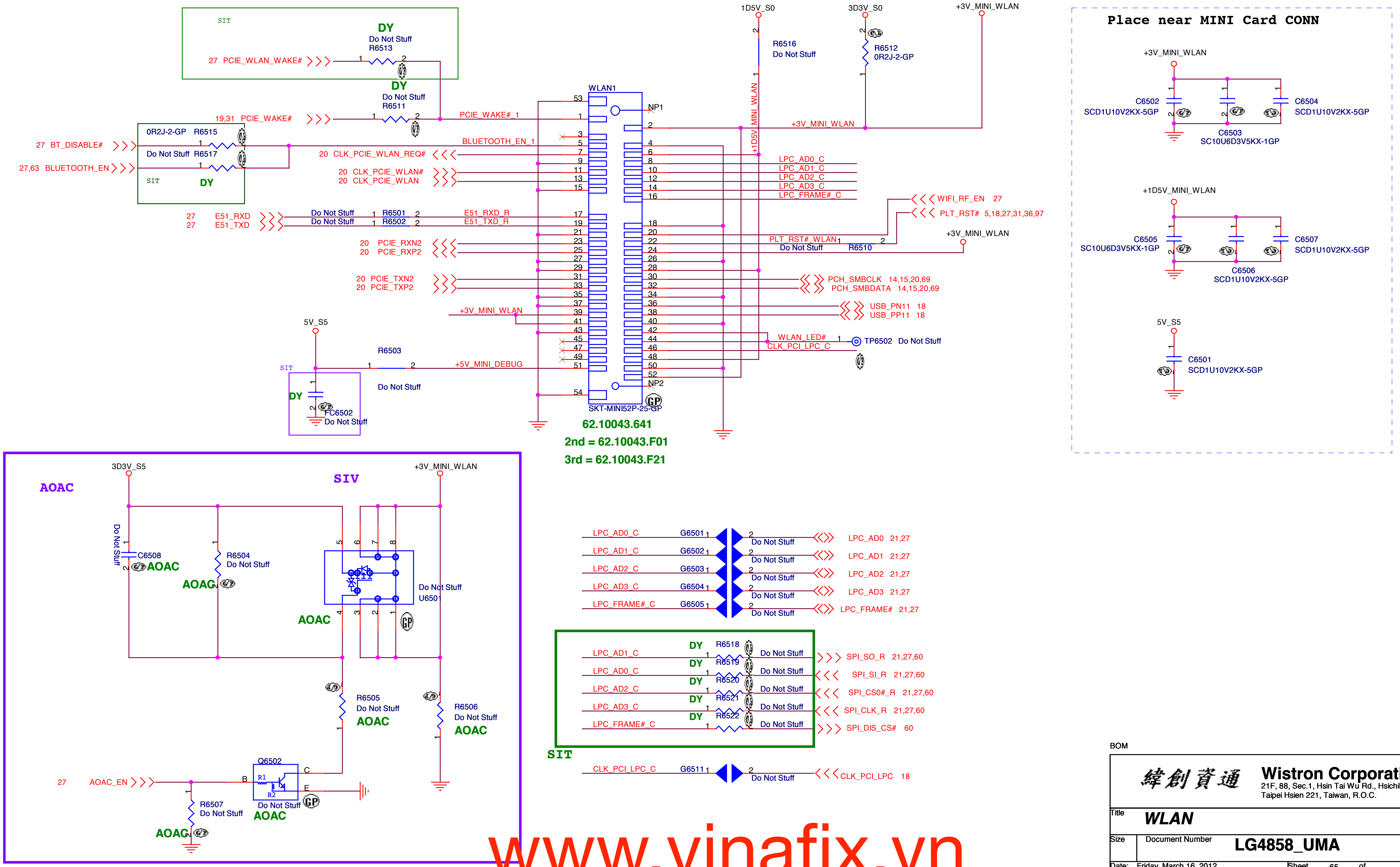
SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	WLAN		
Size	Document Number	LG4858_UMA	Rev -1
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SSID = Wireless

Mini Card Connector(WWAN)

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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***(Reserved)WWAN CONN***
Size / Document Number	**LG4858_UMA** Rev **-1**
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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***(Reserved)3rd MINICARD***		
Size	Document Number **LG4858_UMA**		Rev **-1**
Date: Friday, March 16, 2012	Sheet 67	of	103

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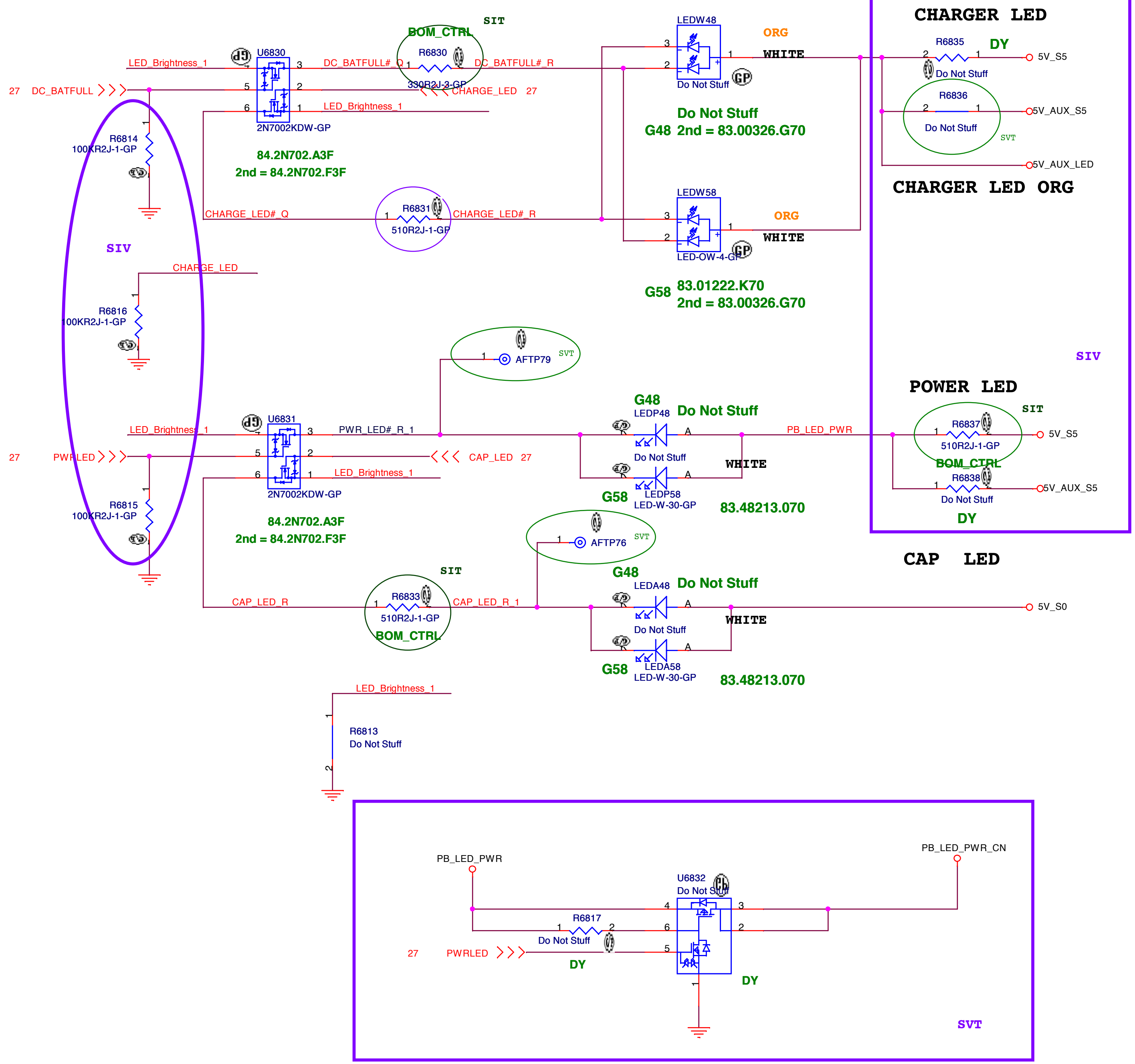
SSID = User.Interface

20110715



BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LED/Power Button/key		
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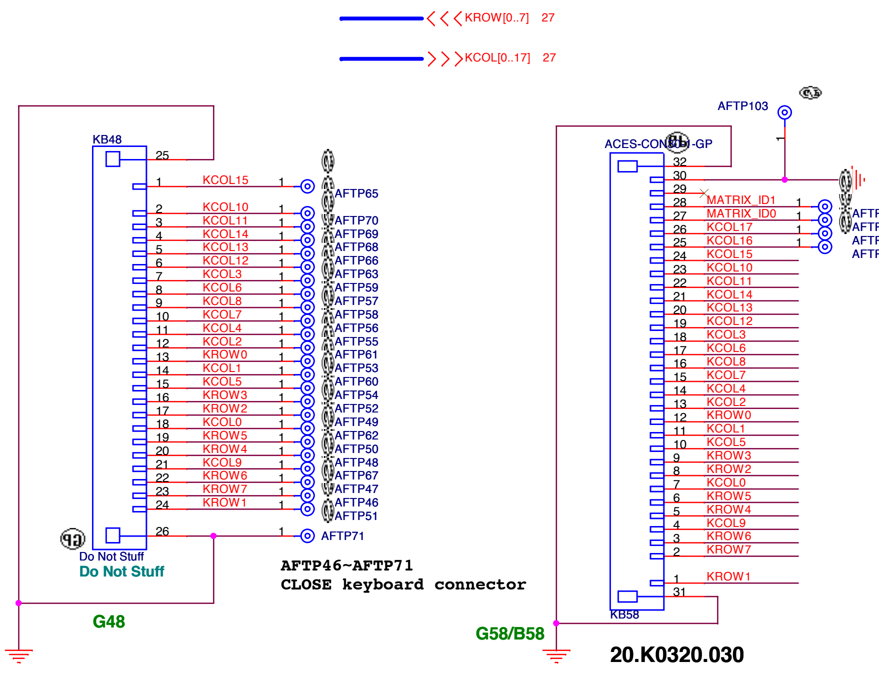
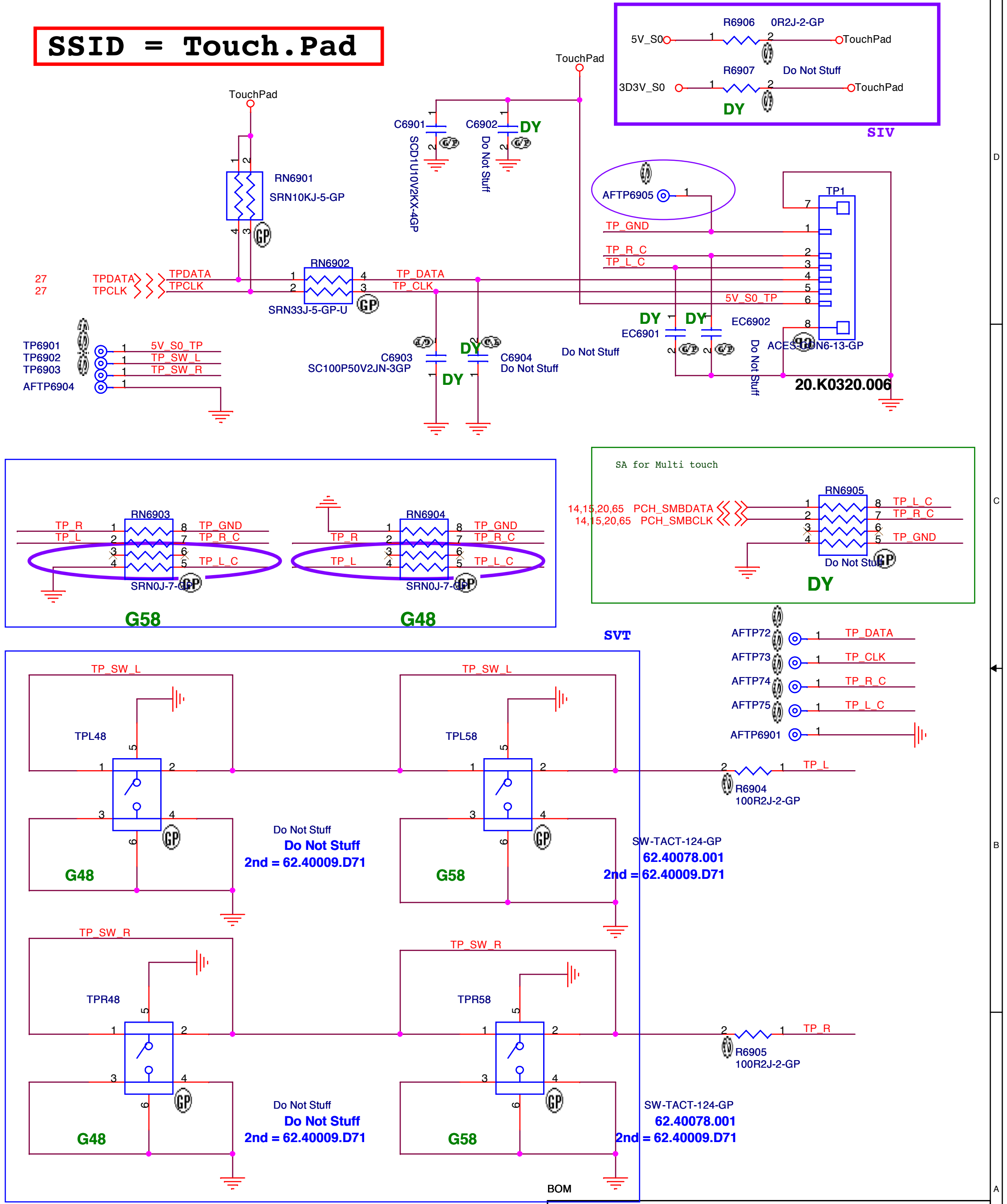
SSID = KBC

KB1 Follow LA47

Internal KeyBoard Connector



SSID = Touch.Pad



14"

* Membrane Pin Out Top View :

PIN #	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	12	1	8	9	5	6	3	2
As-sign	D 1	D 2	D 3	D 4	D 5	D 6	D 7	D 8	D 9	D 10	D 11	D 12	D 13	D 14	D 15	D 16	S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8

15"

* Membrane Pin Out Top View :

PIN #	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	25	26	12	1	8	9	5	6	3	2
As-sign	D 1	D 2	D 3	D 4	D 5	D 6	D 7	D 8	D 9	D 10	D 11	D 12	D 13	D 14	D 15	D 16	D 17	D 18	S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	Key Board/Touch Pad
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緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Hall Sensor	
Size	Document Number: LG4858_UMA	Rev: -1
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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*(Reserved)Debug connector*		
Size	Document Number	LG4858_UMA	Rev -1
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緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title	(Reserved)RJ11+MDC
Size	
Document Number	LG4858_UMA
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緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***(Reserved)CARD Reader CONN***		
Size	Document Number	**LG4858_UMA**	Rev **-1**
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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***(Reserved)Express Card***	
Size	Document Number **LG4858_UMA**	Rev **-1**
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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*(Reserved)Smart Card Socket*	
Size	Document Number **LG4858_UMA**	Rev **-1**
Date: Friday, March 16, 2012	Sheet 76 of 103	

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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	***(Reserved)TPM***		
Size	Document Number	**LG4858_UMA**	Rev **-1**
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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*(Reserved)SIO*
Size	Document Number **LG4858_UMA** Rev **-1**
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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***(Reserved)G-Sensor***	
Size	Document Number **LG4858_UMA**	Rev **-1**
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Title	***(Reserved)RF/Other***		
Size	Document Number **LG4858_UMA**		Rev **-1**
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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	(Reserved)Screw Holes,SPR		
Size	Document Number	LG4858_UMA	Rev -1
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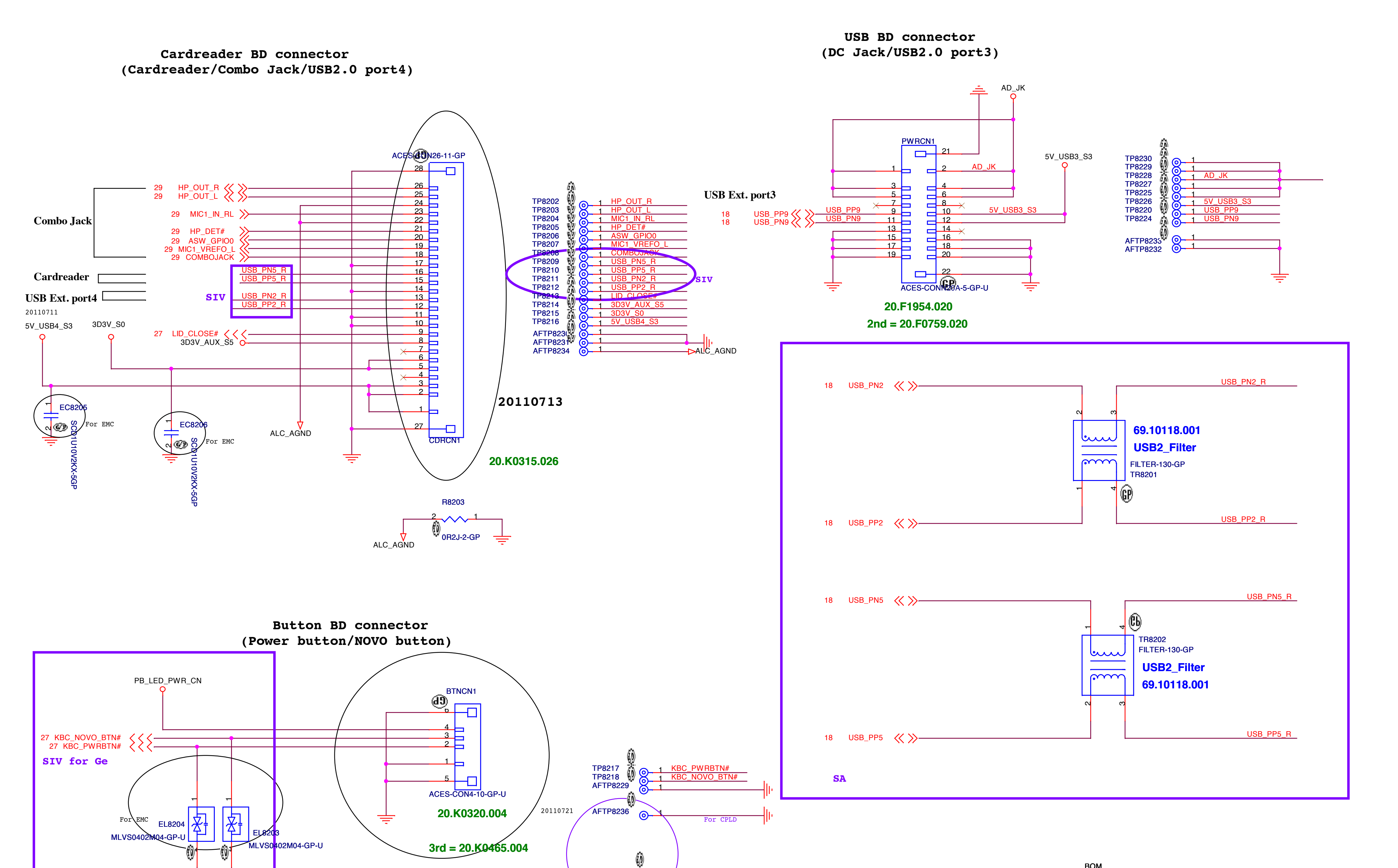

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	IO Board Connector	
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緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	GPU (1/5): PEG	
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	GPU (3/5): VRAM I/F	
Size	Document Number LG4858_UMA	Rev -1
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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	GPU (4/5): GPIO/STRAP	
Size	Document Number: LG4858_UMA	Rev: -1
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	GPU (5/5): PWR/GND	
Size	Document Number LG4858_UMA	Rev -1
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VIDEO FRAME BUFFER PORT A

BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	VRAM1,2 (1/4)		
Size	Document Number	LG4858_UMA	Rev -1
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VIDEO FRAME BUFFER PORT A

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	VRAM3,4 (2/4)		
Size	Document Number	LG4858_UMA	Rev -1
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BOM	VIDEO FRAME BUFFER PORT C
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	VRAM5,6 (3/4)
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VIDEO FRAME BUFFER PORT C

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Title	*(Reserved)Touch panel CONN*		
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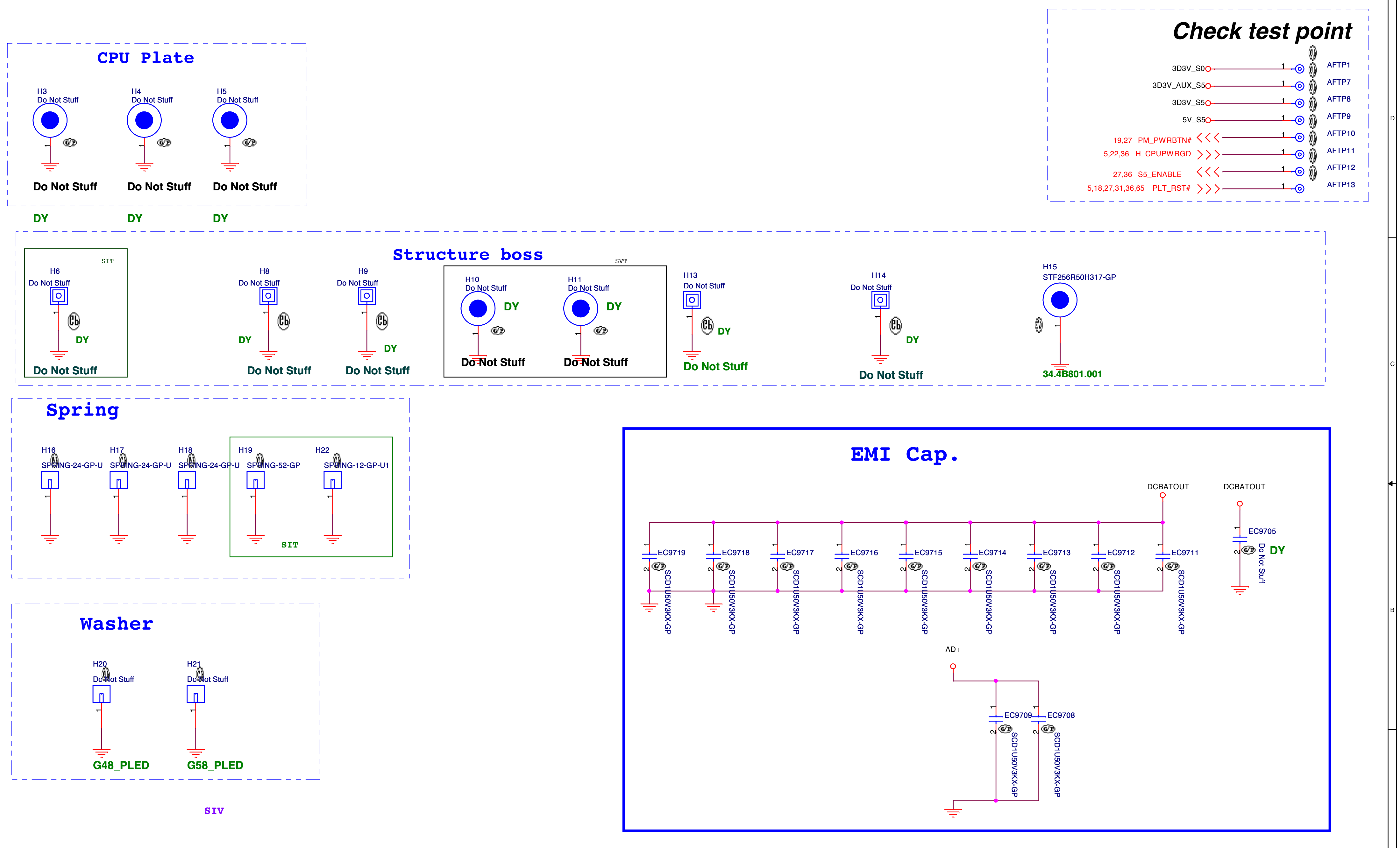

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Title	***Change-History***	
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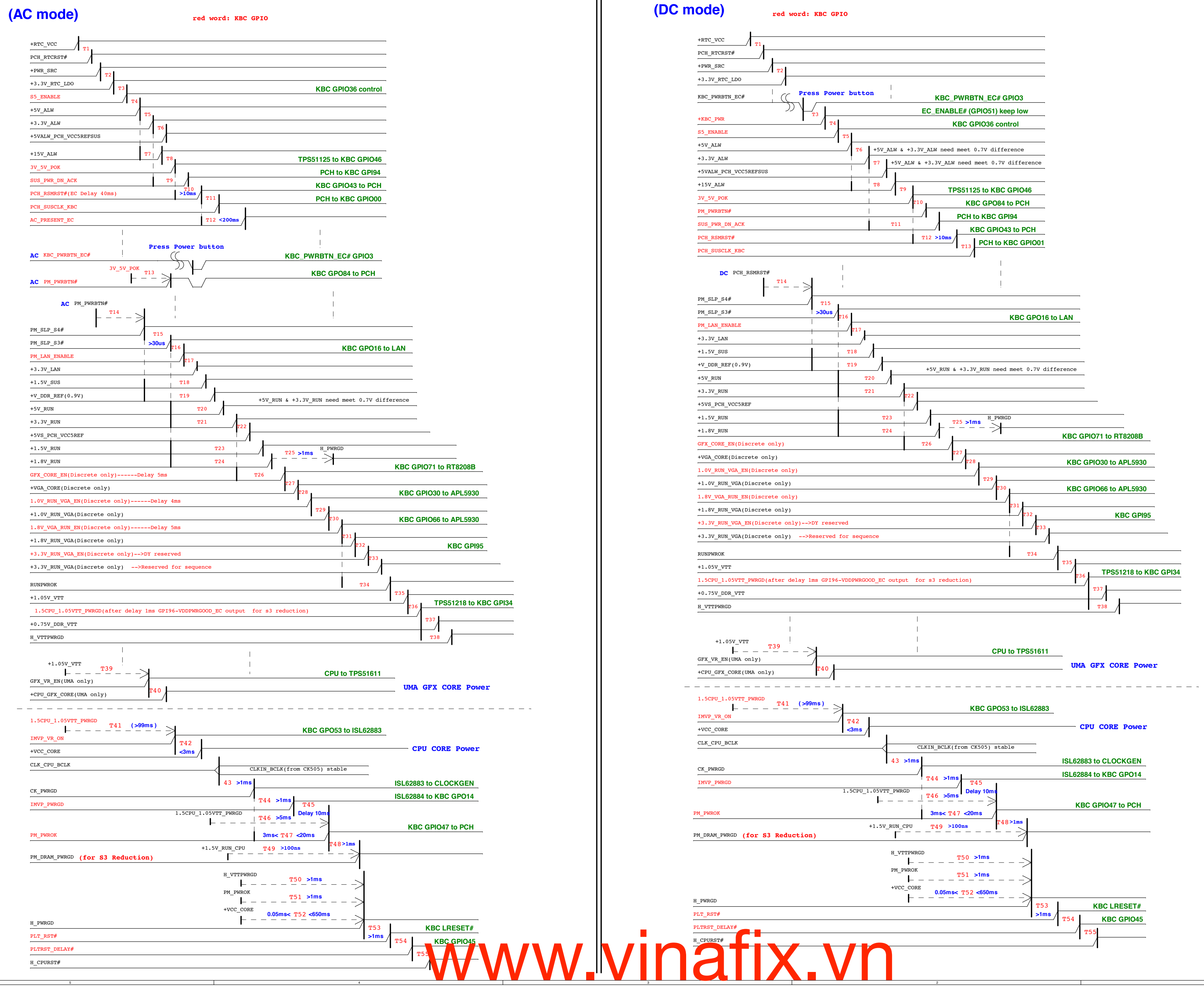
Intel-Power Up Sequence

Not Update



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Title: Power Sequence

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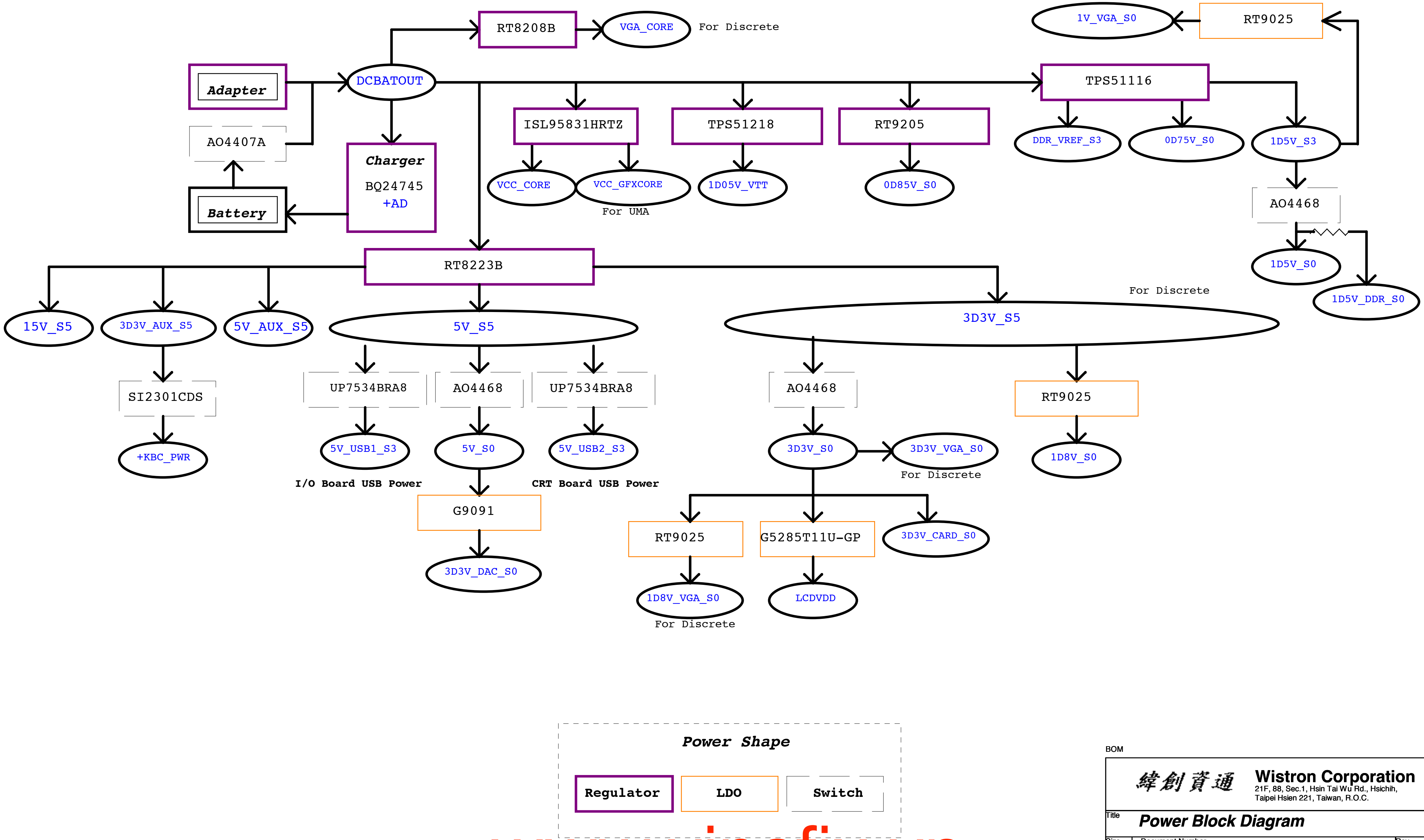
Not Update



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Title	**Power Block Diagram**	
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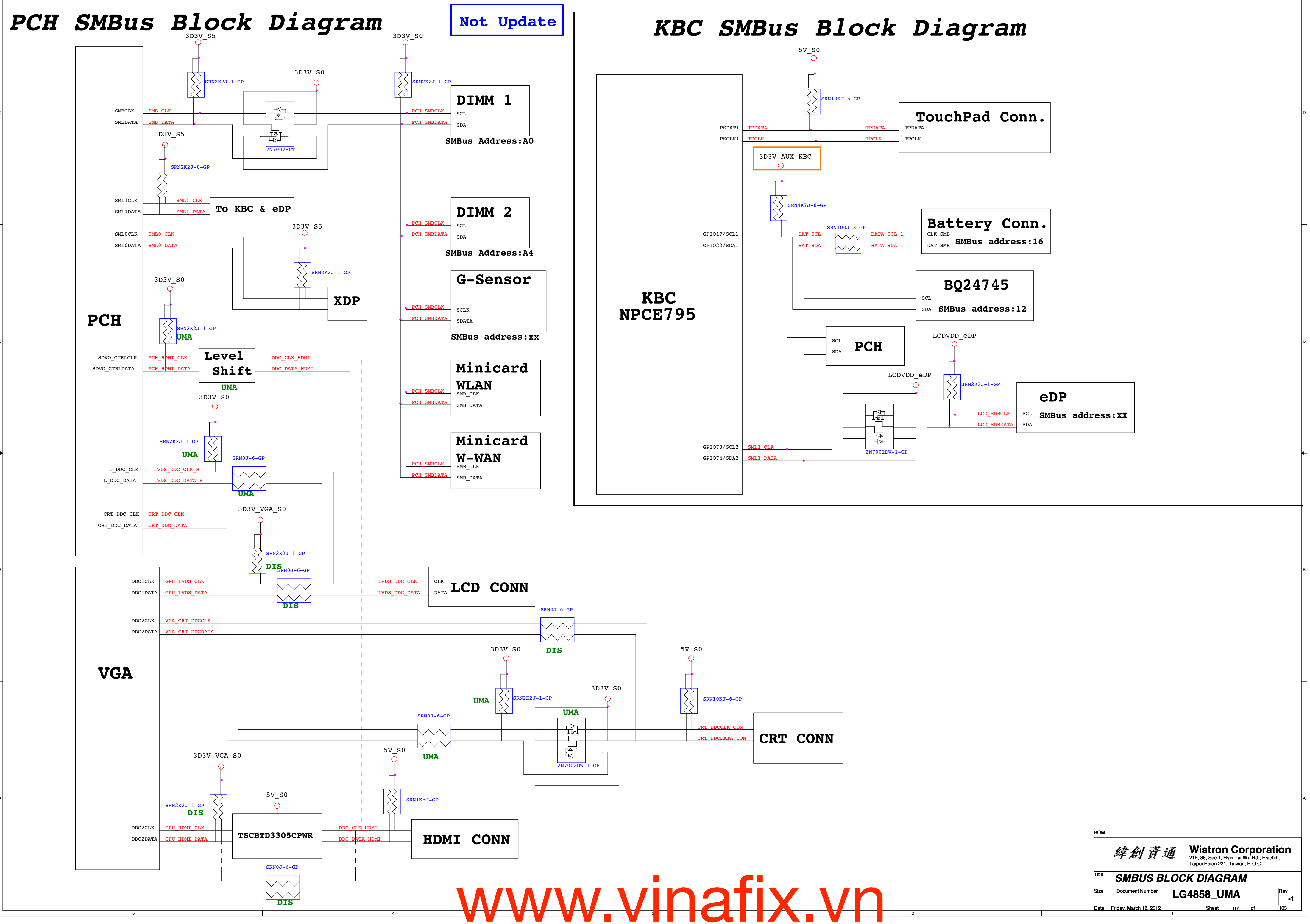

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Title: SMBUS BLOCK DIAGRAM

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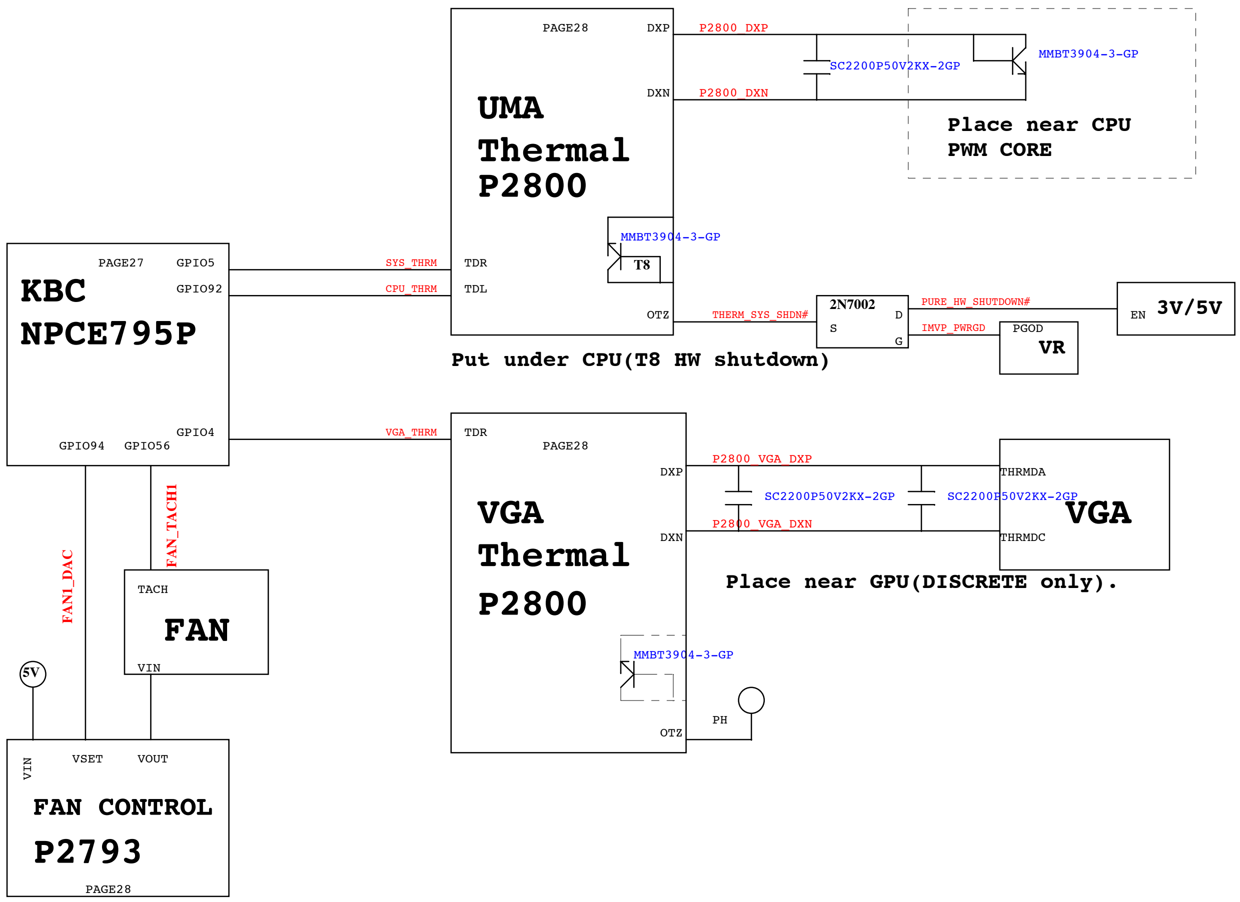
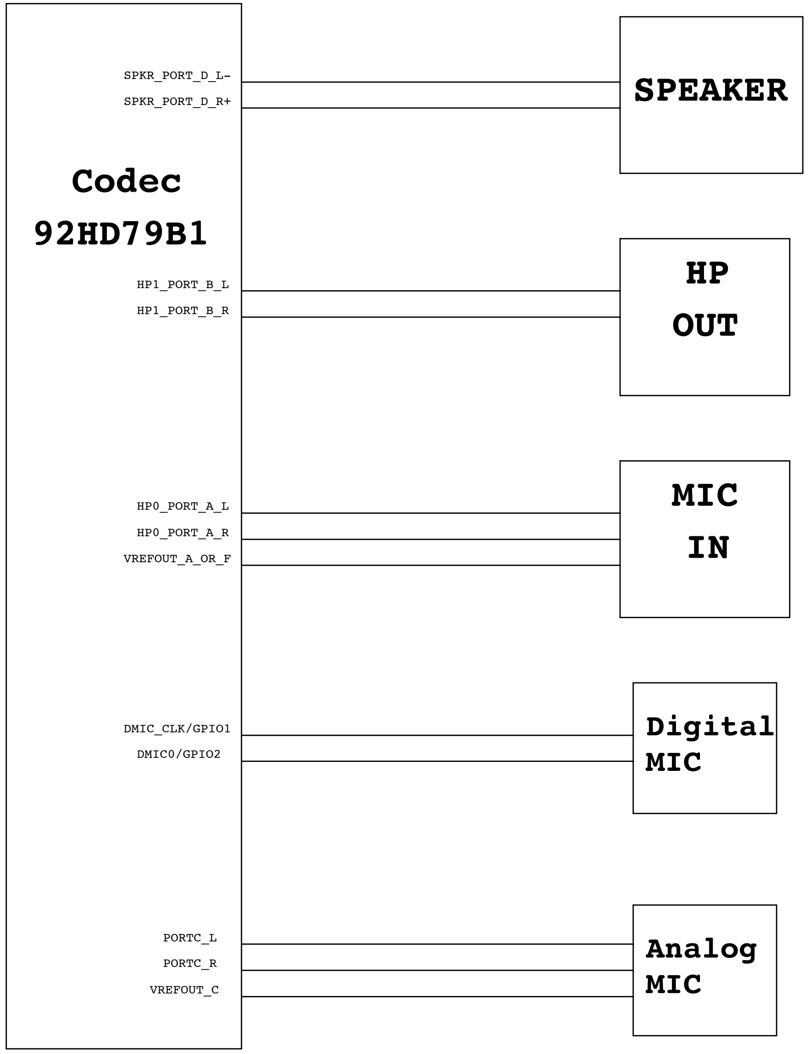
Thermal Block Diagram

Not Update



Audio Block Diagram



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